Online Equivalent Series Resistance Estimation Method for Condition Monitoring of DC-Link Capacitors

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***Abstract*— In this paper, a cost-effective and reliable equivalent series resistance (ESR) estimation method for aluminium electrolytic capacitors used as DC-link capacitors in front-end rectifier fed inverters is proposed. The proposed method is based on the extraction of switching frequency components of DC-link voltage and current using band-pass filters. A limiting value of switching frequency is identified, below which a new solution is proposed to achieve higher accuracy compared to the similar methods using band-pass filters. The proposed method is verified by both simulation and experimental results and it is shown that the estimation error is very low so that this method can be used for condition monitoring of DC-link capacitors.**

Keywords*— *ESR estimation; band-pass filters; electrolytic capacitors; front-end rectifier fed inverters

I. INTRODUCTION

Aluminium electrolytic capacitors are widely used as DC-link capacitors in power electronic converters because of their advantages such as high capacitance, high volumetric efficiency, and low cost. Unfortunately, aluminium electrolytic capacitors are also reported as the most failure prone component in a power electronic system [1]−[3]. Therefore, condition monitoring of aluminium electrolytic capacitor becomes inevitable in critical applications. The equivalent circuit of an aluminium electrolytic capacitor is explained in [4]. The equivalent circuit of a practical capacitor has all its loss components modelled as equivalent series resistance (ESR). The most common methods to monitor electrolytic capacitors involves the estimation of parameters such as the capacitance and ESR. The parameter estimation methods can be broadly categorized into online and offline methods. Offline methods require the capacitor to be disconnected from the system to measure the parameters using a LCR meter or other simple measurement techniques. Several offline parameter estimation methods are proposed in [5]−[7]. The need to disconnect the capacitor makes the offline methods inconvenient for many applications. Online parameter estimation method to estimate the ripple voltage based on the adaptive filter modelling is proposed in [8]. This method requires only the input current of the system to predict the capacitor's life. Online ESR estimation method is proposed in [9]. This method is based on the calculation of power loss inside the capacitor. Since the ESR is the only source of power loss inside a capacitor, it can be estimated by calculating the power loss and RMS current flowing into the capacitor.

A cost-effective ESR and capacitance estimation method is proposed in [10]. This method uses band-pass filters to extract the low frequency and switching frequency components of the capacitor voltage and current, which are then converted into their RMS values to calculate the capacitive reactance and ESR. This method can be used to estimate the ESR only if the switching frequency is high enough to neglect the effect of capacitance. ESR and capacitance estimation method for adjustable speed drives is proposed in [11]. This method estimates the ESR and capacitance using the inverter whenever the motor is stopped. Online ESR estimation method for high-power electric vehicle drive systems is proposed in [12]. The method proposed in [12] estimates the ESR using an ESR model and power loss. ESR estimation by manipulating the capacitor voltage and current components using digital filters is proposed in [13]. Another condition monitoring method for capacitors using the output voltage transient analysis is proposed in [14]. There are several methods proposed for parameter estimation in which only a few are cost-effective but those methods lag in accuracy. A new cost-effective method based on the concept used in [10] but with improved accuracy has been proposed in this paper.

II. ALUMINIUM ELECTROLYTIC CAPACITORS

A. Equivalent Circuit

The electrical equivalent circuit of a practical aluminium electrolytic capacitor is given in Fig. 1, where C is the nominal capacitance, R_P is the leakage resistance of the dielectric, R_S is the series resistance due to the terminals, tabs, and electrolyte. The ESL models the equivalent series inductance due to the loop formed by the terminals and tabs. The diode D1 models the overvoltage and reverse voltage behavior of the electrolytic capacitor. The total series resistance calculated by summing the series equivalent of R_P and the series resistance R_S is called the ESR, which represents all the loss components of a practical capacitor. The simplified equivalent circuit is shown in Fig. 2.

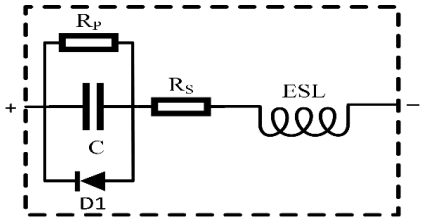

Fig. 1. Practical equivalent circuit of an aluminium electrolytic capacitor

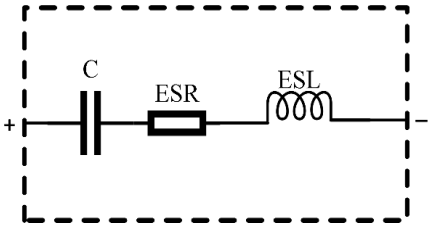

Fig. 2. Simplified equivalent circuit

B. Temperature and Frequency Dependence of ESR

Aluminium electrolytic capacitors are sensitive to both temperature and frequency. The ESR parameter of an electrolytic capacitor varies with the temperature and frequency variations, which makes it difficult to validate the estimated ESR in real operating conditions. The ESR decreases with an increase in temperature due to the increase in the carrier mobility of the electrolyte. It also decreases with an increase in frequency due to the dielectric polarization effects of the dielectric. So, while measuring the ESR, the effect of temperature and frequency should be considered to draw reliable conclusions about the health of the electrolytic capacitor.

III. PROPOSED METHOD

The circuit diagram of a front-end rectifier fed three-phase inverter is shown in Fig. 3. The simulation model of the front-end rectifier fed three-phase inverter has been simulated in PSpice. Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are the most popular modulation strategies used for three phase inverters. In this simulation model, SPWM is used to generate switching pulses and the switching frequency is 5 kHz.

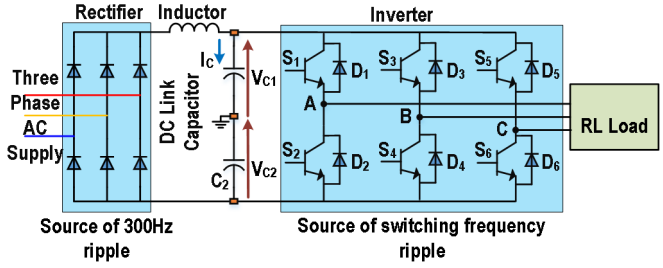

Fig. 3. Front-end rectifier fed three-phase inverter

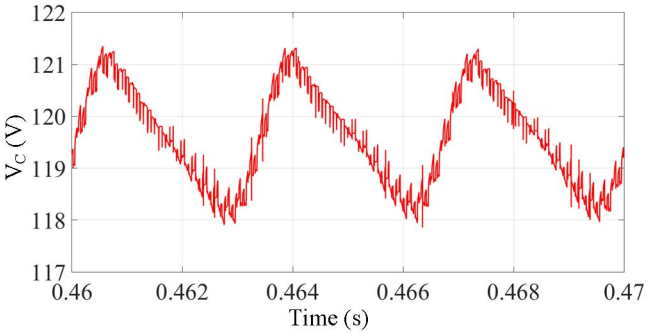

Fig. 4. Voltage across the DC-link capacitor

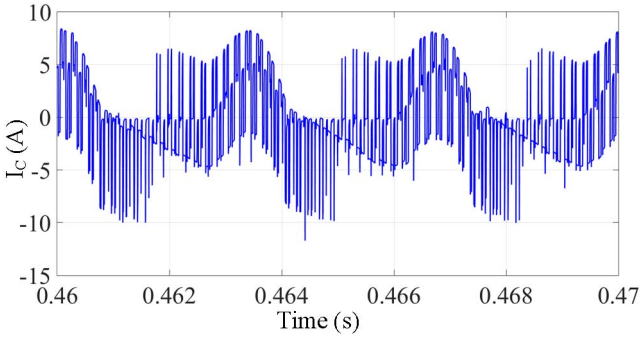

Fig. 5. Current through the DC-link capacitor

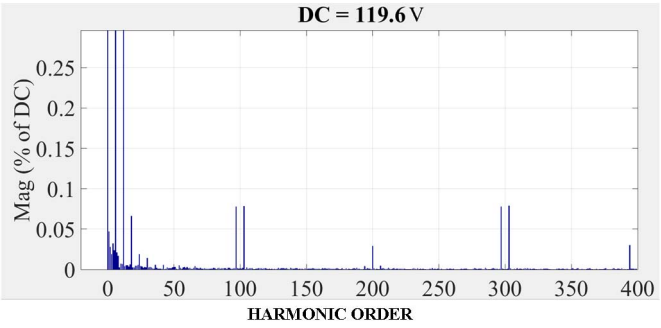

Fig. 6. FFT analysis of capacitor voltage

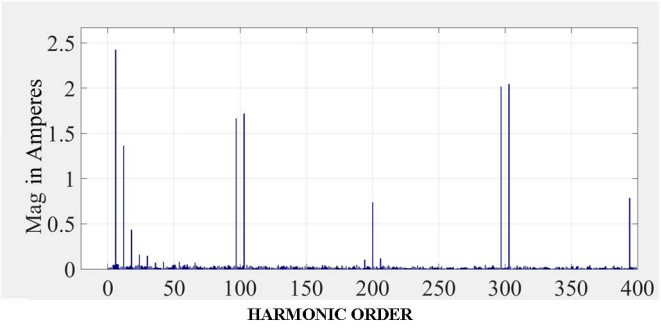

Fig. 7. FFT analysis of capacitor current

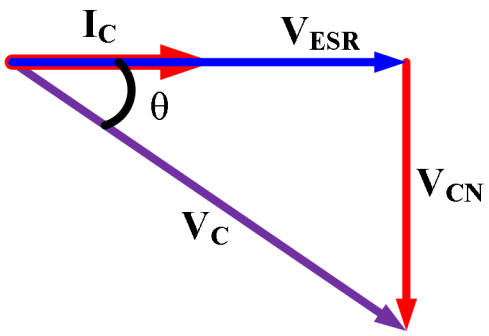

Fig. 8. Phasor diagram of the capacitor voltage

The voltage ripple across the DC-link capacitor is shown in Fig. 4. It can be easily deduced that the ripple voltage across the capacitor mainly has a low frequency 300 Hz component on which the higher frequency components generated by the switching action of the inverter are superimposed. The DC-link capacitor current in Fig. 5 also shows a similar pattern but here the high-frequency components due to the inverter's switching action dominates the low frequency 300 Hz component. To have a deeper understanding of different frequency components in capacitor voltage and current, the waveforms in Fig. 4 and Fig. 5 are analyzed using Fast Fourier Transform (FFT) analysis tool in MATLAB. The results are shown in Fig. 6 and Fig. 7, where 50 Hz is taken as the fundamental frequency and X-axis is harmonic order. The FFT analysis of the capacitor voltage and current shows that the dominant higher frequency harmonics are distributed mainly around the switching frequency and its multiples. From Fig. 6 and Fig. 7, the harmonics are distributed in pairs around the odd multiples of switching frequency whereas, at the even multiples of switching frequency, there is only one higher order harmonic. These harmonic components can be extracted accurately using an analog or digital band-pass filter (BPF) since the magnitude of other nearby frequency components are negligible.

For a frequency component of capacitor terminal voltage, the voltage across different elements in the equivalent circuit *C*, ESR and ESL can be expressed in phasor quantities as $V_{CN}\angle -90°$ or $-jV_{CN}$, $V_{ESR}\angle 0°$or V_{ESR} and $V_{ESL}\angle 90°$or jV_{ESL} respectively. The phasor diagram of the same is shown in Fig. 8. The terminal voltage of capacitor V_c is expressed in (1).

$$V_C = V_{ESR} - jV_{CN} + jV_{ESL} \tag{1}$$

Since the value of ESL is very low (in nH), V_{ESL}can be neglected for terminal voltages in the switching frequency range, where the voltage across ESL is very low compared to the voltage across *C*. The exact value of the frequency up to which the V_{ESL} component can be neglected depends on the value of *C*. Even if the ESL is large, it will not affect the ESR estimation as the ESL will affect only the quadrature component of the capacitor terminal voltage. Assuming the ESL is very less compared to *C*, V_C can be expressed as,

$$V_C = V_{ESR} - jV_{CN} \tag{2}$$

$$V_{ESR} = I_C \times ESR \tag{3}$$

$$V_{CN} = I_C \times -jX_C \tag{4}$$

The capacitive reactance $\left(X_c = \frac{1}{2\pi fC}\right)$ is dominant in the low frequency region and it decreases with the increase in frequency. Therefore, at switching frequency, the value of capacitive reactance is less. The switching frequency component of the terminal voltage of the capacitor can be expressed as,

$$V_{C\_fSW} = I_{C\_fSW} \times \sqrt{{ESR_{fSW}}^2 + \left(\frac{1}{2\pi f_{SW} C}\right)^2} \tag{5}$$

where f_{SW} represents switching frequency and subscript 'fsw' means those components are measured at switching frequency.

As discussed in section II. B, the ESR changes with frequency and hence the ESR is represented as ESR_{fSW} meaning ESR at switching frequency. If the value of the product $f_{SW} \times C$ is sufficiently large, the value of capacitive reactance will be very small compared to ESR and it can be neglected. Therefore, the impedance across capacitor terminals can be assumed almost equal to ESR as shown in (6).

$$\sqrt{{ESR_{fSW}}^2 + {X_{C\_fSW}}^2} \cong ESR_{fSW} \tag{6}$$

From (5) and (6), ESR can be expressed as,

$$ESR_{fSW} = \frac{V_{C\_fSW}}{I_{C\_fSW}} = \frac{V_{C\_fSW\_PEAK}}{I_{C\_fSW\_PEAK}} \tag{7}$$

where $V_{C\_fSW\_PEAK}$ and $I_{C\_fSW\_PEAK}$ are the peak values of switching frequency components of the capacitor voltage and capacitor current respectively. Since the switching frequency components are sinusoidal quantities, the peak value of those components can be used to estimate the ESR. The use of peak values for ESR estimation makes it easier to extract peak values using simple peak detector circuits to estimate the ESR using ADCs in low-cost microcontrollers as the bandwidth requirement is very less, thus reducing the overall cost of the system. (7) can be used to estimate the ESR only when the capacitive reactance X_c is very small compared to the ESR. If that condition fails, the presence of appreciable capacitive reactance will induce error in the ESR estimation. To achieve an estimation error of less than 5%, the relation between $f \times C$ product and ESR can be derived. Theoretically, the estimation error less than 5% can be achieved only if the condition (8) holds true.

$$\sqrt{ESR^2 + {X_C}^2} < 1.05 \times ESR \tag{8}$$

$$ESR^2 + \left(\frac{1}{2\pi fC}\right)^2 < 1.1025 \times ESR^2 \tag{9}$$

$$\frac{1}{fC} < 2.0116 \times ESR \tag{10}$$

$$f > \frac{1}{2.0116 \times ESR \times C} \tag{11}$$

Therefore, (7) can be used only if condition (11) is satisfied. If (11) fails, there are two solutions, which are discussed as follows.

Solution 1: The FFT analysis of the capacitor voltage and current in Fig. 6 and Fig. 7 shows that the harmonics around $3 \times f_{SW}$ or 15 kHz (harmonic order 300) have significant magnitude, which can also be used to estimate ESR. The use of harmonics at $2 \times f_{SW}$ and $4 \times f_{SW}$ are avoided here only because of the less magnitude and can be used in cases where they are sufficiently high. The magnitude of harmonics beyond the order 400 is very less. In summary, if (11) fails for f_{SW}, the harmonics around $3 \times f_{SW}$ can be used to estimate ESR_{3fSW} using (12), provided $f = 3 \times f_{SW}$ satisfies (11).

$$ESR_{3fSW} = \frac{V_{C\_3fSW}}{I_{C\_3fSW}} = \frac{V_{C\_3fSW\_PEAK}}{I_{C\_3fSW\_PEAK}} \qquad (12)$$

Solution 2: The reason for the decrease in accuracy if (11) fails is that the frequency is not high enough to neglect the capacitive reactance voltage drop. To improve the accuracy, the ESR voltage drop V_R must be extracted from the capacitor terminal voltage V_C. From Fig. 8, the capacitor current I_C can be used to measure the phase difference between capacitor terminal voltage V_C and ESR voltage drop V_R. Once the phase difference is known, V_R can be extracted. From Fig. 8, if θ is the angle between V_{ESR} and V_C, then the following equation can be written using the Pythagorean trigonometric identity.

$$\cos\theta = \frac{V_{ESR}}{V_C} \qquad (13)$$

If θ and V_C are known, V_{ESR} can be estimated. Since the capacitor current and the current through the ESR are same, ESR can be estimated using (3). For a frequency component of frequency f,

$$ESR_f = \frac{V_{C\_f} \times \cos\theta_f}{I_{C\_f}} = \frac{V_{C\_fPEAK} \times \cos\theta_f}{I_{C\_fPEAK}} \qquad (14)$$

Since θ_f can be measured as the phase difference between the capacitor voltage and current, (14) can be used to estimate the ESR accurately when (11) fails. This method can be implemented using either analog filters or by performing digital filtering inside a DSP. In this paper, analog BPFs are used. When the analog BPF is used to filter out 5 kHz, the filter output will have the resultant of two frequency components (shown in FFT analysis) on either side of 5 kHz at 4850 Hz and 5150 Hz. The resultant component will reach its peak every 3.33 ms, corresponding to 300 Hz which is the difference between the frequencies of these two components. The peak value of the BPF can be extracted using peak detector circuits and the ESR can be estimated using (14). The proposed ESR estimation scheme is shown in Fig. 9.

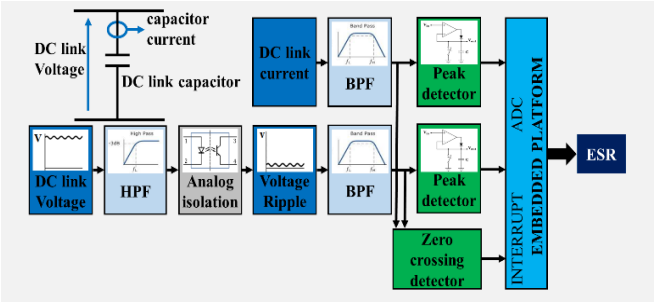

Fig. 9. Proposed ESR estimation scheme

IV. Simulation Results

The proposed ESR estimation scheme is simulated using PSpice circuit simulator for the front-end rectifier fed three-phase inverter circuit model shown in Fig. 3. The DC-link capacitor is modelled as a series RLC circuit of capacitance 1000 µF, ESL 5 nH, and ESR 45 mΩ. The switching frequency of the inverter is 5 kHz. The capacitor current and the ripple voltage extracted using high pass filter are then passed through band-pass filters to extract 5 kHz components. The Sallen-Key band-pass filter is designed using the steps explained in [15]. The outputs of band-pass filters are given in Fig. 10 and Fig. 11. The peak values of the extracted switching frequency components of capacitor voltage and current are indicated for each cycle in their respective figures. Now applying (11) for the switching frequency 5 kHz, capacitance 1000 µF, and ESR 45 mΩ, $\frac{1}{2.0116 \times ESR \times C} = 11047$. Therefore, $5000 < \frac{1}{2.0116 \times ESR \times C}$ and the condition (11) fails, solution 1 or 2 can be adopted. For estimating the ESR using the method described in solution 2, the phase difference between the capacitor voltage and current is necessary. The necessary waveform is shown in Fig. 12.

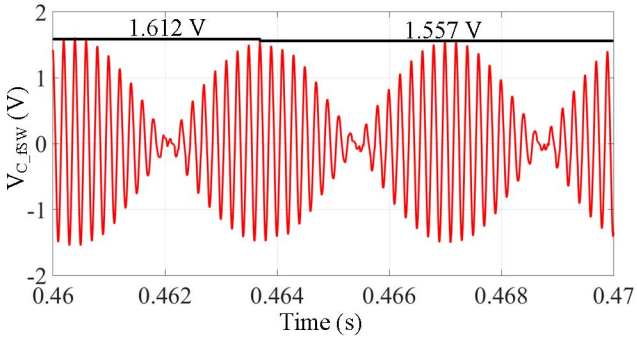

Fig. 10. BPF output – capacitor voltage

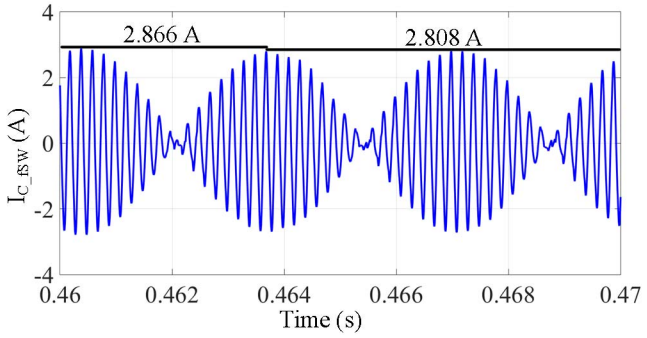

Fig. 11. BPF output – capacitor current

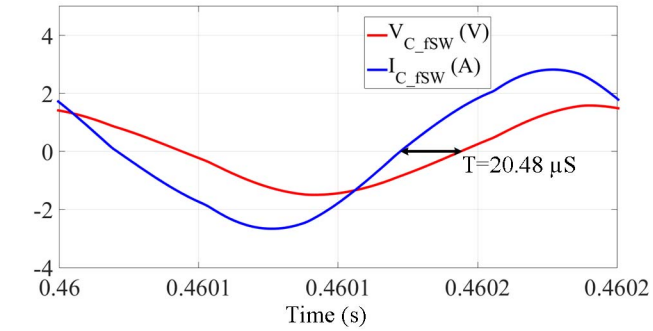

Fig. 12. Phase difference

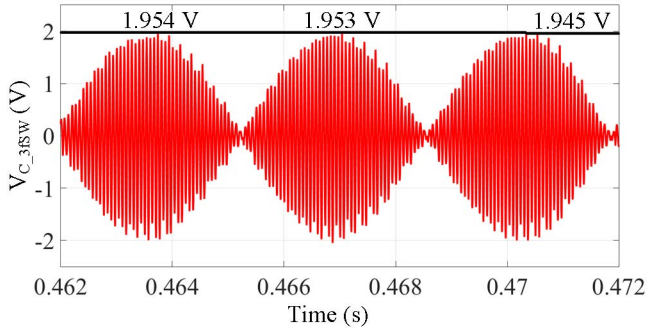

Fig. 13. BPF output – capacitor voltage (15 kHz)

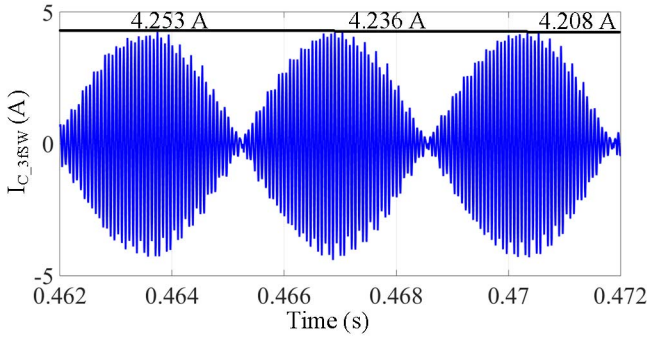

Fig. 14. BPF output – capacitor current (15 kHz)

From Fig. 12, the difference in time between the zero crossing of capacitor voltage and current is 20.48 µs, which corresponds to a phase difference $\theta_{5k} = 0.6434\,rad$. Using (14), the ESR can be estimated as follows.

$$ESR_{5k} = \frac{\left(\frac{1.612 + 1.557}{2}\right) \times 0.1 \times \cos 0.6434}{\left(\frac{2.866 + 2.808}{2}\right)} = 44.68\,m\Omega \quad (15)$$

Since the V_{c_5kPEAK} and I_{C_5kPEAK} have slight variations, their average over 10 ms period is used for calculating the ESR. The additional term 0.1 is used in formula to account for the scaling factors of voltage, current and the gain of BPF. In the simulation model, the DC-link voltage sensor model has zero gain for DC content and unity gain for AC content. The BPF has a gain of 10 for 5 kHz components. Hence, the total voltage scaling factor is 10 and the voltage should be multiplied by 0.1 to get the actual voltage. The current sensor model has a gain of 0.1 and the BPF has a gain of 10. Therefore, the current scaling factor is unity.

The actual value of the ESR is 45 mΩ and the error in estimation is less than 1% (0.32 mΩ or 0.7%). If the phase difference is not considered, the estimation using (7) would have given 55.85 mΩ, leading to an error of 24% which is not acceptable. The value of ESR can also be estimated using the method described in solution 1, if (11) holds for $3 \times f_{SW}$ (15 kHz). As $3 \times f_{SW}$ (15000) > 11047, solution 1 can be applied. The components around $3 \times f_{SW}$ extracted using band pass filters are given in Fig. 13 and Fig. 14. Since the peak value varies slightly, their average over 10 ms period is used. Using (12),

$$ESR_{15k} = \frac{\left(\frac{1.954 + 1.953 + 1.945}{3}\right) \times 0.1}{\left(\frac{4.253 + 4.236 + 4.208}{3}\right)} = 46.08m\Omega \quad (16)$$

The actual value of the ESR is 45 mΩ and the error in estimation is less than 5% (1.08 mΩ or 2.4%). In this simulation model, the variation of ESR with frequency and temperature are not considered.

V. Experimental Results

The proposed method has also been verified experimentally using a front-end rectifier fed three-phase inverter setup. The experimental setup is shown in Fig. 15. The switching frequency of the inverter is 2.5 kHz. The switching pulse generation and data acquisition are carried out using PE-Expert4 controller board from Myway. To verify the accuracy of this method, the experiment is repeated for four different capacitor samples. The details of the capacitors are given in Table. I.

TABLE I. DC-LINK CAPACITOR PARAMETERS

Sample No.	Manufacturer Part No.	Capacitance (2.5 kHz and 25 °C)	ESR (2.5 kHz and 25 °C)
C1	Cornell Dubilier 500R112M500BC2B	954.4 µF	46.4 mΩ
C2	Cornell Dubilier 500R112M500BC2B	963.7 µF	44.8 mΩ
C3	Kemet ALS30A102KF450	850.9 µF	39.5 mΩ
C4	Kemet ALS30A102KF450	845.6 µF	39.8 mΩ

The capacitors have embedded thermocouples to measure the core temperature. As the value of ESR varies with temperature, this core temperature can be used to validate the estimated ESR at different operating temperatures. In this experiment, the variation of ESR with temperature is measured using the LCR meter and modeled as a mathematical equation by using the curve fitting technique in MATLAB. The results are shown in Fig. 16.

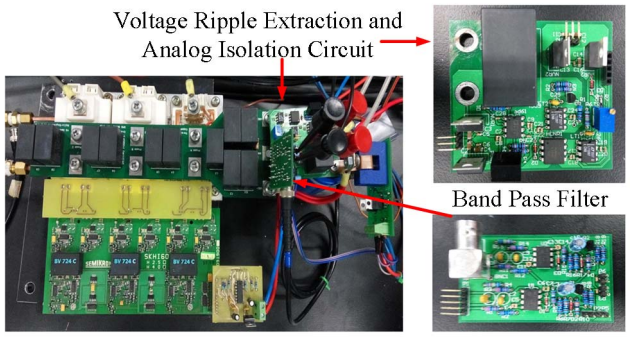

Fig. 15. Experimental setup

The thermal response of the ESR is modeled as shown in (17).

$$ESR(T) = \left(\alpha * e^{-\beta*(T-25)}\right) + \gamma \qquad (17)$$

where α = 0.03385, β = 0.06588, and γ = 0.01255 obtained by curve fitting are the constants for the capacitor used. The dotted lines in Fig. 16 shows the prediction bounds for 95% confidence interval.

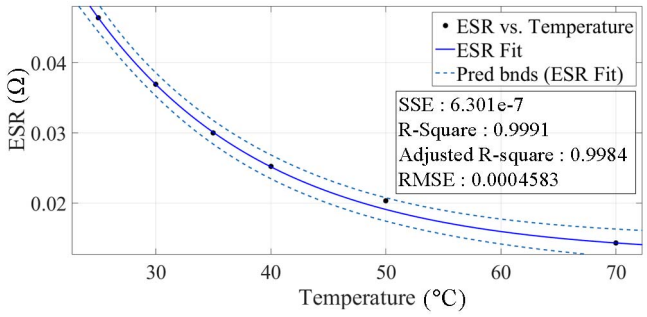

Fig. 16. Thermal response of the ESR

Once the operating temperature and thermal response of the ESR are known, the ESR estimated at any temperature can be compared with its actual value at the same temperature from the mathematical model (17). In this experiment, the mathematical model is used to validate the ESR estimation method whereas in condition monitoring applications, the ESR values from the mathematical model can be used as the initial value of ESR and the health of the capacitor is determined based on the deviation of estimated value from the initial value of ESR.

The ripple content of the DC-link voltage is extracted using the voltage ripple extraction and analog isolation circuit shown in Fig. 15. The circuit consists of a high-pass filter to filter the DC content followed by an analog isolation circuit using HCNR201. The output of the analog isolation circuit is connected to the Sallen-Key BPF to extract the switching frequency components of DC-link voltage. The DC-link capacitor current is measured using the commercial current sensor. The sensor output is filtered using Sallen-key BPF to extract the switching frequency components of capacitor current. The output of BPFs are then passed through the peak detector circuit and zero crossing detector to get their peak values and phase difference between them.

Even though the circuit is carefully designed, the intrinsic variations in the components and different scaling factors for voltage and current may introduce some offsets in the output. The following calibration procedure is adopted to calibrate the estimation circuit. Ideally, if the same signal is given to the voltage and current input of the estimation circuit, the ratio of peak detector outputs should be unity and the phase difference should be zero as shown in (18).

$$ESR_f = \frac{V_{C\_fPEAK}}{I_{C\_fPEAK}} \times \cos\theta_f = 1 \times \cos 0 = 1 \qquad (18)$$

The calibration procedure aims to satisfy (18) by introducing a gain factor and phase in the actual equation for ESR to account for the scaling factors and intrinsic variations. The new equation for estimating the ESR is shown in (19).

$$ESR_f = \frac{V_{C\_fPEAK} \times Gain \times \cos(\theta_f - \emptyset)}{I_{C\_fPEAK}} \qquad (19)$$

The voltage and current inputs of the estimation circuit are fed with the same 2.5 kHz signal from the signal generator. The input signal is varied over the entire range of the estimation circuit and the average gain value to make the ratio of V_{C_fPEAK} to I_{C_fPEAK} unity is calculated as 2.97. The current sensor used in the experiment has a scaling factor of 20. Therefore, the value of gain factor in (19) is calculated as 0.1485. The average value of phase difference $\emptyset$ is 0.04276 radians. The peak detector outputs for the input signal of 300mV is shown in Fig. 17 and the corresponding ZCD output for phase difference measurement is shown in Fig. 18. With these calibration values, the ESR can be estimated using (20).

$$ESR_f = \frac{V_{C\_fPEAK} \times 0.1485 \times \cos(\theta_f - 0.04276)}{I_{C\_fPEAK}} \quad (20)$$

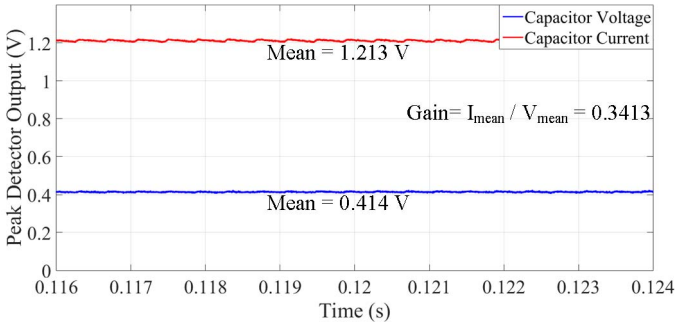

Fig. 17. Peak detector outputs for gain calibration

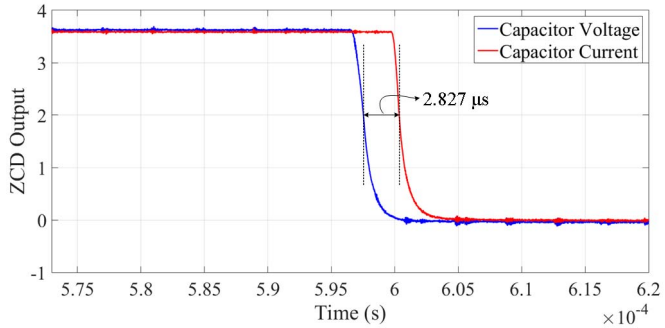

Fig. 17. ZCD outputs for phase calibration

After the calibration procedure, the experiment is carried out with C1 as the DC-link capacitor. The DC-link voltage is shown in Fig. 18. The BPF outputs for voltage and current are shown in Fig.19. The phase difference between them is shown in Fig. 20. The results shown here are for the operating temperature of 23.6 ℃ which is the room temperature before starting the experiment and the results are taken as soon as the inverter is turned on. It is also ensured by measuring the core temperature of the capacitor using thermocouple while taking the measurements. The experiment is repeated for the capacitor samples C2, C3, and C4. The comparison of the estimated ESR with actual ESR measured using the LCR meter is shown in Table II.

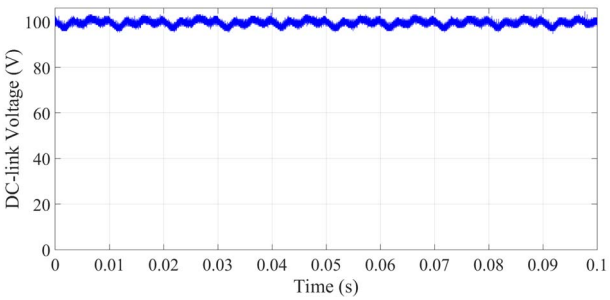

Fig. 18. DC-link voltage of the inverter

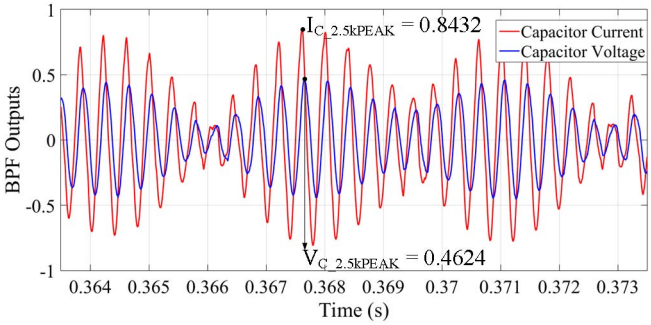

Fig. 19. BPF Outputs for the capacitor voltage and current

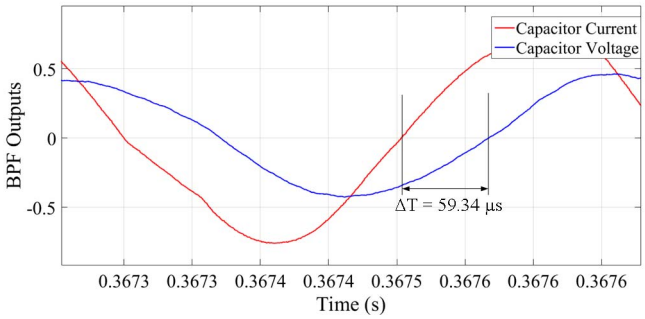

Fig. 20. Phase difference between the capacitor voltage and current

For the switching frequency of 2.5 kHz, θ can be calculated as shown in (21).

$$\theta = \frac{\Delta T}{2 \times 10^{-4}} \times \pi \; radians \quad (21)$$

where 2×10^{-4} is used as π radians correspond to 200 µs for 2.5 kHz.

From Fig. 20, θ can be calculated as,

$$\theta = \frac{0.5934 \times 10^{-4}}{2 \times 10^{-4}} \times \pi \; radians \quad (22)$$

$$= 0.9321 \; radians$$

For the experimental results shown in Fig. 19 and Fig. 20, the ESR of the capacitor C1 can be estimated using (20) as shown in (23)

$$ESR_{2.5k} = \frac{0.4624 \times 0.1485 \times \cos(0.8893)}{0.8432} \quad (23)$$

$$ESR_{2.5k} = 51.30 \; m\Omega$$

The actual value of ESR at 23.6 ℃ can be obtained from (17) as 49.67 mΩ. Therefore, the error in ESR estimation is 1.63 mΩ and the percentage error is 3.28%. This result is just for one cycle of BPF output shown in Fig. 19. In PE-Expert4, the results from every 50 cycles are averaged to achieve better accuracy. The summary of the ESR estimation results is shown in Table II. The value of the estimated ESR and corresponding core temperature for C1 are shown in Fig. 21.

TABLE II. ESTIMATION RESULTS SUMMARY

Sample No.	Actual ESR (2.5 kHz and 23.6 ºC)	Estimated ESR (2.5 kHz and 23.6 ºC)	Percentage Error
C1	49.67 mΩ	50.73 mΩ	2.13 %
C2	47.91 mΩ	49.54 mΩ	3.40 %
C3	42.48 mΩ	44.12 mΩ	3.86 %
C4	42.63 mΩ	44.21 mΩ	3.71 %

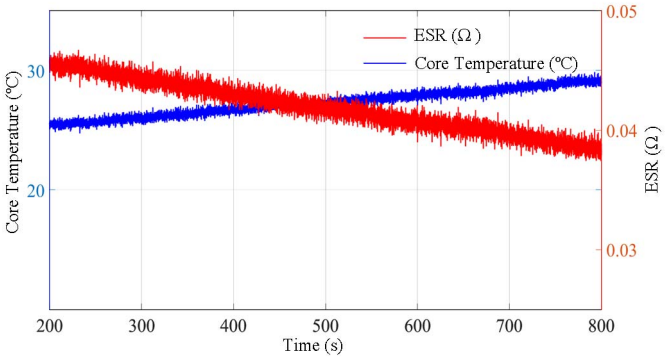

Fig. 21. Estimated ESR and core temperature

VI. CONCLUSION

A cost-effective ESR estimation method, which estimates the ESR with high accuracy, has been presented in this paper. The ESR estimation circuit requires only a few op-amps, passive elements, and a low-cost microcontroller to estimate the ESR. The proposed method has been validated by both simulation and experimental results. As the ESR is dependent on the operating temperature of capacitor, the thermal response of ESR is modeled using the curve fitting technique in MATLAB. Once the core temperature is known, the ESR estimated at any temperature can be compared to its initial value at the same temperature using the thermal response model of ESR to estimate the capacitor's health. In this paper, a thermocouple embedded in the capacitor's core is used to measure the core temperature. In the case of capacitors without thermocouple, the thermal model of capacitor is essential to estimate the core temperature.

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