Modeling, Fabrication and Characterization of 3D Capacitor Embedded in Through Silicon Via (TSV)

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***Abstract*—A new approach to implement integrated capacitors with superb capacitance density, called "three-dimensional (3D) embedded capacitor" is investigated. It is realized by embedding metal-insulator-metal (MIM) layers onto the trenches of through-silicon-vias (TSVs) prior to copper filling. An ultrahigh capacitance density of 5,621.8 nF/mm² was envisioned according to our model, which is ~13× of 440.0 nF/mm² from a conventional trench capacitor with the same design parameters. A set of prototypes were fabricated and characterized for assessment of structure integrity and electrical performance of the 3D embedded capacitors. Scanning electron microscope (SEM), transmission electron microscope (TEM) and energy-dispersive X-ray spectroscopy (EDX) analysis results show good step coverage and stoichiometry of the MIM layers deposited. The capacitance density of up to 3,856.4 nF/mm² was achieved for the prototypes with MIM layers formed by atomic layer deposition (ALD). A leakage current density as low as 1.61×10^{-7} A/cm² at 4.3V and a breakdown voltage greater than 9.5 V were measured for a sample with a capacitance density of 3,776.6 nF/mm².**

***Index Terms*— capacitance density, integrated capacitors, metal-insulator-metal (MIM), through-silicon vias (TSVs), three-dimensional integrated circuits (3D ICs).**

I. Introduction

In recent years, there has been considerable interest in the integration of passive devices into chip packages. It reduces not only the form factor of the passive devices, but also their assembly cost [1], [2]. Among all integrated passive devices (IPDs), integrated capacitor is one of the most critical components due to its wide applications in integrated circuits and systems. For example, an integrated capacitor can be used to improve the power integrity of integrated circuits (ICs) because of its charge storage capability [3], [4]. However, its significant consumption of premium silicon area is a major drawback of integrated capacitor [5]. This issue becomes more challenging, as we enter the era of three-dimensional integrated circuits (3D ICs) because more dies are being stacked within a single IC package and demand for capacitance increases [6], [7]. Therefore, large surface area will be used to realize the desired high capacitance.

Several approaches have been proposed to mitigate the area penalty by improving the capacitance density. On the one hand, many high-κ dielectric materials have been extensively studied

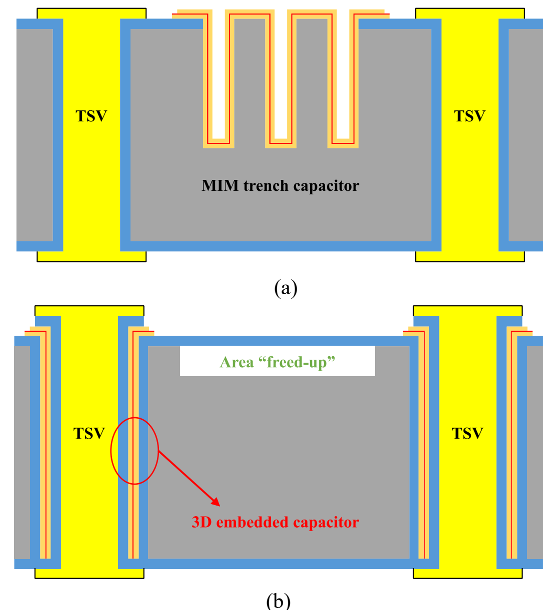

Fig. 1. (a) Conventional stand-alone MIM trench capacitors. (b) 3D embedded capacitors in TSVs. The top surface area is thus freed up.

to replace conventional SiO_2 [8]. Some extra efforts were put to optimize the trade-off between dielectric constant and bandgap for minimization of leakage current [9], [10]. On the other hand, the total surface area of capacitors can be expanded by utilizing the *Z* direction [11]–[13]. For example, trench capacitors make good use of the depth of substrate and achieve extremely high capacitance density [14], [15]. On top of that, 2.5D/3D heterogenous integration enables processing of capacitors in a separated die so that they do not have to compete with transistors for surface areas [16]–[19]. Nevertheless, with all available current technologies, the size of capacitors is still a few times greater than that of the logic circuits in many capacitance-hungry applications, e.g., integrated voltage regulators (IVRs) [20].

To further improve the capacitance density, we investigated a new method to implement integrated capacitors by embedding

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them into through-silicon-vias (TSVs) prior to copper filling. TSVs are electrical interconnects for vertical chip stacks in 3D ICs [21]. The trench of a TSV provides an ideal location to host an integrated trench capacitor due to their structural similarity. As the thicknesses of the capacitor layers are much thinner than the TSV diameter, negligible change in the TSV resistance is expected. The name "3D embedded capacitor" is given, because it utilizes the third dimension of the substrate and is embedded in the trench of TSV. Fig. 1 shows the difference between conventional stand-alone trench capacitors with TSVs and 3D embedded capacitors with TSVs. The top surface area in the middle of the substrate is freed up in Fig. 1(b), as the integrated capacitors are implemented in the trenches of TSVs.

This study reports on our progress so far towards the effectiveness and feasibility assessment of 3D embedded capacitors. Firstly, an analytical model was constructed to predict its ideal capacitance density. An ultrahigh capacitance density of 5,621.8 nF/mm^2 was envisioned according to our model, which is ~13× of 440.0 nF/mm^2 from a conventional trench capacitor with the same design parameters [15]. Then, prototypes were fabricated and characterized to examine their structure integrity and electrical performance. A capacitance density up to 3,856.4 nF/mm^2 was achieved for prototypes with MIM layers formed by atomic layer deposition (ALD). The leakage current density as low as 1.61×10^{-7} A/cm^2 at 4.3V and the breakdown voltage greater than 9.5 V were measured for a sample with capacitance density of 3,776.6 nF/mm^2. In addition, two electrode deposition methods, i.e. sputtering and atomic layer deposition (ALD), and two deep reactive ion etch (DRIE) recipes, i.e. Bosch and Pseudo-Bosch process, were adopted in the fabrication steps, respectively. Their effects on the electrical performance of 3D embedded capacitor were also studied. It is found that ALD is suitable for the pursuit of ultrahigh capacitance density due to its excellent step coverage, whereas sputtering provides moderate capacitance density as a potential candidate for low cost applications. Only the sputtering samples suffer from leakage current degradation, and the impact of two DRIE recipes is negligible.

In this paper, the analytical model of the proposed 3D embedded capacitor is shown in Fig. 2 in section II. The detailed fabrication process steps and the design of test vehicles are illustrated in section III. Both physical and electrical characterization results are presented and discussed in section IV. Lastly, a summary is given in section V.

II. Modeling

In this section, a first-order analytical model of 3D embedded capacitor is presented to predict the ideal capacitance density. Fig. 2 shows the top view of TSVs and 3D embedded capacitors with detailed layer breakdown. In Fig. 2(a), the most basic model is illustrated to show a TSV with an MIM 3D embedded capacitor, whereas in Fig. 2(b), an electrode layer and a dielectric layer are added to form a TSV with an MIMIM 3D embedded capacitor. In this way, more electrode and dielectric layers can be added alternatively to further enhance the capacitance.

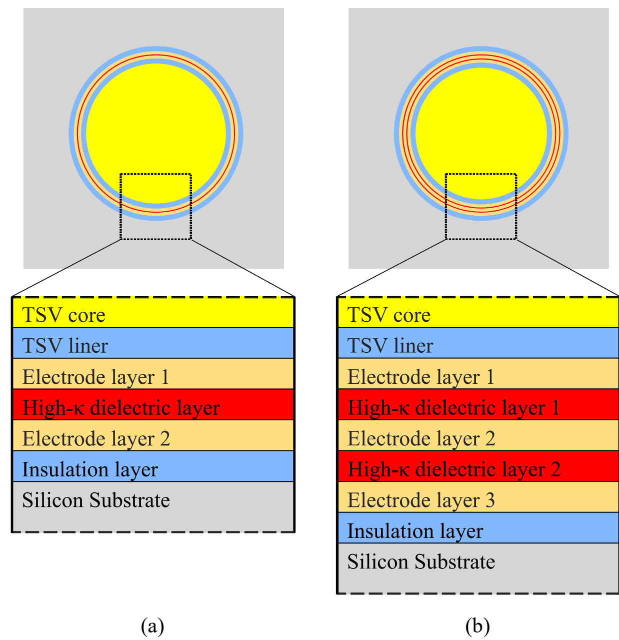


Fig. 2. Top view with layer breakdown of (a) TSV with an MIM 3D embedded capacitor and (b) TSV with a multilayer MIMIM 3D embedded capacitor.

In this study, an MIMIM structure shown in Fig. 2(b) is chosen for modeling, because one should be able to generalize this model to fit all other 3D embedded capacitors with more electrode and dielectric layers. The physical parameters of our model are defined respectively in Table I. The capacitance density is defined as the ratio of the capacitance to its effective planar surface area, where the capacitance is derived based on the coaxial capacitance model [22]. Therefore, the total cylindrical capacitance is:

$$\text{Capacitance} = C_{MIM1} + C_{MIM2} = \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{core} + T_{liner} + T_{el3} + T_{high-\kappa2}}{R_{core} + T_{liner} + T_{el3}}\right)} + \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{core} + T_{liner} + T_{el3} + T_{high-\kappa2} + T_{el2} + T_{high-\kappa1}}{R_{core} + T_{liner} + T_{el3} + T_{high-\kappa2} + T_{el2}}\right)} \quad (1)$$

The effective planar surface area occupied by these MIMIM layers is:

$$\text{Area} = \pi \times \left[(R_{core} + T_{liner} + T_{el3} + T_{high-\kappa2} + T_{el2} + T_{high-\kappa1} + T_{el1} + T_{ins})^2 - (R_{core} + T_{liner})^2\right] \quad (2)$$

Some design parameters were extracted from [15] so that a fair comparison can be made between the capacitance density of 3D embedded capacitors and that of conventional MIM trench capacitors. It is assumed that the thickness of a typical TSV liner is 200 nm, and the radius of a TSV core varies from 5 to 25 μm. The calculated results in Fig. 3 show that the capacitance density of 3D embedded capacitor can achieve up to 5,621.8 nF/mm^2, which is ~13× of 440.0 nF/mm^2 realized by multi-layer MIM trench capacitor [15]. In addition, Fig. 3 also

shows that the capacitance density increases from 5,619.7 to 5,622.8 nF/mm^2 as the radius of TSVs increases from 5 to 25 μm.

TABLE I
DESIGN PARAMETERS OF 3D EMBEDDED CAPACITOR

Name	Symbol	Value [15]
Capacitance of MIM structure1	C_{MIM1}	
Capacitance of MIM structure2	C_{MIM2}	
Thickness of insulation layer	T_{ins}	5nm
Thickness of electrode layer1	T_{el1}	20nm
Thickness of high-κ dielectric layer1	$T_{high-\kappa1}$	10nm
Thickness of electrode layer2	T_{el2}	20nm
Thickness of high-κ dielectric layer2	$T_{high-\kappa2}$	10nm
Thickness of electrode layer3	T_{el3}	20nm
Thickness of TSV liner	T_{liner}	200nm
Radius of TSV core	R_{core}	5~25μm
Depth of trench	H	30μm
High-κ dielectric constant	$\varepsilon_{high-\kappa}$	9

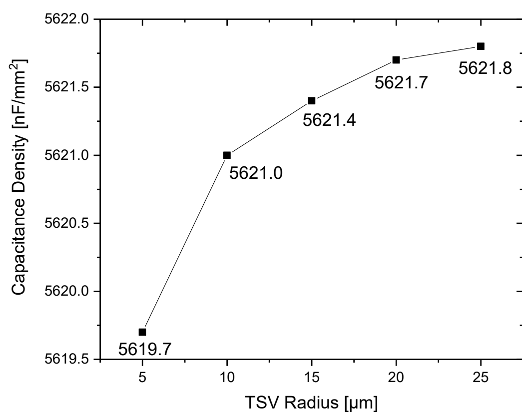


Fig. 3. Simulated capacitance density as a function of TSV radius.

III. EXPERIMENTAL

A. Process Flow

Detailed fabrication steps are illustrated in Fig. 4. A substrate is first patterned with photoresist (PR) and a trench is formed by deep reactive ion etching (DRIE) in steps (a)-(c). O_2 rapid thermal process (RTP) is applied to form a thin SiO_2 insulation layer in step (d). Then, TiN/Al_2O_3/TiN layers are deposited by ALD in steps (e)-(g). More electrode and dielectric layer can be added sequentially to complete a multi-layer MIM structure. The following conventional TSV process steps include plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 liner, sputtering of TiN as a diffusion barrier layer, sputtering of Cu seed layer, and electroplating of Cu TSV core in steps (h)-(j). Then, top surface is planarized by chemical-mechanical polishing (CMP) and patterned by PR again in steps (k)-(l). After that, an etching step is used to remove SiO_2/TiN/Al_2O_3 layers sequentially to define the size of the top electrode in step (m). Lastly, back-grinding and CMP are applied to thin down the substrate and expose the bottom of TSV for backside processing in step (n). Due to our limited fabrication capability, 3D embedded capacitor was built and characterized without the filled Cu core in this work.

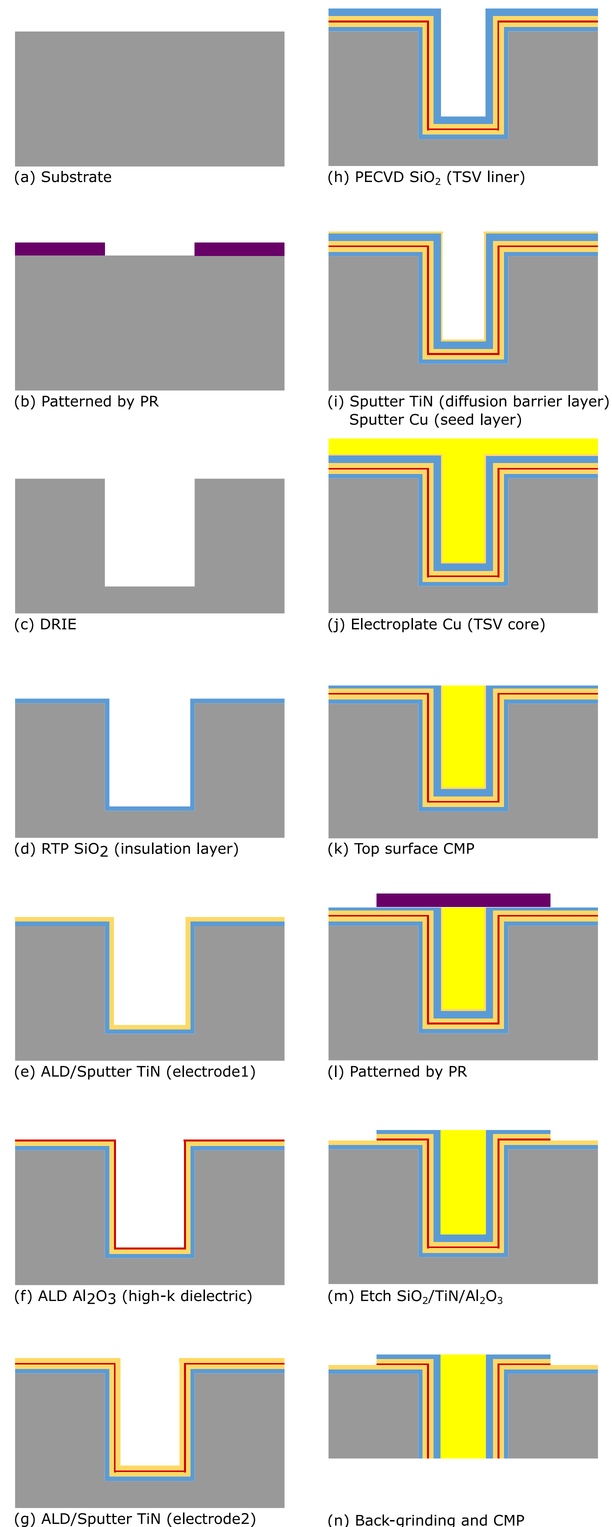


Fig. 4. Process flow of 3D embedded capacitor and TSV.

The choice of electrode deposition process in steps (e) and (g) is worth further discussion. For trench capacitor, ALD process is used due to its superb step coverage. However, for 3D embedded capacitor, the aspect ratio of a TSV trench generally is much smaller than that of a trench capacitor (e.g., 5 vs. 20). This makes sputtering process a possible candidate

for electrode deposition as well. The advantages of sputtering TiN over ALD TiN lie in higher deposition rate and easier integration for chip stacking. Fig. 5 shows that after back-grinding, insulation process will be required to isolate the ALD deposited electrodes at the bottom; whereas insulation process might not be necessary for sputtered electrodes since they are not exposed at the bottom because of non-ideal step coverage. Therefore, two electrode deposition options are explored for 3D embedded capacitor in section IV.

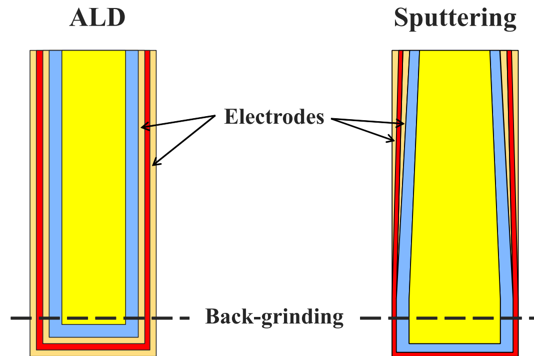


Fig. 5. Effect of back-grinding on bottom electrodes of 3D embedded capacitors. Insulation process is not necessary for sputtered electrodes.

B. Test Vehicles

Test vehicles were created for the assessment of structural integrity and electrical performance of 3D embedded capacitors. A pair of test vehicles, including a de-embedded test vehicle (one planar MIM capacitor) and an embedded test vehicle (one planar MIM capacitor with a 3×3 array of 3D embedded capacitors), are as shown in Fig. 6(a). Fig. 6(b) shows 5 different geometries of test vehicles chosen for a parametric study of the top electrode area, and their values are listed in Table II.

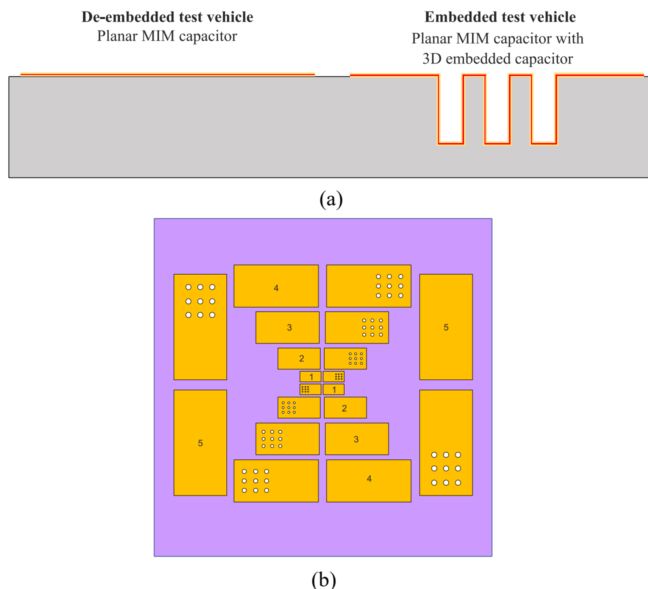


Fig. 6. Design of test vehicles for 3D embedded capacitors. (a) Cross-sectional view of a de-embedded test vehicle and an embedded test vehicle. (b) Top view of test vehicles with 5 scalable geometries.

TABLE II
PARAMETERS OF THE TEST VEHICLES

	Area of top electrode [μm²]	Diameter [μm]	Depth [μm]
1	100 × 200	10	
2	200 × 400	20	
3	300 × 600	30	60
4	400 × 800	40	
5	500 × 1000	50	

Two different DRIE recipes were explored in the fabrication process. The aim is to investigate the effect of trench sidewall roughness on the electrical performance of 3D embedded capacitors. Bosch DRIE process generates rough sidewalls, whereas pseudo-Bosch DRIE process results in smooth sidewalls but at a lower etch rate. This is due to the fact that both etching and passivation gases are simultaneously injected into the chamber in a pseudo-Bosch process, in contrast to alternative switching steps in a Bosch process. In addition to different DRIE recipes, two different electrode deposition methods, i.e. ALD and sputtering, were also applied to trenches with rough and smooth sidewalls, respectively. Due to limited step coverage of sputtering process, the thickness of sputtered TiN electrodes is set much thicker than that of ALD TiN electrodes (i.e., 400 vs. 50 nm). To ensure the uniform deposition of dielectric layer on rough sputtered electrodes, the thickness of Al_2O_3 in sputtering samples is also set thicker than that in ALD samples (i.e., 30 vs. 10 nm). In summary, ALD samples are with 50 nm TiN/10 nm Al_2O_3/50 nm TiN deposited all by ALD; sputtering samples are with 400 nm TiN/30 nm Al_2O_3/400 nm TiN deposited by sputtering/ALD/sputtering.

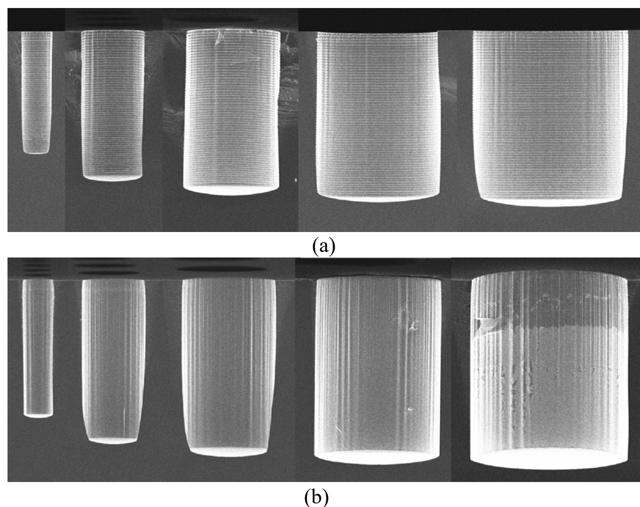
Consequently, in total four types of 3D embedded capacitors were fabricated for characterization, namely: (1) rough-ALD, (2) smooth-ALD, (3) rough-sputtering, and (4) smooth-sputtering. There are 5 scalable geometric sizes for each type of 3D capacitor.

IV. RESULTS AND DISCUSSION

A. Physical Characterization

1) Trench

Firstly, the trenches etched using the two different recipes were examined under scanning electron microscope (SEM). Fig. 7(a) reveals 290 nm of lateral scallops for trenches etched with Bosch process, but only less than 30 nm of lateral scallops for trenches in Fig. 7(b) etched with pseudo-Bosch process. Their diameters and depths have been measured and tabulated in Table III to provide geometrical parameters for the simulation of capacitance based on our model established in section II. Although a 60 μm target depth was set for all test vehicles, trenches with smaller openings tend to be shallower due to micro-loading effect. However, the depth variation will eventually be eliminated during TSV process because a back-grinding step is required for the exposure of all blind TSV vias. In addition, some vertical striations can also be observed on the sidewalls of the trenches, which are due to the wrinkling of the photoresists as shown in Fig. 8.



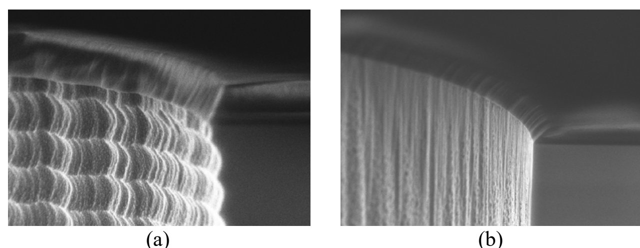
(a)

(b)

Fig. 7. The trenches etched by two different DRIE recipes. (a) Bosch process. (b) Pseudo-Bosch process.

TABLE III
MEASUREMENT RESULTS OF TRENCH GEOMETRIES

	Bosch (rough)		Pseudo-Bosch (smooth)	
	Diameter [μm]	Depth [μm]	Diameter [μm]	Depth [μm]
1	9.6	38.9	9.3	43.1
2	19.7	46.0	19.5	51.3
3	29.7	50.4	29.6	54.5
4	39.6	52.1	40.1	57.1
5	49.5	54.4	49.5	58.1



(a) (b)

Fig. 8. The wrinkling of photoresists on the surface of the trench with (a) Bosch process and (b) Pseudo-Bosch process.

2) 3D Embedded Capacitors with ALD Electrodes

Secondly, the structure integrity of MIM layers deposited by ALD was inspected under SEM. Top, middle, and bottom parts were zoomed-in for trenches with rough and smooth sidewalls, respectively, as exhibited in Fig. 9 and Fig. 10. The aspects ratio of these two trenches are 4.05 and 4.63, respectively. SEM images show excellent step coverage of $TiN/Al_2O_3/TiN$ layers for both types of trenches with a diameter of ~10 μm.

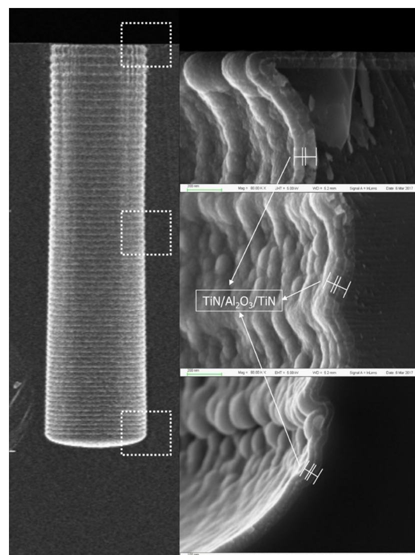


Fig. 9. ALD $TiN/Al_2O_3/TiN$ layers on rough sidewall.

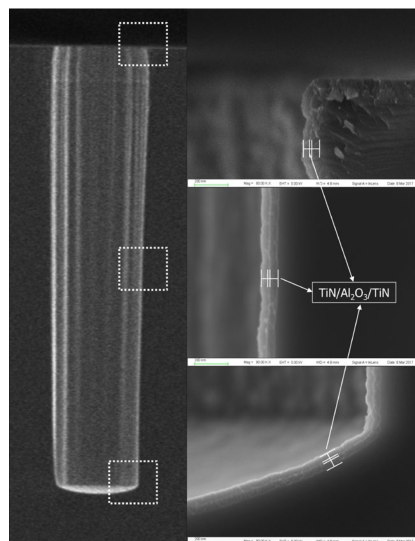


Fig. 10. ALD $TiN/Al_2O_3/TiN$ layers on smooth sidewall.

Then, a rough-ALD sample was sent for transmission electron microscope (TEM) analysis. The thickness of MIM layers was measured more precisely at higher magnification and chemical composition was determined by energy-dispersive X-ray spectroscopy (EDX). The thickness of $TiN/Al_2O_3/TiN$ was measured in Fig. 11 to be 46.9 nm/8.3 nm/51.5 nm on the top surface and 57 nm/10.8 nm/51.9 nm on the sidewall of the trench. At the top corner, it can be observed that a sharp tip is rounded by TiN bottom electrode layer. Therefore, Al_2O_3 layer demonstrates smooth and uniform coverage from lateral to vertical surfaces. The quality of this dielectric layer may be preserved even on a rough surface. An EDX line-scan was performed across MIM layers in the middle of the trench, as shown in Fig. 12(a). The result in Fig. 12(b) confirms good stoichiometry of TiN and Al_2O_3: at distance 40 to 90 nm and 100 to 150 nm, Ti and N are predominant, where the atomic percentage of Ti is slightly higher than that of N for both top and bottom TiN electrodes; at distance 90 to 100 nm, Al and O are predominant, where the atomic percentage of O is slightly higher than that of Al for the Al_2O_3 dielectric layer. Besides, at distance ~50 and ~150 nm, there are another two

peaks of O shown in the plot. The left peak suggests that some oxidation of TiN top electrode layer might happen after exposure to air, and the right one corresponds to O in the SiO_2 insulation layer.

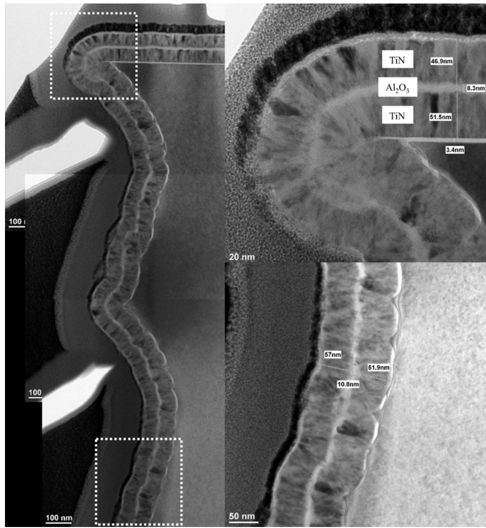
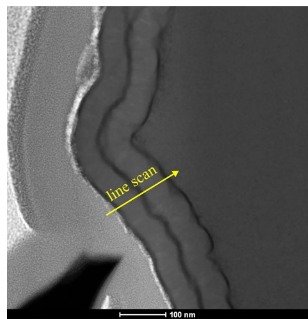
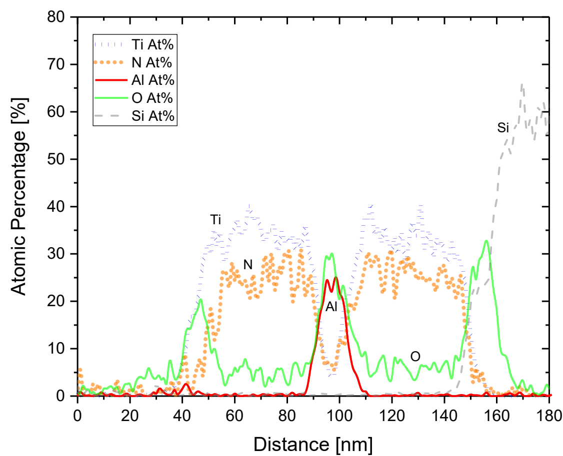


Fig. 11. Rough-ALD sample of 3D embedded capacitor under TEM.



(a)

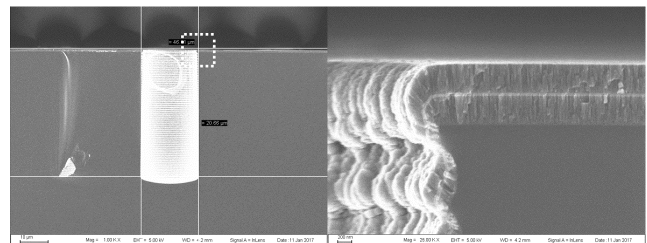


(b)

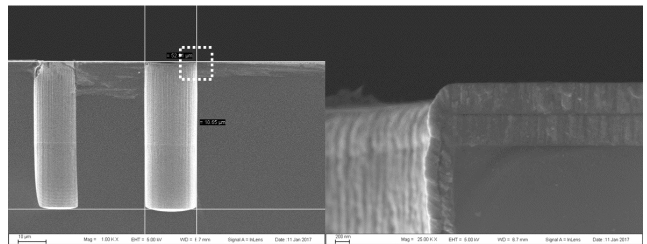
Fig. 12. EDX analysis of TiN/Al_2O_3/TiN layers on an ALD-rough sample. (a) Position of EDX line-scan. (b) Atomic percentage of elements alone the line-scan.

3) 3D Embedded Capacitors with Sputtered Electrodes

Lastly, the step coverage of MIM layers deposited by sputtering was investigated under SEM. Fig. 13(a) shows that the thickness of electrode layers is severely distorted due to the sidewall roughness, in contrast to the continuous coverage of the sputtered electrode layers on the smooth sidewall in Fig. 13(b). Thus, pseudo-Bosch process is highly favored over conventional Bosch process in the process of 3D embedded capacitors with sputtered electrodes. TiN layer was measured to be 400 nm thick on the lateral surface, however, only 200 nm was found even on the upper part of the smooth sidewall. It implies that in order to achieve target electrode thickness of 3D embedded capacitor, sputtering time has to be doubled. SEM images in Fig. 14 compares the electrode coverage, 30 µm below top surface, on smooth sidewalls of two trenches whose diameters are 10 and 40 µm, respectively. Their aspect ratios are 4.63 and 1.42, respectively. No TiN electrode layer can be observed in Fig. 14(a), but there is still two 46 nm thick electrode layers remaining at that depth in Fig. 14(b). This results in more effective MIM surface area for 3D embedded capacitors in trenches with low aspect ratio. Therefore, the impact of sputtering on the performance of 3D embedded capacitors is highly dependent on both sidewall roughness and trench aspect ratio. An EDX line-scan was also conducted on a rough-sputtering sample. The results in Fig. 15 confirm the correct stoichiometry of those MIM layers deposited by sputtering/ALD/sputtering processes sequentially, similar to the analysis mentioned above for Fig. 12(b).

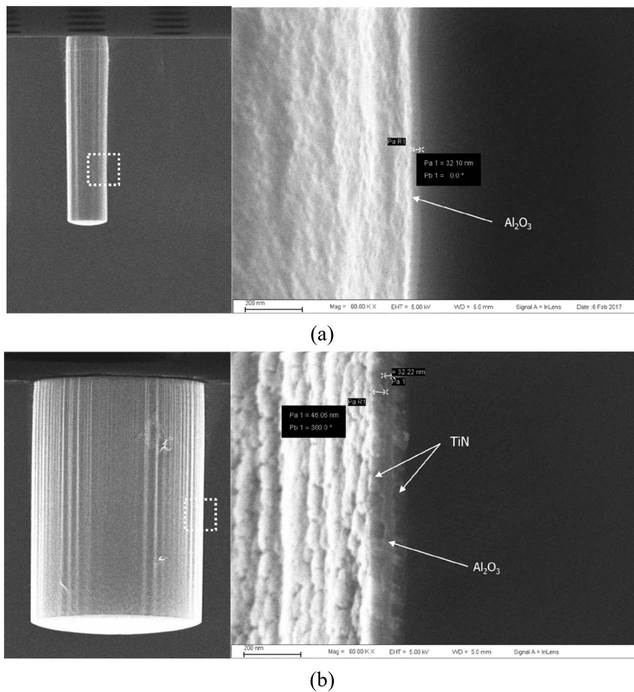


(a)



(b)

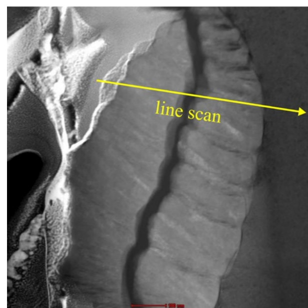
Fig. 13. TiN/Al_2O_3/TiN layers sputtered on (a) rough sidewall. (b) smooth sidewall.



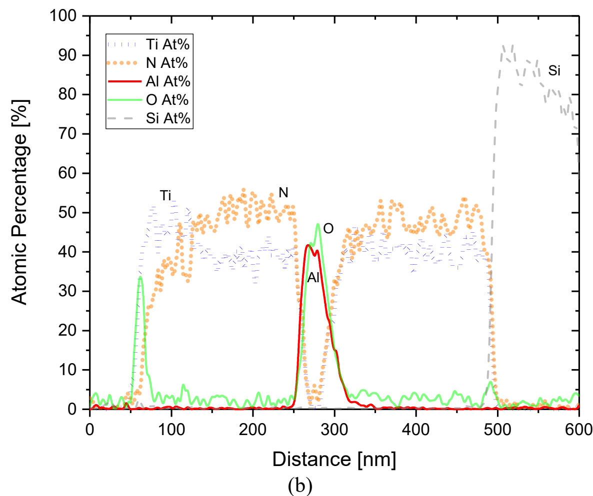
(a)

(b)

Fig. 14. Step coverage of sputtered electrodes in trenches with diameters of (a) 10 µm (b) 40 µm.



(a)



(b)

Fig. 15. EDX analysis of $TiN/Al_2O_3/TiN$ layers on a sputtering-rough sample. (a) Position of EDX line-scan. (b) Atomic percentage of elements alone the line-scan.

B. Electrical Characterization

1) Capacitance Density

In this study, the capacitance from both de-embedded and embedded test vehicles of all four types of samples has been characterized at 100 kHz without DC bias using Keithley 4200SCS. The measurement results are tabulated in

Table IV. The de-embedded test vehicles contain only planar capacitors as benchmarks. The embedded test vehicles contain the combination of planar capacitors and 3×3 arrays of 3D embedded capacitors. Therefore, the difference of capacitance extracted from a de-embedded and its corresponding embedded test vehicle is exactly the capacitance contributed by 9 units of 3D embedded capacitors.

The capacitance of planar capacitors in the de-embedded test vehicles increases by a factor of 1×, 4×, 9×, 16×, 25× for both ALD and sputtering samples, as the size of the top electrodes increases from 100 µm × 200 µm, 200 µm × 400 µm, 300 µm × 600 µm, 400 µm × 800 µm, to 500 µm × 1000 µm, respectively. Each capacitance of the embedded test vehicles is higher than that of their de-embedded counterparts due to extra contribution from the trench structures, as expected. Then the capacitance difference of the de-embedded and embedded test vehicles is compared with the simulation results based on the first-order model constructed in section II. For ALD samples, the measurement results are generally in close agreement with the simulation results with a difference less than 21% because ALD provides conformal layer coverage on the trenches. The measurement results of ALD-rough samples are slightly higher than the corresponding simulation results because the roughness of sidewalls increases the effective surface area along the sidewalls, which leads to higher capacitance. For sputtering samples, the simulation results are ~4× less than those of their respective ALD samples mainly due to 3× thicker dielectric layers and 8× thicker electrode layers. On top of that, the measurement results of sputtering samples are much lower than their simulation results with a difference up to 82% because of the poor step coverage of the sputtered electrodes. The deviation from the simulation results is particularly high for the sputtering-rough samples, as the bottom part of the trenches is not covered by MIM layers due to large sidewall scallops and aspect ratio. Nevertheless, the measurement results are approaching the simulation results rapidly for sputtering-smooth samples, as the diameter of the trenches increases from 10 to 50 µm. It suggests that the sputtered electrodes go deeper into the trenches as their aspect ratio decreases. Thus, sputtering process can be considered for electrode deposition of 3D embedded capacitors in trenches with smooth sidewalls and low aspect ratio.

Finally, the effective capacitance density of 3D embedded capacitors was calculated by finding the ratio of the capacitance difference and the planar surface area occupied by MIM layers.

Table IV shows an ultrahigh capacitance density, i.e. 3856.4 nF/mm^2, demonstrated by an ALD-smooth sample with 49.5 µm diameter and 58.1 µm depth trenches. A moderate capacitance density, up to 227.6 nF/mm^2, has also been demonstrated by 3D embedded capacitors with sputtered electrodes.

Thus, it can be concluded that the capacitance density is indeed boosted up significantly when MIM layers are

embedded in TSV trenches. Besides, ALD is proven as an excellent choice of electrode deposition method for high performance 3D embedded capacitors, whereas sputtering can be considered as a potential candidate for low cost, moderate performance applications.

TABLE IV
SUMMARY OF MEASURED AND SIMULATED CAPACITANCE CONTRIBUTED BY 3D EMBEDDED CAPACITORS AND THEIR EFFECTIVE CAPACITANCE DENSITY

ALD samples (50 nm TiN/10 nm Al_2O_3/50 nm TiN)

	Capacitance [pF]							Planar surface area occupied by MIM layers [mm^2]	Effective capacitance density [nF/mm^2]	
	De-embedded test vehicle	Embedded test vehicle		Difference						
				Trenches (rough)		Trenches (smooth)				
	Planar	Planar + trenches (rough)	Planar + trenches (smooth)	Measurement	Simulation	Measurement	Simulation		Trenches (rough)	Trenches (smooth)
1	160.7	267.6	259.4	106.9	84.1	98.7	90.2	3.24E-05	3327.6	3072.4
2	638.7	866.0	860.0	227.3	204.0	221.3	225.2	6.48E-05	3517.3	3424.4
3	1415.7	1782.5	1732.6	366.8	336.9	316.9	363.1	9.72E-05	3776.6	3262.9
4	2472.1	2954.8	2929.6	482.7	464.4	457.5	515.4	1.30E-04	3723.9	3529.5
5	3800.3	4412.8	4425.5	612.5	606.1	625.2	647.4	1.62E-04	3778.0	3856.4

Sputtering samples (400 nm TiN/30 nm Al_2O_3/400 nm TiN)

	Capacitance [pF]							Planar surface area occupied by MIM layers [mm^2]	Effective capacitance density [nF/mm^2]	
	De-embedded test vehicle	Embedded test vehicle		Difference						
				Trenches (rough)		Trenches (smooth)				
	Planar	Planar + trenches (rough)	Planar + trenches (smooth)	Measurement	Simulation	Measurement	Simulation		Trenches (rough)	Trenches (smooth)
1	43.9	47.5	52.1	3.6	19.8	8.2	21.3	1.18E-04	30.6	69.7
2	174.2	187.9	209.4	13.7	48.1	35.2	53.1	2.40E-04	57.0	146.4
3	390.7	416.8	460.8	26.1	79.4	70.1	85.6	3.64E-04	71.8	192.9
4	694.2	731.2	803.4	37.0	109.5	109.2	121.5	4.86E-04	76.1	224.5
5	1085.0	1178.5	1223.7	93.5	142.9	138.7	152.6	6.09E-04	153.5	227.6

2) Leakage Current Density and Breakdown Voltage

To assess leakage current and breakdown voltage of 3D embedded capacitors, current density–voltage (*J-V*) measurement was performed on all sets of test vehicles. Each set contains a de-embedded test vehicle, an embedded test vehicle with rough-sidewall trenches, and an embedded test vehicle with smooth-sidewall trenches. The aim was to investigate the impact of electrode deposition method and sidewall roughness on both leakage current density and breakdown voltage.

In this paper, the *J-V* characterization results of only one ALD set and one sputtering set, both with 300 µm × 600 µm top electrodes, are presented in Fig. 16, as the other sets with different electrode sizes produce similar results. In Fig. 16(a), the leakage current densities of three ALD test vehicles exhibit identical performance under bias voltage ranging from 0 to 15 V. All three curves rise quickly from 0 to 1.4 V, saturate at 1.33×10^{-7} A/cm^2 from 1.4 to 4.3 V, increase again from 4.3 V onwards, and eventually end at 9.5 V. It shows that the leakage current density and the breakdown voltage of 3D embedded capacitors by ALD are not degraded compared with planar MIM capacitors. In Fig. 16(b), much lower leakage current density and higher breakdown voltage were measured due to thicker dielectric layers of all sputtering test vehicles, though at the expense of lower capacitance density. At 8.5 V, the leakage current density is 1.04×10^{-9} A/cm^2 for the de-embedded test vehicle and it is 3.24×10^{-9} A/ cm^2 for the other two embedded test vehicles. Their breakdown voltages are all greater than 25.7 V. The two embedded test vehicles show almost identical leakage current density under all bias conditions, which is higher than that of their de-embedded counterpart. The higher leakage current density is suspected due to the rough surfaces of the electrodes on the sidewall deposited by sputtering.

In summary, no degradation is observed for ALD 3D embedded capacitors thanks to its superb step coverage of MIM layers. For sputtering samples, the degraded leakage current density of the two embedded test vehicles can be attributed to the rough surfaces induced by the sputtered electrodes, which cause non-uniform and higher electric fields in certain localized area of the dielectric layer. Trade-off can be made to achieve optimization of capacitance density, leakage current density, and breakdown voltage of 3D embedded capacitors for various applications.

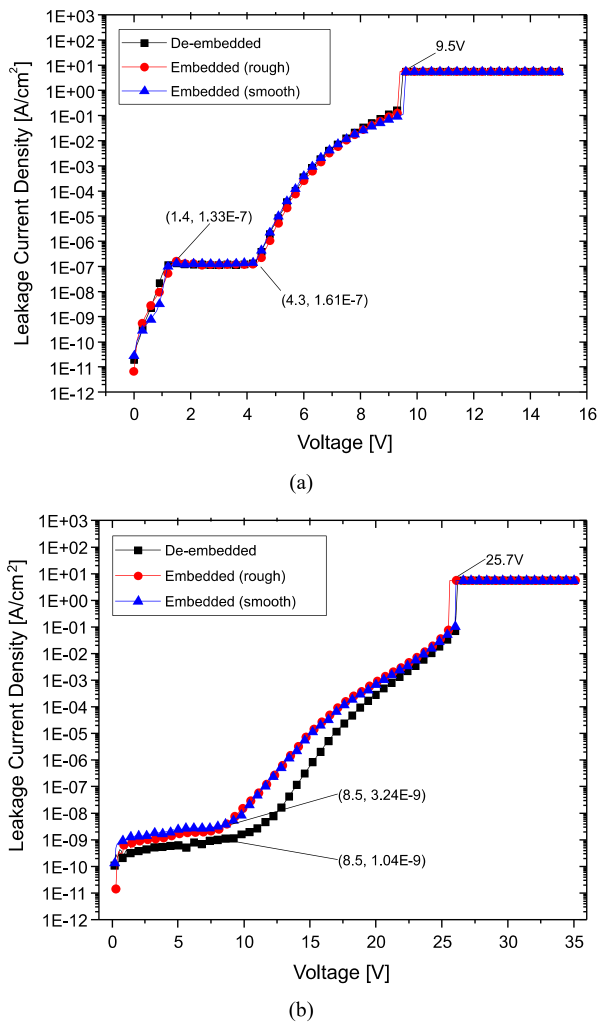


Fig. 16. *J-V* characterization results of (a) a set of ALD samples and (b) a set of sputtering samples.

V. Conclusion

To conclude, 3D embedded capacitors with design variations have been discussed comprehensively in this paper. A model has been constructed to predict the capacitance density successfully. As a benchmark, a capacitance density of 5621.8 nF/mm^2 was envisioned from a 3D embedded capacitor, equivalent to ~13× of 440.0 nF/mm^2 from a conventional trench capacitor with the same design parameters. Prototypes have been fabricated and characterized for structure integrity and electrical performance of 3D embedded capacitors. Excellent capacitance density, leakage current density, and breakdown voltage are demonstrated for samples with electrodes deposited by ALD and sputtering. It is found that ALD is suitable for the pursuit of ultrahigh capacitance density, whereas sputtering can be a potential candidate for low cost applications, which can also provide moderate capacitance density.

Thus, this work proves that integrated capacitors can be implemented without dedicated trenches to utilize the third dimension of the substrate. It is suggested that capacitors could be embedded in other vertical components, which share similar structures, e.g., TSVs. In this way, capacitance density is greatly boosted up and premium silicon surface area is freed up for active transistors.

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