Low-Capacitance Solid-State Transformer Control Using an Analytic Filter

Radhika Sarda*, Ezequiel Rodriguez†, Naga Brahmendra Gorla Yadav‡, Glen G. Farivar§, Josep Pou¶, V. B. Sriram†, and Anshuman Tripathi†

*Energy Research Institute at NTU, Interdisciplinary Graduate Programme, Nanyang Technological University, Singapore
Email: radhika010@e.ntu.edu.sg

†Energy Research Institute at NTU, Nanyang Technological University, Singapore

‡Department of Electrical Engineering, Indian Institute of Technology Palakkad, India 678623
Email: nagabrahmendra.g@iitpkd.ac.in

§Department of Electrical and Electronic Engineering, University of Melbourne, Melbourne, Australia
Email: gfarivar@unimelb.edu.au

¶School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
Email: j.pou@ntu.edu.sg

***Abstract*—In the modular three-stage solid-state transformer (SST), each phase is integrated with large dc-link capacitors as energy buffers, to filter the second harmonic capacitor voltage ripple generated due to single-phase power processing. Although large dc-link capacitors reduce the coupling between stages of the SST and simplify the controller design, they compromise the reliability, safety and power density of the SST. Accordingly, a low-capacitance SST is desirable to address these challenges. To provide a high-bandwidth control for the low-capacitance SST, this paper proposes using an analytic filtering scheme rather than the low-pass filters used in conventional SST control schemes. A portion of the second harmonic power ripple in the high-voltage dc-link capacitors is processed by the SST's dc-dc stage to facilitate the use of low capacitance. The effectiveness of the proposed control is demonstrated through a simulation study in PLECS.**

Keywords: Analytic filter, low-pass filter, solid-state transformer.

I. Introduction

With the rapid growth in the use of renewable energy sources in the power distribution network, the need for smarter technologies to regulate the power flow at critical nodes is increasing. One such solution that provides flexible energy flow control among various sources and loads is a solid-state transformer (SST) [1]-[4]. Fig. 1 depicts a commonly used modular three-stage SST architecture with N strings [5], [6]. It consists of a cascaded H-bridge (CHB) ac-dc converter in Stage I. Each floating high-voltage (HV) dc-link of Stage I is connected to a dual-active bridge (DAB) dc-dc converter in Stage II . The outputs of all DABs are connected in parallel to form a low-voltage (LV) dc-link. Finally, a two-level inverter converts LVdc to LVac in Stage III.

With large capacitors at the HV and LV dc-links, disturbance decoupling among various stages of the SST happens naturally. Thus, the controller for each stage can be designed independently with well-known control approaches [1], [7]-[9]. However, large capacitors add undesired weight and cost to the system, thus limiting the SSTs application and competitiveness with respect to the conventional low-frequency transformers. Furthermore, large capacitances are typically achieved by using electrolytic capacitors, which deteriorates the overall SST reliability [10]. Addressing the reliability issue is critical to make the SST an appealing and commercial option. Low-capacitance allows the use of more reliable capacitor technologies, such as film capacitors.

To facilitate the use of low-capacitance in the system, it is necessary to look into:

1) High-bandwidth controllers to reduce the strain on the dc-link capacitors during any transient conditions, and
2) The maximum allowable second-harmonic power ripple absorbed by the HV dc-link capacitors such that the converters in Stage I do not operate in overmodulation region.

Low-bandwidth outer-control-loops, commonly used in conventional SSTs, are unsuitable for the low-capacitance SST because a reduced electrical inertia leads to increased coupling among various stages of the SST [11], [12]. In this paper, an analytic filtering scheme inspired by that in [10] for low-capacitance static compensators (STATCOMs), is used to improve the bandwidth of the low-capacitance SSTs. In SSTs, the HV dc-link caps interface two stages, whereas in the STATCOM the capacitors are floating. Furthermore, the suggested control is built in a way that allows the HV dc-link and the DAB stage to share a flexible portion of the second harmonic power ripple.

The paper, first, revisits the conventional control used in SSTs in Section II. Then, Section III describes the proposed changes to the conventional control with analytical expressions for the HV dc-link capacitor voltages. Section IV provides simulation results that compare the performance of the conventional and the proposed control of the low-capacitance SSTs. Section V concludes the paper.

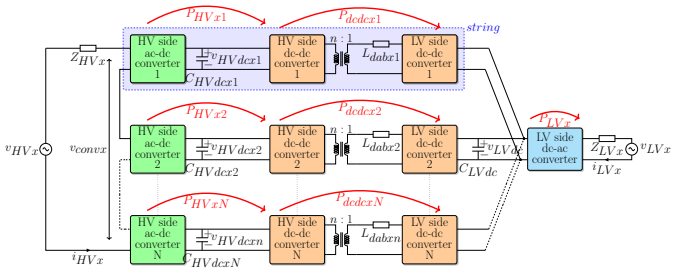


Fig. 1. Three stage cascaded SST.

II. Conventional Control of SST

A single phase of a three-phase three-stage cascaded SST is shown in Fig. 1. The HV grid voltage, v_{HVx}, with operating frequency, ω_{HV} rad/s, and grid impedance, $Z_{HVx} = R_{HVx} + j\omega_{HV}L_{HVx}$, is connected across Nstrings CHB converter of Stage-I. R_{HVx} is the equivalent input resistance and L_{HVx} is the equivalent input inductance, with $x \in \{a, b, c\}$ representing the phase arm. The HV dc-link voltage, v_{HVdcxj}, is held with the use of HV dc-link capacitors with capacitance, $C_{HVdc,xj}$, where $j \in \{1, 2, ...N\}$ is the string index. The individual HV dc-links are connected through DABs with high frequency isolation transformer having turns ratio $n : 1$, and external inductance L_{dabxj}. The output of which is connected in parallel forming the LV dc-link holding voltage, v_{LVdc}, using capacitance C_{LVdc}. The LV dc-link connects to the LV grid with voltage, v_{LVx}, and impedance, $Z_{LVx} = R_{LVx} + j\omega_{LV}L_{LVx}$, through a three-phase inverter, forming the Stage III.

The conventional control of the SST is designed by viewing it in decoupled stages, i.e., Stage I controls the input grid current and total voltage/energy in HV dc-link capacitors, Stage II collectively controls the voltage/energy in LV dc-link capacitor, and Stage III controls the output power requirements to the LV grid.

Stage I control uses a dual loop control strategy, with outer loop energy control and an inner loop current control shown in Fig. 2. The outer loop provides a power reference, P_{HVref}, to the inner loop that consists of two main components: (i) a known power feedforward term, P_{LVref}, and (ii) an incremental term, P_{HVout}, from the output of the proportional-integral (PI) controller, $PI_{HVv^2}(s)$, by processing the error between the presecribed HV dc-link energy reference, E_{HVref}, and the system dc-link energy, E_{HVfb}, where,

$$E_{HVfb} = \sum_{x=a,b,c} \sum_{j=1}^{N} \frac{1}{2} C_{HVdcxj} v_{HVdcxj}^2. \tag{1}$$

Additionally, due to the series cascaded structure in Stage I, additional voltage balancing control loops are required to ensure balanced voltages across the HV dc-links. This is achieved by modifying the modulation signal, $v_{HVxjref}$, using a voltage balancing controller $PI_{vb}(s)$. Note that E_{HVfb} contains a dc term and a second-harmonic ripple in the steady-state. The second-harmonic ripple is conventionally filtered for

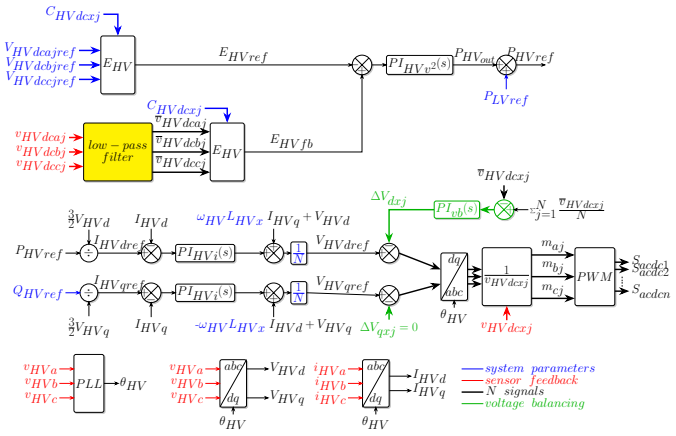


Fig. 2. Control of HV ac-dc converter in Stage I using the conventional method.

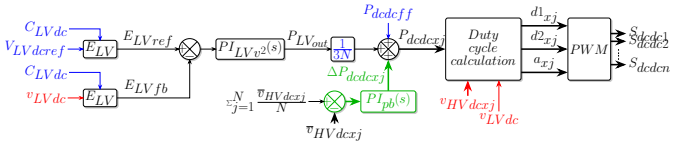


Fig. 3. Control of dc-dc converters in Stage II using the conventional method.

control purposes using a second-order low-pass filter (LPF), as highlighted in the control block diagram of Stage I in Fig. 2. The inner-current controller is a conventional dq frame controller.

Stage II control, shown in Fig. 3, on the other hand, commonly uses a single energy loop. The power reference, P_{dcdcxj}, for duty cycle calculations consists of three components: (i) A known power feedforward term, $P_{dcdcff} = P_{LVref}/3N$, (ii) an incremental power term, P_{LVout}, obtained from a PI controller, $PI_{LVv^2}(s)$, by processing the error between the LV dc-link energy, E_{LVfb} and the prescribed LV dc-link energy reference, E_{LVfb}, where,

$$E_{LVfb} = \frac{1}{2} C_{LVdc} v_{LVdc}^2, \tag{2}$$

and (iii) an incremental power term, ΔP_{dcdcxj}, obtained from a power balancing PI controller, $PI_{pb}(s)$, for power balancing purposes among the N strings.

Stage III control is similar to the inner-dq current control of Stage I, with known active and reactive power references, P_{LVref} and Q_{LVref}, respectively.

III. Proposed Control of SST

The major limiting factor affecting the bandwidth of the system is the LPF used in the outer-energy loop of the ac-dc converter in Stage-I. This filter entails slow control of the capacitor voltages, which could cause severe under/over-voltages in a low-capacitance SST, thus compromising the system safety and stability. Moreover, a percentage of second-harmonic power ripple can be processed by Stage II to avoid overmodulation in Stage I.

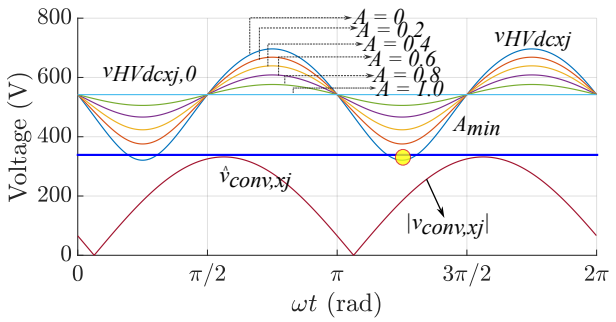


Fig. 4. A visual representation for minimum value of A required to avoid the overmodulation region of Stage I converter operating with unity power factor and 0.6 modulation index.

A. Minimum Percentage of the Second Harmonic Power Through DAB

To realize the low-capacitance SST, a percentage of the second harmonic power (henceforth denoted as A) is processed through the DAB stage. Let p_{HVxj} denote the instantaneous power processed by the j^{th} string of Stage I in x^{th} phase, which includes a dc power term, $\overline{P}_{HVxj}$, and a second-harmonic power ripple term, $\widetilde{p}_{HVxj}$, namely,

$$p_{HVxj} = v_{convxj} i_{HVx} = \overline{P}_{HVxj} + \widetilde{p}_{HVxj}, \tag{3}$$

where v_{convxj} is the converter voltage waveform across the ac-side of the j^{th} string of Stage I. Assuming, v_{convxj} and i_{HVx}, as pure sinusoidal signals, namely,

$$v_{convxj} = \hat{v}_{convxj} \sin(\omega_{HV} t), \tag{4}$$

and,

$$i_{HVx} = \hat{i}_{HVx} \sin\sin(\omega_{HV} t + \theta), \tag{5}$$

where θ is the phase shift between v_{convxj} and i_{HV}, and $\hat{v}_{convxj}$ and $\hat{i}_{HVx}$ denote the respective amplitudes. Substitution of (4) and (5) in (3) yields,

$$\overline{P}_{HVxj} = \frac{1}{2} \hat{v}_{conv,xj} \hat{i}_{HV} \cos(\theta), \tag{6}$$

and

$$\widetilde{p}_{HVxj} = \frac{1}{2} \hat{v}_{conv,xj} \hat{i}_{HVx} \cos(2\omega_{HV} t + \theta). \tag{7}$$

Note that, $\hat{v}_{convxj}, \hat{i}_{HVx}$, and θ are variables readily available from the control of Stage I in Fig. 2, i.e.,

$$\hat{v}_{conv,xj} = \sqrt{V_{HVdref}^2 + V_{HVqref}^2}, \tag{8}$$

$$\hat{i}_{HVx} = \sqrt{I_{HVdref}^2 + I_{HVqref}^2}, \tag{9}$$

and

$$\theta = arctan2(V_{HVqref}, V_{HVdref}). \tag{10}$$

Let p_{dcdcxj} denote the power processed by the DAB, which consists of (i) the dc power $\overline{P}_{HVxj}$ in (6) (since the capacitor does not process active power in the steady-state), and (ii) a fraction A of the second-harmonic power ripple $\widetilde{p}_{HVxj}$ in (7), namely

$$p_{dcdcxj} = \overline{P}_{HVxj} + A\widetilde{p}_{HVxj}. \tag{11}$$

The energy balance equation on the HV dc-link capacitor according to (3) and (11) corresponds to

$$\frac{1}{2} C_{HVdcxj} v_{HVdcxj}^2(t) =$$

$$\frac{1}{2} C_{HVdcxj} v_{HVdcxj,0}^2 + (1 - A) \int_0^t \widetilde{p}_{HVxj}(t)\, dt, \tag{12}$$

where $v_{HVdcxj,0}$ is the average HV dc-link voltage. Substituting (6), (7), and (11) into (12), and solving the integral, yields,

$v_{HVdcxj}(t) =$

$$\sqrt{v_{HVdcxj,0}^2 + (1 - A) \frac{\hat{v}_{convxj} \hat{i}_{HVx} \sin(2\omega_{HV} t + \theta)}{2\omega_{HV} C_{HVdcxj}}} \tag{13}$$

The condition $v_{HVdcxj} \geq |v_{HVconvxj}|/N$ must be satisfied at all times to avoid overmodulation, shown in Fig. 4 for different values of A. Note that $\sin(2\omega_{HV} t + \theta) = -1$ has been considered, which corresponds to the minimum value of (13). Therefore, the overmodulation inequality results in,

$$A \geq 1 - v_{HVdcxj}^2 \left(\frac{1}{m_{xj}^2} - 1\right) \frac{2\omega_{HV} C_{HVdcxj}}{\hat{v}_{convxj} \hat{i}_{HVx}} \tag{14}$$

which provides the minimum value of A, A_{min}, to be processed by DAB while preventing overmodulation for a given operating condition, or equivalently, how much the capacitor size C_{HVdcxj} can be reduced. m_{xj} is the modulation index of the CHB converter, i.e.,

$$m_{xj} = \frac{\hat{v}_{convxj}}{v_{HVdcxj}}. \tag{15}$$

For example, for a 6.6-kV/400-V, 1.2-MVA (1 p.u.) SST with $N = 5$ strings, operating at 10 kHz, with an average HV dc-link voltage, $v_{HVdcxj,0} = 1750$V across each string, A_{min} for two different HV dc-link capacitors, $C_{HVdcxj} = 83$ μF and 20 μF, is shown in Fig. 5. When $C_{HVdcxj} = 83$ μF, the maximum power ripple processed by the capacitor without overmodulation in the steady-state operation is 0.63 p.u. If larger power values are to be processed, the DAB will take care of it, i.e., A_{min} needs to be processed by Stage II. In this case, to transfer 1 p.u. of power, it is essential that $A \geq 0.4$. Similarly, for $C_{HVdcxj} = 20$ μF, the maximum power processed by the HV dc-link capacitor without overmodulation is 0.16 p.u. However, the maximum value of voltage across the HV dc-link capacitors, i.e., $\hat{v}_{HVdcxj}$ reaches 1.28 p.u. To reduce the peak voltage, $\hat{v}_{HVdcxj}$ to 1.1 p.u, corresponding

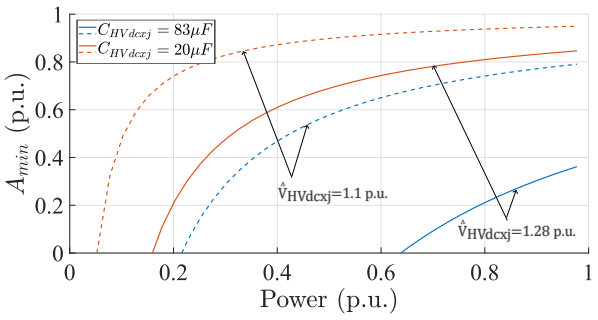


Fig. 5. A_{min} for a 6.6-kV/400-V, 1.2-MVA (1 p.u.) SST with 5 strings with different C_{HVdcxj}.

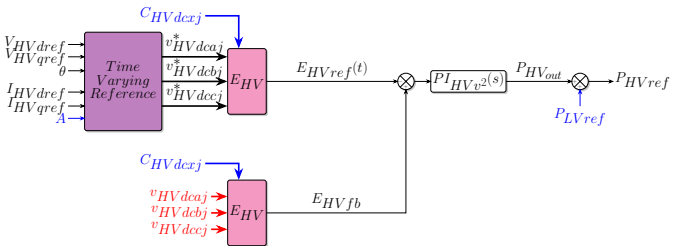


Fig. 6. Proposed control for Stage I with time-varying HV dc-link voltage references, obtained from (13).

value of minimum allowable HV dc-link voltage, $v_{HVdcxj}(t)$, is chosen and (13) is solved for the inequality constraint such that A_{min} curve follows the dashed line for the given choice of C_{HVdcxj}.

B. Proposed Control Using Time Varying References for HV DC-Link Energy Control

In the proposed control scheme, two main changes are made to the conventional control block diagrams shown in Figs. 2 and 3. Specifically, the LPF (highlighted in yellow in Fig. 2) is eliminated. For this purpose, a time-varying reference, $E_{HVref}(t)$ correponding to (13) is used eliminating the need for an LPF. Since the delay in the ripple estimation is one sample, the filtering is almost instantaneous, allowing a higher control bandwidth straightaway. The modified control diagram for the outer energy loop of Stage I is shown in Fig. 6.

Regarding the DAB control, the feedforward power term P_{dcdcff}, used in the conventional DAB control of Fig. 3, is modified by adding a fraction A of power ripple that the DAB must process for overmodulation consideration, such that,

$$P_{dcdcff} = \frac{P_{LVref}}{3N} + A\frac{v_{convxj}i_{HVx} - P_{LVref}}{3N}. \quad (16)$$

IV. Simulations

To validate the proposed improvements in the low-capacitance SST control, a 6.6-kV/400-V, 1.2-MVA (1 p.u.) SST operating at 10 kHz has been simulated using PLECS simulation patform. A detailed list of parameters used for the simulations is given in Table I.

TABLE I
Simulation Parameters

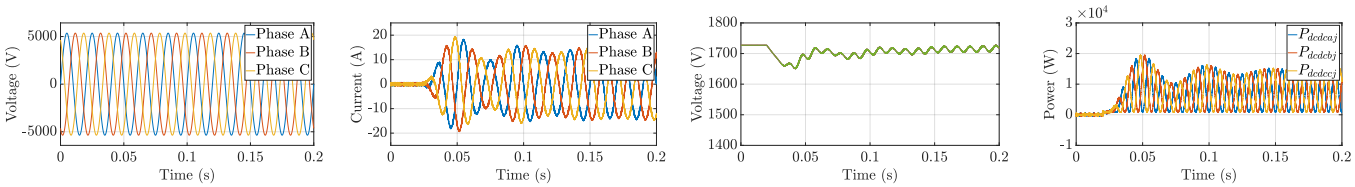
Definition	Symbol	Value
Stage I		
No. of strings per phase	N	5
HV grid voltage amplitude (per phase)	$\hat{v}_{HVx}$	$3.8\sqrt{2}$ kV
HV grid frequency	f_{HV}	50 Hz
HV grid equivalent resistance (per phase)	R_{HVx}	0.12 Ω
HV grid equivalent inductance (per phase)	L_{HVx}	6 mH
Stage I switching frequency	f_{acdc}	5 kHz
average HV dc-link voltage	$v_{HVdcxj,0}$	1.7 kV
HV dc-link capacitance	C_{HVdcxj}	83 μF, 20 μF
Stage II		
DAB external inducatnce	$L_{dab,xj}$	240 μH
Transformer turns ratio	n	7 : 2
Stage II switching frequency	f_{dcdc}	10 kHz
Stage III		
LV grid voltage amplitude (per phase)	$\hat{v}_{LVx}$	$230\sqrt{2}$ V
LV grid frequency	f_{LV}	60 Hz
LV equivalent resistance (per phase)	R_{LVx}	0.8 $m\Omega$
LV equivalent inductance (per phase)	L_{LVx}	40 μH
LV dc-link capacitance	C_{LVdc}	75 mF
average LV dc-link voltage	v_{LVdc}	700 V
Stage III switching frequency	f_{dcac}	18 kHz

TABLE II
Comparison of Simulated Test Cases

C_{HVdcxj}	Control	Test Case	v_{HVdcxj} under-shoot	t_s	THD_i
83 μF	LPF	0 p.u. - 0.1 p.u. (Fig. 7)	<0.05 p.u	0.2 s	0.07%
83 μF	(13)	0 p.u. - 0.1 p.u. (Fig. 8)	<0.01 p.u	<0.01 s	0.07%
20 μF	LPF	0 p.u. - 0.1 p.u. (Fig. 9)	0.1 p.u	0.2 s	2.6%
20 μF	(13)	0 p.u. - 0.1 p.u. (Fig. 10)	<0.01 p.u	0.02 s	2.6%
83 μF	(13)	0 p.u. - 1 p.u. (Fig. 11)	<0.01 p.u	<0.01 s	0.09%

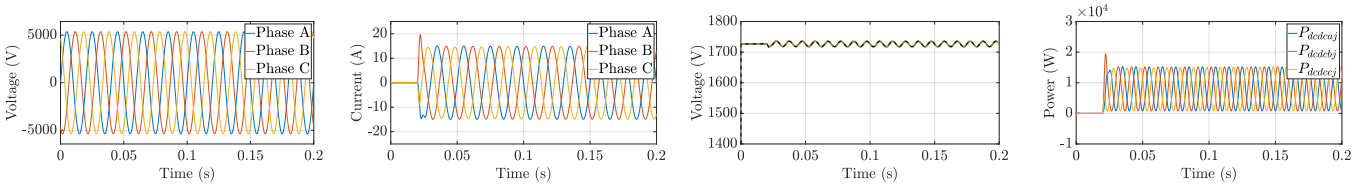
In this study, two different choices of HV dc-link capacitors, 83 μF and 20 μF, are used. 90% power ripple is considered for Stage II, i.e., A=0.9, which is above A_{min} for both choices of the HV dc-link capacitors, according to Fig. 5. This involves a fixed 10% of twice-fundamental-frequency oscillating power flow into the HV dc-link capacitors.

The results obtained for a step change in active power from 0 p.u. to 0.1 p.u., are summarized in Figs. 7 and 8 for $C_{HVdcxj} = 83$ μF and in Figs. 9 and 10 for 20 μF. To



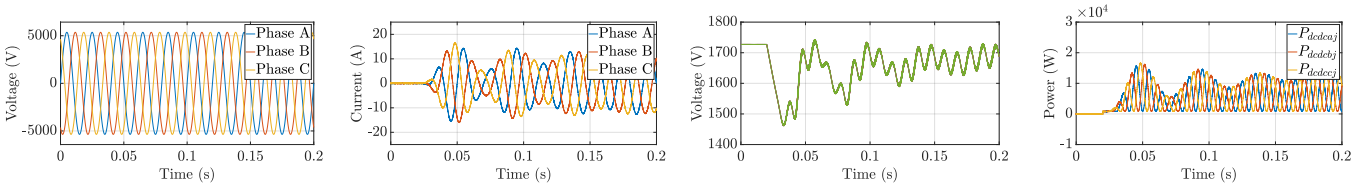
(a) (b) (c) (d)

Fig. 7. Simulation study with a step change in active power from 0 p.u. to 0.1 p.u. for $C_{HVdcxj} = 83\ \mu F$ using LPF: (a) HV grid voltage v_{HVx}, (b) HV grid current i_{HVx}, (c) HV dc-link voltages v_{HVdcxj}, and (d) power through dc-dc stage P_{dcdcxj}.



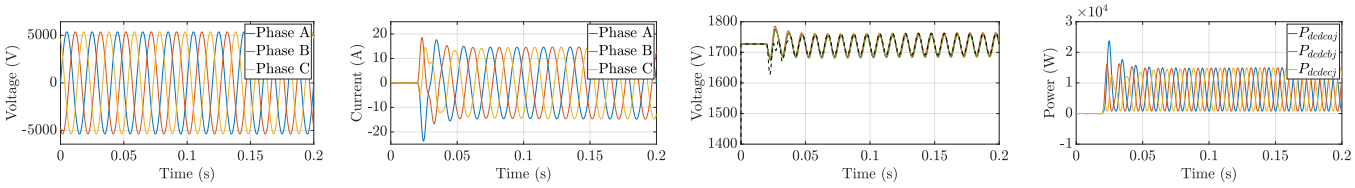
(a) (b) (c) (d)

Fig. 8. Simulation study with a step change in active power from 0 p.u. to 0.1 p.u. for $C_{HVdcxj} = 83\ \mu F$ using (13): (a) HV grid voltage v_{HVx}, (b) HV grid current i_{HVx}, (c) HV dc-link voltages v_{HVdcxj}, and (d) power through dc-dc stage P_{dcdcxj}.



(a) (b) (c) (d)

Fig. 9. Simulation study with a step change in active power from 0 p.u. to 0.1 p.u. for $C_{HVdcxj} = 20\ \mu F$ using LPF: (a) HV grid voltage v_{HVx}, (b) HV grid current i_{HVx}, (c) HV dc-link voltages v_{HVdcxj}, and (d) power through dc-dc stage P_{dcdcxj}.



(a) (b) (c) (d)

Fig. 10. Simulation study with a step change in active power from 0 p.u. to 0.1 p.u. for $C_{HVdcxj} = 20\ \mu F$ using (13): (a) HV grid voltage v_{HVx}, (b) HV grid current i_{HVx}, (c) HV dc-link voltages v_{HVdcxj}, and (d) power through dc-dc stage P_{dcdcxj}.

illustrate the effect of the controller, the power feedforward term, i.e. P_{LVref}, is set to 0. Fig. 7 shows the transient results when adopting a conventional control with LPFs, while Fig. 8 depicts the same waveforms when using the proposed control with time varying reference. Specifically, Figs. 7(c) and 8(c) show the HV dc-link capacitor voltages, and the ripple estimated according to (13) in a dotted line. As seen in these figures, the proposed control shows superior transient responses. Specifically, by using time-varying references, a negligible voltage drop on the C_{HVdcxj} is observed as compared to 0.04 p.u. when LPF are used. This is because of high bandwidth for outer-energy controller achieved by eliminating LPFs. Moreover, the settling time improves from 0.2 s to < 0.1ms. A similar trend is seen for $C_{HVdcxj} = 20\ \mu$F, in Figs. 9 and 10. As the HV dc-link capacitance is reduced, the system is more immune to load transients, and hence, for the given step change in load, the HV dc-link voltage undershoot is increased by 50% when compared with the simulation study for $C_{HVdcxj} = 83\ \mu$F and LPFs. But, with the proposed control, the voltage undershoot is reduced to ≤ 0.01 p.u. as seen in Fig. 10(c).

Looking at the grid current profile in the steady-state in Figs. 8(b) and 10(b), the THD_i is increased to 2.6% with $C_{HVdcxj} = 20\ \mu$F, compared to 0.07% with $C_{HVdcxj} = 83$

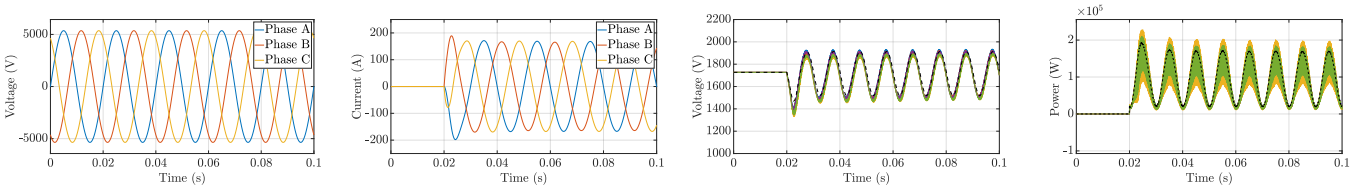


Fig. 11. Simulation study with a step change in active power from 0 p.u. to 1 p.u. for $C_{HVdcxj} = 83\ \mu F$ using (13): (a) HV grid voltage v_{HVx}, (b) HV grid current i_{HVx}, (c) HV dc-link voltages v_{HVdcxj}, and (d) power through dc-dc stage P_{dcdcxj}.

μF. This is because of increased ripple voltage with reduced capacitance. However, the THD_i remains lower than the standard grid requirements of 5%.

A simulation study for a load transient of 0 to 1 p.u is shown in Fig. 11 using the proposed time-varying references and a known power feedforward term, i.e., P_{LVref}. Even with a substantial transient change in the load, the system remains in safe operating limits owing to the high bandwidth controllers. A detailed comparison on the observed load transient conditions, is summarized in Table. II.

V. Conclusion

This paper has proposed the use of time varying references in SST control system with the aim of increasing the bandwidth of the controller, which is especially relevant in the low-capacitance SST due to its lower electrical inertia. The simulation results obtained from a 1.2-MVA low-capacitance SST, confirm the feasibility and effectiveness of the proposed control system as compared to a conventional control system. With the improvised control of Stage I using time varying references, the undervoltage observed on HV dc-link capacitors during the load transient, is improved at least by 80%. Moreover, the settling time is improved from 0.2 s to < 0.02 s. The THD_I of the steady-state grid current remains within the standard grid code limit of 5%, assuring the feasibility of low-capacitance SSTs.

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