Design of a Class G Audio Amplifier

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ABSTRACT

The demand for audio power amplifier in portable multimedia devices has been on a rise. For both manufacturers and consumers, power efficiency to maintain long battery lifetime, miniaturization to achieve smaller form factor and low Total Harmonic Distortion (THD) for quality sound synthesis are the key factors in choosing new audio gear. Linear amplifiers, such as Class A, Class B and Class AB amplifiers have low power efficiency. On the other hand, Class D amplifier which is switching amplifier, despite its relatively higher power efficiency, suffers from large form factor due to the external inductor.

To address the above mentioned problems, an inductorless Class G power amplifier has been designed, operating with a single power supply. It is capable of driving a loudspeaker of up to 8Ω in parallel with a 220pF capacitive load while consuming quiescent current as low as 5mA. The proposed Class G power amplifier consists of the power supply unit and the switched-supply based amplifier unit. The power supply unit utilizes a switched-capacitor DC-DC step-down converter. It has a pulse-skip regulation to convert the external power supply (3.6V) into an internal supply rail with lower voltage (1.6V). Inside the switched-supply based amplifier unit, the supply control circuit selects between the external power supply and internal supply rail. The selection is based on the instantaneous input voltage information.

The preamplifiers and DC control circuit adjust the DC offset of input audio signal into an optimum DC operating level. This design uses bridge-tied-load Class AB configuration in order to maximize the output power.

Unlike other Class G amplifiers that rely on triple-well process technology, the proposed Class G power amplifier is realized using standard twin-well 0.35um CMOS process technology. This design contains only four power transistors while eliminating any use of inductor or power diodes. With 3.6V single power supply, the peak load power is 1.45W. The THD of final output signal is less than 0.1% at 20 kHz and less than 0.05% at 1 kHz. An A-weighted signal-to-noise ratio (SNR) of 97.3dB is achieved. The circuit performance of the Class G amplifier is then compared with prior-art works. It has successfully demonstrated the comparable performance with respect to the commercial products while gaining the stated advantages. As a result, the effectiveness of the circuit architecture is validated.

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CHAPTER 1

INTRODUCTION

1.1 Motivations

In the last decade, there was a significant technological advancement in audio amplifiers due to the demand for portable electronic instruments such as CD players, DVD players, MP4 players and so forth. In these devices, an audio power amplifier is required to drive a portable loudspeaker or an earphone. For most consumers, power efficiency to maintain long battery lifetime and miniaturization to reduce PCB area outweighs other factors in the choice of new audio gear. In addition, a high-efficiency amplifier will generate less heat in the power transistors, resulting in smaller heat sink [1, 2] and smaller chip size.

Moreover, the amplifier should have high fidelity for good sound quality. This leads to another critical performance metric, namely linearity of the audio amplifier. It is quantified by Total Harmonic Distortion (THD). It shows how accurate the audio signal is retained after being processed by the audio system. In a high quality musical system, this is regarded as the most important parameter.

Based on the working principle, audio power amplifiers can be classified into two categories, namely the linear amplifiers and the switch-mode amplifiers. In a linear

amplifier such as the Class A, Class B or Class AB amplifiers, the output is linearity proportional to the input signal. On the other hand, the output signal of a switched-mode amplifier such as the Class D amplifier is a pulse width modulated or pulse density modulated signal. The width of the pulse is proportional to the amplitude of the input signal. The audio signal has to be recovered by passing the pulse modulated signal through a low-pass filter.

For classical linear power amplifiers, the Class B power amplifier has a maximum theoretical efficiency of 78.5% at full swing. However, audio power amplifiers usually do not operate at full signal swing. For typical audio amplification, the crest factor of the audio signal can be as large as 15 dB and the average signal swing is in the range of 15% to 25% of full swing [3, 4]. Under this operation, the power efficiency of linear power will be much lower. Using Class AB amplifier (the most popular linear power amplifier) as an example, the typical power efficiency for audio application is usually less than 20% [3].

Due to poor efficiency of the classical amplifiers, research was focused on the switch-mode power amplifier which offers much higher power efficiency. One of these amplifiers is the Class D amplifier, which is currently most popular due to its very high power efficiency (greater than 90%) [5, 6]. However, the design of the amplifier is extremely complex. It requires an external LC low-pass filter which

occupies significant area on the PCB. Besides, the micro-Henry range inductor is also very expensive. Thus, the need for an external inductor is one of the design issues for Class D amplifier design.

To eliminate the need for the external LC low-pass filter, Class D audio power amplifiers can also be configured as a filterless structure using the output stage to drive the speaker directly [7, 8, 9]. However, the Pulse-width modulation (PWM) switching at the Class D output stage will still generate electro-magnetic interference (EMI) problem. As a result, the quality of the output audio signal will be affected. In a reported work [10], the experiment results show that the output signal of Class D power amplifier is at least ten times higher than the total harmonic distortion (THD) of the classical power amplifiers such as Class AB amplifier.

In summary, the disadvantages of linear amplifiers and switched-mode amplifiers have inspired the search for alternative techniques to overcome all these drawbacks while retaining the high performance at the same time. As such, the Class G amplifier topology with relatively high power efficiency and high linearity provides an attractive solution for portable audio applications.

Class G power amplifier is a combination of Class AB amplifier and power supply unit [11]. Class AB amplifier usually has a good output performance. However, when

the amplitude of output signal is small, the power loss at the output stage due to the large drain-to-source voltage (Vds) across the output power transistors is significant. To solve this problem, a power supply unit which aims to generate different supply rails is used in Class G power amplifier. The block diagram of a typical Class G amplifier is shown in Figure 1.1.

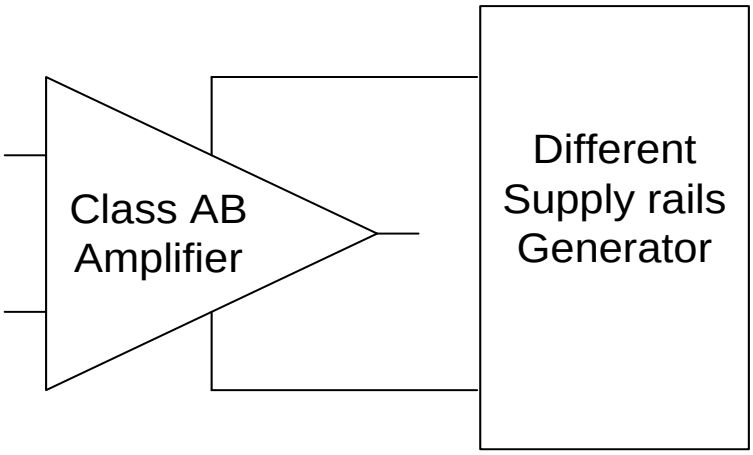


Figure 1.1 Block diagram of a typical Class G power amplifier

The power supply unit can produce different supply voltage levels. A typical Class G operation requires two supply rails: one for the high-voltage power supply and the other for a lower supply voltage. The low-voltage power supply is activated when the output signal amplitude is detected to be small. Consequently, the voltage across the output power transistor as well as their power consumption can be effectively reduced. As long as the output signal increases to a predetermined threshold level, the output stage will be switched to a high-voltage power supply to ensure enough

power to be delivered to the load without creating any clipping effect in a given dynamic swing. Hence, the Class G power amplifier can achieve high power efficiency. Furthermore, its structure is much simpler when compared with that of the switched-mode amplifiers. Therefore, it offers a good audio solution for portable devices.

Class G amplifier has many applications. These include data transmission line [12-14], active magnetic bearing [15] and audio system [16]. This thesis emphasizes on the audio application. For audio scenario, it can be classified into loudspeaker driver and headphone driver. The Class G amplifier introduced here is of primary focus to drive a ceramic loudspeaker. In addition to this application, it is also capable to serve as a headphone driver for different headphone loads. There are several reported Class G audio amplifier topologies. However, they have the disadvantages in terms of multiple supplies, inductor and number of power devices. This raises the motivations of this work to design an improved Class-G amplifier to overcome the drawbacks of the existing designs.

1.2 Objectives

With the above considerations, the main focus of this thesis is to investigate and design a high-performance inductorless, single supply Class G power amplifier for portable applications.

The specifications are shown as follows:

Table 1.1 Design Specifications

Technology	AMS 0.35um CMOS
Supply voltage	3.6V
Quiescent biasing current	<5mA
Load Resistance	8Ω
Load Capacitance	200pF
Power delivered	600mW
THD	<0.1%
Inductor	None

1.3 Organization

The report consists of five chapters. They are given as follows:

Chapter 1 gives a brief introduction of the audio power amplifiers, leading to the motivation of this research. The objective and scope of the research are also discussed. Chapter 2 reviews different types of power amplifier in conjunction with the discussion on their advantages and disadvantages. Different configurations of Class G amplifier are also described. Chapter 3 presents the proposed Class G audio power amplifier and its main building blocks, which is then followed by the detailed

circuit design. Chapter 4 discusses the simulation results in details. Finally, this report is concluded in Chapter 5. The summary of proposed Class G audio power amplifier is presented, and followed by the proposed future work.

1.4 Major Contributions

In this project, several contributions have been made. They are summarized as follows:

1. A novel architecture has been proposed for a single supply inductorless Class G audio power amplifier. It is capable to provide 1.45W peak power and drive a heavy load with 8Ω//200pF

2. A novel supply control circuit is employed to select the proper supply rail in order to achieve the highest possible power efficiency without causing any glitches.

3. A preamplifier circuit with DC signal conditioning is proposed to adjust the DC offset of input signal for optimal DC operating voltage without a big AC coupling capacitor.

4. A novel high PSR voltage reference circuit has been designed. It generates a

stable reference voltage with the temperature coefficient of 25.2 ppm/°C and PSR of -94dB at low frequencies, -60dB at 1MHz and -40dB at 10MHz.

CHAPTER 2

LITERATURE REVIEW

Power amplifiers are designed to magnify both voltage and current of a given input signal and deliver huge power to a heavy load. They are classified into different classes according to their circuit configurations and operating methods. There are two main types of power amplifiers. One type is the linear amplifier which generally has a high linearity but suffers from relatively low power efficiency. The other type is the switched-mode amplifier which features high switching frequencies with respect to that of the analog signals. Switched-mode amplifiers usually have high power efficiency but relatively lower linearity.

Power amplifier has a wide range of audio applications that occupies a big portion in modern life. This chapter gives a description of the different types of power amplifier that are used in audio applications such as Class A, Class B, Class AB, Class D, Class H and Class G.

2.1 Review of Different Types of Power Amplifier

2.1.1 Classical Linear Amplifiers

Figure 2.1 Structure of the linear amplifier

The structure of a typical linear amplifier is depicted in Figure 2.1. It consists of an input stage, multiple gain stages and an output stage. The types of linear amplifier are distinguished according to the different output stage designs as well as the relative amount of time that the amplifying transistor (or transistors) is conducted. The time is measured in degrees of duration of an input sine wave, where 360 degrees represents a full cycle. This is known as the conduction angle [17]. Based on this, linear amplifiers are classified as Class A, Class B or Class AB.

2.1.1.1 Class A

In a Class A power amplifier, the amplifying transistor conducts all the time. The conduction angle of this kind of amplifier is 360°. Figure 2.2 depicts the basic configuration of a Class A amplifier [18,19].

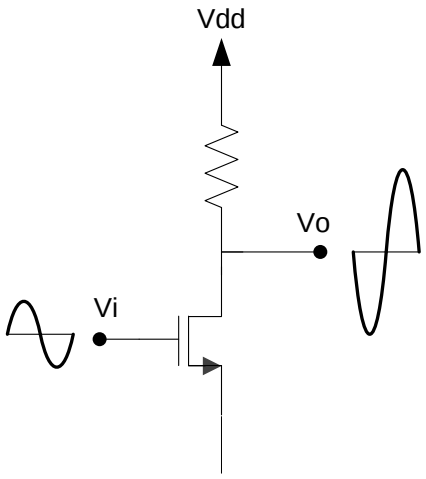


Figure 2.2 Basic configuration of a Class A amplifier

Since the amplifying transistor is always conducting even if there is no input signal, there is huge power consumption especially when a high voltage or current is delivered. Thus, Class A amplifier has the lowest efficiency with a maximum theoretical power efficiency of only 25% for a single-ended configuration and 50% for a push-pull structure [19]. Despite the drawback on low power efficiency, it has the highest linearity and simplest configuration. Therefore, Class A amplifier is usually adopted for high fidelity applications in which the power efficiency is not a critical consideration. However, it is often replaced by other designs with higher power efficiency.

2.1.1.2 Class B

Class B power amplifier usually adopts push-pull configuration at the output stage. There are two output transistors and each of them is biased to be conductive exactly half cycle. The conduction angle is 180º. Figure 2.3 shows the basic configuration of a Class B push-pull amplifier [19].

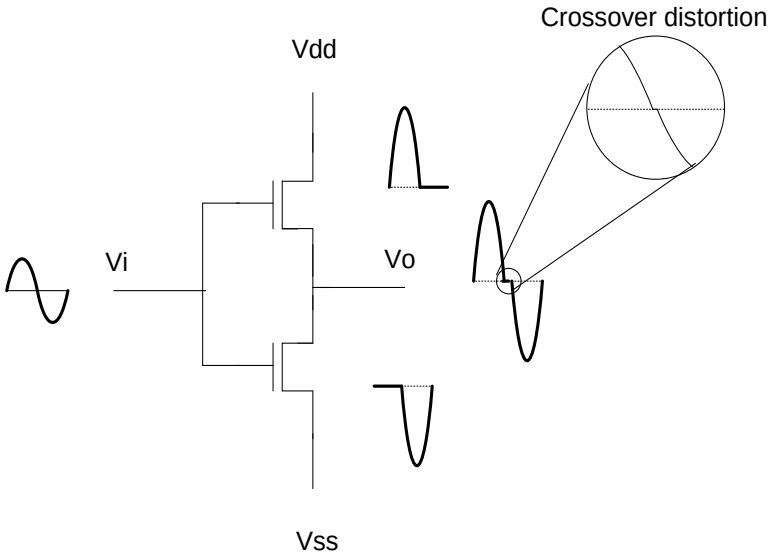


Figure 2.3 Basic configuration of Class B push-pull amplifier with crossover distortion

In Class B amplifier, within each half cycle, only one of the output transistors is conductive. The other output transistor is in the cut-off region. It does not consume any power. Therefore, the power efficiency of Class B amplifier has a maximum theoretical power efficiency of 78.5% [17-19]. This is higher than that of the Class A amplifier. However, during the imperfect transition between two output transistors, there is a small region where neither of them is turned on. This will create an

undesired crossover distortion, as shown in Figure 2.3. This distortion can impose a huge cost on linearity. Thus, it is regarded as the main disadvantage of Class B amplifier.

2.1.1.3 Class AB

Class AB power amplifier is a combination of Class A amplifier and Class B amplifier. It improves the crossover distortion of the Class B amplifier by biasing each output transistor such that they are conducted slightly more than half a cycle. There is a region in transition where the conduction of two output transistors works like a Class A amplifier. When the output goes beyond that region, one of the output transistors is cut off. Thus, the amplifier behaves like a Class B amplifier. The conduction angle of this type of amplifier is between 180º and 360º. Figure 2.4 shows the basic configuration of a Class AB push-pull amplifier [17,20].

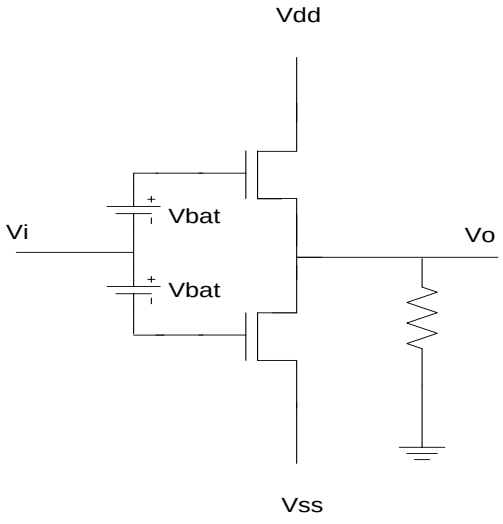


Figure 2.4 Basic configuration of a Class AB amplifier

Note that the two output transistors do not work in cut off region at the same time. Therefore, the crossover distortion is eliminated. This leads to a much better linearity when compared to the Class B amplifiers. However, Class AB amplifier requires more biasing current and consumes more power. When the input signal is zero, there is still a small residual current required to bias the output transistors. Therefore, the maximum power efficiency will be less than 78.5% (the maximum power efficiency of Class B amplifier). However, it is still much higher than that of the Class A amplifier. With a good linearity and power efficiency performance, Class AB push-pull amplifier is the dominant audio amplifier topology.

2.1.2 Switching Amplifiers

The poor efficiency of classical linear amplifier leads to the research of switch-mode power amplifier so as to improve the power efficiency. Although the idea of switching amplifier was invented early in 1950s, it was not accepted at that time due to the lack of fast-switching transistors with low on-resistances at the output stage. When the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is introduced in 1990s, the switching amplifiers became more popular.

2.1.2.1 Class D

Class D amplifier is called switching amplifier as the switches play an important role in the operation. It can be classified into analog Class D amplifier and digital Class D

amplifier. The analog input signal in Class D amplifier is converted into a sequence of pulses by modulation techniques such as Pulse Width Modulation (PWM), Pulse Density Modulation (PDM) and more advanced Sigma Delta modulation. The frequency of the pulse should be at least ten times larger than the highest frequency of the input signal. The basic configuration of a Class D amplifier is shown in Figure 2.5 [7, 21].

The operating principle of a Class D amplifier is as follows. The input signal of Class D amplifier is first compared with a triangular wave signal via a comparator to generate a square wave. This square wave is then fed to the switching controller and output stage to generate a sequence of high frequency output pulses. These pulses have the same amplitude but different widths. The averaged value of these pulses is directly proportional to the instantaneous input signal amplitude. At the last stage, a low-pass filter is applied to remove the harmonics of the output pulses. That is how the final output, which is an amplified replica of input signal, is generated to drive the load.

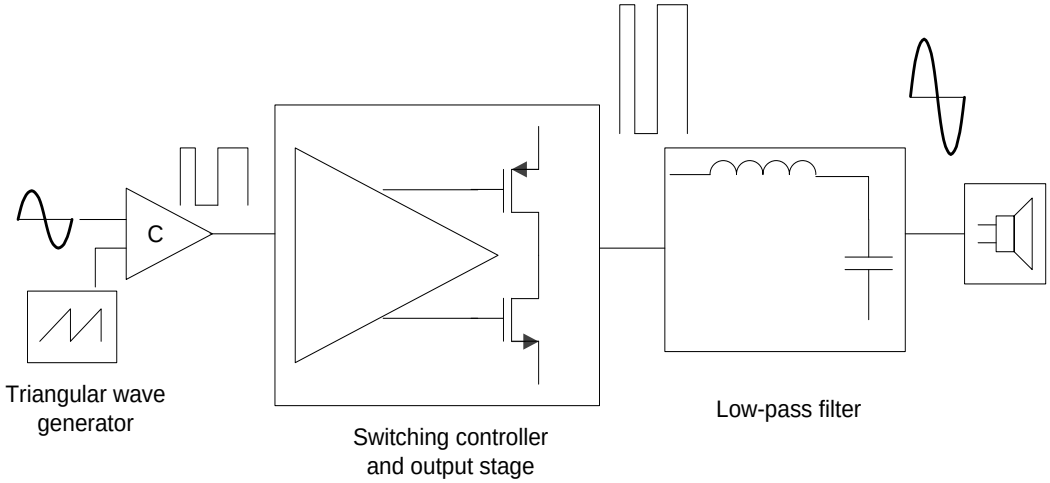


Figure 2.5 Basic configuration of a Class D amplifier

Class D amplifier has the highest power efficiency among all the power amplifiers. The theoretical efficiency is 100%. Even in practical applications it is possible to achieve power efficiency greater than 90% [5, 6]. However, the Class D amplifier is neither cheap nor easy to design owing to its architecture that requires an external low-pass filter, leading to the increase in both cost and board space. It is interesting to note that the *LC* filter is more expensive than the total cost pertaining to the rest of the circuit [12]. In addition, the PWM switching at the Class D output stage will result in electro-magnetic interference (EMI) in some applications. Due to its switching operations and non-perfect components, the total harmonic distortion (THD) is usually higher than those of the classical linear power amplifiers. For instance, the Class B amplifier can have a THD ten times better than Class D amplifier [10].

2.1.2.2 Class H

Class H power amplifier is an improvement of Class AB amplifier. It aims to combine the high linearity of linear amplifier with the high efficiency of switching amplifier. Class H amplifier improves the efficiency of Class AB amplifier by providing a variable supply voltage. This supply voltage is modulated according to the instantaneous output signal. Therefore, the voltage drop across the output transistors can always be kept at a minimum allowable value. The waveform of Class H power amplifier is shown in Figure 2.6 [19, 20].

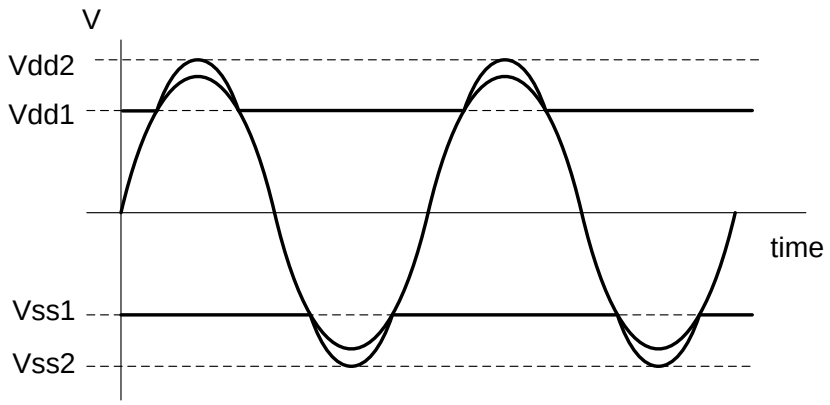


Figure 2.6 Waveform of Class H amplifier output

The power efficiency is kept at the maximum value all the time. In addition, the THD is also increased because of the class AB structure. However, Class H power amplifier has a very complex configuration in order to generate the variable power supply voltage.

2.1.3 Comparison of Audio Power Amplifiers

Generally speaking, linear amplifier has high linearity but low power efficiency. On the contrary, switching amplifier has high power efficiency but low linearity. Some other amplifiers such as Class G and Class H amplifiers combine the best of both linear amplifier and switching amplifier. Table 2.1 shows the comparison of different types of power amplifier in terms of power efficiency, linearity and configuration.

Table 2.1 Comparison of different types of power amplifier

Amplifier	Type	Power Efficiency	Linearity	Configuration
Class A	Linear	Low	High	Simple
Class B	Linear	Medium	Low	Simple
Class AB	Linear	Medium	High	Simple
Class D	Switching	Very High	Medium	Complex
Class G	Switching	High	High	Medium
Class H	Switching	High	High	Complex

2.2 Class G Amplifier

The idea of Class G amplifier [16] came about in the year 1976. At that time, it was mainly used in home applications. In recent years, the Class G amplifier has drawn more attention in the audio applications due to the rapid growth of portable device market.

2.2.1 Working Principle

Class G power amplifier is an improvement of Class AB amplifier by means of different supply rails. As discussed previously, the output power transistor of Class AB is connected to a fixed supply voltage. When the output signal amplitude is small, the Drain-to-Source voltage (Vds) across the output transistor is large. Therefore, the power consumption of the output power transistor, which equals to the product of drain voltage and current, is large. This results in a huge power loss.

Different with Class H which provides a variable supply voltage modulated according to the instantaneous output signal, a typical Class G power amplifier circumvents this problem by using two DC supply rails. When the output signal amplitude is small, the output transistors are connected to the low-voltage supply rail. As such, the voltage drop is effectively reduced across the output transistors, thus decreasing the power consumption. When the output signal increases to above a certain level, the output transistors are switched to the high-voltage supply rail in order to deliver adequate output power without introducing distortion due to clipping.

The waveform of Class G power amplifier is shown in Figure 2.7 [19]. The Class G power amplifier mainly improves the power efficiency when the output signal is small. Therefore, Class G power amplifier is a good option for typical audio

amplification where the crest factor of the signal can be as large as 15 dB [3].

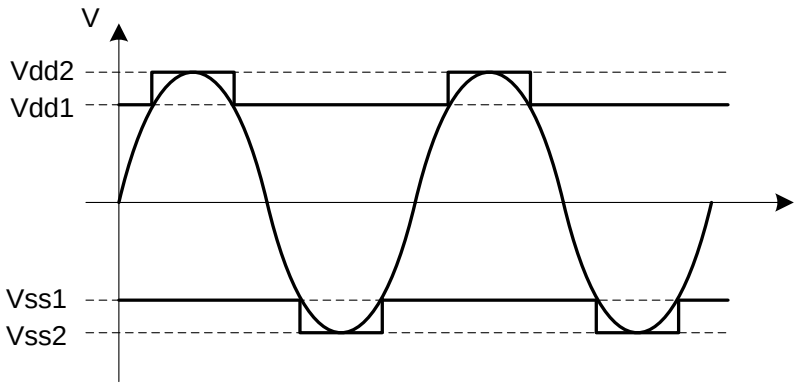


Figure 2.7 Waveform of Class G amplifier output

2.2.2 Basic Architecture

A typical Class G power amplifier consists of two main units. The basic architecture of Class G amplifier is illustrated in Figure 2.8. The power supply unit provides two or more dc power supply rails with different voltages. Those power supplies can be either all external supplies or mixture of external and internal supplies. The switched-supply amplifier unit, which employs Class AB configuration and the switch control unit, amplifies the input signal to drive the load.

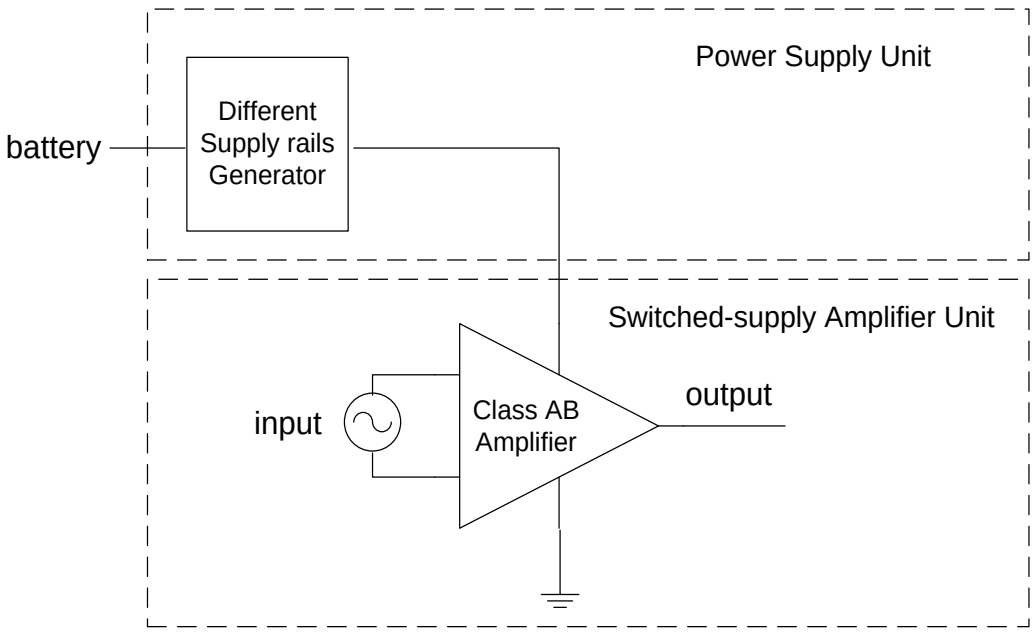


Figure 2.8 Architecture of Class G power amplifier

2.2.3 Power Supply Unit

The power supply section provides two or more supply rails with different voltage values. For the first developed Class G amplifier, all the supply rails are external power supplies. Nowadays with the development of portable devices, audio amplifiers are preferred to operate under uni-polar power supply. Therefore, it is better to generate the internal power supply using the DC voltage converter with high power efficiency.

2.2.3.1 Review of Different DC Voltage Converters

The DC voltage converters are categorized into two topologies. One is linear conversion using the linear regulator. It can provide a low-noise and stable output

voltage with very simple structure, but of inefficiency when the voltage drop is large. The other topology is the switch mode conversion. This converts DC voltage by storing and releasing energy periodically [22]. Based on the energy storing component, the switch mode conversion can be classified as magnetic on the basis of inductor and capacitive if the energy is stored only in the capacitors.

2.2.3.2 Switched-capacitor DC-DC converter

Switched-capacitor (SC) DC-DC converter, which is also called charge pump, makes use of switches and energy-transfer capacitors to convert one DC level into another [23, 24]. It can be employed when various DC voltage levels are generated from a given DC power supply voltage. This kind of converter is simpler, cheaper and of reasonable efficiency when compared with other types of converter using inductor elements.

The generated voltage can be greater (step-up) or smaller (step-down) than the given DC voltage, depending on the circuit topology. The switches are periodically turned on and off so that the energy is transferred by charging and discharging the capacitors. To demonstrate how SC DC-DC converter works, two basic structures [25-27] are depicted in Figure 2.9 and Figure 2.10.

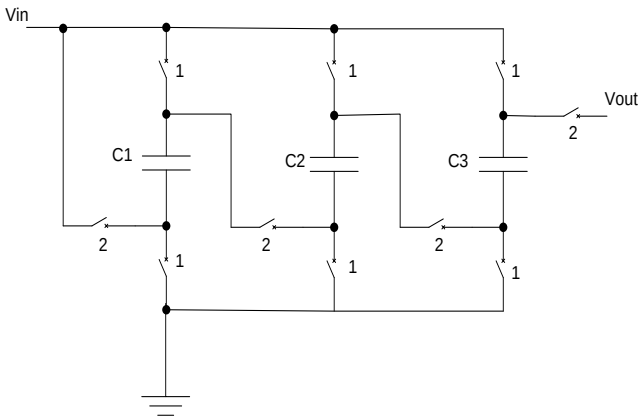


Figure 2.9 Basic structure of step-up switched-capacitor DC-DC converter (heap charge pump)

This DC-DC converter works in two phases. During phase 1, switch 1 is closed and switch 2 is open. Capacitors C1, C2 and C3 are charged in parallel. During phase 2, switch 1 is open whereas switch 2 is closed. Capacitors C1, C2 and C3 are connected in series to discharge to the output load. In the above circuit, an output voltage, which is four times of the input voltage, is generated.

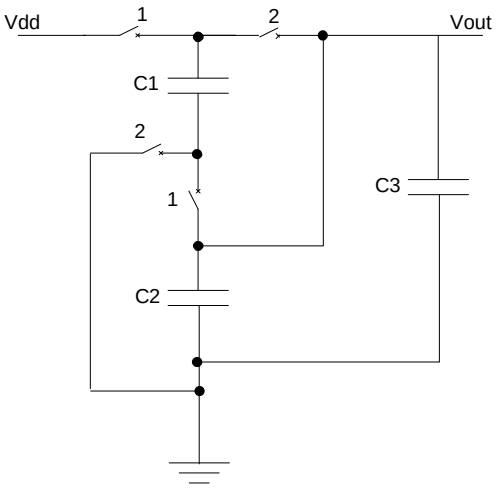


Figure 2.10 Basic structure of step-down switched-capacitor DC-DC converter.

This DC-DC converter works in two phases. During phase 1, switch 1 is closed and switch 2 is open. Capacitors C1 and C2 are charged in series by Vdd. Capacitor C3 discharge to the output load. During phase 2, switch 1 is open whereas switch 2 is closed. Capacitors C1, C2 and C3 are connected in parallel to discharge to the output load. In the above circuit, an output voltage, which is half of the input voltage, is generated. Hence, it is a step-down DC-DC converter.

2.2.3.3 Regulation Schemes

The input voltage of the DC-DC converter usually comes from a battery or rectifier circuit. In some applications, an additional regulator is needed to regulate the DC-DC converter and deliver a stable output voltage. There are mainly three different regulation schemes [28-30].

i) Pulse-Skip Regulation

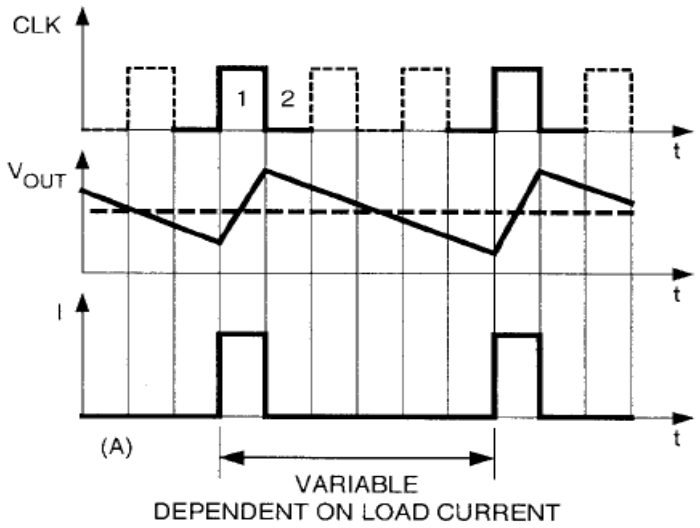


Figure 2.11 Pulse-skip Regulation

In the pulse-skip regulation scheme, the regulation of output voltage is achieved by skipping the unnecessary pulses. As depicted in Figure 2.11, when the output voltage is higher than a certain level, the SC DC-DC converter stops operating and skips the pulse to minimize the power consumption. Only until the output voltage decreases to a certain trigger level, the charge pump starts to operate and charge the output capacitor again to increase the output voltage. This regulation has high power efficiency but relatively higher output ripple. It has variable frequencies.

ii) Constant-Frequency Regulation

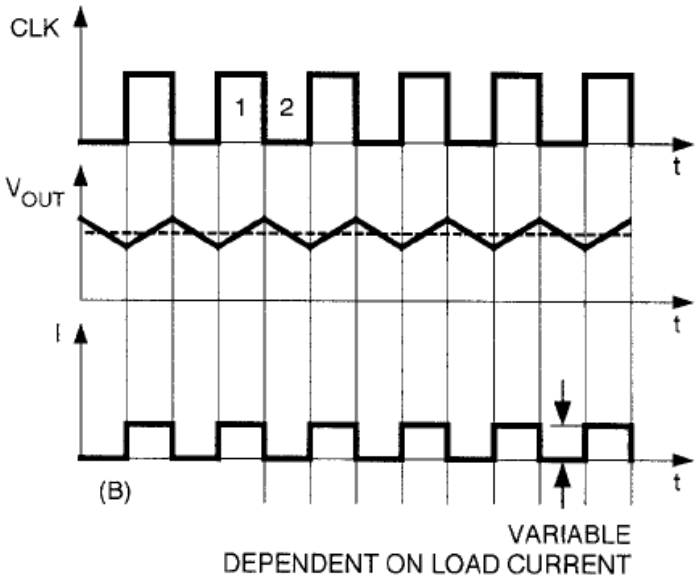


Figure 2.12 Constant-Frequency Regulation

Figure 2.12 depicts the constant-frequency regulation scheme. The SC DC-DC converter is under operation all the time. The output voltage is regulated by controlling the internal switches resistance. When the output voltage is too high, the

regulation circuitry will increase the resistance of the internal switches. Therefore, it decreases the charge that is transferred in each switching cycle. Although the regulation scheme has a low voltage ripple and fixed frequency, it suffers from low power efficiency.

iii) LinSkip Regulation

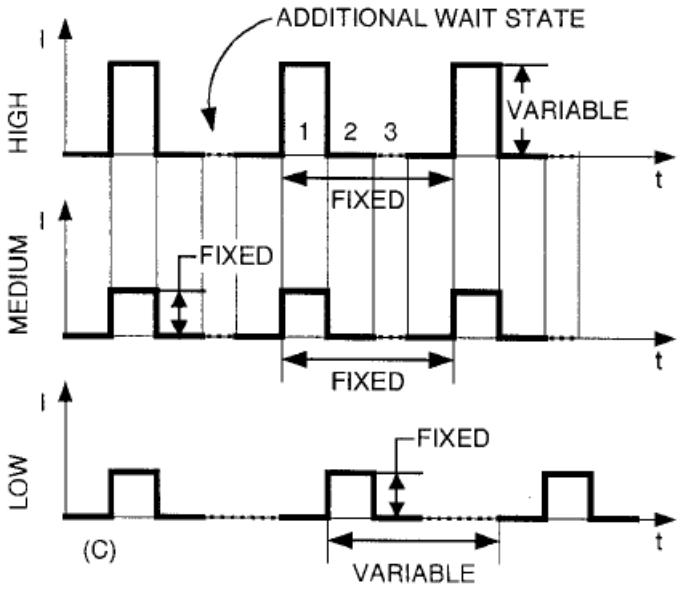


Figure 2.13 LinSkip Regulation

Figure 2.13 depicts the LinSkip regulation scheme. There are three phases called charge phase, transfer phase and wait phase. The regulation is achieved by controlling the current delivered to the output. When the output current demand is high, the charge transferred within each switching cycle is regulated, depending on the load current. When the output current demand is low, the current transferred is fixed and the wait phase increases its duration to reduce the output current. This

scheme has a low voltage ripple and high efficiency. However, the frequency is not fixed and the realization circuitry is complex.

Among all the structures mentioned above, a switched-capacitor DC-DC converter with pulse-skip regulation is most desirable for a Class G amplifier application under uni-polar power supply on the basis of its simple structure, low cost as well as reasonable power efficiency.

2.2.4 Switched-supply Amplifier Unit

The switched-supply amplifier unit comprises the core Class AB amplifier and the switch control circuit which realizes the transition between the two supply rails.

2.2.4.1 Core Amplifier

The switched-supply amplifier unit adopts the Class AB amplifier as its core amplifier because of its high linearity. The amplifier configurations can be divided into two topologies, single amplifier and bridge amplifier [31, 32]. In general, single amplifier is simpler. However, the bridge amplifier exhibits better power efficiency. It can produce a higher output power in audio application.

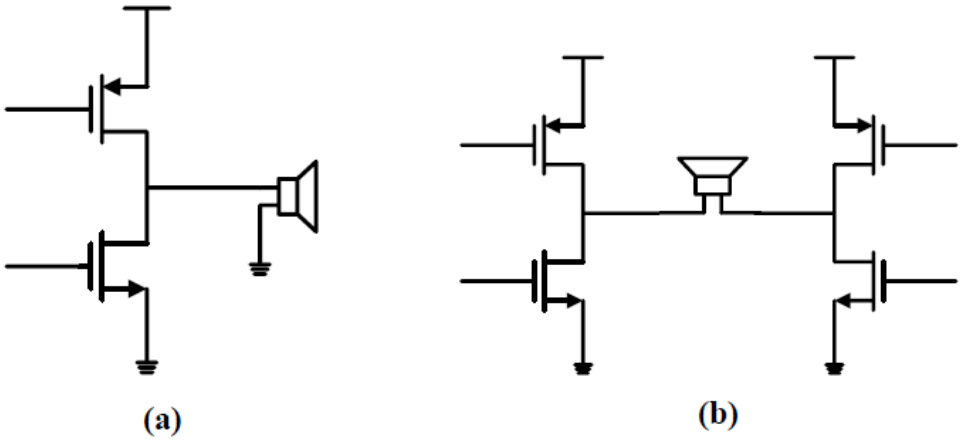


Figure 2.14 (a) Single amplifier (b) Bridge amplifier

Figure 2.14 depicts the simplified configurations of single amplifier and bridge amplifier. Although the bridge amplifier configuration has twice the components when compared with single amplifier counterpart, its differential structure can cancel the even order harmonic distortion components. Therefore, it has the technical merit of an improved linearity. In addition, the bridge amplifier fixes the DC operating voltage to half the power supply voltage because of its symmetric structure. Thus, the big DC decoupling capacitor is eliminated. Besides, the amplification of bridge amplifier is twice that of the single amplifier for the same power supply. With these benefits, the bridge amplifier configuration is popular for usage in audio applications.

2.2.4.2 Switching Control Circuit

In order for the Class G amplifier to achieve high linearity, other than a highly linear Class AB amplifier, the transition between the two supply rails is also critical. This is

controlled by the switch control circuit of the amplifier. It can be implemented in different ways.

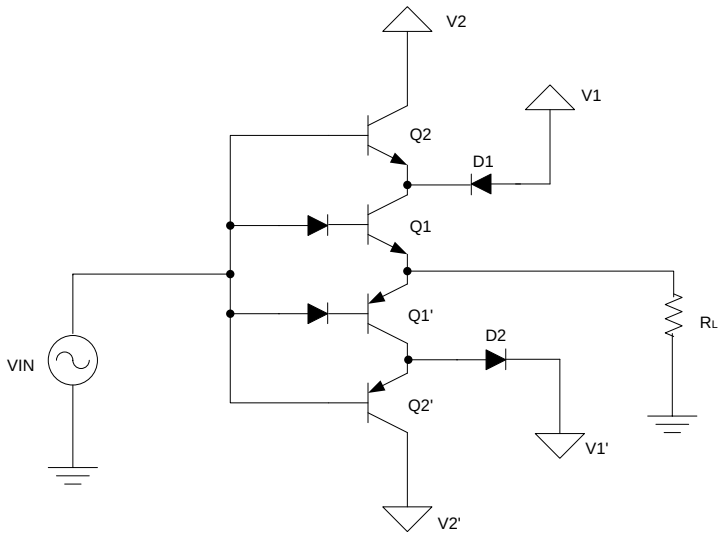


Figure 2.15 Basic configuration of Class G amplifier using diodes as control unit

The conventional Class G amplifier which uses diodes as switching control unit is depicted in Figure 2.15 [33, 34]. This configuration contains two pairs of complementary output transistors. V2 is the high voltage supply connected to the collector of Q2, while V1 is the low voltage supply connected to the collector of Q1 through a diode. As long as the input voltage VIN is smaller than V1, the transistor Q2 is cut off. When VIN exceeds V1, Q2 is turned on and current is supplied from V2. Meanwhile, the diode D1 is reversely biased. Consequently, it cuts off the current from V1.

In this configuration, four diodes are employed. This consumes large chip area. Therefore, several configurations are developed to reduce the number of diodes.

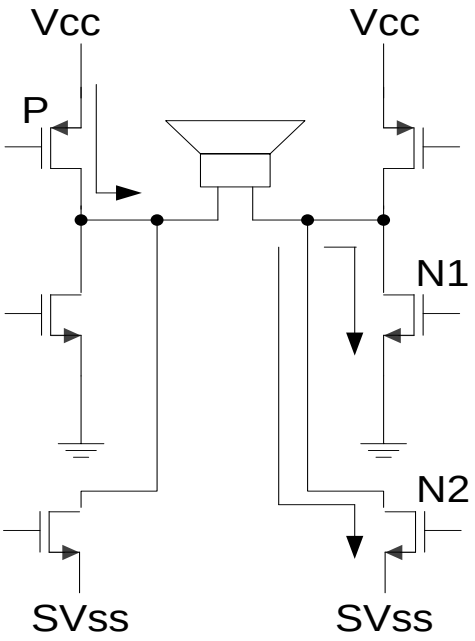


Figure 2.16 Basic configuration of Class G amplifier without diodes

Figure 2.16 depicts a bridge-tied-load Class G amplifier output stage [35]. It has two supply ranges. The low supply ranges from Vcc to GND whereas the high supply ranges from Vcc to SVss. For small signals, the device operates within low supply range. As the signal increases, the device starts to switch to the high supply range. To ensure a seamless transition, both transistors N1 and N2 are operating at the same time. As the signal continues to increase, N1 turns off while N2 remains on. The whole transition completes without creating discontinuous operation. Although the diodes are eliminated, six power transistors are needed to build up a bridge output stage.

After reviewing the related topologies, the focus of this project will be on Class G amplifier due to its good potential for portable audio applications. A switched-capacitor DC-DC converter with pulse-skip regulation will be employed on basis of its simple and power efficient structure. Finally, a new switching control circuit is developed to achieve a seamless transition.

CHAPTER 3

PROPOSED CLASS G AMPLIFIER

Class G amplifier is attractive because of its high power efficiency in the range where the output signal is less than half of the full swing while maintaining a relatively simple configuration. It is especially desirable for high crest factor audio applications in which the signal is less than 20% of the peak value most of the time. However, the existing Class G amplifier designs still have the disadvantages. These include bipolar power supplies [36-39] which introduce the inconvenience of supply system, triple-well process [36,37,39,41] which leads to high cost process and external inductor [42,43] that is both bulky and costly. A new Class G amplifier design is proposed to relax these constrains.

In this chapter, the overall architecture of the proposed Class G power amplifier is introduced. This is then followed by detailed discussion of each block in terms of circuit configuration, operation and advantages.

3.1 Architecture of Class G Power Amplifier

Class G power amplifier has a similar structure with Class AB amplifier except for the difference in the multiple power supply system. Class G power amplifier improves Class AB amplifier architecture by using two or more supply rails with

different voltage values. To demonstrate how the multiple power supply system operates, a dual supply system is considered. The low-voltage power supply is firstly used to reduce the power consumption when the output voltage is small. As long as it increases to a predetermined threshold voltage, the high-voltage power supply is switched in as required to allow the output voltage to continue increasing without clipping. In that case, the power efficiency can be optimized due to the signal-dependent dynamic selection of the appropriate power supply rail.

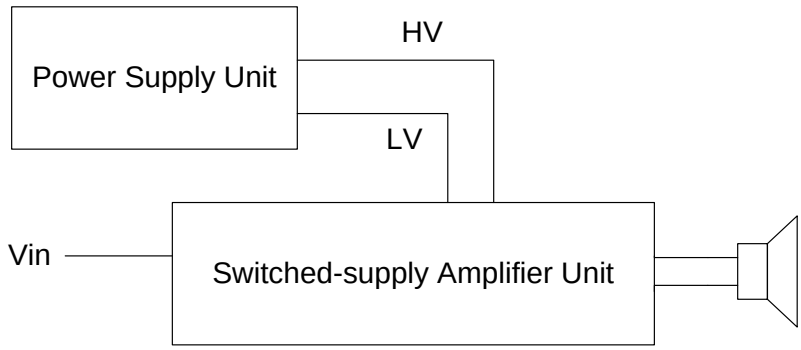


Figure 3.1 Simplified block diagram of Class G amplifier

As depicted in Figure 3.1, the whole Class G power amplifier consists of two parts which are described as follows:

1. Power supply unit

The power supply unit provides the supply rails to the output stage of amplifier. Two separate supply rails are available. The low-voltage supply rail (LV) is

generated by the internal DC-DC converter whereas the high-voltage supply rail (HV) is obtained from the external power supply.

2. Switched-supply amplifier unit

The switched-supply amplifier unit employs a bridge-tied-load (BTL) output configuration to amplify the audio input signal. The loudspeaker is connected between the two amplifier outputs. A supply control circuit monitors the input voltage level and selects the suitable supply rail. A DC control circuit generates a DC operating voltage based on the instantaneous supply rail voltage. The preamplifier operates with the DC control circuit and a voltage reference circuit. Based on the original DC offset of the input signal, it generates appropriate DC operating voltage according to the supply rail.

The overall block diagram of the proposed Class G amplifier is displayed in Figure 3.2. The detail of the subsystem as well as the individual block will be described in the next sections.

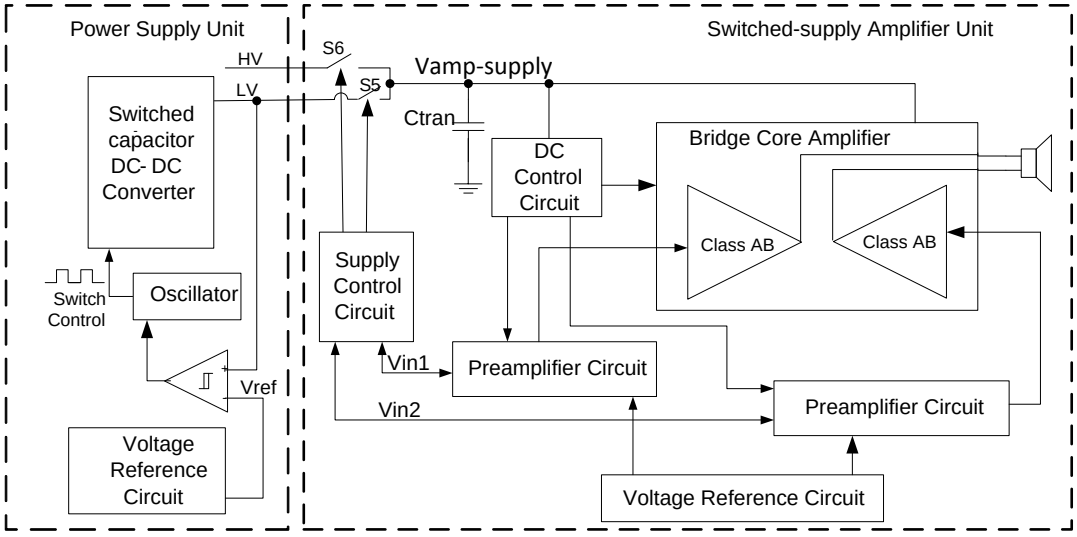


Figure 3.2 Overall block diagram of the proposed Class G amplifier

3.2 Power Supply Unit

As depicted in Figure 3.3, the power supply unit consists of a switched-capacitor (SC) DC-DC step down converter using pulse-skip regulation scheme. The regulation scheme is realized using a hysteresis comparator, a ring oscillator and a high Power Supply Rejection (PSR) voltage reference. Two supply rails are provided by the power supply unit. The low-voltage supply rail (LV) is generated by the DC-DC converter whereas the high-voltage supply rail (HV) is obtained from the direct external power supply. The low-voltage supply rail LV, which is used by the switched-supply amplifier unit when the input amplitude is small, is regulated by the pulse-skip regulation to improve the power efficiency of the DC-DC converter and the overall Class G amplifier.

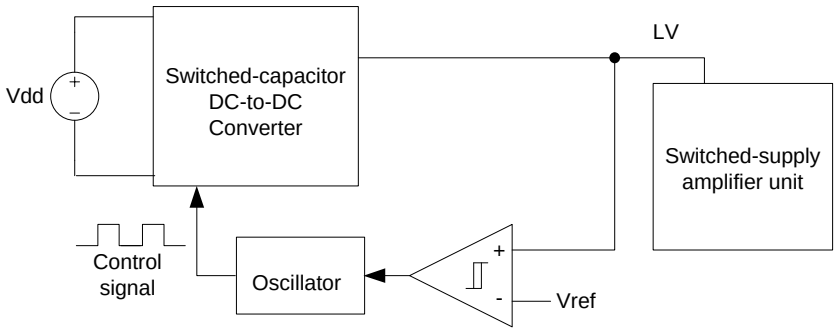


Figure 3.3 Block diagram of the power converter system

3.2.1 Switched-capacitor (SC) DC-to-DC Converter

Since the audio signal operates in the range of less than 20% of the full swing most of the time, a 1/2 step down conversion charge pump configuration is employed in this Class G amplifier. With the output voltage being half of the power supply, it provides enough headroom for the main operation range. In addition, when compared with the step down charge pumps having other conversion ratios such as 1/3 or 2/3, the 1/2 step down charge pump is smaller in terms of the reduced number of external components.

The configuration of the SC DC-to-DC step down converter is shown in Figure 3.4 [44]. It comprises two capacitors and four switches. C1 is the flying capacitor which transfers the charge from the power supply to C2. C2 is the driving capacitor which provides the driving current to the switched-supply amplifier. The generated low-voltage supply rail is labeled as LV. C1=C2=1μF.

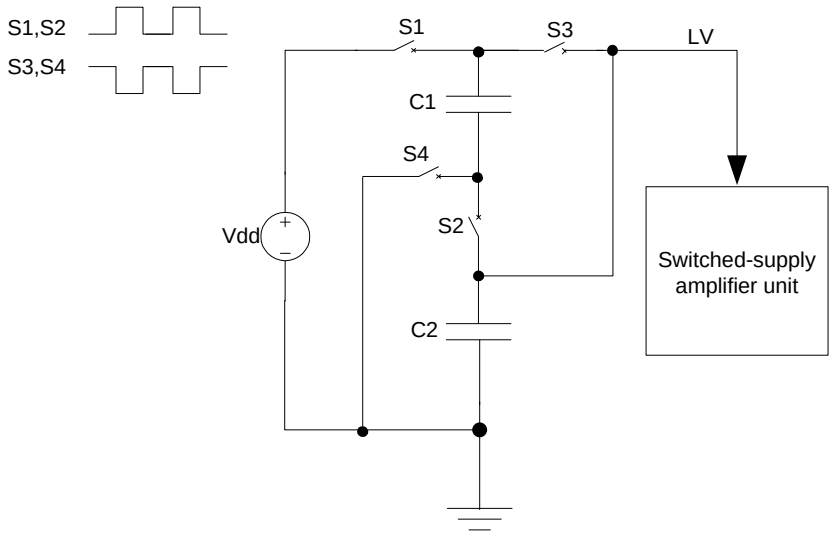
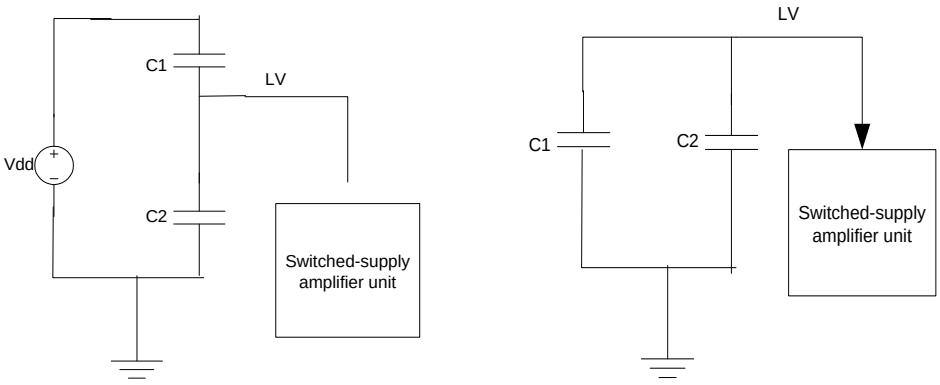


Figure 3.4 Configuration of the SC DC-to-DC step down converter

The typical operation of SC DC-to-DC converter is separated into two phases as illustrated in Figure 3.5. In phase 1, switches S1 and S2 are turned on while S3 and S4 are turned off. The capacitors C1 and C2 are connected in series with the external power supply. The power supply delivers charges into C1 and C2 whilst providing current to the switched-supply amplifier unit simultaneously. In phase 2, S1 and S2 are turned off whereas S3 and S4 are turned on. C1 and C2 are connected in parallel. Both of them discharge the current to the switched-supply amplifier unit. The phases are periodically repeated.



(a) (b)

Figure 3.5 (a) Configuration of the DC-to-DC converter at phase 1

(b) Configuration of the DC-to-DC converter at phase 2

The DC-to-DC converter has a high switching frequency of several hundred kHz. The switching period is so small that at the steady state the driving current I_d, provided to the switched-supply amplifier within each switching cycle, can be considered as constant. In the ideal case, the output voltage ripple is ignored. Within one cycle, all the charge provided from the power supply is completely delivered into the switched-supply amplifier unit. The duty cycle of this converter is 0.5. The timing diagram is shown at Figure 3.6. Based on these assumptions, the power efficiency of this converter can be calculated as follows [45]:

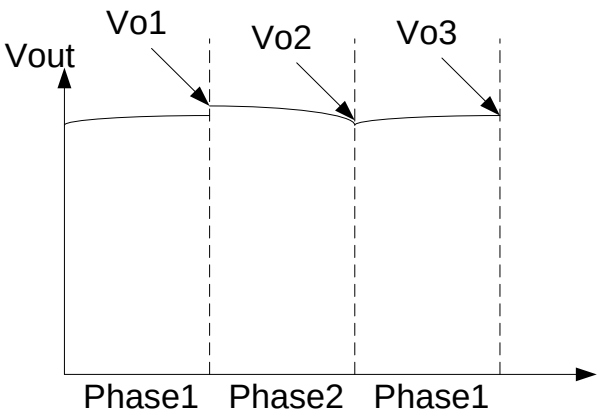


Figure 3.6 Timing diagram of DC-DC converter

- At phase 1, the power supply charges C1 and C2 whilst supplying the driving current to the switched-supply amplifier.

When a capacitor is charged or discharged, the current flowing through the capacitor is given as

$$i = C\frac{dv}{dt} \tag{3.1}$$

In phase 1 the total charge Q1 flowing into C1 can be obtained as

$$Q1 = C1 \bullet \Delta V_{C1} = C1 \bullet (Vdd - V_{O3} - V_{O2}) = \int_0^{\frac{T}{2}} i_s dt \tag{3.2}$$

where i_s is the instantaneous power supply current.

The net current flowing into C2 is obtained from the difference between the power supply current and the load current. Therefore, the total charge Q2 flowing into C2 is obtained as

$$Q2 = C2 \bullet \Delta V_{C2} = C2 \bullet (V_{O3} - V_{O2}) = \int_0^{\frac{T}{2}} (i_s - i_d) dt = \int_0^{\frac{T}{2}} i_s dt - I_d \bullet \frac{T}{2} \tag{3.3}$$

- At the instant of phase 2, C1 is placed in parallel with C2 and redistributes charge with C2 and the output jumps from V_{O3} at the end of phase 1 to V_{O1} instantly. The corresponding KQL is:

$$C1 \bullet (Vdd - V_{O3}) + C2 \bullet V_{O3} = (C1 + C2) \bullet V_{O1} \tag{3.4}$$

In phase 2, the switched-supply amplifier drives current from both C1 and C2. V_{O1} decreases to V_{O2} at the end of phase 2.

$$(C1 + C2) \bullet (V_{O1} - V_{O2}) = I_d \bullet \frac{T}{2} \tag{3.5}$$

Substituting (3.2), (3.3), (3.4) into (3.5), it is obtained as

$$C1 \bullet (Vdd - V_{O3} - V_{O2}) = I_d \bullet \frac{T}{2} \tag{3.6}$$

Since the power supply only provides current for half of the cycle in the DC-to-DC converter, the average current provided by the power supply I_S is

$$I_S = \frac{\int_0^{\frac{T}{2}} i_s dt}{T} = \frac{C1 \bullet \Delta V_{C1}}{T} = \frac{I_d}{2} \tag{3.7}$$

The efficiency of power amplifier can be expressed as

$$\eta = \frac{\text{power delivered to the load}}{\text{power supply } V_{DD} \times \text{Average current provided by } V_{DD}} \tag{3.8}$$

From eqn (3.7), it is noted that the average current provided by the power supply is only half of the average current delivered to the load in each switching cycle. Therefore, for the same driving condition, the power efficiency of the Class G amplifier is theoretically doubled when the low-voltage supply rail generated by this

1/2 step-down DC-to-DC converter is used. This is compared with that of normal Class AB amplifier. In order to minimize the charge redistribution loss, MOSFET switches with high aspect ratios of 10000µm/0.35µm.are used in this converter.

3.2.2 Pulse-skip Regulation

The pulse-skip regulation is one of the most popular architectures used today. The simplicity of the design allows for both high efficiency and high accuracy while maintaining relatively small area. Therefore, this design employs the pulse-skip regulation scheme to regulate the output voltage of DC-to-DC converter. The block diagram of the regulation configuration is depicted in Figure 3.7. The switches in the DC-to-DC converter are controlled by a ring oscillator. The output voltage LV is compared with a high PSR reference voltage denoted as Vref in a hysteresis comparator. When LV is less than a certain internal set level, the comparator activates the oscillator so that the power supply can charge the output capacitor. Once LV is higher than a desired level, the output of the comparator will disable the oscillator. Therefore, the switching cycles are skipped and the switching loss is reduced.

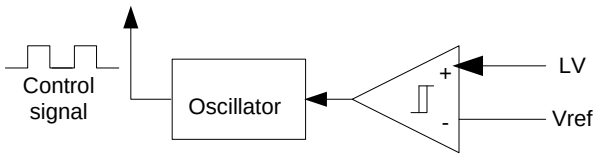


Figure 3.7 Block diagram of pulse-skip regulation

3.2.2.1 Ring Oscillator

The switching power loss is proportional to the switching frequency. It is given as follows:

$$P_{switch} = C \bullet V_s^2 \bullet f \tag{3.9}$$

where C is the capacitance value, V_s is the supply voltage and f is the switching frequency.

This formula shows that the switching frequency should be made low to avoid any switching power loss. However, if a DC-DC converter is designed with low switching frequency, it will exhibit a high ripple in the output voltage. This power supply noise will be easily coupled to the other analog blocks having a finite power supply rejection ratio (PSRR). Therefore, the optimum switching frequency is controlled to be several hundred kHz. In this design, the oscillator, as depicted in Figure 3.8, has an output signal having the frequency of 330 kHz. The ratio of the rain oscillator inverters is 1:1:4:25.

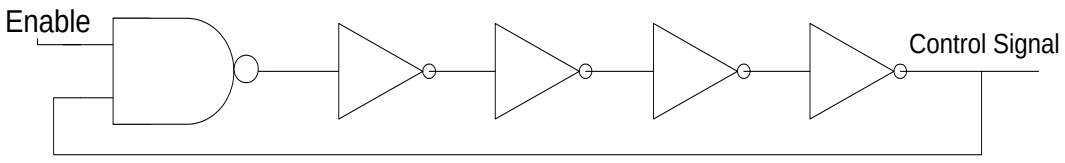


Figure 3.8 Schematic of the ring oscillator

3.2.2.2 Comparator

This project uses a typical comparator design [46, 47]. The comparator consists of three stages, a pre-amplification stage, a positive feedback decision stage and an output buffer. As depicted in Figure 3.9, M_{C1}-M_{C7} forms the pre-amplification stage. Not only does this stage amplify the input signal, it also isolates the input signal from any kickback noise coming from the positive feedback decision stage. The following positive feedback decision stage, which is consisted of M_{C8}, M_{C9}, M_{C10} and M_{C11}, is the heart of this comparator. The positive feedback from the cross-gate connection of M_{C8} and M_{C10} increases the stage gain. A small hysteresis of 10mV is designed to reject any noise on the signal. The detail calculation of hysteresis is shown in Appendix B. A NMOS transistor M_{C12} moves the output of decision stage into the common-mode input range of the output buffer. The output buffer uses a self-biased differential amplifier (M_{C13}-M_{C17}) to convert the output of decision stage into a logic signal. An inverter is added at the output to isolate the self-biased differential amplifier from any load capacitance. The transistor sizes are shown in Appendix E.

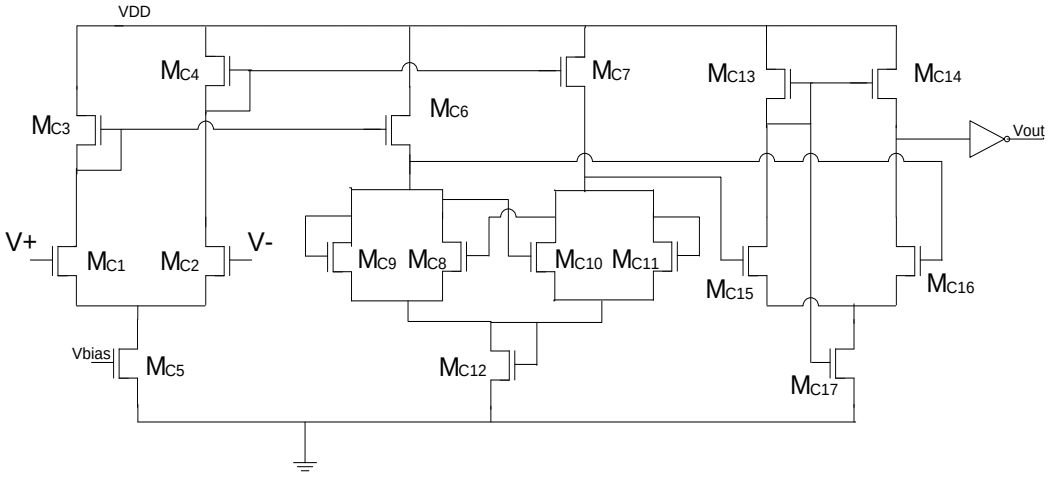


Figure 3.9 Schematic of the comparator

3.2.2.3 High PSR Voltage Reference

The switched-capacitor converter may have a large switching noise at the supply line under heavy loading condition. Thus, a voltage reference with high power supply rejection (PSR) is desired. In this project, a proposed high PSR voltage reference [48] design is based on pseudo-differential signal conditioning of a high-PSR based pseudo floating voltage source.

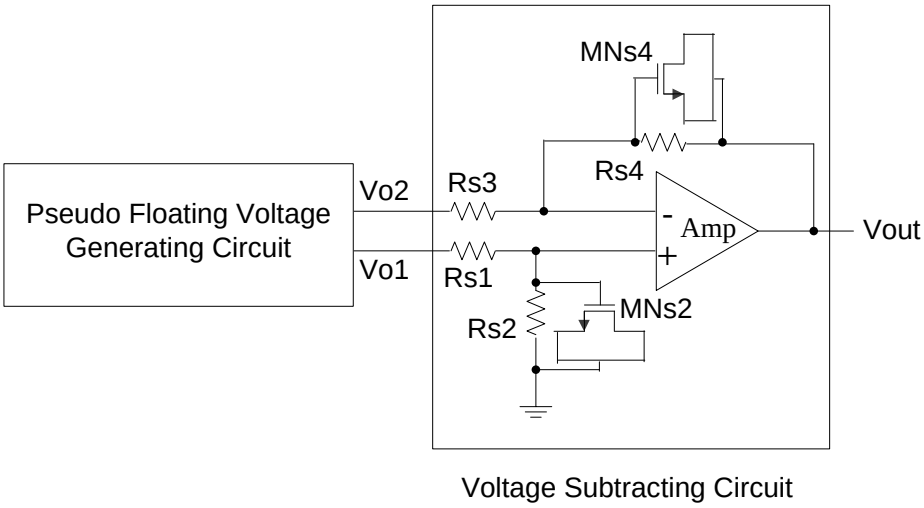


Figure 3.10 Proposed high-PSR pseudo-differential reference circuit architecture

Figure 3.10 depicts the voltage reference architecture. The circuit consists of two stages. The first stage is a pseudo floating voltage source having good immunity against supply noise for first level supply ripple rejection. The residual common-mode supply noise will be continuously rejected by the high-PSR difference amplifier in second level through voltage subtraction process. Besides, the second stage also serves as a first-order low-pass filer to suppress the high frequency components. As a result, high frequency noise will be significantly reduced through the cascaded structure.

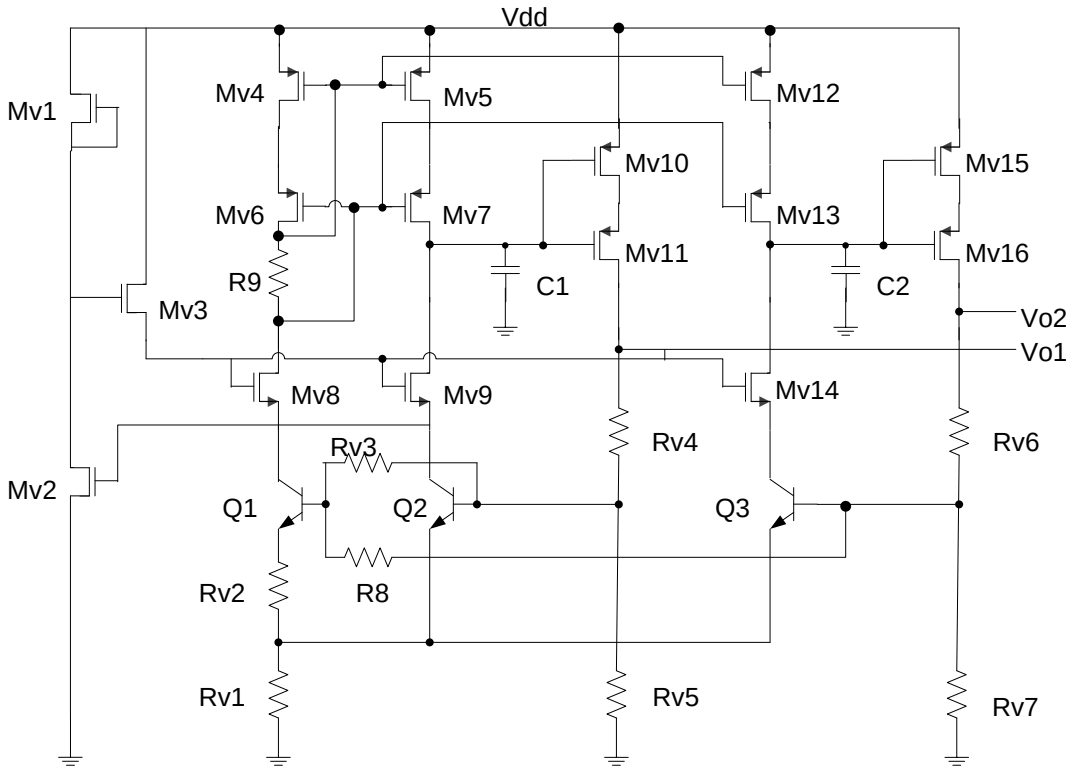


Figure 3.11 Schematic of the pseudo floating voltage generator

A pseudo floating voltage generating circuit, which is merged by two Brokaw's reference network, is shown in Fig. 3.11. The start-up circuit is formed by transistors

M_{V1}, M_{V2} and M_{V3} to pull the circuit out of the undesired stable state. When the starting up process has completed, the cascode transistors M_{V8}, M_{V9} and M_{V14} are now biased by the stable output of Vo1. M_{V3} will subsequently be turned off so that the start-up circuit is isolated from the core circuit. The core circuit comes from the BJT devices *Q1:Q2*=8:1, resistors R_{V1}=38.93kΩ, R_{V2}=11.4kΩ, current mirror transistors M_{V4} and M_{V5}, source follower consisting of M_{V11} and scaling resistors R_{V4}=15.89kΩ, R_{V5}=42.34kΩ. Merged design approach is employed by adding another simplified network of Brokaw's reference network with Q1:Q3=8:1, R_{V6}=12.71kΩ, R_{V7}=126.9kΩ [49]. The base current of a BJT is small compared with the emitter current. In order to achieve a high-performance reference voltage, the effect of the base current must be considered. The resistors R_{V3}= R_{V8}=3.385kΩ are introduced for base currents compensation. The detailed component values are shown in Appendix E.

The merged design has a big advantage in hardware resource with respect to the two independent sources method which generates the two reference voltages using two separated Brokaw's reference circuit. This pseudo floating voltage generating circuit generates two interim outputs Vo1=1.75V and Vo2=1.4V with the similar characteristic of the supply voltage variation.

Intuitively, the PSR transfer function can be simply viewed as a voltage divider caused by (i) the impedance between the power supply and the output and (ii) the impedance between the output and ground [4]. In this high-PSR circuit design perspective, the cascode devices such as M_{V6}, M_{V7}, M_{V8}, M_{V9}, M_{V13} and M_{V14} are added to increase the impedance between the supply and individual branch so as to minimize supply noise coupling to the output at the various circuit paths. Finally, *C1* and *C2* are compensation capacitors that improve high-frequency PSR [50].

The voltage subtracting circuit in Fig. 3.10 makes use of transistors MNS2 and MNS4 to form the MOS-based capacitors rather than using the metal-insulator-metal (MIM) capacitors. The size of 100pF MIM capacitor is 1000um x 98.79um, while the size of 100pF MOS-based capacitor is only 405um x 50um. Therefore, the replacement of the metal-insulator-metal (MIM) capacitors using MOS-based capacitors leads to a reduction of 4.88 times on the capacitor area. The output voltage is Fig 3.10 can be expressed as follows:

$$V_{out} = \frac{R_{S2}}{R_{S1}(1 + SR_{S2}C_{S2})}(V_{O1} - V_{O2}) \tag{3.10}$$

where R_{S1}=R_{S3}=35kΩ and R_{S2}=R_{S4}=155kΩ, Vo1 and Vo2 are the two interim outputs of pseudo floating voltage generator as labeled in Figure 3.11, C_{S2} and C_{S4} are the equivalent capacitance of the transistor capacitor M_{NS2} and M_{NS4}.

As can be seen, the final dc value can be scaled to the targeted value by setting the resistor pair ratio RS2/RS1 and RS4/RS3 whereas the filter bandwidth can be controlled by resistive components RS1, RS2, RS3, RS4 and/or capacitive components realized by size of transistors MNS2 and MNS4. The detailed calculation is shown in Appendix C.

3.3 Switched-Supply Amplifier Unit

The block diagram of switched-supply amplifier unit is depicted in Figure 3.12. As previously described, the switched-supply amplifier unit consists of a supply control circuit, a DC control circuit, a voltage reference circuit, a preamplifier circuit and a core bridge amplifier.

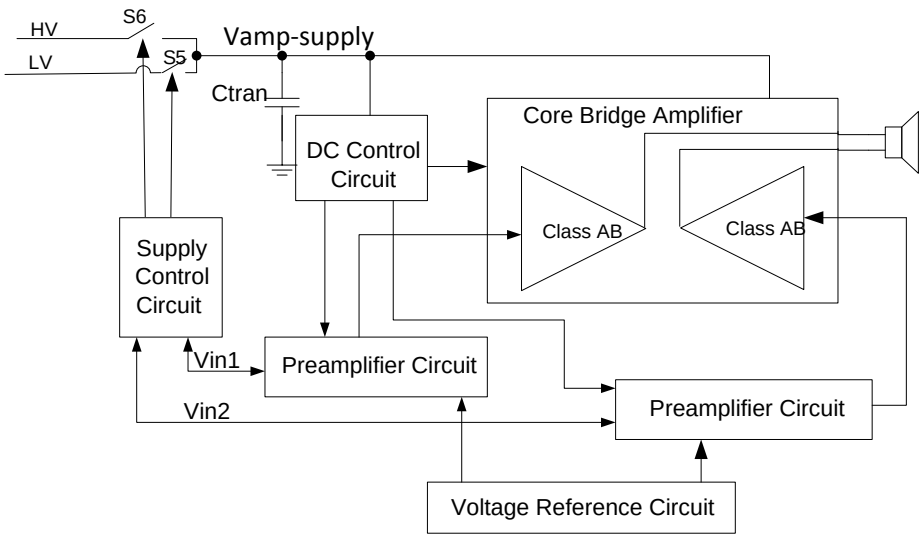


Figure 3.12 Block diagram of the switched-supply amplifier unit

In order to maximize the power efficiency, a supply control circuit is used to detect the input voltage and select the suitable supply rail. The DC operating voltage of an

amplifier is usually set to be half of the supply voltage. This ensures that the amplifier can generate a full swing output and deliver the largest output power. However, in Class G amplifier, there are two different operating supply rail voltages. Therefore, the DC operating voltage should be adjusted according to the instantaneous supply rail voltage. This is done by the DC control circuit in the architecture. However, the input audio signal consists of an AC signal as well as the DC offset. Hence, instead of using an external capacitor, a preamplifier with offset conditioning is proposed to adjust the DC offset for appropriate DC operating voltage to maximize the operation headroom.

The waveform of output signal as well as the output stage power supply is shown in Figure 3.13. The power supply switches from LV to HV when the output amplitude increases while the DC operating voltage also shifts accordingly.

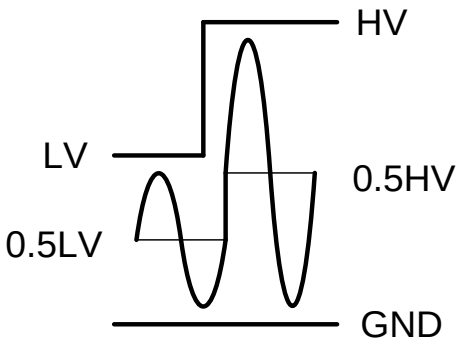


Figure 3.13 Waveform of output signal at different power supply rails

3.3.1 Supply Control Circuit

The power efficiency in Class G amplifier is improved by optimizing the power supply according to the instantaneous input voltage. As mentioned in section 3.2, a dual supply rail is provided by the power supply unit: the low-voltage supply rail (LV) and the high-voltage supply rail (HV). With the purpose of maximizing the power efficiency while maintaining a high linearity of Class G amplifier, a novel Supply Control Circuit is designed to provide the power supply of the amplifier output stage (Vamp-supply) for a proper selection between these two supply rails (LV and HV).

The final output signal, which is the voltage difference between the loudspeaker terminals, is a faithful multiple replica of the input signal. However, the interim output at each terminal is distorted due to the change of DC operating level. Therefore, instead of selecting the supply by monitoring the output signal via diodes [33], the proposed supply control circuit detects the input signal to control the operation of supply rails. This is considered the major difference between the proposed scheme and the prior-art work [33].

This Class G amplifier amplifies a pair of differential input signal via a bridge amplifier configuration. The bridge amplifier shares the same power supply (Vamp-supply) for the two output stages. In order to maximize the power efficiency while maintaining a high linearity of Class G amplifier, the output stage power

supply (Vamp-supply) always does the selection based on the input with higher instantaneous value as illustrated in Figure 3.14.

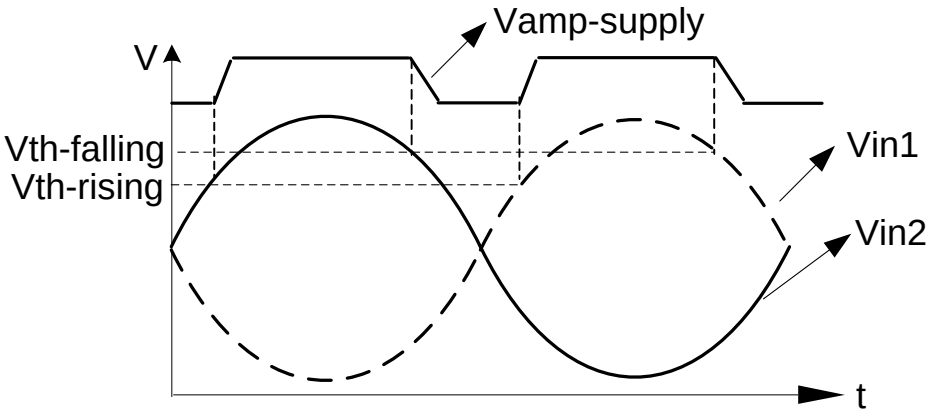


Figure 3.14 Transient response of Vin1, Vin2 and Vamp-supply

The low-voltage supply rail LV is selected when the input level is small. In the rising part of input signal, as long as it reaches a predetermined threshold voltage, labeled as Vth-rising, the high-voltage supply rail HV is switched as required. This allows the final output signal to continue increasing without clipping. Similarly in the falling part, once the input voltage drops below another predetermined voltage Vth-falling, the supply of output stage Vamp-supply switches back to low-voltage supply rail LV to minimize the power loss. The optimum trigger point of the transition occurs where the output voltage is somewhat below the supply voltage just before clipping. Thus, the rising threshold voltage Vth-rising is less than the falling threshold voltage Vth-falling.

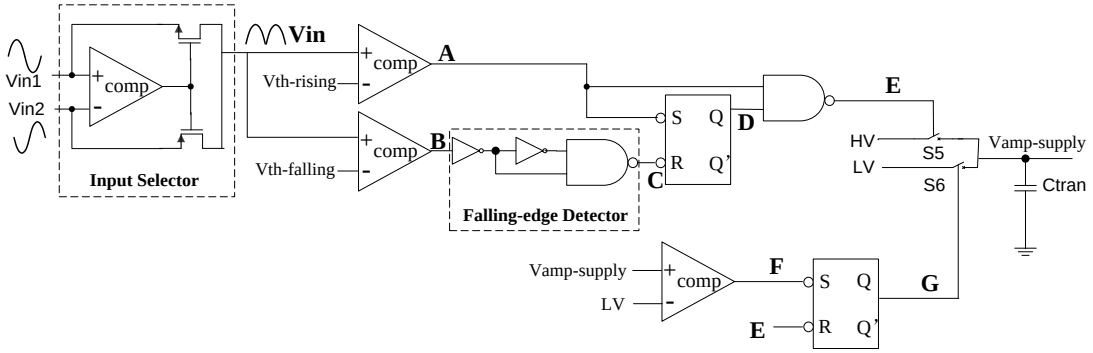


Figure 3.15 Block diagram of Supply Control Circuit

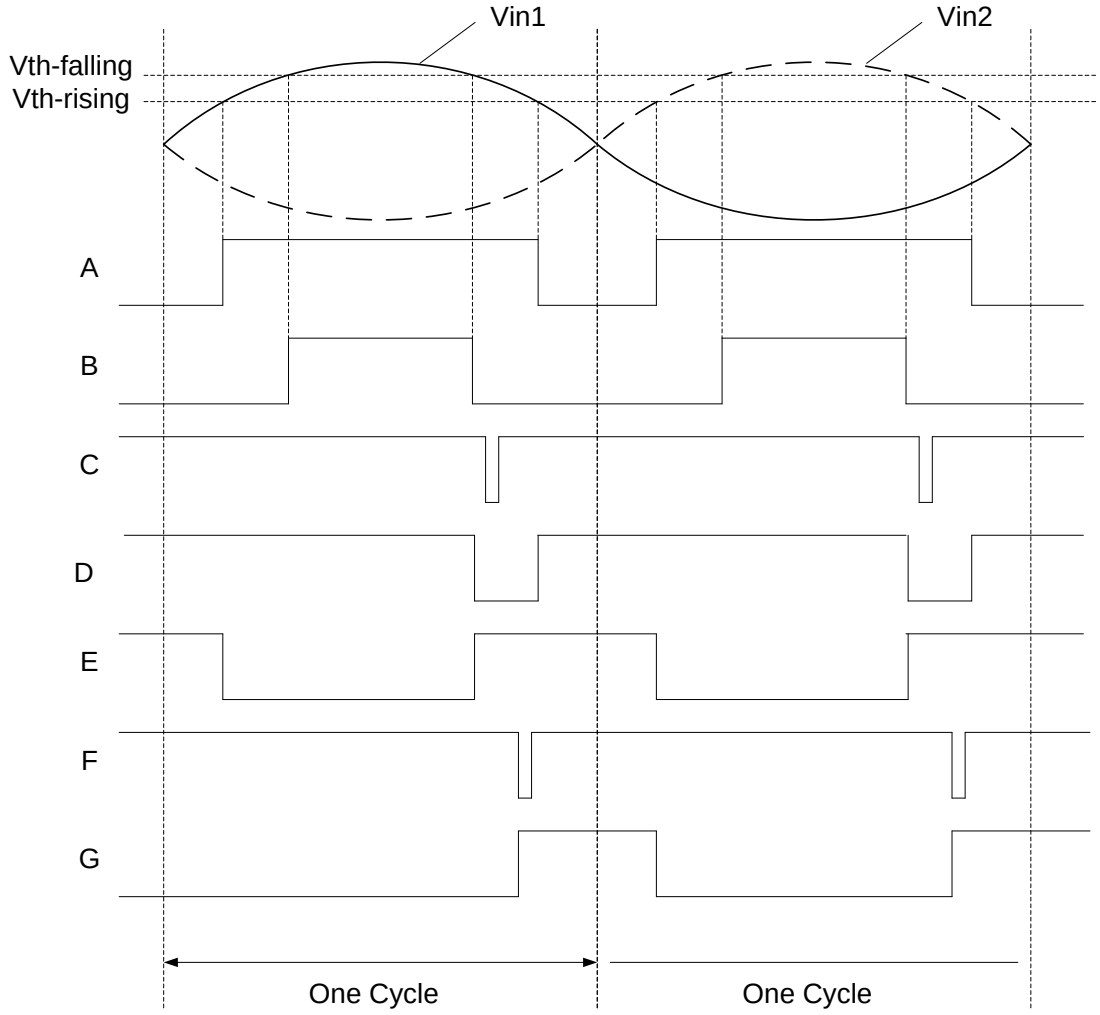


Figure 3.16 Timing diagram of each node

The block diagram of Supply Control Circuit is depicted in Figure 3.15. The input selector compares the two differential inputs and selects the input signal with higher

instantaneous voltage for further comparison with the threshold voltages Vth-rising and Vth-falling. As shown in Figure 3.16, A='1' indicates that Vin ≥Vth-rising while B='1' indicates that Vin≥ Vth -falling. The Falling-edge detector circuit detects the falling-edge of node B signal. It generates a pulse signal at node C to indicate the moment that Vin drops below Vth-falling in the input signal falling part. A SR NAND-Gate Latch and a NAND Gate process the signals at node A and node C to control the selection of the high-voltage power supply HV at node E. The output stage supply Vamp-supply selects between the two supply rails HV and LV using two MOSFET switch transistors (S5 and S6) as switches. S5 is a PMOS transistor while S6 is a NMOS transistor. Therefore, HV is selected when E='0'. This indicates the period started from the point that Vin≥ Vth -rising in the input signal rising part to the point that Vin≤ Vth -falling in the input signal falling part. After S5 is open, S6 (LV select switch, NMOS) does not close until Vamp-supply falls less than LV (F='0'). Then, LV is selected until the point that Vamp-supply switches to HV again in the next cycle.

The speed of the transition needs to be controlled appropriately for avoiding any distortion due to the big spikes. A large capacitor Ctran=1μF is connected between Vamp-supply and ground to prevent any sudden change in the supply of output stage. In addition, this capacitor and switch S6 forms a low-pass filter. This filter functionally reduces the ripple as well as the switching noise of LV.

3.3.2 DC Control Circuit

The optimum DC operating level of an amplifier is usually set to be half of power supply in order to achieve a maximum possible output swing. In this project, the power supply Vamp-supply switches between LV and HV. Therefore, the DC operating voltage Vdc-op should always be half of the instantaneous power supply value. A voltage divider which is formed by a buffer and two resistors with same value is used to realize this function. The configuration is depicted in Figure 3.17. R1=R2=40kΩ.

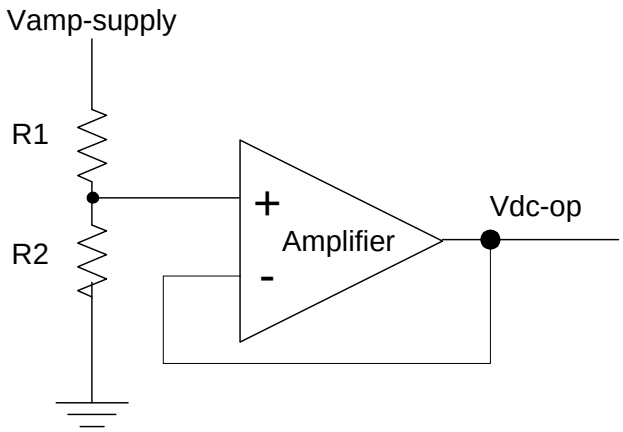


Figure 3.17 Configuration of the DC control circuit

3.3.3 Preamplifier

The input audio signal contains an AC signal as well as a DC offset. An inappropriate DC offset value consumes the headroom and prevents the output power from reaching the maximum possible value. In order to solve this problem, it is known that a conventional amplifier uses a big AC coupling capacitor to separate different DC offset for operation between the interface. In this project, as discussed in section

3.3.2, the optimum DC operating voltage is not constant but switching between two DC values, shown in Figure 3.18.

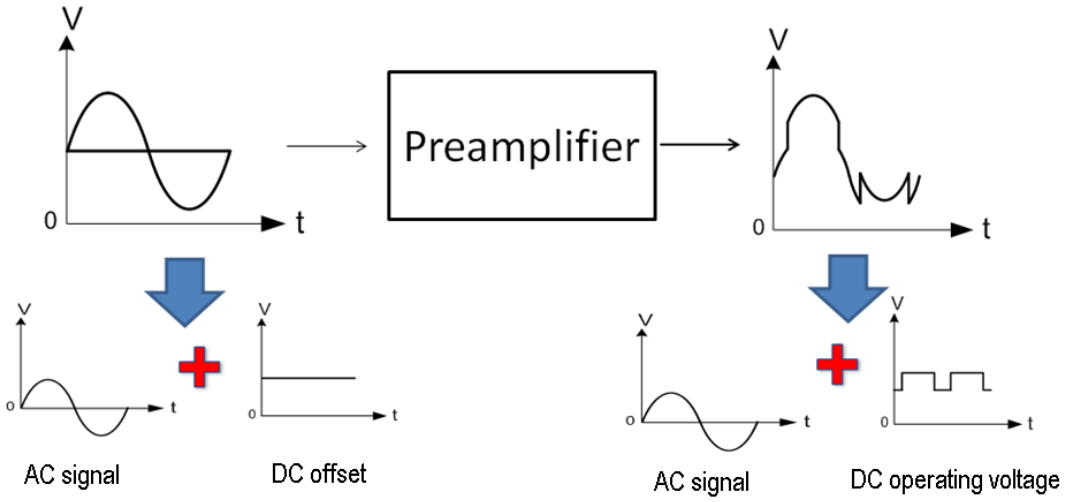


Figure 3.18 Pre-amplifier conceptual diagram

Therefore, rather than using a big AC coupling capacitor to adjust the DC offset like the conventional amplifiers [40], the preamplifiers are designed to adjust the DC offset of input signal for appropriate DC operating voltage through the use of DC control circuit. The configuration of preamplifier is depicted in Figure 3.19. It is a non-inverting gain configuration with the potential dividers for setting the quiescent operating voltage. The Vdc-offset, which represents the DC offset value of the audio input signal, is generated by a voltage reference circuit using the same configuration as described in section 3.2.2.3. In this project, two identical preamplifiers are used for the differential inputs in opposite phase.

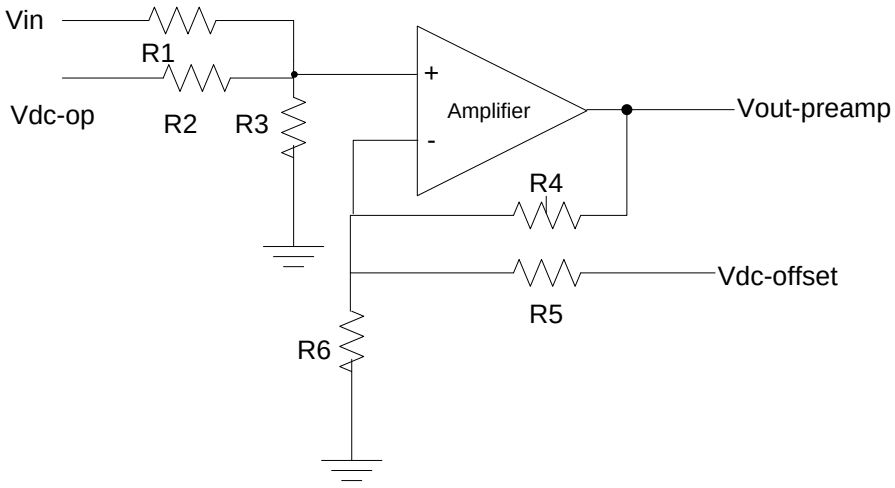


Figure 3.19 Configuration of preamplifier

The output expression of this configuration is obtained as

$$\text{Vout-preamp} = \text{Vin} - \text{Vdc-offset} + \text{Vdc-op} \tag{3.11}$$

where Vout-preamp is the output of preamplifier. Vin is the audio input signal. Vdc-offset is the DC offset value of the audio input signal. Vdc-op is the DC operating voltage generated by the DC control circuit. R1=R2=R3=200kΩ, R4=R5=R6=40kΩ

3.3.4 Core Bridge Amplifier

A common problem in portable audio application is on how to deliver more power to the loudspeaker with limited power supply voltage. The audio power amplifier solves this problem by using the common source transistors for output stage design so as to maximize the common-mode output range whenever possible. It can be further improved by means of the well-known bridge amplifier configuration. It is mainly

because a larger voltage across the load can be achieved through adding a second inverting amplifier with the load connected between the two outputs [31]. As a result, the maximum output voltage across the load is doubled when compared with that of a single-ended amplifier under the same power supply voltage. Hence, the power delivered, which is equal to the square of the voltage divided by the load impedance, is increased to four times. The basic configuration of bridge amplifier is depicted in Figure 3.20. Vo1 and Vo2 are the two preamplifier outputs which are in opposite phase. R1=R2=R3=R4=20kΩ.

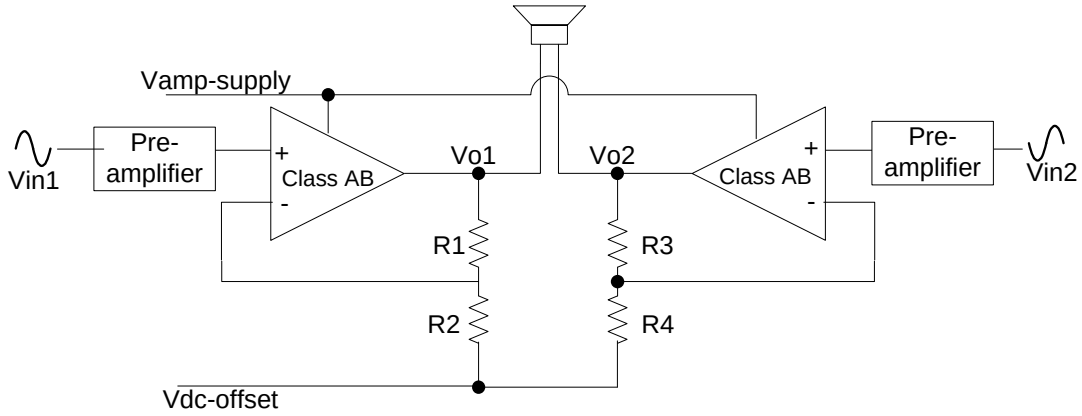


Figure 3.20 Basic configuration of the bridge amplifier

This bridge amplifier consists of two identical Class AB power amplifiers. The detailed schematic design of each amplifier is shown in Figure 3.21 [46]. It has two parts, the input stage with supply voltage labeled as VDD and the back-end stage with a different supply voltage labeled as Vamp-supply.

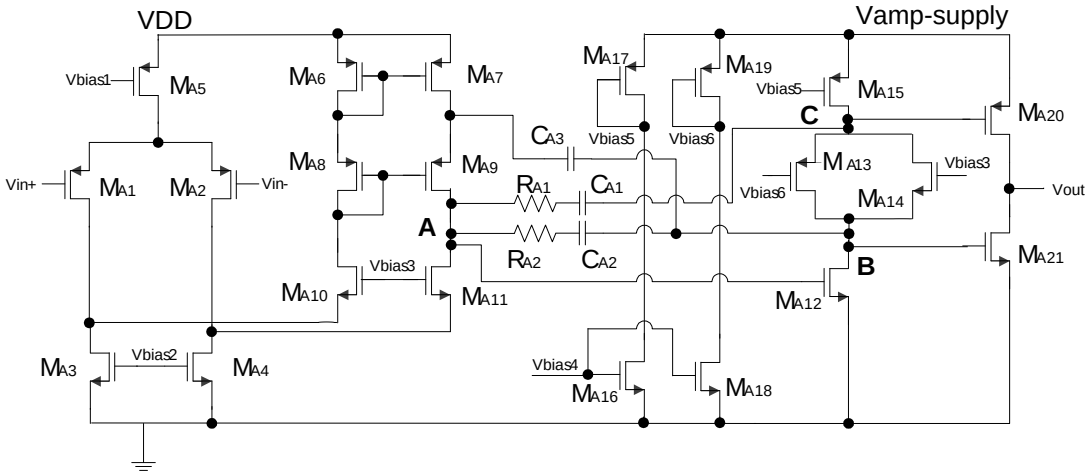


Figure 3.21 Schematic of the core amplifier

The input stage (M_{A1}-M_{A11}) employs folded-cascode configuration to obtain a high front-end stage gain. M_{A1}, M_{A2}, M_{A10} and M_{A11} form the folded-cascode structure. The current mirror (M_{A6}-M_{A9}) converts the voltage difference between the differential input terminals into a single-ended voltage at node A. M_{A3}-M_{A5} provide the biasing currents for the input stage. The input stage supply voltage (labeled as VDD) is powered to high-voltage supply rail for obtaining good input common-mode range whereas the back-end stage supply voltage (labeled as Vamp-supply) is switched between the high-voltage supply rail and low-voltage supply rail to reduce power loss.

The back-end stage consists of a gain stage (M_{A12} and M_{A15}) as well as the push-pull Class AB configuration output buffer (M_{A20} and M_{A21}). The Class AB control unit is comprised of a floating current source (M_{A13} and M_{A14}) with supply dependent

biasing circuit (M_{A16}-M_{A19}). The diode-connected transistor M_{A17} provides a bias voltage to M_{A15} which varies consistent with the supply voltage Vamp-supply. Therefore, although the output stage switches between the two supply rails, the Source-to-Gate voltage of M_{A15} is almost fixed, so it is with M_{A13} and M_{A20}. In principle, the quiescent current is almost constant under two supply conditions. However, it subjects to the non-ideal effect contributed by the channel length modulation.

To demonstrate how the floating current source controls the output buffer operation, a voltage increase at node A is considered. As it increases, the drain voltage of the common source transistor M_{A12} at node B decreases, thereby increasing the current to pass through M_{A14} which, in turn, reduces the current through M_{A13} or even turns it off completely. Subsequently, the voltage at node C, which is also the gate of PMOS output transistor M_{A20}, decreases. As a result, the output buffer sources more current to the load. Both the Miller and Cascode compensation are applied in this design [51, 52]. The transistor sizes are shown in Appendix E.

CHAPTER 4

SIMULATION RESULTS AND DISCUSSIONS

The Class G power amplifier has been realized using AMS 0.35μm CMOS process technology. It is verified by BSIM3 models. The simulation results are presented and discussed in this chapter.

4.1 Simulation Performance of Power Supply Unit

The limit to the Class G amplifier's power efficiency depends mainly on the efficiency of DC-DC converter in power supply unit. This part discusses the performance of power supply unit comprising the DC-DC converter and its closed-loop feedback regulation scheme. Figure 4.1 shows the block diagram of power converter system. Firstly, the simulation result of single DC-DC converter block without feedback regulation is shown. Secondly, the high PSR voltage reference is simulated. Lastly, the overall performance of DC-DC converter with closed-loop feedback regulation is shown.

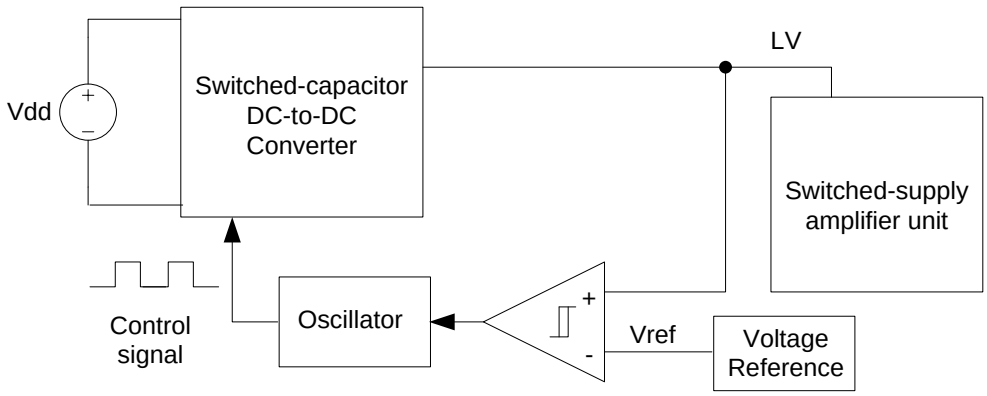
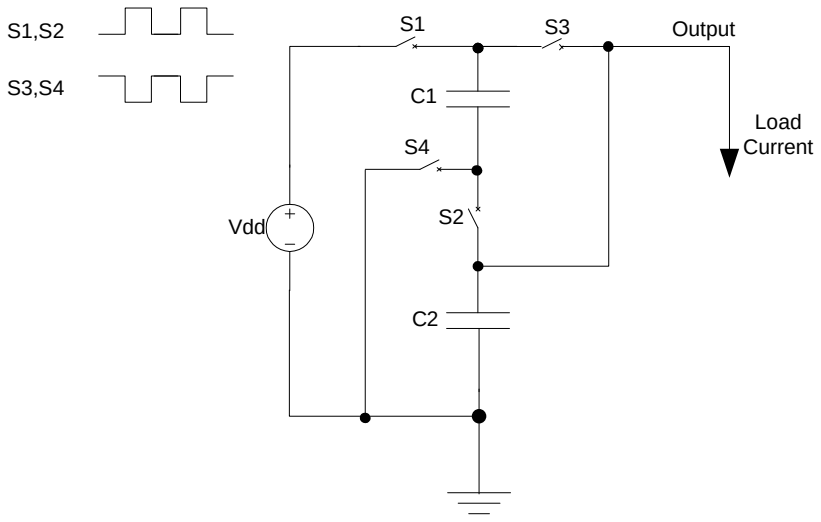


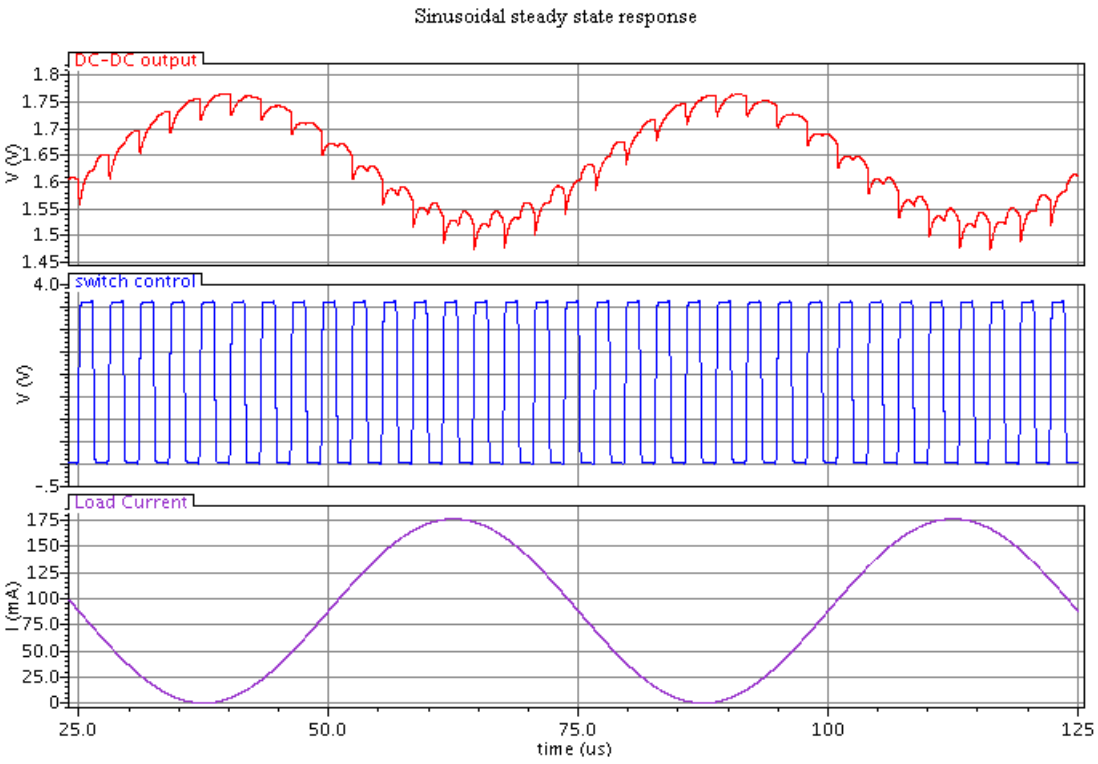
Figure 4.1 Block diagram of the power converter system

4.1.1 DC-DC Converter

The single DC-DC converter block converts the external power supply into an internal supply voltage with relative lower voltage so as to improve the power efficiency of the system for the range of small input signal. The proposed design employs a 1/2 step down DC-DC converter. However, the realistic output of DC-DC converter is slightly less than half of the power supply due to the conduction loss of switches. Thus, when driving an 8Ω loudspeaker, the peak current delivered from the DC-DC converter is approximately 175mA. Figure 4.2 shows the output voltage of DC-DC converter that delivers a sinusoid output current with peak-to-peak current of 175mA at a switching frequency of 330 kHz. By calculation, the average current flowing from the power supply is 68.2mA. This turns out that the power efficiency of this DC-DC converter is 71.96%.



(a)



(b)

Figure 4.2 (a) Configuration of DC-DC converter block

(b) DC-DC converter output and switch control signal

4.1.2 Bandgap Reference

The DC-DC converter exhibits a high switching noise. Thus, if it were integrated in the chip, there is a need to design a quality reference voltage independent of supply and temperature variations. In DC-DC converter operation, the voltage reference serves as a reference voltage for the feedback system.

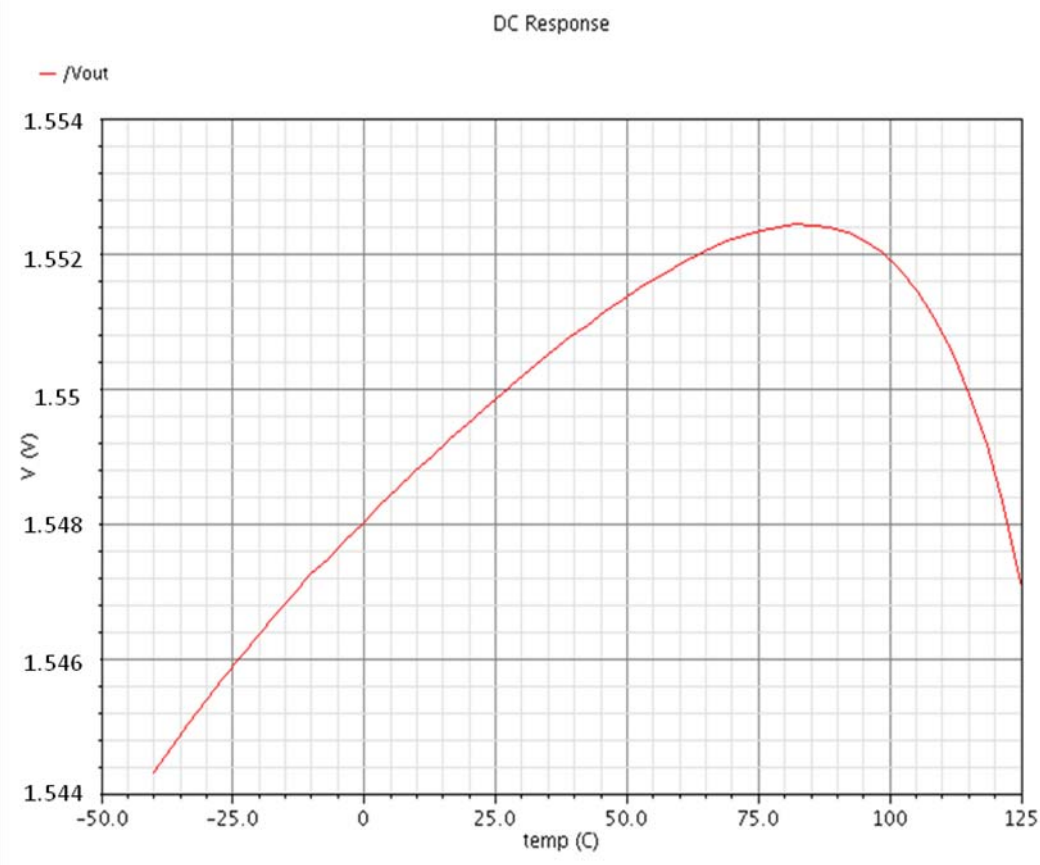


Figure 4.3 Voltage reference output voltage versus temperature

The most important performance metric of a reference voltage is that of stability in a range of temperature. In this project, the voltage reference is simulated over the temperature range from -40°C to 125°C. The result of the simulation is plotted in Figure 4.3. In typical case, the temperature coefficient is 25.2 ppm/°C. The

temperature coefficient employed for its calculation is given as [53]. It is defined as

$$TC = \left(\frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} * (T_{MAX} - T_{MIN})} \right) * 10^6 \quad (5.1)$$

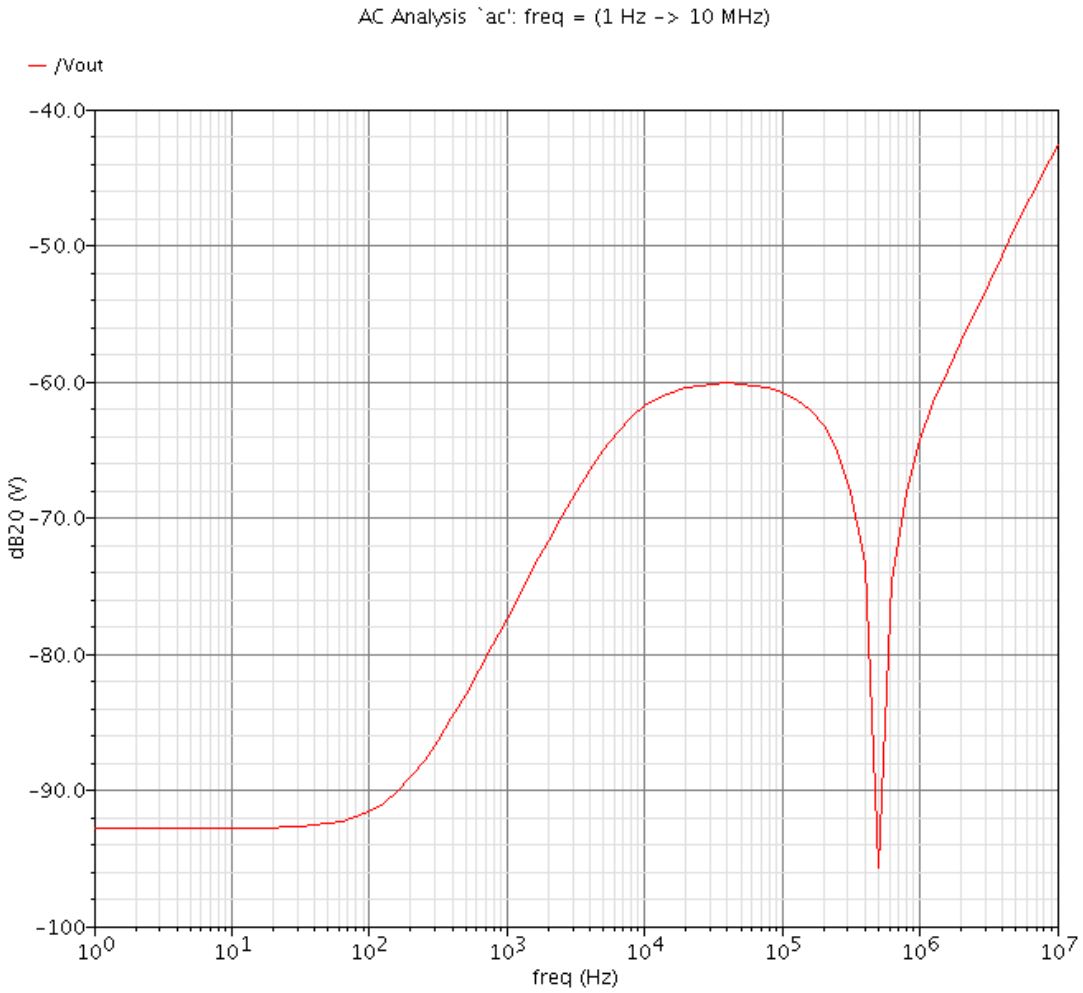


Figure 4.4 PSR of reference voltage

The simulated power supply rejection (PSR) result of the reference voltage is shown in Figure 4.4. The obtained PSR is -92.816dB at DC at low frequencies, -64.218dB at 1MHz and -42.575dB at 10MHz. This shows that the power supply noise at low frequency is significantly attenuated. At a frequency less than 1MHz, the output

variation due to power supply noise is less than -60dB, which is considered adequate for the DC-DC converter application.

4.1.3 DC-DC Converter Incorporating Regulation Scheme

Under the same load condition, the output voltage of DC-DC converter incorporates the regulation scheme as well as the switch control signal generated by the oscillator. The simulated result is depicted in Figure 4.5.

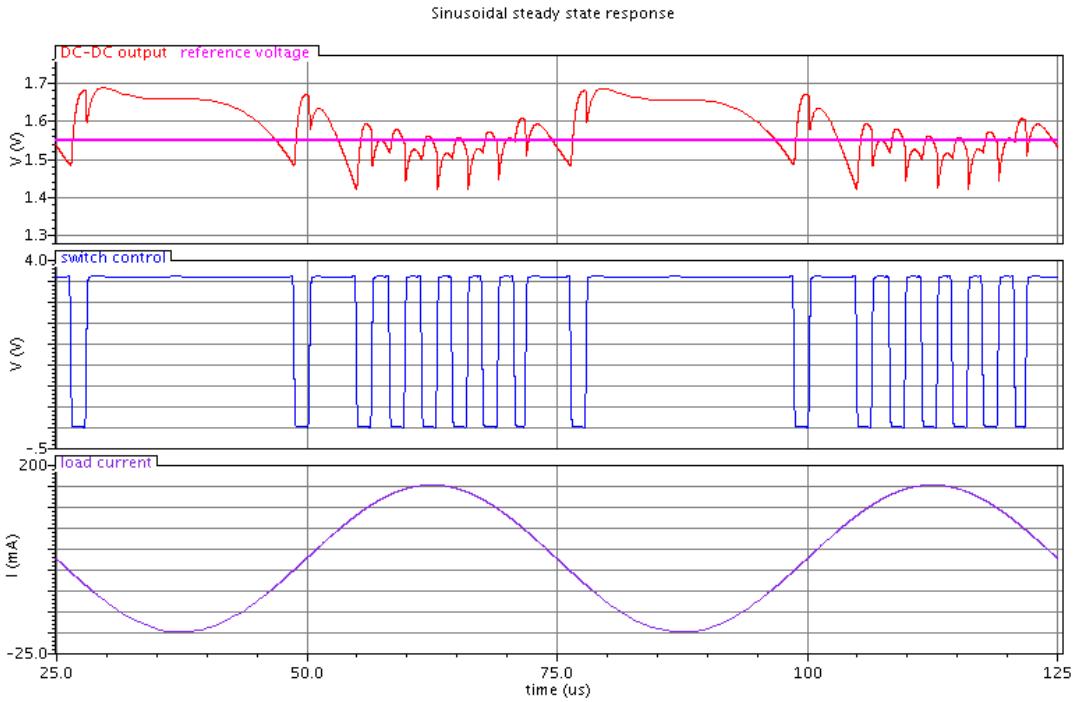


Figure 4.5 DC-DC regulated converter output and switch control signal

The reference voltage, as discussed in section 3.2.2.1 and 4.1.2, is 1.55V. When the output voltage is less than this reference voltage (48µs-77µs), the oscillator is activated to generate a switch control signal so that the power supply charges the output capacitor. When the output is higher than the reference voltage (27µs-48µs),

the switching cycles are skipped. Thus, the switching loss is reduced. Therefore, the efficiency is improved. As expected, the obtained power efficiency in the regulated DC-DC converter is 83.81%. It is higher than that of the unregulated counterpart. However, the ripple of the output voltage is larger (244mV). Although this ripple is big, it does not have a huge effect on the final output. That is due to (i) the employment of low-pass filter in the switched-supply amplifier unit which further minimizes this ripple and (ii) the use of high PSR of bridge amplifier.

4.2 Simulation Performance of Switched-supply Amplifier Unit

The main block in the switched-supply amplifier unit is the core bridge amplifier. The bridge amplifier configuration is formed by inverting the output of one amplifier via a second amplifier. The load is connected between the two outputs. The single amplifier performance will be discussed prior to that of the bridge amplifier.

4.2.1 Single Amplifier

In order to obtain a low total harmonic distortion (THD) output, the amplifier needs to be designed to have large open-loop gain as well as high bandwidth. The output stage of the amplifier has dual supply rails. The simulated performance of the single amplifier under each supply rail is discussed as follows:

- High-voltage supply rail

The frequency response of the amplifier under high-voltage supply rail with a sinusoidal input (Vp-p=200mV) is shown in Figure 4.6. It can be seen that the dc gain of this amplifier is 107.8dB. The phase margin of the amplifier is around 60.4° at the unity gain bandwidth of 20.3MHz.

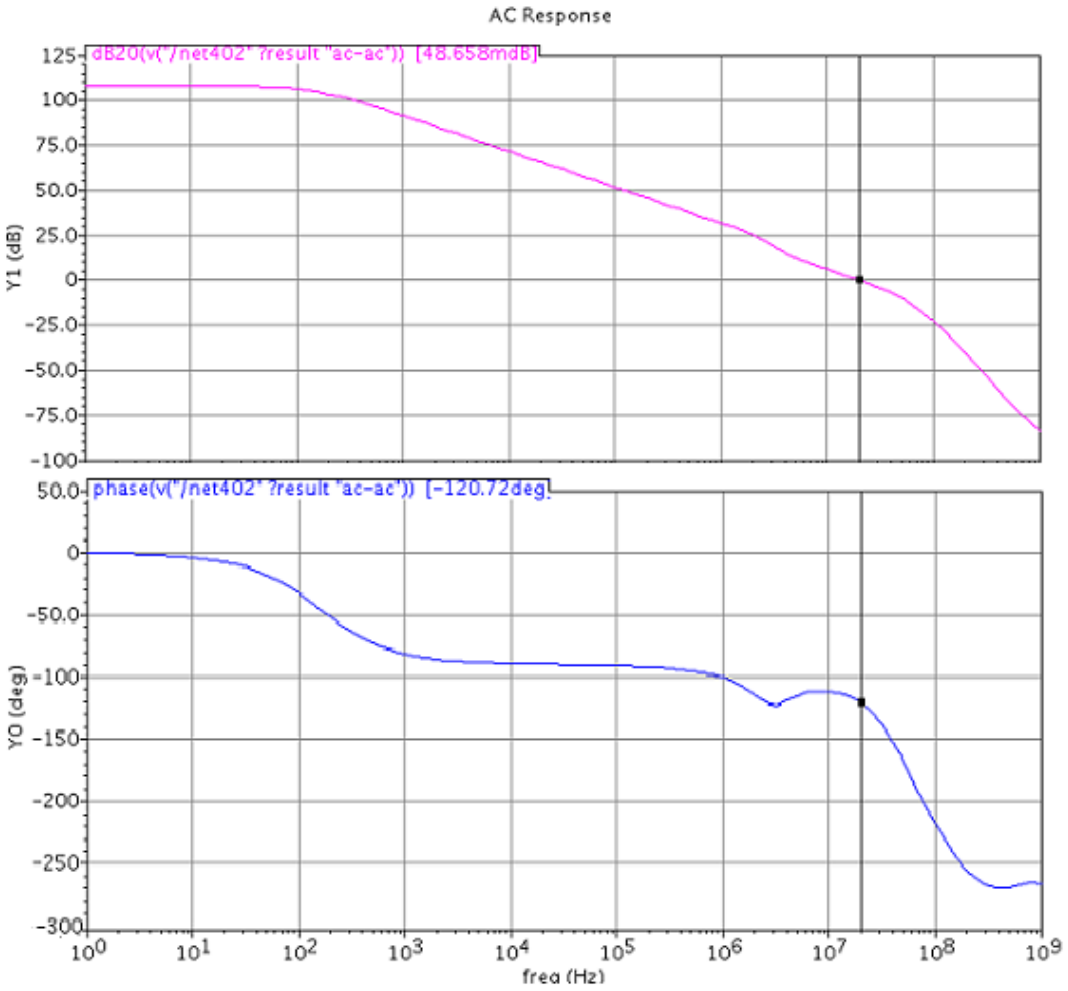


Figure 4.6 Frequency response of amplifier in high-voltage supply condition

The PSR in high-voltage supply condition is shown in Figure 4.7. The PSR is -60.38dB at DC and low frequencies. It increases to -38.28dB at 1MHz. Although this value may not be adequate to reject the supply noise for the standard application,

the bridge configuration used in the proposed design, which is discussed in the next section, provides a good PSR for the final output.

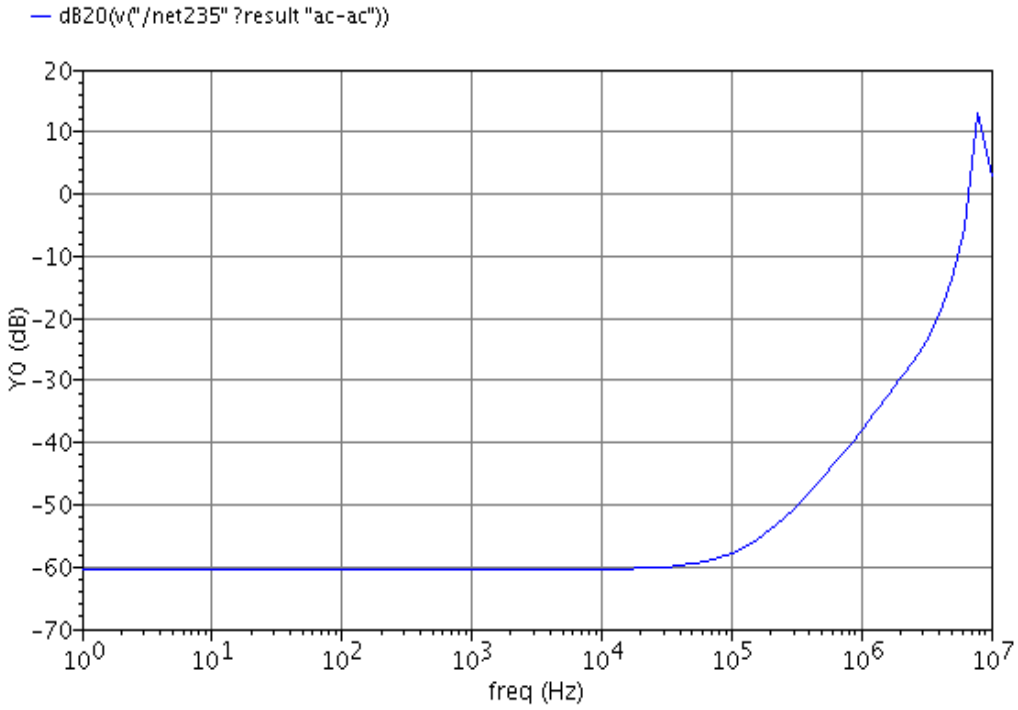


Figure 4.7 Simulated PSR in high-voltage supply condition

- Low-voltage supply rail

When low-voltage supply rail is used to power the output stage, the headroom is highly reduced. This leads to the output transistors to leave the saturation region and enter into the triode region easily. Consequently, the transconductance *gm* and the quiescent current of output stage decrease, thereby decreasing the open-loop gain. Therefore, the output transistors are designed with small lengths and very large aspect ratios so that they are capable to deliver huge output power and do not degrade significantly.

The frequency response of the amplifier under low-voltage supply rail is shown in Figure 4.8. The dc gain of the amplifier is 99.72dB which is less than that in high-voltage supply condition. The phase margin of the amplifier is around 60.7° at the unity gain bandwidth of 10.04MHz. However, this is adequate for processing the audio signal under small magnitude.

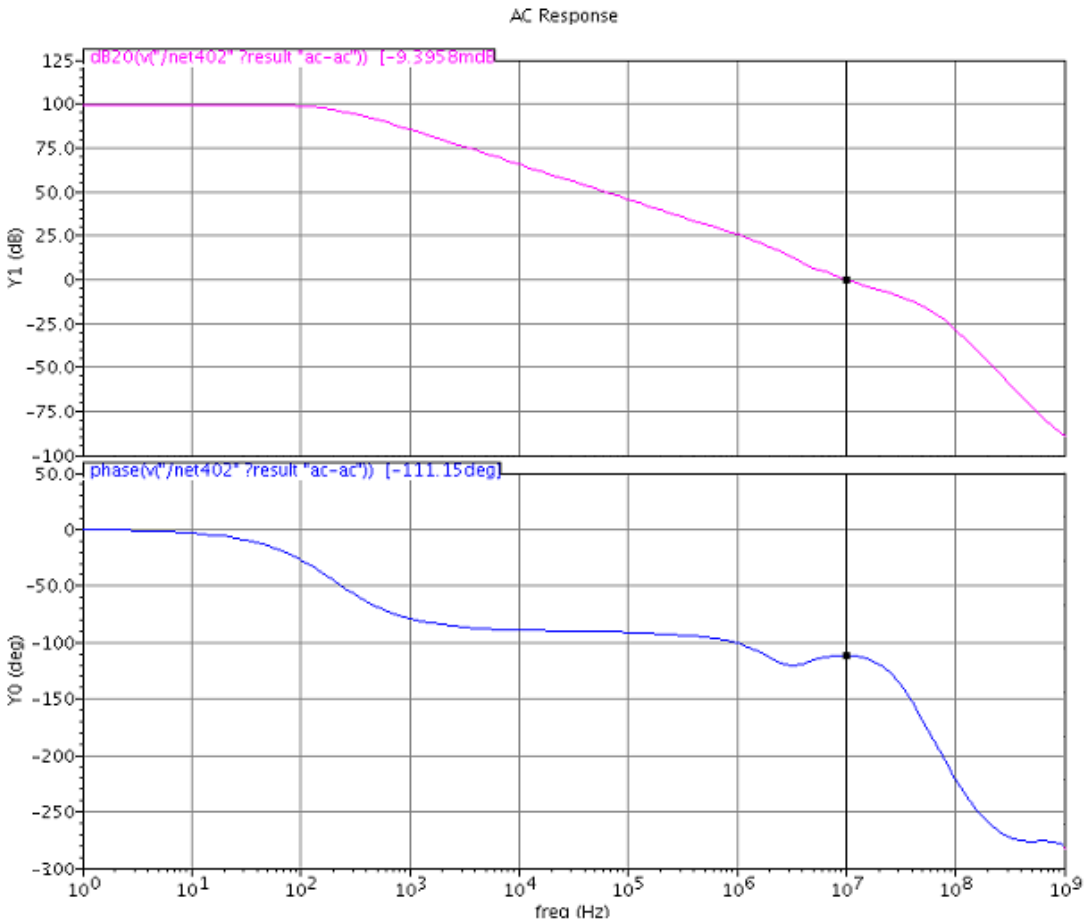


Figure 4.8 Frequency response of amplifier in low-voltage supply condition

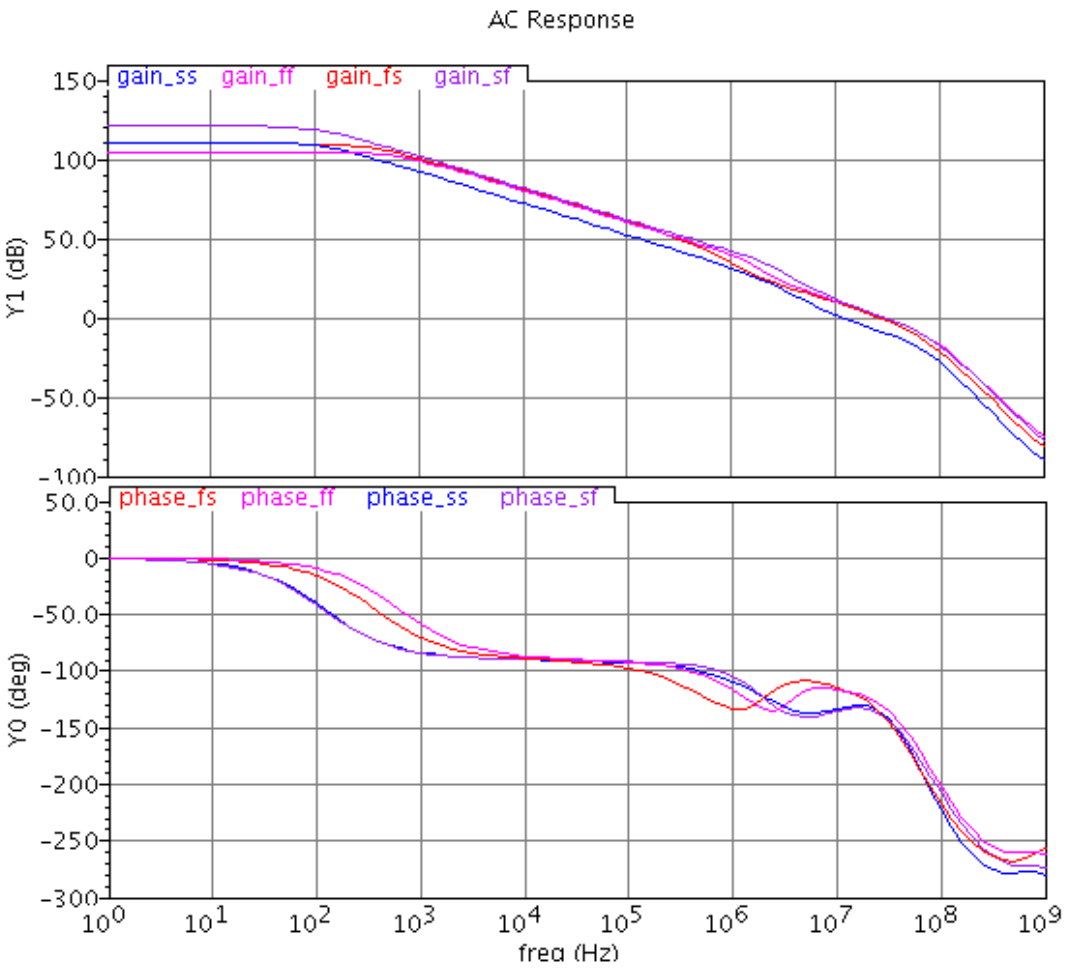


Figure 4.9 Frequency responses of amplifier at various process corners: ss (slow NMOS, slow PMOS), ff (fast NMOS, fast PMOS), fs (fast NMOS, slow PMOS) and sf (slow NMOS, fast PMOS)

Figure 4.9 presents the frequency response of single amplifier at various process corners: ss (slow NMOS, slow PMOS), ff (fast NMOS, fast PMOS), fs (fast NMOS, slow PMOS) and sf (slow NMOS, fast PMOS). In worst case of slow-fast process corner, the phase margin is 47.3 degree. Hence, it has confirmed that this amplifier is stable at various process corners.

The PSR in low-voltage supply condition is shown in Figure 4.10. The PSR is -57.19dB at DC or low frequencies. It decreases rapidly after 1kHz. As discussed, the PSR will be improved by the bridge configuration to achieve an adequate value for rejecting the supply noise in the application.

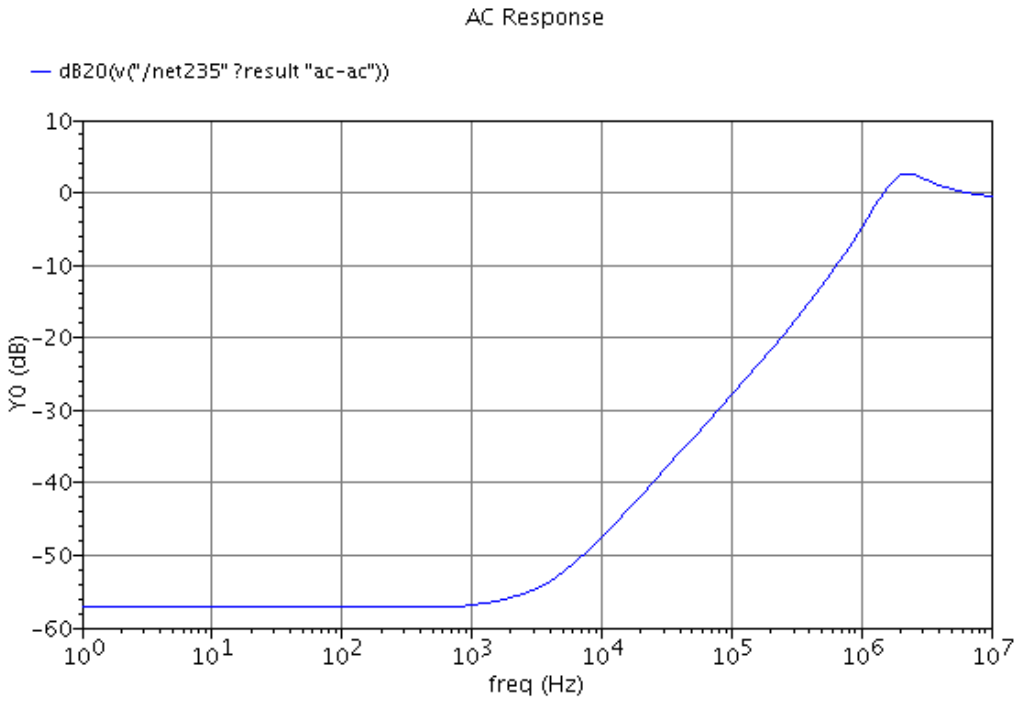


Figure 4.10 Simulated PSR in low-voltage supply condition

4.2.2 Bridge Amplifier

For bridge configuration, the final output voltage amplitude is doubled. The output power is four times more than that of the single configuration. The two interim outputs of the amplifiers have the similar variation with respect to the power supply noise. Therefore, the PSR of final output, which is on the basis of subtraction of the two interim outputs, is greatly improved. The PSR of final output is displayed in

Figure 4.11. At low frequency, the PSR is -107.55dB, which is much higher than that of the single amplifier.

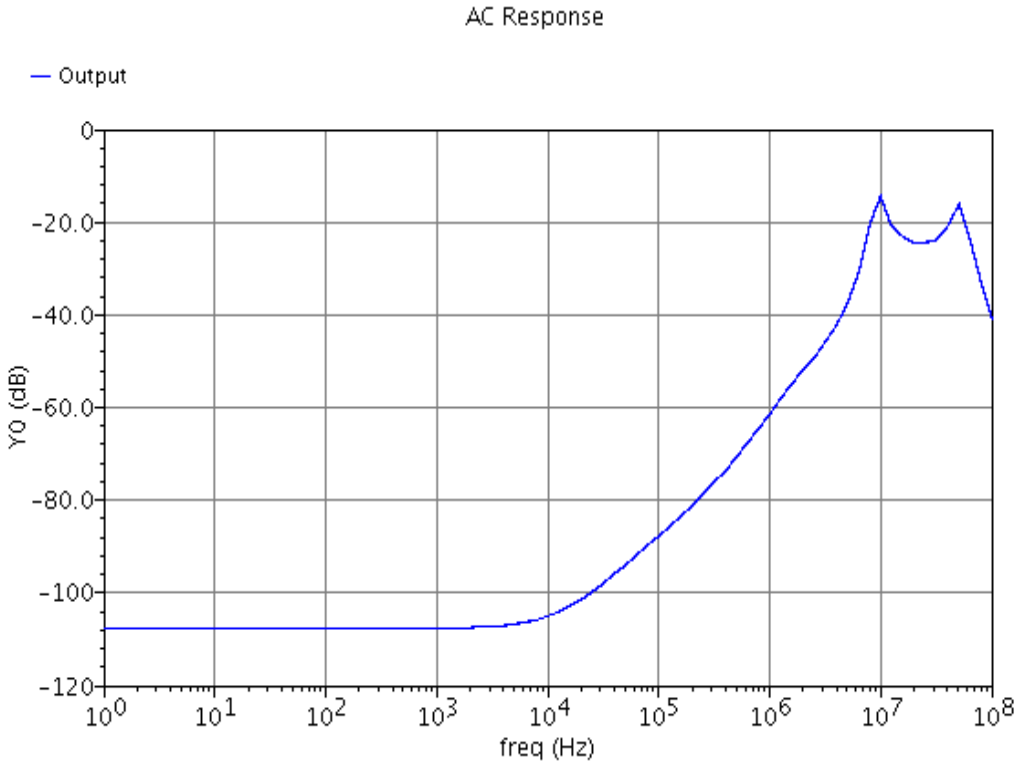


Figure 4.11 Simulated PSR of bridge amplifier

Figure 4.12 shows the harmonic spectrum of single amplifier and bridge amplifier at the same load condition. It is observed that even order harmonic distortion components are significantly attenuated in the bridge amplifier. This is due to the differential architecture.

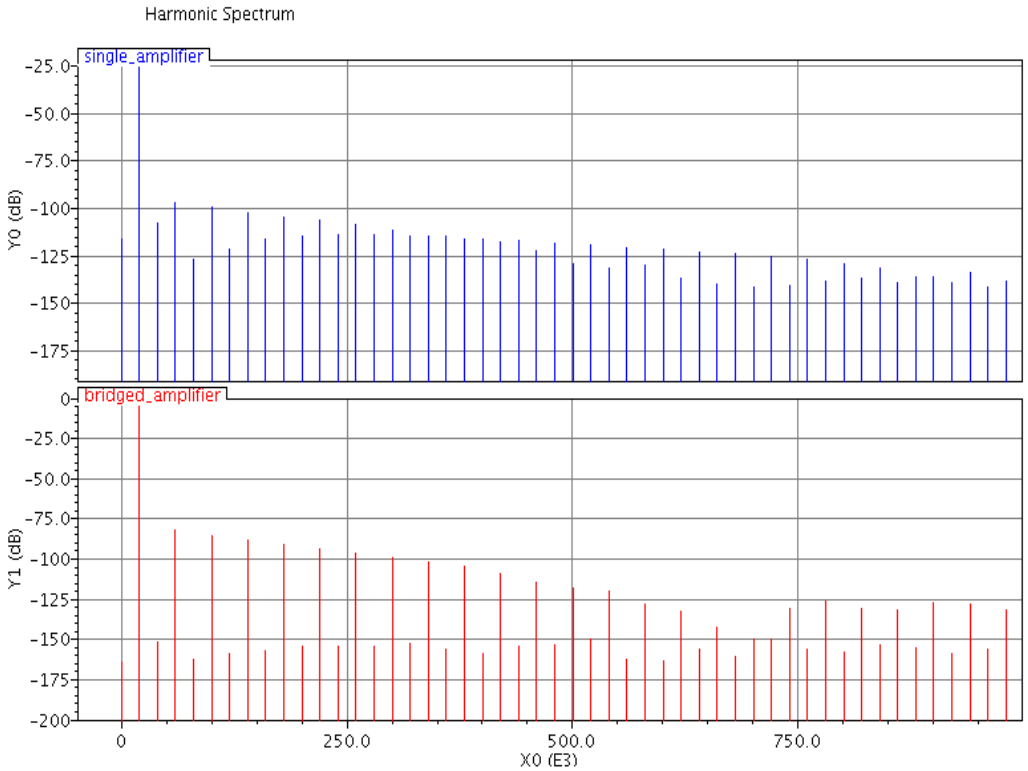


Figure 4.12 Harmonic spectrum of single amplifier and bridge amplifier

4.3 Class G Amplifier

The Class G amplifier operates under two power supply conditions. When the output signal amplitude is small, only the low-voltage supply rail is used. The sinusoidal steady state response of final output voltage and output stage supply voltage is shown in Figure 4.13. Vo1 and Vo2 are the two outputs at each terminal of the loudspeaker. Vout is the final difference output which is the voltage across the loudspeaker. The power supply Vamp-supply only selects the low-voltage supply rail which is the output of the regulated DC-DC converter discussed previously. Vdc-op is the the DC operating voltage. It is always half of the instantaneous Vamp-supply value. Although the supply voltage contains certain switching noise, the final output does

not have a big effect due to the high PSR of the bridge amplifier.

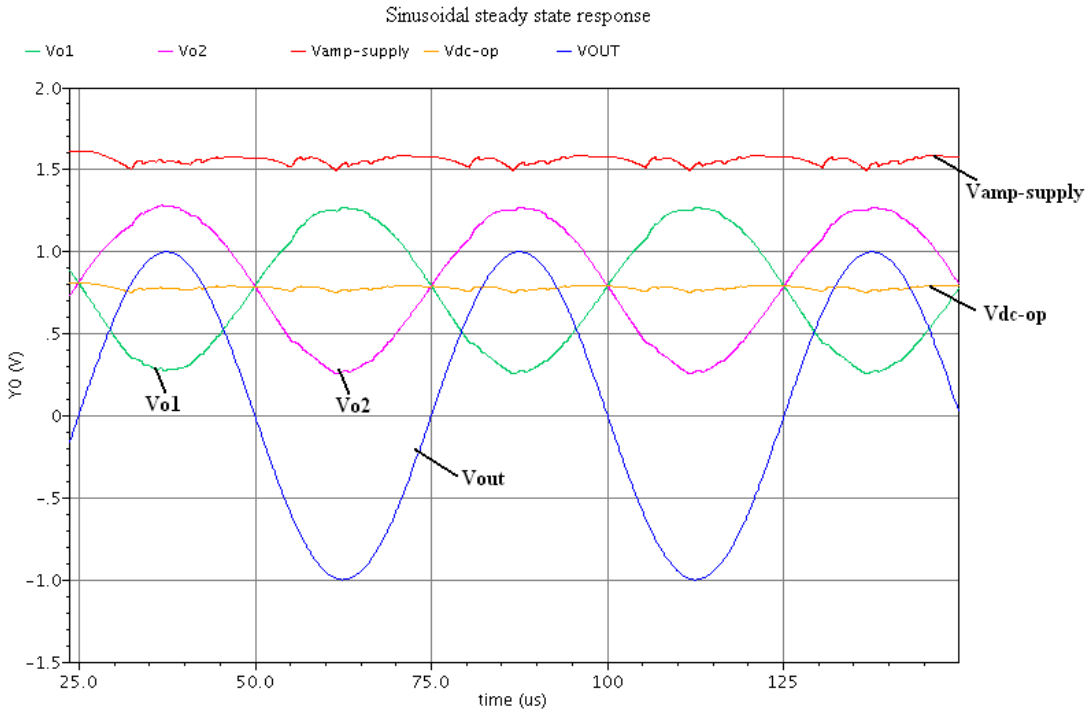


Figure 4.13 Sinusoidal steady state responses of small amplitude output voltage at low-voltage supply voltage

When the amplitude of the output signal becomes large, the supply is switched from low-voltage supply rail to high-voltage supply rail. A common issue for the class G amplifier is that during the transition between the two supply rails, there is always a glitch or spike in the output which highly reduces the amplifier linearity. The proposed design solves this problem using a supply control circuit. The sinusoidal steady state responses of final output and supply voltage are depicted in Figure 4.14. It can be seen that although the output voltage at each loudspeaker terminal looks distorted, the final output still remains a high linearity because of the differential

subtraction on both signals. The dynamic power supply Vamp-supply shows a smooth transition from low to high voltage and back to low voltage. This validates the function of supply control circuit.

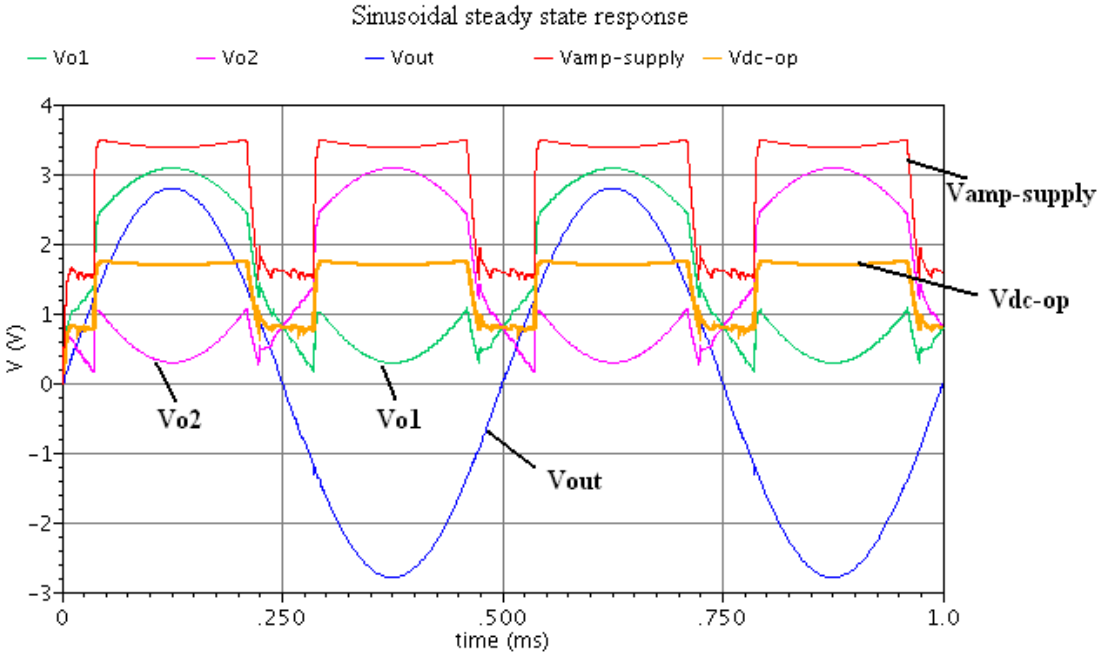


Figure 4.14 Sinusoidal steady state responses of large amplitude output voltage at high-voltage supply voltage

The THD performance of the overall Class G amplifier is shown in Figure 4.15. When the audio signal frequency reaches 20 kHz, the THD is in the range of 0.05% to 0.1%. When the audio signal frequency is 1 kHz, the THD decreases to around 0.02%. These values are adequate for the typical audio applications.

HV is the external power supply while LV is derived from HV using a 1/2 step down charge pump that has some supply ripple. Therefore, high output voltage using HV

should have better THD than low output voltage using LV. In Figure 4.15, although there is some small fluctuation, the overall trend shows a decrease in THD with the increasing of output voltage. It should be noticed that the output voltage of 2.45Vrms has an extremely high THD. That is because the peak voltage is too close to the power supply voltage that a big distortion occurs due to the lack of headroom. It is already out of the valid operation range.

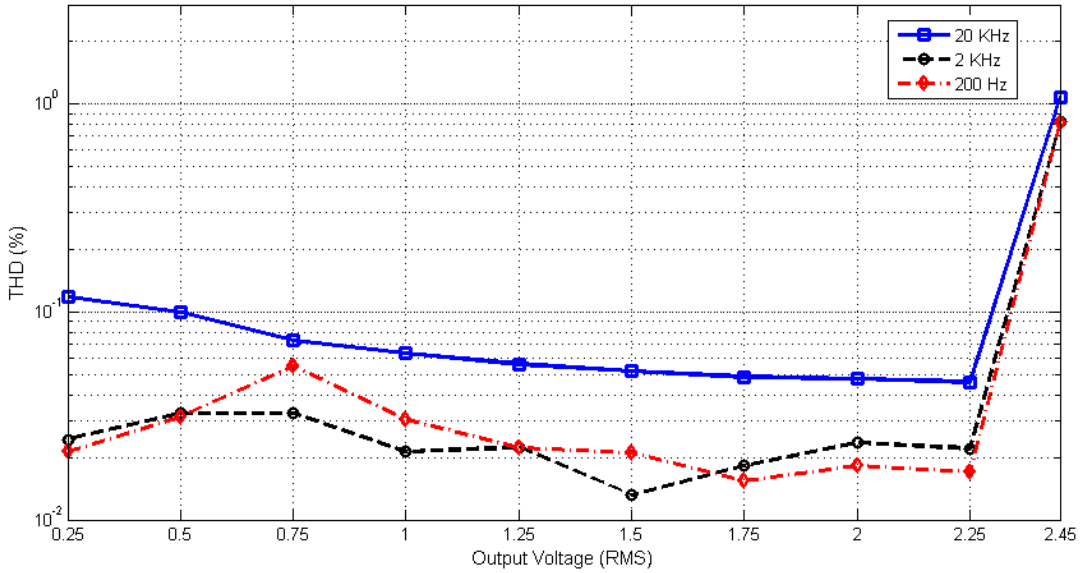


Figure 4.15 THD performance of Class G amplifier

The harmonic spectrums of different frequency signals are also illustrated in Figure 4.16. All the even harmonics are suppressed to the very low levels whilst the odd harmonics of the worse case test signal at 20kHz are less than -67.7dB at an output full swing of 2.4Vrms. It demonstrates that even for a complex audio signal consisting of different audio signal frequencies, the linearity of the Class-G amplifier is good.

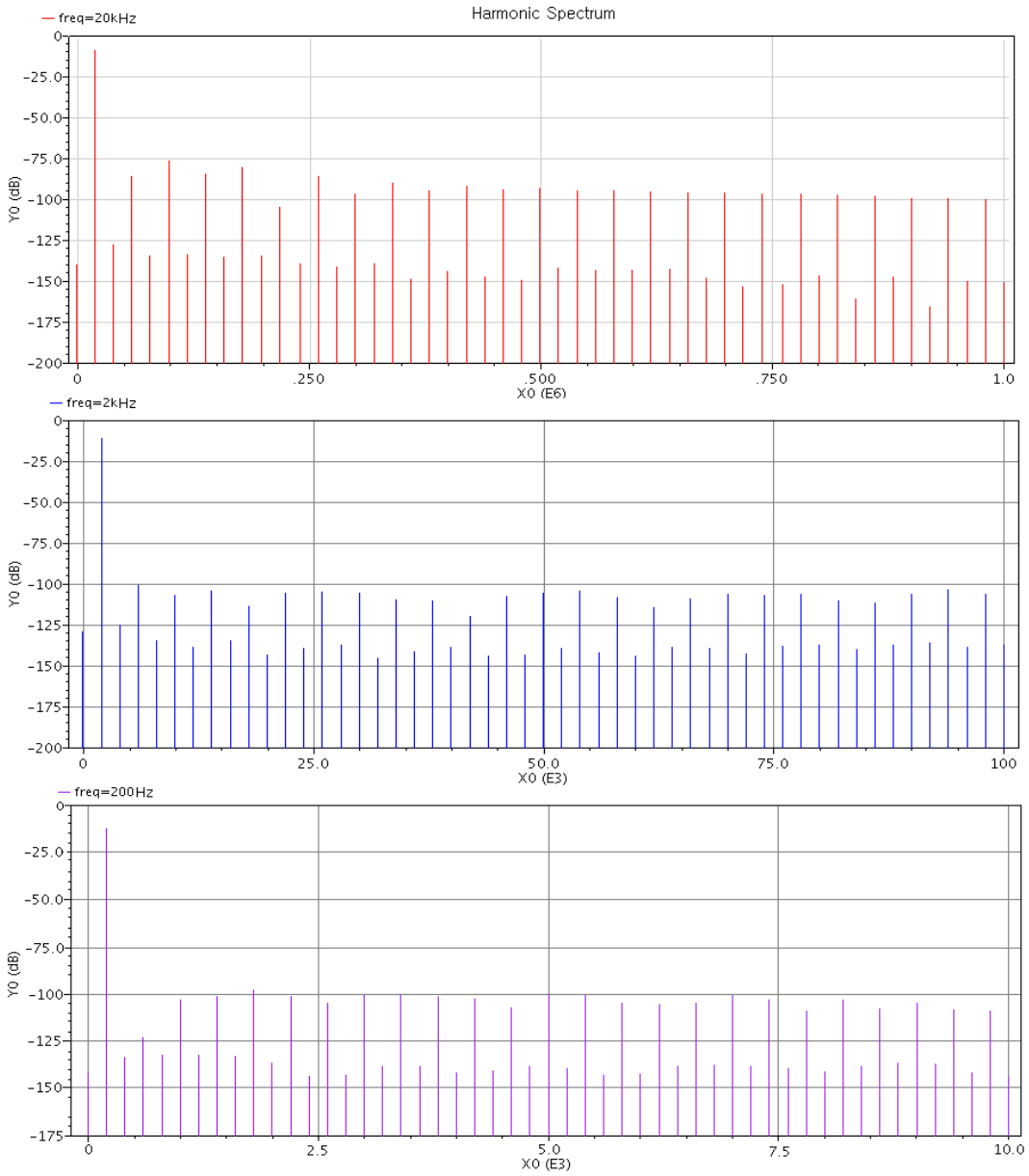


Figure 4.16 Harmonic Spectrum of frequency signal at 20kHz, 2kHz and 200Hz

The simulation results of power efficiencies of proposed Class G amplifier and typical Class AB amplifier versus output voltage are illustrated in Figure 4.17. As depicted in Figure 4.17, it can be observed that in the range of output voltage with small RMS value, the power efficiency of Class G amplifier is about twice of the

efficiency of Class AB amplifier. This proves the theory for improving the efficiency using two supply rails. In the range of output voltage with large RMS value, as displayed in Figure 4.13, the low-voltage supply rail is also used when the instantaneous output voltage is small. Therefore, the power efficiency of Class G amplifier in this range is slightly higher than that of Class AB amplifier. The difference is insignificant and of no concern.

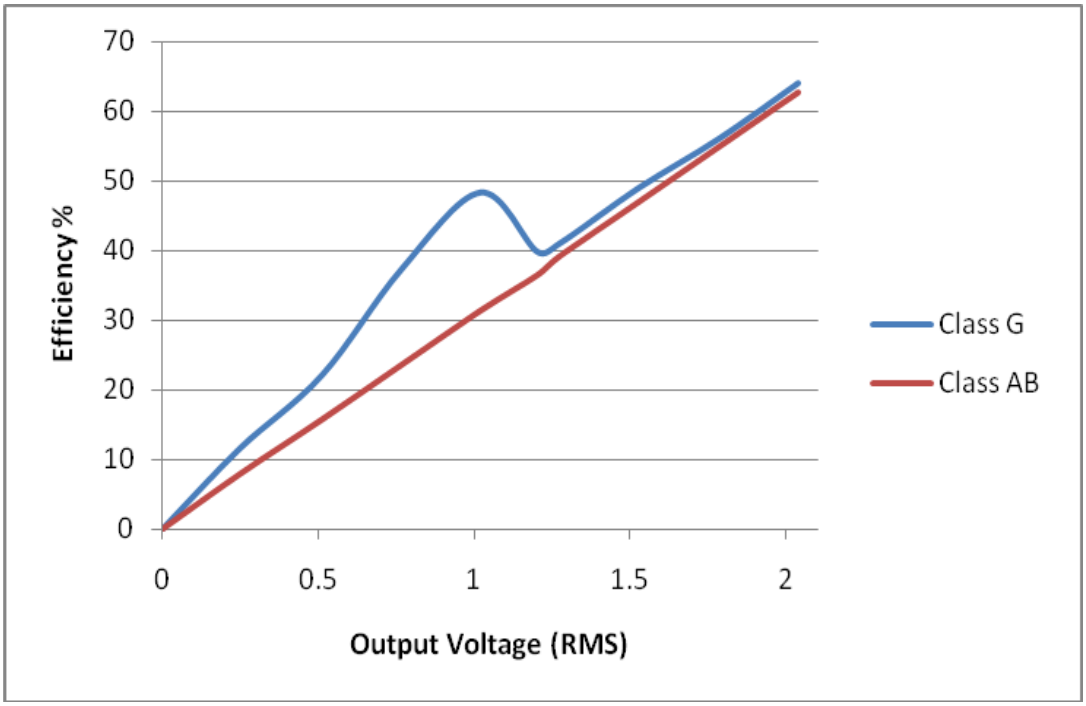


Figure 4.17 Power efficiencies of Class G amplifier and Class AB amplifier versus output voltage

4.4 Performance Summary

Table 4.1 compares various performance parameters of the previously published works with that of the proposed Class G power amplifier. Class G amplifier was a

popular research topic 20 years ago realized by two or more external power supplies. After that, Class D amplifier has received attention because of its high power efficiency. Class G amplifier becomes popular recently due to its simplicity and high linearity for the cost-critical and space-constrained portable applications. Therefore, only a few existing Class G amplifier designs can be used as benchmark for comparison.

The figure-of merit (FOM) [56], which is defined as a ratio between the peak power delivered to load and the quiescent power consumption, is employed. The proposed class-G amplifier exhibits comparable FOM whilst achieving low total harmonic distortion across a wide range of audio frequencies as well as low noise for standard audio specification. This suggests the effectiveness of the proposed class-G architecture.

Finally, the smallest number of area-consumed components compared with all the references shows another attraction for low cost implementation. In Class G structure, compared with other components, the most area-consumed components are the power transistors, diodes and inductors. The exact size of the power transistors and diodes are not given by the reference designs. Instead of using the area parameter, the number of area-consumed components is compared in the performance summary table. As can be seen, each has different architectural design, leading to the use of

different number of area-consumed components. The comparison is still fair. Furthermore, when all prior-art works and the proposed work are realized in identical CMOS technology, it is clear that the proposed design will have area-efficiency on the basis of identical power transistor in design. Hence, the proposed class-G amplifier demonstrates its suitability for the portable device audio applications.

Table 4.1 Performance Summary

Parameter	This work	[33]	[40]	[41]
Result	Simulation	Simulation	Experimental	Experimental
Technology	0.35um CMOS	BJT	BiCMOS	BiCMOS
No. of Area-consumed components	4	18	6	-
Supply Voltage	3.6V	+/- 5V +/- 15V	3.6V	1.5V
Load	8 Ohm 200pF	10 Ohm	8 Ohm 200pF	16 Ohm
Peak Load Power	1.45W	20W	2.4W	25mW (per channel)
THD @ 20kHz	0.0404%	0.279%	0.02%	0.06% (16ohm)
THD @ 1kHz	0.0172%	0.0147%	0.11%	0.02% (16ohm)
SNR (A-weighted)	97.3dB	-	95dB	92dB
FOM $\frac{\text{Peak load power}}{\text{Quiescent power}}$	80.28	-	80	31.8

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In this thesis, the analysis and implementation of a class G amplifier for high performance audio application has been presented. The proposed design consists of two parts, namely the power supply unit and the switched-supply amplifier unit.

The power supply unit, formed by a closed-loop high efficient SC DC-to-DC step down converter with pulse-skip regulation, provides two supply rails (LV and HV) for the switched-supply amplifier unit. An internal supply rail LV, which has a value of half of the external power supply, is generated for the utilization when the input signal amplitude is small. When this supply rail is used, the power efficiency is theoretically doubled when compared with using external power supply. The external power supply HV is switched in for a large input signal to avoid clipping.

The switched-supply amplifier unit is consisted of preamplifiers, core bridge amplifier, supply control circuit and DC control circuit. The bridge amplifier configuration improves the peak output power by four times when compared to a single amplifier. The supply control circuit traces the input level to select the appropriate supply rail. Furthermore, the DC control circuit and preamplifiers adjust

the DC offset of the input signal according to the selected supply rail.

Compared with the existing Class G amplifier designs, this proposed Class G amplifier has many advantages. First, the proposed design uses only one external power supply so that it is realizable in simple and low cost process technology. Second, this design eliminates the need of a high-cost inductor. As a final remark, only four power transistors are used. This gives the benefit of smaller area. The Class G amplifier is shown to have higher power efficiency than Class AB amplifier. It also fulfills the linearity requirement of audio application

5.2 Recommendation

A common problem in portable audio applications is the limited supply voltage available to the speaker amplifier while the speaker requires more power to generate acceptable sound pressure levels. Consequently, a bridge-tied-load configuration, which allows four times the output power to be delivered to the speaker, is popularly used. Although the bridge amplifier configuration is sufficient to provide enough power in many cases, there are some applications requiring even more output power such as GPS devices and piezoelectric speakers. The common solutions are either to boost the supply voltage via a separate DC-DC boost converter or to generate a negative supply rail by an inverting DC-DC converter. However, these will cause a consequent restriction on the realization process technology. In the future work, more

research can be done on how to increase the peak output power while remaining the simple and low cost process technology for realization.

The life time of a battery is one of the critical problems for almost all portable devices. In order to extend the life time of the battery, high efficiency power amplifier is required. The main limit of the power efficiency of Class G power amplifier depends on the power efficiency of DC-DC converter. The switching loss and conduction loss in DC-DC converter occupies a big portion of the total power loss. Therefore, an improved power efficient DC-DC converter is always desirable.

This design uses a dual supply system as the power supply unit of Class G power amplifier. With the purpose of achieving higher power efficiency, a multiple supply system can be employed to reduce the power loss for different input signal amplitudes. However, the more supply rails are generated, the more complex DC-DC converter will be. There is always a trade-off between the performance and the simplicity.

This design employs a bridge amplifier configuration by adding a second identical amplifier with the load connected between the two outputs. This forms a pseudo differential amplifier. The THD performance is improved since the even order harmonic distortions have been cancelled by this differential structure. It also leads to

a higher Power Supply Rejection (PSR). For further improvement in future works, a truly fully differential amplifier can be employed to replace this bridge amplifier configuration. A better THD and PSR performance can be expected. Besides, the fully differential structure also helps the reduction of the circuit overhead among the two identical amplifiers.

The functional blocks such as voltage reference, supply control circuit, DC control circuit and the preamplifiers consume certain among of quiescent currents that reduce the power efficiency of the Class G amplifier. In the future work, the current consumption of these functional blocks should be minimized so as to improve the overall power efficiency.

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Appendix A: Terminology and Definition

Total Harmonic Distortion

The non-linear behavior of the amplifier would induce harmonic distortions. Furthermore, the distortions will depend on parameters as signal level, frequency, and load parameters [54]. Total Harmonic Distortion (THD) is the index used to measure the harmonic distortions. In general, the lower the THD, the higher is the fidelity. A THD rating <1% is considered to be in high-fidelity and inaudible to the human ear [55].

A commonly used THD definition is a ratio of the square root of the sum of the squares of all harmonic root-mean-square (rms) amplitudes located at frequencies (above the fundamental frequency) over the fundamental amplitude [54]. THD is normally demonstrated in dB or percentage, and defined as following

$$THD = 10\log\left(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}{V_f^2}\right) \tag{A.1}$$

or

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}}{V_f} \times 100\% \tag{A.2}$$

where V_f is the rms amplitude of the fundamental signal, V_{hn} is the rms amplitude of the n^{th} harmonic.

THD is usually presented in percentage.

Total Harmonic Distortion + Noise

Total Harmonic Distortion + Noise (THD+N) is the ratio of the noise and distortion level to the signal level. THD is expressed as:

$$\mathrm{THD+N(dB)} = 10\log\frac{\mathrm{D+N}}{\mathrm{S}} \tag{A.3}$$

where D is the distortion power, N is the noise power, and S is the signal power.

Signal-to-Noise Ratio

Signal to Noise Ratio (SNR) is often used as the index of linearity. SNR is defined as the ratio of signal power and noise power. The equation is given by

$$\mathrm{SNR} = 10\log\left(\frac{\mathrm{S}}{\mathrm{N}}\right) \tag{A.4}$$

where S is the signal power and N is the noise power

Power Efficiency

The power efficiency is defined as the ratio of the power delivered to the load to the power supplied from a power supply. The equation is defined as

$$\eta = \frac{\text{power delivered to the load}}{\text{power supply } V_{DD} \times \text{Average current provided by } V_{DD}} \tag{A.5}$$

A-weighting

A-weighting is the most commonly used of a family of curves defined in the International standard IEC 61672:2003 and various national standards relating to the

measurement of sound pressure level. The gain curve is defined by the following s-domain transfer function.

$$G_A(s) = \frac{k_A \cdot s^4}{(s+129.4)^2(s+676.7)(s+4636)(s+76655)^2} \quad \text{(A.6)}$$

Appendix B: Calculation of Hysteresis in Comparator

The input voltages of comparator can be related into the output currents of the pre-amplification stage by

$$i_{op} = \frac{g_m}{2}(v_p - v_n) + \frac{I_{ss}}{2} \tag{B.1}$$

$$i_{on} = \frac{g_m}{2}(v_n - v_p) + \frac{I_{ss}}{2} \tag{B.2}$$

where vp, vn are the AC signals of input voltages, gm is the transconductance of input transistor, ISS is the biasing current of pre-amplification stage, iop, ion are the small-signal AC output currents of pre-amplification stage.

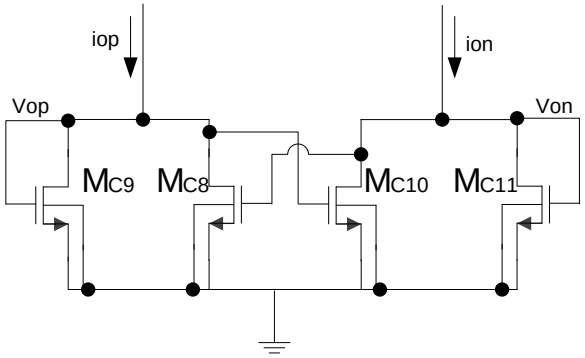

Figure B.1 Schematic of decision circuit in comparator

Figure B.1 depicts the decision circuit of the comparator. Assume that iop is much larger than ion, so that Mc9 and Mc10 are on and Mc8 and Mc11 are off. If we start to increase ion and decrease iop, the switching will take place when the gate-source voltage of Mc11 is equal to threshold voltage Vthn. At the switching point, where

Mc11 is just about to turn on (Vgs is approaching Vthn but drain current is still zero) the current flowing in Mc10 is

$$i_{on} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{10}\left(V_{op} - V_{thn}\right)^2 \tag{B.3}$$

The current flowing in Mc9 is

$$i_{op} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{9}\left(V_{op} - V_{thn}\right)^2 \tag{B.4}$$

Substitute B.2, B.3 and B.4 into B.1, we can get the equation of hysteresis of the comparator is

$$V_{SPH} = v_p - v_n = \frac{I_{SS}}{g_m} \times \frac{\left(\frac{W}{L}\right)_{10} - \left(\frac{W}{L}\right)_{9}}{\left(\frac{W}{L}\right)_{10} + \left(\frac{W}{L}\right)_{9}} \text{ for } \left(\frac{W}{L}\right)_{10} \geq \left(\frac{W}{L}\right)_{9} \tag{B.5}$$

Appendix C: Calculation of Reference Voltage

In Figure 3.11, the resistors Rv3 and Rv8 are introduced for base currents compensation. It is assumed that the base currents for the three BJTs are the same. Through classical circuit analysis, the interim output Vo1 can be derived as

$$Vo_1 = \left(V_{BE} + 3\frac{\Delta V_{BE}}{R_2} * Rv_1 - 1.5I_B * \frac{Rv_3 Rv_1}{Rv_2} \right) * \left(\frac{Rv_4 + Rv_5}{Rv_5} \right) + 1.5I_B * Rv_4 \tag{C.1}$$

The design equation of Rv3 for base current compensation is obtained as

$$Rv_3 = \frac{Rv_2}{Rv_1} * \left(\frac{Rv_4 Rv_5}{Rv_4 + Rv_5} \right) \tag{C.2}$$

Similarly, we have

$$Rv_8 = \frac{Rv_2}{Rv_1} * \left(\frac{Rv_6 Rv_7}{Rv_6 + Rv_7} \right) \tag{C.3}$$

Therefore, the two interim outputs are given as follows:

$$Vo_1 = \left(V_{BE} + 3\frac{\Delta V_{BE}}{Rv_2} * Rv_1 \right) * \left(\frac{Rv_4 + Rv_5}{Rv_5} \right) \tag{C.4}$$

$$Vo_2 = \left(V_{BE} + 3\frac{\Delta V_{BE}}{Rv_2} * Rv_1 \right) * \left(\frac{Rv_6 + Rv_7}{Rv_7} \right) \tag{C.5}$$

where $$\Delta V_{BE} = nV_T * \ln\left(\frac{A_{E1}}{A_{E2}} \right) \tag{C.6}$$

and n is a constant, VT is the thermal voltage, AE1 is the emitter area of Q1, AE2 is the emitter area of Q2. In order to get zero temperature coefficient, the ratio of Rv1 and Rv2 is obtained as

$$\frac{Rv_1}{Rv_2} = \frac{-\frac{\partial V_{BE}}{\partial T}}{3\left(\frac{nV_T}{T} \right) * \ln\left(\frac{A_{E1}}{A_{E2}} \right)} \tag{C.7}$$

where T is the temperature.

The output voltage in Fig. 3.10 can be expressed as follows:

$$V_{out} = \frac{R_{S2}}{R_{S1}(1+SR_{S2}C_{S2})} * (V_{O1} - V_{O2})$$
$$= \frac{R_{S2}}{R_{S1}(1+SR_{S2}C_{S2})} * \left(V_{BE} + 3\frac{\Delta V_{BE}}{R_2} Rv_1\right)\left(\frac{Rv_4}{Rv_3} - \frac{Rv_6}{Rv_7}\right) \quad \text{(C.8)}$$

where R_{S1}=R_{S3} and R_{S2}=R_{S4}.

Appendix D: Quiescent Current in Each Block

Table D.1 Quiescent current distribution table

Block Name	No. of block	Block quiescent current
DC-DC converter	1	87uA
Voltage reference	3	198uA
Supply control circuit	1	231uA
DC control circuit	1	81uA
preamplifier	2	83uA
core amplifier	2	1.94mA

Appendix E: Device Sizing

Table E.1 Device Sizing of the Voltage Reference Voltage Generating Circuit

Device (MOS)	Sizing (μm/μm)	Device (Resistor)	Sizing (Ω)
M_{V1}	2/20	R_{V1}	38.93k
M_{V2}	10/2	R_{V2}	11.4k
M_{V3}	10/1	R_{V3}	3.385k
M_{V4}	90/2	R_{V4}	15.89k
M_{V5}	90/2	R_{V5}	42.34k
M_{V6}	90/2	R_{V6}	12.71k
M_{V7}	90/2	R_{V7}	126.9k
M_{V8}	40/2	R_{V8}	3.385k
M_{V9}	40/2	R_{V9}	40k
M_{V10}	90/1.2		
M_{V11}	90/2	Device (BJT	Sizing (Multiplier)
M_{V12}	90/2	Q1	8
M_{V13}	90/2	Q2	1
M_{V14}	40/2	Q3	1
M_{V15}	90/1.2		
M_{V16}	90/2		

Table E.2 Device Sizing of the Comparator

Device (MOS)	Sizing (μm/μm)	Device (MOS)	Sizing (μm/μm)
M_{C1}	3/2	M_{C10}	1/10
M_{C2}	3/2	M_{C11}	1/10
M_{C3}	5/2	M_{C12}	12/2
M_{C4}	5/2	M_{C13}	1.05/2
M_{C5}	6/2	M_{C14}	1.05/2
M_{C6}	5/2	M_{C15}	1/4.5
M_{C7}	5/2	M_{C16}	1/4.5
M_{C8}	1/10	M_{C17}	2.5/10
M_{C9}	1/10		

Table E.3 Device Sizing of the Core Amplifier

Device (MOS)	Sizing (μm/μm)	Device (MOS)	Sizing (μm/μm)
M_{A1}	20/0.5	M_{A16}	60/10
M_{A2}	20/0.5	M_{A17}	1.95/10
M_{A3}	34.5/0.5	M_{A18}	50/10
M_{A4}	34.5/0.5	M_{A19}	2.6/10
M_{A5}	39.7/10	M_{A20}	24000/0.35
M_{A6}	2.5/1	M_{A21}	7000/0.35
M_{A7}	2.5/1		
M_{A8}	7/1	Device (Resistor)	Sizing (Ω)
M_{A9}	7/1	R_{A1}	24k
M_{A10}	19/0.5	R_{A2}	24k
M_{A11}	19/0.5		
M_{A12}	50/3	Devide (Capacitor)	Sizing (pF)
M_{A13}	320/1	C_{A1}	0.4
M_{A14}	48/3	C_{A2}	0.4
M_{A15}	53/3	C_{A3}	0.6