Design and Fabrication of RF Devices by Novel MEMS Technologies

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Abstract

With today's fast expansion of the wireless communication industry, integrated circuits are being driven to a higher level of integration by consumer market that is desired for products with higher performance, low cost, light weight, small size, and minimum power dissipation.

The active components such as, diodes, transistors, have been well developed for RFICs (radio frequency integrated circuits) in the few GHz frequency range and they are easily integrated onto chips using today's IC technologies (CMOS, BiCOMS, BiPolar). However, for the development of RFICs, passive components including inductors, capacitors, resistors, and filters et al. are indispensable. Unfortunately, these passive devices, especially inductors and filters, are still not satisfied with the RFICs requirement. The bottlenecks for the full integration to realize SOC (system on chip) are the development of passive components such as inductors and filters with high quality factor and small size.

Inductors are essential in RF circuits for functions such as tuning, filtering, impedance matching, and gain control. Nowadays, on-chip RF inductors are mostly fabricated on the GaAs substrate, which is much more expensive than silicon substrate and can not be integrated with silicon substrate. The fabrication of inductors on silicon substrate, like the other components based on silicon, can obviate the present need for external connections, thus resolving issues such as electrical and magnetic coupling as well as parasitic losses due to pad and bond wire in the RF designs. On the other hand, the commonly used silicon substrate has high conductivity in the high operating frequency range of up to few GHz. The

electromagnetic fluxes of inductors can easily penetrate into the substrate, resulting in large losses. In addition, compared with other circuit components, RF inductors always occupy much larger area; hence further reduce their performance in RF circuits.

The developments of RF resonators and filters are also important for RFICs. In modern transceiver architectures, the integrated band-select filters and IF (intermediate frequency) filters are not available because these necessary filters have very large size compared to currently integrated components. The current filters for RFICs are discrete devices, which makes the integration of these filters with IC chips very challengeable.

This work is focused on development of novel MEMS fabrication technologies to realize high performance RF inductors, RF resonators, and RF filters based on silicon substrate.

As silicon substrate losses are the main obstacle to fabricate RF inductors with high quality factor, SiDeox (silicon Deep etching and oxidation) MEMS technology is specially developed to reduce the substrate losses. During the development of SiDeox technology, DRIE (deep reactive ion etch) and controllable thermal oxidation techniques are elaborately investigated. Thick SiO_2 blocks up to 20 μm are successfully fabricated for the development of RF passive devices with high performance.

To design RF inductors, the aspects including layout designs, substrate losses, and series resistance of conductor wires, are analyzed since they contribute to the low quality factor of inductors. Then, the figures of merit of an inductor including quality factor, self-resonant frequency, and inductance, are explored in detail. Subsequently, the modeling and three-dimensional electromagnetic simulations have been carried out to predict the performance of proposed inductors using the SiDeox technology. Finally, the designed inductors are fabricated and tested in Micromahcines Center, NTU. The results show that the quality

factor and self-resonant frequency are significantly improved due to the advantages of SiDeox technology.

RF passive resonators and filters have been explored in the design and manufacturing technologies. By combining various transmission structures including CPW, CBCPW, and MSL, novel RF resonators and filters are developed with high quality factor and small structural size. To eliminate the power leakage issues in the CBCPW structure, through-wafer vias are created to connect the CPW guard surroundings to backside ground. In the fabrication process, high-aspect-ratio electroplating technique is developed for vias formation. The resonators and filters developed by MEMS technologies have been measured with satisfied performance and small feature size.

In this thesis, the developed SiDeox technology is applied to the development of low loss RF inductors. The potential of this fabrication technique can be further explored with more extensive RF passive devices, which suffer from high substrate losses when they are built on silicon substrate. The electroplating technique has the potential to be used for wafer level packaging in order to reduce packaging size and improve the reliability.

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Chapter 1

Introduction

The explosive growth in commercial electronic and mechanical markets has generated tremendous interest in the MEMS (Microelectromechanical System), which is one of the most promising areas of 21st century. MEMS, a revolutionary manufacturing technology, is a new way of making complex electromechanical systems using batch fabrication techniques, which are similar to the way that integrated circuits are made, and making these electromechanical elements along with electronics. The MEMS revolution arises directly from the ability of engineers to explore IC technology and use it to build working micro systems with micromechanical and microelectronic elements. A linguistic examination of the MEMS acronym reveals the key words of "micro", which demonstrates the advantages gained by size downscaling, and "electromechanical", which implies a potential for the integration of many functionalities based on all-kinds of transduction combinations such as chemical, mechanical, thermal, electrostatic, magnetic transducers etc. The advantages of MEMS are compelling. The smaller size of the devices and the fewer components of a system, benefit the lesser power consumption and the higher reliability. Additionally, the integrated functions make MEMS devices more powerful. Since it is a revolutionary manufacturing technology, MEMS covers a large number of research and development areas with many state-of-art technologies. Based on the prior research, MEMS activities have been grouped into following categories [1]:

- Inertial measurement, such as micro-accelerometers, gyroscopes etc.;
- Microfluidics, such as gene chips and related DNA analysis tools;
- Optical MEMS-based devices, such as micro-mirrors, optical switches;
- Pressure measurement, such as pressure sensors;
- Radio frequency MEMS (RF MEMS), such as RF switches, inductors;
- Other areas.

Each of the above mentioned categories has made momentous progress since the last decade. At present, MEMS market is dominated by pressure sensors, accelerometers, microgyros, inkjet nozzles, and hard disk drive heads devices, which are commonly used in the automotive and information technology sectors. The most famous MEMS based device is the airbag trigger accelerometer used in cars. Although the present MEMS market is dominated by inertial, pressure, and fluidic areas, the developments on optical MEMS (or called MOEMS, Micro-optical-electro-mechanical System), BioMEMS (MEMS applied for biography), and RF MEMS, have become more attractive in the recent years and have the potential to be the major applications of MEMS devices in the future.

For RF MEMS, compared with other more developed MEMS technology fields, it is relatively new in MEMS activities, but it has generated a tremendous amount of excitement, because both the performance enhancements and manufacturing cost reduction are evident characteristics of this technology.

1.1 Background

The performance of standard CMOS technologies, thanks to the impetus of the microprocessor and memory markets, has improved constantly and consistently. The submicron CMOS devices now have a cutoff frequency of 100 GHz and exhibit sufficient

performance for radio frequency applications in the 1-5 GHz range. These advantages permit the integration of the RF and IF (intermediate frequency) stages of all kinds of communication units, the holy grail for system-on-chip solutions. However, this goal is not easy to achieve unless the passive components in RF stage also have as good performances and reliable integrations as CMOS devices. CMOS technologies, as mature and standard "machine tools" for DPS (data processes stage), have commercially yielded all kinds of integrated circuit chips such as the memory chip, CPU. However, CMOS technologies currently can not be used to produce many front-end devices of all kind transceivers because these devices always work at high-frequency with analog signals, so that much more losses may be generated in the normal silicon substrate used for CMOS devices.

RF MEMS technology provides a solution to this problem. It is a technology that addresses the advantages of increased functionality and reduced power consumption, and also offers the performance advantages of electromechanical components on size-scale commensuration with single solid-state devices. In many cases, a single RF MEMS component replaces and outperforms an entire solid-state circuit. Figure 1.1 shows an example of three-band transceiver architecture consisting of a tunable antenna, a number of RF switches, low noise amplifiers, band pass filters, phase shifter, and oscillator [2]. These devices in RF stage are not easy to be integrated in a same substrate as the devices in the base band stage. However, by taking the advantages of MEMS technology, a lot of discrete components in RF stage can be removed to simplify the circuit and the whole system can be realized on the same substrate.

In a normal transceiver, there is a large amount of devices, which could be integrated into the system level and designed with novel architectures. Figure 1.2 shows the possible MEMS applications in the RF stage of a normal transceiver [3]. It is clear that the off-chip passive

components, switches, filters, VCOs, mixers, oscillators, and diplexers are all candidates for direct replacement by their MEMS counterparts.

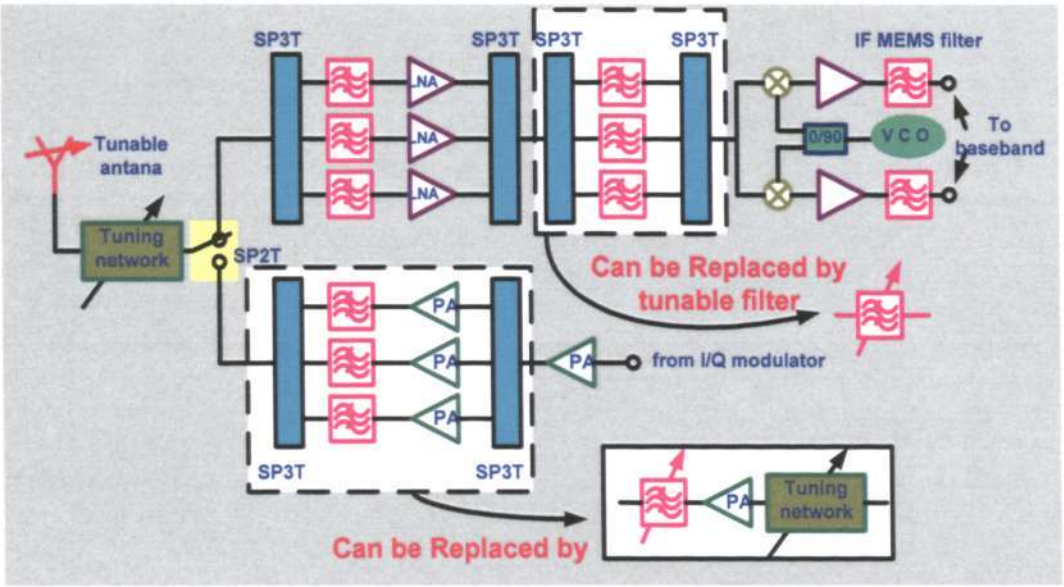


Fig 1.1: The simplification of three-band transceiver using RF MEMS devices [2]

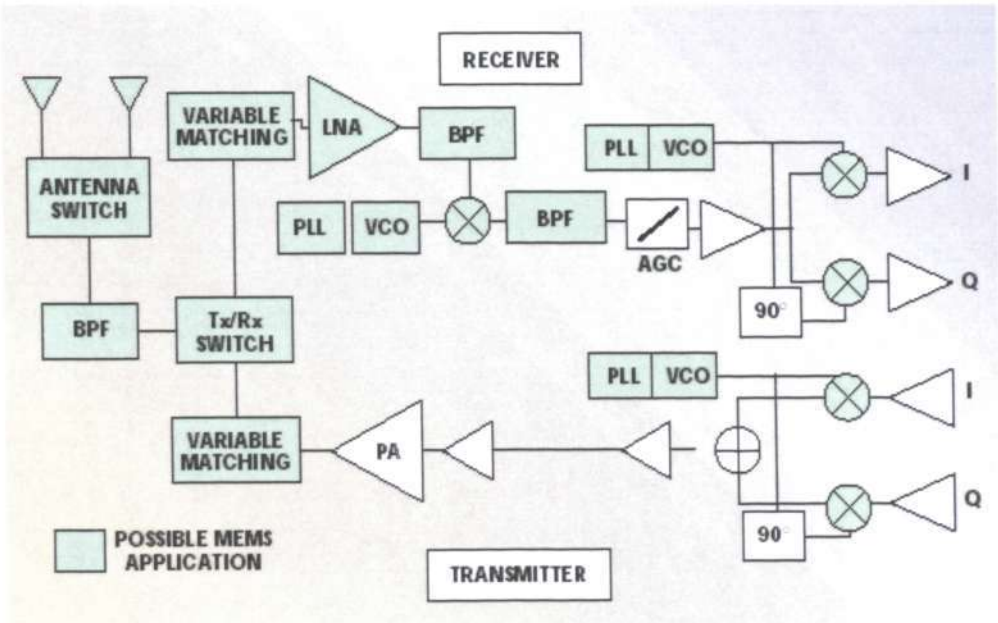


Fig 1.2: Possible MEMS applications in the conventional transceiver architecture [3]

The RF MEMS research started in 1991 when the first MEMS switch was especially developed for microwave applications by Dr. Larry Larson at the Hughes Research Labs in Malibu, California [4]. The initial results of Larson were so outstanding that they stirred the interest of many research groups and companies. By now, there are more than 30 companies working in this area, including the giants of consumer electronics, such as Motorola, Analog Devices, Samsung, Omron, NEC, and ST-Microelectronics. Today, with the global MEMS market, from accelerometers to digital projectors, nearing US $14 billion a year [5], even the most pessimistic forecasters believe that MEMS will change our life at a very real degree. The commercial market trend on the RF MEMS devices has been investigated by the Wicht Technologie Consulting [6], as shown in Figure 1.3.

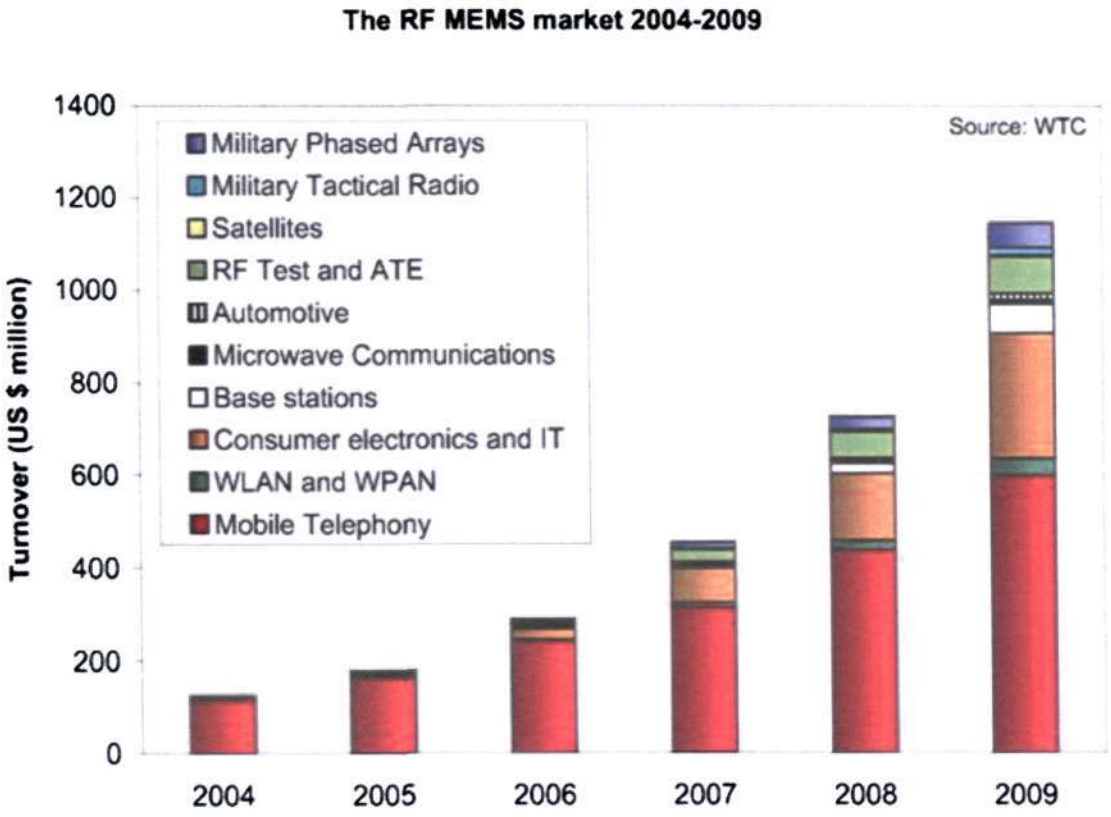


Fig1.3: RF MEMS market trend by applications [6]

To replace the solid-state devices of RF circuits and reduce the discrete components as many as possible, variable RF MEMS devices have been developed so far. The research areas of RF MEMS involve the follows:

- RF MEMS switches, tunable capacitors or varactors, and inductors;
- Micromachined transmission lines, high-Q resonators, filters, and antennas;
- Thin film bulk acoustic resonators and filters that use acoustic vibrations in thin films;
- RF micromechanical resonators and filters that use the mechanical vibrations of extremely small beams.

RF switches, tunable capacitors, inductors, and micromechanical filters are the most important and basic RF devices. They are the fundamental RF components, which can construct complicated RF devices such as tunable RF filters, RF VCOs, RF phase shifters. These devices are presently on the horizon that would find applications to RF systems.

It is a very tough task to develop MEMS technologies for all the RF devices mentioned above. However, a long journey of a thousand miles begins with a single step. This work mainly concentrates on the development of special silicon MEMS technologies for RF MEMS applications including RF inductors, RF resonators and filters, which should be integrated with other on-chip devices with good performances.

1.2 Motivation

There are many researchers devoting their efforts to develop RF MEMS devices, and they have contributed a lot on the RFICs in the past decades. Among the developing devices, RF MEMS switches have been explored so much and close to having viable prototypes

developed by Rockwell (RSC) [7], Raytheon/TI [8-11], HRL Labs [11-12], University of Michigan [13], Siemens AG [14], NEC Corporation [15] etc., and could reach the marketplace in about two years. Tunable capacitors also have very promising results [16-21]. The associated Q factors of such capacitors were found to be good enough, making MEMS capacitors become perspective passive elements in RF technology.

Unfortunately, MEMS technologies for low loss RF devices such as RF transmission lines, RF resonators, especially RF inductors, are urgently desired. Even though significant efforts have been emphasized on the analysis, modeling, dimensional and material optimizations of RF inductors in the last decade, the MEMS technologies for fabricating low loss inductors with high electric and mechanical quality still need to be developed. Although the inductors having inductance less than 1 nH, can be achieved by using transmission lines, the inductors with larger than 1 nH are of planar spiral structures, which occupy larger area in a chip system compared of other devices such as resistors, capacitors, and transistors. This is the reason that the losses of an inductor fabricated on normal silicon substrate are of great concern. For RF resonators and filters, the trend is to fabricate such devices using silicon substrate, since silicon has many advantages as a system substrate material, such as low cost and mature technologies in low-frequency applications. However, substrate loss remains a big problem.

MEMS technologies have many opportunities to be explored for development of RF devices. In this thesis, new fabrication technologies based on silicon substrate are developed for low-loss RF passive devices including RF inductors, RF resonators and RF filters, which can be integrated on silicon substrate with improved performance.

1.3 Objectives of This Work

The purpose of this project is to develop new MEMS technologies, and to apply them to fabricate RF inductors, RF resonators and RF filters with high performance.

The main objectives of this work are given below:

- To analyze the difficulties in developing RF MEMS devices on silicon substrate.
- To develop new fabrication technologies aiming to reduce the substrate losses of RF devices.
- To apply the developed technologies to fabricate high performance RF inductors, which are benefited by the low substrate losses.
- To design and fabricate RF resonators and filters using the developed MEMS technologies, which can reduce the size of the devices and improve the performance.

1.4 Organization

Chapter 1 introduces the background of this work.

Chapter 2 reviews the state-of-the-art technologies used in MEMS and the current developments on RF devices. Since the work is to develop RF inductors, passive resonators and filters, we focus on the reviews of these three RF components. The proposed designs in this work are presented in the end of this chapter.

Chapter 3 describes the developments of new fabrication technology, which is SiDeox (Silicon Deep Etching and Oxidation). First, the optimized DRIE technologies are investigated. Afterwards, the technologies of well controlled thermal oxidation are described. By using the SiDeox process, the thick SiO_2 blocks are fabricated to be used for development of low loss RF devices.

Chapter 4 gives the analysis of layouts, loss mechanisms, modeling of RF spiral inductors built based on silicon substrate. Electromagnetic simulations are performed to validate the considerations during the design of RF spiral inductor.

Chapter 5 presents the fabrication processes of RF spiral inductors using developed MEMS technologies. The designed inductors are fabricated using MEMS fabrication faculties. The measurement and analysis results are reported at the end of this chapter.

Chapter 6 presents the design and fabrication of RF resonators and filters by taking advantages of developed electroplating technology. The new designed Conductor-Backed-Coplanar-Waveguide (CBCPW) resonators and filters are realized by SiDeox process and through-wafer electroplating. The fabrication, measurement and analysis are described in detail in this chapter.

Chapter 7 summarizes the contributions of this work and recommendations for the future work

Chapter 2

Literature Review and Proposals

In this chapter, the technologies used in MEMS and RF MEMS devices involving RF inductors, resonators and filters, are reviewed. Section 2.1 discusses the commonly used MEMS materials, followed by the important micromachining technologies including oxidation, lithography, bulk micromachining, and surface micromachining. At end of the section 2.1, the fabrication of forming silicon dioxide blocks is reviewed as a foundation for novel SiDeox fabrication process in this work. Section 2.2 describes the state-of-the-art developments of RF MEMS devices for RF inductors, RF resonators and filters. Section 2.3 proposes the development of micromachining technologies for RF MEMS applications.

2.1 MEMS Technologies

In the late 1980s, the design and manufacturing tools developed for VLSI was adapted to be used in MEMS. Instead of handling only electrical signals, MEMS also bring mechanical elements, some with moving parts, making possible systems such as miniature fluid-pressure and flow sensors, accelerometers, RF MEMS switches. Micro electro mechanical system, literally, involves electric, electronic and mechanical parts fabricated by IC processes (e.g. CMOS, BiCMOS or Bipolar) and micromachining processes (e.g. etching, bonding), thereby, realizing the fabrication of a complete system on chip. The MEMS devices involve both

electronic and non-electronic elements, and perform functions including sensing, signal processing, actuation, display and control.

Now MEMS is considered as a toolbox, a physical product, and a methodology all in one. The products fabricated by MEMS methods possess a number of distinctive features. These products are the miniature embedded systems involving one or many micromachined components or structures in order to enable higher level functions. They often integrate smaller functions into one package for greater utility, and also bring cost benefits. Like many other emerging technologies with significant future potential, MEMS is subject to a rising level of excitement and publicity. Because of its excessive optimism, any end users try to consider developing a MEMS solution or incorporating one into a design. In practice, a MEMS solution becomes attractive if it enables a new function, provides significant cost reduction, or both. Nowadays, MEMS products have existed in many environments, especially automotive, medical, consumer, industrial and aerospace.

The basic technologies involving in MEMS can be categories as follows:

- Lithography technologies, which consist of ultraviolet lithography, extreme ultraviolet lithography, X-ray lithography, and charged-particle-beam lithography for different applications.
- Wet micromachining technologies that comprise isotropic etching techniques, anisotropic etching techniques, and etch-stop techniques.
- Dry etching technologies that include physical etching such as ion etching and ion-beam milling, plasma etching, physical and chemical etching such as RIE, DRIE, and vapor-phase etching.
- Deposition technologies, which involve physical vapor deposition such as sputtering and thermal evaporation, chemical vapor deposition, sol-gel deposition etc.

- Special technologies for MEMS such as bulk micromachining based on wet etching and DRIE, surface micromachining, and LIGA micromolding.

Many methods used in the fabrication of MEMS are largely borrowed from the integrated circuit industry, in addition to a few others developed specially for silicon micromachining. Specialized processes such as anisotropic chemical wet etching, sacrificial layer etching, deep reactive ion etching, and wafer bonding etc., have been emerged for MEMS fabrications over the last years. In the following subsections, we will review some technologies used in MEMS in details.

2.1.1 Materials Used in MEMS

Micromachining processes are demonstrated in silicon, glass, ceramics, polymers, compound semiconductors, and metals. Because of the large momentum of the electronic integrated circuit industry and the derived economic benefits, silicon remains the primary material of choice for the MEMS.

Silicon itself exists in any of three forms: single crystalline, polycrystalline and amorphous. Single crystalline silicon is used to make the silicon substrate as circular wafers. Silicon oxide and silicon nitride are usually used as sacrificial layers and insulting thin films. Silicon dioxide can be achieved by oxidizing silicon at temperatures above 800°C, whereas the other forms of oxides are deposited by CVD (chemical vapor deposition). Silicon nitride is very effective as a barrier against mobile ion diffusion and alkaline solutions etching. But both of them are grown with large intrinsic stresses and should be annealed. Metals are widely used to construct MEMS devices structures. The choice of metal greatly depends on the final applications. Table 2.1 lists some metals that are usually used as electrical interconnects and adhesion layers. Al, Au and Cu are the most commonly used electrical interconnects metals

by taking the advantage of their low electrical resistivities. Cr and Ti are the well-known adhesion metals. Polymers commonly used in the form of polyimide or photoresist, are another much important materials for micromachining. Standard photoresist is spin-coated to a thickness varying from 1 μm to 10 μm, but special photoresist such as SU-8 can form layers up to 1 mm. However, the applications of polymers are generally limited because they shrink significantly after the solvent evaporates and can't sustain at the temperatures above 200°C [22].

Table 2.1: Metals deposited as electrical interconnects and adhesion layers

Metal	**Electrical Resistivity ρ (μΩ·cm)**	**Typical areas of applications**
Al	2.7	Electrical interconnects. Optical reflection in the visible and the infrared.
Au	2.4	High temperature electrical interconnects. Optical reflection in the infrared. Electrochemistry.
Cu	1.7	Low resistivity electrical interconnects.
Cr	12.9	Intermediate adhesion layer.
Ti	42	Intermediate adhesion layer.

Over the past years, micromachining methods have been applied to a variety of substrates other than silicon to fabricate passive microstructures, especially microwave passive devices. Materials including quartz, glass, silicon carbide, and gallium arsenide are widely used in different cases by taking advantage of their high resistivity property.

2.1.2 Oxidation of Silicon

One of the great virtues of silicon as the semiconductor material is that a high-quality oxide can be thermally grown on its surface. In dry oxidation, pure oxygen is used as the oxidant. Because silicon is readily oxidized even at room temperature, forming a thin native oxide approximately 20 Å thick, the oxygen must diffuse through the native oxide layer to reach the interface between oxide and silicon. With the oxide layer growing thicker, the oxidation growth rate decreases. The diffusion rate of oxygen through oxide can be significantly enhanced if there is water vapor present because water can break silicon-oxygen-silicon bonds, forming two OH^- groups. This broken-bond structure is relatively more mobile than molecular oxygen, hence the rate is higher. The thickness of dry oxidation is on the order of 10 nm, but wet oxidation can make thicker oxide up to 2 μm. The reaction relationships are as follows:

In dry oxidation: $Si+O_2 \rightarrow SiO_2$;

In wet oxidation: $Si+2H_2O \rightarrow SiO_2+H_2$.

The oxidized thickness can be calculated by Deal-Grove model of oxidation kinetics [23]:

$$x_f = 0.5A_{DG}\left[\sqrt{1+\frac{4B_{DG}}{A_{DG}^2}(t+\tau_{DG})}-1\right] \tag{2.1}$$

$$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{(B_{DG}/A_{DG})} \tag{2.2}$$

Table 2.2: Deal-Grove constants for dry and wet oxidation of silicon

Temperature (°C)	A_{DG} **(μm)**		B_{DG} **(μm²/hr)**	
	Dry	**Wet**	**Dry**	**Wet**
920	0.235	0.05	0.0049	0.203
1000	0.165	0.226	0.0117	0.287
1100	0.090	0.11	0.027	0.510

where x_f is the final oxide thickness, x_i is the initial oxide thickness, t is the oxidation time, τ_{DG} takes into account any initial oxide thickness x_i at the start of oxidation and is used to provide a better fit to the data in the thin oxide region. A_{DG} and B_{DG} are temperature-dependent constants shown in Table 2.2.

The ratio of silicon thickness, x_s, converted to resulting oxide thickness, x_{ox}, is proportional to their respective densities: x_s=0.46x_{ox}. Thermal oxidation of silicon generates compressive stress in the silicon dioxide film, because silicon dioxide molecules take more volume than silicon atoms, and there is a mismatch between the CTE (coefficients of thermal expansion) of silicon (CTE: 2.6×10^{-6}°C^{-1}) and silicon dioxide (CTE: 0.7×10^{-6}°C^{-1}) [24]. Therefore, after thermal oxidation, an anneal process is needed to minimize the compressive stress. The anneal process is to keep the oxidized wafer in inert gas atmosphere at high temperature for a period in order to relax the stress. Normally, the anneal process is carried out in N_2 gas at above 1000°C.

2.1.3 Bulk Micromachining

In bulk micromachining, three-dimensional features are etched into the bulk of crystalline or noncrystalline materials. In wet bulk micromachining, features are sculpted in the bulk of materials by using orientation-dependent (anisotropic) or orientation-independent (isotropic) wet etchants. Wet etching works very well for etching thin films on substrates, and can also be used to etch the substrate itself. The problem with substrate etching using isotropic etching process is that it will cause the undercutting of the mask layer by the same distance as etching depth. So anisotropic etching is usually adopted to form regular substrate structure. The principle of anisotropic and isotropic wet etching is illustrated in the Figure 2.1.

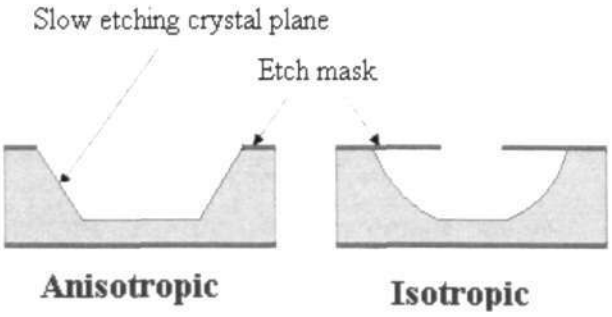


Fig 2.1: Difference between anisotropic and isotropic etching

Thanks to the good single crystal characteristic of silicon, the silicon substrate can be anisotropicly etched due to the different etch rates along different crystal plane. The classic anisotropic etchant for silicon is KOH solution. Etching rate towards <111> crystal plane direction is much slower than that towards <100> crystal plane direction due to the different densities of covalent bonds. As a result, an inverted-pyramid pit, which is shown in Figure 2.2, will be formed. In Figure 2.2, the width of the square cavity on the bottom, W_0, is completely defined by the etch depth, Z, the mask opening W_m, and the sidewall space, since these sidewalls cannot be vertical to the surface when etching holes or cavities slope. This results in a loss of chip space.

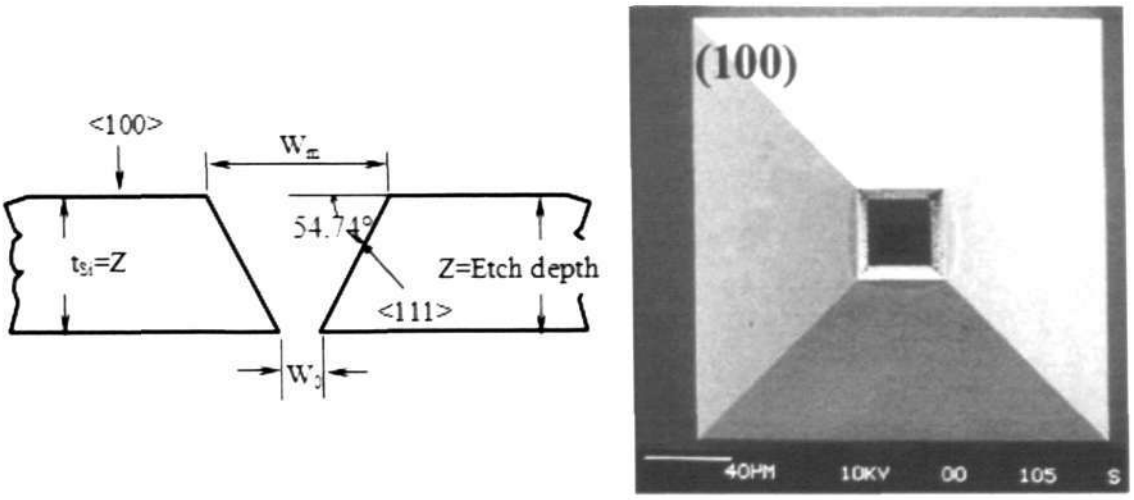


Fig 2.2: The inverted-pyramid pit etched by KOH wet etchant

Despite the introduction of etch-stop techniques with better control, wet micromachining exhibits several limitations, including large die areas, restrictive micro-structural shapes, not an applicable submicron technology and limited degree of freedom when attempting to move mechanical elements. Because of the above limitations, dry etching is required in many cases. Deep reactive ion etching (DRIE) of silicon as a replacement for wet etching eliminates many of the above mentioned restrictions, and allows perfectly vertical sidewall angles (which reduce device size) and randomly shaped planar geometries. This technology largely improves the feature resolutions and obtains vertical sidewalls for deep etching in the substrate.

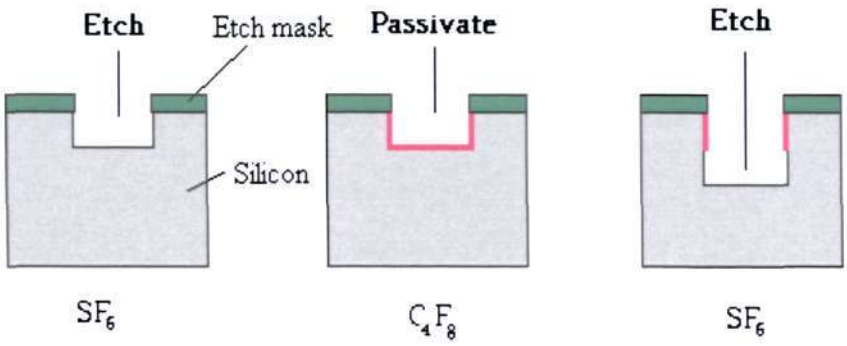


Fig 2.3: DRIE of silicon with process of alternating etching and passivation steps

Deep reactive ion etching using the Bosch process takes advantage of a side effect of a glow discharge, the tendency to create polymeric species by chemical crosslinking. The deposition of the created polymer from the passivating gas is used to great advantage such as protecting the sidewalls. DRIE is capable of anisotropically etching high aspect ratio trenches and etching rate is substantially larger than the conventional plasma etching or RIE. The etching cycle, typically lasting 10 to 15s, uses SF_6 to etch silicon. In the passivation cycle, typically lasting 5-10s, an around 10nm layer of fluorocarbon polymer, is plasma deposited using C_4F_8 as a source gas. In the followed etching cycle, energetic ions (SF_x^+) remove the

protective polymer at the bottom of the trench. The processes of alternative etching and passivation are shown in Figure 2.3. The repetitive alternations between etch and passivation steps results in a very directional etch at rates between 1.5 and 4 μm/min.

2.1.4 Surface Micromachining

In contrast to bulk micromachining, which can be considered as a subtractive process in the substrate, surface micromachining features are built up, layer by layer, on the surface of a substrate. The basic processes of surface micromachining include pattern transfer to sacrificial layer, deposition, and selective etching of structural material and sacrificial material. Fully integrated surface micromachined MEMS employs standard circuit interconnects to wire the MEMS devices to the on-chip electronics, yielding connections with the minimum possible capacitance. Many techniques are used for surface micromachining to complete a fabrication such as physical vapor deposition, chemical vapor deposition, RIE.

2.1.5 Silicon Dioxide Blocks Fabrication

The fabrication of silicon dioxide blocks is quite challenging using micromachining process, but it very useful and unique process for some MEMS applications in term of its thermal and electrical properties. Quite a few efforts have been conducted on this research area in recent years. H.R.Jiang et.al have fabricated 20 μm thick oxide blocks on SOI wafer [25] and bulk silicon wafer as the sacrificial material for an electrostatic torsional actuator application [26]. In his study, the DRIE was used to create a narrow trench-beam structure firstly, followed by thermal oxidation to refill the deep trenches. But the trenches were not totally filled by thermal oxidation. The small gaps existed, so a LPCVD oxide refilling was adopted to further seal the gaps after oxidation. Finally, the oxide blocks were planarized by CMP

process. After the top devices were completed, the oxide blocks were removed by wet etching. It is a smart way to create the thick silicon dioxide as the bottom for surface micromachining. The thick silicon dioxide as sacrificial material is much better than normally used polymers in terms of the mechanical and thermal properties. A similar work has also been done by C.Zhang and K.Najafi [27]. Thick silicon dioxide blocks have also been fabricated by H.Ou et.al, in which anodization was used to produce 20 μm deep porous silicon. Then thermal oxidation was performed to oxidize the porous silicon, and finally the 20 μm thick silicon dioxide blocks were created [28].

In this work, the thick silicon oxide blocks have also been fabricated by SiDeox process, which is to optimize the silicon trench-beam geometry in order to fully refill the trenches after DRIE. No gaps found after thermal oxidation. The oxide blocks are used as the substrate for low-loss RF inductors. The detailed processes will be described in the following Chapters.

2.2 Reviews on RF MEMS Devices

With today's rapid expansion of the wireless communication industry, integrated circuits are being driven to higher levels of integration by consumer market desires for products of high performance, low cost, light weight, small size, and the minimum power dissipation. Wireless communication, especially RFICs as one of the field in MEMS applications, has been largely exploited because of the advantages of integration. MEMS technologies can minimize the device structures and improve the performance of the devices. The less external components exist, the smaller the size of the circuit board and the lower the power consumption. Integration also enhances the reliability and robustness of the end products.

MEMS technology is increasingly applied in radio frequency field and a number of RF MEMS devices have been developed in the last decade. The typical devices are RF switches, tunable capacitors, high-Q mechanical resonators, micromachined transmission lines, and on-chip inductors. By taking advantages of these high performances of such basic devices, various MEMS components for RF circuits including RF MEMS filters, phase shifters, VCOs, LNAs and so on, can be made. The final aim of research on RF MEMS is to realize the integration of whole RF front-end and data processes stage on the same substrate, which is known as the system on-chip.

With the great developments of such devices including resistors, transistors, and capacitors, it is becoming increasingly more challenging to add inductors and transformers to the family of available design components, thus allowing the use of passive filtering, impedance matching, inductive loading, and other techniques that until now have not been available at the integrated circuit level. This work is focused on the development of fabrication technologies, especially for RF inductors, RF resonators and filters. The following sections give a brief introduction of the developed RF devices in the past.

2.2.1 RF Inductors

2.2.1.1 Applications of RF Inductors

The characteristic function of an inductor is to store magnetic energy in high operating frequency, so that high frequency signal can not pass through the inductor. On the contrary, a capacitor stores electric energy in low operating frequency and acts as short circuit at high frequency. When an inductor combined with a capacitor at certain frequency, the stored magnetic energy and electric energy will transformed to each other, thus a resonating circuit tank is formed, and the signal only can pass through the circuit under certain frequency range.

The principle of various electronic filters lies in these phenomena. However, in the high frequency range, the distributed components in the devices can not be ignored to any further extent, that means, the inductor and capacitor can not be looked as the purely function of inductor and capacitor. The distributed capacitance in an inductor, the distributed inductance in a capacitor, and the distributed resistance in both of them must be considered. One parameter used to evaluate the quality of an inductor and a capacitor is the quality factor. The higher the quality factor is, the better the performance of these devices is.

Figure 2.4 shows an application of RF inductors, a two-poles RF signal filter. All the inductors (L_1, L_2) in the filter can potentially be replaced by MEMS high-Q integrated inductors, and the variable capacitors (C_3) can be replaced by MEMS tunable capacitors.

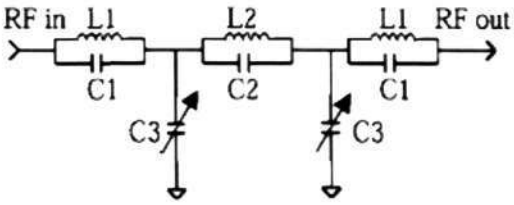


Fig 2.4: RF inductor application in a RF filter

It is clear that the quality of the filter is determined by the quality of every RF components, that is, the quality factors and self-resonance frequencies of the inductors and capacitors.

Figure 2.5 gives the application of inductors used in a low noise amplifier. Three inductors (L_c, L_b, L_e) are shown in this circuit that is connected to a DC voltage supply, V_{cc}.

In this circuit, the inductors (L_c, L_e) that connect to emitter and connector see one-port ac grounded. The base inductor (L_b) is serially connected in the circuit. The inductors L_b and L_e together with the parasitic capacitance between base and emitter, C_{be} of the transistor, resonate at certain frequency to match the input impedance by the inductive degeneration

method, while the inductor L_c functions as a tuned load. The inductors L_c and L_e, whatever they function as a load or emitter degeneration, are one-port ac grounded. This allows increased output swing, since there is no DC voltage drop across the inductors if they are ideal devices. Similarly, the inductor L_b also has no dc drop across it.

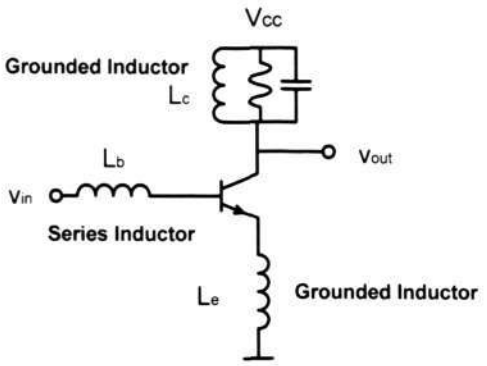


Fig 2.5: Inductors used in LNA circuit

The advantages of using inductors are unique:

- Parasitic capacitances are resonated out for matching the network.
- It provides the bias current with no DC drop, improving the linearity.
- The emitter degeneration increases the linearity without an increase in noise.

However, if the performance of the inductors is not ideally, which means the parasitic resistance and capacitance are significant at the high operating frequency, these advantages will be largely affected. A balanced tuned amplifier with a gain of 14 dB centered at 770 MHz was been implemented by using a 100 nH suspended inductor [29].

RF inductors are indispensable in an oscillator circuit. The basic structures of LC oscillators consist of an active circuit to amplify the input signal and a frequency selective network to select the desired frequency range, while they construct a ring for the signal to oscillate, as shown in Figure 2.6.

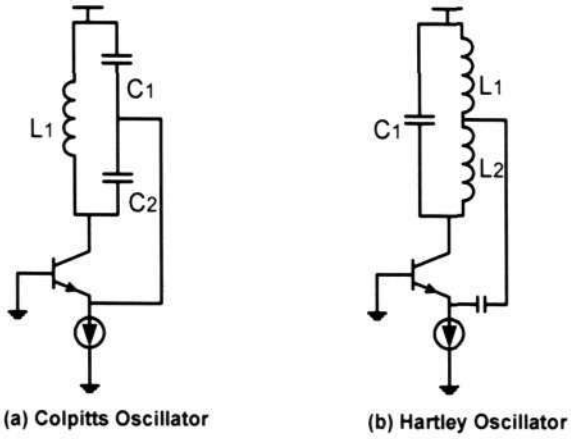


Fig 2.6: Inductors application in oscillators

In this kind of circuit, the oscillating frequency is ideally expected at a single frequency. But an actual oscillator has a spectrum that exhibits skirts around the carrier frequency because of the phase noise in the circuit. The phase noise of LC oscillators usually depends on their qualify factor. Intuitively, the LC resonating tank is expected to be a high quality factor. The sharper the resonance is, the lower the phase noise skirts are. So the inductors with high quality factor will improve the performance of the whole circuit. A 1.8 GHz low-phase-noise CMOS voltage controlled oscillator with phase noise as low as -116 dBc/Hz with an offset frequency 600 kHz was realized by using hollow spiral inductors [30].

Except for filters, low noise amplifiers, and oscillators, almost all of RF front-end devices such as low-power converters, need high Q inductors as well.

2.2.1.2 Development on RF Inductors

On-chip inductors, compared to the transistors and resistors, which are easily integrated on silicon chip due to the research done for microprocessors and memory chips over the past several decades, have not been used in microprocessors or memories. But they are increasingly employed in radio frequency circuits for wireless communication. Consequently,

for the past decade research activity has increased in the design, modeling, optimization, and fabrication based on the MEMS technology.

In the mid-1960 s through the early 1970 s, both silicon and gallium arsenide substrates were studied for possible applications in high frequency microwave circuits. It was found that the substrate resistivity would need to be at least greater than 1000 Ω·cm to overcome the problem of substrate loss. This requirement can be easily satisfied by semi-insulating GaAs or glass since their resistivities can be high up to10^6 Ω·cm. However, this required value is difficult for a regular device on silicon to achieve because the resistivity of average silicon wafer varies from 1 Ω·cm to 200 Ω·cm for a modern silicon process technology.

With the dramatic improvement of bipolar and CMOS technology in the past decades, silicon microwave integrated circuits have increasingly become attractive for the existing wafer foundry for applications in integrated circuits, and it becomes possible to add integrated inductors to the available components for integrated circuits on silicon substrate.

The original research of RF inductors on silicon was investigated by Nhat M. Nguyen and Robert G. Meyer, University of California, Berkeley, in 1990 [31]. Before that, RF inductors were almost fabricated on ceramic and GaAs substrates because of the low resolution of lithography on silicon processes and relatively low operation frequency of silicon devices limited the development of RF silicon inductors.

In 1990, due to the rapid development in silicon IC technologies such as bipolar, CMOS fabrication processes, it was possible to develop RF inductors and other passive devices on silicon substrate. Two inductors developed by Nguyen were square-spiral shape with a 6.5 μm metal width and 5.5 μm space. The metallization is aluminum with 1.7 μm thickness. The substrate is 500 μm thickness of p-type silicon with 14 Ω·cm resistivity. The bigger one

is nine turns with an outer dimension of 230 μm, while the smaller one is four turns with an outer dimension of 115 μm. The measured results of the bigger one were useful with the maximum Q value of 3 and inductance of 9.7 nH at 0.9 GHz. At the same time, a simple model of the RF inductor was developed too. The photograph and model of the inductors are shown in Figure 2.7.

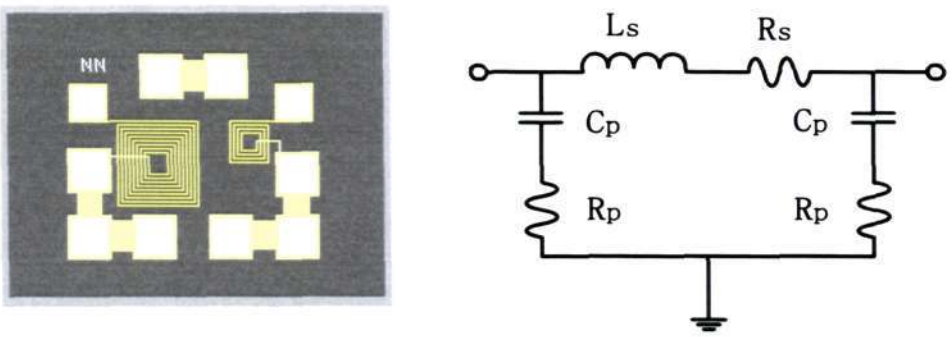


Fig 2.7: The fabricated inductor and model developed by Nguyen and Meyer [31]

AT&T Bell laboratories designed and fabricated a number of RF inductors in a complementary silicon bipolar process in 1996 [32]. Kirk B. Ashby et al. fabricated totally 16 inductors with different geometries using AT&T's CBIC-V2 technology. The gold material was used with a thickness of 6 μm and lower resistivity. Compared to the 1.7 μm thick aluminum in Nguyen's work, the series resistance of the metal layer is significantly reduced; consequently the quality factor is improved.

IBM T.J Watson research center pointed out a new method of fabricating silicon inductors by taking advantages of BiCMOS technology in 1995 [33-35]. Burghartz et al. designed spiral inductors with the structures of parallel stacked metal layers since a 0.8 μm BiCMOS technology which can build up to five-level metal layers on silicon substrates was commercially available. Normally, a spiral inductor consists of two metal layers that are top spiral routing and underpass. But the inductors developed in the multilevel BiCMOS

technology have more than two metal layers and the layers except for the underpass are connected together through dense via arrays. Various inductors by interconnecting different metal layers through via holes were fabricated. Figure 2.8 shows the cross section of one type of the fabricated inductor's structure, in which the first metal layer M1 is not used for getting a larger separation between inductors and silicon substrate.

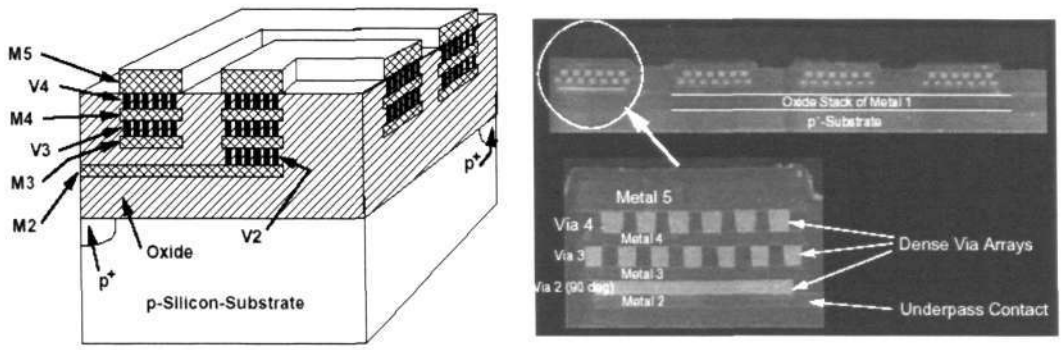


Fig 2.8: The cross section pictures of multilevel interconnected inductor [33]

The inductors with the parallel-interconnected metal layers have an effective metal thickness double than that of normal inductors, so the series resistance is reduced. The effect of shunt parasitic capacitance in the substrate should be removed as much as possible because it can decrease the resonant frequency of the inductors. It achieved by using a minimum doping concentration under the inductor fabricated by BiCMOS technology (i.e., a high value of substrate resistance under the inductor), so that the self resonance occurs mainly via the small inter-wire capacitance instead of via the comparably much larger shunt parasitic capacitance [36].

Ferenc Mernyei et al. reported another kind of fabricated inductors, while reducing the substrate losses by using BiCMOS technology in 1998 [37]. The schematic fabrication of such inductors is illustrated in Figure 2.9. The surface of the p-type substrate is firstly heavily doped as p^+ layer, so that the eddy current in the substrate flows in the doped layer.

Then the doped p^+ layer is broken by heavily doped n^+ regions to form some p-n-p junctions, thus the eddy current can not flow in the doped p^+ region. Consequently, the substrate losses are reduced. Using this method, the quality factor increases from 5.3 to 6 at 3.5 GHz.

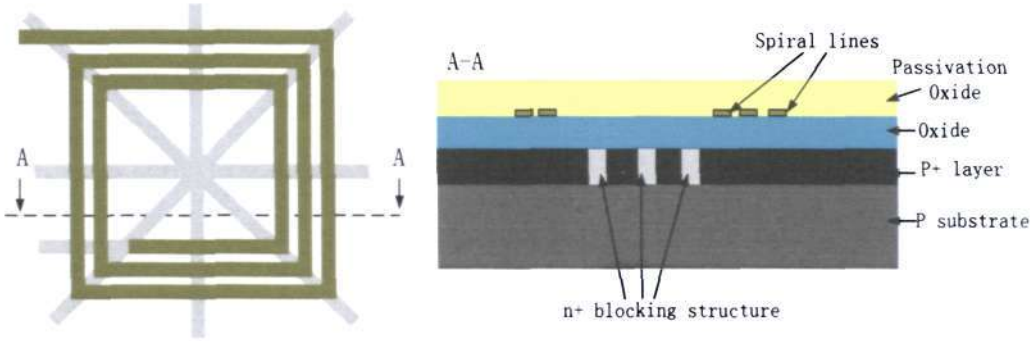
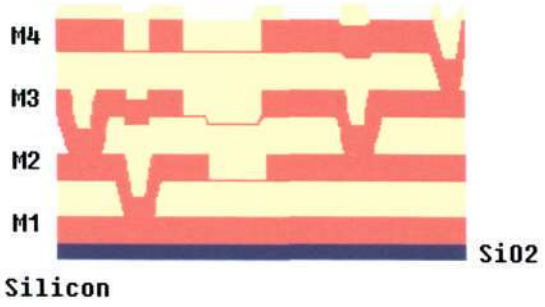


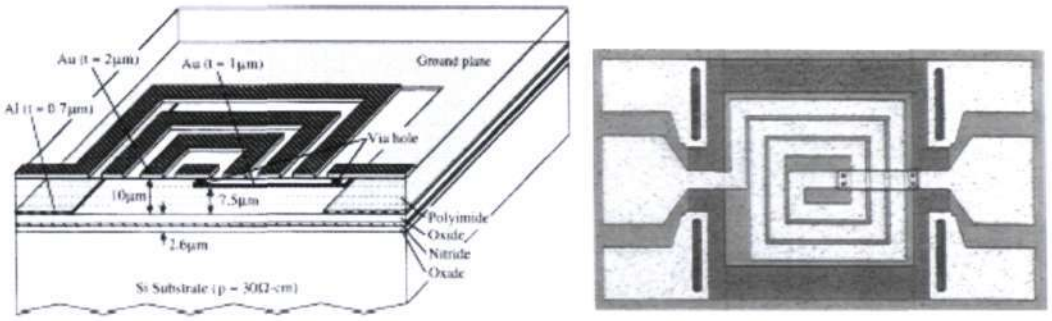
Fig 2.9: The schematic structure of inductors developed by F. Mernyei [37]

In 1992, Arnold et al. developed RF spiral inductors in multi-chip module technology [38]. In his work, thin films of aluminum-polyimide deposited implementation were applied to construct multi-layer interconnects. Four aluminum metal layers including ground plane (M1), power plane (M2) and two signal routing layers (M3, M4), which were separated each other by polyimide material, were deposited on an oxide isolated silicon wafer. The schematic of the aluminum-polyimide MCM interconnection structure is shown in Figure 2.10 (a). It can deposit thicker metal films about 3 μm and interlayer polyimide of 6 μm than those of CMOS and bipolar IC, hence reducing the parasitic capacitance and series resistance. But the polyimide material also caused some problems such as mismatch of expansion coefficient and moisture adsorption. Most importantly, the close proximity between ground plane and signal plane significantly decreases the performance of the inductors to about 50% of the value with no ground plane. For the designed inductor with 140 μm separated center distance and 5 turns, the measured inductance is only 4.03 nH compared to the designed value of 10.24 nH.

Larry Zu, Yicheng Lu et al. in 1996 also fabricated spiral inductors on multi-chip module silicon substrates [39]. A similar work as Arnold's was reported by KenJi Kamogawa et al. in 1998 [40], in which a ground plane and thick polyimide layers overlay on a conductive silicon substrate. The performance of spiral inductors is improved because of the ground plane shield and thick dielectric layers, as shown in Figure 2.10 (b).



(a) Schematic structure of an inductor with multi metal interconnect layer [38]

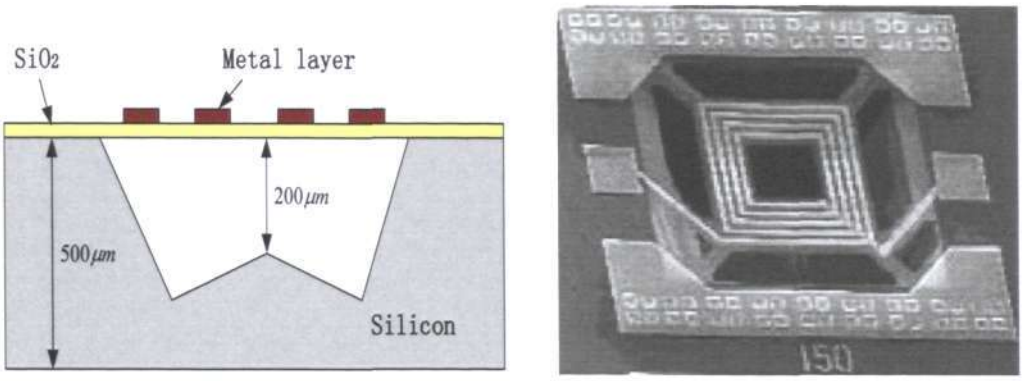


(b)Fabricated inductor with a ground plane [40]

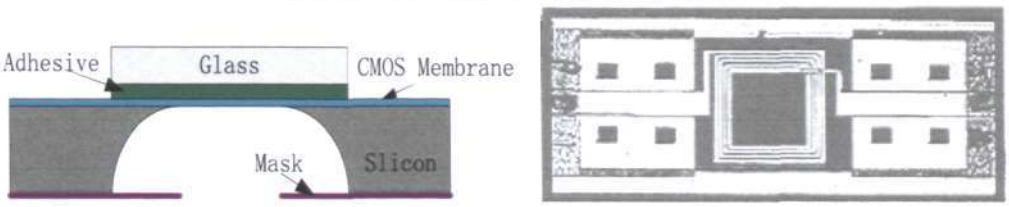
Fig 2.10: Fabricated inductor using Al-polyimide MCM interconnect technology

The most important difficulty in developing an integrated silicon inductor is the loss due to the semi-conducting substrate. It is natural to fabricating inductors with a micromachined substrate so that the loss is reduced. The first known work about micromachined inductors is developed by Chang et al. in 1993 [29]. As shown in Figure 2.11 (a), a planar inductor is suspended on a thin SiO_2 membrane using KOH etching and by defining small holes in the

SiO_2 layer. The CMOS silicon substrates is anisotropic etched by KOH that naturally stops at the <111> crystal planes. A 200 μm deep rectangle cavity is formed under where the spiral inductor is located. A 100 nH inductor of a 20 turns square spiral of 4 μm wide lines was designed with a resonant frequency 3 GHz, which is only 800 MHz before the removal of the underlying substrate. A similar work was done by Sun et al.[41].



(a) Wet etching from top side [29]

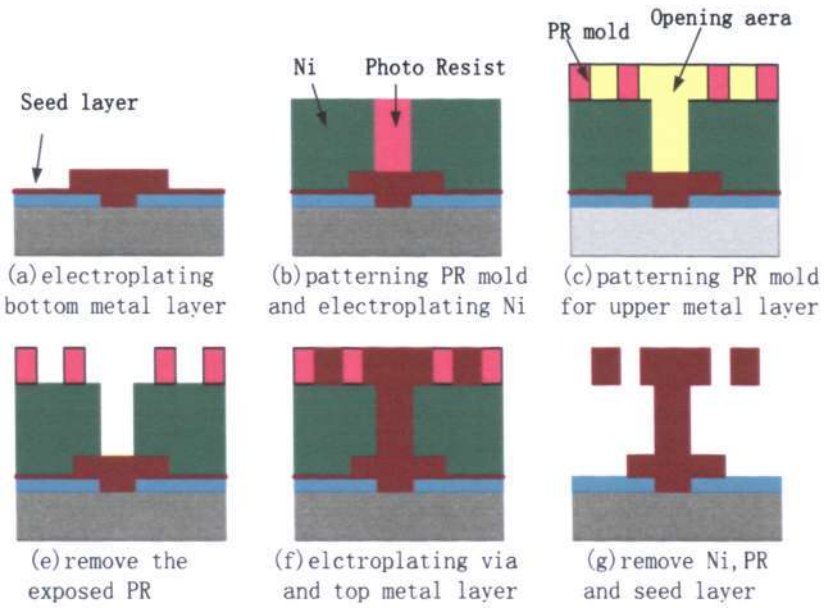


(b) Wet etching from back side [42]

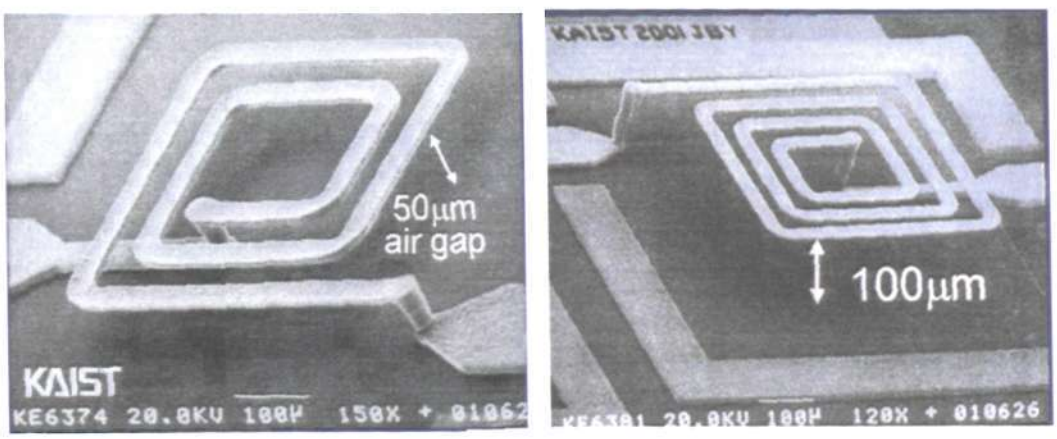
Fig 2.11: MEMS inductors by wet etching

In 1999, Mehmet Ozgur et al. built spiral inductors with backside etch using 1.2 μm CMOS process, as shown in Figure 2.11 (b) [42]. Firstly, they attached glass material on top of the area to be micromachined. This process is used to ensure the suspended membrane planar under internal stresses in the CMOS layers. Then the silicon is etched through the exposed areas in the backside using isotropic silicon etchant (XeF_2). A quality factor of 10 is measured at 4.6 GHz for an 8.9 nH inductor.

A special kind of micromachined inductors was developed by Jun-Bo Yoon et al. in 1999. This research group at Korea Advanced Institute of Science and Technology, reported a 3D electroplating method using a novel sacrificial metallic mold [43]. After that, a series of inductors were fabricated based on this technology [44-46]. The fabrication processes are shown in Figure 2.12 (a).



(a) Fabrication processes [43]



(b) Fabricated inductors [44]

Fig 2.12: Floating inductor fabricated by electroplating

The processes start with plating the bottom metal layer after the deposition of seed layer. Secondly, nickel is plated through patterned photoresist mold as the sacrificial metallic mold. Next, the resist mold on top of the plated nickel is patterned and the exposed part is removed for plating of top metal and via holes. Finally, the plated nickel material is selectively etched. Figure 2.12 (b) shows the fabricated inductors using this process. The main advantage of this method is that multilevel electroplating can be done easily, so the metal thicknesses of the fabricated inductors can easily go up to 20 μm, and the inter gaps between layers relatively large depend on the plated thick nickel material.

In 2000, H Jiang et al. fabricated suspended spiral inductors with an underneath 30 μm deep cavities [47-48]. Such deep cavities were formed by fabricating silicon dioxide blocks those are then etched away after the top inductors were completed. The schematic and fabricated inductors are shown in Figure 2.13. Different from the inductors developed by Chang, this kind of inductors uses polysilicon spirals coated with copper by electroless plating, and the inner surface of the cavity is also coated by electroless copper plating. The surface-conducting cavity functions as a RF ground plane, which is much better than the ground metal layer of inductors developed by Arnold using MCM technology [38], because the bottom of the cavity is 30 μm far away from the suspended inductor.

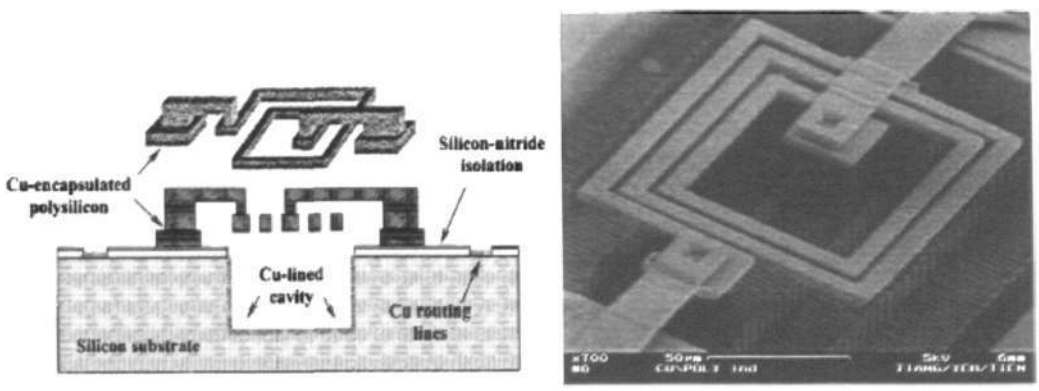
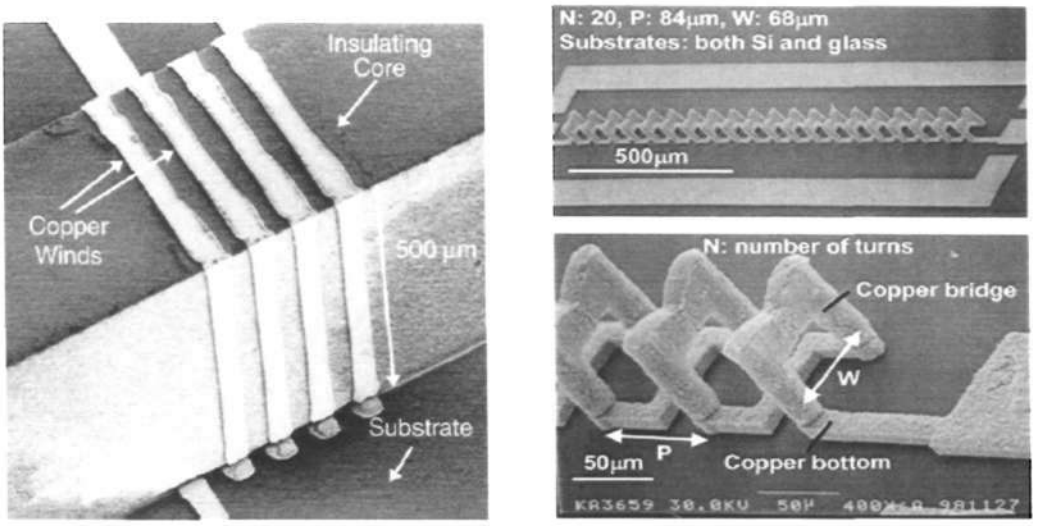


Fig 2.13: Floated MEMS inductor fabricated using polysilicon [47]

The developed RF inductors are almost the spiral structure because it is easy to be integrated with other circuit devices on the same substrate. Three dimensional inductors are seldom developed because the fabrication processes are very difficult and hard to be integrated with other planar devices. However, three dimensional inductors such as the solenoid structure have special advantages because the magnetic flux are most go through the center of the solenoid, which can not penetrate into the substrate so that the substrate losses could be much less.

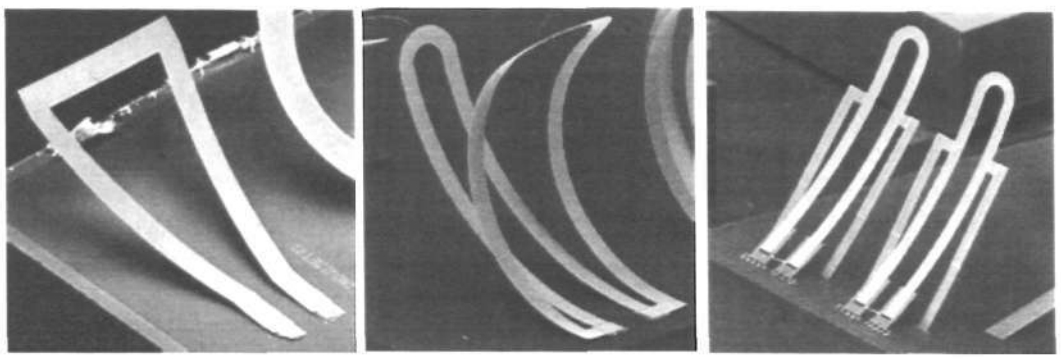


(a) 3D inductor developed by UC Berkeley [49] *(b) Solenoid inductor plated [51]*

Fig 2.14: 3D coil inductors developed by electroplating

Livermore National Laboratory and UC Berkeley fabricated the first three dimensional coil inductors on silicon in 1998 [49], whose structure is shown in Figure 2.14 (a). The bottom traces of the inductors are firstly electroplated to 5 µm copper metal. After that, the core of the inductor is formed from an alumina sheet which is cover with a 75 µm insulating adhesive film and then diced into 500 µm wide strips, finally centered on the bottom copper traces. The side and top copper traces of the core are electroplated like the bottom traces after a three-dimensional maskless direct-write laser lithography process [50]. A similar

work, which used multi-exposure and single development lithography method, was done by Jun-Bo Yoon et al [51]. In this method, the three-dimensional lithography for plating the side and top metal of the inductors is not realized by maskless laser lithography process. Instead, by shallowly exposing and deeply exposing to the desired parts of the deposited thick resist on the plated bottom metal, respectively, a three-dimensional resist mold for plating is formed. Finally, the three-dimensional inductors are finished using over electroplating, which are shown in Figure 2.14 (b).



(a) (b) (c)

Fig 2.15: Self-assemble 3D inductors

Recently, three-dimensional MEMS inductors, which use warping members to assemble themselves away from the substrate, were developed by V.M. Lubecke, B. Barber et al. [52]. By using two or more material layers deposited with different stresses, the inductors, which are made of polysilicon and Cr-Au metal layers, can be curled away from the substrate after etching away the oxide sacrificial layer. Figure 2.15 (a) shows the fabricated self-assembling inductors. The structures were formed as a 0.5 μm thick Cr-Au layer over a 1.5 μm thick polysilicon layer, patterned on a 2 μm thick sacrificial oxide over the substrate, with a final etch-release step to achieve the desired 3-D structures. Fabrication was carried out using MUMPS (Multi-User Microelectromechanical Process). The hair-pin structure shown in

Figure 2.15 (b) are using temperature variations which are environmental or localized joule heating effects induced by an applied DC current to create a relative angle between the two loops. Figure 2.15 (c) shows the structure replacing the contact pads by hinges, thus to reduce the parasitic effects due to the pads.

Three-dimensional inductors fabricated in this way can reduce the parasitic losses to the substrate; however, they do couple to each other through electromagnetic radiation resulted in EM interference in a transceiver system.

There is much work reported on inductors on different substrates in the last decade such as the inductors developed on GaAs substrate [53-54], SOI substrate [55], changing normal silicon to porous silicon and so on [56]. At the same time, modeling of the spiral inductors as a separated work was done in the past few years [57-60]. Even though so much work focuses on the development of RF inductors, this device is still the last passive monolithic component that needs intensive research to improve its performance. Currently, the interesting operation radio frequencies range from 1 GHz to 6 GHz. In such high frequency range, the inductances for many applications do not need to be very high, and are on the order of nano-Henry. But the quality factors require very high value (5-30, commonly depending on the final applications), because the devices are working with very weak signals.

2.2.2 RF Resonators and Filters

With the increased demand of broadband and mobile wireless communication systems, the need for high performance, low cost, low power, and small size micro-wave circuits becomes more pronounces. One of the most important components in a wireless system is the band-pass filter, which is both used in receiver and transmitter for keeping unwanted signals away from other parts of the system. These band-pass filters are also key elements

for future direct digital RF receivers. In order to achieve the superior performance required by these applications, the filters need to be designed with high quality factors.

RF resonators and filters, different with the lumped-element devices of circuit theory, use distributed elements including transmission lines, rectangular and circular waveguides, and dielectric cavities. Ideal lumped elements are usually unattainable at microwave frequencies, so distributed elements are more commonly used. In the lower frequency range, waveguide are large, very difficult to be integrated with other planar circuits and costly to be manufactured, so transmission line resonators are popular to be used in low frequency range. However, due to the development of micromachining technologies in the past years, researches have focused on silicon micromachined cavities and membrane resonators that can provide superior quality factors at micro wave frequencies [61-64]. But the waveguide resonators are not easy to be integrated into planar integrated circuits because they are normally not finished by planar processes. Now the popular resonators and filters are using microstrip and CPW structures. In the following, microstrip resonators and filters are reviewed.

2.2.2.1. Microstrip resonators

A microstrip resonator is any structure that is able to permit resonant oscillation of electromagnetic field at the specific frequencies. There are numerous forms of microstrip resonators. In general, microstrip resonators for filter designs may be classified as lumped-element or quasi lumped-element resonators and distributed line or patch resonators. Some typical configurations of these resonators are illustrated in Figure 2.16.

Figure 2.16 (a) and (b) are lumped-element or quasi lumped-element resonators, formed by the lumped or quasi lumped inductors and capacitors. They obviously resonate

at: $\omega_0 = \frac{1}{\sqrt{LC}}$. However, they may resonate at some higher frequencies when their sizes are no longer much smaller than the wavelength, thus, by definition, they are no longer lumped or quasilumped elements.

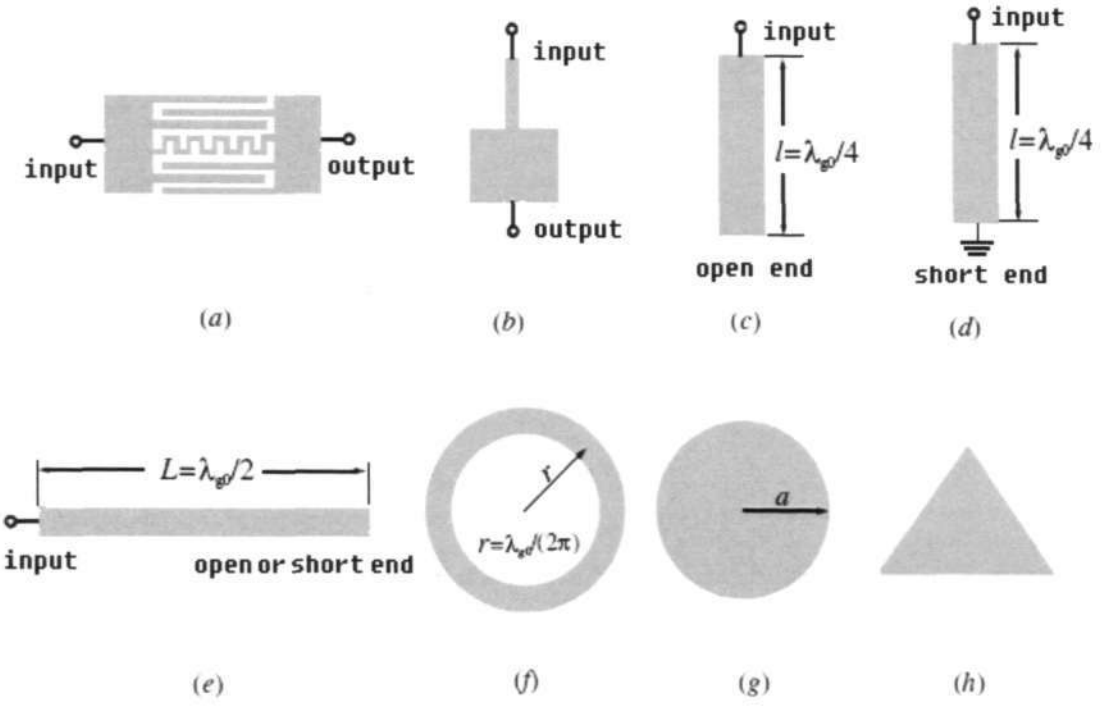


Fig 2.16: Typical microstrip resonators: (a) lumped-element resonator; (b) quasilumpedelement resonator; (c) $\lambda_{g0}/4$ line resonator (shunt series resonance); (d) $\lambda_{g0}/4$ line resonator (shunt parallel resonance); (e) $\lambda_{g0}/2$ line resonator; (f) ring resonator; (g) circular patch resonator; (h) triangular patch resonator.

The distributed line resonators shown in Figure 2.16 (c) and (d) are termed quarter-wavelength resonators. Their lengths are $\lambda_{g0}/4$, where λ_{g0} is the guided wavelength at the fundamental resonant frequency f_0. The open-end $\lambda_{g0}/4$ resonator achieves a series type of resonance, while the short-end $\lambda_{g0}/4$ resonator achieves a parallel type of resonance. They can also resonate at other higher frequencies when $f \approx (2n-1)f_0$ for n=2, 3……. Another typical

distributed line resonator is the half-wavelength ($\lambda_{g0}/2$) resonator, as shown in Figure 2.16 (e). Contrasted to $\lambda_{g0}/4$ resonators, the open-end $\lambda_{g0}/2$ resonator behaves as a parallel resonant circuit, while the short-end $\lambda_{g0}/2$ resonator behaves as a series resonant circuit. They can also resonate at $f \approx nf_0$ for n=2, 3…… [65]. It can be used in the filter designs by changing the line shape to many different configurations as filter implementations, such as the open-loop resonator [66].

The ring resonator shown in Figure 2.16 (f) is another type of distributed line resonator, where r is the median radius of the ring. The ring resonate at its fundamental frequency f_0 when its median circumference $2\pi r \approx \lambda_{g0}$. The higher resonant modes occur at $f \approx nf_0$ for n=2, 3……. Because of its symmetrical geometry a resonance can occur in either of two orthogonal coordinates. This type of line resonator therefore has a distinct feature; that is, it can support a pair of degenerate modes that have the same resonant frequencies but orthogonal field distributions. This feature can be utilized to design dual-mode filters. Similarly, it is possible to construct this type of line resonator into different configurations, such as square and meander loops.

Patch resonators are of interest for the design of microstrip filters, in order to increase the power handling capability [67-68]. An associated advantage of microstrip patch resonators is their lower conductor losses as compared with narrow microstrip line resonators. Although patch resonators tend to have a stronger radiation, they are normally enclosed in a metal housing for filter applications so that the radiation loss can be minimized. Patch resonators usually have a larger size; however, this would not be a problem for the application in which the power handling or low loss has a higher priority. The size may not be an issue at all for the filters operating at very high frequencies. Depending on the applications, patches may take different shapes, such as circular in Figure 2.16 (g) and triangular in Figure 2.16 (h).

These microstrip patch resonators can be analyzed as waveguide cavities with magnetic walls on the sides. The fields within the cavities can be expanded by the TM^{Z}_{nm0} modes, where z is perpendicular to the ground plane. For instance, the fields for each of the cavity modes in a circular microstrip patch (disk) resonator may be expressed in a cylindrical coordinate system.

2.2.2.2. Microstrip filters

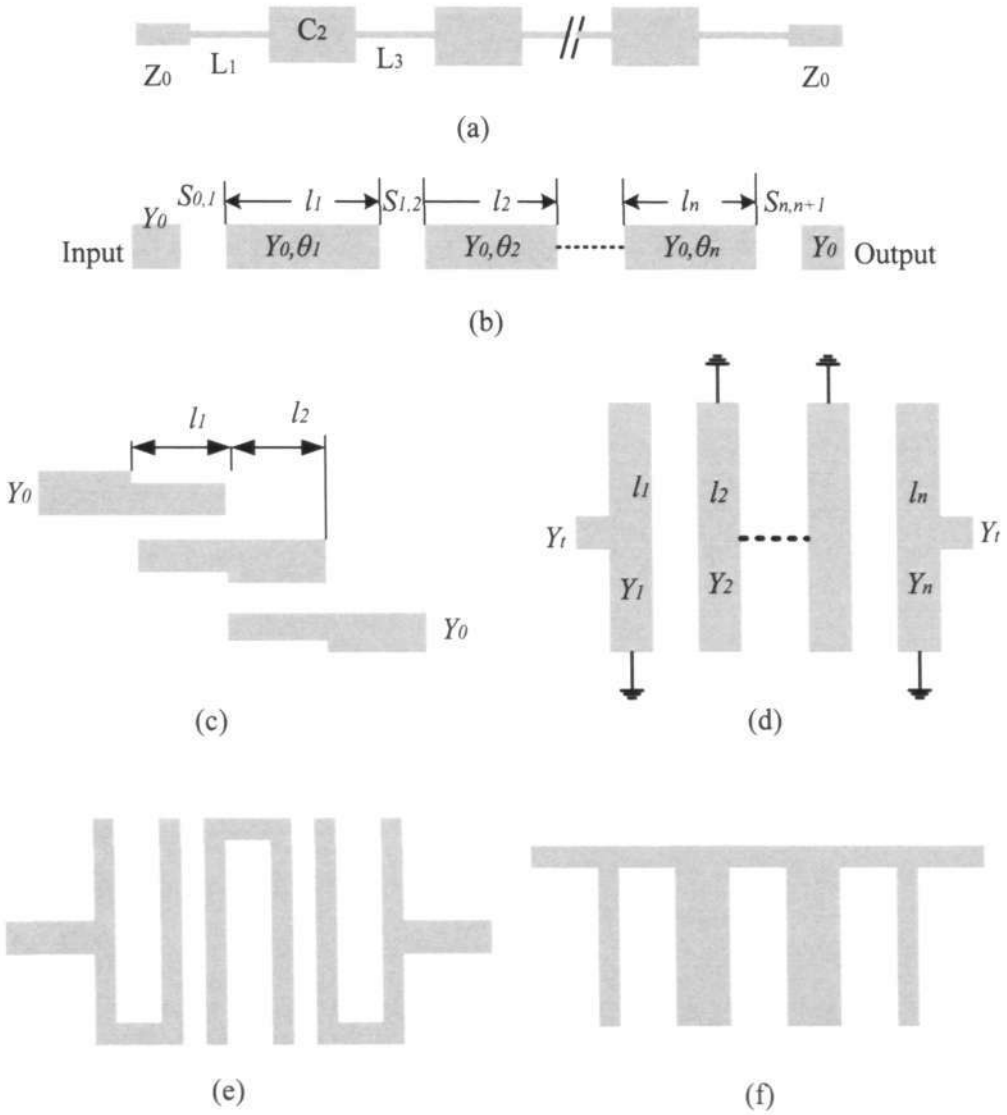


Fig. 2.17: Typical microstrip filters: (a) stepped-impedance microstrip filter, (b) end-coupled bandpass filter, (c) parallel-coupled microstrip filter, (d) interdigital microstrip filter, (e) hairpin line microstrip filter, (f) stub microstrip filter

The main design of microstrip filters is to find an appropriate microstrip realization that approximates the lumped-element requirement. The conventional microstrip realizations for the microstrip filters are stepped-impedance structures, end and parallel-coupled half wavelength resonators, hairpin-line structure, interdigital structure, and stub-line structure, which are widely used in many RF/microwave applications. Figure 2.17 shows these configurations of microstrip filters.

Figure 2.17 (a) shows a general structure of the stepped-impedance lowpass microstrip filters, which use a cascaded structure of alternating high and low impedance transmission lines. These are much shorter than the associated guided-wavelength, so as to act as semi-lumped elements. The high-impedance lines act as a series inductors and the low-impedance lines act as shunt capacitors. Therefore, this filter structure directly realizes the L-C ladder type of lowpass filter.

An end-coupled microstrip bandpass filter is illustrated in Figure 2.17 (b), where each open-end microstrip resonator is approximately a half guided wavelength long at the mid-band frequency f_0 of the bandpass filter. The coupling from one resonator to the other is through the gap between the two adjacent open ends, and hence is capacitive. In this case, the gap can be represented by the inverters. These inverters tend to reflect high impedance levels to the ends of each of the half-wavelength resonators. This causes the resonators to exhibit a shunt-type resonance [69].

Figure 2.17 (c) illustrates a general structure of parallel-coupled (or edge-coupled) microstrip bandpass filters that use half-wavelength line resonators. They are positioned, so that adjacent resonators are parallel to each other along half of their length. This parallel arrangement gives relatively large coupling for a given spacing between resonators, and thus, this filter structure is particularly convenient for constructing filters having a wider

bandwidth as compared to the structure for the end coupled microstrip filters described in above.

Figure 2.17 (d) shows a type of interdigital bandpass filter commonly used for microstrip implementation. The filter configuration, as shown, consists of an array of n TEM-mode or quasi-TEM-mode transmission line resonators, each of which has an electrical length of 90° at the midband frequency and is short-circuited at one end and open-circuited at the other end with alternative orientation. In general, the physical dimensions of the line elements or the resonators can be different, as indicated by the lengths l_1, l_2……ln and the widths W_1, W_2……Wn. Coupling is achieved by way of the fringing fields between adjacent resonators separated by spacing $S_{i,i+1}$ for i=1……n–1. The filter input and output use tapped lines with a characteristic admittance Y_t, which may be set to equal the source/load characteristic admittance Y_0. An electrical length θ_t, measured away from the short-circuited end of the input/output resonator, indicates the tapping position, where $Y_1 = Y_n$ denotes the single microstrip characteristic impedance of the input/output resonator. This type of microstrip bandpass filter is compact, but requires use of grounding microstrip resonators, which is usually accomplished with via holes. However, because the resonators are quarter-wavelength long using the grounding, the second passband of filter is centered at about three times the mid-band frequency of the desired first passband, and there is no possibility of any spurious response in between.

Hairpin-line bandpass filters shown as Figure 2.17 (e) are compact structures. They may conceptually be obtained by folding the resonators of parallel-coupled, half-wavelength resonator filters, which were discussed in the previous section, into a "U" shape. This type of "U" shape resonator is the so-called hairpin resonator. Consequently, the same design equations for the parallel-coupled, half-wavelength resonator filters may be used [70].

However, to fold the resonators, it is necessary to take into account the reduction of the coupled-line lengths, which reduces the coupling between resonators. Also, if the two arms of each hairpin resonator are closely spaced, they function as a pair of coupled line themselves, which can have an effect on the coupling as well.

Figure 2.17 (f) is the configuration of stub microstrip filter. It can behave as bandpass filter if the shunt stubs are short-circuited and $\lambda_{g0}/4$ long with connecting lines that are also $\lambda_{g0}/4$ long, or the shunt stubs are open-circuited and $\lambda_{g0}/2$ long, where λ_{g0} is the guided wavelength in the medium of propagation at the mid-band frequency f_0. When the stubs are open-circuited and $\lambda_{g0}/4$ long, or are short-circuited and $\lambda_{g0}/2$ long, the filter behaves as a bandstop filter.

2.3 Analysis and Proposals

2.3.1 Analysis of RF Inductors

We have reviewed the developed RF inductors based on silicon substrates fabricated using bipolar technology, BiCMOS technology, multi-chip-module technology, and micromachining technology.

The simplest fabricated inductors are to use the bipolar process. Its acceptable performance of the silicon inductors is due to the improvement of fabrication process such as the lithography resolution. However, the insertion loss is larger because silicon substrates consume a lot of power, even the loss can be reduced by increasing the thickness of metal layers.

The advanced BiCMOS fabrication process can built multi-layer devices by interconnecting through vias. By taking advantages of this property, the top metal layer of the RF inductors

based on silicon can be separated far away from the substrate, thus reducing the parasitic capacitance between the metal and substrate and the effective metal thickness is increased. However, the multilevel metal layers bring additional parasitic capacitance between the metal layers at the same time. The substrate still has much parasitic losses, which limit the improvement of the inductor performance.

Inductors, which are fabricated using the multi-chip-module process, are similar to those fabricated using CMOS multilevel interconnected layers. Compared to CMOS and bipolar, multi-module technology can deposit thicker metal films and interlayer polyimide, hence reduce the parasitic capacitance and series resistance. But the polyimide material also causes some problems such as mismatch of coefficient of thermal expansion and moisture adsorption. The losses due to silicon substrates still exist and largely restrain the quality of inductors.

MEMS technologies are very useful to reduce the substrate losses by modifying the substrate properties. The substrate could be removed by bulk micromachining such as top etching or bottom etching, resulted in the floating inductors and membrane inductors. The quality factors of inductors could be significantly increased since the substrate losses disappear. Using electroplating techniques, many kinds of 3D structures of inductors with high performance have been created. The advantages of these fabrication methods are unique for MEMS. However, they have fatal defects: poor mechanical strength and easy broken structures related to floating and membrane inductors, difficulty of integration to RFICs related to 3D inductors, and incompatibility with planar CMOS processes for other components of the integrated circuits. So in this work, we develop new MEMS fabrication technologies to overcome these shortcomings.

2.3.2 Analysis of RF Resonators and Filters

The conventional types of RF resonators and filters are reviewed, but they can not fulfill the demands for advanced RF circuits, because every simple structure has its own drawbacks. For example, the size of microstrip half wavelength open-ring resonators is too large to design a filter in high frequency range. The mean radius of the open-ring resonator could be as large as 16 mm if its fundamental model can work in the L-band [71]. Now the requirements of RF resonators and filters for RFICs or MMICs are miniature size and low loss with the increasing of operating frequency. To meet these requirements, many applications of microstrip circuits require the flexibility to use combination of different planar structures (microstrip, coplanar waveguide, etc.). Advanced designs of RF resonators and filters with high performance are created by the combinations of microstrip line structures (MSL), microstrip patch structures, coplanar waveguide structures (CPW), and conductor-backed coplanar waveguide structures (CBCPW). The coplanar waveguide structures are introduced into the designs because they can separate the circuit from its environment.

2.3.3 Proposals of RF Inductors, Resonators, and Filters

To develop passive RF inductors on silicon substrates, the serious problem is the substrate losses which can deteriorate the performance of these devices. The electromagnetic flux that propagates in the substrate generates eddy currents in the lossy substrate.

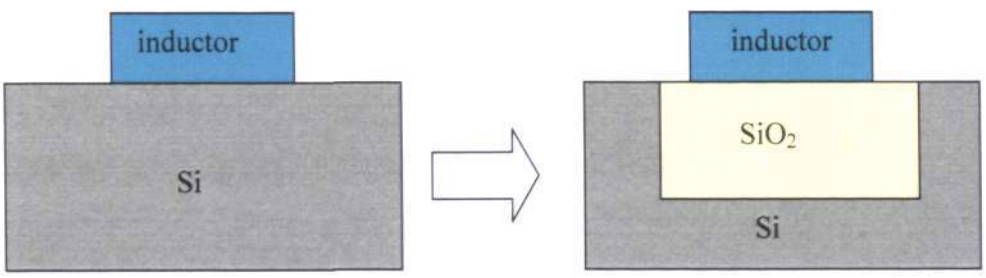


Fig 2.18: Proposed SiO_2 block in silicon substrate for RF inductor fabrication

To remove losses, the idea is to replace the bulk silicon substrate by thick silicon oxide block, which is schematically shown as Figure 2.18. Compared to normally used silicon substrate in semiconductor industry, silicon dioxide has much lower dielectric constant and is non-conductive. These properties prevent the induced eddy current and reduce the parasitic capacitance in the substrate.

Conventionally, the silicon dioxide layer is grown up to 2 μm by thermal oxidation. In this work, we explore MEMS fabrication technologies to build thick oxide block, which could be an attractive platform for the fabrication of passive RF devices with low losses.

In this work, novel RF resonators and filters are designed and fabricated with smallest sizes by combining CBCPW structures and microstrip structures. The advantages of these structures are: lowers Z_0, lessens dispersion, improves mechanical strength, allows easier implementation of mixed coplanar waveguide microstrip circuits, and provides a convenient heat sink. However, CBCPW structures also introduce certain important dangers. The most important problem is leakage of power into surface waves or into the dielectric region between the plates, resulting in unexpected or even harmful coupling to the neighboring transmission lines or devices. Many researches have been done on these leakage phenomena [72-75]. To solve the leakage problem, high-aspect-ratio electroplating technology is also developed to fabricate these devices, schematically shown in Figure 2.19.

The through-wafer electroplated vias electrically connect top and bottom ground, and are placed periodically along the propagation direction. The parasitic parallel-plate mode associated with the CBCPW structure, which normally propagate along various transverse directions inside the dielectric substrate, can be suppressed by the vias because they establish a RF short between the top CPW ground and substrate bottom ground. The dominant

propagation mode is the desired CPW mode along with the transmission line. Thus the power leakage due to the parallel-plate propagation mode is minimized.

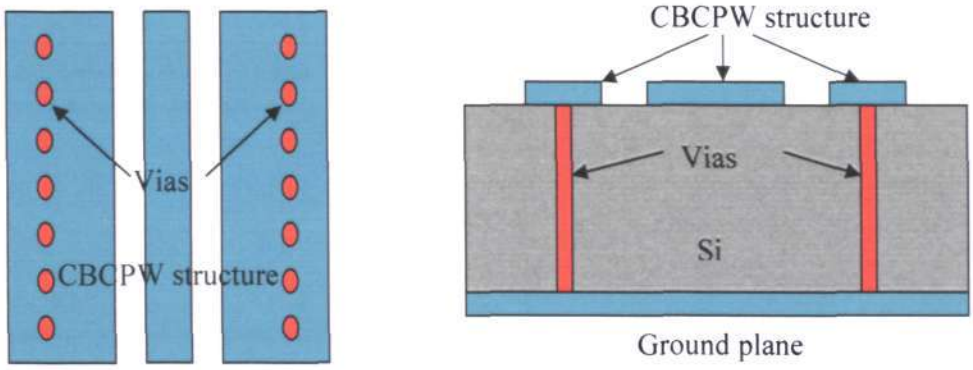


Fig 2.19: Proposed CBCPW resonators and filters with electroplating technology

2.4 Summary

In this chapter, MEMS technology is first reviewed. The materials used in MEMS, property of oxidizing silicon, bulk micromachining, surface micromachining, and the techniques of fabricating silicon dioxide blocks are briefly introduced. Thereafter, the applications of inductors such as filters, amplifiers, oscillators, are described, and the developments of RF inductors, filters and resonators are reviewed in terms of different fabricating technologies. The proposed new kinds of inductors, filters and resonators in this work are briefly introduced at the end of this chapter. It shows that the developments of RF inductors, RF filters and resonators are very active and meaningful especially by using micromachining technologies.

Chapter 3

Thick SiO_2 Blocks by Si DRIE and Thermal Oxidation Processes

In this chapter, the SiDeox process (silicon DRIE and oxidation) will be presented using MEMS technologies to fabricate thick silicon oxide blocks in the substrate. In section 3.1, the optimized DRIE process parameters will be described to deeply etch silicon to obtain vertical profile of the sidewalls. The multi-step release processes of DRIE are also developed in situ to etch the underneath silicon isotropically, leaving freestanding structure. In section 3.2, thermal oxidation for the deep etched silicon structure is investigated. With good control of the thermal oxidation, nano channels and nano silicon beams are achievable. Section 3.3 describes the formation of thick silicon oxide blocks. These fabrication processes can be used for RF devices applications because the thick silicon dioxide formation can largely reduce the substrate losses. In this work, we use it for RF inductor fabrication which will be described in following chapters. Section 3.4 concludes this chapter.

3.1 High Aspect Ratio DRIE Techniques

DRIE (deep reactive ion etching) process provides the MEMS community a method of fabricating high aspect ratio structures in silicon, with accurate critical dimension control, and a high degree of anisotropy. As MEMS technology matures, it places ever more demands on the higher degree of anisotropy and critical dimension control. Larmer and Schilp of Robert Bosch GmbH originally invented a fluorine-based chemistry process with

high anisotropy, by using the concept of alternate etch and passivation steps [76]. The basic principle of DRIE was reviewed in Chapter 2. The time-multiplexing etching technique utilizes an etching cycle flowing SF_6 and then switching to a sidewall passivation cycle using C_4F_8. During the subsequent etching cycle, the passivating film at the bottom of the trench is preferentially removed due to the ion bombardment, while preventing etching of the sidewall. Based on this concept, several companies have developed DRIE systems such as Plasmatlab 100 system of Oxford Plasma Technology, METlab system of Alcatel, SLR system of Plasmatherm, ASE system of STS. In this work, STS multiplex ICP system is used to develop high aspect ratio silicon structures, and Alcatel A601E ICP system is used for high aspect ratio deep etching with isotropic silicon etching for bottom silicon release.

3.1.1 Optimization of Deep Silicon Etching

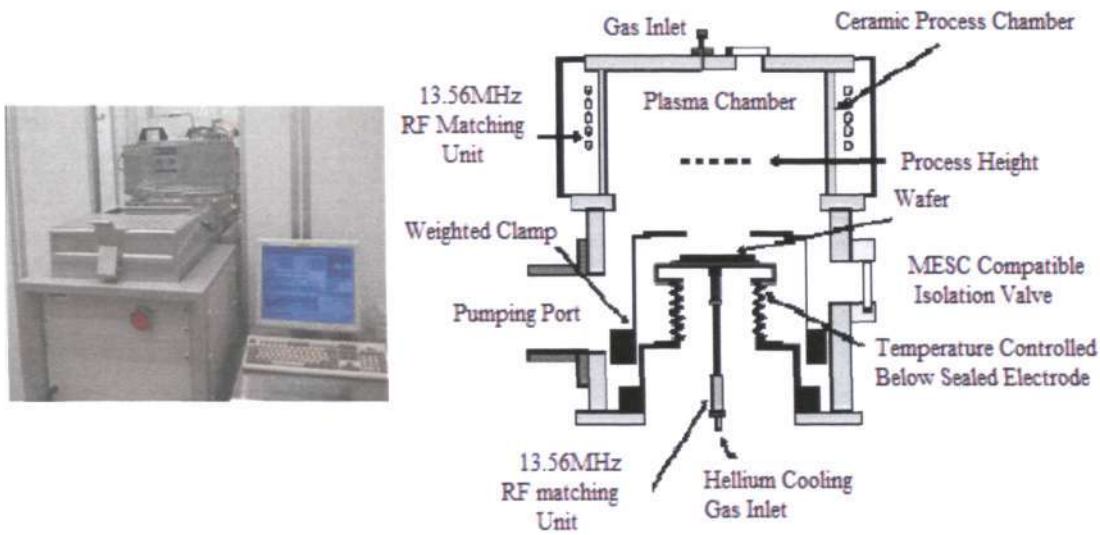


Fig 3.1: STS multiplex ICP equipment

As shown in Figure 3.1, the STS multiplex ICP includes two independent 13.56 MHz RF power sources: a 1000 W supply for the coil around the etching chamber and a 300 W supply connected to the wafer electrode. The coil power source which is also called

inductively coupled plasma source (ICP) is to generate a high radical and ion density. Another source called coupled plasma (CCP) is to direct the ions from the plasma glow region towards the wafer surface. The efficient inductive power coupling of the coil to the plasma allows high density plasma to be maintained. The helium backside cooling is to stabilize the wafer temperature during etching.

As geometries of device components become smaller, it requires silicon to be etched with vertical profiles. It is well known that many parameters including the flow rate, chamber pressure, electrode power, etching cycle and passivation cycle, affect the etching profile of silicon in the DRIE process. In this study, these process parameters will be investigated and optimized.

Single crystal silicon <100> wafers were coated with photoresist AZ7220 spun at 2000 rpm. The thickness of resist mask is around 2 μm. Then the wafers were baked on hotplate at 100°C for 90 seconds. The samples were exposed in a contact Karl Suss aligner with the i-line UV-lamp source and power density of 10 mW/cm^2 for 4 seconds. After post baking at 100 °C for 60 seconds, the exposed photoresist was developed with AZ300 for 90 seconds.

The parameter setting in this study is listed in Table 3.1. The coil power or ICP power is set at 800 W for both etching cycle and passivation cycle to generate high density plasma. The flow rates of etching gas SF_6 and O_2 are set at 130 sccm and 13 sccm, respectively. The flow rate of C_4F_8 for passivation is set at 100 sccm. The chamber pressure is set at 15 mTorr by automatic pressure control valve (APC). Etching time is 8 seconds and passivation time is 5 seconds for every cycle. The temperature is set at 20°C by the back side helium cooling system. In order to obtain the desired vertical sidewall of the deep etched channels, the platen power is varied from 10 W to 100 W for etching cycle. During passivation cycle, the platen power is switched off.

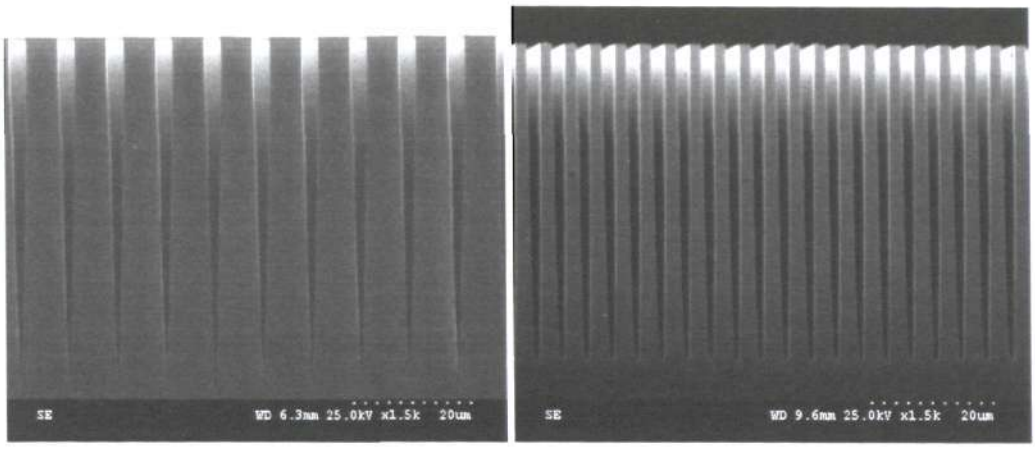
Table 3.1: Variables setting during DRIE process

	Etching	Passivation
Coil Power	800W	800W
Platen Power	Varied	—
SF_6	130sccm	—
O_2	13sccm	—
C_4F_8	—	100sccm
Pressure	15mT	15mT
Time Cycle	8s	5s
Temperature	20°C	20°C

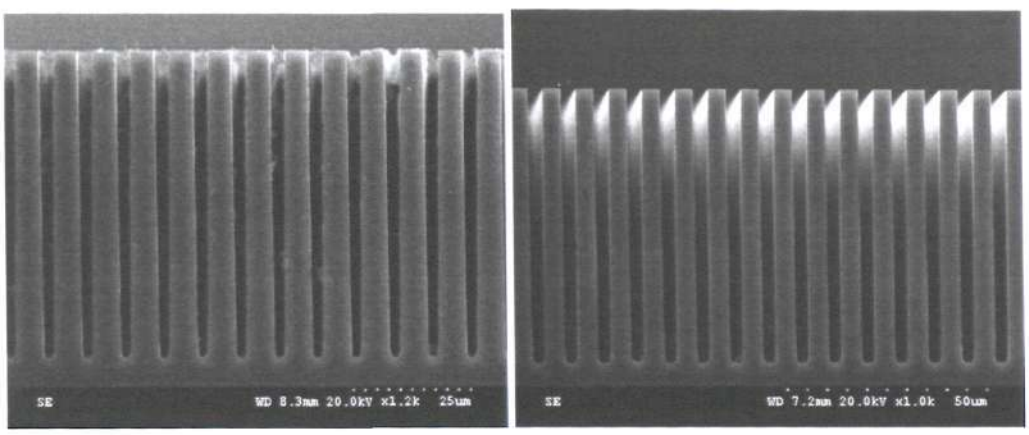
The samples are patterned with 2 μm opening mask and etched for 30 minutes. The etched depth is about 65 μm, the aspect ratio is as high as 32. For the first sample, the platen power is set at 10 W. The etched result is seriously positive tapered, shown as Figure 3.2 (a) which has a profile angle 88°. The second sample is etched at platen power 50 W. Shown as Figure 3.2 (b), the tapered shape is minimized to a profile angle 88.9°. By further improving the flatten power to 80 W, shown as Figure 3.2 (c), the profile angle is 89.3°. The last sample is etched with 100 W flatten power. Shown as Figure 3.2 (d), the profile turns from positive tapered angle to vertical angle. The definitions of positive and negative profile are illustrated as the sketch in Figure 3.3.

The high platten power can turn the positive profile to a straight one. The reason can be explained. During DRIE process, the passivation layer thickness is mainly controlled by the pressure and time of the deposition cycle. The ion bombardment energy is mainly controlled by the platen power. As the etching depth increases, the transportation of reactive etch species to the bottom of the trenches and the evacuation of the etched products out of the trenches become more difficult. So the efficiency of the ion bombardment weakens, so that the energy of these ions is not enough to etch away the passivation layer in the bottom of the

channels, finally leading the positive tapered shape or even early termination of etching. By increasing the platen power, the energy of the ion bombardment on the bottom of channels is increased. Accordingly, the higher platen power causes a less positively tapered profile.

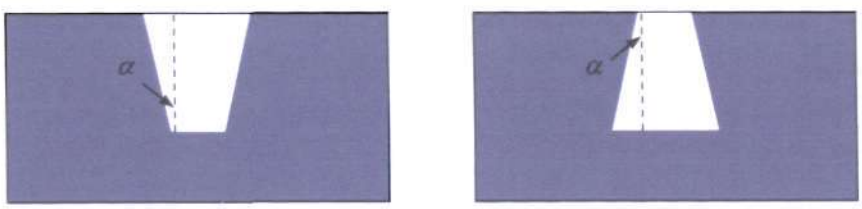


(a) profile angle 88°, platen power 10W *(b) profile angle 88.9°, platen power 50W*



(c) profile angle 89.3°, platen power 80W (d) profile angle 89.8°, platen power 100W

Fig 3.2: The side wall profiles corresponding to different platen power



positive angle: α *negative angle: α*

Fig 3.3: The sketch of positive profile and negative profile after etching

During the process investigation, the roughness of the top sidewall is found that it decreases as the etched depth increases. It can be explained as follows. The trenches are etched by a very energetic ion bombardment at the beginning of the process. The deposited passivation layer is removed quickly from the base of the trenches, and the isotropic etching takes place rapidly. At the bottom of the trench, the undercutting of the photoresist mask can deplete reactive species for etching entering into the deep, resulting the improper removal of the passivation layer on the bottom of the trench during etch cycles. Therefore the ion bombardment weakens as the etched depth increases, and the passivation becomes more dominant. The ripples have diminished and the sidewall becomes smooth. As Shown in Figure 3.4, the roughness of top sidewall is about 50 nm, however, the bottom of the trenches is quite smooth.

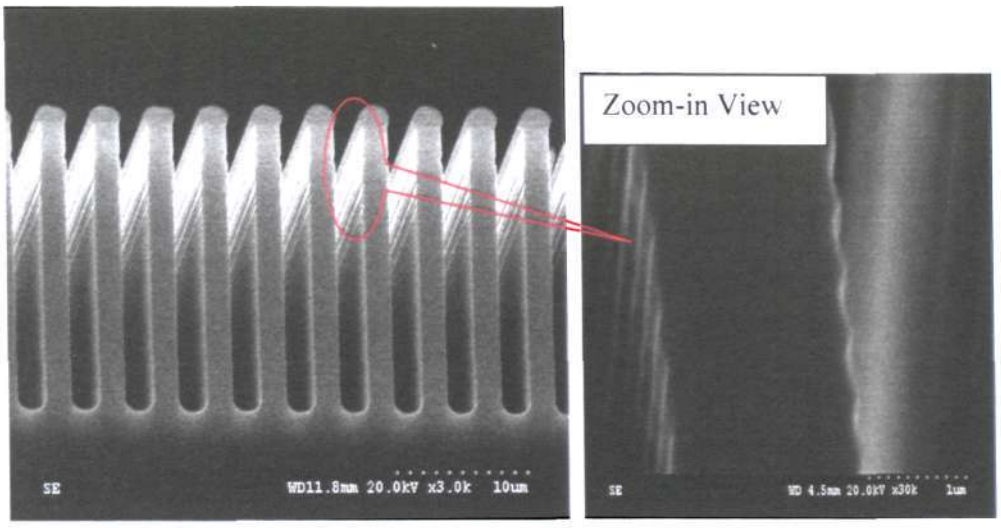
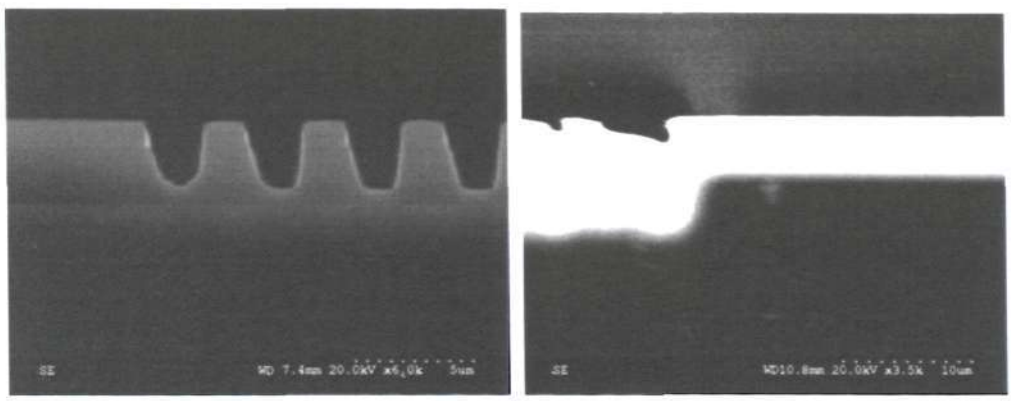


Fig 3.4: Sidewall roughness after DRIE

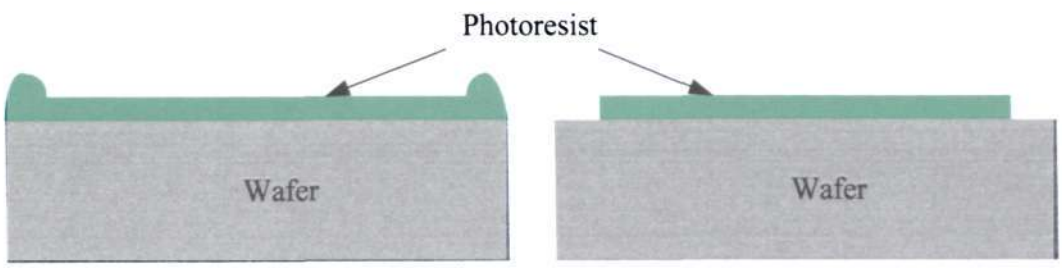
The lithography for 2 μm feature size should be paid much attention before DRIE process. Figure 3.5 shows the failed processes because the photoresist is not exposed completely, causing the failure of deep reactive ion etching. The reason is the non-uniformity of the spin-

coated photoresist. As see in Figure 3.6 (a), the coated resist at the edge of wafer is thicker, so the mask can not tightly contact with the surface of the wafer during exposure. The non-uniformity of coated photoresist can be improved by EBR (edge beard removal) process, as shown in Figure 3.6 (b). After the edge thicker photoresist is removed, the glass mask can then be tightly contacted on the resist surface using vacuum contact mode during UV exposure. The success lithography process with satisfaction is shown in Figure 3.7, where the photoresist opening is 2 μm.



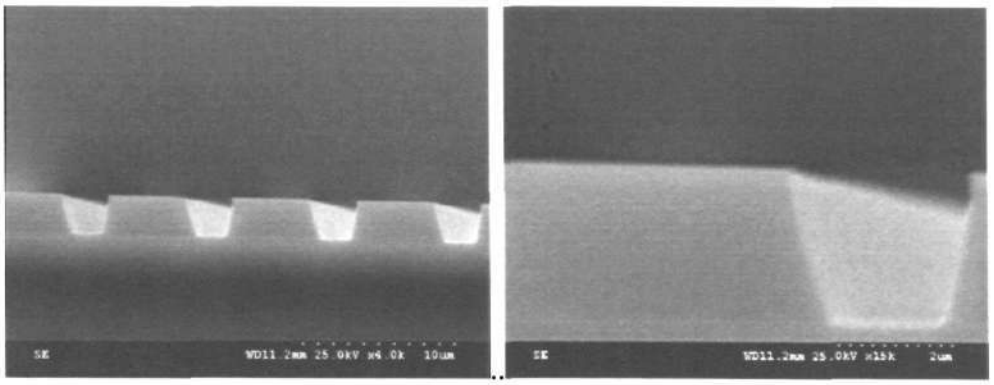
(a) Under-exposed lithography *(b) Failed DRIE process*

Fig 3.5: Failed lithography and DRIE Process



(a) Without EBR process *(b) With EBR process*

Fig 3.6: Comparison of coated photoresist with and without EBR process



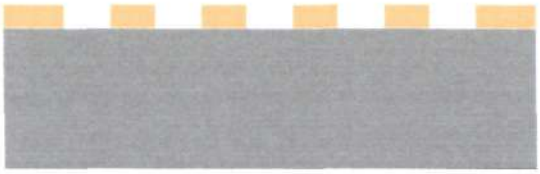
(a) Lithography result with 2μm opening *(b) Zoom-in view*

Fig 3.7: Success lithography process

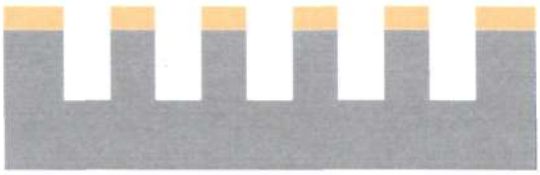
3.1.2 Novel DRIE Processes with Release Etching

An optimized DRIE process with in-situ dry release etching is investigated using Alcatel A601E ICP system in collaboration with Adixen Micro Machining Systems, Alcatel Vacuum Technology, France.

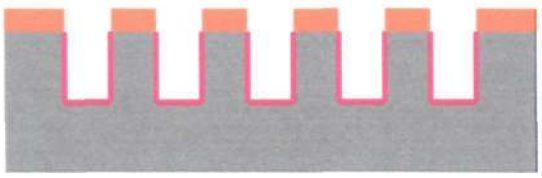
The process to etch, to passivate, and to release silicon structure totally in just only one process is schematically shown as Figure 3.8. Firstly, photoresist as etching mask is spin-coated on the wafer and patterned. Then, the trenches with vertical sidewall are uniformly etched. During the third process step, a polymeric film C_xF_y is uniformly deposited on the sidewalls of the etched channels, using C_4F_8 gas. The polymer C_xF_y on the bottom of the trenches is then removed by anisotropic etching step using high energetic SF_6 plasma. Finally, a selectively isotropic SF_6 etch of silicon is performed to release the etched structures from the substrate.



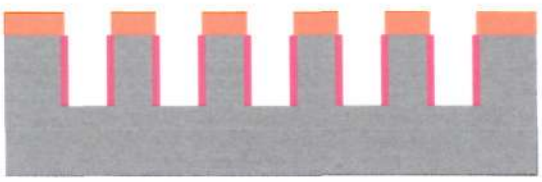
(a). Spin and pattern resist as the etching mask



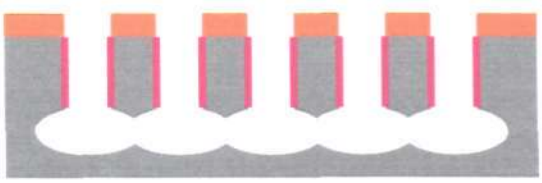
(b). Etch the trenches by DRIE



(c). Deposit C_xF_y film on the sidewalls by C_4F_8 passivation

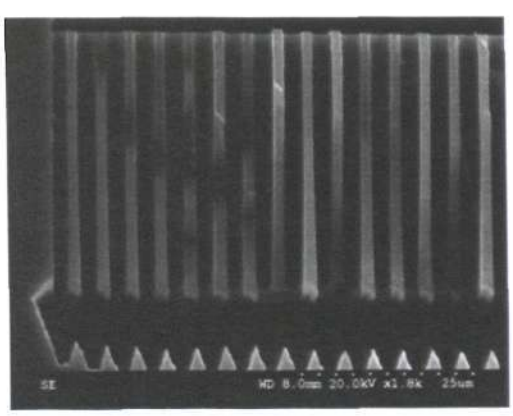


(d). Remove the passivating film on bottom by high energetic etching

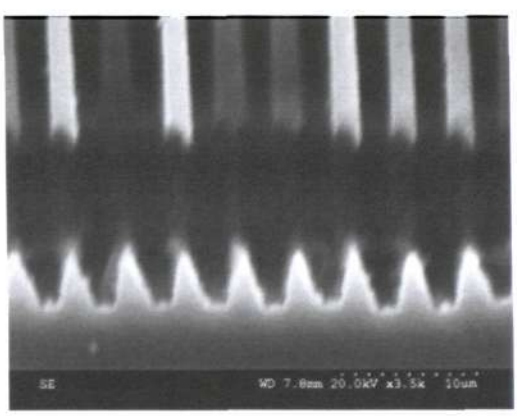


(e). Release the structure by isotropic silicon etching using SF_6 plasma

Fig 3.8: Novel DRIE processes with bottom release



(a) 35μm deep trenches with released bottom



(b) Zoom-in view of released bottom

Fig 3.9: SEM photos of DRIE fabrication results with dry release

Figure 3.9 shows the etched results. The process settings give a 3 μm/min etching rate with almost vertical sidewalls of silicon structures. After 12 minute etching, 35 μm deep trenches are created in the silicon wafer. The gap between the etched trenches and bulk substrate is about 8 μm after the release etching step.

3.2 Lateral Thermal Oxidation

Silicon dioxide formed by thermal oxidation of silicon is frequently used for insulating purpose. The quality of silicon dioxide depends on its growth method. Dry oxidation at high temperature in pure oxygen produces better quality of oxide than steam oxidation. But the dry oxidation speed is very slow and the thickness of silicon dioxide is very thin compared to wet oxidation. Wet oxidation in steam occurs much faster, normally can achieve 2 μm oxide layer. In this section, thick silicon dioxide blocks are fabricated by using the developed SiDeox (Silicon Deep Etching and Oxidation) process.

3.2.1 Controllable Thermal Oxidation

The quality of silicon oxidation is determined by the temperature and pressure. When oxygen reacts with silicon, either volatile silicon monoxide SiO, (so called active oxidation) or silicon dioxide SiO_2 (so called passive oxidation) film can be formed. Formation of SiO occurs at high temperatures and low O_2 pressures. Increasing the O_2 pressure and decreasing the temperature leads to the formation of a continuous SiO_2 film. A lot of study has been done on the mechanism of active oxidation, passive oxidation and the transition regime [77-80]. In this work, the oxidation is performed at temperature around 1100°C in one atmosphere pressure. After oxidation, 20 minutes annealing process in a high purity inert gas, nitrogen (N_2) is followed to reduce the compressive stress during oxidation. The intrinsic

compressive stress in SiO_2 during thermal oxidation is due to the mismatch of molecular volume and thermal expansion coefficients between Si and SiO_2.

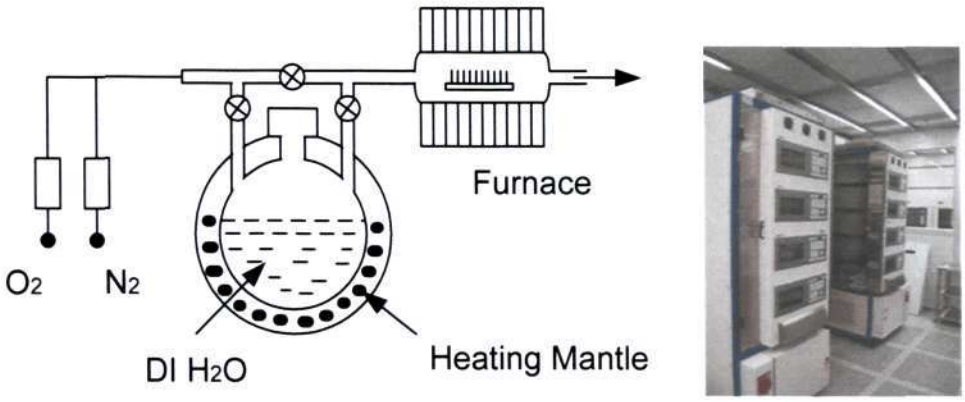
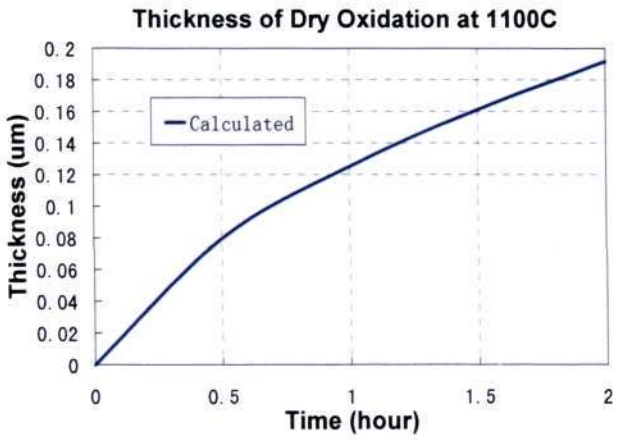
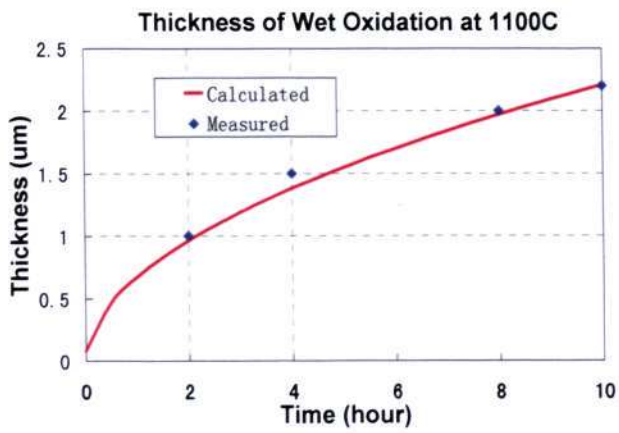


Fig 3.10: Wet oxidation set up



(a) Dry oxidation



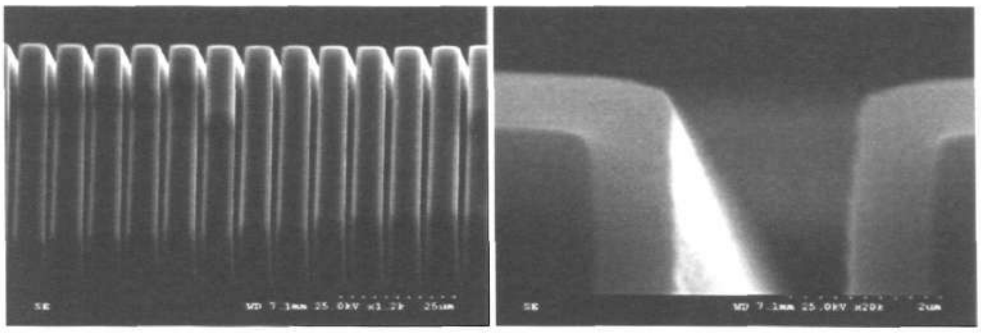
(b) Wet Oxidation

Fig 3.11: Thickness of silicon dioxide versus time at 1100°C by dry oxidation and wet oxidation

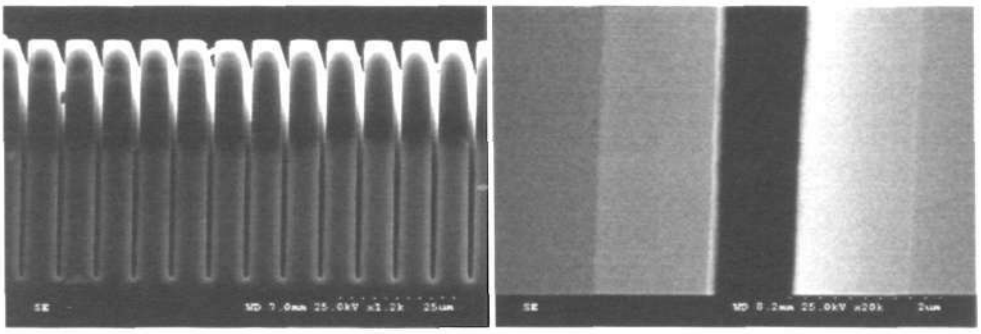
The oxidation set-up is shown as Figure 3.10. During dry oxidation, only oxygen (O_2) is used as the oxidant. The wet oxidizing species is a mixture of O_2 and H_2O. DI water is heated at 97°C by the heating mantle to produce water steam. The wafers are placed vertically on the quartz boat. Using the Deal-Grove formulas (equation 2.1 and 2.2), the oxide thickness by thermal oxidation at 1100°C is estimated and shown in Figure 3.11.

In this work, the deep trenches fabricated by DRIE are firstly oxidized using dry oxidation for 30 minutes. According to the estimation of dry oxidation shown in Figure 3.11 (a), the oxide thickness after 30 minutes dry oxidation is about 80 nm. Afterwards, the wet oxidation is processed for different time durations of 2 hours, 4 hours, 8 hours, and 10 hours. Figure 3.11 (b) shows the calculated thicknesses of wet oxidation with 80 nm initial silicon dioxide, which are 1 μm, 1.4 μm, 2 μm, 2.2 μm corresponding to these oxidation time durations, respectively. As shown in Figure 3.12, the experimental thicknesses are measured by the cross section SEM. Figure 3.12 (a), (b), (c), (d) are the oxidation results for 2 hours, 4 hours, 8 hours, and 10 hours, respectively. The experimental thicknesses have very good agreement with the estimations by the Deal-Grove formula, which are compared in Figure 3.11 (b).

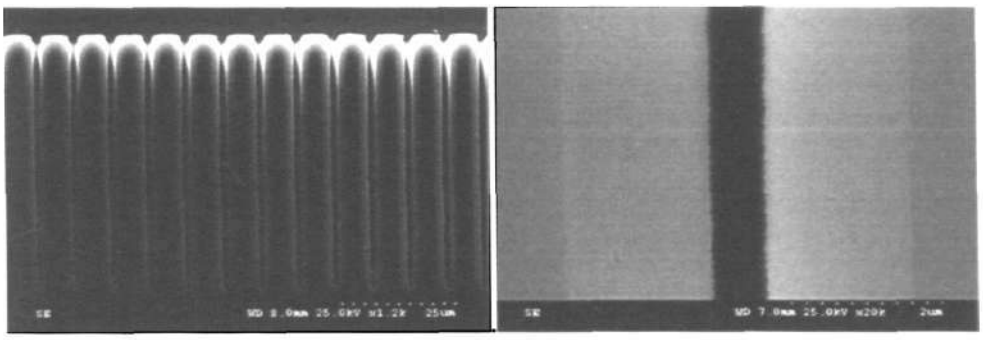
The well controllable thermal oxidation is the fundamental process for the structures in following sections. The high-aspect-ratio channels, nano beams, and thick oxide blocks can be realized by the well-controlled thermal oxidation process.



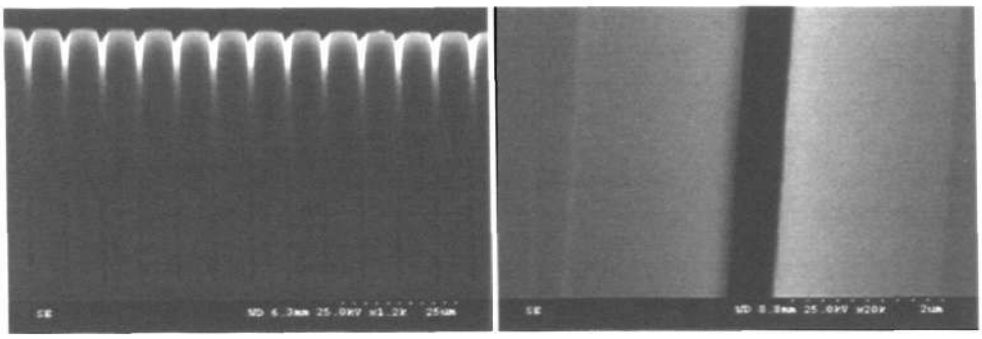
(a) 1 μm thick SiO_2 after 2 hours wet oxidation



(b) 1.5 μm thick SiO_2 after 4 hours wet oxidation



(c) 2 μm thick SiO_2 after 8 hours wet oxidation



(d) 2.2 μm thick SiO_2 after 10 hours wet oxidation

Fig 3.12: SEM photos of grown SiO_2 thickness with different oxidation time

3.2.2 High-Aspect-Ratio Nano Channels

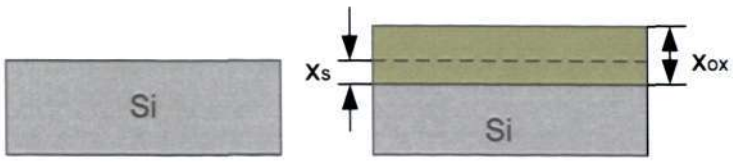
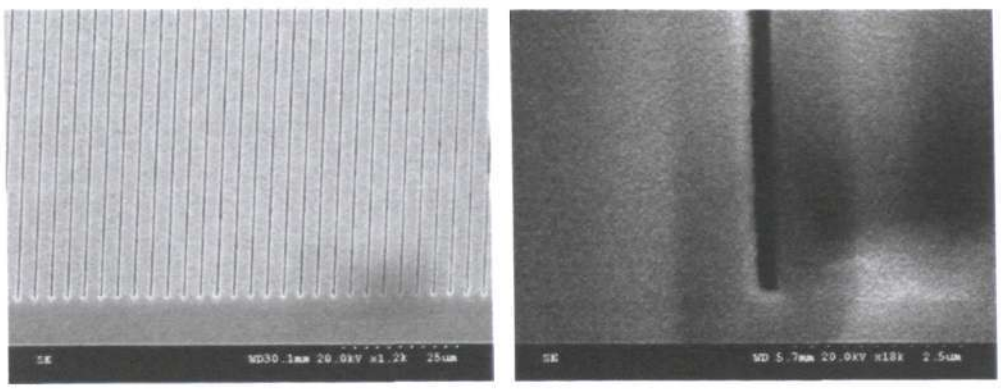


Fig 3.13: Silicon thickness converted to oxide thickness during thermal oxidation

The ratio of silicon thickness converted, x_s, to resulting oxide thickness, x_{ox}, which is shown is Figure 3.13, is: x_s=0.46x_{ox}. In this work, nano channels were created by well controlled thermal oxidation. A silicon wafer was patterned using photoresist with 2 μm openings and 2 μm beams, and then etched by DRIE to 10 μm deep. After 4 hour oxidation, the 2 μm wide channels are shrinked to 500 nm, which are shown in Figure 3.14. To further oxidize the wafer up to 6 hours, the channels were narrowed to 150 nm, as shown in Figure 3.15.

Such narrow channels with large depth can not be fabricated using normally micromachining technology. The high aspect ratio of a 10 μm deep, 150 nm wide channel is up to 67. These nano channels can be used as molds for growth of carbon nanotubes, replication of high-aspect-ratio silicone rubbers and so on [81].



(a) Top view *(b) Cross section view*

Fig 3.14: 500 nm nano channels fabricated by DRIE and controllable thermal oxidation

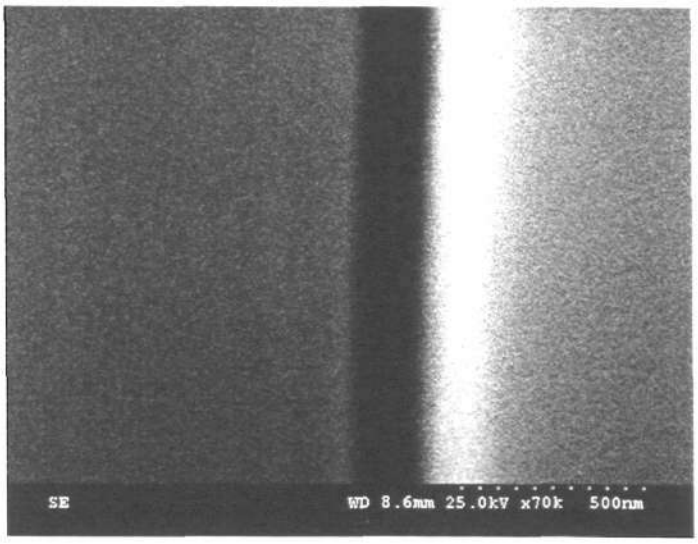
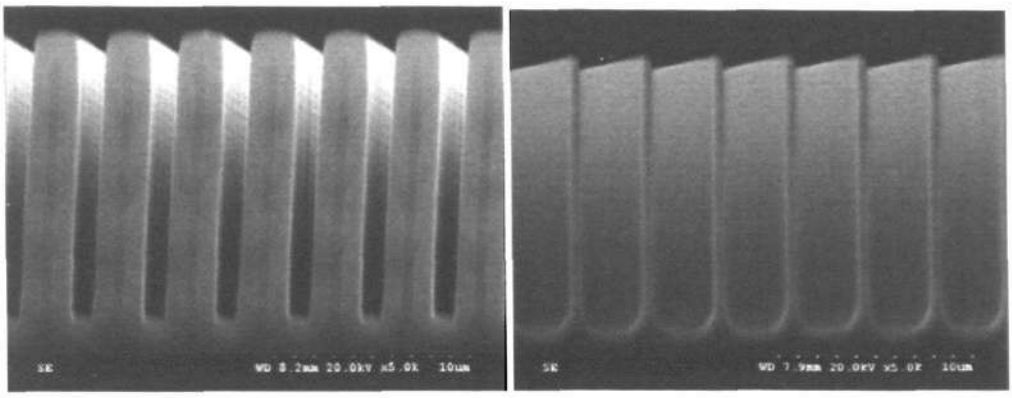


Fig 3.15: Fabricated 150 nm nano channels

3.2.3 Nano Beams



(a) After thermal oxidation *(b) After SiO_2 strip by BOE*

Fig 3.16: Fabricated nano beams by SiDeox process and wet etching

As shown in Figure 3.16, the nano beams are fabricated using this SiDeox process. A 2 μm gap-to-beam structure is firstly etched by DRIE. The structure is then oxidized using wet oxidation for 5 hours. 0.75 μm silicon materials from both sides of the 2 μm beams are consumed. After the thermal oxidation, the oxide is selectively etched by BOE (buffered oxide etch) for 20 minutes. The 500 nm silicon beams are formed as shown in Figure 3.16

(b). This is a good method to fabricated nano needles, nano nozzles used for the applications of drug delivery and nanodroplet generator [82].

3.3 Formation of Thick SiO_2 Block

Thick silicon oxide layer is very desirable in small-scale high temperature devices such as micro hotplates, infrared detectors etc. [83-84], because it has good thermal isolation. Thick silicon oxide layer also has good mechanical strength and low thermal expansion coefficient. Thermal property of the thick SiO_2 diaphragm has been studied recently [85]. The aim of this work is to develop MEMS technologies and processes to build thick insulation layer, SiO_2 block, in order to reduce the substrate losses for RF devices such as inductors. The silicon dioxide blocks are formed by the developed SiDeox process. The thick silicon dioxide blocks can significantly suppress the substrate losses for passive RF devices. The detailed fabrication will be described in this section.

3.3.1 Mask Design Issues

To fabricate the silicon oxide block, the widths of beams and trenches should be designed properly. For a 2 μm wide gap, 1.7 μm silicon is needed to be consumed. Conventional pulsed ICP based deep etching results in an undercut of about 250 nm for the given structures, as shown in Figure 3.17. The patterned resist strips are 2 μm wide with 2 μm gaps. After deep etching, the silicon beams become 1.5 μm and the gaps are 2.5 μm. In this case, the gaps can not be fully filled by thermal oxidation. Therefore, during the mask design, the undercut during DRIE process must be taken into consideration. In the following experiment, the mask will be designed with 2.5 μm width for photoresist patterns and 1.5 μm width for openings.

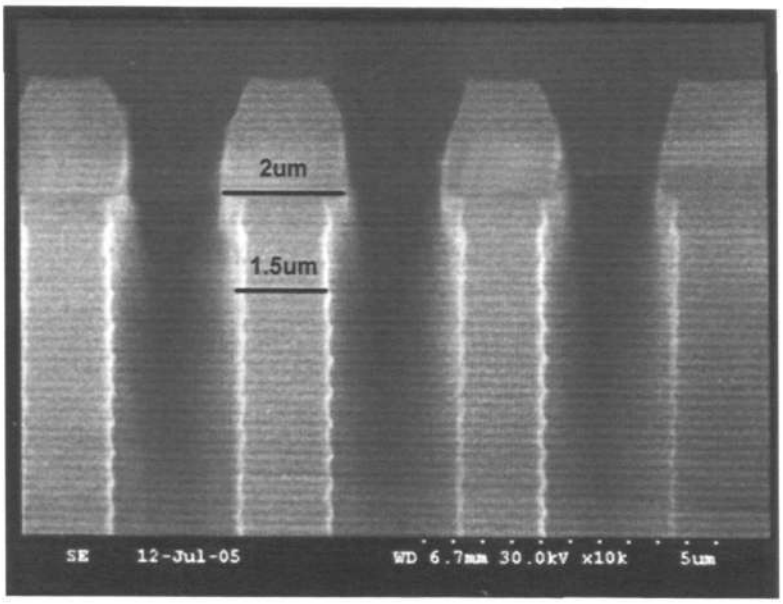
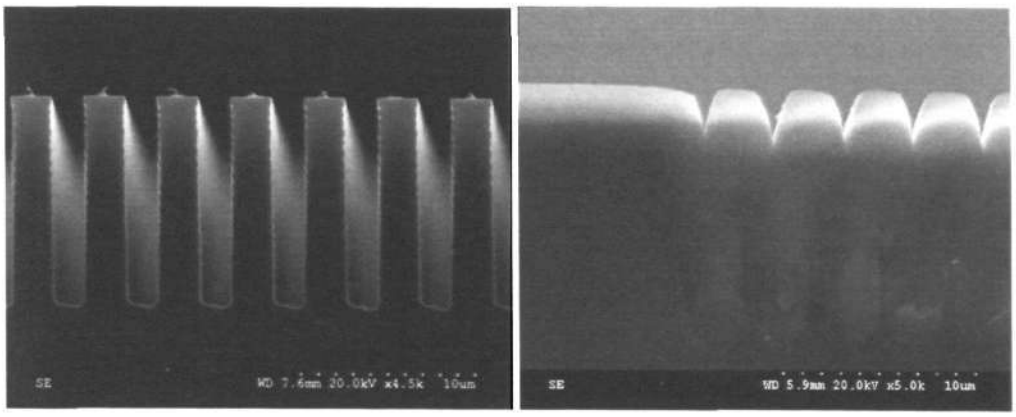


Fig 3.17: The undercut of 2 μm beams after DRIE etching

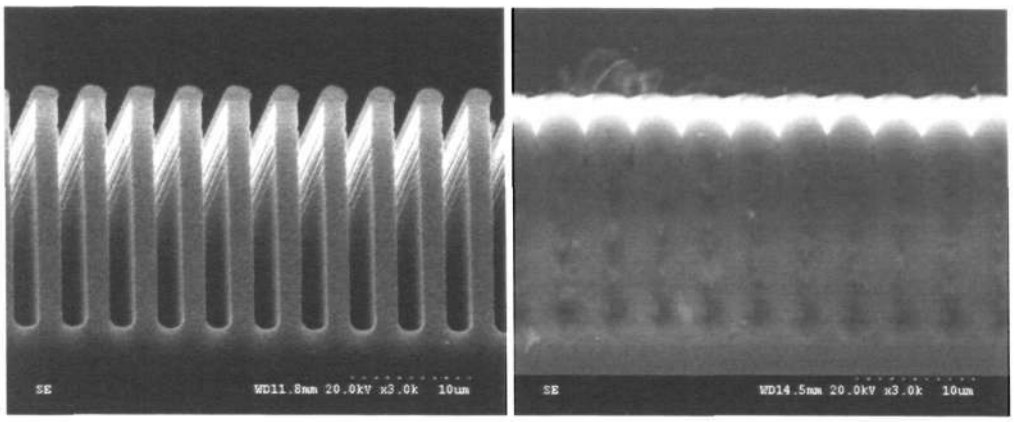
3.3.2 Experiment Results

The silicon wafers (100) with the resistivity 1-10 Ω·cm are selected. These wafers are cleaned using piranha solution which consists of 96% H_2SO_4 and 30% H_2O_2 in a ratio of 56:1, and is heated at 120°C. Then photoresist AZ 7220 is spin-coated and patterned. The samples are etched using the DRIE recipe as shown in Table 3.1. The platen power is set at 100 W. One of the samples is etched for 6 minutes. The etching depth of the channel is about 10 μm. The second sample is etched for 12 minutes. The channel depth is about 20 μm. The third sample is etched for 30 minutes with etching depth of 50 μm. The etched silicon beam structures are about 2 μm with 2 μm trenches.

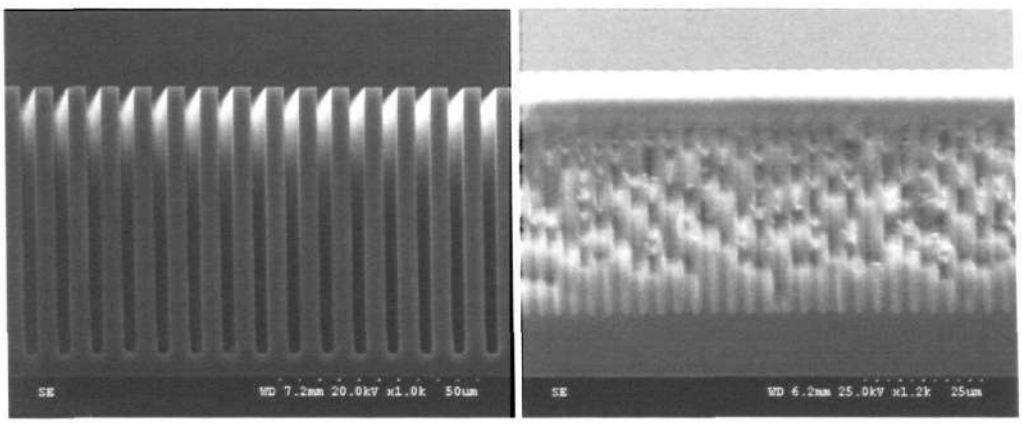
After DRIE process, the photoresist is then removed after DRIE process by the reactive ion etching (RIE) using the oxygen gas, instead of using Acetone, to avoid the damage of 2 μm silicon structures. The etched silicon wafers are then transferred to a Tystar thermal furnace to perform the thermal oxidation at the temperature of 1100°C. Silicon oxide is formed by



(a) 10 μm thick SiO_2 block by SiDeox process



(b) 20 μm thick SiO_2 block by SiDeox process



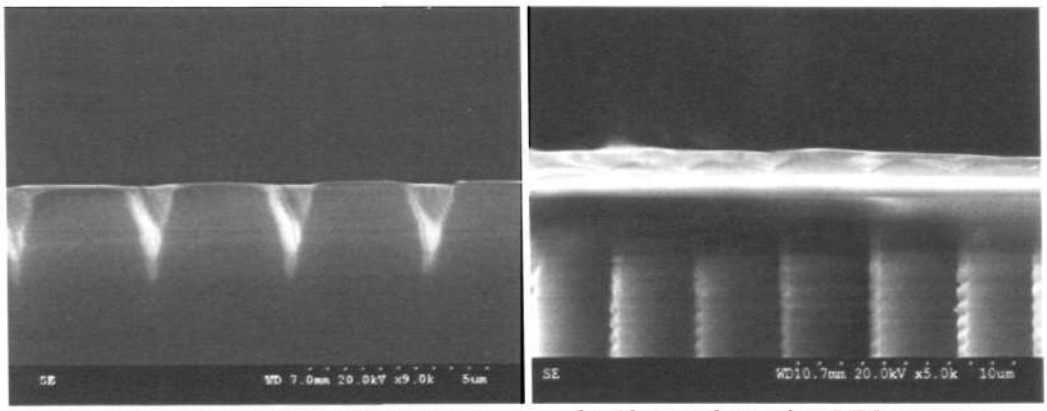
(c) 50 μm thick SiO_2 block by SiDeox process

Fig 3.18: SiO_2 blocks with different thicknesses

half hour dry oxidation and 10 hours wet oxidation to make sure that the 2 μm silicon structures are fully consumed to fill the 2 μm channels. As shown in Figure 3.18, after

thermal oxidation, the silicon microstructures were completely oxidized to form 10 μm thick, 20 μm thick, 50 μm thick silicon oxide blocks.

After refilling the trenches by thermal oxidation, the surface of thick silicon oxide blocks is not flat because V-shape ripples are formed, as shown in Figure 3.19 (a). The depth of such V-shape ripples is around 2 μm. The ripple surface is a big problem for the following processes. This problem can be solved by further refilling of the ripple surface by LTO (Low Temperature Oxidation) process with SiH_4 and N_2O at the temperature of 450°C for 2 hours. Around 2 μm LPCVD oxide layer was then deposited on the ripple surface. As shown in Figure 3.19 (b), the flatness of surface is much improved. The average roughness (R_a) of the LTO surface measured by a stylus is less than 40 Å. It is acceptable for many MEMS applications, which require planar surface.



(a) Ripple surface before LTO process *(b) Flat surface after LTO process*

Fig 3.19: Wafer surface after SiDeox process and LTO refilling

To avoid cutting of the fabricated wafer, a wafer sample with fabricated 20 μm deep silicon dioxide blocks after SiDeox process was verified using SIMS (secondary ion mass spectrometry) as well. The depth profiles of O and Si of the sample are shown in Figure 3.20. The y axis represents the detected intensities of elements O and Si. The x axis represents

analyzed depth of the sample with unit μm. The interface between silicon dioxide and silicon is very clear at the depth of around 20 μm, which is of very good agreement with the fabrication process.

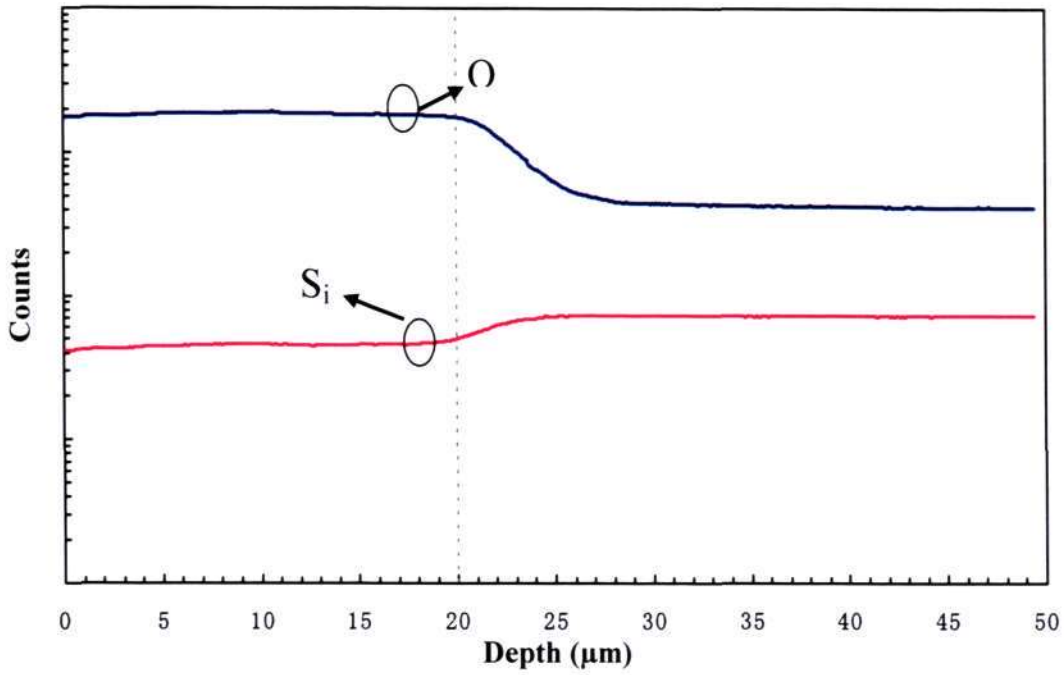


Fig 3.20: SIMS measured depth profile of fabricated 20 μm SiO_2 block on Si substrate

3.4 Summary

In this chapter, the silicon deep reactive ion etching and oxidation (SiDeox) process is developed to form thick silicon oxide blocks in the silicon substrate. Large high-aspect-ratio DRIE process using STS ICP etcher is optimized to get vertical profile of the sidewall. Furthermore, the technology of DRIE with bottom release in one process is developed. Thermal oxidation of the deep etched silicon structures is studied, and the nano channels and nano beams are fabricated by using the thermal oxidation of deep etched silicon structures and wet etching. Thick silicon oxide blocks are also fabricated by SiDeox process.

Thick silicon oxide layer has excellent mechanical strength and can sustain large extrinsic shear stress, so it is good material used for mechanical support of elements. It is also desirable for high temperature sensors and heaters because it has good thermal isolation property. In this work, we will use its good electrical isolation and low dielectric constant properties for the application of RF inductors, which will be discussed in following chapters.

Chapter 4

Design and EM Simulation of RF Spiral Inductors

Spiral inductors have a deceptively simple geometry but are notoriously difficult to analyze because the accurate characteristics of the structures in the microwave range of frequencies require an analysis of the parasitic losses, especially, the effects of the conductive substrate on the component performances. Electromagnetic (EM) simulations have become increasingly important in the design of microwave devices nowadays with the advance of computer technology and available tools. Fortunately, HFSS module of Ansoft software, which is a simulator for 3-D structure EM analysis, can be used to design and validate spiral inductors before the actual fabrication. In this chapter, various layouts of RF inductors, the mechanisms of substrate loss and metal loss, and the calculation of quality factors, self resonant frequency and inductance, will be discussed in section 4.1. Section 4.2 will discuss the modeling of RF spiral inductors, while the equivalent electric circuit of spiral inductors will be given. In section 4.3, the considerations on design and validation will be presented using EM simulations. Finally, this chapter will be summarized in section 4.4.

4.1 Layouts, Loss Mechanisms, Characteristics of Inductors

Radio frequency circuits fabricated in monolithic microwave integrated circuit technologies make extensive use of on-chip transmission lines to realize an inductance, while the inductor being a key component in many high-performance narrowband circuit designs. The purely

passive inductors are usually required for high-frequency LC circuits and for synthesis of an inductive reactance with an active circuit. Silicon IC technologies have rarely been used for analog applications in the radio and microwave range of frequencies, primarily because transmission line structures perform poorly on the semiconducting substrates used to manufacture silicon IC's. In this section, the knowledge of RF inductors based on silicon substrates, especially the limitations imposed by silicon IC technology on the inductor performance will be addressed. We will present the layouts, loss mechanism, modeling, and the characteristics of RF inductors.

4.1.1 Layouts

Passive inductors can be implemented on-chip using transmission lines. However, these transmission lines are limited by their low space efficiency, and are only used for small value of inductances. When inductances go up, transmission lines no longer fulfill the requirement. Recalling the reviews of RF inductors in chapter two, the passive inductors have two general different layouts: solenoid structure and planar spiral structure. The solenoid inductor fabricated on silicon substrate has the advantage that the main electromagnetic flux is parallel to the substrate. This could produce minimal substrate losses. However, this kind of structure suffers from considerable contact resistance because of a numbers of vias. In addition, it is very complicated to be fabricated and occupies larger area than the planar structure. It is not compatible for the high integration of the IC's chips. Hence, for the applications of radio frequency integrated circuits, planar structure of inductors has been widely adopted. Different from the solenoid inductors, planar inductors have the electromagnetic flux which are penetrating into the substrates. The parasitic losses due to the substrate significantly affect the performance of RF inductors. To overcome the substrate losses, the planar structures of inductors are modified into many shapes such as multilevel

spiral inductors, spiral inductors with eddy-current blocking structure, inductors on thin membrane, and inductors with cavity structure. The substrate losses of these kinds of inductors are reduced. The inductors for RF circuits are almost designed as the planar spiral structure because it is easy fabrication, and most of importance, it is compatible with CMOS for integration. In this work, we just focus on the design of planar inductors on silicon substrate.

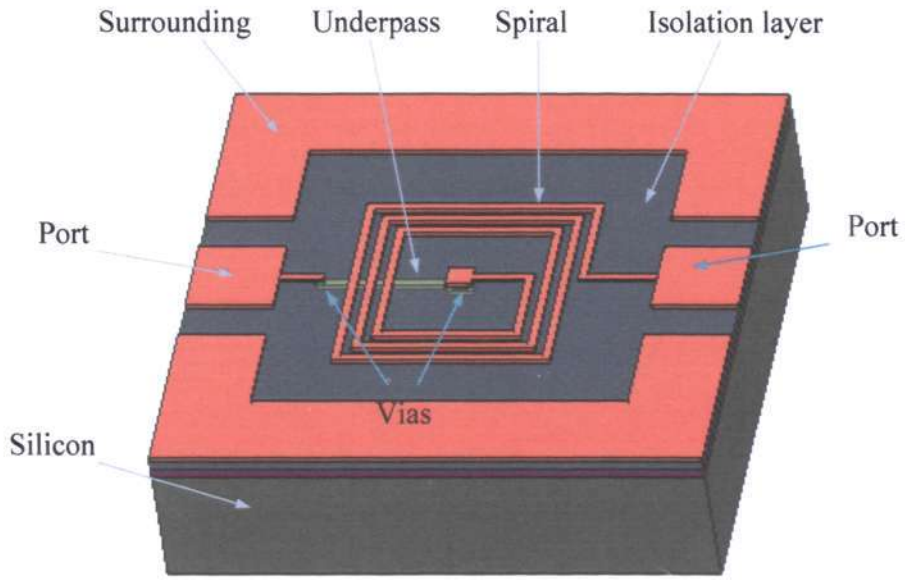
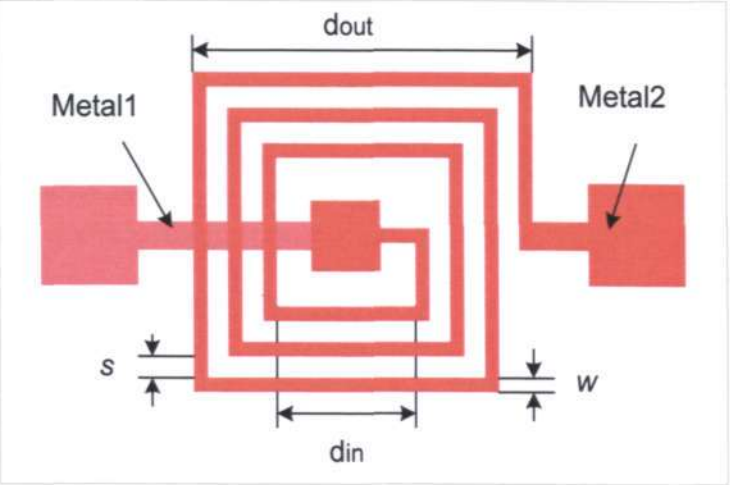
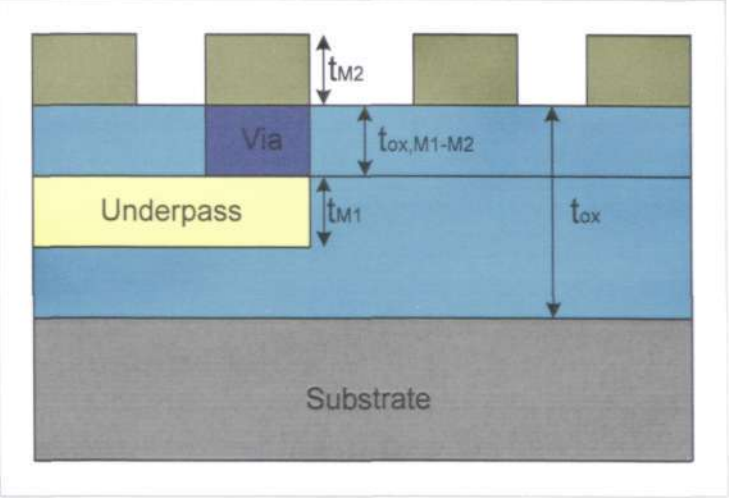


Fig 4.1: The schematic of 3D view of a square spiral inductor

Figure 4.1 shows the structure of a square planar inductor. A spiral inductor is built on a silicon substrate with a thin thermal oxidized silicon dioxide layer. The RF signals from one port pass through spiral interwinding, underpass to another port. The underpass and the spiral metal are connected through vias, and separated by an isolation layer. The surroundings are used as ground for measurement and shield the electromagnetic flux.



(a) Lateral layout parameters



(b) Vertical layout parameters

Fig 4.2: Layout parameters of a spiral inductor

The geometries of a spiral inductor are specified in the following, as shown in Figure 4.2.

- w, metal width
- s, spacing between adjacent turns
- d_{out}, outer separation, or d_{in}, inner separation
- N, number of turns
- t_{M1}, t_{M2}, metal thickness
- t_{ox}, oxide thickness (from the spiral to substrate)
- $t_{ox,M1\text{-}M2}$, isolation layer thickness (between the spiral and the underpass)

Except for square shape, planar structures are also designed as polygonal structures such as hexagonal and octagonal shape, and circle structures. The inductors' layouts in the work are only designed as square shape because: (a) square layout is easy for photo mask fabrication; (b) circular and polygonal layouts consume larger chip area and introduce difficulties in the generation of photo masks although an improvement in quality factor is possible using a circular rather than a square design [86-87]; (c) the interaction between the magnetic field components on adjacent sides of a non-rectangular spiral inductor is difficult for modeling because the mutual inductances exit among the non-orthogonal adjacent metal traces.

4.1.2 Analysis of Loss Mechanism

Losses are the main problem to be considered when one designs an inductor on silicon substrate. As shown in Figure 4.3, when RF signal passes through spiral inductors, magnetic field B(t), and electric field $E_1(t)$, $E_2(t)$, $E_3(t)$ will be generated in the structure. The magnetic field B(t) is generated due to the currents flowing through the metal traces of the inductor. It produces not only the inductive behavior, but also the parasitic currents in the metal traces and the silicon substrate because of the low resistivity of commonly used silicon wafer. The electric field $E_1(t)$ is generated due to the voltage difference in the spiral traces. Current flowing along the metal traces produce the ohmic losses. The electric field $E_2(t)$ is caused by the voltage difference between the metal segments of the spiral structure, and induces capacitive coupling between segments of the spiral inductor. The electric field $E_3(t)$ is generated due to the voltage difference between the inductor and the substrate. The penetration of the electric field into the conductive substrate will generate eddy currents in the substrate. Spiral inductors based on silicon substrate suffer from these parasitic losses, severely limiting their performance.

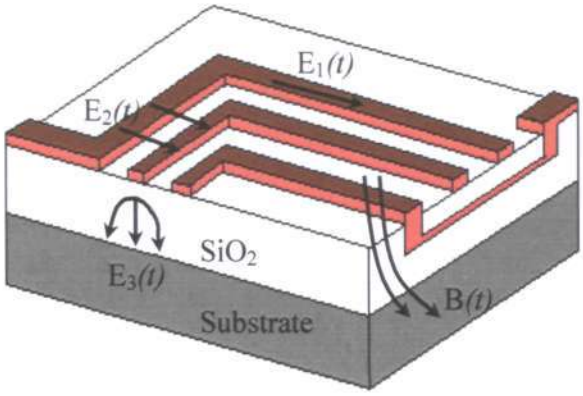


Fig 4.3: The schematic illustration of electric field and magnetic field in an inductor

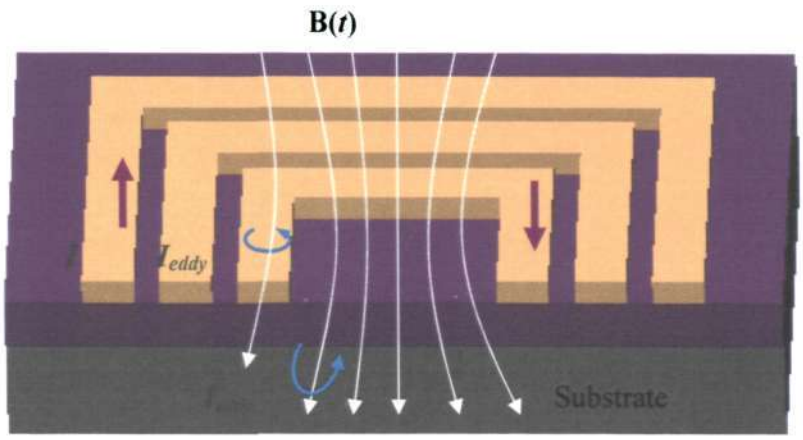


Fig 4.4: The schematic diagram of eddy current in an inductor

Let's consider the metal loss in a spiral inductor. At DC or low frequency, the resistance of a rectangular cross-section conductor with resistivity ρ, length l, width w, and height h, is

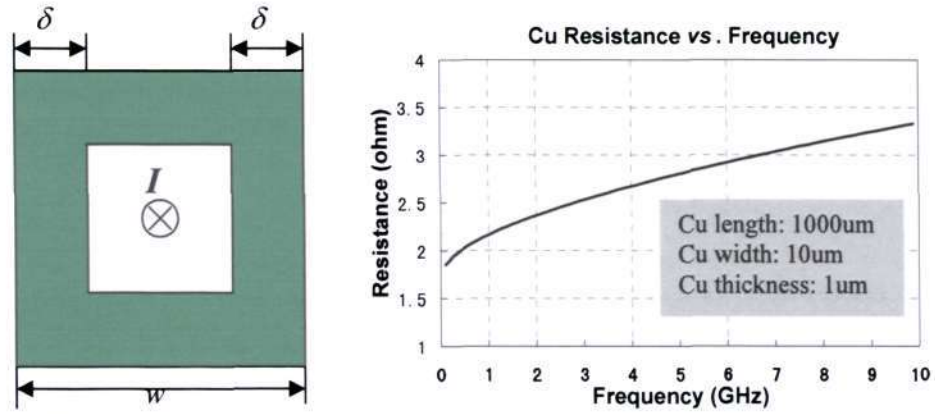
$$R = \rho \frac{l}{wh} \tag{4.1}$$

But this expression of resistance can not represent the resistive losses for an inductor working at high operation frequency, because magnetically induced losses are now present, which is well known as eddy current. As seen in Figure 4.4, the magnetic field generated by the high frequency RF signals penetrates the metal strips and produces eddy currents.

The eddy currents make the current flowing in the traces non-uniformly and being the tendency to only go through the surfaces of the metal traces. That is the so-called skin effect. At high frequencies, the skin effect causes the current to flow in the outer area of the conductor instead of the full area of the conductor. To quantify the phenomena of skin effect, skin depth δ is defined as the distance where the amplitude of the fields in the conductor decay by an amount 1/e or 36.8%, which is illustrated in Figure 4.5 (a). The skin depth δ can be calculated as:

$$\delta = \sqrt{\frac{1}{\pi \cdot \mu \cdot \sigma \cdot f}} \tag{4.2}$$

where μ is the permeability of material, σ is the conductivity of material, f is the operation frequency.



(a) The schematic of skin depth *(b) Skin effect on Cu resistance*

Fig 4.5: The conductor's skin effect

The exact calculation of the frequency dependent resistance of a metallic conductor is a difficult task. Different methods have been reported in [88-90]. The popularly used method for calculating the resistance at high frequency is deduced in [91], and the formula is described as follows with consideration of the skin effect.

$$R(f) = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \tag{4.3}$$

where l, w, t represent the conductor's length, width, and thickness, respectively. Figure 4.5 (b) shows the example of skin effect on a Cu line with 1000 μm length, 10 μm width, and 1 μm thickness. It is obvious that the resistance of a conductor at high frequencies is frequency-dependent. The metal loss is seriously deteriorated because the skin effect increases the resistance very much.

Compared with other components used in RFICs, inductor has bigger structure and occupies much larger area on chip. The substrate losses of silicon inductors are quite considerable and always limit the whole performance of the circuit. It is the reason why the inductors become the bottleneck of integrated circuits [92].

The silicon substrate influences the inductor performance in two ways. It adds parasitic capacitances and introduces eddy current in the substrate. The eddy current of substrate, which is shown in Figure 4.4, are induced from: (a) capacitive coupling between the spiral and the substrate, (b) magnetic coupling caused by the alternative magnetic field. The induced eddy currents dissipate the power in the substrate; consequently degrade the performance of the inductors. The induced eddy currents in the substrate also introduce negative magnetic coupling between the substrate and the spiral metal, thus reduces the inductance, because the induced currents in the substrate flow in the opposite direction to the current in the spiral metal according to Faraday Neumann-Lenz law.

4.1.3 Characteristics of RF Inductors

Quality factor of an inductor is especially important because it is the most important figure of merit that provides effective means for quickly estimating circuit performance. Self resonant frequency of an inductor needs to be as high as possible so that the operation frequency is much lower than it. This is because the inductor functions no more as an

inductor, but as a pure resistor at self resonance frequency. Inductance value is another important merit factor when we design an inductor for certain circuit.

The Q factor of a device is defined as the sum of total stored magnetic energy (E_m) and electric energy (E_e) divided by the average power dissipation (P_{diss}).

$$Q = \frac{\omega \cdot (E_m + E_e)}{P_{diss}} \tag{4.4}$$

where ω is the angular frequency.

Unfortunately, the distributed nature and frequency dependence of these values make difficulty to extract the values of an inductor. Therefore, the accurate value of quality factor in terms of the maximum stored magnetic energy and electric energy is hard to be evaluated. In some cases such as band pass filters, oscillators, the accurate calculation of electric and magnetic energy is not necessary. The interesting parameters are the loss, bandwidths and frequency stability factors. The quality factor for band pass filters and oscillator is defined as formula (4.5) and (4.6), respectively.

$$Q = \frac{\omega_0}{\Delta\omega} \tag{4.5}$$

$$Q = \frac{S_F}{2} \tag{4.6}$$

where $\Delta\omega$ is the 3-dB bandwidth of a band pass filter, and S_F is the frequency stability factor of an oscillator. These definitions do not require an equivalent circuit model and model parameter extraction. These definitions of the quality factor are defined when the devices operate near the resonant frequency. They can not be used for an inductor because it works far away from the resonant frequency.

When we analyze the spiral inductor model, it can be simplified as a series LRC circuit. The power transferred into the inductor is:

$$P_{in} = \frac{1}{2} Z_{in} |I|^2 = \frac{1}{2} |I|^2 (R + j\omega L - j\frac{1}{\omega C}) \tag{4.7}$$

The power dissipated by the resistor, R is:

$$P_{diss} = \frac{1}{2} |I|^2 R \tag{4.8}$$

The average magnetic energy stored in a pure inductor, L, is:

$$E_m = \frac{1}{4} |I|^2 L \tag{4.9}$$

And the average electric energy stored in a pure capacitor, C, is:

$$E_e = \frac{1}{4} |I|^2 \frac{1}{\omega^2 C} \tag{4.10}$$

Substituting the terms in (4.7) by formula (4.8)-(4.10), we can obtain:

$$P_{in} = P_{diss} + 2j\omega(E_m - E_e) \tag{4.11}$$

And it is well known that the input impedance can be expressed as:

$$Z_{in} = \frac{2P_{in}}{|I|^2} = \frac{P_{diss} + 2j\omega(E_m - E_e)}{|I|^2 / 2} \tag{4.12}$$

An inductor stores magnetic energy, whereas some electric energy also is stored due to the parasitic capacitance. The stored electric energy is much smaller than the stored magnetic energy, so there is no much difference between (E_m+E_e) and (E_m-E_e). Therefore, the most widely used quality factor for analysis of inductors is defined in terms of the net stored magnetic energy (E_m-E_e) and the average power dissipation during one oscillation cycle (P_{diss}), which is shown as:

$$Q = \frac{2 \cdot \omega \cdot (E_m - E_e)}{P_{diss}} \tag{4.13}$$

Comparing of equation (4.12) and (4.13), the quality factor of inductors actually is expressed as the ratio of imaginary part of the input impedance to the real part of the input impedance.

$$Q = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} \tag{4.14}$$

which also can be expressed as formulas (4.15) by using simple network theory.

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{4.15}$$

where Y_{11} is the admittance seeking from one port in the inductor model, while another port is grounded.

This is the special definition of the quality factor for inductors because it is only accurate when inductors work far away from resonant frequency. The disadvantage of this formula is that it is not accurate near the resonant frequency range where the parasitic effects are significant, so that the stored electric energy is comparable with the stored magnetic energy. The quality factor is zero at the self-resonant frequency of the inductor because of the equal stored magnetic energy and electric energy. This is physically unreasonable according to the fundamental definition of equation (4.4). Although the quality factor is not physically reasonable when working near the self-resonance frequency, it is useful in the range that is much lower than the self-resonance frequency. A designed inductor should be operated far away from its self resonant frequency, in other words, its self resonant frequency should be as high as possible.

Inductance value is another important parameter during the design of an inductor. The inductance value is complicated to be calculated even though the structure of an inductor looks like quite simple. It is well known that if two parallel conductors are put close to each other, the change in current that passes through one of the conductors will produce a change in magnetic field around it, and thus induce a voltage in another conductor, and vice versa. This is the phenomena of mutual inductance. When the currents in these parallel conductors

have same direction, the mutual inductance is positive, and it is negative when the currents flow in opposite direction.

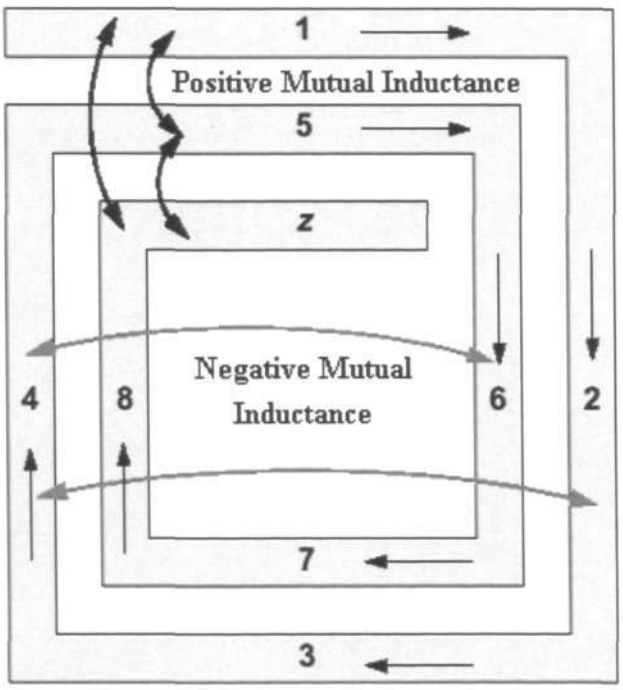


Fig 4.6: Mutual inductance between the segments of a spiral inductor

For a square planar inductor, the total inductance is the sum of self inductance of each segments, and mutual inductance between the parallel segments. As seen in Figure 4.6, the mutual inductances between segments 1 and 5 are positive because of the same directions of current flows. The analogous relationship exists between segments (2, 6), (3, 7), and (4, 8). The mutual inductances between segments (1, 5)-(3, 7), (2, 6)-(4, 8) are negative because the currents flow in opposite directions. Thanks to the simplicity of orthogonal segments when the currents flow in orthogonal directions, for example, the segments 1 and 2, the mutual inductances are zero, which has been proven by Neumann [93].

For the spiral inductor, much research has been done on the calculation of inductance in the past [94-96]. Sunderarajan S.Mohan has done a lot of contributions on the calculation of

inductance and he reported three simple methods to obtain accurate inductance values, which are modified Wheeler formula, current sheet expression, and data fitted monomial expression [97]. Another well-known inductance calculation of spiral inductor is Greenhouse method [98]. In this work, Greenhouse method is adopted to calculate the inductance for inductor design and it is particularly deduced in Appendix A.

4.2 Modeling of Spiral Inductors

An ideal inductor should only store magnetic energy, but all conductors have resistive loss because they are not perfect conductors. Therefore, the model of an inductor at least has to include series parasitic resistance. For the inductor built on lossy silicon substrate, additional parasitic parameters due to the substrate have to be added into the model. These parasitic losses are distributed along the inductor structure so that the accurate electric equivalent model is very difficult to obtain. To understand the physical models of RF inductors, we start with the simplest case: two parallel conductors on a lossy substrate.

4.2.1 Coupled Unit Strip Lines

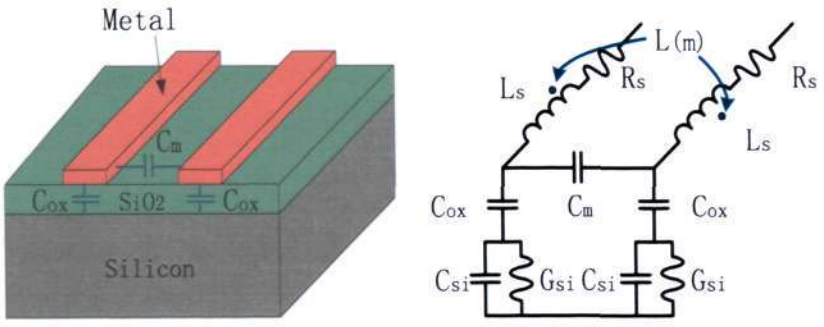


Fig 4.7: The equivalent model of two parallel conductors on Si-SiO_2 substrate

As seen in Figure 4.7, two unit metal strips are built on a SiO_2/Si silicon substrate. The metal strip itself is modeled as an inductor L_s associated with a parasitic resistor R_s. Between the two strips, fringe effect is modeled as the fringe capacitance C_m. The mutual inductance of the two strips is modeled as $L_{(m)}$, whose value can be positive or negative depending on the directions of current flows. The high frequency signals flow in the metal traces will penetrate into the silicon substrate through the oxide layer. C_{ox} is modeled as the parasitic capacitance due to the oxide layer. The losses in the lossy silicon substrate can be modeled as conductance G_{si} and the parasitic capacitance C_{si}.

4.2.2 Segmented Circuit Model

By expending the unit strips to one turn spiral inductor and summing up the unit distributed components of every segment, the segmented circuit model is shown in Figure 4.8. Each side of the spiral is modeled as a lumped segment. Each segment contains the conductor's self-inductance, series resistance, fringing capacitance, parasitic resistance and capacitance in the substrate. The mutual inductance between segments is represented as a dependent current.

A number of other parasitics should be taken into consideration. The capacitance between underpass and top spiral metal can be modeled using lumped capacitors between external terminal and the appreciate lumped-element sections. At the bending corners, additional parasitic capacitances and inductances due to the current crowding or discontinuity effects can be modeled by adding capacitors and inductors. For frequencies in low GHz range, this effect is small and is often neglected [99]. These parasitic capacitors and inductors are not shown in Figure 4.8. The segmented model is a scalable inductor model. Scalability implies that the electrical circuit parameters of the inductor model can be extracted from geometric and technological parameter specifications. The problem for the segmented model is very

bulky and complicated as the number of segments increases. A lumped model is needed for faster optimization of the inductor performance.

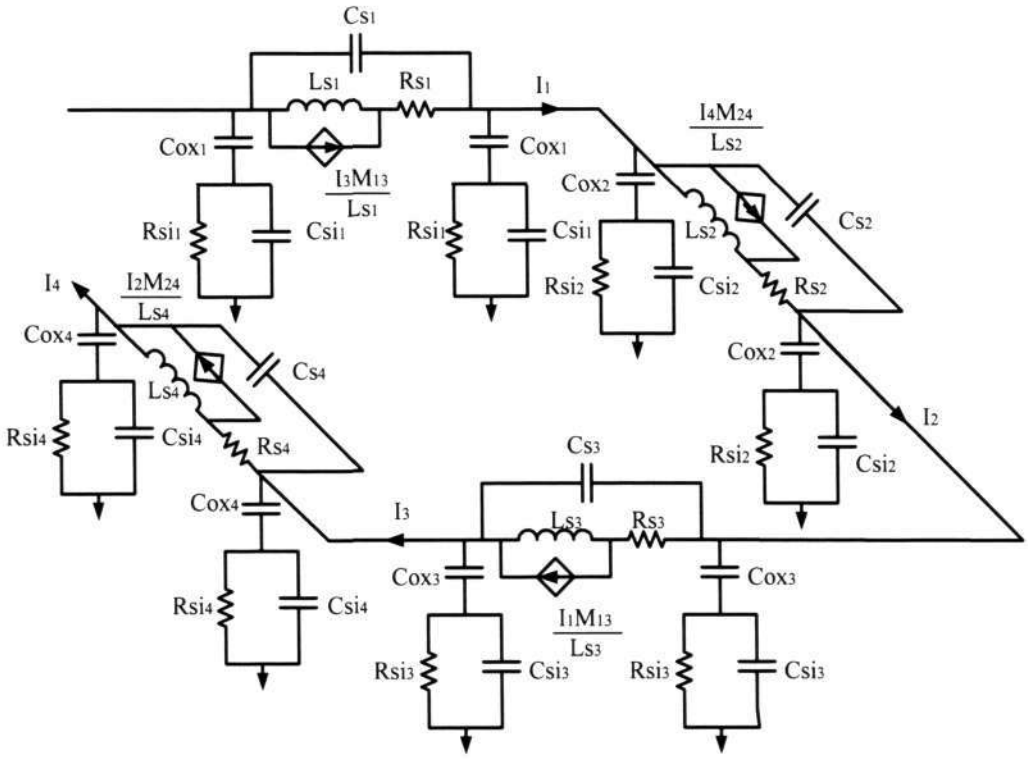


Fig 4.8: Segmented model for one turn square spiral

4.2.3 Lumped Inductor Model

By summing up the series components and shunt components in Figure 4.8, a spiral inductor can be represented by a lumped π model consisting of inductance, series resistance, and capacitance in the series branch, and the oxide capacitances, the substrate parasitic capacitances and resistances in the shunt branches. Lumped π models have been developed in various ways to represent the equivalent circuit [31,32,34,57]. Among some π models, the parasitic effects such as fringing capacitances, substrate capacitances are neglected because

they are much smaller compared to other parasitics. The lumped π model shown in Figure 4.9 is normally used to fit experimental measurements of a silicon spiral inductor.

In this model, L is the total inductance value of an inductor. R_s is the frequency dependent series resistance and has been discussed in section 4.1. The capacitance C_s represents the fringing capacitance between lines and the capacitance between top metal and underpass. This capacitance leads to crosstalk between the input and output port, resulting in the signal direct flow from one port to another port instead of flow through the spiral metal trace. The capacitance C_{ox} represents parasitic capacitance of the oxide layer between the metal and silicon substrate. It is the most significant among the parasitic losses because it allows high frequency RF signals penetrate into lossy substrate. The capacitance C_{si} and resistance R_{si} represent substrate losses. Some studies have been reported to evaluate the substrate losses [100-103]. Compared to C_{si}, the resistance R_{si} is the major contributor to the substrate loss because of the generated eddy current in the substrate.

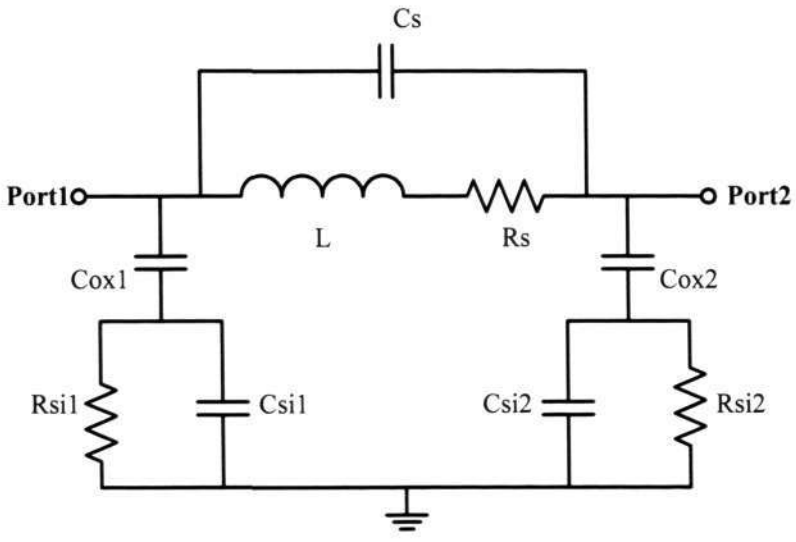


Fig 4.9: Lumped π circuit model for a spiral inductor

There are some limitations on using lumped π models for inductors. The signal can be

deemed to be reasonably constant along the entire length of a transmission line when the total length is no longer than 1/10 of wave length λ. With the increase of the spiral length of an inductor, the distributed effect begins to impact. When the length is longer than λ/10, transmission line model should be used [104]. The critical lengths for using lumped π model for an inductor are calculated in Table 4.1. The designed inductor should be small so that its total length is within 6000 μm in the operation frequency range from 1 GHz to 5 GHz.

Table 4.1: Critical lengths for use of lumped model

Frequency (GHz)	0.5	2	5	10
Length for lumped model (μm)	60000	15000	6000	3000

4.3 Design Aspects and EM Simulations

Layout parameters need to be optimized to achieve desired inductance and quality factors at a certain frequency. The work on layout optimization has been studied and reported in some papers [105-107]. The layout parameters for optimization are the occupied area, the trace width, the trace space, the center gap, and the distance to surrounding metal. But there are many trade off when optimizing these parameters. The effects of these parameters are discussed in following sub sections.

4.3.1 Geometries Design Aspects

The area occupied by the inductor affects the cost of the inductor. Typically, the more chip area a circuit occupies, the more expensive it is. The inductor area occupies also affects its performance. The larger the inductor area is, the more capacitive coupling to the substrate will be, consequently lowering the self-resonant frequency and quality factor.

Spiral inductors store energy as magnetic flux that passes through the center and around the exterior of the inductor. Eddy currents in the metal may generate opposite magnetic flux, which will reduce the amount of energy stored in the inductor's field, thus reducing the performance of the inductor. Moreover, a gap of insufficient size permits flux generated in the opposite sides to partially cancel each other, as shown in Figure 4.10. The center space should be free of metal to avoid generating eddy currents and canceling the magnetic flux. Parasitic electric and magnetic coupling between conductors is inversely proportional to the separation. Maintaining sufficient space in center gap will keep unwanted parasitic effects from disturbing the inductor's electrical characteristics. The center gap should have a minimum distance of five line widths between opposite sides of the inductor in order to reduce this magnetic field canceling effect [57].

The magnetic flux also penetrates into the exterior of the inductor, as they pass through the center of the inductor. As shown in Figure 4.10, the flux from the inductor can cause eddy currents in metals around the inductor. These eddy currents drain energy from the inductor and reduce the overall performance of the spiral. Therefore, the surroundings which serve as ground should not be too close to the spiral windings. A space of greater than five line widths is also recommended [57].

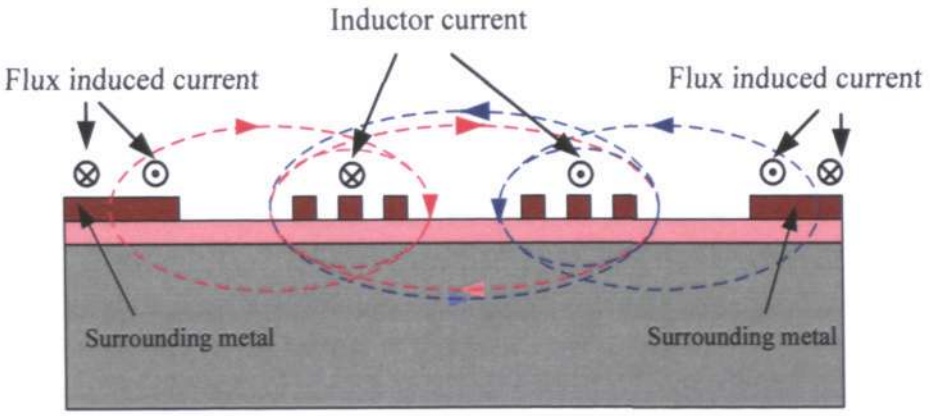


Fig 4.10: The schematic magnetic flux of an inductor

The line width and line space are variable design parameters. But the minimum width and space is limited by the fabrication technology. Increasing the width leads to a greater cross sectional conductor area, may yield lower resistive winding losses. On the other hand, increasing the trace width also increases the overall area of the inductor, leading to greater capacitive coupling to the substrate and resulting in a lower self-resonant frequency and quality factor. For the line space, it is well known that the closer the line spacing is, the greater the mutual coupling between adjacent lines will be. This mutual coupling is desirable because it serves to increase the overall inductance of the spiral windings, which directly increases the quality factor of the device. However, reduced line spacing increases the inter-winding capacitance of the inductor.

The occupied area of the inductor, which is mainly determined by the number of turns, also affects the quality factor, self resonant frequency and inductance of the designed inductor. The more turns are, the larger the inductance is. However, more turns have larger occupied area, and result in larger parasitic capacitance and resistance.

In this work, the study is emphasized on the decrease of substrate losses by modifying substrate using MEMS technology, even though the design aspects on inductor geometries have been investigated using EM simulations. The effects of thickness of oxide layer which significantly affects the performance of an inductor are mainly focused.

4.3.2 HFSS Simulator

HFSS is a high-frequency simulator, which is specially developed by Ansoft Corporation for 3D electromagnetic field simulation. It is widely used for the design of on-chip embedded passives, PCB interconnects, antennas, RF/Microwave components, and high-frequency IC

packages. HFSS utilizes a 3D full-wave Finite Element Method (FEM) to compute the electrical behavior of high-frequency and high-speed components.

The HFSS analysis flowchart is shown in Figure 4.11. In the pre-processing stage, the model of the simulated structure is created, and material properties such as dielectric constant, conductivity, and loss tangent in the created model are assigned Afterwards, the source and boundary conditions such as the port assignment are assigned properly in the model. Finally, the solution requirements have to be defined. Then HFSS will solve the problem automatically. In the post-processing stage, HFSS can provide S, Y, Z parameters, and visualized 3D electromagnetic fields.

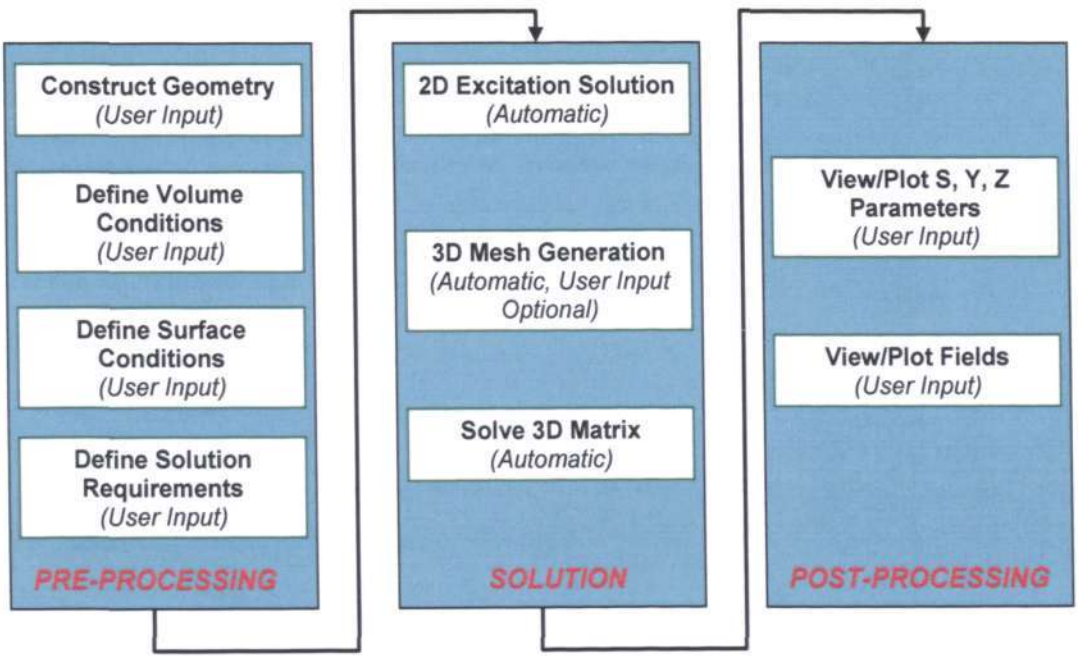


Fig 4.11: The simulation flowchart using HFSS software

4.3.3 Ground Surrounding Effects

Figure 4.12 is the model of a three turns inductor created by HFSS 3D modeler. The geometries of the inductor are listed in Table 4.2. The line width and space are 10 μm. The

outer diameter of the spiral inductor is 260 μm. The center gap is 160 μm. The thickness of the metal is set to be 1 μm. The thickness of silicon dioxide is 5 μm. The thickness of silicon substrate is 450 μm and conductivity of silicon substrate is 10 S/cm.

Table 4.2: Geometries of the inductor 3D model shown in Figure 4.12

line width w	line space s	outer diameter d_{out}	inner diameter d_{in}	metal thickness t_m	turn N
10 μm	10 μm	260 μm	160 μm	1 μm	3

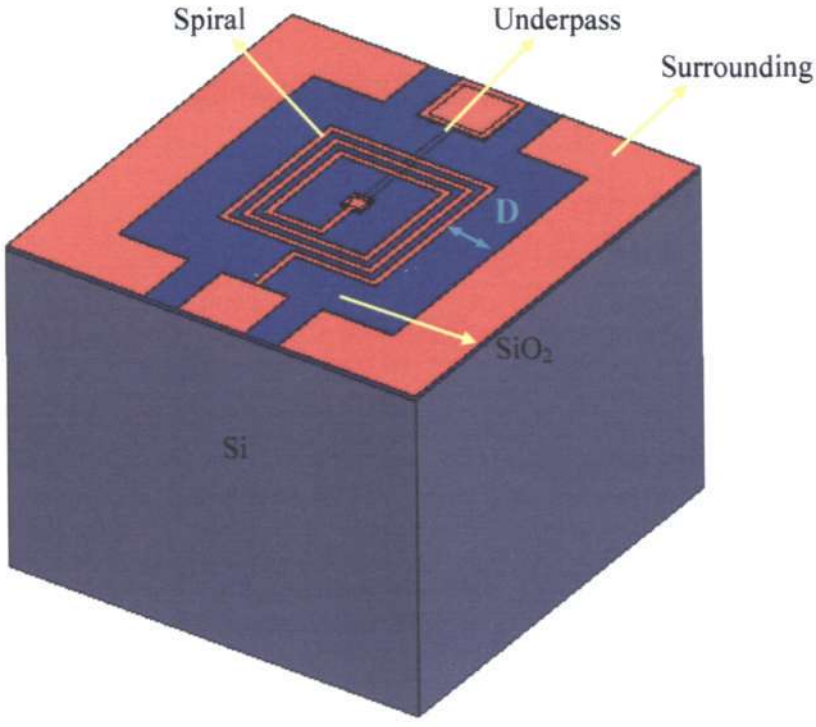
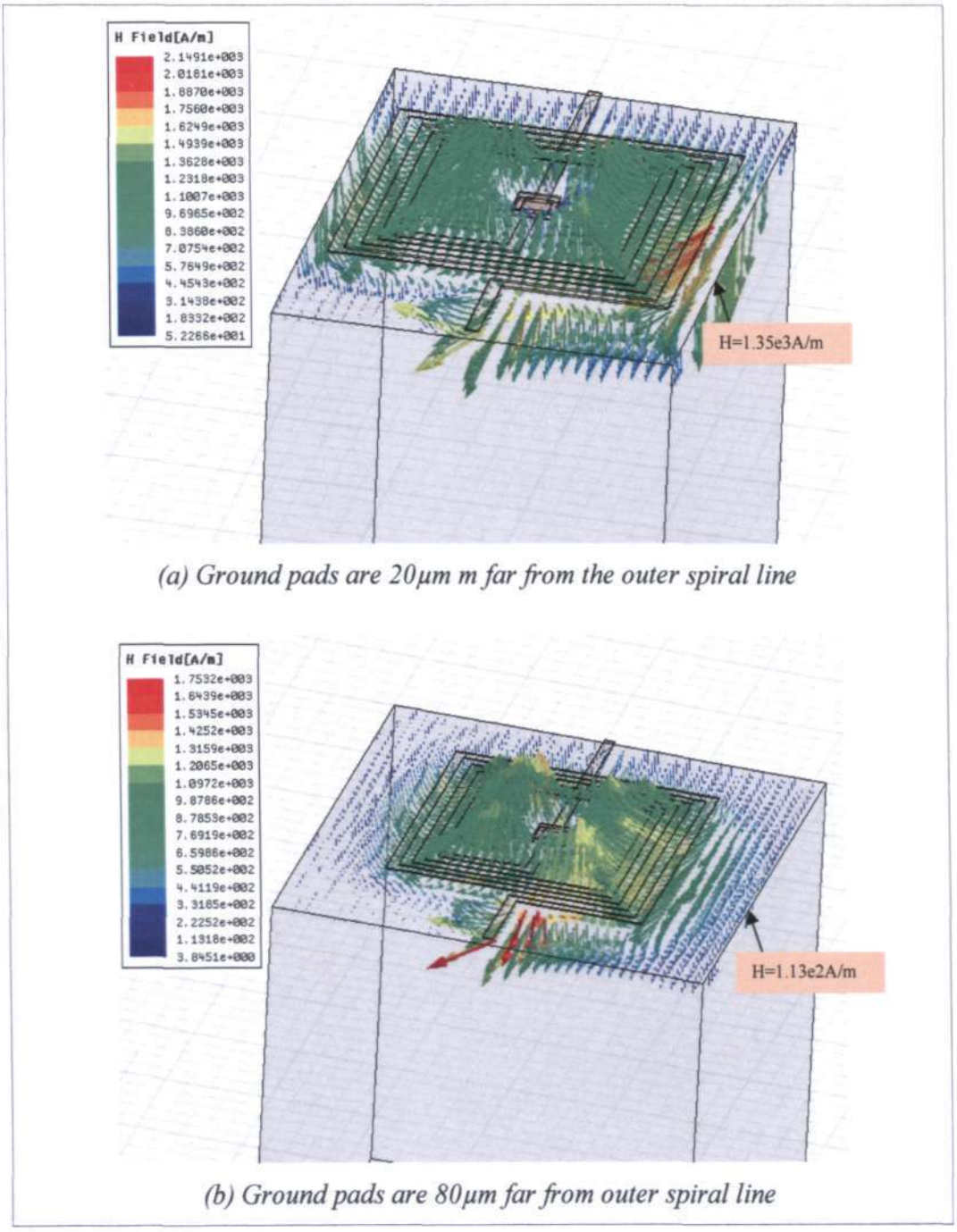


Figure 4.12: Inductor model in HFSS simulator

In Figure 4.12, the distance D, which is from the surrounding to the spiral, has been varied from 20 μm to 80 μm to validate the surrounding effect on the performance of inductor. The simulation results are shown in Figure 4.13 and 4.14. Figure 4.13 is the distribution of magnetic flux of the inductor with D values of 20 μm and 80 μm. The magnetic flux density

is 1.13e2 A/m at the surrounding when the distance is set to be 80 μm, compared to the larger flux density of 1.35e3 A/m while the distance is set to be 20 μm. The larger magnetic flux density near the surroundings results in larger losses due to the eddy current in the surroundings.



(a) Ground pads are 20μm m far from the outer spiral line

(b) Ground pads are 80μm far from outer spiral line

Fig 4.13: Simulated magnetic flux density using HFSS

The simulated quality factors for different values of distance D are shown in Figure 4.14. The peak value of quality factor slightly increases as the distance increases. With a distance of 20 μm, the peak value of quality factor is 5.05. When the distance is increased to 80 μm, the peak quality factor is 5.24. This improvement can be explained as the less coupling to the surroundings for larger distance D. But, from the simulation results we can see the surrounding effect is neglectable on the performance of inductor. The designed gaps between the surrounding and spiral structure is set to be 80 μm in following designs.

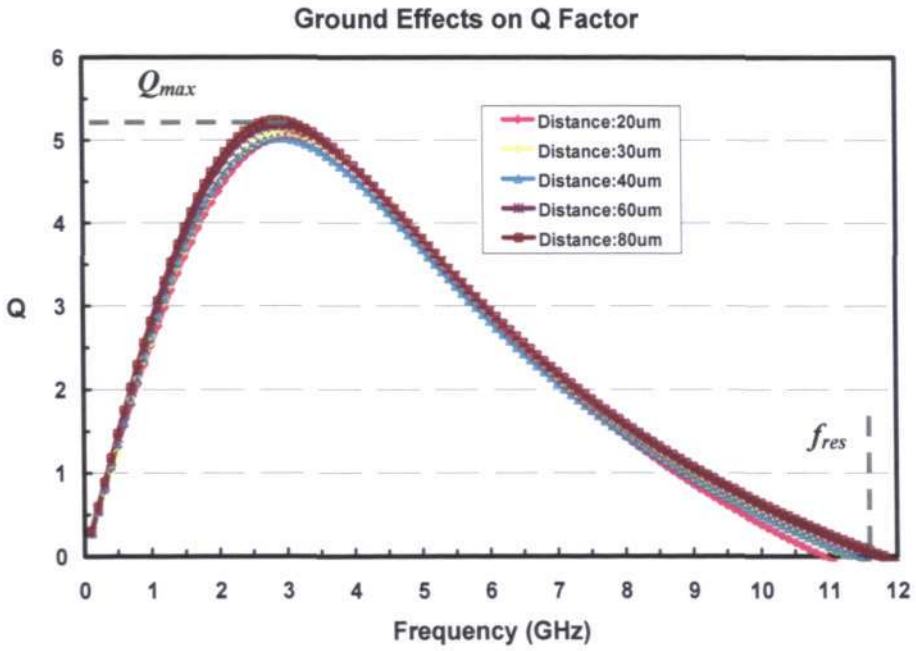


Fig 4.14: The distance effects of ground pads on the quality factor

4.3.4 Line Width Effects

By varying the value of line width in Table 4.2, the effects of line width on the performance of inductor are explored. Figure 4.15 shows the simulation results of different line widths, which are changed from 2 μm to 16 μm. From this figure we can see that the peak value of quality factor increases with increase of line width, while the self resonant frequency

decreases with increase of line width. At low frequency, the quality factor increases much rapidly because the wider line width is, the smaller series resistance of the inductor will be, and the parasitic substrate losses are neglectable. However, at higher operation frequency, the parasitic losses of the larger line width become more and more considerable, resulting in the fast decrease of the quality factor and lower self-resonant frequency compared to the inductors with the smaller line width. So there is a compromise between quality factor and self resonant frequency when the line width is to be set. As seen from Figure 4.15, the maximum Q value and the self-resonant frequency for the inductor with line width of 2 μm is 2.5 and 14 GHz, respectively, while these values are 5.5 and 10.7 GHz for the inductor with line width of 16 μm. The line width value is set to be 10 μm in the following designs.

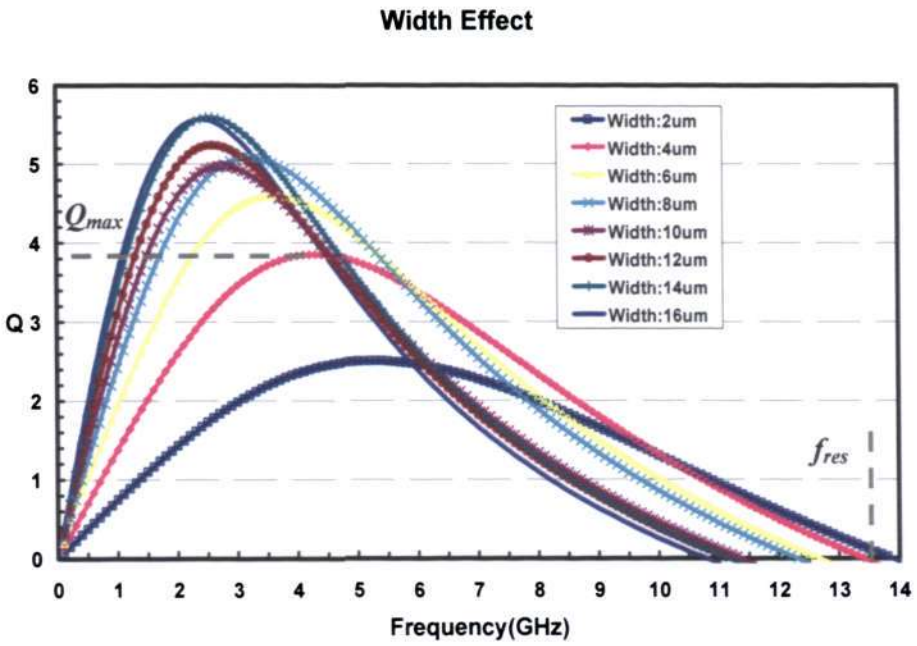


Fig 4.15: Simulated quality factors of inductors with different line widths

4.3.5 Line Space Effects

Figure 4.16 shows the quality factors of the inductors with different line space of 5 μm, 10 μm, and 15 μm, respectively. The results show that the smaller line space contributes better inductor performance. The reason is that the smaller value of line space generates larger positive magnetic coupling, even though smaller line space also causes larger fringing capacitive coupling. The fringing capacitive coupling is slight compared to the magnetic coupling. However, the smaller line space brings difficulty for the fabrication. For example, if the metal pattern is deposited using lift off method, the small space is not feasible because of lift off limitation.

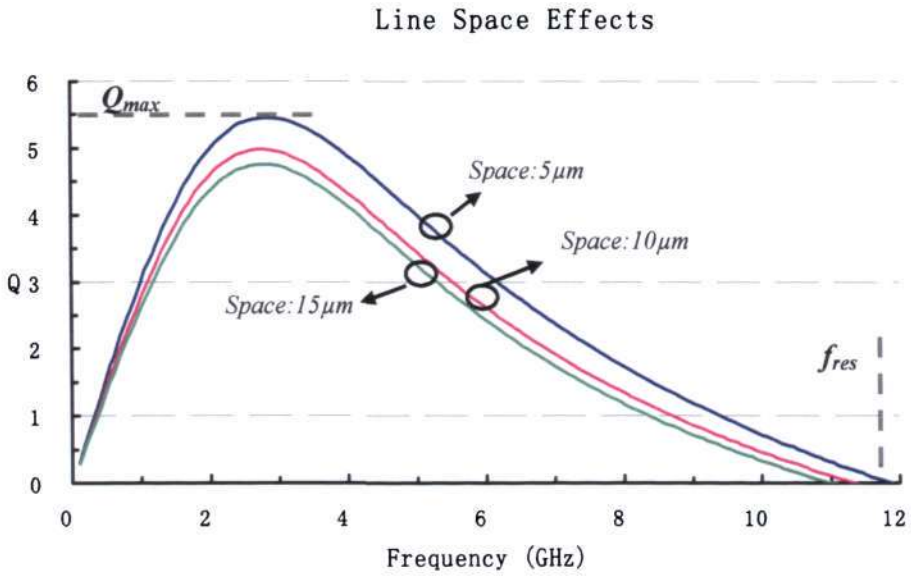


Fig 4.16: Simulated quality factors of inductors with different line spaces

4.3.6 Substrate Effects

Due to the relatively low resistivity of silicon compared with GaAs, substrate losses are the most important factor to degrade the performance of silicon integrated RF inductors. As the loss matters discussed in section 4.1.2, a major source of substrate losses is the capacitive coupling that allows conduction current flow not only through the metal strip, but also

through the silicon substrate. Another important source of substrate losses is inductive coupling. Due to the planar geometry of the inductor, the magnetic field penetrates deeply into the silicon substrate, inducing currents and related losses. If the substrate is simply undoped silicon, its influence on the inductor is only capacitive because it is high resistivity, thus it only affects the self-resonant frequency. Many silicon bipolar or BiCMOS technologies use lightly doped substrates. A spreading resistance must be included to model this type of substrate. This resistance reduces the Q value of the inductor and lowers its self-resonant frequency. For highly conductive silicon substrates used in modern CMOS technology, eddy currents are also magnetically induced in the substrate and adversely affect the inductance of inductors. The comparison of the different substrates is shown in Figure 4.17.

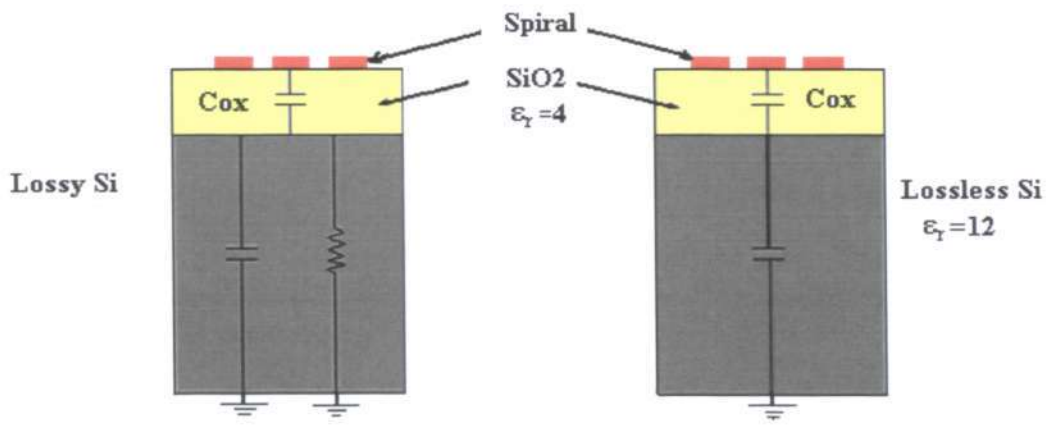


Fig 4.17: Substrate comparison: doped vs. undoped silicon

Since the resistivity of commonly used silicon wafer is in the range of 1-100 Ω·cm, the substrate losses are the main reason for low quality factor of inductor. To reduce the substrate losses, one apparent method is to increase the thickness of oxide layer as insulation layer between spiral metal and silicon substrate.

4.3.7 Oxide Thickness Effects

The thickness of silicon dioxide layer is the most important parameter, which may significantly affect the performance of RF silicon inductors. Compared with silicon substrate, silicon dioxide is insulation material without conductive losses. The permittivity of SiO_2 is 3.9, which is much lower than silicon's permittivity of 11.9. According to the simple capacitance formula: $C = \varepsilon \cdot \frac{A}{d}$, the parasitic capacitance in silicon dioxide is much less than that in the same thick silicon layer because permittivity ε reduced. For RF passive devices built on silicon substrate, the thicker the silicon oxide layer is, the better the performance of these devices will be. The schematic of electronic flux of RF silicon inductor is shown in Figure 4.18. The fluxes penetrate into the substrate and emit into the surroundings.

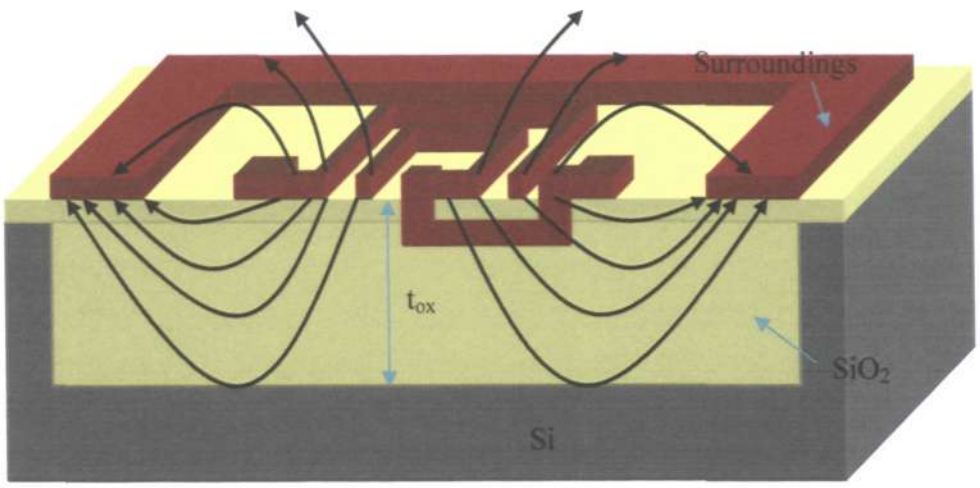


Fig 4.18: The schematic electronic flux of a RF spiral inductor

The simulations of silicon oxide thickness influence on the performance of inductor have been done using HFSS simulator. In the setting of the model structure, the thicknesses of oxide block are varied from 2 μm to 30 μm. The input port in the inductor model is driven by 5 mW RF power. Figure 4.19 shows the electric field distribution at the interface of

silicon and silicon dioxide block at 5 GHz frequency. In Figure 4.19 (a), the oxide layer thickness is 2 μm. Figure 4.19 (b) shows the case of 10 μm oxide layer. Figure 4.19 (c), (d) show the oxide layer of 20 μm and 30 μm, respectively. As shown in Figure 4.19, the electric field penetrated in silicon substrate decreases rapidly with the increase of oxide thickness.

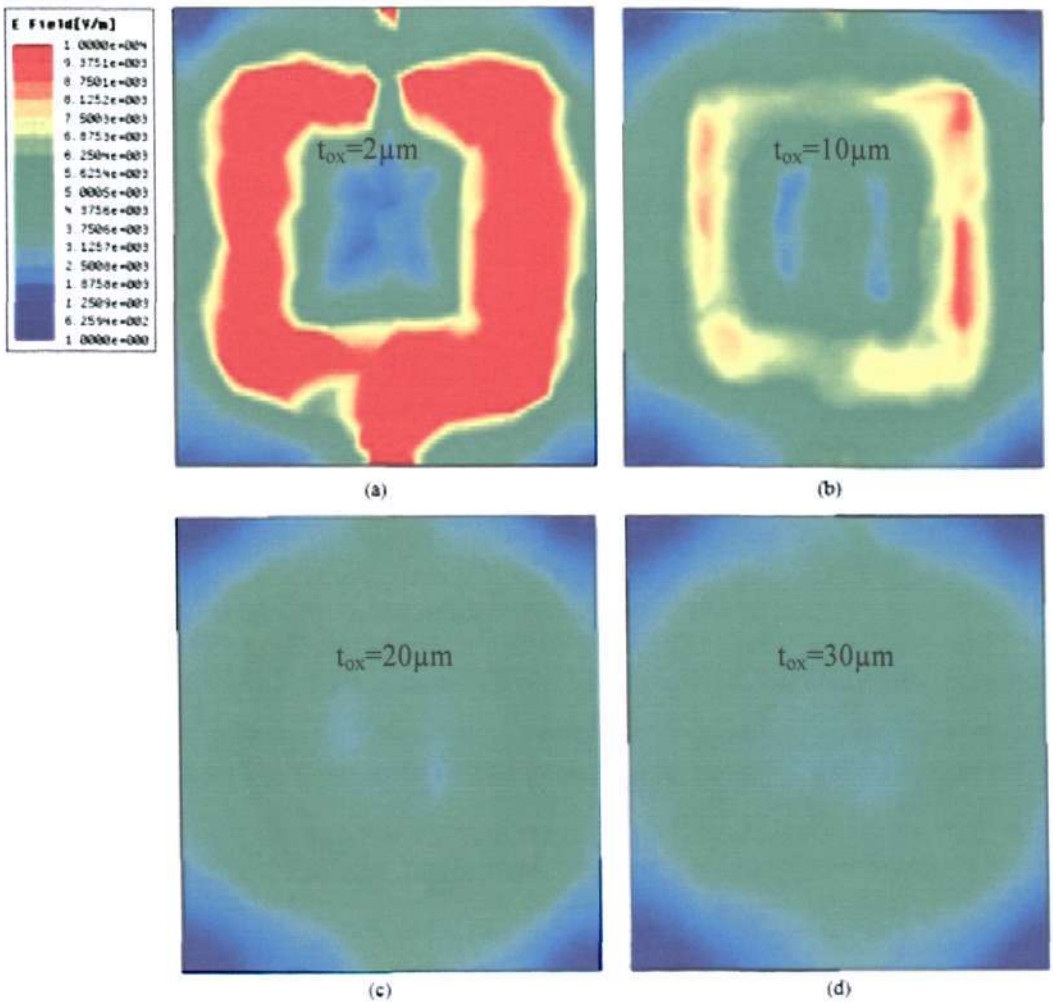


Fig 4.19: Electronic field distribution at the interface of oxide and silicon for an inductor fabricated on different thick SiO_2 based on silicon substrate at 5 GHz

The simulated quality factors of inductors on different thick oxide block are shown in Figure 4.20. The peak value of quality factor is 5 for an oxide layer of 2 μm. When the oxide layer

increases up to 20 μm, the maximum quality factor is increased to 8.1. Another improved characteristic is the self-resonant frequency, which is 14 GHz for an oxide layer of 20 μm, while it is only 11 GHz for an oxide layer of 2 μm. The simulation results show that both quality factor and self resonant frequency are much improved by increasing the thickness of oxide layer. This is because the substrate losses are significantly reduced.

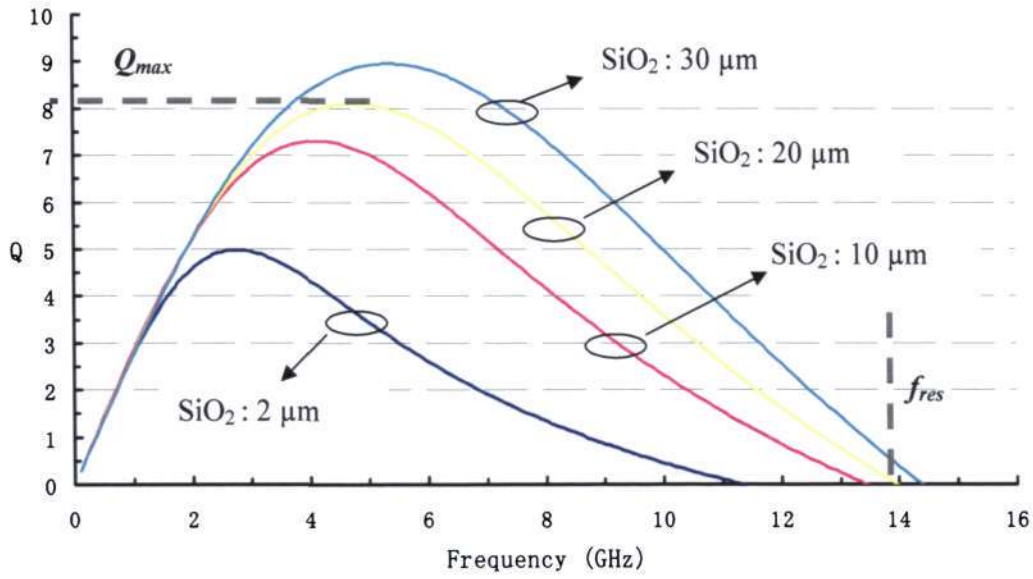


Fig 4.20: Simulated quality factors of an inductor fabricated on SiO_2 blocks with different thicknesses

4.4 Summary

In this chapter, we have discussed the layouts of RF inductors, the mechanisms of parasitic losses, and the characteristics of spiral inductors. The modeling of spiral inductors is also presented for the analysis purpose. The different design aspects including effects of line width, line space, surroundings etc. are analyzed and validated by EM simulations. In the next chapter, the fabrication and measurement of RF spiral inductors will be presented using our developed MEMS technology.

Chapter 5

Fabrication and Measurement of RF Spiral Inductors

Spiral inductor on silicon substrate is an important component in integrated circuit, has in general quite low quality factor by using standard IC technologies. Fortunately, micromachining technologies may provide a way to improve the performance of the RF integrated inductors. In this chapter, RF spiral inductors are fabricated using the so-called SiDeox technology developed during this project. The substrate losses of these RF inductors based on silicon substrate are reduced to a great extent by fabricating them on thick silicon oxide blocks. In section 5.1, the designed inductor masks and the structures of the fabricated inductors are described, and the whole fabrication processes are presented. Section 5.2 reports the measurement results of the fabricated inductors, followed by section 5.3 to summarize this chapter.

5.1 Fabrication of RF Inductors

As presented in Chapter 2, low loss inductors are built on thick SiO_2 block using SiDeox fabrication technology. This section presents the details of photo mask design, the geometries, and fabrication processes of the designed inductors.

5.1.1 Photo Mask Design

The CAD software used in the design of masks for the fabrication of MEMS RF Si inductors is L-Edit Version 10.0. The layout of one inductor die is shown in Figure 5.1. There are altogether four masks designed for the fabrication of RF inductor: fabricate silicon dioxide block, pattern underpass, etch via hole, and pattern top metal layer.

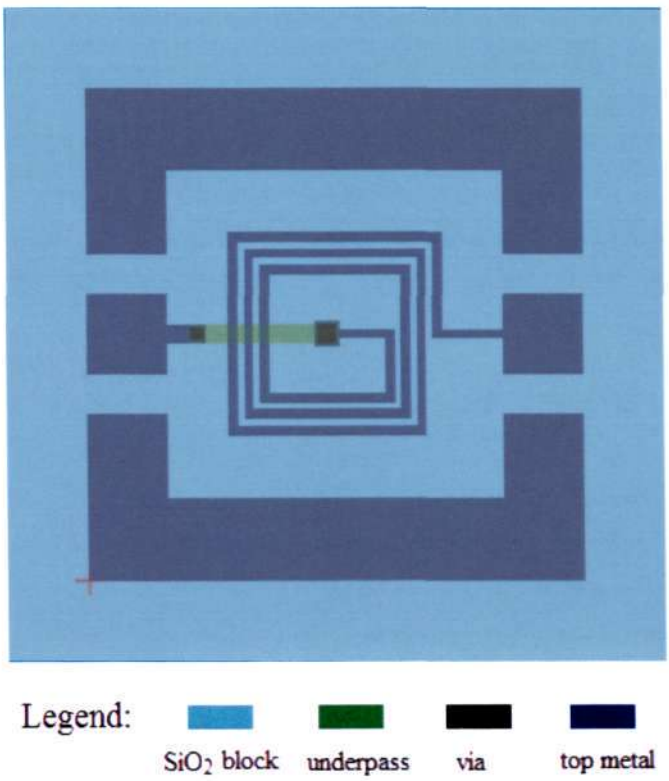


Fig 5.1: Mask layers for fabrication of the RF Inductor

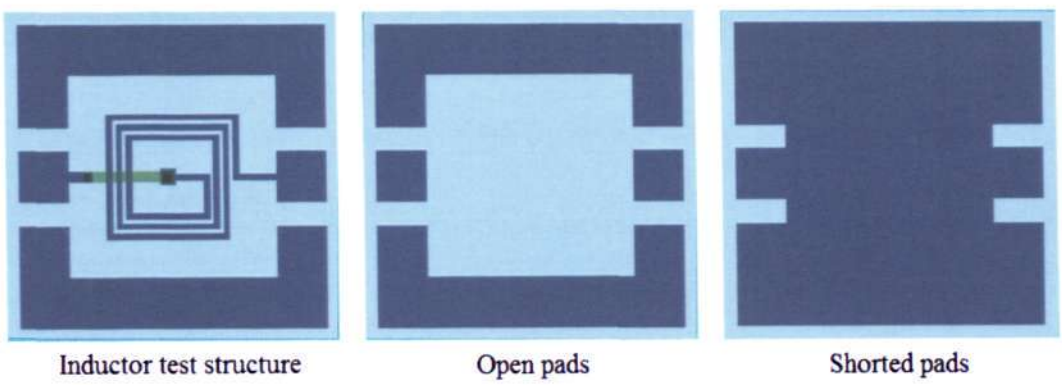


Fig 5.2: Layouts for de-embedding measurement

By taking into consideration of the parasitic losses due to probe pads, de-embedding should be carried out during measurement. Each designed inductor accompanies with a set of open and shorted probe pads for the purposes of de-embedding as shown in Figure 5.2.

5.1.2 Dimensions of Designed Inductors

Inductors with three turns and five turns are fabricated in this work. Line width and line space of the inductors are set to be 10 μm. The total length of the spiral windings are 2700 μm and 5160 μm, respectively. The inductors are fabricated on both oxide blocks of 20 μm, and on 2 μm oxide layer for comparison. The detailed geometries for these inductors are listed in Table 5.1.

Table 5.1: Designed geometries of two spiral inductors

No.	Description	Symbol	Unit	Inductor 1	Inductor 2
1	Line width of spiral inductor	w	μm	10	10
2	Line space of spiral inductor	s	μm	10	10
3	Total line length of spiral inductor	l	μm	2700	5160
4	Outer diameter of spiral inductor	d_{out}	μm	270	350
5	Inner diameter of spiral inductor	d_{in}	μm	150	150
6	Number of turns of spiral inductor	N	no.	3	5
7	Thickness of silicon oxide between spiral windings and underpass	$t_{ox,M1\text{-}M2}$	μm	2	2
8	Thickness of underpass	t_{mu}	μm	1	1
9	Thickness of spiral windings	t_m	μm	1	1
10	Thickness of silicon dioxide	t_{ox}	μm	20	20
11	Thickness of silicon substrate	t_{si}	μm	430	430
12	Permittivity of silicon dioxide	$\varepsilon_{rSiO2}\cdot\varepsilon_0$	F/m	3.542e-11	3.541e-11
13	Permittivity of silicon wafer	$\varepsilon_{rSi}\cdot\varepsilon_0$	F/m	1.054e-10	1.054e-10
14	Conductivity of silicon wafer	σ_{si}	S/m	10	10

5.1.3 Fabrication Processes

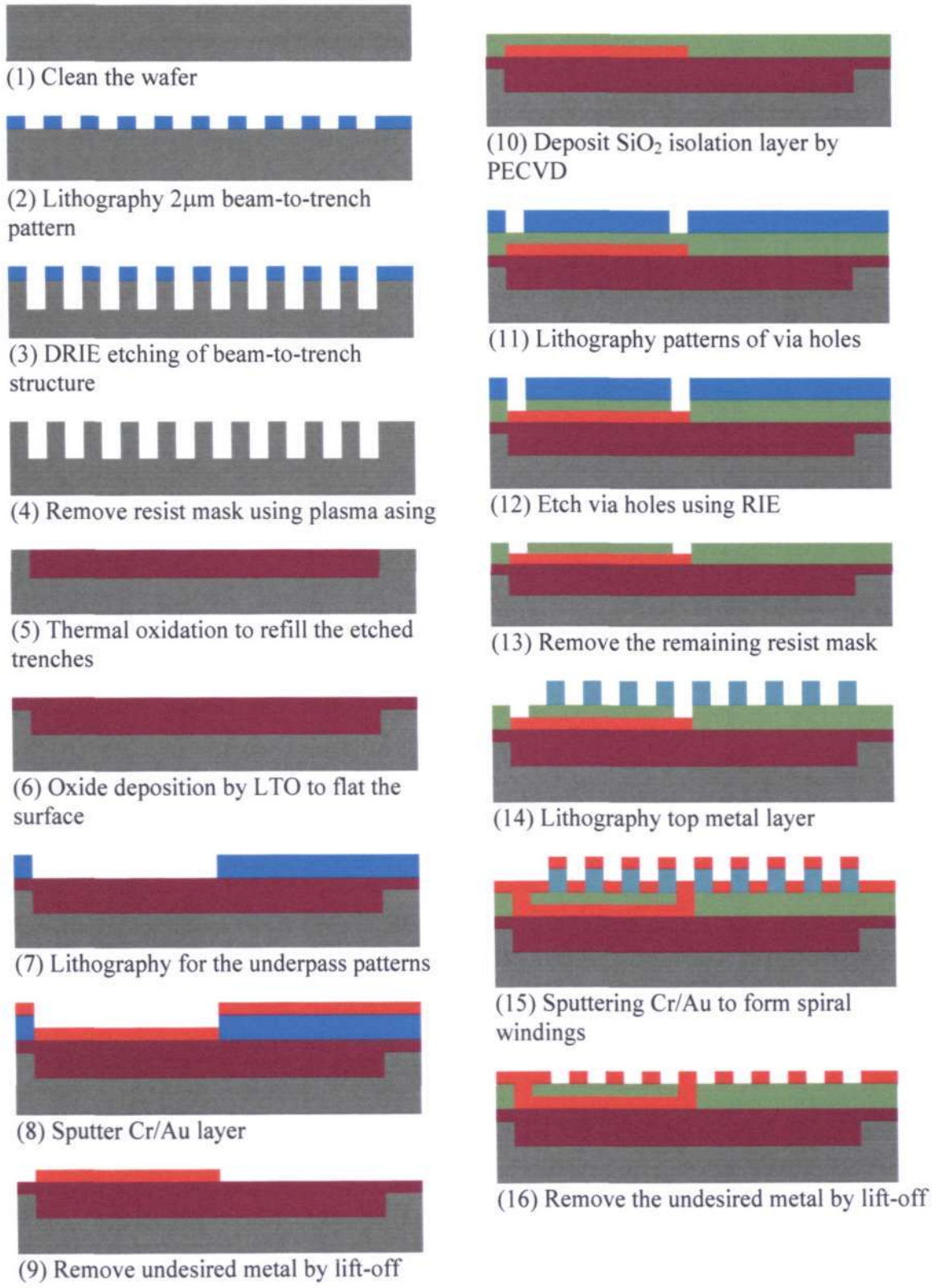


Fig 5.3: Fabrication process flow of spiral inductors on 20 μm SiO_2/Si substrate

Using the designed masks, the inductors are fabricated on both thick silicon dioxide block and thin silicon dioxide layer. The thickness of silicon wafer is 450 μm, and its conductivity is 10 S/m. The fabrication flow is shown in Figure 5.3.

Firstly, the wafer was cleaned in piranha solution. A layer of photoresist AZ 7220 of 2 μm was then spun on the silicon substrate. The beam-to-trench patterns were formed by photo lithography, shown in Figure 5.3 (2). The narrow beam-to-trench structures are etched as deep as 20 μm by DRIE. The widths of the beams and trenches were 2 μm, respectively, and the remained resist mask was etched away using O_2 plasma in RIE machine (step 3-4). Silicon oxide block was then formed after the refilling of the etched structures by thermal oxidation at 1100°C for 10 hours (step 5). After thermal oxidation to form thick silicon dioxide block, a 3 μm silicon dioxide layer was deposited using LTO (low temperature oxidation) at 450°C to make the wafer surface flat (step 6). LTO silicon dioxide was chosen because of its high conformability. Then the underpass of the inductor was created by sputtering Cr (30 nm)/Au (1 μm) layers on the substrate surface patterned with 7 μm AZ9260 photoresist, and removing the undesired metal materials by lift-off process in acetone (step 7-9). The thin Cr layer was used here to improve the adhesion ability between the metal layer and the substrate. The isolation layer between spiral windings and underpass was deposited to be 2 μm thick PECVD silicon dioxide at 300°C (step 10). Thereafter, a layer of 7 μm thick AZ9260 photoresist was spun and patterned on the substrate surface, then via holes connecting underpass and top windings were etched using RIE CF_4/O_2 plasma (step 11-13). Finally, the top spiral windings and surroundings were created by patterning a layer of 7 μm AZ9260 photoresist, sputtering Cr (30 nm)/Au (1 μm) layers, and lift-off process (step 14-16). The detailed process parameters and used machines of the above-mentioned steps, are listed in Appendix B.

5.2 Measurement Procedures

The measurement of the fabricated RF inductors is carried out using a vector network analyzer Anritsu 37347C. S parameters of the measured inductors are then obtained. However, S parameters, which commonly show the reflection loss and transmission loss related to the transmitted wave power, are not adequate to indicate the whole performance of RF inductors.

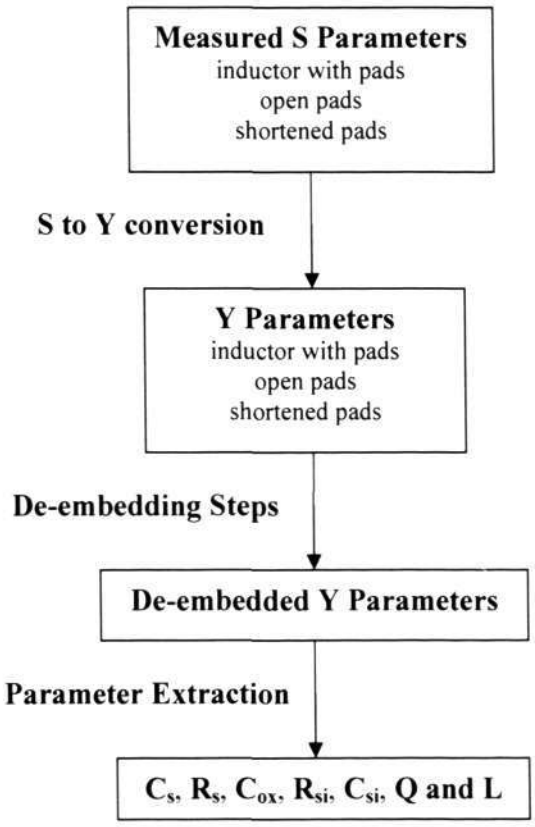


Fig 5.4: Measurement procedures for RF spiral inductors

To calculate the characteristics including quality factor, self resonant frequency, and inductance, S parameters need to be converted to Y parameters, which represent admittance parameters. The parasitic losses due to the probe pads should be excluded from the measured raw data. De-embedding process is required to remove the influences of probe pads. Finally,

the parameters such as the quality factors Q, inductances L, and the parasitic values of the components in the equivalent circuits of the inductors etc. are extracted from the Y parameters. The process flow to deal with the measured data, which is to be discussed in the section, is shown in Figure 5.4.

5.2.1 Two-Port Network of an Inductor

The two-port network of a spiral inductor is illustrated in Figure 5.5. S parameters represent the transmission coefficients and reflection coefficients at the two ports of the inductor. When the port 2 is shorted to ground, S_{11} means the reflection loss due to the impedance mismatching, and S_{21} means the insertion loss which refers to the RF loss dissipated in the inductor. As shown in the Figure 5.5, V_1^+ represents the incident voltage wave from port 1, and V_1^- represents the reflected voltage wave from port 1. V_2^+ and V_2^- are the ones for port 2. The S parameter matrix of a two port network is:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{5.1}$$

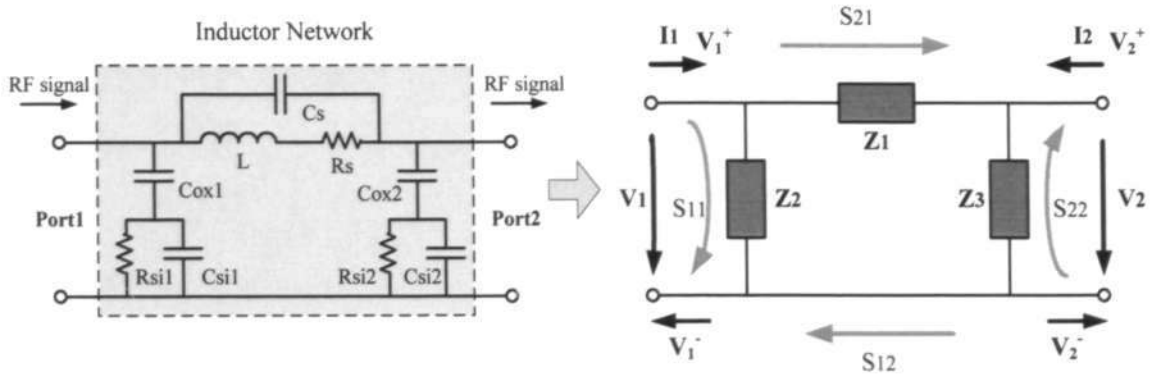


Fig 5.5: Two-port network of a spiral inductor

The S parameters for a spiral inductor, which are derived using the network theory, are shown as follows:

$$S_{11} = \frac{Z_2 // (Z_1 + Z_3 // Z_0) - Z_0}{Z_2 // (Z_1 + Z_3 // Z_0) + Z_0} \tag{5.2}$$

$$S_{21} = (1 + S_{11}) / (1 + \frac{Z_1}{Z_3 + Z_0}) \tag{5.3}$$

$$S_{22} = \frac{Z_3 // (Z_1 + Z_2 // Z_0) - Z_0}{Z_3 // (Z_1 + Z_2 // Z_0) + Z_0} \tag{5.4}$$

$$S_{12} = (1 + S_{22}) / (1 + \frac{Z_1}{Z_2 + Z_0}) \tag{5.5}$$

where "//" means resistors are connected in parallel. Z_1, Z_2, Z_3 are the branch impedances as shown in Figure 5.5. Z_0 is the characteristic impedance of the terminators.

Y parameters, which are the admittance matrix of two-port network of a spiral inductor, are defined as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5.6}$$

For the spiral inductor network as shown in Figure 5.5, each component of the Y matrix can be derived as follows:

$$Y_{11} = \frac{Z_1 + Z_2}{Z_1 Z_2} \tag{5.7}$$

$$Y_{12} = Y_{21} = -\frac{1}{Z_1} \tag{5.8}$$

$$Y_{22} = \frac{Z_1 + Z_3}{Z_1 Z_3} \tag{5.9}$$

Y_{11}, in equation (5.7), is the input admittance of port 1 when port 2 is shorted to ground. Therefore, it can be used to calculate the quality factor of a spiral inductor as equation (4.15).

For an inductor working in high frequency range, Y parameters can not be obtained directly because current and voltage at the ports are not available to be measured. The Y parameters can be calculated after the measurement of S parameters using the following formula:

$$[Y] = \frac{[I]-[S]}{Z_0([I]+[S])} \tag{5.10}$$

where **[Y]**, **[S]** are the matrices of Y parameters and S parameters and **[I]** is the unit matrix.

5.2.2 Measurement Setup

The S parameters of the fabricated inductors are characterized experimentally from on-wafer measurements by the mean of vector network analyzer (Anritsu 37347C) and a probe station with GSG (ground-signal-ground) pattern probe tips. The probes consists of two ground-signal-ground coaxial probes mounted on port 1 and port 2, respectively. In order to eliminate the imperfection of the measurement system, calibrations are conducted before the actual measurement. A short-load-open-through (SLOT) calibration technique as shown in Figure 5.6 is applied.

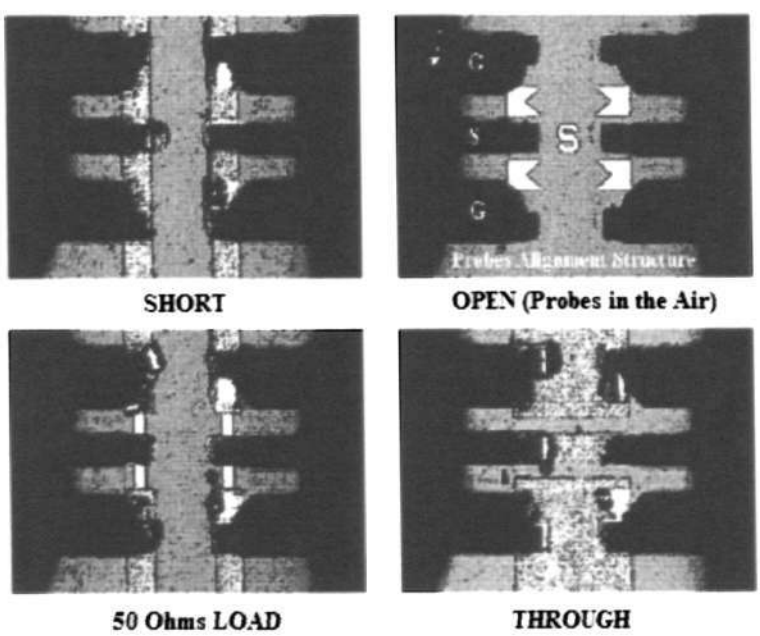


Fig 5.6: SLOT calibration process

The short calibration is to short each GSG probe by a straight Au line for the calibration of S11=-1. For open calibration, the two GSG probes are floated in the air so that S11=1. This two cases mean that all the power is totally reflected back from the port. In the load calibration, each GSG probe is terminated to a 50 ohm resistor for the calibration of S11=0 and S21=0, which means the input power are totally dissipated. The through calibration is to connect the two probes by a short Au line so that S11=0 and S21=1, which means all the power transmitted from port 1 to port 2. The S-parameter measurements are then carried out from the frequency range of 0.1 GHz to 20 GHz.

5.2.3 De-embedding Theory

The measurement results of S parameters include the parasitic losses of the probe pads, which may have the same order of magnitude compared to the inductor impedances. As a result, measurement errors occur. In order to remove these measurement errors, de-embedding technique is applied.

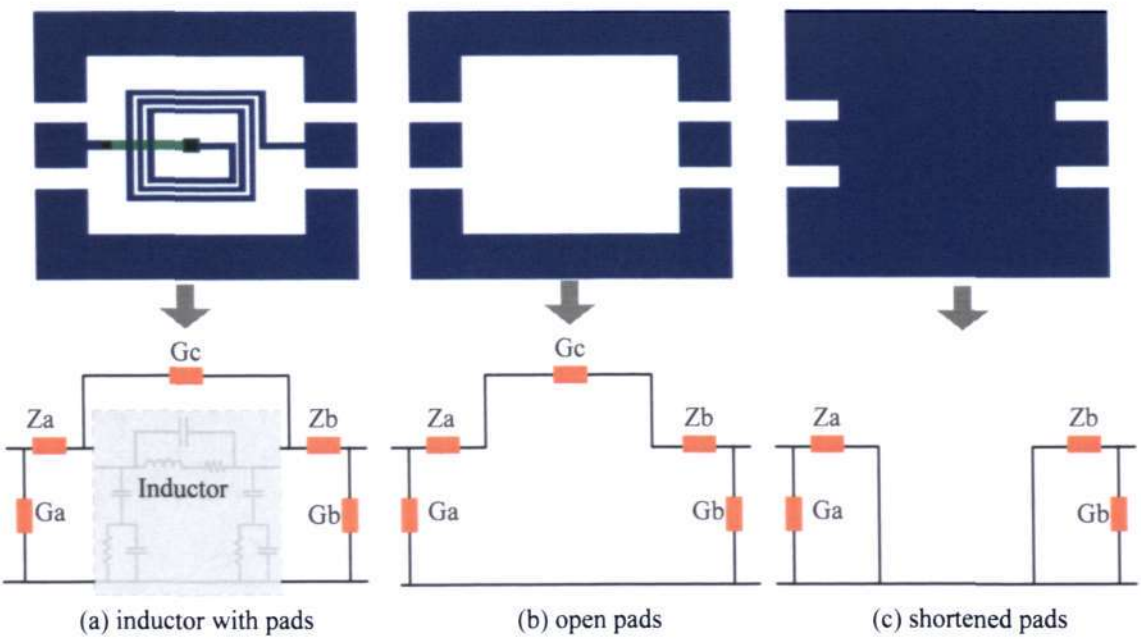


Fig 5.7: De-embedding models

As shown in Figure 5.7, the parasitic losses due to the probe pads can be modeled as series impedances (Z_a, Z_b) and shunt admittances (G_a, G_b). G_c represents the coupling parasitic between two pads.

After converting S parameters to Y parameters, three groups of Y parameters of Y_{toatal} with pads, Y_{open} with open pads, and Y_{short} with shortened pads, are obtained.

For the open pads model in Figure 5.7 (b), Y_{open} parameter includes the values of the pad shunt parasitic G_a and G_b as well as coupling parasitic G_c. The values of Z_a and Z_b can be neglected compared to $1/G_c$. Hence

$$Y_{11openpads} = G_a + G_c \tag{5.11}$$

$$Y_{22openpads} = G_b + G_c \tag{5.12}$$

$$G_c = \frac{-(Y_{21openpads} + Y_{12openpads})}{2} \tag{5.13}$$

G_a and G_b can be obtained from above equations. G_a and G_b are then subtracted from the inductor test measurement result of Y_{total} to obtain Y_a, after removal of G_a and G_b from Y parameters.

$$Y_{11a} = Y_{11total} - G_a \tag{5.14}$$

$$Y_{22a} = Y_{22total} - G_b \tag{5.15}$$

$$Y_{12a} = Y_{12total} \tag{5.16}$$

$$Y_{21a} = Y_{21total} \tag{5.17}$$

The Y_{short} parameters are used to obtain Z_a and Z_b. As shown in Figure 5.7 (c), the values of Z_a and Z_b can be calculated as:

$$Z_a = \frac{1}{Y_{11short} - G_a} \tag{5.18}$$

$$Z_b = \frac{1}{Y_{22short} - G_b} \tag{5.19}$$

After Y_a parameters are converted to Z_a parameters through matrix inversion, the series impedances Z_a and Z_b are then removed from the Z_a parameters by:

$$Z_{11b} = Z_{11a} - Z_a \tag{5.20}$$

$$Z_{22b} = Z_{22a} - Z_b \tag{5.21}$$

$$Z_{12b} = Z_{12a} \tag{5.22}$$

$$Z_{21b} = Z_{21a} \tag{5.23}$$

By inverting the matrix of Z_b parameters, Y_b parameters which corresponds to the inductor test structure with G_a, G_b, Z_a and Z_b removed are obtained. The final de-embedded Y parameters Y_{de} are found as follows:

$$Y_{11de} = Y_{11b} - G_c \tag{5.24}$$

$$Y_{12de} = Y_{12b} + G_c \tag{5.25}$$

$$Y_{21de} = Y_{21b} + G_c \tag{5.26}$$

$$Y_{22de} = Y_{22b} - G_c \tag{5.27}$$

After the de-embedding process has been conducted, the parasitic losses due to probing pads are excluded from the measurement.

5.2.4 Parameter Extraction Method

Knowledge of the layout of the equivalent circuit model for an inductor is needed to determine the L, R, and C components values analytically. Together with the de-embedded Y parameters, these component values in the inductor circuit model are extracted with the aid of numerical computation tools.

See from equations (5.7)-(5.9), the de-embedded Y parameters can be expressed as:

$$Y_{12de} = -\frac{1}{Z_1} = -j\omega C_s - \frac{1}{j\omega L + R_s} \tag{5.28}$$

$$Y_{11de} + Y_{12de} = \frac{1}{Z_2} = \frac{1}{\frac{1}{j\omega C_{ox1}} + \frac{R_{si1}}{1 + j\omega C_{si1} R_{si1}}} \tag{5.29}$$

$$Y_{22de} + Y_{12de} = \frac{1}{Z_3} = \frac{1}{\frac{1}{j\omega C_{ox2}} + \frac{R_{si2}}{1 + j\omega C_{si2} R_{si2}}} \tag{5.30}$$

Obviously, the extraction process of each component value is actually an optimization problem. In this process of parameters extraction, a genetic algorithm is implemented to fix these component values with the de-embedded Y parameters. The values of given random populations within the possible ranges for each individual component are utilized to generate derived Y parameters. The measured Y parameters together with the derived Y parameters are applied to the objective function $F_0(X)$. The objective function $F_0(X)$ of this program as described in equation (5.31) consists of two parts. The first part is the average errors between the derived Y parameters and the measured Y parameters. The latter part is the variance of the average errors.

$$F_0(X)\Big|_{X=(x_1, x_2, \cdots x_n)} = \sum_{i=1}^{m} (f_i(X)^2 + [f_i(X) - F_{mean}]^2) \tag{5.31}$$

In equation (5.31), the vector $X = (x_1, x_2, \ldots, x_n)$ represents the component values to be extracted (L, R_S, C_S of block Z_1, C_{Ox1}, R_{Si1}, C_{Si1} of block Z_2 and C_{Ox2}, R_{Si2} and C_{Si2} of block Z_3) where n is the total number of parameters in each block. *m* is the total number of frequency points under consideration. The definition of $f_i(X)$, given in equation (5.32), is the error between the derived Y parameters and the measured Y parameters at each frequency

point. F_{mean} is the mean error within the whole concerned frequency range, which is defined in equation (5.33).

$$f_i(X) = \frac{Y_{derived(i)} - Y_{measured(i)}}{Y_{measured(i)}} \tag{5.32}$$

$$F_{mean} = \frac{\sum_{i=1}^{m} f_i(X)}{m} \tag{5.33}$$

In the Genetic Algorithms, each chromosome is a vector consisting of values of L, R_S, C_S, C_{Ox1}, R_{Si1}, C_{Si1}, C_{Ox2}, R_{Si2} and C_{Si2}. The fitting value of each chromosome is evaluated according to the objective function $F_0(X)$ in equation (5.31). After evaluation, chromosomes with smaller fitting value have higher chance to be selected out for reproduction. The generated offsprings are evaluated as well and the reproduction is continued. After 100 generations, the most optimized chromosomes are obtained as the final answer. The optimized values are the ones that are able to make the simulation results fit the measured data closest over the whole concerned frequency range.

The whole procedures to extract the component values from the measured Y parameters are realized using MATLAB program as presented in Appendix C.

To extract the quality factor of an inductor from the measured Y parameters, the following equation, which has been derived in Chapter 4, is used:

$$Q = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} = \frac{\mathrm{Im}(\frac{1}{Y_{11}})}{\mathrm{Re}(\frac{1}{Y_{11}})} = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{5.34}$$

The inductance value of an inductor is extracted from Y parameters as:

$$L = \frac{\mathrm{Im}(\frac{1}{Y_{11}})}{2\pi f} \tag{5.35}$$

The self-resonant frequency f_0 is the frequency value when the imaginary part of input impedance equal to zero, that means when the Q value is zero.

As described in Chapter 4, the extracted values of quality factor and inductance are accurate when the frequency is far away from self-resonant frequency f_0. At the frequency range near self-resonant frequency, they may be no more accurate because of the significant influence of the substrate parasitic losses.

5.3 Results and Discussions

The designed inductors are fabricated using the developed SiDeox fabrication technology. Figure 5.8 shows the SEM picture of the fabricated three-turn inductor built on the 20μm silicon dioxide block, while Figure 5.9 shows a five-turn inductor.

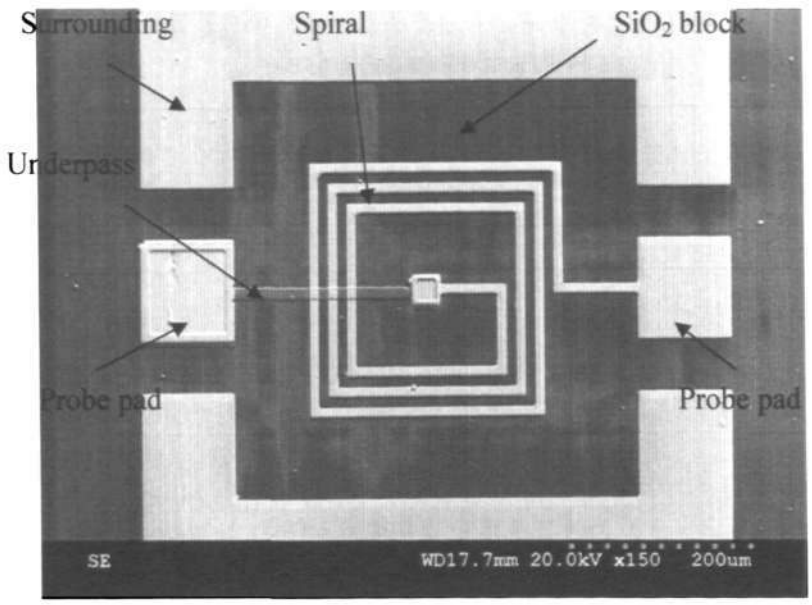


Fig 5.8: SEM photo of fabricated three turn inductor on 20μm oxide block

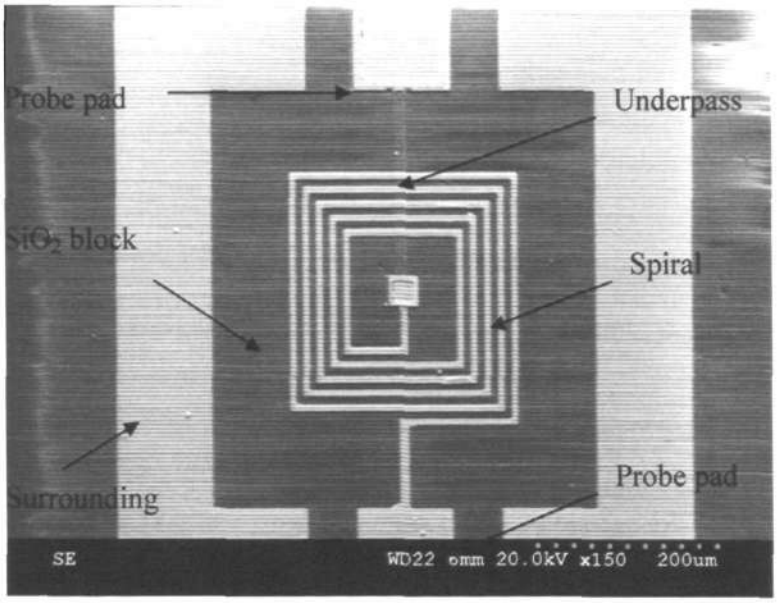


Fig 5.9: SEM photo of fabricated five turn inductor on 20 μm oxide block

As shown in these pictures, the ripples on the surface are still visible, partly due to the transparent property of the deposited PECVD SiO_2 layer. Of course, the surface is not extremely smooth even though additional PECVD SiO_2 deposition can give much improvement. But it has no significant influences on the success of inductor fabrication.

Table 5.2: Fitting parameters for the three-turn inductor

No.	Description	Symbol	Units	On 2μm SiO_2	On 20μm SiO_2
1	Inductance	L	nH	4.02	3.84
2	Series resistance	R_s	Ω	20.25	19.76
3	Series capacitance	C_s	fF	9.46	7.86
4	Oxide capacitance	C_{ox1}	fF	298.34	29.46
5	Silicon resistance	R_{si1}	Ω	682.45	679.45
6	Silicon capacitance	C_{si1}	fF	84.26	73.82
7	Oxide capacitance	C_{ox2}	fF	287.52	24.81
8	Silicon resistance	R_{si2}	Ω	742.36	738.91
9	Silicon capacitance	C_{si2}	fF	76.14	67.36

Table 5.3: Fitting parameters for the five-turn inductor

No.	Description	Symbol	Units	On 2μm SiO_2	On 20μm SiO_2
1	Inductance	L	nH	10.46	9.72
2	Series resistance	R_s	Ω	28.16	25.71
3	Series capacitance	C_s	fF	10.42	8.94
4	Oxide capacitance	C_{ox1}	fF	502.36	53.48
5	Silicon resistance	R_{si1}	Ω	781.32	785.16
6	Silicon capacitance	C_{si1}	fF	97.16	82.56
7	Oxide capacitance	C_{ox2}	fF	478.16	50.63
8	Silicon resistance	R_{si2}	Ω	795.85	805.63
9	Silicon capacitance	C_{si2}	fF	81.76	78.69

The properties of these inductors on thick oxide blocks are compared with the normally fabricated inductors which are on 2 μm SiO_2/Si. As shown in Table 5.2 and 5.3, the values of the components in circuit model for the fabricated three-turn inductors are fixed in the whole measured frequency range using Genetic Algorithms optimization.

Figure 5.10 and 5.11 show the parameter fitting circuit models for the measured three-turn and five-turn spiral inductors on 20 μm SiO_2/Si substrate. The values in bracket are the extracted parameters for the inductors on 2 μm SiO_2/Si substrate. The shunt parasitic capacitances are lower at the output port because the inner turn of the spiral is shorter in length than the input port outer turn. This results in an asymmetry in the extracted parameter values for C_{ox}, C_{si} and R_{si} in the model.

Compared with the extracted parameters for the inductors built on thin oxide layer and thick oxide block, all the component values except the parasitic capacitance C_{ox} are almost similar. However, the C_{ox} value for inductors fabricated on thick oxide block significantly decreases to about one tenth of the values for the inductors on thin oxide layer. Consequently, the

power that penetrates into the substrate is notably reduced, thus the qualify factors and self-resonant frequencies are improved a lot.

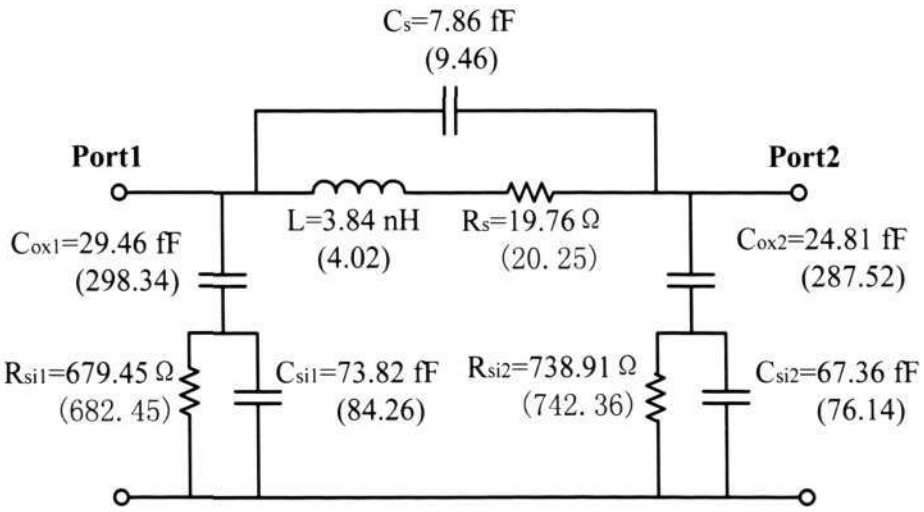


Fig 5.10: Parameter fitting circuit model for the measured three turn inductor

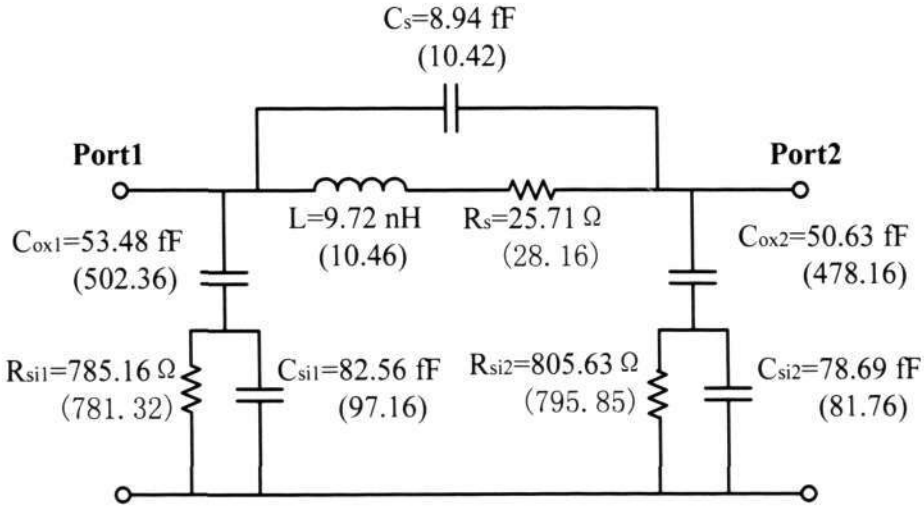


Fig 5.11: Parameter fitting circuit model for the measured five turn inductor

Figure 5.12 shows the quality factors and inductances for the three-turn inductors fabricated on oxide block and thin oxide layer. The measurement values are quite agreed with the simulation values. The maximum value of quality factor for the inductor on 2 μm thin SiO_2

is 4.2. However, the maximum quality factor achieves to 7.6 when the inductor is built on 20 μm SiO_2 block. The self-resonant frequency also increases from 10 GHz to 14 GHz. The extracted inductance value show in Figure 5.12 is around 3.2 nH at low frequency. The calculated inductance value for the three-turn inductor is 3.56 nH using Greenhouse method. The extracted inductance value gradually increases with the frequency increases because the coupling capacitance boosts the effective inductance L as a function of frequency.

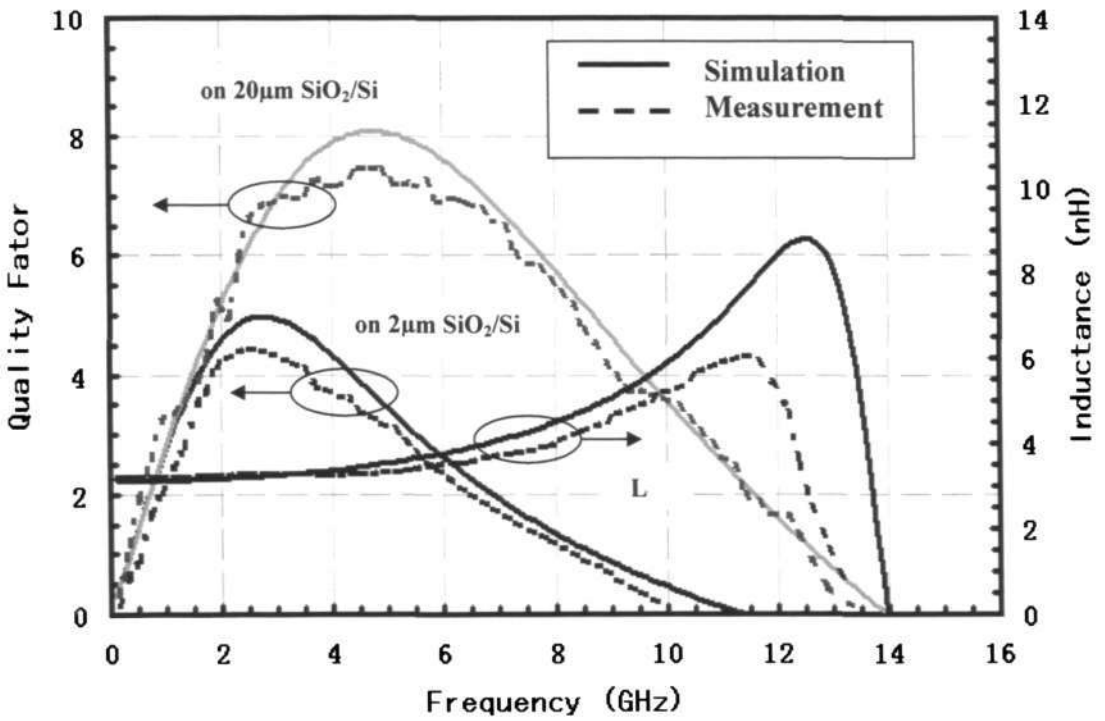


Fig 5.12: Inductance and quality factors of three-turn inductors fabricated on 2 μm SiO_2/Si and 20 μm SiO_2/Si.

Figure 5.13 shows the simulated and measured results of the five-turn inductor. The quality factor and self-resonant frequency of the five-turn inductor on thick SiO_2 is about 7 and 6.6 GHz, compared to 3.5 and 4.6 GHz of that inductor on the thin SiO_2, respectively. The calculated inductance using Greenhouse method is 8.8 nH, which is shown in Appendix D, while the extracted inductance at the low frequency is 8.5 nH, which is very close to the

calculated value. The extracted inductance value also gradually increases with the frequency due to the coupling capacitance.

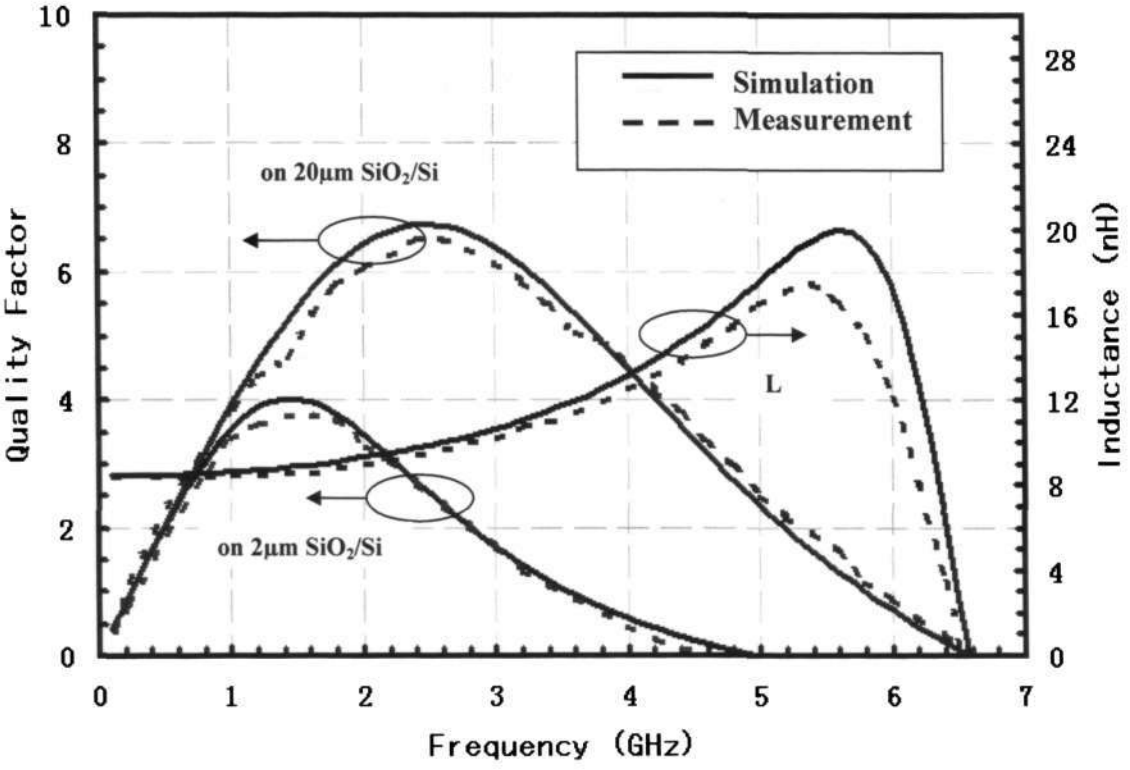


Fig 5.13: Inductance and quality factors of the five-turn inductor fabricated on 2 μm SiO_2/Si and 20 μm SiO_2/Si

5.4 Summary

In this chapter, the fabrication and measurement results of the spiral inductors are presented. In the fabrication part, the design of photomasks, two different geometries of fabricated inductors, and the fabrication processes of these inductors on 20 μm thick oxide block are described in detail. The two-port network theory of inductors is derived to calculate the S and Y parameters. To measure the inductors, de-embedding process and the method of parameter extraction are discussed. The measurement results of the inductors on thick SiO_2 block using SiDeox processes and on thin SiO_2 layer using normal fabrication processes are

compared, showing that the thick oxide block can significantly reduce the substrate losses and contribute to the improvement of inductor performance.

Chapter 6

Design and Fabrication of RF Resonators and Filters Using MEMS Technologies

In the previous chapter, the fabrication of RF inductors based on silicon substrate was presented. Silicon has many advantages as a substrate material for integrated electronic system including low cost, good thermal [108] and stable mechanical properties [109]. These make silicon capable of supporting high-performance microwave and millimeter wave circuitry. Most importantly, the precise micromachining of grooves and holes in silicon substrate by MEMS technology has been utilized to produce many kinds of high performance microwave and millimeter wave components [110-115]. For example, micromachining of grooves in the apertures between the signal and ground conductors in finite ground coplanar waveguide (FGCW) has produced extremely low loss planar transmission lines to a frequency extending beyond 100 GHz [110].

In this chapter, the research work on passive RF resonators and filters for microwave and millimeter wave applications is explored by using developed MEMS technology. Several devices had been designed and fabricated by using SiDeox (silicon deep etching and oxidation) fabrication processes and through-hole electroplating technology. These special resonators have relative smaller size and can be used for filters or VCOs (voltage controlled oscillators) [116-118]. These resonators are constructed using different planar structures such as the conductor-backed coplanar waveguides and microstrip lines. In section 6.1, three designs of resonators and filters are introduced: they are a conductor-backed coplanar

waveguide (CBCPW) feed coplanar strip ring resonator, a novel high pass filter made by CBCPW and microstrip line (MSL), and a miniaturized ground guided patch resonator and filter. In section 6.2, the fabrication technologies are presented. Section 6.3 gives the measured results and discussions of the performances of these devices. Section 6.4 concludes this chapter with a summary.

6.1 Designs of Passive RF Resonators and Filters

6.1.1 CBCPW-Fed-CBCPS Ring Resonator

In this subsection, a conductor backed CPW (CBCPW) feed conductor backed CPS (CBCPS) ring resonator is designed as shown in Figure 6.1. This resonator combines the advantages of ring resonator, CBCPW and CPS. The ring resonators have been widely used to measure the effective dielectric constant, dispersion, phase velocity, discontinuity parameters, and also to determine the optimum thickness of the substrate thickness [119-121]. They can also be used to build up filters, oscillators, mixers and antennas. The ring resonators have the freedom from the open-end effects, compact size, low radiation loss and negligible curvature effects if its diameter is large enough with respect to the line width [119]. Ring resonators are commonly constructed using microstrip lines (MSL). Even though MSL is the most popular planar transmission line, other transmission line such as coplanar waveguide (CPW), coplanar strips (CPS), waveguide, and slotline are alternatives to MSL in microwave and millimeter wave circuits. The CPS, a complementary component to CPW, has all of the advantages of a CPW and is useful in manufacturing lines with high characteristic impedances for resonator with smaller size [73]. The transmission line structures (a) CPS, (b) CPW, and (c) CPW with vias are shown in Figure 6.2.

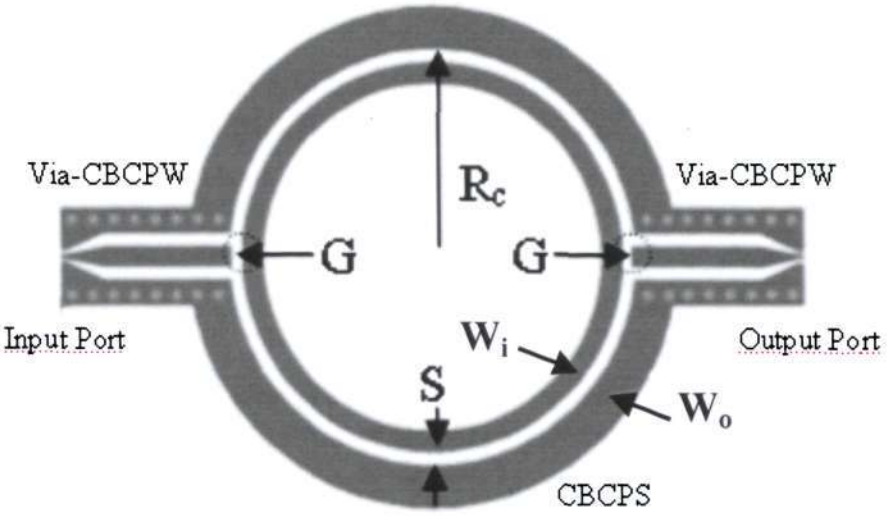


Fig 6.1: Top view of the CBCPW feed CBCPS ring resonator

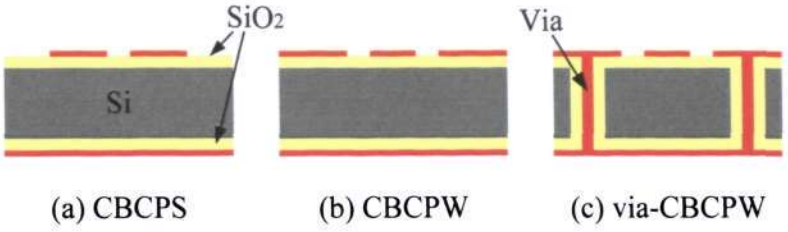


Fig 6.2 Cross section of different transmission lines

The conductor backing leaves the CPW circuit susceptible to leakage of power into surface waves or into the region between conductor plates due to the parasitic parallel plate (PP) mode as demonstrated in Figure 6.3. As shown the designed resonator in Figure 6.1, two ground plates on the topside of CBCPW are connected to the bottom ground plate by metal vias. By introducing these metal vias, the PP mode can be suppressed [117], thus reduce the power leakage in the substrate. Analytical results show that the leaky wave can be controlled by properly choosing the structure of the vias or shorting pins [75].

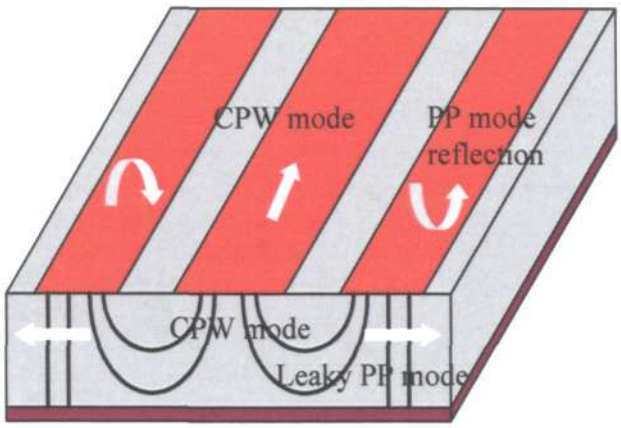


Fig 6.3: Leaky PP mode in a CBCPW structure

Without consideration of the loading effect, the resonant frequency of the CBCPW fed CBCPS ring resonator can be determined by assuming that the structure will support only waves of integral multiple of the wavelength equal to the mean circumference of the ring slot. This is similar to the MSL ring [119] and can be expressed as:

$$2\pi R = n\lambda_g \qquad n = 1,2,3,... \tag{6.1}$$

$$f_n = \frac{nc}{2\pi R\sqrt{\varepsilon_{eff}}} \tag{6.2}$$

where λ_g is the guided wavelength, R is the mean radius of the slot, n is the mode number, f_n is the resonant frequency of the mode n, c is the speed of light in free space, and ε_{eff} is the effective relative dielectric constant and has different values for MSL ring and CBCPS ring.

As shown in Figure 6.1, the via-CBCPW transmission line with 50 Ω characteristic impedance is used in the input and output port. The transition of different physical size via-CBCPW transmission lines with the same characteristic impedance is to meet the requirement of probe test and coupling. The geometries of this resonator are listed in Table 6.1. The mean radius of the slot between the inner and outer ring conductor R_c=1.88 mm, the

width of slot S=0.12 mm, the width of inner ring conductor W_i=0.23 mm, and the width of outer ring conductor W_o=0.4 mm. As shown in Figure 6.4, under the same via-CBCPW fed lines and coupling gaps G=0.06 mm, MSL ring resonator with the mean radius of R_m=1.73 mm and conductor width of W=0.23 mm is compared with CBCPS ring resonator in Figure 6.1. The spectrum characteristics of two resonators are compared in Figure 6.5 by using EM software simulation.

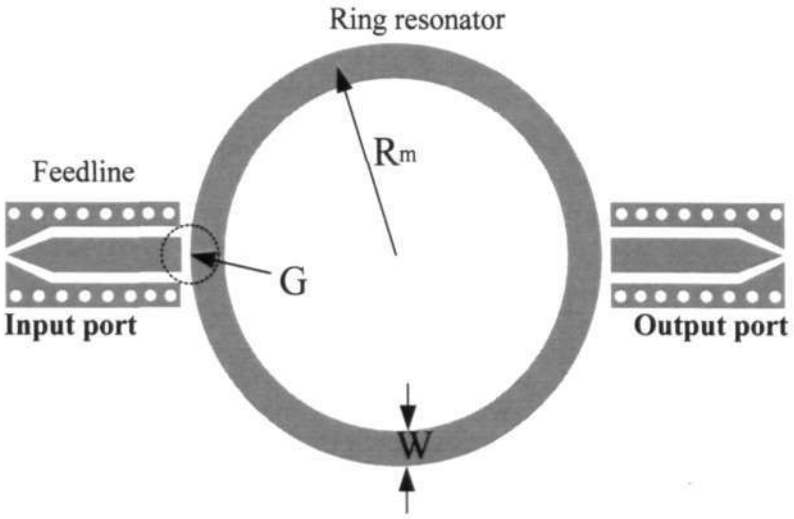


Fig 6.4: The sketch of MSL ring resonator fed by CBCPW lines

Table 6.1: The geometries of the designed CBCPS ring resonator

CBCPS resonator	**R_c**	**S**	**W_i**	**W_o**	**G**
	1.88mm	0.12mm	0.23mm	0.4mm	0.06mm
MSL resonator	**R_m**		**W**		**G**
	1.73mm		0.23mm		0.06mm

The MSL ring: fundamental resonant frequency f_m=9.83 GHz, f_{3dB}=80 MHz, insertion loss 9.8 dB at f_m. The CBCPS ring: fundamental resonant frequency f_c=10.2 GHz, f_{3dB}=75 MHz, insertion loss 10.2 dB at f_c. The loaded Q-factor can be obtained by

$$Q_L = f_r / f_{3dB} \tag{6.3}$$

where f_r is resonant frequency and f_{3dB} is 3-dB bandwidth of the resonator, the Q_L values of the MSL ring and CBCPS are 122.9 and 136, respectively.

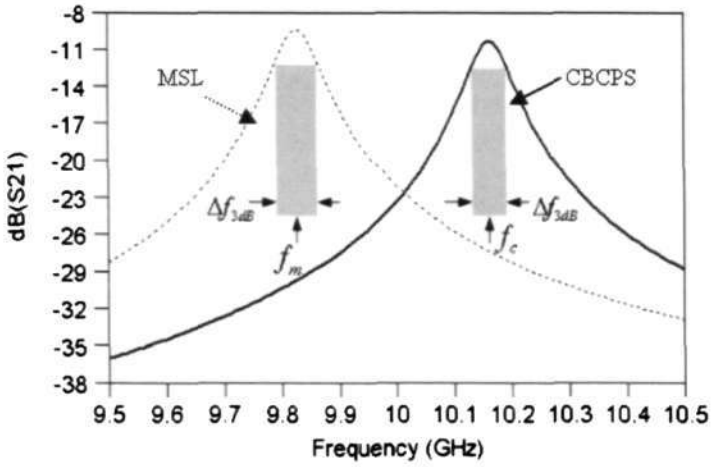


Fig 6.5 Resonant characteristics of the CBCPW feed MSL ring and CBCPS ring

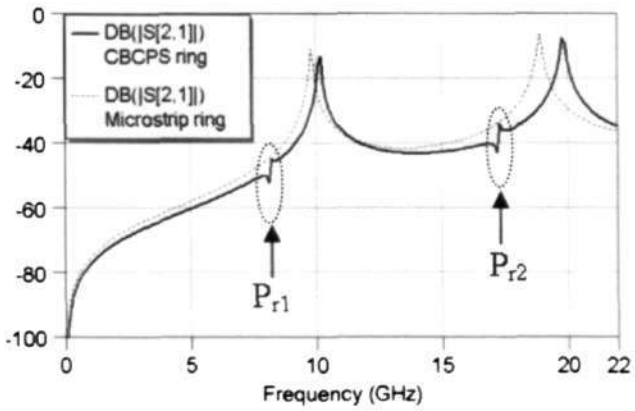


Fig 6.6 Comparison of the CBCPW feed MSL ring and CBCPS ring

The spectrum characteristics from 0~22 GHz of MSL ring and CBCPS ring are demonstrated by EM simulation in Figure 6.6. The second resonant frequencies of MSL ring and CBCPW ring are 18.9 GHz and 19.8 GHz, respectively. The two rings have similar spectrum response, and there exist the weak parasite resonant phenomena in spectrum of the CBCPS ring resonator. The parasitic resonances in 8.15 GHz and 17.3 GHz due to the leakage modes [122] are marked as Pr1 and Pr2, respectively. The leakage power due to PP modes in the CBCPS transmission line re-enters into the CBCPS transmission line of the

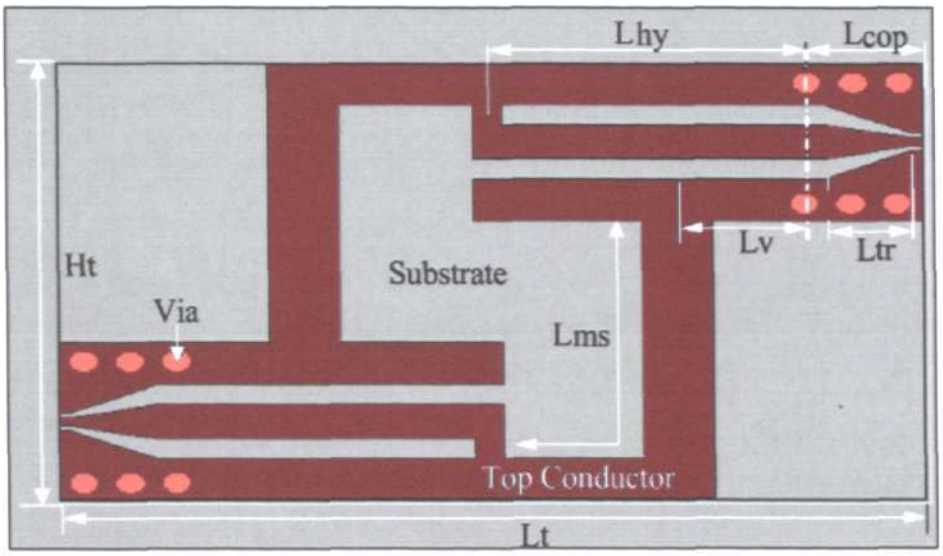
confined CBCPS ring resonator. This leads to the parasitic resonances in the spectrum response. Fortunately, the interference PP modes are very weak.

6.1.2 A Planar Miniaturized High Pass Filter

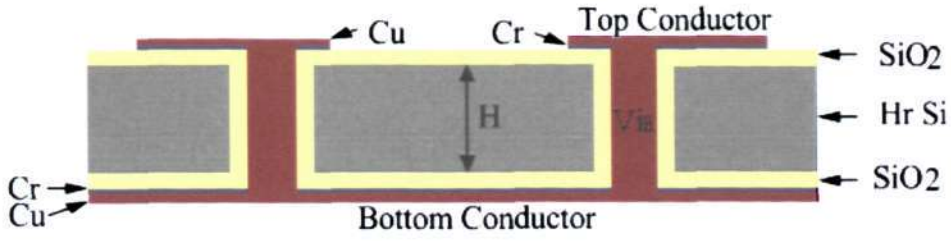
In this subsection, a miniaturized high-pass filter is designed, which are based on the silicon substrate using a conductor backed coplanar waveguide (CBCPW) with via ground (via-CBCPW) cascaded with three coupling microstrip lines (been called Hybrid Coupling Transmission Line or HCTL). The filter design makes use of the transition from the CBCPW to the microstrip line, by which the necessary coupling of the filter is also achieved. Therefore, the smallest size working in the same frequency range can be achieved by omitting the extra length for the transition from CBCPW to the MSL. The via-holes for the CBCPW ground also suppress the PP mode leakage. Due to the mode transition and multi-coupling, the additional zero point and pole point will be generated. Pseudo high-pass filter [119] performance will be improved. Because the zero point in stop band increases the roll off in stop-band near to the pass-band and the additional poles extend the pass-band bandwidth in upper pass-band. The top view of the proposed HCTL high pass filter is shown in Figure 6.7 (a), and the vias are used to connect the top conductor to the bottom conductor. In Figure 6.7 (b), H denotes the thickness of the high resistivity silicon wafer (H=0.5 mm, resistivity is 4000 Ω·cm before fabrication) and SiO_2 layer is thermally oxidized on Si substrate to reduce the substrate losses.

The circuit is composed of three parts: the coplanar waveguide L_{cop}, the hybrid coupling transmission line L_{hy} and the MSL L_{ms}. As shown in Figure 6.7, the via-CBCPW is used in the input and output ports. In this via-CBCPW part circuit, there is a 50 Ω to 50 Ω transition with the length of L_{tr} which realizes the transition from the internal 50 Ω transmission line with the dimension of W_1=0.2 mm and S_1=0.12 mm to 50 Ω transmission line with W_2=0.1

mm and S_2=0.05 mm for the RF-probe measurement (here W_1 and W_2 are center conductor width and S_1 and S_2 are the distances from the center conductor to the side conductor). As listed in Table 6.2, the physical size of the high pass filter is H_t=2.53 mm, L_t=3.7 mm, the radius of vias R_{via}=0.05 mm, L_{hy}=1.36 mm, L_{tr}=0.36 mm, L_v=0.55 mm, the distance between the center of the two adjacent vias on the same side conductor of CBCPW D_{via}=0.2 mm. Compared to the 50 Ω quarter wavelength operating at 12 GHz microstrip line of the length of 2.1 mm with the width about 0.43 mm, the proposed filter has the smallest size compared to the reported structures for the planar microstrip filter under the same substrate condition as well as the similar operating frequency ranges.



(a) Top view



(b) Vertical partial cutting

Fig 6.7: Proposed HCTL high pass filters

Table 6.2: The geometries of the designed high pass filter

H_t	L_t	R_{via}	L_{hy}	L_{tr}	L_v	L_{ms}	D_{via}
2.53mm	3.7mm	0.05mm	1.36mm	0.36mm	0.55mm	2.1mm	0.2mm

6.1.3 Guarded Patch Resonator and Filter with Ground Shunt

Microstrip patch resonators are the interesting design of microstrip filters with the power handling capability [123-124]. Microstrip patch resonators also have lower conductor losses as compared with narrow microstrip resonators.

It is well known that filter performances and sizes are mainly determined by the characteristics of the resonators when the type of filter is determined. In the past, as a fundamental building block for filters, the resonator has been extensively studied [124-129]. Microstrip patch resonators, which have different shapes of triangular, circular, etc, are the interesting design of microstrip filters with high power handling capability. However, the patch resonator filters tend to have stronger radiation loss to the space as well as to the substrate. These radiations are also possible to generate interference to nearby circuits, thus a metal housing is generally needed to minimize the radiation loss and interference [123]. The big limitation for the use of traditional patch resonator is the larger size, which limits its utilization for the high density integrated circuits.

In this subsection, a miniaturized ground ring guided patch resonator and filter, compatible with direct CBCPW feeding structures in I/O ports, is proposed and investigated. The proposed filter shown in Figure 6.8 is realized on silicon wafer by using micromachining technology. The ground ring guarded structure formed by surrounding metal trace with a number of vias connected to the back ground metal, is used to decrease the unexpected PP mode power leakage.

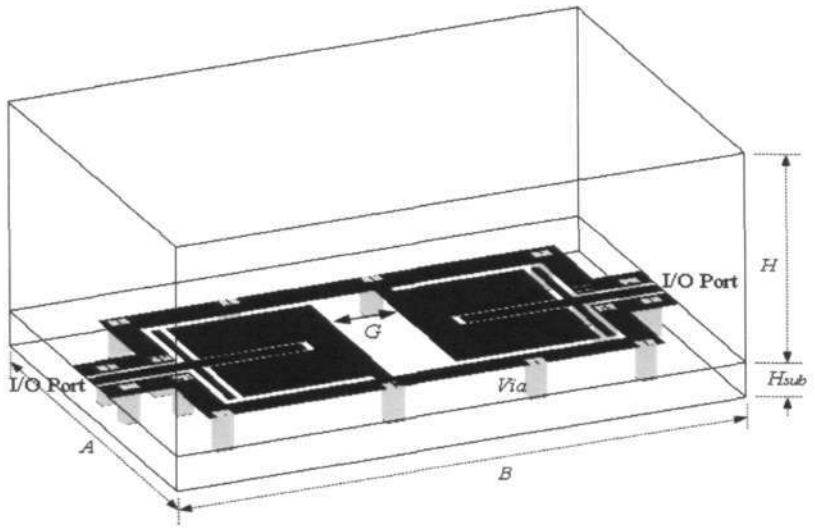


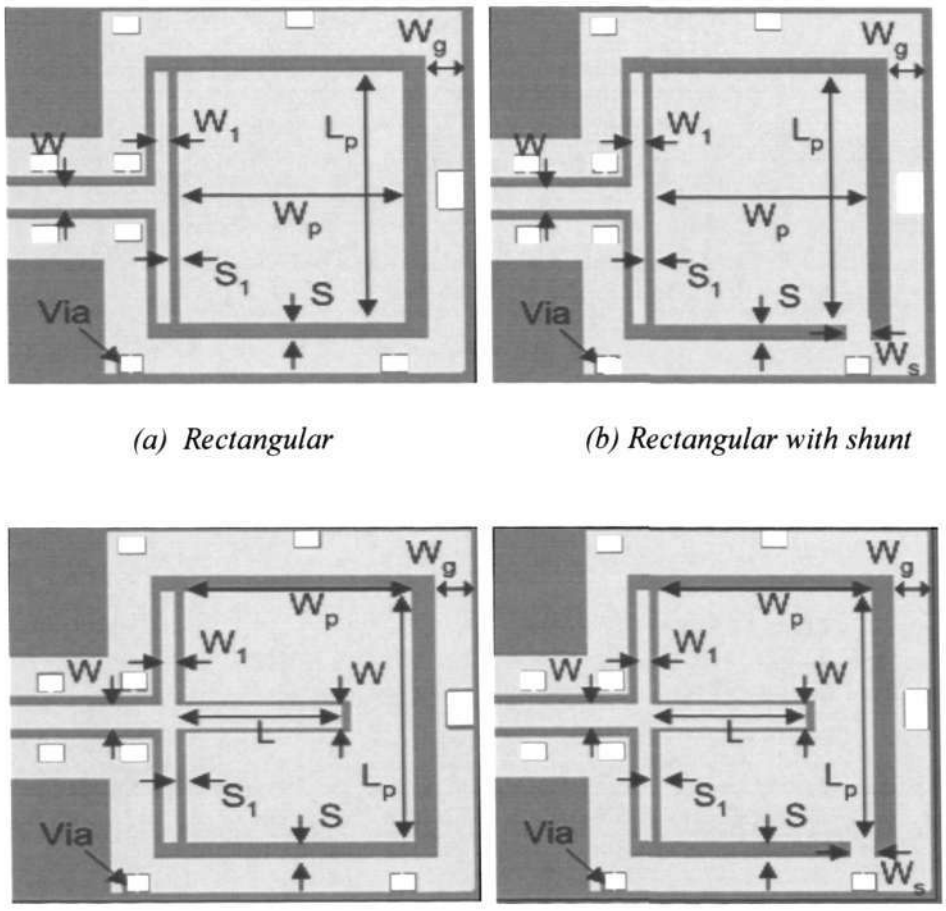
Fig 6.8: Perspective view of the designed patch filter with ground shunt

Four patch resonators which are shown in Figure 6.9 are designed for comparison. The patch resonators with width W_p and length L_p, are surrounded by the metal ground ring which is directly connected with the lateral ground of the input CBCPW transmission line with center strip width W and slot width S_{in}. In Figure 6.9 (a) and (b), a vertical metal trace with width W_1 is connected to the end of the input CBCPW center strip to couple the power between patch resonator and transmission line. A "T" shape feed-in structure is formed. The ground ring can shift up the operating frequency of patch resonator a little with increased via number, by changing the fringing field at the edge of the patch resonator. The resonant frequency for mnth mode can be obtained using the following formula:

$$f_{mn} = \frac{c}{2\pi\sqrt{\varepsilon_{dyn}}}\sqrt{\left(\frac{m\pi}{L_{eff}}\right)^2 + \left(\frac{n\pi}{W_{eff}}\right)^2} \tag{6.4}$$

where ε_{dyn} is the dynamic permittivity of patch defined in [130] and c is the speed of the light in free space, L_{eff} and W_{eff} are effective width and length, respectively [131]. The ground ring guarded patch resonator with ground shunt is shown in Figure 6.9 (b). Compared

with the structure in Figure 6.9 (a), the difference in Figure 6.9 (b) is that a ground shunt with width *Ws* connects the patch to the ground ring. In Figure 6.9 (c) and (d), the patches are changed as "U" shape with and without shunt respectively, and the center strip of the CBCPW feed line is extended with length of *L* to increase coupling effects.



(a) Rectangular *(b) Rectangular with shunt*

(c) "U" shape *(d) "U" shape with shunt*

Fig 6.9: Ground ring guarded resonators with different patch shapes

The frequency response characteristics of the structures have been simulated using HFSS software and presented in Figure 6.9. The fundamental mode resonant frequencies in Figure 6.9 (a) are 20.7 GHz (m=1, n=0) and 21.3 GHz (m=0, n=1), respectively, while the fundamental mode resonant frequencies of Figure 6.9 (b) are 5.9 GHz and 18.9 GHz, respectively. Obviously, for the same dimensions, the lowest resonant frequency of the

ground ring shunted resonator in Figure 6.9 (b) is only about 30% of the resonator without ground shunt. For the "U" shape resonators in figure 6.9 (c) and (d), the similar frequency ratio of the lowest operating frequencies, which are 18.7 GHz and 5.5 GHz, respectively, exists. These results clearly show that for the same operating frequency the ground shunt can contribute to a size reduction of more than three times compared to the patch resonator without ground shunt.

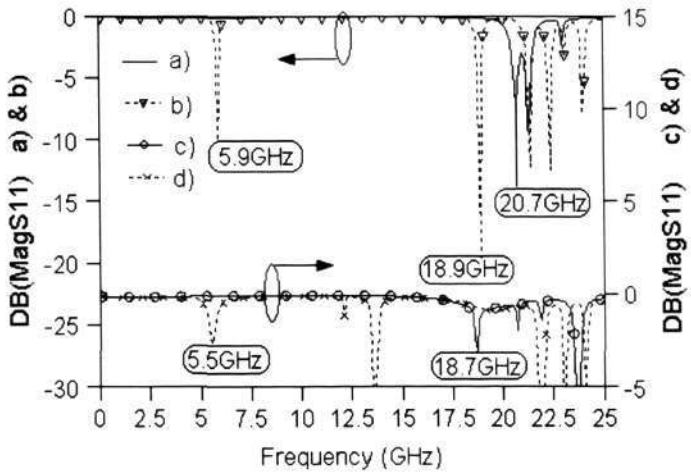


Fig 6.10: The frequency response of the resonators with geometries: W_l=50um, W_p=2mm, L_p=2.28mm, W_s=0.2mm, S=0.15mm, W_l=0.1mm, S_l=0.1mm, W_g=0.3mm, L=1.8mm, W=0.2mm, and S_{in}=0.12mm

As shown in Figure 6.8, the I/O ports coupling is mainly determined by the line width W_l and coupling gap S_l, while the extended feed line with length L and width W can further increase the coupling. The inter-stage coupling is mainly determined by the gap width G between two patch resonators. Since we mainly focus on the ground ring guided patch filter characteristics with/without ground shunt, the design procedure in [123] is adopted and not detailed here. As shown in Figure 6.8 with geometries A=5 mm, B=7.9 mm, H=5 mm, S_l=0.05 mm, and G=1 mm, two filters constructed by Figure 6.9 (a) and (b) resonators are simulated using HFSS software. The frequency response characteristics of the two-pole

filters are shown in Figure 6.11. The resonant frequencies of filters with and without ground shunt, as denoted by arrows, are 5.5 GHz and 20.5 GHz, respectively. The filter with shunt also has wider rejection band width and deeper rolloff.

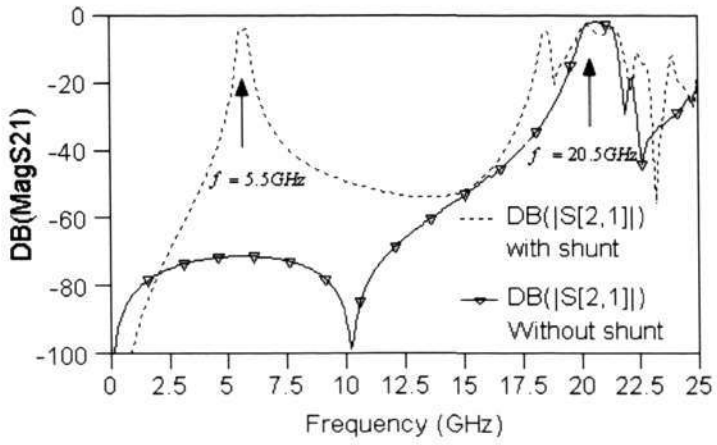


Fig 6.11: Simulation of frequency response for two-pole filters with and without ground shunt.

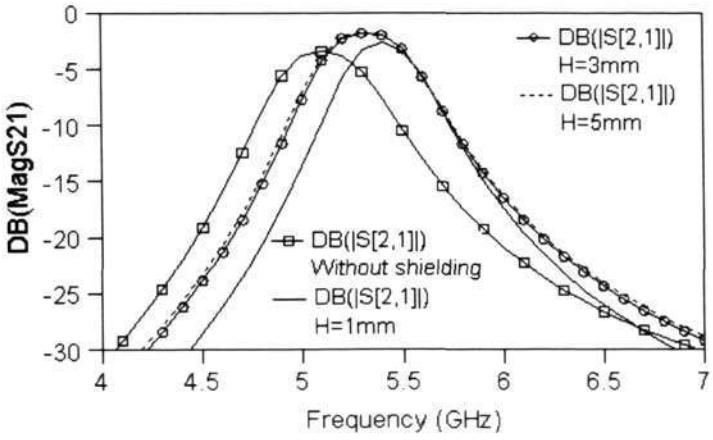


Fig 6.12: Shielding effect of the guarded patch filter with ground shunt

By using the four types of patch resonators, four two-pole patch band pass filters can be constructed. Since the architecture of these filters is similar, only the filter built by the patch resonators shown in Figure 6.9 (d) is demonstrated. The filter shown in Figure 6.8, with 11% relative bandwidth, is designed and the shielding effect of metal housing height H is

investigated by simulation. As shown in Figure 6.12, without metal housing, the insertion loss is 3.4 dB, which is much larger than that with metal housing 1.7 dB, while the housing height H=3 mm. When H is below 3 mm (six times of the substrate height H_{sub}=0.5 mm), the decreased height H can shift the operating frequency up. When H is larger than 3 mm, the increased height H almost has no effect on the frequency response.

6.2 Fabrication of RF Resonators and Filters

The manufacture of these designed devices is completed in our Micromachines Center. The whole processes are handled by myself and new fabrication techniques are developed during fabrication of these devices. The details are described in the following.

6.2.1 Fabrication Processes

The fabrication processes are shown in Figure 6.13. Firstly, a high resistivity silicon wafer is cleaned in piranha solution. The resistivity of the wafer is 4000 Ω·cm. Such high resistivity wafer is chosen to reduce the substrate losses for the devices operating in high frequency range. Step 2 is to deposit photoresist mask and make holes pattern. The patterned wafer is etched through by DRIE, shown in step 3. The etched through holes is used to form vias connected the top ground to bottom ground in the later process. Step 4 is to remove the remained resist mask and the wafer must be clean before put it into furnace. The wafer is cleaned using acetone in ultrasonic bath for 5 minutes. Step 5 is to oxidize the wafer with etched through holes in furnace. The purpose of oxide layer in the wafer surfaces and sidewall of the through holes is to isolated metal material deposited later with the silicon substrate. In order to plate Cu into the through holes, another wafer is prepared to provide the plating seed layer. As shown in step 7, the wafer is sputtered with Au. As shown in step 8 and 9, a thin layer resist is spun on top of the sputtered wafer and the etched wafer attached

with the sputtered wafer together by the photoresist. After hard bake the attached wafers, the step 10 is to etch away the bottom resist under the holes using RIE.

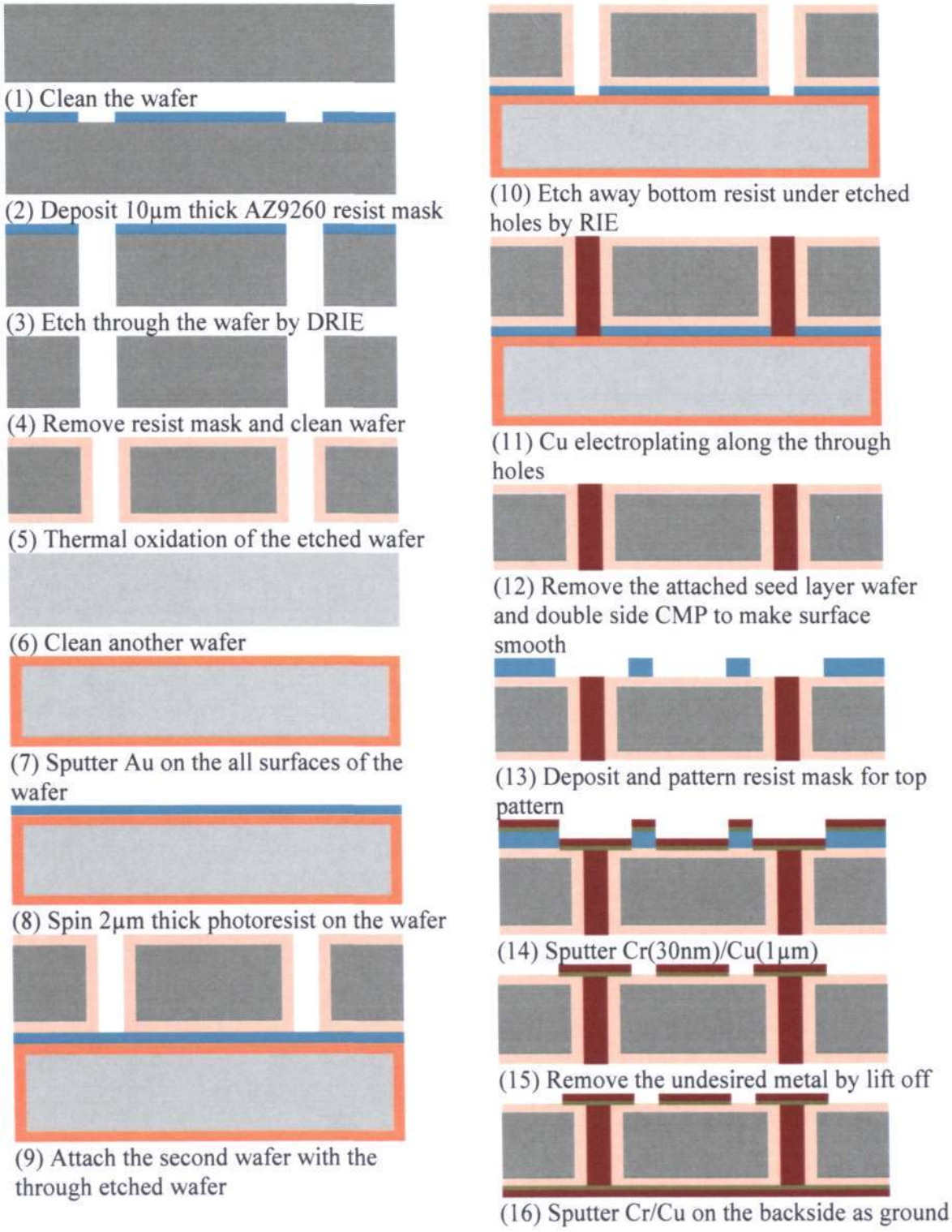


Fig 6.13: Fabrication processes of RF resonators and filters

This way can provide very good seed layer with flat surface and void-free at the attached surface, which is very important for electroplating. Step 11 is to plate Cu in the etched through holes using bottom-up electroplating technology. This is a challenging work to plate Cu through a whole wafer. The details of electroplating techniques are described in next subsection. After electroplating, the attached wafers are separated by dissolve the inter resist layer using acetone in ultrasonic bath. Double sided CMP is performed to make the surfaces of plated wafer smooth, which is shown in step 12. The resonator and filter patterns and deposition of top metal layer are made in step 13 and 14. The Cu layer of 1 μm is deposited using sputtering. A 30nm Cr layer is also deposited to increase the adhesion of Cu metal with substrate. The filters and resonators are formed by lift off the undesired metal materials. Finally, the back side ground is sputtered using Cr/Cu.

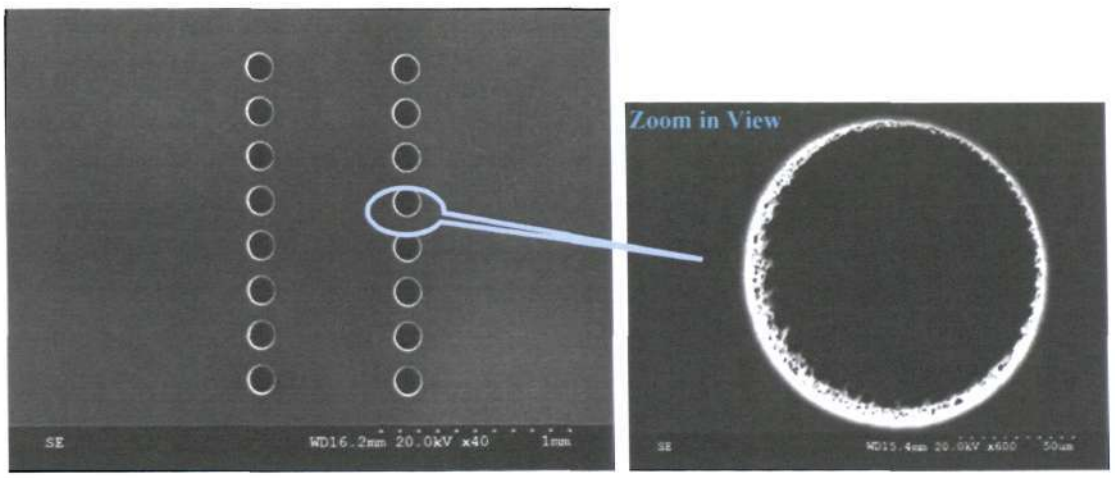


Fig 6.14: Etched through holes using DRIE

Figure 6.14 is the SEM photos of etched through holes. The thickness of the wafer is 500 μm, and the diameter of the holes 100 μm. It takes about two hours to etch through this wafer. Such long time brings obvious undercut and rough sidewall at the entrance of the hole that can be seen as the zoom in view. The roughness of sidewall can be improved after thermal

oxidation. Figure 6.15 is the SEM photo of the etched hole after thermal oxidation. The thin oxide layer on surface of one sample is stripped in order to take the clear sidewall picture. The cracks in the photo are caused during strip surface oxide. This oxide layer isolates the plated Cu from silicon substrate to reduce the substrate losses.

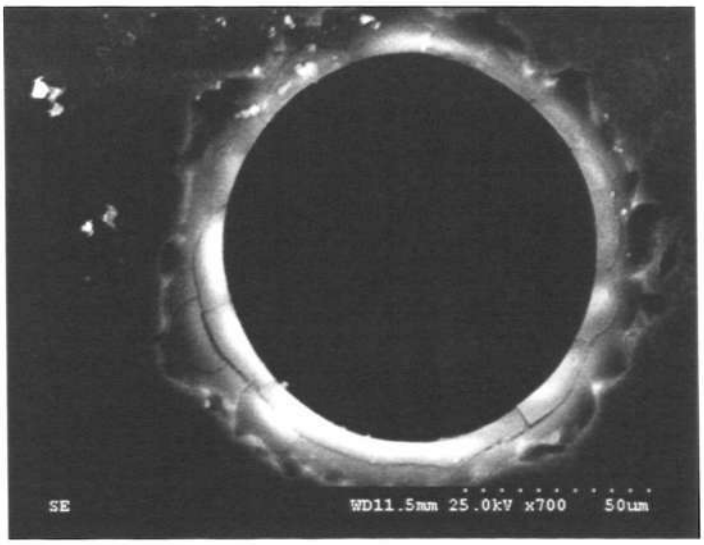


Fig 6.15: Etched hole after thermal oxidation

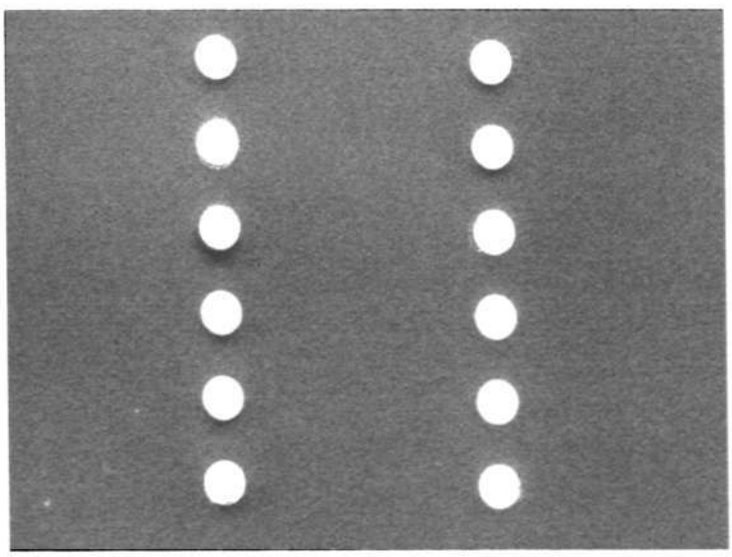


Fig 6.16: Electroplated Cu vias along the etched through holes

Figure 6.16 shows the electroplated holes. The holes are filled fully by the plated Cu. Chemical Mechanical Polish (CMP) should be used to make the surfaces smooth. The details of electroplating technology for the through holes will be introduced in the next subsection.

Figure 6.17 shows a SEM photo of the fabricated HCTL high pass filter. The top metal transmission lines are completed by sputtering and lift-off process.

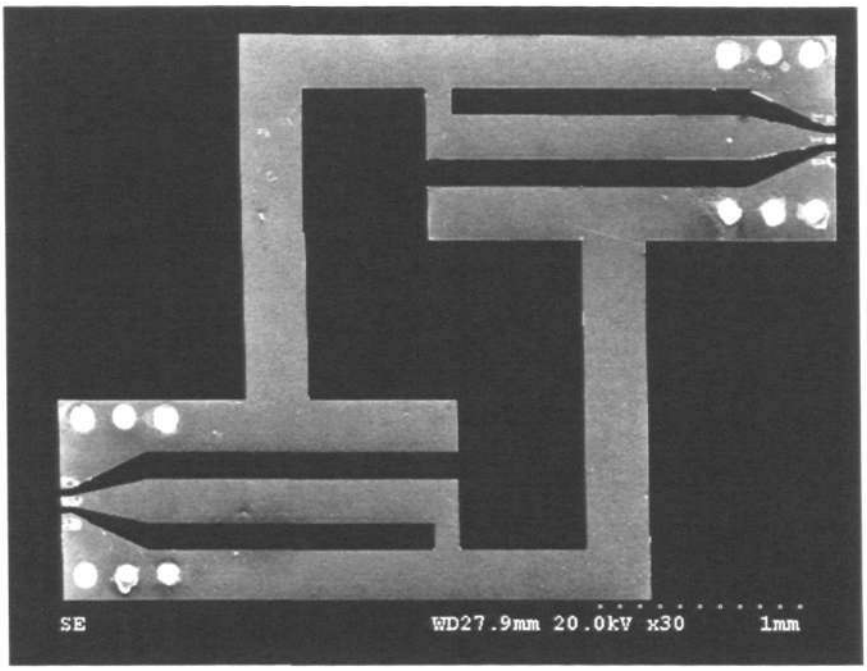


Fig 6.17: SEM photo of the fabricated HCTL high pass filter

6.2.2 Electroplating

Although copper electroplating is a well-established process and its principles have been well known for decades, void-free filling in deep through-holes is still a challenging work. The big trouble for the through wafer electroplating is the uneven local current density distribution inside the through holes so that the current density does not remain uniform along the depth during electroplating. A new electroplating process so called aspect-ratio-dependent copper electroplating has been investigated in Micromachines Center, NTU [132].

The electroplating experiments are carried out in a home-made electroplating system and the schematic of this system is shown in Figure 6.18.

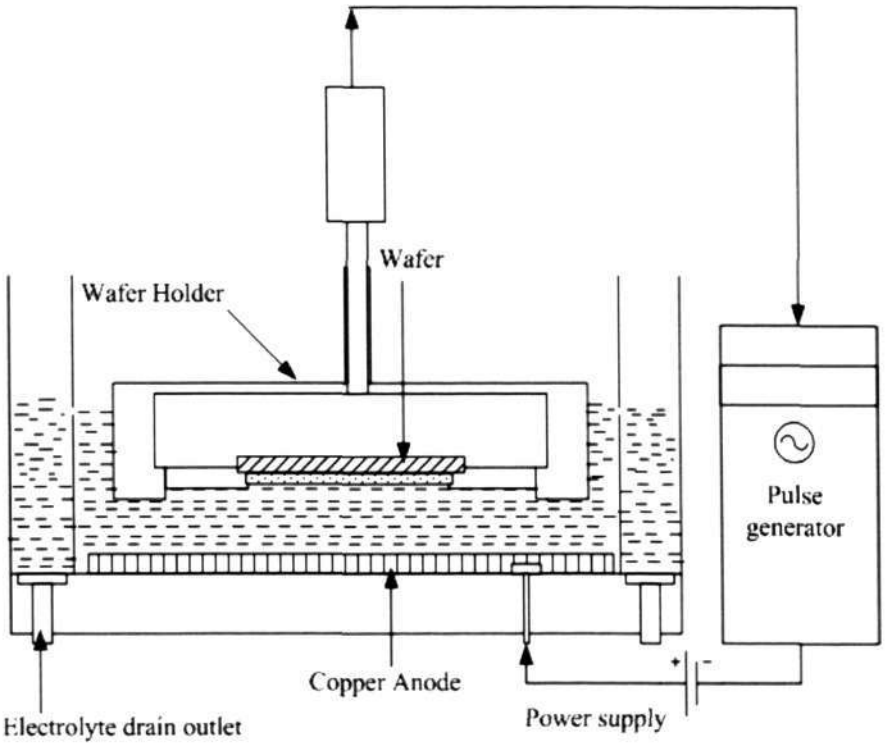


Fig 6.18: The schematic of electroplating system

Table 6.3: Electrolyte composition and operating conditions

Electrolyte Composition	
Copper Sulphate (g/l)	40
Sulphuric Acid (g/l)	150
Chroride Ion (mg/l)	50
Brightener (ml/l)	10
Leveler (ml/l)	15
Operating Conditions	
Temperature (°C)	28
PH value	1
Current Density ($mA/cm^{2)}$	10-60
Plating Mode	Pulse plating

The anode of the power generator connects to the Cu plate, and the cathode connects to the wafer sample through a wafer holder. The acid electrolyte for copper plating contains copper sulfate, sulfuric acid, hydrochloric acid, and organic additives including brightener and leveler, which is listed in Table 6.3.

In the electroplating process, current density is the most important parameter which can significantly influence the plated result. The effect of current density on Cu electroplating has been explored as shown in Figure 6.19. The grain size increases as the current density goes up during electroplating. The quality of the growing layer is determined by three factors: the rate of electrons transfer to form the adatoms, diffusion of the adatoms across the surface into the lattice position, and the current density [133]. At low current density, surface diffusion will be fast compared with electron transfer so the newly deposited atom is likely to end up in a favored position in its characteristic lattice structure. At higher current density, adatoms are formed so fast compared with their rates of surface diffusion that many newly depositing atoms cannot diffuse to a favorable lattice site because their motion is impeded by other depositing atoms, resulting in rougher surface or less ordered layers. When the current density increases higher enough, the metal ions cannot be supplied fast enough at such high current density so that only part of the supplied ions goes to metal discharge while the rest goes to hydrogen evolution. This will result in the deposition of Cu material become dark and powdery. It is clear that the surface morphology severely degrades with increasing current density. The grown grains become much bigger when current density increases from 10 mA/cm^2 to 50 mA/cm^2. The current density in our work varies from 10 mA/cm^2 to 30 mA/cm^2 during pulse plating.

In the process of DC electroplating, the concentration of the metal ions in the region of the solution close to the cathode is less than the value in the bulk solution. The depletion of the

metal ions occurs at the cathode as shown in Figure 6.20. The concentration of the metal ions in the bath is designated as C_b, the concentration of the ions at the surface is C_s, and δ represents the effective diffusion layer thickness. To improve the depletion of metal ions concentration near the cathode, a reverse plating short time and high current density, that is, pulse plating, is adopted in this work.

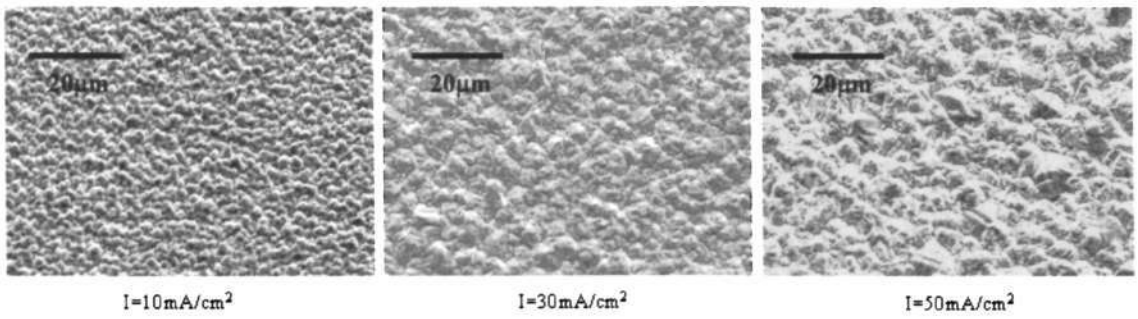


Fig 6.19: The effect of current density on morphology of copper electroplating

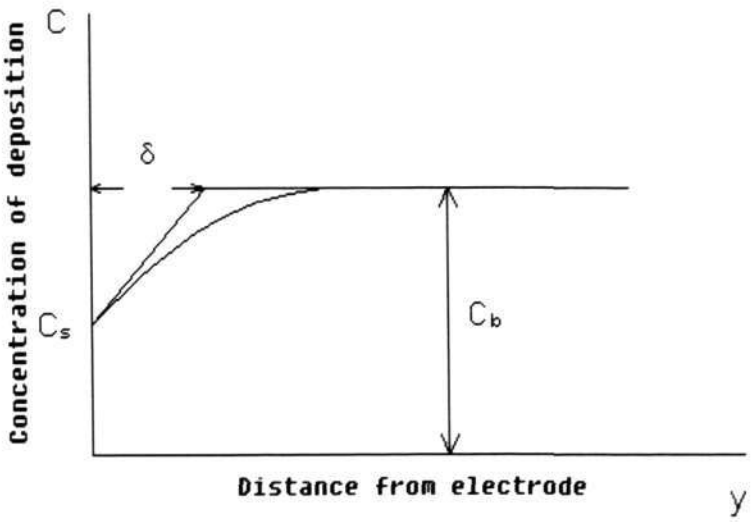


Fig 6.20: The schematic of metal ion concentration near a cathode during electroplating

In this work, an aspect-ratio-dependent pulse electroplating is presented, which means the pulse current varies with the change of aspect ratio of the holes. As shown in Figure 6.21, the high aspect ratio of the hole becomes smaller and smaller because the unfilled depth of

through-hole (H-h) decreases during electroplating. At the beginning of electroplating, the current density should be as small as possible because the electrolyte in the bottom of the hole is difficult to refresh. As the unfilled depth is continuously reducing, electrolyte kinetics and cupric ion mass transfer increase. As a result, the current density should increase.

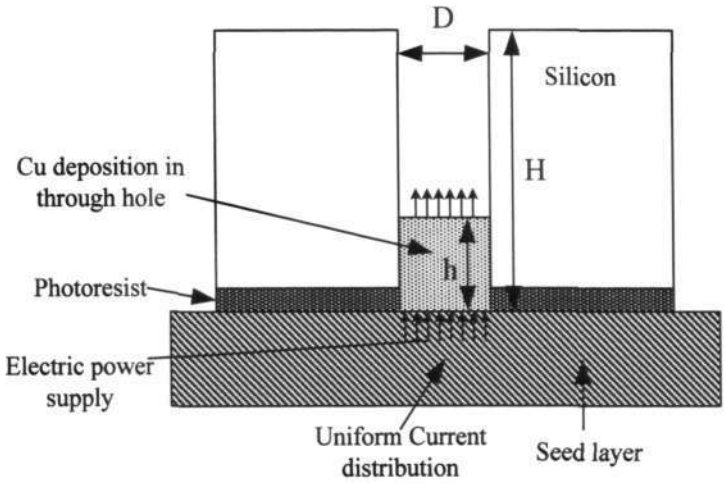


Fig 6.21: Varied aspect ratio of the through hole during electroplating

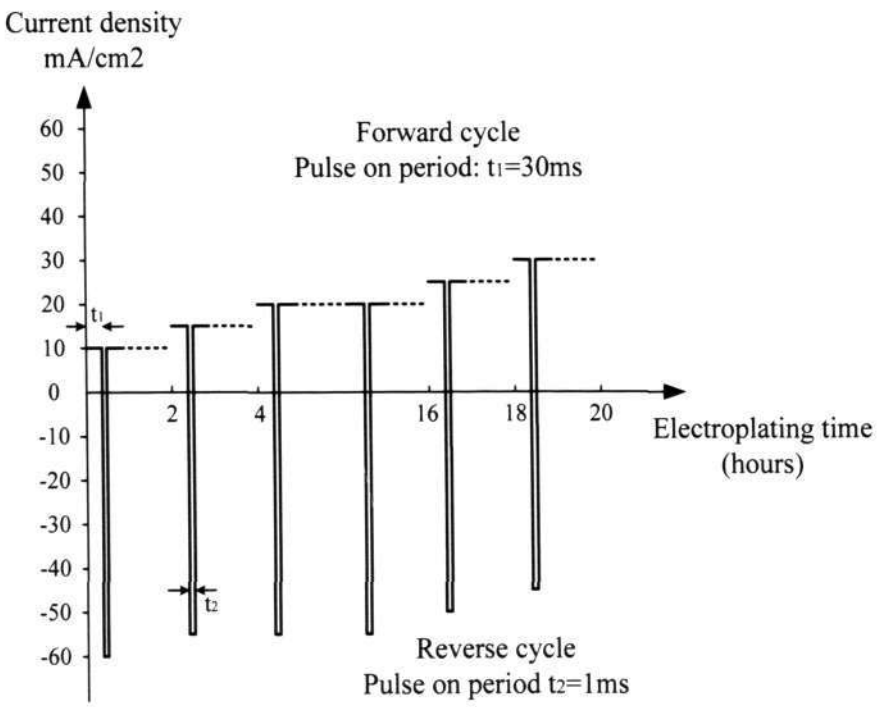
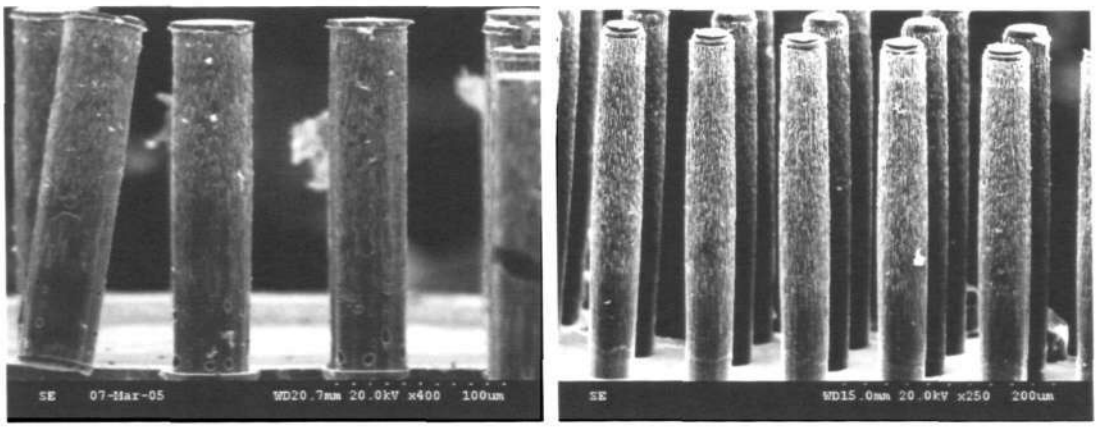


Fig 6.22: Varied current density for the aspect-ratio-dependent electroplating

Figure 6.22 shows the setting of current density varying with electroplating time. Forward current density varies from 10 mA/cm^2 to 30 mA/cm^2, while reverse current density varies from 40 mA/cm^2 to 60 mA/cm^2. The total plating time is 20 hours for 500 μm thick copper pillars. The average plating rate is around 0.4 μm/min.

Figure 6.23 shows the plated Cu pillars through a 200 μm thick wafer and a 350 μm thick wafer using this developed plating technique. The etched through wafers are completely dissolved in KOH solution.



(a) 200 μm Cu pillars *(b) 350 μm Cu pillars*

Fig 6.23: SEM photo of Cu pillars by aspect-ratio-dependent electroplating

6.3 Measured Results and Discussions

The measurement of the fabricated resonators and filters was carried out using network analyzer HP8510B. The S parameters with frequency range from 100MHz to 25 GHz are obtained directly from the network analyzer.

6.3.1 Measured Results of CBCPW-Fed-CBCPS Ring Resonator

Figure 6.24 illustrate the characteristic of a section via-CBCPW line with longitude length of 5.85 mm and transverse size is the same as the ring feed line , one can see no pp mode is

excited, on the other hand, the total transmission loss of $(1-|S_{11}|^2-|S_{21}|^2)$ due to the radiation, substrate and metal can be obtained.

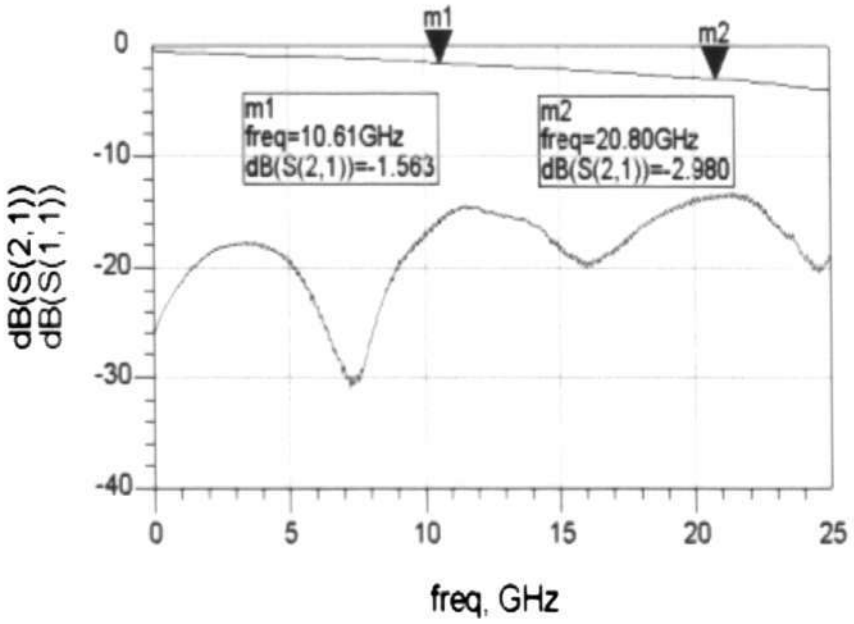


Fig 6.24: Measured spectrum response of Via-CBCPW

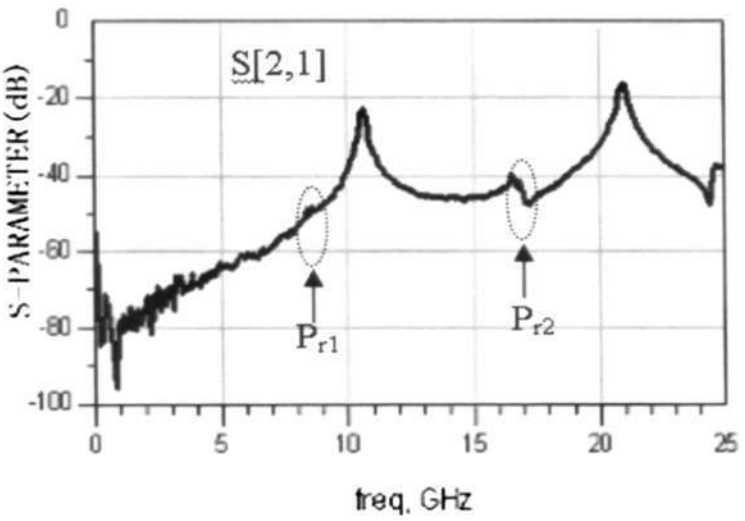


Fig 6.25: Measured spectrum response of CBCPS ring

In Figure 6.25, the minimum insertion loss is -23.2 dB, and the measured resonant frequency f_c and f_{3dB} of the CBCPS ring are 10.62 GHz and 220 MHz respectively, the measured Q_L is about 48.3 by using equation (6.3) and the measured unloaded Q of the resonator can be obtained by

$$Q_{u,measure} = \frac{Q_{L,measure}}{1-10^{-L_{measure}/20}} \tag{6.5}$$

where $Q_{L,measure}$ is measured loaded quality factor, L_{measue} the measured insertion loss in decibels of the resonator at resonant frequency.

The measured unloading Q-factor of the resonator is 53.5. The unloading Q-factor of the n=2 resonant mode is 45 using the same method as n=1. The resonant frequency is shifted to higher frequency side by 4.1% because the thin SiO_2 layers with low permittivity (about 4) decrease ε_{eff}, and then increase the resonant frequency. The higher insertion loss of test results compared with that of simulation results is mainly due to the fabrication in the thickness of top conductor (measured sheet resisitivity is 0.078 Ω/□), because the thin thickness of sputtering conductor reduces the coupling coefficient between the fed-CBCPW line and the CBCPS ring and leads to more metal loss in the lower operating frequency range (the skin depth of copper is 0.66 μΩ·cm at 10 GHz). The degradation of the resistivity of the silicon during fabrication as mentioned in [120] also increases the measured loss.

6.3.2 Measured Results of Miniaturized HCTL High Pass Filter

Figure 6.26 shows the simulated result of the HCTL high pass filter. The chosen lengths of L_{ms} causes four poles (two are at 12 GHz and other two are at about 22 GHz) in the pass band and one zero (at about 11 GHz) in the low stop band. The on-wafer probe-tip measure system is used.

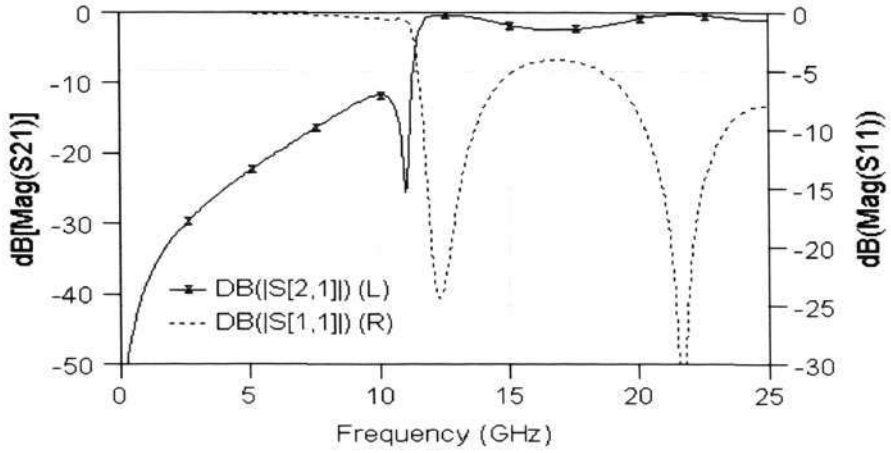


Fig 6.26: Simulation results of the HCTL high pass filter

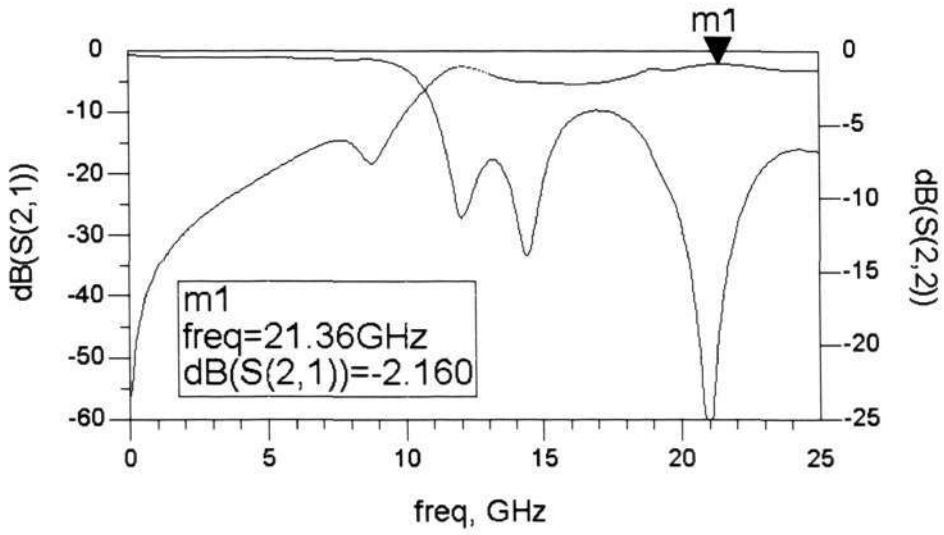


Fig 6.27: Measured results of the HCTL high pass filter

The measured results are shown in Figure 6.27, the simulation results and the test results are agreed well in the trend and the number of the zero and poles. The shift of the simulation results from the test results is partially due to the fabrication in the thickness of top conductor, because the thin sputtering conductor thickness reduces the coupling between the HCTL and lead to more metal loss in the low operating frequency range. The higher measured loss is due to the degradation of the resistivity of the silicon as explained in [134] and the conductor loss.

6.3.3 Measurement Results of Guarded Patch Filter with Ground Shunt

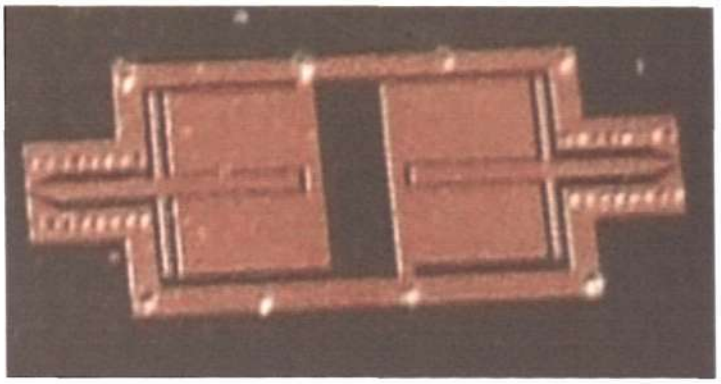


Fig 6.28: Fabricated guarded patch filter with size 8.7 mm X 2.9 mm

Figure 6.28 shows the fabricated guarded patch filter. The filter size is 8.7mm X 2.9mm. The measurement results and the theory results of this filter are compared in Figure 6.29 and Figure 6.30. The experiment results shown in Figure 6.29 are in good agreement with the simulation results.

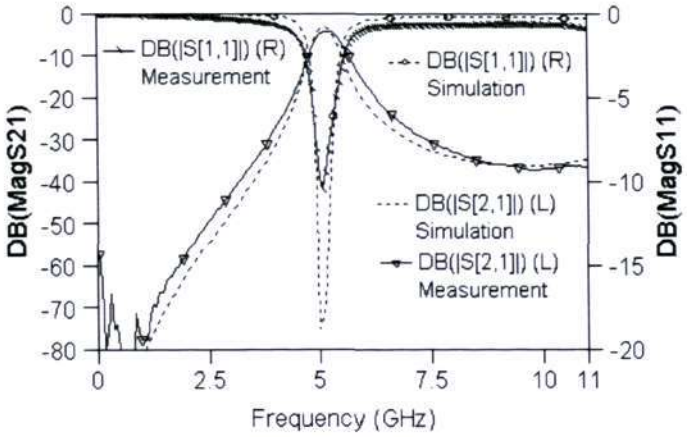


Fig 6.29: The simulation and experiment results of the fabricated filter

The simulated and measured loss factor ($1-|S_{11}|^2-|S_{21}|^2$) of the filter are compared in Figure 6.30. The filter losses are composed of substrate loss, metal loss as well as the radiation loss. Since the wafer is measured without metal housing, the radiation loss is about 3.4 dB in pass band compared to the 1.7 dB radiation loss with metal housing effects, as demonstrated in

Figure 6.12. That means if the filter is properly shielded with metal housing, the measured insertion loss can be reduced to about 2.5 dB from the measured 4.2 dB shown in Figure 6.29.

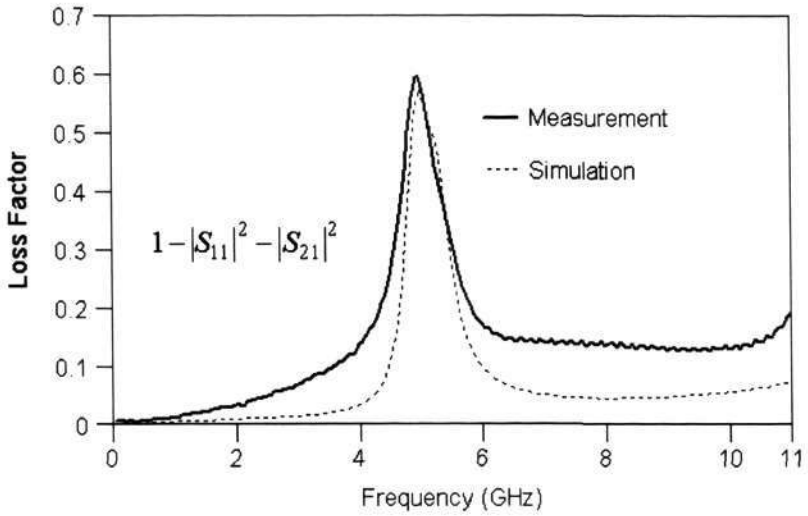


Fig 6.30: The simulation and experiment loss factor of the filter

6.4 Summary

The designs of novel passive resonators and filters of CBCPW-fed-CBCPS ring resonator, High-pass filter, and patch filter are explored in this chapter. Simulations using HFSS software show the designed devices have outstanding performances with small feature sizes. New MEMS fabrication processes are developed and carried out on these designs. Measurement results are analyzed and discussed at end of this chapter.

Chapter 7

Conclusion

This thesis has investigated the novel fabrication technology so-called SiDeox for creating thick silicon dioxide blocks for the development of low-loss RF inductors, the design and EM simulation of spiral inductors, the fabrication processes and measurement of the designed inductors, the novel designs and fabrication of RF passive resonators and filters. To conclude the project, major contributions summarized and further research considerations are identified in this chapter.

7.1 Contributions

In order to develop RF MEMS devices for radio frequency integrated circuits, the following research work has been done and relevant conclusions and results have been achieved.

- Optimized isotropic DRIE (deep reactive ion etch) process has been studied with adjustments of its process parameters to achieve vertical etch profile based on silicon substrate. By tuning the platen power to increase the etching plasma at trench bottom, the v-shape profile during DRIE is eliminated to obtain high-aspect-ratio deep trench with 1.5 μm DICD (development inspect critical dimension). The aspect ratio can achieve as high as above 30.

- Traditional DRIE structure with bottom lateral release so-called multi-step release process is explored to obtain floating DRIE structure. By separating the alternate

passivation and etching steps after traditional DRIE process, the sidewalls of trenches are passivated with a layer of polymer, then etched by high energetic plasma and isotropic etching plasma. The multi-step release process is a unique technology to make an air gap beneath DRIE structure.

- Controllable wet oxidation process is investigated to refill the deep etched trenches. By oxidizing the silicon structure after DRIE in lateral direction, the gaps are refilled gradually to obtain silicon structures with higher aspect ratio and thick silicon oxide blocks. The so-called nano trenches with large depths, which can not be achieved using DRIE technology, are obtained. By dissolving the oxide layer in the deep etched silicon structures, nano silicon beams are realized. These fabrication technologies have the potential applications for nano molding and nano needles.

- Thick silicon oxide blocks using SiDeox (silicon DRIE and oxidation) technology have been fabricated with the proper design of mask dimension. Compared to normal oxide thickness limited to 2 μm, the fabricated oxide layer by SiDeox has several tens micro meter without any void. By creating such thick oxide blocks in silicon substrate, RF inductors with high performance can be accomplished for RFICs.

- To understand the RF inductor, the layout, loss mechanisms, and factors of merit involving quality factor, self-resonant frequency, and inductance, are discussed in detail. The spiral layout is selected for RF inductor design because it is easy to be integrated into RFICs compared to solenoid structure. The losses for spiral RF inductors built on silicon substrate come from the parasitic substrate losses and metal resistance losses. The quality factor for an inductor is defined as the imaginary part of input resistance divided by real part of input resistance. It is not accurate near the self-resonant frequency because of the effect of significant parasitic capacitance.

Therefore, the definition of quality factor for the inductors is a problem to be corrected in future study. The inductance of spiral inductors includes the self inductance and mutual inductance of the spiral windings, which is calculated using Green House method.

- The electric modeling technology for RF spiral inductors is studied to understand the work performance. Two coupled unit metal lines generate the components including unit self inductance, unit series resistance, unit mutual inductance, fringing coupled capacitance, parasitic oxide capacitance, parasitic silicon resistance and capacitance. By expending the unit model concept to a whole turn inductor, the segmented inductor model has been obtained. However, this segmented model shows a complicate construction, which is inefficient for evaluating inductor performance. Lumped inductor model, which is created by summing up the series and shunt components in the segmented model, presents the advantages of simple structure and easy analysis for inductor development. But new model still need to be developed for spiral inductor with large line length.

- The effects of inductor geometries including surrounding, line width, line space, substrate reristivity, and oxide thickness, are investigated in detail using simulator HFSS to get a proper design for fabrication. The simulation results show that the oxide thickness has dramatically influenced the RF inductor performance. By increasing the thickness of oxide layer, both the quality factor and self-resonant frequency are greatly enhanced.

- The fabrication processes of RF spiral inductors using SiDeox technology have been carried out in this work. The de-embedded measurement technique is presented for the fabricated inductors. The component values in the equivalent circuit are extracted

from measured results using GA method. The inductors fabricated both on 20 μm oxide block and on 2 μm oxide layer are compared. The results show that the measurement and simulation are in good agreement and the performances have been much improved on the thicker oxide block.

- Novel RF resonators and filters, which are CBCPW-Fed-CBCPS ring resonator, HCTL high-pass filter, patched resonator and filter with shunt ground, are designed in this work. To suppress the PP mode leakage in the CBCPW structure, through-wafer vias are adopted to connect top surroundings with bottom ground.

- The fabrication processes for the designed RF passive resonators and filters have been carried out. To form the through-wafer vias, high-aspect-ratio electroplating technique is developed. The aspect-ratio dependent electroplating technology can refill the through-holes with satisfaction of requirement.

- The fabricated resonators and filters have been measured with good agreement to the simulation results. These devices have good performances and small sizes, which are in fulfillment of design expects.

7.2 Future Considerations

This section identifies topics covered in this thesis which merit further study in the future.

- DRIE process still requires further optimization for fabricating silicon structure with larger high-aspect-ratio compared to the current high-aspect-ratio of around 32. The larger the high-aspect-ratio, the thicker the silicon dioxide block can be formed.

- Currently, the development of RF inductor is just focused on the removal of substrate losses by MEMS technology. Another important aspect in the design of RF inductors is metal resistance, which normally need 3 μm to overcome skin effects in few GHz range of operation frequency. The fabricated inductors with 1μm thick metal significantly surfer from the skin effects limited their performance. Copper electroplating is essential to be adopted to build thicker metal traces in order to reduce the metal resistance.

- When the designed inductor with a total line length beyond λ/10 (λ wavelength) at the operation frequency, the single lumped π model is not efficient any more because of the distribution effects along the metal line. Therefore, new modeling technique is required for large inductor.

- The developed inductors, resonators and filters, are on the individual device level. In fact, these devices are commonly used in RFICs. Accordingly, to realize the integration of these devices on a system deserves more studies in future.

Appendix A

The Inductance of Spiral Inductors

For the simplest case, only line filaments, which are shown in Figure A.1, the mutual inductance can be evaluated using the Neumann double integral:

$$M = \frac{\mu}{4\pi} \oint\oint \frac{1}{R} d\boldsymbol{I}_1 \bullet d\boldsymbol{I}_2 \qquad \text{(A.1)}$$

where $d\boldsymbol{I}_1$ and $d\boldsymbol{I}_2$ are the vector current elements and R is the distance between the elements.

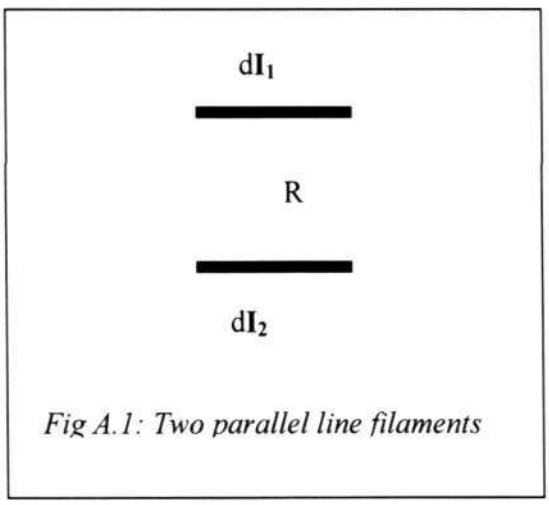


Fig A.1: Two parallel line filaments

Thus the mutual inductance is proportional to the inner product of the vector current elements and is inversely proportional to the distance between them. The vector dot product quantifies the well-known observation that the mutual inductance between two elements is a maximum when the current elements are parallel to one another and the current flow is in the same direction. When the current flow is in opposite directions, the mutual inductance is a

minimum (negative). When the current elements are in orthogonal directions, the mutual inductance is zero.

1. Parallel Line Filaments

When two parallel lines are unequal in length as shown in Figure A.2 and positioned so that a line through their centers is orthogonal to the two lines, we can get the closed form solution by solving equation (A.1).

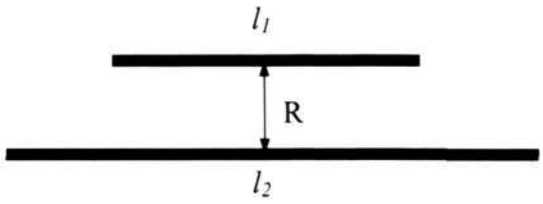


Fig A.2: Two unequal lines

The expression for the mutual inductance evaluates to:

$$M_{line} = \frac{\mu}{2\pi}\left[\frac{l_1+l_2}{2}\ln\left(\sqrt{\left(\frac{l_1+l_2}{2R}\right)^2+1}+\frac{l_1+l_2}{2R}\right)-\sqrt{\left(\frac{l_1+l_2}{2}\right)^2+R^2}\right]$$
$$-\frac{\mu}{2\pi}\left[\left|\frac{l_1-l_2}{2}\right|\ln\left(\sqrt{\left(\frac{l_1-l_2}{2R}\right)^2+1}+\left|\frac{l_1-l_2}{2R}\right|\right)-\sqrt{\left(\frac{l_1-l_2}{2}\right)^2+R^2}\right] \quad \text{(A.2)}$$

If two lines are equal in length, l, the above expression simplifies to:

$$M_{line} = \frac{\mu}{2\pi}\left[l\ln\left(\sqrt{\left(\frac{l}{R}\right)^2+1}+\frac{l}{R}\right)-\sqrt{l^2+R^2}+R\right] \quad \text{(A.3)}$$

When R<<l, the above equation can be transformed as follow:

$$M_{line} = \frac{\mu l}{2\pi}\left[\ln\frac{l}{R}\left(\sqrt{1+\left(\frac{R}{l}\right)^2}+1\right)-\sqrt{1+\left(\frac{R}{l}\right)^2}+\frac{R}{l}\right]$$
$$= \frac{\mu l}{2\pi}\left[\ln\frac{l}{R}+\ln\left(\sqrt{1+\left(\frac{R}{l}\right)^2}+1\right)-\sqrt{1+\left(\frac{R}{l}\right)^2}+\frac{R}{l}\right] \quad \text{(A.4)}$$

for $\sqrt{1+\left(\frac{R}{l}\right)^2} \approx 1+\frac{1}{2}\left(\frac{R}{l}\right)^2$,

$$M_{line} \approx \frac{\mu l}{2\pi}\left[\ln\frac{l}{R}+\ln\left(2+\frac{1}{2}\left(\frac{R}{l}\right)^2\right)-1-\frac{1}{2}\left(\frac{R}{l}\right)^2+\frac{R}{l}\right] \quad \text{(A.5)}$$

Because of $\ln\left(1+\left(\frac{R}{2l}\right)^2\right) \approx \left(\frac{R}{2l}\right)^2$,

$$M_{line} \approx \frac{\mu l}{2\pi}\left[\ln\frac{l}{R}+\ln 2+\left(\frac{R}{2l}\right)^2-1-\frac{1}{2}\left(\frac{R}{l}\right)^2+\frac{R}{l}\right] = \frac{\mu l}{2\pi}\left[\ln\frac{2l}{R}+\frac{R}{l}-1-\frac{R^2}{4l^2}\right] \quad \text{(A.6)}$$

Although valid strictly only for parallel line filaments, equation (A.6) forms the basis for deriving simple expressions for the self and mutual inductances of systems of conductors with finite cross sections.

Noting that equation (A.6) contains three terms that are functions of the distance between the two lines, *R*. Among these three terms, the dominant one is proportional to $\ln\frac{2l}{R}$. This term is followed in order of importance by first the linear term and then the quadratic one. In the case of parallel line filaments, the distance *R* is a constant.

2. Conductors with Finite Cross Sections

When equation (A.6) is extended to cases of finite conductor cross sections, the total inductance is now the weighted average of the mutual inductance between parallel line

filaments separated by a distance R, where R is now a continuous variable that spans distances between all possible combination of points in the cross section. Therefore each of the three terms involving R is transformed to a mean distance that represents the weighted average of that term over all possible values of R.

By definition, the mean of the term $\ln R$ is replaced by the natural logarithm of the geometric mean distance (GMD), while R and R^2 terms are replaced by the arithmetic mean distance (AMD) and the arithmetic mean square distance (AMSD), yielding the following general approximate expression:

$$M_{gen} \approx \frac{\mu l}{2\pi}\left[\ln\frac{2l}{GMD}+\frac{AMD}{l}-1-\frac{AMSD^2}{4l^2}\right] \qquad \text{(A.7)}$$

3. Geometric Mean Distance

By definition, the geometric mean distance of distances, d_1, d_2, d_n is given by well known expression:

$$\text{GMD}=\sqrt[n]{d_1 d_2 \ldots\ldots d_n} \qquad \text{(A.8)}$$

The equivalent representation can be obtained by taking the natural logarithm of both sides so that:

$$\ln(GMD)=\frac{1}{n}[\ln(d_1)+\ln(d_2)+\ldots\ldots+\ln(d_n)] \qquad \text{(A.9)}$$

Thus the GMD between p points on one set and q points on another set is:

$$\ln(GMD)=\frac{1}{pq}\left[\sum_{i=1}^{p}\sum_{j=1}^{q}\ln(d_{i,j})\right] \qquad \text{(A.10)}$$

The GMD may also be defined for distances involving continuous variables. The continuous equivalent of equations (A.10) was first introduces as an aid in inductance calculations by Maxwell. Maxwell discussed the value of the GMD for cross sections that span two dimensions as well as one dimension. In particular, he highlighted that the sensible observations that the GMD of straight lines is useful in determining inductances of current sheets, whereas the GMD of rectangles is useful in determining inductances of conductors with rectangular cross sections. He defined the GMD between two conductors with fixed cross sections of areas A_1 and A_2 as that value that satisfied the following relations:

$$A_1 A_2 \ln(GMD) = \iiiint \ln r dx dy dx' dy' \qquad (A.11)$$

where $dxdy$ is the clement of area of the first conductors cross section, $dx'dy'$ is the element of area of the second conductors cross section, r is the distance between these elements, the integration extended first over every element of the first section and then over every element of the second.

For line filaments, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1 l_2 \ln(GMD) = \iint \ln r dx dx' \qquad (A.12)$$

Here l_1 and l_2 are the lengths of the two lines and dx and dx' are the element of line of the first and second lines.

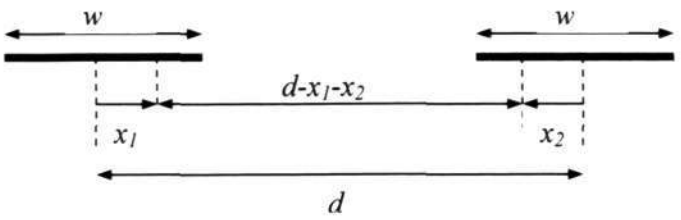


Fig A.3: Two equal length straight lines on the same axis

In general, the evaluation of the multiple integrals can be tedious. Even when closed form solutions exist, the results can be bulky and inconvenient. Fortunately the GMD of geometries common to practical inductance calculations have simple forms. Figure A.3 illustrates two equal straight line segments of length, w, that lie on the same line and are separated by center to center distance, d. The GMD is given by appropriate substitution into equation (A.12):

$$\ln(GMD) = \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} \ln|d - x_1 - x_2| dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} \tag{A.13}$$

Although this integral has a closed form solution, the result does not provide much insight. Instead, a series expansion of the result in terms of $\frac{w}{d}$ yields a more useful result:

$$\ln(GMD_{2lines}) \approx \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} \cdots\cdots \tag{A.14}$$

This result is widely used in calculations of the mutual inductance between straight parallel conductors. In the same manner that the GMD between two distinct cross sections is used in mutual inductance calculations, the GMD of a single cross section is used in self-inductance calculations. The GMD of a straight line of length w, as shown in Figure A.4, is used in the calculation of the self-inductance of current sheets, the result is:

$$\ln(GMD_{1line}) = \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} \ln|x_1 + x_2| dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} = \ln w - 1.5 \tag{A.15}$$

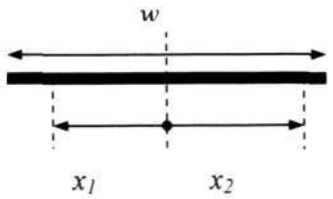


Fig A.4: A single straight line of length w

The procedure for calculating the GMD of a rectangular cross section of width, w, and thickness, t, as shown in Figure A.5, is more tedious. Although a closed form expression does exist, the exact result does not provide any insight. Fortunately, this expression may be approximated to give enough accuracy by replacing w in equation (A.15) by $(w+t)$:

$$\ln(GMD_{\text{rect}}) \approx \ln(w+t) - 1.5 \qquad \text{(A.16)}$$

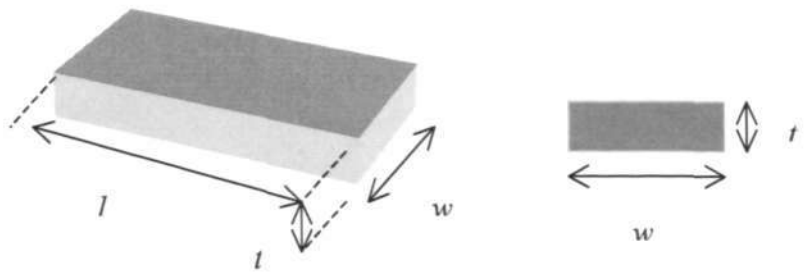


Fig A.5: A conductor with rectangular cross section

4. Arithmetic Mean Distance

The arithmetic mean distance (AMD) of n distance is simply the mean of these distances:

$$AMD = \frac{1}{n}\left[d_1 + d_2 + \cdots\cdots + d_n\right] \qquad \text{(A.17)}$$

The AMD may be defined for multiple variables. Thus the AMD between p points on one set and q points on another set is:

$$AMD = \frac{1}{pq}\left[\sum_{i=1}^{p}\sum_{j=1}^{q} d_{i,j}\right] \qquad \text{(A.18)}$$

where $d_{i,j}$ refers to the distance between point i (on the first set) and point j (on the second set). This idea may be extended to cases where the distances involve continuous variables. Once again, the AMD is the mean of the variable distances. The AMD between two

conductors with fixed cross sections of areas A_1 and A_2 is that value which satisfies the following relation:

$$A_1 A_2 AMD = \iiiint rdxdydx'dy' \tag{A.19}$$

where $dxdy$ is the element of area of the first conductor's cross section, $dx'dy'$ is the element of area of the second cross section and r is the distance between these elements.

For geometries involving lines, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1 l_2 AMD = \iint rdxdx' \tag{A.20}$$

Lengths l_1 and l_2 are those of the two lines and dx and dx' are the elements of line of the first and the second lines.

Easy to evaluate the AMD of a straight line of length, w:

$$AMD = \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w}|x_1 + x_2|dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} = \frac{w}{3} \tag{A.21}$$

For a rectangle of length, w, and thickness, t, an approximated value of AMD is given by:

$$AMD_{1rect} \approx \frac{w+t}{3} \tag{A.22}$$

5. Arithmetic Mean Square Distance

The arithmetic mean square distance, AMSD, between two conductors with fixed cross sectional areas A_1 and A_2 is the value that satisfied the following relation:

$$A_1 A_2 AMSD^2 = \iiiint r^2 dxdydx'dy' \tag{A.23}$$

where the meanings of $dxdy$, $dx'dy'$ and r are same to those in equation (A.19). For geometries involving lines, the area integrals become line integrals and the quadruple integrals reduce to double integrals:

$$l_1 l_2 AMSD^2 = \iint r^2 dxdx' \tag{A.24}$$

The AMSD of a straight line is used in several inductance calculations. The AMSD of a straight line of length, w, is:

$$AMSD^2 = \frac{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} |x_1 + x_2|^2 dx_1 dx_2}{\int_{-0.5w}^{0.5w}\int_{-0.5w}^{0.5w} dx_1 dx_2} = \frac{w}{\sqrt{6}} \tag{A.25}$$

Similarly, the result for the AMSD of a rectangle of length, w, and thickness, t, is:

$$AMSD = \frac{\sqrt{w^2 + t^2}}{\sqrt{6}} \tag{A.26}$$

6. The Inductance of a Practical Spiral Inductor

Considering equation (A.7), (A.16), (A.22) and (A.26), we can obtain the self-inductance expressions for a straight conductor:

$$L = \frac{\mu l}{2\pi}\left[\ln\frac{2l}{w+t} + \frac{w+t}{3l} + 0.5 - \frac{w^2 + t^2}{24l^2}\right] \tag{A.27}$$

where μ is permeability of air, which value is equal to $4\pi x10^{-7}$ H/m, l is the length of conductor, w is the width of conductor and t is the thickness of conductor.

For the value of mutual inductances of two conductors, substituting R by GMD in equation (A.3) we can obtain:

$$M_{line} = \frac{\mu}{2\pi}\left[\frac{l_1+l_2}{2}\ln\left(\sqrt{\left(\frac{l_1+l_2}{2GMD}\right)^2+1}+\frac{l_1+l_2}{2GMD}\right)-\sqrt{\left(\frac{l_1+l_2}{2}\right)^2+GMD^2}\right]$$
$$-\frac{\mu}{2\pi}\left[\left|\frac{l_1-l_2}{2}\right|\ln\left(\sqrt{\left(\frac{l_1-l_2}{2GMD}\right)^2+1}+\left|\frac{l_1-l_2}{2GMD}\right|\right)-\sqrt{\left(\frac{l_1-l_2}{2}\right)^2+GMD^2}\right] \quad \text{(A.28)}$$

where GMD, according to equation (A.14), is:

$$\ln GMD = \ln d - \left[\frac{w^2}{12d^2}+\frac{w^4}{60d^4}+\frac{w^6}{168d^6}+\frac{w^8}{360d^8}+\frac{w^{10}}{660d^{10}}+\cdots\right] \quad \text{(A.29)}$$

The inductance of a spiral inductor in Figure A.6 is equal to the sum of the self-inductance for each segment in the coil plus the mutual inductance, which are determined by the geometry and the phase relationship between the current carried by those lines.

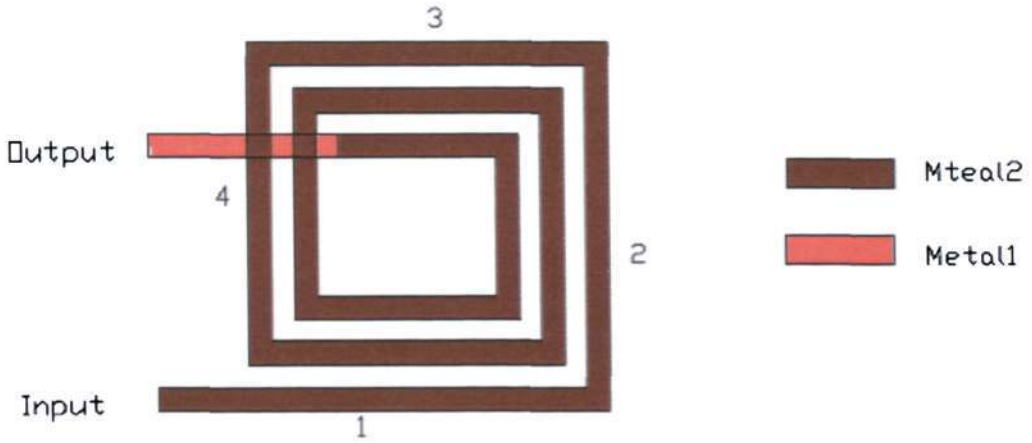


Fig A.6: Layout of a typical rectangular spiral inductor

The model of two straight conductors carrying in-phase or out-of-phase current is shown in Figure A.7.

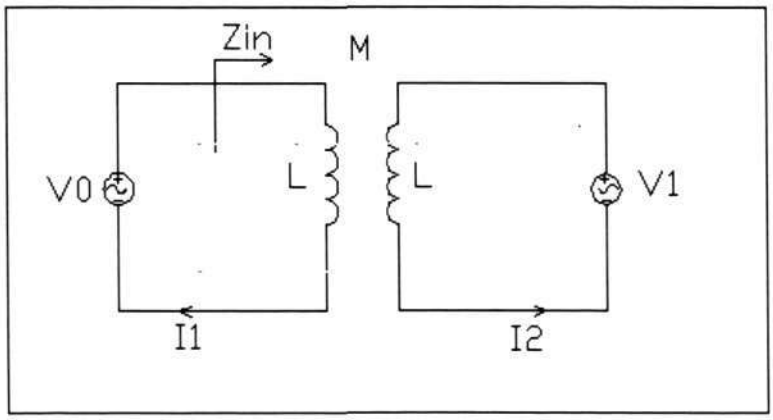


Fig A.7: Modeling of two conductors carrying in-phase and out-of-phase current

There is a mutual inductance of M between the two conductors. For in-phase current such as the current in segment 1 and 5 of the inductor in Figure A.6, two equations govern the voltages and currents in the two conductors:

$$V_0 = I_1(j\omega L) + I_2(j\omega M) \tag{A.30}$$

$$V_1 = I_2(j\omega L) + I_1(j\omega M) \tag{A.31}$$

For in phase current, V_1 is equal to V_2. After manipulation of the equation (A.30) and (A.31), we can calculate that the impedance Z_{in} of segment 1 is:

$$Z_{in}=j\omega(L+M) \tag{A.32}$$

which means the inductance of the conductor increase by M, and M is the mutual inductance between the two conductors. So, parallel currents traveling in phase can contribute positive mutual components of inductance. Obviously, for the case of out-of-phase current, it will contribute negative mutual components of inductance. Thus the inductance of a conductor can be expressed as:

$$L = L_{self} \pm M \tag{A.33}$$

The total inductance of the spiral in Figure A.6, is the sum of the self-inductances of each of the straight segment plus the mutual inductances between segments, which is:

$$L_T = L_0 + M_+ - M_- \tag{A.34}$$

where L_T is the total inductance, L_0 is the sum of the self-inductances of all straight segments, M_+ is the sum of the positive mutual inductances and M_- is the sum of the negative mutual inductances.

For a rectangular planar inductor with n complete turns and 4n segments, the total inductance is:

$$L_{total} = \sum_{i=1}^{4n} L_{self_i} + 2\left[\sum_{j=1}^{n}\left(\sum_{i=1}^{4n-4} M_{i,i+4j} - \sum_{i=1}^{4n-2} M_{i,i+2j}\right)\right] \tag{A.35}$$

Appendix B

Process Parameters and Equipments for Spiral Inductors

Table B.1: Lithography processes for photoresist mask

Process	AZ7220	AZ9260
Spin speed	2000 rpm/30sec	2000 rpm/30sec
Pre bake	100°C/1.5 mins	110°C/5 mins
Exposure	4 sec	70 sec
Post bake	100°C/1mins	———
Develop time	45sec in AZ300 developer	120sec in AZ421 developer
Rinsing	in DI water	in DI water
Drying	using spin machine	using spin machine
Thickness	2 μm	7 μm

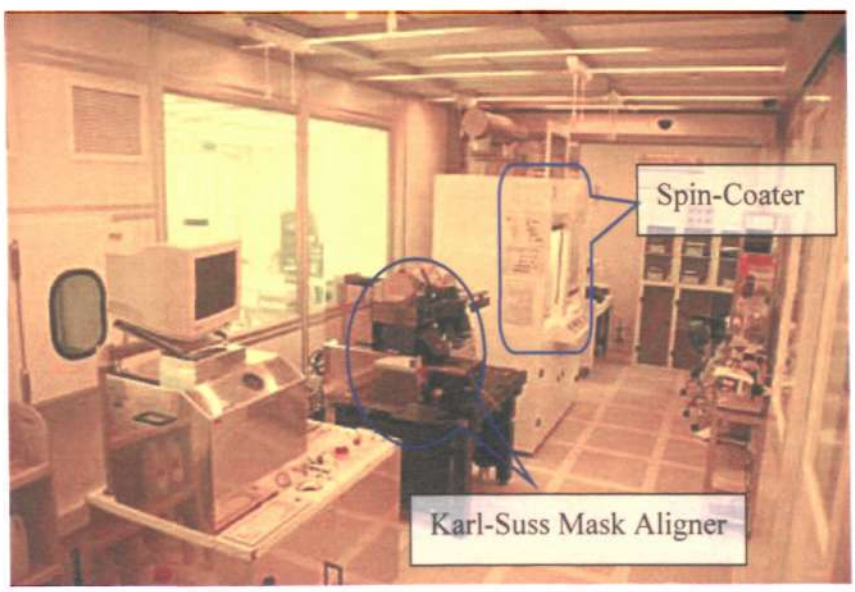


Fig B.1: Lithography equipments

Table B.2: DRIE parameters for etching 2 μm beam-trench structures

	Etching	Passivation
Coil Power	800 W	800 W
Platen Power	100 W	—
SF_6	130 sccm	—
O_2	13 sccm	—
C_4F_8	—	100 sccm
Pressure	15 mT	15 mT
Time Cycle	8 s	5 s
Temperature	20°C	20°C

Fig B.2: STS DRIE equipment

Table B.3: Process recipe of thermal oxidation

Processes	Gas/Flow (sccm)	Temperature (°C)	Time (hours)
Dry Oxidation	O_2/3000	1100	0.5
Wet Oxidation	O_2/120, H_2O	1100	9
Dry Oxidation	O_2/3000	1100	0.5
Annealing	N_2/3000	1100	0.5

Table B.4: Recipe of LTO process

SiH_4	80 sccm
O_2	120 sccm
Pressure	300 mT
Temperature	450°C

Fig B.3: Tystar furnaces for thermal oxidation and LTO

Table B.5: STS PECVD for SiO_2 deposition process

Low Frequency	380 KHz
Temperature	300°C
SiH_4	50 sccm
N_2O	2000 sccm
Power	60 W
Pressure	900 mT
Dep. Rate	400 nm/min

Table B.6: RIE process parameters

Etching Material	Gas/Flow	Pressure	Power	Etching rate
AZ7220/AZ9260	O_2/10 sccm	100 mT	350 W	200 nm/min
SiO_2	CF_4/9 sccm, O_2/1 sccm	100 mT	350 W	25 nm/min

Fig B.4: Micro RIE equipment

Table B.7: Metal sputtering process

Metals	Gas/Flow	Pressure	Voltage	Current	Deposition rate
Cr	He/40 sccm	2 mT	0.336 kV	598 mA	15 nm/min
Au	He/40 sccm	2 mT	0.380 kV	528 mA	35 nm/min

Fig B.5: Sputtering equipment

Appendix C

MATLAB Program of GA for Parameter Extraction

```
function [opt,fitness]=smallestfitness(components)
% main function, Extract Ls,Rs,Cs
% options contains the following:
% options(1) = 0 no printout
%              1 prints out summary statistics only
%              2 prints out summary statistics and initial and final populations
% options(2) = 0 standard binary encoding
%              1 Gray encoding
% options(3) = 0 uses standard replacement for the next generation
%              N combine offspring with best N parents to form next generation
% options(4) = 0 roulette wheel selection
%              1 stochastic universal sampling
% options(5) = 0 one-point crossover
%              1 uniform crossover
% options(6) = 0 no fitness scaling
%              1 linear fitness scaling (scaling parameter c=2)

meanfhistory=[];
minfhistory=[];
opthistory=[];
numgens=100;

compsize=200;
lbits=[20,20,20]; % [ Ls, Rs, Cs]
vlb=[3.0,15,8];
vub=[4.0,20,12];

pc=0.65;
pm=0.1;
options=[0,1,100,1,1,1];

% Generate the initial population
gen=0;
comp=Initialise(compsize,lbits);

% Decoding the binaray data to interger LRC data
component=Decode(comp,lbits,vlb,vub,options);

componentlen=length(component);

% Obtain fitness statistics for the initial population
fitness=fun(component);

fitness1=fitness;
Ls=component(:,1);
Rs=component(:,2);
```

```
Cs=component(:,3);

meanf=sum(fitness)/length(fitness);
[minf,imin]=min(fitness);
opt=component(imin,:);
opthistory=[opthistory;opt];
minfhistory=[minfhistory;minf];
meanfhistory=[meanfhistory;meanf];

% Main generation loop
for gen=1:numgens

    % Reproduce
    matingpairs =Reproduce(comp,fitness,options);

    % Crossover
    offspring = Crossover(comp,pc,options);

    % Mutate
    newcomp = Mutation(offspring,pm);

    % Obtain current interger LRC data by decoding the binaray data
    component=Decode(newcomp,lbits,vlb,vub,options);

    % Obtain fitness of the current population
    newfitness=fun(component);
    fitness1(gen*componentlen+1:(gen+1)*componentlen)=newfitness(1:componentlen);
    Ls(gen*componentlen+1:(gen+1)*componentlen)=component(1:componentlen,1);
    Rs(gen*componentlen+1:(gen+1)*componentlen)=component(1:componentlen,2);
    Cs(gen*componentlen+1:(gen+1)*componentlen)=component(1:componentlen,3);

    % Calculate population statistics to be saved in the history parameters
    meanf=sum(newfitness)/size(component,1);
    [minf,imin]=min(newfitness);
    opt=component(imin,:);
    opthistory=[opthistory;opt];
    minfhistory=[minfhistory;minf];
    meanfhistory=[meanfhistory;meanf];

    % Selection procedure for the next generation
    if options(3) == 0
        % Replace parents by offspring
            comp=newcomp;
            fitness=newfitness;
      else
        % Sort parent population and combine offspring with best options(3) of parents
                [parsort,sorti]=sort(fitness);
                combcomp=[comp(sorti(1:options(3)),:);newcomp];
                combfit=[fitness(sorti(1:options(3)));newfitness];
                % Sort combined population and choose best of parents and offspring
                [fitsort,fiti]=sort(combfit);
              comp=combcomp(fiti(1:compsize),:);
                fitness=combfit(fiti(1:compsize));
                component=Decode(comp,lbits,vlb,vub,options);
        end
        if min(fitness)<0.01 break, end;
    end;

% Output results
opt=component(imin,:)
```

```
opthistory=[opthistory;opt];
minfhistory=[minfhistory;minf];
meanfhistory=[meanfhistory;meanf];

% End of main function

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function comp=Initialise(compsize, lbits)
% Initial generates the initial population
comp=(rand(compsize,sum(lbits))<0.5);

% End of Initial

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function component = Decode(comp,lbits,vlb,vub,options)
% Decode converts a population (popn) of strings from binary to real.
% Each string in popn is of length sum(lbits) and consists of m=length(lbits)
% substrings which decode to the variables x_1,...,x_m
% If options(2)=1, first decodes Gray code into binary

% First decode each substring to an unsigned decimal integer: xint
index1=1;
index2=0;
if options(2)==0
        newcomp=comp;
end

for i=1:length(lbits)
        % This part converts from Gray code to binary
        if options(2)==1
                newcomp(:,index1)=comp(:,index1);
                for j=1:lbits(i)-1
                newcomp(:,index1+j)=mod(newcomp(:,index1+j-1)+comp(:,index1+j),2);
                end;
        end;
        % String is now binary
        index2=index2+lbits(i);
        twopowers=2.^(lbits(i)-1:-1:0);
        xint(:,i)=newcomp(:,index1:index2)*twopowers';
        index1=index1+lbits(i);
end

% Now calculate the x values
factor=(vub-vlb)./(2.^lbits-1);
component=ones(size(comp,1),1)*vlb+xint*diag(factor);

% End of Decode

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [matingpairs,select]=Reproduce(comp,fitness,options)
% Reproduce produces the mating pairs for crossover.
% select contains the numbers of each string in popn which has been added to
% the mating pool

if options(6)>0
        % First call for linear fitness scaling
        fitness=Scalefitness(fitness,2);
```

```
end

if options(4)==0
        % Roulette wheel selection
        randnums=rand(size(fitness));
else
        % Stochastic universal sampling
        rr=rand;
        spacing=1/length(fitness);
        randnums=sort(mod(rr:spacing:1+rr-0.5*spacing,1));
end

re_fit=1./fitness;
norm_re_fit=re_fit/sum(re_fit);
partsum=0;
count(1)=0;
matepool=[];

for i=1:length(re_fit)
        partsum=partsum+norm_re_fit(i);
        count(i+1)=length(find(randnums<partsum));
        select(i,1)=count(i+1)-count(i);
        matepool=[matepool;ones(select(i,1),1)*comp(i,:)];
end;

% Now re-order the strings for mating so that the string in row 1
% is to be mated with the string in row 2, etc.
[junk,mating] = sort(rand(size(matepool,1),1));
matingpairs = matepool(mating,:);

% End of Reproduce

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function offspring=Crossover(comp,pc,options)
% Crossover creates offspring from a population (ordered mating pool)
% using crossover with probability pc.

if options(5)==0
        % One-point crossover
        lbits = size(comp,2);
        sites = ceil(rand(size(comp,1)/2,1)*(lbits-1));
        sites = sites.*(rand(size(sites))<pc);

        for j = 1:length(sites);
                offspring(2*j-1,:) = [comp(2*j-1,1:sites(j)) comp(2*j,sites(j)+1:lbits)];
                offspring(2*j,:) = [comp(2*j,1:sites(j)) comp(2*j-1,sites(j)+1:lbits)];
        end
else
        % Uniform crossover
        for i=1:size(comp,1)/2
                if rand<pc
                        template=rand(1,size(comp,2))<0.5;
                        offspring(2*i-1,:)=template.*comp(2*i-1,:)+(1-template).*comp(2*i,:);
                        offspring(2*i,:)=template.*comp(2*i,:)+(1-template).*comp(2*i-1,:);
                else
                        offspring(2*i-1,:)=comp(2*i-1,:);
                        offspring(2*i,:)=comp(2*i,:);
                end
        end
```

```
end

% End of Crossover

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function newcomp = Mutation(offspring,pm)
% Mutation changes a gene of the offspring with probability pm.
mutate = find(rand(size(offspring))<pm);

% mutate contains the positions of the genes to be mutated as a column vector
% going down the columns of the matrix offspring
newcomp = offspring;
newcomp(mutate) = 1-offspring(mutate);

% End of Mutation

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function scfitness=Scalefitness(fitness,fmultiple)
% Scalefitness performs linear scaling on the fitness values and returns the
% results in scfitness
% Calculate the parameters a and b
favg=sum(fitness)/length(fitness);
[fmax,i]=max(fitness);
[fmin,j]=min(fitness);
a=favg*(fmultiple-1)/(fmax-favg);
b=favg*(1-a);
if a*fmin+b<0
        a=favg/(favg-fmin);
   b=favg*(1-a);
end

% The scaled fitness
scfitness=a*fitness+b*ones(size(fitness));

% End of Scalefitness

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function fitness = fun(component)

format long

Ls=component(:,1);
Rs=component(:,2);
Cs=component(:,3);

Z1=[];
Y12S=[];
Diff=[];

Y = input('Measured Y12 parameter, Y= ');
Y12M=Y;
f=0.1*10^9:0.1*10^9:10*10^9;
w=2*pi*f;

for i=1:length(w)
ZZ1=(Rs+j*w(i)*Ls*10^(-9))./(1-w(i)^2*Ls*10^(-9).*Cs*10^(-15)+j*w(i)*Cs*10^(-15).*Rs);
Y12SS=-1./ZZ1;
```

```
Dif=(Y12SS-Y12M(i))./Y12M(i);

Z1=[Z1  ZZ1];
Y12S=[Y12S  Y12SS];
Diff=[Diff  Dif];
end;

Diffmean=sum(Diff,2)/length(w);
Meanexpand=Diffmean*ones(1,length(w));

fit=Diff.^2+(Diff-Meanexpand).^2;
fitn=sum(fit,2);

fitness=1000*(abs(fitn)+abs(angle(fitn)));

% End of fun

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% End of file
```

Appendix D

Mathcad Program for Calculating Inductance of Spiral Inductors

$$\left(\text{Calculate} - \text{five} - \text{turns} - \text{inductor}, \text{Unit}, \text{length}, \text{cm}, \text{L}, \text{nH}, \mu, \frac{\text{nH}}{\text{cm}}\right)$$

$t := 0.0001 \quad s := 0.001 \quad w := 0.001 \quad l_1 := 0.035 \quad N := 5 \quad \mu := 4\cdot\pi$

$$k := 4\cdot N$$

$$r := 2..2\cdot N$$

$$l_2 := l_1$$

$$l_3 := l_1$$

$$l_{2,r} := l_2 - (r-1)\cdot(w+s)$$

$$l_{2,r-1} := l_1 - (r-2)\cdot(w+s)$$

$$\text{length} := \sum_{y=1}^{k} l_y$$

$l_1 = 0.035$

$l_2 = 0.035$

$l_3 = 0.035$

$l_4 = 0.033$

$\text{length} = 0.538$

$$y := 1..k$$

$$L_y := \frac{\mu}{2\cdot\pi}\cdot l_y\cdot\left[\ln\left(2\cdot\frac{l_y}{w+t}\right) + \left(\frac{w+t}{3\cdot l_y}\right) + 0.5 - \frac{w^2+t^2}{24\cdot\left(l_y\right)^2}\right]$$

$$L_0 := \sum_{y=1}^{k} L_y$$

$L_0 = 4.763 \qquad (\text{self} - \text{inductance})$

$$GMD1 := \left| \begin{array}{l} \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad t_{j,(j+4\cdot n)} \leftarrow e^{\ln(n\cdot(s+w)) - \left[1 + \frac{1}{12\cdot\left[\frac{n\cdot(s+w)}{w}\right]^2} + \frac{1}{60\cdot\left[\frac{n\cdot(s+w)}{w}\right]^4} + \frac{1}{168\cdot\left[\frac{n\cdot(s+w)}{w}\right]^6}\right]} \quad \text{if } (j+4\cdot n)\le k \\ \quad\quad 0 \quad \text{otherwise} \\ t \end{array} \right.$$

$$M1 := \left| \begin{array}{l} sum \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad sum \leftarrow sum + 2\cdot l_j \cdot \left[\ln\left[\frac{l_j}{GMD_{j,(j+4\cdot n)}} + \left[1 + \left[\frac{l_j}{GMD_{j,(j+4\cdot n)}}\right]^2\right]^{0.5}\right] - \left[1 + \left[\frac{GMD_{j,(j+4\cdot n)}}{l_j}\right]^2\right]^{0.5} + \frac{GMD_{j,(j+4\cdot n)}}{l_j}\right] \quad \text{if } (j+4\cdot n)\le k \\ \quad\quad 0 \quad \text{otherwis} \\ sum \end{array} \right.$$

$$M1m := \left| \begin{array}{l} sum1m \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad sum1m \leftarrow sum1m + 2\cdot l_{j+4n} \cdot \left[\ln\left[\frac{l_{j+4n}}{GMD1_{j,(j+4n)}} + \left[1 + \left[\frac{l_{j+4n}}{GMD1_{j,(j+4n)}}\right]^2\right]^{0.5}\right] - \left[1 + \left[\frac{GMD1_{j,(j+4n)}}{l_{j+4n}}\right]^2\right]^{0.5} + \frac{GMD1_{j,(j+4n)}}{l_{j+4n}}\right] \quad \text{if } (j+4\cdot n)\le k \\ \quad\quad 0 \quad \text{otherwise} \\ sum1m \end{array} \right.$$

$$M1p := \left| \begin{array}{l} sum1p \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad sum1p \leftarrow sum1p + 2\cdot\left(l_j - l_{j+4n}\right) \cdot \left[\ln\left[\frac{\left(l_j - l_{j+4n}\right)}{GMD1_{j,(j+4n)}} + \left[1 + \left[\frac{\left(l_j - l_{j+4n}\right)}{GMD1_{j,(j+4n)}}\right]^2\right]^{0.5}\right] - \left[1 + \left[\frac{GMD1_{j,(j+4n)}}{\left(l_j - l_{j+4n}\right)}\right]^2\right]^{0.5} + \frac{GMD1_{j,(j+4n)}}{l_j - l_{j+4n}}\right] \quad \text{if } (j+4\cdot n)\le k \\ \quad\quad 0 \quad \text{otherwise} \\ sum1p \end{array} \right.$$

$$M1 = M1j + M1m - M1p \quad \text{(Positive mutual inductance)}$$

$$GMD2 = \left| \begin{array}{l} \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad \left| \begin{array}{l} u_{j,(j+4\cdot n-2)} \leftarrow e^{\ln\left[l_{j+1}-n\cdot(s+w)\right]-\left[1+\frac{1}{12\cdot\left[\frac{l_{j+1}-n\cdot(s+w)}{w}\right]^2}+\frac{1}{60\cdot\left[\frac{l_{j+1}-n\cdot(s+w)}{w}\right]^4}+\frac{1}{168\cdot\left[\frac{l_{j+1}-n\cdot(s+w)}{w}\right]^6}\right]} \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ u \end{array} \right.$$

$$M2j = \left| \begin{array}{l} sum2 \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad \left| \begin{array}{l} sum2 \leftarrow sum2 + 2\cdot l_j \cdot \left[\ln\left[\frac{l_j}{GMD2_{j,(j+4\cdot n-2)}} + \left[1+\left[\frac{l_j}{GMD2_{j,(j+4\cdot n-2)}}\right]^2\right]^{0.5}\right] - \left[1+\left[\frac{GMD2_{j,(j+4\cdot n-2)}}{l_j}\right]^2\right]^{0.5} + \frac{GMD2_{j,(j+4\cdot n-2)}}{l_j} \right] \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ sum2 \end{array} \right.$$

$$M2m = \left| \begin{array}{l} sum2m \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad \left| \begin{array}{l} sum2m \leftarrow sum2m + 2\cdot l_{j+4\cdot n-2} \cdot \left[\ln\left[\frac{l_{j+4\cdot n-2}}{GMD2_{j,(j+4\cdot n-2)}} + \left[1+\left[\frac{l_{j+4\cdot n-2}}{GMD2_{j,(j+4\cdot n-2)}}\right]^2\right]^{0.5}\right] - \left[1+\left[\frac{GMD2_{j,(j+4\cdot n-2)}}{l_{j+4\cdot n-2}}\right]^2\right]^{0.5} + \frac{GMD2_{j,(j+4\cdot n-2)}}{l_{j+4\cdot n-2}} \right] \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ sum2m \end{array} \right.$$

$$M2p = \left| \begin{array}{l} sum2p \leftarrow 0 \\ \text{for } j \in 1..k \\ \quad \text{for } n \in 1..N \\ \quad\quad \left| \begin{array}{l} sum2p \leftarrow sum2p + 2\cdot\left(l_j - l_{j+4\cdot n-2}\right) \cdot \left[\ln\left[\frac{l_j - l_{j+4\cdot n-2}}{2\cdot GMD2_{j,(j+4\cdot n-2)}} + \left[1+\left[\frac{\left(l_j - l_{j+4\cdot n-2}\right)}{2\cdot GMD2_{j,(j+4\cdot n-2)}}\right]^2\right]^{0.5}\right] - \left[1+\left[\frac{2\cdot GMD2_{j,(j+4\cdot n-2)}}{\left(l_j - l_{j+4\cdot n-2}\right)}\right]^2\right]^{0.5} + \frac{2\cdot GMD2_{j,(j+4\cdot n-2)}}{l_{j+4\cdot n-2}} \right] \text{ if } (j+4\cdot n-2)\le k \\ 0 \text{ otherwise} \end{array} \right. \\ sum2p \end{array} \right.$$

$$M2 = M2j + M2m - M2p \quad \text{(Negative mutual inductance)}$$

$$L = L_0 + M1 - M2$$

$$L = 8.76 \qquad \text{(Total - Inductance)}$$

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