CMOS Integrated Circuits for Millimeter-Wave Imaging Applications

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Abstract

Thanks to the aggressive scaling of CMOS technology and promising applications of millimeter-wave (mm-wave) imaging, mm-wave imaging systems in CMOS have greatly evolved in recent years. Indeed, III-V compound semiconductor technologies are the desirable platforms for mm-wave imagers to achieve sufficient thermal sensitivity, typically on the order of 0.5 K, because of their superior noise figure and power gain at mm-wave frequencies compared to their silicon counterparts. Nevertheless, imaging systems implemented in CMOS demonstrate merits of low cost, high-level integration, and high yield, making CMOS technology more attractive for the implementation of multi-pixel imaging systems. This research explores CMOS integrated circuit design techniques for mm-wave imaging systems.

In the first part of this research, two wideband mm-wave LNAs for mm-wave imaging applications are presented. One is a five-stage cascode LNA based on peak-gain distribution technique. By distributing peak gains of the first four stages at only two frequency points, the five-stage cascode LNA exhibits 3-dB bandwidth of 21.5 GHz with 16.7-dB power gain. The other is a three-stage cascode LNA based on a novel pole-converging technique for intra-stage bandwidth extension. Its bandwidth is significantly extended by the proposed

design technique without increasing power consumption and die size. The fabricated prototype exhibits 3-dB bandwidth of 30 GHz with power consumption of 27 mW. To the author's best knowledge, this LNA achieves the widest 3-dB bandwidth among multi-stage mm-wave LNAs in CMOS technology.

In the second part, a direct-detection Dicke receiver with a switchable dual-path LNA (SDP-LNA) is designed for mm-wave imaging systems. Pole-converging technique for intra-stage bandwidth extension is adopted in the design of the SDP-LNA. Under a 1.8-V supply voltage, the SDP-LNA consumes 52.3 mW, and exhibits peak power gain of 26.8 dB, minimum NF of 6.4 dB, and 3-dB bandwidth of 25.5 GHz. Based on the SDP-LNA, a direct-detection Dicke receiver is implemented in a 65-nm CMOS technology. The prototype achieves noise-equivalent power (NEP) of 9.3 fW/Hz$^{0.5}$ and radiometer resolution, $\Delta T_{\min}$, of 0.65 K with power consumption of 52.6 mW.

The last part presents an ultra-low-power and low-cost mm-wave imaging receiver in a 65-nm CMOS technology. Based on super-regenerative reception, a charge-accumulation super-regenerative receiver (CA-SRR) is proposed, which significantly improves receiver responsivity and sensitivity. Furthermore, a new power injection method is adopted without loading the *LC*-tank of super-regenerative oscillator (SRO). The prototype achieves 2.8-fW/Hz$^{0.5}$ NEP and 0.21-K $\Delta T_{\min}$ with power consumption of 0.9 mW and core area of 0.02 mm^2.

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Abbreviations

AMMW	Active Millimeter-Wave
BWER	Bandwidth Extension Ratio
CA	Charge-Accumulation
CG	Common-Gate
CMOS	Complementary Metal-Oxide Silicon
CS	Common-Source
DA	Distributed Amplifier
DSP	Digital Signal Processing
FPA	Focal Plane Array
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
ISSCC	International Solid-State Circuits Conference
ITRS	International Technology Roadmap for Semiconductors
IoT	Internet of Things

LNA	Low-Noise Amplifier
NEP	Noise-Equivalent Power
NF	Noise Figure
MM-Wave	Millimeter-Wave
OOK	On-Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PMMW	Passive Millimeter-Wave
PSK	Phase Shift Keying
QPSK	Quadrature Phase Shift Keying
RFIC	Radio Frequency Integrated Circuit
RTPS	Reflective-Type Phase Shifter
RX	Receiver
SDP	Switchable Dual-Path

SNR	Signal-to-Noise Ratio
SoC	System on Chip
SPDT	Single Pole Double Throw
SRO	Super-Regenerative Oscillator
SRR	Super-Regenerative Receiver
THz	Terahertz
TL	Transmission Line
TRX	Transceiver
TX	Transmitter
UWB	Ultra-Wideband
WBAN	Wireless Body Area Network
WLAN	Wireless Local Area Network
WSN	Wireless Sensor Network

Table of Contents

Chapter 3

Chapter 4

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

List of Tables

Chapter 1

Introduction

1.1 Millimeter-Wave Applications

Millimeter-wave (mm-wave) frequencies range from 30 GHz to 300 GHz with corresponding free space wavelength between 10 mm and 1 mm. Because of unique characteristics and promising applications, research in mm-wave integrated circuits has grown considerably in the last 15 years. Figure 1.1 illustrates the worldwide publications related to mm-wave integrated circuits. Search results are obtained from the Scopus database using “millimeter-wave" and “integrated circuit" as keywords.

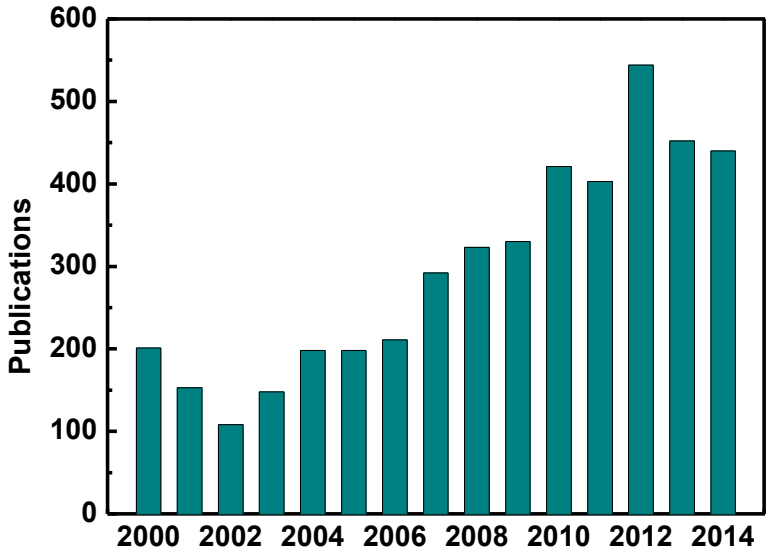


Figure 1.1 The number of mm-wave integrated circuit papers published in the past 15 years.

$$C = BW \cdot \log_2(1 + SNR) \tag{1.1}$$

Mm-wave systems provide much wider channel bandwidth and compact chip size compared to those implemented in low frequencies. Based on the Shannon's Theorem, expressed as (1.1), channel capacity *C*, is proportional to channel bandwidth BW, and signal-to-noise ratio (SNR). Increasing BW will enhance the channel capacity or alleviate the requirement of SNR for a given specification of channel capacity or data rate. Thanks to ultra-wide bandwidth in mm-wave frequency band, extremely high data rate can be achieved in mm-wave communication systems [1], [2]. The size of passive components such as antenna,

inductor, and transmission line, is obviously reduced at mm-wave frequencies, making multi-antenna systems much more compact. In addition, the resolution of radar and imaging systems is also enhanced, which is proportional to carrier frequency and bandwidth. Furthermore, mm-waves exhibit great propagation advantages, which result from the characters of atmospheric attenuation over the mm-wave frequency band due to the resonant absorption from atmospheric constituents, as shown in Figure 1.2. This phenomenon of atmospheric attenuation is called “atmospheric windows” [3].

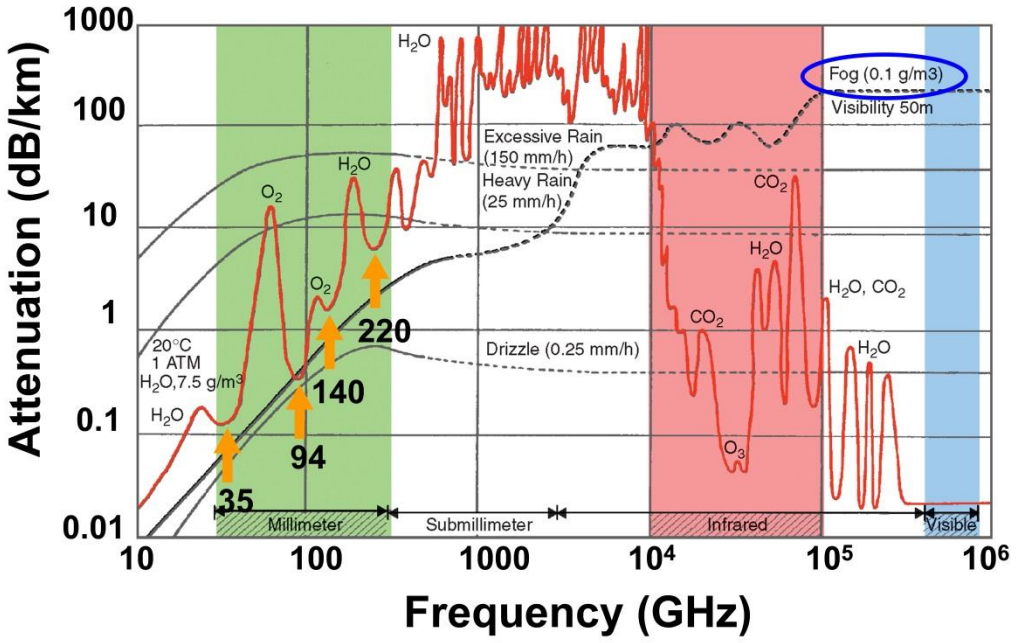


Figure 1.2 Attenuations of millimeter waves by atmospheric gases, rain, and fog [3]**.**

Promising applications of mm-waves have attracted more and more attention from the military and consumer. First of all, wireless uncompressed HD-video streaming known as the last-inch application lays in an unlicensed spectrum, 57-64 GHz [2], [4]. Because the attenuation in this band is extremely high, it is very suitable for short-range and high-data-rate communications with less interference with other nearby 60-GHz networks, which results in more users in one particular scene and the improvement of frequency reuse. Furthermore, mm-wave cellular wireless networks with wide bandwidth have tremendous potential to provide huge capacity and data rates for cellular communications, which may be adopted by next-generation cellular systems in the future [1]. The second one is ultra-high capacity point-to-point communications in the licensed E-band (71-76 GHz and 81-86 GHz) known as the last-mile application [5], [6], which is used for inter-building communications. The third brand of applications is targeted at automotive industry, such as long range radar in 76-77 GHz used for anti-crash and short range radar in 77-81 GHz used for lane change assistant [7], [8]. The forth one is mm-wave imaging and sensing applications at 94 GHz and above 100 GHz [9], [10]. Because of the atmospheric windows located at 35, 94, 140, and 220 GHz, the mm-waves at these frequencies exhibit low atmospheric attenuation and good penetrability. The potential applications of mm-wave circuits and systems are summarized in Table 1-1.

Table 1-1 Potential applications of mm-wave circuits and systems.

High-speed Communication	Radar Application	Imaging and Sensing
Wireless:	***Automotive:***	***Security:***
Wireless local area network (57-64 GHz) Wireless backhaul Point-to-point communication (E-band: 71-76,81-86 GHz) Inter-chip wireless connection Inter-satellite communication Mm-wave cellular wireless networks	Long range radar Short range radar Road condition detection	Search and rescue Drug and explosive detection Surveillance and targeting
Digital:	***Space:***	***Sensing:***
Data switches (Mux/DeMux) Broadband ADCs	Airplane navigation Aircraft landing aids	Earth sensing Radio astronomy Spectroscopy
	Industrial:	***Bio-imaging:***
	Distance measurement Building damage detection Spectrometer Motion detection	Medical imaging Tumor recognition Genetic screening

In the field of mm-wave imaging, the development is greatly driven by its promising applications, such as concealed weapons and explosives detection, surveillance and precision targeting for military imaging, all-weather visibility for airplane navigation, and non-intrusive imaging for medical applications [3]. Mm-wave imaging systems are classified into two categories, passive mm-wave (PMMW) imaging and active mm-wave (AMMW) imaging. PMMW imaging systems form images by detecting the naturally occurring mm-wave radiation from a scene without high-power source to illuminate and making use of the black-body radiation, as demonstrated in Figure 1.3. The black body radiation has

a specific spectrum and intensity that depends on temperature and emissivity of the body. PMMW imaging system is much like an infrared camera; however, infrared wavelengths are too short to pass through obstacles such as clothing, smoke, and fog. Because the cold sky acts as a powerful illuminative source to enhance image contrast, PMMW imaging is very suitable for outdoor stand-off detection. However, AMMW imaging system needs a high-power source for illumination working at the corresponding frequency to obtain better contrast or higher SNR, and receives reflected signal for imaging, which is similar to the concept of radars. Unlike X-ray systems with harmful ionizing radiation, AMMW imaging systems do not present any health issues to persons under inspection or operators, because radiations from mm-wave illuminative source are non-ionizing. Furthermore, compared to microwave imaging, mm-wave imaging demonstrates advantages of smaller chip size and higher resolution.

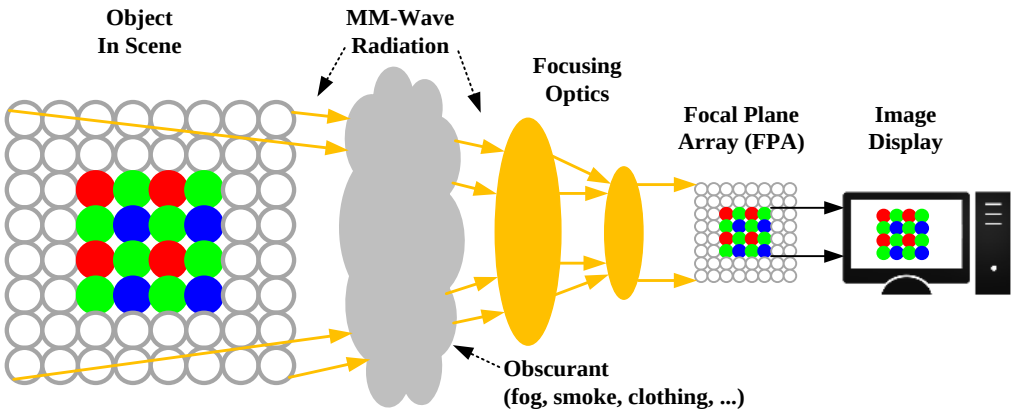


Figure 1.3 Cartoon demonstration of PMMW imaging system.

1.2 CMOS Technology to Address MM-Wave Solutions

Traditionally, III-V compound semiconductor technologies are the preferred platforms to implement mm-wave circuits and systems. Compared to CMOS technology, III-V technologies, such as GaAs MESFETs, pHEMT, InP HEMT, GaAs mHEMT, GaAs HBT, and InP HBT, have superior noise and power gain performance at high frequencies. Nevertheless, the fabrication cost of III-V technologies is quite high, while manufacturing yield is relatively low. Besides, systems implemented in III-V compound semiconductor usually use module-based level of integration with multi-chips. Due to incompatibility with mainstream integrated circuit technologies, it is impossible to integrate RF front-end and IF/baseband on a single chip.

Complementary metal-oxide silicon (CMOS) technology was invented in the 1960s. For a long time, the silicon MOSFET has been considered as a slow and noisy device that is not suitable for RF applications. Thanks to the continuous scaling of CMOS technology, RF performance of the silicon MOSFET has been improved considerably during the late 1990s and early 2000s. Nowadays, the silicon MOSFET is widely used in radio frequency integrated circuit (RFIC) design. Most RFICs are about system-on-chip (SoC) solutions for cellular, Bluetooth, wireless local area network (WLAN), global position system (GPS),

wireless sensor network (WSN), and Internet of things (IoT) with requirements for low cost, small size and incorporation of significant digital circuitries.

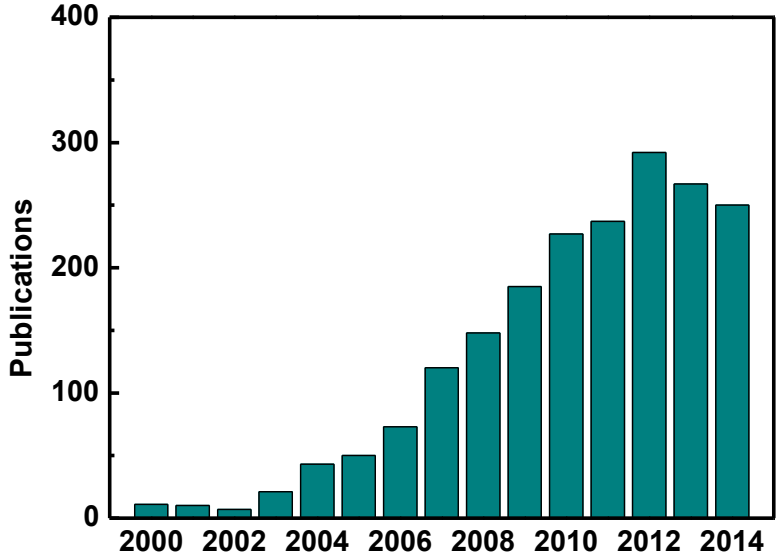


Figure 1.4 The number of CMOS mm-wave integrated circuit papers published in the past 15 years.

Recently, however, mm-wave CMOS integrated circuits have evolved greatly and entering the military and commercial market. The applications can be divided into high data-rate communications, vehicle radars, mm-wave imaging and sensing applications. As evident in Figure 1.4, interests in mm-wave integrated circuits in CMOS technology have grown considerably in the past 15 years. Search results are obtained from Scopus database using “millimeter-wave", “integrated circuit", and “CMOS" as keywords (refined results from Figure 1.1). Thanks to aggressive

technology scaling, the f_T and f_{max} of CMOS technology increase dramatically. Figure 1.5 depicts the f_T and f_{max} trends with the scaling of CMOS technology according to the international technology roadmap for semiconductor (ITRS) 2006 [11]. As can be seen, with the continuous scaling of CMOS technology, the f_T and f_{max} will be enhanced beyond 600 GHz in the year 2018. The performance of CMOS technology becomes comparable with that of III-V technologies in the mm-wave regime. Therefore, CMOS technology is an alternative solution for high-performance mm-wave systems. Besides, industries prefer to embrace CMOS technology rather than traditional III-V compound semiconductors.

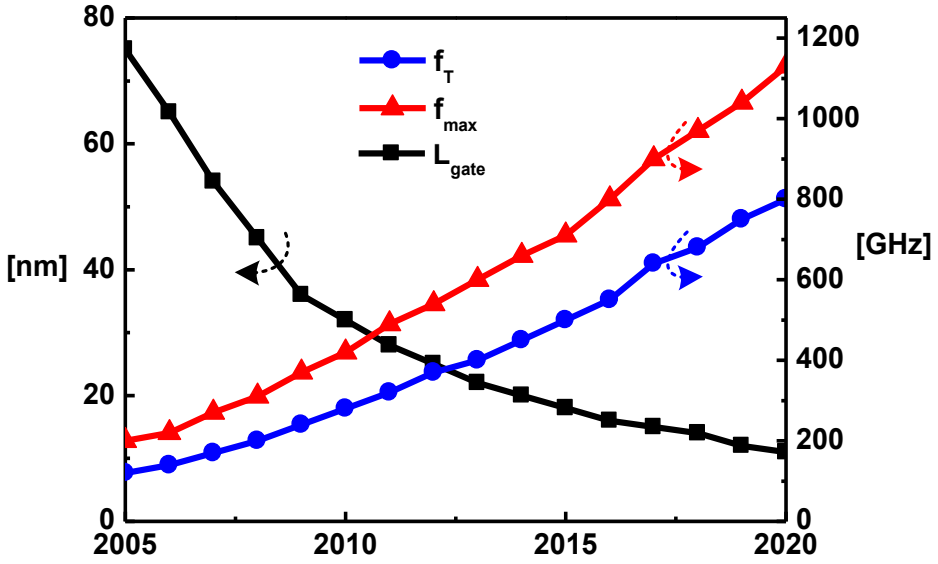


Figure 1.5 The f_T and f_{max} trends with the scaling of CMOS technology according to the ITRS 2006 [11].

Compared to III-V compound semiconductors, the main superiority offered by CMOS technology at mm-wave frequencies is overwhelmingly high-level integration with high yield, which results in systems with much lower cost. In the past several years, the integration level of CMOS technology developed from single transceiver (TRX) to multi-band TRX with digital baseband and even with power amplifier (PA), as demonstrated in Figure 1.6 [12]. This trend can be seen in all areas of RFIC design, from cellular and wireless sensors up to mm-wave systems. Thanks to the capability of integration with IF and baseband digital signal processing (DSP) function, even with PA, CMOS technology makes true SoC achievable.

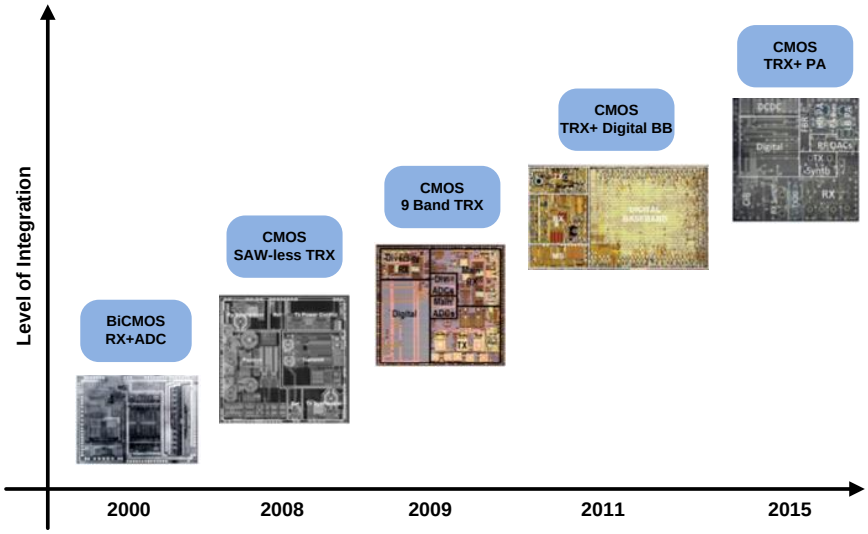


Figure 1.6 Integration trend in cellular wireless according to the ISSCC 2015 trends [12].

Although there are tremendous opportunities present for CMOS mm-wave systems, there are also a few challenges to be addressed in their successful deployment. First, the propagation of mm-waves suffers from more attenuation because of less discernible diffraction due to shorter wavelengths, which pose a challenge on the link budget of mm-wave communication system. However, high propagation attenuation is preferred for some applications because of effective channel reuse. Second, compared to compound semiconductor, silicon substrate introduces high energy loss due to low substrate resistivity. Therefore, passive devices suffer from significant energy loss at mm-waves. It is difficult to achieve an on-chip antenna with high power efficiency and an on-chip inductor with high quality factor on a silicon substrate. Third, power generation in small-feature size silicon technologies also presents a very serious challenge, mostly due to the lower breakdown voltages resulting from the scaling process and the shrinking of the depletion regions in the transistors. Finally, the modeling of the transistors and passive devices becomes more challenging at mm-wave frequencies. The smaller parasitic components within the models are more prone to error, and hence special attention must be paid to guarantee reliable results, especially in the presence of process variations and environmental changes [13]. Overall, research enthusiasms to CMOS mm-wave integrated circuits and systems would entry an even higher level in the future.

1.3 CMOS MM-Wave Imaging

Since the early 1960s, mm-wave radiometers have been used for radio astronomy [14]. However, mm-wave imaging systems have only recently become more and more attractive to the military and consumer due to great progress in monolithic mm-wave integrated circuit technologies. Current mm-wave imaging systems are mainly implemented in III-V compound technologies and utilize mechanical scanning to achieve very high resolution, around 0.5 K, which is typically cited as the threshold for constructing a good image with acceptable contrast in the indoor scenario [15], [16]. However, these systems exhibit several drawbacks of low-level integration, limitation of DSP electronics, high cost, and excessive pixel power consumption, which are critical for practical imaging systems with focal plane arrays (FPA). For a square array with $n \times n$ pixels, the total power consumption and chip size will be inflated by a factor of n^2.

In recent years, the continuous scaling of CMOS technology has led to better performance and higher level of integration. Furthermore, CMOS technology has a strong superiority in the DSP electronics. Thus, CMOS technology makes the system performance meet stringent requirements of imaging systems.

However, to achieve practical mm-wave imaging systems in CMOS technology, several challenges must be conquered. First of all, it is hard to achieve a high-

power illumination source. The output power of PA in CMOS is quite limited due to low breakdown voltage of CMOS transistors and high loss of on-chip passive components. Although the “atmospheric windows” exits in the mm-wave regime, the propagation loss is still quite high at mm-wave frequencies. For the transmissive mm-wave imaging system, the insertion loss of human bodies or obstacles is much higher. Therefore, imaging receivers with high sensitivity are extremely crucial for long-range imaging or alleviating the stringent requirement of link budget. Secondly, the intrinsic device gain is quite limited when working near the cut-off frequencies. Image resolution is inversely proportional to signal wavelength; therefore, higher frequency means better resolution. However, design of high resolution mm-wave imaging system is limited by low device gain near f_T and f_{max}, which also greatly reduces the sensitivity of imaging systems. Thirdly, the gain-bandwidth product in CMOS technology is limited compared to that of III-V technologies. Because naturally-radiating power of objects is extremely weak, wide front-end bandwidth and high gain are significant for PMMW imaging systems to achieve high quality images, especially the gain and bandwidth of LNA. Fourthly, the inferior noise performance degrades the sensitivity and responsivity of CMOS detector. Additional calibration or compensation circuits are needed to alleviate the effects from device noise, especially strong flicker noise. Fifthly, further work about the assembly and

packaging of mm-wave systems needs to be done, in order to fully integrate front-end and back-end.

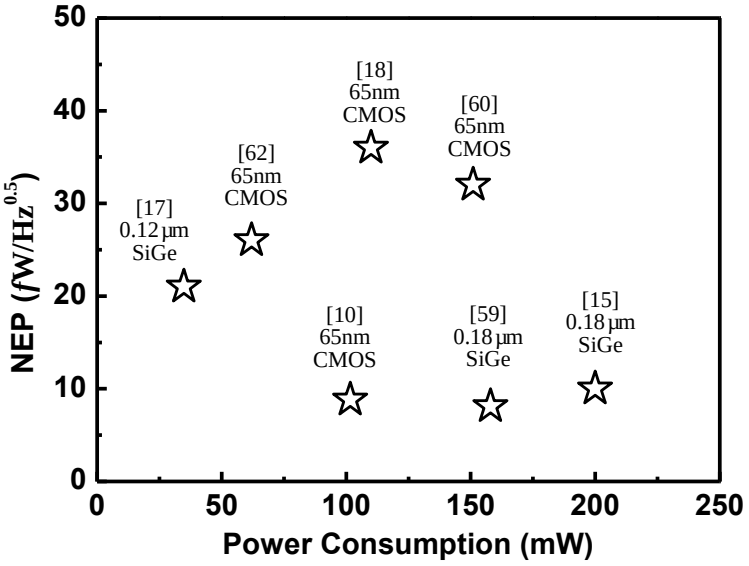


Figure 1.7 NEP and power consumption of the state-of-the-art mm-wave imaging receivers.

Considerable efforts have been devoted to developing mm-wave imaging systems in CMOS technology. Several approaches have been proposed in literature to implement CMOS imaging systems, such as direct detection (total power radiometer) [15], [17], [18], direct conversion [19], [20], heterodyne detection [10], and super-regenerative reception [21], [22]. Key parameters of imaging receiver are NEP, $\Delta T_{\min}$, and responsivity. NEP is defined as the input signal power that makes a SNR of unit in one hertz output bandwidth. Smaller NEP

means better sensitivity. ΔT_{min} describes the change in temperature of a thermal source required to produce post detection SNR of unit [23]. Responsivity is the ratio of output voltage divided by input power. Figure 1.7 illustrates the NEP and power consumption of the state-of-the-art mm-wave imaging receivers. As shown in Figure 1.7, if NEP of 10 fW/Hz$^{0.5}$ is required, the power consumption of imaging receiver (per pixel) is quite large, which poses great challenge on the thermal dissipation issue when integrated in a large-size focal plane array (FPA).

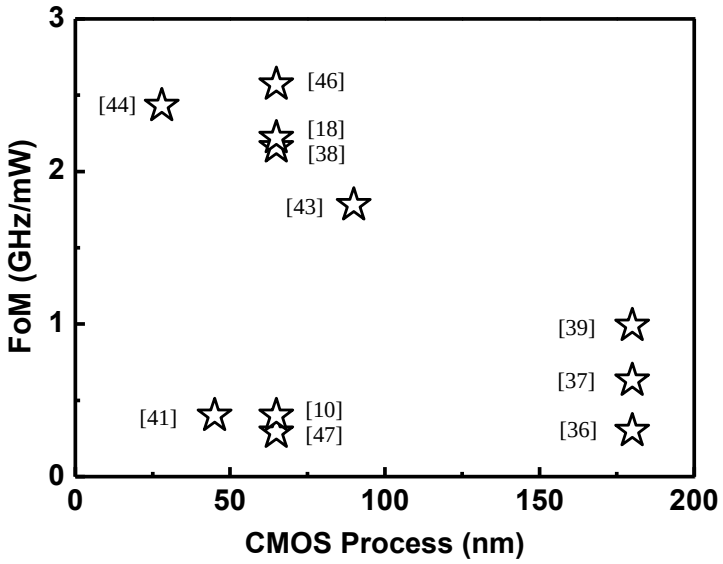


Figure 1.8 FoM of the state-of-the-art mm-wave LNAs in CMOS.

As the first amplification stage of imaging receiver, LNA is the key building block. High power gain and wide bandwidth will greatly improve the radiometer resolution [24]. Figure 1.8 shows the comparison of the state-of-the-art mm-wave

LNA in different CMOS processes. The adopted FoM takes the power gain, 3-dB bandwidth, noise factor, and power consumption into account, defined as

$$FoM = \frac{Gain[\text{abs.}] \times BW[\text{GHz}]}{(F-1) \times P_{\text{DC}}[\text{mW}]}. \tag{1.2}$$

With the motivations discussed above, the goal of this dissertation is to design high sensitivity receiver with low power consumption in a 65-nm CMOS technology for mm-wave imaging applications. To begin with, different design techniques are explored to improve the power gain and bandwidth of LNA. Based on the proposed LNA, Dicke receiver with novel switching method is implemented. Sensitivity degradation due to the insertion loss of Dicke switch is eliminated, further improving the imaging performance. In addition, super-regenerative reception is also explored for mm-wave imaging application with ultra-low power and high radiometer resolution.

1.4 Major Contributions of the Dissertation

This research focuses on CMOS integrated circuits for mm-wave imaging applications, and there are four important contributions.

Firstly, gain-distribution technique is investigated and part peak-gain distribution is proposed in the design of a five-stage cascode LNA. If all peak gains locate at

the same frequency, the LNA exhibits very high gain but narrow bandwidth. When peak gains of the first four stages are fully distributed at different frequency points, a wideband gain response is achieved but with certain level of ripples. Alternatively, we partly distribute peak gains of the four stages at only two frequency points. The resonant frequencies of the first and fourth inter-stage matching networks are designed at lower frequency, while those of the other two stages are designed at upper frequency. As a result, it is much easier to achieve a flat gain response over a wide frequency range. Although the bandwidth is extended by distributing peak gains of the five-stage LNA, power consumption and silicon size are also increased due to many cascaded stages. In order to improve performance of LNAs under the constraint of power consumption and fabrication cost, a novel pole-converging technique is proposed.

Secondly, a novel pole-converging intra-stage bandwidth extension technique is proposed for wideband amplifiers. By employing gate-inductor gain-peaking and negative drain-source transformer-feedback techniques in intra-stages, the transfer function of each stage exhibits two dominant poles. By reducing the gap between the two poles with proper values of gate inductor and coupling coefficient, a flat gain-frequency response over an ultra-wide bandwidth is achieved. Since the gain is boosted in a passive way and stacked transformers are adopted, the 3-dB bandwidth is greatly extended without increasing power consumption and chip

area. Based on the pole-converging technique, a switchable dual-path LNA is proposed in the design of Dicke receivers.

Thirdly, a switchable dual-path LNA (SDP-LNA) is proposed in the design of a direct-detection Dicke receiver for mm-wave imaging systems. In traditional Dicke receivers, insertion loss of silicon-based mm-wave switches is unacceptably high, ~4-5 dB for CMOS switches, which directly degrades receiver sensitivity. System-level analysis indicates that 5-dB insertion loss prior to the LNA will degrade radiometer resolution by a factor of 3. In the proposed SDP-LNA-based Dicke receiver, the sensitivity degradation introduced by the insertion loss of Dicke switch is eliminated because of the internal switching of the SDP-LNA. Therefore, a high-sensitivity Dicke receiver for mm-wave imaging is obtained. Nevertheless, power consumption and chip size of the SDP-LNA-based Dicke receiver are quite large. In order to further reduce power consumption and fabrication cost, super-regenerative reception is explored.

Fourthly, a charge-accumulation technique is proposed in the design of super-regenerative receiver (SRR). Furthermore, a new power-injection method is adopted without loading the *LC*-tank of super-regenerative oscillator (SRO). Instead of directly detecting the oscillation buildup time (logarithmic mode) or peak amplitude (linear mode) of SRO, a charge-accumulation technique is proposed in the design of a 100-GHz linear-mode SRR. By accumulating the

output charge of peak detector, the output voltage of imaging receiver is greatly enhanced, leading to extremely high responsivity and sensitivity with ultra-low power consumption and small silicon size. Focal plane arrays using the implemented CA-SRR will significantly enhance sensitivity, reduce fabrication cost, and save system power consumption.

1.5 Organization of the Dissertation

The remainder of this dissertation is organized as follows:

Chapter 2 reports state-of-the-art wideband mm-wave LNAs, and presents two wideband LNAs in 65-nm CMOS for mm-wave imaging applications. The first one is a five-stage cascode LNA based on part peak-gain distribution technique. By distributing peak gains of first four stages at two frequency points, the LNA achieves a flat gain response over a wide bandwidth. The second one is a three-stage cascode LNA based on a novel pole-converging technique for intra-stage bandwidth extension. By employing gate-inductor gain-peaking and negative drain-source transformer-feedback techniques in intra-stages, transfer function of each stage exhibits two dominant poles, achieving a flat gain-frequency response over an ultra-wide bandwidth. The bandwidth is significantly extended by the proposed design technique without increasing power consumption and die size.

Chapter 3 reports the recent development of CMOS mm-wave imaging systems together with pros and cons of different architectures, and presents a novel direct-detection Dicke receiver with a SDP-LNA for mm-wave imaging systems. Pole-converging technique for intra-stage bandwidth extension is adopted in the design of the SDP-LNA. Based on the SDP-LNA, a direct-detection Dicke receiver is designed and implemented. Thanks to the internal switching of the SDP-LNA, sensitivity degradation due to the insertion loss of Dicke switch is eliminated, enhancing the sensitivity of imaging receiver.

Chapter 4 reports different topologies of SRR used for mm-wave imaging, and presents an ultra-low-power and low-cost mm-wave imaging receiver based on super-regenerative reception. A charge-accumulation technique is proposed in the design of super-regenerative imaging receiver. By accumulating the output charge of peak detector, the output voltage is greatly enhanced, leading to extremely high responsivity and sensitivity with ultra-low power consumption. The theory of super-regenerative reception, implementation of charge-accumulation super-regenerative receiver (CA-SRR), and experimental results are presented.

Finally, conclusions and recommendations for the future work are given in Chapter 5.

1.6 Summary

This chapter gives an introduction and overview of the whole dissertation. It starts with the research background, i.e. the promising applications of mm-waves and aggressive scaling of CMOS technology. Then, the topic of CMOS integrated circuits for mm-wave imaging applications is confirmed as my research focus. The approaches and challenges of CMOS mm-wave imaging are discussed, followed by the objectives and major contributions of this dissertation. Finally, the organization of the dissertation is reported.

Chapter 2

Wideband MM-Wave Low-Noise Amplifier

Due to exceedingly low received signal, wide bandwidth and high gain are significant for PMMW imaging systems to achieve high quality images. Unfortunately, the gain-bandwidth product in CMOS technology is quite limited compared to that of III-V technologies. To conquer this challenge, two bandwidth extension techniques for CMOS mm-wave LNAs are proposed in this chapter. One is part peak-gain distribution technique, and the other is a novel pole-converging technique for intra-stage bandwidth extension. Circuit analysis and design methodology are provided.

2.1 Background and Literature Review

With the aggressive scaling of CMOS technology in recent years, mm-wave CMOS circuits are greatly explored for many promising applications, such as wireless uncompressed HD-video streaming (W-HDMI) systems, automatic radars, ultra-high capacity E-band point-to-point links, and mm-wave imaging systems. As the first amplification stage in the receiver chain, LNA plays a critical role in determining the system SNR and link budget. The power gain of LNA must be high enough to enhance the received signal and minimize noise contributions of following stages. Besides, in wideband receivers, gain flatness facilitates roughly the same signal amplification in the whole spectrum and relaxes dynamic range requirement of ADCs in baseband [25]. Therefore, it is significant to achieve a wideband frequency response with high power gain and excellent gain flatness.

At mm-wave frequencies, conventional single-stage amplifiers exhibit relatively low power gain because of operating near the cut-off frequency f_T of transistors. Moreover, device parasitic effects and passive losses also increase with operation frequencies. Although overall gain can be enhanced by increasing the number of stages, power consumption is also increased greatly. Therefore, G_m-boosting techniques are developed to improve the gain of each single stage. The basic operation principle of G_m-boosting is increasing the voltage swing, v_{gs}, between

the gate and source of transistor in either active or passive way, as shown in Figure 2.1(a). Since the active implementation introduces more noise and consumes additional power, the passive method is more attractive for the realization of G_m-boosted LNA.

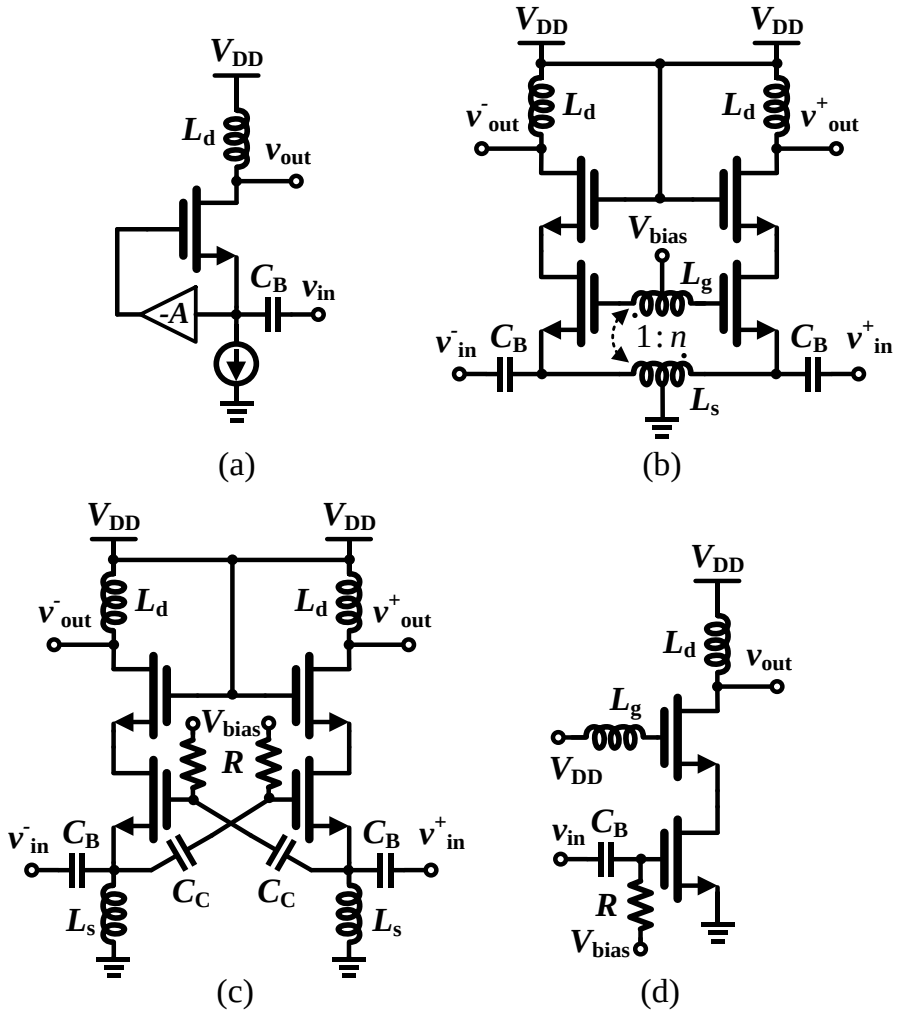


Figure 2.1 G_m-boosted LNA: (a) basic operation principle of G_m-boosting, (b) transformer-coupled G_m-boosting [26]**, (c) capacitor cross-coupling G_m-boosting** [27]**, (d) gate-inductor gain-peaking G_m-boosting** [25]**.**

There are several kinds of passive implementation for G_m-boosting in literature, such as transformer-coupled G_m-boosting [26], capacitor cross-coupling (CCC) [27], [28], and gate-inductor gain peaking [25], [29], as shown in Figure 2.1. The transformer-coupled G_m-boosting technique provides anti-phase operation between gate inductor and source inductor, leading to the increase of v_{gs}. However, it is limited by turn ratio of the transformer, which is usually less than three at mm-wave frequencies. Besides, the transformer is quite bulky, occupying large silicon area. The CCC is passive amplification and very suitable for differential LNAs. Compared to single-ended counterparts, differential LNAs consume twice power and silicon size. The amplification depends on the ratio between the cross-coupled capacitor and gate-source parasitic capacitor, and its value is lower than one [26]. On the contrary, G_m-boosting of gate-inductor gain-peaking technique can be very large, which is dependent on the value of gate inductor.

Besides the power gain, LNA's operating bandwidth is also an important parameter. For a total-power radiometer in imaging systems, when ignore the noise contribution introduced by the detector, the image quality is quantified by the minimum resolvable temperature, ΔT_{min}, which is defined as

$$\Delta T_{\min} = T_S \sqrt{\frac{1}{B\tau} + \left(\frac{\Delta G}{G}\right)^2} \tag{2.1}$$

where T_s is the system noise temperature, B is the RF front-end bandwidth, τ is the receiver's integration time, G is the overall gain of the receiver front-end, and ΔG is the root-mean-square (RMS) variation of G in the time domain [18], [24]. To achieve excellent thermal resolution, LNA must provide a stable high power gain over a wide frequency band. Besides, mm-wave cellular wireless networks with wide bandwidth have tremendous potential to provide huge capacity and data rates for cellular communications [1]. Furthermore, for FMCW radars, wider bandwidth leads to higher range resolution [30]. Therefore, wideband LNAs are greatly desired in these systems. Indeed, III-V compound semiconductor technologies have been the desirable platforms for wideband amplifiers with extremely high power gain and low noise figure at high frequencies when compared to their silicon counterparts [31]–[34]. However, CMOS technology demonstrates merits of overwhelmingly low cost, high yield, and high level of integration, which make it more attractive for the implementation of multi-antenna systems with complex digital circuitries [35].

In literature, distributed architecture and multi-stage architecture are two common topologies for broadband amplifiers. However, the former has drawbacks of high power consumption and large chip size, besides, extensive modeling and electromagnetic (EM) simulation are needed to achieve good performance [36]–[39]. For multi-stage amplifiers, bandwidth is limited by intrinsic capacitances of

transistors and other parasitic capacitances at the nodes of input, output, and inter-stages.

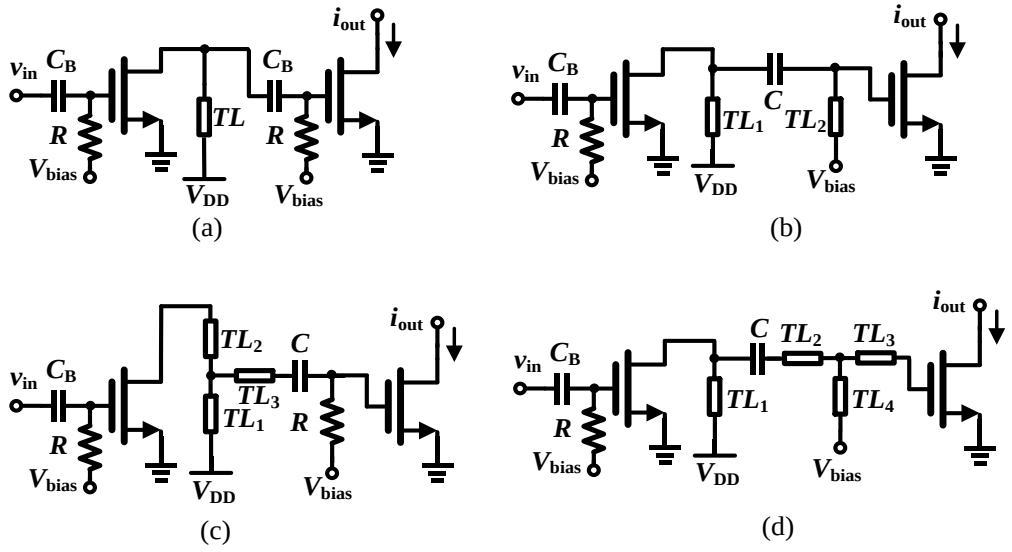


Figure 2.2 Inter-stage matching networks: (a) L-type, (b) π-type, (c) T-type, (d) combination of L-type and T-type.

To extend bandwidth of multi-stage amplifiers, different matching networks and peaking techniques are explored to achieve higher bandwidth extension ratio (BWER), which is defined as the ratio of 3-dB bandwidth to that of reference common-gate (CG) or common-source (CS) amplifier without peaking techniques [40]. Four topologies of inter-stage matching network are adopted to broaden the bandwidth, namely L-type [18], [41]–[43], π-type [44], T-type [24], [45], [46], and combination of different types [15], [47], as illustrated in Figure 2.2. By

combining L-type and T-type matching networks, the work in [47] demonstrated a wide 3-dB bandwidth of 21 GHz with peak gain of 14.8 dB in CMOS technology. More recently, one LNA in SiGe BiCMOS technology achieved 3-dB bandwidth over 30 GHz using a T-type matching network [24].

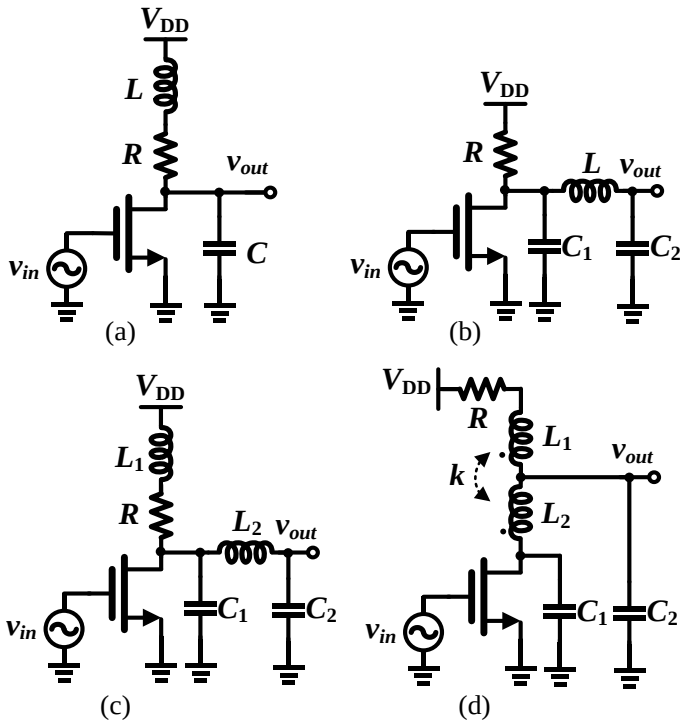


Figure 2.3 Bandwidth extension techniques [40]**: (a) shunt peaking, (b) series peaking, (c) shunt-series peaking, (d) T-coil peaking.**

On the one hand, complex matching networks provide wideband matching but introduce additional insertion loss and chip area. On the other hand, peaking techniques, such as shunt peaking, series peaking, shunt-series peaking, and T-

coil peaking, are highly relied on the ratio of drain capacitance to load capacitance, as shown in Figure 2.3. The ratio varies from 0.2 to 0.5 for CS amplifiers, depending on drive and load conditions. Thus, the theoretical BWER of these techniques is only 2 to 5 [33], [40]. Table 2-1 summarizes the performance of state-of-the-art wideband mm-wave LNAs.

Table 2-1 Performance summary of state-of-the-art wideband mm-wave LNAs

Reference	Technology	Topology	Gain (dB)	BW* (GHz)	NF (dB)	Power (mW)	Size (mm^2)
[45] MWCL′10	0.18-µm SiGe	2-stage cascode	14.5	14.5	6.9 - 8.0	37	0.41
[15] JSSC′11	0.18-µm SiGe	5-stage CE	19	19#	8.0 - 12#	63	1.00
[24] JSSC′13	0.13-µm SiGe	2-stage cascode	22.5	30	6.0 - 7.2#	52	0.52
			25	70#	6.2 - 9.0#	54	0.33
[36] JSSC′07	0.18-µm CMOS	Distributed	20	39.4	8.0 - 9.4	250	2.24
[37] TMTT′13	0.18-µm CMOS	Distributed	24	33	6.5 - 7.5	238	0.83
[38] TMTT′12	65-nm CMOS	Distributed	22	65	6.9 - 7.9	97	0.93
[39] IMS′15	0.18-µm CMOS	Distributed	25	34	6.5 - 8.0	176	0.86
[41] TMTT′12	45-nm SOI CMOS	3-stage CS	10.7	18	6.0 - 11	52	0.32
[42] JSSC′08	65-nm CMOS	3-stage cascode	13.5	20	6.4 - 9.0#	-	-
[43] EL′12	90-nm CMOS	3-stage cascode	14	23	4.8 - 7.0#	32	0.22
[18] JSSC′10	65-nm CMOS	5-stage cascode	27	13.5#	6.8 - 9.0#	36	-
[44] TMTT′15	28-nm CMOS	2-stage cascode	13.8	18	4.0 - 5.8	24	0.38
[46] IMS′12	65-nm CMOS	4-stage cascode	25.3	20#	6.0 - 8.3	48	0.25
[47] ISSCC′09	65-nm CMOS	4-stage CS	14.8	21	7.5 - 9.0#	86	0.33
[10] JSSC′11	65-nm CMOS	3-stage cascode	15	12	7.0 - 10#	42	-

* 3-dB bandwidth; # estimated value

In comparison, CG LNA presents high stability, linearity, and reverse isolation [48]. However, because of the difficulty in wideband noise matching, its NF performance is poorer than that of CS LNA. CS LNA has the drawback of poor reverse isolation at mm-wave frequencies due to parasitic drain-to-gate capacitance. The cascode topology is widely used because of high gain and reverse isolation, but it presents high power consumption. To achieve high-gain wideband LNAs, two bandwidth extension techniques are presented in following sections. One is based on part peak-gain distribution, and the other is based on a novel pole-converging technique. Circuit analysis and design methodology are also provided.

2.2 88.5–110 GHz LNA Based on Peak-Gain Distribution

This work presents a wideband mm-wave LNA in a 65-nm CMOS technology. Figure 2.4 shows the schematic of proposed five-stage cascode LNA with the gate width (W) and the number of fingers (N_f) of the transistor declared in the caption. By distributing peak gains of first four stages at two frequency points, the LNA achieves a flat gain response over a wide bandwidth.

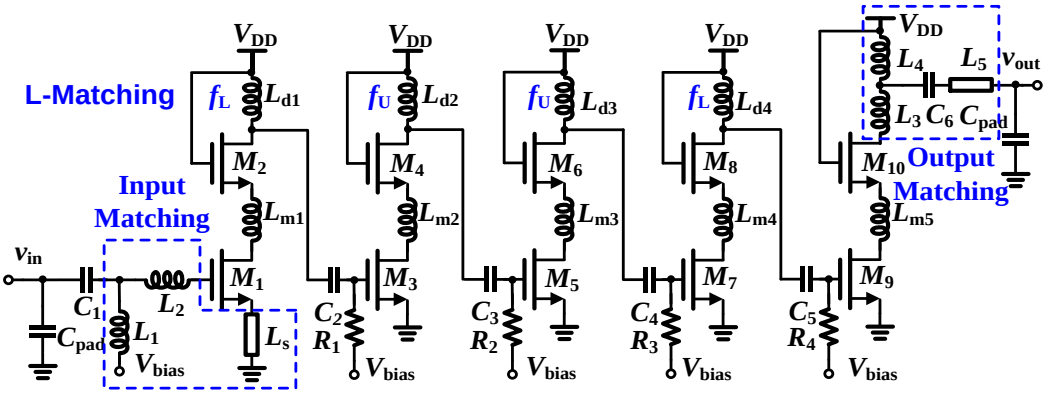


Figure 2.4 Schematic of the proposed wideband LNA, M_1-M_{10}: W=25 μm, N_f=25.

2.2.1 Peak-Gain Distribution

Figure 2.5 investigates the simulated AC gain responses in three different scenarios based on peak-gain distribution. If all peak gains locate at the same frequency, the LNA exhibits very high gain but narrow bandwidth, as shown in Figure 2.5(a). When peak gains of the first four stages are fully distributed at different frequency points, a wideband gain response is achieved with certain level of ripples, as illustrated in Figure 2.5(b). However, to minimize the ripples and maintain wide bandwidth, great efforts are needed to obtain the optimal values of peak gains and frequency points, which are quite complicated in design procedures.

Alternatively, we partly distribute peak gains of the first four stages at only two frequency points, as shown in Figure 2.5(c). The resonant frequencies of the first

and fourth inter-stage matching networks are designed at lower frequency f_L, while those of the other two stages are designed at upper frequency f_U. Considering the noise contribution of each stage and the mismatch between the two frequency points, we design the first stage at lower frequency with higher peak gain. Thus a flat overall gain response G_T is relatively easier to obtain over a wide frequency range with part peak-gain distribution. Compared to no distribution and full distribution, the part distribution provides the best performance in terms of the gain flatness and bandwidth, as illustrated in Figure 2.5(d).

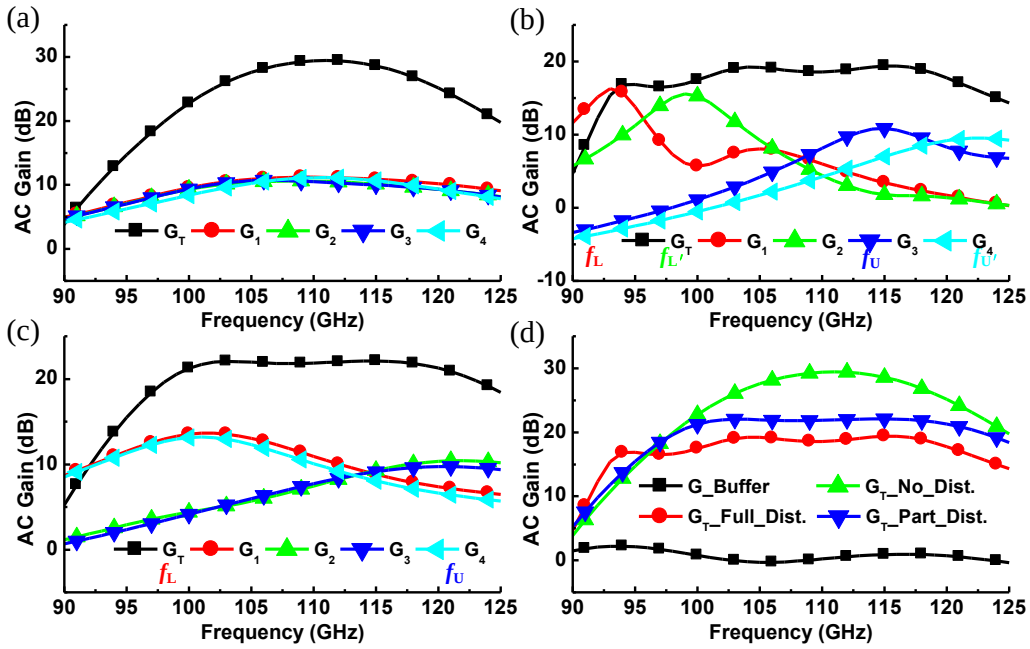


Figure 2.5 Simulation and comparison of AC gain responses in three different scenarios: (a) no distribution, (b) full distribution, (c) part distribution, (d) comparison of the overall AC gain responses.

2.2.2 L-Type Input Matching

In Figure 2.6, the L-type input matching network with its small-signal equivalent circuit is analyzed. At mm-wave frequencies, parasitic capacitance of testing pads C_{pad} must be designed as part of matching network. Based on the small-signal analysis, input admittance can be derived as

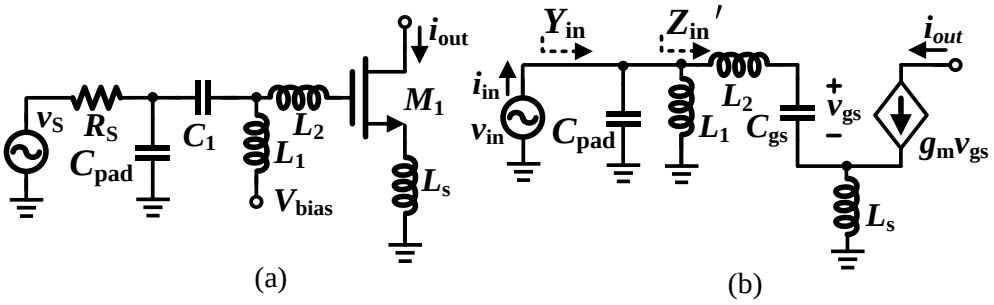


Figure 2.6 (a) Schematic of the input stage with pad capacitance. (b) Simplified small-signal equivalent circuit.

$$Y_{in} = \frac{1}{j\omega L_1} + j\omega C_{pad} + [Z_{in}']^{-1} = \frac{1}{j\omega L_1} + j\omega C' + \frac{1}{R'} \tag{2.2}$$

$$Z_{in}' = j\omega(L_2 + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{2.3}$$

$$C' = C_{pad} + \frac{C_{gs} - \omega^2 (L_2 + L_s) C_{gs}^{\ 2}}{[1 - \omega^2 (L_2 + L_s) C_{gs}]^2 + \omega^2 g_m^{\ 2} L_s^{\ 2}} \tag{2.4}$$

$$R' = \frac{[1-\omega^2(L_2+L_s)C_{gs}]^2}{\omega^2 g_m L_s C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{2.5}$$

where C_{gs} and g_m are the gate-source capacitance and trans-conductance of the MOS transistor, respectively, Z_{in}' is the input impedance of conventional inductive degeneration matching network, C′ is equivalent capacitance, and R' is equivalent resistance. For the conventional inductive degeneration matching network with the effect of C_{pad}, large L_2 and L_s are needed to cancel out C_{gs} and C_{pad}, resulting that C' equals to zero and R' equals to 50 Ω. However, by using L-type matching topology with source degeneration inductor L_s, the input matching network functions as a parallel circuit with C' and R', expressed in (2.4) and (2.5), respectively. The effect of C_{pad} is alleviated by L_1, which is connected to the matching network in parallel with C_{pad}. Thus C_{pad} and C_{gs} can be cancelled out by small values of L_1, L_2, and L_s, achieving simultaneous noise and impedance matching [42].

Table 2-2 Inductor values of input matching network at 100 GHz

Inductor	L_1 (pH)	L_2 (pH)	L_s (pH)
L-type matching	50	20	40
Conventional matching	-	150	100

Table 2-2 lists the inductances needed in the ideal case to achieve the same matching condition with the effect of parasitic pad capacitance, which is around 20 *f*F at 100 GHz. Figure 2.7 shows the simulated input matching conditions of L-type matching and conventional matching based on the inductances listed in Table 2-2. As evident in Figure 2.7, L-type input matching significantly reduces the inductance of matching inductors and thus the chip size.

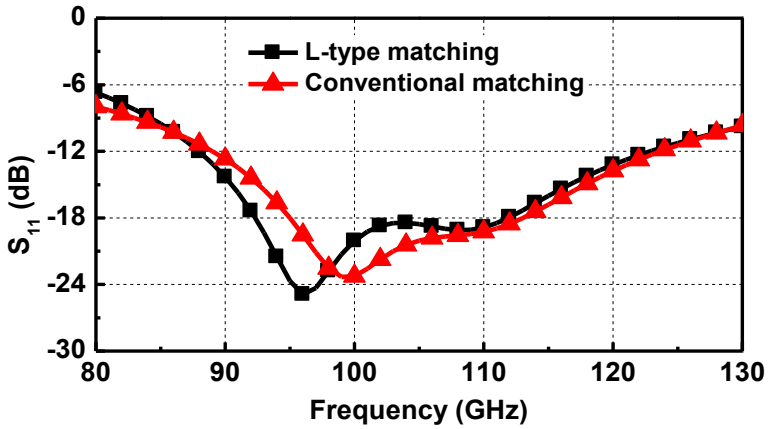


Figure 2.7 Simulated S_{11} of two matching topologies based on the inductances listed in Table 2-2.

2.2.3 Circuit Implementation

The schematic of the proposed wideband LNA is depicted in Figure 2.4. Double-sided gate contacts have been chosen to reduce the gate resistance, which is the limitation factor for the high-frequency gain and noise performance. The total width and number of fingers have been chosen as a tradeoff between maximum

available gain, minimum noise figure (NF) and power consumption of the cascode stage. Each stage adopts transistors with same size and bias current. The total transistor width is 25 μm with a finger number of 25. In each stage, series inductors $L_{m1\text{-}6}$ are added between CG and CS transistors to improve the f_T of CMOS cascode structure [49]. The input L-type matching network is optimized to transform the 50-Ω impedance at the input pad to the optimum noise source impedance at the first gain stage. L_{d1} and L_{d4} resonate with the parasitic capacitances at 100 GHz, while L_{d1} and L_{d4} resonate with the parasitic capacitances at 120 GHz, so that the peak gains of first four stages are distributed at two frequency point. The output stage adopts the T-type matching network to provide a wideband output matching, working as an output buffer. Custom designed inductors were developed in 3D EM simulator HFSS and adopted for the design and simulation of the LNA. The optimized inductor parameters at 100 GHz are listed in Table 2-3.

Table 2-3 Inductor parameters of the LNA at 100 GHz

@100GHz	L_s	L_1	L_2	L_3	L_4	L_5	$L_{m1\text{-}6}$	$L_{d1\&4}$	$L_{d2\&3}$
Ind. (pH)	24	40	25	59	48	14	95	55	35
Q	13	15	14	17	16	11	19	17	15

2.2.4 Experimental Results

The proposed wideband LNA was fabricated in GlobalFoundries 65-nm CMOS technology. The die occupies a silicon area of 0.66 mm × 0.44 mm including all pads with core circuit size of only 0.45 mm × 0.11 mm, as shown in Figure 2.8. At a supply voltage of 1.8 V, the LNA exhibits power consumption of 48.6 mW.

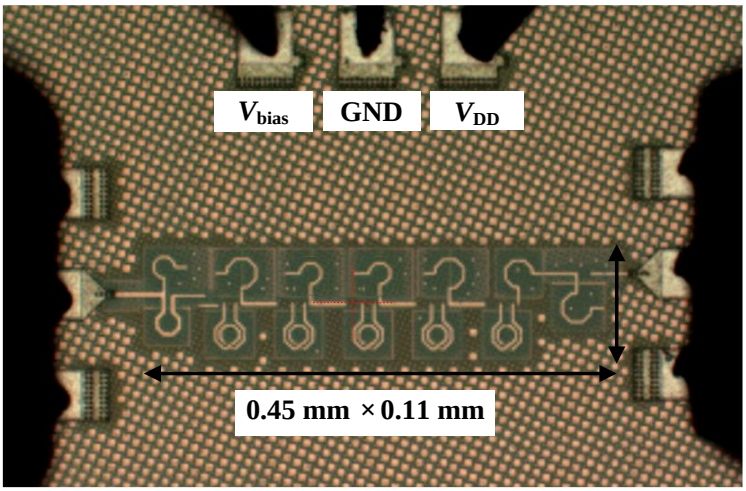


Figure 2.8 Die micrograph of the wideband LNA.

The LNA was measured through on-wafer testing by using Cascade Microtech Elite 300 probe station and Agilent N5247A PNA-X microwave network analyzer with N5256A mm-wave head controller, as demonstrated in Figure 2.9. The S-parameters of the LNA were measured up to 110 GHz due to the equipment limitation, and compared to simulated S-parameters in Figure 2.10. The measured

gain response shifts down by ~4 GHz and degrades by ~4 dB. It is mainly due to parasitic capacitances caused by dummy metal fills which were not fully considered in EM simulation. The LNA exhibits a very flat gain response with peak value of 16.7 dB at 104 GHz. The measured 3-dB bandwidth is from 88.5 GHz to 110 GHz that is limited by the measurement setup, but up to 114 GHz can be expected. The input return loss is better than 10 dB from 86 GHz to 105 GHz, while the output return loss is better than 10 dB from 78 GHz to 107 GHz. The measured reverse isolation is better than 50 dB in the whole W-band. The Rollett Stability factor K and Δ calculated from measured S-parameters are shown in Figure 2.11, which indicate that the proposed amplifier is unconditional stable.

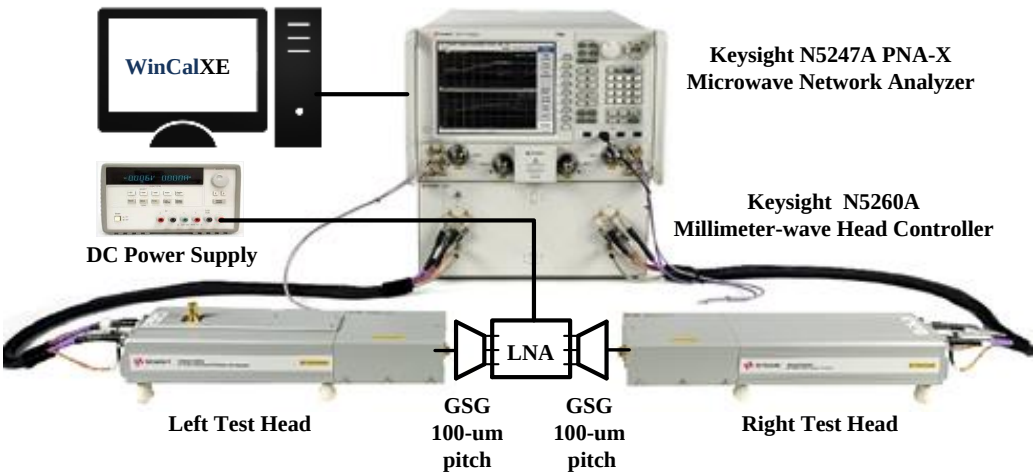


Figure 2.9 Setup for on-wafer S-parameters measurement.

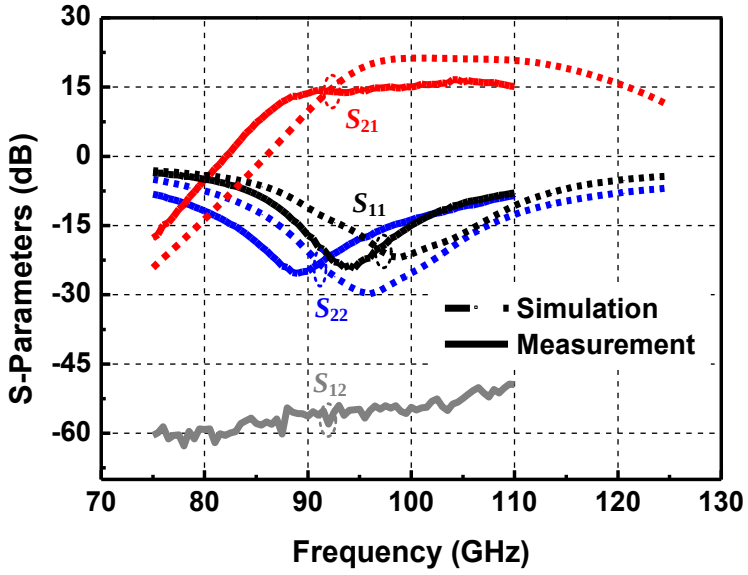


Figure 2.10 Simulated and measured S-parameters.

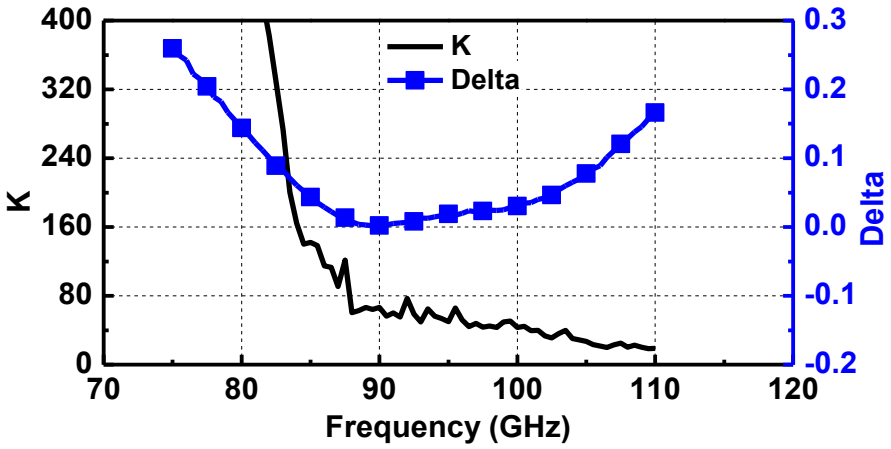


Figure 2.11 Measured stability factor *K* and Δ.

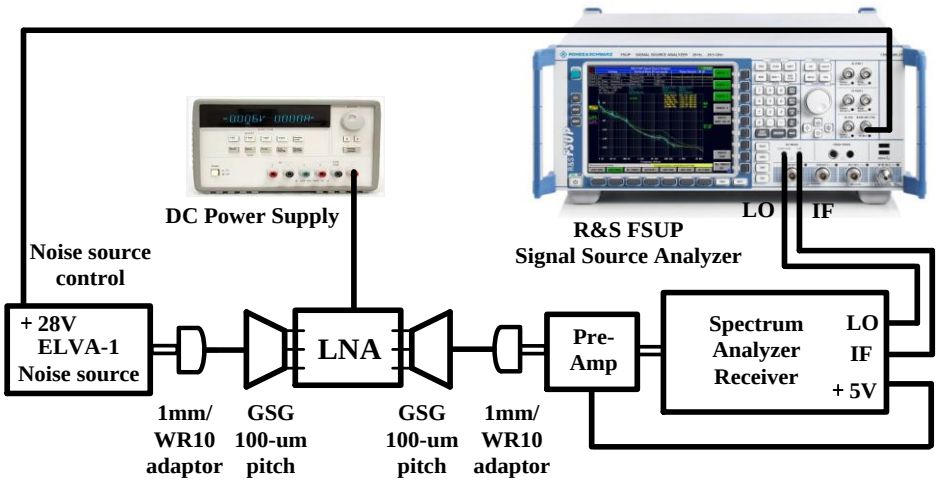


Figure 2.12 Measurement setup for the W-band noise figure measurement.

The setup for NF measurement is illustrated in Figure 2.12. This measurement setup utilizes Y-factor method through turning on and off the noise source, which delivers a uniform level of noise power spectral density with a typical excess noise ratio (ENR) of 12 dB within the full W-band. The setup consists of a W-band noise source, a W-band pre-amplifier, a spectrum analyzer receiver (SAR), and a FSUP signal source analyzer. The pre-amplifier is used to improve sensitivity level. The SAR down-converts W-band frequencies and converts waveguide interface to co-axial interface for LO and IF connections. The FSUP, equipped with LO/IF option for external mixer, provides a control voltage of 28 V to the noise source and measure the noise figure of the LNA. To obtain a more accurate NF, a 2nd stage calibration was performed to remove the noise figure of

the spectrum analyzer, and the average of 20 measurements was taken. Figure 2.13 shows the simulated and measured noise figures. The measured NF ranges from 7.2 dB to 9.0 dB in the 3-dB bandwidth with a minimum value of 7.2 dB at 104 GHz.

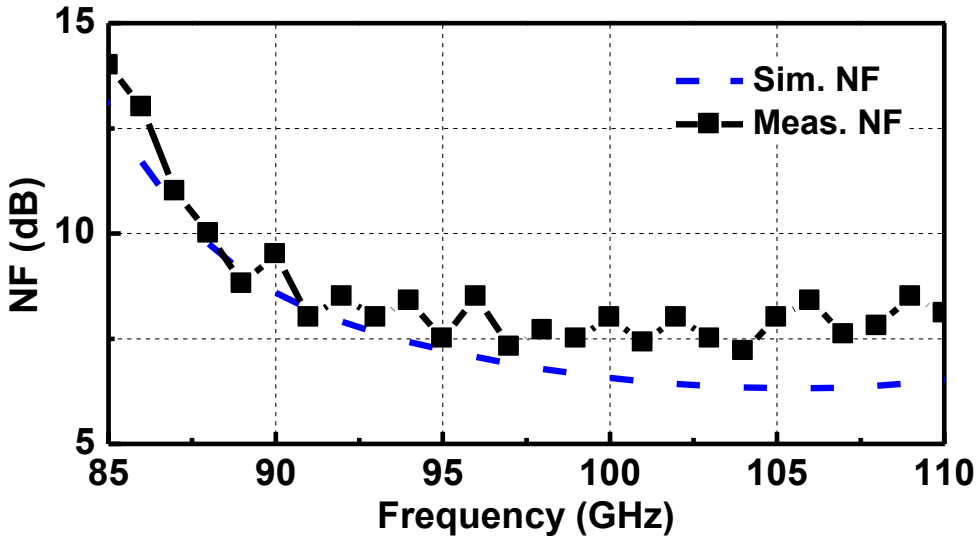


Figure 2.13 Simulated and measured noise figure.

Performance of the proposed wideband LNA is summarized and compared to state-of-the-art mm-wave wideband LNAs in Table 2-4. The fabricated LNA based on part peak-gain distribution exhibits peak gain of 16.7 dB at 104 GHz, minimum NF of 7.2 dB, and 3-dB bandwidth of 21.5 GHz. The LNA consumes DC power of 48.6 mW and occupies a compact core area of 0.05 mm^2.

Table 2-4 Performance summary and comparison to state-of-the-art wideband mm-wave LNAs

Ref.	Tech.	Top.	Gain (dB)	BW (GHz)	NF (dB)	Power (mW)	Area (mm^2)	FoM
[32] MWCL 2015	50-nm InGaAs mHEMT	5-stage CS	26[#]	57[#]	3.2-4.8[†]	24	2.00	23.5-43.5
[34] IMS 2014	50-nm GaAs mHEMT	3-stage CS	26[#]	62[#]	1.3-2.3[†]	45	3.62	39.4-78.8
[50] TMTT 2015	80-nm InP HEMT	3-stage CG	18	42	3-4[†]	12	0.41	18.4-27.9
[41] TMTT 2012	45-nm SOI CMOS	3-stage CS	10.7	18	6[*]	52	0.32	0.40
[44] TMTT 2015	28-nm CMOS	2-stage Casc.	13.8	18	4-6[†]	24	0.38	1.23-2.42
[10] JSSC 2011	65-nm CMOS	5-stage CS	15	12	7-10[#]	42	0.79	0.18-0.40
[51] MWCL 2012	65-nm CMOS	3-stage Casc.	18.9	12	6.1-7.8[†]	45	0.25	0.47-0.76
This Work	**65-nm CMOS**	**5-stage Casc.**	**16.7**	**21.5**	**7.2-9**	**48.6**	**0.29**	**0.44-0.71**

[#] estimated value from figures; [*] NF at 95 GHz; [†] NF within part range of the 3-dB bandwidth.

2.3 62.5-92.5 GHz LNA Based on Pole-Converging Technique

In this work, pole-converging technique for bandwidth extension in intra-stages of multi-stage amplifiers is proposed. By using gate-inductor gain-peaking and negative drain-source transformer-feedback techniques in intra-stages, transfer

function of each stage exhibits two dominant poles, demonstrating a flat gain-frequency response over an ultra-wide bandwidth. The analyses of pole-converging technique and negative drain-source transformer-feedback technique are provided. To verify the proposed design technique, a three-stage cascode LNA was designed and implemented in a 65-nm CMOS technology. The design procedure and experimental results are reported. The prototype demonstrates a flat high gain response with low NF over a broad bandwidth without increasing power consumption and die size.

2.3.1 Pole-Converging Technique

Gate-inductor gain-peaking technique is widely used to boost the power gain of amplifiers in literature [25], [29]. However, one significant merit of this technique was ignored in published works, i.e. introducing a second pole in transfer function, which can significantly extend the 3-dB bandwidth combined with our proposed negative drain-source transformer feedback. This phenomenon of frequency compensation is denominated as *pole converging*.

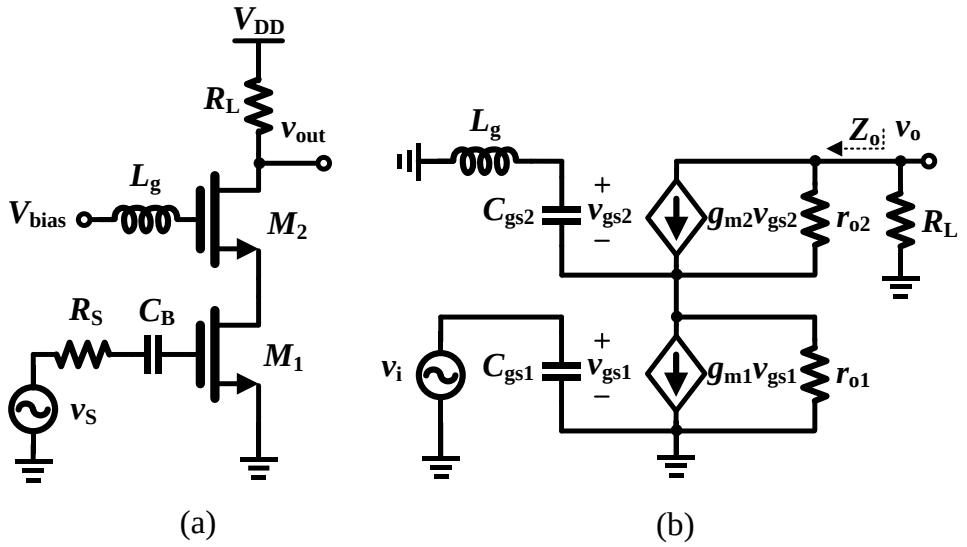


Figure 2.14 (a) Schematic of a cascode LNA with gate-inductor gain peaking, (b) Simplified small-signal equivalent circuit.

Figure 2.14 shows the G_m-boosting technique of gate-inductor gain peaking. Instead of connecting to the bias voltage directly, the gate terminal of M_2 is biased through a gate inductor L_g. Figure 2.14(b) illustrates the simplified small-signal equivalent circuit of the G_m-boosting cascode LNA. Because of the added L_g, the gate terminal of M_2 is no longer a perfect AC ground. Based on small-signal analysis, the voltage drop on the intrinsic capacitor C_{gs2} and real part of output impedance are expressed as (2.6) and (2.7), respectively. Since ω_0 is much larger than the frequencies of interest and inversely proportional to the value of L_g, v_{gs2} and Z_o increase with the gate inductor. Thus a positive feedback is introduced by the gate inductor, which results in the gain boosting of the cascode LNA.

However, the value of L_g cannot be larger than $1/\omega^2 C_{gs2}$, otherwise, the real part of output impedance will become negative, leading to stability issue.

$$v_{gs2}(\omega) = \frac{g_{m1} r_{o1} R_A v_{in}}{R_B\left(1 - \frac{\omega^2}{\omega_0^{\,2}}\right) + R_C + j\omega R_A \tau_0} \tag{2.6}$$

$$\mathrm{Re}[Z_o] = r_{o2} + \frac{r_{o1}\left(g_{m2} r_{o2} + 1\right)\left(1 - \frac{\omega^2}{\omega_0^{\,2}}\right)}{\left(1 - \frac{\omega^2}{\omega_0^{\,2}}\right)^2 + \left(\omega C_{gs2}\right)^2} \approx \frac{R_C}{1 - \frac{\omega^2}{\omega_0^{\,2}}} \tag{2.7}$$

$$\frac{v_o(s)}{v_i(s)} = -\frac{g_{m1} r_{o1} R_L\left(g_{m2} r_{o2} + 1 + \frac{s^2}{\omega_0^{\,2}}\right)}{R_B \frac{s^2}{\omega_0^{\,2}} + R_A \tau_0 s + R_B + R_C} \tag{2.8}$$

$$p_1 = -\frac{1}{2R_B}\left(R_A \tau_0 \omega_0^{\,2} - \omega_0 \sqrt{R_A^{\,2} \tau_0^{\,2} \omega_0^{\,2} - 4R_B^{\,2} - 4R_B R_C}\right) \tag{2.9}$$

$$p_2 = -\frac{1}{2R_B}\left(R_A \tau_0 \omega_0^{\,2} + \omega_0 \sqrt{R_A^{\,2} \tau_0^{\,2} \omega_0^{\,2} - 4R_B^{\,2} - 4R_B R_C}\right) \tag{2.10}$$

$$\frac{v_o'(s)}{v_i(s)} = -\frac{g_{m1} r_{o1} R_L\left(g_{m2} r_{o2} + 1\right)}{R_A \tau_0 s + R_B + R_C} \tag{2.11}$$

$$p_0 = \frac{R_B + R_C}{R_A \tau_0} \tag{2.12}$$

where,

$$R_A = r_{o2} + R_L \tag{2.13}$$

$$R_B = r_{o1} + r_{o2} + R_L \tag{2.14}$$

$$R_C = g_{m2} r_{o1} r_{o2} \tag{2.15}$$

$$\tau_0 = r_{o1} C_{gs2} \tag{2.16}$$

$$\omega_0 = 1/\sqrt{L_g C_{gs2}} \tag{2.17}$$

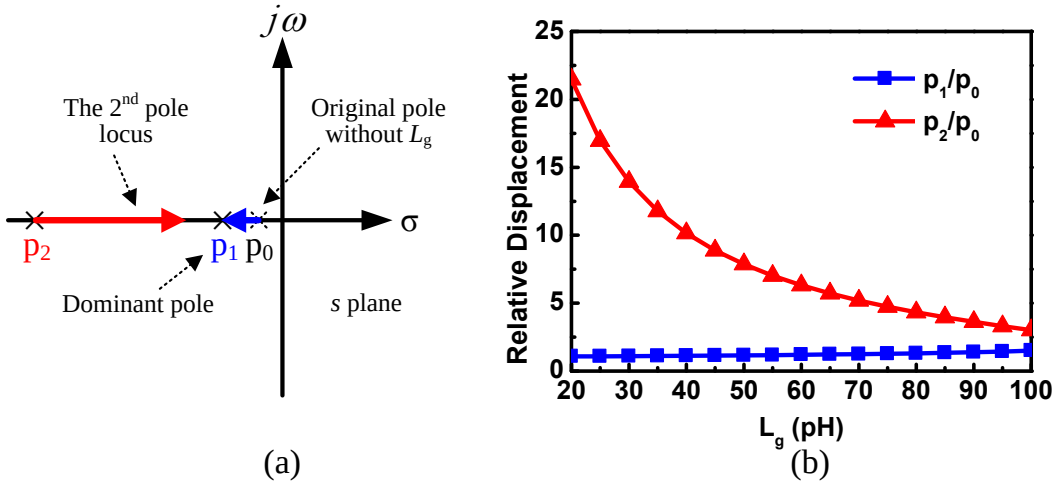
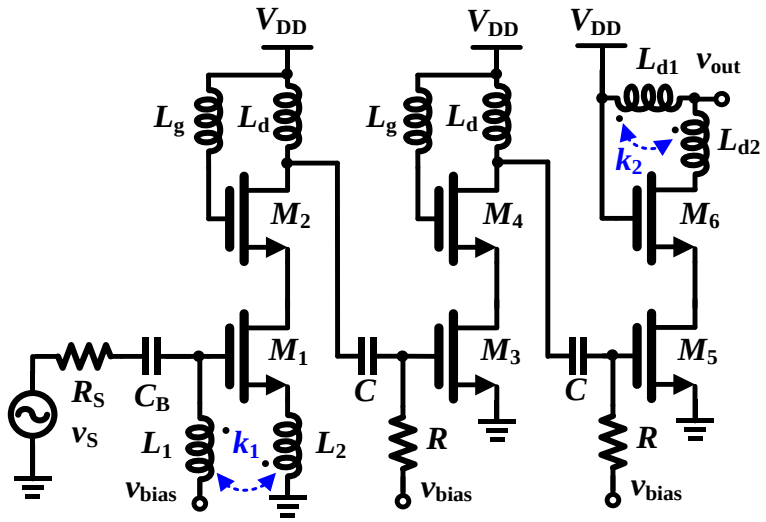


Figure 2.15 Demonstration of the pole converging: (a) locus of the second pole as gate inductor varies, (b) calculated relative displacement of two poles as gate inductor varies ,when $g_{m1} = g_{m2} = 25$ mS, $r_{o1} = r_{o2} = 400$ Ω, $C_{gs1} = C_{gs2} = 15$ *f*F, $R_L = 1$ kΩ.

In addition to the benefit of gain boosting, the gate-inductor gain-peaking technique also introduces a second dominant pole in the transfer function, which is a significant merit but ignored in literature. Based on the small-signal equivalent circuit shown in Figure 2.14(b), the transfer function of the cascode

LNA is derived as (2.8). From the second-order polynomial in the denominator of (2.8), two poles are derived as (2.9) and (2.10), respectively. An interesting phenomenon, *pole converging*, can be seen in examining (2.9) and (2.10) as gate inductor increases. Note that p_2 is directly dependent on ω_0, in other words, it is inversely proportional to L_g, while the dominant pole p_1 has very weak correlation with L_g. When the gate inductor is removed, the transfer function is simplified as (2.11) with single original pole p_0, expressed as (2.12). With the increasing of the gate inductor, the non-dominant pole p_2 is pushed towards to p_1 and finally becomes the second dominant pole. The mechanism of pole converging is illustrated in Figure 2.15(a), and Figure 2.15(b) demonstrates the relative displacement of p_1 and p_2 as L_g increases.



M_1-M_6	25 μm
R	20 kΩ
C	150 *f*F
L_1	50 pH
L_2	30 pH
L_d	70 pH
L_{d1}	50 pH
L_{d2}	80 pH
k_1	0.4
k_2	0.5

Figure 2.16 Schematic of the three-stage LNA based on pole-converging technique.

To verify the theoretical analysis of pole converging, a three-stage cascode LNA with the gate-inductor gain-peaking technique is simulated using Cadence Virtuoso, as shown in Figure 2.16. The input stage with shunt-series feedback exhibits wideband input matching and the last stage with asymmetric T-coil peaking works as a wideband output buffer. Figure 2.17 illustrates the simulated gain-frequency responses as the gate inductor varies. As can be seen in Figure 2.17, the simulated pole-converging tendency exhibits good agreement with the numeric calculations shown in Figure 2.15(b). By exploiting the pole-converging technique, the bandwidth of amplifiers can be significantly extended if the gain at the dominant pole is restrained while that at the second pole is enhanced.

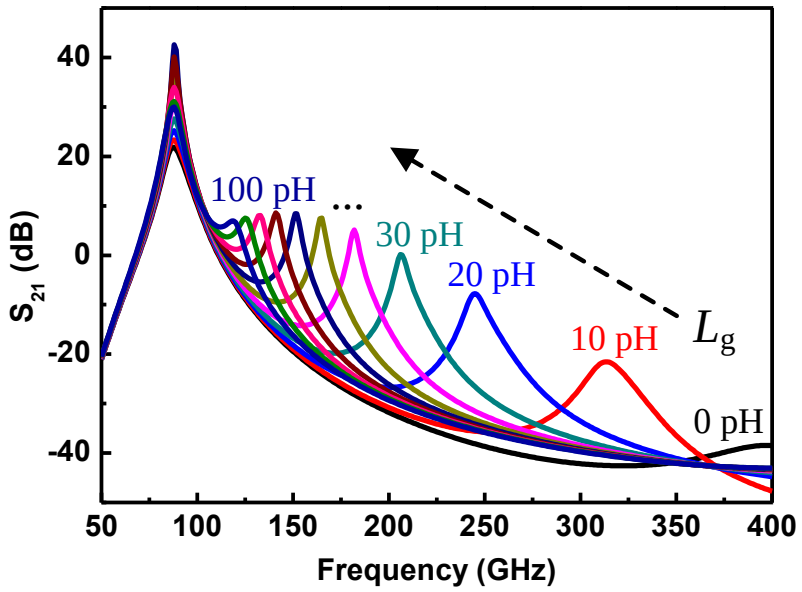
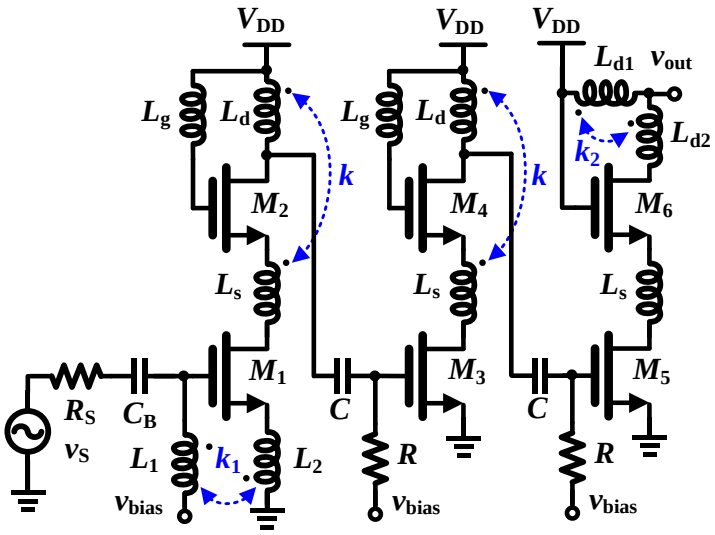


Figure 2.17 Simulated pole converging of the three-stage LNA as gate inductor varies.

2.3.2 Negative Drain-Source Transformer Feedback

As previously discussed, only when the gain at the dominant pole is restrained and that at the second pole is enhanced will the cascode LNA with gate-inductor gain peaking achieve a flat gain-frequency response over a broad bandwidth. In literature, transformer feedback is extensively used for the design of wideband amplifiers. Based on different configurations, this technique can achieve various benefits such as neutralization [52], transconductance enhancement [26], wideband matching [42], [53], noise cancellation [53], and bandwidth extension [33], [40]. Nevertheless, negative transformer feedback has an inevitable drawback of gain reducing in almost direct proportion to other benefits achieved, which actually can improve the gain-frequency response of the gain-peaking cascode LNA. Therefore, a negative drain-source transformer feedback is introduced through magnetically coupling the drain inductor and source inductor of the CG amplifier in the cascode stage, as shown in Figure 2.18. The source inductor L_s tunes out the parasitic gate-source and gate-drain capacitances of the CG and CS transistors, respectively, which leads to higher f_T of cascode structure, improving the performance of cascode amplifiers at mm-wave frequencies [49]. The drain inductor L_d, as a shunt-peaking inductor itself, leads to more initial charging current to the load capacitor of next stage by delaying current flow to resistive branch. Besides, the transformer introduces a negative feedback current

into L_d through magnetic coupling. Thus, the charging process of the load capacitor becomes much faster, which further extends the 3-dB bandwidth.



M_1-M_6	25 µm
R	20 kΩ
C	150 *f*F
L_1	50 pH
L_2	30 pH
L_{d1}	50 pH
L_{d2}	80 pH
k_1	0.4
k_2	0.5

Figure 2.18 Schematic of the three-stage LNA with gate-inductor gain peaking and negative transformer feedback.

However, the theoretical analysis of gain-frequency response is quite tough because of many energy storage elements, and the numerical result is too complicated to provide any circuit design insights. *Zero-value time constant analysis* has been developed to convey the design insight of intricate circuits [54]. Unfortunately, this approximate method is only suitable for circuits with one dominant pole, which is not the case in the proposed design methodology. Therefore, simulation results of the three-stage LNA are used to illustrate the pole converging and the benefits of the proposed negative transformer feedback.

To investigate the effects on the gain-frequency responses from the negative transformer feedback, various values of magnetic coupling coefficient k , drain inductor L_d, and source inductor L_s are examined in the simulation, as shown in Figure 2.19 and Figure 2.20. As expected, with the increasing of k, the gain at the first pole is reduced, and most importantly the gain at the second pole is significantly enhanced.

Figure 2.19(a) shows the gain-frequency responses when L_g = 40 pH. Since the gate inductor is not large enough, the second pole is far away from the dominant pole. Thus, strong coupling is required to enhance the gain at the second pole. Nevertheless, it is difficult to achieve high magnetic coupling coefficient at mm-wave frequencies for on-chip transformers. Besides, flat gain-frequency response can hardly be achieved if two poles are far away from each other. However, when the gate inductor is increased to 90 pH, narrowing the gap between the second pole and the dominant pole, a flat wideband gain-frequency response is presented with a reasonable value of coupling coefficient (k = 0.4). Therefore, the gate inductor L_g, which boosts the G_m of CG transistor, provides an additional design flexibility to adjust the power gain, bandwidth, and gain-flatness. Figure 2.20 illustrates the frequency responses with different values of L_d and L_s. Compared to k, L_d and L_s have few impacts on the gain-frequency response, which actually offers a design freedom to obtain optimal k by changing L_d or L_s.

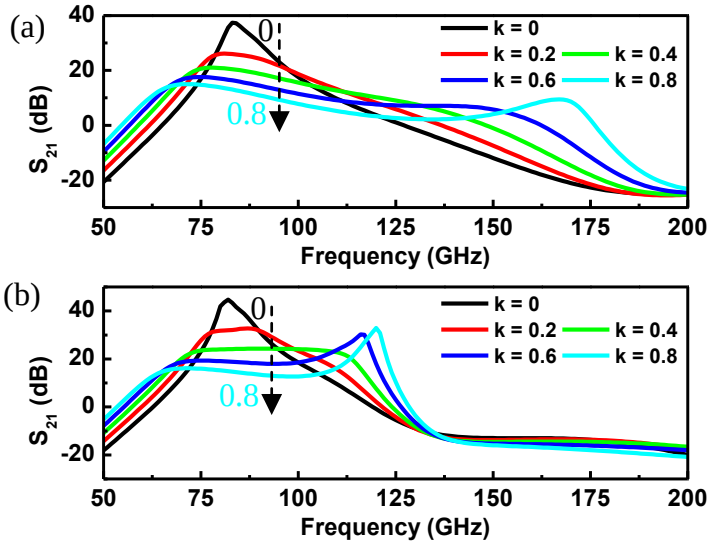


Figure 2.19 Gain-frequency responses as the magnetic coupling coefficient *k* varies with L_d = 70 pH and L_s = 100 pH: (a) L_g = 40 pH, (b) L_g = 90 pH.

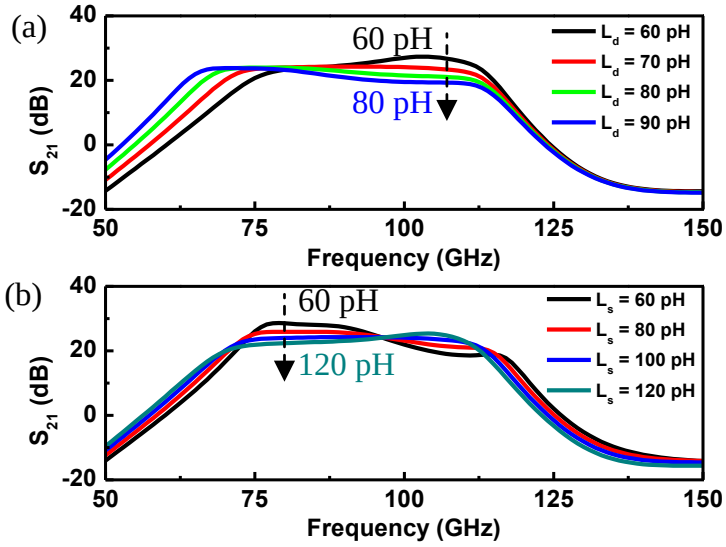


Figure 2.20 Gain-frequency responses as: (a) drain inductor L_d varies (when L_g = 90 pH, L_s = 100 pH, and *k* = 0.5), (b) source inductor L_s varies (when L_g = 90 pH, L_d = 70 pH, and *k* = 0.5).

2.3.3 Wideband Input Matching

At mm-wave frequencies, the parasitic pad capacitance C_{pad} reduces the matching bandwidth of conventional source degeneration matching network by introducing an additional parallel resonant circuit at the input. Thus, C_{pad} must be designed as part of the matching network. By using a shunt-series feedback, C_{pad} and the input capacitance of the transistor can be simultaneously compensated over a wide bandwidth [42].

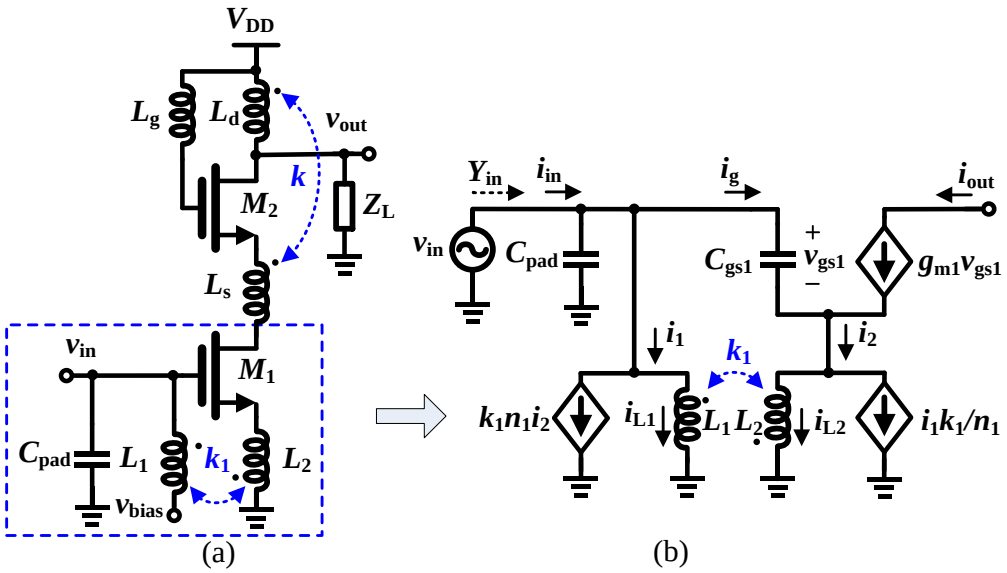


Figure 2.21 (a) Input stage of the cascode LNA with shunt-series feedback, (b) Simplified small-signal equivalent circuit of the common-source amplifier.

Figure 2.21 shows the input stage of the cascode LNA with shunt-series transformer feedback and the simplified small-signal equivalent circuit of the CS

amplifier. Based on small-signal analysis, the input admittance can be derived as (2.18), where n_1 is the turns ratio between L_2 and L_1. As can be seen in (2.18), C_{pad} is absorbed into the input capacitance of M_1, forming one parallel resonant circuit with L_1. The simulated effects on input matching from k_1 and L_1 are illustrated in Figure 2.22(a) and Figure 2.22(b), respectively.

$$Y_{in}(s) = sC_{pad} + \frac{1}{sL_1} + \frac{\frac{k_1}{n_1}\left(1+\frac{k_1}{n_1}\right)g_{m1} + \left(1+\frac{k_1}{n_1}\right)^2 sC_{gs1}}{1+(1-k_1^2)sL_2g_{m1} + (1-k_1^2)s^2L_2C_{gs1}}$$
$$\approx \frac{k_1}{n_1}\left(1+\frac{k_1}{n_1}\right)g_{m1} + \frac{1}{sL_1} + s\left[C_{pad} + \left(1+\frac{k_1}{n_1}\right)^2 C_{gs1}\right] \quad (2.18)$$

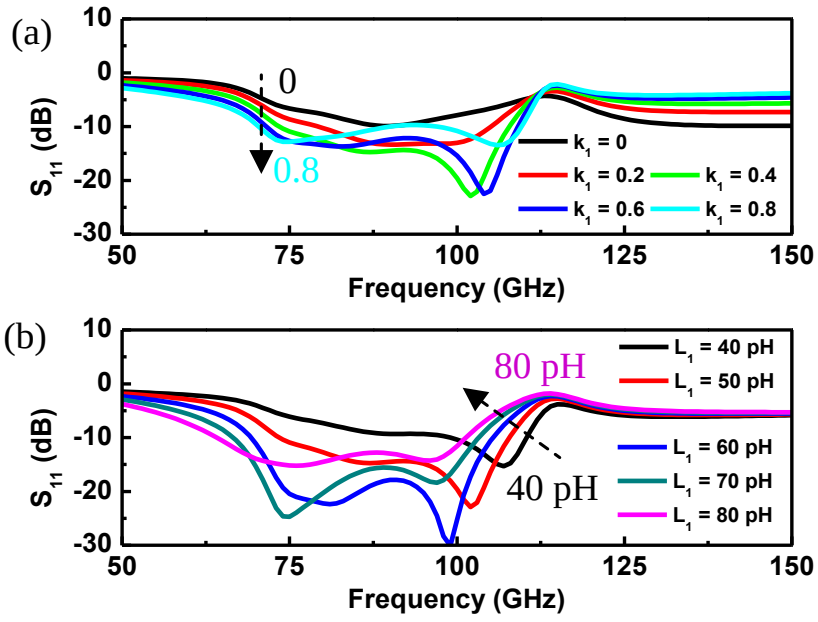


Figure 2.22 Simulated input matching: (a) as k_1 varies (when L_1 = 50 pH, L_2 = 30 pH, L_d = 70 pH, L_s = 100 pH, L_g = 90 pH, and k = 0.5), (b) as L_1 varies (when L_2 = 30 pH, L_d = 70 pH, L_s = 100 pH, L_g = 90 pH, k = 0.5, and k_1 = 0.4).

To analyze the impacts on the input matching from the gate inductor and the drain-source transformer, further analysis about the input stage of the three-stage cascode LNA will now be provided. As shown in Figure 2.23, the shunt-series transformer feedback of M_1 itself provides a wideband input matching, but the load impedance is affected by the input impedance of the CG amplifier as the magnetic coupling coefficient varies. For the sake of simplicity, only the input impedance of the CG amplifier is mathematically analyzed. Based on the small-signal model shown in Figure 2.23(b), the input impedance can be derived as (2.19).

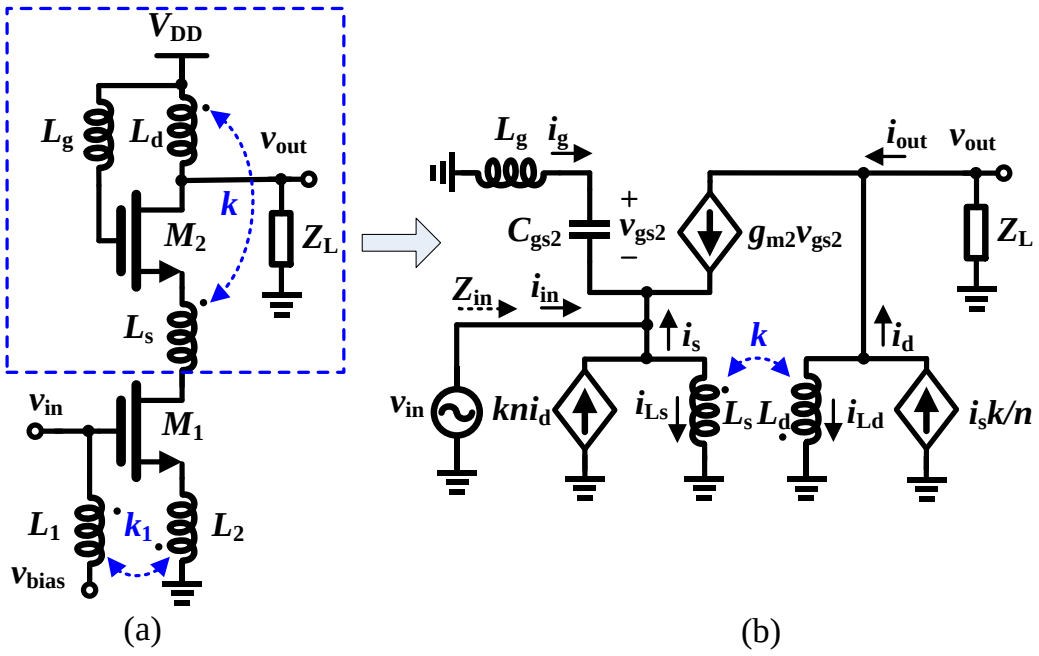


Figure 2.23 (a) Input stage of the cascode LNA with shunt-series feedback, (b) Simplified small-signal equivalent circuit of the common-gate amplifier.

$$Z_{in}(s)=\left[\beta g_{m2}+\beta C_{gs2}+\frac{1}{sL_s}+\frac{\beta kn}{1-k^2}\cdot\frac{g_{m2}Z_L}{(sL_d+Z_L)}\right]^{-1} \tag{2.19}$$

$$Z_{in}^{'}(s)=\left[\beta g_{m2}+\beta C_{gs2}+\frac{1}{sL_s}\right]^{-1} \tag{2.20}$$

$$\beta=\frac{1}{1+s^2L_gC_{gs2}} \tag{2.21}$$

$$n=\sqrt{L_d/L_s} \tag{2.22}$$

where β is the G_m-boosting coefficient, n is the turn ratio of the drain-source transformer, and Z_L is the load impedance including the parasitic inductance of interconnections and the load capacitor from the next stage. As can be seen in (2.19), magnetic coupling introduces additional zeros in the fourth term, thus the input impedance bandwidth is enlarged. However, when k changes to zero, the input impedance turns out to be (2.20) and the bandwidth is reduced. As illustrated in Figure 2.24(a), with the increasing of k, matching bandwidth becomes much better than that of the amplifier without magnetic coupling. However, if the magnetic coupling becomes too strong, the negative transformer feedback may make the amplifier oscillate at the second pole. Therefore, cares should be taken when using this transformer feedback to avoid unstable operation.

Further to the magnetic coupling coefficient, the G_m-boosting coefficient β also exhibits great effects on the input matching. Note that the gate inductor boosts not

only the effective transconductance of M_2 but also effective gate-source capacitance. Due to the boosted effective gate-source capacitance, the charging process becomes much slower. Thus the second pole is pushed to lower frequency with few effects on the first dominant pole, as illustrated in Figure 2.17. As a result, the input matching bandwidth is reduced, as shown in Figure 2.24(b). In brief, gate inductor enhances the power gain but reduces the input matching bandwidth; nevertheless, the bandwidth degeneration is compensated by the drain-source transformer feedback to some extent.

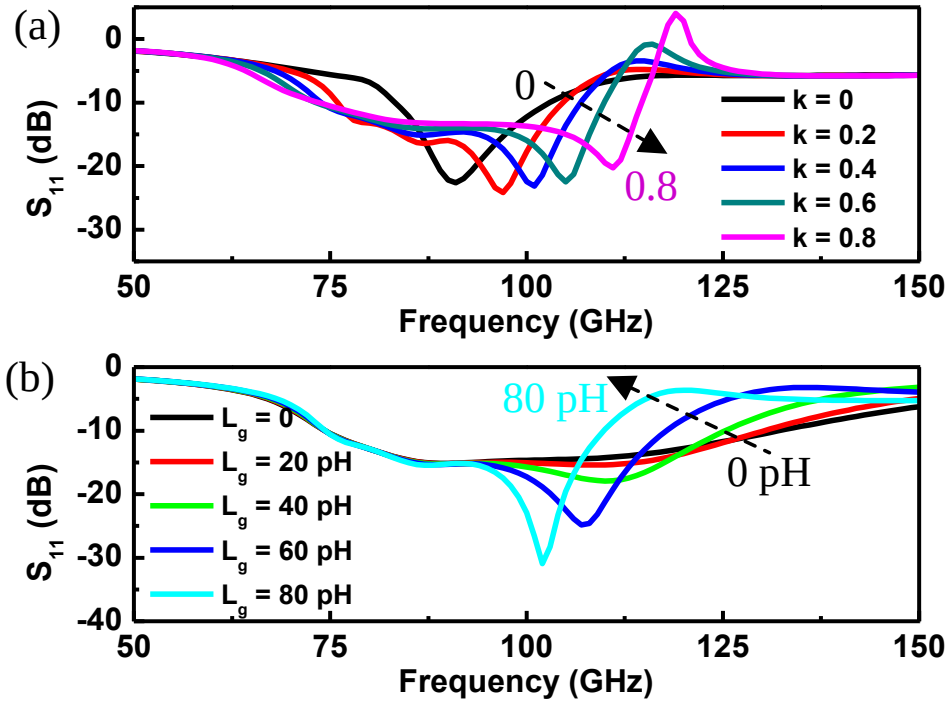


Figure 2.24 Simulated input matching: (a) as the magnetic coupling coefficient *k* varies (when L_d = 70 pH, L_s = 100 pH, and L_g = 90 pH), (b) as the gate inductor L_g varies (when L_d = 70 pH, L_s = 100 pH, and *k* = 0.4).

2.3.4 Design Methodology and Circuit Implementation

The presented pole-converging intra-stage bandwidth extension technique can be used to extend the bandwidth of multi-stage amplifiers in the common-gate or cascode topology. Compared to CG amplifiers, cascode amplifiers provide better reverse isolation, higher power gain, and simultaneous noise and power matching over a wideband bandwidth. A design methodology has been developed for the implementation of a CMOS cascode LNA based on the pole-converging technique, as shown in Figure 2.21(a).

Step 1: Choose the minimum length to maximize power gain and set the bias to the optimum NF_{MIN} current density ($J_{OPT} \approx 0.15$mA/μm) to minimize transistor noise.

Step 2: Choose the optimal W_f to minimize NF_{MIN}. For 65/90-nm CMOS, W_f is 0.7 - 1.5 μm [55]. Finger width of 1 μm is used for this design.

Setp 3: Choose the number of fingers (N_f) with respect to the current consumption specification.

Step 4: Find the best value of L_s for the cascode by plotting the f_T of the cascode versus L_s through simulation under the condition of no drain-source magnetic coupling ($k = 0$). Note that the value of L_s scales with N_f^{-1}.

Step 5: Based on (2.18), estimate the value of L_1 assuming that $k_1 = 0.5$ and $n_1 = 1$.

Step 6: Find the best value of L_2 by plotting the S_{11} of the cascode versus L_2 through simulation. And optimize the value of L_1.

Step 7: Design the shunt-series transformer with the optimized L_1 and L_2.

Step 8: Find the best value of L_d to maximize the power gain at frequencies of interest under the condition of no drain-source magnetic coupling ($k = 0$).

Step 9: Design the drain-source transformer with maximum coupling coefficient based on the values of L_s and L_d achieved in Step 4 and Step 8, respectively.

Step 10: Add the gate inductor L_g to boost the power gain and introduce the second dominant pole in the transfer function. Optimize the value of L_g to achieve a flat gain response over a broad bandwidth through simulation.

Step 11: Return to Step 6 and Step 7 to optimize the shunt-series transformer to improve the input matching with the consideration of effects from the Step 9 and Step 10.

Step 12: Optimize the biasing voltage, and make a trade-off between minimizing the noise figure and maximizing the power gain.

Step 13: After the layout and parasitic parameters extraction, repeat Step 4 to Step 12.

Following this design methodology, a three-stage cascode LNA based on the proposed pole-converging technique has been implemented in GlobalFoundries 65-nm CMOS technology. As shown in Figure 2.18, the input stage adopts shunt-series feedback to provide wideband input matching and the last stage with asymmetric T-coil peaking works as a wideband output buffer. The parasitic capacitances of testing pads are designed as part of the input and output matching networks. The gate-inductor gain-peaking and negative drain-source transformer-

feedback techniques for intra-stage bandwidth extension are implemented in the first two stages, and L-type inter-stage matching network is adopted. The transformers used for shunt-series feedback and T-coil peaking are implemented in a planar topology for medium magnetic coupling coefficient; while the drain-source transformer is designed in a stacked topology for high magnetic coupling coefficient and small footprint.

All the inductors, transformers, and testing pads were custom designed with interconnections and simulated using the 3D EM simulator ANSYS HFSS. Table 2-5 lists the optimized parameters of circuit elements in the three-stage cascode LNA. All the transistors have finger width of 1 μm with the minimum gate length, which results in a good compromise between gate-resistance reducing and f_T degradation due to gate-bulk capacitance.

Table 2-5 Design parameters of the three-stage cascode LNA

@80GHz	L_1	L_2	L_3	L_g	L_s	L_d	L_{d1}	L_{d2}
Ind. (pH)	45	27	89	71	108	55	39	63
Q	10.3	13.7	12.1	13.3	15.1	9.6	12.6	13.2
	k	k_1	k_2	R	C	M_1-M_6	V_{DD}	V_{bias}
	0.43	0.41	0.31	18 kΩ	176 *f*F	25 μm	1.8 V	0.8 V

2.3.5 Experimental Results

The proposed broadband LNA was fabricated in GlobalFoundries 65-nm CMOS technology. Figure 2.25 shows the die micrograph of the broadband LNA. This amplifier occupies silicon area of 0.24 mm^2 including all the pads with a core circuit size of only 0.06 mm^2. The LNA draws 15.2 mA from a 1.8-V supply for high power gain (hereinafter, "high-gain mode"), while it has a power consumption of 12 mW under the nominal supply voltage of 1.2 V for low-power operation (hereinafter, "low-power mode").

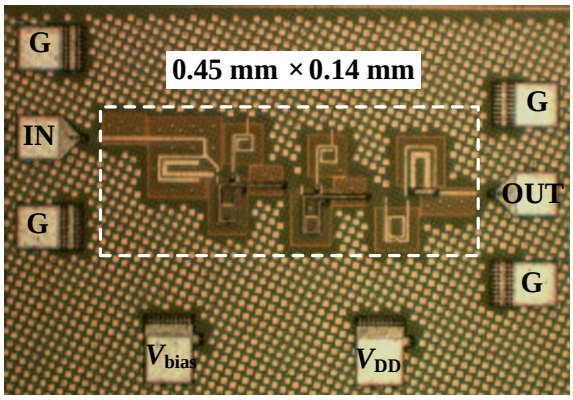


Figure 2.25 Die micrograph of wideband LNA based on pole-converging technique.

The measured S-parameters of high-gain mode are plotted in Figure 2.26(a). The prototype achieves a 3-dB bandwidth from 62.5 GHz to 92.5 GHz with peak gain of 18.5 dB at 68 GHz. The input return loss is better than 10 dB from 60.5 GHz to beyond 110 GHz, while the output return loss is better than 6 dB in the entire 3-

dB bandwidth. When there is a constraint on the power consumption, the proposed LNA can provide a power gain of 13.3 dB at 69 GHz with a 3-dB bandwidth from 63.5 GHz to 91 GHz in the low-power mode, as depicted in Figure 2.26(b). Wideband input and output matching are also obtained, $|S_{11}| < -12.1$ dB and $|S_{22}| < -6.5$ dB in the 3-dB bandwidth. Compared to simulated results, the 3-dB bandwidths of both scenarios reduce by ~8 GHz mainly due to the degradation of magnetic coupling coefficient. Such degradation is caused by randomized dummy metal fills. The dummy metal fills introduce additional parasitic capacitance, degrading inductance and quality factor, which were not fully considered in EM simulation.

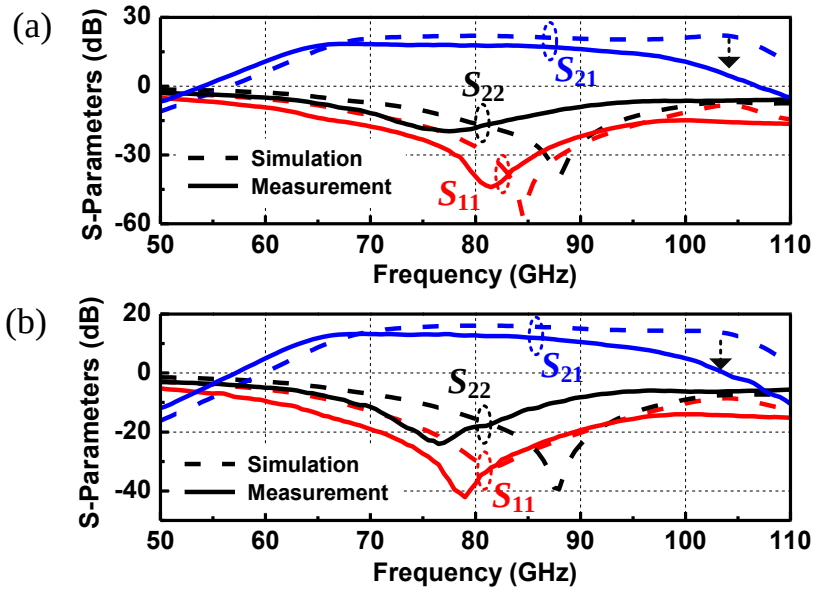


Figure 2.26 Simulated and measured S-parameters: (a) in high-gain mode, (b) in low-power mode.

Figure 2.27 shows the measured reverse isolation and group delay of the proposed wideband LNA. Within the entire 3-dB bandwidth, the isolation is better than 45 dB, and the group delay is 35 ps with a variation of ±5 ps.

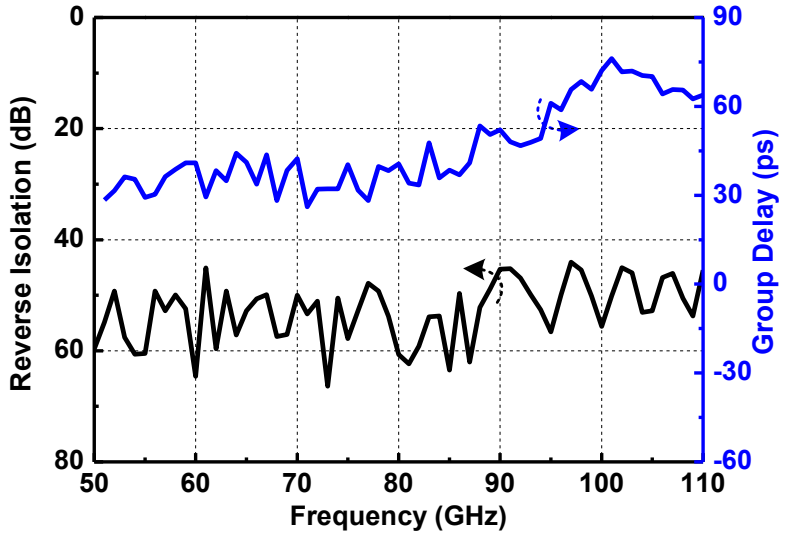


Figure 2.27 Measured reverse isolation and group delay in high-gain mode.

Figure 2.12 demonstrates noise figure measurement setup. This measurement setup utilizes the Y-factor method through turning on and off the noise source, which delivers a uniform level of noise power spectral density with a typical excess noise ratio (ENR) of 12 dB within the full W-band. To obtain a more accurate NF, a 2nd stage calibration was performed to remove the noise figure of the spectrum analyzer, and the average of 20 measurements was taken. Due to the limitation of measurement setup, NF was measured from 75 GHz to 100 GHz.

The average NF of the high-gain mode is 6.8 dB with a minimum value of 5.5 dB at 90 GHz, while the LNA in the low-power mode exhibits an average NF of 7.6 dB with a minimum value of 6.4 dB at 82 GHz, as depicted in Figure 2.28.

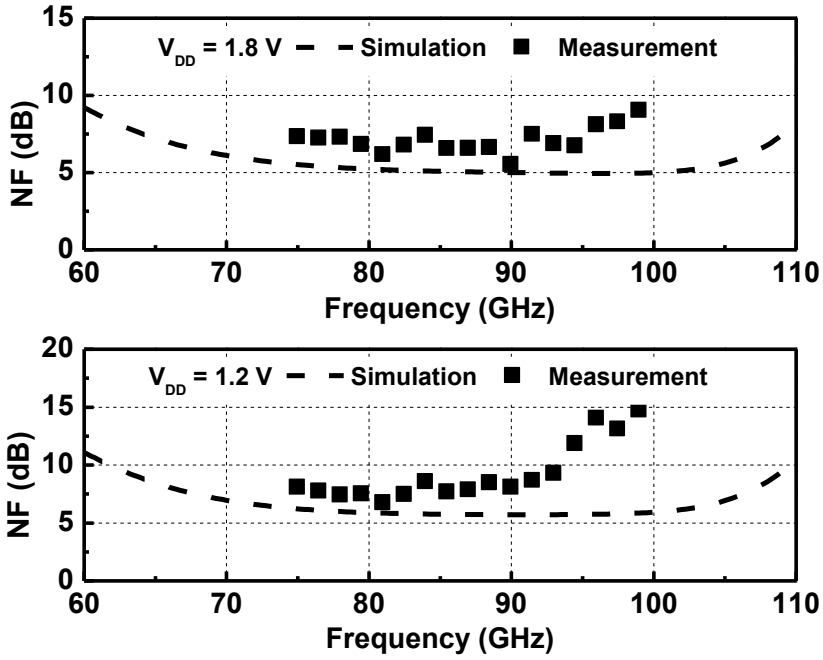


Figure 2.28 Simulated and measured noise figures in high-gain mode and low-power mode.

Figure 2.29 shows large-signal measurement setup. This setup is composed of a microwave signal generator, an active multiplier (×6) with output power of ~12 dBm, a tunable attenuator with maximum attenuation of 40 dB, and a thermal power sensor. Before testing the LNA, point A was directly connected to point B to measure the input power. By tuning the attenuator, different levels of input

power were obtained. Then the output power of the LNA was measured through on-wafer testing. After de-embedding the insertion losses of GSG pads and cables, large-signal characterizations of the amplifier were achieved.

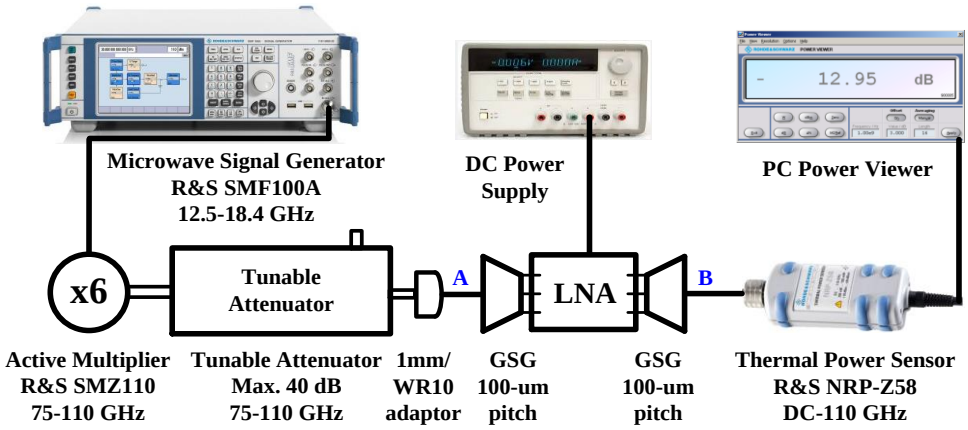


Figure 2.29 Large-signal measurement setup.

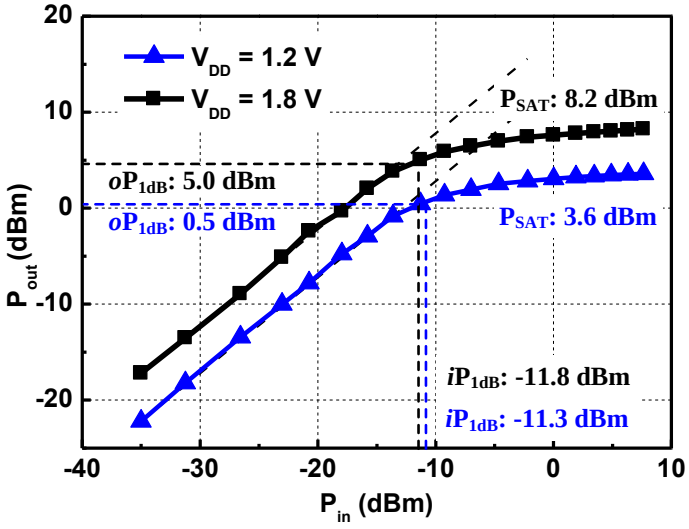


Figure 2.30 Measured output power versus input power at 80 GHz.

Figure 2.30 shows the measured output power of two modes as input power varies at 80 GHz. The proposed amplifier exhibits an output-referred P_{1dB} of 5.0 dBm and P_{SAT} of 8.2 dBm in high-gain mode, while those in low-power mode are 0.5 dBm and 3.6 dBm, respectively.

Table 2-6 summarizes the performance of the proposed broadband LNA and compares it to state-of-the-art LNAs. A commonly used *Figure-of-Merit* (FoM) [40] is adopted for comparison, which takes the power gain, 3-dB bandwidth, noise factor, and power consumption into account, defined as

$$FoM = \frac{Gain[\text{abs.}] \times BW[\text{GHz}]}{(F-1) \times P_{DC}[\text{mW}]} \tag{2.23}$$

The bandwidth of proposed LNA is significantly extended by the proposed pole-converging technique without increasing power consumption and die size. To the author's best knowledge, the presented LNA achieves the widest 3-dB bandwidth and the best FoM among multi-stage mm-wave LNAs in CMOS.

Table 2-6 Performance summary and comparison to state-of-the-art wideband mm-wave LNAs

Reference	Technology	Topology	Gain (dB)	BW[†] (GHz)	NF (dB)	Power (mW)	V_{DD} (V)	Size (mm^2)	FoM
[31] JSSC′10	70-nm GaAs mHEMT	4-stage CS	25	40[*]	2.5 - 2.7	40	1.3	6.00	20.63 - 22.85
[32] MWCL′15	50-nm GaAs mHEMT	5-stage CS	26[#]	57[#]	3.2 - 4.8	24	-	2.00	23.46 - 43.50
[33] TMTT′15	0.10-µm GaAs pHEMT	3-stage CS	23	28	2.1 - 3.0	80	2.0	1.70	4.97 - 7.95
[34] IMS′14	50-nm GaAs mHEMT	3-stage CS	26	62[#]	1.3 - 2.3	45	2.0	3.62	39.37 - 78.78
[45] MWCL′10	0.18-µm SiGe	2-stage cascode	14.5	14.5	6.9 - 8.0	37	3.3	0.41	0.39 - 0.53
[15] JSSC′11	0.18-µm SiGe	5-stage CE	19	19[#]	8.0 - 12[#]	63	1.8	1.00	0.18 - 0.51
[24] JSSC′13	0.13-µm SiGe	2-stage cascode	22.5	30	6.0 - 7.2[#]	52	2.5	0.52	1.81 - 2.58
			25	70[#]	6.2 - 9.0[#]	54	2.5	0.33	3.32 - 7.27
[36] JSSC′07	0.18-µm CMOS	Distributed	20	39.4	8.0 - 9.4	250	2.8	2.24	0.20 - 0.30
[37] TMTT′13	0.18-µm CMOS	Distributed	24	33	6.5 - 7.5	238	2.8	0.83	0.48 - 0.63
[38] TMTT′12	65-nm CMOS	Distributed	22	65	6.9 - 7.9	97	1.3	0.93	1.63 - 2.16
[39] IMS′15	0.18-µm CMOS	Distributed	25	34	6.5 - 8.0	176	2.8	0.86	0.65 - 0.99
[41] TMTT′12	45-nm SOI CMOS	3-stage CS	10.7	18	6.0 - 11	52	1.4	0.32	0.10 - 0.40
[42] JSSC′08	65-nm CMOS	3-stage cascode	13.5	20	6.4 - 9.0[#]	-	1.5	-	-
[43] EL′12	90-nm CMOS	3-stage cascode	14	23	4.8 - 7.0[#]	32	2.0	0.22	0.90 - 1.78
[18] JSSC′10	65-nm CMOS	5-stage cascode	27	13.5[#]	6.8 - 9.0[#]	36	1.2	-	1.21 - 2.22
[44] TMTT′15	28-nm CMOS	2-stage cascode	13.8	18	4.0 - 5.8	24	2.0	0.38	1.31 - 2.43
[46] IMS′12	65-nm CMOS	4-stage cascode	25.3	20[#]	6.0 - 8.3	48	2.0	0.25	1.33 - 2.57
[47] ISSCC′09	65-nm CMOS	4-stage CS	14.8	21	7.5 - 9.0[#]	86	1.2	0.33	0.19 - 0.29
[10] JSSC′11	65-nm CMOS	3-stage cascode	15	12	7.0 - 10[#]	42	1.2	-	0.18 - 0.40
This Work	**65-nm CMOS**	**3-stage cascode**	**13.3**	**27.5**	**6.4 - 8.5**	**12**	**1.2**	**0.24**	**1.73 - 3.12**
			18.5	**30**	**5.5 - 7.9**	**27**	**1.8**		**1.78 - 3.62**

[†] 3-dB bandwidth; [*] about 4-dB bandwidth; [#] estimated value from figures

2.4 Summary

In this chapter, background and literature review of wideband LNAs are reported at the beginning. Then, two wideband LNAs are presented, together with the circuit analysis and design methodology. One is based on part peak-gain distribution, and the other is based on a novel pole-converging technique for intra-stage bandwidth extension. The former wideband LNA achieves peak gain of 16.7 dB at 104 GHz, minimum NF of 7.2 dB, and 3-dB bandwidth of 21.5 GHz with power consumption of 48.6 mW. The pole-converging-based LNA exhibits peak power gain of 18.5 dB, minimum NF of 5.5 dB, power consumption of 27 mW, P_{1dB} of 5.0 dBm, and 3-dB bandwidth of 30 GHz. The bandwidth of this LNA is significantly extended by the proposed pole-converging technique without increasing power consumption and die size. To the author's best knowledge, this LNA achieves the widest 3-dB bandwidth and the best FoM among multi-stage mm-wave LNAs in CMOS technologies. Furthermore, the pole-converging technique can be combined with other inter-stage bandwidth enhancement techniques to achieve greater bandwidth extension.

Although the proposed pole-converging technique is adopted to design a wideband mm-wave LNA in this work, the design methodology can be extended to wideband amplifiers design at lower frequencies. In addition, an amplifier with variable gain or bandwidth can be achieved, if the gate inductor is switchable or

the magnetic coupling coefficient of the drain-source transformer is reconfigurable.

Chapter 3

SDP-LNA-Based Direct-Detection Dicke Receiver

Thanks to the aggressive progress of CMOS technology and promising applications of mm-wave imaging, the mm-wave imaging systems using CMOS platform have greatly evolved, and several approaches have been proposed in literature to implement CMOS mm-wave imaging systems. The building blocks are similar to those used in communication systems, but mm-wave imaging receiver detects the strength of radiation or reflection to construct object images, rather than modulated signal. In this chapter, a novel direct-detection Dicke receiver is implemented for mm-wave imaging systems.

3.1 Background and Literature Review

Mm-wave imaging receiver employs two main architectures: direct detection (total-power radiometer) and heterodyne detection, no matter it is passive mm-wave imaging or active mm-wave imaging. Direct-detection mm-wave imaging receiver is based on total-power radiometer, with a LNA at the front-end, as shown in Figure 3.1. The receiver is composed of a LNA, a power detector, and an optional low-frequency amplifier, followed by an integrator. Such a receiver acts as a single pixel of imaging systems, and the output voltage is proportional to incident RF signal strength. Figure 3.2 shows a typical heterodyne imaging receiver. The incident signal is amplified by a LNA, then down-converted to a lower frequency by a mixer, followed by an IF amplifier, a post-detector, and an integrator. Mixer is the most important component of heterodyne receiver, which contributes the most noise to heterodyne receiver and is responsible for its responsivity.

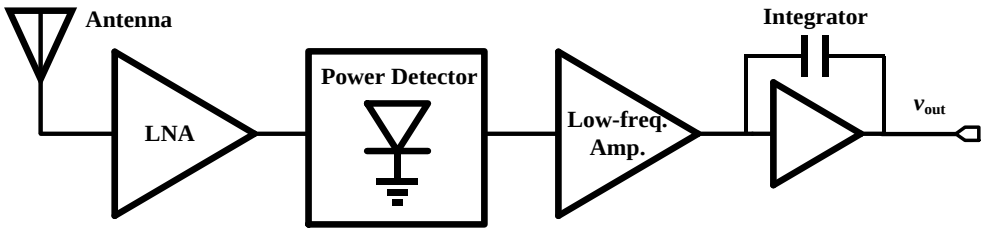


Figure 3.1 Imaging receiver based on direct-detection architecture.

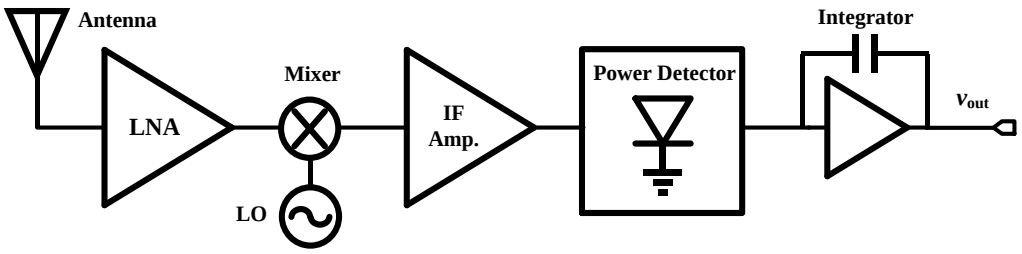


Figure 3.2 Imaging receiver based on heterodyne architecture.

Because of several advantages of no need of a local oscillator, low noise, low cost, and low power consumption, the direct detection receivers are utilized widely in the field of mm-wave imaging [56]. In general, heterodyne detection can provide very high spectral resolution because $f_{IF} \ll f$, while direct detection offers moderate spectral resolution. Compared to direct detection, the heterodyne detection presents some pros and several cons [57]. The pros of heterodyne detection are summarized as follows: (a) both frequency information and phase information can be detected; (b) IF amplifier can be implemented with high gain much more easily, so that the overall gain of the system can be made much larger; (c) conversion gain is proportional to P_{LO}/P_s (P_{LO} is power of local oscillator, and P_s is the power of radiant signal) and thus, much weaker incident signal power can be detected. The cons of heterodyne detection are summarized as follows: (a) LO distribution problem; (b) limitations of LO drive power; (c) large DC power consumption; (d) not easy to produce large format arrays.

In practice, no matter the imaging receiver is based on direct-detection or heterodyne reception, fluctuations of the overall RF-power-gain have great effects on receiver sensitivity. Imaging receivers themselves cannot distinguish between the change of radiant power and the fluctuations of RF-power-gain. The sensitivity of mm-wave imaging systems can be expressed in terms of the minimum temperature difference that can be detected. One Figure-of-Merit (FoM) of imaging systems is radiometer resolution, which describes the smallest change in input brightness temperature or radiance required to produce a post detection SNR of unit [10], [18], expressed as:

$$\Delta T_{\min} = T_S \sqrt{\frac{1}{B\tau} + \left(\frac{\Delta G}{G}\right)^2} \tag{3.1}$$

where T_s is the system noise temperature, B is the RF front-end bandwidth, τ is the receiver's integration time, ΔG is the effective value of the imaging receiver gain variation, and G is the overall gain of the receiver front-end.

In order to achieve a sufficient radiometer resolution, the value of $\Delta T_{\min}$ is typically on the order of 0.5 K [16], [58]. Because the temperature across a typical scene changes only a few K, too high $\Delta T_{\min}$ results in failing to capture usable images. However, the fluctuations of the system's overall gain, the second item under the square root in (3.1), presents great effects on the $\Delta T_{\min}$. For example, if

the power gain of the system is 30 dB, the system noise temperature is 3000 K, the RF front-end bandwidth is 10 GHz, the integration time is 20 ms, and the gain variation of 0.004 dB is assumed, $\Delta T_{\min}$ changes from 0.21 K to 3 K, much larger than 0.5 K for practical mm-wave imaging applications. Another critical issue about advanced CMOS technology is stronger flicker noise (1/*f* noise) compared to the III-V and SiGe technologies. The flicker noise can cause DC drift at the receiver's output, which presents effects on the receiver sensitivity similarly as the front-end gain variation [10].

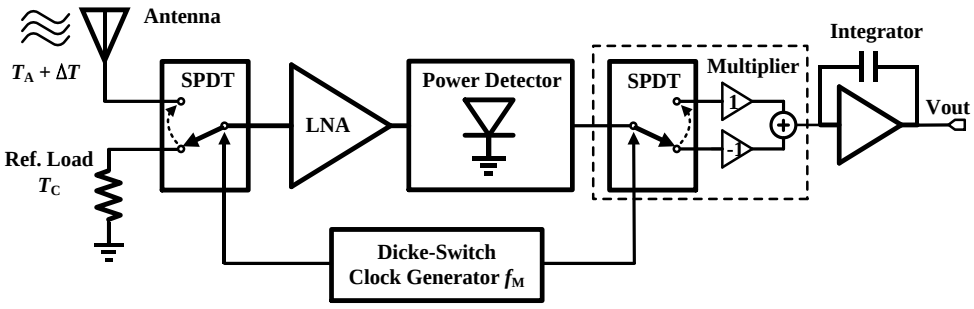


Figure 3.3 Dicke receiver based on derect-detection architecture.

The effects of the low-frequency front-end gain fluctuations and the flicker noise can be greatly alleviated through calibrating the receiver periodically using the Dicke-switch architecture [18], [59], [60]. Dicke is the first to introduce modulation principle for eliminating the impacts on radiometer resolution caused by the receiver instabilities [61]. The imaging receiver based on Dicke receiver

architecture is shown in Figure 3.3. The input of the LNA is switched by a single-pole-double-through (SPDT) switch between a reference load resistor and the antenna at a frequency f_M, which should be much higher than corner frequency. At the output of power detector, a multiplier switches the detector output to the integrator synchronously but in the opposite phase, so that the output voltage corresponding to reference load is subtracted from that introduced by the received signal. If the noise temperature T_C from the reference resistor equals to the antenna noise temperature T_A, the output voltage of the integrator is directly proportional to the signal power and modulated at the frequency f_M. If the modulation frequency is high enough compared to the front-end gain variation frequencies, then it is possible to detect the RF signal without worrying about the receiver gain fluctuations and the DC drift caused by flicker noise. Nevertheless, for Dicke receiver, the signal is received when the switch is connected to the antenna, only half of the total time, leading to a 3-dB degradation of the radiometer resolution, expressed as (3.2).

$$\Delta T_{\min} = \frac{2T_S}{\sqrt{B\tau}} \tag{3.2}$$

In literature, mm-wave imaging systems in CMOS have been greatly explored to achieve single-chip imaging receiver with small pixel size and low power consumption. In [18], the first W-band passive imaging receivers implemented in

a 65-nm CMOS technology were presented. Both total power radiometer and Dicke receiver were fabricated and discussed in this paper. The total power radiometer with a LNA at the input shows an average responsivity of 148 kV/W, NEP of 162 fW/Hz$^{0.5}$, and ΔT_{min} of 5.0 K. And the Dicke receiver is composed of a W-band CMOS LNA with power gain of 27 dB and noise figure of 6.8 dB, a differential square-law detector, and a W-band SPDT switch. With a supply voltage of 1.2 V, the Dicke receiver presents total power consumption of 38.4 mW, an average responsivity of 60 kV/W, NEP of 381 fW/Hz$^{0.5}$, and ΔT_{min} of 12.5 K. However, when the supply voltage is increased to 2.4 V, the gain of LNA is greater than 36 dB, and the Dicke receiver achieves 666-kV/W average responsivity, 36-fW/Hz$^{0.5}$ NEP, and 1.1-K ΔT_{min}. Although the ΔT_{min} is decreased a lot, the power consumption of single pixel is as much as 110 mW. In [62], a fully differential CMOS passive imaging receiver was presented. The peak responsivity with an enable/disable switch is 1.6 MV/W and 1.8 MV/W, respectively, which is increased to 100 MV/W with an on-chip programmable gain amplifier (PGA). NEPs are 26 fW/Hz$^{0.5}$ and 23 fW/Hz$^{0.5}$, respectively, and ΔT_{min} is less than 2 K. In [10], a direct-conversion receiver front-end was implemented in a 65-nm CMOS technology. The responsivity is 16.147 MV/W, while ΔT_{min} and average NEP are 1 K and 9 fW/Hz$^{0.5}$, respectively. However, this CMOS radiometer utilizes multi-chip solution with front-end and baseband chipsets wire-bonded to a printed circuit board (PCB). Therefore, the total chip

size is quite large, i.e. 3 mm^2, and the power consumption is 101.6 mW. Despite the large chip size and power consumption, this direct-conversion receiver demonstrates the lowest ΔT_{min} among CMOS mm-wave imaging receivers reported so far. Table 3-1 summarizes the performance of state-of-the-art mm-wave imaging receivers.

Table 3-1 Performance summary of state-of-the-art mm-wave imaging receivers

Reference	[10] JSSC'11	[15] JSSC'11	[17] TMTT'10	[18] JSSC'10	[18] JSSC'10	[62] EL'11
Technology	65-nm CMOS	0.18-μm SiGe	0.12-μm SiGe	65-nm CMOS	65-nm CMOS	65nm CMOS
Integration	LNA Mixer PD BB	LNA RTPS PD BB	LNA SPDT PD	LNA PD	LNA SPDT PD	LNA PD PGA
3-dB BW (GHz)	11	26	14	18	18	-
NEP ($fW/Hz^{0.5}$)	8.8	10	21	162	36	26
ΔT_{min} (K, 30ms)	1	0.4	0.83	5	1.1	2.0
Responsivity (MV/W)	16	43	5	0.15	0.67	100[#]
Power (mW)	101.6	200	34.8	38.4	110	62
Area (mm^2)	3	12.5	0.4	0.31	0.41	0.55

PD = power detector; BB = baseband; [#] with programmable amplifier

However, due to high substrate losses, poor device gain, and strong flicker noise, the ΔT_{min} of CMOS imaging receivers is still larger than 0.5 K [10], [18], [62], as illustrated in Table 3-1. Furthermore, the insertion loss of Dicke switch directly increases front-end noise figure, which degrades the receiver sensitivity. The

insertion loss is not a big problem in the III-V semiconductor technologies because low-loss PIN diode switches are available. However, insertion loss of on-chip SPDT switch in 65nm CMOS is around 4-5 dB [18], [63], [64]. System-level analysis indicates that 5-dB insertion loss prior to the LNA degrades the ΔT_{min} by a factor of 3 [15].

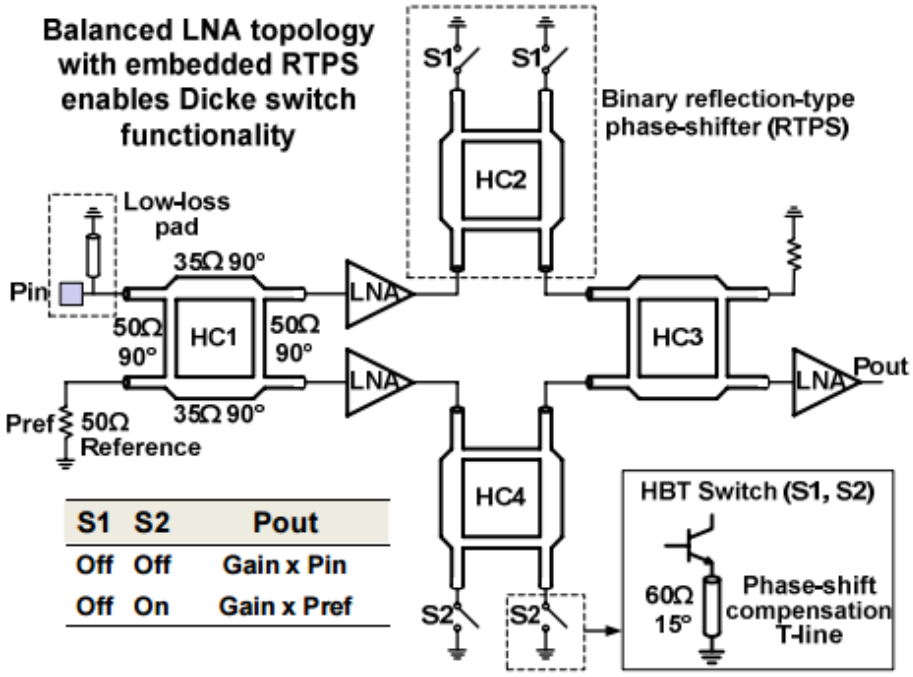


Figure 3.4 Balanced LNA with embedded Dicke switch [15]**.**

A novel structure proposed by Leland Gilreath in [15] eliminates the above mentioned problem by embedding Dicke switch in a balanced LNA, so that the effect from the insertion loss of the CMOS switch is minimized. Figure 3.4

illustrates the proposed balanced LNA with embedded Dicke switch. When both phase shifters are in the same state, namely both S1 and S2 are turned off, the incident signal power is amplified and delivered to the output port and the reference noise power is suppressed. On the contrary, when S1 and S2 are in the opposite state, the reference noise power is amplified and signal power is suppressed. In order to further increase the pre-detection gain, an additional LNA is employed after the balanced structure.

Although the insertion loss of hybrid coupler at input is much smaller than that of SPDT, there are several drawbacks of this topology. Firstly, four bulky hybrid couplers dramatically increase the chip size. Secondly, three LNAs are adopted, increasing the chip area and system power consumption. Thirdly, two binary RTPSs present insertion loss of ~8 dB. The insertion loss of RTPS does not degrade the $\Delta T_{\min}$ and NF of imaging system as that of conventional Dicke switch, but reduces the power gain of RF front-end.

3.2 Design Specifications

Figure 3.5 shows the main block diagram of backscattering mm-wave imaging system for active imaging applications, which can also be used in the trans-

missive mm-wave imaging system. No matter it is passive imaging or active imaging, there is no much difference in the receiver part.

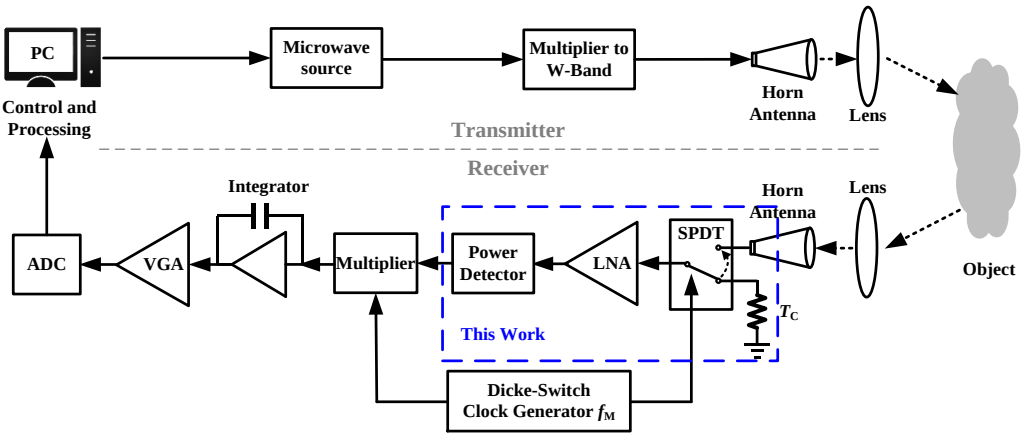


Figure 3.5 Block diagram of backscattering mm-wave imaging system.

Sensitivity is one critical characteristic of imaging receiver because it determines the image quality and acquisition time. Passive imaging systems depend only on the black-body radiation, which is quite weak at mm-wave frequencies. And for active mm-wave imaging, higher sensitivity means lower illustration power, which is quite limited in CMOS technology. Besides, the path loss of free space is very large at mm-wave frequencies. The choice of frequency is based on a simple rule: lower frequency for deeper penetration of the dielectric materials; higher frequency for higher resolution. According to (3.3), with the transmission distance of 1 cm, the path loss (FSPL) is 31.5 dB at 90 GHz, which becomes 71.5 dB when

the distance is increased to 1 m. To alleviate the stress on the link budget of imaging systems, the receiver must have extremely high sensitivity.

$$\mathrm{FSPL}(dB) = 20\log_{10}(d) + 20\log_{10}(f) + 32.45 \tag{3.3}$$

where f is measured in units of GHz and d in m.

This work focuses on the RF front-end design of the imaging receiver. Table 3-2 summarizes the design specifications of the imaging receiver for active and passive mm-wave imaging applications.

Table 3-2 Design specifications of the mm-wave imaging receiver and its main building blocks

	Receiver	**LNA**	**Power Detector**
Operation Frequency (GHz)	80-100	80-100	80-100
Sensitivity (dBm)	-60	-	-30
Responsivity (MV/W)	5	-	0.005
NEP ($pW/Hz^{0.5}$)	0.01	-	10
ΔT_{min} (K)	0.5	-	-
Gain (dB)	-	30	-
NF (dB)	10	6	-
Power Consumption (mW)	60	55	1

3.3 Implementation of SDP-LNA-Based Dicke Receiver

As discussed previously, the gain fluctuations and the flicker noise exhibits great effects on the receiver sensitivity. Dicke receiver was proposed to alleviate such effects. However, on-chip SPDT switch in CMOS technology presents high insertion loss, ~4-5 dB, which directly degrades the system's ΔT_{min} and NF. In [15], an balanced LNA with embedded Dicke switch was proposed to eliminate the degradation introduced by insertion loss of SPDT switches. However, this approach dramatically increases the chip area due to the bulky RTPS, and therefore the cost of multi-pixel imaging systems. In this work, a switchable dual-path LNA (SDP-LNA) is proposed in the design of Dicke receiver. Thanks to the internal switching of the SDP-LNA, the sensitivity degradation due to the insertion loss of Dicke switch is eliminated. The pole-converging technique for intra-stage bandwidth extension is adopted in the design of the SDP-LNA. Based on the SDP-LNA, a direct-detection Dicke receiver is designed and implemented in a 65-nm CMOS technology.

Figure 3.6 shows the schematic of the SDP-LNA-based direct-detection Dicke receiver, which consists of a dual-path LNA with a path-enable controller, a power detector, and an output buffer. One input port of the SDP-LNA is used to inject RF signal, while the other input port is connected to a reference load resistor. The output port of the SDP-LNA is directly connected to the power

detector. An output buffer is utilized to drive the large load capacitor from testing equipment.

Different from traditional Dicke receivers, the SDP-LNA-based Dicke receiver removes SPDT switches. Through the path-enable controller of the SDP-LNA, the input signal and reference load are switched periodically without degrading the radiometer resolution. In addition to the elimination of Dicke switch in the proposed Dicke receiver, the isolation between two input ports is also significantly enhanced due to the high isolation of cascode amplifiers.

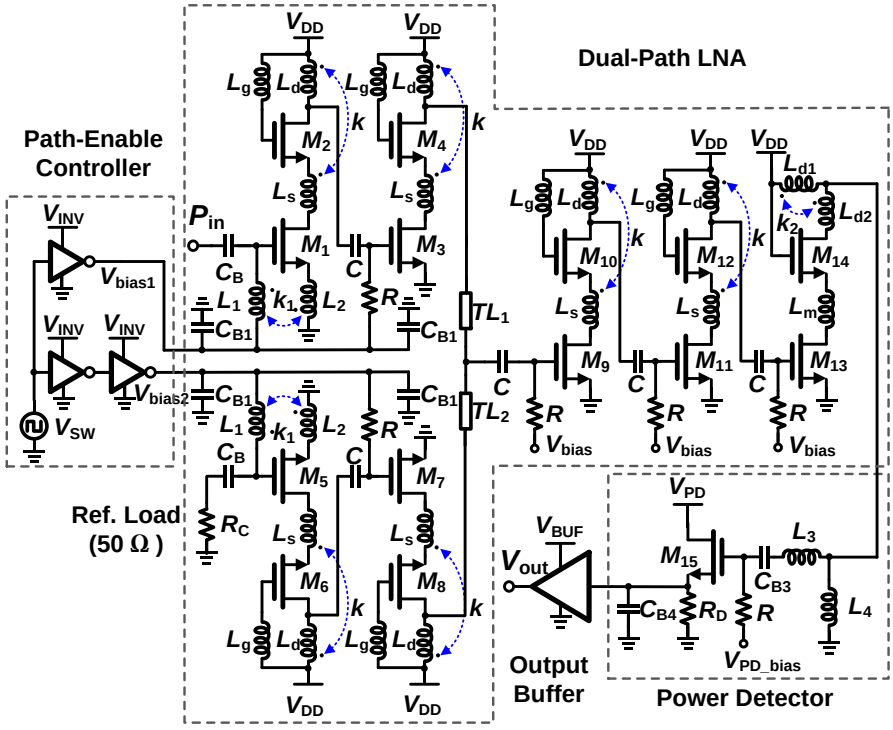


Figure 3.6 Schematic of the proposed SDP-LNA-based direct-detection Dicke receiver.

3.3.1 SDP-LNA

The SDP-LNA consists of two parts, switchable stages and shared stages, and each stage is a cascode amplifier. Pole-converging technique for intra-stage bandwidth extension is introduced in each stage to achieve high gain and wide bandwidth, except for the output stage, which functions as an output buffer. To obtain good reflection coefficients over a wide bandwidth, the input and output matching networks are designed with shunt-series transformer feedback and asymmetric T-coil gain peaking, respectively.

The switchable stages are composed of two identical branches controlled by a path-enable controller, as shown in Figure 3.6. When V_{sw} is low, the upper path is enabled, otherwise, the under path is activated. When either path is enabled, the corresponding bias voltage is set to high and equals to V_{INV}. By changing the value of V_{INV}, various biasing voltage for the first two stages can be obtained. Note that, bypass capacitors C_{B1} are introduced to provide a good AC ground at bias points. By increasing the number of switchable stages, the isolation between two input ports can be further enhanced. However, the number of shared stage is reduced for a SDP-LNA with given total stages under the consideration of overall power consumption. Therefore, the symmetry uncertainty between the two signal paths is increased, which is undesired.

By using the gate-inductor gain-peaking and negative drain-source transformer-feedback techniques in the intra-stages, the transfer function of each stage exhibits two dominant poles. With proper designs of drain-source transformer and gate inductor, a high-gain wideband LNA can be achieved without increasing the overall power consumption. The analyses of gate-inductor gain-peaking and negative drain-source transformer-feedback techniques are provided in Chapter 2. The drain-source transformer feedback is implemented in the common-gate (CG) amplifier of each cascode stage by magnetically coupling the drain inductor L_d and source inductor L_s. Furthermore, L_s tunes out the parasitic gate-source and gate-drain capacitances of the common-gate and common-source transistors, respectively, which leads to higher f_T of cascode amplifiers. The gate terminal of the CG transistor is biased through a gate inductor L_g, which enhances the effective trans-conductance G_m. Therefore, L_g boosts the overall gain without extra power consumption.

Based on the design methodology presented in Chapter 2, a five-stage cascode LNA with high gain and wide bandwidth can be achieved. The only modification is that one duplicate of first two stages is introduced as the second input branch and the outputs of two branches are combined at the input of third stage, as shown in Figure 3.6. All the inductors, transformers, and testing pads were custom designed with interconnections and simulated using the 3D EM simulator ANSYS

HFSS. Table 3-3 lists the design parameters of circuit elements in the SDP-LNA. All the transistors have a finger width of 1 μm with the minimum gate length, which results in a good compromise between gate-resistance reducing and f_T degradation due to gate-bulk capacitance.

Table 3-3 Design parameters of circuit elements in the SDP-LNA

@80GHz	L_1	L_2	L_3	L_g	L_s	L_d	L_{d1}	L_{d2}
Ind. (pH)	45	27	89	71	108	55	39	63
Q	10.3	13.7	12.1	13.3	15.1	9.6	12.6	13.2
	k	k_1	k_2	R	C	C_B	C_{B1}	M_1-M_{14}
	0.43	0.41	0.31	18 kΩ	176 *f*F	200 *f*F	1 pF	25 μm

3.3.2 Power Detector

In direct-detection receivers, a power detector is used to convert the input RF power to an output DC voltage. As shown in Figure 3.6, the power detector consists of M_{15} and R_D with L_3 and L_4 forming input matching network. The gate of M_{15} is biased through a large resistor. A small bypass capacitor C_{B4} is used to filter out injected RF signal and its harmonics caused by the nonlinearity of power detector.

The power detector should operate in the square-law region; therefore, the input power and output voltage have a linear relationship. A short-channel transistor has a very linear I-V characteristic; nevertheless, it can generate relatively large second order harmonics by proper biasing [10]. Thus, the responsivity of power detector can be improved with optimal bias. The minimum NEP is obtained when the transistor is biased at where the derivative of responsivity in terms of bias current reaches its maximum, which occurs with the smallest transistor size and lowest bias currents [17]. However, smaller transistors exhibit increased flicker noise and increase the complexity of input matching network. Therefore, the final choice of transistor size is determined by a tradeoff among minimum NEP, flicker noise, and matching network. A transistor width of 25 μm with finger length of 1 μm and minimum channel length of 65 nm is chosen with a bias current of 150 μA for the detector to achieve good NEP and low flicker noise.

3.4 Experimental Results

The SDP-LNA-based direct-detection Dicke receiver was fabricated in GlobalFoundries 65-nm CMOS technology. Figure 3.7 and Figure 3.8 show the die micrographs of the standalone SDP-LNA and the Dicke receiver, respectively. The two dies occupy silicon sizes of 0.47 mm^2 and 0.50 mm^2, respectively, including all the pads. Under a supply voltage of 1.8 V, the standalone LNA

exhibits power consumption of 52.3 mW, while the power detector and output buffer consume 0.3 mW DC power under a 1.2-V power supply. The total power consumption of the SDP-LNA-based direct-detection Dicke receiver is 52.6 mW.

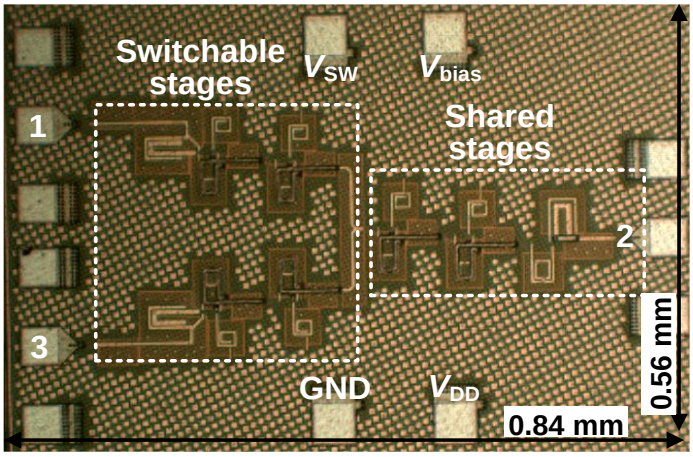


Figure 3.7 Die micrograph of the standalone SDP-LNA

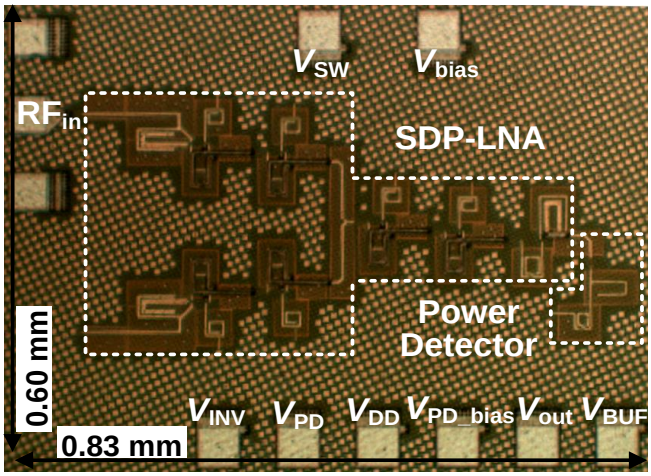


Figure 3.8 Die micrograph of the SDP-LNA-based direct-detection Dicke receiver

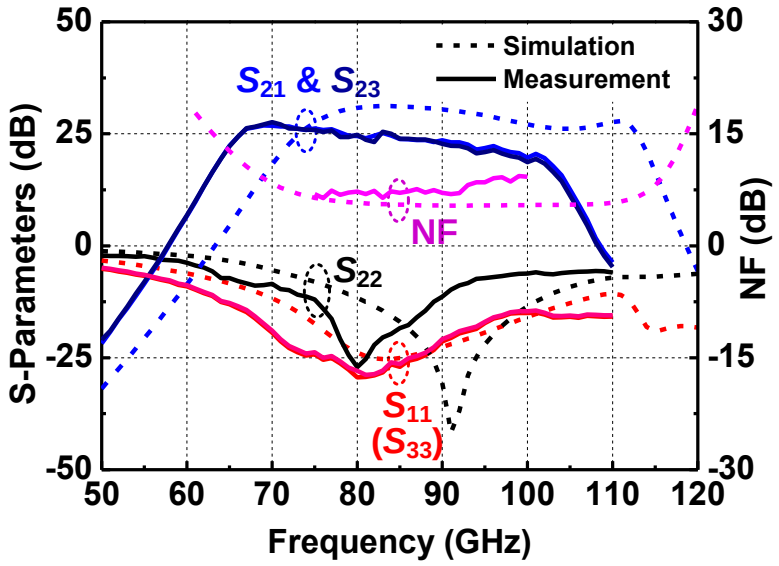


Figure 3.9 Measured and simulated S-parameters and NF of the SDP-LNA

Figure 3.9 depicts the measured and simulated S-parameters and NF of the SDP-LNA. The SDP-LNA achieves a 3-dB bandwidth from 65.5 GHz to 91 GHz with peak gain of 26.8 dB at 70 GHz, and the power gains of two paths show good agreement with each other. The input return loss is better than 10 dB from 62 GHz to beyond 110 GHz, while the output return loss is better than 8 dB within the entire 3-dB bandwidth. Compared to the simulated result, the frequency response shifts down ~10 GHz and the 3-dB bandwidth is reduced by ~11.5 GHz, mainly due to the degradation of magnetic coupling coefficient caused by randomized dummy metal fills. The net effect of having dummy metal fill shapes underneath the spiral then, is to increase the capacitance, thus inductances and

electromagnetic coupling factor of transformer are affected. Due to the limitation of measurement setup, NF was measured from 75 GHz to 100 GHz. The average NF is 7.1 dB with a minimum value of 6.4 dB at 83 GHz. The S_{12} (S_{32}) is the reversion isolation and is better than 45 dB in the frequencies of interest, as shown in Figure 3.10. Higher reversion isolation means better stability. The S_{13} is the isolation between the two input ports and it is higher than 35 dB within the entire 3-dB bandwidth. Compared to the isolation of CMOS SPDT [18], that of the SDP-LNA exhibits more than 15-dB improvement because of the high isolation of cascode topology.

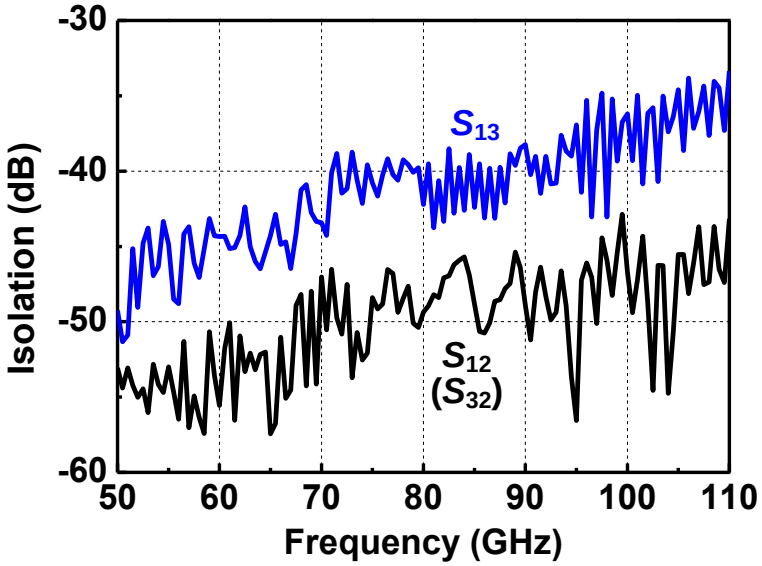


Figure 3.10 Measured isolation of the SDP-LNA

Figure 3.11 depicts the measurement setup of the proposed Dicke receiver. This setup is composed of a microwave signal generator, an active multiplier (×6) with output power of ~12 dBm, a tunable attenuator with maximum attenuation of 40 dB, and a fixed 40-dB attenuator. Before testing the Dicke receiver, point A was directly connected to a W-band power meter to measure the power level. By tuning the attenuator, different levels of input power are obtained. The Dicke switch clock is provided by an external arbitrary waveform generator. The output voltages corresponding to the injected power and reference load are measured by an oscilloscope, as shown in Figure 3.12 and Figure 3.13. The voltage difference ΔV_{out} is calculated by subtracting the output voltage corresponding to reference load from that introduced by the received signal.

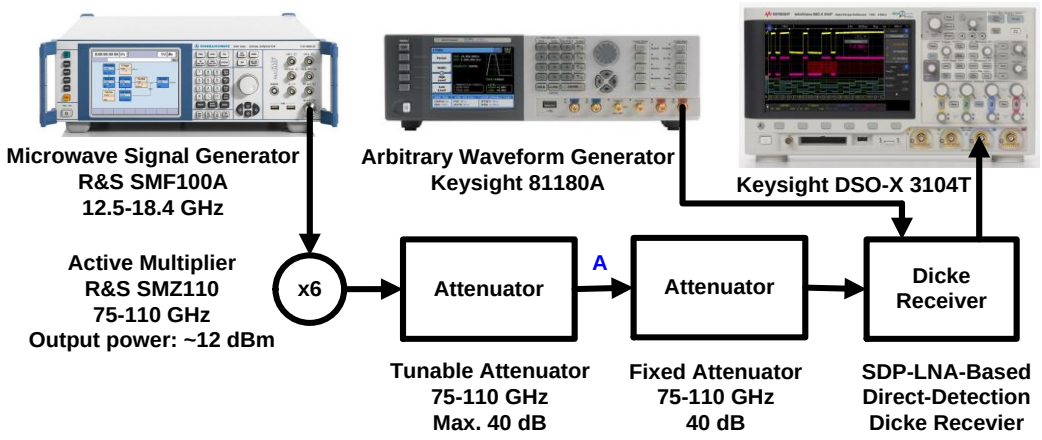


Figure 3.11 Measurement setup of the SDP-LNA-based direct-detection Dicke receiver.

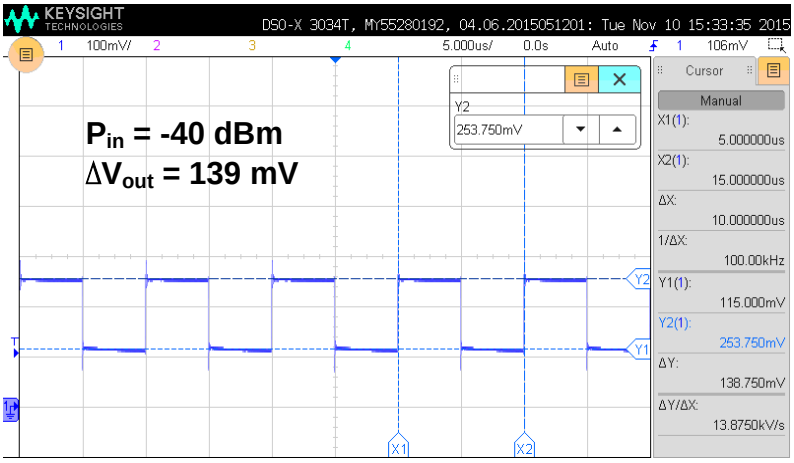


Figure 3.12 Output waveform of the Dicke receiver under an 80-GHz input signal with power level of -40 dBm.

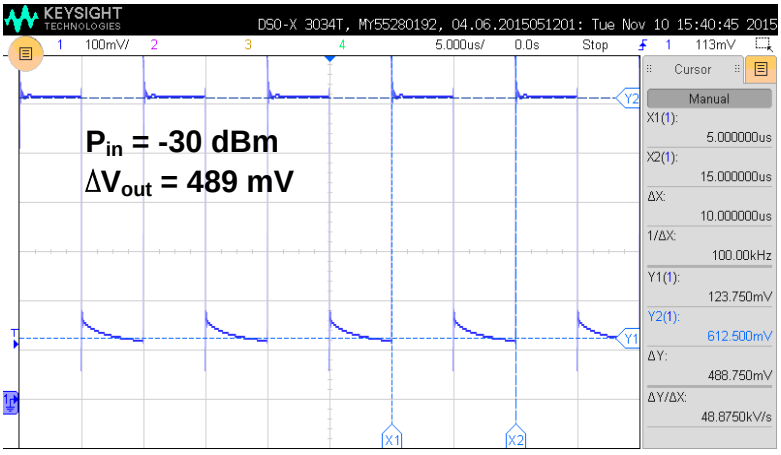


Figure 3.13 Output waveform of the Dicke receiver under an 80-GHz input signal with power level of -30 dBm.

Figure 3.14 and Figure 3.15 illustrate the output voltages of the Dicke receiver under input RF signal with various power levels and frequencies, respectively. To

characterize the input power sensitivity and responsivity of the Dicke receiver, the power level of an 80-GHz input RF signal is swept from -15 dBm to -65 dBm under a Dicke switch clock of 100 KHz. The receiver achieves sensitivity of -60 dBm and peak responsivity of 2.5 MV/W, as shown in Figure 3.14. The receiver demonstrates 3-dB bandwidth of 11.5 GHz and peak conversion gain of 12 dB, as depicted in Figure 3.15. To characterize the receiver bandwidth, a -40-dBm RF signal is injected into the receiver with frequency being swept from 75 GHz to 95 GHz. The output voltage is recorded by the oscilloscope, and the conversion gain (CG) is calculated from (3.4).

$$CG(\text{dB}) = 10\log\left(V_{out}{}^{2}/50\right) - P_{in} \tag{3.4}$$

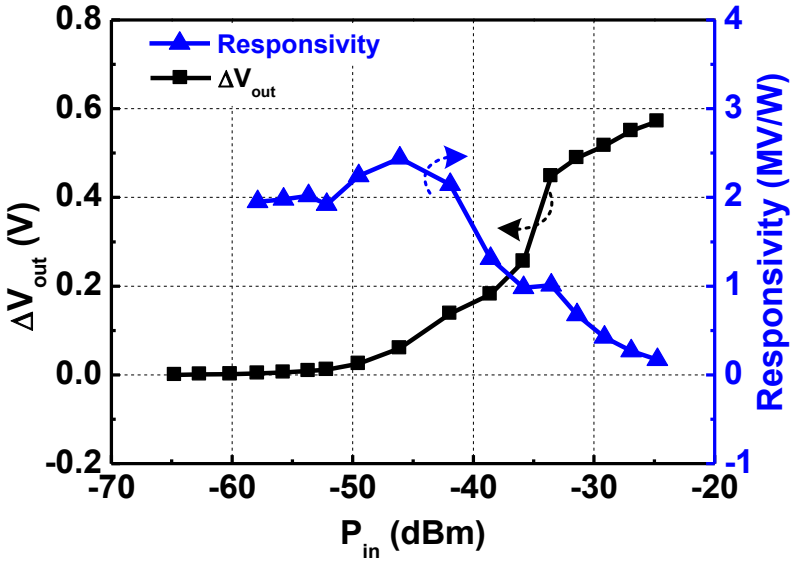


Figure 3.14 Output voltage and corresponding responsivity versus input power at 80 GHz

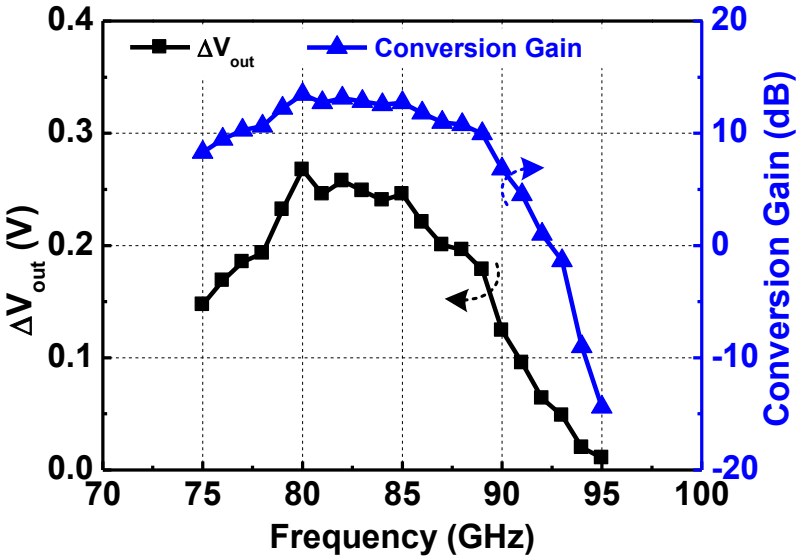


Figure 3.15 Output voltage and corresponding conversion gain versus input signal frequency with power level of -40 dBm

Two figure-of-merits are introduced for the comparison of imager sensitivity, NEP and $\Delta T_{\min}$. NEP is defined as the input signal power that makes a SNR of unit in one hertz output bandwidth. Smaller NEP means better sensitivity. $\Delta T_{\min}$ describes the change in temperature of a thermal source required to produce post detection SNR of unit. According the definitions, the NEP and $\Delta T_{\min}$ of Dicke receiver can be derived as (3.5) and (3.7), respectively.

$$NEP = \frac{V_n / \sqrt{B}}{V_{out} / S} = \frac{S}{\sqrt{B}} \tag{3.5}$$

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S / KT_0 B}{V_{out}^{\ 2} / V_n^{\ 2}} = \frac{S}{KT_0 B} \tag{3.6}$$

$$\Delta T_{\min} = \frac{2T_S}{\sqrt{B\tau}} = \frac{2T_0 \cdot (F-1)}{\sqrt{B\tau}} \tag{3.7}$$

where V_{out} is output voltage, V_n is output noise, K is the Boltzmann constant (K = 1.38×10^{-23} J/K), S is the injection power at sensitivity level, B is receiver bandwidth, T_S is system noise temperature in Kelvin, T_0 is the room noise temperature (290 K), and τ is integration time (typically 30 ms).

Calculated from (3.5)-(3.7), the NEP, NF, and $\Delta T_{\min}$ of the designed SDP-LNA-based Dicke receiver are 9.3 fW/Hz$^{0.5}$, 13 dB, and 0.65 K, respectively. Performance of the designed SDP-LNA is summarized in Table 3-4, and that of the SDP-LNA-based direct-detection Dicke receiver is summarized and compared to published mm-wave imaging receivers in Table 3-5. It is worth to mention that linearity is not a big concern for passive mm-wave imaging applications since the input signal, i.e., noise, collected by the antenna is quite low [65], [66]. Compared to the design specifications, the bandwidth of the receiver is much less than the design specification, which is mainly because of the mismatch between the LNA and power detector. The matching network is affected by the dummy metal fill and process variations, which were not fully considered. The degradation of the responsivity can be easily compensated by a low frequency amplifier. The prototype almost achieves the targeted NEP and ΔT_{min} with less power consumption.

Table 3-4 Performance summary of the SDP-LNA and comparison to state-of-the-art wideband mm-wave LNAs

Reference	Technology	Topology	Gain (dB)	BW* (GHz)	NF (dB)	Power (mW)	Size (mm^2)	FoM†
[45] MWCL′10	0.18-µm SiGe	2-stage cascode	14.5	14.5	6.9 - 8.0	37	0.41	0.39 - 0.53
[15] JSSC′11	0.18-µm SiGe	5-stage CE	19	19#	8.0 - 12#	63	1.00	0.18 - 0.51
[24] JSSC′13	0.13-µm SiGe	2-stage cascode	22.5	30	6.0 - 7.2#	52	0.52	1.81 - 2.58
			25	70#	6.2 - 9.0#	54	0.33	3.32 - 7.27
[36] JSSC′07	0.18-µm CMOS	Distributed	20	39.4	8.0 - 9.4	250	2.24	0.20 - 0.30
[37] TMTT′13	0.18-µm CMOS	Distributed	24	33	6.5 - 7.5	238	0.83	0.48 - 0.63
[38] TMTT′12	65-nm CMOS	Distributed	22	65	6.9 - 7.9	97	0.93	1.63 - 2.16
[39] IMS′15	0.18-µm CMOS	Distributed	25	34	6.5 - 8.0	176	0.86	0.65 - 0.99
[41] TMTT′12	45-nm SOI CMOS	3-stage CS	10.7	18	6.0 - 11	52	0.32	0.10 - 0.40
[42] JSSC′08	65-nm CMOS	3-stage cascode	13.5	20	6.4 - 9.0#	-	-	-
[43] EL′12	90-nm CMOS	3-stage cascode	14	23	4.8 - 7.0#	32	0.22	0.90 - 1.78
[18] JSSC′10	65-nm CMOS	5-stage cascode	27	13.5#	6.8 - 9.0#	36	-	1.21 - 2.22
[44] TMTT′15	28-nm CMOS	2-stage cascode	13.8	18	4.0 - 5.8	24	0.38	1.31 - 2.43
[46] IMS′12	65-nm CMOS	4-stage cascode	25.3	20 #	6.0 - 8.3	48	0.25	1.33 - 2.57
[47] ISSCC′09	65-nm CMOS	4-stage CS	14.8	21	7.5 - 9.0#	86	0.33	0.19 - 0.29
[10] JSSC′11	65-nm CMOS	3-stage cascode	15	12	7.0 - 10#	42	-	0.18 - 0.40
This Work	**65-nm CMOS**	**5-stage cascode**	**26.8**	**25.5**	**6.4 - 7.6**	**52.3**	**0.47**	**2.24 - 3.17**

* 3-dB bandwidth; # estimated value from figures; † based on Equation (2.23)

Table 3-5 Performance summary of the SDP-LNA-based Dicke receiver and comparison to state-of-the-art mm-wave imaging receivers

Reference	[10] JSSC'11	[15] JSSC'11	[17] TMTT'10	[18] JSSC'10	[62] EL'11	**This work**
Technology	65-nm CMOS	0.18-μm SiGe	0.12-μm SiGe	65-nm CMOS	65nm CMOS	**65-nm CMOS**
Integration	LNA Mixer PD BB	LNA RTPS PD BB	LNA SPDT PD	LNA SPDT PD	LNA PD PGA	**LNA PD**
3-dB BW (GHz)	11	26	14	18	-	**11.5**
NEP (fW/Hz$^{0.5}$)	8.8	10	21	36	26	**9.3**
ΔT_{min} (K, 30ms)	1	0.4	0.83	1.1	2.0	**0.65**
Responsivity (MV/W)	16	43	5	0.67	100[#]	**2.5**
Power (mW)	101.6	200	34.8	110	62	**52.6**
Area (mm^2)	3	12.5	0.4	0.4	0.55	**0.5**

PD = power detector; BB = baseband; [#] with programmable amplifier

3.5 Summary

In this chapter, the recent development of CMOS mm-wave imaging systems is reported together with their pros and cons. To improve the performance of mm-wave imagers, a novel direct-detection Dicke receiver with a switchable dual-path LNA (SDP-LNA) is designed and analyzed. Pole-converging technique for intra-stage bandwidth extension is adopted in the design of the SDP-LNA. Under a 1.8-V supply voltage, the SDP-LNA consumes 52.3 mW and exhibits peak power

gain of 26.8 dB, minimum NF of 6.4 dB, and 3-dB bandwidth of 25.5 GHz. Based on the SDP-LNA, a direct-detection Dicke receiver is implemented in a 65-nm CMOS technology. The prototype achieves NEP of 9.3 fW/Hz$^{0.5}$ and ΔT_{min} of 0.65 K with power consumption of 52.6 mW.

Chapter 4

Charge-Accumulation Super-Regenerative Receiver

Direct detection and heterodyne detection remain dominant in communications as they offer the advantages of coherent detection and recovery of phase information. Nevertheless, there is no need or value to detect the phase information for mm-wave imaging systems, which are based on power sensing. In addition, for an imaging focal plane array (FPA) with $n \times n$ pixels, the total power consumption and chip size will be inflated by a factor of n^2. Imaging pixel (receiver) with low power and small size significantly saves the system power consumption and fabrication cost. Therefore, the super-regenerative reception architecture becomes

a promising competitor in mm-wave imaging applications. This chapter explores ultra-low power and low cost design techniques for mm-wave imaging systems. A charge-accumulation technique is proposed in the design of super-regenerative imaging receiver. The theory of super-regenerative reception, implementation of charge-accumulation super-regenerative receiver (CA-SRR), and experimental results are reported.

4.1 Background and Literature Review

The super-regenerative conception dates back to the inventions of Edwin Armstrong in 1922 [67], [68]. Armstrong was one of the greatest inventors in the early radio communications, whose inventions have become the fundamental of all modern radio, radar, and television. Armstrong had invented the regenerative circuit (1912), the super-heterodyne circuit (1918), the super-regenerative circuit (1922), and the frequency modulation system (1933) [69]. Although the super-regenerative receiver has the drawback of low selectivity compared to its counterpart, the heterodyne receiver, this architecture is also widely used from radar identification of aircraft and ships in the wartime to modern wireless sensor networks [70]–[72].

Due to low cost, simple topology, and low power consumption, super-regenerative receivers are getting more and more attention in the field of low-power wireless data links. Based on super-regenerative principle and on-off keying (OOK) modulation, a 2.4 GHz ultra-low power OOK single-chip transceiver was proposed in [73] for wireless body-area network (WBAN) applications, which is a special purpose sensor network used for communication among sensors and appliances, located on, in or around the human body, such as for medical and healthcare purposes. Besides the OOK modulation, there are several works to apply the super-regenerative conception to phase shift keying (PSK) and quadrature phase shift keying (QPSK) modulations [74], [75]. Preserving the phase information of RF signals is one of the characteristics of super-regenerative oscillator, which is well-known but usually unexploited fact [74]. However, the excessive received bandwidth of super-regenerative architecture results in inferior frequency selectivity for narrowband communications. Nevertheless, it is particularly appropriate for ultra-wideband (UWB) communications. The super-regenerative topology is very sensitive to time-domain-located energy, which can be seemed as a time-domain filter where the received signal is collected and filtered, so it is well suitable for UWB impulse signals [76].

Recently, the super-regenerative principle is adopted in mm-wave imaging receivers [21], [22], [35], [77], and the performance of state-of-the-art super-regenerative imaging receivers is summarized in Table 4-1. Because of the aggressive progress of CMOS technology, the f_T/f_{MAX} of transistors is greatly improved, leading to higher working frequency of super-regenerative oscillators. For advanced CMOS technology, the intrinsic device gain is very limited compared to III-V devices; however, super-regeneration provides extraordinary gain, which comes from the growth of oscillation. Besides, the super-regenerative circuits offer low power consumption and small circuit area, making it very attractive for multi-pixel mm-wave imaging systems. In [22], a time-encoded regenerative receiver (TRR) was proposed for mm-wave imaging applications with simple architecture and low power consumption. The regenerative receiver of the proposed TRR is controlled by a digital CMOS circuitry, and in each cycle, the TRR generates a time-encoded output signal. When the oscillator is engaged by the clock, the envelope of the oscillation begins to increase. Once it exceeds a designed threshold, a reset signal would be generated and the oscillation is terminated. The time between set and reset is inversely proportional to the incident signal power. However, the buildup process of SRO is extremely rapid, thus the time difference is small and hard to capture, especially at higher frequencies. In [77], an inter-modulated regenerative receiver (IRR) for tri-color mm-wave imaging was presented. In this topology, a conventional regenerative

receiver is employed as regenerative oscillator, which is quenched by the quench signal. A free-running oscillator at a lower frequency is directly injected into the regenerative oscillator. Because of high non-linearity, the injection of free-running oscillator creates inter-modulation between the two frequencies within the regenerative oscillator, thus additional receiving bands are achieved. The great advantage of such architecture is that the receiver is able to operate beyond f_{MAX}, which is not possible for traditional receivers. Nevertheless, this imaging receiver has relatively low sensitivity to the changes of input power level. A video amplifier could be used to amplify its output, but inevitably increases the overall receiver power consumption.

Table 4-1 Performance summary of state-of-the-art mm-wave imaging receivers based on super-regenerative reception

Reference	[9]	[10]	[18]	[21]	[22]
Technology	65nm CMOS	65nm CMOS	65nm CMOS	65/40nm CMOS	65nm CMOS
Frequency (GHz)	140	81-91	81-93	349/495	183
NEP (fW/Hz$^{0.5}$)	53	9	36	668/108*	1.51*
ΔT_{min} (K, 30ms)	1.5	1	1.1	n/a	0.45#
Responsivity (MV/W)	0.6	16.15	0.67	187/3180	1.3†
Power (mW)	152	101.6	110	18.2/5.6	13.5
Area (mm^2)	0.228	3	0.4	0.45/0.11	0.013

*calculated from (4.21); #calculated from (4.23); †time encoded (ms/W).

To improve the sensitivity of SRR, the theory of super-regenerative receiver is analyzed, and a charge-accumulation technique is proposed in the design of SRR for mm-wave imaging applications.

4.2 Theory of Super-Regenerative Receiver

The operation concept of super-regeneration is quite straightforward; however, the mathematical analysis is very complex because of the nonlinear and time-varying nature of the SRR. A generic approach to the theory of super-regenerative receiver was presented by F.Xavier Moncunill-Geniz in 2005 [70]. And more recent works have further discussed the theory of SRR in the frequency domain [78], [79].

4.2.1 Block Diagram of SRR

Figure 4.1 shows the detailed block diagram of the super-regenerative receiver. The variables shown in this figure represent the input and output voltages, which should be changed to current depending on different cases. The core of super-regenerative receiver is the super-regenerative oscillator (SRO). Different from the general oscillators, which are expected to work in steady state, providing a stable periodic signal for RF communication systems, the SRO actually is a RF

oscillator controlled by quench oscillator at much lower frequency compared to the free oscillation frequency of the SRO. As a dynamic circuit, the SRO also presents transient response before reaching its maximum oscillation value. This transient response is used to filter and amplify weak RF signals, which is the principle of any super-regenerative receivers.

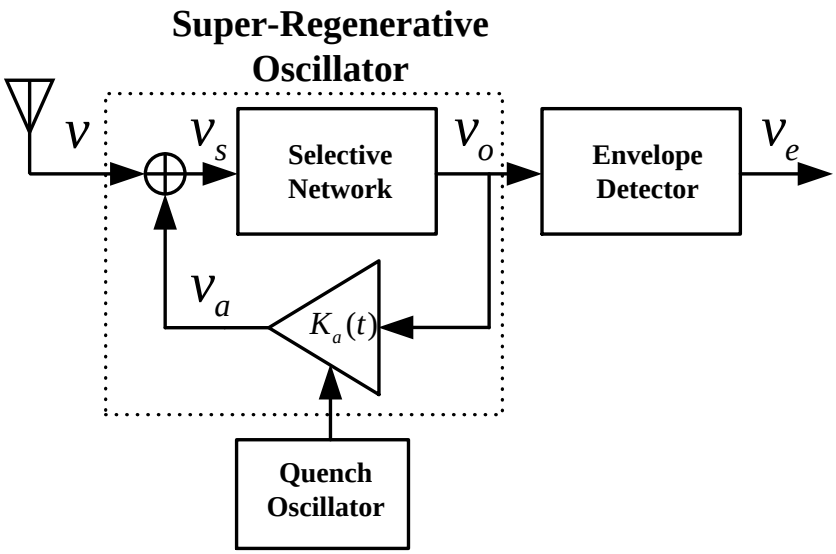


Figure 4.1 Block diagram of the super-regenerative receiver

The SRO is modeled as a selective band-pass filter fed back through a time-varying amplifier. The gain of the amplifier is controlled by the quench signal, which quenches the oscillation periodically. Without any incident RF signal, the oscillation is built up by thermal noise in a quite slow process, while the buildup process becomes much faster when RF signal with sufficient energy is injected

into the oscillator. Thus, the waveform of the oscillation consists of a series of RF pulses separated by the quench period, and the buildup time of the oscillator can be used as an indicator of the strength of incident RF signal.

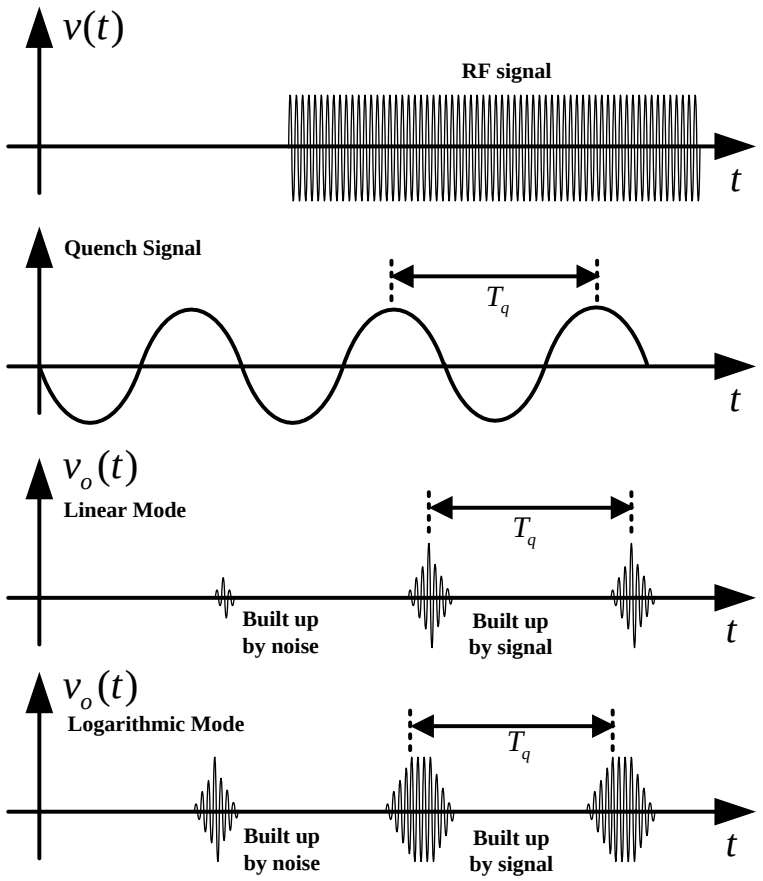


Figure 4.2 SRO's input RF signal, quench signal, output voltage in the linear and logarithmic mode.

Depending on the decay time of the super-regenerative oscillation, the operation of SRR is classified into two categories: linear mode and logarithmic mode.

Figure 4.2 shows the typical waveforms of super-regenerative receiver in the two modes. In the linear mode, the transient oscillation exponentially grows, but is damped before reaching the steady-state. The peak amplitude is proportional to the amplitude of the incident RF signal. When operating in the logarithmic mode, the oscillator is allowed to reach its maximum value, which is determined by the nonlinearity of the feedback amplifier and the supply voltage. The peak amplitude of output signal does not change, but the incremental area under the envelope is proportional to the logarithm of the strength of the injected RF signal.

4.2.2 Circuit Model and Analysis

The super-regenerative receiver has been modeled as a band-pass network fed back through a time-varying amplifier, which is controlled by a quench signal. Without loss of generality, the frequency selective network is assumed to have two dominant poles with a band-pass response centered at ω_0. Figure 4.3 shows the simplified parallel *RLC* circuit model of super-regenerative receiver, which is commonly used to analyze the behavior of SRO. The main parameters of the SRO circuit model are: resonant frequency ω_0, quality factor Q_0, characteristic impedance Z_0, and quiescent damping factor ζ_0. The following expressions can be derived:

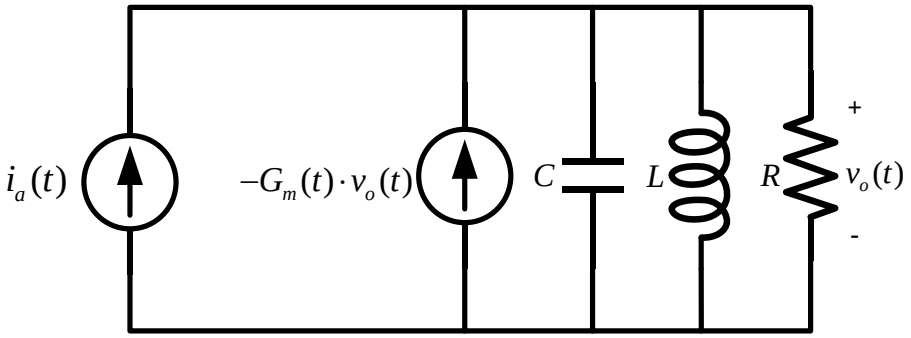


Figure 4.3 Simplified parallel *RLC* circuit model of super-regenerative receiver.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.1}$$

$$Q_0 = \frac{1}{\omega_0 RC} = \frac{\omega_0 L}{R} \tag{4.2}$$

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{1}{\omega_0 C} = \omega_0 L \tag{4.3}$$

$$\zeta_0 = \frac{\omega_0 RC}{2} = \frac{R}{2\omega_0 L} = \frac{1}{2Q_0} = \frac{Z_0}{2R} \tag{4.4}$$

Then, the impedance of the parallel *RLC* circuit can be expressed as:

$$Z_{RLC}(s) = \frac{Z_0 \omega_0 s}{s^2 + 2\zeta_0 \omega_0 s + \omega_0^2} \tag{4.5}$$

On the condition that $G_m(t)$ varies slowly enough with respect to ω_0, the transfer function of SRO can be expressed as:

$$H(s,t)=\frac{V_o(s,t)}{I_a(s)}=\frac{Z_{RLC}(s)}{1-G_m(t)\cdot Z_{RLC}(s)}=\frac{Z_0\omega_0 s}{s^2+2\zeta(t)\omega_0 s+\omega_0^{\ 2}} \tag{4.6}$$

Where $\zeta(t)$ is the damping function and defined as:

$$\zeta(t)=\zeta_0(1-G_m(t)\cdot R) \tag{4.7}$$

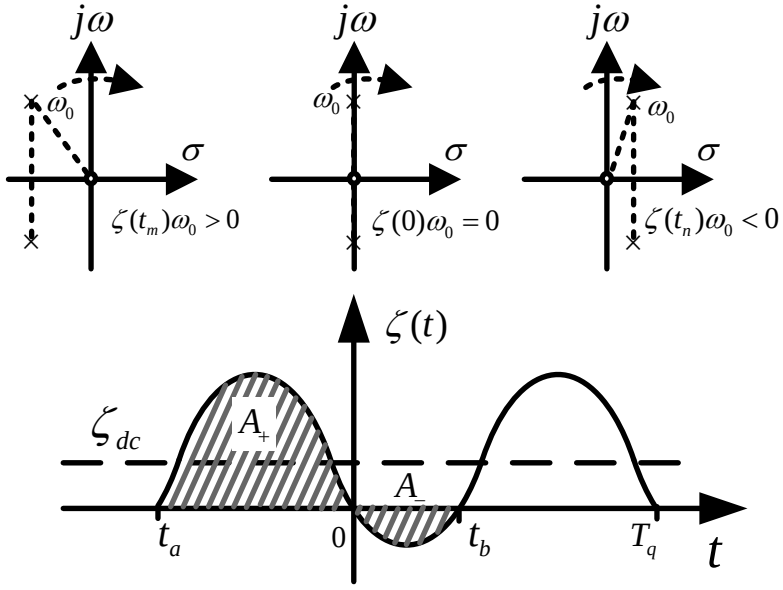


Figure 4.4 Pole and zero locations of the SRR change with the damping function.

The only difference between (4.5) and (4.6) locates in the denominator where ζ_0 is replaced by $\zeta(t)$. Thus, the feedback from trans-conductance $G_m(t)$ can be viewed as a negative resistance that only affects the damping function of the super-regenerative oscillator, and the SRR is modeled as a time-varying, second-order system. Unlike the linear time-invariant systems, the locations of pole and zero of SRR shifted between the left-hand side and the right-hand side of the complex plane periodically, due to the time-varying damping function $\zeta(t)$, as shown in Figure 4.4. The time-varying damping function leads to the buildup (negative $\zeta(t)$, A_-) and decay (positive $\zeta(t)$, A_+) of the oscillation periodically. In each cycle, the transient response of the SRR is used to filter and amplify the incident weak RF signal.

As discussed in the beginning, there are two operation modes of super-regenerative receiver: linear mode and logarithmic mode, depending on whether the oscillator is allowed to reach its maximum steady-state value. The Analysis of operation in the logarithmic mode is quite complex, and the following mathematical analysis is valid for the linear mode.

Since $\zeta(t)$ varies slowly enough with respect to ω_0, which is regarded as a constant in order to simplify the mathematical analysis., the super-regenerative receiver is characterized by the simplified differential equation:

$$v_o^{''}(t) + 2\zeta(t)\omega_0 v_o^{'}(t) + \omega_0^2 v_o(t) = 2R\zeta_0\omega_0 i_a^{'}(t) \tag{4.8}$$

The general solution of (4.8) can be expressed as the sum of the general solution of homogeneous equation and particular solution of the complete equation, namely the free response and the forced response:

$$v_o(t) = v_{oh}(t) + v_{op}(t) \tag{4.9}$$

Where $v_{oh}(t)$ is the free response, $v_{op}(t)$ is the forced response.

In practical applications, the free response is zero, which means the oscillation is completely quenched before the startup of a new cycle. Otherwise, the proceeding remnant oscillation will greatly affect the buildup of oscillation in the next cycle, which indicates that it shows little or no sensitivity to the input RF signal. Such phenomenon is called hangover, which must be avoided in order to ensure the oscillation in present cycle only depend on the incident RF signal. The sufficient quench can be achieved by pushing the poles far to the left-hand side, in other words, the damping function need to have a large positive value A_+, shown in Figure 4.4.

According to the general solution in [70], we can get the general expression of SRR's output voltage in the linear mode by changing the input voltage to input current:

$$v_o(t) = v_{op}(t) = e^{-\omega_0 \int_{t_a}^{t} \zeta(\lambda) d\lambda} \times 2\,\mathrm{Re}\left[-jR\zeta_0 \int_{t_a}^{t} i_a^{'}(\tau) e^{\omega_0 \int_{t_a}^{\tau} \zeta(\lambda) d\lambda} e^{j\omega_0 (t-\tau)} d\tau \right] \quad (4.10)$$

In order to get a compact expression, some parameters in literature can be reused:

- Super-regenerative gain:

$$K_s = e^{-\omega_0 \int_0^{t_b} \zeta(\lambda) d\lambda} \quad (4.11)$$

- Normalized envelope of SRR output voltage:

$$p(t) = e^{-\omega_0 \int_{t_b}^{t} \zeta(\lambda) d\lambda} \quad (4.12)$$

- Sensitivity curve:

$$s(t) = e^{\omega_0 \int_0^{t} \zeta(\lambda) d\lambda} \quad (4.13)$$

Then, the output voltage of SRR can be expressed as:

$$v_o(t) = 2R\zeta_0 K_s p(t) \int_{t_a}^{t} i_a^{'}(\tau) s(\tau) \sin \omega_0 (t-\tau) d\tau \quad (4.14)$$

Suppose that incident RF signal is expressed as (4.15), which is only received in the interval (t_a, t_b), and the carrier frequency is the resonant frequency.

$$i_a(t) = Ip_c(t) \cos(\omega_0 t + \phi) \quad (4.15)$$

Where $p_c(t)$ is the normalized pulse envelope and I is the peak current. $p_c(t)$ is supposed to be zero beyond the interval (t_a, t_b). Then the response of the super-regenerative receiver is:

$$v_o(t) = IRK_s K_r p(t)\cos(\omega_0 t + \phi) \tag{4.16}$$

Where K_r is the regenerative gain, expressed as:

$$K_r = \zeta_0 \omega_0 \int_{t_a}^{t_b} p_c(\tau) s(\tau) d\tau \tag{4.17}$$

The regenerative gain illustrates that sensitivity curve $s(t)$ acts as the function that weights the incoming signal envelope $p_c(t)$. Thus, the more energy concentrates around the peak of the sensitivity curve, the higher regenerative gain the receiver presents.

4.3 Implementation of CA-SRR

Instead of directly detecting the oscillation buildup time (logarithmic mode) or peak amplitude (linear mode) of SRO, a charge-accumulation (CA) technique is proposed in the design of a 100-GHz linear-mode SRR. By accumulating the output charge of peak detector, the output voltage is greatly enhanced, leading to extremely high responsivity and sensitivity with ultra-low power consumption.

Furthermore, a new power-injection method is adopted without loading the *LC*-tank of SRO. Figure 4.5 shows the schematic of the proposed CA-SRR, which consists of a super-regenerative oscillator, a peak detector with a current mirror and a load capacitor, and a quench controller.

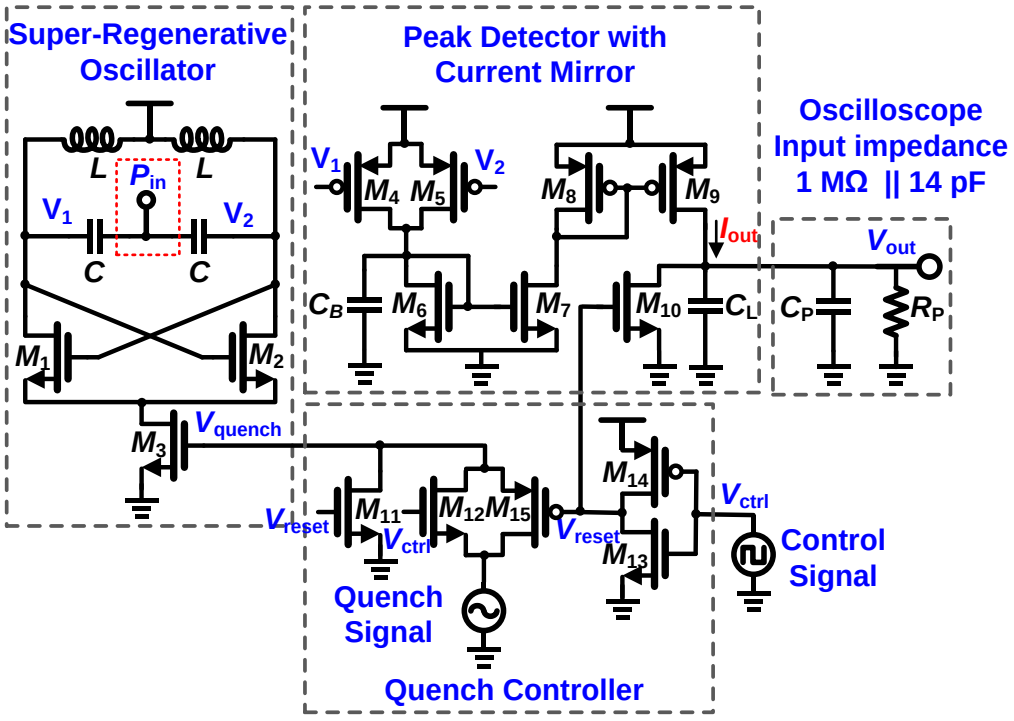


Figure 4.5 Schematic of the proposed charge-accumulation super-regenerative receiver (nets with the same label are connected together).

M_1-M_2, L, and C form the SRO with a free-running frequency of 100 GHz. The core of CA-SRR is the SRO, which is an RF oscillator controlled by a low-frequency quench signal, quenching the oscillation periodically. The buildup time

of oscillation is affected by the power level of input RF signal, while the oscillation is controlled by a quench signal through changing the bias of the tail current source M_3. M_4, M_5, C_B, and diode-connected M_6 compose the peak detector, which operates similarly to a diode-based rectifier, extracting the RMS power information from the super-regenerative oscillation. The C_B is a bypass capacitor to filter out the fundamental frequency of SRO and its harmonics. The diode-connected M_6 is part of current mirror, thus the output current of peak detector is copied to the load capacitor C_L. A quench controller is introduced to control the quench signal and reset signal. M_{13} and M_{14} form an inverter, and M_{12} and M_{15} compose a transmission gate controlled by the control signal, V_{ctrl}. When V_{ctrl} is high, the SRO is enabled and C_L is repeatedly charged by the output current of peak detector. When V_{ctrl} changes to the low state, the SRO is disabled to prevent introducing charge into the load capacitor, and C_L is reset for the next cycle. All the design parameters are listed in Table 4-2.

Table 4-2 Component parameters of CA-SRR

L	C	C_B	C_L	$M_{1\text{-}2}$	M_3
60 pH	13 *f*F	200 *f*F	20 pF	5/0.06	20/0.06
$M_{4\text{-}5}$	$M_{6\text{-}7}$	$M_{8\text{-}9}$	$M_{10\text{-}11}$	$M_{12\text{-}13}$	$M_{14\text{-}15}$
8/0.06	5/0.30	10/0.30	10/0.06	1.5/0.06	3/0.06

Transistors: W/L (μm/μm)

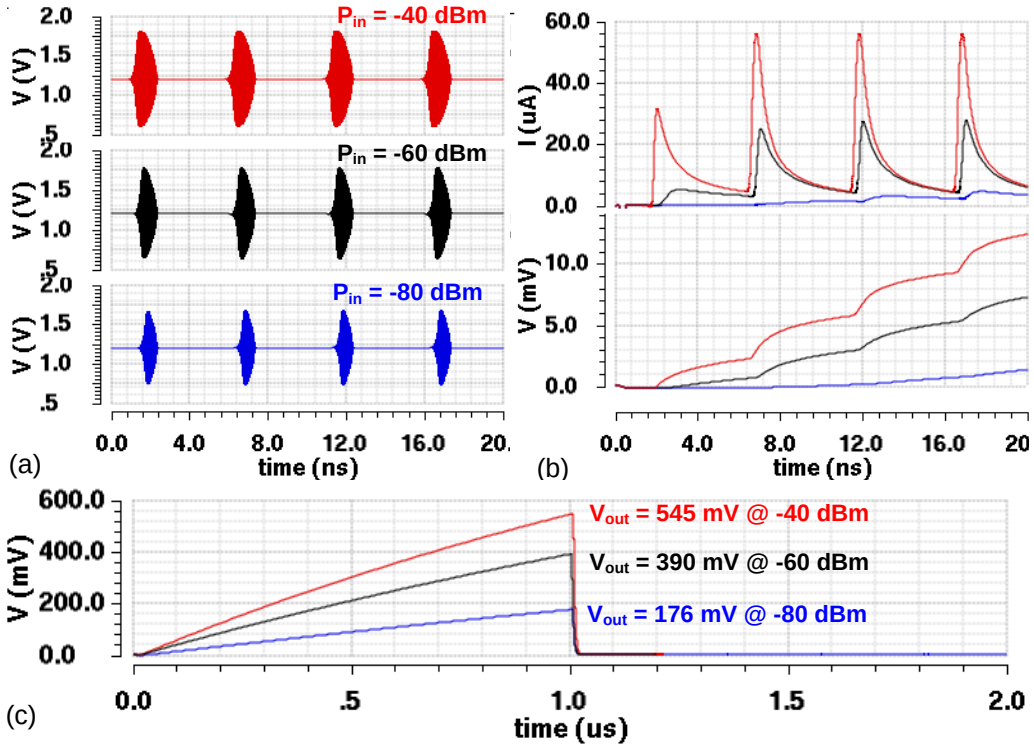


Figure 4.6 Simulated transient responses of CA-SRR at different injection power levels: (a) transient responses of SRO under a 200-MHz quench signal, (b) output currents of peak detector and charging process of the load capacitor, (c) output voltages under a reset period of 2 μs.

Note that a new power injection method is adopted, as shown in Figure 4.5. The conversional power injection is implemented by a single common-source (CS) amplifier, which has no gain but prevents the low impedance antenna from loading the SRO [21]. However, this amplifier increases the power consumption and introduces imbalance to the *LC*-tank. Besides, the reverse isolation of CS amplifier is poor due to the parasitic gate-drain capacitance at mm-wave frequencies. The oscillation of SRO will coupled to the antenna, leading to strong

interferences to other adjacent pixels in the FPA. In the proposed CA-SRR, as shown Figure 4.5, the input signal is injected into the common-mode node of two capacitors and is coupled to the *LC*-tank though capacitive coupling without loading the SRO. Thanks to the balanced operation of SRO, the fundamental frequency is greatly suppressed at the common-mode node.

Figure 4.6 illustrates the simulated transient responses of the proposed 100-GHz CA-SRR with component parameters listed in Table 4-2. A 200-MHz quench signal is adopted to make the SRR work in the linear mode. With the increasing of input power level, the buildup process of the SRO becomes faster and the peak value of output current increases, as a result, the output voltage increases.

Since the SRO keeps operating in the linear mode, a linear relationship between the average value of output current I_{out} and input power P_{in} can be assumed as:

$$I_{out} = \alpha \cdot P_{in} \tag{4.18}$$

where α is a constant determined by the nonlinearity of the SRO, related to (4.16). Then the output voltage V_{out} of the CA-SRR can be expressed as:

$$V_{out} = \frac{I_{out} \cdot \beta \cdot T_R / 2}{C_L + C_P} = \frac{\alpha \beta T_R P_{in}}{2\left(C_L + C_P\right)} \tag{4.19}$$

where T_R is the period of reset signal with 50% duty cycle, β is the ratio between the effective charging time per quench cycle and the quench signal period, which is determined by the dumping function, as shown in Figure 4.4. By increasing the reset signal period, or reducing the load capacitance, the output voltage is greatly enlarged, as well as the responsivity of the CA-SRR, which is defined by the ratio of output voltage divided by the input power. However, small C_L is fully charged quickly, thus the resolution is unacceptably degraded for a given reset period. In practice, a large C_L is utilized with a low-frequency reset signal. Therefore, C_L can absorb more current pulses before saturation. As a result, the output voltage difference under various input power levels is also accumulated, enhancing the responsivity and resolution.

4.4 Experimental Results

Figure 4.7 shows the die micrograph of the fabricated CA-SRR in GlobalFoundries 65-nm CMOS technology, which occupies silicon area of 0.50 mm × 0.81 mm with a core area of 0.023 mm^2. Under a power supply of 1.2 V, the CA-SRR presents power consumption of 0.9 mW.

Figure 4.8 depicts the measurement setup of the proposed CA-SRR. An mm-wave signal source chain is utilized to generate the input RF signal with variable power

levels. This setup is composed of a microwave signal generator, an active multiplier (×6) with output power of ~12 dBm, a tunable attenuator with maximum attenuation of 40 dB, and a fixed 40-dB attenuator. Before testing the CA-SRR, point A was directly connected to a W-band power meter to measure the power level. By tuning the attenuator, different levels of input power were obtained. The quench signal and reset signal are provided by an arbitrary waveform generator. The output voltage of the receiver is captured by an oscilloscope. Figure 4.9 shows the output waveforms of the CA-SRR under 100-GHz input signal with different input power levels.

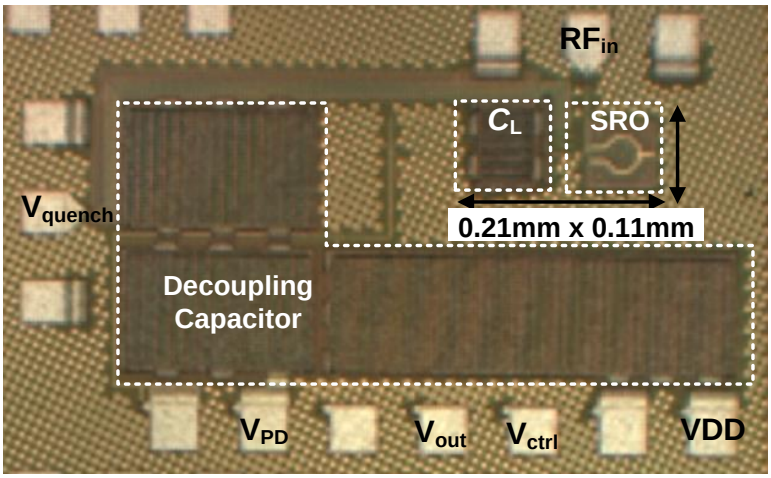


Figure 4.7 Die micrograph of the CA-SRR.

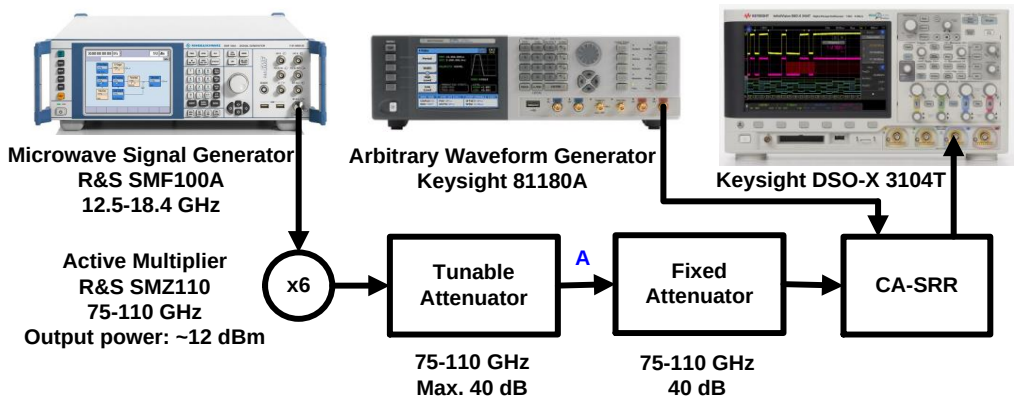


Figure 4.8 Measurement setup of the CA-SRR.

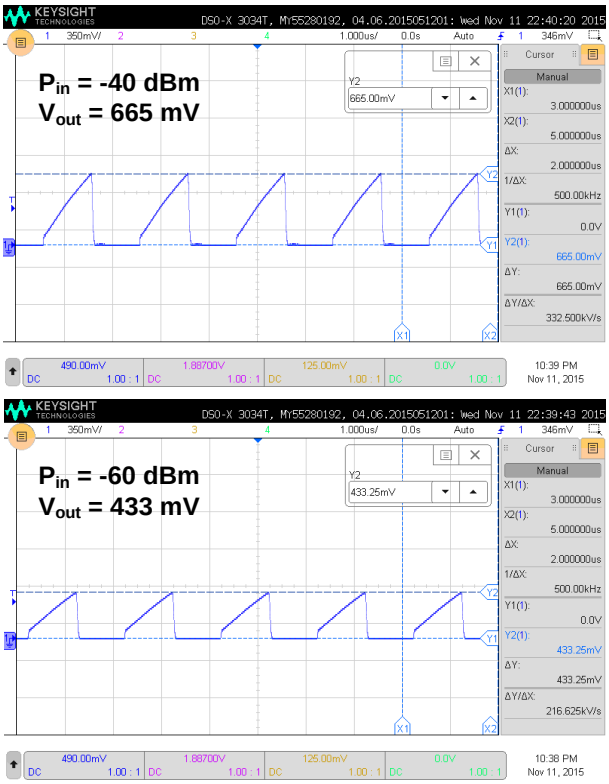


Figure 4.9 Output waveforms of the CA-SRR under 100-GHz input signal with different power levels.

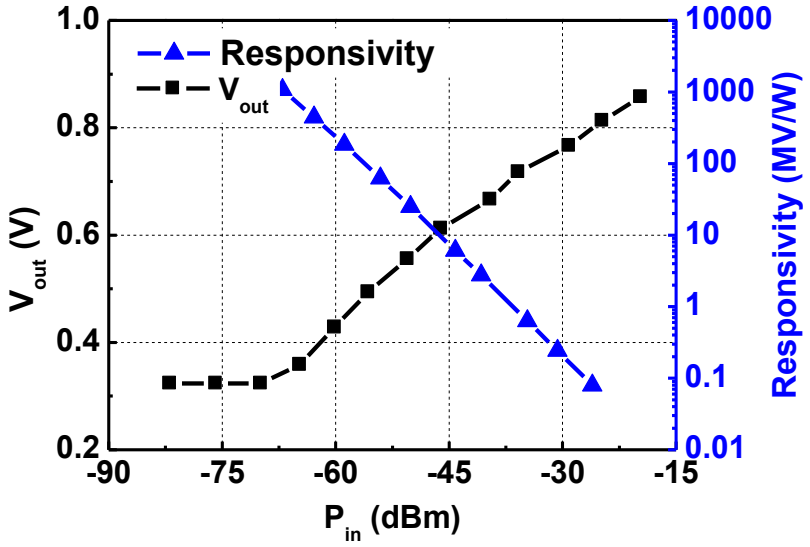


Figure 4.10 Output voltage and corresponding responsivity versus input power at 100 GHz

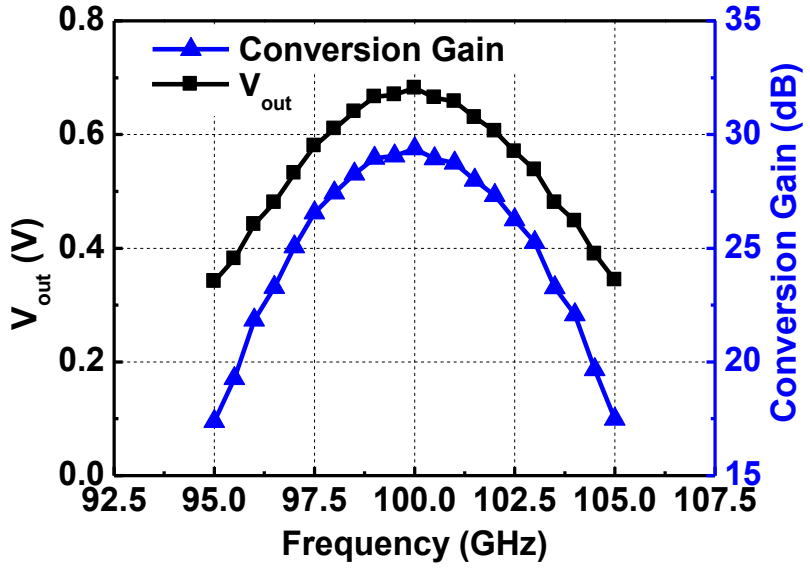


Figure 4.11 Output voltage and corresponding conversion gain versus input signal frequency with power level of -40 dBm.

Figure 4.10 and Figure 4.11 illustrates the output voltages of CA-SRR under input RF signal with various power levels and frequencies, respectively. To characterize the input power sensitivity and responsivity of the proposed CA-SRR, the power level of a 100-GHz input signal is swept from -20 dBm to -80 dBm. Due to the system noise, the buildup process becomes faster than that of simulation, so a 250-MHz quench signal is used. The CA-SRR achieves a sensitivity of -67 dBm and a responsivity of 1068 MV/W under a reset signal with period of 2 μs, as shown in Figure 4.10. Note that the responsivity is inversely proportional to the input power. Due to the effect from receiver noise, the buildup process is much faster, and the sensitivity is greatly degraded by the noise. The receiver demonstrates 3-dB bandwidth of 5 GHz and peak conversion gain of 29.5 dB, as depicted in Figure 4.11. To characterize the receiver bandwidth, a -40-dBm RF signal is injected into the CA-SRR with frequency being swept from 95 GHz to 105 GHz. The output voltage is recorded by the oscilloscope, and the conversion gain (CG) is calculated from (4.20).

$$CG(\mathrm{dB}) = 10\log\left(V_{out}{}^{2}/50\right) - P_{in} \tag{4.20}$$

Two figure-of-merits are introduced for the comparison of imager sensitivity, NEP and $\Delta T_{\min}$. NEP is defined as the input signal power that makes a SNR of unit in one hertz output bandwidth [10], [21]. $\Delta T_{\min}$ describes the change in temperature of a thermal source required to produce post detection SNR of unit.

According the definitions, the NEP and $\Delta T_{\min}$ can be derived as (4.21) and (4.23), respectively. Smaller values indicate better sensitivity.

$$NEP = \frac{V_n / \sqrt{B}}{V_{out} / S} = \frac{S}{\sqrt{B}} \tag{4.21}$$

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S / KT_0 B}{V_{out}^{\ 2} / V_n^{\ 2}} = \frac{S}{KT_0 B} \tag{4.22}$$

$$\Delta T_{\min} = \frac{T_S}{\sqrt{B\tau}} = \frac{T_0 \cdot (F - 1)}{\sqrt{B\tau}} \tag{4.23}$$

where V_{out} is output voltage, V_n is output noise, K is the Boltzmann constant (K = 1.38×10^{-23} J/K), S is the injection power at sensitivity level that results in SNR_{out} of unit (V_{out} equals to V_n), B is the receiver bandwidth, T_S is the system noise temperature in Kelvin, T_0 is the room noise temperature (290 K), and τ is integration time (typically 30 ms). Calculated from (4.21)-(4.23), the NEP, NF, and $\Delta T_{\min}$ of the CA-SRR are 2.8 fW/Hz$^{0.5}$, 10 dB, and 0.21 K, respectively.

Performance of the proposed CA-SRR is summarized and compared to state-of-the-art mm-wave imaging receivers in Table 4-3. The CA-SRR exhibits the best $\Delta T_{\min}$, lowest power consumption, and compact size.

Table 4-3 Performance summary of CA-SRR and comparison to state-of-the-art mm-wave imaging receivers

Reference	[9]	[10]	[18]	[21]	[22]	**This work**
Technology	65nm CMOS	65nm CMOS	65nm CMOS	65/40nm CMOS	65nm CMOS	**65nm CMOS**
Frequency (GHz)	140	81-91	81-93	349/495	183	**100**
NEP (fW/Hz$^{0.5}$)	53	9	36	668/108[*]	1.51[*]	**2.8[*]**
ΔT_{min} (K, 30ms)	1.5	1	1.1	n/a	0.45[#]	**0.21[#]**
Responsivity (MV/W)	0.6	16.15	0.67	187/3180	1.3[†]	**1068**
Power (mW)	152	101.6	110	18.2/5.6	13.5	**0.9**
Area (mm^2)	0.228	3	0.4	0.45/0.11	0.013	**0.023**

*calculated from (4.21); [#]calculated from (4.23); [†]time encoded (ms/W).

4.5 Summary

A charge-accumulation technique and a new injection method were adopted in the design of a 100-GHz SRR. The fabricated CA-SRR achieves high responsivity of 1068 MV/W and excellent radiometer resolution of 0.21 K with ultra-low power consumption of 0.9 mW and small core size of 0.023 mm^2. Focal plane arrays using the implemented CA-SRR will significantly enhance the sensitivity, reduce the fabrication cost, and save system power consumption.

Chapter 5

Conclusions and Future Work

In this chapter, the conclusions of the whole dissertation will be drawn and some recommendations for the future work will be presented.

5.1 Conclusions

The author's research work is focused on the CMOS integrated circuits for mm-wave imaging applications. Two broadband LNAs in 65-nm CMOS for mm-wave imaging receivers were proposed and analyzed. One is based on part peak-gain distribution, and the other is based on pole-converging technique. A direct-

detection Dicke receiver was designed based on a novel SDP-LNA, which eliminates the sensitivity degradation due to the insertion loss of Dicke switch. In addition, charge-accumulation technique was proposed in the design of ultra-low-power and low-cost mm-wave super-regenerative receiver. All the proposed designs were verified through on-wafer measurements and competitive results were obtained.

Firstly, two wideband LNAs for mm-wave imaging receivers in 65-nm CMOS were reported. The first one is a five-stage cascode LNA based on part peak-gain distribution technique. By distributing the peak gains of first four stages at two frequency points, the LNA achieves a flat gain response over a wide bandwidth. The measurement results show that the amplifier features peak gain of 16.7 dB at 104 GHz, minimum NF of 7.2 dB, and 3-dB bandwidth of 21.5 GHz. The LNA consumes 48.6 mW and occupies a compact core area of 0.05 mm^2. The second one is a three-stage cascode LNA based on a novel pole-converging technique for intra-stage bandwidth extension. The bandwidth is significantly extended by the proposed technique without increasing power consumption and die size. The fabricated prototype features peak gain of 18.5 dB, minimum NF of 5.5 dB, and 3-dB bandwidth of 30 GHz with power consumption of 27 mW. To the author's best knowledge, this LNA achieves the widest 3-dB bandwidth and the best FoM

among multi-stage mm-wave LNAs in CMOS technologies. Figure 5.1 illustrates the FoM of the proposed LNAs and the state-of-the-art mm-wave LNAs in CMOS.

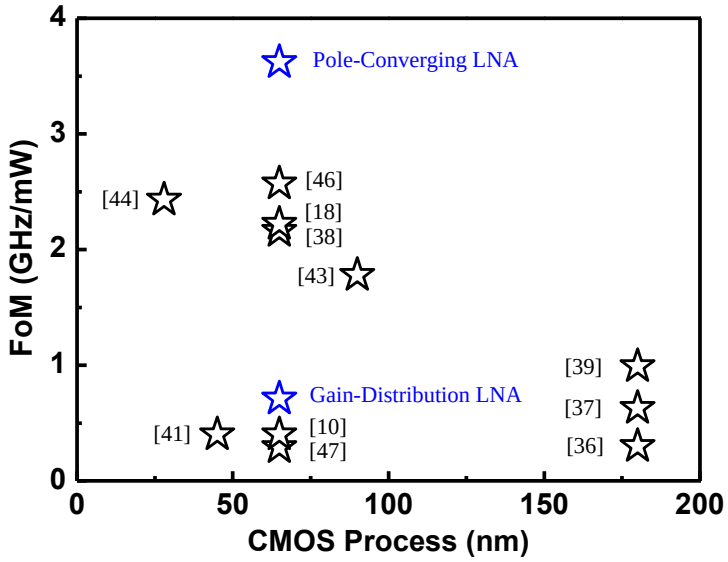


Figure 5. 1 FoM of the proposed LNAs and the state-of-the-art mm-wave LNAs in CMOS.

Secondly, a SDP-LNA-based direct-detection Dicke receiver for mm-wave imaging systems was demonstrated. Pole-converging technique for intra-stage bandwidth extension was adopted in the design of the SDP-LNA. Thanks to the internal switching of SDP-LNA, the sensitivity degradation due to the insertion loss of Dicke switch is eliminated. Under a 1.8-V supply voltage, the standalone SDP-LNA consumes 52.3 mW and exhibits peak power gain of 26.8 dB, minimum NF of 6.4 dB, and 3-dB bandwidth of 25.5 GHz. The SDP-LNA-based

direct-detection Dicke receiver achieves NEP of 9.3 fW/Hz$^{0.5}$ and ΔT_{min} of 0.65 K with total power consumption of 52.6 mW.

Thirdly, a CA-SRR in 65-nm CMOS was presented. By accumulating the output charge of peak detector, the output voltage is greatly enhanced, leading to extremely high responsivity and sensitivity with ultra-low power consumption. The fabricated CA-SRR achieves high responsivity of 1068 MV/W, NEP of 2.8 fW/Hz$^{0.5}$ and ΔT_{min} of 0.21 K with ultra-low power consumption of 0.9 mW and small size of 0.023 mm^2.

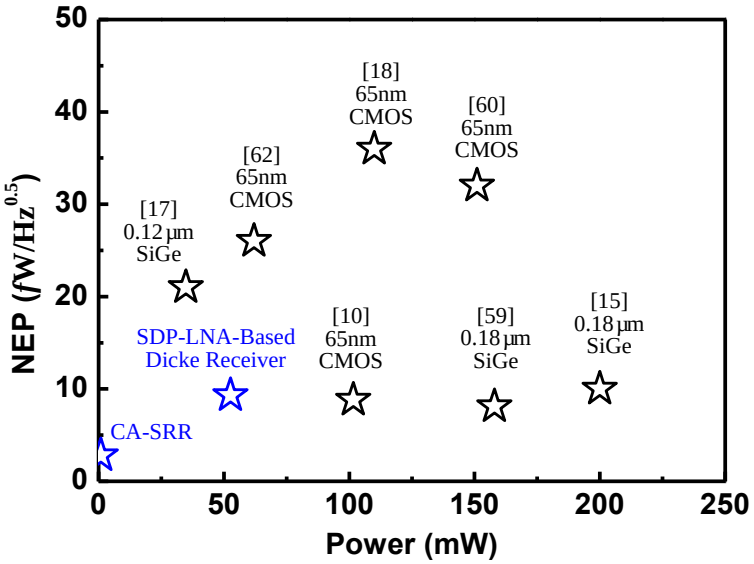


Figure 5. 2 NEP and power consumption of the proposed imaging receivers and the state-of-the-art mm-wave imagers.

Figure 5.2 shows the NEP and power consumption of the proposed imaging receivers and the state-of-the-art mm-wave imagers in CMOS. Compared to the published mm-wave imagers, the SDP-LNA-based Dicke receiver achieves a comparable NEP with lower power consumption. Nevertheless, power consumption of the proposed Dicke receiver is more than 50 mW, and chip size is quite large. The proposed CA-SRR presents a NEP of 2.8 fW/Hz$^{0.5}$ with power consumption of 0.9 mW, which is much better than previous works. Focal plane arrays using the implemented CA-SRR will significantly enhance receiver resolution, reduce fabrication cost, and save system power consumption.

5.2 Recommendations for Future Work

In this research, several integrated circuits for mm-wave imaging applications were implemented in GlobalFoundries 65-nm CMOS technology, and all the prototypes demonstrated excellent performance. Nevertheless, there are several recommendations and improvements for the future work.

First, although the proposed SDP-LNA is adopted to design a direct-detection Dicke receiver for mm-wave imaging systems, the SDP-LNA can be extended to the design of switchable multiband LNA for multiband applications, such as imaging, automatic radar, and other communication systems. The design

challenge of multiband LNA is to configure the matching networks for different frequency bands without degrading RF performance, especially NF. The input and output matching networks of conventional multiband LNAs are tunable or switchable to achieve multiband frequency response. However, it is hard to achieve low NF under each band, which is greatly affected by the input matching. One method to alleviate this problem is to adopt the proposed SDP-LNA. Since the NF of LNA is mainly determined by the first two stages, the two switchable branches is configured at separated operation frequencies, achieving power matching and noise matching, respectively. The shared stages use the traditional methods to obtain multiband operations. Therefore, it is possible to achieve high performance multiband amplifiers based on the proposed SDP-LNA.

Second, antenna is an indispensable component for imaging systems. Patch antenna and dipole antenna are two widely used on-chip antennas. However, CMOS on-chip antenna exhibits relatively low radiation efficiency and gain. Thus, to improve on-chip antenna performance, new design technique or antenna structure should be explored. Integrated with on-chip antennas and digital circuitry, it is possible to design a focal plane array with low cost and low power consumption using the proposed CA-SRR presented in Chapter 4.

Third, the operation frequency of imaging systems will be pushed towards to terahertz (THz) (300 GHz – 3 THz). This spectrum range is called THz gap,

loosely describing the lack of adequate technologies to effectively bridge this transition region between electronics and optics. However, advanced CMOS technology makes the implementation of THz imaging system possible. Due the extremely short wavelength, the spatial resolution of imaging system is significantly enhanced, leading to more distinct imaging, which can be used for tumor recognition, genetic screening, and spectroscopy. Furthermore, the size of passive components is greatly reduced, such as antennas and inductors. Nevertheless, due to high substrate losses, inductor quality factor and antenna gain are relatively low; besides, the device gain is quite limited. Given all the promising applications and technical challenges, THz imaging in CMOS technology is a new exciting research area.

Author's Publications

1. **G. Feng**, C. C. Boon, F. Meng, X. Yi, and C. Li, "An 88.5-110 GHz CMOS Low-Noise Amplifier for Millimeter-wave Imaging Applications," *IEEE Microw. Compon. Lett.*, vol. 26, no. 2, pp. 134–136, Feb. 2016.
2. **G. Feng**, C. C. Boon, F. Meng, and X. Yi, "A 100-GHz 0.21-K NETD 0.9-mW Charge-Accumulation Super-Regenerative Receiver in 65-nm CMOS," *IEEE Microw. Compon. Lett.*, vol. 26, no. 7, pp. 531–533, Jul. 2016.
3. F. Meng, K. Ma, K. S. Yeo, C. C. Boon, X. Yi, J. Sun, **G. Feng**, and S. Xu, "A Compact 57-67 GHz Bidirectional LNAPA in 65-nm CMOS Technology," *IEEE Microw. Compon. Lett.*, vol. 26, no. 8, pp. 628–630, Aug. 2016.
4. T. N. Huang, C. C. Boon, F. X. Zhu, X. Yi, X. He, **G. Feng**, W. M. Lim, and B. Liu, "A 65 nm CMOS LNA for Bolometer Application," *J. Infrared, Millimeter, Terahertz Waves*, vol. 37, no. 4, pp. 356–372, Apr. 2016.
5. N. Huang, X. Yi, C. C. Boon, X. He, **G. Feng**, W. M. Lim, and X. Zhu, "A CMOS W-Band 4x Quasi-Subharmonic Mixer," *IEEE Microw. Compon. Lett.*, vol. 25, no. 6, pp. 385–387, Jun. 2015.
6. J. Lin, C. C. Boon, X. Yi, and **G. Feng**, "A 50-59 GHz CMOS Injection Locking Power Amplifier," *IEEE Microw. Compon. Lett.*, vol. 25, no. 1, pp. 52–54, Jan. 2015.

7. X. Yi, Z. Liang, **G. Feng**, C. C. Boon, and F. Meng, "A 93.4-to-104.8GHz 57mW Fractional-N Cascaded Sub-sampling PLL with True In-Phase Injection-Coupled QVCO in 65nm CMOS," in *IEEE RF Integr. Circuits Symp*., May 2016, pp. 122-125.
8. X. Yi, K. Yang, Z. Liang, B. Liu, K. Devrishi, C. C. Boon, C. Li, **G. Feng**, D. Regev, S. Shilo, F. Meng, H. Liu, J. Sun, G. Hu, and Y. Miao, "A CMOS Transceiver for IEEE 802.11ax WLAN Applications in 65nm CMOS," in *IEEE RF Integr. Circuits Symp*., May 2016, pp. 67-70.
9. N. Huang, X. Yi, C. C. Boon, J. Sun, and **G. Feng**, "Design of a Fully Integrated CMOS Dual K- and W- band Lumped Wilkinson Power Divider", *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2013, pp. 788-791.

Bibliography

[1] S. Rangan, T. S. Rappaport, and E. Erkip, "Millimeter-wave cellular wireless networks: potentials and challenges," *Proc. IEEE*, vol. 102, no. 3, pp. 366–385, Mar. 2014.

[2] N. Saito, T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, and K. Takinami, "A fully integrated 60-GHz CMOS transceiver chipset based on WiGig/IEEE 802.11ad with built-in self calibration for mobile usage," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3146–3159, Dec. 2013.

[3] L. Yujiri, M. Shoucri, and P. Moffa, "Passive millimeter wave imaging," *IEEE Microw. Mag.*, vol. 4, no. 3, pp. 39–50, 2003.

[4] L. Kong, D. Seo, and E. Alon, "A 50mW-TX 65mW-RX 60GHz 4-element phased-array transceiver with integrated antennas in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 234–235.

[5] E. R. (05)07, "Radio frequency channel arrangements for fixed service systems operating in the bands 71-76 GHz and 81-86 GHz." Oct-2005.

[6] O. Katz, R. Ben-Yishay, R. Carmon, B. Sheinman, F. Szenher, D. Papae, and D. Elad, "High-power high-linearity SiGe based E-band transceiver gchipset for broadband communication," in *IEEE RF Integr. Circuits Symp.*, 2012, pp. 115–118.

[7] V. H. Le, H. T. Duong, A. T. Huynh, C. M. Ta, F. Zhang, R. J. Evans, and E. Skafidas, "A CMOS 77-GHz receiver front-end for automotive radar," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3783–3793, Oct. 2013.

[8] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.

[9] Q. J. Gu, Z. Xu, A. Tang, and M.-C. F. Chang, "A D-band passive imager in 65 nm CMOS," *IEEE Microw. Compon. Lett.*, vol. 22, no. 5, pp. 263–265, May 2012.

[10] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS receiver chipset for millimeter-wave radiometer systems," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 378–391, Feb. 2011.

[11] A. M. Niknejad and H. Hashemi, *mm-Wave silicon technology: 60 GHz and beyond*. Springer Science & Business Media, 2008.

[12] ISSCC, "ISSCC 2015 trends." Presented at ISSCC 2015. [Online]. Available: http://isscc.org/doc/2015/isscc2015_trends.pdf.

[13] A. Hajimiri, "mm-wave silicon ICs: challenges and opportunities," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2007, pp. 741–747.

[14] C. Martin, S. Clark, J. Galliano, and J. Lovberg, "Advances in millimeter-wave imaging technology for enhanced vision systems," in *Proceedings of Digital Avionics Systems Conference*, 2002, vol. 2, pp. 11D4–1.

[15] L. Gilreath, V. Jain, and P. Heydari, "Design and analysis of a W-band SiGe direct-detection-based passive imaging receiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2240–2252, Oct. 2011.

[16] J. J. Lynch, H. P. Moyer, J. H. Schaffner, Y. Royter, M. Sokolich, B. Hughes, Y. J. Yoon, and J. N. Schulman, "Passive millimeter-wave imaging module with preamplified zero-bias detection," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1592–1600, Jul. 2008.

[17] J. W. May and G. M. Rebeiz, "Design and characterization of W -band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1420–1430, May 2010.

[18] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981–1991, Oct. 2010.

[19] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Förster, H. M. Keller, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "A 1 k-pixel video camera for 0.7-1.1 terahertz imaging applications in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, 2012.

[20] H. Sherry, J. Grzyb, Y. Zhao, R. Al Hadi, A. Cathelin, A. Kaiser, and U. Pfeiffer, "A 1kpixel CMOS camera chip for 25fps real-time terahertz imaging applications," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 252–254.

[21] A. Tang and M.-C. F. Chang, "Inter-modulated regenerative CMOS receivers operating at 349 and 495 GHz for THz imaging applications," *IEEE Trans. THz Sci. Technol.*, vol. 3, no. 2, pp. 134–140, Mar. 2013.

[22] A. Tang and M.-C. F. Chang, "183GHz 13.5mW/pixel CMOS regenerative receiver for mm-wave imaging applications," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 296–298.

[23] J. Randa, J. Lahtinen, A. Camps, A. Gasiewski, M. Hallikainen, D. M. Le Vine, M. Martin-Neira, J. Piepmeier, P. W. Rosenkranz, C. S. Ruf, and others, *Recommended terminology for microwave radiometry*. US Department of Commerce, National Institute of Standards and Technology, 2008.

[24] G. Liu and H. Schumacher, "Broadband millimeter-wave LNAs (47–77 GHz and 70–140 GHz) using a T-type matching topology," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2022–2029, Sep. 2013.

[25] Y.-H. Yu, Y.-S. Yang, and Y.-J. Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 502–509, Mar. 2010.

[26] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[27] H. G. Han, D. H. Jung, and T. W. Kim, "A 2.88 mW +9.06 dBm IIP3 common-gate LNA with dual cross-coupled capacitive feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 1019–1025, Mar. 2015.

[28] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[29] A. C. Ulusoy, P. Song, W. T. Khan, M. Kaynak, B. Tillack, J. Papapolymerou, and J. D. Cressler, "A SiGe D-band low-noise amplifier

utilizing gain-boosting technique," *IEEE Microw. Compon. Lett.*, vol. 25, no. 1, pp. 61–63, Jan. 2015.

[30] Y.-A. Li, M.-H. Hung, S.-J. Huang, and J. Lee, "A fully integrated 77GHz FMCW radar system in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 216–217.

[31] W. Ciccognani, E. Limiti, P. E. Longhi, and M. Renvoise, "MMIC LNAs for radioastronomy applications using advanced industrial 70 nm metamorphic technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2008–2015, Oct. 2010.

[32] G. Moschetti, A. Leuther, H. Massler, B. Aja, M. Rosch, M. Schlechtweg, O. Ambacher, V. Kangas, and M. Genevieve-Perichaud, "A 183 GHz metamorphic HEMT low-noise amplifier with 3.5 dB noise figure," *IEEE Microw. Compon. Lett.*, vol. 25, no. 9, pp. 618–620, 2015.

[33] G. Nikandish and A. Medi, "Transformer-feedback interstage bandwidth enhancement for MMIC multistage amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 441–448, Feb. 2015.

[34] P. Smith, M. Ashman, D. Xu, X. Yang, C. Creamer, P. Chao, K. Chu, K. Duh, C.-K. Koh, and J. Schellenberg, "A 50nm MHEMT millimeter-wave MMIC LNA with wideband noise and gain performance," in *IEEE MTT-S Int. Dig*, 2014, pp. 1–4.

[35] A. Tang, Q. J. Gu, and M.-C. F. Chang, "CMOS receivers for active and passive mm-wave imaging," *IEEE Commun. Mag.*, vol. 49, no. 10, pp. 190–198, Oct. 2011.

[36] J.-C. Chien and L.-H. Lu, "40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2715–2725, Dec. 2007.

[37] J.-C. Kao, P. Chen, P.-C. Huang, and H. Wang, "A novel distributed amplifier with high gain, low noise, and high output power in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1533–1542, Apr. 2013.

[38] A. Jahanian and P. Heydari, "A CMOS distributed amplifier with distributed active input balun using GBW and linearity enhancing

techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1331–1341, May 2012.

[39] T.-Y. Huang, Y.-H. Lin, J.-H. Cheng, J.-C. Kao, T.-W. Huang, and H. Wang, "A high-gain low-noise distributed amplifier with low DC power in 0.18-μm CMOS for vital sign detection radar," in *IEEE MTT-S Int. Dig*, 2015, pp. 1–3.

[40] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.

[41] B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170-200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 692–701, Mar. 2012.

[42] M. Khanpour, K. W. Tang, P. Garcia, and S. P. Voinigescu, "A wideband W-band receiver front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717–1730, Aug. 2008.

[43] R. Sananes and E. Socher, "52-75 GHz wideband low-noise amplifier in 90 nm CMOS technology," *Electron. Lett.*, vol. 48, no. 2, pp. 71–72, Jan. 2012.

[44] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1910–1922, Jun. 2015.

[45] A. Y.-K. Chen, Y. Baeyens, Y.-K. Chen, and J. Lin, "A low-power linear SiGe BiCMOS low-noise amplifier for millimeter-wave active imaging," *IEEE Microw. Compon. Lett.*, vol. 20, no. 2, pp. 103–105, Feb. 2010.

[46] D.-R. Lu, Y.-C. Hsu, J.-C. Kao, J.-J. Kuo, D.-C. Niu, and K.-Y. Lin, "A 75.5-to-120.5-GHz high-gain CMOS low-noise amplifier," in *IEEE MTT-S Int. Dig*, 2012, pp. 1–3.

[47] D. Sandstrom, M. Varonen, M. Karkkainen, and K. Halonen, "W-band CMOS amplifiers achieving +10dBm saturated output power and 7.5dB NF," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 486–487,487a.

[48] D. J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *IEEE RF Integr. Circuits Symp.*, 2004, pp. 97–100.

[49] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[50] M. Sato, T. Takahashi, and T. Hirose, "68-110-GHz-band low-noise amplifier using current reuse topology," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 7, pp. 1910–1916, Jul. 2010.

[51] Y.-K. Hsieh, J.-L. Kuo, H. Wang, and L.-H. Lu, "A 60 GHz broadband low-noise amplifier with variable-gain control in 65 nm CMOS," *IEEE Microw. Compon. Lett.*, vol. 21, no. 11, pp. 610–612, Nov. 2011.

[52] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18µm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.

[53] H. F. Leung and H. C. Luong, "A 1.2-6.6GHz LNA using transformer feedback for wideband input matching and noise cancellation in 0.13µm CMOS," in *IEEE RF Integr. Circuits Symp.*, 2012, pp. 17–20.

[54] P. R. Gray, *Analysis and design of analog integrated circuits.*, 5th ed. New York: John Wiley & Sons, Inc., 2009, pp. 518–533.

[55] S. Voinigescu, *High-frequency integrated circuits*. Cambridge, New York: Cambridge U P, 2013, pp. 374–551.

[56] B. G. Ulrich Pfeiffer Janusz Grzyb Duixian Liu, *Advanced millimeter-wave technologies:antennas, packaging and circuits*. John Wiley & Sons Ltd., 2009.

[57] F. Sizov and A. Rogalski, "THz detectors," *Progress in quantum electronics*, vol. 34, no. 5, pp. 278–347, Sep. 2010.

[58] C. A. Martin, C. E. GarcÃ a GonzÃ ¡lez, V. G. Kolinko, and J. A. Lovberg, *Rapid passive MMW security screening portal*, vol. 6948. 2008, p. 69480J–69480J–9.

[59] Z. Chen, C.-C. Wang, H.-C. Yao, and P. Heydari, "A BiCMOS W-Band 2x2 focal-plane array with on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2355–2371, 2012.

[60] Q. J. Gu, K. Yang, Y. Xue, Z. Xu, A. Tang, C.-C. Nien, T. Wu, J.-H. Tarng, and M.-C. F. Chang, "A CMOS integrated W-band passive imager," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 11, pp. 736–740, 2012.

[61] R. H. Dicke, "The measurement of thermal radiation at microwave frequencies," *Review of Scientific Instruments*, vol. 17, no. 7, pp. 268–275, Jul. 1946.

[62] Q. J. Gu, Z. Xu, H.-Y. Jian, A. Tang, M.-C. F. Chang, C.-Y. Huang, and C.-C. Nien, "100 GHZ integrated CMOS passive imager with >100 MV/W responsivity, 23fW/Hz$^{0.5}$ NEP," *Electron. Lett.*, vol. 47, no. 9, pp. 544–545, Apr. 2011.

[63] F. Meng, K. Ma, and K. S. Yeo, "A 130-to-180GHz 0.0035mm^2 SPDT switch with 3.3dB loss and 23.7dB isolation in 65nm bulk CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

[64] F. Meng, K. Ma, K. S. Yeo, C. C. Boon, W. M. Lim, and S. Xu, "A 220-285 GHz SPDT switch in 65-nm CMOS using switchable resonator concept," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 4, pp. 649–651, Jul. 2015.

[65] L. Mereni, D. Pepe, and D. Zito, "Analyses and design of 95-GHz SoC CMOS radiometers for passive body imaging," *Proc. Analog Integr. Circuits Signal Processing—Special Issue (ICECS'12)*, vol. 77, no. 3, pp. 373–383, 2013.

[66] D. Pepe and D. Zito, "32 dB gain 28 nm bulk CMOS W-band LNA," *IEEE Microw. Compon. Lett.*, vol. 25, no. 1, pp. 55–57, 2015.

[67] E. H. Armstrong, "Some recent developments of regenerative circuits," *Proc. of the Institute of Radio Engineers*, vol. 10, no. 4, pp. 244–260, Aug. 1922.

[68] E. H. Armstrong, *Wireless receiving system.* US Patent 1,113,149, 1914.

[69] *The legacies of Edwin Howard Armstrong: the regenerative circuit, the superheterodyne circuit, the superregenerative circuit, frequency modulation*. Radio Club of America, 1991.

[70] F. X. Moncunill-Geniz, P. Pala-Schonwalder, and O. Mas-Casals, "A generic approach to the theory of superregenerative reception," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 1, pp. 54–70, Jan. 2005.

[71] B. Otis, Y. H. Chee, and J. Rabaey, "A 400μW-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 396–606 Vol. 1.

[72] J. R. Whitehead, *Super-regenerative receivers*. University Press, 1950.

[73] M. Vidojkovic, X. Huang, P. Harpe, S. Rampu, C. Zhou, L. Huang, K. Imamura, B. Busze, F. Bouwens, M. Konijnenburg, J. Santana, A. Breeschoten, J. Huisken, G. Dolmans, and H. de Groot, "A 2.4GHz ULP OOK single-chip transceiver for healthcare applications," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 458–460.

[74] P. Pala-Schonwalder, J. Bonet-Dalmau, F. Xavier Moncunill-Geniz, F. del Aguila-Lopez, and R. Giralt-Mas, "A superregenerative QPSK receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 258–265, Jan. 2014.

[75] P. Pala-Schonwalder, F. X. Moncunill-Geniz, J. Bonet-Dalmau, F. del Aguila-Lopez, and R. Giralt-Mas, "A BPSK superregenerative receiver. Preliminary results," in *IEEE International Symposium on Circuits and Systems*, 2009, pp. 1537–1540.

[76] M. Pelissier, D. Morche, and P. Vincent, "Super-regenerative architecture for UWB pulse detection: from theory to RF front-end design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 7, pp. 1500–1512, Jul. 2009.

[77] A. Tang, Q. Gu, Z. Xu, G. Virbila, and M.-C. F. Chang, "A max 349 GHz 18.2mW/pixel CMOS inter-modulated regenerative receiver for tri-color mm-wave imaging," in *IEEE MTT-S Int. Dig.*, 2012, pp. 1–3.

[78] J. L. Bohorquez, A. P. Chandrakasan, and J. L. Dawson, "Frequency-domain analysis of super-regenerative amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 2882–2894, Dec. 2009.

[79] J. Bonet-Dalmau, F. X. Moncunill-Geniz, P. Pala-Schonwalder, F. del Aguila-Lopez, and R. Giralt-Mas, "Frequency domain analysis of superregenerative receivers in the linear and the logarithmic modes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 1074–1084, May 2012.