A Cantilever-based Non-volatile Memory Utilizing Vibrational Reset for High Temperature Operation

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***Abstract*—This paper proposes a cantilever-based memory structure for storing binary data at extreme operating temperature (up to 300 °C) in rugged electronics. The memory bit (0/1) is formed by opening/closing of an electrostatic switch. Permanent retention is obtained by adhesive force between two smooth surfaces in contact, eliminating leakage observed in all types of storage-layer-based NVMs. The *Reset* utilizes a train of short pulses to break the adhesion between the electrodes. This allows the Nano-electromechanical switch (NEMS) memory to be implemented using a simple bi-layer design and easily integrated with CMOS platforms. We propose an array structure where each memory cell consists of a NEMS memory device and one NMOS transistor for full random-access operation.**

Keywords—NEMS, NVM, cantilever-based, vibrational reset.

I. INTRODUCTION

Over the last few decades, power, performance, and capacity of embedded memories have constantly benefited from the scaling of CMOS technology. However, lower threshold voltage and smaller device channel length in scaled CMOS devices have led to an exponential increment in the leakage current (I_{off}) [1]. As a result, designing mainstream memories such as SRAM, DRAM or Flash in nano-scale technology is facing critical issues such as tight requirements on leakage and degraded immunity to process variations.

Recent publications have reported several emerging technologies for achieving zero standby leakage in memory design. These include resistive RAM (R-RAM) [2], magnetic RAM (M-RAM) [3], phase-change RAM (PC-RAM) [4], conductive-bridge RAM (CB-RAM) [5], and ferroelectric-RAM (Fe-RAM) [6]. In these devices, different physical mechanisms (FLASH: floating gate, M-RAM: free magnetic layer, and Fe-RAM: ferroelectric polarization) are exploited to store data without power supply. However, they also fail to offer a good data retention at extreme temperature such as 200 °C and above like mainstream technologies [7].

NEMS-based memory devices utilize electrostatic force to perform set/reset operation and adhesion force between two smooth metal surfaces to retain data. It has been shown that metal-metal adhesion improves at higher temperature [8]. This is because metal soften as temperature increases. As a result, NEMS-based memory devices can potentially offer seamless operation over a wide temperature range for industrial or defense electronic applications.

This work reports a NEMS NVM device that can retain data even at 300 °C. It can be integrated with a MOSFET transistor to form a complete memory bit cell for fully random-access operation. The rest of the paper is organized as followed: Section II discusses the operating principles of the NEMS device. Section III presents our measurement results. In Section IV, we propose a new bit cell for memory array implementation. The new NEMS device is modeled using Verilog-A, and combined with other CMOS devices to illustrate our proposed NEMS-CMOS integration. Full array simulation was performed using Cadence tools and 0.18 um CMOS technology. Section V concludes the paper.

II. CANTILEVER-BASED NEMS NVM CELL WITH VIBRATIONAL RESET PROCEDURE

A. Device Structure and Operating Principles

The proposed NEMS-based NVM structure is a three-terminal device that can be fabricated on top of silicon substrate as shown in Fig. 1. The three terminals are named *Contact*, *Actuator* and *Cantilever*, respectively. A potential difference between *Cantilever* and *Actuator* forms electrostatic force, which actuates the *Cantilever* terminal to obtain two distinctive states (i.e. data zero and one). For the sake of clarity, data one is represented by the case where the *Cantilever* head is attached to *Contact*. Similarly, data zero is represented by the case where *Cantilever* is detached from *Contact*. The act of memory switching from zero to one is called *"Set"* and that from one to zero is called *"Reset"*. Both *Set* and *Reset* operations are performed by controlling *Cantilever* and *Actuator* properly. This simplifies the NEMS device structure, allowing better scalability and fabrication cost effectiveness.

In the *Set* operation, a large swing pulse (V_{SET}) is applied to *Actuator* while *Cantilever* is kept at ground. This induces an attractive electrostatic force between *Actuator* and *Cantilever*, which is proportional to the voltage difference across the overlapped surfaces. The attractive electrostatic force pulls down the *Cantilever* beam. If the electrostatic force is strong enough, the head of the beam will touch the *Contact* surface. The required voltage to create such force is defined as the pull-in voltage (V_{pin}). In conventional cantilever switches, the beam

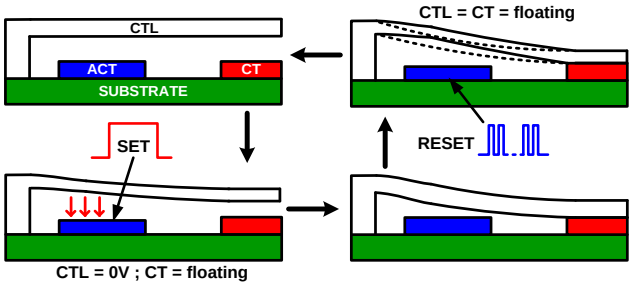

Figure 1. Operation of the proposed 3-terminal cantilever-based NEMS NVM device with vibrational reset procedure.

will return to its original position due to the spring-like elastic restoring force (F_r) when the voltage on *Actuator* is removed. However, if the two surfaces are close enough (i.e. ~ 5 nm or less), the Van der Waals adhesion force (F_{ad}) will come into effect [7]. Magnitude of F_r and F_{ad} are calculated as [7, 9]:

$$F_r = \frac{EWt^3 g}{4L^3} \quad (1) \qquad F_{ad} = \frac{A_{metal}}{12\pi D_{rms}^2} \quad (2)$$

where *E*, *W*, *t* and *L* are the Young's modulus, width, thickness and length of the cantilever, respectively and *g* is the original gap between the *Cantilever* and the *Contact* surface (Fig. 1). A_{metal} is the Hamaker constant of the metal and D_{rms} is the roughness of the surface. The adhesion force (F_{ad}) can be larger than the restoring force (F_r) by carefully engineering the smoothness and the size of the *Contact* and *Cantilever* surfaces. This makes the beam remain at the *close* position (i.e. data one) permanently, which is used as memory operation.

In the *Reset* operation, the *Cantilever* beam must be detached from the *Contact* terminal to go back to the *open* position (i.e. data zero). In the conventional structures, a forth terminal is required on top of the cantilever to pull up the *Cantilever* beam since the electrostatic force between two differential plates is always attractive. This complicates the fabrication process, affects scalability, and raises costs significantly. To address the above issues, we propose a vibrational reset scheme using *Actuator* for resetting the memory data. This is done by applying a train of short pulses to *Actuator*. Each time a short pulse is sent to the *Actuator*, it pulls down the *Cantilever* beam. Since the beam is already in contact with the *Contact* pad, the middle part of the beam will bend down. Furthermore, the magnitude and duration of each pulse are much smaller than that of the *Set* pulse. As a result, the beam vibrates. If the frequency of the pulses is close to the resonant frequency of the beam, the amplitude of the vibration will grow gradually until it is strong enough to break the adhesion force between *Contact* and *Cantilever*. Finally, the beam will move back to its open position.

B. Proposed NEMS Memory Device Fabrication

The whole fabrication process only requires five lithographic steps under moderate process temperature to preserve any underlying CMOS stacks. In addition, three materials are used for the integration of the memory: metal, insulator and a sacrificial material. Molybdenum metal is used to provide ideal contact properties: hardness, low wear-out over cycles, no native oxidation, and excellent thermal stability [10]. The device was fabricated on 8 inch silicon wafers. LPCVD silicon nitride and ALD aluminum oxide (Al_2O_3) was deposited for electrical isolation from substrate. The metallic contact and actuation electrodes were created by depositing and patterning PVD molybdenum (Mo) layer of 200 nm. The actuation electrode was sealed by a Al_2O_3 layer and it serves to anchor fixed electrodes on the substrate. Silicon dioxide with the thickness of 500 nm was used as a sacrificial layer. The *Cantilever*'s anchor and contact dimples were pre-patterned in sacrificial layer before depositing and patterning 300 nm PVD Mo to create the *Cantilever* beam.

An SEM image of one of the fabricated devices is shown in Fig. 2. The head of the *Cantilever* beam has an array of 15 dimples. Each dimple has the dimension of 500 nm × 500 nm. The number of dimples is of crucial as it decides the adhesion force between *Cantilever* and *Contact*. Too many dimples create a large adhesion force, leading to a higher reset voltage or a reset failure. On the other hand, too few dimples will fail

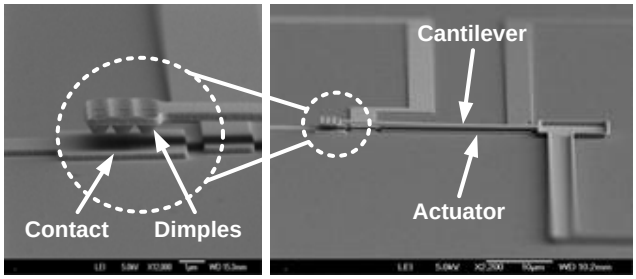

Figure 2. (Right) SEM image of a single electrostatic non-volatile memory. (Left) Magnified zoom-in of the head portion of the beam.

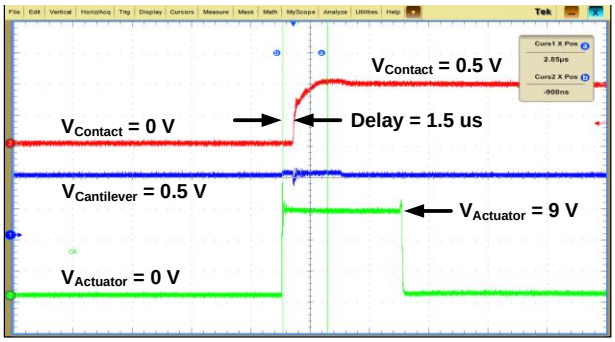

Figure 3. Measured waveforms of the proposed NEMS device in a *Set* operation at room temperature with 1.5 µs delay.

to hold the beam at the close state and thus the device behaves like a switch, not a memory element.

III. Proposed NEMS Device Measurement

A. Set Operation

The Set operation is executed by applying a potential difference between *Actuator* and *Cantilever* while *Contact* is left floating. Fig. 3 shows the measured waveforms in a *Set* operation where an actuation pulse is applied to *Actuator*. The *Set* delay is defined by the time from the rising edge of the pulse to the rising edge of *Contact*. In this measurement, *Cantilever* is biased at 0.5 V to easily observe the voltage change at *Contact*. In actual operation, *Cantilever* can be grounded. As Fig. 3 shows, the *Contact* node starts to follow the *Cantilever* voltage after a short delay (~1.5 µs).

The minimum required pull-in voltage (P_{in}) of different devices ranges from 4 V to 6 V. Larger devices have higher minimum pull-in voltages. In this prototyping, the implemented devices are relatively large (~15 µm). The device dimension can be significantly scaled if contemporary NEMS technology is employed. This indicates that the proposed NEMS memory device has the potential to operate at the supply voltage of CMOS integrated circuits. Fig. 4 illustrates how the *Set* delay improves when we increase the pull-in voltage. As expected, higher pull-in voltages lead to smaller delays in all the *Cantilever* lengths.

We also attempted to examine the impact of the *Cantilever* biasing voltage on the *Set* delay (Fig. 5). As the *Cantilever* voltage is lowered to a negative level, the *Cantilever-Actuator* potential difference increases and thus the *Set* delay decrements. Another factor contributing to the *Set* delay improvement is the electrostatic force between the head of *Cantilever* and the *Contact* plate. However, this causes huge DC current between *Cantilever* and *Contact* when they are in contact. Therefore, *Contact* is left floating during the *Set* operation.

Impact of operating temperature on the NEMS device is shown in Fig. 6. It can be seen that at higher temperature, the

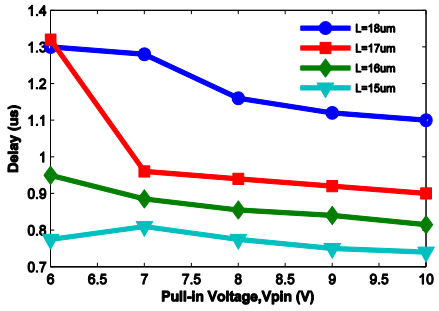

Figure 4. Measured *Set* delay versus pull-in voltage using different cantilever length. Delay reduces with smaller device size.

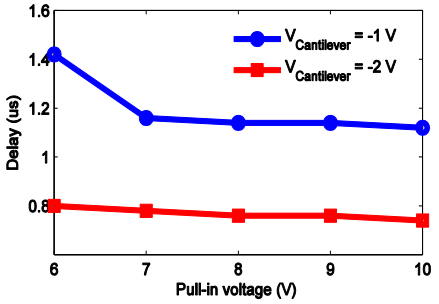

Figure 5. Measured *Set* delay versus pull-in voltage.

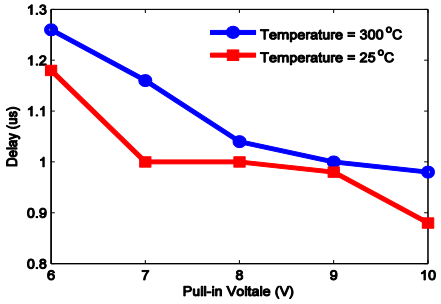

Figure 6. Measured *Set* delay versus pull-in voltage at different operating temperature. Delay increases with temperature but insignificantly.

delay is longer. However, the additional delay is insignificant and proves that the NEM device still functions at 300 °C.

B. *Reset Operation*

For *Reset* operation, various pulse frequencies and voltage levels are tested to find the most effective signal. Measurement showed that the most suitable *Reset* is 4 V peak-to-peak at 1 MHz for all device lengths. To find the required number of pulses for resetting, the following procedures are used: (1) Conduct a *Set* operation, (2) apply a train of pulses with the period of 1 µs to *Contact*, (3) measure *Cantilever-Contact* impedance for checking detac0hment, and (4) repeat (2) and (3) with a larger number of pulses until *Cantilever* is detached. Fig. 7 illustrates the measured *Reset* operation.

To confirm the deactivation of the *Cantilever*, current through the *Contact-Cantilever* ($I_{C\text{-}C}$) path is monitored. Originally, the *NEM* memory device is in the *Set* state. Thus $I_{C\text{-}C}$ of 2 nA is observed. $I_{C\text{-}C}$ was controlled by the measurement set-up to avoid excessive current through the dimples. After applying the reset pulses for 10 µs, $I_{C\text{-}C}$ drops to 10 pA, confirming that *Cantilever* has been detached from *Contact*. The leakage of 10 pA is due to the test equipment.

IV. Array Implementation using 1T-1NEMS Bit Cell

A. *Proposed 1T-1NEMS Bit Cell and Array Structure*

The proposed NVM device is combined with an NMOS transistor to form a complete bit-cell. The new bit-cell can be

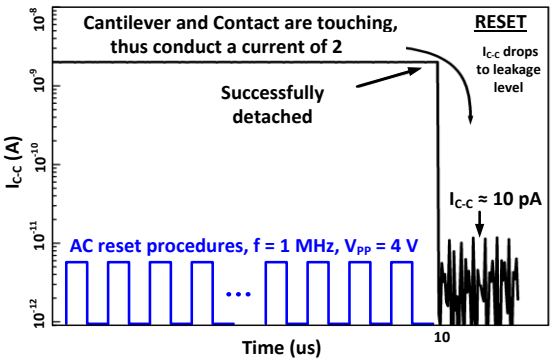

Figure 7. Measured $I_{C\text{-}C}$ in a *Reset* operation. The NEMS cell is successfully detached after 10 pulses, 1 µs each.

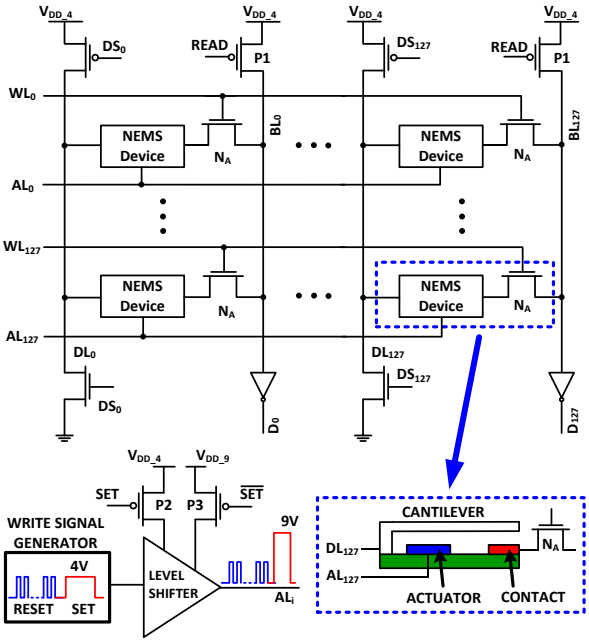

Figure 8. Proposed architecture of the 1T-1NEMS NVM array.

integrated using standard CMOS technology to realize a random-access memory. Fig. 8 illustrates a 128×128 memory array using 0.18 µm CMOS technology and the Verilog-A model of the NEMS device. The whole array is powered by 4 V and 9 V supplies (V_{DD_4} and V_{DD_9}). These values are decided by the required voltage for the *Set* and *Reset* operations. Each column shares one bitline (BL) and one data-line (DL) running vertically. Each row has one word-line (WL) and one actuation-line (AL). The access transistor (N_A) bridges the *Contact* terminal of the NEMS device and BL. WLs are connected to the gates of N_A while ALs are connected to the *Actuator* nodes of NEMS devices in each row. As expected, the power supply for the array can be completely turned off and the stored data are still retained in the proposed NEMS devices thanks to the non-volatile property. When the memory enters the active mode, all BLs are pre-charged to V_{DD_4} while all WLs, DLs and ALs are pre-discharged to ground. The detailed read and write cycles of the array are described in the following section.

B. *Read Operation*

Fig. 9 illustrates simulated read operation of the proposed design. When a read cycle starts (RE = 1), a particular row is chosen by an address decoder and a corresponding WL is enabled, turning on the access transistors (N_A). At the same

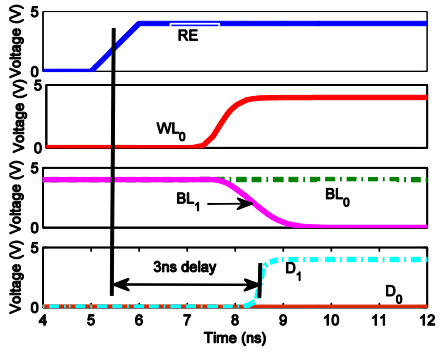

Figure 9. Simulation waveforms of our proposed array during a read cycle.

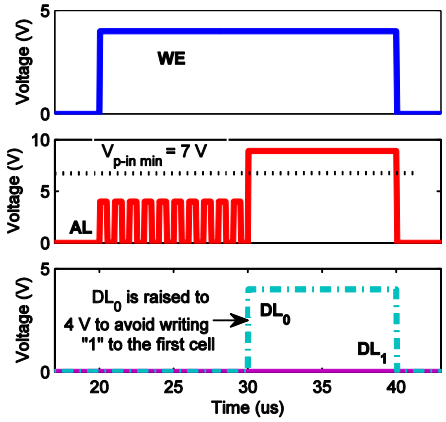

Figure 10. Simulation waveforms of our proposed array during a write cycle.

time, READ is triggered high to turn off the PMOS transistors (P1), leaving the BLs floating. If the accessed cell is storing data one (*i.e. Contact* touches *Cantilever*), a direct path is formed between BL and DL. Because DLs are clamped at ground by N1, BLs for data zero will be discharged to a lower level. If the cell stores data zero, the NEMS device behaves like an open switch and thus the BL stays at V_{DD_4}. The stored data is generated by sensing the BL level. The simulated delay is 3 ns, which is primarily determined by the contact resistance between.

C. Write Operation

Write operation consists of two consecutive operations, *Reset* and selective *Set*. In the *Set* phase, all cells in the selected row are *Reset* by a train of pulses as shown in Fig. 10. This is followed by a *Set* operation to the selected cells. For example, if we want to write "01011...1" to a row. First, a train of 10 pulses with the peak-to-peak value of 4 V is sent to the AL of the selected row (AL_i) for reset ting. All the NEMS devices in the selected row are reset to data zero. Next, we need to write data '1' in all except the first and the third cells. After *Reset*, pull-in voltage is sent to AL_i. To avoid writing data '1' into the first and the third cells, DL_0 and DL_2 are raised to V_{DD_4}., which reduces the voltage difference between *Cantilever* and *Actuator* smaller than the pull-in voltage. Consequently, after a selective set-after-reset operation, write data is found at the selected row. In Fig. 10, DL_1 is kept at ground level while DL_0 is raised to V_{DD_4} so that the *Reset* data remains. Note that the DL_0 level can be higher than 4V as far as the voltage difference between *Cantilever* and *Contact* is kept smaller than the pull-in voltage.

Write delay is the sum of *Set* and *Reset* delays. As presented in section III, *Set* delay is about 1.5 µs while the *Reset* delay is about 10 µs. Thus, a total delay of only 11.5 µs is required, which is much shorter than NAND Flash (~200 µs) and comparable to that of NOR Flash (~10 µs). Note that faster write speed can be achieved with device scaling.

The *Actuator* electrode utilizes two signal levels, 4 V and 9 V, through the AL lines. Therefore, the AL lines must be driven by a level shifter that can switch between 9 V and 4 V (Fig. 8, bottom). During *Set*, P2 is off and P3 is on to raise the supply level to 9 V.

The *Reset* pulses can be applied to the horizontal or vertical lines. However, applying them to the vertical lines leads to a huge power consumption since each cell requires one separate pulse signal. In the proposed array architecture, *Actuators* are connected horizontally and thus only one AL is activated during write operation. As a result, it significantly reduces the *Reset* energy consumption.

V. Conclusion

A 3-terminal cantilever-based NEMS device is proposed as a NVM structure with fast read/write and good data retention at extremely high temperature (up to 300 °C). The proposed vibrational reset operation significantly simplify the device structure complexity and hence fabrication cost. A selective set-after-reset scheme is introduced for energy efficient write operation in the proposed array architecture. When integrated with CMOS technology, our 1T-1NEMS bit cell features random-access with 3 ns read delay and 11.5 µs write delay. This write delay can be improved with more aggressive device scaling. The experimental results validate that the proposed NEMS NVM is a promising candidate for various systems requiring very high operating temperature.

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