A Rectifier-less AC-DC Interface Circuit for Ambient Energy Harvesting from Low-Voltage Piezoelectric Transducer Array

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***Abstract*—This paper presents a rectifier-less AC-DC energy harvesting circuit capable of harvesting energy from multiple low-voltage Piezoelectric Transducers (PETs). Synchronous electric charge extraction (SECE) technique, with bi-directional switches is adopted to achieve rectifier-less AC/DC direct conversion. The inductor is engaged only during the voltage peak of the PET output for a short period of time and therefore, a single inductor can be shared by multiple transducers. A split-capacitor charging topology is employed to harvest both positive and negative half-cycle energies, without the use of an input rectifier. In addition, a self-startup function is incorporated to kick-start the system from low input voltages. A prototype has been implemented with off-the-shelf components. Energy harvesting from three PET energy sources with different resonance frequencies is demonstrated. A peak overall power conversion efficiency of 79% is achieved with a system self-startup voltage of 650 mV.**

***Index Terms*— AC–DC power conversion, energy harvesting, piezoelectric transducers, synchronous electric charge extraction.**

I. Introduction

THE Internet of Things (IoT) has triggered massivity in sensor usage such as for the environment, structural health and human health monitoring systems. There is significant challenge to power these wireless sensors with a traditional battery, as the limited energy storage can be a bottleneck for long term operation of the sensors [1]. With the fast-increasing number of sensors deployed, it is extremely time-consuming or even impractical to access individual sensor for battery replacement.

Energy harvesting from ambient environment is a promising solution to the issues described above. Light, heat and motion are the three most commonly available ambient energy sources [2]. Among different ambient energy harvesting methods, vibration energy harvesting with Piezoelectric Transducer (PET) has attracted enormous research interests because of its compatibility with both macroscale and microscale fabrication processes and its relatively high energy density [3-6].

Numerous Piezoelectric Energy Harvesting (PEH) interface circuits have been reported in the literature. The simplest one is a Diode Bridge Rectifier (DBR). However, DBR circuits have low conversion efficiencies due to the V_{th} drop across the diode. Variations of the DBR circuit such as Negative Voltage Converter (NVC) and active diodes [7] have been reported. Various linear techniques based on impedance matching have been reported [8-10]. The interface circuit's input impedance is transformed to match the internal impedance of PET for maximum power transfer. Recently, the non-linear interface circuits that utilize the intrinsic capacitive source impedance to maximize the energy transfer have attracted significant attention. Though non-linear techniques such as series-SSHI and parallel-SSHI flip the PET voltage and harvest power closer to the theoretical maximum, the harvested power has a strong dependence on the voltage across the energy storage and an impedance matching circuit is required to achieve high efficiency [11]. On the other hand, Synchronous Electric Charge Extraction (SECE) technique is effective in providing immunity to the PET source from output voltage variations [12]. SECE achieves this immunity by decoupling the load from the PET source using an inductor as the intermediate energy storage bank. The SECE technique is capable of harvesting energy from random vibrations without employing an MPPT circuit.

Device miniaturization is a key driver towards smaller form-factor PET, which usually have lower output voltage and power. Multilayer Piezoelectric Transducers (MPET) are employed which consists of multiple stacked PETs to enhance the output power [14], [15]. MPETs are made up of multiple thin film PETs stacked on top of each other. Reducing the thickness by a factor of n causes the capacitance of the PET to increase by a factor of n^2 [27]. With such a high intrinsic capacitance [16], MPETs often have lower voltage levels compared to their single-layer counterparts. In all the above cases, the PET output voltage is in the range of a few hundred millivolts to a few volts. Under low input voltage scenarios, rectifier in the interface circuit has a detrimental effect on the energy efficiency, and has been the motivation for works carried out in [17–19]. While [18] and [19] used enhanced versions of input rectifiers, [17] implemented a rectifier-free design. However, the need for an external negative voltage supply and manual tuning in [17] limits its practical use.

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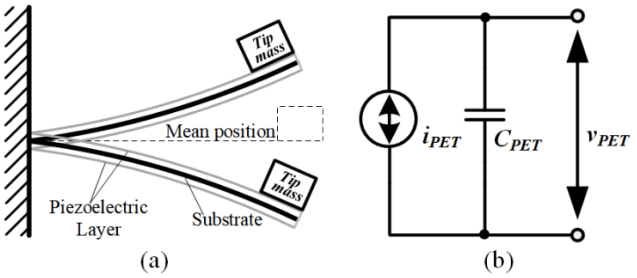

Fig. 1. (a) Structure of a piezoelectric bimorph cantilever beam with an attached tip mass. (b) Simplified, uncoupled, equivalent circuit model of a piezoelectric transducer.

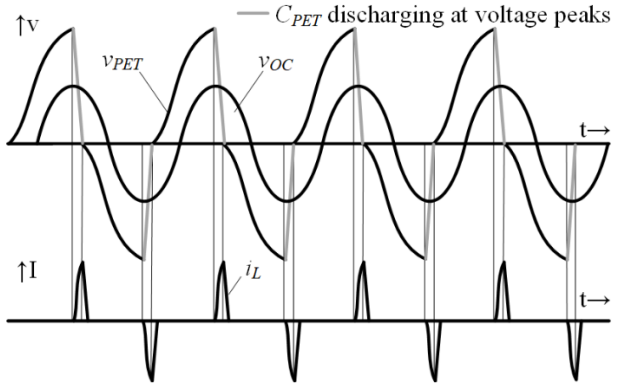

Fig. 2. Voltage and current waveforms during SECE operation. v_{OC} is the open circuit voltage across the PET, v_{PET} is the voltage across the PET when it is connected to the SECE circuit. i_L is the current flowing through the inductor.

Rectifier-free topologies which use intrinsic inductance of Electromagnetic Generators (EMG) have been successfully employed in the past [24], [28] to extract energy from voltages less than 1 V. High-frequency rectifier-free topologies [30] with Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) were used with EMGs to reduce switching losses and solution size. Though the solution could be extended to PETs delivering small output voltages with an additional inductor, the efficiency in the microwatt power range was lower compared to milliwatts range, mostly because of the use of high-frequency switching.

Another limiting factor is that the PET output power can decrease drastically as the ambient vibration frequency shifts away from the PET resonant frequency [20]. Wideband PETs include multiple structures with different resonance frequencies into a single system that have been proposed by [21]. In [22], a DBR circuit was used for each PET in the group and the outputs were tied together, causing the individual PETs to contribute to the load current at their non-optimal power points. To solve this problem, [23] employed the SECE technique for individual harvester in an inductor-sharing configuration, with a Micro-Controller Unit (MCU) providing the control signals needed. However, the peak power conversion efficiency is achieved at high input voltages and is not suitable for low voltage PET applications.

In this paper, the SECE architecture is adopted to harvest ambient vibrational energy from a PET array in the absence of a rectifier. One of the major focus of this work has been on the system integration of ultra-low-power sub-circuits which could harvest power in the microwatt range, with very little impact on the system's power efficiency. The circuit uses a shared inductor scheme to reduce the overall system size. The control circuit is capable of generating timing signals for any PET-inductor combination, doing away with manual tuning [17] or reprogramming [23]. The system standby current is about 550 nA/PET at 2.7 V input. To the best of the authors' knowledge, this is one of the lowest reported power for discrete SECE circuits.

This paper is organized as follows. System architecture is presented in Section II. The circuit implementation is discussed in detail in Section III. Section IV reports the measurement results and Section V concludes the paper.

II. Multi-PET Rectifier-Less SECE Topology

A. Introduction to the SECE technique

A PET with a weak electromechanical coupling in cantilever configuration (see Fig. 1(a)) can be approximated as a simplified, uncoupled circuit model consisting of a sinusoidal current source in parallel with a capacitor C_{PET} (see Fig. 1(b)). The sinusoidal current source is represented as

$$i_{PET} = I_{PET}\,\mathrm{Sin}\left(\omega_{VIB} t\right) \tag{1}$$

where I_{PET} is the peak amplitude of the current and ω_{VIB} is the angular frequency of mechanical vibration. The voltage across the capacitor, v_{PET} has a peak amplitude of V_{PET} and lags i_{PET} by a phase of $\pi/2$. The SECE technique extracts the charge in C_{PET} at each voltage peak of v_{PET}. Charge extraction causes the v_{PET} voltage to fall to zero and the inductor current to rise to a peak value as shown in Fig. 2. Energizing and de-energizing of the inductor occurs during both positive and negative half-cycles of the v_{PET} waveform. Except during the charge extraction phase, the PET is left in its open circuit condition. A switch connects the PET to the inductor for a brief duration of t_{SECE} given by (2)

$$t_{SECE} = \frac{\pi}{2}\left(\sqrt{LC_{PET}}\right) \tag{2}$$

where L is the value of the inductor. t_{SECE} is usually small compared to the time period of the mechanical vibration, T_{VIB} and the discharge can be considered quasi-instantaneous in a practical scenario.

B. Overview of the System Architecture

To overcome the frequency dependence associated with the conventional PEH system and to design a system suitable for low input voltages, the proposed architecture can work simultaneously with multiple low-voltage PETs tuned to different resonant frequencies, without using an input rectifier. Owing to the short duration of t_{SECE} when compared to T_{VIB}, it is possible that multiple PETs can share a single inductor. This is different from the conventional switching converters where the inductor is continuously engaged. The multi-PET rectifier-less system implemented in this work is based on a split-capacitor topology originally used for electromagnetic generators [24]. However, different from the previous work, which was based on a conventional boost converter topology, the system here uses the SECE technique.

The block diagram of the proposed system is shown in Fig. 3. It has a Bi-directional Switching Converter (BSC), Dual Level Shifter (DLS), Peak Detector (PKD), Zero Crossing Detector (ZCD), Digital Logic Controller (DLC), Start-up block and an Under Voltage Lock Out (UVLO) block. The BSC block

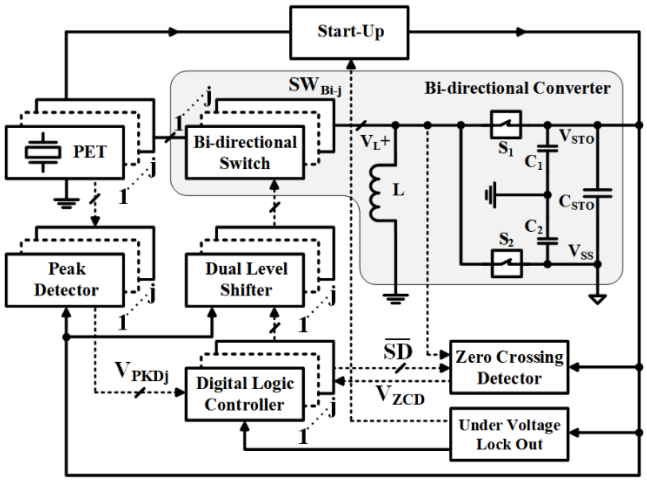

Fig. 3. System block diagram of the proposed multi-PET energy harvesting system. The shaded area represents the Bi-directional converter. The dashed lines connecting the blocks indicate control signals and the solid lines indicate power flow. The cascaded boxes represent the blocks replicated for each PET.

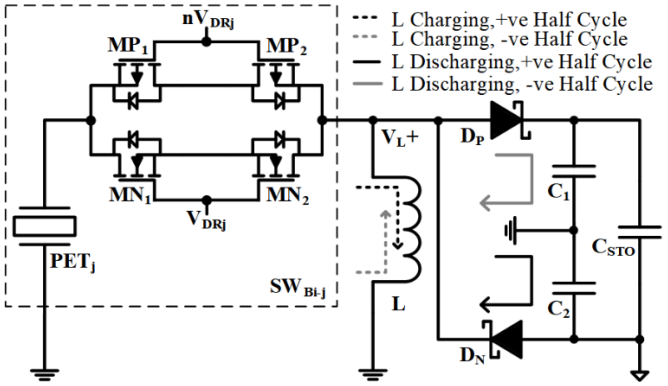

Fig. 4. Schematic of the bi-directional switching converter. The dashed box highlights the bi-directional switch which is replicated for each additional PET. Dashed and solid lines indicate the direction of the inductor charging and discharging current, respectively.

consists of a bi-directional switch SW_{Bi}, two unidirectional switches $S_{1\text{-}2}$, inductor L and capacitors $C_{1\text{-}2}$. $SW_{Bi\text{-}j}$ can conduct and block current in either direction to ensure that the energy extraction from one PET does not affect other PETs. When v_{PET} reaches a positive peak, $SW_{Bi\text{-}j}$ is closed and the respective C_{PET} starts to discharge through L. When C_{PET} is completely discharged, the current i_L in the inductor reaches a positive peak and SW_{Bi} is opened. The inductor tends to maintain the flow of current through it by lowering the voltage at V_L+ node, facilitating the flow of i_L through L-S_2-C_2 path, charging C_2. The above process repeats itself in the negative half-cycle. The energy is ultimately transferred into the storage capacitor C_{STO} by charge recycling; the details of which can be found in [24]. In the split-capacitor topology used here, there are two separate reference voltages indicated by different ground symbols in Fig. 3. The PET's reference voltage (V_{REF}) is different from C_{STO}'s reference voltage (V_{SS}) and all the blocks in the system are referenced to the latter unless otherwise stated.

The DLS block serves both as a gate driver and a level shifter. The PKD block is used for detecting both positive and negative voltage peaks of v_{PET}. An instance of this block is replicated for each PET in the array. The ZCD block detects the zero crossing events of the v_{PET} waveform, i.e. positive to negative transition and vice versa. However, unlike PKD, the ZCD is shared among multiple PETs and monitors the V_L+ node which starts following the PET terminal voltage when the respective $SW_{Bi\text{-}j}$ switch is closed. The ZCD block has a shutdown feature to save power. The output of the PKD and ZCD blocks, i.e. V_{PKD} and V_{ZCD}, are fed to the DLC block which generates the control signals for $SW_{Bi\text{-}j}$. The Start-up block helps to kick start the circuit when C_{STO} is fully depleted or partially discharged below the minimum voltage for normal operation. To avoid such a scenario, the UVLO block cuts off the power supply to the PKD, ZCD, DLC blocks and the load. Simultaneously, the UVLO block enables the Start-up block to charge C_{STO} back to the required voltage threshold.

The PKD and ZCD blocks are directly powered by V_{STO}, whereas the DLC and the load are powered by the regulated V_{DD} output from the UVLO output. Since DLC is powered from a voltage different from that of PKD and ZCD, voltage level translation is needed for signals in the DLC block.

III. Implementation – Device Selection and Tradeoffs

This section provides details of the circuit implementation along with the design trade-offs as part of the device selection process. Since the target input power range is within a few hundred microwatts, circuit elements were carefully chosen to limit the circuit's power consumption to few tens of microwatts. Since ambient energy is intermittent in nature, special emphasis is given to limit the circuit standby power consumption. Circuit design ensures that the selected devices function reliably within the V_{STO} range of 2.7 V – 5 V.

A. Bi-directional Switching Converter (BSC)

The main component in the BSC block is the bi-directional switch, SW_{Bi} which is implemented using a parallel combination of series connected NMOS and PMOS transistors as shown in Fig. 4. The back-to-back configuration of MOSFETs ensures that the internal body diodes do not conduct inadvertently. Both PMOS and NMOS transistors are required to complement each other, since none of the MOSFETs conduct efficiently in both half-cycles. The bi-directional switch used here has been previously used in a system [23] with a combination of DBR and NVC as the rectification stage. $S_{1\text{-}2}$ are Schottky diodes with voltage drop V_F = 320 mV at a forward current of 10 mA and a maximum reverse leakage current, I_R of 500 nA. While a 2.2 µF capacitor is used for C_1 and C_2, a 3.3 mH inductor with a DCR = 3.2 Ω is used for L. In the bi-directional switch, though the series connection of NMOS transistors doubles the ON-state resistance of the NMOS pair ($R_{DS(ON\text{-}N)}$), it is balanced by the parallel PMOS pair ($R_{DS(ON\text{-}P)}$) during the period when both pairs conduct. The resulting series resistance $R_{SW\text{-}Bi}$ is given by (3)

$$R_{SW-Bi} = \left(2\times R_{DS(ON-P)}\right) \| \left(2\times R_{DS(ON-N)}\right) \quad (3)$$

The PMOS transistor has a higher value of gate capacitance compared to its NMOS counterpart for the same value of $R_{DS(ON)}$. A large gate capacitance translates to higher switching losses in the gate driver circuit but reduces conduction losses. The switching losses in the gate driver circuit is proportional to the total gate charge, Q_g. The MOSFETs were chosen as a

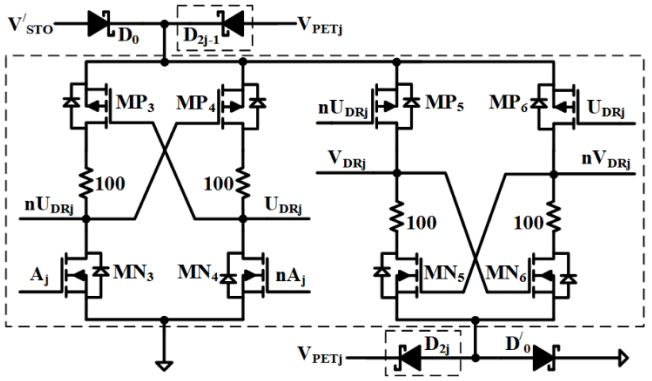

Fig. 5. Schematic of the dual level shifter. The section of the circuit in the dashed boxes requires replication for each additional PET.

trade-off between Q_g and $R_{DS(ON)}$. Also, it was ensured that the MOSFETs have extremely low values of drain to source leakage current (I_{DSS} < 100 nA) and can withstand the voltage stress encountered when the MOSFETs are off (V_{DSS} > 8V). The diodes D_P and D_N are Schottky diodes (NXP PMEG4002) with a forward voltage drop (V_F) of 320 mV at a forward current (I_F) of 10 mA. The maximum reverse leakage current (I_R) of the selected diodes is 500 nA at a reverse voltage (V_R) of 25V. Schottky diodes with even lower V_F values were available; however, the I_R value increased drastically in those cases. For e.g., BAT754 Schottky diode has a lower V_F compared to the selected diode. However, upon comparing the I_R values of both diodes, it was observed that the I_R value of BAT754 is four times that of the selected diode, which leads to significant losses during standby.

A 3.3 mH through hole inductor with a DC Resistance (DCR) of 3.2 Ω and a volume of 1990 mm^3 is used for testing the prototype. Increasing the inductance by keeping the resistance minimal will improve power efficiency at the expense of size. However, an important point to note here is that, increasing the inductance of the inductor increases the time t_{SECE} needed for charge transfer. This causes the control circuits to operate longer accompanied by an increase in intrinsic power consumption. There is a critical inductance value beyond which increasing it would adversely affect the system's power efficiency. In discrete implementations, the critical value would be reached at a lower value of inductance due to the relatively higher intrinsic power demand. The inductor was chosen as a trade-off between an acceptable efficiency and size.

A value of 2.2 µF was used for C_1 and C_2, whereas a much higher capacitance of 100 µF was used for the storage capacitor, C_{STO}. A large capacitance reduces the ripple across the split-capacitors and eliminates issues during start-up. During the transition phase from start-up to SECE, there is a slightly higher current draw from C_{STO} causing V_{STO} to drop. If C_{STO} were a small value, the drop in V_{STO} would be large and this would lead to oscillations around the point and the system would fail to start up.

B. Dual Level Shifter (DLS)

At the start of the SECE process, the PET's ground is level shifted by V_{STO}/2 with reference to V_{SS} ground. Hence, even if the switch control signals from the DLC had a voltage level of

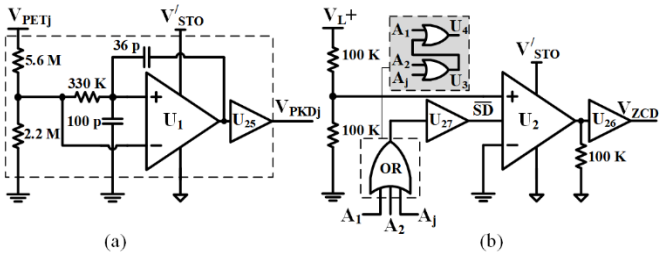

Fig. 6. Schematic of the (a) peak detector, (b) zero-crossing detector. An instance of the circuit in the dashed box is required for each additional PET. The 3-input OR gate is implemented using two 2-input OR gates as shown inside the dashed box (shaded).

$V_{OH(MAX)} = V_{STO}$ and $V_{OL(MIN)} = VSS$, it would not have been sufficient to completely turn-off the PMOS and NMOS transistors inside SW_{Bi} when condition (4) is encountered.

$$|V_{PET(peak)}| \geq (V_{STO}/2) + |V_{TH}| \quad (4)$$

The dual level shifter (DLS) shown in Fig. 5 serves two purposes: (1) to shift voltage of DLC to a higher level in both positive and negative directions. For example, 0 V ~ +2.5 V is level shifted to -3.5V ~ +3.5V with respect to V_{SS} (2) to choose the most positive and negative voltages from the two available voltages, V_{PET} and V_{STO}. The DLS uses cross-coupled PMOS transistors in the first stage to shift the level in the positive direction and uses cross-coupled NMOS transistors in the second stage to shift the level in the negative direction. Diodes D_0-$D_{(2j-1)}$ and D'_0-$D_{(2j)}$ select the most positive and negative voltages, respectively from the V_{STO} and V_{PET} voltages, where j is the number of PETs used. A 100 Ω resistor is used to limit the short-circuit current in each branch of the driver circuit when both PMOS and NMOS transistors conduct during a switching event. In the DLS circuit, the MOSFETs are required to switch fast enough to minimize shoot-through current and hence low values of Q_g is preferred over $R_{DS(ON)}$ for MOSFETs $MP_{3\text{-}6}$ and $MN_{3\text{-}6}$. The DLS circuit has been adapted from [23], [29] for level shifting gate driving voltages in both positive and negative directions.

C. Peak Detector (PKD)

A schematic of the peak detector is given in Fig. 6(a). A comparator, U_1 compares the scaled version of v_{PET} with a delayed version of the same. An RC low-pass filter formed by a 330 kΩ resistor and a 100 pF capacitor is used to create a delayed version of $v_{PET,}$ with approximately 40 µs delay. The chosen delay is small enough for accurate peak detection, and at the same time sufficiently large to prevent erroneous triggering due to noise. The design of the PKD block has been adapted from [29] for use with both positive and negative input voltages. Since the peak detector circuit is an always-on block, a low-power comparator (TS881) which consumes a quiescent current of 220 nA at 2.7 V is selected. Dynamic hysteresis provided by a 36 pF capacitor prevents oscillations at the output. A voltage divider formed by resistors, 5.6 MΩ and 2.2 MΩ, scales the voltage to a suitable range and sets the minimum v_{PET} voltage for peak detection to 500 mV. The chosen voltage division ensures that the harvesting process is not triggered by a signal which is unable to provide a positive power budget. The comparator's output V_{PKDj} toggles from low to high (L→H) when v_{PET} reaches a positive peak and vice versa at the negative peak. U_{25} is used at the output of U_1 to

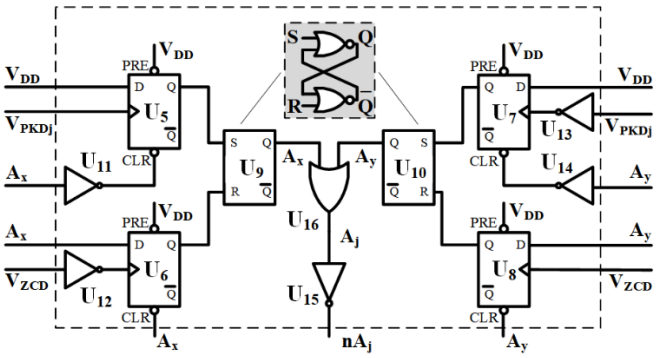

Fig. 7. Schematic of the control circuit. The SR latch is implemented using two NOR gates as shown inside the dashed box (shaded).

translate the voltage level of V_{PKDj} to V_{DD}. The amount of power lost due to an inaccurate peak detection is given by (5).

$$P_{Peak-Loss} = CV_{PET}^2\left(1-\mathrm{Cos}^2\,\omega_{VIB}t_{dly}\right)\Big/T_{VIB} \quad (5)$$

D. Zero Crossing Detector (ZCD)

The circuit schematic of ZCD is shown in Fig. 6(b). A comparator U_2 is used for zero crossing detection and utilizes a comparator which is faster than the PKD comparator by two orders of magnitude. The ZCD circuit should be quick enough to respond to the zero-crossing event. Since U_2 consumes a high quiescent current, it is enabled only when a peak detection event has occurred and is immediately disabled after the zero-crossing event. The shutdown signal ($\overline{SD}$) is generated by the DLC. Since the output of U_2 is tri-stated when shut down, a 100 kΩ resistor is added at the output to connect the CMOS input of the following stage to power supply ground. Two 100 kΩ resistors generate a scaled version of V_L+ voltage at the non-inverting terminal of the comparator and is compared with the PET ground. The output of the comparator V_{ZCD} toggles from High to Low (H→L) when V_L+ crosses zero to become negative and vice versa, i.e. when V_L+ crosses zero to become positive. Since the ZCD circuit is shared among multiple PETs, individual shutdown requests are sent to the comparator via an OR logic implemented by U_3 and U_4. U_{26} is engaged at the output of U_2 to translate the voltage level of V_{ZCD} to V_{DD}. During the design phase, it was observed that options for a low power (< 500 µA at 5 V) comparator with a shutdown feature were limited to a few, such as the MAX9030 from Maxim Integrated and LMV761 from Texas Instruments (TI). Though MAX9030 is rated to consume lower power, LMV761 was chosen due to the lower input offset voltage and the availability of a simulation model. LMV761 is a fast comparator with a maximum t_{PD} of 120 ns (at V_{DD} = 5 V) with 50 mV overdrive at its inputs.

E. Digital Logic Controller (DLC)

The circuit shown in Fig. 7 is the DLC that generates the control signals for SW_{Bi-j}. The circuit consists of two sections, each handling the signal generation in one half-cycle. The circuit comprising D flip-flops, U_{5-6}, inverters, U_{11-12} and SR latch, U_9, control the generation of signal, A_x, whereas the circuit consisting of D flip-flops, U_{7-8}, inverters, $U_{13-14}$and SR latch, U_{10}, control the generation of signal, A_y. The OR gate, U_{16} ensures that the switch control signal, A_j is high (i.e. SW_{BI-j} is closed), when either of the signals, A_x or A_y is high. All the flip-flops used are positive edge triggered and have a clear (CLR) and pre-set (PRE) input.

Initially, when both A_x and A_y are low, U_6 is cleared (Q = 0) and only U_5 is enabled. The V_{PKD} signal toggles from L→H when a positive peak is detected, which causes the Q output of U_5=1 which sets (S = 1, R = 0) the Q output (A_x = 1) of U_9. Since A_x remains high, the output of U_{11} becomes low, forcing U_5 to enter and U_6 to exit, a cleared state. However, the output of U_9 remains unchanged (A_x = 1) since S = R = 0. The V_{ZCD} signal toggles from H→L when V_L+ crosses zero to become negative. Inverter U_{12} is used to convert the H→L transition of the V_{ZCD} signal to a L→H transition, which sets U_6. The output Q of U_6 goes high which resets (S = 0, R = 1) the Q output (A_x = 0) of U_9, opening SW_{BI-j}. The operation mentioned above repeats in the negative half-cycle, when the V_{PKD} signal toggles from H→L (negative peak), setting A_y = 1 and closing the switch. The switch is opened again when A_y = 0 due to the L→H transition of the V_{ZCD} signal at D input of U_8.

All the logic devices used for implementing the DLC block are selected from TI's Advanced Ultra-Low Power (AUP) family of devices, mainly owing to their ultra-low dynamic power and quiescent current consumption.

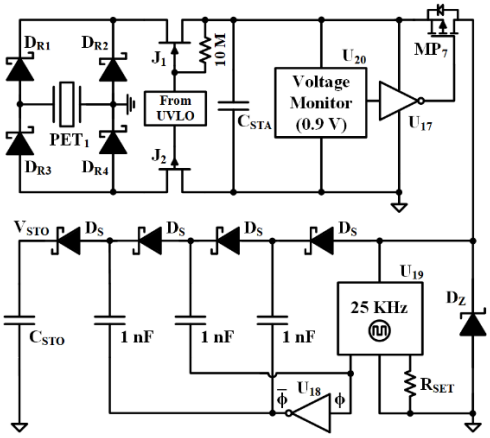

Fig. 8. Schematic of the start-up circuit, comprising of an input rectifier followed by a 4-stage charge pump. A resistor of 5.6 MΩ sets the frequency of the clock generator to ~20 kHz.

F. Self-startup Circuit

The storage capacitor, C_{STO} is initially charged through a start-up circuit connected to PET_1, which consists of a DBR followed by a four-stage Dickson Charge Pump (DCP) as shown in Fig. 8. A diode implementation was chosen for the DCP to avoid the need for a complex control circuitry. To facilitate start-up, two normally-on switches J_{1-2} are used to provide the initial conduction path which is later cut-off by the UVLO block, when SECE circuit starts operation. A filter capacitor, C_{STA} is connected at the output of the DBR and is continuously monitored by a supply voltage monitoring circuit, U_{20} with a preset upper (V_{PRE+}) and lower (V_{PRE-}) threshold voltage of 975 mV and 900 mV, respectively. When $V_{STA} > V_{PRE+}$, the output of U_{20} turns PMOS switch, MP_7 on, which connects the C_{STA} to the DCP. If the input power is not high enough to maintain $V_{STA} > V_{PRE-}$, MP_7 is disabled and is re-enabled only when $V_{STA} > V_{PRE+}$, gradually charging C_{STO} to the desired voltage level. A 25 kHz, 50% duty cycled clock signal to drive the switching capacitors in the DCP is generated

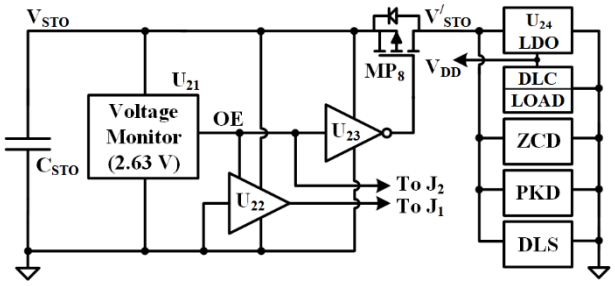

Fig. 9. Schematic of the Under Voltage Lock Out circuit. The output of the circuit controls the power to the sub-circuits and controls the JFETs J_1 and J_2 in the start-up circuit.

using a resistor-tuned CMOS oscillator, U_{19}. An inverter, U_{18} generates the 180° degree out of phase signal needed for the DCP. U_{19} has an operating voltage range of 0.9 V – 2 V and is hence protected against an over-voltage condition using a low leakage Zener diode, D_Z, which regulates the supply voltage of U_{19}.

Diodes $D_{R1} - D_{R4}$ and D_S use NXP PMEG4002EB and were selected for having the lowest V_F within an acceptable I_R limit of < 200 nA at V_R < 5 V. BF862 (N-Ch) is used for JFET J_1, whereas MMBFJ177 (P-Ch) is used for JFET J_2. JFETs were selected to have the lowest $V_{GS\text{-}OFF}$ voltage among available options. TPS3839A09 (U_{20}) is a voltage monitoring chip with a threshold setting of 0.9 V and an ultra-low current consumption of 150 nA at 5 V. U_{17} and U_{18} are low-power Schmitt-trigger inverters for logic-level inversion and are implemented using SN74AUP1G14 from TI's AUP family of logic devices. NX3008P (MP_7) is a P-Ch MOSFET with a low gate-source turn-on voltage, V_{GSth} = 0.9 V, ideal for starting up from low voltages. TS3001 (U_{19}) is a resistor tuned CMOS oscillator which produces a 25 kHz, 50% duty cycled, clock signal, chosen mainly because of its lowest current consumption of 1 µA at 1 V.

G. Under Voltage Lock Out and Low Dropout Regulator

In the absence of ambient vibrations, V_{STO} could fall below the working voltage of the control circuits. To prevent such a situation, the load and control circuits are disconnected from C_{STO} when $V_{STO} < V_{PRE\text{-}}$ = 2.63V and is re-enabled only when $V_{STO} > V_{PRE+}$ = 2.66 V. This is accomplished using an Under-Voltage Lock Out (UVLO) circuit shown in Fig. 9, which deactivates MP_8. Additionally, the UVLO circuit disables the JFETs J1 and J2, when VSTO > VPRE+ and re-enables the same when VSTO falls below VPRE-, enabling the start-up circuit. The UVLO circuit comprises of a voltage monitoring circuit U21, a tristate buffer, U22, and an inverter, U23. If the gate of J1 were driven using a CMOS output from the UVLO block during an under-voltage condition, a high voltage at J1's gate would cause excessive current flow through its gate and cause the start-up circuit to fail. Hence a tristate buffer, U22 is used for driving the gate of J1. The start-up circuit is disabled by driving the gate of the J1 to the lowest and J2 to the highest potential available in the system. J1 has a typical VGS-OFF value of 0.8 V, which causes the drain end of J1 to be at 0.8 V when turned off. If the drain end needs to be at 0V, the gate needs to be pulled down further to –0.8V which is not feasible without additional circuitry. However, the start-up circuit is not activated by the 0.8 V at CSTA because U20 needs a minimum voltage of 975 mV to enable MP7. A 10 MΩ resistor is added between the drain and the gate of J1 to speed up turn-on from a disabled state.

TABLE I
COMPONENT LIST

REFERENCE DESIGNATOR	PART NUMBER / VALUE	REFERENCE DESIGNATOR	PART NUMBER / VALUE
U_1	TS881	U_{27}	ADG3301
U_2	LMV761	D_Z	MMSZ4678
$U_{3\text{-}4,\ 16}$	SN74AUP2G32	$D_{P,\ N,\ R1\text{-}R4,\ S}$	PMEG4002EB
$U_{5\text{-}8}$	SN74AUP1G74	D'_0, $D_{0,\ 2j\text{-}1,2j}$	BAS70
$U_{9\text{-}10}$	SN74AUP2G02	J_1	BF862
$U_{11\text{-}15}$	SN74AUP3G04	J_2	MMBFJ177
$U_{17\text{-}18}$	SN74AUP1G14	$MN_{1\text{-}2}$	BSS806N
U_{19}	TS3001	$MP_{1\text{-}2,8}$	NX2301P
U_{20}	TPS3839A09	$MP_{3\text{-}7}$	NX3008P
U_{21}	TPS3839L30	$MN_{3\text{-}6}$	NX3008N
U_{22}	SN74AHC1G126	R_{SET}	4.32 MΩ
U_{23}	SN74AHC1G14	L	ELC10D332E
U_{24}	ISL60002-25	C_{STO}	100 µF
$U_{25\text{-}26}$	SN74LVC1G34	$C_{1,2}$, C_{STA}	2.2 µF, 1 µF

U_{21} is implemented using TI's TPS3839L30, which is a voltage monitoring chip with a lower voltage threshold of 2.63 V and an ultra-low current consumption of 150 nA at 5 V. The chip has an upper voltage threshold of 2.66 V at which other sub-circuits commence operation due to the turn-on of MP_8, a P-Ch MOSFET. MP_8 is implemented using NX2301P which has a very low $R_{DS(ON)}$ of 155 mΩ at a V_{GS} of 2.7 V. U_{22} uses a non-inverting buffer, SN74AHC1G126 with a 3-state output and an ENABLE input, whereas U_{21} uses an inverting buffer, SN74AHC1G14. Both the above buffers where chosen due to their wide operating range (2 – 5.5 V) and low quiescent current consumption of 1 µA at 5 V.

The logic devices used to implement the DLC circuit have very low dynamic power and quiescent current consumption but have a limited operational voltage range of 0.8 V to 3.6 V. C_{STO} voltage varies from 2.7 V to 5 V and if directly powered would damage the DLC circuit. Instead, the DLC circuit is powered using a LDO (U_{24}) which provides a fixed voltage of 2.5 V from an input voltage as low as 2.7 V. The LDO consumes a quiescent current of 350 nA, the least current among the available design choices.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. PCB prototype and experimental setup

A double layer Printed Circuit Board (PCB) measuring 50 × 100 mm² was fabricated and assembled with off-the-shelf components listed in Table I. To demonstrate the functionality of the developed prototype, three PETs from Mide Technologies (PPA-4011) with different resonant frequency of 60, 65 and 70 Hz were selected; and the corresponding internal capacitances were 400 nF, 404 nF and 408 nF, respectively. The PETs were mounted using screws on an electromagnetic shaker (Sentek Dynamics VT-20) driven by a power amplifier (Sentek Dynamics LA-100). The sinusoidal signal was provided by a vibration controller (Dynatronic Corp. VENZO-820), which received feedback from an accelerometer

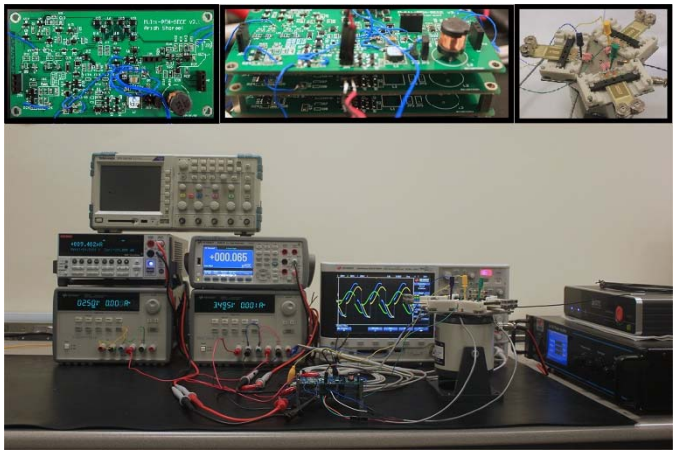

Fig. 10. Measurement setup. The multiple PETs mounted on the shaker and stacked PCBs are shown in the inset.

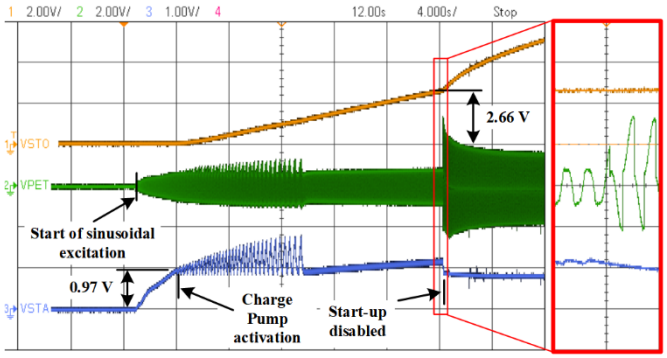

Fig. 11. Startup time-domain waveforms. The zoom-in figure is the waveform during the transition from start-up to SECE. Upon activation of the SECE technique, the V_{STO} waveform can be seen rising at a faster rate.

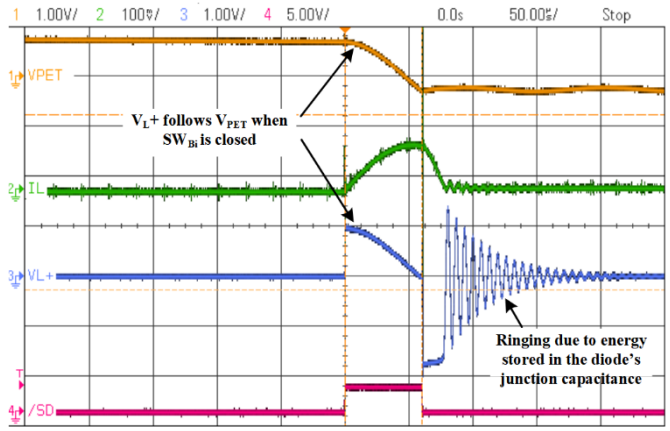

Fig. 12. Acquired characteristic voltage and current waveforms associated with the SECE technique.

(Bruel & Kjaer 4519-003) mounted on the shaker plate as shown in Fig. 10.

B. *Self-startup mechanism and transition to SECE*

The start-up mechanism is demonstrated in Fig. 11, where the start-up circuit charges a 100 µF capacitor from 0 V to 2.7 V. In the same figure, the UVLO circuit can be seen disabling the start-up circuit and enabling the SECE circuit simultaneously, which can be verified by the characteristic voltage enhancement associated with the SECE technique

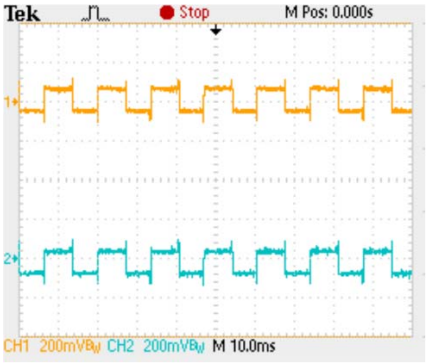

Fig. 13. Voltage across capacitors C_1 (Channel 1) and C_2 (Channel 2) measured using an isolated channel oscilloscope. Though voltage across individual capacitors vary as shown, the difference V_{C1} - V_{C2} is constant.

shown in the inset. The start-up circuit starts to harvest energy from a voltage as low as 650 mV across PET_1. When V_{PET1} = 650 mV, C_2 is charged to a voltage of about 325 mV through diode D_{R3} which increases the DC level of v_{PEH} by 325 mV, making V_{STA} = 975 mV and activating U_{20}. The V_F of diodes D_{R1}-D_{R4} drops to a very low value when I_F (C_{STA}'s charging current) is weak, which enables starting up from 650 mV but takes over 427 s to complete. As expected, start-up time improves significantly with increasing input power.

To verify successful operation of the energy harvesting circuit, typical waveforms associated with SECE are acquired using an oscilloscope and is shown in Fig. 12. A 10 Ω sensing resistor is added in series with inductor to measure i_L. Ideally, upon commencement of SECE, the voltage across the PET should be twice the open circuit voltage. However, once SECE is activated, the voltage measured across the PET device is only 1.6 (at resonance) and 1.78 (at off-resonance) times the open circuit voltage. Delay in peak detection due to the RC network, delay in zero crossing detection due to the comparator's input offset error, aggravated by voltage scaling contribute to non-doubling of the open circuit voltage at resonance and off-resonance. However, the effect of electromechanical damping is significant at resonance and hence the lower voltage magnification compared to off-resonance. Similar results have been reported in [25]. Fig. 13 shows the voltage across the split capacitors C_1 and C_2, which was measured using an isolated channel oscilloscope (TPS2014B) to avoid shorting of supply ground. The voltage across the split capacitors can be seen varying when charge is deposited on them, but the voltage difference, V_{C1} - V_{C2} is fixed, due to the large value of C_{STO}.

C. *SECE operation with multiple PETs*

The ability of the system to handle multiple PETs is demonstrated by stacking two additional PCBs to the fully assembled main board as shown in the inset of Fig. 10. For testing purposes, each PCB was designed such that more number of PETs could be easily added to the system by stacking one on top of the other. Fig. 14 shows the input waveforms of the multiple PETs functioning at the same time. To demonstrate the merits of SECE when combining multiple PETs, Table II shows the actual combined power output of the three-PET system versus the expected power output, which is the summation of the power outputs of individual PETs activated one at a time. It can be observed that the combined

TABLE II
POWER OUTPUT FROM MULTIPLE PETS

V_{STO} (V)	P_{OUT1} (μW)	P_{OUT2} (μW)	P_{OUT3} (μW)	EXPECTED $P_{OUT(1+2+3)}$ (μW)	ACTUAL $P_{OUT(1+2+3)}$ (μW)	*COMBINING EFFICIENCY (%)
2.7	96.9	26.5	115.3	238.7	237.5	99.4
3.0	99.9	27	121.2	248.1	247.4	99.7
3.5	100.1	27.6	126.7	254.4	253.9	99.8
4.0	100.8	27.7	128.6	257.1	256.7	99.8
4.5	102.2	27.9	128.8	258.9	258	99.6
5.0	103.5	28	130	261.5	259.7	99.1

*Combining efficiency is the ratio of actual power output to the expected power output.

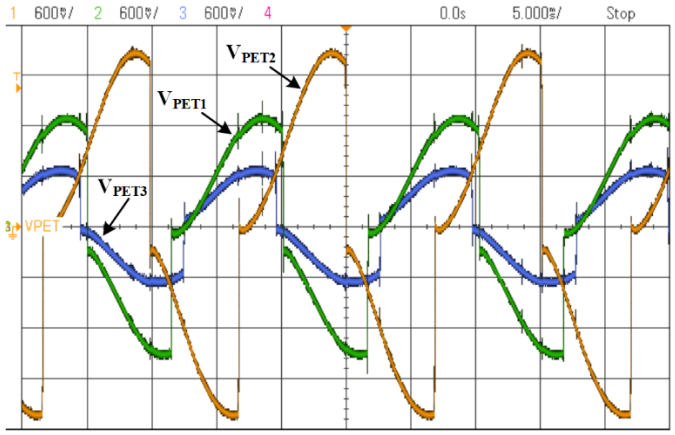

Fig. 14. Oscilloscope capture showing multiple-PET operation. The frequency of vibration was set to 65 Hz.

power output is almost equal to sum of the individual power outputs, which demonstrates the efficiency of combination. Combining multiple PETs in this manner is beneficial for broadband operation. However, there are certain limits which need to be considered. The maximum number of PETs, j_{max} which can be combined is given by (6); approximated to the lower integer.

$$j_{max} \leq \frac{T_{VIB}}{2\left(t_{SECE-max} + t_{store-max}\right)} \quad (6)$$

where $t_{SECE-max}$ is the maximum time taken for C_{PET} to discharge into L, $t_{store-max}$ is the maximum time taken for L to discharge into C_1 or C_2. An approximate value of j_{max} could be determined by observing the waveform shown in Fig. 12. $t_{SECE-max} + t_{store-max}$ is approximately equal to 75 μs, which sets j_{max} = 102. A more thorough analysis of the timings can be found in [23]. Equation (6) does not take into account the delays associated with the control circuits when responding to a peak or zero crossing event, which when considered, will further reduce the value of j_{max}. The system complexity and intrinsic power consumption will increase with the number of transducers since each PET requires dedicated PKD, DLS and DLC blocks. However, the intrinsic power consumption per PET remains constant.

It must be noted here that when working with large number of PETs an arbitration mechanism (arbitrator) helps to handle the assignment of the inductor to each PET reliably when multiple adjacent voltage peaks are present. In the proposed system, the converter would operate at a lower efficiency when a peak occurs on one PET and the inductor is being engaged by another PET. However, the probability of occurrence of such a

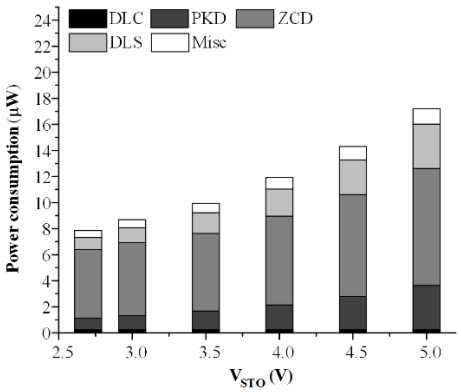

Fig. 15. Measured intrinsic power consumption (normalized to three sources) of the sub-circuit blocks at different storage voltages.

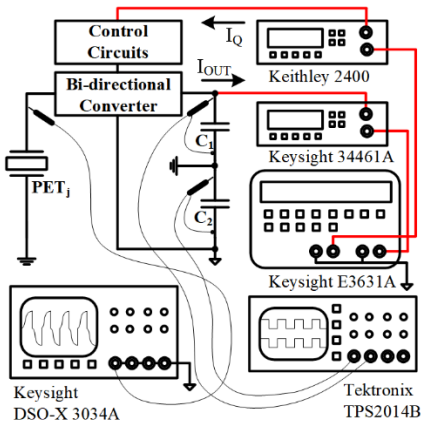

Fig. 16. Schematic of the test setup used for measuring efficiency of the converter and intrinsic power consumption of the circuit blocks. A digital storage oscilloscope (DSO-X 3034) is used for acquiring the input waveform. An isolated channel oscilloscope (TPS2014B) is used solely for measuring the voltage across the split capacitors.

scenario is very low in the lower frequency range because of the quasi-instantaneous nature of the energy transfer between resonant circuits C_{PET}-L and L-C_{STO}. The 3.3 mH inductor used in the design is engaged by the PET for a duration as small as 0.15 ms in a cycle spanning 15.3 ms (at 65 Hz test frequency), which translates to an occupancy rate of 1% of the inductor for a single PET system and 3% for a 3-PET system.

D. Intrinsic Power Consumption and Converter Efficiency

A block level power consumption breakdown of all sub-circuits such PKD, ZCD, DLS and DLC is shown in Fig. 15. The Miscellaneous (Misc.) power consumption is dominated by the 350 nA quiescent current drawn by the LDO, followed by the 150 nA leakage drawn by the diodes $D_{P,N}$ and the rest by the voltage monitoring chip in the UVLO. The power consumed by individual blocks were calculated by taking the product of the voltage and current supplied using a Keithley 2400 source meter as shown in Fig. 16. During normal operation, the intrinsic power consumption of all the sub-circuits except the DLS is only dependent on the V_{STO} voltage. The DLS circuit's power consumption is also dependent upon the input voltage levels when condition (4) is encountered. When no vibrations are present, there is no switching activity, but, there is a standby current varying from 1.65 μA to 1.9 μA when V_{STO} is swept from 2.7 V to 5 V. This translates to a standby current of 560 nA/PET at 3 V, which is

TABLE III
COMPARISON WITH EXISTING PIEZOELECTRIC ENERGY HARVESTING CIRCUITS

Parameters	[17]	[26]	[18]	[23]	**This work**
Technology	2-µm Bi-CMOS	0.35-µm CMOS	0.32-µm BCD	Discrete	**Discrete**
Technique	Rectifier-free SECE	SECE, NVC	SECE, eNVC[1,2]	SECE	**Rectifier-free SECE**
No. of PETs	1	1	1	3	**3**
Inductance [volume mm^3]	160 µH [27]	10 mH [8478]	10 mH, 560 µH [7085]	10 mH [2448]	**3.3 mH [1990]**
Self-Startup	No	Yes	Yes	Yes	**Yes**
Input voltage	Up to 1.2 V	Up to 20 V	Up to 5 V	Up to 20 V	**Up to 3.5 V**
Standby Power	n.a.	n.a.	160 nA @ 3V	930 nA[3] @ 3V	**560 nA[3] @ 3V**
Output Power	30 µW	59 µW[5]	56.3 µW[4]	33 µW[4]	**254** µW
Intrinsic Power	n.a.	3 µW @ 3V	1.3 µW @ 3V	10 µW @ 3V	**10** µW @ 3V
Timing control	Preset	Adaptive	Adaptive	Preset	**Adaptive**
LV Efficiency	50%	69%	85.3%*	62%*	**79%***

[1]eNVC stands for enhanced negative voltage converter. [2]Uses two inductors. n.a. = not available. [3]Per PET. [4]Calculated from efficiency curve. [5]Data extracted from efficiency curve in author's PhD thesis. *Excludes losses due to intrinsic power consumption.

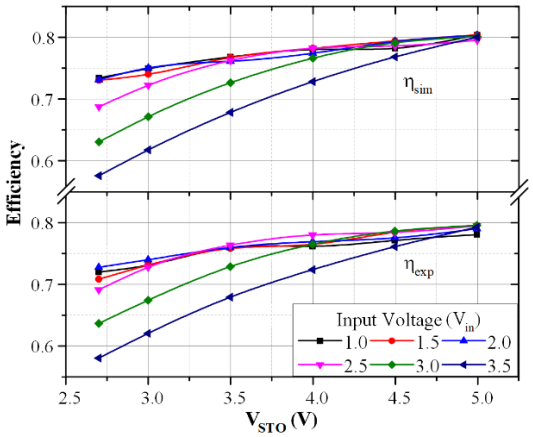

Fig. 17. Simulated (top) and experimental (bottom) efficiency of the bi-directional converter plotted against output voltage, V_{STO}. The efficiency is plotted for different input voltages, V_{in} ranging from 1.0 V to 3.5 V. The efficiency values do not include control circuit losses.

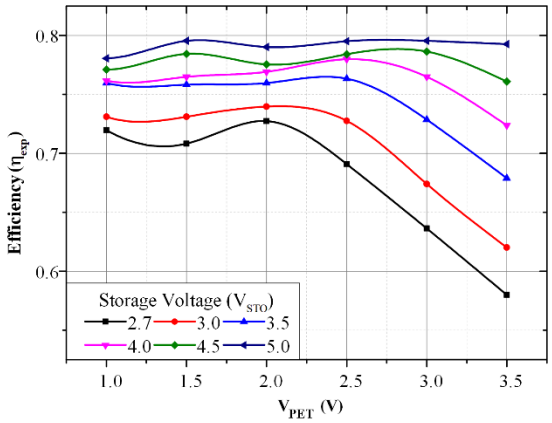

Fig. 18. Plot showing the variation of efficiency (experimental) w.r.t. the input voltage. The multiple curves are the various efficiency values at different storage voltages. The efficiency values do not include control circuit losses.

one of the lowest reported result thus far for a discrete SECE implementation. Energy stored in C_{PET} is given by $1/2C_{PET}V_{PET}^2$ and since the harvesting circuit extracts energy from the transducer twice during T_{VIB}, the input power, P_{in} into the harvester is given by $C_{PET}V_{PET}^2 f_{VIB}$ [26]. The output power, P_o is calculated as $V_{STO} \times I_{OUT}$, where I_{OUT} is measured using the arrangement shown in Fig. 15. The bench multi-meter, Keysight 34461A displays the current, I_{OUT} flowing into the power supply, which is set at a certain V_{STO} voltage. Power conversion efficiency, η of the bi-directional switching converter is given by (7) and is dependent on the input voltage, V_{PET} as well as the output voltage, V_{STO}.

$$\eta = \frac{V_{STO} I_{OUT}}{C_{PET} V_{PET}^2 f_{VIB}} \tag{7}$$

Both experimental, η_{exp} and simulated efficiency, η_{sim} of the bi-directional converter are plotted in Fig. 17. The simulation was carried out in Cadence OrCAD PSpice using device models obtained from their respective manufacturers. Since P_{in} is constant at a particular V_{PET}, the efficiency increases with an increasing V_{STO} as the converter needs to transfer the same amount of energy to the output capacitors at a higher voltage ($V_{STO} + V_F$) and shorter time, which reduces conduction losses at the output side. The converter achieved a peak power conversion efficiency of 79% during experiments and 80% during simulations. The measured efficiency is also plotted against the input voltage, V_{PET} for different V_{STO} values in Fig. 18. It can be observed that the topology proposed here provides power efficiencies higher than 70% for input voltages lower than 2.4 V and has efficiency greater than 58% in the entire input voltage range. The sub-circuits of the PEH system were powered separately to measure their intrinsic power consumption and to identify the efficiency of power conversion of the BSC block.

The design has the best power conversion efficiency at high output voltages, and this is due to the reduction in conduction losses as discussed earlier. Nonetheless, an efficiency loss is observed for $V_{PET} > V_{STO} + V_F$. This is attributed to the two discharge paths for C_{PET} when the switch is closed at peak voltage. A part of the charge in C_{PET} discharges through the split capacitor and the rest through the inductor. The current through the diode path is high compared to the inductor charging current, causing higher conduction losses in the

diodes. This can be observed in the efficiency curves presented in Fig. 17 and Fig. 18. Nevertheless, as the output voltage, V_{STO} rises, the conversion efficiency improves.

Table III provides a performance comparison with the state-of-the-art piezoelectric energy harvesting circuits. Efficiency of the state-of-the-art circuits in the Low Voltage (LV) range is compared with the efficiency of the proposed circuit. For that purpose, 0 – 5 V has been set as the 'LV range'. The integrated SECE circuit reported in [17] uses the smallest inductor amongst all the compared designs and achieves a peak efficiency of 50%. However, the design lacked a start-up circuit and requires an external negative supply voltage. The timing control for the switches must be externally fed. The authors in [26] reported a self-powered SECE circuit with a peak efficiency of 85% across its input range of operation, which is 0 V to 20 V. The design used a 10 mH inductor which is bulky due to the lower DCR. The peak efficiency of the above circuit in the LV range is 69% at 5 V, which corresponds to a P_{in} of 85.3 µW. The PET used in this work provided an equivalent amount of power at 1.8 V and the proposed design has a peak efficiency of 78% at 1.8 V, with a smaller 3.3 mH inductor, which shows the advantage of using a rectifier-free design. The authors in [18] demonstrated a dual-inductor based IC with 85.3% peak efficiency using the Residual Charge Inversion (RCI) method. However, the design used a 560 µH inductor for RCI in addition to the 10 mH inductor for the SECE converter. In [23], the authors demonstrate a discrete implementation of an SECE circuit, capable of handling multiple PETs. The design uses a 10 mH inductor and the peak efficiency of the circuit in the LV range is 62 % at 5V, which corresponds to a P_{in} of 52 µW. The PET used in the proposed topology provided an equivalent amount of power at 1.4 V and the proposed design has a peak efficiency of 78% at 1.4 V. From the above discussion, it can be concluded that the high efficiency of 79% achieved by the proposed design is not by using a larger inductor; rather by reducing the conduction losses in the circuit through a rectifier-less topology.

V. Conclusion

A multi-input rectifier-free piezoelectric energy harvesting system capable of extracting energy from very low voltages, is presented here. The topology is well optimized for MPETs with high intrinsic capacitance and outperforms diode bridge rectifiers through non-linear energy harvesting. The system does not require reprogramming or external tuning and can adjust its system parameters to fit different types of PET devices. The use of SECE as the preferred technique has enabled sharing of the inductor with multiple PETs and to harvest energy from irregular vibrations without the need for complex maximum power point tracking circuits. In the presence of ambient vibrations, the control circuits consume an intrinsic current of 3 µA at 2.7 V, which is only a small portion of the harvested power. The circuit techniques pursued in this work has helped to achieve an ultra-low quiescent current consumption of 550 nA/PET at 2.7 V, thus saving the energy for the load during normal operation.

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