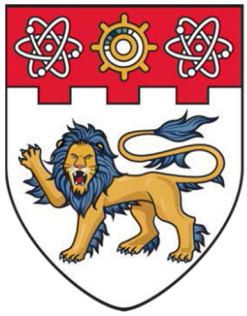

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

HIGH-PERFORMANCE AMORPHOUS INDIUM-GALLIUM-ZINC-OXIDE THIN-FILM-TRANSISTOR AND ITS APPLICATIONS

LI YUANBO

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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HIGH-PERFORMANCE AMORPHOUS INDIUM-GALLIUM-ZINC-OXIDE THIN-FILM-TRANSISTOR AND ITS APPLICATIONS

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2022

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

03/01/2023

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LI YUANBO

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Date

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Prof. Chen Tupei

Authorship Attribution Statement

This thesis contains materials from 3 papers published in the following peer-reviewed journals in which I am listed as the first author.

Chapter 4 is published as Y. Li, J. Sun, T. Salim, R. Liu, and T. Chen, "Performance Enhancement of Transparent Amorphous IGZO Thin-Film Transistor Realized by Sputtered Amorphous AlOx Passivation Layer," *ECS Journal of Solid State Science and Technology*, 2021, 10, 045006. DOI:10.1149/2162-8777/abf724.

Prof. Chen supervised the whole project and revised and edited the manuscript.

I conceptualized the idea, performed the device fabrication, characterized the device with TEM, analyzed the data, and prepared the manuscript.

Dr. Sun and Dr. Liu helped formulate the research goals and aims.

Dr. Salim conducted XPS analysis on the device.

Chapter 5 is published as Y. Li, T. Chen, X. Jun, and T. Salim, "Transparent electronic and photoelectric synaptic transistors based on the combination of an InGaZnO channel and a TaO_x gate dielectric," *Nanoscale*, 2022, 14, 10245. DOI:10.1039/d2nr02136f.

Prof. Chen supervised the whole project and revised and edited the manuscript.

I conceptualized the idea and formulated the research goals and aims, performed the device fabrication, data acquisition, and fitting simulation, and prepared the manuscript.

Dr. Ju helped conceptualize the idea and provided the pulse testing probe station.

Dr. Salim conducted the XPS experiment and performed the XPS analysis.

Chapter 6 is partially published as Y. Li=, J. Zhang=, J. Sun, and T. Chen, "A Large-Size HfO_2 Based RRAM Structure Suitable for Integration of One RRAM with One InGaZnO Thin Film Transistor for Large-Area Application," *ECS Journal of Solid State Science and Technology*, 2021, 10, 115004. DOI:10.1149/2162-8777/ac3ad1.

Prof. Chen supervised the whole project and revised and edited the manuscript.

As the co-first author, I conceptualized the idea, fabricated the device, collected the data, and prepared the manuscript together with Dr. Zhang.

Dr. Sun contributed to device fabrication and revised the manuscript.

03/01/2023
Date

LI YUANBO

This thesis is dedicated to my parents.

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Abstract

Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistor (TFT) is an emerging electronic device with many applications, such as active-matrix high-resolution display, wearable electronics, embedded memories, synaptic devices, sensors, etc. The broad spectrum of applications of the IGZO TFT is attributed to the TFT′s large carrier mobility, low leakage current, high transparency, good uniformity, low-temperature, low-complexity, and low-cost fabrication process, as well as the compatibility with various dielectric materials. Nevertheless, there still exist some challenges for IGZO TFT such as the limited driving current for ultrahigh definition display and poor reliability under external stress. In this thesis, the author was dedicated to improving the performance of the IGZO TFT through various techniques. Applications based on high-performance IGZO TFTs were explored and demonstrated as well.

IGZO TFTs were fabricated with the staggered bottom-gate structure thanks to its simple fabrication process. From the top to the bottom, novel source/drain contacts engineering, room-temperature passivation technology, and novel ion-conductive gate-dielectric adoption were applied on the transparent IGZO TFTs respectively for the improvements of IGZO TFT performance and realization of advanced applications. In the end, an 8×8 1T1R array was fabricated based on the integration of high-performance IGZO TFTs and HfO_2-based resistive memory (ReRAM), which is promising in applications for embedded memory technology.

Specifically, 1) by virtue of the good contact between Ti and IGZO, a transparent IGZO TFT with an ultrathin Ti layer as the source/drain contacts was demonstrated. The insertion of

a 10 nm Ti layer between ITO and IGZO successfully improved the carrier mobility of the TFT by three folds and reduced the contact resistance of the TFT by over three folds, with the optical transmittance of the whole device maintained at a high level. 2) a layer of 20 nm sputtered AlO_x was capping on the transparent IGZO TFT as a passivation layer, which aimed to provide protection to the IGZO layer from the penetration of ambient molecules. At the same time, the deposition of the AlO_x layer induced an interfacial In-rich layer at the AlO_x/IGZO interface, which increased the carrier concentration in the IGZO layer. As a result, the mobility of the TFT was largely improved from 6.292 cm^2/Vs to 69.01 cm^2/Vs. This tremendous enhancement of the carrier mobility increased the driving current of the IGZO TFT by one order as well. 3) by changing the dielectric material from Al_2O_3 to the ion-conductive TaO_x, a transparent synaptic IGZO TFT was achieved under stimulation of either electronic pulses or photoelectric pulses. Under various stimulations, behaviors of drain current of the TFT can well emulate the excitatory post-synaptic current, short-term memory plasticity, short-term memory transition to long-term memory, and long-term potentiation/depression. Particularly, long-term potentiation/depression with large G_{max}/G_{min} and small nonlinearity was achieved. 4) the high-performance IGZO TFTs were integrated with HfO_2-based ReRAM. The TFT with Ti/Au/Ti/Pt multi-stack source/drain contacts showed large driving current and good reliability under self-heating stress. On the other hand, the ReRAM with an ultrathin tunnelling layer inserted between the top electrode and the HfO_2 switching layer showed largely reduced device-to-device and cycle-to-cycle variations in memory parameters under a small compliance current (0.5 mA).

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List of Abbreviations

a-Si:H ····· hydrogenated amorphous silicon

AES ····· Auger electron spectroscopy

AFM ····· atomic force microcopy

ALD ····· atomic layer deposition

AMLCD ····· active-matrix liquid-crystal display

AMOLED ····· active-matrix organic light-emitting diode

AMQLED ····· active-matrix quantum dot light emitting diode

AR ····· augmented reality

BCE ····· back-channel-etch

BEOL ····· back end of line

BGTC ····· bottom-gate-top-contact

BLA ····· blue laser annealing

CB/CBM ····· conduction band/conduction band minimum

CBRAM ····· conductive-bridge memory

CMOS ····· complementary metal-oxide-semiconductor

CNL ····· charge neutral level

CPU ····· central processing unit

CTEF ····· charge-trapping-engineered flash

CTF ····· charge-trapping-flash

CTL ····· charge-trapping layer

DG ····· double-gate

DOS ····· density of states

DRAM ····· dynamic random access memory

ELA ····· excimer laser annealing

EPDs ····· electrophoretic displays

EPSC ····· excitatory postsynaptic current

ES ····· etch-stop

FeTFT ····· ferroelectric thin-film transistor

FIB ····· focused ion beam

FOM ····· figure of merits

FOV ····· field of view

FPDs ····· flat-panel displays

IGZO ····· Indium-Gallium-Zinc-Oxide

IoT ····· Internet of Things

IR ····· Infrared

LDA ····· local-density approximation

LLO ····· laser-lift-off

LTM ····· long-term memory

LTPS ····· low-temperature polycrystalline silicon

MOSFET ····· metal-oxide-semiconductor field-effect transistor

MTR ····· multiple trapping and release

NBIS ····· negative bias illumination stress

NBS ····· negative bias stress

NBTS····· negative bias temperature stress

NDD····· nano-dot-doping

NVM ····· non-volatile memory

OSCs ····· organic semiconductors

OTFT····· organic thin-film transistor

P/D····· potentiation/depression

PBIS ·····positive bias illumination stress

PBS ····· positive bias stress

PBTS ····· positive bias temperature stress

PCRAM ·····phase change memory

PEALD·····plasma-enhanced atomic layer deposition

PECVD ····· plasma-enhanced chemical vapor deposition

PI····· polyimide

PLD····· pulsed laser deposition

PPF ····· paired pulse facilitation

PVL····· passivation layer

PZT ····· lead zirconate titanate

QVGA····· quarter-video-graphics-array

ReRAM/RRAM····· resistive random access memory

RTA ····· rapid thermal annealing

SCS ····· semiconductor characterization system

S.S. ····· subthreshold swing/slope

S/D ····· source/drain

SG ····· single-gate

SIMS ····· secondary-ion mass spectrometry

SQM ····· symmetric quadrature method

STM ····· short-term memory

TCOs ····· transparent conductive oxides

TEM ····· transmission electron microscopy

TFT ····· Thin-film transistor

TLC ····· trap-limited conduction

TLM ····· transmission line method

UV ····· Ultra-violet

VB/VBM ····· valence band/valence band maximum

VR ····· virtual reality

VRH ····· variable-range hopping

VTFT ····· vertical thin-film transistor

WXGA ····· wide-extended-graphics-array

XPS ····· X-ray photoelectron spectroscopy

XRD ····· X-ray diffraction

Chapter 1. Introduction

This thesis mainly focuses on the study of thin-film transistors (TFTs) based on Indium-Gallium-Zinc Oxide (IGZO), including the optimization of performance for single device, realization of synaptic behaviors in transistors and application in one-transistor one- ReRAM array, etc. This chapter provides a brief introduction to the study of IGZO TFTs covering the background, motivation, research objectives and scope. The major contributions and organization of this thesis are also stated.

1.1 Background and Motivation

In the recent half-century, the mainstream display technology has evolved rapidly from cathode-ray tubes (CRTs) to flat-panel displays (FPDs), typically like liquid-crystal display (LCD) [1] and organic light-emitting diode (OLED) [2]. Driven by the pursuit of larger area, lighter and slimmer body, and better imaging quality for the display screen, active-matrix display panels undoubtfully become favorable compared to passive-matrix ones. In the active-matrix driving scheme, each pixel is integrated with a controlling field-effect transistor (FET) and a charge-storage capacitor, which could largely improve the refresh rate, reduce the power consumption, and avoid the crosstalk between pixels [3].

Since the first successful demonstration of amorphous silicon (a-Si) based TFT-LCD in 1973 [4], TFT, as a sort of FET, started to play an essential role in the active-matrix display technology. At the early stage, active-matrix LCD (AMLCD) mainly adopted hydrogenated amorphous silicon (a-Si:H) TFT as the driving transistor. However, the limited carrier

mobility (around 1 cm^2/Vs) [5] and driving current have made it insufficient to match the growing pixel density and physical area of the display panel. Another Si-based alternative is low-temperature polycrystalline silicon (LTPS) TFT, which shows high carrier mobility up to 100 cm^2/Vs [6]. Nevertheless, the complicated fabrication process, bad uniformity and high cost make it hard to be widely used in large-area electronic applications. Till 2004, Nomura demonstrated the transparent amorphous IGZO TFT, initiating the era of metal-oxide TFTs [7]. The IGZO thin film could be synthesized by room-temperature sputtering with high uniformity and large bandgap. In addition, the IGZO TFT could be fabricated with simple and low-cost processes, meanwhile showing high carrier mobility (10~20 cm^2/Vs) [8], small subthreshold swing (S.S.), large driving current and extremely low leakage current. These characteristics make the IGZO TFT a competitive candidate in the next-generation display technology, especially for the current-driving active-matrix OLED (AMOLED) [9].

Besides the traditional display technology, other advanced applications based on IGZO TFTs are also realized. For instance, 1). the wide bandgap (~ 3.2 eV) gives the IGZO layer high optical transmittance, leading to the development of transparent displays [10]; 2). the sputtering deposited IGZO layer always shows good uniformity and high strain resistance, making the IGZO TFT suitable for flexible electronics [11]; 3). ultrahigh-resolution virtual reality (VR)/ augmented reality (AR) [12] has also been achieved based on IGZO TFTs with large driving current and carrier mobility; 4). neuromorphic synapses [13] could be emulated with the IGZO TFT through special device structure or dielectric material engineering; 5). three-terminal non-volatile memory devices are emerging [14] by applying the charge trapping

layer, floating-gate structure or ferroelectric layer in the transistor; 6). fabrication of IGZO TFT is compatible with the complementary metal-oxide-semiconductor (CMOS) process at low temperature, which makes it possible to integrate the TFT with memory, composing an active-matrix memory in the back end of line (BEOL) [15].

Still, there exist some challenges and research gap for current IGZO TFT technology. 1). Transparent IGZO TFT employing transparent conductive oxides always show limited mobility and driving current due to the non-ideal source/drain contacts. 2). Driving current of the state-of-art IGZO TFT is limited at around 1 mA with high driving voltage, which could cause high power consumption. 3). As mentioned in the former paragraph, there are various advanced applications based on IGZO TFTs to be further explored and realized. Accordingly, this thesis is devoted to further improving IGZO TFT performance and applying the high-performance IGZO TFT in various areas.

1.2 Objectives and Scope

IGZO TFT has shown promising prospects in various applications. Nevertheless, there still exists space for electrical performance improvement. This thesis will mainly target at optimizing performance of the IGZO TFT and realizing various advanced IGZO TFT-based applications like neuromorphic artificial synapse, one-transistor one-resistive memory (1T1R) array, etc. In detail, the objectives and scope are listed below:

1). Bottom-gate-top-contact (BGTC) IGZO TFTs will be fabricated with vacuum-based techniques, including atomic layer deposition (ALD), RF magnetron sputtering, electron-

beam evaporation, and plasma-enhanced chemical vapor deposition (PECVD), etc.

2). Drain current (I_D) vs. gate voltage (V_{GS}) transfer curves and drain current (I_D) vs. drain voltage (V_{DS}) output curves will be measured to extract the device parameters of IGZO TFTs with various ratios of channel width to length (W/L).

3). Different external stress schemes (e.g., positive bias illumination stress (PBIS), negative bias illumination stress (NBIS), etc.) will be applied to assess the reliability and instability of the TFT.

4). Different source/drain (S/D) materials will be adopted in the IGZO TFT structure to investigate how the bulk of electrodes and contact characteristics influence the device performance.

5). TFT structure modifications will be explored to improve the IGZO TFT performance, such as S/D engineering, passivation technology, etc.

6). Nano-ionic dielectric layer will be used in the IGZO TFT structure to realize the three-terminal artificial synaptic device.

7). HfO_2-based resistive random-access memory (ReRAM) with the insertion of tunnelling layer will be investigated to optimize the performance, variation, and endurance of the memory operations.

8). The IGZO TFT will be integrated with the ReRAM to form one transistor one ReRAM (1T1R) array, which is promising for applications in Internet of Things (IoT) and embedded memory.

1.3 Major contribution of the thesis

The major contributions of this thesis are as follows:

1. IGZO TFTs were fabricated with different sorts of S/D electrodes (Ti, Al, Cu, Ti/Au). The transfer and output characteristics were measured to study how the S/D electrodes affected the performance and reliability of the TFT. Particularly, transmission line method (TLM) was applied to evaluate the contact characteristics of the TFTs. Meanwhile, various external stress schemes (PBIS, NBIS, PBTS, NBTS, etc.) were applied to the TFT. The changes in the transfer characteristics of the devices after various stresses were measured and analyzed. The origins of instabilities from different stress scenarios were systematically studied and summarized. Eventually, ITO/ultrathin-Ti S/D structure was adopted in the transparent IGZO TFT. The performance of the TFT was successfully improved to a certain extent in terms of contact characteristics, field-effect mobility (μ_{FE}), driving current, etc.

2. Transparent IGZO TFTs passivated by sputtering deposited AlO_x were fabricated. Passivation technology has been widely used to improve the TFT reliability. In this work, the amorphous AlO_x passivation layer enormously improved the μ_{FE} and driving current of the TFT. To study the mechanism of the remarkable performance improvement, TEM, XPS, AES, and XRD were carried out to characterize the thin film structure, elements (In, Al, O) depth profiling, and AlO_x crystalline status. It turned out that the sputtering process could induce an interfacial layer between the passivation and channel layer. This interfacial layer was abundant in metallic Indium, increasing the carrier concentration in the channel layer. For reliability, the passivated TFT, which was stored in the ambient environment for a long period

(e.g., 6 months), showed nearly no performance degradation. Besides, the passivated TFT showed better reliability under PBIS compared with the TFT without the passivation.

3. A transparent synaptic IGZO TFT was fabricated with a high dielectric constant (κ) gate insulator layer TaO_x. TaO_x is known as a kind of ion conducive but electron insulating oxide, which is extensively used as a switching layer in ReRAMs. In this work, TaO_x layer provided ion movement when an electrical signal was applied to the gate terminal. A large and stable anti-clockwise hysteresis window existed under the forward and backward DC gate voltage sweep. When electrical pulses were applied to the gate terminal, the drain current I_D, which represented the excitatory postsynaptic current (EPSC), showed good short-term memory (STM) plasticity and potentiation/depression (P/D). On the other hand, the IGZO layer is sensitive to light illumination. UV, and visible light (referring to blue, green, and red lights) pulses were shone to the TFT, respectively. The synaptic behaviors mentioned previously were also observed. Thus, a transparent synaptic transistor was demonstrated under either electronic or photoelectric pulses stimulation.

4. An 8×8 1T1R array was designed and fabricated in this work. The '1T' refers to one IGZO TFT, and the '1R' refers to one HfO_2-based ReRAM. To provide large driving current for the memory operations in ReRAM, a multi-stack S/D contacts with Ti/Au/Ti/Pt were employed in the IGZO TFT. The TFT showed large saturation mobility (μ_{sat}) and driving current, as well as good reliability under collective stress of large gate voltage (V_{GS}) and drain voltage (V_{DS}). To optimize the HfO_2-based ReRAM performance and reliability, an ultrathin tunnelling layer of Al_2O_3 was inserted between the top electrode and switching layer

(i.e., 6 nm HfO_2). The ReRAM with Pt/6 nm HfO_2/2 nm Al_2O_3/6 nm Ti/TiN structure showed better device-to-device and cycle-to-cycle variations under a small compliance current (0.5 mA). Ultimately, the 8×8 1T1R array based on the above IGZO TFTs and HfO_2-based ReRAMs was fabricated and demonstrated successfully.

1.4 Organization of the thesis

This thesis consists of 7 chapters, and is organized as follows:

Chapter 1 introduces the background of display technology development, superiority of the IGZO TFT among three main TFT technologies, advanced applications of the IGZO TFT, and objectives, contributions, and organization of this Ph.D. thesis.

Chapter 2 presents a literature review on IGZO TFT, including the fundamental physics of the device, methods to improve the device performance and reliability, and advanced applications.

Chapter 3 investigates the influence of S/D contacts (Ti, Al, Cu, Ti/Au) on the IGZO TFT performance and reliability. The Ti layer is found to form the best contact with the IGZO layer. Thus, ITO/ultrathin Ti S/D structure is adopted to improve the performance of the transparent IGZO TFT.

Chapter 4 presents a study of passivation effect on the performance and reliability of the IGZO TFT. A 20 nm amorphous AlO_x passivation layer is deposited by RF magnetron sputtering. The passivated TFT shows remarkable performance enhancement and improved reliability under PBIS. To understand the performance improvement mechanism, the

structural and chemical properties of the material system of the device are characterized with various analysis techniques including TEM, XPS, AES, and XRD.

Chapter 5 reports a transparent synaptic transistor based on IGZO channel layer and high-κ TaO_x gate dielectric. Either electric pulses applied to the gate terminal or light pulses shone on the IGZO are able to excite the synaptic behaviors.

Chapter 6 systematically studies the 1T1R structure formed by one IGZO TFT and one HfO_2-based ReRAM. The ReRAMs with and without a tunnelling layer (2 nm Al_2O_3) are fabricated. The ReRAM with 2 nm Al_2O_3 tunnelling layer between the switching layer and top electrode is chosen to integrate with the IGZO TFT with Ti/Au/Ti/Pt S/D contacts, A 64-bit 1T1R array based on such TFT and ReRAM structures is fabricated.

Chapter 7 concludes and summarizes all the works done in this thesis. Also, continuous, and promising future works are recommended.

Chapter 2. Literature Review

IGZO TFT has attracted much attention in both research and industry areas. In this chapter, the author mainly shows a systematic review of literatures from the following aspects: 1) background of different TFT technologies, 2) the basic physics of IGZO TFT (i.e., device structure, figure of merits, device model), 3) methods to enhance the performance of IGZO TFT, and 4) advanced applications of IGZO TFT.

2.1 Background of different TFT technologies

Since the first TFT based on CdS was successfully demonstrated in 1960 by P.K. Weimer [16], TFTs with different semiconductor channel materials have been investigated enormously in recent decades. Fig. 2. 1 shows the roadmap of the TFT technology development. [17] There are four kinds of semiconductor materials being widely used as the channel layer of the TFT: 1) hydrogenated amorphous silicon (a-Si:H) TFT, which was first demonstrated in 1979 by P. Le Comber, W. Spear, and A. Ghaith [4] ; 2) low temperature poly-crystalline silicon (LTPS) TFT, which started to boom since S. Depp succeeded in producing the first working device in 1980 [18]; 3) organic TFT, which was first reported with polythiophene channel layer by A. Tsumura in 1986 [19]; 4) metal-oxide TFT, which was first demonstrated with p-type SnO_2 channel layer by Klasens in 1964 [20]. The first crystalline GIZO TFT fabricated on the YSZ(111) substrate was reported in 2003 by Hosono team [44]. The basic working principles, and the merits and shortcomings of each sort of TFT are discussed in the following.

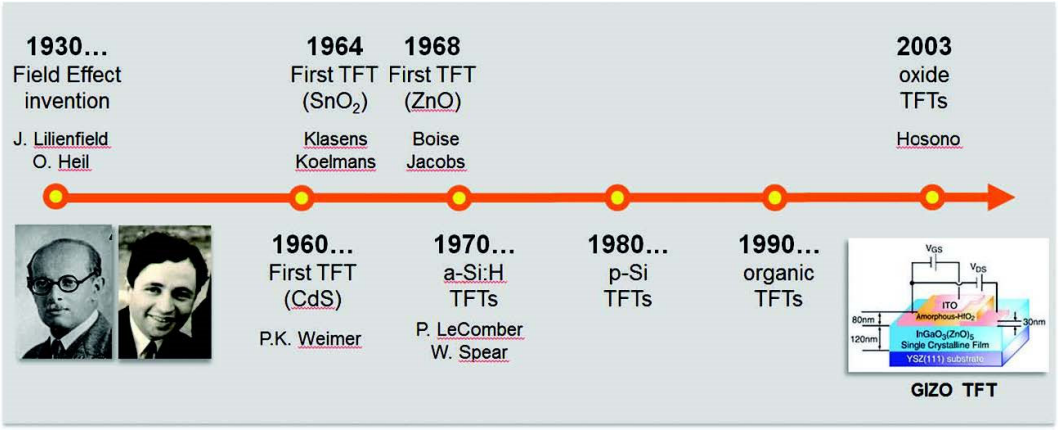


Fig. 2. 1 TFT technology development roadmap. [17]

2.1.1 Hydrogenated amorphous silicon (a-Si:H) TFT

Driven by the rapid development of thin-film transistor and solar cell technology, amorphous silicon (a-Si) started to take a place in microelectronics. Silicon is a purely covalent semiconductor with all identical covalent bonds and equally shared electrons. In other words, all the chemical bonds are derived from *p* or sp^3 orbitals, which always exhibit

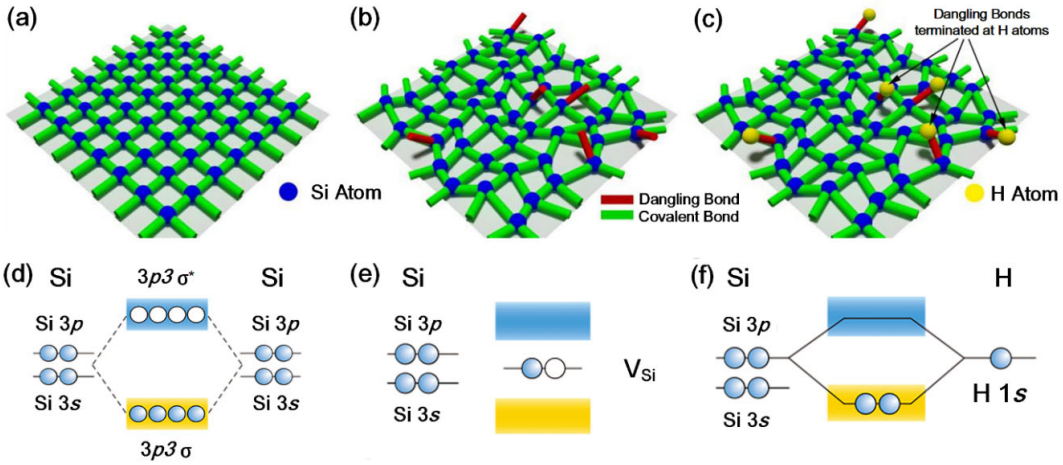


Fig. 2. 2 2D illustration of bonding structures in (a) crystalline silicon (c-Si), (b) amorphous silicon (a-Si), (c) hydrogenated amorphous silicon (a-Si:H). [21] Electronic structures for (d) illustration of band gap formation in covalent silicon, (e) defects in a-Si, (f) defects in a-Si:H. [22]

high spatial directivity. As shown in Fig. 2. 2(a)-(c), crystalline silicon (c-Si) presents regular and perfectly symmetrical Si-Si bonds, whereas a-Si (either undoped or hydrogenated) shows Si-Si bonds with spreading bonding energy.

In a-Si, as shown in Fig. 2. 2(d), the anti-bonding states and bonding states of the sp^3 hybrid orbitals are split, forming the energy band gap (E_g). The anti-bonding states are located at the bottom of the conduction band (CB), and the bonding states are located at the top of the valence band (VB). [22] These electronic states located at the two mobility edges show the weakest Si-Si bonding energy. They are localized states which induce band tails reaching into the E_g. Besides, as shown in Fig. 2. 2(b), dangling bonds could be produced in the middle of the E_g when there is silicon vacancy. A dangling bond is an unpaired electron, which could be negatively charged once trapping an electron, or positively charged once trapping a hole (Fig. 2. 2(e)). Consequently, dangling bonds are regarded as defect states which are unfavourable in a-Si. [5],[22]

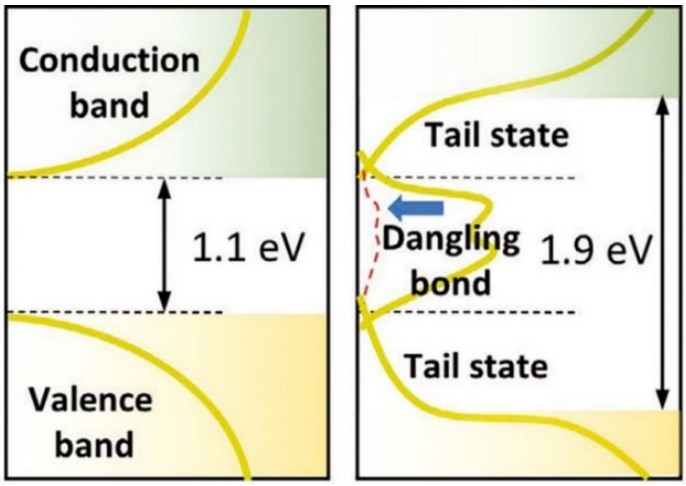


Fig. 2. 3 Density of states (DOS) distribution of c-Si (left) and a-Si:H (right). [23]

According to different electronic states distribution, the density of states (DOS) of c-Si and a-Si are shown in Fig. 2. 3. For c-Si, electronic states are extended along the whole solid. In contrast, for a-Si, electronic states are extended beyond the E_g, whereas within the E_g, only localized states, and defect states produced by dangling bonds exist. [5] It is widely advocated that the hopping of electrons between the localized states is the main origin of conductivity in a-Si at room temperature. At the same time, the electronic transport could be obstructed by defect states. [5],[23],[24]

Now that the density of defect states is critical to the electronic transport in a-Si, it is necessary to passivate the dangling bonds. In undoped a-Si, there would happen conversion between strained Si-Si bonds and dangling bonds under external stress like illumination or electrical bias. [25],[26] When the a-Si is at equilibrium (i.e., no external stress), the density of dangling bond states is around 10^{20} cm^{-3}, which is excessively high to pin the Fermi level of a-Si and prevent the electrons transport. [5] As shown in Fig. 2. 2(c) and (f), to reduce the density of defect states to a reasonable level, hydrogen is injected into a-Si as a dopant. Those unpaired electron states could be bonded with the doping hydrogen. Thus, the density of defect states in the a-Si:H reaches a lower level at around 10^{16} cm^{-3}. [5],[22]

The a-Si:H layer was deposited by RF glow discharge at the early stage [4]. While with the development of thin film deposition technology, PECVD became the dominating technique. The deposition is carried out at a relatively low temperature ($\leq 300℃$). Likewise, the deposited a-Si:H is free of crystalline boundary, showing high uniformity. These fabrication process superiorities have made a-Si:H TFT popular in large-area display

technology for periods.

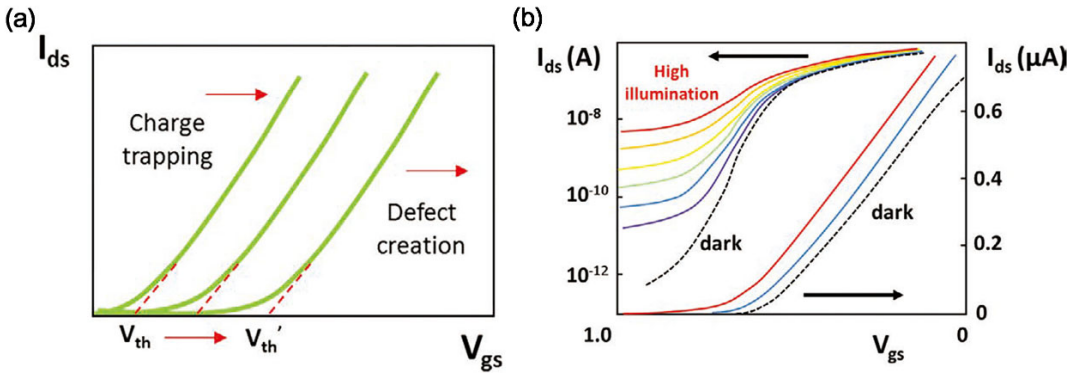


Fig. 2. 4 (a) V_{th} shift under electrical bias for a-Si:H TFT, (b) Instability of a-Si:H TFT under light illumination. [23]

Still, there are some intrinsic drawbacks of a-Si:H TFT, which makes it gradually inferior compared to other emerging TFT technologies. One of the biggest concerns is the limited carrier mobility in a-Si:H TFT. With the band-tail states from the strained Si-Si bonds and defect states from the dangling bonds in the a-Si:H channel layer, the field-effect mobility (μ_{FE}) of the transistor could only reach 1 cm^2/Vs [22], which seriously limits the driving capability of the a-Si:H TFT.

Another issue is the instability under electrical and illumination stress. Under the electrical bias, the threshold voltage (V_{th}) shift is the most noteworthy instability. The bias applied to the TFT gate induces charge trapping and creates dangling bonds in the E_g. As shown in Fig. 2. 4(a), these two mechanisms both contribute to the shift of V_{th}. [27] On the other hand, in active-matrix display panels, the scattered light would inevitably shine at the a-Si:H layer. This could excite the band tails to produce more carriers and increase of the off current (Fig. 2. 4(b)). [28]

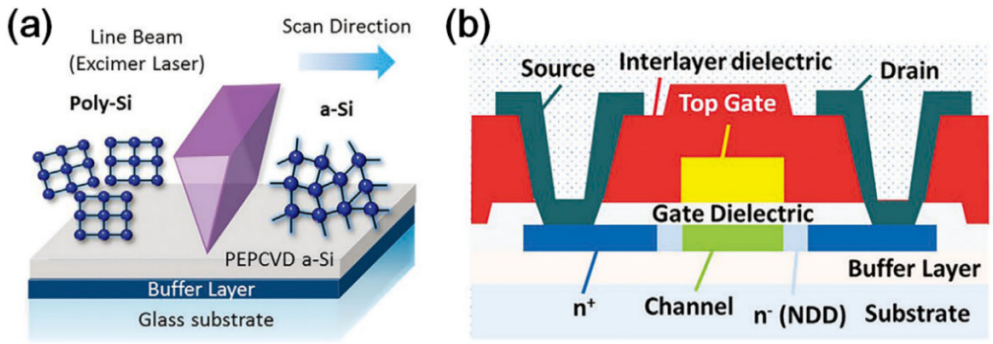


Fig. 2. 5 (a) Crystallization process from a-Si to poly-Si under ELA, (b) Schematic of the cross section of a typical top-gate n-type LTPS TFT. [23]

2.1.2 Low temperature poly-crystalline silicon (LTPS) TFT

As the current-driving OLED emerges rapidly in the display industry, the TFT with higher mobility and better reliability is in high demand. TFTs with the c-Si-based channel layer began to draw attention. Traditionally, crystallization of the a-Si needs strong laser irradiation or large thermal energy (~1000 ℃). The extremely high temperature of the crystallization process limits the choice of substrate for TFTs tightly. [29] Accordingly, a lower temperature crystallization process combined with laser irradiation is introduced – excimer laser annealing (ELA). Fig. 2. 5(a) shows the process of the crystallization from a-Si to poly-crystalline silicon (poly-Si) under ELA [23]. The top-gate is the most appropriate structure for the LTPS TFT, as shown in Fig. 2. 5(b). In the TFT, a buffer layer (silicon oxides or nitrides) is grown on the substrate to prevent the diffusion of impurities from the substrate to the channel layer, and the diffusion of heat from ELA to the substrate.

Typically, LTPS TFTs own carrier mobility at around 100 cm^2/Vs, which is much higher than other TFT technologies. Another significant superiority of the LTPS TFT is its

compatibility with the complementary metal-oxide-semiconductor (CMOS) technology. By different doping schemes, both n-type and p-type LTPS TFTs can be implemented.

Display panels based on LTPS TFTs are usually small in size. It originates from the eigen flaws of poly-Si. On the one hand, the laser beam size used for crystallization is limited to around 600 mm^2. On the other hand, grain boundaries would form plenty of small crystallites in the poly-Si film with various grain sizes. [23] These two factors would induce serious non-uniformity issue if the LTPS TFT is applied in large-area display panels. In addition, the relatively higher temperature, complexity and cost of the fabrication process are to be solved for further mass production.

2.1.3 Organic TFT

Organic TFT (OTFT) is named after the organic semiconductor (OSC) channel layer and solution-based polymer dielectrics. For channel layer, OSCs could be classified into two categories – polymers and small molecules. Most of the OSCs are p-type, which could be attributed to two main reasons. [30] Firstly, the large E_g of OSCs induces high injection barriers for electrons. Likewise, electrons are more inclined to be trapped in the dielectric.

Polymers with conjugated structures emerged earlier as OSCs. The conjugation delocalizes one of the four electrons in each carbon atom, forming the molecular conjugated system which is the basis of the charge transport. [31] As usual, the channel layer of OTFTs contains lots of polymer molecules which are bonded by weak van der Waals interactions. Thus, the electronic states are not extended over the whole bulk but localized to some of the

molecules. Charge trapping in the localized states is viewed as the main limitation of the carrier transport from one organic molecule to another. Primitive typical polymeric OSCs like poly (3-hexylthiophene-2,5-diyl) (P3HT) with high regioregularity [32], polytriarylamines (PTAA) [33], poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (PBTTT) [34], etc. show low carrier mobility (< 1 cm^2/Vs). Then, donor-acceptor (D-A) copolymers was developed, breaking through the 1 cm^2/Vs bottleneck of the mobility. Typically, indacenodithiophene-benzothiadiazole (IDT-BT) exhibits disorder-free charge transport in the entire molecular volume. [35],[36] To be specific, all the molecular sites in IDT-BT are thermally approachable. Consequently, the carrier is no longer transported between limited localized states.

Small molecules are another type of OSCs, which show higher mobility than polymer-based OSCs. Some representative materials like triisopropyl-silylethynyl pentacene (TIPS-pentacene) [37], benzothieno[3,2-b] [30], the relevant derivatives (Cn-BTBT) [38], etc. all show remarkable mobility enhancement. The ‘band-like’ charge transport in the small molecule OSCs is always in debate. Whereas, in [39], T. Sakanoue and H. Sirringhaus discussed the band-like and temperature-dependent carrier mobility systematically. They conclude that carrier transport differs at different lateral electric fields. With small fields, carriers are localized in individual small molecules at low temperature. With moderate fields, those trapped carriers are released, causing nonlinear charge transport. With high fields, the charge transport shows negative temperature dependence. The authors attribute this phenomenon to localized transport which is limited by the fluctuations of the thermal lattice.

For those crystalline small-molecule OSCs, the mobility could be even higher (~100 cm^2/Vs) since the charge transport happens in the extended states. Nevertheless, the ambient impurities or external strains could become mortal defects to affect the charge transport and deteriorate the whole device performance. One popular solution is to blend the small-molecule OSCs with either high-k or low-k polymeric binders. [40],[41] The binders could induce better control of the crystallization process, guaranteeing high carrier mobility and good uniformity at the same time.

As can be seen, OTFTs have high potential to be applied in flexible and wearable electronics thanks to the simple and low-cost fabrication processes. However, it is still a challenge to achieve the high performance and good reliability of the OTFT at the same time. In addition, the difficulty to control the uniformity of OSCs has obstructed the OTFTs to be applied in large area electronics.

2.1.4 Metal-oxide TFT

Since R. L. Hoffman reported the ZnO-based TFTs in 2003 [42], the post transitional metal-oxide based TFT showing high mobility started to emerge. In addition, H. Hosono team came up with the hypothesis of the high mobility of amorphous semiconductor oxides with wide E_g in 1996 [43]. Then his team reported high-performance TFTs based on either crystalline IGZO (c-IGZO) in 2003 [44] or amorphous IGZO (a-IGZO) in 2004 [7]. The IGZO layers were both grown by pulsed laser deposition (PLD). Then, the amorphous IGZO TFT with high mobility was successfully fabricated by RF magnetron sputtering by his team in

2006. [8] From then on, IGZO TFT, as a rising star, has been continuously playing a predominant role in display and other advanced applications. This section will take the IGZO as a representative of metal oxide.

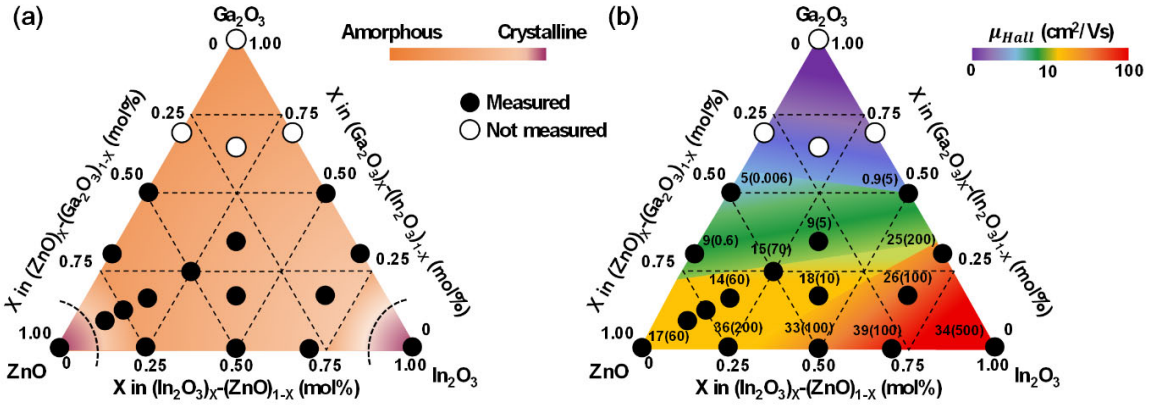


Fig. 2. 6 (a) Amorphous or crystalline status with different proportions of In_2O_3, ZnO, and Ga_2O_3. (b) Charge transport properties with different proportions of In_2O_3, ZnO, and Ga_2O_3. Values inside the triangle are the hall mobility (μ_{Hall}) and carrier density ($\times 10^{18}$ cm^{-3}) which is shown in parentheses. [22]

IGZO is composed of oxygen and three kinds of heavy metals – Indium, Gallium, and Zinc. The outstanding characteristics of the IGZO thin film are originated from the co-effects of the three metal ions. Fig. 2. 6 depicts the distribution of amorphous (or crystalline) states and carrier transport properties (including mobility and concentration) of IGZO with different compositions of In_2O_3, ZnO and Ga_2O_3. [22] The pure ZnO and In_2O_3 both demonstrate crystalline states even at room temperature (Fig. 2. 6(a)). Meanwhile, the hall mobility of ZnO and In_2O_3 is as high as 17, and 34 cm^2/Vs, respectively (Fig. 2. 6(b)). The origin of the high mobility of these two oxides is the small effective electron mass (m_e^*). Both In_2O_3 and ZnO show m_e^* in the range of 0.25~0.35 m_e, where m_e denotes the rest mass of the electron.

[45] Furthermore, the high dispersion of conduction band minimum (CBM) has contributed to the small m_e^* of these two oxides. The detailed mechanisms are different in ZnO and In_2O_3 as proposed by H. Hosono in [46]. In ZnO, the dispersion of the CBM is enhanced by the small distance of Zn-Zn, which is attributed to the fourfold coordination. While in In_2O_3, the CBM is formed by the *ns* orbitals provided by In. The n in '*ns*' denotes the principal quantum number, i.e., the principal electron shell. When n is larger than 4, the highly dispersed CBM is formed. Accordingly, researchers have tried to combine ZnO and In_2O_3, deriving IZO thin film.

The IZO thin film exhibits high mobility but terrible controllability due to the excessively high electron concentration. To control the carrier concentration at a reasonable level (~ 10^{17} cm^{-3}), it is necessary to incorporate a stabilizer, i.e., a strong metal-oxide bond, in IZO. Gallium is the most extensively adopted stabilizer since it has a stable and strong bond with oxygen. Correspondingly, the mobility of the pure Ga_2O_3 is extremely low (Fig. 2. 6(b)). [47],[48]

With the incorporation of Ga, H. Hosono team depicted the structure of the a-IGZO based on relaxation calculation, which was carried out at local-density approximation (LDA) level. [49] The ZnO_4, GaO_6, GaO_5, InO_6, InO_5 marked in Fig. 2. 7(a) refer to the specific polyhedral structures. In addition, a supercell pseudo band calculation was performed based on the LDA-relaxed structure of IGZO. They found that the CBM of IGZO is made up of the In *5s* orbitals. The CBM is shown in Fig. 2. 7(b) in the form of the iso-surface of $|\psi|^2$ map (i.e., the wave function).

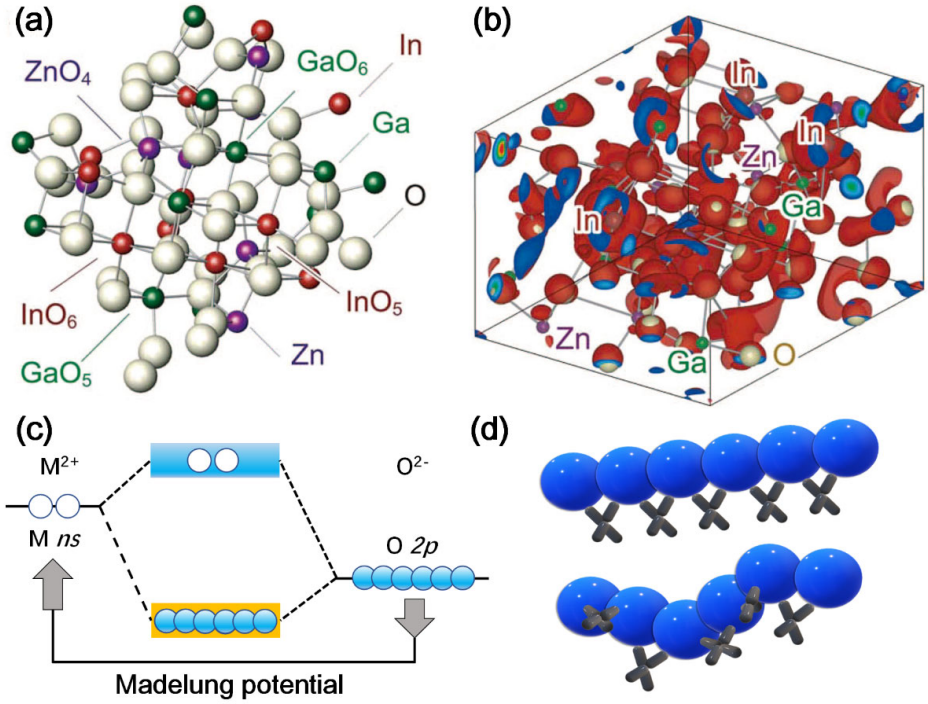


Fig. 2. 7 (a) The structure of IGZO based on relaxation calculation at LDA level. [49] (b) The LDA-relaxed structure of IGZO in combination with demonstration of the iso-surfaces of CBM wave function. [49] (c) Illustration of band gap formation in the ionic IGZO. [22] (d) Carrier transport path in crystalline IGZO (upper) and amorphous IGZO (below). [22]

As mentioned previously, the formation of the CBM and the valence band maximum (VBM) of IGZO is different from that of covalent Si. With the strong ionicity, there always exists charge transfer between the metal atoms and the O atom, which forms Madelung potential. Driven by the potential, the *ns* orbitals of the heavy metals form the CBM and the *2p* orbitals of O form the VBM (Fig. 2. 7(c)). In addition, the *ns* orbitals are large and spherically extended. As shown in Fig. 2. 7(d), each *s* orbital overlaps with its neighbour. There is little difference in the arrangement between the in-order and out-of-order orbitals. Consequently, the mobility of IGZO does not deteriorate much from crystalline status to amorphous status. [22]

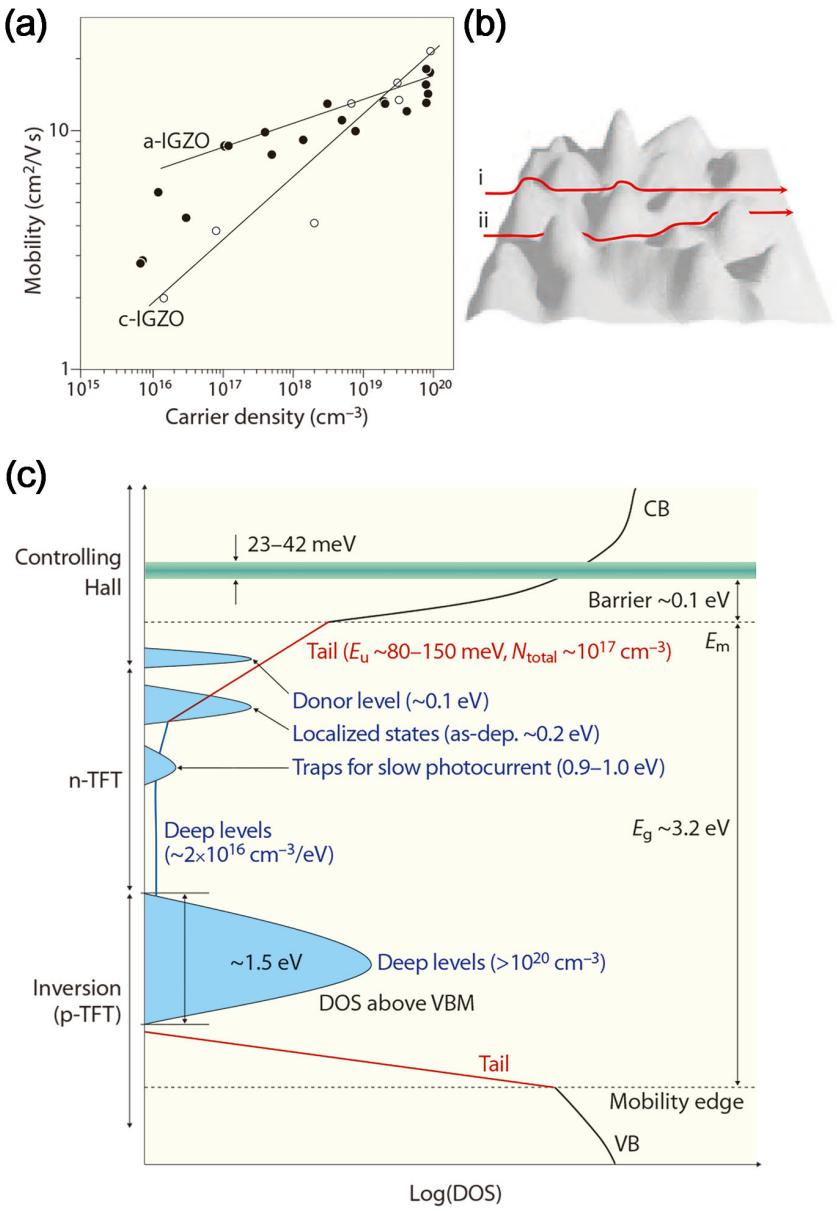


Fig. 2. 8 (a) Relationship of carrier mobility vs carrier density in IGZO. [22] (b) Schematic showing potential heights above CBM in IGZO. Path i and Path ii are the shorter and longer path, respectively. [22] (c) Electronic structure of IGZO showing the states distribution along the whole band gap of IGZO. [22]

From the Hall effect measurement, the carrier transport of the IGZO layer shows several different points compared with the covalent Si. 1). In a-Si, the sign of Hall voltage and Seebeck coefficient is an anomaly. In other words, n-doped a-Si shows the p-type Hall effect

and p-doped a-Si shows the n-type Hall effect. [50],[51] In contrast, the Hall voltage of the amorphous oxide semiconductors is definite, which could be attributed to the large mean free paths (0.5 ~ 1 nm) of the electrons in the CB. [52] 2). As shown in Fig. 2. 8(a), the Hall mobility increases with the carrier concentration in either c-IGZO or a-IGZO, which is opposite to that in Si. The most widely adopted explanation for this positive correlation is the percolation model. [52] It could well explain the temperature dependence of the concentration and conductivity of carriers and correct the deviation in the conventional Arrhenius model. In this model, as the obstacles of the carrier transport, potential barriers are assumed to exist above CBM with an energy distribution in the Gaussian function. [22] At room temperature, carriers tend to transport in a longer path with lower potential heights (Fig. 2. 8(b)). [22] The Hall mobility of the carrier could be estimated by using Equation (2.1), where μ_{Hall} and μ_0 are the Hall mobility and intrinsic mobility of the carriers, respectively, and Φ_0 is the potential height. μ_0 is called intrinsic mobility since it refers to the mobility of carriers in the well formed by potential barriers. μ_0 could be estimated by using Equation (2.2), where τ_{CB} is the relaxation time of carriers moving in the well region. [52] With the increase of carrier density, τ_{CB} will get longer and Φ_0 will become lower, which contributes to the increase of the carrier mobility.

$$\mu_{Hall} = \mu_0 \exp\left(-\frac{\Phi_0}{kT}\right) \tag{2.1}$$

$$\mu_0 = \frac{q\tau_{CB}}{m_e^*} \tag{2.2}$$

IGZO TFTs possess high μ_{FE} (~10 cm^2/Vs), low operation voltage with small subthreshold swing (S.S.), low leakage current, simple device structure and process, high

uniformity, and low process temperature. These advantages are attributed to the electronic structure as shown in Fig. 2. 8(c). Firstly, the large E_g (~ 3.2 eV) makes the IGZO TFT widely applied in the transparent display. Then, the green stripe above the CBM represents the potential barriers mentioned in the above content. Near the mobility edge in the n-type region, there lie localized states with much lower density compared with that in Si. [53] The low S.S. and operation voltage both originate from the low density of localized states. At the inversion (i.e., p-type) region, deep states with high density (> 10^{20} cm^{-3}) are formed near and above the VBM. These deep levels impede the mobilization of holes and formation of the inversion layer, which guarantees a low leakage current. Also, a large variety of metal oxides are appropriate to be adopted as the dielectric layer of the TFT thanks to the unipolarity of the IGZO layer.

There are still some challenges for IGZO TFTs to be solved. 1). Reliability issue is inevitable due to the charge trapping problems, hot carrier effects, and the sensitivity of the IGZO layer to high temperature and light illumination. This will be introduced in detail in **section 3.3**. 2). The carrier mobility and driving current of the IGZO TFT are needed to be improved for more advanced applications. 3). P-type IGZO TFT is unable to be realized, which makes it hard to apply IGZO TFTs in CMOS-compatible circuits.

2.1.5 Comparison of the main TFT technologies

Table 2.1 compares the four main TFT technologies (a-Si:H, LTPS, organic, and IGZO) from device performance, fabrication process, cost, applications, etc. There always exists

amounts of trade-offs to evaluate different TFT technologies. While the state-of-art IGZO TFT accommodates more advantages over other technologies in terms of the next-generation (either transparent or flexible), high-resolution, and large-area display technology, and other

Table 2. 1 Comparison of different TFT technologies [54],[55]

	a-Si:H TFT	**LTPS TFT**	**Organic TFT**	**IGZO TFT**
Channel material	Amorphous Si	Polycrystalline Si	Polymer/Small molecules	Amorphous IGZO
Mobility	~1 cm^2/Vs	~100 cm^2/Vs	0.1~1/~100 cm^2/Vs	10~40 cm^2/Vs
Uniformity	Good	Poor	Poor	Good
Leakage current	Low	High	High	Low
Process temperature	~300 ℃	>400 ℃	Room temperature	~300 ℃
Stability	Poor	Good	Poor	Medium
Cost	Low	High	Low	Low
TFT type	N-type	N/P-type	N/P-type	N-type
Applications	AMLCD	AMOLED, AMQLED	E-paper, Flexible ICs	AMOLED, Transparent display, Sensors, Memory

emerging CMOS-compatible devices (synaptic devices, non-volatile memory (NVM), dynamic random-access memory (DRAM), and photodetectors, etc.).

2.2 Basic physics of IGZO TFT

This section mainly reviews the device physics of the IGZO TFT from the device structure, figure of merits (FOM), and compact models.

2.2.1 Device structure of IGZO TFT

TFT is a sort of field-effect transistor with three terminals, in which gate electrode and channel layer are separated by a layer of dielectric. In contrast to the conventional metal-oxide-semiconductor field-effect transistor (MOSFET), the TFT is made up of layers of thin films, including gate electrode, dielectric layer, channel layer, S/D electrodes, and passivation layer (optional). The conduction of IGZO TFT is achieved by the formation of an accumulation layer at the interface of the channel layer (IGZO) and the dielectric layer. As shown in Fig. 2. 9, there are four kinds of fundamental structures of TFT: staggered bottom gate (bottom gate top contact), coplanar bottom gate (bottom gate bottom contact), staggered top gate (top gate bottom contact), and coplanar top gate (top gate top contact). [17] The staggered or coplanar structure is defined by the relative position of the gate electrode and S/D electrodes. When the gate electrode and S/D electrodes lie on the opposite sides regarding the IGZO channel layer, the TFT structure is staggered. Conversely, the TFT structure is coplanar.

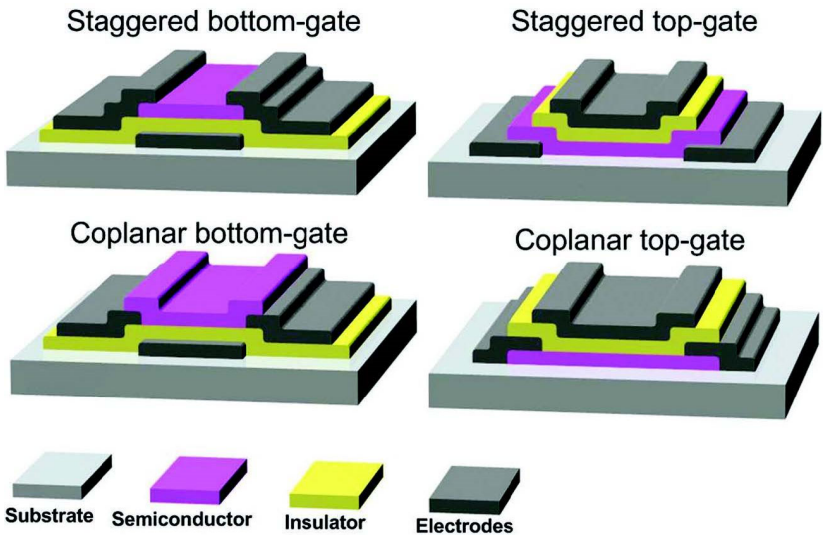


Fig. 2. 9 Schematic of the cross section of the TFT with four kinds of fundamental structures. [17]

Bottom-gate TFT: 1). For the staggered structure, the sequence of the layer deposition is gate electrode, dielectric layer, channel layer, and S/D electrodes. 2). For the coplanar structure, the sequence of the layer deposition is gate electrode, dielectric layer, S/D electrodes, and channel layer.

Top-gate TFT: 1). For the staggered structure, the sequence of the layer deposition is S/D electrodes, channel layer, dielectric layer, and gate electrode. 2). For the coplanar structure, the sequence of the layer deposition is channel layer, S/D electrodes, dielectric layer, and gate electrode.

The main advantage of the bottom-gate TFT is the simple fabrication process, which requires fewer lithography steps (1 or 2 steps) compared with the top-gate TFT. With 1 or 2 lithography steps, the TFT is fabricated with patterned S/D electrodes, common or patterned channel layer and common gate electrode. This is the simplest structure, but it always suffers from parasitic capacitance problem. [56] Likewise, a special method, grey-tone mask, is

adopted with 2 lithography steps to pattern gate electrode, channel layer and S/D electrodes. [57] Another appealing point of the bottom-gate TFT is the channel layer is free of the influence from the deposition of the dielectric layer thanks to the stacking order. In the top-gate TFT, the dielectric layer is grown on the IGZO layer. PECVD and ALD are the most common deposition methods of the dielectric layer, which could induce high temperature and hydrogen diffusion, affecting the characteristics of the IGZO layer. [58] Researchers prefer to adopt the bottom-gate structure for the study of IGZO TFTs in the laboratory. On the one hand, the fabrication process requirement is friendly with that of the research lab; on the other hand, the back surface of the IGZO layer is exposed to the air, which makes it convenient to study the factors affecting the characteristics of the IGZO layer and tune the performance of the TFT with a more focused target.

There are some literatures studying the limitation of these fundamental structure thoroughly. In [59], J. Jang team reported the edge effects which exist in the TFT with the staggered bottom-gate structure. The edge effects originate from the topology design of the TFT, with which the effective channel width is underestimated, and the μ_{FE} is overestimated. In [60], S. Oh compared the reliability of the TFT with bottom-gate and top-gate structure, respectively. The top-gate TFT suffers a larger V_{th} shift under PBTS, which is attributed to the higher density of tail states induced by the deposition of the top dielectric layer SiO_2. The bottom-gate TFT shows a larger V_{th} shift under NBTS, which results from the trapping of the oxygen vacancies accumulating at the interface between the IGZO layer and the bottom dielectric layer. The reliability issue of the TFT is noteworthy to be studied and solved. For

the bottom-gate TFT, an etch-stop (ES) layer prevents the IGZO layer from the damage of the etch process, and a passivation layer protects the whole device from the penetration of oxygen, moisture, hydrogen and other gases in the air, which are both common in use. Fig. 2. 10 shows the ES type and back-channel-etch (BCE) type bottom gate IGZO TFT. [61]

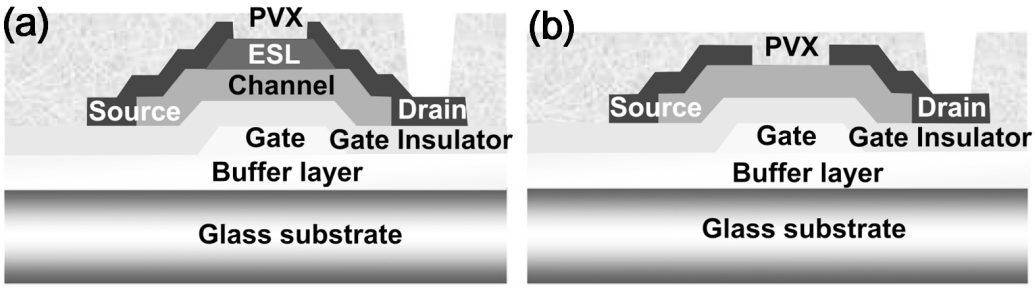


Fig. 2. 10 (a) Cross section of ES type staggered bottom gate TFT. (b) Cross section of BCE type staggered bottom gate TFT. [61]

Besides the above-mentioned fundamental structures, there are some advanced structures adopted for IGZO TFT.

Double-gate (DG) is widely used for IGZO TFT for better performance and reliability. In [62], J. Jang team has compared the DG IGZO TFT with the single-gate (SG) IGZO TFT. Fig. 2.17(a) shows the cross-section image of the device. It turns out that the DG BCE-type IGZO TFT has 50% lower S.S. and 2.53 times higher driving current than those of the SG IGZO TFT. In the DG BCE structure, the accumulation layer is not limited to the interface region but spread over the whole bulk of the IGZO layer. And the top gate is not overlapping with the S/D region with a 2-μm offset, avoiding the effect of parasitic capacitance.

Vertical IGZO TFT is promising for its high potential in flexible electronics. L. Yuan successfully demonstrated a flexible and scalable vertical IGZO TFT in [63]. Fig. 2. 11(b)

shows the 3D schematic (left) and cross-section image (right) of the device. In the vertical TFT (VTFT), the stack of source electrode graphene with tunable work function, the channel layer IGZO, and the drain electrode Ti forms a vertical heterostructure. The contact characteristics between the graphene and the IGZO layer could be modified by changing the work function of the graphene through the gate electrode. The on-off ratio (i.e., switching characteristics) of the TFT comes from the change of contact characteristics between the graphene and the IGZO. The biggest advantage of VTFT is its high tolerance to the mechanical bend, which makes it appropriate in large-area wearable devices.

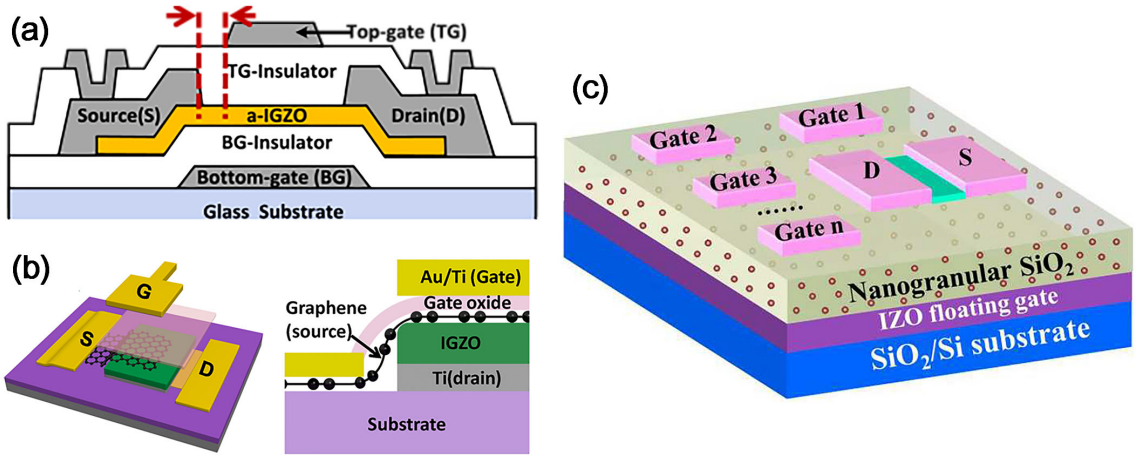


Fig. 2. 11 (a) Cross section of the DG BCE IGZO TFT. [62] (b) 3D schematic (left) and cross section (right) of the vertical IGZO TFT. [63] (c) 3D schematic of the multi-gate IGZO TFT. [64]

Multiple-gates is another kind of emerging structure for IGZO TFT. In [64], W. Qing team developed a multiple-coplanar-gate IGZO neuromorphic transistor based on nanogranular electrolyte. Fig. 2. 11(c) shows the schematic of the device. Those multiple gates are capacitively coupled to the IZO floating gate, providing single or multiple pulse inputs to realize the neuromorphic summation function with high linearity in either temporal

or spatial way. The multi-gate IGZO TFT is effective in neuromorphic computing applications, or sensors which need various input signals.

2.2.2 Figure of merits of IGZO TFT

As a kind of FET, the drain current (I_D) of the IGZO TFT can be calculated with the applied gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). With different values of V_{GS} and V_{DS}, the TFT works in different regions and I_D shows different behaviors. Equations (2.3) and (2.4) show the description of I_D in the linear region and saturation region, respectively:

When $V_{DS} < V_{GS} - V_{th}$, the TFT works at the linear region:

$$I_D = C_{ox}\mu_{FE}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (2.3)$$

When $V_{DS} > V_{GS} - V_{th}$, the TFT works at the saturation region:

$$I_D = \frac{1}{2}C_{ox}\mu_{sat}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (2.4)$$

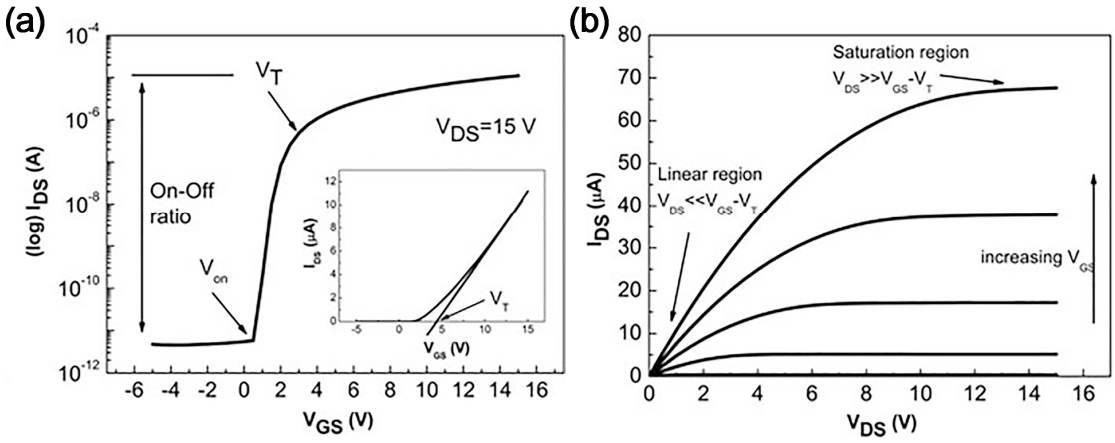


Fig. 2. 12 (a) Typical transfer curve of the IGZO TFT, and (b) Typical output curve of the IGZO TFT [65] Note: V_T inside the figures is right V_{th} in the following contents

In these two equations, W is the width of the channel layer, L is the length of the channel layer, μ_{FE} is the field-effect mobility of carriers, μ_{sat} is the saturation mobility of carriers, V_{th} is the threshold voltage, and C_{ox} is the capacitance per unit area of the gate oxide, which is calculated by Equation (2.5), where κ_{ox} and t_{ox} refer to the relative dielectric constant and thickness of the dielectric layer, respectively:

$$C_{ox} = \frac{\varepsilon_0 \kappa_{ox}}{t_{ox}} \tag{2.5}$$

To evaluate the performance of the IGZO TFT, the transfer curve which reflects the relationship of I_D versus V_{GS}, and the output curve which reflects the relationship of I_D versus V_{DS} are depicted from the measured data. Fig. 2. 12 shows the typical transfer curves and output curves of the IGZO TFT. Based on the transfer curves and output curves, the figure of merits (FOMs) of the IGZO TFT like μ_{FE}, μ_{sat}, S.S., V_{th}, on/off ratio, etc. are extracted.

On/off ratio: On/off ratio always refers to the ratio of I_D at on state and off state as indicated in Fig. 2. 12(a). On current is also known as driving current, which is one of the most important parameters for the TFT as a driving element in active-matrix display panels. According to Equations (2.3) and (2.4), large I_D always benefits from the large mobility (μ_{FE} or μ_{sat}), large W/L ratio of the channel, large C_{ox}, etc. Off current is also called the leakage current of the TFT. The leakage current comes from the excess carriers in the as-deposited IGZO layer, [66] and the inferior quality of the interface of channel/dielectric layer or the bulk of the dielectric layer. [67]

***Threshold voltage*:** V_{th} is the voltage at which most carriers accumulate at the interface of the dielectric layer and the channel layer. It is highly correlated with the carrier

concentration and carrier transport in the channel layer. The shift value of V_{th} is a significant indicator of the TFT reliability. There are many methodologies to determine V_{th}: 1). Predefine an I_D value, then the corresponding V_{GS} is the right V_{th}. In [68], J.-S. Park team defined V_{th} at which I_D equals L/W×10 nA. This method is straightforward and fast, whereas the carrier transport in IGZO TFT is complicated, and the predefine rule of I_D is arbitrary among different research teams. 2). As shown in the inset of Fig. 2. 12(a), extrapolation is a widely used method. At the linear transfer curve with a small V_{DS} (i.e., linear region), a tangent line is drawn at the point with the maximum slope. The intercept of the tangent line with the V_{GS} axis is the right V_{th}. This method is appropriate with TFTs free of the effects of mobility degradation at high V_{GS} [69], whose transfer curves show good linearity at the full span of V_{GS}. 3). In [70], Z. Chumin proposed a subgap DOS model to extract V_{th} with the aid of the 2-D numerical simulation. They take the difference between the built-in potential (V_{BI}) and the pinch-off voltage (V_p) as V_{th}. V_{BI} and V_p are found to be affected by the concentration of background carriers and the concentration of the ionized acceptor-like states in the depletion region. 4). In [71], L. Qiang and R. Yao took the carrier transport in IGZO films into consideration to develop the V_{th} extraction model. They define V_{th} to be the voltage at which the degenerate conduction forms. Degenerate conduction means high carrier concentration. This method could calculate the accurate V_{th} which is close to the measured value and help understand the carrier transport of the IGZO TFT. However, the calculation process is complicated and involves excess parameters, which makes it less practical when extracting V_{th} in an as-fabricated TFT.

The polarity of V_{th} decides the mode of the TFT. Negative or positive V_{th} corresponds to the depletion-mode or enhancement-mode TFT, respectively. By tuning the carrier concentration of the IGZO layer, the polarity of V_{th} could be modified, which is a good compensation for the lag development of p-type oxide-based TFT. In [72], I.-T. Cho demonstrated a full-swing inverter based on IGZO TFT. With the stress of negative bias in combination with light illumination and high temperature (60℃), the transfer curve of the TFT shows a negative shift in parallel. The depletion-mode IGZO TFT is realized. With the enhancement-mode TFT as a driver and the depletion-mode TFT as a load, an inverter with a fast switching speed and high voltage gain is achieved.

Subthreshold swing: S.S. is an FOM evaluating the switching speed of the TFT. As shown in Equation (2.6), it is defined as increment of V_{GS} with the increase of I_D by one order in the subthreshold region.

$$S.S. = \left(\frac{d\log(I_D)}{dV_{GS}}\middle|\max\right)^{-1} \tag{2.6}$$

The value of S.S. is extracted at the subthreshold region in the logarithm-based transfer curve as shown in Fig. 2. 12(a). Smaller S.S. indicates steeper subthreshold slop, which is desired for the TFT. The quality of the dielectric/channel interface could directly influence S.S., which means S.S. can be expressed by a series of terms considering the density of the interface trap states (D_{it}). Equations (2.7) and (2.8) show the expression of S.S. with and without interface traps, respectively. [73]

$$S.S._{(0)} = (\ln 10) \times \left(\frac{\partial V_{GS}}{\partial \ln I_{DS}}\right) = (\ln 10)\left(\frac{kT}{q}\right)\left(\frac{C_{ox}+C_D}{C_{ox}}\right) \tag{2.7}$$

$$S.S. = S.S._{(0)} + (\ln 10)\left(\frac{kT}{q}\right)\left(\frac{C_{it}}{C_{ox}}\right) = (\ln 10)\left(\frac{kT}{q}\right)\left(\frac{C_{ox}+C_D+C_{it}}{C_{ox}}\right) \tag{2.8}$$

In these two equations, C_{ox}, C_D and C_{it} denote the capacitance of gate oxide, depletion region in semiconductor, and interface trap states, respectively. k is the Boltzmann constant and q is the charge of the carrier. According to the expression of $C_{it} = q^2 D_{it}$, C_{it} is positively correlated with D_{it}. From Equation (2.8), S.S. of the TFT can be minimized by choosing gate oxide with a high dielectric constant (large C_{ox}), reducing IGZO bulk defect states (small C_D), and eliminating the interface traps (small C_{it}). [74],[75]

Mobility: The mobility of carriers in the channel layer is another crucial parameter, which directly determines the driving capability and the switching speed of the TFT. According to different extraction methods, the mobility of the channel is classified into field-effect mobility (μ_{FE}), saturation mobility (μ_{sat}), and effective mobility (μ_{eff}), which can be calculated by Equations (2.9), (2.10), and (2.11), respectively.

$$\mu_{FE} = \frac{g_m}{C_{ox}\frac{W}{L}V_{DS}} \tag{2.9}$$

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2}{\frac{1}{2}C_{ox}\frac{W}{L}} \tag{2.10}$$

$$\mu_{eff} = \frac{g_{DS}}{C_{ox}\frac{W}{L}(V_{GS}-V_{th})} \tag{2.11}$$

μ_{FE} is the most widely used parameter to characterize the carrier mobility of the TFT thanks to its concise formula. In addition, g_m in Equation (2.9) refers to the transconductance which is also defined as the gain of the transistor. It can be derived from the derivative of I_D over V_{GS}, which is right the slope of the linear transfer curve as shown in Fig. 2. 12(a). Ideally, in the linear region, g_m changes with V_{DS} linearly, but it is not affected by V_{GS}; while in the saturation region, g_m changes with V_{GS}, but it is not affected by V_{DS}. Thus, μ_{FE} is calculated at low V_{DS} (i.e., linear region).

μ_{sat} is calculated at high V_{DS}. The numerator of Equation (2.10) can be derived from the slope of $\sqrt{I_{DS}}$ versus V_{GS} curve. The limitation of μ_{sat} is that the effective channel length L_{eff} would be smaller than the practical channel length L at the saturation (or pinch-off) region. The smaller L_{eff} makes the extracted μ_{sat} physically inaccurate. [65]

μ_{eff} is also extracted at low V_{DS}. In Equation (2.11), the non-ideal change of mobility with V_{GS} is incorporated for consideration. In the linear region, the channel shows resistance characteristics, which means the conductance of the channel (g_{DS}) can be derived from the ratio of I_D over V_{DS}. This extraction method is considered the most accurate methodology. However, V_{th} is required to be determined in advance, which could induce some physical errors.

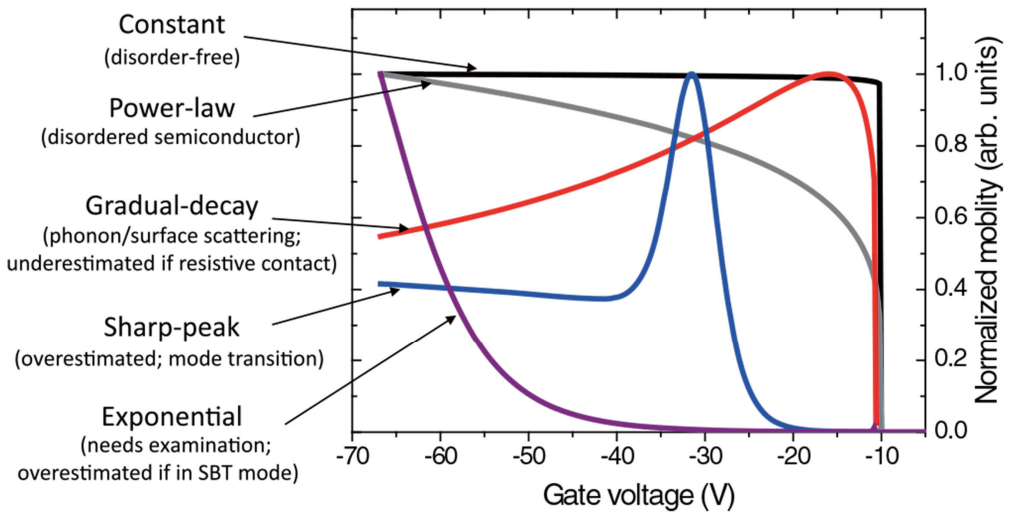


Fig. 2. 13 Mobility vs. V_{GS} curves of FETs with different contact conditions [76]

The most common issue when extracting the carrier mobility is the overestimation or underestimation. In [76], Chuan Liu systematically analyzed the carrier mobility extraction problems in FET regarding different contact types. As shown in Fig. 2. 13, mobility versus

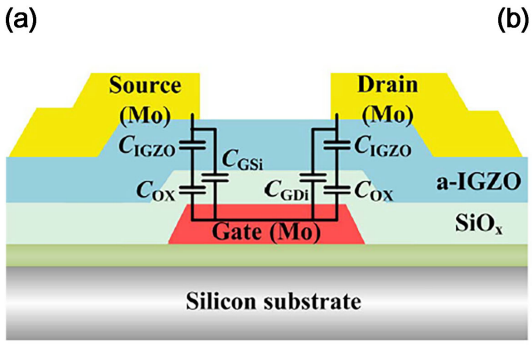
V_{GS} curves are drawn under various conditions. As marked in figure: 1). The black line at which the mobility maintains constant always refers to the FET with a channel based on a disorder-free semiconductor. [36] 2). The grey line at which the mobility curve obeys the power-law function usually refers to the FET with a channel based on a disorder semiconductor. [36] This power-law trend of mobility could originate from the hopping transport of charges between localized states. 3). The red line shows that the mobility curve follows a gradual-decay trend, possibly referring to two situations. Firstly, the gradual decay may be caused by the surface roughness scattering or phonon scattering at the high gate electric field. [77] Also, when the good ohmic contact reaches, g_m of the TFT would slightly decrease with V_{GS}. [78] In this situation, the contact resistance is much less dependent on V_{GS} compared with the channel resistance, the mobility is underestimated. 4). The blue line shows the mobility curve with an abrupt and sharp peak, which means the contact resistance is highly dependent on the gate electric field, and the FET contact turns into Schottky contact. In this case, the extracted mobility using the previously mentioned methods would be overestimated. 5). The purple line shows an exponential trend of the mobility curve. In this case, the FET turns into a pure Schottky barrier transistor. Those fundamental methodologies to extract the carrier mobility are no more correct, causing serious overestimation. [79]

2.2.3 Compact models of IGZO TFT

A large amount of research has been conducted to build the compact model of IGZO TFTs to physically describe the circuit-level behaviors of the device (current, capacitance,

transconductance, etc.) with more accurate mathematical expressions. Based on the main physical parameters used for calculation and simulation, the models of IGZO TFTs are generally classified into two types: charge-based model and surface-potential-based model.

Charge-based model: The charge-based model describes current-voltage (I-V) or capacitance-voltage (C-V) relationships in terms of varieties of charges (Q) in the TFT. The superiority of this kind of model is the incorporation of the capacitive couplings between every two terminals in the TFT, which largely improves the accuracy of the model. [80]-[81]



(b)

Intrinsic Capacitance	Extrinsic Capacitance
$C_{Gi} = \left.\frac{\partial Q_G}{\partial V_G}\right\|_{V_S, V_D = const}$ [F]	$C_G = C_{Gi} + 2C_{OV}$ [F] $C_{GD} = C_{GDi} + C_{OV}$ [F] $C_{GS} = C_{GSi} + C_{OV}$ [F]
$C_{GSi} = \left.\frac{\partial Q_S}{\partial V_G}\right\|_{V_S, V_D = const}$ [F]	**Overlap Capacitance (C_{OV})** $C_{OV} = C_{OX} // C_{IGZO}$ [F]
$C_{GDi} = \left.\frac{\partial Q_D}{\partial V_G}\right\|_{V_S, V_D = const}$ [F]	$C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} \times WL_{OV}$ [F] $C_{IGZO} = \frac{\varepsilon_{IGZO}}{T_{IGZO}} \times WL_{OV}$ [F]

Fig. 2. 14 (a) Demonstration of all equivalent capacitances in the IGZO TFT. (b) Expressions of varieties of capacitances as functions of different charges. [80]

In [80], M. Bai developed a dynamic charge-based model to express the C-V behaviors of the a-IGZO TFT. As shown in Fig. 2. 14, the basis of this model is the derivation of the charge in the three terminals (gate charge Q_G, drain charge Q_D, and source charge Q_S). To acquire the value of Q_G, Q_D and Q_S, the charge per unit area in the IGZO layer $Q_{TOT(y)}$ is important, which is the summation of the free charges ($Q_{FREE(y)}$) and the localized charges ($Q_{LOC(y)}$). 'y' in the subscript refers to the position in the axis of channel length. The simulated result of this model shows good agreement with the C-V curves. This is the first

analytical charge-based C-V model for IGZO TFTs, which is successfully applied in the inverter circuit simulation.

In [81], O. Moldovan reported a new analytical charge-based model for capacitance in the a-IGZO TFT, which is valid in both the subthreshold region and the above-threshold region. In the subthreshold region, the Fermi level of IGZO is located at deep states. Parameters used in the model include: the flat band voltage (V_{FB}), the mobility of the device when V_{GS} is at V_{FB} (μ_d), distribution of acceptor-like deep states (g_{ado}), and other function parameters for fitting. In the above-threshold region, the Fermi level of IGZO is leveled up to tail states. Parameters used in the model include the threshold voltage (V_{th}), the field effect mobility (μ_{FE}), distribution of acceptor-like tail states (g_{ato}), and other fitting parameters. To achieve better agreement between the measured and simulated data, a smoothing function (hyperbolic tangent, *tanh*) is applied. Eventually, the capacitances between every two terminals (G, D, S), and all intrinsic capacitances could be modelled with small deviation with the aid of 3D numerical Technology Computer Aided Design (TCAD) simulation. The parameter extraction in this work is precise, which makes it possible to model the transient AC characteristics of the IGZO TFT-based circuits.

Surface-potential-based model: Surface-potential-based model is more frequently utilized in IGZO TFTs thanks to its high accuracy and agreement level with experimental data of practical devices even without complex smoothing functions. [83]-[87] In the model, the surface potentials are usually derived based on the distribution of DOS. Then, different parameters like drain current, capacitance, etc. are modelled with the surface potential.

In [83], A. Tsormpatzoglou came up with an analytical I_D model based on surface potential for the a-IGZO TFT. The authors approximate the subgap states with two exponential distributions and describe I_D with two parts (diffusion and drift current) in the full span of V_{GS} and V_{DS} (i.e., the model fits for all operation regions). In addition, by considering the effects of both vertical and horizontal field on the mobility of carriers, the characteristics of the IGZO TFT are well modelled in either transfer curves or output curves.

In [84], L. Colalongo utilized CAD simulators to propose a complete surface-potential-based compact model for flexible IGZO TFTs. The author provides a new and concise formulation to model the TFT in the subthreshold region, as well as the linear and saturation regions. This model adopts the symmetric quadrature method (SQM) to derive I_D as the function of the surface potential, electric field, and contact charges. In addition, the trapped charges and transport of free carriers are explained with the MTR model and percolation model over the mobility edge.

In [85], J. Guo developed a novel surface-potential-based capacitance model for the independent DG IGZO TFTs with Verilog-A code. The transport of carriers in the TFT is described with the percolation model, trap-limited conduction (TLC) model, and variable-range hopping (VRH) model [88]. Also, the front surface potential and back surface potential of the IGZO are calculated in one single formular in the whole operation region with ultra-high accuracy. To improve accuracy, the threshold compensation effect is also considered in the model, which is important for the precise circuit-level simulation. In [85], the surface potential model, mobility model, current model, and capacitance model are all accomplished

with high accuracy and validated by experimentally fabricated devices. The effects of temperature and trap states on the independent DG IGZO TFT can be well predicted. Moreover, the simulation of ring oscillators and pixel circuit based on IGZO TFTs are both realized. [85]

2.3 Methods to improve performance of IGZO TFT

There are plenty of research reporting effective methods to improve the performance of the IGZO TFT in terms of various FOMs, which is one of the most concerning targets in this thesis. This section lists several typical reported methodologies following the sequence of the TFT structure: channel layer engineering, dielectric layer engineering, and S/D contacts engineering.

2.3.1 Channel layer engineering

The characteristics of the channel layer such as charge transport properties, carrier concentration, subgap DOS, and bonding states directly decide nearly all the behaviors of the IGZO TFT. Modifications on the channel layer through doping, semiconductor structure engineering, other treatments, etc., are proved to effectively improve the performance of the IGZO TFT.

Doping: Unlike doping in conventional Si-based FETs which is mainly realized by ion implantation, doping in IGZO has more convenient and diverse methods, including the dispersion of nano-structure materials like nanowires, nanoparticles, etc., co-sputtering during the deposition of the IGZO layer, and gas treatments, etc.

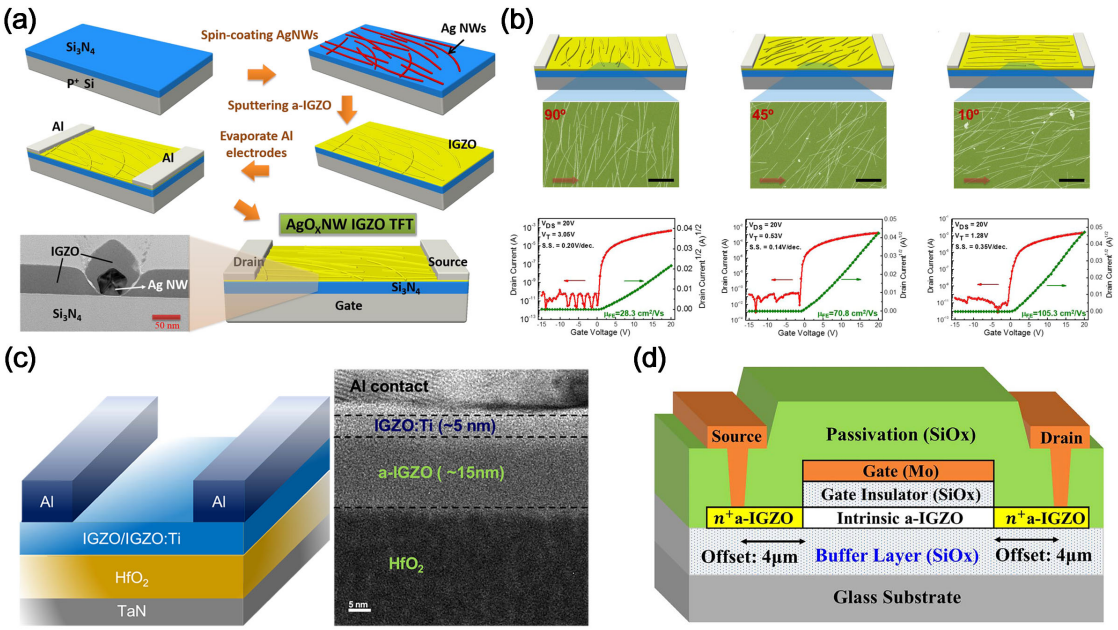


Fig. 2. 15 (a) Fabrication processes of the IGZO TFT doped by Ag nanowires. (b) Comparison of IGZO TFTs with different Ag nanowires doping orientations. [90] (c) 3D schematic and TEM image of cross section of the TFT with IGZO/IGZO:Ti bilayer channel. [94] (d) 3D schematic of cross section of the IGZO TFT with F-doping offset region. [97]

Doping the nano-structure materials into IGZO is always an efficient method to largely increase the carrier mobility of the IGZO TFT by providing resistance-less conduction paths with lower potential barrier heights. [89],[90]

In [89], H.-W. Zan used self-organized polystyrene spheres (200 nm diameter) as dopants for nano-dot-doping (NDD) in the IGZO TFT. The top-gate IGZO TFT with NDD shows the highest μ_{eff} of 79 cm^2/Vs, which is 19 times higher than that of the TFT without the NDD. According to the authors, the potential barrier height is closely related to the concentration of NDD. With the increase of NDD density, the effective length of the channel is reduced, and the potential barrier height becomes lower.

In [90], H.-C. Liu grew the silver (Ag) nanowire array in certain directions between the

IGZO layer and the dielectric layer. Fig. 2. 15(a) shows the fabrication processes of the TFT. Ag nanowires are grown on the dielectric layer by spin-coating or blade-coating with the length of 10 ~ 15 μm, and the diameter of 70 ~ 100 nm. In comparison, blade-coated Ag nanowires show random distribution, while spin-coated Ag nanowires can be oriented at specific angles thanks to the centrifugal force. Fig. 2. 15(b) shows the comparison of IGZO TFTs with different growth directions. When the Ag nanowire array lies in the orientation forming 10 degrees with the current flow direction, μ_{FE} of the modified IGZO TFT reaches 114.3 cm^2/Vs, which is nearly 10 times higher than that of the standard IGZO TFT. At the same time, V_{th} of the modified IGZO TFT decreases a lot from 2.1 V to 0.6 V. S.S. of the TFT is maintained at the same level (~ 200 mV/dec), indicating that the quality of the IGZO/SiN_x interface does not deteriorate by the doping of Ag nanowires. The authors attribute the tremendous mobility enhancement to the incorporation of Ag nanowires at the IGZO/SiN_x interface, which is also the accumulation region for electrons. These aligned nanowires provide highly conductive paths for the transport of electrons, reducing the effective channel length. Consequently, higher parallelism between Ag nanowires orientation and the current flow direction produces larger carrier mobility and driving current of the IGZO TFT.

Doping specific metals like Mg, Ti etc. into IGZO is an effective scheme to change its carrier concentration, bonding states, and density of defect states, and it is usually accomplished by co-sputtering. [91]-[94]

In [91] and [92], the authors both demonstrated Mg-doped IGZO TFTs with improved performance. For instance, H.-C. Wu reported that the TFT with a composite of IGZO and

Mg-IGZO shows a larger on/off ratio and smaller S.S. compared with the pure IGZO TFT. However, the carrier mobility of the doped TFT degrades. [91] The incorporation of Mg can change the oxygen bonding state, effective electron mass and carrier concentration in IGZO. To further improve μ_{FE} of the Mg-doped IGZO TFT, A. Abliz fabricated a hydrogenated Mg-doped IGZO (IGZO:Mg/H) TFT in [92]. With the mix of H_2, stable bonds between oxygen vacancy (V_O) and H are formed, acting as shallow donor states in IGZO. On the other hand, the doping of Mg increases the formation possibility of V_O and promotes the formation of complexes of Mg-V_O. Under the balance of V_O-H bonding and Mg-V_O complex, the carrier concentration of IGZO is controlled at a reasonable level. As a result, μ_{FE} of the IGZO:Mg/H TFT is enhanced to 35.6 cm^2/Vs which is nearly twice higher than that of the pristine IGZO TFT (13.5 cm^2/Vs).

Ti is another common dopant in IGZO. [93],[94] In [94], H.-H. Hsu realized high mobility TFTs with bilayer channel structure of IGZO and Ti-doped IGZO. Fig. 2. 15(c) shows the 3D schematic and TEM image of the TFT. The 5 nm IGZO:Ti film is deposited by co-sputtering with Ti and IGZO targets. For the TFT with a pure IGZO channel, the driving current is 1 μA, V_{th} is 1.15 V, S.S. is 171 mV/dec, and μ_{FE} is 5.1 cm^2/Vs. While for the TFT with a bilayer channel, driving current is the 160 μA, V_{th} is 0.86 V, S.S. is 73 mV/dec, and μ_{FE} is 53 cm^2/Vs. The reduction of V_{th} and S.S. results from the improved efficiency of carrier injection at the interface of IGZO:Ti and S/D contacts. Moreover, Ti atoms in the upper IGZO:Ti layer tend to capture O atoms from the bottom IGZO layer, which increases the concentration of V_O (i.e., carrier concentration) in the IGZO layer. Based on the percolation model, μ_{FE} of the TFT is

greatly increased. At the same time, IGZO:Ti itself is a passivation layer with low carrier concentration, which guarantees the low off current of the TFT.

Gas plasma treatments, for instance, nitrogen, hydrogen, fluorine, etc., could also effectively dope the IGZO layer in the TFT. [95]-[97] Doping of nitrogen (N_2) into IGZO is an effective way to passivate excess oxygen vacancies in IGZO, which significantly improves the reliability and stability of the IGZO TFT. [95] Hydrogen doping could increase the carrier concentration in IGZO, which realizes a high μ_{FE} of 26.5 cm^2/Vs in the TFT. Meanwhile, as mentioned earlier, hydrogen can combine with excess V_O, becoming shallow donor states, which enhances the reliability of the TFT. [96] Fluorine (F) is an interesting dopant as reported in [97]. A. Rahaman fabricated a coplanar IGZO TFT with a 4-μm offset length in the channel region as shown in Fig. 2. 15(d). The authors highly dope the offset region of the IGZO layer by F plasma treatment. On the one hand, the resistance of the offset region is largely reduced. On the other hand, F is inclined to diffuse into the channel layer and substitute O to bond with metals in IGZO, increasing the density of V_O in the channel. [98] The increased carrier concentration in the channel layer leads to the high μ_{FE} (27.17 cm^2/Vs) of the TFT. At the same time, F atoms in the channel/dielectric interface would form SiO_x:F passivation layer, reducing the density of trap states and weakly bonding states. This passivation effect keeps the low leakage current and improves the reliability of the TFT.

Semiconductor structure engineering: A series of papers are devoted to applying multi-layer channel structure in IGZO-based TFTs. [99]-[102] The biggest contribution of the multi-layer structure is the formation of heterostructure and the introduction of 2D electron gas in

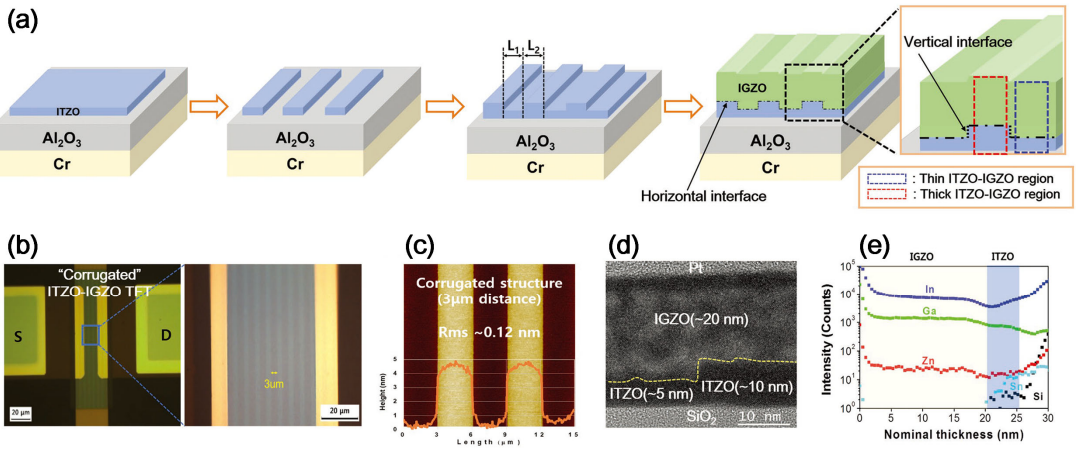


Fig. 2. 16 (a) Fabrication processes of the corrugated heterojunction metal oxide TFTs. (b) Optical vertical view of the TFT. (c) AFM scan image showing the surface profile of the channel structure. (d) TEM image of the cross section of the channel region. (e) Profiling of each element in the bilayer corrugated channel region by ToF-SIMS. [102]

the carrier transport. A bilayer metal oxide TFT fabricated in [102] is a typical case taking advantages of the semiconductor heterostructure. M. Lee designed a channel layer with corrugated heterostructure based on Indium-Tin-Zinc-Oxide (ITZO) and IGZO. As shown in Fig. 2. 16(a), corrugated structure means that the thickness of ITZO/IGZO is alternating. Other images in Fig. 2. 16 characterize the corrugated structure from various aspects. By optimizing the thickness of ITZO and IGZO, the TFT achieves a high μ_{FE} larger than 50 cm^2/Vs with a high on/off ratio 3.6×10^8. Firstly, the high mobility and driving current are attributed to the formation of 2D electron gas at the heterointerface of ITZO and IGZO. The origin of the high mobility of 2D electron gas is the confinement of electrons at the potential well created by the band alignments between ITZO and IGZO. By suppressing the movement of electrons in the direction perpendicular to the interface, the mobility of electrons is raised remarkably. Then, the low leakage current of the TFT benefits from the vertical region of the

corrugated structure. When a negative bias is applied to the gate, 2D electron gas refrains at the vertical interface, which effectively prevents electrons migrating into the region with high carrier concentration (ITZO).

Other treatments: Some other typically novel means to modify the IGZO layer are stated in the following:

In [103], W.-S. Liu improved the performance of DG IGZO TFTs with the combination of Ar-O_2 plasma treatments and rapid thermal annealing (RTA). These two treatments are effective in reducing the surface roughness and tuning the carrier concentration to a reasonable level (3.8×10^{18} cm^{-3}). The performance of the TFT shows tremendous improvement (on/off ratio 5.46×10^8, μ_{FE} 58.8 cm^2/Vs, S.S. 120 mV/decade) thanks to the attenuated surface scattering effect.

In [104], Y. Shin demonstrated a high-mobility c-IGZO TFT with 300 ℃ crystalline temperature. The authors induce a tantalum (Ta) metal catalytic layer, forming a top interface with the amorphous IGZO layer. Electrons released from Ta move to the anti-bonding orbitals of In-O and Ga-O bonds. Under low-temperature annealing (300 ℃), those M-O bonds weakened by the invasion of electrons would be broken. Then, crystalline IGZO is formed with the rearrangement and diffusion of broken M-O bonds and metallic In, Ga. After the transformation from a-IGZO to c-IGZO, the TFT shows increased μ_{FE} from 18.1 cm^2/Vs to 54 cm^2/Vs, reduced S.S. from 800 mV/dec to 300 mV/dec, decreased V_{th} from 0.9 V to 0.2 V, and enlarged on/off ratio from 1.2×10^7 to 4.4×10^7.

In [105], J. Sheng adopted plasma-enhanced atomic layer deposition (PEALD) to grow

the IGZO layer as the channel of TFTs. ALD can precisely control the thickness of the thin film within sub-nanometer. In this work, the channel layer is composed of interlayers of GaZnO/In_2O_3 heterostructure. By controlling the thickness of the In_2O_3 layer to 1.8 nm, μ_{sat} of the TFT reaches 74 cm^2/Vs. At the same time, GaZnO layer suppresses the redundant V_O produced in In_2O_3, which prevents the large leakage current and excessively negative shift of V_{th}.

It is not practical to cover all the methods of modifying the IGZO channel layer in this thesis. Nevertheless, all methods applied in the literature have the same motivations, i.e., controlling the carrier concentration, ameliorating the surface (front and back sides) quality, and reducing the density of defect states in IGZO.

2.3.2 Dielectric layer engineering

The dielectric layer in IGZO TFTs is crucial as well, which is the origin of the field effect in the TFT. The dielectric constant κ directly determines the driving current, S.S., V_{th} of the TFT, and the band offset relative to the IGZO layer affects the gate leakage of the device. This section contains methods to balance trade-offs among dielectric constant, insulating ability and interface trap density of the dielectric layer.

As indicated by the classic I_D calculation equations for FETs (Equations (2.3) and (2.4)), high-κ of the dielectric layer is consistently pursued for IGZO TFTs. A lot of oxides and nitrides with high κ have been attempted in the early stage, such as ZrO_2 [106], Ta_2O_5 [107], Y_2O_3 [108], HfLaO [109], etc. However, the E_g and charge neutrality level (CNL) of the

dielectric layer are also important to decide the band offset between the dielectric and semiconductor layer. A large band offset is necessary to block the charge transport between the channel layer and gate terminal through the dielectric layer. Table 2. 2 summarizes some typical high-κ dielectrics with their E_g, CNL, κ, and CB offset regarding metal oxide semiconductors. [110],[111]

Table 2. 2 Summary of dielectric characteristics of oxides and nitrides on metal-oxide semiconductor [110],[111]

	E_g (eV)	CNL (eV)	κ	CB offset (eV)
SiO_2	9	4.5	3.9	4.27
Si_3N_4	5.3	3.0	7	2.35
Al_2O_3	8.8	5.5	9	2.34
HfO_2	6	3.7	25	2.26
ZrO_2	5.8	3.6	25	2.7
Ta_2O_5	4.4	3.3	22	1.1
Y_2O_3	5.7	2.4	15	2.63
La_2O_3	6.0	2.4	30	3.1
Gd_2O_3	6.0	2.4	16~18	2.55
$LaAlO_3$	5.6	3.8	30	2.91
MgO	7.8	4.0	6.8~9.6	3.79

To merge high-κ, low trap density and large band offset, multi-layer dielectrics are widely employed in IGZO TFTs [112]-[115]. In [112], L. Yuan achieved high performance a-

IGZO TFTs by adopting a sandwich-like structure of $HfO_xN_y/HfO_2/HfO_xN_y$ (NON) as dielectrics. HfO_2 is a competitive candidate as gate insulator in CMOS technology for its high κ. But ion conductivity in HfO_2 would bring high density of trap states, large gate leakage and large hysteresis in transfer curves of transistors. The HfO_xN_y layer is prepared by reactive sputtering (Ar/N_2 (7%)) using the HfO_2 target. Doping of N effectively passivates V_O and reduces the density of trap states in HfO_2. Thus, the HfO_xN_y layer interfacing gate terminal supresses the gate leakage of the TFT, and the HfO_xN_y layer interfacing IGZO reduces the interface trap states. Compared to the TFT with a pure HfO_2 dielectric layer, the TFT with NON dielectrics shows a higher on/off ratio of 2.2×10^6, smaller S.S. of 130 mV/dec, and higher μ_{sat} of 10.2 cm^2/Vs.

Optimization of the deposition process is also a feasible way to modify the dielectric layer. In [116], Y. Shao deposited Al_2O_3 with O_2 plasma-enhanced ALD at room temperature as the dielectric of IGZO TFTs. Secondary-ion mass spectrometry (SIMS) analysis on the H profile in the stack of IGZO/Al_2O_3 shows that the Al_2O_3 layer deposited at room temperature has a higher H concentration compared with that deposited at a higher temperature. H in Al_2O_3 could be released during the deposition of IGZO, which passivates the interface trap states and eliminates excess V_O in IGZO. At the same time, H acts as donor in IGZO and elevates the electron concentration. [116] In sum, the authors realize a high-performance IGZO TFT with a large on/off ratio of 4.5×10^8, high μ_{FE} of 19.5 cm^2/Vs, low V_{th} of 0.1 V, and small S.S. of 160 mV/dec by inducing an H-rich Al_2O_3 dielectric layer.

2.3.3 Source/drain contacts engineering

The choice of S/D electrodes which covers various metals and transparent conductive oxides (TCOs), and the layout of S/D contacts with IGZO both have a great impact on the behavior of IGZO TFTs. 1). Difference between the work function of S/D and the electron affinity of IGZO determines the contact type, i.e., ohmic contact or Schottky contact. An ohmic contact is desirable to minimize barrier heights for electrons to flow in and out of IGZO. [117] 2). Intrinsic properties of S/D electrodes, like diffusivity, resistivity, enthalpy of oxidation, etc., would affect the performance and lifetime of IGZO TFTs. [118] 3). The overlap area between S/D and IGZO produces offset resistance, influencing V_{th} and S.S. of the TFT. [119] Methods to improve S/D contact characteristics have been extensively reported in literature.

Metals like Ti, Cu, Al, TiN, etc., and TCOs like ITO, AZO both show good contact with IGZO as S/D electrodes. Cu is the most widely used electrode material in CMOS technology thanks to its low cost and resistivity. However, Cu has a high potential to diffuse into IGZO to deteriorate the TFT performance by hybridizing with O atoms in IGZO and forming acceptor-like states above the VB. [120] To prevent the diffusion of Cu, insertion of the barrier layer is an effective method. [120],[121] In [120], S. Hu inserted a 30 nm ITO layer between Cu and IGZO as a barrier layer. μ_{FE} is raised from 5.2 cm^2/Vs for the Cu-based TFT to 11.5 cm^2/Vs for the Cu/ITO-based TFT. In [121], C. K. Lee inserted a 5 nm Ca-doped CuO_x as a barrier layer between CuCa and IGZO. The alloy CuCa could mitigate the diffusion of Cu into IGZO effectively. Still, the leakage current of the IGZO TFT with CuCa S/D contacts is

high. Then, the insertion of the ultra-thin $CuCaO_x$ dielectric layer between CuCa and IGZO successfully further prevents the Cu diffusion, achieving high performance of the IGZO TFT with a higher μ_{FE} of 20.7 cm^2/Vs, smaller S.S. of 430 mV/dec, and larger on/off ratio of ~10^8.

For TCOs, ITO is the most frequently used S/D electrode in transparent IGZO TFTs for its low resistance and high optical transparency. However, it is hard to achieve perfect ohmic contact between ITO and IGZO. In [122], S.-H. Choi formed an interlayer between ITO and IGZO, which is a layer of co-sputtering deposited IGZO-doped ITO. The SIMS profiles of O, Zn, Ga, and In in the IGZO TFT structure show that there exists oxygen interdiffusion between the IGZO-doped ITO interlayer and the IGZO channel layer, which increases the concentration of V_O and metallic In in IGZO. With the channel layer turning into In-rich IGZO, the contact resistance of the TFT extracted from the gated-transmission line method shows an enormous reduction from 7.04×10^3 Ω/μm to 4.14 Ω/μm. Meanwhile, μ_{sat} of the TFT increases from 9.1 cm^2/Vs to 35.4 cm^2/Vs.

2.4 Advanced applications of IGZO TFT

The IGZO TFT is popular for its high potential in a variety of areas. By making use of different properties of IGZO or dielectrics, researchers have succeeded in applying IGZO TFTs in high-resolution displays, flexible electronics, sensors and detectors, synaptic and memory devices, etc.

2.4.1 High-resolution displays

Since the first commercial phone with IGZO-based LCD screen was announced by

Sharp company in 2012, IGZO TFTs started to substitute Si-based TFT and become the main driving technology in high-resolution active-matrix display panel markets.

FPDs: Flat panel displays like AMLCD, AMOLED and transparent displays have been extensively reported based on IGZO TFTs. In [123], T. Arai from Sony company demonstrated an 11.7 inch-diagonal quad-high-definition (QHD) AMOLED panel based on IGZO TFTs (Fig. 2. 17(a)). The IGZO TFT adopts an ES-type bottom-gate inverted structure, which shows the optimized carrier mobility of 11.5 cm^2/Vs, S.S. of 270 mV/dec, and V_{th} of 0.3 V. The panel has the highest brightness over 600 cd/m^2, resolution of 960×540 pixels, contrast ratio over 10^6:1, and color saturation higher than 100% NTSC. In [124], Y.-M. Ha from LG Display company successfully implemented a 65-inch ultra-high-definition (UHD) television based on OLED driving by IGZO TFTs (Fig. 2. 17(b)). The IGZO TFT is grown on light shielding layers with a self-aligned top-gate coplanar structure. The television shows a resolution of 3840×2160 pixels, aperture ratio of 31.6% on average, highest white brightness of 450 cd/m^2, and contrast ratio higher than 10^6:1. Also, the authors realized a 27-inch quad-quad-high-definition (QQHD) AMLCD panel based on IGZO TFTs which adopts the ES-type bottom-gate inverted structure (Fig. 2. 17(c)). The resolution of the panel is extremely high at 5120×2880 pixels with a high density of 218 ppi. In [125], N. Gong from LG Display company demonstrated a 55-inch ultra-definition (UD) AMLCD panels based on a-IGZO TFTs with μ_{FE} of 11.53 cm^2/Vs, S.S. of 260 mV/dec, V_{th} of -0.6V (Fig. 2. 17(d)). The panel has a resolution of 3840×2160 pixels, charging time of 1.6 μs, brightness of 500 nit, and contrast ratio of 1600:1.

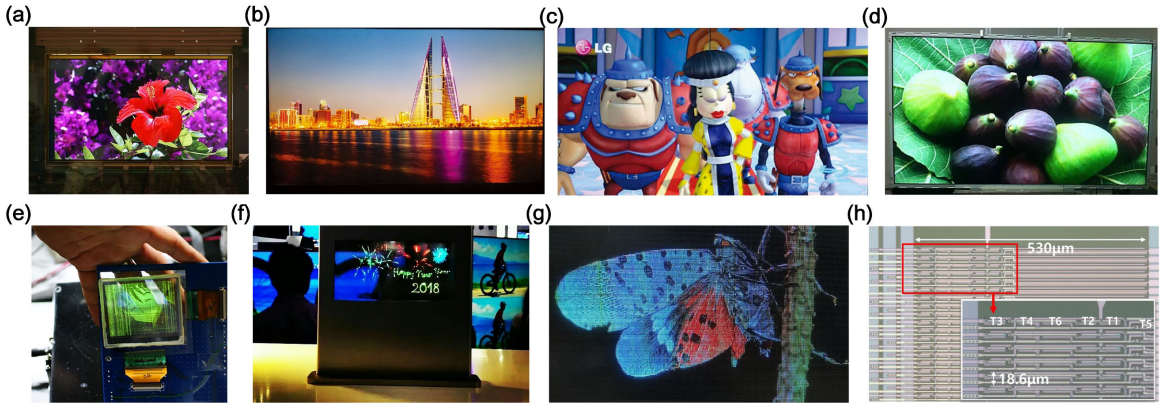


Fig. 2. 17 (a) 11.7 inch-diagonal QHD AMOLED panel based on IGZO TFTs. [123] (b) 65-inch UHD AMOLED panel based on IGZO TFTs. [124] (c) 27-inch QQHD AMLCD panel based on IGZO TFTs. [124] (d) 55-inch UD AMLCD panel based on a-IGZO TFTs. [125] (e) 3.2-inch transparent AMOLED panel based on IGZO TFTs. [126] (f), (g) 8-inch transparent AM-μ-LED panels based on IGZO TFTs. [127] (h) Gate driver circuit based on BCD-type DG IGZO TFTs appropriate for AR/VR display. [12]

Transparent panels based on IGZO TFTs are emerging thanks to the wide E_g of IGZO and the development of TCOs as S/D electrodes. In [126], S.-H. K. Park from NeoView Kolon company achieved a 3.2-inch quarter-video-graphics-array (QVGA) transparent AMOLED panel with transparent top-gate IGZO TFTs (Fig. 2. 17(e)). This panel shows high transparency of 80%, resolution of 320×240 pixels, and an aperture ratio of 67.68%. In [127], J. Fan from China Star Optoelectronics Semiconductor Display company implemented an 8-inch transparent active-matrix μ-LEDs panel with the transparent IGZO TFT backplane (Fig. 2. 17(f) and (g)). The panel shows high transparency of over 60%, color saturation higher than 114% NTSC, and a high aperture ratio of 82%.

Flexible displays: As the main branch of flexible electronics, flexible displays have been massively reported based on flexible IGZO TFTs.

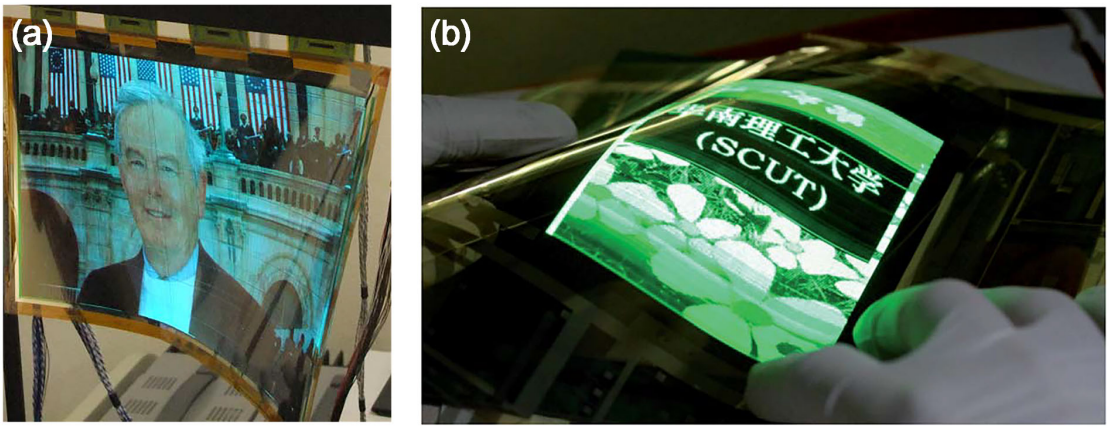


Fig. 2. 18 (a). 11.7-inch flexible QHD AMOLED on PI substrate based on IGZO TFTs. [128] (b). 5-inch flexible QVGA AMOLED on PEN substrate based on IGZO TFTs. [129]

Up till now, there are already many demonstrations of flexible displays based on IGZO TFTs. [128]-[131] In [128], as shown in Fig. 2. 18(a), H. Yamaguchi from Toshiba Mobile Display company demonstrated an 11.7-inch QHD AMOLED on a transparent and flexible PI substrate based on flexible transparent IGZO TFTs. The TFT exhibits high μ_{sat} of 17.3 cm^2/Vs, low S.S. of 210 mV/dec, and small V_{th} of 0.86 V. In the meantime, the TFT shows an extremely small shift of V_{th} (< 0.03 V) under PBTS for 2000s. The display shows a resolution of 94 ppi with each-pixel area of 270×270 μm^2. In [129], as shown in Fig. 2. 18(b), H. Xu reported a 5-inch QVGA AMOLED fabricated on flexible polyethylenenaphthalate (PEN) substrate with high-performance flexible bottom-gate IGZO TFTs. The authors adopt a costless and high-efficiency deposition method for gate/gate insulator: Al:Nd/anodic AlO_x:Nd, which shows good side-face-coverage characteristics and effectively prevents the shortage between the gate and S/D electrodes. For performance, the TFT owns a large on/off ratio reaching 10^9, high μ_{sat} of 12.87 cm^2/Vs, and low S.S. of 200 mV/dec. For mechanical robustness, the TFT shows -0.42 V V_{th} shift and 90 mV/dec S.S. increment under the bending

with a 20-mm radius of curvature.

2.4.2 Sensors and detectors

IGZO TFTs can be employed as sensors for various physical signals, like light illumination, pressure, bio-chemicals, temperature, etc., with different mechanisms. For different kinds of sensors, the evaluation criteria for TFT performance are different.

Photodetectors: The photo sensitivity of IGZO is observed early, which causes the obvious instability of the IGZO TFT under light illumination. [132] When the IGZO TFT is exposed to the light with large photon energy (larger than the E_g of IGZO), electron-hole pairs would be generated near the VBM. Electrons in these pairs would be expelled to surpass the Fermi level and increase the carrier concentration in the IGZO layer. As a result, V_{th} of the TFT shifts in the negative direction, and S.S. of the TFT deteriorates for the creation of more trap states below CBM. This intrinsic photo instability, which is regarded as a flaw for the IGZO TFT to be applied in the display-pixel circuits, conversely becomes the basis for the TFT to be employed as a photodetector.

As shown in Fig. 2. 19, IGZO TFTs are enormously reported to successfully detect light illumination with a wide range of wavelengths. [133]-[139] Take the infrared (IR) detector based on IGZO TFT for an instance, IGZO shows little absorption in far IR wavelengths due to its low photon energy. Still, researchers have succeeded in detecting IR based on IGZO TFTs with the aid of structural modifications. In [139], H. Ferhati fabricated an IGZO TFT utilizing a high-κ dielectric layer in combination with a Ge capping layer (Fig. 2. 19(c)).

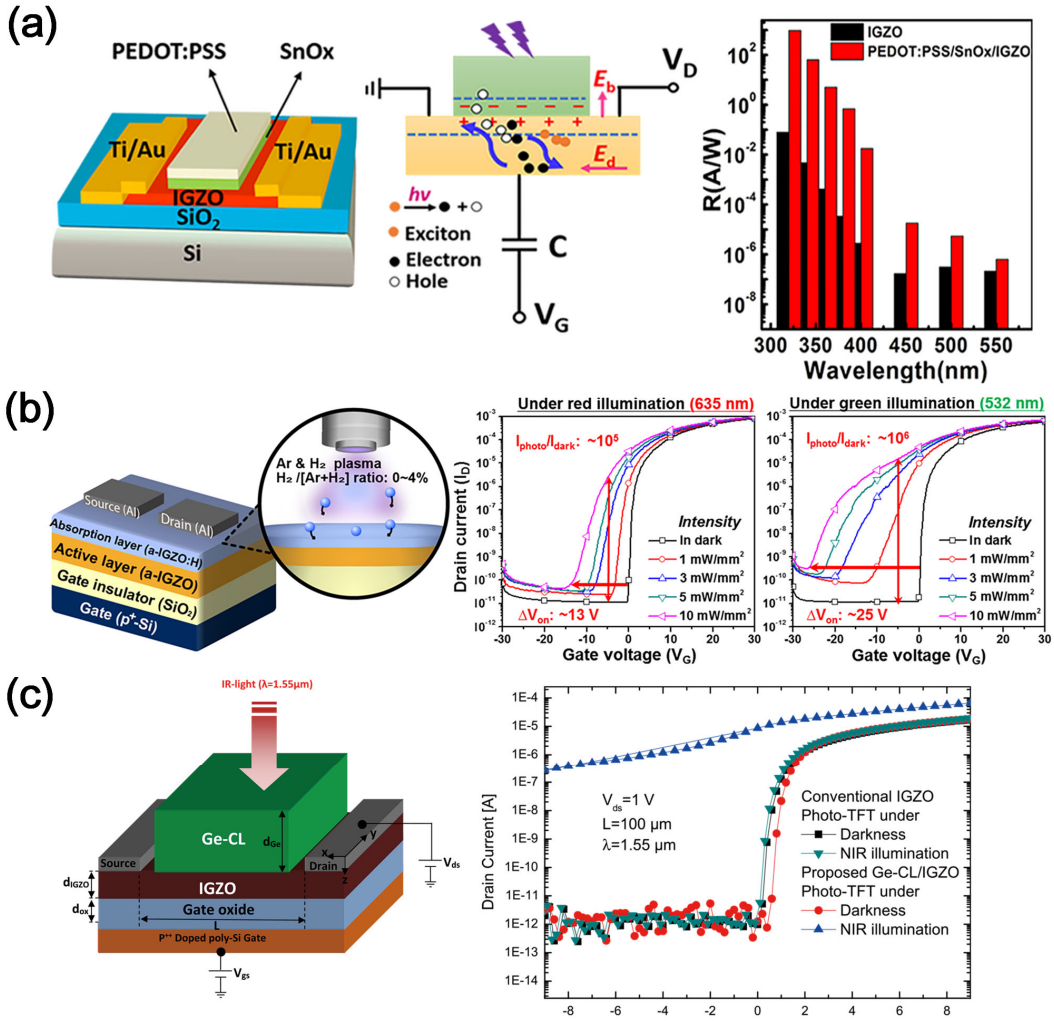


Fig. 2. 19 (a) Device schematic and responsivity of the visible-blind UV detector based on IGZO hybrid phototransistor. [134] (b) Device schematic and responses to green/red lights of the visible light detector based on IGZO phototransistor. [137] (c) Device schematic and response to infrared of the infrared detector based on Ge-capped IGZO phototransistor. [139]

Firstly, the dielectric layer with high κ is beneficial for IR detection by enhancing the controllability of the gate terminal over the IGZO conductivity, and modulating the distribution of potential in the IGZO layer. Results in [139] show higher responsivity to IR of TFTs with HfO_2, ZrO_2, Ta_2O_5 and TiO_2 dielectrics than that of the TFT with SiO_2 dielectric. Secondly, Ge is a typical p-type semiconductor, which has high IR absorption efficiency. The

integration of Ge and IGZO forms a p-n junction, which promotes the separation of the photo-generated electron-hole pairs and drives more electrons to the conduction path in IGZO. As shown in Fig. 2. 19(c), the IGZO TFT proposed in this paper shows high responsivity to IR of 4.1×10^2 A/W. The responsivity is calculated from the ratio of photocurrent of the IGZO TFT to the IR intensity.

Pressure sensors: Pressure sensors based on IGZO TFTs are mainly developed on plastic substrates for next-generation touch screens and wearable devices. By integrating with piezo-electric or piezo-capacitive materials, the output current of the TFT could be effectively tuned by applied pressure. [140]-[144] In [141], C. Xin developed a flexible capacitive pressure sensor array by integrating micro-structured piezo-capacitive PDMS thin film with IGZO TFTs (Fig. 2. 20(a)). When external pressure is applied to the PDMS thin film, the change of capacitance would change the bias applied to the gate terminal. Thanks to the microstructures of PDMS and the steep S.S. of the TFT, the device shows high sensitivity to the pressure below 1.5 kPa, and good linearity with the pressure from 0 to 7 kPa. In [142], Z. Zhang proposed a flexible piezoelectric pressure sensor by combining a-IGZO TFT with AgNWs-doped P(VDF-TrFE) thin film. As shown in Fig. 2. 20(b), the P(VDF-TrFE)-based capacitor is integrated with the IGZO TFT through the bottom gate. When external pressure is applied to the top gate of the capacitor, a potential would be produced and biased to the bottom gate of the TFT, inducing the change of the output current. This piezoelectric pressure sensor system has shown high sensitivity to external pressure of 1100 mV/N, as well as high linearity.

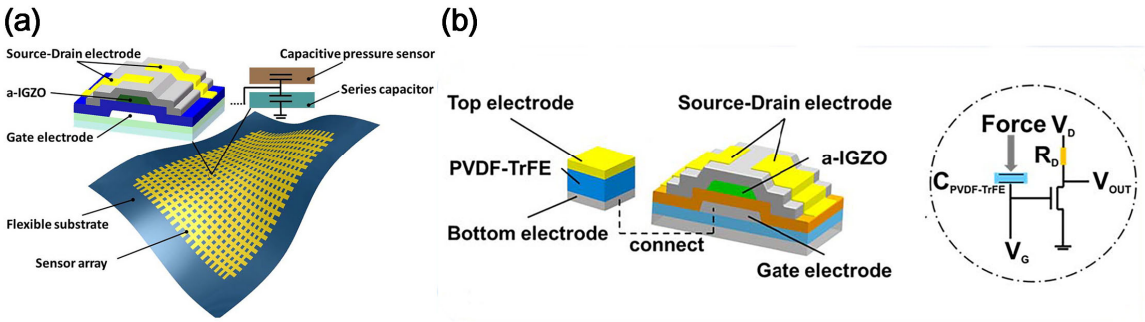


Fig. 2. 20 (a). Schematic of the capacitive pressure sensor based on IGZO TFT. [141] (b). Schematic of the piezoelectric pressure sensor based on IGZO TFT. [142]

Besides above mentioned representative sensors, other sensing schemes like biosensors [145]-[147], gas sensors [148],[149], temperature sensors [150],[151], etc. are all widely reported. There is no doubt that IGZO TFT has become an indispensable element in the emerging development of IoTs and MEMS technologies.

2.4.3 Memory and synaptic devices

Another significant application for IGZO TFTs is memory and synaptic devices. As the limit of Moore's Law for the conventional CMOS process becomes closer and closer, the development of next-generation memory and computing system is imminent. IGZO TFT has become an outstanding candidate for either memory or synaptic devices thanks to its low leakage current, low-temperature and low-complexity process, high uniformity, diversity of memory mechanisms, and feasibility to either flexible or highly transparent substrate.

Charge-trapping-flash transistor memory: Positive gate bias has been extensively reported to cause V_{th} shift of the IGZO TFT, which is caused by charge trapping in the bulk of dielectric and the channel/dielectric interface. V_{th} shift is a sort of serious instability for

TFT as a driving switch in display-pixel circuits, whereas researchers utilize this charge trapping to realize memory behavior in TFTs. When the program signal (positive pulse bias) is applied to the gate, V_{th} of the IGZO TFT is expected to shift to and be retained at a value until erased by a negative pulse bias. For conventional TFTs, charge-trapping-caused V_{th} shift is a temporary phenomenon, which will be recovered soon when trapped electrons spontaneously diffuse back to the channel layer. To enhance the controllability of gate bias

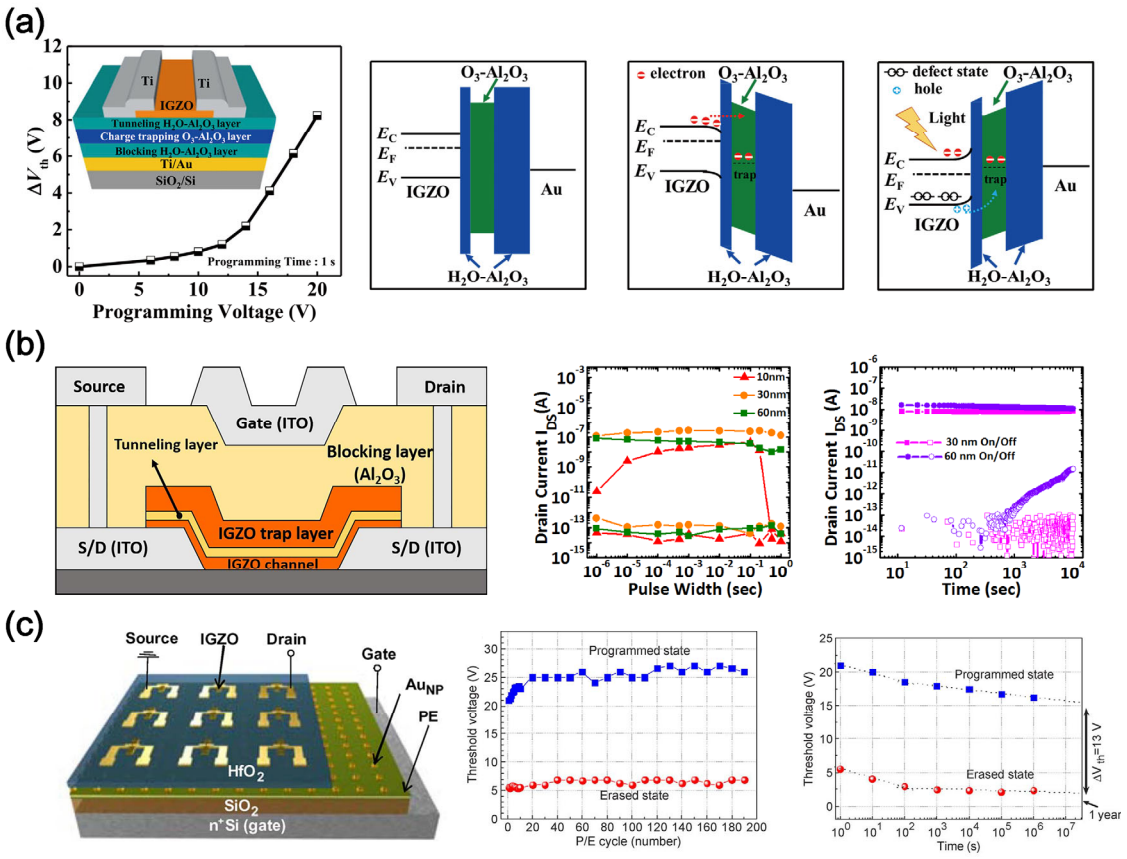


Fig. 2. 21 (a) Device schematic and band diagrams of the IGZO CTF memory transistor with Alumina-CTL. [158] (b) Device schematic and retention test of the IGZO CTF memory transistor with IGZO-CTL. [161] (c) Device schematic and memory window of the IGZO memory transistor with embedded Au-nanoparticle floating gate. [163]

over V_{th} value and realize the non-volatility of the memory, the charge-trapping-engineered flash (CTEF) structure is applied in the dielectrics. This structure refers to a sandwich-like stack of blocking layer (BL) interfacing with gate electrode to reduce leakage current, charge-trapping layer (CTL) providing abundant trap sites to capture/release carriers when the program/erase signal is applied, and tunneling layer (TL) interfacing with IGZO to prevent trapped carriers diffusing back to IGZO. [152]-[154]

The commonly used materials for CTL include SiN_x [155], HfO_2 [156], defect-engineered AlO_x [157],[158], Sm_2O_3 [159], etc. P. Ma designed and demonstrated a charge-trapping-flash (CTF) memory with IGZO channel in combination with an Alumina-based gate stack (Fig. 2. 21(a)). [158] In this memory device, CTL is the layer of Al_2O_3 deposited by ALD with O_3 oxidation source (O_3-Al_2O_3), while TL and BL are both the layer of Al_2O_3 deposited by ALD with H_2O oxidation source (H_2O-Al_2O_3). According to XPS data, O_3-Al_2O_3 shows a high density of defect states originating from carbon-related impurities, while H_2O-Al_2O_3 is filled with pure Al-O bonding with few defects. Defects in O_3-Al_2O_3 provide trap sites for carriers when a programming voltage pulse is applied to the gate terminal. Then TL and BL create a high potential barrier to prevent carriers from moving back to the channel and diffusing into gate electrodes, respectively (the three band diagrams in Fig. 2. 21(a) are unbiased, programmed, and erased states from left to right). Multilevel memory states (different V_{th} values) are realized by voltage pulses with different amplitudes and pulse width of 1s. Illumination combined with a negative pulse with an amplitude of 5 V is effective to erase the memory. Likewise, each memory state shows good retention up to 10^4 s.

A metal-oxide semiconductor with high V_O concentration is another promising option for CTL.[160],[161] In [161], D.-J. Yun fabricated a CTF memory TFT using IGZO as both the channel layer and CTL. As shown in Fig. 2. 21(b), the CTEF structure is composed of Al_2O_3-TL, IGZO-CTL, and Al_2O_3-BL. The TL has two layers of Al_2O_3 which provide extra protection for the wet-etching process. The authors have investigated the effects of the thickness of bi-layer Al_2O_3 TL and the deposition process of IGZO-CTL on the performance of the memory. It turns out that 1). the transistor with 5 nm/5 nm Al_2O_3 TL shows the optimized memory window in transfer curves, 2). the transistor with 30 nm IGZO CTL shows small variations under different pulse widths and best retention up to 10^4 s.

A floating gate (FG) is a conventional charge-trapping technology used in transistor memory. Researchers have succeeded in embedding metallic nanostructures in dielectrics of IGZO TFTs to realize FG-based charge trapping memory.[162]-[164] In [163], Y.-S. Park developed an IGZO TFT memory with polyelectrolytes doped with Au nanoparticles (AuNPs) as CTL. Each AuNP acts as a nano-floating gate to trap electrons when the TFT is biased with a positive voltage pulse. As shown in Fig. 2. 21(c), the TFT memory shows a large memory window ($\Delta V_{th} \geq 13$ V), small variations in both programmed states and erased states with 200 program/erase cycles, and good retention in two states up to 10^6 s.

Ferroelectric transistor memory: Ferroelectricity is widely applied in emerging memory devices recently. When the electric field is applied to a ferroelectric capacitor, the direction of polarization will be reversed. The transition between the upward or downward polarization inside the ferroelectric gate insulator controls the formation of the accumulation

layer in the channel layer, causing the shift of V_{th} of the TFT. [165] Varieties of ferroelectric materials have been successfully applied as the gate insulator in IGZO TFTs to realize memory function.

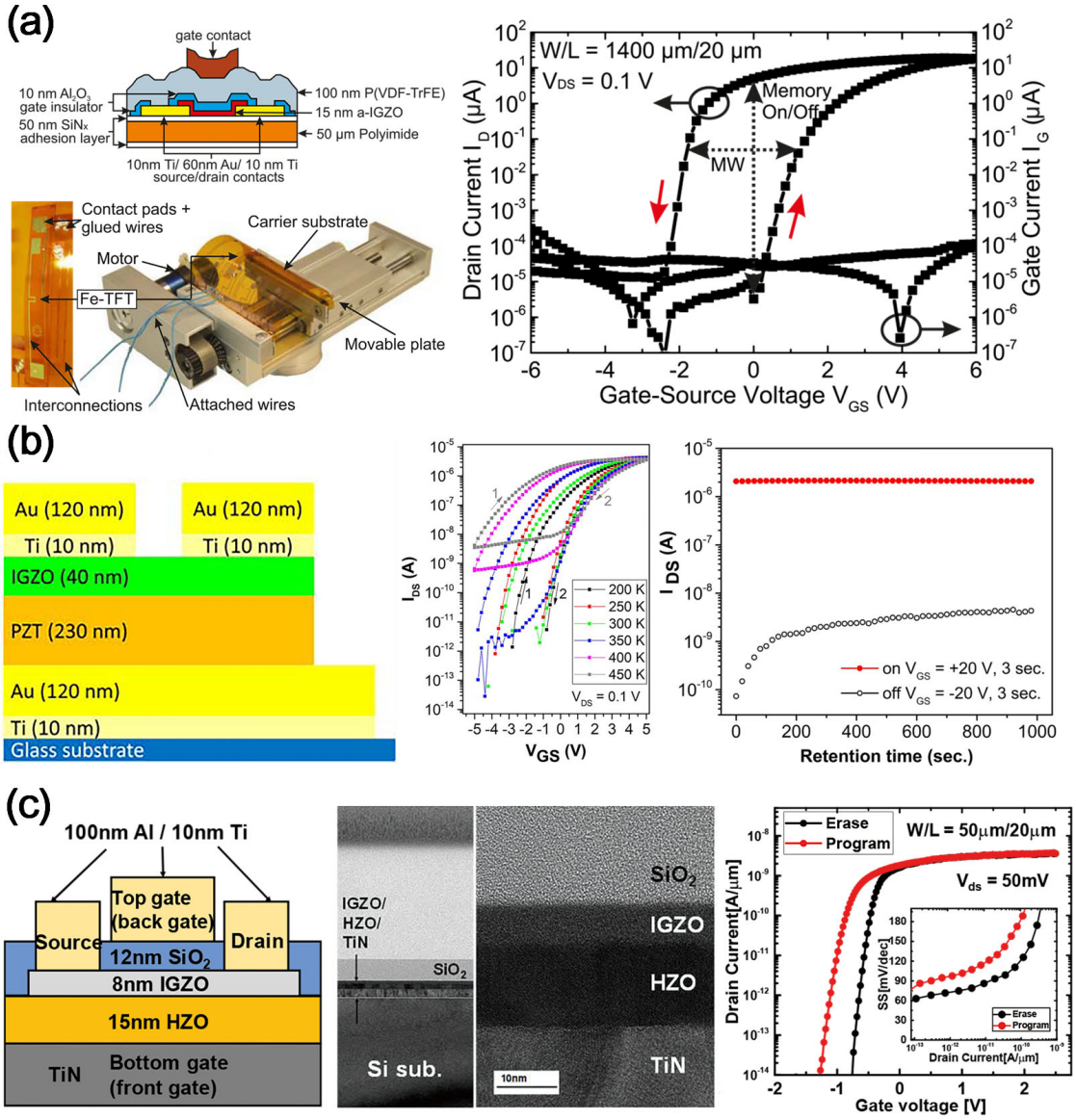


Fig. 2. 22 (a) Device schematic, bendable test system, and hysteresis window of the P(VDF-TrFE) based IGZO FeTFT. [167] (b) Device schematic, hysteresis window, and retention test of the PZT based IGZO FeTFT. [170] (c) Device schematic, cross section TEM image, and program/erase scheme of the HfZrO2 based IGZO FeTFT. [173]

IGZO TFTs in combination with ferroelectric P(VDF-TrFE) gate insulator are frequently reported to show large memory window and good retention. [166]-[169] The biggest advantage of the P(VDF-TrFE) based ferroelectric TFT (FeTFT) is its low-temperature process and mechanical bendability, which is promising for the flexible memory device. In [167], L. Petti presented a flexible IGZO FeTFT memory based on P(VDF-TrFE). As shown in Fig. 2. 22(a), the TFT is fabricated on a PI substrate with a staggered top-gate structure. P(VDF-TrFE) layer is synthesized by spin-coating followed by a 140 ℃-crystallization process. A layer of 10 nm Al_2O_3 is deposited to interface with IGZO, aiming to protect the channel from the corrosion of wet etchant and the diffusion of the Cu top gate. The TFT shows a large V_{th} shift window from 1.3 V under forward sweep to -1.9 V under reverse sweep. Bendable tests are carried out on the TFT with both tensile strain and compressive strain, which show strengthening and weakening effects on the polarization, respectively. The affected polarization strength will change the carrier concentration, resulting in the shift of V_{th}, variation of the maximum of I_D, and deteriorated S.S.

Perovskite-type materials are also popular in IGZO FeTFT memory since their ferroelectricity is not limited by the film thickness. [170],[171] In [170], C. Besleaga developed a staggered bottom-gate IGZO FeTFT based on lead zirconate titanate (PZT), as shown in Fig. 2. 22(b). The ferroelectric PZT layer is prepared in a solution-based method under 650 ℃. In the transfer curves of the TFT, the hysteresis window increases with the testing temperature, which could be attributed to the alleviated charge trapping issue between the PZT layer and the IGZO layer. On the other hand, the retention of the TFT maintains good up to 10^3 s. As an

alternative gate insulator in the IGZO FeTFT memory, the perovskite material shows high competence if the charge trapping issue could be solved further.

Recently, Hf-based binary oxide ($HfZrO_x$, $HfAlO_x$) appeals researchers a lot as an emerging ferroelectric material since it is highly compatible with the CMOS process. In addition, the crystallization temperature of Hf-based binary oxide (400~500 ℃) is relatively lower than that in the synthesis process of perovskite-type ferroelectric materials. By combining the IGZO channel and Hf-based oxides ferroelectric gate insulator, the FeTFT can show high performance with a large memory window, fast program/erase, and good retention. [172]-[175] In [173], F. Mo demonstrated a FeTFT memory in combination of IGZO channel and $HfZrO_2$ ferroelectric gate insulator with a double-gate structure (Fig. 2. 22(c)). The thicknesses of the IGZO layer and $HfZrO_2$ layer are 8 nm and 15 nm respectively. Plenty of experiments have shown that the $HfZrO_2$ layer shows the best remnant polarization (P_r) with thickness ranging from 10 to 20 nm. [176] Likewise, the ultrathin IGZO layer reduces the program and erase voltage amplitude. As shown in Fig. 2. 22(c), the program/erase voltage amplitude is 2.5 V/-3 V. $HfZrO_2$-based ferroelectric dielectric is a promising candidate for next-generation memory, which can be applied to the back-end-of-line (BEOL) process and promote the development of embedded memory in CMOS technology. However, precise thickness control is required to achieve perfect P_r, and the thermal budget of the film crystallization process needs to be further lowered.

Synaptic transistor: To break the bottleneck of Moore's Law basically, conventional von Neumann computing architecture needs to be revolutionized. Specifically, memory and

computation are two separate function blocks which are connected by bus lines in the von Neumann structure. When the central processing unit (CPU) is executing complex tasks sequentially, all related information which is stored in the memory blocks needs to be shuttled back and forth through bus lines. It has resulted in an upper limit for the computation speed. [177] On the other hand, the separate distribution of memory and computation units consumes a large area physically, which limits the density of function modules even with the extreme scalability of the state-of-art CMOS process. In contrast, the neural system in the human brain which contains billions of neurons and synapses connected shows a high-efficiency learning and memory mode. When a stimulus is applied to the membrane of the presynaptic cell, neurotransmitters will be released to the synapse cleft and bind with the channel of the postsynaptic cell to open the ion-gates and change the weight of synapse. This is defined as excitatory postsynaptic current (EPSC). Short-term memory (STM) plasticity of the synapse means that the weight change of synapse could be modulated by the stimulation pulse shape, including amplitude, pulse width, time interval between two successive pulses (paired-pulse facilitation, PPF), etc., which corresponds to the learning process of synapse. With the number of stimulation pulses increasing, the weight change of synapse becomes permanent, STM could be evolved to long-term memory (LTM) with a structural change of the synapse connection. [178]

In sum, memory and computation can be achieved concurrently in synapse, which largely improves the speed of operation execution and physically saves space. To emulate synapse, two-terminal devices like resistive random-access memory (ReRAM), phase change

memory (PCRAM), conductive-bridge memory (CBRAM), etc., and three-terminal devices, i.e., various field-effect transistors, are both extensively reported. The advantages of three-terminal artificial synapses over two-terminal ones lie in 1) the concurrence of signal transmission and weight change, 2) high uniformity and stability of the device, 3) feasibility of multi-gate operation to mimic spatiotemporal effects, 4) compatibility with a large variety of ion-conductive or ferroelectric dielectrics. [178] Literature reporting IGZO synaptic TFTs will be introduced in **section 5.1** in detail.

2.5 Summary

Inspired by the above literature, various methods will be adopted to improve the performance of IGZO TFTs. For instance, source/drain structure engineering will be attempted to realize the ideal contact characteristics for carriers to flow through. Likewise, the essence of doping in IGZO is to increase the carrier concentration and lower the potential barrier heights over CBM in IGZO. Therefore, passivation layer will be deposited by RF sputtering to cap IGZO, which aims to provide ion-bombardment energy to break M-O bonds inside IGZO and create more mobile carriers.

IGZO TFT can not only provide high driving current for the sensing, display, or memory pixel in an array structure, but also be directly applied as a memory or synaptic device. Thanks to its simple fabrication process, and compatibility with CMOS technology, it has high potential to substitute the traditional Flash memory becomes one of the mainstream next-generation embedded memory technologies.

Chapter 3. Study of contact characteristics and reliability of IGZO TFTs with different source/drain contacts

With the shrinkage of the device dimension, source/drain (S/D) contacts are more and more significant to affect the performance of IGZO TFTs. Specifically, S/D species with different work function can form different contact types with IGZO, i.e., ohmic contact and Schottky contact. An ideal ohmic contact is favored for the IGZO TFT, which means there is nearly no barriers for carriers to flow through the electrodes/channel interface. Also, low resistivity and high stability of the bulk of S/D species are both crucial to guarantee the small contact resistance and little influence on the IGZO layer. In this chapter, staggered bottom-gate IGZO TFTs with different device W/L ratios and S/D materials are fabricated on ITO-coated glass to systematically study the effects of different S/D electrodes on the contact characteristics and reliability of the TFT. In the end, a transparent IGZO TFT with an ultrathin-Ti/ITO S/D structure is developed with high performance.

3.1 Device fabrication and characterization

The fabrication processes of TFTs were all accomplished by vacuum-based techniques. ITO-coated glass was used as the transparent common bottom-gate. The Al_2O_3 dielectric layer with the thickness of 40 nm was grown by atomic layer deposition (ALD) at 250 ℃. The precursor and oxidant used for ALD were Trimethylaluminium (TMA, $Al(CH_3)_3$), and H_2O, respectively, which were pulsed into the reaction chamber cycle by cycle. The thickness of Al_2O_3 was set to 40 nm to compromise the good insulation and large capacitance per unit area. To form the active semiconductor and S/D contacts, the lift-off process was applied, in

which the patterns with different sizes and W/L ratios were defined by UV-photolithography in prior to the layer deposition. For the active semiconductor, an IGZO layer with the thickness of 45 nm was deposited by RF magnetron sputtering at room temperature with RF power of 100 W, and pure Ar gas flow of 50 sccm. For S/D contacts, various metals (i.e., Cu, Al, Ti, Ti/Au, etc.) were deposited by electron-beam (e-beam) evaporation at room temperature. All S/D electrodes had thickness of 200 nm. The thermal budget for the whole fabrication process was no higher than 300 °C. The 3D schematic of the device is shown in Fig. 3. 1(b). At the same time, a sandwich-like structure of Ti-Al_2O_3-ITO was fabricated to acquire the dielectric constant κ of the ALD-deposited Al_2O_3 layer, whose 3D schematic is shown in Fig. 3. 1(c). The overlap area S of the top electrode (Ti) and the bottom electrode (ITO) was 100×100 μm^2, and the thickness of the Al_2O_3 (i.e., the distance d between Ti and ITO) was 40 nm. The top view under electronic microscope demonstrating the TFTs with

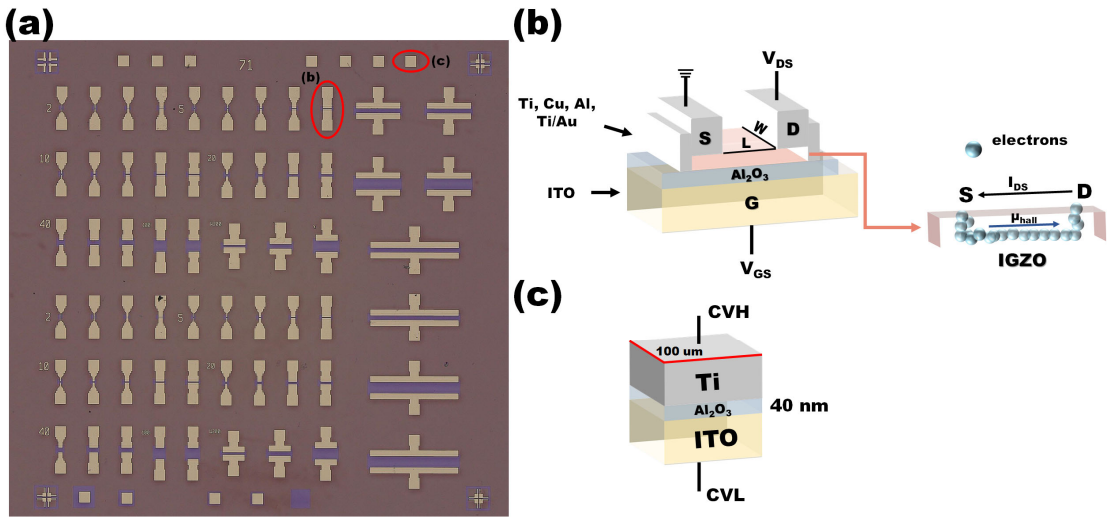


Fig. 3. 1 (a) Top view of the devices containing TFTs with different W/L ratios, and Al_2O_3-based capacitor structure. (b) 3D schematic of the as-fabricated IGZO TFT. (c) 3D schematic of the Ti-Al_2O_3-ITO sandwich structure with overlap area of 100×100 μm^2 and electrode distance of 40 nm.

different sizes and W/L ratios, and Al_2O_3-based capacitors is shown in Fig. 3. 1(a).

Keithley 4200 semiconductor characterization system (SCS) was employed to measure the electrical characteristics of the TFTs, including I_D vs. V_{GS} transfer curves, I_D vs. V_{DS} output curves, and capacitance-voltage (C-V) curves, etc. These curves collectively contributed to derive the basic FOMs of the TFT, including on/off ratio of I_D, carrier mobility (either μ_{FE} or μ_{sat}), threshold voltage (V_{th}), subthreshold slope/swing (S.S.), etc. Transmission line method (TLM) was utilized based on the original test data to extract the contact resistance, IGZO sheet resistance and transfer length (L_T) for the TFTs. In addition, different kinds of external stress scenarios (e.g., positive/negative bias stress (PBS/NBS), positive/negative bias illumination stress (PBIS/NBIS), positive/negative bias temperature stress (PBTS/NBTS) , etc.) were applied to the TFT with Ti S/D contacts to systematically study the origins of the TFT instabilities.

3.2 Electrical performance of TFTs with different S/D contacts

This section covers the comparisons of basic FOMs of TFTs with different S/D contacts, and the investigation of contact characteristics of TFTs with various S/D electrodes, and different dimensions.

3.2.1 Extraction and Comparison of basic FOMs for TFTs

The TFTs with W/L ratio of 40 μm/5 μm are picked for measurements of transfer curves and output curves, and comparisons of FOMs with different S/D contacts. The measurement is conducted in the dark and air environment at room temperature. For transfer curves, V_{GS} is sweeping from -7 V to 10 V; V_{DS} is fixed at 0.1 V and 5 V for the TFT working in the linear

and saturation region, respectively. For output curves, V_{DS} is sweeping from 0 to 7 V; V_{GS} is fixed at 5 V, 7 V, and 10 V, respectively. Fig. 3. 2 and Fig. 3. 3 show the transfer curves and output curves, respectively, of the TFTs with Ti, Cu, Al, and Ti/Au S/D contacts. FOMs TFTs are extracted based on the two curves.

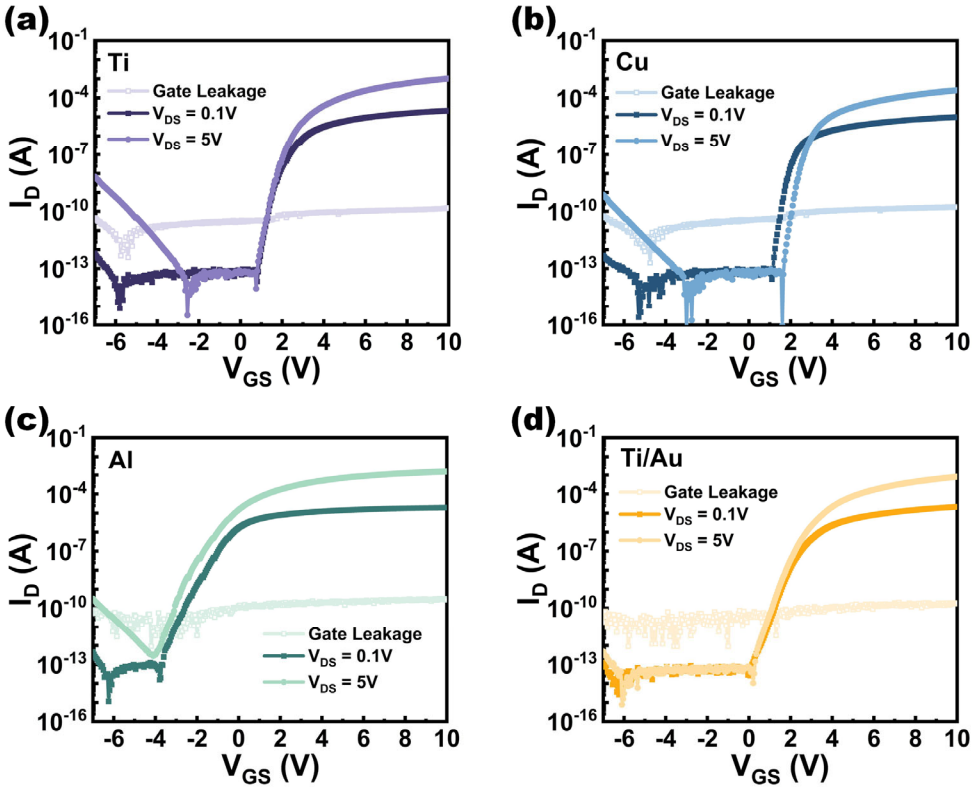


Fig. 3. 2 Transfer curves of TFTs with (a) Ti, (b) Cu, (c) Al, and (d) Ti/Au S/D

On/off ratio: From Fig. 3. 2(a)-(d), the on/off ratio of I_D for each TFT can be derived directly. In the linear region (V_{DS} = 0.1 V), the driving currents reach 21.60 μA, 9.953 μA, 19.62 μA, and 21.67 μA with the leakage currents of 69.27 fA, 69.57 fA, 81.35 fA, and 56.53 fA, deriving the on/off ratio to be 3.1×10^8, 1.4×10^8, 2.4×10^8, and 3.8×10^8 for the TFTs with Ti, Cu, Al and Ti/Au S/D contacts, respectively. Similarly, the on/off ratios of these four TFTs working in the saturation region (V_{DS} = 5 V) reach 1.7×10^{10}, 4.7×10^9, 5.5×10^9, 2.1×10^{10}, respectively. The Al-based TFT shows highest I_D at large V_{GS} and V_{DS}

as shown in Fig. 3. 3, however, its leakage current increases as well with the increase of V_{DS}, which causes smaller on/off ratio compared with that of Ti- and Ti/Au-based TFTs. The relatively limited on/off ratios for Al- and Cu-based TFTs result from their tendency to diffuse into IGZO. The diffusion would increase the density of acceptor-like trap states below the CBM of IGZO to limit the transport of carriers.

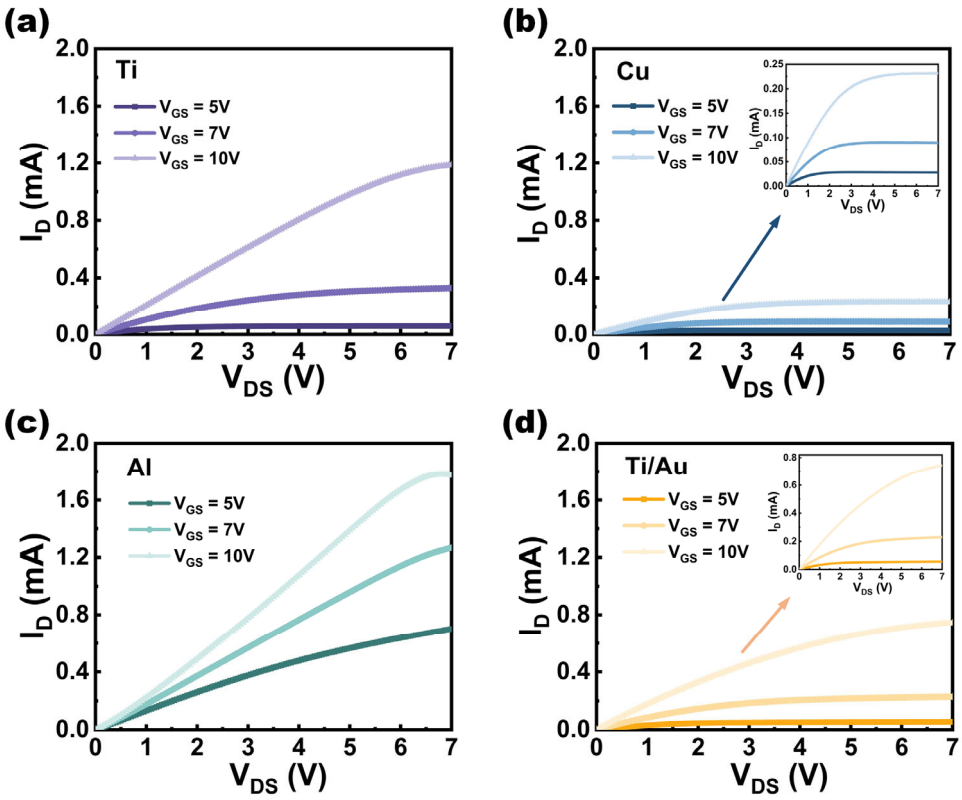


Fig. 3. 3 Output curves of TFTs with (a) Ti, (b) Cu, (c) Al, and (d) Ti/Au S/D contacts.

S.S.: S.S. of the TFT is defined as the increment of V_{GS} with a one-order increase of I_D at the subthreshold region. In this work, all the S.S. values are extracted from where I_D equals to 10^{-10} A, which turn out to be 156 mV/dec, 160 mV/dec, 463 mV/dec, and 360 mV/dec for the TFTs with Ti, Cu, Al, and Ti/Au S/D contacts, respectively. The Al-based TFT shows the largest S.S., indicating the most inferior switching speed.

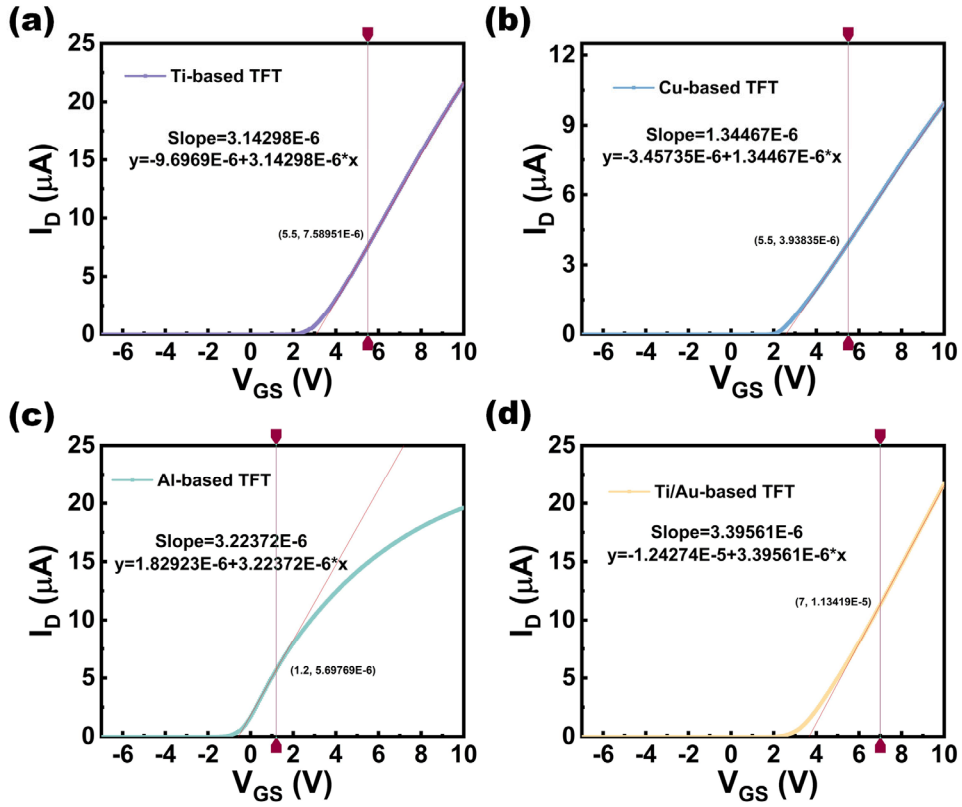


Fig. 3. 4 Linear transfer curves of TFTs with (a) Ti, (b) Cu, (c) Al, and (d) Ti/Au S/D contacts.

V_{on} and V_{th}: The turn-on voltage (V_{on}) is determined from the transfer curves at which I_D starts to increase. As shown in Fig. 3. 2, these four TFTs show V_{on} of 0.8 V, 1.1 V, -3.75 V, and 0.05 V, respectively. In addition, V_{th} is extracted from the transfer curve with I_D in linear scale as shown in Fig. 3. 4. The intercept of the tangent line of the transfer curve at the axis of V_{GS} is the right V_{th} of the TFT, which turns out to be 3.09 V, 2.57 V, -0.57 V, and 3.66 V for the four TFTs. Thereinto, the Al-based TFT shows negative V_{th}, which means the TFT is working at the depletion-mode.

μ_{FE}: To derive the field effect mobility in the channel layer, some parameters need to be derived first according to Equation (2.9). Capacitance per unit area of the gate oxide C_{ox} is measured with the structure as shown in Fig. 3. 1(c). The capacitance value of 40-nm ALD-deposited Al_2O_3 is 16.14 pF. Capacitance of the dielectric is usually calculated with Equation

(3.1),

$$C_{dielecrtic} = \frac{\varepsilon_0 \kappa_{ox} S}{t_{ox}} \quad (3.1)$$

where ε_0 is the permittivity of vacuum, which is $8.85e^{-12}$ F/m, κ_{ox} is the dielectric constant of the Al_2O_3 layer, S is the overlap area, which is 10^4 μm^2, and t_{ox} is the thickness of the Al_2O_3 layer, which is 40 nm. By combining Equations (2.5) and (3.1), the κ_{ox} and C_{ox} of the Al_2O_3 layer are derived to be 7.3 and 1.614×10^{-7} F/cm^2, respectively. Another important parameter is the transconductance g_m, which is the derivative of I_D over V_{GS}. The methodology to extract g_m is to draw the tangent line in the transfer curve with I_D in linear scale. The slope of the tangent line is right the g_m, which is derived to be 3.14×10^{-6} S, 1.34×10^{-6} S, 3.22×10^{-6} S, and 3.40×10^{-6} S, respectively, as shown in Fig. 3. 4. Based on Equation (2.9), μ_{FE} of these four TFTs are calculated to be 9.72, 4.15, 9.98, and 10.53 cm^2/Vs, respectively. To examine the uniformity of the as-fabricated TFT, transfer curves of 10 devices with the same dimension in one substrate were measured. It turned out that the coefficient of variations for V_{th}, S.S., and μ_{FE} were as small as 4.3%, 7.1%, and 6.6%, respectively.

Table 3. 1 Summary of FOMs of TFTs with different S/D contacts

S/D species	On/off ratio ($\times10^8$)		S.S.	V_{on} (V)	V_{th} (V)	μ_{FE}
	Linear	Saturation	(mV/dec)			(cm^2/Vs)
Ti	3.1	170	156	0.8	3.09	9.72
Cu	1.4	47	160	1.1	2.57	4.15
Al	2.4	55	463	-3.75	-0.57	9.98
Ti/Au	3.8	210	360	0.05	3.66	10.53

All FOMs of these four TFT are summarized in Table 3. 1 above for comparison.

3.2.2 Analysis of contact characteristics based on TLM

Contact characteristics are significant for TFTs which are decided by the contact type between S/D electrodes and the channel layer. The contact type can be mainly categorized into ohmic contact and Schottky contact. [117] An ohmic contact is achieved when the work function of S/D electrodes ($\Phi_{S,D}$) is close to the electron affinity of IGZO (ψ_{IGZO}). There is nearly no Schottky barrier for the electron transport between S/D electrodes and IGZO. In contrast, Schottky contact is formed when $\Phi_{S,D}$ is much larger than ψ_{IGZO}, producing high Schottky barrier for the electron transport. To quantify the contact characteristics, transmission line method (TLM) is applied which divides the total resistance of the conduction path in the TFT into the channel resistance and contact resistance. In detail, this methodology is described in Equation (3.2) below, [117]

$$R_{total} = \frac{V_{DS}}{I_D} = \frac{L}{W} R_{IGZO} + 2R_C \quad (3.2)$$

where L is channel length, W is channel width, R_{IGZO}/W is the sheet resistance of IGZO, $2R_C$ is the S/D contact resistance. R_{total} is the y-axis variable, which is derived from the ratio of V_{DS} over I_D; L is the x-axis variable. By plotting the relationship of R_{total} versus L, the channel sheet resistance and S/D contact resistance can be extracted from the slope and the intercept at y-axis, respectively. To evaluate the contact characteristics of each TFT, channel width W is fixed at 40 μm, with five different channel lengths (L = 2, 5, 10, 20, 40 μm). Fig. 3. 5 depicts the R_{total} vs. L curves of TFTs at V_{GS} = 10 V with different S/D contacts. Contact resistance $2R_C$ for each TFT is extracted to be 3148.6, 6578.1, 5500.3, and 225.5 Ω,

respectively. Meanwhile, IGZO sheet resistance R_{IGZO}/W for each TFT is extracted to be 1877.4, 1831.9, 3743.9, and 1471.1 Ω/μm, respectively. The Ti-based (either pure Ti or Ti/Au) S/D electrodes show the best contact with IGZO. It could be attributed to two reasons: 1). Φ_{Ti} is around 4.3 eV, and ψ_{IGZO} is around 4.5 eV. There is a negligible barrier height for the electron transport between Ti and IGZO, which proves the existence of nearly ohmic contact between Ti and IGZO. [179] 2). The enthalpy of formation (ΔH) of the TiO_x species is lower than that of the ZnO, GaO_x, and InO_x inside IGZO. [180] The active Ti metal interacts with IGZO, forming a contact region with higher carrier concentration. [179] Al also tends to oxidize and decompose oxygen from IGZO due to the low ΔH of the AlO_x species. However, the formed AlO_x would become a new barrier for the electron transport between Al and IGZO, which result in a larger contact resistance in Al-based TFT.

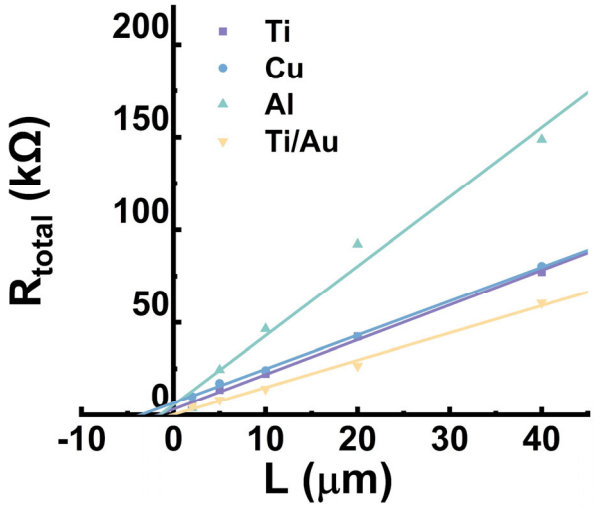


Fig. 3. 5 R_{total} vs. L curves based on TLM for TFT with different S/D contacts.

Transfer length (L_T) is another parameter for S/D contact with IGZO. It is defined as the distance between the contact edge and a point in the S/D, in which most of the I_D flows between S/D and IGZO. Good contacts always have small L_T which is close to or smaller

than 1 μm. When $L > L_T$, L_T can be approximated by the ratio of R_C over R_{IGZO}/W. [181] Since the smallest channel length among these TFTs is 2 μm, we could derive L_T for each TFT directly using the approximation, which turns out to be 0.84, 1.79, 0.73, and 0.077 μm, respectively. All contact characteristics for each TFT are summarized in Table 3. 2. In conclusion, the TFT with Ti/Au S/D contacts shows the best contact characteristics, which also shows the highest on/off ratio and the largest μ_{FE} as demonstrated in Table 3. 1. It proves that the contact characteristics between S/D electrodes and IGZO directly affect the switching performance of the IGZO TFT.

Table 3. 2 Summary of contact characteristics of TFTs with different S/D contacts

S/D species	$2R_C$ (Ω)	R_{IGZO}/W (Ω/μm)	L_T (μm)
Ti	3148.6	1877.4	0.84
Cu	6578.1	1831.9	1.79
Al	5500.3	3743.9	0.73
Ti/Au	225.5	1471.1	0.077

3.3 Reliability of TFTs under different external stresses

Reliability of the TFT is of great importance which directly influences the stability of brightness, resolution, and lifetime of active-matrix pixels in the display panels. Common external stresses include voltage bias, illumination, heat etc. In this section, the Ti-based TFTs with different W/L values (40 μm/2 μm, 800 μm/40 μm) are chosen for a study of reliability

under different external stresses.

3.3.1 Positive/negative bias stress (PBS/NBS)

Gate bias is necessary to modulate the conductance of the channel in the TFT. However, long-term bias of gate voltage could induce instabilities of the TFT behaviors. To test the reliability under PBS/NBS, a gate bias with fixed value of 7 V/-7 V is applied to the TFT for 3600 s. The transfer curve of each TFT is sampled with a time step in logarithm scale. The trends of V_{th} shift (ΔV_{th}) and μ_{FE} with the stress time are depicted in Fig. 3. 6(a) and (b), respectively. The TFT with 40/2 μm W/L ratio shows an increment of V_{th} from 2.29 V to 5.42 V under 3600 s PBS (ΔV_{th} = 2.37 V), and a reduction of V_{th} from 3.06 V to 0.43 V under 3600 s NBS (ΔV_{th} = -2.63 V). In comparison, the TFT with 800/40 μm W/L ratio shows an increment of V_{th} from 2.49 V to 5.66 V under 3600 s PBS (ΔV_{th} = 3.17 V), and nearly unchanged V_{th} from 3.78 V to 4.1 V under 3600 s NBS (ΔV_{th} = 0.32 V). ΔV_{th} under PBS/NBS is well fitted by the simple power-law model as a function of stress time (t_{stress}) (Equation (3.3)),

$$\Delta V_{th} = a + bt_{stress}{}^{c} \tag{3.3}$$

where a, b and c are parameters related with the gate bias level and TFT dimensions. Likewise, μ_{FE} of the TFTs demonstrates a negligible alteration with stress time under all stress schemes.

Band diagrams of the TFT under PBS and NBS are shown in Fig. 3. 6(c) and (d), respectively. For the TFT without passivation layer, the instabilities under PBS and NBS mainly come from two aspects: 1). Charge trapping/release at the dielectric/semiconductor

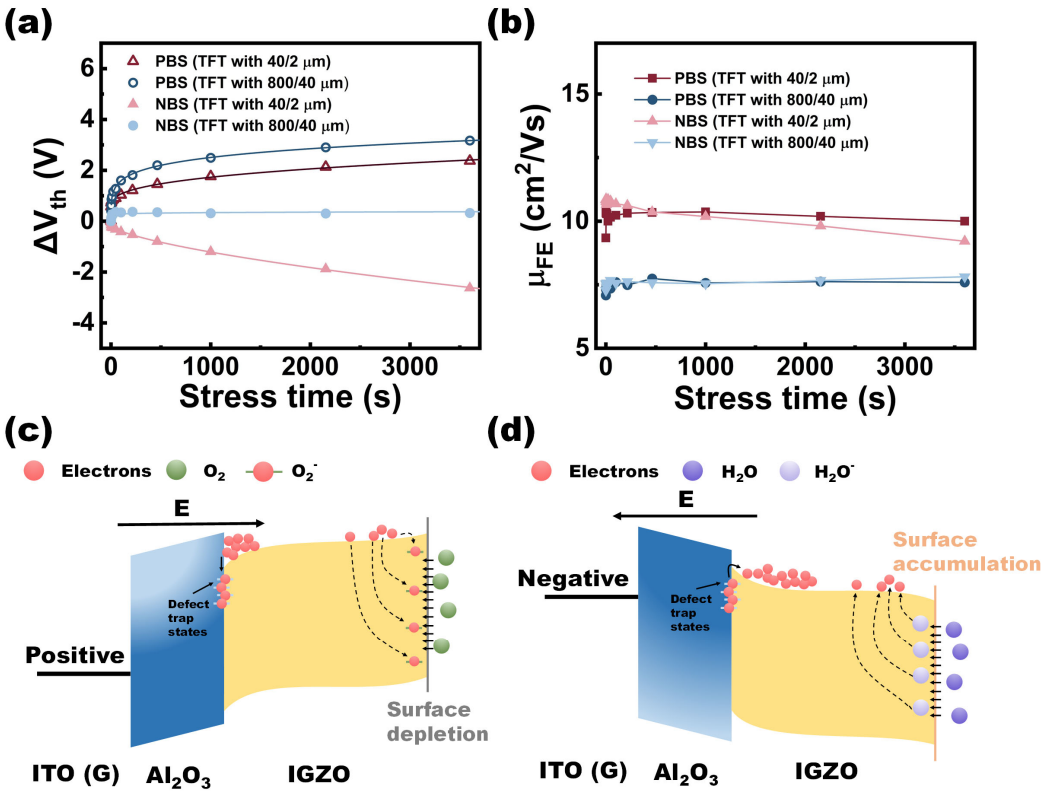


Fig. 3. 6 (a) V_{th} shift (ΔV_{th}) vs. stress time under PBS and NBS for 3600 s, respectively. (b) μ_{FE} vs. stress time under PBS and NBS for 3600 s, respectively. (c) Band diagram of the TFT under PBS. (d) Band diagram of the TFT under NBS.

interface, which is determined by the density of defect states in the bulk of the dielectric and the dielectric/semiconductor interface. [182] A larger ΔV_{th} of the TFT with large channel size (800/40 μm) can be attributed to more serious charge-trapping effect with the larger dielectric/channel interfacing area. When positive bias is applied, partial carriers would be trapped at the interfacial defect states and the bulk of dielectric, resulting in the positive shift of V_{th}. When negative bias is applied, those trapped carriers would be released, resulting in the negative shift of V_{th}. 2). The absorption of gases in the ambient environment into the IGZO layer under the gate bias. When a positive gate bias is applied, O_2 in the air is absorbed into the channel and becomes an acceptor-like state which captures electron in the channel:

$O_2 + e^- = O_2^-$. When a negative gate bias is applied, H_2O in the air is absorbed into the channel and becomes a donor-like state which releases electron into the channel: $H_2O - e^- = H_2O^+$. [183],[184] Increment or reduction of the electron concentration results in the negative or positive shift of the V_{th}. These molecules penetration are partially reversible with annealing process. Considering the local climate in Singapore, humidity in the test laboratory is maintained high which is at around 70%, causing obvious negative V_{th} shift under NBS for the TFT with 40/2 μm W/L ratio. As for the TFT with large size (800/40 μm), the penetration of H_2O gas shows negligible impact on the carrier concentration in the whole bulk of IGZO. On the other hand, stable μ_{FE} under PBS/NBS indicates the charge trapping/release induced by PBS/NBS is temporary, which can be recovered with a short relaxation time. [184]

3.3.2 Positive/negative bias illumination stress (PBIS/NBIS)

In the display technology, light illumination is inevitable for the TFT, which causes serious instability combined with the gate bias. To evaluate the reliability under PBIS/NBIS, illumination with a focused halogen light (light intensity is 8 W/m^2) and gate bias with a fixed value of 7 V/-7 V are applied concurrently for 3600 s to the chosen TFTs. The transfer curve of each TFT is sampled with a time step in logarithm scale. The trends of ΔV_{th} and μ_{FE} with the stress time are depicted in Fig. 3. 7(a) and (b), respectively. The TFT with W/L ratio of 40/2 μm shows an increment of V_{th} from 1.67 V to 2.97 V under 3600 s PBIS (ΔV_{th} = 1.3 V), and a reduction of V_{th} from 2.97 V to -3.61 V under 3600 s NBIS (ΔV_{th} = -6.58 V). In contrast, the TFT with W/L ratio of 800/40 μm shows an increment of V_{th} from 3.56 V to 5.28 V under 3600 s PBIS (ΔV_{th} = 1.72 V), and a reduction of V_{th} from 5.08 V to -1.82 V under

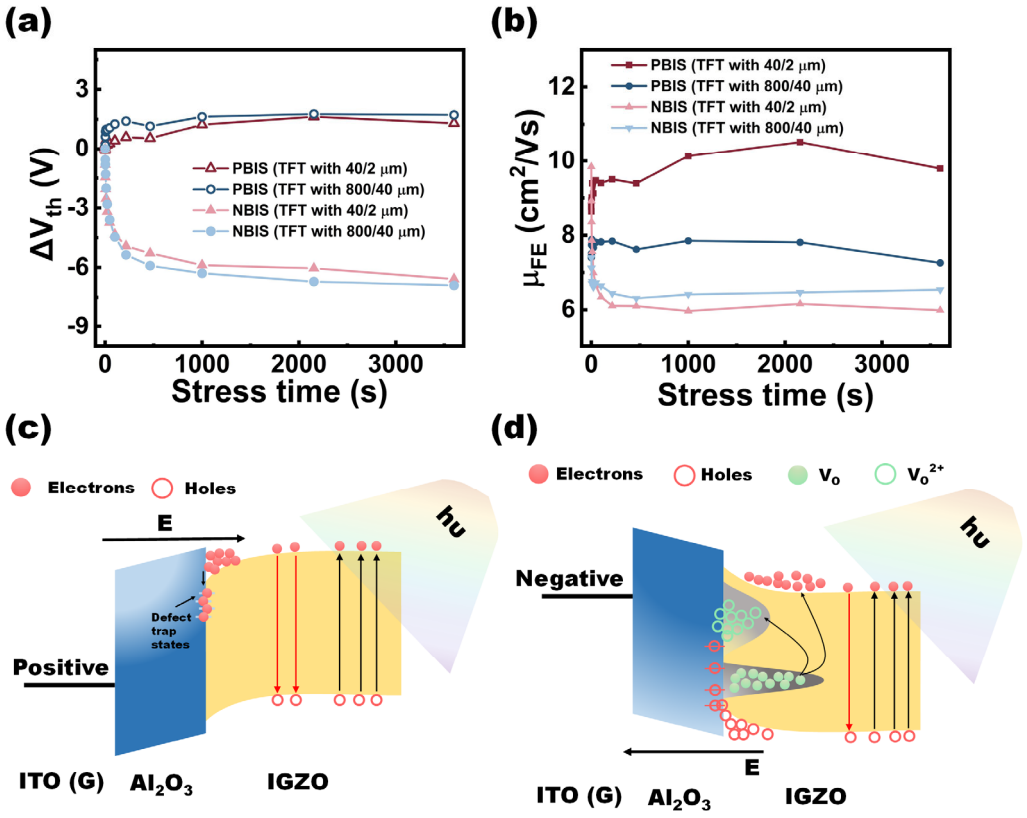


Fig. 3. 7 (a) V_{th} shift (ΔV_{th}) vs. stress time under PBIS and NBIS for 3600 s, respectively. (b) μ_{FE} vs. stress time under PBIS and NBIS for 3600 s, respectively. (c) Band diagram of the TFT under PBIS. (d) Band diagram of the TFT under NBIS.

3600 s NBIS (ΔV_{th} = -6.9 V). In addition, μ_{FE} is stable under PBIS for the two TFTs; while it decreases from 9.84 to 5.99 cm^2/Vs, and from 7.40 to 6.54 cm^2/Vs under NBIS for the TFT with W/L ratio of 40/2 μm and 800/40 μm, respectively. To explain the different behaviors of V_{th} shift and μ_{FE} under different stress schemes, band diagrams of the TFT under PBIS and NBIS are shown in Fig. 3. 7(c) and (d), respectively.

The spectrum of halogen light is continuous from UV to IR. Thus, activities of charges inside IGZO excited by halogen illumination are complicated. When the TFT is biased by PBIS, charge trapping effect still exists under the positive gate bias; while light illumination

excites electrons from the VB to the CB in IGZO and generate electron-hole pairs. The polarity and amount of ΔV_{th} is decided by the predominance between the charge-trapping effect and the band-to-band excitation of electrons. From Fig. 3. 6(a) and Fig. 3. 7(a), ΔV_{th} under PBIS is still positive but smaller compared with that under PBS, which indicates the charge-trapping effect induced by positive gate bias is predominant, and the compensation of carrier concentration contributed by photon-generated electron-hole pairs is limited. The limited density of photon-generated electron-hole pairs mainly results from the lack of hole trapping centers. Under the positive gate bias, the band of IGZO is bending downwards as shown in Fig. 3. 7(c), which confines the holes in the VB to recombine with electrons rapidly. From Fig. 3. 7(b), μ_{FE} under PBIS is stable for the TFTs with different channel size. When the TFT is biased by NBIS, charge activities inside IGZO become complex. On the one hand, both the two TFTs show tremendous negative ΔV_{th} as shown in Fig. 3. 7(a). The large ΔV_{th} of the TFTs could be originated from the following aspects (Fig. 3. 7(d)): 1). Band-to-band excitation of electrons is induced by the near-UV spectrum with high photon energy ($h\upsilon >$ 3.2eV). Under the negative bias, photon-generated holes at the VB are attracted to the dielectric and get captured by defect states near the VB, which decreases the recombination rate of electrons and holes. 2). The recombination of electrons and holes would release energy, which promotes the break of weak bonds inside IGZO, forming neutral V_O states above the VB. These V_O states compose a hole trapping center. With the injected photon energy from the halogen light, V_O states can be photon-ionized to V_O^{2+} and release electrons to the CB of IGZO. These electrons would not recombine with holes fast since the photon-generated holes are trapped in the hole trapping center with the aid of the negative gate bias. [132],[184],[185]

Consequently, NBIS applied to the TFT could induce large amounts of photo-generated electrons and refrain them in the CB of IGZO for a long term to change the carrier concentration. On the other hand, μ_{FE} of the two TFTs both show a trend of deterioration with the stress time. It could be caused by the greatly increased carrier concentration in the channel layer, which makes the predominant resistance along the conduction path change from the channel sheet resistance to the contact resistance. For the TFT with small channel size, the influence of contact resistance is more prominent, which is the reason for the larger degradation of μ_{FE} of the TFT with W/L ratio of 40/2 μm than that of the TFT with W/L ratio of 800/40 μm. [186]

3.3.3 Positive/negative bias temperature stress (PBTS/NBTS)

The heat is always produced during the operation of TFT-based circuits. Thus, the impact of temperature in combination with gate bias on the TFT behaviors is investigated. The substrate of the probe station is heated up to 85 ℃ for I-V curve measurement. Fig. 3. 8(a) and (b) show the transfer curves of the TFT with W/L ratio of 40/2 μm under PBTS and NBTS, respectively. The gate bias for PBTS/NBTS is still set to 7 V/-7 V. The legend ‘pristine’ refers to the I-V curve of the TFT tested at room temperature. Once the TFT is put on the heated substrate, the I-V curve shows an immediate negative shift and an obvious stretch-out behavior at the subthreshold region. The phenomenon can be caused by the holes generated by high temperature. When the gate voltage is lower than the V_{th} of the TFT, the thermal-generated holes are driven by the transverse electric field between S/D electrodes and accumulate at the source terminal, which effectively lowers the barrier height between the

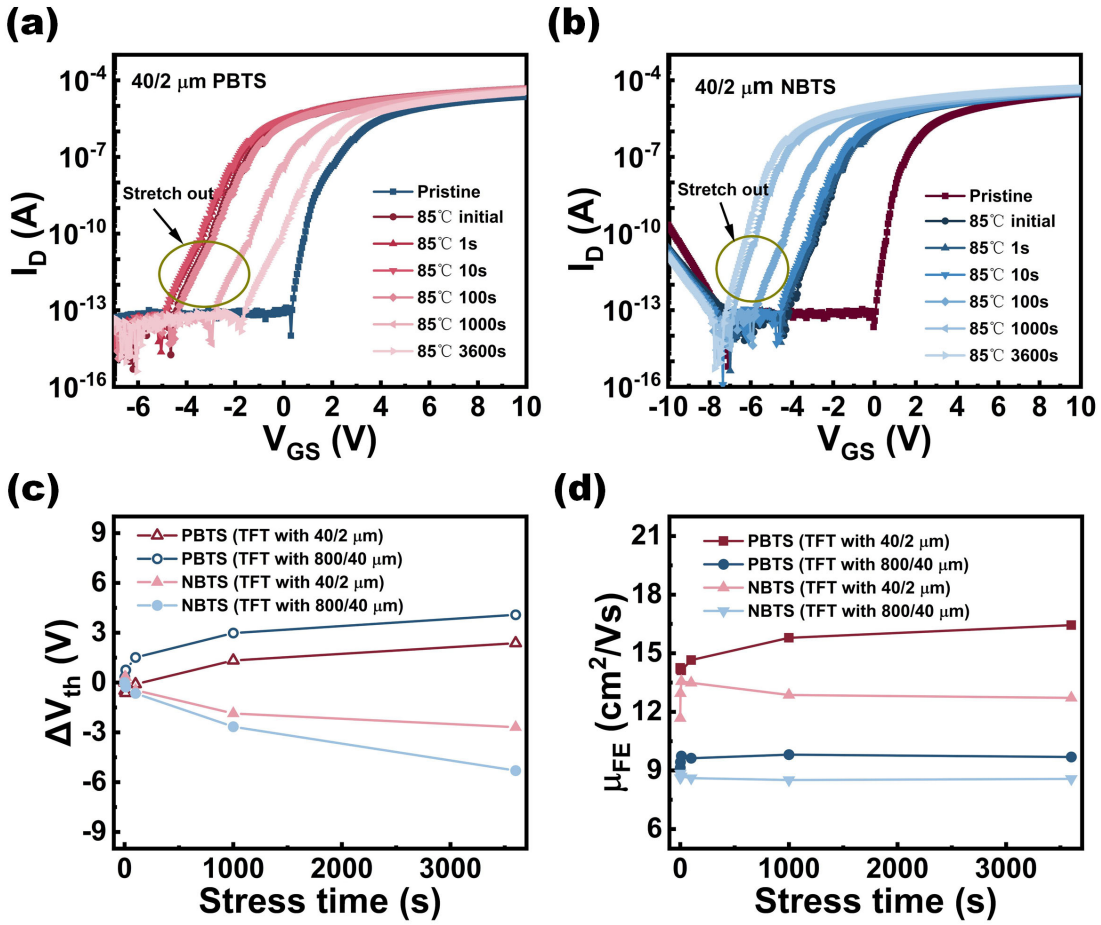


Fig. 3. 8 (a) Transfer curves of the TFT under PBTS for 3600 s. (b) Transfer curves of the TFT under NBTS for 3600 s. (c) V_{th} shift (ΔV_{th}) vs. stress time under PBTS and NBTS for 3600 s, respectively. (d) μ_{FE} vs. stress time under PBTS and NBTS for 3600 s, respectively.

source electrode and the IGZO layer. The lowered barrier height allows electrons to transport between S/D contacts and IGZO, increasing I_D at low V_{GS}. [187]

Fig. 3. 8(c) shows the curve of ΔV_{th} versus stress time of the two TFTs under PBTS and NBTS, which is 3.35 V, 4.08 V, -2.69 V, and -5.3 V for the TFT with 40/2 μm channel under PBTS, 800/40 μm channel under PBTS, 40/2 μm channel under NBTS, and 800/40 μm channel under NBTS, respectively. Compared with the ΔV_{th} under PBS and NBS (Fig. 3. 6(a)), the high temperature has enlarged the shift of V_{th} with the same direction under each stress scheme. When the TFT is applied by PBTS, the elevated temperature has enhanced the

charge trapping effect at the dielectric/channel interface, resulting in larger ΔV_{th}. [188] When the TFT is applied by NBTS, the elevated temperature provides the activation energy of holes generation from defect states. These thermal-generated holes are attracted to and trapped in the bulk of the dielectric and the dielectric/channel interface by the negative gate bias, forming an additional electric field to attract more electrons. Thus, there appears to be a larger negative ΔV_{th} with higher carrier concentration under NBTS. [189] Besides, Fig. 3. 8(d) shows the trend of μ_{FE} with stress time, which is stable with negligible fluctuations.

3.4 High-performance transparent IGZO TFT with ultra-thin Ti S/D contacts

The transparent IGZO TFT is an indispensable element in the emerging transparent display technology. The most popular material for the transparent electrode is ITO, which accommodates low resistivity and high transparency at the same time. However, as a candidate for S/D electrode, the contact between ITO and IGZO is always not ideal, which deteriorates the performance of the TFT. Based on the basic study conducted in the above-sections, an ultra-thin Ti layer with the thickness of 10 nm is inserted between ITO and IGZO,

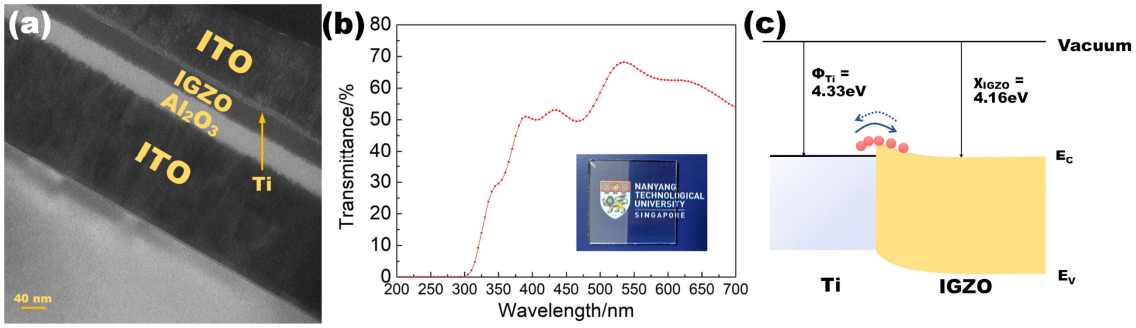


Fig. 3. 9 (a) TEM image of the cross section of the device B. (b) Transmittance test of the device within visible light range. Inset is the picture of practical device B. (c) Band structure of the Ti/IGZO contact. χ_{IGZO} is electron affinity of IGZO; Φ_{Ti} is work function of Ti.

aiming to provide a good ohmic contact. The fabrication process is nearly the same with the one introduced in **section 3.1**, except for the deposition of S/D electrodes. 200 nm ITO is deposited by RF sputtering as S/D contacts for reference device A; while 10nm Ti and 200 nm ITO are deposited by DC sputtering and RF sputtering successively as S/D contacts for device B. In addition, to promote the reduced reaction between Ti and IGZO, the as-fabricated devices are annealed in 300 ℃ N_2 environment for 10 min.

Fig. 3. 9(a) shows the cross-section TEM image of the device B. Fig. 3. 9(b) shows the optical transmittance test result of the device with an inset of the practical device picture. The high optical transmittance (~ 70%) of the device B with an insertion of the ultra-thin Ti layer

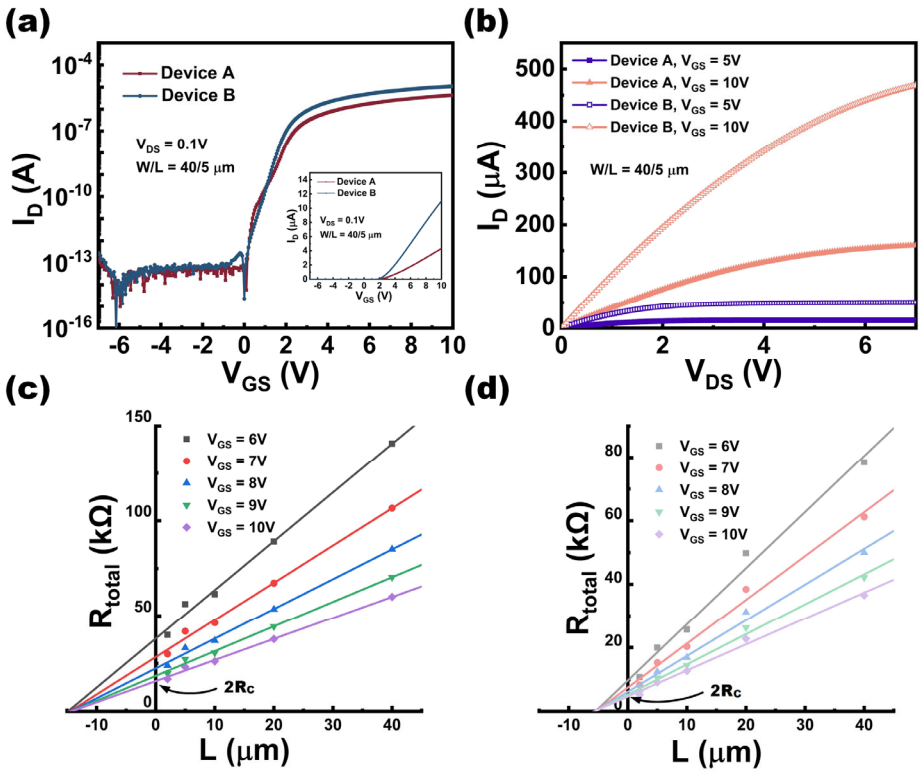


Fig. 3. 10 (a) Transfer curves of the device A and device B at V_{DS} = 0.1 V. Inset depicts the transfer curves with I_D in linear scale. (b) Output curves of the device A and device B at V_{GS} = 5 V and 10 V, respectively. (c) R_{total} vs. L curves based on TLM for device A. (d) R_{total} vs. L curves based on TLM for device B.

in the S/D region is attributed to the reduced reaction between Ti and IGZO, which turns the Ti layer into a TiO_x layer.

To investigate the influence of the ultra-thin Ti S/D contacts on the performance of the transparent TFT, the transfer curves and output curves of device A and B with W/L ratio of 40/5 μm are measured and compared as shown in Fig. 3. 10(a) and (b). To get the transfer curve of the TFT working in the linear region, V_{GS} is sweeping from -7 V to 10 V, and V_{DS} is fixed at 0.1 V. To get the output curve of the TFT, V_{DS} is sweeping from 0 to 7 V, and V_{GS} is fixed at 5 V and 10 V, respectively. Furthermore, contact characteristics of the two devices are derived from Fig. 3. 10(c) and (d), which are sampled at V_{GS} = 6, 7, 8, 9, and 10 V, respectively. Based on the methodologies introduced in **section 3.2**, FOMs of device A and device B are derived and summarized in Table 3. 3 below. Both $2R_C$ and R_{IGZO}/C are extracted at V_{GS} = 10 V.

By inserting the ultra-thin Ti layer as S/D contacts, the contact characteristics of the TFT are improved with over three times reduction of the contact resistance. At the same time, μ_{FE} of the TFT shows a nearly three-times increment from 4.75 cm^2/Vs to 12.1 cm^2/Vs; V_{th} of the TFT reduces from 3.11 V to 2.8 V; and I_D on/off ratio has a two-fold enlargement from 7×10^7 to 1.54×10^8. On the one hand, as shown in Fig. 3. 9(c), Ti has work function close to the electron affinity of IGZO. An ideal ohmic contact can be formed for electrons to flow through IGZO and Ti with a negligible barrier. On the other hand, Ti can react with IGZO to break those weak In-O bonds near the source/drain contacts regions. The reaction would increase the oxygen vacancies, i.e., carrier concentration in IGZO channel, and reduce the effective channel length of IGZO as well.

Table 3. 3 Summary of FOMs for device A and device B

Device	On/off ratio	S.S. (mV/dec)	V_{th} (V)	μ_{FE} (cm^2/Vs)	$2R_C$ (kΩ)	R_{IGZO}/W (kΩ/μm)
A	7×10^7	153	3.11	4.75	15.74	1.1
B	1.54×10^8	292	2.80	12.10	4.64	0.82

Instabilities of devices A and B with W/L ratio of 40/2 μm induced by PBS, NBS, PBIS and NBIS are tested and compared. The stress scenarios are totally the same as the ones applied in **section 3.3**. Fig. 3. 11 shows the curves of ΔV_{th} and μ_{FE} versus stress time of device A and B under PBS, NBS, PBIS and NBIS. Under PBS, device A and B shows a positive shift of V_{th} with ΔV_{th} of 0.6 V and 0.54 V, respectively. Under NBS, device A and B shows a negative shift of V_{th} with ΔV_{th} of -0.44 V and -0.18 V, respectively. Under PBIS, device A and B shows a positive shift of V_{th} with ΔV_{th} of 0.22 V and 0.4 V, respectively. Under NBIS, device A and B shows a negative shift of V_{th} with ΔV_{th} of -4.71 V and -4.23 V, respectively.

μ_{FE} under different stress schemes all show good stability for the two devices. Apparently, PBS, NBS and PBIS have induced much smaller shift of V_{th} for both device A and B compared with the TFT with the pure Ti S/D contacts. Still, obvious instability under NBIS is observed in these two devices, while smaller ΔV_{th} is achieved compared with the TFT with the pure Ti S/D contacts.

One assumption to explain the largely enhanced PBS, NBS, and PBIS reliability, and slightly improved NBIS reliability for the TFT is that pure Ti S/D contacts provide active

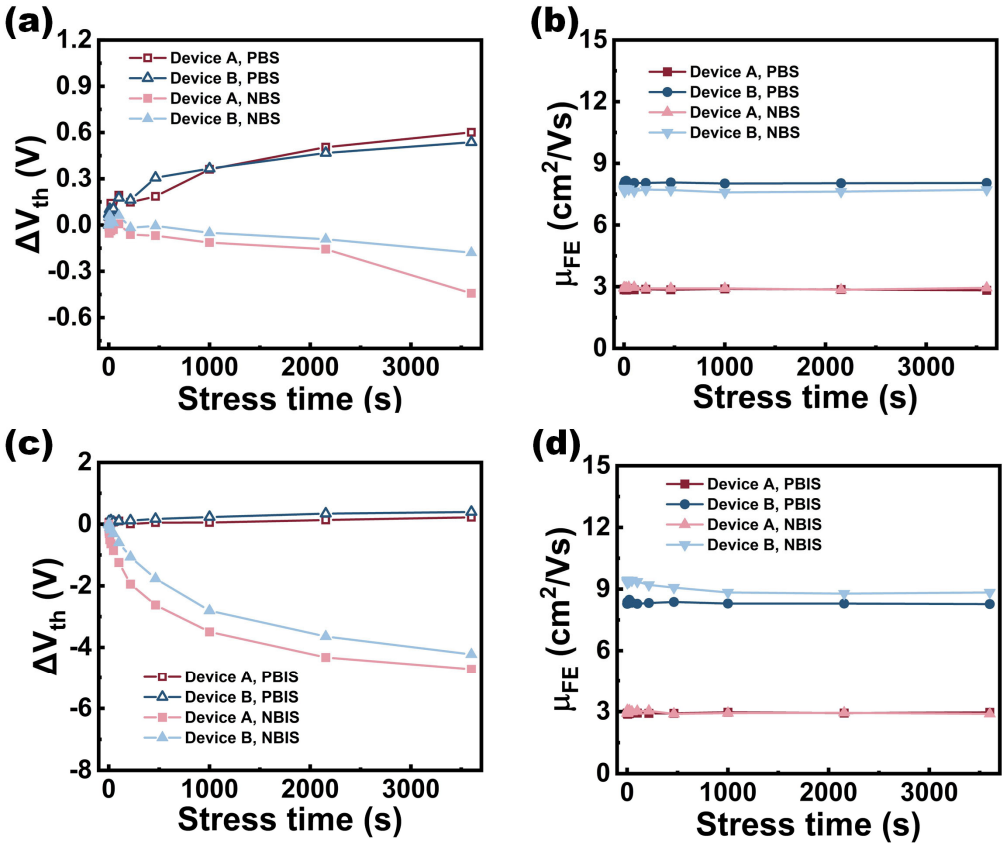


Fig. 3. 11 (a) ΔV_{th} vs. stress time under PBS and NBS for 3600 s, respectively. (b) μ_{FE} vs. stress time under PBS and NBS for 3600 s, respectively. (c) ΔV_{th} vs. stress time under PBIS and NBIS for 3600 s, respectively. (d) μ_{FE} vs. stress time under PBIS and NBIS for 3600 s, respectively.

reduced reactions with IGZO, producing excess V_O in IGZO. In comparison, there is no and limited reduced reaction in device A and B, respectively. Less V_O would be created through S/D contacts. More V_O in IGZO can induce more defect states, which causes a larger shift of V_{th} for the TFT with the pure Ti S/D contacts.

3.5 Summary

This chapter introduces the techniques to characterize the as-fabricated IGZO TFTs. The transfer, output and contact characteristics of TFTs with different S/D contacts are extracted and compared. The instability tests are conducted on the TFT with Ti S/D contacts and

different channel size (40/2 μm, and 800/40 μm) under three categories of external stress scenarios (i.e., PBS/NBS, PBIS/NBIS, PBTS/NBTS). The mechanisms of all the instabilities are discussed. Ultimately, an ultra-thin Ti layer with the thickness of 10 nm is inserted between ITO and IGZO as the S/D contacts for a transparent IGZO TFT. The transparent TFT with ITO/Ti S/D contacts shows apparently improved contact characteristics, as well as enhanced μ_{FE}, enlarged I_D on/off ratio, and reduced V_{th} compared to the transparent TFT with the pure ITO S/D contacts. Both the TFTs with ITO and ITO/Ti S/D contacts show much improved stability under PBS, NBS, PBIS, and a slightly alleviated shift of V_{th} under NBIS compared to the TFTs with the pure Ti S/D contacts.

Chapter 4. Performance enhancement of transparent IGZO TFTs realized by sputtered AlO_x passivation layer

In this chapter, we report a high-mobility transparent IGZO TFT with a sputtered AlO_x passivation layer. The interfacial region between the IGZO layer and the AlO_x layer plays a crucial role in improving μ_{FE} (the maximum μ_{FE} increases from 6.292 cm^2/Vs for the TFT without the passivation layer to 69.01 cm^2/Vs for the TFT with the passivation layer) and the on/off current ratio (from ~10^7 without the layer to ~10^8 with the layer). The driving current of IGZO TFT is also significantly enhanced. The formation of the interfacial layer has been investigated and verified. The ion bombardment during the AlO_x deposition breaks the In-O bond in IGZO, generating oxygen ions (O^{2-}). The segregation of the O^{2-} is facilitated by the sputtered amorphous AlO_x. A metallic In-rich layer with high oxygen vacancy concentration is formed at the interface, leading to an increase in the carrier concentration in the interfacial layer. Besides the electrical performance, the reliability tests, including long-term exposure in the ambient environment and PBIS, show improved results as well.

4.1 Introduction

As introduced in chapter 2, a-IGZO has gradually replaced a-Si:H and LTPS as the channel semiconductor of TFT due to the high transparency, high μ_{FE} (up to 10 cm^2/Vs), good uniformity, small V_{th}, small S.S., and low-temperature fabrication process. Nevertheless, for the next generation FPD, uniform brightness, larger area,

higher resolution, and higher frame rates are in demand. Improving the driving capability and reliability of a-IGZO TFT becomes one of the critical concerns for many researchers. [190]

One of the most important reliability issues is the V_{th} shift of the TFT, which causes brightness variation of the display pixel [191]. This instability could originate from ambient molecules penetration, positive or negative bias stresses and illumination stress, as explained in section 3.3. To solve the reliability issue, a useful method is to deposit a passivation layer on the back surface of the channel layer [132],[192], which could effectively prevent the ambient gases (hydrogen and oxygen) and moisture from penetrating into the channel region. To date, SiO_2 or SiN_x deposited by plasma-enhanced chemical vapor deposition (PECVD) and Al_2O_3 deposited by atomic layered deposition (ALD) are common materials used for passivation. [66],[192],[193] The above options could effectively reduce the shift of the threshold voltage under light illumination, high temperature and positive or negative bias. In the meantime, both ALD and PECVD processes could introduce hydrogen into the channel region, which slightly improves the electron mobility. [66]

Although the TFT reliability has been improved significantly by the passivation, the mobility and driving current of the TFT may be not large enough for certain applications, such as virtual/augmented reality, micro-LED, biometric sensing applications, etc. [105] In this work, we report an amorphous aluminium oxide (AlO_x) passivation layer deposited by RF magnetron sputter at room temperature. After post-passivation annealing, the passivated TFT shows much higher mobility, larger driving

current and better reliability compared with the TFT without the passivation layer.

4.2 Device fabrication and characterization

TFTs with BGTC structure were fabricated, as shown in Fig. 4. 1(a)-(c). A 35 nm-thick Al_2O_3 layer was deposited on ITO (200nm) glass by ALD at 250 ℃ with TMA and H_2O as the precursor and oxidant, respectively, followed by a 5nm-thick SiO_2 layer deposition by PECVD at 300 ℃. This bilayer dielectric structure aimed to lower the off current and decrease the interface defect states. [114] After the formation of bilayer gate dielectric, a 45nm-thick amorphous IGZO (In: Ga: Zn=1:1:1) was deposited by RF magnetron sputtering with RF power of 100 W and Ar flow rate of 50 sccm. Then, a 250 nm-thick ITO layer, which served as the S/D contacts, was deposited by RF magnetron sputtering with RF power of 100 W and Ar flow rate of 50 sccm. Subsequently, we deposited an amorphous AlO_x passivation layer at the top of the device by RF magnetron sputtering. The target used for sputtering deposition of the AlO_x passivation layer was an Al_2O_3 target with purity of 99.99% purchased from ACI Alloy. The RF sputtering was conducted with RF power of 100 W at process pressure of 8 mTorr with 100% Ar flow. All the sputtering processes for deposition of the IGZO, ITO and AlO_x layers were performed at room temperature. The patterning of the IGZO, ITO, and AlO_x layers was carried out by using the UV lithography and lift-off processes. TFTs with various channel W/L ratios were fabricated. Finally, the as-fabricated TFTs were annealed at 300 ℃ in N_2 atmosphere for 1 hour. Schematic illustration of the TFT structure, top view of the structure observed through an optical

microscope, and photo image of the structure are shown in Fig. 4. 1(a), (b) and (c), respectively. In the meantime, a stack-layered structure was fabricated for the optical transmittance measurement of the TFT structure. Schematic illustration and photo image of the stack-layered structure are shown in Fig. 4. 1(d) and (e), respectively. In addition, for comparison of electrical performance, TFT without the AlO_x passivation layer was fabricated as well.

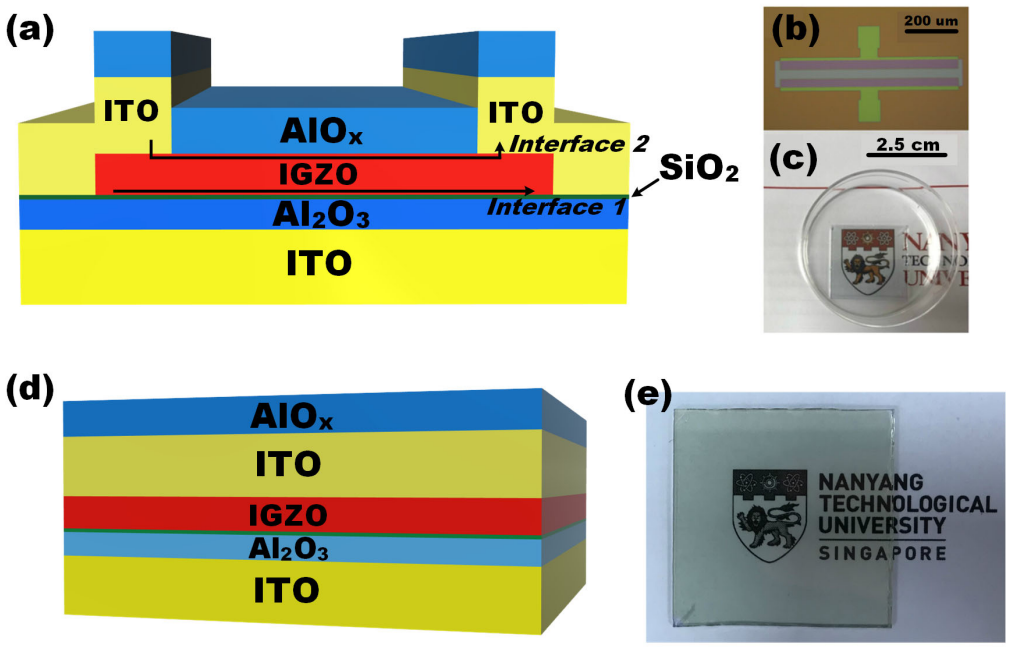


Fig. 4. 1 Schematic illustration of the TFT structure (a), top view of the TFT structure (W/L = 800 μm / 40 μm) observed through an optical microscope (b), photo image of the TFT structure (c), schematic illustration of the stack-layered structure for optical transmittance measurement (d), and photo image of the stack-layered structure (e).

Optical transmittance measurement of the stack-layered structure was conducted with LAMBDA 365 UV/Vis Spectrophotometer (PerkinElmer). The light wavelength for the measurement was swept from 400 nm to 700 nm, namely in the visible light

range. The electrical characteristics of TFT were measured with a Keithley 4200 SCS parameter analyzer in dark environment. For the measurement of the transfer curves, V_{GS} was sweeping from -7 V to 10 V, while V_{DS} was fixed at 1 V. For the measurement of the output curves, V_{DS} was sweeping from 0 to 7 V and V_{GS} is fixed 10 V, respectively. To investigate the structure of the passivated TFT, High–Resolution TEM (JEOL 2010 HR) was used to observe the IGZO/AlO_x interface. Likewise, XPS and AES depth profiling were used to track the shift of the binding energy for the elements of interest, usually attributed to the change in the oxidation state and chemical environment, with depth. Firstly, AES depth profiles were obtained using a field-emission Auger microprobe (JEOL JAMP-7830F) with a primary electron beam having an accelerating voltage of 10 keV and a probe current of 10 nA. The sample was tilted at 30° throughout the analysis and the analysis area was approximately 15 × 15 μm^2. The analyzer was operated at a constant retarding ratio (CRR) mode (energy resolution < 0.5%). Floating micro-ion etching device (FMIED) delivering an ion beam of 500-eV Ar^+ was used to sputter the thin-film samples over an area of 1.5 × 1.5 mm^2 from the AlO_x surface onwards for depth profiling. The AES spectra were recorded at an etching rate of 30 s/cycle.

XPS analysis was performed using an AXIS Supra spectrometer (Kratos Analytical Inc., UK) equipped with a hemispherical analyzer and a monochromatic Al K-alpha source (1487 eV) operated at 25 mA and 15 kV. XPS depth profiling experiments were carried out using an Ar Gas Cluster Ion Source (GCIS, Kratos Analytical Inc. Minibeam 6) operated at 5 keV Ar^+ with a raster size of 1 × 1 mm^2.

Selected-area XPS spectra were acquired after each etching cycle (20 s) from an area defined by a 110-μm aperture at a take-off angle of 90°. A 3.1-volt bias was applied to the sample to neutralize charge built up on the sample surface. The high-resolution scans were recorded at 40 eV pass energy. The binding energies (BEs) were charge-corrected based on the C 1s at 284.8 eV.

To verify the crystalline state of sputtered AlO_x, X-ray diffraction (XRD) was performed in the 2θ scan mode with Bruker D8 Discover XRD system operated with Cu-K_a radiation (40 V, 40 mA) at an incidence angle of 0.5°. The grazing-incidence wide-angle scattering (GiWAXS) pattern was obtained with Nano-inXider (Xenocs) with Cu-K_a microsource (30 W) at an incidence angle of 0.2°. The measurement was done at the rotation angle $\Psi = 0°$ to capture the out-of-plane scattering pattern from the sample.

4.3 Results and discussion

4.3.1 Characterization and comparison of TFT performance

Optical transmittance measurement result of the stack-layered structure is shown in Fig. 4. 2(a). In the visible light range (400 nm ~ 700 nm), the structure shows a transmittance of around 80%, indicating that the fabricated device is highly transparent.

Transfer curve of the TFT with the AlO_x passivation layer without post-annealing is shown in Fig. 4. 2(b). It can be observed from Fig. 4. 2(b) that the device is at a

normally on state and could not be turned off. Fig. 4. 2(c) shows the comparison of the transfer characteristic measured at V_{DS} = 1 V between the TFTs with and without the AlO_x passivation after annealing, while Fig. 4. 2(d) shows the comparison of the output characteristic measured at V_{GS} = 10 V between the TFTs with and without the AlO_x passivation after annealing.

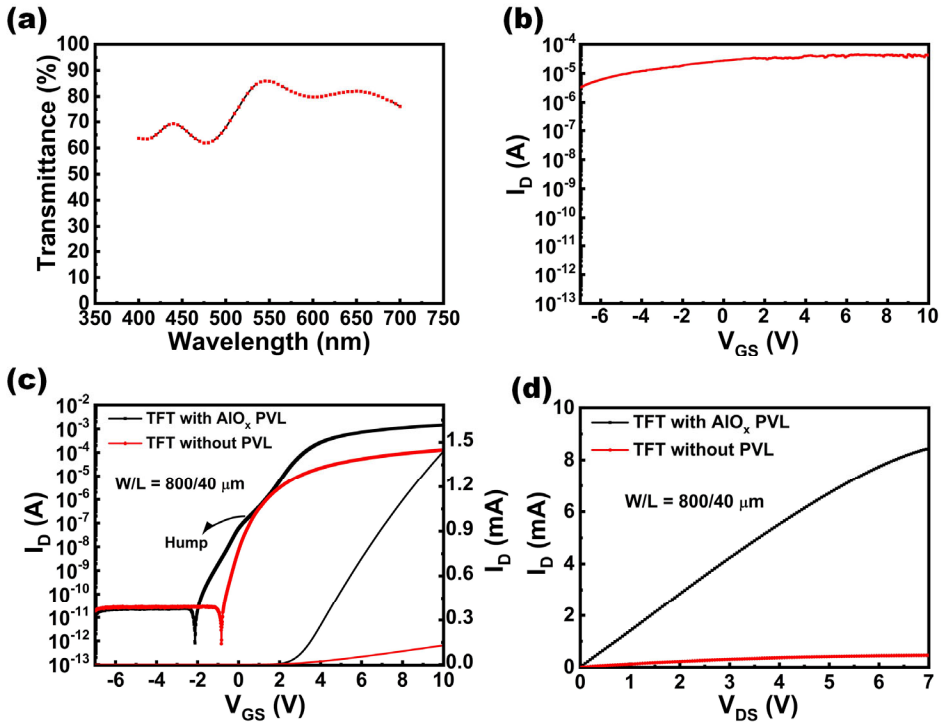


Fig. 4. 2 (a) Optical transmittance measurement of the stack-layered structure, (b) transfer curve measured at V_{DS} = 1 V of the TFT with PVL, with W/L of 800/40 μm, and without post-annealing, (c) comparison of the transfer characteristic measured at V_{DS} = 1 V between the TFTs with and without PVL after annealing, and (d) comparison of the output characteristic measured at V_{GS} = 10 V between the TFTs with and without PVL after annealing.

From the transfer curves, I_D on/off ratio, V_{th}, S.S., and μ_{FE} of the TFTs are extracted and calculated based on the methods used in **section 3.2**. To calculate μ_{FE},

the value of C_{ox} is obtained to be 1.712×10^{-7} F/cm^2 by taking the 35 nm Al_2O_3 and 5 nm SiO_2 layers into account. For the TFT without passivation, I_D on/off ratio is 1.3×10^7, V_{th} is 3.8 V, S.S. is 250 mV/decade, and the maximum μ_{FE} is 6.292 cm^2/Vs. For the TFT with AlO_x passivation, I_D on/off ratio is 1.87×10^8, V_{th} is 2.7V, S.S. is 580 mV/decade, and the maximum μ_{FE} is 69.01 cm^2/Vs. Note that the calculation of the mobility assumes that the gate capacitance does not change significantly during the deposition of the passivation layer (PVL). The assumption is supported by the C-V measurement of the gate capacitance of the TFTs with and without the PVL.

Besides the above measurements of electrical characteristics, TLM is conducted to measure the contact characteristics between the ITO S/D electrodes and the IGZO layer and investigate the effect of the sputtered AlO_x PVL on the contact resistance and sheet resistance of the IGZO layer. TFTs with fixed channel width of 80 μm and

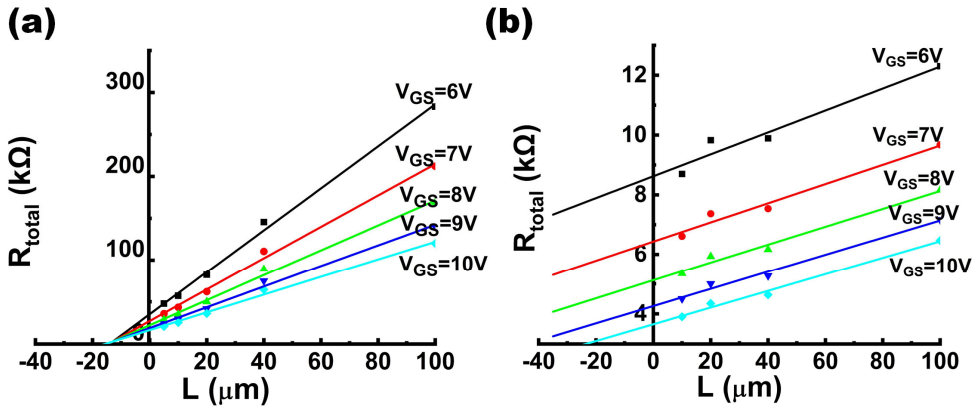


Fig. 4. 3 TFT TLM curves under different applied V_{GS}: (a) without PVL and (b) with AlO_x PVL.

various channel lengths of 5 μm, 10 μm, 20 μm, 40 μm, and 100 μm are selected to construct the curves of R_{total} versus channel length (L) at different V_{GS}, as shown in Fig. 4. 3. To exclude the influence of channel width (W), Equation (3.2) is W-normalized when extracting the contact resistance (i.e., $2R_CW$). As Fig. 4. 3 shows, for the TFT without the PVL, with increasing V_{GS} from 6V to 10V, the slope of the curves, i.e., R_{IGZO}/W, decreases from $2.5 \times 10^3\ \Omega/\mu m$ to $1.0 \times 10^3\ \Omega/\mu m$, and at the same time the intercept at L = 0, i.e., $2R_c$, also decreases from$3.5 \times 10^5\ \Omega$ to $1.6 \times 10^5\ \Omega$. In contrast, for the TFT with PVL, R_{IGZO}/W is much smaller and maintained at around $30\ \Omega/\mu m$, and the contact resistance decreases from $8.6 \times 10^3\ \Omega$ to $3.6 \times 10^3\ \Omega$. These results clearly show that the AlO_x PVL reduces both r_{IGZO}/W and $2R_CW$. The reduction of sheet resistance and contact resistance concurrently enhances the TFT performance. Likewise, L_T is obtained for the two TFTs. At V_{GS} = 10 V, for the TFT without PVL, L_T = 8.0 μm, for the TFT with AlO_x PVL, L_T = 11.4μm. With the PVL, the length of current transfer path is increased. All the fabricated TFTs have the overlap distance between S/D and IGZO d = 20 μm, which is significantly larger than the above L_T values of both un-passivated and passivated TFTs. In the above approach, we neglect the difference between the IGZO sheet resistance under the contact and the one in the channel. It should be considered in a more precise calculation. A comparison of all FOMs for the TFT with and without PVL is summarized in Table 4. 1. Note that ‘A’ and ‘B’ in the first column refer to the devices with and without the AlO_x PVL, respectively; $2R_CW$ and R_{IGZO}/W are both extracted at V_{GS} = 10 V.

Table 4. 1 Comparison of electrical and contact characteristics between TFTs with (A) and without (B) AlO_x PVL

	On/off ratio	S.S. (mV/dec)	V_{th} (V)	μ_{FE} (cm^2/Vs)	$2R_CW$ (Ωcm)	R_{IGZO}/W ($\Omega \mu m^{-1}$)
A	1.87×10^8	580	2.7	69.01	33.6	27.8
B	1.30×10^7	250	3.8	6.292	151	1.0×10^3

4.3.2 Discussion on the alteration of FOMs for the passivated TFT

The conduction mechanism of a-IGZO TFT has been introduced in detail in **section 2.1.4**, which tells that the carrier mobility increases with the carrier concentration in IGZO. As shown in Table 4. 1, the TFT with sputtered AlO_x PVL shows higher on/off ratio by nearly one order, smaller V_{th}, much higher μ_{FE} by over one order, much lower sheet resistance of IGZO and lower contact resistance. Nevertheless, at the same time, S.S. slightly increases for the TFT with PVL, and a 'hump' is also observed in the transfer curve (Fig. 4. 2(c)). These obvious performance changes suggest that there could be donor-like defects at the IGZO/AlO_x interface (i.e., interface 2 in Fig. 4. 1(a)). As shown in Fig. 4. 2(b), the as-fabricated TFT without post-deposition annealing could not be switched off, indicating existence of excessive free carriers due to the donor-like defects at the interface. Thus, post-deposition annealing is necessary for reducing the concentration of the donor-like defects to a reasonable level. The mechanism for the lower contact resistance of the

TFT with the passivation layer is not clear yet. One possible explanation is given in the following. As demonstrated in [194], lateral free carrier diffusion occurring due to the gradient of carrier concentration in the IGZO layer in the edge region between the S/D contact and the channel significantly affects the contact resistance. In the present study, the deposition of the PVL produces excessive free carriers in the exposed region of the IGZO layer. During the post-deposition annealing, the free carriers could laterally diffuse into the source/drain contact region of the IGZO layer, leading to reduction in the contact resistance. [194]

4.3.3 Discussion on the two conduction paths in the passivated TFT

The curves of μ_{FE} vs. V_{GS} for the TFTs without and with the AlO_x PVL are shown in Fig. 4. 4(a) and (b), respectively. Without PVL, μ_{FE} of the TFT gradually increases with V_{GS} and becomes saturated at V_{GS} of ~ 8V (a slight decrease can be observed at V_{GS} of ~ 10 V), which can be well explained by the percolation model. Whereas in the passivated TFT, the mobility rapidly increases following by a gradual decrease with increasing V_{GS} with the maximum μ_{FE} occurring at V_{GS} of ~ 4.5 V. It is suspected that the gradual decrease in the mobility of the passivated TFT might be related to the change in contact resistance. As V_{GS} increases, the actual voltage drop across the channel region might change. According to Equation (2.9) in **section 2.2.2**, substituting the fixed V_{DS} by an actual channel voltage drop could change the trend of mobility at high gate-field. To verify the impact of contact resistance, we choose five feature points (V_{GS} = 6, 7, 8, 9 and 10 V) to calculate the actual voltage drop across

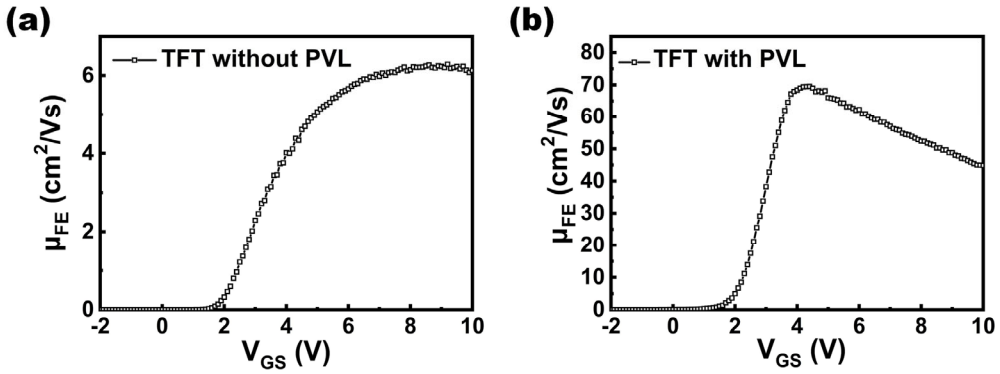


Fig. 4. 4 μ_{FE} vs. V_{GS} of (a) TFT without passivation layer (PVL), (b) TFT with AlO_x passivation layer (PVL)

the channel and then recalculate the mobility. The calculated mobilities corresponding to the V_{GS} values are 162.67, 140.80, 117.66, 108.64 and 94.56 cm^2/Vs, respectively. There is still a large decrease in the mobility. It is found that the decrease of transconductance g_m has a more significant impact than the change of actual channel voltage drop. The mechanisms responsible for the decrease of transconductance (which means decrease of actual mobility of the passivated device at high V_{GS}) are not clear yet. Two possible mechanisms are explained in the following. As shown in Fig. 4. 1(a), the passivated TFT could have two conduction channels, i.e., the channels at interface 1 and interface 2, respectively; and both channels contribute to the drain current. Deposition of the AlO_x layer by sputtering process could induce charges at interface 2 or other charged defects in the IGZO layer, which might cause decrease of the mobility in the conduction channel at interface 1 at high V_{GS} for the passivated device. On the other hand, the sputtering process could increase the roughness of the IGZO back surface, which would enhance the surface scattering. The enhanced

surface scattering at interface 2 at high gate fields could lead to a decrease of the mobility in the conduction channel at interface 2. [68],[77] Decrease of mobility of one of the channels or both channels would lead to decrease of the mobility of the passivated device at high V_{GS}.

As both channels contribute to the drain current, the passivated TFT has lower IGZO layer resistance as compared to the TFT without passivation. The channel at interface 2 has a lower turn-on voltage compared to the channel at interface 1 because the channel region at interface 2 has excess free carriers. Thus, V_{th} of the passivated TFT is lower than that of the TFT without PVL. The existence of the two conduction channels could also explain the hump behavior observed in the transfer curve, [195], [196] and the defect states at interface 2 could be responsible for the increase in the subthreshold swing.

4.3.4 Investigation on the ion bombardment effect from the AlO_x layer

Previous studies have proposed that ion bombardment during the AlO_x sputtering process could break the In-O bond in the IGZO. [197],[198] Ar plasma has also been shown to effectively break the In-O bond with the Ar ion bombardment in high sputtering field. [199] In order to further investigate the ion bombardment effect, the TFTs passivated by 20 nm sputtered AlO_x layer with different Ar flow rate (25 sccm, 50 sccm, 75 sccm, 100 sccm and 120 sccm) are fabricated. Transfer curves of these devices are measured at V_{DS} = 1 V and shown in Fig. 4. 5(a). The TFT passivated by AlO_x sputtered at 120 sccm Ar flow rate is identical to the one shown in Fig. 4. 2(c).

Fig. 4. 5(a) clearly shows that ion bombardment has a significant impact on the electrical performance. As shown in Fig. 4. 5(a), no 'hump' is observed in the transfer curves of those passivated by the AlO_x deposited at low Ar flow rates. Adversely, the devices passivated by the AlO_x deposited at the low Ar flow rates of 25, 50 and 75 sccm show a lower on-current compared with the un-passivated device. A low Ar flow rate could facilitate the oxygen ions from AlO_x to penetrate into the IGZO layer, and the oxygen ions reduce the free carrier (or V_O) concentration in the IGZO layer. On

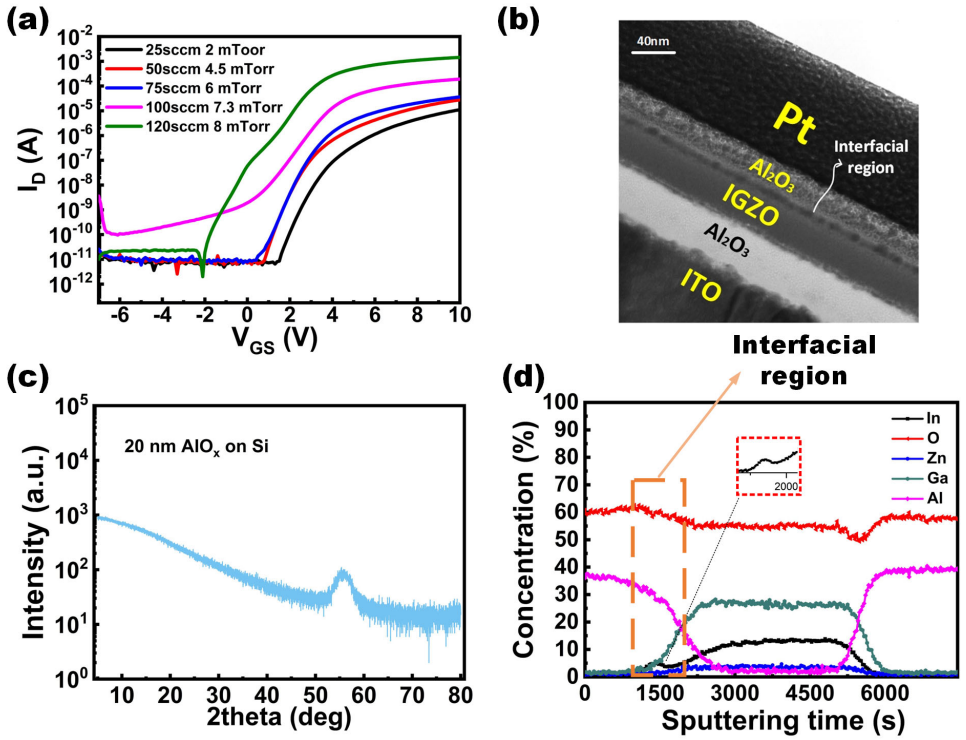


Fig. 4. 5 (a) Transfer curves measured at V_{DS} =1 V of the TFTs passivated by AlO_x sputtered at different Ar gas flow rates (Note: The transfer curve at 120 sccm is the same as that in Fig. 4.2 (c)). (b) HR-TEM image of the cross sections of the TFT passivated by AlO_x. (c) XRD pattern of the AlO_x film formed by sputtering deposition on Si substrate with an incidence angle of 0.5°. (d) AES depth profiling of In, O, Zn, Ga, and Al atoms in the TFT passivated by the sputtered AlO_x layer.

the other hand, as discussed later, deposition of AlO_x onto IGZO by sputtering could produce oxygen vacancies in the IGZO layer due to the ion bombardment. A low Ar flow rate leads to a low level of ion bombardment, which means a low free carrier concentration at interface 2. Thus, the TFTs fabricated with low Ar flow rates has lower on-currents.

The existence of the interfacial layer at interface 2 induced by the ion bombardment could be proven from the HR-TEM (JEOL 2010) cross-section imaging, as shown by the arrow-highlighted region in Fig. 4. 5(b). In Fig. 4. 5(b), the sputtered AlO_x layer is not as smooth as other amorphous layers. Thus, we conduct an X-Ray Diffraction (XRD) analysis for a layer of sputtered AlO_x on Si substrate, aiming to clarify the crystalline state of the sputtered AlO_x. The result is shown in Fig. 4. 5(c), which proves that the AlO_x film has an amorphous nature due to the lack of sharp diffraction peak. The grainy structure of the AlO_x film in the TEM image could result from the electron beam induced crystallization during the lamella preparation in focused ion beam microscope (FIB). [200] Some studies have showed that oxygen species could easily diffuse into the amorphous alumina. [201],[202]

To further analyze the formation of an intermixing region between AlO_x and IGZO, we also utilize a combination of both Auger Electron Spectroscopy (AES) and X-ray Photoelectron Spectroscopy (XPS) depth profiling techniques to study the change in the elemental composition and the chemical states with depth.

As shown in the AES depth profile (Fig. 4. 5(d)), there is an obvious hump for the indium profiling in the interfacial layer, which suggests that the AlO_x-IGZO

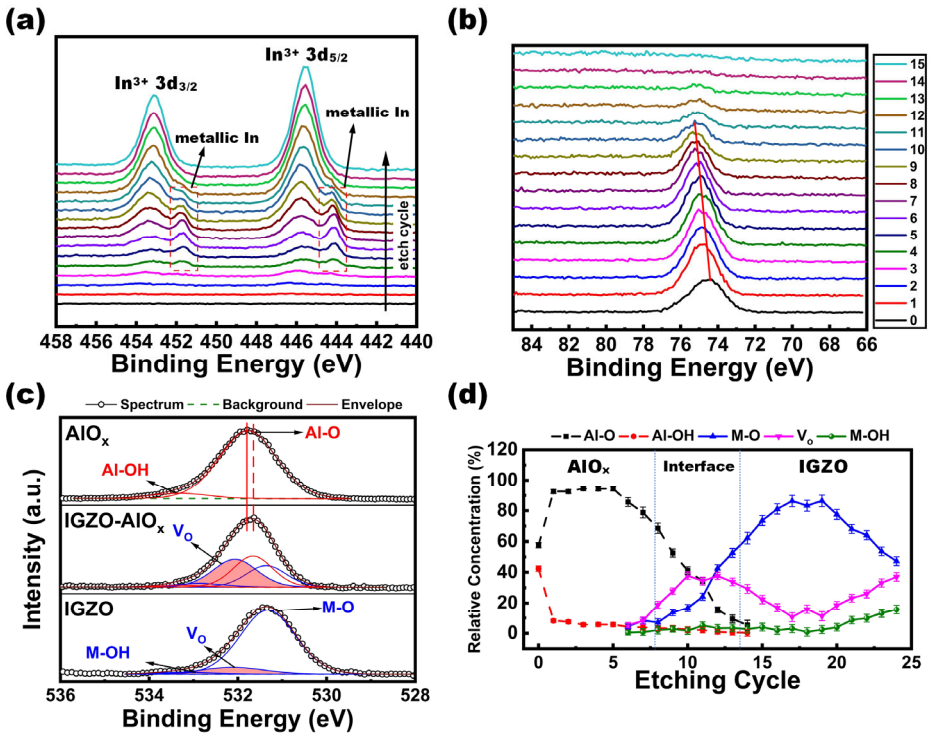


Fig. 4. 6 (a) Waterfall plot of In 3d XPS spectra for the AlO_x/IGZO stack with etching cycles in 2D format (Intensity vs. Etching cycles). (b) Waterfall plot of Al 2p XPS spectra for the AlO_x/IGZO stacks with etching cycles in 2D format. (c) O 1s XPS peaks measured in the bulk of the AlO_x layer, IGZO-AlO_x interface region, and bulk of the IGZO layer, respectively. The two red vertical lines show the slight shift of O 1s peak of the interface region relative to the bulk of the AlO_x layer. (d) Depth profiling of O-related species.

interface is indeed rich in In. Besides, the O/Al ratio increases compared with the bulk AlO_x, indicating both oxides could have changed chemically within the interfacial layer.

To further investigate the change in the chemical states with depth, Fig. 4. 6 shows the In 3d, O 1s and Al 2p XPS spectra from the AlO_x/IGZO stacks. As seen in the In 3d spectra (Fig. 4. 6(a)), with the etching cycle increasing, two additional minor peaks positioned at around 444 eV and 451.5eV, respectively, (i.e., the regions

highlighted by the red dotted lines), emerge; and they disappear when the etch cycle further increases. They are attributed to the metallic indium generated at the AlO_x/IGZO interfacial region during the sputtering deposition of AlO_x. [203],[204] This phenomenon agrees with what the TEM image (Fig. 4. 5(b)) shows. The transition region is also characterized by a slight increase in the concentration of V_O, which is obtained via deconvolution of the O 1s spectra, compared to the bulk of the IGZO layer. The higher concentration of V_O correlates with higher charge-carrier concentration, giving rise to the improvement in the device performance. At the same time, the O 1s BE peak of AlO_x slightly shifts in the negative direction relative to that of the interface, as shown by the two vertical red lines in Fig. 4. 6(c). It has been reported that O 1s peak would negatively shift when the O/Al ratio increases in AlO_x. [205] The Al 2p XPS spectra for the AlO_x/IGZO stack for various etching cycles are shown in Fig. 4. 6(b). When the etch cycle goes to 14, the detection goes into the bulk of IGZO, and thus the Al 2p peak disappears. For the Al 2p, as shown in Fig. 4. 6(b), the XPS peak energy positively shifts by around 1 eV. Positive shift of Al 2p BE indicates a higher oxidation level [206], and a transition from metastable to stable state [207].

Thus, it could be concluded that when depositing amorphous AlO_x onto IGZO by sputtering, oxidation/reduction reactions happen at the interface. Since Al_2O_3 has lower enthalpy of formation (-1675.7 kJ/mol) than In_2O_3 (-925.9 kJ/mol), Al ions from the Al_2O_3 target capture oxygen from IGZO, which is encouraged by the ion bombardment. Thus, In-O bond in the IGZO layer is broken, generating metallic

indium (i.e., V_O) in the IGZO layer. Simultaneously, the deposited amorphous AlO_x might accommodate the free O^{2-} diffusing from the IGZO layer. The metallic-In-rich layer is formed at the interface and provides more mobile carriers. In the percolation model, higher carrier concentration lowers the potential barrier heights over the mobility edge, leading to higher carrier mobility for the IGZO TFT.

4.3.5 Reliability test of the TFTs

Besides the electrical performance, reliability of the TFT passivated by sputtered AlO_x is also investigated. Firstly, the AlO_x passivated TFT has been stored in air in a lab with well-controlled air conditioning at room temperature with humidity of 70% ~ 71% for 6 months. The transfer curves are measured and shown in Fig. 4. 7(b). The V_{th} of the TFT has nearly no shift after exposing in air for 6 months, which is in contrast with the situation of the TFT without passivation (Fig. 4. 7(a)). It indicates that the AlO_x passivation layer has effectively suppressed the penetration of the ambient molecules (H_2O and O_2, etc.). There is still a hump in the semi-log I_D-V_{GS} curve but not so remarkable compared with the initial curve. During the 6-month exposure in air, some free metallic In and oxygen ions recombine with each other in the interface layer at interface 2. The contribution of the channel at interface 2 is suppressed such that the hump is slightly alleviated.

Subsequently, tests under PBIS and NBIS are carried out. The light source used for both PBIS and NBIS measurements is a 21V 150W tungsten halogen lamp (GX5.3, OSRAM SYLVANIA). The wavelength range of the lamp is 360 - 2500 nm. For PBIS,

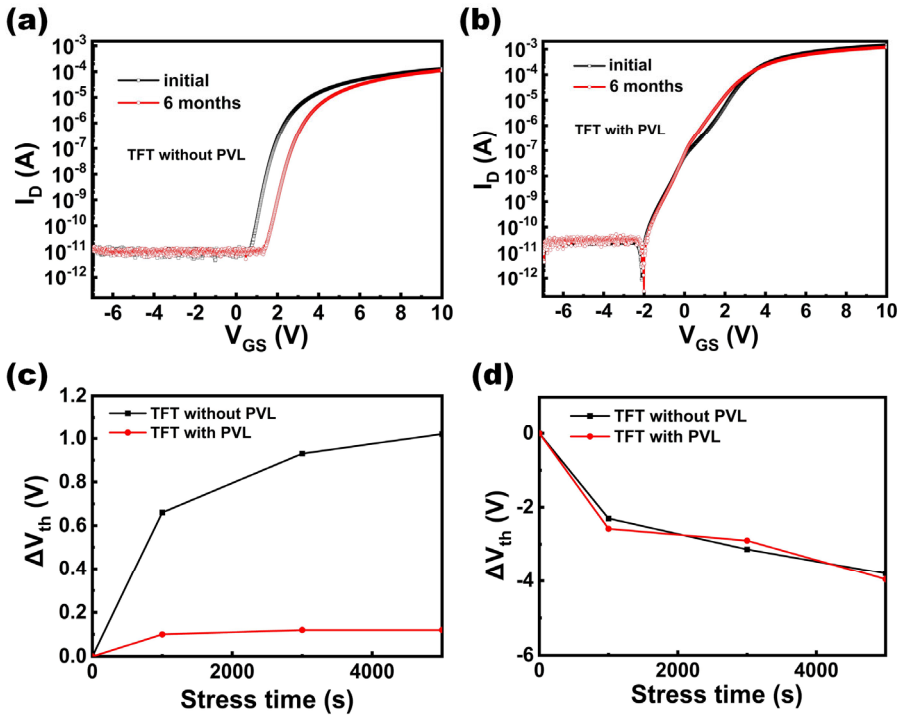


Fig. 4. 7 Transfer curves (measured at V_{DS}=1V) of the TFTs without passivation (a) and with the AlO_x passivation layer (b) after 6 months of exposure in air. Note: The initial curves were both the same as the transfer curves shown in Fig. 4.2 (c). (c) ΔV_{th} versus stress time under PBIS. (d) ΔV_{th} versus stress time under NBIS.

the gate of the device is biased at 7 V with illumination of optical power of 2.65 mW from a halogen light source for 5000 s. Fig. 4. 7(c) shows the curves of ΔV_{th} versus stress time under PBIS for the TFT with and without AlO_x PVL. It can be observed that the passivation layer greatly reduces the shift of V_{th} of the TFT under PBIS from 1.02 V to 0.12 V. It proves that the passivation layer effectively blocks the absorption of O_2 from the ambient at positive gate bias and prevents the formation of acceptor-like electron trap sites at the IGZO surface. For NBIS, the gate of the device is biased at -7 V with illumination of optical power of 2.65 mW for 5000 s. Fig. 4. 7(d) shows the curve of ΔV_{th} versus stress time under NBIS. For the stress duration of 5000 s, the

V_{th} of the TFT without passivation layer shows a negative shift of 3.8 V, while the V_{th} of the passivated TFT shows a negative shift of 3.96 V. The slight increase of V_{th} shift could result from the creation of V_O-related defects states in IGZO induced by the PVL. In other words, the transparent passivation layer is not able to reduce the NBIS instability. To suppress the NBIS instability, a light shielding layer could be used. Besides, the electronic structure of the channel layer should be modified to lower its VBM and maintain the large dispersion of the CB, aiming to prevent the generation of the photon-excited electron-hole pairs and keep high mobility at the same time. [208]

4.4 Summary

In this work, a transparent a-IGZO TFT passivated by the sputtering-deposited AlO_x layer is fabricated. The mobility and on/off current ratio of the TFT are enhanced by nearly one order, i.e., the maximum μ_{FE} increases from 6.292 cm^2/Vs without the PVL to 69.01 cm^2/Vs with the PVL; and the on/off current ratio increases from 1.3×10^7 without the PVL to 1.87×10^8 with the PVL. Such a large improvement results from the interfacial layer formation at the IGZO/AlO_x interface. The ion bombardment during the sputtering deposition of the AlO_x layer could prompt Al ions to capture oxygen from the IGZO layer and break the In-O bonds; and at the same time, the deposited AlO_x layer might accommodate the free O^{2-} diffusing from the IGZO layer. Then a metallic-In-rich layer is formed at the interface with high carrier concentration. Besides, the passivated TFT shows better reliability under exposure in air for 6 months, and much smaller V_{th} shifts under PBIS.

Chapter 5. IGZO transparent electronic and photoelectric synaptic TFTs based on TaO_x gate dielectric

In this chapter, we report IGZO transparent electronic and photoelectric synaptic TFTs based on TaO_x gate dielectric. A transparent TFT in the combination of IGZO channel and high-κ (the dielectric constant is about 42.6) TaO_x gate dielectric layer is fabricated. The TFT shows robust anticlockwise hysteresis under DC voltage sweep and synaptic behaviors (i.e., excitatory postsynaptic current, short-term memory plasticity, short-term memory to long-term memory transition, and potentiation and depression) under voltage pulse stimulus. In addition, the TFT shows high responsivity to illumination of light with various wavelengths (ultraviolet and visible lights). Synaptic behaviors in response to light pulse stimuli, which could be employed in vision-based neuromorphic applications, are demonstrated. Large conductance change ($G_{max}/G_{min}>10$) and ultra-low non-linearity ($\alpha<0.5$) of the potentiation and depression can be inspired by either gate bias pulses or photoelectric pulses with short pulse widths and small amplitudes.

5.1 Introduction

Artificial synaptic devices have been attracting growing attention since the conventional von Neumann architecture was confronted with bottleneck, especially in the emerging neuromorphic computing area. [177],[209],[210] To characterize the synapse, there are several fundamental indices: excitatory postsynaptic current (EPSC), short-

term memory (STM) plasticity, STM transition to long-term memory (LTM), and potentiation and depression (P/D). [178],[211],[212] EPSC refers to the opening of ion gates in the channel of postsynaptic cell and the strengthening of synaptic transmission in response to external stimulus applied to the presynaptic cell. STM plasticity reflects the tunability of synaptic weight in response to different presynaptic activities. For instance, paired-pulse facilitation (PPF) is a typical form of STM plasticity, which shows the impact of time interval between two successive pulse stimuluses on the amplification of EPSC. To extend the decay of EPSC in STM and achieve the transition from STM to LTM, multiple repeated stimulus pulses can be applied, which evolves the synapse function from simple learning to the concurrence of learning and memory. With further increasing of the stimuli pulse number, P/D of the synaptic strength could happen. [213]

IGZO-based TFT is a promising candidate for artificial synapse, which could be attributed to the following superiorities. 1). As a three-terminal synapse, conductance change controlled by the gate terminal and signal transmission through the semiconductor channel layer can be achieved concurrently in IGZO TFT, which improves the efficiency of learning process compared with two-terminal synapses. [178] 2). The conductance of IGZO channel can be modulated by carrier concentration effectively thanks to the potential-model based carrier transport mechanism in IGZO. [52] Meanwhile, the incorporation of stabilizer Ga balances the excess carrier concentration in In- and Zn-based oxides, which enhances the gate controllability over the channel conductance. [47] 3). IGZO has large bandgap at around 3.2 eV,

facilitating IGZO TFT to be applied as highly transparent artificial synapse. 4). IGZO is compatible with a large variety of dielectrics regardless of the valence band offset between each other, which benefits from the inhibited transport of holes in IGZO. [22] 5). Amorphous IGZO can be deposited by RF magnetron sputtering at room temperature with good uniformity, which makes IGZO TFT very suitable for use in large-area arrays fabricated on flexible substrates. 6). In contrast to some metal-oxide based two-terminal synaptic devices (e.g., memristors or resistive random-access memory (ReRAMs)) which show large device-to-device variations, [214] IGZO TFT has a small device-to-device variation. 7). IGZO is sensitive to light with specific wavelength range, which makes the output current of IGZO TFTs tunable by external light illumination. [132],[185],[215]

Either electronic or photoelectric IGZO synaptic TFTs have been reported based on different working principles. Ferroelectric IGZO TFTs are used to emulate the electronic synapses by gradually modulating the direction of polarization in the ferroelectric layer under the stimulation of electric pulses. [216],[217] The main limitations for ferroelectric IGZO synaptic TFT are: 1) large amplitude of the electric pulse is required to inspire the reverse of polarization, 2) the deposition of ferroelectric layer needs precise thickness control and high temperature annealing. Charge-trapping based IGZO synaptic TFTs are also demonstrated with a variety of defect-rich dielectrics. SiO_x based double-gate IGZO synaptic TFT was presented in [218], which showed electro-sensitivity based on the charge trapping/release and photo-sensitivity under UV stimulation. The charge-trapping effect inspired the

inhibited postsynaptic current (IPSC), while UV illumination stimulated the EPSC. IPSC and EPSC could be transformed mutually by changing the predominance between electric pulses and UV pulses. Optoelectronic synaptic TFT in combination of IGZO channel and alkylated graphene oxide (GO) charge-trapping layer was developed in [219]. The mixture of UV light pulses and electric pulses accelerated the release of trapped carriers in alkylated GO, which enlarges the ratio of maximum conductance (G_{max})/minimum conductance (G_{min}) with retained small non-linearity in P/D of the synapse. Oxygen-deficient HfO_x is a special material which owns charge-trapping effect and ferroelectricity at the same time. In [220], W. Yang investigated an IGZO synaptic transistor with bipolar plasticity based on a $HfO_xN_y/HfO_x/HfO_xN_y$ sandwich-stack dielectric structure. Positive electric pulses stimulated the IPSC by charge trapping/release effect, while negative electric pulses stimulated the EPSC by ferroelectric effect. This bipolar plasticity could emulate the distinct response of neurons to the stimuli (i.e., favorite or unwanted). Some drawbacks for charge-trapping synaptic TFTs include: 1) EPSC could hardly be excited by electric pulses directly since the carrier concentration in IGZO is reduced with charge trapping effect which leads to the positive shift of V_{th} of the IGZO TFT; 2) the memory window induced by charge trapping is small, resulting in the small G_{max}/G_{min} ratio in P/D of the synapse; and 3) charge-trapping effects are not enduring and stable without special structure engineering.

Ion-conductive dielectric is also an emerging candidate to be applied in IGZO synaptic TFTs, which contains movable ions to emulate the neurotransmitters in the

synaptic cleft. Proton-rich chitosan electrolyte deposited by spin-coating is widely employed as the gate insulator in photoelectric synaptic IGZO TFTs. [13],[221] Protons inside chitosan will migrate to the IGZO/chitosan interface driven by positive electric pulses, which excites the EPSC flowing through the IGZO accumulation layer. STM plasticity, STM transition to LTM, and P/D are all successfully mimicked under the synergistic modulation of electric and light pulses. However, organic chitosan could induce serious instability and poor endurance of the device. In addition, organic material is not compatible with complementary-metal-oxide-semiconductor (CMOS) process. TaO_x is a sort of metal oxide which has been extensively used in ReRAM as a resistance switching layer. [222]-[224] The superiorities of TaO_x lie in 1) high dielectric constant, 2) abundance in movable ions, 3) compatible with CMOS process, 4) high transparency, and 5) room-temperature deposition. Pure electronic metal-oxide synaptic TFTs have been reported by utilizing TaO_x as gate insulator. [225],[226] In this work, a staggered bottom-gate IGZO synaptic TFT with TaO_x dielectric is demonstrated with high stability and endurance. Large G_{max}/G_{min} ratio and small non-linearity are achieved in P/D of the synaptic strength under the stimulation of pure electric pulses with small voltage amplitudes and short pulse widths thanks to the abundant free ions and high dielectric constant of the sputtering-deposited TaO_x layer. By applying negative pulses with step-increasing amplitudes for the depression, the non-linearity of depression and the endurance of G_{max}/G_{min} ratio under repeated P/D cycles are improved significantly. On the other hand, the synaptic behaviors including EPSC, STM plasticity, STM transition to LTM, P/D with large G_{max}/G_{min} ratio and

small non-linearity are successfully mimicked under the stimulation of either UV or visible light pulses (here for the visible light experiment, blue, green, and red light with the wavelengths of 470 nm, 525 nm, and 633 nm, respectively, are used.). The transparent IGZO TFT of this work is promising in vision-based neuromorphic applications with high learning accuracy. [227],[228]

5.2 Device fabrication and characterization

The BGTC structure is chosen for the TFT fabrication. In this structure, the dielectric layer (160 nm TaO_x), channel layer (45 nm IGZO), source/drain (S/D) electrodes (200 nm ITO) and passivation layer (100 nm SiO_2) are deposited on the ITO-coated (bottom-gate) glass layer by layer. Deposition of the TaO_x, IGZO and ITO (S/D electrodes) layers are all carried out by RF magnetron sputtering with 100 W RF power at room temperature in pure Ar atmosphere. The Ar flow rates for the sputtering deposition of TaO_x, IGZO and ITO are set to 100, 50 and 20 sccm, respectively. PECVD is utilized for the deposition of the SiO_2 passivation layer. To define the patterns of the channel layer and S/D contacts, photolithography and lift-off process are applied. Finally, to stabilize the carrier concentration in the channel layer, the as-fabricated device is annealed at 300 ℃ in N_2 atmosphere for 1 hour. It is worthy to mention that thermal budgets of all processes are controlled at or below 300 ℃. To measure the dielectric constant of the TaO_x layer, a capacitor with ITO-TaO_x-ITO sandwich structure is fabricated with the dielectric thickness of 160 nm and

the overlap area between top electrode and bottom electrode of 100×100 μm^2, as shown in Fig. 5. 1(d).

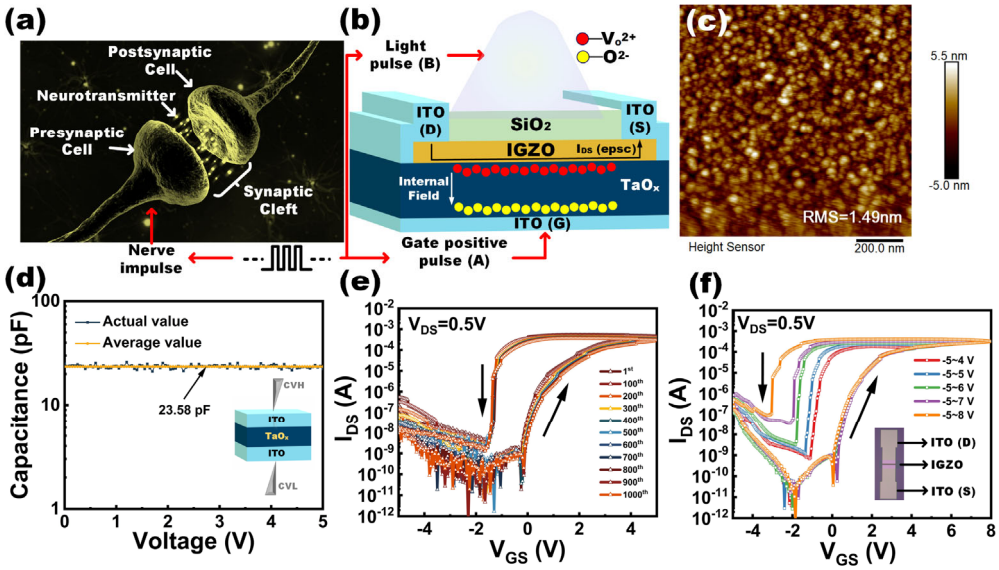


Fig. 5. 1 (a) Schematic illumination of human brain synapse. (b) 3D schematic of the IGZO TFT device of this work. (c) 2D AFM image of the TaO_x layer deposited by RF magnetron sputtering. The root mean square (RMS) of the roughness is 1.49 nm. (d) Result of the C-V measurement at 100k Hz of the TaO_x layer. The inset is the schematic of the capacitor structure for C-V measurement. (e) Transfer curves of the TFT under DC dual sweep with 1000 cycles. (f) Transfer curves of the TFT under DC sweep with different positive stop V_{GS}. W/L ratio of the TFT is 80/5 μm. The inset is an optical image of the practical device.

The surface roughness of the TaO_x layer is measured with Atomic Force Microscopy (AFM) from Bruker company. The 2D morphology of the TaO_x layer is shown in Fig. 5. 1(c). Electrical characteristics (including transfer characteristics, and capacitance-voltage relationships) of the device and their response to the stimulation of voltage or light pulses are measured with a Keithley 4200 semiconductor

characterization system (SCS). LIGHTNINGCURE Spotlight source LC8 is used to deliver UV light in the wavelength range of 300~400 nm. SugarCUBE ULTRA LED light source is used to provide visible light at different wavelengths (here blue, green, and red light with the wavelengths of 470 nm, 525 nm, and 633 nm, respectively are used) for the experiment of examining the wavelength selectivity of the synaptic behaviors in the as-fabricated TFT. In addition, XPS analysis towards the as-deposited TaO_x layer is performed using an AXIS Supra spectrometer (Kratos Analytical Inc., UK) equipped with a hemispherical analyser and a monochromatic Al K-alpha source (1487 eV) operated at 15 mA and 15 kV. XPS depth profiling experiments are carried out using an argon Gas Cluster Ion Source (GCIS, Kratos Analytical Inc. Minibeam 6). The ion beam is rastered over an area of 1 x 1 mm^2. To minimize the preferential sputtering of oxygen from TaO_x, Ar_n^+ with a cluster size (n) of 1000 and incident energies of 10 keV is employed. The XPS spectra are acquired at pass energy of 20 eV after each etching cycle (30 min). A 3.1-volt bias is applied to the sample to neutralise charge build up on the sample surface. The binding energies (BEs) are charge-corrected based on the C 1s peak of adventitious carbon at 284.8 eV.

5.3 Results and discussion

Fig. 5. 1(b) shows the schematic diagram of the IGZO TFT device, which can be used to mimic the human brain synapse shown in Fig. 5. 1(a). The bottom-gate (ITO) applied with positive electric pulses (A), or the light pulses shone on the whole device (B) plays a role as the presynaptic cell. Then, the ITO (D) – IGZO – ITO (S) structure

of the TFT could be regarded as the postsynaptic cell where the drain current (I_{DS}) would flow through. I_{DS} represents the EPSC. The region between the presynaptic and postsynaptic cells is called synaptic cleft where neurotransmitters are released and stimulate the EPSC change in the postsynaptic cell. In this device, the dielectric layer TaO_x is expected to be the 'cleft', where neurotransmitter-like species would be created under external stimuli. Electrical and illumination pulses are applied respectively to evaluate the device synaptic behavior.

5.3.1 Electronic synapse

Following electrical characterization is conducted for the TFT device. Firstly, DC dual sweep is applied to the TFT. Fig. 5. 1(e) shows the transfer curves of the TFT under 10^3 cycles of V_{GS} dual sweep from -5 V to 5 V. V_{DS} is fixed at 0.5 V. A robust hysteresis between the forward sweep and backward sweep can be observed in Fig. 5. 1(e). The memory window (i.e., the difference in V_{th} of the TFT between the forward sweep and backward sweep) maintains at around 3.2 V. Furthermore, as the positive stop voltage of the DC sweep increases, the memory window tends to enlarge, as shown in Fig. 5. 1(f). The capacitance-voltage (C-V) measurement is also carried out with the ITO-TaO_x-ITO capacitor structure (Fig. 5. 1(d)). The measured capacitance is 23.58 pF at the frequency of 100 kHz. Thus, the dielectric constant at 100 kHz of the TaO_x layer is 42.6. S.S. of the TFT at I_{DS} = 1 nA are 50 and 150 mV dec^{-1} for the forward sweep and backward sweep, respectively. As discussed in **section 2.2.2**, based on Equation (2.8), S.S. is determined by the oxide capacitance,

interface trap density and semiconductor depletion capacitance. In this device, the small S.S. benefits from large C_{ox} of the TaO_x layer due to the high dielectric constant of TaO_x, which makes it possible to inspire synaptic behaviors with electric pulses with small amplitudes. Meanwhile, when V_{GS} is sweeping forward, ions in the TaO_x would be driven to accumulate at the TaO_x/IGZO interface and passivate the interface traps, which reduces S.S. in the backward sweep by three times compared with that in the forward sweep. [229],[230] The I_{DS} on/off ratio of the TFT is in the order of ~10^7.

The stable anticlockwise hysteresis under DC sweep of the TFT indicates there exists active ion movement in the dielectric layer driven by the applied electric field. [231],[232] The XPS results of the as-deposited TaO_x layer are shown in Fig. 5. 2(a)-(d). From Fig. 5. 2(a), the O/Ta ratio in the TaO_x is around 2.15, which means that the TaO_x is oxygen-deficient. Fig. 5. 2(b) depicts the wide scan of the bulk of the TaO_x from 0 to 1200 eV in the 7th etching cycle. The Ta 4f spectra in Fig. 5. 2(c) demonstrates there exist dominant Ta^{4+} species in combination with a small amount of Ta^{3+} species, which matches well with the O/Ta ratio. Furthermore, Fig. 5. 2(d) shows the O 1s spectra in the bulk of the TaO_x, which is deconvoluted into two peaks, i.e., the dominant Ta-O peak (O_L) with the binding energy of 530.1 eV, and oxygen vacancy (V_O) peak with the binding energy of 531.6 eV. From the above four figures, we could confirm the as-deposited TaO_x contains oxygen ions.

To explore the detailed ion movements in the TaO_x layer under electric signals, a positive electric pulse with amplitude of 5 V, pulse width of 30 ms, and base level of 0.1 V, followed by a negative pulse with amplitude of 3 V, pulse width of 30 ms, and

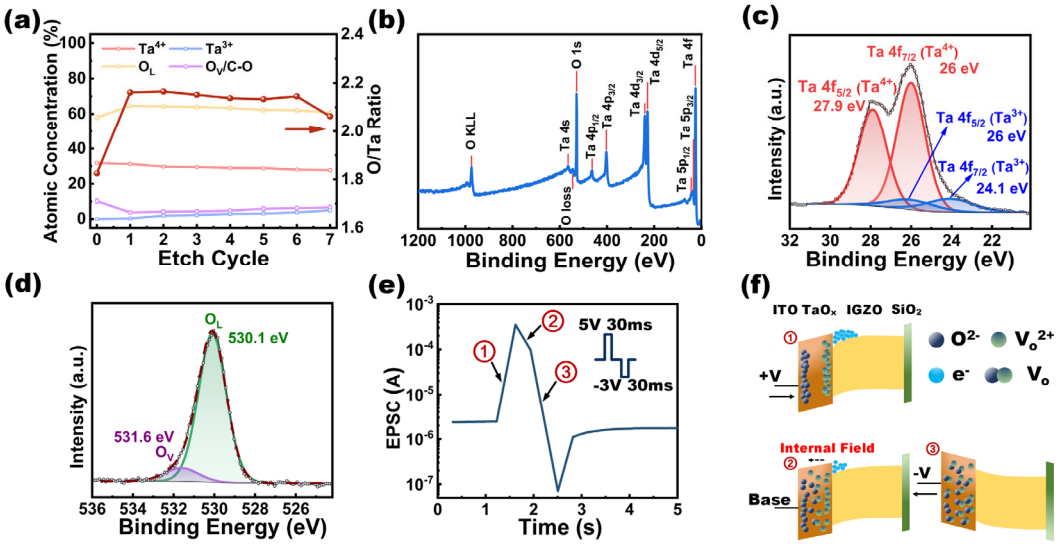


Fig. 5. 2 (a) Atomic concentration (left y-axis) and O/Ta ratio (right y-axis) in the as-deposited TaO_x layer. (b) Wide scan of the bulk TaO_x in the 7th etching cycle. (c) Ta 4f spectra in the bulk of TaO_x, deconvoluted into two Ta^{4+} and Ta^{3+} peaks. (d) O 1s spectra in the bulk of TaO_x, deconvoluted into lattice oxygen (O_L) and oxygen vacancy (O_V). (e) EPSC of the TFT under stimulation of a positive gate pulse with the amplitude of 5 V, pulse width of 30 ms, and base level of 0.1 V, followed by a negative gate pulse with the amplitude of 3 V, pulse width of 30 ms, and base level of 0.1 V. (f) Band diagrams of the TFT showing the ion movements in TaO_x layer in different stages.

base level of 0.1 V is applied to the bottom-gate. According to the polarity of the applied voltage and different responses of I_{DS} (Fig. 5. 2(e)), the status of the device could be categorized into three stages. The band diagrams in the three stages (positive bias, base level, and negative bias) are shown in Fig. 5. 2(f). The bandgap of the IGZO is around 3.2 eV; and the bandgap of TaO_x is around 3.7 eV. [233] At stage 1, the positive bias 5 V provides an external field, attracting negatively charged oxygen ions O^{2-} which exist in the as-deposited oxygen-deficient TaO_x layer to the TaO_x/bottom-

gate interface, and driving the oxygen vacancy ions V_o^{2+} in the TaO_x layer to the TaO_x/IGZO interface. [225],[234] These accumulated V_o^{2+} together with the large positive bias attract a large amount of electrons in the IGZO layer to the interface, contributing to the large EPSC spike. At stage 2, under the base level of 0.1 V, the segregated V_o^{2+} and oxygen ions (O^{2-}) start to recombine slowly with the nearly-zero external field. Still, there remain some V_o^{2+} near the interface, forming an internal field inside the TaO_x layer. The remaining V_o^{2+} keep attracting electrons in the IGZO layer to the interface, which slows down the EPSC decay. At stage 3, the negative bias -3 V accelerates the recombination of V_o^{2+} and O^{2-}, pulling the EPSC to an extremely low level.

To further evaluate the synaptic behaviours of the TFT, voltage pulses with different pulse widths, periods, and amplitudes are applied to the bottom-gate. Firstly, to investigate the short-term memory (STM) and its plasticity of the TFT, three experiments are conducted accordingly as described below, and all the results are summarized in Fig. 5. 3.

In the first experiment, four sets of 15 consecutive pulses with the same amplitude (5 V) and base level (0.1 V) are applied to the gate terminal. Each set of pulses has a different pulse width (50 μs, 500 μs, 1 ms and 10 ms), but the same duty ratio (50%). The first EPSC signal and fifteenth EPSC signal are denoted as A1 and A15, respectively. As shown in Fig. 5. 3(a), with the increase of the pulse width, the EPSC signal becomes stronger. The trend of A1 and A15 with the pulse width is depicted in Fig. 5. 3(c). When the pulse width increases from 50 μs to 1 ms, the EPSC

signals of both A1 and A15 and EPSC ratio of A15/A1 all increase gradually. There is a large increase in the EPSC signals of both A1 and A15 and EPSC ratio for the pulse width of 10 ms.

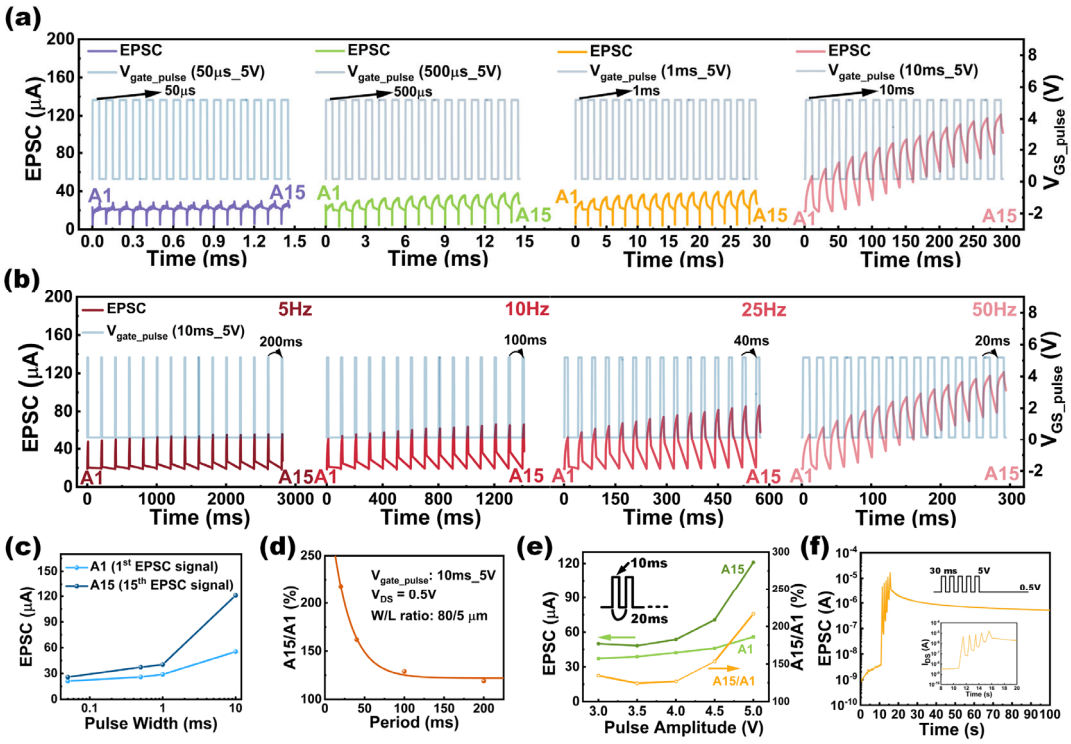


Fig. 5. 3 (a) EPSC under stimulation of 15 consecutive voltage pulses for different pulse widths. A1 and A15 denote the current spike in response to the 1st and 15th V_{GS} pulse, respectively. (b) EPSC under stimulation of 15 consecutive pulses for different pulse periods (pulse frequencies). (c) A1 and A15 EPSC signals vs. pulse width. (d) A15/A1 EPSC ratio vs. pulse period. (e) A1 and A15 EPSC signals and A15 / A1 EPSC ratio vs. pulse amplitude. (f) EPSC of the TFT under stimulation of 5 consecutive voltage pulses with pulse width of 30 ms, amplitude of 5 V and base level of 0.5V. The inset is the zoom-in region of the EPSC under 5 voltage pulses.

In the second experiment, four sets of 15 consecutive pulses with the same amplitude (5 V), base level (0.1 V), and pulse width (10 ms) are applied to the gate terminal; but the pulse frequency f_p is different for a different set of pulses (i.e., f_p is 5,

10, 25, and 50 Hz for the four sets of pulses, respectively). The A1 - A15 EPSC for different f_p is illustrated in Fig. 5. 3(b); and the relationship between the A15/A1 EPSC ratio and pulse period f_p^{-1} (= 20, 40, 100, and 200 ms) is shown in Fig. 5. 3(d). As the period of the pulse increases, the A15/A1 EPSC ratio decreases and remains almost unchanged for a period longer than 100 ms.

In the third experiment, five sets of 15 consecutive pulses with the same base level (0.1 V), pulse width (10 ms), and pulse period (20 ms) are applied to the gate terminal; but the amplitude of the pulses is increased from 3 V to 5 V with a step of 0.5 V. The result is shown in Fig. 5. 3(e). It can be observed from the figure that the A1 EPSC increases with the pulse amplitude gently, but both the A15 EPSC and A15/A1 EPSC ratio show a trend of large increase starting at 4 V. From the above three test schemes, the electrical pulse widths, periods, and amplitudes all show the capability to modulate the EPSC signal strength and STM retention time. The transition from STM to long-term memory (LTM) of the device is achieved with 5 consecutive pulses with amplitude of 5 V, pulse width of 30 ms, and base level of 0.5 V. Under the stimulation of the positive voltage pulses, the EPSC of the device lasts in high level for more than one minute as shown in Fig. 5. 3(f).

Besides STM plasticity, the capability to strengthen or weaken the EPSC signal in response to different activities is another important property of synapse, i.e., synaptic potentiation and depression (P/D). The most significant parameters to evaluate the P/D performance of the synapse are G_{max}/G_{min} ratio, non-linearity, and asymmetry of non-linearity between potentiation and depression. 1). G_{max}/G_{min} ratio is

the ratio of the maximum of EPSC and minimum of EPSC in the P/D in essence. Large G_{max}/G_{min} ratio (>10) is favourable which is the basis of high accuracy (>80%) of the neural network. [235] 2). Non-linearity α of P/D also determines the learning accuracy of the neural network. Usually, small α (<0.5~1) of the P/D means the weight change of the synapse under P/D is nearly linear, and the learning accuracy could exceed 80%. [236] 3). Asymmetry of α indicates the symmetric characteristics of the P/D, which is equal to the absolute difference value of α_P and α_D. Zero value of the asymmetry implies the perfect symmetric characteristics of P/D. [237]

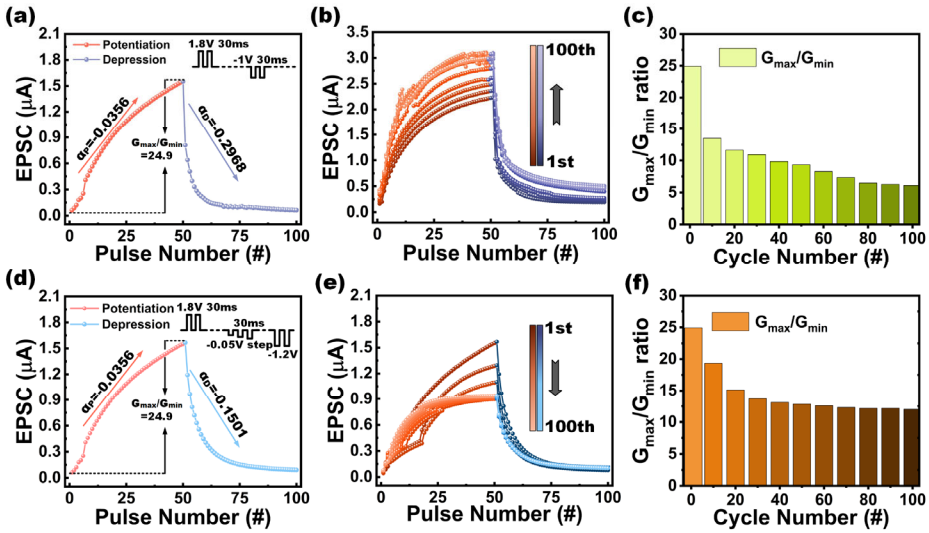


Fig. 5. 4 (a) P/D of the synapse under stimulation of 50 consecutive positive voltage pulses, followed by 50 consecutive negative voltage pulses. The base level of all pulses is fixed at 0.1 V. (b) Endurance of P/D under 100 cycles with the pulse schemes used in (a). (c) G_{max}/G_{min} ratio vs. P/D cycle with the pulse schemes used in (a). (d) P/D of the synapse under stimulation of 50 consecutive positive voltage pulses, followed by 50 consecutive negative voltage pulses with step-increasing amplitudes from 0.05 V to 1.2 V. The base level of all pulses is fixed at 0.1 V. (e) Endurance of P/D under 100 cycles with the pulse schemes used in (d). (f) G_{max}/G_{min} ratio vs. P/D cycle with the pulse schemes used in (d).

To verify whether the TFT could realize the synaptic P/D and evaluate the characteristics of P/D, 50 positive pulses with amplitude of 1.8 V, and pulse width of 30 ms, and negative pulses with amplitude of 1 V, and pulse width of 30 ms are applied to the gate terminal successively. The EPSC is read at the base level (0.1 V) of each pulse. As shown in Fig. 5. 4(a), the EPSC of the TFT increases from 62.16 nA to 1.55 μA under the repeated positive pulses and reduces back to 63.52 nA under the repeated negative pulses. The calculation of G_{max}/G_{min} ratio is straightforward, which is equal to 24.9. To derive the value of α_P (for potentiation) and α_D (for depression), the following exponential fitting model is adopted [238]:

$$G = \lambda \exp(\alpha x + \beta) + \gamma \tag{5.1}$$

In Equation (5.1), G is the conductance or EPSC value of the synapse, x is the number of pulse, α is the non-linearity of potentiation or depression, and λ, β, and γ are the fitting coefficients. Fitting to the experimental data is conducted in MATLAB. The fitting yields that α_P is -0.0356 and α_D is -0.2968. Correspondingly, the asymmetry $\left||\alpha_p| - |\alpha_D|\right|$ of the P/D under the proposed stimulation scheme is 0.2612. α_D is about 10 times higher than α_P, which results in a large asymmetry of the P/D. To evaluate the endurance of the synaptic behavior under stimulation of pure electronic pulses, 100 repeated P/D cycles are applied to the TFT. Fig. 5. 4(b) and (c) show the test results. Both G_{max} and G_{min} increase with P/D cycle, but G_{max}/G_{min} ratio decreases to lower than 10 after 50 cycles. It could be due to the inefficient depression by the negative pulses with fixed amplitude. To alleviate the extremely deteriorated

G_{max}/G_{min} ratio under repeated P/D cycles, reduce the absolute value of depression non-linearity and shrink the asymmetry of P/D, depression by 50 consecutive negative voltage pulses with step-increasing amplitudes is applied. [237] The amplitude of the negative pulses is set to 0.05 V initially, then it increases with a fixed step of 0.05 V till 1.2 V. The amplitude of the rest 26 pulses is fixed at 1.2 V. As shown in Fig. 5. 4(d), α_D is improved from -0.2968 to -0.1501; and thus, the asymmetry of P/D shrinks from 0.2612 to 0.1145. In Fig. 5. 4(e), the G_{max} of the P/D shows downwards shift with applied cycles, while the G_{min} shows little change. As shown in Fig. 5. 4(f), the G_{max}/G_{min} ratio is maintained at around 12 after 100 cycles. The gradual reduction of G_{max} suggests that there still exists slight charge-trapping effect due to the non-passivated defect states in the interface region.

5.3.2 Photoelectric synapse

Besides the pure electrical signal, light pulses with specific wavelengths could also inspire the synaptic behaviour of the TFT by changing carrier concentration in the IGZO layer. In this work, several illumination scenarios have been adopted to excite and modulate the EPSC in the TFT, i.e., UV light with the wavelength range of 300 ~ 400 nm, and visible light (i.e., blue, green, and red light with the wavelengths of 470 nm, 525 nm, and 633 nm, respectively), are used.

UV light is well known as a source to produce photon-generated electron-hole pairs in the IGZO TFT. The drain current I_{DS}, namely the EPSC, could be modulated at a low and fixed gate bias under UV illumination. To evaluate the STM plasticity

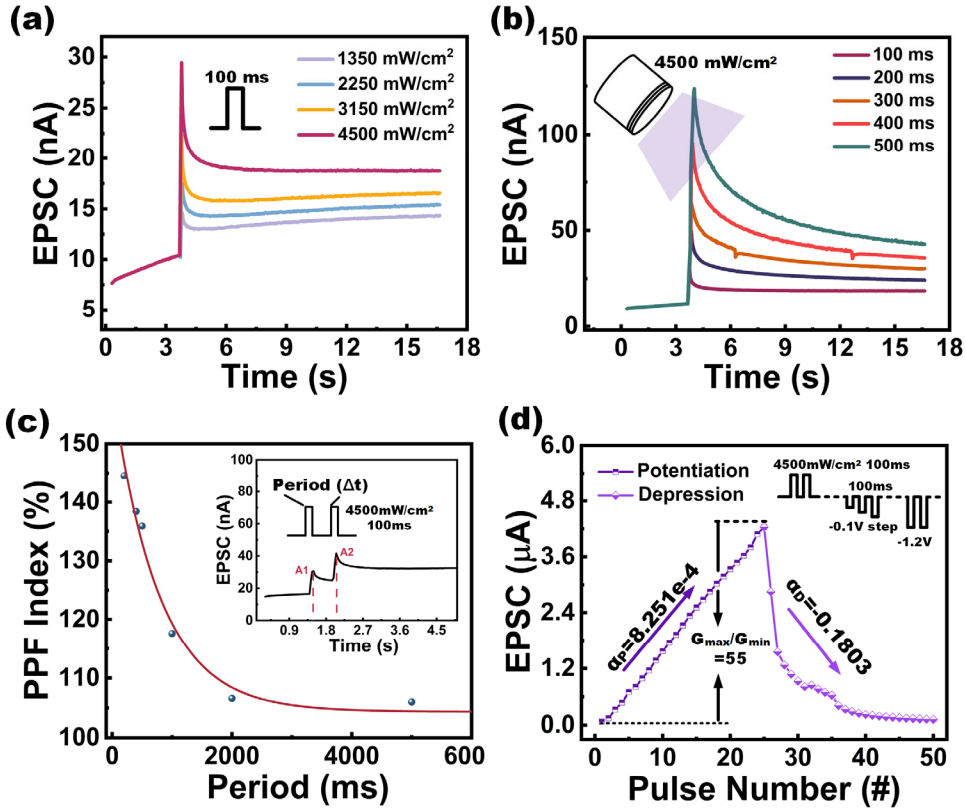


Fig. 5. 5 (a) EPSC of the TFT under stimulation of UV light pulses with various light intensities. (b) EPSC of the TFT under stimulation of UV light pulses various pulse widths. (c) PPF index of the TFT under stimulation of 2 consecutive UV light pulses with varying time interval (Δt). (d) P/D of the TFT under stimulation of 25 UV light pulses, followed by 25 negative gate voltage pulses with pulse amplitude increasing from 0.05 V to 1.2 V with a step of 0.1 V. The base level of all the voltage pulses is fixed at 0.1 V.

under photoelectric pulses, the UV light pulses with different irradiance and pulse widths are shone on the TFT. Fig. 5. 5(a) and (b) show the modulation of the EPSC signals by UV irradiation with various intensities (i.e., 1350, 2250, 3150 and 4500 mW cm^{-2}) and various UV pulse widths (i.e., 100, 200, 300, 400, 500 ms), respectively. As can be seen from the figures, higher UV irradiance and larger pulse width could both enhance the STM of the TFT. To investigate the paired pulse

facilitation (PPF) property of the TFT, the TFT is exposed to 2 consecutive UV pulses with the irradiance of 4500 mW/cm^2, pulse width of 100 ms and various time intervals (in terms of pulse period Δt = 200, 400, 500, 1000, 2000 and 5000 ms). A1 and A2 represent the first and second EPSC signals, respectively. The ratio of A2/A1 is defined as the PPF index, reflecting the STM plasticity of the synapse. Fig. 5. 5(c) depicts the PPF index vs. the time interval of the two pulses. The highest value of PPF index is 145% at the shortest time interval (i.e., Δt = 200 ms); and the PPF index decays with the increase of the time interval. Finally, the P/D property of the TFT is tested with successive 25 pulses of UV light followed by 25 pulses of negative gate bias. For potentiation, the UV light pulses have irradiance of 4500 mW/cm^2 and pulse width of 100 ms, and the base level is 0.1 V. For depression, negative gate voltage pulses are applied to the TFT with the pulse width of 100 ms and pulse amplitude increasing from 0.5 V to 1.2 V with fixed step of 0.1 V (the pulse amplitude is maintained at 1.2 V after it reaches 1.2 V), and the base level is 0.1 V. As shown in Fig. 5. 5(d), the potentiation of the TFT is realized with the EPSC increasing from 77 nA to 4.239 μA, achieving a large G_{max}/G_{min} ratio of 55; and the values of α_P and α_D obtained from the fittings based on Equation (5.1) are 8.521×10^{-4} and -0.1803, respectively. The asymmetry of the P/D is 0.1795. The 25 successive UV illumination pulses with the base level of 0.1 V have successfully inspired potentiation of the synaptic transistor with nearly zero non-linearity, which facilitates the proposed TFT to be applied in neural network with ultra-high accuracy under photoelectric mode.

Furthermore, 10 cycles of repeated P/D test are carried out on the device, and the result shows good endurance and reproducibility (Fig. 5. 7(a)).

In the visible light experiment, blue, green, and red light with the wavelengths of 470 nm, 525 nm, and 633 nm, respectively, are used. The light pulses with luminous flux of 3955 lm and pulse width of 400 ms are applied to the TFT. The EPSC signals for the three wavelengths are shown in Fig. 5. 6(a). The EPSC signal becomes weaker

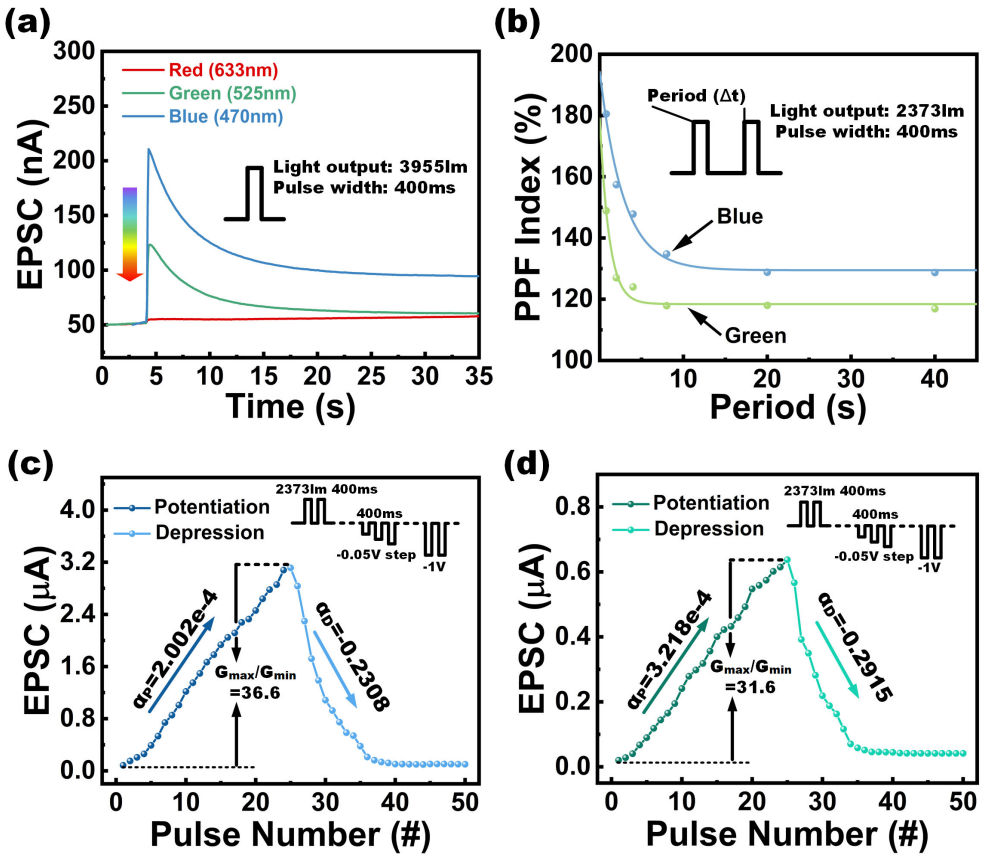


Fig. 5. 6 (a) EPSCs of the TFT under stimulation of visible light pulses with the wavelengths of 470, 525 and 633 nm. (b) PPF indexes of the TFT under stimulation of 2 consecutive blue or green light pulses with various time intervals. P/D of the TFT under the stimulation of 25 consecutive pulses of blue light (c) or green light (d), followed by 25 negative gate voltage pulses with pulse amplitude increasing from 0.05 V to 1 V with a step of 0.05 V. The base level of all the voltage pulses is fixed at 0.1 V.

with a longer light wavelength. There is almost no EPSC signal for the red light illumination. The PPF property of the TFT is characterized by applying 2 consecutive blue or green light pulses with 2373 lm, pulse width of 400 ms and various time intervals (the period Δt = 0.8, 1.6, 4, 8, 20, and 40 s). Fig. 5. 6(b) shows that the PPF index decreases with the increase of time interval under the stimulation of 2 consecutive blue or green light pulses. At the shortest time interval (Δt = 0.8 s), the PPF index reached the highest level of 148% under the green light pulses, and 180% under the blue light pulses. Fig. 5. 6(c) and (d) demonstrate the potentiation of the TFT under the stimulation of 25 consecutive blue and green light pulses, respectively; and they also show the depression of the TFT under 25 consecutive negative gate voltage pulses. Some relevant results can be obtained from Fig. 5. 6(c) and (d), as described in the following. The G_{max}/G_{min} ratios achieved by the stimulation of blue and green light pulses are 36.6 and 31.6, respectively (note that the red light pulses are not able to produce significant EPSC). The values of α_P and α_D are obtained from the fittings based on Equation (5.1). For the P/D inspired by the blue-light pulses/negative gate voltage pulses, α_P and α_D are 2.002×10^{-4} and -0.2308 respectively; for the P/D inspired by the green-light pulses/negative gate voltage pulses, they are 3.218×10^{-4} and -0.2915, respectively. The asymmetry of the P/D is 0.2306 for the blue light pulses and 0.2913 for the green light pulses. On the other hand, 10 repeated P/D cycles with blue and green light pulses stimulation are conducted to examine the endurance of the P/D. The results are shown in Fig. 5. 7(b) and (c). The G_{max} of the potentiation slightly decreases with the P/D cycle under the stimulation of blue light

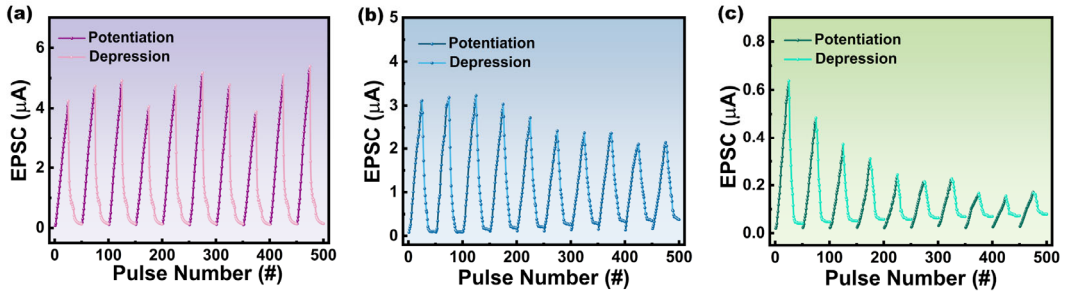


Fig. 5. 7 P/D endurance under 10 repeated cycles of the TFT under the stimulation of UV light pulses (a), blue light pulses (b) and green light pulses (c).

pulses, but deteriorated fast with the P/D cycle under the stimulation of green light pulses. A comparison of P/D characteristics among the different stimulation schemes (including pure electronic pulses and photoelectric pulses) is summarized in Table 5. 1. It should be noted that # refers to the pulse number; $\left||\boldsymbol{\alpha_p}| - |\boldsymbol{\alpha_D}|\right|$refers to the asymmetry in the table.

As discussed above, both UV and visible light pulses show the capability to trigger the synaptic behaviors in the TFT. There is an obvious wavelength selectivity of the EPSC signal as shown in Fig. 5. 6(a). Light intensity, pulse width and period show a high controllability on the EPSC signal of the TFT (Fig. 5. 5(a)-(c), and Fig. 5. 6(b)). Potentiation is achieved by the stimulation of consecutive photoelectric pulses (i.e., light illumination plus a small positive gate bias); and depression is achieved by the stimulation of consecutive negative voltage pulses. UV light owns over-band photo-energy ($h\upsilon$>3.2 eV) to excite electrons from the VB to CB in IGZO directly, generating electron-hole pairs. [185] On the other hand, blue and green lights with high light intensity could generate electron-hole pairs in intrinsic sub-gap defect states and

excite electrons from the defect states to the conduction band. [132] These photon-generated electrons are attracted to the IGZO/TaO_x interface under the influence of positive gate bias and contribute to the production of EPSC. At the light-off state, the positive base level (0.1 V) drives the ion movement in TaO_x, which provides an internal electric field inside the dielectric layer to keep attracting electrons to the IGZO/TaO_x interface. At the same time, those sub-gap defect states are ionized and turned to be a hole trap center under illumination. [132] Photon-generated holes are trapped in the ionized defect states, leading to a photo-gating effect under the collective stimulation of light illumination and positive bias. [228],[239] The photo-gating effect could contribute to the long-term potentiation in the photoelectric synapse. When a negative bias is applied to the gate terminal, oxygen ions recombine with oxygen vacancies in the TaO_x layer, causing the vanish of the internal electric field. At the same time, the negative bias expelled the accumulated electrons away, the EPSC drops back to the pristine low level.

Table 5. 1 Comparison of P/D characteristics among different stimulation schemes

External pulse	#	$\frac{G_{max}}{G_{min}}$	$\lvert\alpha_P\rvert$	$\lvert\alpha_D\rvert$	$\lvert\lvert\alpha_p\rvert - \lvert\alpha_D\rvert\rvert$	**Endurance**
Electronic	50	24.9	3.56×10^{-2}	0.1501	0.1145	Good
UV	25	55	8.25×10^{-4}	0.1803	0.1795	Good
Blue	25	36.6	2.00×10^{-4}	0.2308	0.2306	Fair
Green	25	31.6	3.22×10^{-4}	0.2916	0.2913	Poor

5.4 Summary

This chapter introduces an IGZO TFT with simple structure showing synaptic behaviors in either pure electric mode or photoelectric mode. Thanks to the high dielectric constant and strong ion conductivity of the TaO_x dielectric, as well as the sensitivity of IGZO to light illumination, I_{DS} of the TFT has successfully emulated a series of synaptic behaviors, like STM plasticity, STM transition to LTM, and long-term P/D under various stimulation schemes. For P/D, UV-photoelectric pulses have inspired the G_{max}/G_{min} ratio as large as 55; blue-photoelectric pulses have inspired the smallest non-linearity of potentiation as low as 2.002×10^{-4}; negative pulses with step-increasing amplitude in the pure electronic mode have inspired the smallest non-linearity of depression as low as 0.1501. The TFT demonstrated in this work is promising to be applied in 1) the large-area wearable patten recognition system with high learning accuracy (>80%) due to the good uniformity of the IGZO and low-temperature fabrication process for the whole device, 2) the vision-based neuromorphic computing system with high learning accuracy (>80%) under the stimulations of blue or green pulses.

Chapter 6. 1T1R array based on integration of IGZO TFTs and HfO_2-based ReRAMs

The work reported in this chapter aims to construct a 1T1R cell by integrating a HfO_2-based resistive random-access memory (ReRAM) and a high-performance IGZO TFT, which is promising for large-area applications such as flexible electronic circuits. Here one of the major concerns is that the compliance current (CC) required for the formation of stable and strong conductive filaments in the forming and set processes as well as the maximum current required in the reset process in a large-size ReRAM should be lower than that the maximum current of a TFT can deliver. In this chapter, an IGZO TFT is fabricated with S/D contacts of a Ti/Au/Ti/Pt-multilayer structure, showing high driving current, large μ_{FE}, low leakage current, and good stability under hot carrier stress (HCS). On the other hand, an ultrathin Al_2O_3 layer (2 nm) is inserted between the HfO_2 switching layer and the reactive Ti layer of the top electrode in the ReRAM with the structure of Pt (bottom electrode)/HfO_2/Al_2O_3/Ti/TiN (top electrode). With the ultrathin Al_2O_3 layer, the forming voltage of the ReRAM is reduced largely, and the CC for stable forming and set operations and $I_{reset,max}$ can reach a reasonable current level that the IGZO TFT is able to provide; meanwhile the device-to-device variation of the forming operation and cycle-to-cycle resistance variations of the set and reset operations for the ReRAM are improved significantly. Finally, the 8×8 1T1R array is fabricated based on the above optimized IGZO TFTs and HfO_2-based ReRAMs, and the TFT succeeds in

providing different CC levels for the forming, set, and reset operations in the ReRAM.

6.1 Introduction

Oxide-based resistive random-access memory (ReRAM) is emerging as a next generation non-volatile memory (NVM) for various applications, such as embedded NVM [240], storage-class memory [224],[241], and neuromorphic computing [242]. Typically, a ReRAM cell is in the form of 1T1R structure, i.e., it consists of one ReRAM device and one transistor (i.e., MOSFET). For examples, a high-performance 2-Mbit TaO_x-based ReRAM with 1T1R structure was reported in 2015 [223], and a 14nm-FinFET 1Mb embedded 1T1R ReRAM with a 0.022μm^2 cell size was reported recently [243]. Besides MOSFET fabricated with CMOS process, TFT based on metal oxides (e.g., amorphous IGZO) can be also used to form the 1T1R structure for large-area applications. IGZO TFT is a mature technology with the advantages of low cost, high optical transparency, and good uniformity as emphasized in the former chapters. The integration of ReRAM with IGZO TFT has various potential large-area applications, such as memory-in-pixel (MIP) [244]-[246], flexible electronics [247],[248], and wearable devices [249],[250].

Compared with the conventional MOSFET with a large μ_{FE} (i.e., a few hundreds of cm^{2}V/s [251]), generally, μ_{FE} of IGZO TFT is only in the range of tens of cm^2/Vs. Therefore, the driving current of IGZO TFT is smaller than that of MOSFET, for example, it was reported that the driving current of IGZO TFT was less than 1 mA even with a very large channel W/L ratio (i.e., 1000/5 μm) under the bias conditions

of 5 V V_{GS} and 5 V V_{DS} [247]. In the 1T1R structure, the driving current of the TFT would limit the compliance current (CC) required for the formation of stable conductive filaments in the forming and set processes as well as the maximum current in the reset process in the ReRAM. For low-cost large-area electronic applications, the size of ReRAM devices is usually large (e.g., in the scale of 100 μm). For large-size ReRAM devices, the above-mentioned currents are generally larger than 1 mA. For examples, for a Pt/Al:HfO_2/TiN ReRAM device with 100 nm Pt electrode, the CC used in the set operation and the maximum current in the reset operation were about 5 mA [252]; for the HfO_x-based ReRAM devices with a diameter of 100 μm, the CC used in the set operation and the maximum current in the reset operation were also several mA [253]. Thus, for the application of the integration of IGZO TFT with ReRAM in large-area thin-film circuits, one of the major concerns is that the CC required for the formation of stable and strong conductive filaments in the forming and set processes as well as the maximum current required in the reset process in the ReRAM should be lower than the maximum current that the TFT can provide.

To address the above concern, on the one hand, an IGZO TFT with a Ti/Au/Ti/Pt-multilayer S/D structure is fabricated. The bottom Ti layer provides a good ohmic contact with the IGZO layer, which contributes to the large μ_{sat} and high driving current of the TFT. The top Pt layer can serve as the bottom electrode (BE) for the integration with the ReRAM. Likewise, the TFT transfer characteristics are stable under the collective stress of large V_{GS} and V_{DS}.

On the other hand, an ultrathin Al_2O_3 layer (2 nm) is inserted between the HfO_2

switching layer and the reactive Ti layer of the top electrode (TE) in the ReRAM with the structure of Pt (BE)/HfO_2/Al_2O_3/Ti/TiN (TE). With the insertion of the ultrathin Al_2O_3 layer, the forming voltage is reduced largely, and the CC for stable forming and set operations and maximum reset current ($I_{reset,max}$) are at a low current level that the IGZO TFT can provide; while the switching variability under the set/reset conditions is improved largely. The improvements by the insertion of the ultrathin Al_2O_3 layer are attributed to the reaction between the Ti layer and the Al_2O_3 layer. The Ti layer serves as an oxygen getter layer, which reacted with both the ultrathin Al_2O_3 layer and the HfO_2 switching layer. The reaction between the Ti layer and the ultrathin Al_2O_3 layer produces some Al ions. In the forming process, the Al ions could migrate to dope the HfO_2 switching layer under the influence of positive bias at the top electrode. The doping of Al in HfO_2 decreases the formation energy of oxygen vacancies [254] and thus reduces the forming voltage. At the same time, oxygen vacancies would easily gather around the dopants to improve the resistive switching stability [252],[255]. Additionally, the ultrathin Al_2O_3 layer also serves as an electron tunnelling barrier, which largely suppresses the currents during the switching processes. Such large reduction in the currents is useful to the applications of large-area devices.

In the final, an 8×8 1T1R array which integrates the above high-performance IGZO TFTs and Al_2O_3-inserted HfO_2-based ReRAMs is fabricated and demonstrated successfully.

6.2 Device fabrication and characterization

6.2.1 Fabrication of standalone IGZO TFT

To evaluate the basic FOMs of the TFT with the proposed multilayer S/D structure, single IGZO TFTs were fabricated on the ITO-coated glass with BGTC structure. The fabrication process was the same as described in **section 3.1**, except for the deposition of S/D electrodes which was finished by e-beam evaporation in the sequence of Ti (20 nm)-Au (120 nm)-Ti (20 nm)-Pt (20 nm). The as-fabricated TFT was annealed in 300 ℃ N_2 environment for 1 h to stabilize the carrier concentration in the IGZO layer. The 3D schematic of the single IGZO TFT is shown in Fig. 6. 1(a).

6.2.2 Fabrication of standalone HfO_2-based ReRAM

The ReRAM with the structure of Pt (bottom electrode)/HfO_2/Al_2O_3/Ti/TiN (top electrode) was fabricated on Si substrate. Firstly, 20 nm Pt thin films was deposited by e-beam evaporation as the bottom-electrode (BE) layer. A 6 nm HfO_2 layer was deposited as the resistive switching layer by using ALD with the precursor of Tetrakis (dimethylamino) hafnium (TDMAH) and oxidant of H_2O at 250 ℃. To study the effect of an ultrathin Al_2O_3 layer, an Al_2O_3 layer with the thickness of 2 nm was deposited on the HfO_2 layer in the same ALD chamber with the precursor of TMA and oxidant of H_2O at 250 ℃. Finally, a 6 nm Ti layer and a 100 nm TiN layer were deposited sequentially by sputtering to form a reactive metal layer and the top-electrode (TE) layer, respectively. The UV-lithography technique and lift-off process were used to produce the ReRAM structure which has a cylinder shape with diameter of 100 μm. Fig. 6. 1(b) shows the 3D schematic of the reference ReRAM without the

Al_2O_3 insertion layer (upper) and ReRAM with the 2 nm Al_2O_3 insertion layer (lower).

6.2.3 Fabrication of 1T1R array

The 8×8 1T1R array was developed on Si substrate. To provide good electrical insulation, a layer of 390 nm SiO_2 was formed by thermal oxidation. Before the TFT bottom gate deposition, 200 nm troughs (gate lines and pads) were formed by the reactive ion etching (RIE Oxford Plasmalab80), which were patterned by UV-lithography. Then, 20 nm Ti, 160 nm Au were deposited by e-beam evaporation in sequence. The replacement of the gate-electrode material from ITO to Au was to

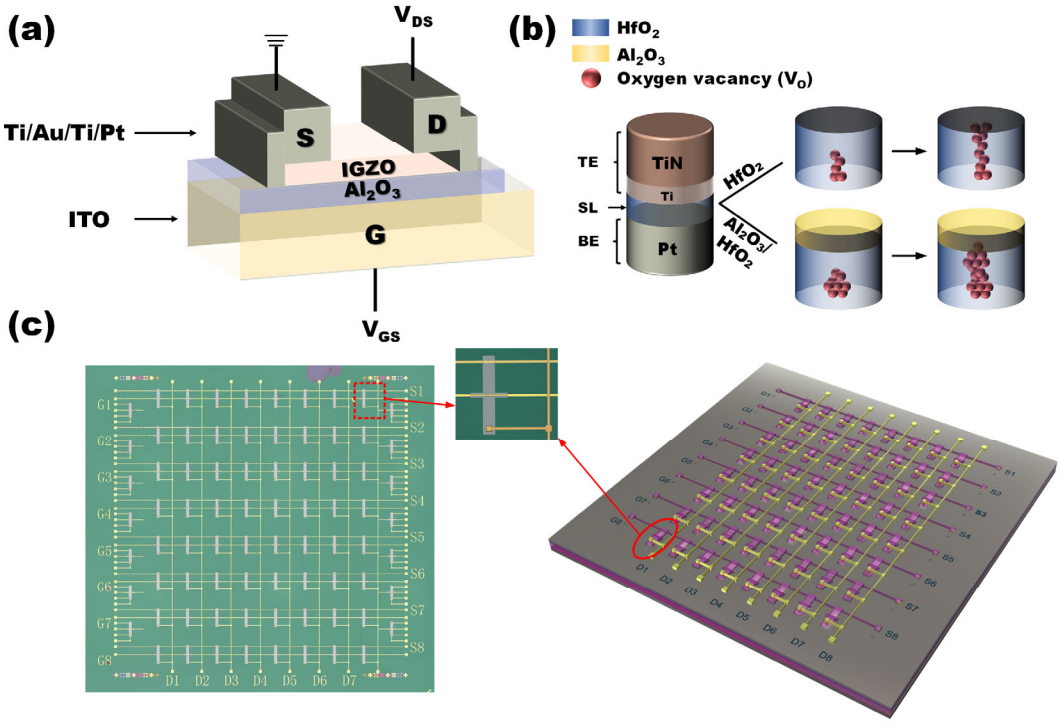


Fig. 6. 1 (a) Schematic of the IGZO TFT with Ti/Au/Ti/Pt S/D contacts. (b) Schematic of the HfO_2-based ReRAM with and without the 2 nm Al_2O_3 tunnelling layer. (c) Optical microscope image of the top view (left) and schematic (right) of the 8×8 1T1R array. The inset is the optical microscope image of one of the 1T1R cells in the 8×8 1T1R array.

reduce the resistance of the gate lines. Subsequently, a layer of 40 nm Al_2O_3 was grown by ALD as the dielectric for TFTs. For the channel layer, 45nm IGZO was deposited by RF magnetron sputtering with the same recipes. To form the S/D contacts, 20 nm Ti, 120 nm Au, 20 nm Ti and 20 nm Pt were deposited layer by layer using e-beam evaporation. The W/L ratio of all TFTs in the array were defined as 600/20 μm. To connect all the source electrodes in each row, 20 nm Ti and 100 nm Au were deposited in sequence by e-beam evaporation as the source line. The overlap of the source lines and bit lines was unavoidable, which could cause large leakage current. Thus, a layer of 100 nm SiO_2 was grown by PECVD to reduce the overlap effect, which functioned as the passivation layer for the TFT as well. Then, post-annealing at 300 ℃ N_2 atmosphere was conducted for 1 h to 1). reduce the defect states at the channel/dielectric interface, 2). alleviate the hydrogen diffusion from the PECVD-deposited SiO_2. To integrate ReRAM with TFT, a square via was opened on the drain electrode by RIE with an area of 50×50 μm. Switching layer for the ReRAM consisted of 6 nm HfO_2 and 2 nm Al_2O_3 which were both grown by ALD. Next, 6 nm Ti/100 nm TiN was deposited by sputtering as the TE of the ReRAM. Lastly, to connect all the TEs in each column, 8 lists of bit line (20 nm Ti/100 nm Au) were grown with the same process of the source lines. Fig. 6. 1(c) shows the optical microscope image of the top view (left) and 3D schematic (right) of the 1T1R array.

Transfer characteristics and output characteristics of the TFTs and memory operations (including forming, set, and reset processes) of the ReRAMs were all measured with Keithley 4200 SCS analyzer.

6.3 Results and discussion

6.3.1 Performance of standalone IGZO TFT

The TFT with a W/L ratio of 40/2 μm is picked for the measurement of transfer curves and output curves. To measure the transfer curve, V_{GS} is sweeping from -5 V to 10 V, and V_{DS} is set to 0.1 V, 1.1 V, and 10.1 V for the TFT working in the linear and saturation region, respectively. To measure the output curve, V_{DS} is sweeping from 0 to 10 V, and V_{GS} is set to 5 V, 7 V, and 10 V, respectively. Fig. 6. 2(a) and (b) show the

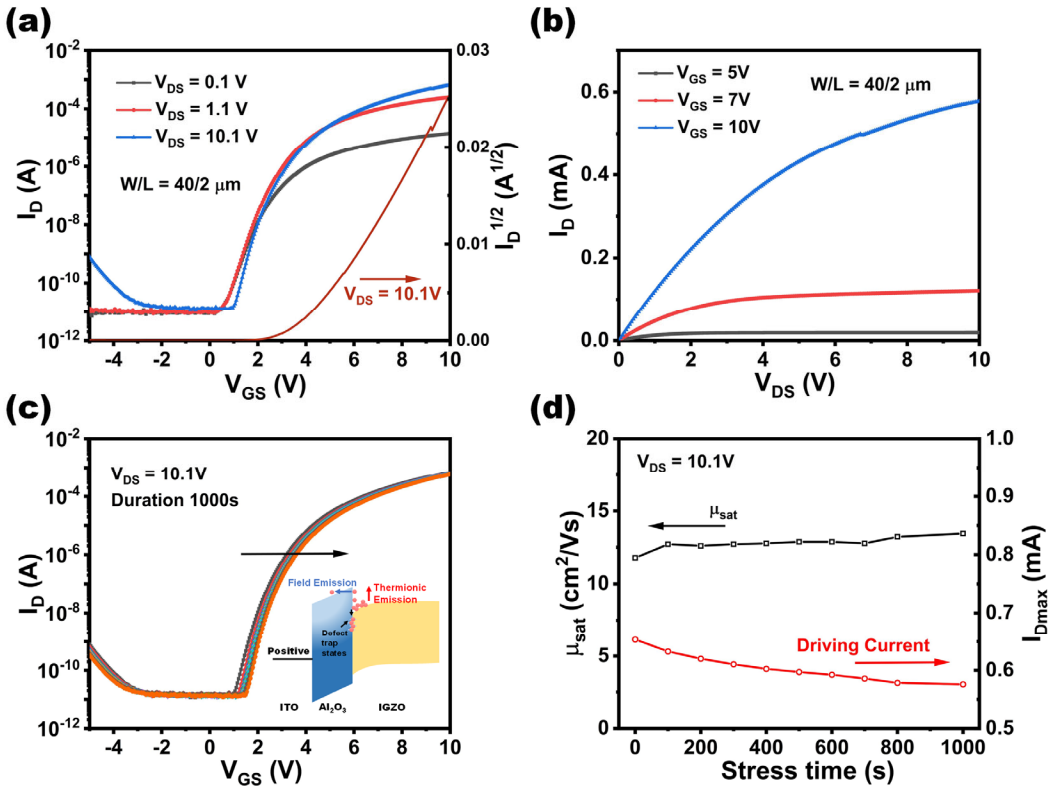


Fig. 6. 2 (a) Transfer curves of the TFT at V_{DS} = 0.1, 1.1, and 10.1 V, respectively. (b) Output curves of the TFT at V_{GS} = 5, 7, 10 V, respectively. (c) Transfer curves of the TFT under self-heating stress for 1000 s. (d) μ_{sat} vs. stress time (left) and I_{Dmax} vs. stress time.

transfer curves and output curves of the TFT, respectively. The right-side y-axis of Fig. 6. 2(a) represents the square root value of I_D, which means to calculate μ_{sat} of the TFT at V_{DS} = 10.1 V based on Equation (2.10). From these two curves, S.S. of the TFT is derived to be 349 mV/dec, V_{th} is 4.45 V, μ_{sat} is calculated to be 11.78 cm^2/Vs, and the maximum driving current I_D at V_{GS} = 10 V and V_{DS} = 10 V is 0.65 mA. The maximum I_D (I_{Dmax}) can be further improved by capping a passivation layer which introduces hydrogen diffusion into IGZO. It will be discussed in **section 6.3.3** with the passivated TFT.

On the other hand, to provide sufficient current flow for the memory operations of ReRAM, large V_{GS} and V_{DS} are always biased to the TFT, which could induce the serious charge-trapping effects due to the self-heating stress. [256],[257] When large current is flowing through the channel layer under large V_{DS}, joule heat would be produced. Electrons inside IGZO would be driven towards shallower barriers with the thermionic emission. Then these electrons are more inclined to be trapped in the dielectric with field emission. To evaluate the reliability of the TFT under such stress, V_{GS} with a fixed value of 5 V and V_{DS} with a fixed value of 10 V are collectively applied to the TFT for 1000 s. The transfer curves of the TFT at V_{DS} = 10.1 V are sampled with a time step of 100 s. As shown in Fig. 6. 2(c), there is a small positive shift of the transfer curve. Likewise, the relationships of μ_{sat} versus stress time and I_{Dmax} versus stress time are depicted in Fig. 6. 2(d) at the left- and right-side of the y-axis, respectively. It is obvious that the concurrent stress of V_{GS} and V_{DS} shows no impact on μ_{sat} of the TFT, and causes a tolerant and slight decrease of I_{Dmax} of the TFT. In conclusion, the TFT with

Ti/Au/Ti/Pt S/D contacts shows good electrical performance and stability which is qualified to drive ReRAMs in the 1T1R array.

6.3.2 Performance of standalone HfO_2-based ReRAM

A DC voltage sweep from 0 to 6 V is carried out to perform the forming process on the ReRAM with 100 μA CC that is found to be large enough for creating stable conductive filaments (CFs) to connect the TE and BE. In the forming operation, the TE (Ti/TiN) is positively biased, and the BE (Pt) is grounded. The typical I-V characteristics of the ReRAM devices without and with the ultrathin Al_2O_3 layer in the forming operation are shown in Fig. 6. 3(a). As can be observed from the figure, the forming voltage is reduced largely by the ultrathin Al_2O_3 layer. To examine the device-to-device variation in the forming voltage, 8 devices are randomly picked out for both the ReRAMs with and without the ultrathin Al_2O_3 layer to run the forming process. For the group of ReRAMs without the ultrathin Al_2O_3 layer, the mean value of the

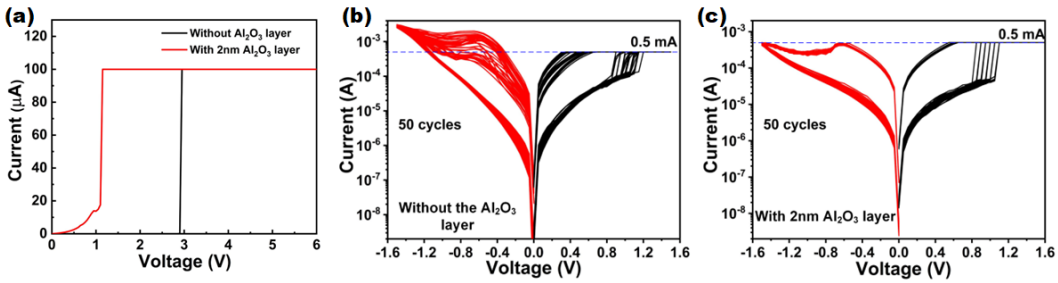


Fig. 6. 3 (a) Typical I–V characteristic of the forming operation with the CC of 0.1 mA for the ReRAMs without and with the ultrathin Al_2O_3 layer. I-V curves of the set and reset operations of the ReRAMs without the ultrathin Al_2O_3 layer (b) and with the ultrathin Al_2O_3 layer (c) for 50 DC sweeping cycles. The CC for the set operation is 0.5 mA.

forming voltage is 3.22 V, and the coefficient of variation (CoV), which is defined as the ratio of the standard deviation to the mean value, is 48%. In contrast, for the group of ReRAMs with the ultrathin Al_2O_3 layer, the mean value of the forming voltage is largely reduced to 1.26 V, and the CoV is also largely reduced to 21%. Obviously, the ultrathin Al_2O_3 layer can reduce both the forming voltage and device-to-device variation largely.

A plausible explanation to the above phenomena observed in the forming process is given in the following. Ti is known to have a high solubility for oxygen, which could react with both the ultrathin Al_2O_3 layer and the HfO_2 switching layer. [256] The reaction between the Ti layer and the ultrathin Al_2O_3 layer produces some Al ions. In the forming process, the Al ions could migrate to dope the HfO_2 switching layer under the influence of positive bias at the TE. The doping of Al in HfO_2 decreases the formation energy of V_O and thus reduces the forming voltage. [255],[258] During the forming process, V_O could be generated in both the Al_2O_3 layer and the HfO_2 layer. CFs are mainly formed in the HfO_2 switching layer (Fig. 6. 1(b)), while the ultrathin Al_2O_3 layer serves as an interfacial layer because of the relatively higher Gibbs free energy of Al_2O_3 (-1088.2 kJ/mol for HfO_2, -1582.3 kJ/mol for Al_2O_3). [259]. At the same time, V_O would relatively easily gather around the Al dopants to improve the resistive switching stability. [253],[258] As a result, the random nature of resistive switching is supressed, and thus the device-to-device variation in the forming voltage is reduced.

In the set and reset operations, a DC voltage sweeping from 0 to 1.5 V and from

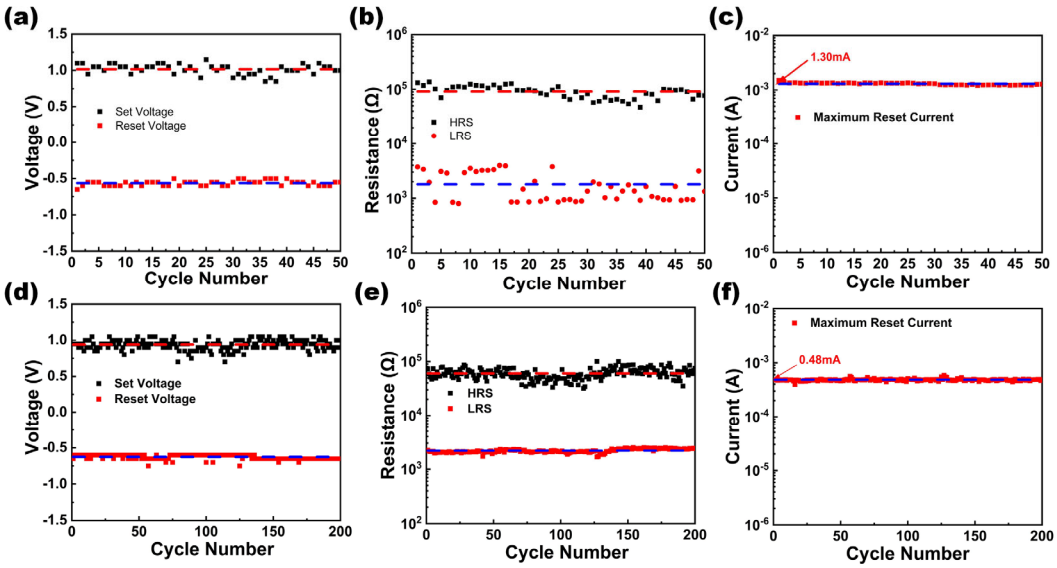


Fig. 6. 4 Cycle-to-cycle variations for the ReRAM without the ultrathin Al_2O_3 layer under 50 DC set/reset cycles: (a) V_{set} and V_{reset}; (b) resistances of the LRS and HRS; and (c) $I_{reset,max}$. Cycle-to-cycle variations of the ReRAM with the ultrathin Al_2O_3 layer under 200 DC set/reset cycles: (d) V_{set} and V_{reset}; (e) resistances of the LRS and HRS; and (f) $I_{reset,max}$. The lines represent the mean values.

0 to -1.5 V is applied to the TE, respectively, while the BE is grounded. To ensure the TFT could drive the ReRAM in the 1T1R cell, the CC for the set operation is set at 0.5 mA that is found to be large enough for stable set operation. The high resistance state (HRS) resistance and low resistance state (LRS) resistance are measured at 0.1 V DC voltage. Fig. 6. 3(b) and (c) show the I-V curves of the set and reset operations of the ReRAMs without and with the ultrathin Al_2O_3 layer for 50 DC sweeping cycles. The set and reset voltages and $I_{reset,max}$ which corresponds to the reset voltage are obtained from the I-V curves. From Fig. 6. 3 (b) and (c), $I_{reset,max}$ of the ReRAM with the ultrathin Al_2O_3 layer is significantly lower than that of the ReRAM without the ultrathin Al_2O_3 layer, i.e., the average $I_{reset,max}$ is 0.48 mA and 1.30 mA for the

ReRAMs with and without the ultrathin Al_2O_3 layer, respectively. On the other hand, cycle-to-cycle variations in the I-V characteristics are also largely reduced by the introduction of the ultrathin Al_2O_3 layer.

Cycle-to-cycle variations of the ReRAMs are examined. Fig. 6. 4 shows the cycle-to-cycle variations for the ReRAM without the ultrathin Al_2O_3 layer under 50 DC set/reset cycles (Fig. 6. 4(a)-(c)) and the ReRAM with the ultrathin Al_2O_3 layer under 200 DC set/reset cycles (Fig. 6. 4(d)-(f)). The results shown in these figures indicate that the introduction of the ultrathin Al_2O_3 layer largely reduces the cycle-to-cycle variation for the HRS resistance and LRS resistance while the set voltage (V_{set}) and reset voltage (V_{reset}) as well as $I_{reset,max}$ exhibit small cycle-to-cycle variations in both devices. The HRS and LRS resistances and $I_{reset,max}$ exhibit a small decrease in their magnitudes in the device without the ultrathin Al_2O_3 layer after 50 DC set/reset cycles; in contrast, the device with ultrathin Al_2O_3 layer does not show such phenomenon even after 200 DC set/reset cycles. To quantitatively analyse the cycle-to-cycle variations of the resistive switching, Table 6. 1 shows comparison of the

Table 6. 1 Comparison of COVs for cycle-to-cycle variations of various parameters between the ReRAMs with and without the Al_2O_3 layer

Device structure	**V_{set}**	**V_{reset}**	**LRS**	**HRS**	**Memory window**	**$I_{reset,max}$**
without the Al_2O_3 layer	6.6%	12.5%	59.3%	25.0%	36.5%	11.4%
with the Al_2O_3 layer	6.1%	11.2%	3.6%	3.6%	22.3%	5.1%

COVs of various memory parameters between the two devices. A major observation from Table 6. 1 is that the COVs for both the LRS resistance and HRS resistance are significantly reduced by the introduction of the ultrathin Al_2O_3 layer (from 59.3% to 3.6% for the LRS; from 25.0% to 17.1% for the HRS). This translates to a reduction of the COV of the memory window from 36.5% to 22.3% of the device with introduction of the Al_2O_3 layer. On the other hand, the COVs of V_{set} and V_{reset} show only small difference between the devices without and with the Al_2O_3 layer, while the COV of $I_{reset,max}$ shows a relatively large reduction from 11.4% to 5.1% with introduction of the Al_2O_3 layer.

To explain the large reduction of COVs for both the LRS resistance and HRS resistance, the Al ions doping as discussed in the forming process is also taking effect. Stable CFs can be formed along the Al-doped sites, thus uniform set/reset behaviors are expected. [258] However, except the stable CFs formed along the Al-doped sites, there are still other CFs formed by V_O in other undoped lattice sites in the HfO_2 layer which behave similarly to the CFs formed in the ReRAM without the ultrathin Al_2O_3 layer. In other words, the filamentary conducting paths include the CFs formed along the Al-doped sites, and in the un-doped regions in the HfO_2 layer. Therefore, the introduction of the ultrathin Al_2O_3 layer would reduce the COVs for both the LRS resistance and HRS resistance, but it could not eliminate the variations completely.

By comparing Fig. 6. 4(a) with Fig. 6. 4(d), one can conclude that the there is no large difference in V_{set} and V_{reset} between the ReRAMs with and without the insertion of the insulating barrier layer Al_2O_3. In other words, the electric fields in the HfO_2

layer required for the set/reset process in the ReRAM can be lower after the insertion of the ultrathin Al_2O_3 layer. This could be explained in terms of relatively easy generation of V_O and recombination of V_O with O^{2-} in the set and reset processes in the ReRAM with the ultrathin Al_2O_3 layer. According to [260], either a lower energy barrier (E_a) for generating V_O or a higher local electric field increases V_O generation probability; and a lower O^{2-} hopping energy barrier (E_h) or a higher local electric field increases the probability of an O^{2-} hopping to recombine with V_O (i.e., rupture of the CF involving the V_O). As discussed early, Al doping in the HfO_2 layer reduces the formation energy of V_O at the Al-doped sites, which could be interpreted as a reduction in the E_a. The reduction of the E_a compensates with the reduction of the electric field in the set process in the HfO_2 layer in the ReRAM with the ultrathin Al_2O_3 layer. This explains the small difference in the V_{set} between the ReRAMs without and with the ultrathin Al_2O_3 layer. On the other hand, Al doping could reduce the energy barrier (E_m) for Vo migration. [255] Reduction in E_m can be translated to a reduction in the above-mentioned E_h. The reduction of the E_h also compensates with the reduction of the electric field in the HfO_2 layer in the reset process in the ReRAM with the ultrathin Al_2O_3 layer. This explains the small difference in the V_{reset} between the ReRAMs without and with the ultrathin Al_2O_3 layer.

Based on the above discussions, the resistive switching processes are mainly determined by the electric fields in the HfO_2 layer. On the other hand, for the ReRAM with the ultrathin Al_2O_3 layer, the electron transport between the TE and BE is limited by the ultrathin Al_2O_3 layer which is basically still an insulating layer although there

are some V_O generated in the Al_2O_3 layer. In the HfO_2 layer, there are many V_O which form trap levels inside the energy bandgap of the HfO_2 layer. Under influence of external electric field, electrons could easily travel via the trap levels via the processes like trap-assisted tunnelling and Poole-Frenkel emission. [261] In contrast, the ultrathin Al_2O_3 layer forms a tunnel barrier for electron transport, i.e., electrons travel across the Al_2O_3 layer via direct tunnelling [261] under the influence of the voltage dopped in the Al_2O_3 layer. As electrons could easily travel via the V_O in the HfO_2 layer, the electron transport between the TE and BE is limited by the tunnelling process across the Al_2O_3 layer. This explains the phenomenon that the introduction of the ultrathin Al_2O_3 layer largely reduces the $I_{reset,max}$. In the present study, with the device diameter of 100 μm, the ReRAM without the ultrathin Al_2O_3 layer has an $I_{reset,max}$ of larger than 1 mA; in contrast, the ReRAM with the ultrathin Al_2O_3 layer has an $I_{reset,max}$ of only ~ 0.5 mA. Such large reduction in the current is useful to be integrated with IGZO TFTs and form 1T1R array in large-area applications.

6.3.3 Demonstration of 1T1R array

The optimization techniques applied in **section 6.3.1** for IGZO TFTs and **section 6.3.2** for HfO_2-based ReRAMs are proved to be effective. However, the device characteristics would vary from the standalone status to the integration status. Fig. 6. 5 shows the transfer curves and output curves of the IGZO TFT of one of the 1T1R cells in the 8×8 1T1R array. The transfer curves are measured with V_{GS} sweeping from -15 V to 15 V, and V_{DS} at 0.1 V and 1 V, respectively. The output curves are

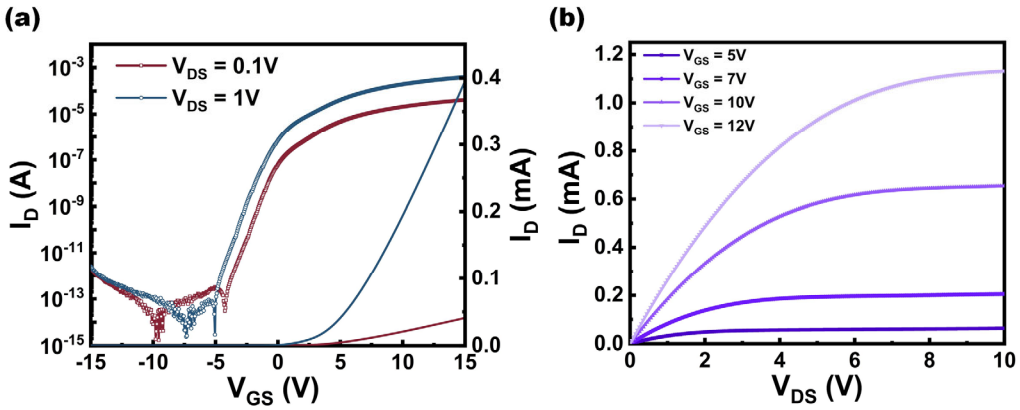


Fig. 6. 5 (a) Transfer curves of the IGZO TFT of one of the 1T1R cells in the 8×8 1T1R array at V_{DS} = 0.1 V and 1 V, respectively. (b) Output curves of the IGZO TFT of one of the 1T1R cells in the 8×8 1T1R array at V_{GS} = 5, 7, 10, and 12 V, respectively.

measured with V_{DS} sweeping from 0 to 10 V, and V_{GS} at 5, 7, 10, and 12 V, respectively. From these two figures, FOMs of the IGZO TFT are extracted as the following. I_D on/off ratio of at V_{DS} = 0.1 V and 1 V is 9.9×10^8 and 6.4×10^9, respectively. V_{th} is 4.57 V. S.S. is 544 mV/dec. μ_{FE} is 8.19 cm^2/Vs. The maximum driving current of the TFT can reach 1.13 mA at V_{GS} = 12 V and V_{DS} = 10 V, as shown in Fig. 6. 5(b). It is obvious that I_D increases compared with that measured in the standalone IGZO TFT as discussed in **section 6.3.1**. It could benefit from the deposition of 100 nm SiO_2 deposition layer, which injects hydrogen into IGZO during deposition and increases the carrier concentration in the TFT.

To form CFs in the ReRAM in the 1T1R cell, the test configuration changes with three probes respectively placed at the source terminal of the TFT connecting with ground, the gate terminal of the TFT providing voltage to change the conductance of IGZO, and the TE of the ReRAM providing DC sweep voltages to accomplish the

memory operations including forming, set and reset for the ReRAM. When V_{GS} is at low level, the IGZO channel resistance is extremely high with an ultra-low leakage current (Fig. 6. 5(a)). At this condition, a large proportion of the voltage between the grounded source terminal and TE of the ReRAM (V_{TE_S}) will be applied to the IGZO channel instead of the HfO_2 switching layer. Thus, no memory operation will be executed in the ReRAM. When V_{GS} is leveled up, resistance of the IGZO channel is decreased, and the voltage distribution between the channel of the TFT and the switching layer of the ReRAM will change. As discussed in **section 6.3.2**, when the electric field applied to the ReRAM increases under the DC sweep of V_{TE_S}, V_O starts to be generated, and CFs are formed eventually. To realize this forming process, V_{GS} is set to 5 V, and V_{TE_S} is sweeping from 0 to 8 V in the 1T1R structure. Fig. 6. 6

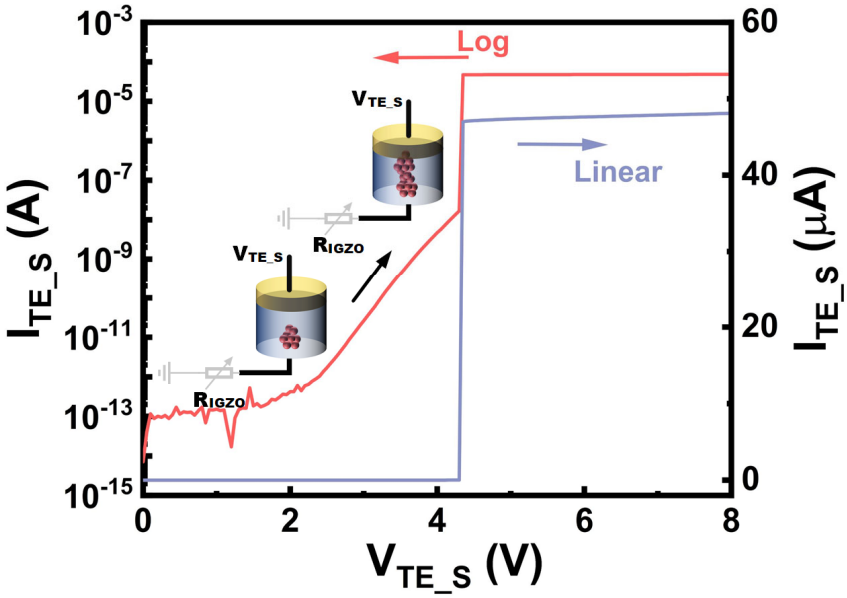


Fig. 6. 6 Forming process of the ReRAM driven by the IGZO TFT in one of the 1T1R cells in the 8×8 1T1R array at V_{GS} = 5 V

shows the forming process of the ReRAM with integration of the IGZO TFT. Note that the current flowing through the ReRAM is represented by I_{TE_S}. As shown in the figure, I_{TE_S} starts to increase at V_{TE_S} = 1.4 V, where CFs in the ReRAM start to grow. Then at V_{TE_S} = 4.35 V, I_{TE_S} abruptly increases to 47 μA, i.e., CFs are successfully formed between TE and BE (drain of the TFT) in the ReRAM. After the forming process, set and reset processes for the ReRAM are tested with and without the incorporation of the IGZO TFT, respectively. The results are demonstrated and discussed in the following.

For the individual ReRAM regardless of the IGZO TFT, the I-V measurements are carried out with two probes placed at the TE and BE (drain of the IGZO TFT), respectively. Fig. 6. 7(a) shows the I-V curves of the ReRAM under set and reset processes with 200 DC cycles. Voltage between the TE and BE (V_{TE_BE}) is sweeping from 0 to 1.5 V for set operation, while from 0 to -1.5 V for reset operation. It can be observed that the ReRAM has small variations of the set and reset processes in terms of either V_{set}/V_{reset} or HRS/LRS. As shown in Fig. 6. 7(b), the HRS resistance and LRS resistance are both maintained with small fluctuations and the memory window ratio is derived to be 5.4 on average with 200 DC cycles.

For the ReRAM driven by the IGZO TFT, the I-V measurements are carried out with the same configuration of the forming process. V_{GS} is set to 10 V to further decrease the resistance of IGZO and provide higher CC for the ReRAM. Fig. 6. 7(c) shows the I-V curves of the integrated ReRAM under set and reset processes with 10 DC cycles. V_{TE_S} is sweeping from 0 to 8 V for the set operation, while it is sweeping

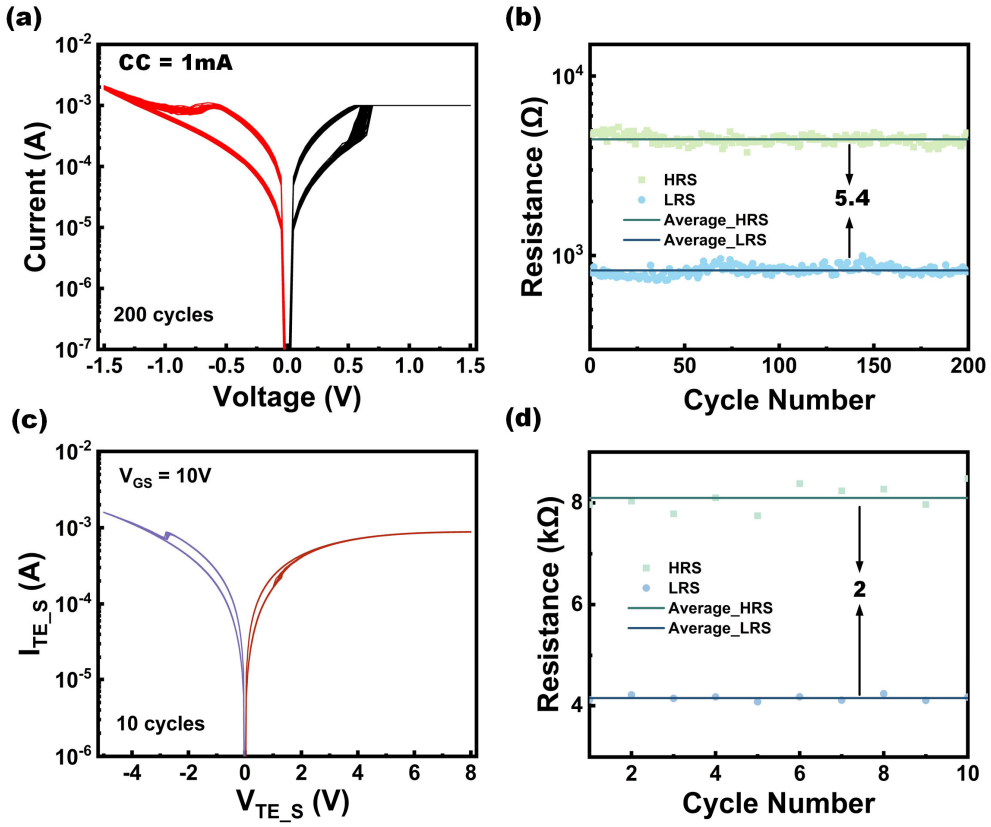


Fig. 6. 7 (a) I-V curves of the set and reset operations of the individual ReRAM for 200 DC sweeping cycles. (b) Cycle-to-cycle variations of the HRS/LRS resistance for the individual ReRAM. (c) I-V curves of the set and reset operations of the integrated ReRAM in one of the 1T1R cells in the 8×8 1T1R array for 10 DC sweeping cycles. (d) Cycle-to-cycle variations of the HRS/LRS resistance for the integrated ReRAM in one of the 1T1R cells in the 8×8 1T1R array.

from 0 to -5V for the reset operation. Also, the set and reset processes both show small variations. However, as shown in Fig. 6. 7(d), the memory window ratio is shrunk from 5.4 to 2. The shrinkage of window ratio comes from the voltage distribution of the IGZO channel. From Fig. 6. 5(b), the resistance of IGZO R_{IGZO} is around 4.5 kΩ at V_{GS} = 10 V and V_{DS} = 0.1 V. From Fig. 6. 7(b), the HRS resistance and LRS resistance of the ReRAM is 4.4 kΩ and 827 Ω, respectively. After involving

the IGZO TFT in the set/reset process of the ReRAM, the window ratio becomes the ratio of $(R_{IGZO}+R_{HRS})/(R_{IGZO}+R_{LRS})$, which is reduced from 5.4 to 2 naturally. To enlarge the window ratio, resistance match between the IGZO at on state and the ReRAM at HRS/LRS is the most important issue to be solved. One of the author's major future works is to find a ReRAM collectively owning high resistance and small operation variations and realize large memory window ratio in the 1T1R array.

6.4 Summary

In this chapter, the standalone high-performance IGZO TFT with multi-stack S/D contacts and HfO_2-based ReRAM with ultrathin Al_2O_3 tunneling layer inserted between the TE and HfO_2 layer are fabricated. The IGZO TFT shows high saturation mobility (μ_{sat}), large driving current, and good reliability under collective stress of large V_{GS} and V_{DS}. On the other hand, with the introduction of the ultrathin tunneling layer, the HfO_2-based ReRAM shows largely reduced forming voltage and device-device variation. The cycle-to-cycle variations of HRS/LRS resistance, V_{set}/V_{reset}, and memory window ratio of the ReRAM are largely reduced under small CC (0.5 mA) for the ReRAM with the ultrathin Al_2O_3 layer as well. Ultimately, the 8×8 1T1R array based on IGZO TFTs and HfO_2-based ReRAMs is fabricated and demonstrated. Before being applied in embedded memory technologies, the 1T1R array in this work still needs to be improved from two aspects: 1). Solve the mismatch between the on-resistance of IGZO and HRS/LRS of ReRAM. 2). Yield of ReRAM should be improved further which is around 1/10 currently.

Chapter 7. Conclusion and Recommendations

7.1 Conclusion

Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistor (TFT) has been emerging in recent decades thanks to its high electron mobility, low leakage current, low thermal budget of its fabrication process, and good uniformity in large-area applications. However, with the rapid development of next-generation display technologies with larger display area and higher resolution, and other advanced applications like embedded memory for IoTs, wearable electronics, etc., the higher driving current, larger electron mobility, faster switching speed, and better reliability under various external stresses are required for the IGZO TFT. In this thesis, the improvements of IGZO TFT performance and advanced applications based on IGZO TFTs have been achieved by employing various techniques which target at different layers of the TFT (i.e., S/D contacts, channel layer, and dielectric layer). Detailed summaries for each chapter are stated in the following.

- In Chapter 3, Ti was found to provide the most ideal contact characteristics for IGZO TFT among different S/D metals. Insertion of an ultrathin Ti layer between the bulk of ITO and the IGZO channel layer has successfully enhanced the carrier mobility by three times and reduced the contact resistance by three times. Instabilities of the IGZO TFTs under different external stresses (PBS/NBS, PBIS/NBIS, PBTS/NBTS) were also characterized and systematically discussed.

- In Chapter 4, a transparent IGZO TFT with high electron mobility and driving current was realized by a sputtered-deposited AlO_x passivation layer. The deposition of the passivation layer has induced an In-rich interfacial layer at the back surface of the IGZO layer, which largely increased the carrier concentration. Consequently, μ_{FE} of the TFT was increased from 6.292 to 69.01 cm^2/Vs, and I_D on/off ratio was enlarged from 1.3×10^7 to 1.87×10^8 compared with the TFT without passivation. The demonstrated TFT is promising for applications in need of high driving current and low power consumption.
- In Chapter 5, a transparent synaptic IGZO TFT was fabricated based on TaO_x dielectric. Thanks to the high-κ (42.6) and ion-conductivity of the TaO_x. Different pulse schemes (including pure electronic and photoelectric pulses) applied to the gate of the TFT has successfully inspired various synaptic behaviors like EPSC, STM plasticity, STM transition to LTM, and P/D. Notably, P/D under stimulation of either pure electric pulses or photoelectric pulses showed large G_{max}/G_{min} ratio (>10) and extremely small non-linearity ($\alpha<0.5$), making the transparent synaptic IGZO TFT promising to be applied in the large-area and vision-based neuromorphic computing systems with high learning accuracy.
- In Chapter 6, an 8×8 1T1R array was demonstrated based on high-performance IGZO TFTs and HfO_2-based ReRAMs. The TFT showed high performance with μ_{sat} of 11.78 cm^2/Vs, driving current of 0.65 mA, and good reliability under the collective stress of large V_{GS} and V_{DS}. On the other hand, ultra-thin Al_2O_3 (2 nm) tunnelling layer was inserted between the TE and HfO_2 in the ReRAM, which

largely reduced the forming voltage and device-to-device variation of forming voltage for the ReRAM. Also, the ReRAM with the inserted tunnelling layer showed much smaller cycle-to-cycle variations in the HRS/LRS resistance, V_{set}/V_{reset} and memory window under 0.5 mA CC. Finally, in the 1T1R array which integrated the above TFTs and ReRAMs, memory operations were successfully demonstrated. However, the memory window can be further enlarged by increasing the HRS/LRS resistance of the ReRAM.

7.2 Recommendations for future work

The following future works based on IGZO TFTs are recommended.

1) Our research shows that IGZO TFT can be used as a synaptic device as discussed in chapter 5. In the future, different suitable ion-conductive materials that can be used in the TFT should be explored to optimize the synaptic behaviors and further reduce the non-linearity asymmetry and enhance the endurance of P/D of the TFT under stimulation of successive pulses. In addition, synaptic TFT arrays can be fabricated to realize pattern recognition with high learning accuracy.

2) 1T1R array demonstrated in chapter 6 can be optimized by increasing the HRS and LRS resistances of the ReRAM. Our on-going research shows that insertion of an ultrathin tunnelling layer (0.5 ~ 1 nm) between the BE and HfO_2 is able to increase the resistances, improve the yield, and maintain good memory performance of the ReRAM. 1T1R array with better performance should be fabricated using the above improved ReRAM technology in the future.

3) Charge-trapping flash memory based on IGZO TFTs can be further investigated. Different charge trapping layer will be applied in the TFT. For instance, SiO_x deposited by reactive sputtering has potential to accommodate Si nanocrystals after annealing process. These nanocrystals can serve as charge-trapping sites in the dielectric layer and cause the non-volatile shift of V_{th}. The discrete nanocrystals can improve the write/erase cycling endurance and increase data retention time. Also, IGZO layer can be crystallized by annealing at 400 ~ 500 ℃. The crystalline IGZO is possible to be used as the charge-trapping layer, improving the endurance of programmed/erased states of the TFT.

4) Dynamic random-access memory (DRAM) based on 2T structure can be investigated and fabricated. '2T' refers to a structure combining two IGZO TFTs, in which one TFT is for program/erase operation and another TFT is for charge storage. By virtue of the high-κ of dielectric layer in the charge-storage TFT, the retention of the charge stored in the TFT can be improved, and thus the refresh interval of the memory will be prolonged. The prolonged refresh interval and ultra-low leakage current of the IGZO TFTs will collectively contribute to the low power consumption of the DRAM.

5) A systematic simulation and modelling study based on IGZO TFT can be conducted. A good physical compact model for IGZO TFT is crucial for researchers to clearly understand the intrinsic behaviors of IGZO TFT in different working environment.

Publications

1. **Yuanbo Li**, Jianxun Sun, Teddy Salim, Rongyue Liu, and Tupei Chen. "Performance Enhancement of Transparent Amorphous IGZO Thin-Film Transistor Realized by Sputtered Amorphous AlO_x Passivation Layer." April 2021, *ECS Journal of Solid State Science and Technology* 10 (4). DOI: 10.1149/2162-8777/abf724.

2. **Yuanbo Li**,[=] Jun Zhang,[=] Jianxun Sun, and Tupei Chen. "A Large-Size HfO_2 Based RRAM Structure Suitable for Integration of One RRAM with One InGaZnO Thin Film Transistor for Large-Area Applications." November 2021, *ECS Journal of Solid State Science and Technology* 10 (11). DOI:10.1149/2162-8777/ac3ad1.

3. **Yuanbo Li**, Tupei Chen, Xin Ju, and Teddy Salim. "Transparent Electronic and Photoelectric Synaptic Transistors Based on the Combination of an InGaZnO Channel and a TaO_x Gate Dielectric." July 2022, *Nanoscale* 14. DOI:10.1039/d2nr02136f.

4. **Yuanbo Li**, Rongyue Liu, Jianxun Sun, Jun Zhang, and Tupei Chen. "Improvement of Transparent IGZO Thin-Film Transistors Performance with Ti/ITO Bilayer as Source and Drain," in *International Conference on Materials for Advanced Technologies*, 2019.

5. Jianxun Sun, **Yuanbo Li**, Yiyang Ye, Jun Zhang, Gang Yih Chong, Juan Boon Tan, Zhen Liu, and Tupei Chen. "3D Geometric Engineering of the Double Wedge-Like Electrodes for Filament-Type RRAM Device Performance Improvement." December 2019, *IEEE Access* 8. DOI: 10.1109/ACCESS.2019.2962869.

6. Kejun Wu, Jun Zhang, **Yuanbo Li**, Xiangzhan Wang, Yang Liu, Qi Yu, and Tupei Chen. “Design of AM Self-Capacitive Transparent Touch Panel Based on a-IGZO Thin-Film Transistors.” April 2020, *IEEE Access* 8. DOI:10.1109/ACCESS.2020.2989435.

7. Rongyue Liu, Ying Chen, Shuyu Ding, **Yuanbo Li**, and Yong Tian. “Preparation of Highly Transparent Conductive Aluminum-Doped Zinc Oxide Thin Films Using a Low-Temperature Aqueous Solution Process for Thin-Film Solar Cell Applications.” December 2019, *Solar Energy Materials and Solar Cells* 203. DOI:10.1016/j.solmat.2019.110161.

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