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Process and Device Characterisation of Advanced SOI Devices

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SUMMARY OF THESIS

SOI technologies offer solutions to low power, high performance applications. The key device-architecture issue is the choice between partially depleted and fully depleted devices. While each structure has pros and cons, the choice needs to be balanced between process complexity and performance. Thereafter, engineers have ventured into some non-classical transistor structures will likely take over due to their delivery of higher performance with lower leakage than traditional scaled SOI CMOS approaches. The possibility of using a back gate have sparked a large research activity in the field of novel SOI devices. Among all other multiple gate design, it is well known that Gate-All-Around (GAA) MOSFET offers the most attractive properties for digital application. GAA MOSFET is being examined as extension of planar CMOS technology with potential to increase performance and packing density over the conventional technique. Besides that, the novel n-gate device is an improvised triple-gate structure to address the "early turn on" effect that is caused by the presence of the corner transistors between the promixty of two gates forming together. Both design take advantage of the concept of volume inversion to achieve: higher current, enhanced tranconductance, ideal subthreshold swing and attenuated short channel effects. Hence, the goal of this work is to investigate and develop fabrication technology for quadruple-gate (hereby called Double-gate-all-around) MOSFET and the novel n-gate device. It focuses on the process and device characterization of such advanced SOI devices. Most importantly, the process proposed in this work to fabricate such devices is compatible with standard bulk CMOS manufacturing.

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CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

In the 2003 edition of the International Technology Roadmap for Semiconductor (ITRS), the concept of device scaling has been consistently endorsed in meeting high performance and low power consumption requirement in Ultra Large Scale Integrated (ULSI) circuits. The physical gate length has been scaled by approximately 30% at every generation and such trend (see Figure 1.1) has followed the Moore's Law, which states that the number of transistors doubles about every 18 months.

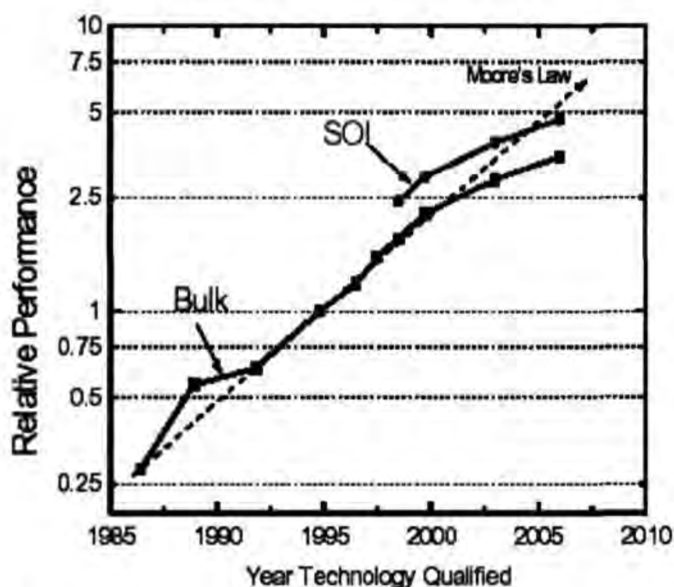

Figure 1.1: Moore's chart: SOI will cause a jump in performance road map.

Aggressive scaling of the gate length in high performance applications however makes sub-micron device parameter optimization quite difficult, especially with the pace quickening in recent technologies, as denoted in Figure 1.2. The formation of ultra-shallow junction to suppress the short channel effects (SCE) cannot be attained without incurring a significant increase of parasitic junction capacitance.

The doping of devices involves precise profile design and process control, but increasing channel doping concentration degrades carrier mobility and hence the

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lowering of drain current. Moreover, the statistical fluctuation of channel dopants causes an increasing variation of threshold voltage, thereby posing difficulty in the circuit design, not to mention further complication during scaling of supply voltage. Gate insulator, on the other hand, becomes thinner due to the requirement for rapid switching speed improvement. Excessive gate leakage through the ultra-thin oxides is a major concern at below ~15 Å.

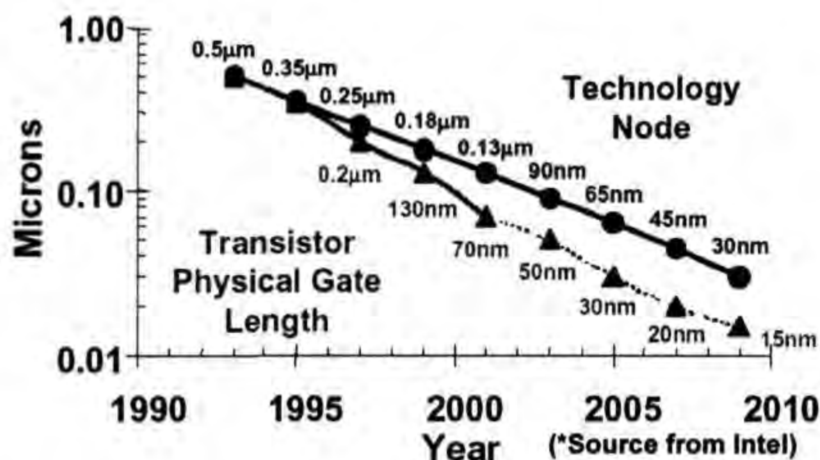

Figure 1.2: Transistor Physical Gate Length Trend (Lithography generation > L_{gate})

Tremendous effort has been put forth in seeking innovative development to sustain the growth of the ULSI industry in the nano-generation. Presently, engineers are considering other viable resolutions- one that is compatible with existing wafer processes, able to provide superior device and circuit performance than bulk silicon, allows smaller linewidth definition, and the reduction of number of mask level for a given design. The Silicon On Insulator (SOI) technology offers such capability and is therefore the focus of this project.

Sometime within the next ten years, some non-classical SOI transistor structures will likely to emerge due to their delivery of higher performance with lower off state leakage than the traditional scaled SOI CMOS approaches. In fact, research

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laboratories in industry and academia have explored several promising SOI device architectures [1] to improve on the scalability and performances of the transistors in upcoming generations. These include the single gate depleted-substrate transistor (DST) [2], double- gate FinFET and the tri-gate transistor [3]. All three devices utilize a fully depleted substrate and can be used to improve short channel performances [4]. Table 1.1 summarizes the advantages and manufacturing challenges of some of these structures.

Table 1.1: Non classical CMOS device characteristics.

Non-Classical CMOS Devices					
Device	Ultra Thin Body (UTB) Transistor	Band-Engineered Transistor	Vertical Transistor	FinFET	Double-Gate Transistor
Concept	Fully-Depleted SOI (FDSOI)	SiGe or Strained Si channel; bulk Si or SOI	Double-gate or surround-gate structure		
Advantages	Improved subthreshold slope; V_t controllability	Higher drive current; compatible with bulk Si and SOI	Higher drive current; lithography-independent L_g	Higher drive current; improved subthreshold slope; improved short-channel effect (SCE)	
Scaling Issues	Si Film thickness; gate stack; worse SCE than bulk CMOS	High mobility film thickness (SOI); gate stack; integratability	Si film thickness; gate stack; intergratability; process complexity; accurate TCAD including quantum mechanical(QM) effect		Gate alignment; Si film thickness; gate stack; intergratability; process complexity
Design Challenges	Device characterization ; compact model and parameter extraction	Device characterization	Device characterization;PD versus FD; compact model and parameter extraction; applicability to mixed signal applications		

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1.2 OBJECTIVES

The aim of this project is to fabricate two types of novel 3 dimensional (3D) SOI MOSFET devices, namely the n-gate and Gate-All-Around (GAA) CMOS device. The following describes the objectives of this project:

1) Literature review on various kinds of SOI device structure extending from basic planar design to non classical 3D SOI device structures. The pros and cons of each design are also discussed extensively in this work.

2) To design and develop the novel n-gate SOI device structure using the 0.13 μm technology node.

3) To realize a patent filed by Chartered Semiconductor Manufacturing Limited, whereby a GAA SOI device structure is to be fabricated using the 0.13 μm technology.

4) To investigate and develop the SOI fabrication technology using the existing bulk CMOS process technique. This includes the SOI process characterization and recipe optimization to cater to non planar SOI MOSFETs fabrication.

5) To study the above mentioned 3D SOI MOSFET on its electrical performances and behaviours.

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1.3 MAJOR CONTRIBUTION OF THE THESIS

The tri-gate structure developed recently by Intel has shown many attractive electrical properties [3]. Unfortunately, it suffers from early turn-on effect due the higher current density at the edges [5]. It causes a "hump" in the operating voltage and gives rise to unstable threshold performance. Hence, a new n-gate structure concept is introduced in this thesis to address the problem. The design utilizes an additional step to round the corners of the tri-gate for improved threshold behaviour. In addition, the n-gate sidewalls are extended into the buried oxide to shield the back of the channel region from the electric field lines directed from the drain. In this way, an almost perfect shielding like an actual back gate can be achieved.

The second half of the thesis will account for the development of the GAA device structure. GAA MOSFET has been demonstrated to have the potential to be the highest performing MOSFET for digital application [6]. They exhibit most attractive properties among all other MOSFET variations such as having high transconductance, reduced short-channel effect as well as allowing a steep and nearly ideal subthreshold slope [1][4]. The Gate-all-around (GAA) controls roughly 4 times as much current as a single gate (see Figure 1.3), hence giving stronger switching signals respectively.

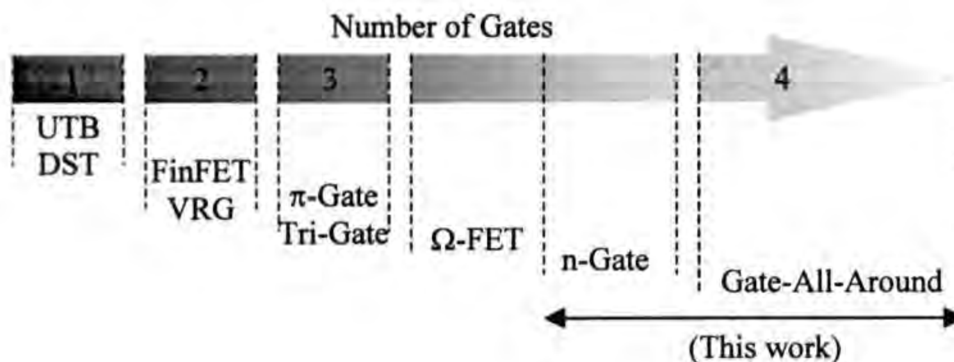

Figure 1.3: Proposed Device Structure

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1.4 ORGANIZATION OF REPORT

The introductory chapter 1 gives a general introduction and discusses the advantages of emerging SOI technology. The focuses of the thesis are also stated.

Chapter 2 provides a clear illustration of the silicon-on-insulator (SOI) material, before moving on to discuss the differences between the thick and thin films and the partially or fully depleted SOI films. The advantages and drawbacks of each approach will be examined. This section also includes discussion on basic transistor design choices and the different types of novel 3D CMOS structures.

Chapter 3 presents the concept of a Double Gate-All-Around (DGAA) device with gate wrapping at all the sidewalls of the silicon channel and a newly proposed corner rounded n-gate device respectively. Apart from the superior advantages over bulk CMOS devices, key benefits of the proposed structure will also be highlighted in this section. The schematic process flow of each structure will be illustrated.

Chapter 4 describes the preparation and process fabrication with designed gate length of down to 0.13 μm. The process issues and concerns will be discussed in detailed. Chapter 5 concludes the preliminary studies and lists the results and findings obtained.

Lastly, Chapter 6 summarizes the conclusions derived from the study and gives an outlook on possible further development of the research work.

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CHAPTER 2: LITERATURE REVIEW ON SOI TECHNOLOGY AND DEVELOPMENT

This chapter describes the various approaches for producing Silicon-On-Insulator (SOI) materials and highlights the distinct differences among the thick and thin film SOI devices. The basic device structures and non planar SOI devices found in SOI CMOS technologies are also presented extensively with coverage on the advantages and drawbacks of each approach.

2.1 SOI WAFER FABRICATION

The SOI wafer is made up of a thin silicon film lying above an insulating material with the bottom substrate acting as a handling wafer. The aim is to fabricate device on the top silicon film such that the body is electrically isolated from the substrate for better electrical properties such as the latch up immunity and reduced short channel effects. This electrical insulating region is typically made of silicon dioxide (SiO_2) and is known as the buried oxide (BOX). The BOX structure can be formed by using one of three following techniques: SIMOX [7], Bonded SOI [8] or Smart Cut [9].

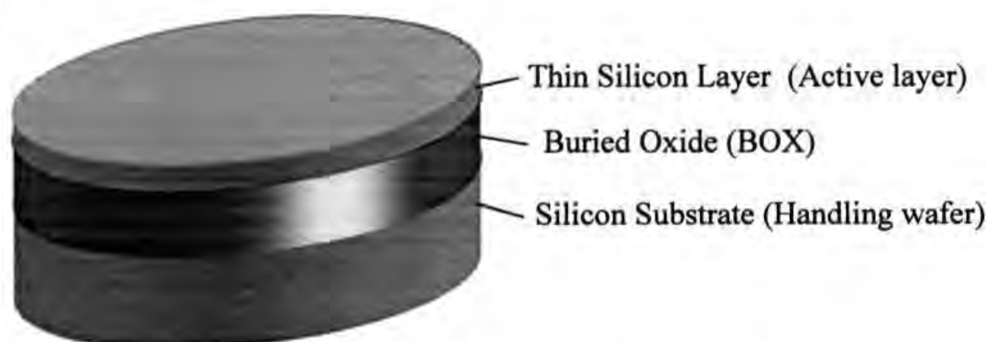

Figure 2.1: Silicon On Insulator (SOI) wafer.

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2.1.1 SIMOX

SIMOX stands for Separation by IMplantaion of Oxygen [7]. As shown in Figure 2.2, this technique uses a high energy oxygen O_2 implant that ranges from 4×10^{17} to 2×10^{18} cm^{-2} and is performed on an epitaxial wafer to force a massive dose of oxygen deep beneath the surface. The energy used is typically 100-200 keV. The buried oxide thickness varies with different doping concentration and the implant energy will determine the top silicon thickness. Upon completion, a high temperature anneal (>1300 °C) is carried out preferably in an argon ambient to activate the buried oxide layer and recrystallize the top silicon film which is heavily damaged during the earlier ion bombardment. The quality of the surface silicon can be further improved by optimizing the temperature ramping conditions [10]. Recently, much attention has been oriented towards the usage of low-energy and dose implantation as an economical perspective to produce thin film SOI wafers. Besides that, low dose SIMOX wafers have significant reduced defect density and better BOX uniformity.

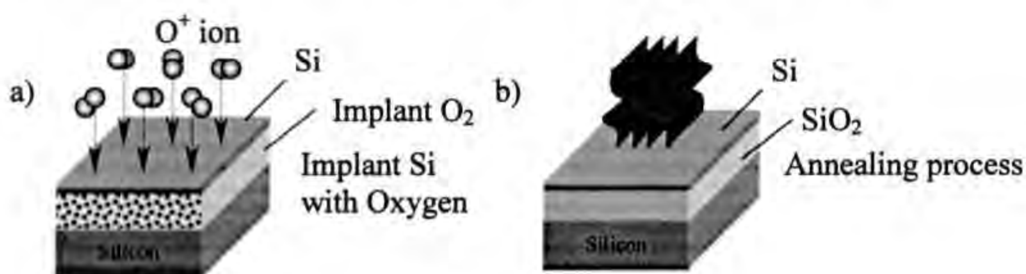

Figure 2.2: SIMOX process steps.

2.1.2 BONDED SOI WAFERS

Bonded SOI wafer [8] creates the buried oxide without the ion implantation process. Figure 2.3 illustrates the processing steps for bonded wafers. At first, two separate wafers are oxidized to form a SiO_2 layer on the surface. The two oxidized surfaces are then thermally bonded together to form the buried oxide. Subsequently, the device wafer is grinded at the backside to a desired silicon thickness. Lastly, the

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SOI wafer is annealed and polished to produce a thin layer of silicon above the bonded buried oxide (BOX). The thermally grown BOX is more superior than the O_2 implanted SIMOX wafers in terms of the higher breakdown voltage and sharper Si/SiO_2 interface. However, this approach is costly as it utilizes two wafers for every bonded SOI wafer made.

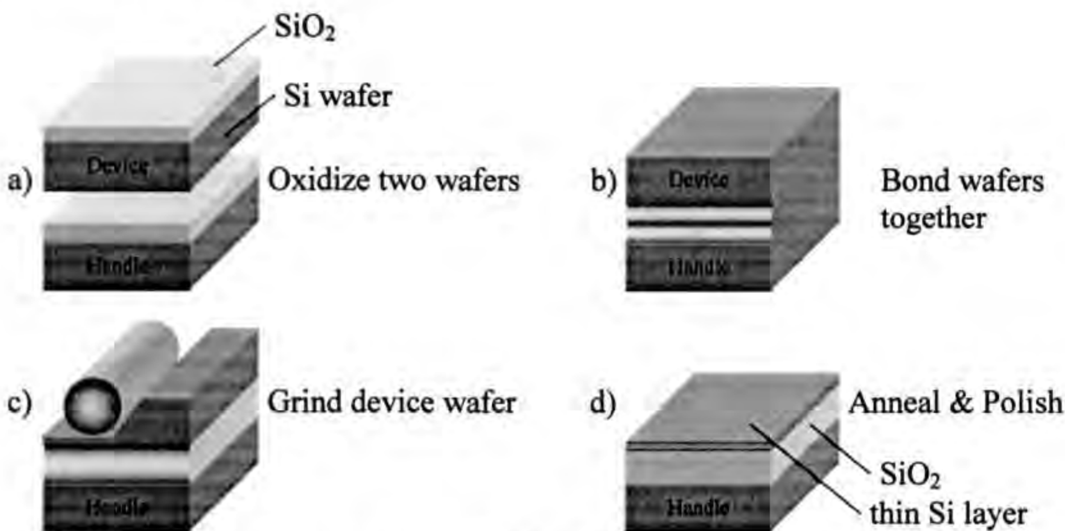

Figure 2.3: Process steps for SOI wafer created using the bonded wafer.

2.1.3 SMART CUT

The Smart Cut approach [9] is an improved bonded technique to reduce cost by reclaiming the remaining portion of the device wafer. The process starts with the oxidation of the device wafer. Protons (hydrogen nucleus) are then implanted through the oxide layer. Next, a handling wafer is thermally bonded to the oxide layer. A post oxidation thermal annealing is then performed to create a stress fracture along the plane where the hydrogen (H_2) are implanted previously. The original silicon wafer can now be removed from the trilayer stack leaving behind a thin layer of silicon on top of the buried oxide. The SOI wafer shall later undergo both annealing and polishing steps to complete the SMART Cut process. The remaining portion of the device wafer can be used again to form the substrate of another smart cut wafer. In this

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way, the silicon is recycled to reduce cost effectively. The SMART Cut process is clearly depicted in Figure 2.4.

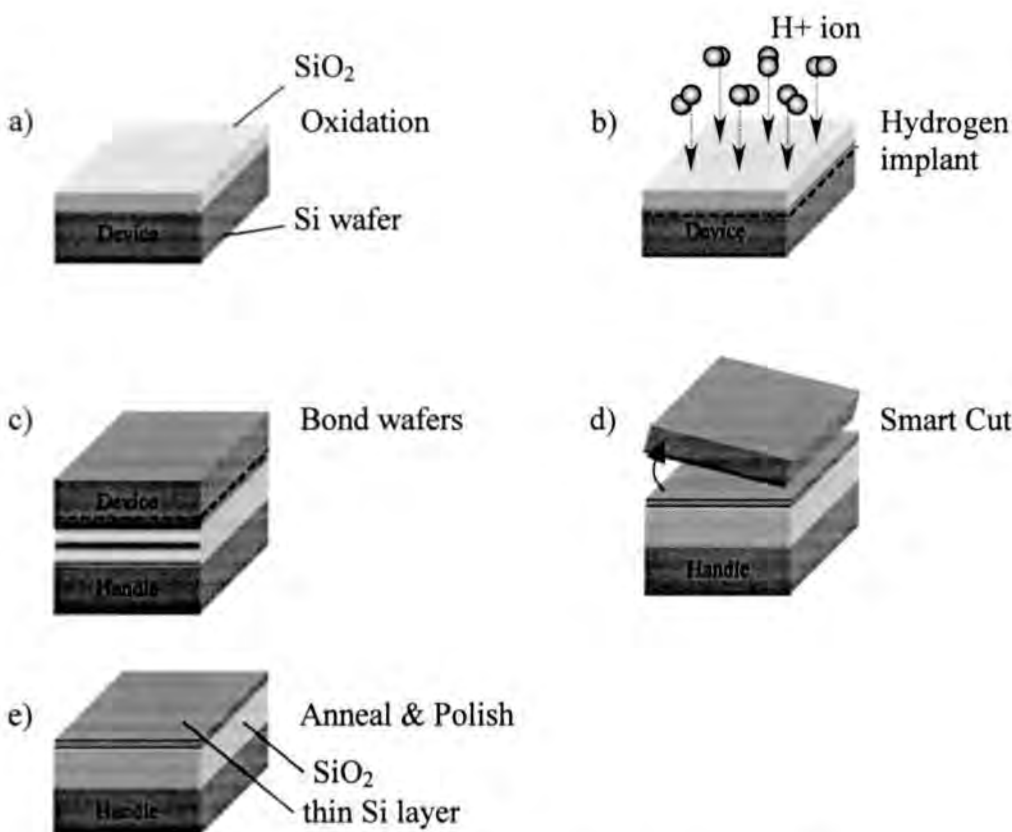

Figure 2.4: Process steps for smart cut.

2.2 THICK AND THIN FILM SOI MOSFET

The physics of the SOI transistor depends greatly on the fundamental parameter of the SOI MOSFET and that is, the film thickness of the top silicon layer. Basically, one can distinguish between thick-film and thin film devices. Based on the definition, it is the maximum width of the depletion zone extending from the silicon/oxide interface. This distinction is schematically illustrated in Figure 2.5. The criterion is classically given by

$$W_{depl} = \sqrt{\frac{4\varepsilon_{si}\phi_f}{qN_A}} \qquad \text{Eq. (1)}$$

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The Fermi potential,

$$\phi_f = \frac{kT}{q}\ln\frac{N_A}{n_i} \qquad \text{Eq. (2)}$$

Here, ε_{si} is the silicon permittivity, N_A the silicon doping concentration (acceptor concentration in case of an NMOS transistor) and n_i the intrinsic carrier concentration.

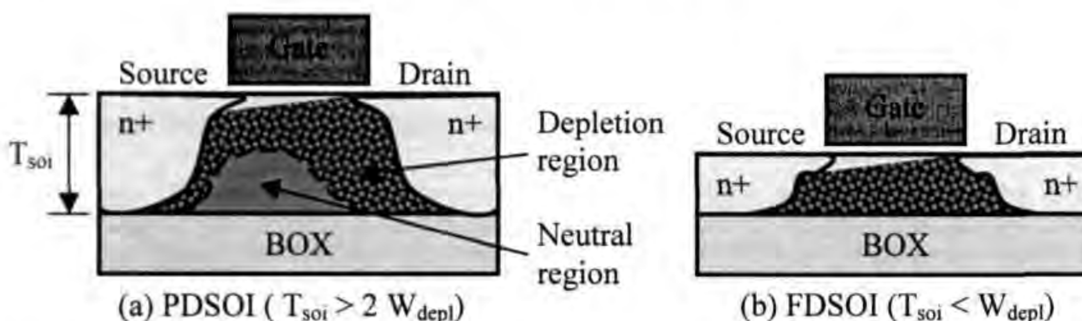

Figure 2.5: Different operating conditions in: (a) partially depleted and (b) fully depleted SOI MOSFETs.

2.2.1 THICK FILM SOI MOSFET

The depletion region is represented by the shaded areas shown in Figure 2.5. The thickness of the silicon film, T_{soi} is twice that of the depletion width, W_{depl}, of the thick-film devices. As the substrate is thick enough, a neutral region (see Figure 2.5a) will exist between the depletion zone arising from the front and back interfaces and because of this partial depletion of the SOI layer, the device is known as partially depleted SOI transistor (PDSOI). The transistor basically behaves like a bulk device with the neutral zone (also called body) grounded by means of a body contact. If the potential of the body is left floating, it will give rise to two parasitic effects [11], namely the kink-effect and the bipolar single transistor latch up.

Kink effect can be observed in the output characteristics of the SOI MOSFET, and an example of which is given in Figure 2.6. The primary cause begins with a significant amount of secondary electrons and holes being generated from the energetic

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electron near the drain region, due to the impact ionization mechanism. Generated electrons move rapidly into the channel, while holes migrate to the lowest potential region of the device, which is the floating body. The accumulation of holes in the floating body will then take place and gradually reach to a positive threshold potential where it forward biases the source-body diode. When the latter event occur, it will decrease the threshold voltage, V_{th}, of the SOI MOSFET. As a result, the lowered V_{th} induces an increase of the drain current as a function of drain voltage and is hence called the "kink effect". SOI device exhibits lesser kink effect owing to the reduced mobility of holes.

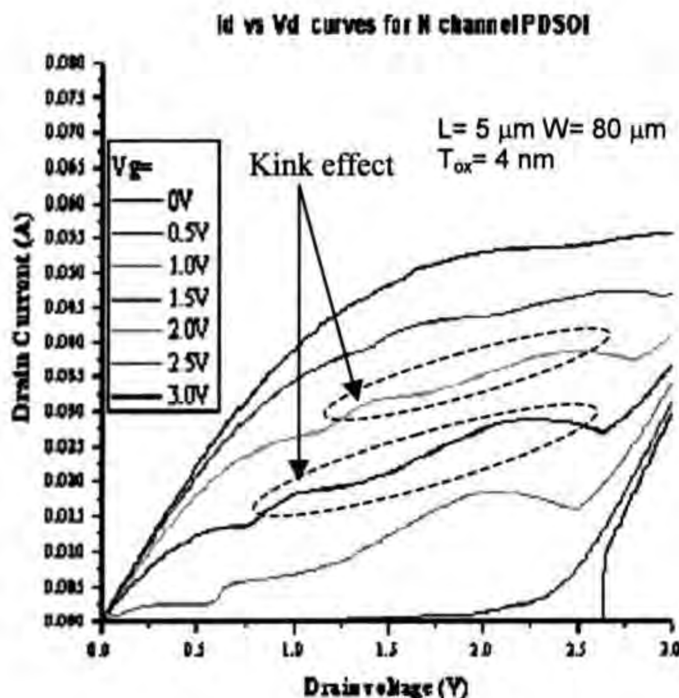

Figure 2.6: Kink effect observed in NMOS SOI MOSFET in output characteristics.

In the NMOS PDSOI transistor, the n+ type source , drain and the p type body may inevitably form the emitter, collector and base of an npn bipolar transistor if the body is allowed to remain floating. When the parasitic bipolar gain becomes ≥ 1 due to the positive feedback loop caused by the amplified base current (generated holes current), it results in a sudden increase in drain current. An infinite subthreshold slope

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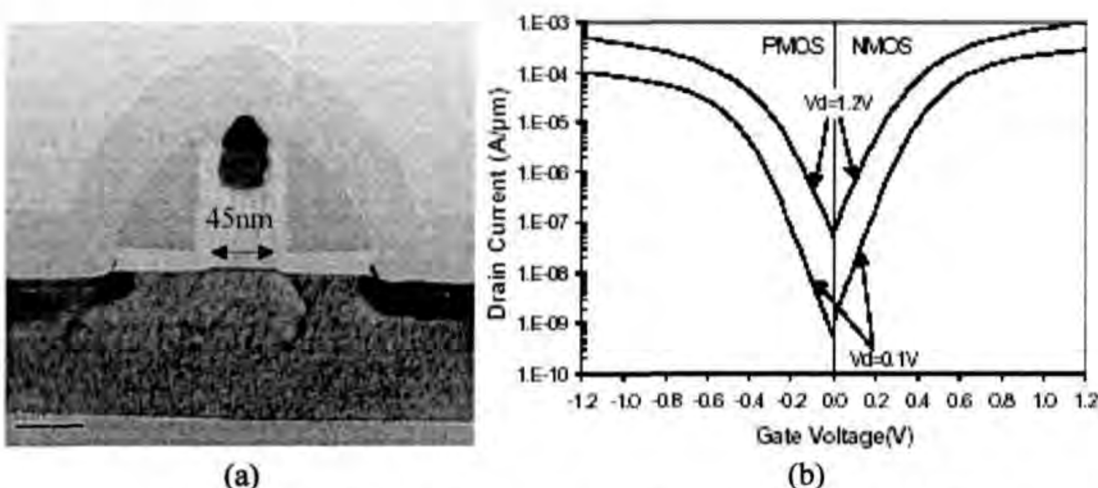
can be observed with hysteresis behavior for the forward and reverse gate voltage scan. Once the positive feedback loop is triggered, the device current cannot be cut off. This phenomenon is known as single transistor latch up [12]. Loss of gate control is a severe consequence of the bipolar phenomenon.

Figure 2.7 features the drive performance of a 45 nm PDSOI transistor [13]. At an operating voltage of 1.2 V, the drive currents of 940 μA/μm and 460 μA/μm were achieved at 20 nA/μm for the NMOS and PMOS respectively. Floating body effects (FBE) were minimized by special diode junction engineering [14] to achieve maximum performance and minimum hysteresis.



(a) (b)

Figure 2.7: (a) TEM of 45 nm L_g transistor, (b) I_d vs V_g at 1.2 V.

2.2.2 THIN FILM SOI MOSFET

The thin-film SOI MOSFET device type is categorized by the fact that the silicon film thickness is smaller than the maximum depletion width, W_{depl}, of Eq. (1). In that case, the silicon layer is fully depleted at threshold. This type of device is known as fully depleted SOI transistor (FDSOI). In thin-film, FDSOI devices, deep implants like well and punch-through are unnecessary and the entire impurity profile in

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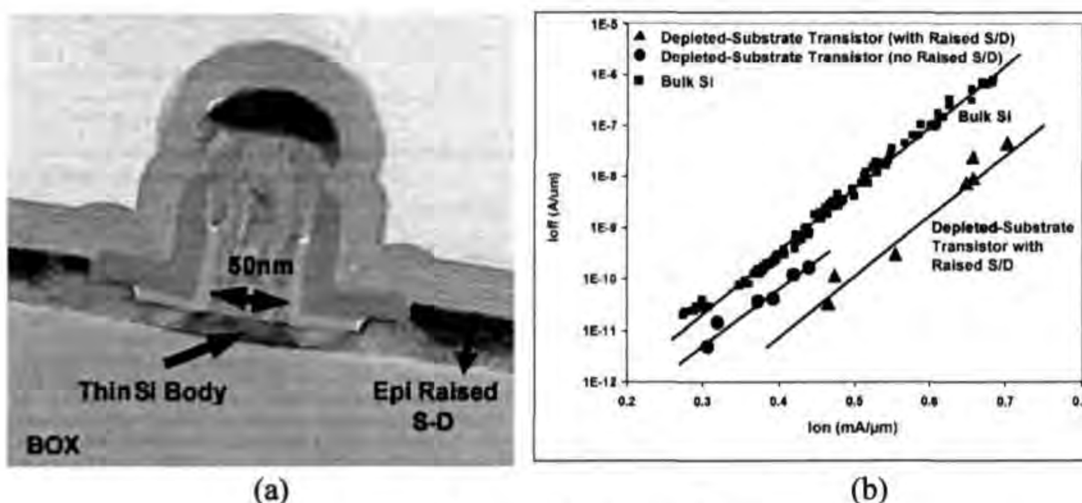
the channel is determined by a single shallow implant. Unlike PDSOI, standard FDSOI transistors eliminate floating body effects (FBE) that has placed a significant burden on circuit design. Furthermore, they exhibit enhanced device performances among the rest (which will be illustrated in next section), by offering low electric fields, reduced junction capacitance and improved subthreshold slope.

Seen in Figure 2.8 is an example of a NMOS FDSOI transistor and it is a 50 nm Depleted Substrate Transistor (DST) designed by Intel [2]. It is able to achieve a drain induced barrier lowering (DIBL) of 45 mV/V, a subthreshold slope of 75 mV/dec, an I_{on} of 1180 μA/μm and a I_{off} of 60 nA/μm at a supply, V_{cc}, of 1.3 V. Significant improvement in the I_d-V_d characteristics is also noted. This is due to a 60 % reduction in DIBL and the greater than 25 % improvement in subthreshold slope over the bulk Si. In addition, the use of raised source/drain has help to reduce the parasitic resistances and to further improve upon the I_{on} by ~20 %.



(a) (b)

Figure 2.8: (a) X-SEM of 50 nm DST, (b) I_{on} vs I_{off} .

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2.2.3 COMPARSION ON THE ELECTRICAL PROPERTIES OF PDSOI AND FDSOI MOSFET

The merits of the various types of SOI MOSFETs mentioned in sub-section 2.2.2 are listed in Figure 2.1, where some electrical properties of the devices are also compared [15]. Note that the bulk silicon devices have been taken as a reference. The SOI MOSFETs present several properties that allow them to operate in harsh environments whereby in the case of bulk devices would fail to operate satisfactorily. Generally, the main popularity of PDSOI over FDSOI devices is due to the independence of their threshold voltage on silicon film thickness as well as the charges in the buried oxide. Nevertheless, one can see that the thin-film Depleted-Substrate Transistor (DST) devices offer the most attractive properties for ULSI applications.

Table 2.1: Comparison of some electrical properties of thick- and thin- film SOI MOSFETs with the bulk devices taken as a reference

Properties	Bulk	PDSOI	DST
Si on Oxide Layer	NA	~100 nm	<50 nm
Raised source drain	No	No	Yes
Junction capacitance	Low	Lower	Lowest
Off state leakage	Low	Lower	Lowest
Soft error rate	Low	Lower	Lowest
Floating Body Effect	No	Yes	No
Gate delay	1.0x	0.9x	0.7x
Operating voltage	1.0x	1.0x	0.8x
V_{th} sensitivity on t_{soi}	Lowest	Low	High
Subthreshold Slope (mV/Dec)	~95	-	<75
Drain Induced Barrier Lowering (mV/V)	~100	-	~40

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2.4 BASIC SOI MOSFET DEVICES

There are different types of existing designs of SOI transistor designs. The densest and most common layout is presented in Figure 2.9a. It is made up of a rectangular active area, a gate, and contact holes on top of the source/drain region, which is in fact very similar to the bulk structure. Considering the case of an n-channel device (which will be illustrated throughout this section), the device area is first defined by an active mask pattern through lithography. The n-channel V_{th} adjust, the back-channel stop dosage, as well as for the N+ source and drain implant steps are all implanted subsequently after the gate definition. This is the simplest form of SOI device structure with no body contact made to the substrate. Floating body effect can become a problem if the device is partially depleted. On the other hand, if it operates in fully depleted mode, the thin source and drain film can reach very high sheet resistance and this can jeopardize the speed performance (sheet resistance is inversely proportional to film thickness). This can be remedied by increasing the thickness of the source/drain using elevated source/drain technique [16]. This approach uses selective silicon epitaxy to form an elevated source/drain structure so that it reduces the sheet resistance and also allows a relatively thick silicidation process.

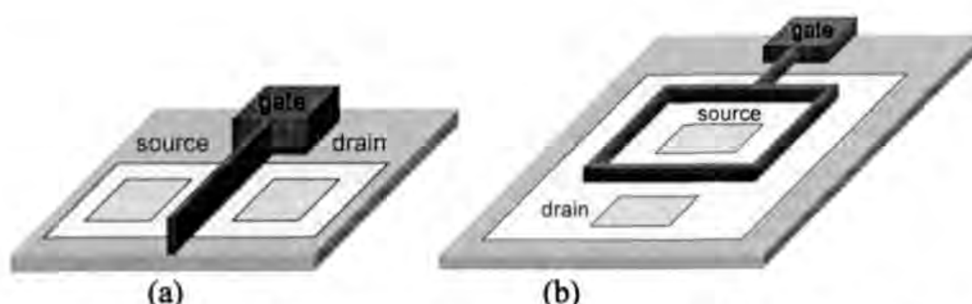

Figure 2.9: Common SOI MOSFETs layout: (a) normal device, (b) edgeless device.

Figure 2.9b shows a "edgeless" device design that can be used to replace the conventional circuit that suffers from edge leakage problems (such as in devices which

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create significant amount of oxide charges in the oxide at the edges of the silicon region when subjected to ionizing radiation). In such a device, the silicon island provides no edge underneath the gate between the source and the drain. However, it is worth noting that edgeless devices take up much more silicon active areas than the conventional devices, and are not implemented if the prime concern is in achieving high integration density.

Figure 2.10 provides several schemes used in some applications where it requires devices having body contacts to effectively suppress floating body effect. The conventional contact solution is presented in Figure 10a. It consists of a P+ diffusion between the source/drain regions and alongside with the poly-gate width, which is in contact with the P-type silicon underneath the gate. In addition, such a device can also be used as lateral bipolar transistor; the P+ diffusion being the base contact with the source and the drain acting as the emitter and collector respectively.

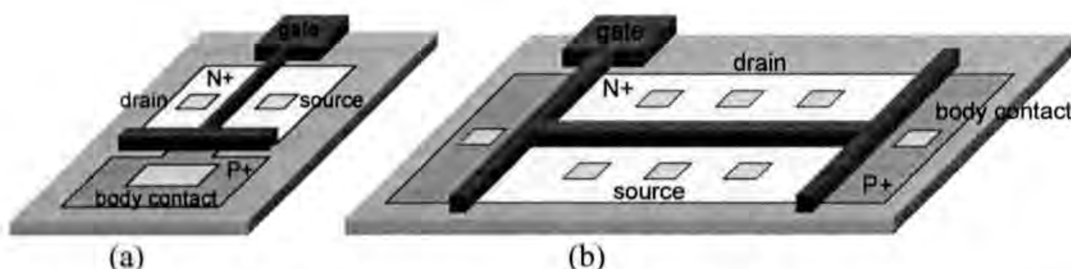

Figure 2.10: Transistor with body contact, (a): T-gate device, (b) H-gate device.

In application where larger gate width transistor are required, a single body contact at one end of the channel region may not be able to completely suppress the FBE. In fact, the FBE phenomenon can sometime occur directly underneath the gate but "far" away from the body contact due to the high resistance of the weakly doped channel region. The H-gate MOSFET design in Figure 10b helps to resolve this problem by inserting body contacts at both ends of the channel. Furthermore, there is

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no direct edge leakage path between the source and drain (the edges run only from N+ to P+ diffusions).

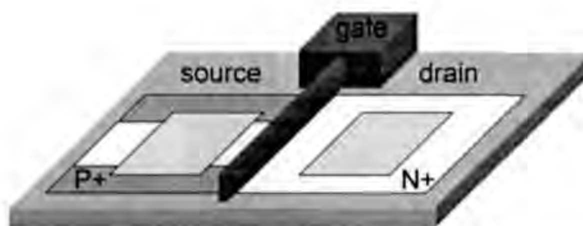

Figure 2.11: NMOS SOI transistor with body tie together at the source.

Lastly, a more compact design than the previous ones is given in Figure 2.11. The concept is to create the P+ body on the both side of the N+ source diffusion so that the contact can ground the source/body together. This device has a major disadvantage of being asymmetrical (source and drain cannot be swapped), and the effective channel width, W_{eff}, is smaller than the width of the active area. It is worth mentioning that body contacts are only used in "thick film" partially depleted devices where the neutral region is exposed to floating body effects.

2.5 DUAL GATE MOSFET

The continuous aggressive scaling of gate length will definitely impose greater difficulties in future applications where planar devices are required to meet high drive performances without compromising the device integrity, such as low leakage current, short channel effects (SCE) and reliability. For instance, the planar gate Depleted-Substrate Transistor (DST) illustrated in Figure 2.8 above is able to meet the drain current requirement while controlling the short channel effects (SCE) effectively. However, as the gate length of the transistor scaled down to sub 45 nm and beyond, such devices will face difficult challenges in the control of fluctuation in channel dopants thereby creating increasing variation of the threshold voltage in the ultra-thin

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silicon film, gate oxide scaling, ultra shallow junction formation and reliability problems due to large electric field.

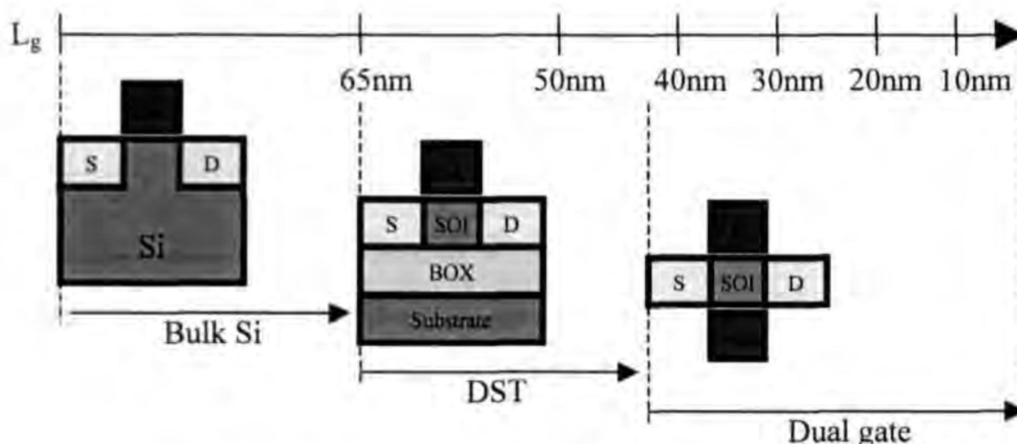

Figure 2.12: Transistor scaling with gate length dimension.

Alternative structures have been proposed over the years and one of which contains the dual-gate architecture of Figure 2.12. It offers better scalability than any other planar gate devices. In dual configuration, the channel is well controlled from both sides of the gate electrodes, leading to minimum leakage current across the channel and also the ability allow to suppress short channel effects with further device scaling. It does not require heavy channel doping to control the SCE. In fact, channel can be undoped in some applications and for such devices, the undoped channel reflects higher carrier mobility due to no impurity scattering. Three possible orientations of the double gate MOSFET on a silicon wafer will be discussed in the subsections to follow.

2.5.1 TYPE I- PLANAR CHANNEL

Current in X-Y plane carried in X direction. Type I (planar channel) has a standard circuit layout with an advantage of having the best controlled silicon channel thickness, T_{soi}, defined by thin film processing rather than lithography. Major

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drawbacks include high process complexity to insert a bottom gate beneath the channel and difficulty to achieve self-alignment of both gates. The top and bottom gates must be perfectly aligned to prevent any possible extra gates to form the source/drain overlap capacitances as well as the loss of current drive due to misalignment. Figure 13a depicts such device: the front and back gates are symmetrical (the same gate oxide thickness is used) and tied together electrically. The cross-sectional scanning electron microscopy (X-SEM) of a planar gate is shown in Figure 13b. This approach has been examined by both IBM [17] and MIT [18].

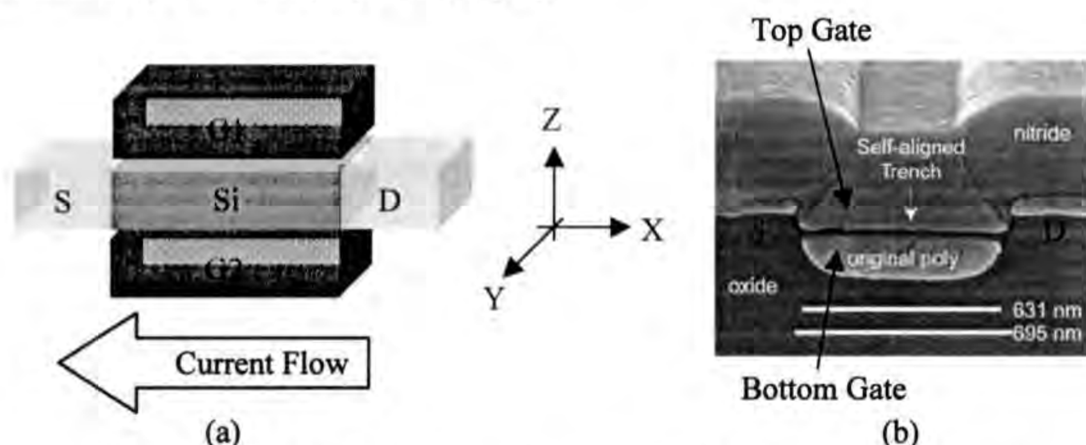

Figure 2.13: TYPE I: (a) Schematic diagram, (b) X -SEM of Planar gate.

2.5.2 TYPE II- VERTICAL CHANNEL

Current in Z-X plane carried in Z direction. Type II also permits the gate length to be determined by well controlled thin film processing rather than lithography. In other words, it uses non-lithography gate definition which produces more consistent gate lengths. However, it suffers from high process complexity which is not compatible with conventional CMOS process and also requires special technique to define the source contact underneath. An example of research in this area is the smallest 15 nm Vertical Replacement Gate (VRG) MOSFET reported by Hitachi [19].

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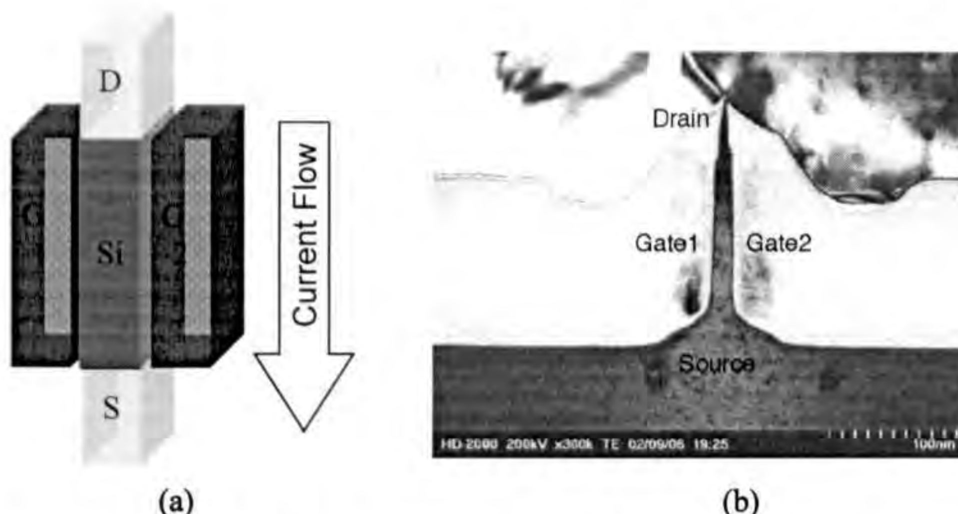
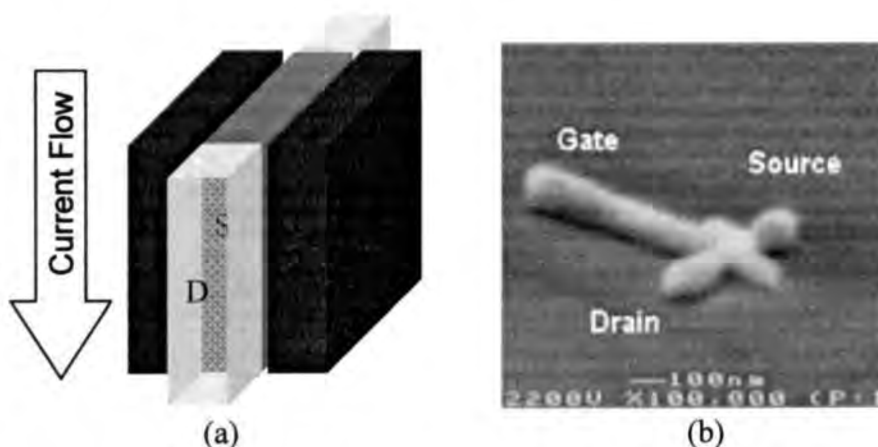


(a) (b)

Figure 2.14: TYPE II: (a) Schematic diagram and (b) X-SEM of Vertical Replacement-Gate (VRG).

2.5.3 TYPE III- FIN CHANNEL

Current in Z-Y plane carried in Y direction. The type III (Fin channel) structure requires the gate length to be determined by lithography and fixes the gate width. Circuits requiring varying gate widths must essentially use many devices in parallel rather than wider transistors. An example of researches in this area is by AMD and Berkeley, where both featured the 10-nm FinFETs.



(a) (b)

Figure 2.15: TYPE III: (a) Schematic diagram and (b) X-SEM of 10-nm FinFET.

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An major drawback of the fully depleted type II and III devices is that the channel thickness is usually defined by lithography and must be thinner than the gate length (film thickness < 2/3 L_g).

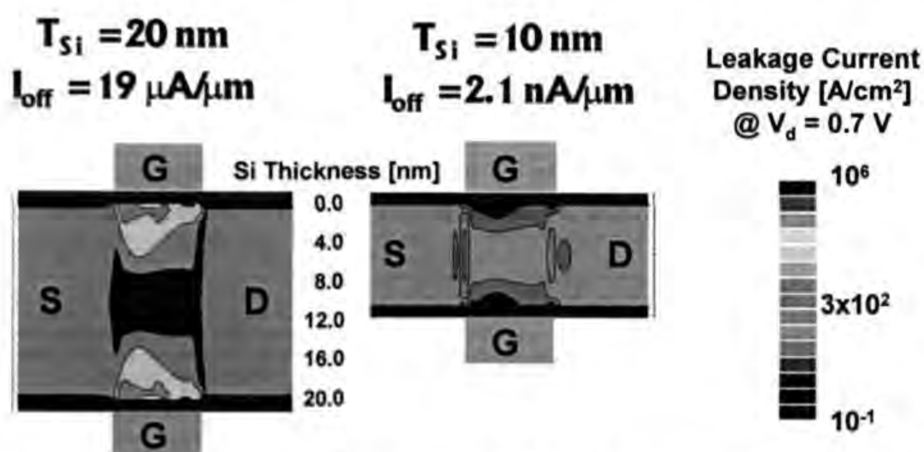

Figure 2.16: Simulation of leakage current in double-gate transistor with L_g = 25 nm and $T_{ox,eq}$ = 12 Å.

In Figure 2.16, body thickness, T_{si}, of 20 and 10 nm have been compared with the same oxide thickness, T_{ox}, at L_g = 25 nm. The results show that the leakage path that is far from the gate are substantially reduced in the 10-nm double gate MOSFET. The off-state leakage current is therefore decrease and the short channel effect can be minimized by using a thin silicon body in the order of 0.7 * L_g [20]. Based on the stringent requirement, Type II and III devices therefore require more aggressive lithography than type I devices.

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2.6 OTHER MULTIPLE-GATE SOI MOSFET

Although CMOS remains the most obvious field of application for SOI, the possibility of using a back gate has sparked a large research activity in the field of novel SOI devices. In Figure 2.17, other existing gate configurations for thin-film SOI MOSFETs is presented. It is a particularly promising candidate for ultimate CMOS scaling due to its superior control of SCE, near-ideal subthreshold slope and mobility enhancement.

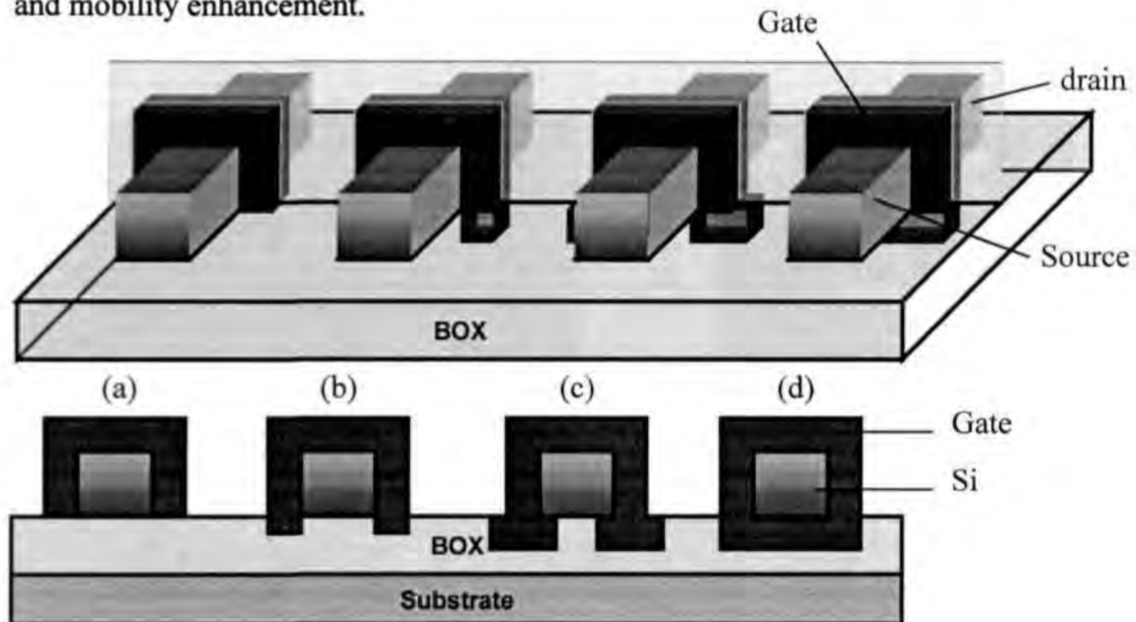

Figure 2.17: Different gate configurations: (a) triple gate, (b) Pi (π)-gate, (c) Omega Ω-gate and (d) quadruple gate.

2.6.1 TYPE I- TRI GATE

The tri-gate device (type 1) consists of a top and two side gates that encast the silicon channel on top of an insulating BOX layer. The device fabrication process resembles very much that of the bulk transistor since it does not require aggressive lithography patterning to define the channel. It can attain full depletion at silicon body dimensions, at approximately 1.5–2 times greater than either the single gate SOI or the non-planar double-gate SOI for similar gate lengths. This also implies that the tri-gate devices are easy to fabricate by simply using the

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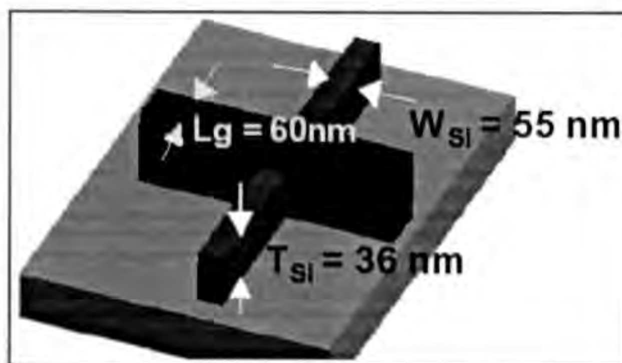
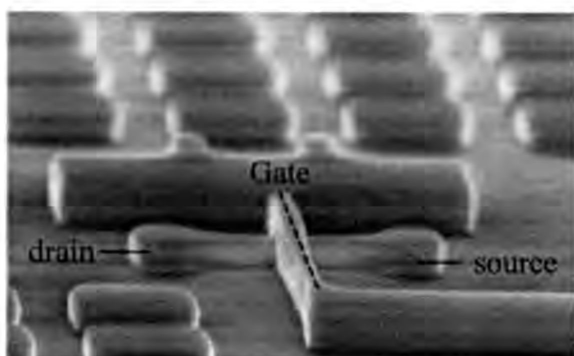
conventional fabrication tools. In other words, tri-gate body dimensions are more flexible and relaxed as compared to the single-gate or double-gate devices.



(a)



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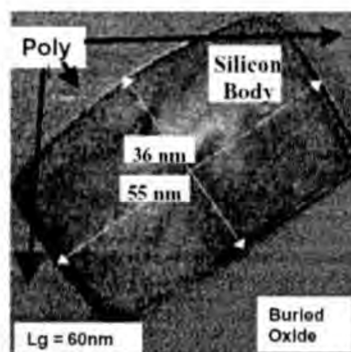

(c)

Figure 2.18:Tri-gate: (a) Schematic, (b) Tilted SEM and (c) TEM of silicon body.

It has been reported that the Tri-gate NMOS transistor (see Figure 2.18) is able to exhibit excellent short channel effect with a drain induced barrier lowering (DIBL) of 41 mV/V and a near ideal subthreshold slope (S/S) at 68 mV/decade. It has a drive current characteristic of 1.14 mA/μm at I_{off} = 70 nA/μm and this is higher than any non-planar devices reported so far [5]. The Tri-gate PMOS device on the other hand has a subthreshold slope of 69.5 mV/decade, DIBL of 48 mV/V, I_{on} = 520 mA/μm and I_{off} = 24 nA/μm at a operating voltage of 1.3 V. Figure 2.19 further illustrates that the Tri-gate device is fully depleted and is absence of any kink effect. It is found that the corner of the body plays a dominant role in the subthreshold behavior.

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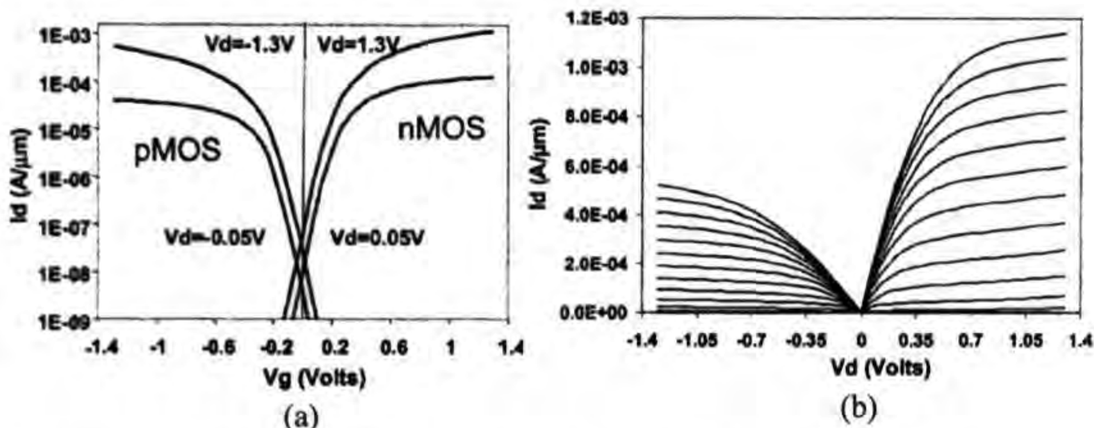

Figure 2.19: (a) I_d-V_g plot of 60 nm NMOS and PMOS, (b) I_d-V_d characteristics with gate voltage ramped to 1.3 V in steps of 0.1 V.

The presence of corner device due to the proximity of two adjacent gates has greatly affected the shape of the subthreshold I-V characteristics and the degree of DIBL control, as well as the early device turn-on. Figure 2.20 indicates that the corner device provides most of the total transistor current until V_g = 0.4-0.5 V. At this subthreshold regime, the corner regions have the highest electron density. Based on simulation results, sharper corner will produce a greater early turn on effect of the corner device as well as suffering from smaller DIBL.

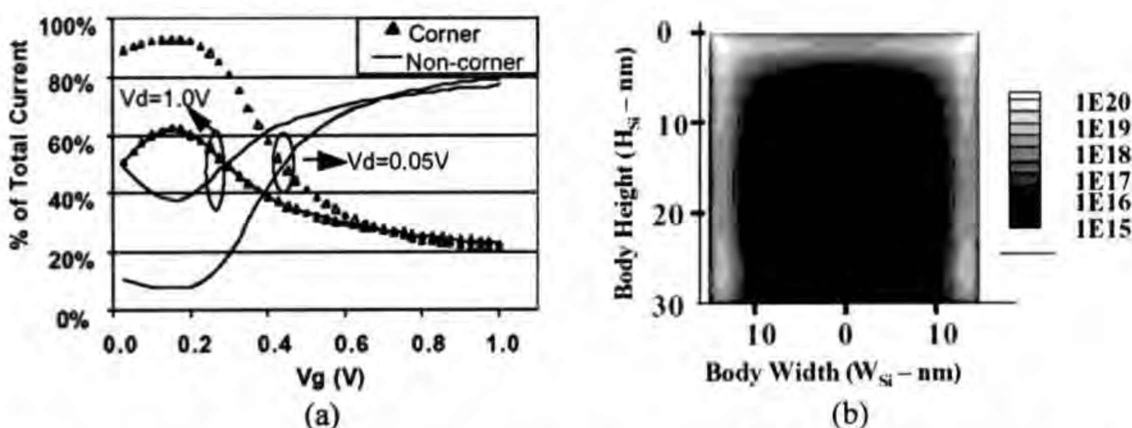

Figure 2.20: (a) Percentage contribution of corner and non corner device to total current, (b) Simulation of electron density in the body at mid point between source and drain, for V_d= 1 V and V_g= 0.4 V.

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Thus, the best design involves keeping the body width small to prevent a hump in the I_d-V_g to allow lowering of I_{on}. The rounding of corners will also help to prevent early switching on of corner devices.

2.6.2 TYPE II- PI GATE

The Pi-gate (Type 2) structure is an "improved" triple gate MOSFET with the gate electrode extends further some depth into the buried oxide at both sides of the device channel [21]. The gate structure seen in Figure 2.21c resembles the shape of the uppercase Greek π (Pi) letter.

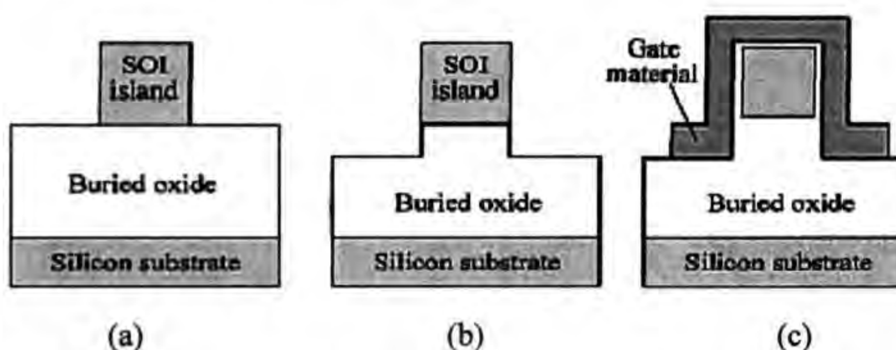

Figure 2.21: Pi gate fabrication step: (a) active patterning, (b) shallow buried oxide RIE and (c) gate oxide growth , gate material deposition and patterning.

The purpose of gate extension in the buried oxide is to shield the backside of the channel region from electric field lines coming from the drain end and function almost as perfectly as an actual back gate. Based on the simulation results, the tranconductance and current drive are 3.56 times greater that of the single-gate device. This indicates that the lower part of the gate sidewalls can effectively act as a back gate through lateral field effect in the buried oxide. Unlike the gate-all-around structure, the Pi-gate SOI MOSFET can be readily manufactured, since it requires merely an addition of a masking and a RIE buried oxide etch step to a conventional SOI CMOS fabrication process. Figure 2.22a proves that the DIBL is

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most effectively suppressed by the quadruple- gate structure but the Pi- gate structure is also another comparable candidate. Similarly, the threshold voltage roll off is well minimized by the use of Pi-gate which comes second close to that of the quadruple gate. The subthreshold swing of Figure 2.22b, with different gate structures and gate lengths indicates that the Pi- gate device exhibits degradation in close proximity to that of the quadruple gate structure. In view of the high process complexity in the quadruple gate fabrication, one would considered the Pi-gate structure to be a promising candidate because of its ease of fabrication and that offers its electrical characteristics similar to the much complex quadruple gate.

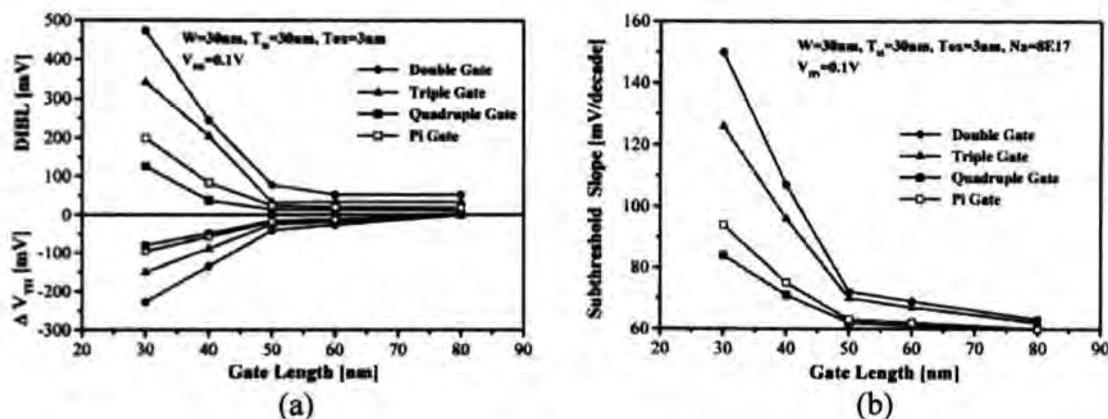

Figure 2.22: (a) DIBL and threshold channel roll-off in fully depleted SOI MOSFETs with different gate structures and different gate lengths. (b) Subthreshold swing in fully depleted SOI MOSFETs with different gate structures and different gate lengths.

2.6.3 TYPE III- OMEGA GATE

The Omega (Ω) FET (Type 3) has the closest resemblance to the Pi-gate with special gate extension under the silicon body (see Figure 23). It adopts a fabrication process that is very similar to that of the FinFET [22] with an additional wet oxide etch to remove a certain amount of buried oxide under the silicon body to form the gate extension [23]. This gate extension shields the electric field lines induced by the drain voltage, to effectively suppress DIBL as well as to provide

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enhanced gate–to-channel controllability than other non planar SOI devices. The Ω-FET also has a top gate that is similar to the conventional DST and two sidewall gates. Unlike FinFET, the additional gate extension and top gate of the Ω-FET offer less stringent dimension in the body thickness, T_{sb}.

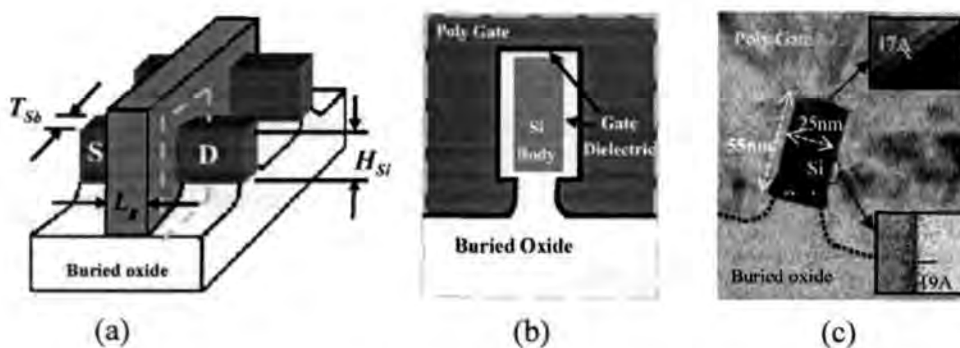

Figure 2.23: Omega FET: (a) schematic illustration, (b) cross-sectional View, (c) X-SEM image.

It has been reported that the 25 nm Omega FET transistors presented in Figure 24 can achieve a drive currents of 1440 μA/μm and 780 μA/μm with off state leakage currents of 8 nA/μm and 0.4 nA/μm for N-FET and P-FET respectively, at 1 V operation. The gate delay (CV/I) of 0.39 ps for NFET and 0.88 ps for P-FET are the lowest among all non planar devices reported so far for the 25 nm gate length.

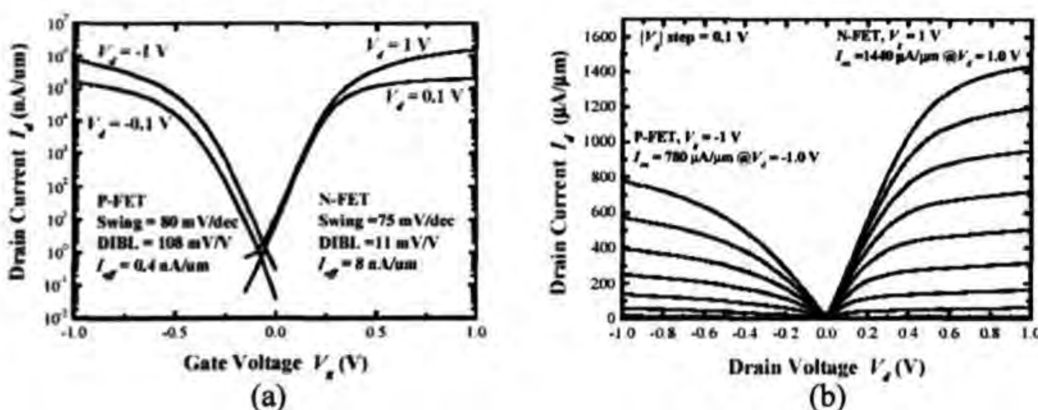

Figure 2.24: (a) I_d-V_g, (b) I_d-V_d characteristics of 25nm L CMOS Ω-FET.

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2.6.4 TYPE IV- QUADRUPLE GATE

It is well known that the gate-all-around (GAA) MOSFET (Type 4) offers best performances and electrical behavior when compared to the rest of the multiple gate structures. However, it suffers from major drawback such as high process complexity and implementation difficulties. The extra process step involves in etching a cavity underneath the silicon using buffered hydrofluoric (HF) acid. Upon completion, it can precede using conventional process steps, as per any planar SOI device.

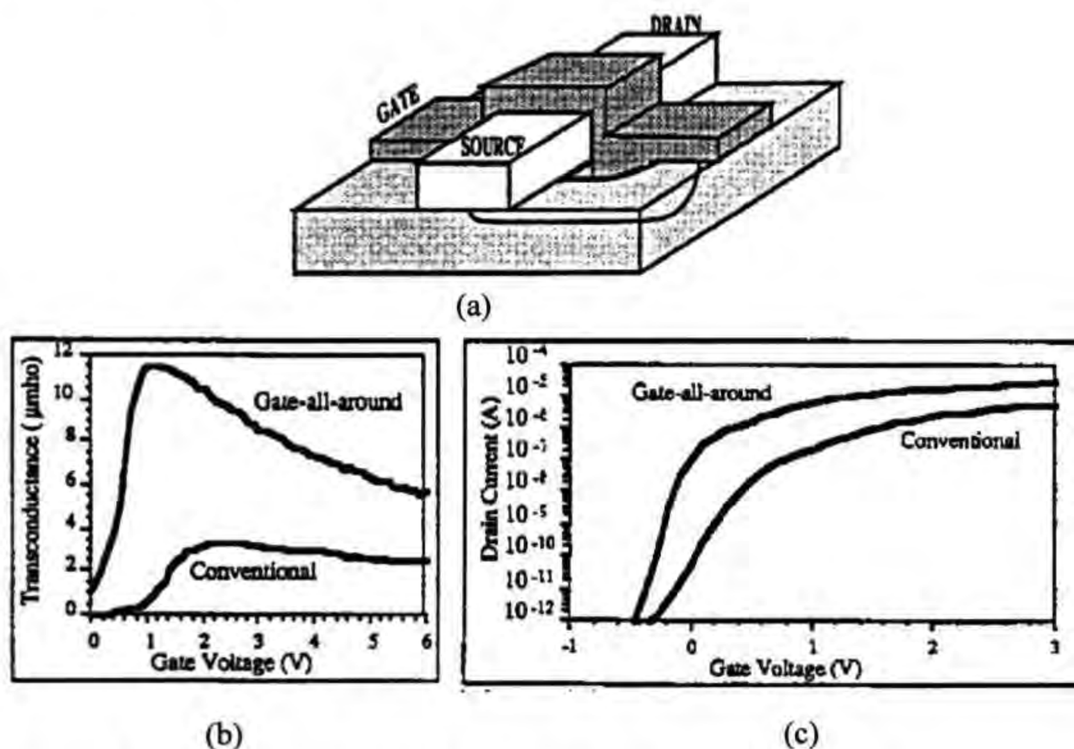

Figure 2.25: (a) A completed GAA device, (b) Transconductance as a function of gate voltage at V_{ds} = 100 mV, (c) I_d-V_d characteristics comparison.

The 3 µm gate length CMOS transistor illustrated in Figure 2.25 has demonstrated a subthreshold slope of 63 mV/decade and 3 times higher maximum transconductance at V_d = 100 mV. At sub-micron regime, the simulation results show a transconductance and a drive current of a GAA transistor to be approximately 4 times that of the single gate device. Furthermore, it exhibits

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excellent short channel effect immunity with near ideal subthreshold slope of 60 mV/V and a lowest DIBL for a given sub micron gate length. Until now, this area of approach is not examined extensively in sub micron regime due to the high resources incurred.

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CHAPTER 3: MULTIPLE GATE SOI MOSFET

In this project, a multiple gate design that gathers more than one planar gate to control the silicon channel is proposed. In this multiple configuration, it can improve the scalability of CMOS MOSFET as well as delivering its superior electrical properties. The main advantages of the proposed structure includes greater drive current enhancement, improved switching speed and reduced short channel effects. All of which will be explained in details at a later section. Two types of novel gate have been fabricated in this work. They are namely the Gate-all-around (GAA) and the "n" gate structures.

3.1 GATE- ALL-AROUND (GAA) SOI MOSFET

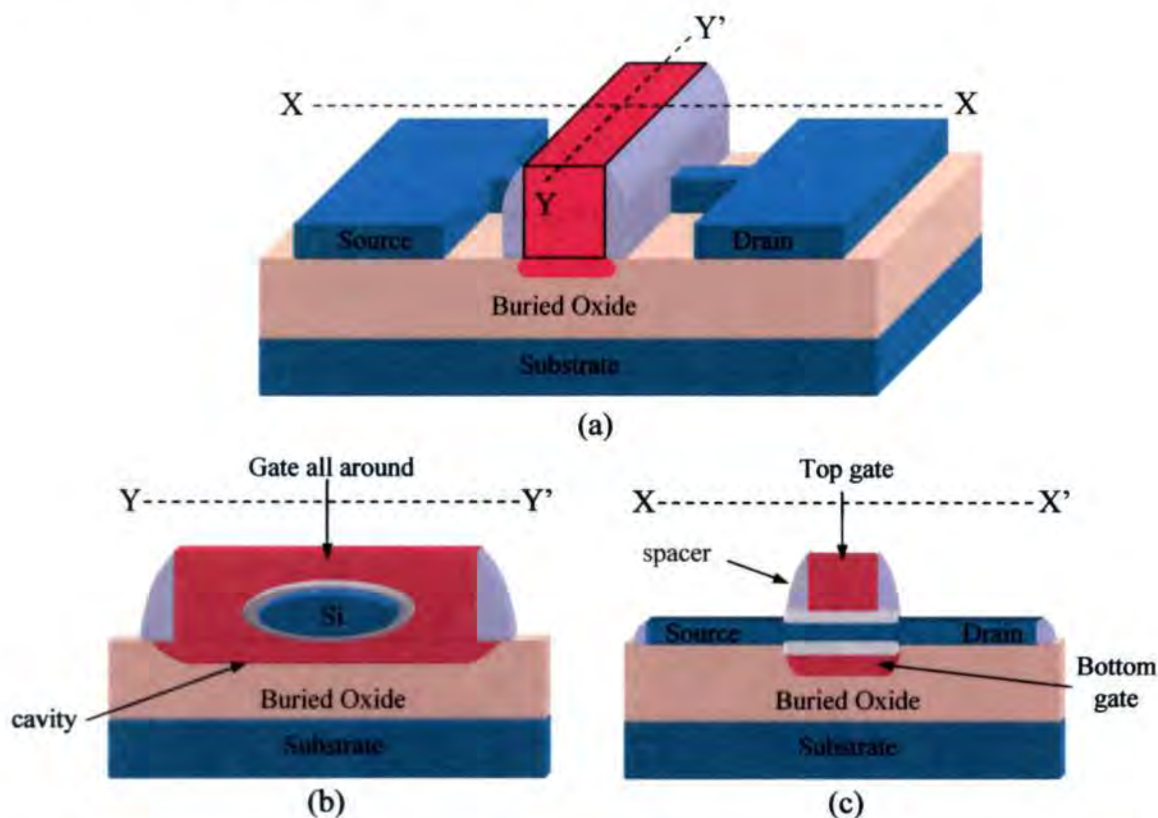

Figure 3.1: (a) Gate-all-around (GAA) MOSFET structure, (b) cross sectional view perpendicular and (c) cross sectional view parallel to the source to drain current flow.

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With a bottom gate electrode inserted underneath the channel, it completes the optimum concept [1] where the entire channel is totally enclosed by the gate (see Figure 3.1). The development concept adopts a process sequence which is similar to that used for regular bulk CMOS fabrication, with only one additional replacement mask step and a wet etch step in buffered hydrofloride solution (BHF).

3.1.1 BENEFITS OF GAA MOSFET

The GAA provides enhanced gate controllability over other multiple gate designs. The advantages of the GAA MOSFET over other multiple gate designs are listed as follows:

1. The GAA transistor offers multiple surface inversions where the inversion charge spreads throughout the entire surface of the ultrathin silicon body. The device characteristics can be enhanced tremendously (see Figure 3.2). The two fold increased in the transconductance of a GAA device as compared to that of a conventional device [2].

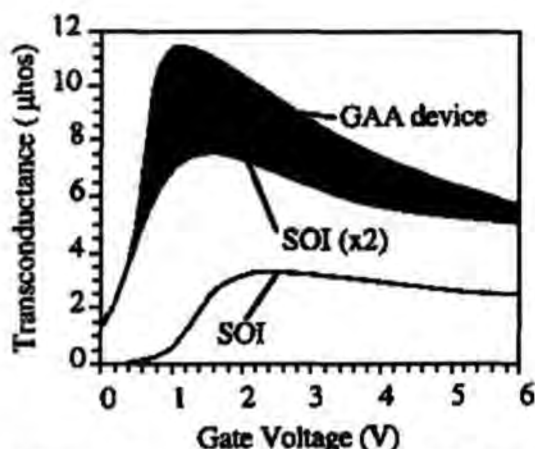

Figure 3.2: Transconductance of GAA device.

The tranconductance and current drive of the quadruple (GAA) gate structure is approximately four times greater than that of the single gate device at the

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threshold, where the inversion layer is distributed across the entire silicon film and where the effect of bulk mobility (in contrast to surface mobility) can be felt. At higher voltages, there is still inversion in the center of the silicon film, but the carriers are mainly localised in the inversion layers near the interfaces. As a result, more scattering occurs and the tranconductance tends towards to two times that of a conventional device.

2. Besides the beneficial effects derived from the multiple surface inversions, GAA presents other interesting features in the fields of high temperature applications. Being thin-film SOI device with minimal junction area, the GAA is equipped with the classical SOI low leakage current characteristics of the SOI. Because of complete depletion, the variation of threshold voltage with temperature is minimized, where the dual gate control of the channel region allows the GAA MOSFET to remain fully depleted at higher temperatures, similar to that seen in a fully depleted SOI MOSFET that has the same silicon film thickness. In regular SOI devices, they are thermally isolated from the substrate by a relatively thick buried oxide layer, which presents low thermal conductivity. In the case of a GAA device, the channel region is thermally isolated from the substrate by a polysilicon layer and two thin gate oxide layers. Hence, a much better thermal conductivity path to the substrate is allowed and the GAA is less prone to the self-heating effect than regular SOI devices.

3. GAA devices also offer excellent total-dose and SEU (single-event upset) radiation hardness [4]. Indeed, the active area of the device is completely

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surrounded by thin thermal gate oxide and by the polysilicon gate. Therefore, the device has no edges. In that sense, no field or buried oxide layers are in contact with the channel region and to ensure no dose-induced edge leakage.

4. The GAA is reputed to has the most suitable device structure for suppressing short channel effect (SCE) such as Drain Induced Barrier Lowering (DIBL) and subthreshold slope degradation [3][4]. As the drain voltage increases for regular SOI devices, DIBL results in an exponentially decreasing barrier near the drain/source and increase the subthreshold current. In contrast, GAA designed with a bottom gate extended into the buried oxide underneath the active silicon film, will effectively shield the back of the channel region from the electric field lines directed from the drain. Thus, it is capable of suppressing the DIBL effect and reducing the subthreshold current.

5. The most important benefit of GAA transistor is in the fabrication process in that it is compatible with standard industrial bulk CMOS manufacturing.

3.1.2 GAA PROCESS FLOW

This section presents a detail description of the realization of the proposed GAA structure. To better explain the GAA process, all implantation steps are skipped and emphasis is placed on the development of the physical GAA device structure. The main features of the fabrication process are the development of the replacement gate mask (starting from step 8) and the formation of the bottom gate electrode (at step 15) using an isotropic etch technique. The process steps can be described as follows:

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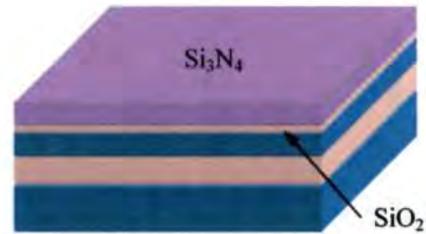
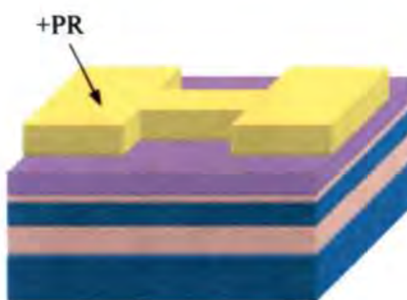
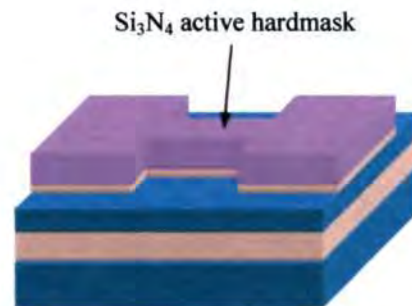
(1) SOI substrate: The starting wafer is a thin film 300 mm SOI P-type substrate of <100>-crystallographic orientation. The SOI film thickness is < 1000 Å with a buried oxide (BOX) thickness of 2500 Å. The substrate is used as a handling wafer.



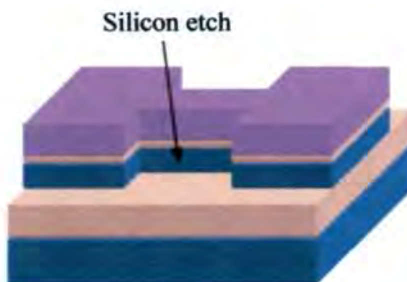
(2) Oxide and nitride deposition: Thermal oxidation step to produce 100 Å of sacrificial oxide is performed. Afterwhich, a layer of 1600 Å nitride is deposited on top.



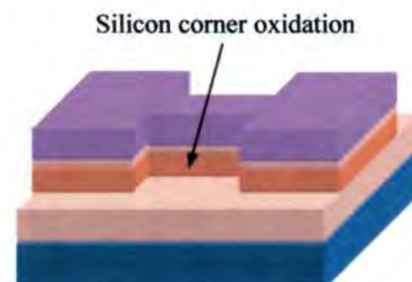
(3) Active lithography: The photoresist is developed, exposed and patterned to create the active hardmask. Positive resist (+PR) is used in the entire process.



(4) Hardmask patterning: The nitride and oxide are patterned and etched selectivity to the bottom thin film SOI to form the active hardmask. PR is stripped and wafer is cleaned to remove any remaining polymer.



(5) Active definition: The SOI film is directionally etched to define the active region. The BOX underneath the SOI film acts as an etch stop layer (ESL).



(6) Corner rounding: A 250 Å oxide is then grown around the active silicon. The oxidation will round the corners as well as protect the silicon from subsequent processing steps.

Figure 3.3a: Process flow of proposed GAA structure.

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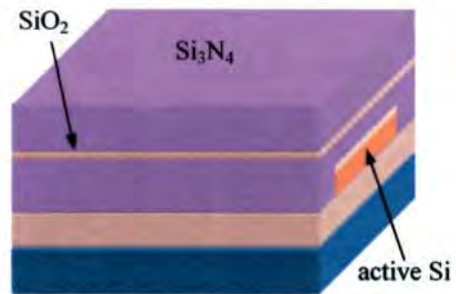
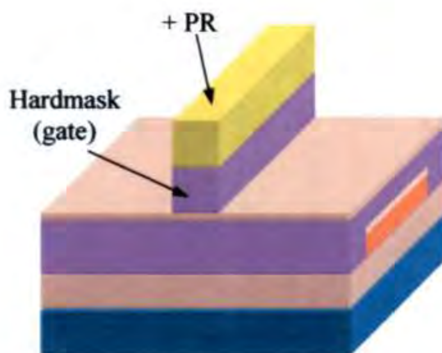
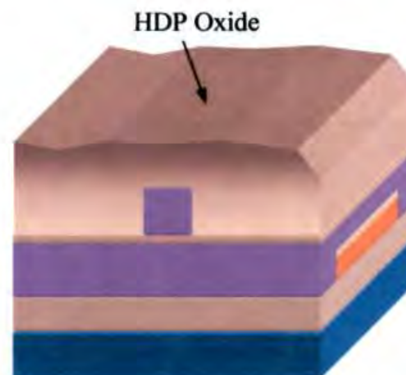
(7) Nitride removal: Dip in hot phosphoric acid to remove all nitride hardmask. It is worth mentioning that the surrounding sacrificial oxide prevents the acid solution from damaging the silicon surface.



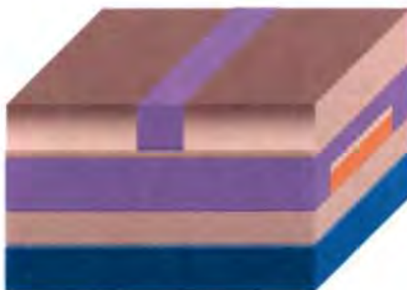
(8) Stack layer deposition: A stack layer of 1600 Å nitride/ 150 Å oxide/ 1600 Å nitride is then deposited. The concept of Replacement Gate Mask (RGM) is implemented here to create a hardmask for cavity etch in later steps.



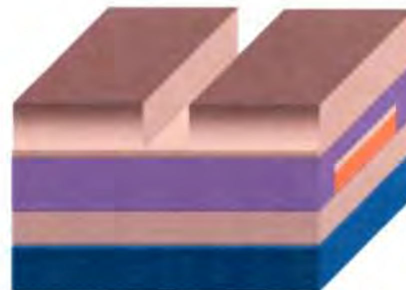
(9) RGM hardmask definition: The gate hardmask is patterned, etched and stopped selectively at the sacrificial oxide layer. +PR is then stripped and the wafer is cleaned.



(10) RGM oxide deposition: Using high-density plasma (HDP) to deposit approximate 3000 Å of oxide. Oxide thickness is required to be to cover the 1600 Å nitride line significantly.



(11) RGM oxide polishing: An oxide Chemical Mechanical Polishing (CMP) is carried out to planarize the surface. An end point technique is used to stop the CMP process upon detecting the nitride strip.



(12) RGM nitride removal: The substrate is dipped into hot phosphoric acid to remove the nitride strip. It has a high selectivity to oxide.

Figure 3.3b: Process flow of proposed GAA structure (continue).

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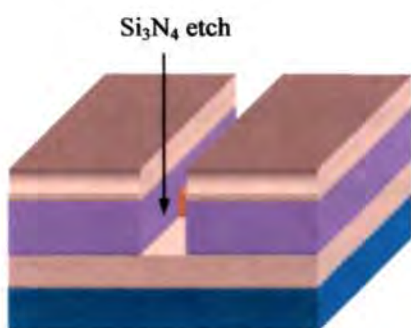
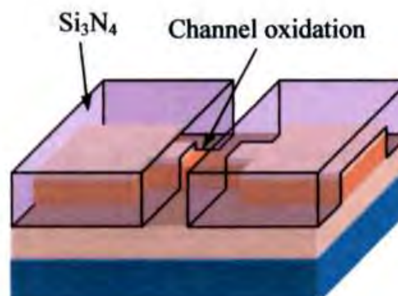
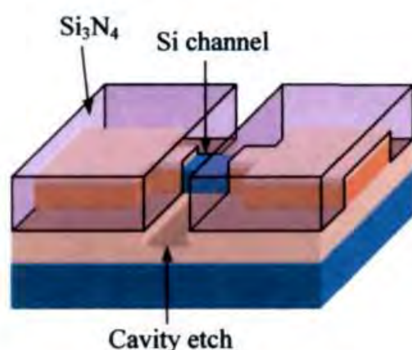


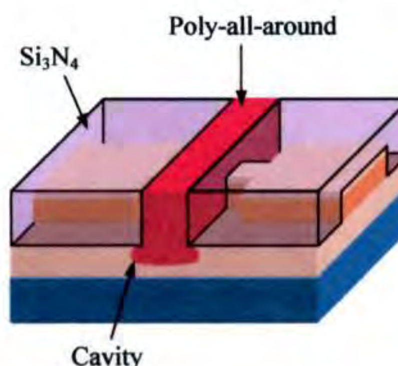
(13) RGM nitride etch: The thin bottom layer of oxide is etched away. Thereafter, an anisotropic nitride etch is performed to open up the gate region. This is to serve as a hardmask for cavity etch in the subsequent step.



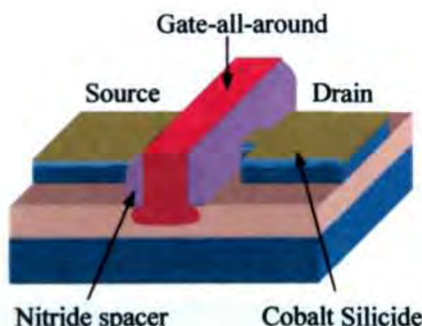
(14) Channel oxidation: The exposed silicon channel will undergo thermal oxidation to produce 200 Å of SiO_2 to help smoothen the channel edges and also to minimize the surface damage during cavity etch in the subsequent steps.



(15) Cavity etch: Diluted HF etch is performed to undercut the oxide underneath the silicon channel. Meanwhile, the sacrificial oxide that covers the silicon channel will be removed as well.



(16) Gate Formation: For gate formation, a conformal 20 Å SiO_2 gate oxide is grown before depositing the poly-silicon. A CMP is then carried out. Since poly-silicon has good gapfill properties and the growth is quite conformal, the poly-gate will wrap around the silicon channel.



(17) Nitride spacer & Silicide formation: The hardmask nitride is removed with hot phosphoric acid. Spacer formation and cobalt silicidation are next done to form the transistor. The front end of line (FEOL) is hence completed.

Figure 3.3c: Process flow of proposed GAA structure (continue).

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3.2 "n" GATE SOI MOSFET

The proposed structure is an "improved" design of the triple gate MOSFET with two major structural differences. Unlike the tri-gate structure, the sidewall gate electrodes are deliberately extended further into some depth of the buried oxide, at both sides of the device channel. In addition, the top surface of the silicon channel is made rounder. This shape resembles the letter "n" (hereby called "n" gate structure). It can readily be manufactured, since it merely requires the addition of a masking and RIE buried oxide etch step to a standard SOI CMOS fabrication process. The "n" gate structure is of the closest resemblance to the Pi-gate structure which has been reported [21], offering attractive electrical properties with better scalability and is therefore a promising candidate for future nanometer MOSFETs.

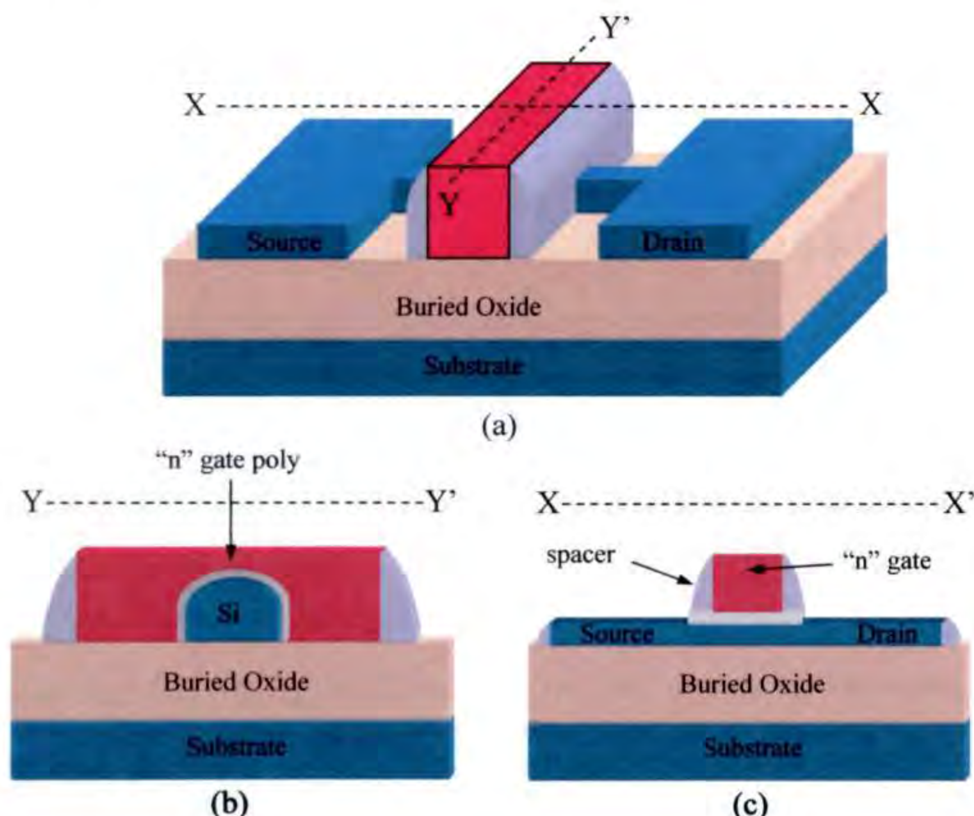

Figure 4.4: (a) "n"-gate MOSFET structure, (b) cross sectional view perpendicular and (c) cross sectional view parallel to the source to drain current flow.

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3.2.1 BENEFITS OF "n" GATE SOI MOSFET

The advantages of "n" gate over the conventional tri-gate can be summarized by the following key points:

1. With gate extension into the buried oxide, it almost perfectly acts as an actual back gate to shield off the electric field lines directed from the drain. In this way, it can effectively suppress DIBL as well as to provide enhanced gate–to-channel controllability over other non planar SOI devices

2. The "n" gate design eliminates the "hump" appearance in the threshold voltage characteristics (see Figure 2.20). This unwanted signature is caused by the early turn effect in the proximity of two adjacent electrodes, due to the higher current density trapping occurrence. Hence, the rounded surface "n" gate structure can remove the unusual behavior in the threshold voltage.

3. With rounded channel edges, the induced drain electric field can be uniformly distributed across the entire channel during operation. In this way, it can effectively improve the reliability of the device lifetime.

3.2.2 "n" GATE PROCESS FLOW

The fabrication process of proposed structure is similar to the GAA development. The only difference is that it does not require any wet etching to do a cavity etch beneath the silicon channel but an additional RIE step is carried out to etch the buried oxide isotropically. This is to have the gate extended to some depth in the buried oxide on both sides of the device. Figure 3.5 illustrates the formation of "n" gate physical structure.

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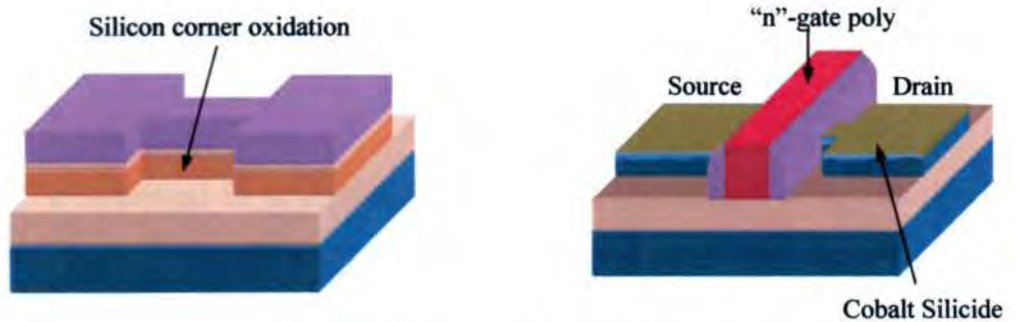
(a) SOI substrate: The starting wafer is a thin film 300 mm SOI P-type substrate of <100>-crystallographic orientation. The SOI film thickness is < 1000 Å with a buried oxide (BOX) thickness of 2500 Å. The substrate is used as a handling wafer.

(b) Active hardmask patterning: The nitride and oxide are patterned and etched selectivity to the bottom thin film SOI to form the active hardmask. PR is stripped and wafer is cleaned to remove any remaining polymer.

(c) Active definition: The SOI film is directionally etched to define the active region. The BOX underneath the SOI film acts as an etch stop layer (ESL).

(d) Gate extension etch: An RIE oxide etch is carried out to remove the underneath buried out to some depth.



(e) Corner rounding: A 250 Å oxide is then grown around the active silicon. The oxidation will round the corners as well as protect the silicon from subsequent processing steps.

(f) Gate & Silicide formation: The hardmask nitride is removed with hot phosphoric acid. Gate formation and cobalt silicidation are next done to form the transistor. The front end of line (FEOL) is hence completed.

Figure 3.5: Process flow of proposed "n" gate structure.

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3.4 PROCESS PARAMETER CONSIDERATIONS

Despite the fact that the fabrication process proposed in section 3.3 is compatible to bulk CMOS processing, each step parameter has to be carefully considered to anticipate any possible process difficulties or issues that may affect the actual GAA profile. The considerations and changes are highlighted as follows:

1. As the SOI silicon thickness is limited to < 1000 Å, some important conditions, such as the dose and energy must be modified to control the 2-D effects (short-channel, and the drain induced barrier lowering (DIBL) that affect the threshold voltage. In thin film SOI devices, deep implants such as punchthrough and pocket implants are not incorporated into the process flow as the entire impurity profile in the channel area is determined by a single shallow implant.

2. The rapid thermal anneal (RTA) process must be slightly modified (typically 30°C less than in bulk processes) so that the buried oxide that acts as a thermal barrier will not be subjected to excessive heat treatment. This is because the oxide thermal conductivity is about 100 times lower than that of silicon.

3. It is critical to determine the precise etch parameter of the diluted HF for forming the cavity underneath the active silicon. One cannot under-etch the profile as it will result in insufficient coverage of the bottom gate to the active silicon film. On the other hand, the profile cannot be over-etched because the excessive etch area in the buried oxide tends to cause extra parasitic gate-drain/source capacitance as well as loss of current drive upon forming the gate

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electrode [17]. Hence, the design consideration is to ensure that the top and bottom gates are aligned accurately based on the etch parameters.

4. Another important issue to overcome is the reduction of the parasitic source/drain series resistance. Various methods have been in use such as the raised source/drain or precise silicidation. To achieve reasonably low series resistance, it is reported that when the contact resistivity between silicide and silicon is greater than 1×10^{-7} Ω-cm^{-2}, the silicide thickness should be less than 80% of the whole silicon thickness [4]. From this requirement, a highly stable and controlled formation of ultra-thin silicide under a limited silicon film thickness must be established. However, as the device dimension is scaled, it is impossible to form thin silicide layer with low sheet resistance.

The above considerations discussed have all been incorporated into the proposed process flow. In this project, n-gate and GAA MOSFET structure will be implemented to study the electrical properties and hence evaluating the performance these structures proposed in this project.

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CHAPTER 4: MULTIPLE GATE PROCESS CHARACTERIZATION

This chapter describes the process for fabricating the two proposed multiples gate SOI device structure. As these fabrication steps are being detailed, the key problems encountered will also be discussed here. The process will be discussed under the following section:

- SOI wafer preparation
- SOI active region
- Replacement gate mask formation
- GAA physical structure
- "n"-gate physical structure

4.1 SOI WAFER PREPARATION

The starting substrate is a 200 mm SIMOX P-type wafer consisting of a 1000 Å SOI film above a 2000 Å buried oxide (BOX) layer (see Figure 4.1).

Figure 4.1: X-SEM of SOI wafer.

The process begins with the growth of a 100 Å sacrificial-oxide layer, which is grown thermally on the surface of the SOI layer. The sacrificial-oxide is used to cushion the SOI layer from interfacial stress contributed by the silicon nitride film (1600 Å) that is to be deposited on it. The nitride layer serves as a hardmark for the active region definition. After hard mask deposition, a 4200 Å photoresist is coated to define the active region through the use of 248 nm DUV (deep ultra-violet) optical

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lithography. Upon mask definition, an etch process is carried out to pattern the hard mask.

4.2 SOI ACTIVE REGION

A reduced timing of the conventional shallow trench isolation (STI) etch recipe is used initially to define the active region. However, it resulted in severe undercut at the bottom sides of the active layer as illustrated in Figure 4.2. The undercuts have consumed more than 35 % of the active area.

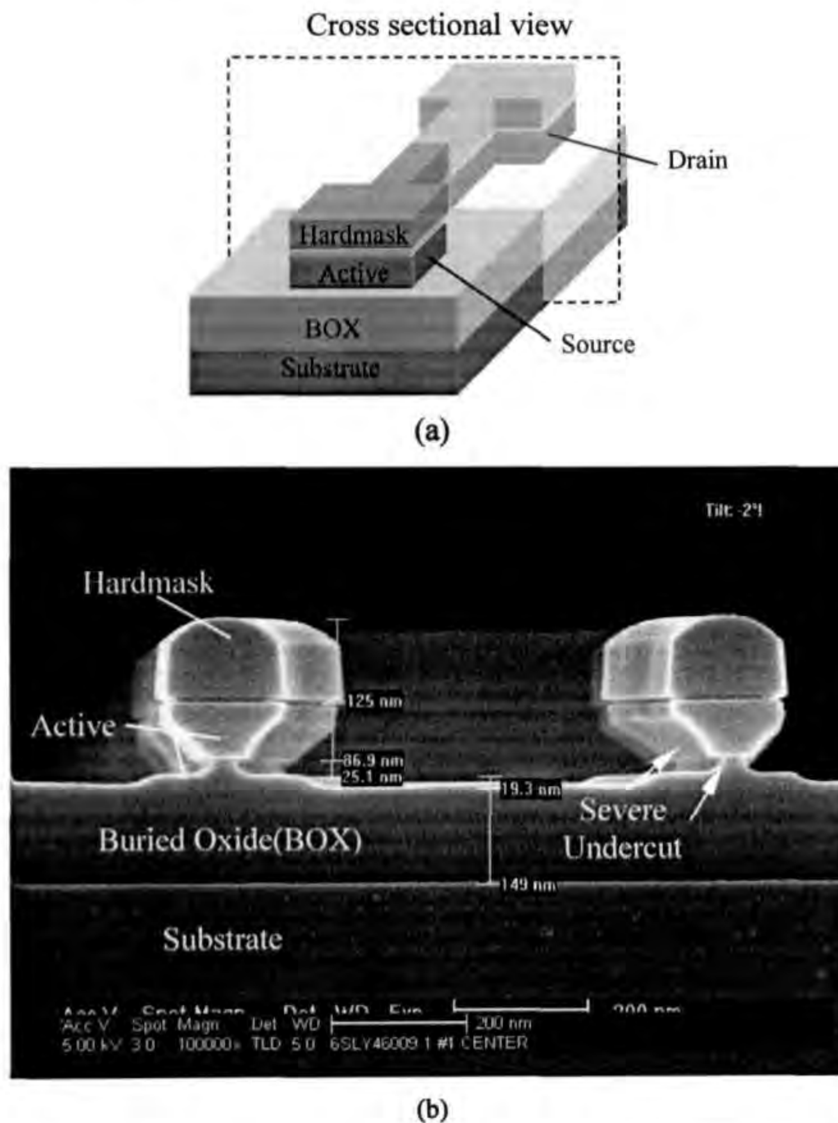

Figure 4.2: (a) Cross sectional schematic illustration and (b) XSEM etch profile of silicon channel using STI etch, under high MAG (100Kx).

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The massive removal is probably due to the low selectivity and the long duration that is applied during the etch process. Besides, the buried oxide also suffers from rigid removal during the ion etchant bombardment. The condition is worsen by the dilute HF that is being used during the post STI clean. As a result, a narrow distorted silicon base is formed underneath. The top and bottom gate dimensions are no longer symmetrical and this can lead to an increase in parasitic gate-drain/source capacitance later on. In fact, the remaining active silicon island is likely to "topple off" in the subsequent fabrication steps since dilute HF is being used as a cleaning agent in every diffusion steps to remove contaminations.

4.2.1 POLY-SILICON RECIPE

Considering the undercutting problem, the STI process is hence replaced by a poly silicon recipe to avoid unnecessary undercut. In this recipe, two main stages are involved.

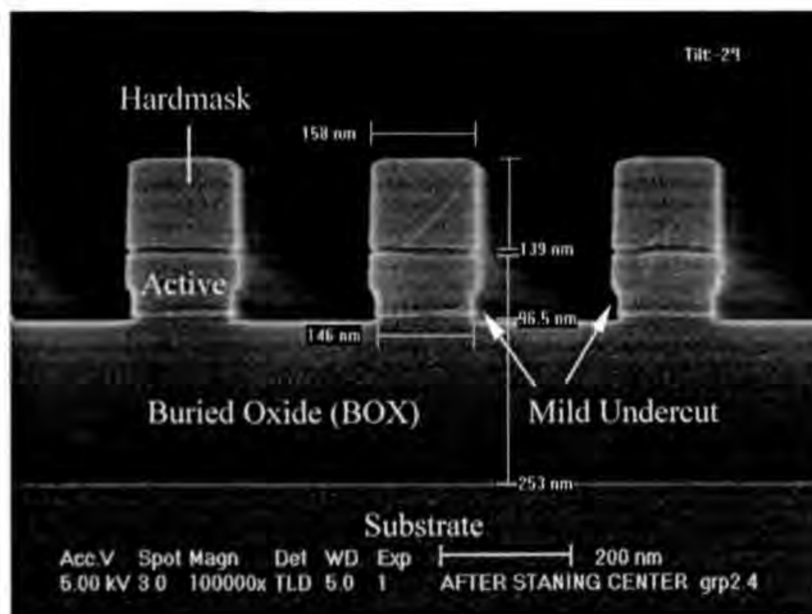

Figure 4.3: XSEM of multiple channels after poly etch seen at high MAG (100Kx).

The end-point detection etch used in the first stage removes silicon material until it reaches the oxide etch stop layer (ESL). The standard time based overetch

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process is next used to remove the remaining stubborn silicon spacers that are formed at the sidewalls of the structure. In Figure 4.3, it is clearly seen that the poly silicon recipe can still create minor undercuts at the footage of the active region.

4.2.2 REVISED POLY-SILICON RECIPE

From the observations, it is noted that the chipped off at the sidewalls are partly contributed by the strong "back blast" effect of the etchant upon bombarding the BOX layer over an excess period of time during the standard over-etch procedure as illustrated in Figure 4.3. On the other hand, the BOX layer shows high selectivity with negligible oxide loss during silicon etch. Findings indicate that the best etch profile can be achieved by using end-point detection etch method with a reduced overetch duration of 15 seconds instead of the normal timing of 45 seconds (see Figure 4.4). There is no sign of significant undercut in the dense structure and especially in isolated structure. Furthermore, nearly zero oxide loss is seen on the BOX layer. A straight sidewall profile can be achieved using the revised recipe.

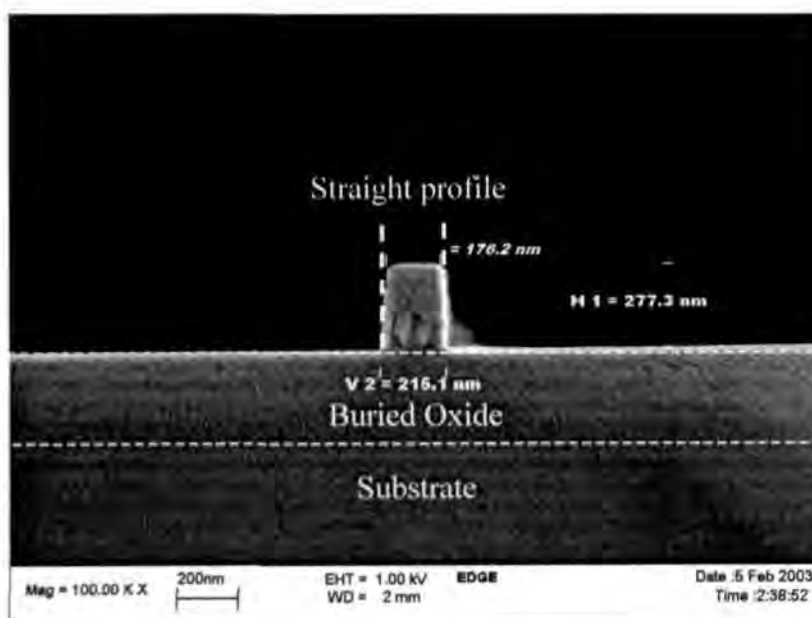

Figure 4.4: XSEM profile of silicon channel using optimised etch recipe.

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4.3 REPLACEMENT GATE MASK FORMATION

Upon forming the SOI active region, a hardmask trench for the BOX cavity known as the replacement gate mask is to be developed. The concept uses the original gate mask and performs a reversal definition of the gate region in a series of steps. In other words, the area that is supposed to form the gate electrode will create a gate trench instead. A stack layer of 1600 Å nitride/ 150 Å oxide/ 1600 Å nitride is first deposited. Next, the wafer is exposed and patterned via gate mask lithography. The top nitride layer is then patterned using standard composite nitride etch recipe (see Figure 4.5). This recipe consists of two procedures, namely the main etch and the overetch processes and some problems have been noted among these critical steps. The end-point detection timing (main etch) is noted to reach to a maximum limit of 55 seconds instead of normal detection timing of 40 seconds. Following the main etch, a normal overetch step is carried out to complete the process. As a result of the two etching procedures, the excess etch causes a punchthrough of the 150 Å into the oxide as well as another 800 Å (approximate) of the bottom nitride film (see Figure 4.5b).

This phenomenon is unusual because the reticle transmission (RT) for gate mask is higher than active mask. This means that more regions will be needed to remove away using the gate mask than the active mask. With more regions exposed, the etch rate should become slower. The etch recipe is also found to have low selectivity for nitride and silicon oxide. It will remove both layers regardless of the presence of the etch-stop layer (SiO_2). Even though the nitride etch rate is slower, it removed the top nitride as well as the 150 Å silicon oxide during the maximum duration of 55 seconds. Subsequently, it went through the over-etch stage which accounted for the other ~800 Å of nitride loss.

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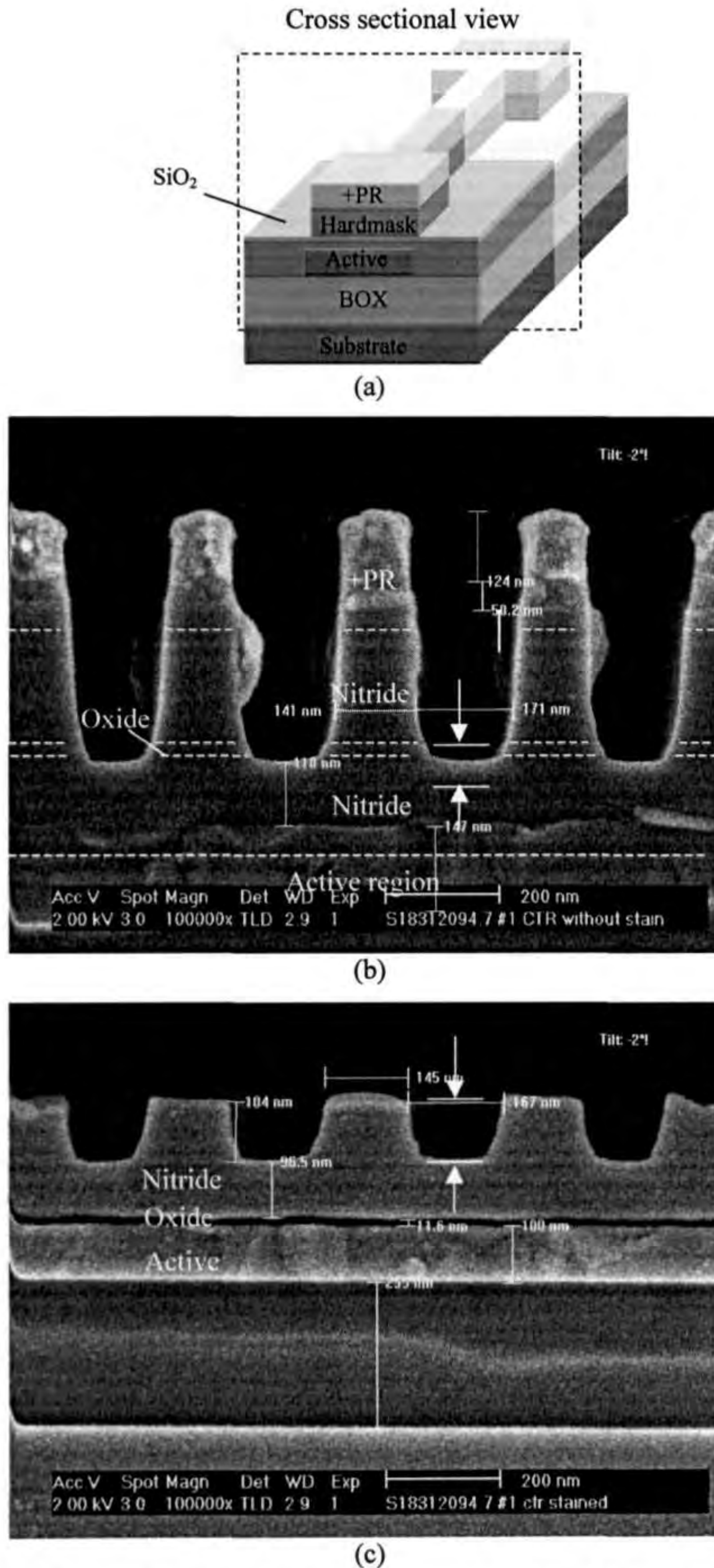

Figure 4.5: (a) Schematic illustration of replacement gate mask formation, (b) XSEM of nitride profile after etch before staining and (c) after BOE staining.

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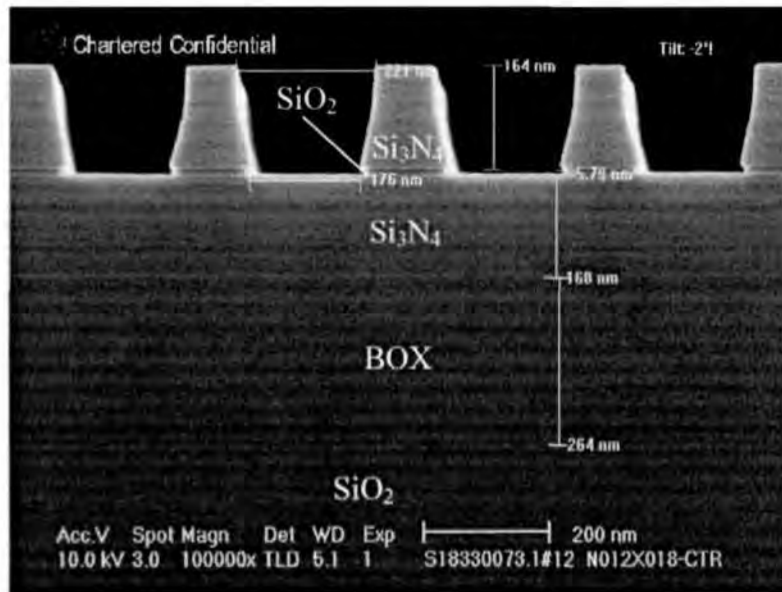
Considering the above, the recipe is replaced by a STI hardmask etch which provides a relatively higher selectivity for nitride and thin silicon oxide. The XSEM images of Figure 4.6 shows that the pitch dimension generally remains the same over the multiple and iso silicon channel, at about 0.18 μm for every opening. The 150 Å sacrificial oxide, which acts as an etch stop layer, retards the etch chemistry from reaching the bottom Si_3N_4 layer. No nitride loss is observed at the bottom.



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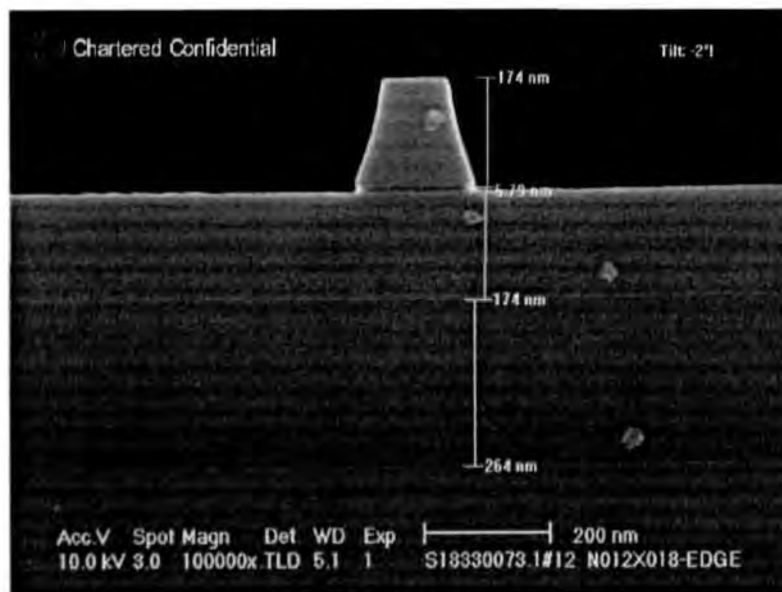

(b)

Figure 4.6: XSEM of nitride profile in (a) multiple channels and (b) single channel.

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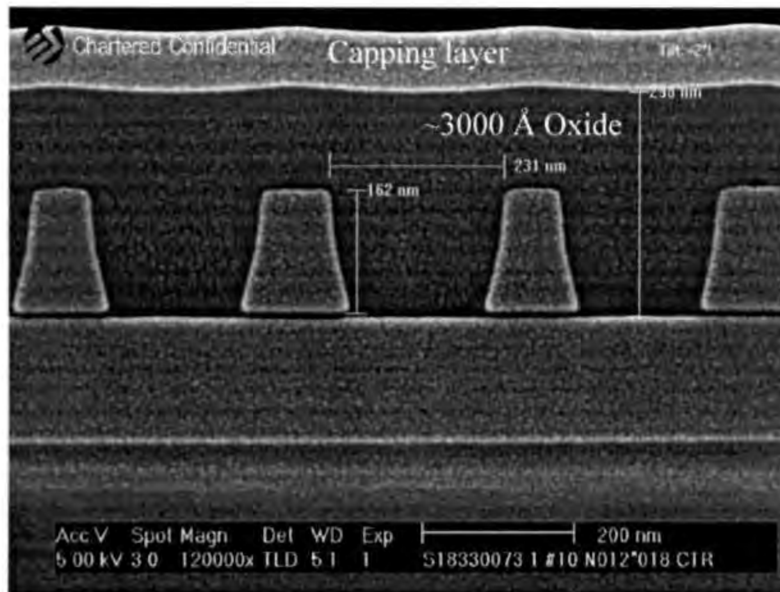
The patterned wafers are then deposited with 3000 Å of oxide, followed by a high temperature oxide densification step at > 950°C for about 15 seconds. In this step, the oxide must be uniformly thick, catering up till at least the top of the nitride strips. This is to allow sufficient room for chemical mechanical polishing (CMP) to be carried out in the following step. Most importantly, the high density plasma (HDP) deposition exhibits good oxide gapfill properties (see Figure 4.7).



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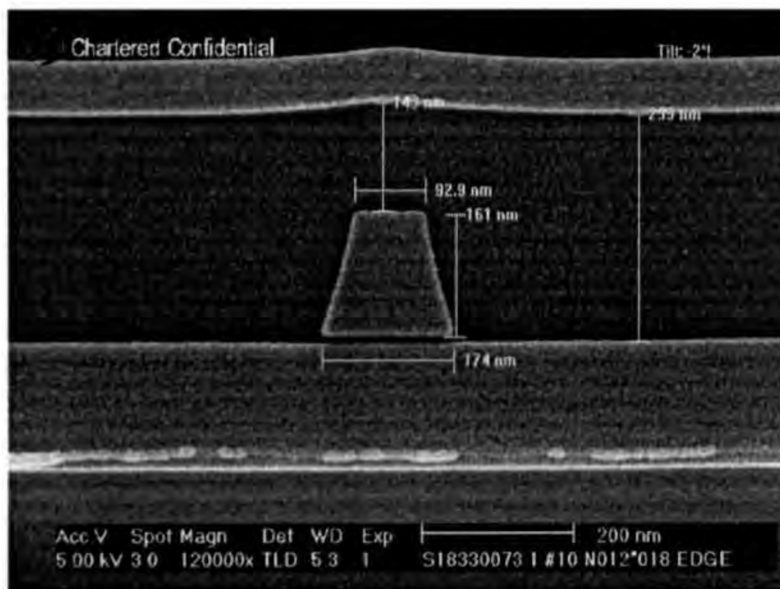

(b)

Figure 4.7: XSEM of oxide deposition profile in (a) multiple channel, (b) single channel.

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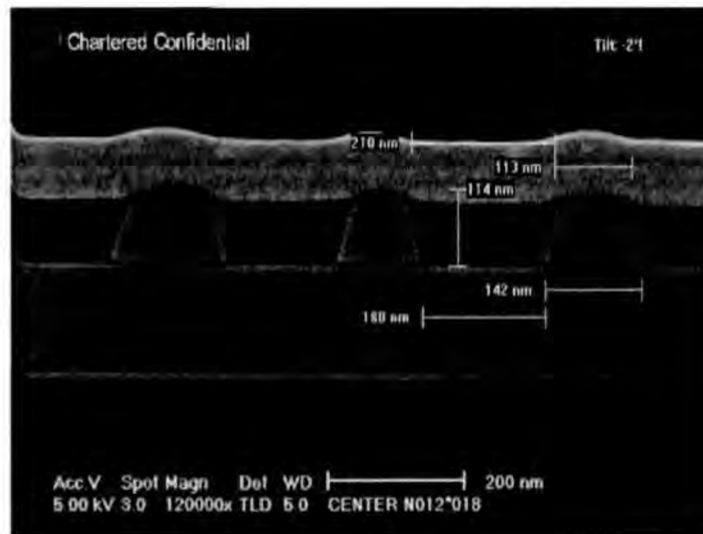
A capping layer is laid on top of the sample to prevent surface oxide removal during light buffered oxide etch (BOE) staining, which is used to provide better contrast for viewing. It is an etching solution containing hydrofluoric acid, HF, and ammonium fluoride, NH_3F. The hydrofluoric acid etches silicon dioxide and the ammonium fluoride raises the solution pH to reduce the solution rate of attack rate on photoresist. So far no pinhole has been found at the edges and sidewalls in the dense and single channels. The rough surface topography attained after post deposition is not a prime concern since CMP is able to planarize the surface at a later stage.



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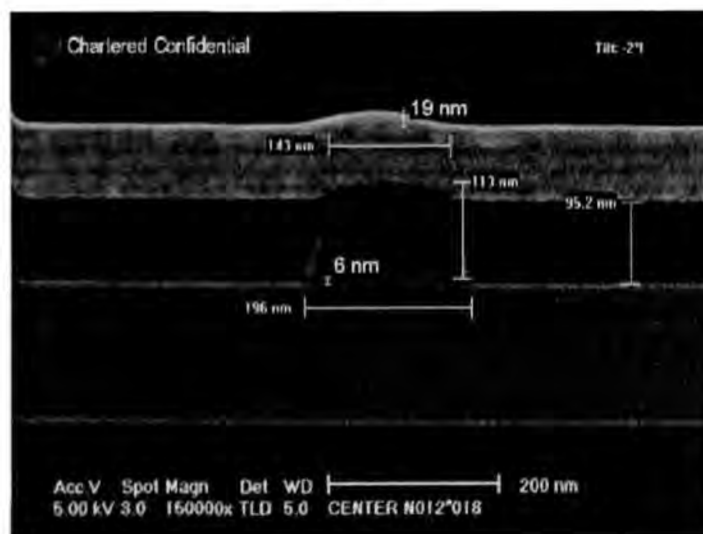

(b)

Figure 4.8: XSEM of oxide CMP profile in: (a) multiple channels and (b) single channel

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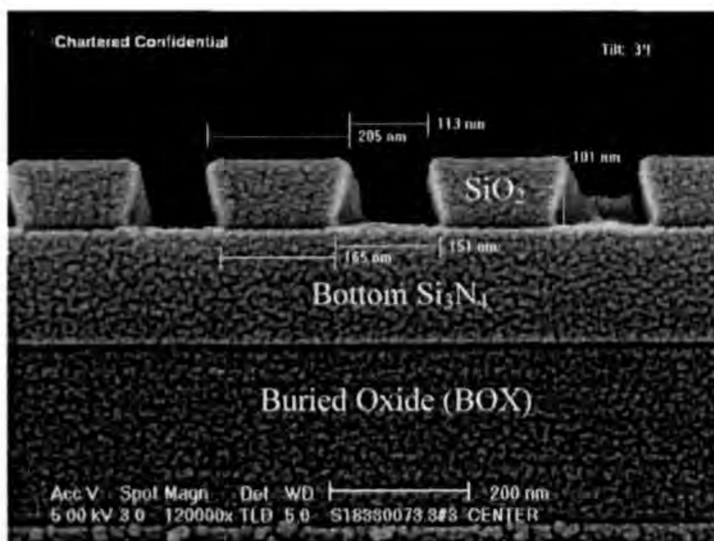
Time based polishing is then carried out to planarize the oxide until it reaches the nitride surface. A total time of 65 seconds is recorded in the two polishing steps to obtain the correct oxide thickness (with a remaining Si_3N_4 > 1000 Å). In addition, a separate final polishing procedure is used to provide light polishing and to remove slurry particles and small wafer defects. A small amount of oxide is buffed away during this procedure (typically 300 to 400 Å), which also aids in the removal of defects. Figure 4.8 shows the uniform profile achieved across the dense (multiple channels) and iso (single channel) structure after polishing.



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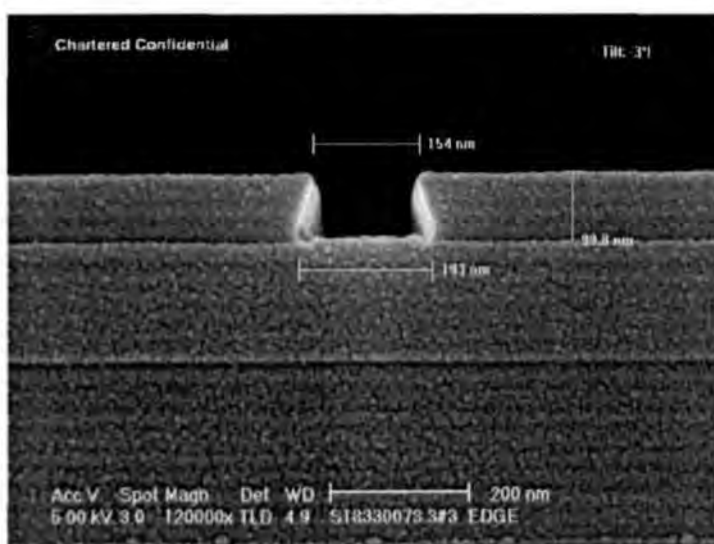

(b)

Figure 4.9: Profile after H_3PO_4 etch for: (a) multiple channels and (b) single channel.

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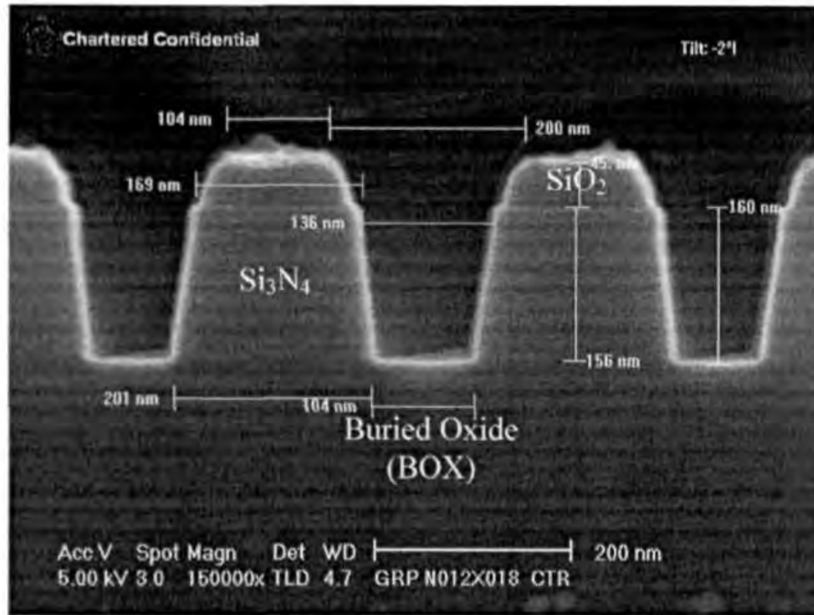

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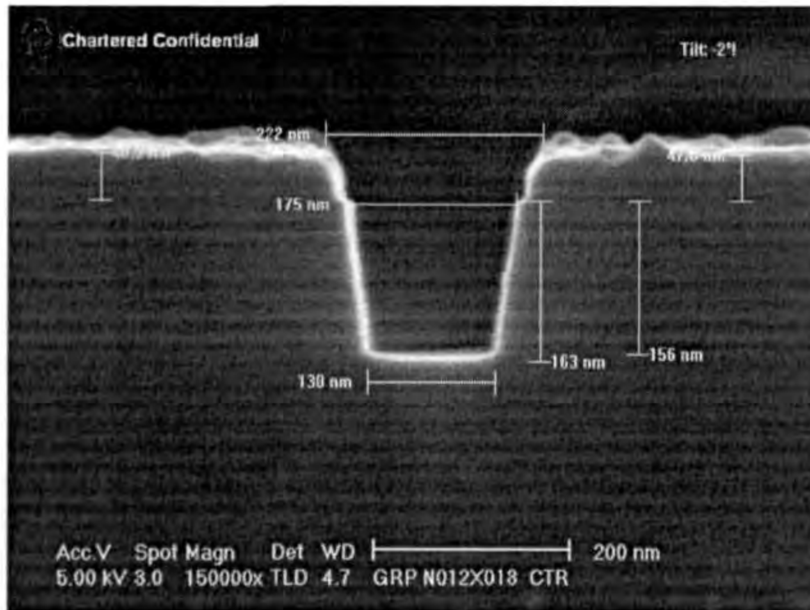

(b)

Figure 4.10: XSEM profile after nitride removal (a) multiple channel, (b) single channel.

Thereafter, the bottom layer of nitride is etched anisotropically for a total time of 65 seconds in a two step removal procedure. Roughly about 500 Å of oxide is also removed during this stage. It is interesting to note that the final profile for the multiple channels hardmask is much smaller than the initial gate length overlay of 0.13 µm (see Figure 4.10). In fact, the measured 100 nm channel width is constantly recorded

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throughout the entire wafer. Hence, we would expect the channel width of the completed device to be much smaller for dense structure (multiple channels). The remaining oxide mask on top of the nitride will be removed during the stage of cavity etch. At this time, it completes the final formation of the replacement gate mask.

4.4 PROPOSED GAA PHYSICAL STRUCTURE

Once the replacement gate mask is formed, it involves an additional wet etch step to form the structure. A diluted HF wet etch is carried out to dig a cavity underneath the gate channel. The objective is to have the deposited poly material wrap around the channel and at the same time fill up the cavity to form the bottom electrode. Initially, experiment with different conditions are carried out to determine the etch rate based on a given standard wet etch recipe. This is to ensure that the cavity profile is well optimized. Should there be any overetch of the cavity, it will result in unnecessary formation of undercut below the source/drain region as well. Once the gate material flows underneath the source/drain region, it will definitely cause a short circuit between the source and drain region. Based on the etch results obtained, the calculated etch rate is approximately equals to 4.5 Å/s. A major problem has been encountered during the formation of the silicon "bridges" for long channel gate length, L_g. During the undercutting process, the source and drain region, which act as supporting pillars at both end are not strong enough to withstand the weight of the silicon bridge. As a result, the channels break apart without the support of the beneath buried oxide (See Figure 4.11). The problem is also aggravated in the subsequent pre-clean step contribute by the strong vibration of the megasonic cleaning technique prior to the gate deposition.

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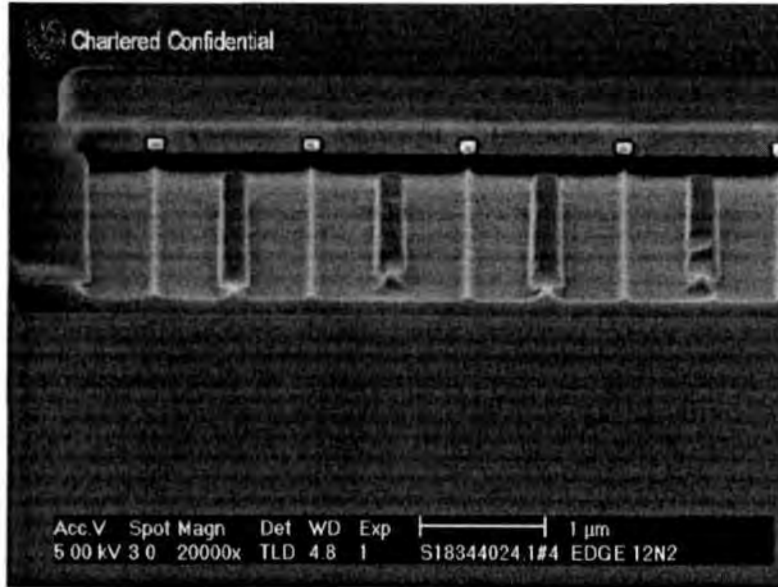

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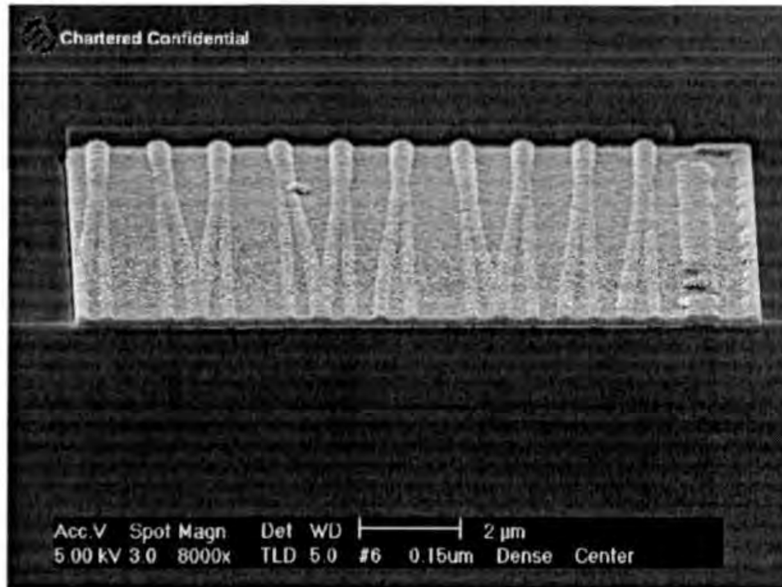

(b)

Figure 4.11: XSEM profile of "fallen" silicon channel (a) before and (b) after gate deposition.

It is noted that the concept of having cavity formation underneath the silicon channel can only be realised in the short channel width. Nevertheless, a set of different etch conditions (see Table 4.1) are carried out to investigate the effect of the undercut beneath the silicon channel over its various electrical behaviour. Figure 4.11 illustrates the GAA profile after 100 and 150 seconds of wet undercut respectively.

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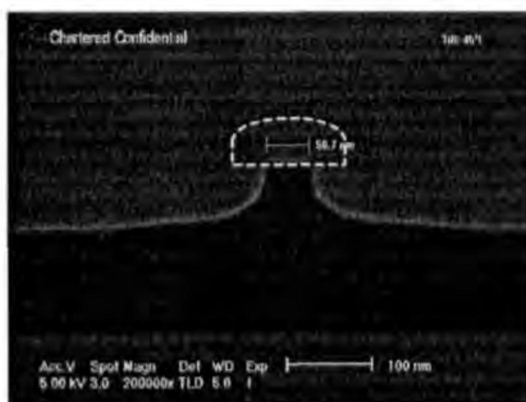
Table 4.1: Different cavity etch conditions.

Wafer	Etch duration (s)	Lateral removal (Å)	Expected oxide remaining (Å)
GAA 11	100	900	500
GAA 12	125	1050	350
GAA 13	150	1200	200
GAA 14	175	1400	0



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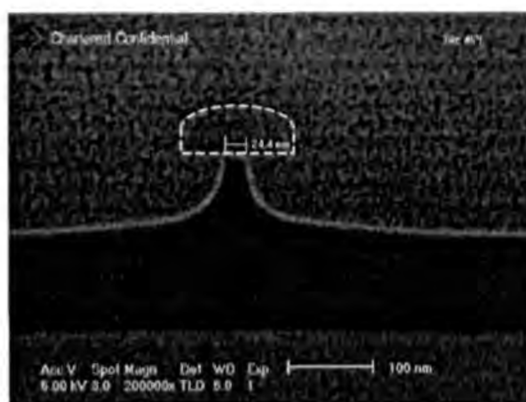

(b)

Figure 4.12: XSEM profile after wet etch of (a) 100 seconds and (b) 150 seconds.

The smallest GAA transistor demonstrated has a dimension of 0.15 μm in width and 0.12 μm in gate length that the 0.13 μm technology can feature (see Figure 4.13). Due to the long channel breakage issue, the usage of mega sonic treatment in the pre clean step is lifted after the cavity formation. This to ensure that the long silicon bridges can physically survived and remain intact after cleaning. However, the absence of the megasonic treatment causes some undesirable effects, such as in higher particle

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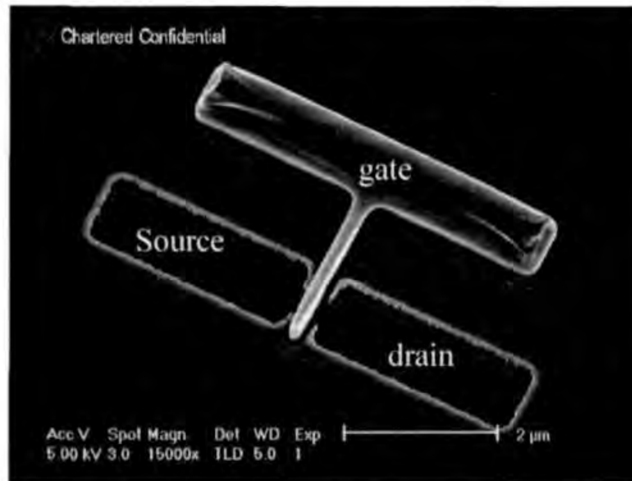
content on the wafer surface since the particles are not being washed out. The other may cause the creation of "crater holes" in the field region (see Figure 4.13b).



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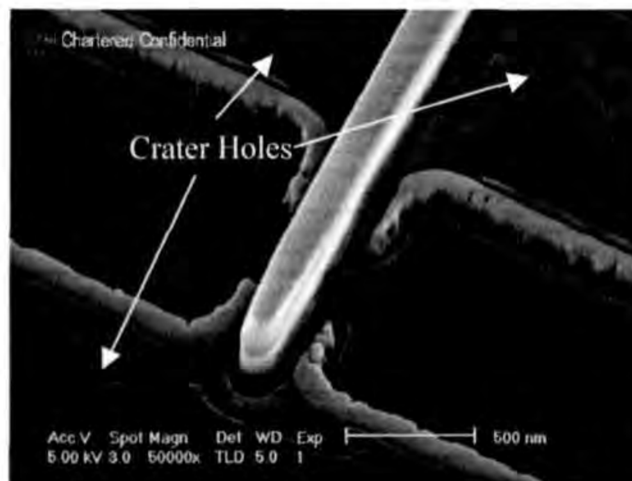

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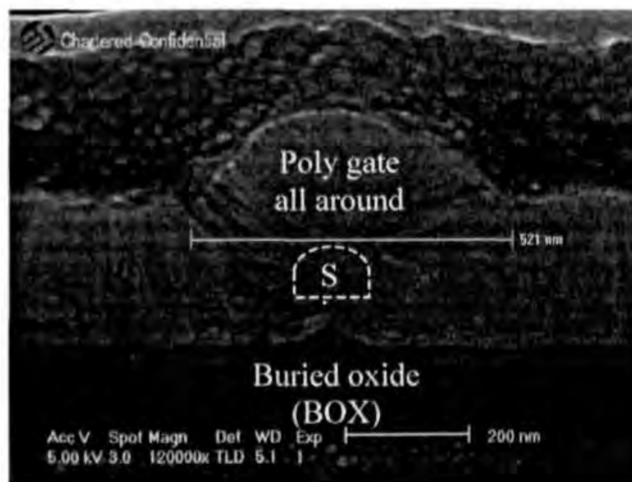

(c)

Figure 4.13: SEM profile of GAA at (a) 15000x, (b) 50000x and (c) 120000x MAG.

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4.5 "n"- GATE PHYSICAL STRUCTURE

The formation is similar to the GAA structure as mentioned above. The only difference is that an etching process is inserted after the active definition so as to achieve a rounded surface channel. It begins with a 1600 Å of nitride layer deposited onto the active region and followed by the etch process. This process consists of two stages, namely the main etch and the overetch procedure. Firstly, the end point detection main etch is carried out to clear most of the nitride hardmask until it reaches the buried oxide etch stop layer (refer to Figure 4.14a). Then, the time based overetch process is in placed to remove the remaining nitride spacers at the sidewalls of the silicon and some stubborn nitride found at the surface. With more directional etch used in the second stage, the removal of the thin layer of nitride capping at surface actually helps to tailor the rounding of the silicon surface (see Figure 4.14b). In other words, the rounded shape of the hardmask formed initially after the first etch is been transferred onto the silicon channel.

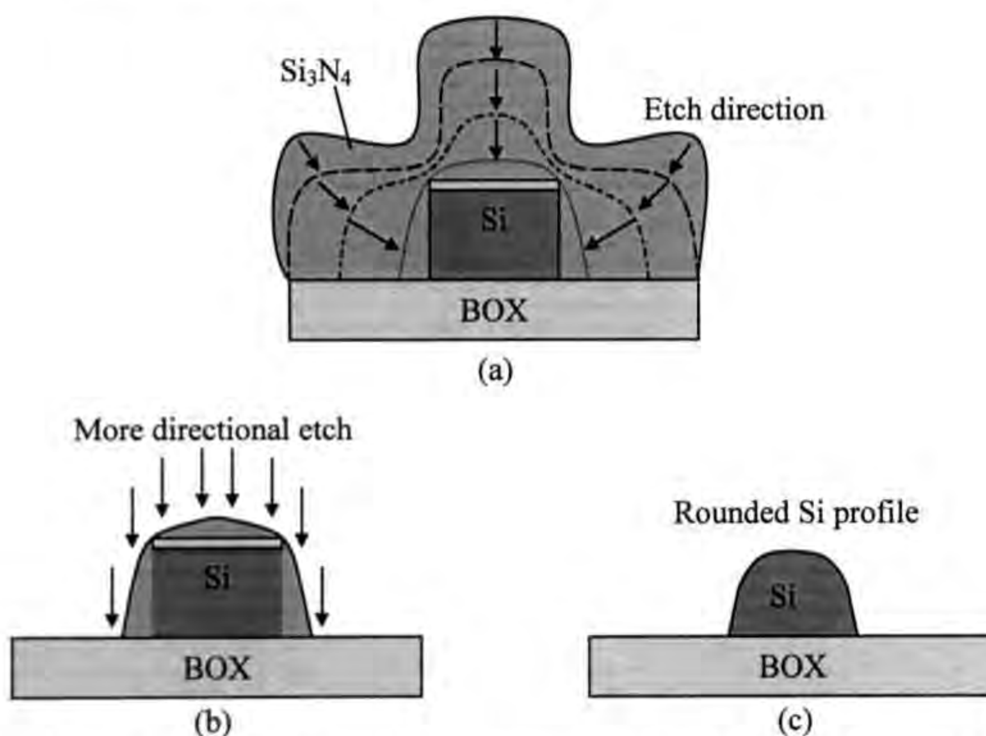

Figure 4.14: Creation of surface rounding (a) main etch, (b) directional overetch and (c) final profile after oxidation and annealing.

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Once the rounded channel is formed, a thermal oxidation is carried out to smoothen the surface roughness, followed by a rapid thermal annealing (RTA) to repair the silicon lattice damages that occur during the nitride etch bombardment (see Fig. 4.14c). The surface rounding technique is successfully demonstrated on both the single and dense channel using the 0.13 μm technology node.

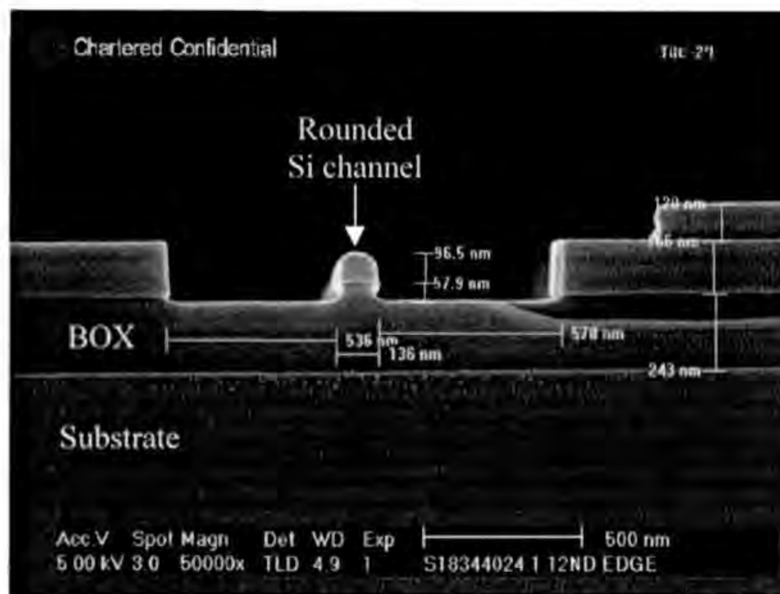

Figure 4.15: XSEM profile of channel width after nitride removal.

Figure 4.15 depicts the cross sectional view of the transistor channel width for both channels. As expected, the multiple channel width (100 nm) is much smaller than the single channel (130 nm) due to the smaller hardmask definition in the earlier stages. The thickness of the body is 960 Å with the top surface smoothly rounded. The structure resembles the shape of a letter "n". Next, the silicon channel is exposed to rapid thermal nitrided oxidation (RTNO) to form a 20 Å layer of gate dielectric. A 2000 Å thick polysilicon is deposited and patterned afterwards to form the gate electrode with sidewalls extend into some depth (~ 500 Å) of the buried oxide. Figure 4.16 presents the SEM images of the "n"-gate single channel transistor structure. The featured gate length is approximately 0.13 μm with a narrow width of 0.09 μm.

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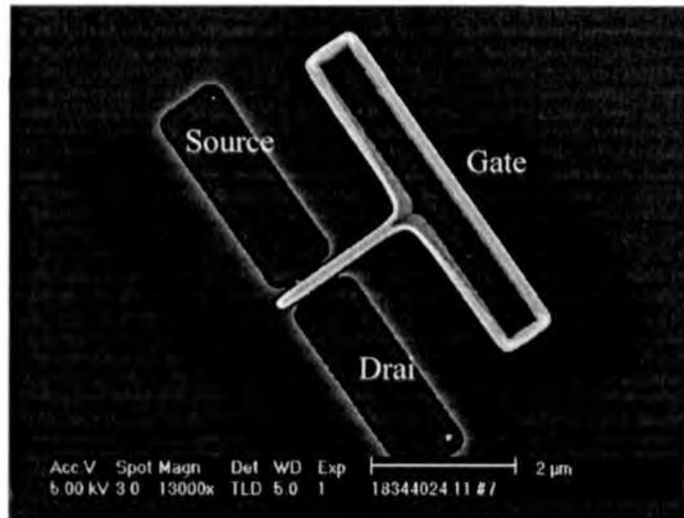

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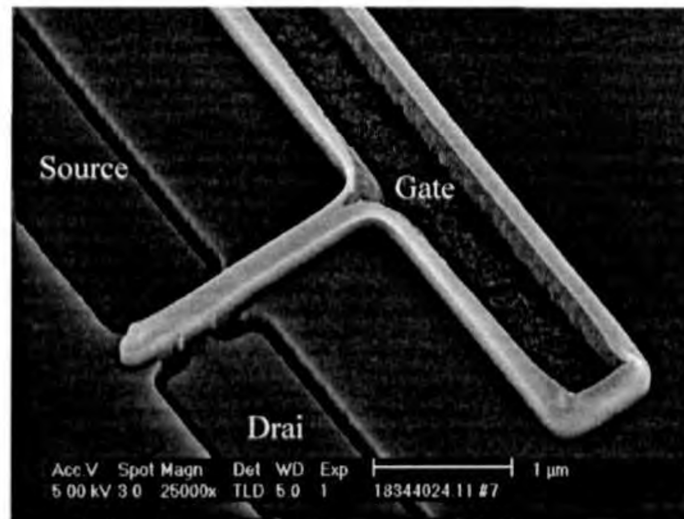

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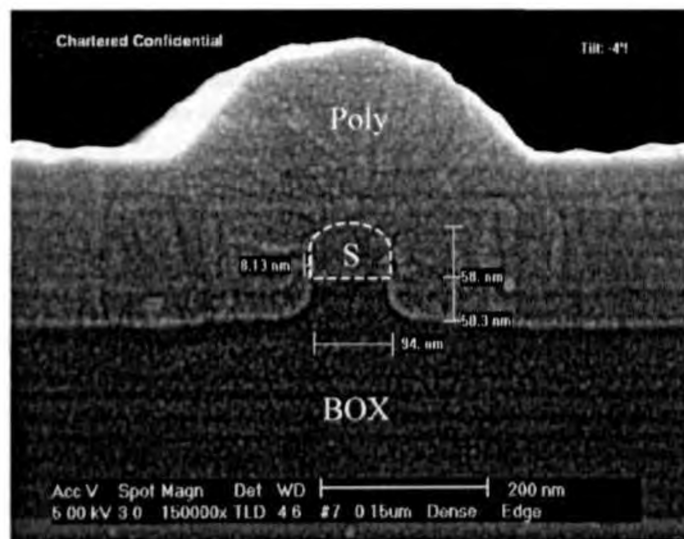

(c)

Figure 4.16: Tilt SEM profiles of NMOS transistor (a) 13000x and (b) 25000 x MAG.

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CHAPTER 5: MULTIPLE GATE DEVICE CHARACTERISATION

This chapter discusses the experimental results derived from the short channel SOI MOSFETs that have been fabricated and outlined in chapter 4. Emphasis is also given to the comparison of experimental findings with different transistor dimensions (0.13 μm and below) for both the SOI n-gate and GAA NMOS transistors. The transistor current-voltage (I-V) characteristics and the short channel behaviour of various transistor parameters are extracted from the experiments will all be detailed.

5.1 PROPOSED "n"-GATE NMOS TRANSISTOR CHARACTERISTICS

As discussed in chapter 3, the proposed n-gate structure provides enhanced gate–to-channel controllability and offers excellent short channel effect properties over other non planar SOI devices. In addition, it eliminates the early turn on effect in the threshold voltage characteristic (see Figure 5.1). The electrical properties of the 0.15 μm and 20 μm channel width NMOSFET n-gate transistors are presented here. This includes the drive current performance, transconductance and short channel effects behaviour. The effects of gate length and channel width variation are also explored in this chapter. The results obtained are separately discussed in the following sub-sections.

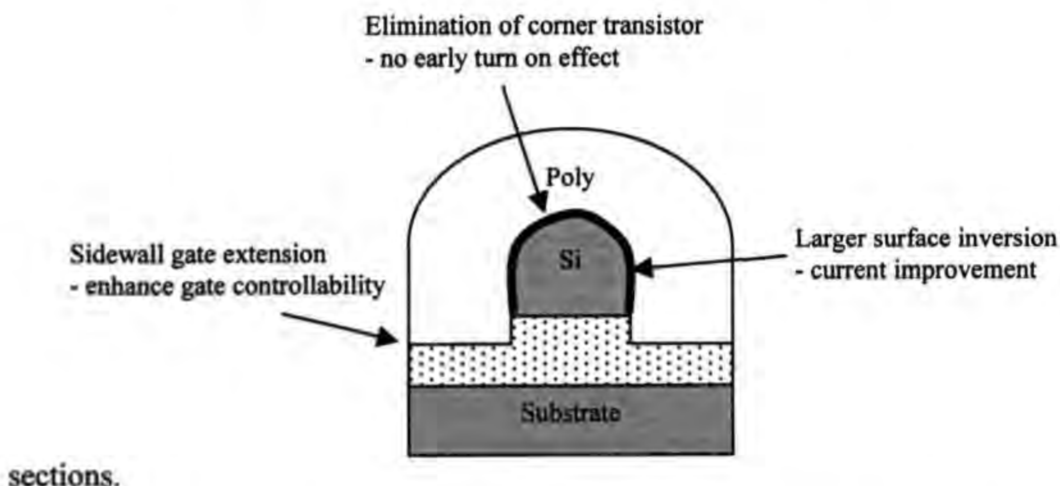

Figure 5.1: The device characteristics of an n-gate NMOSFET.

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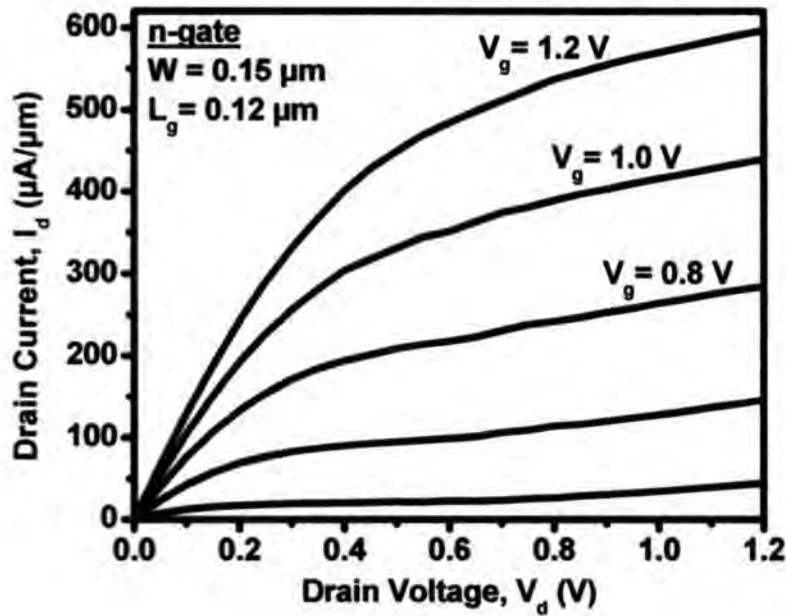
5.1.1 "n"-GATE NMOS TRANSISTOR (SHORT CHANNEL WIDTH)

In Figure 5.2a, the drive current is plotted as a function of drain voltage for different gate overdrive. The narrow width 0.12 μm n-gate NMOS transistor displays a drive current capability of 600 μA/μm at V_g = 1.2 V. The threshold voltage is recorded as 0.223 V (see Figure 5.2b). The extracted V_{th} is defined as the voltage measured at I_d = 0.1*(silicon width/ gate length) and in this case, the corresponding I_d is of 125 nA.



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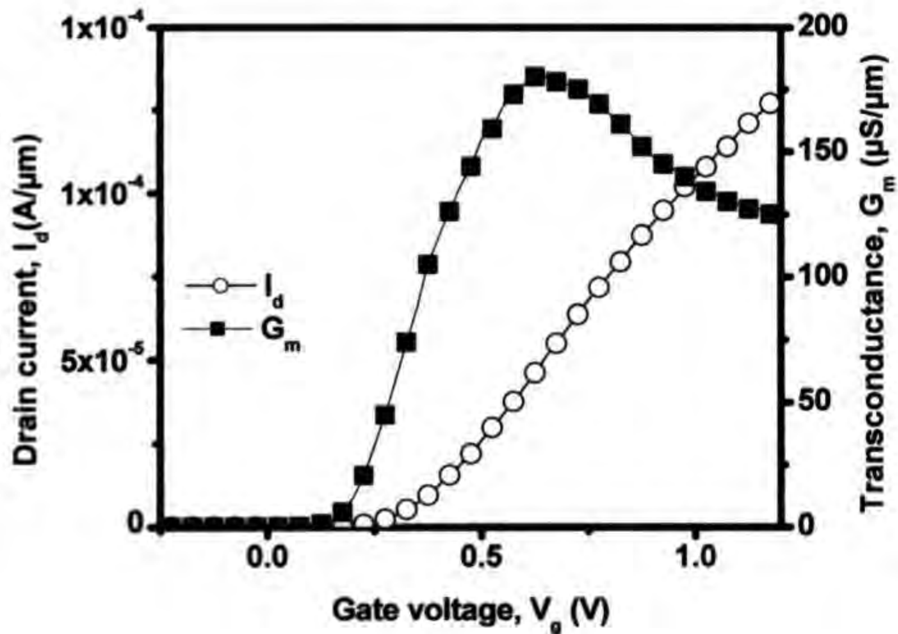

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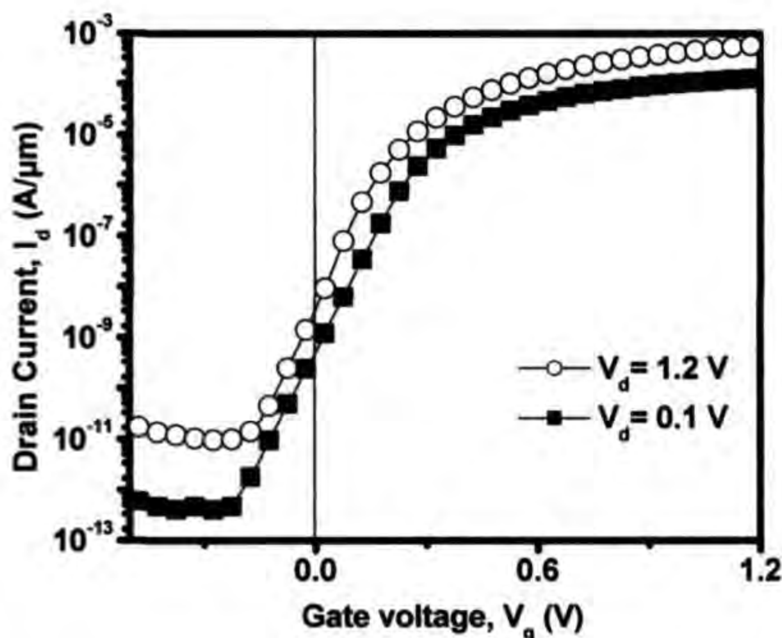

(c)

Figure 5.2: A narrow width 0.11 µm n-gate NMOSFET (a)I_d- V_d characteristics (b) I_d-V_g characteristics and (c) Subthreshold slope and off state leakage current characteristic.

The observed device transconductance beta (the slope of the I_d-V_d curve in linear region) is quite steep. This reflects the low parasitic resistance can be achieved by the use of cobalt silicidation in source/drain regions. The novel n-gate device also managed to achieve excellent short channel characteristics, whereby a near ideal substhreshold slope of 64 mV/dec is observed during linear and saturation region, where V_d = 0.1 and 1.2 V respectively. The drain induced barrier lowering (DIBL) is of 83 mV/V and the low off-state leakage current I_{off}, is only of 3.11 nA/µm at V_d = 1.2 V (see Figure 5.2c). Here, the subthreshold slope is defined as the gate voltage shift required to increase the drain current in the exponential subthreshold region by one order of magnitude. The experimental results are unanimous in proving that the short channel effects are much attenuated in the proposed narrow width n-gate device as compared those derived from bulk silicon technology.

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5.1.2 "n"-GATE NMOS TRANSISTOR (LONG CHANNEL WIDTH)

Figure 5.3 features the I_d-V_d characteristics of the 20 μm width by 0.11μm gate length n-gate NMOS transistor. The NMOS device current drive performance is found to be 430 μA/μm at a drain voltage of 1.2 V. It is interesting to note that an abrupt increase in saturation current occurs when the drain voltage is increased above 0.6 V. This phenomenon denotes the setting-in of the kink effect under strong biasing conditions.

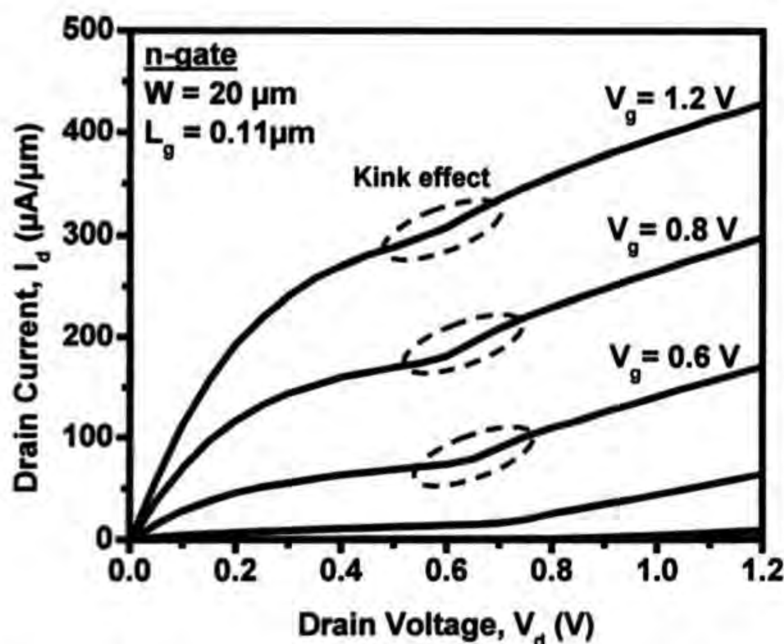

Figure 5.3: I_d-V_d characteristics of a 0.11 μm n-gate NMOSFET.

This is mainly due to the creation and accumulation of electron-hole pairs via impact ionization in the large neutral body width that is left floating underneath the depletion region. When the forward biasing of the body-to-source junction is sufficient to turn on the device, the body potential will decrease and lower the operating threshold voltage. The kink effect leads to improved current and transconductance value. It is not entirely harmful for digital application. In fact, such devices inherently

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Next, Figure 5.4 presents the graphical threshold voltage, V_{th} and the transconductance, G_m at a drain voltage, V_d of 0.1 V. The transconductance is a measure of the effectiveness of the control of the drain current by the gate voltage. Given $V_d = 0.1$ V, the V_{th} and $G_m(max)$ are measured to be 0.525 V and 260 μS (see Figure 5.4) respectively.

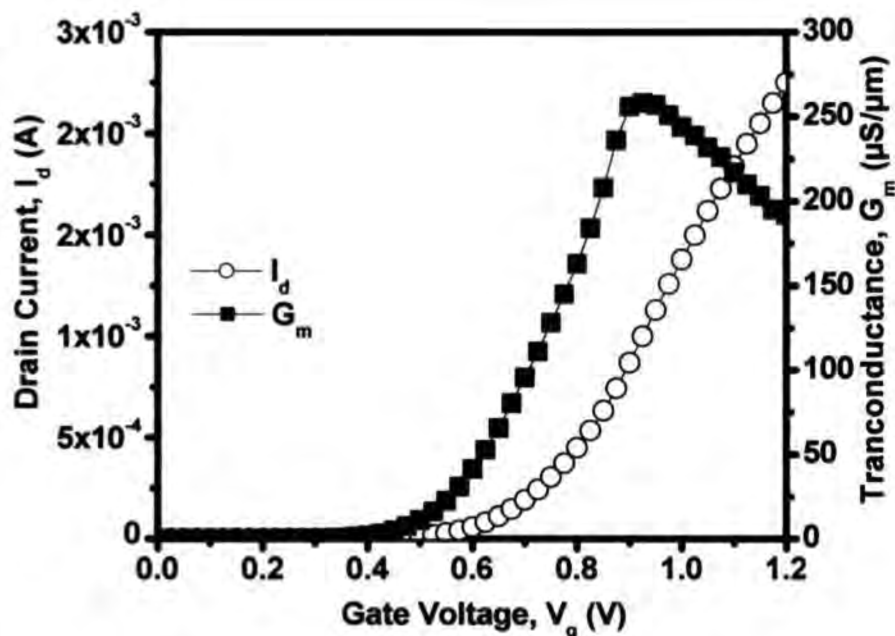

Figure 5.4: I_d- V_g characteristics of a 0.11 μm n-gate NMOSFET.

Figure 5.5 shows the subthreshold I_d-V_g characteristics of the n-gate NMOS transistor. The drain bias,V_d is taken as a parameter and varies from 0.1 to 1.2 V. It demonstrates quite good subthreshold transistor behaviour of 73 mV/dec at smaller drain voltage of 0.1 V. However, it degrades significantly to 140 mV/dec at higher drain bias of 1.2 V. This is an immediate consequence of the increased potential at the SOI/buried oxide interface. A high off-state leakage current, I_{off} of 740 nA/μm is also recorded at 1.2 V operating conditions.

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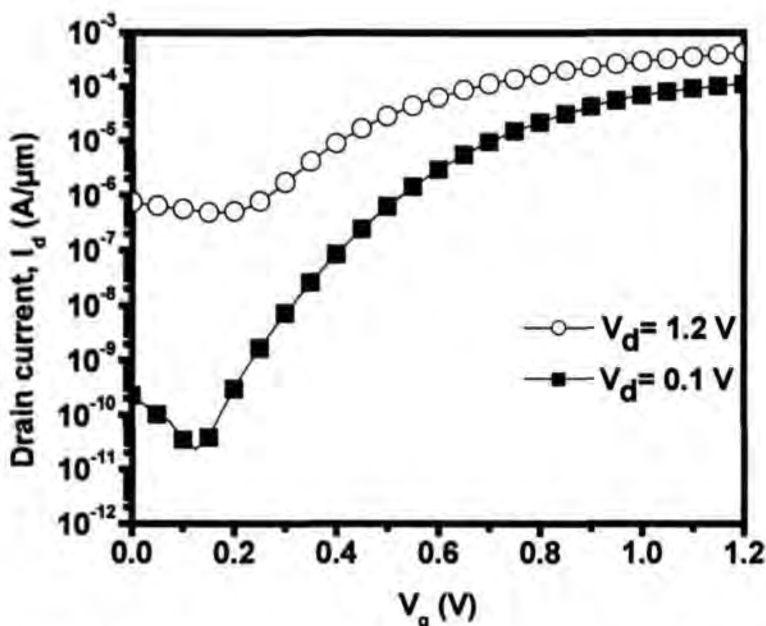

Figure 5.5: Subthreshold characteristics of the 0.11 μm n-gate NMOSFET.

Other than the poor subthreshold behaviour at higher drain voltage and high off-state leakage, the long width n-gate device also presents a poor DIBL value of 275 mV/V, which becomes artificially high and to some extent loses its meaning. The elevated DIBL degradation attributes to the floating body effect where the potential is able to rise as drain charges leak through the drain-body junction diode. As a result, the threshold voltage of the device lowers, complementing the natural barrier lowering of normal CMOS at shorter channel lengths. As the body voltage rises, the channel length actually remains long because the space charge region surrounding the high-voltage shrinks. This subdues short channel effect threshold voltage reduction. Nonetheless, the body voltage has a larger influence on the threshold voltage and so the device appears to have large DIBL. Depending on process, an n-gate device with its body contact connected to a stable potential will revert to the bulk-CMOS DIBL value.

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5.1.3 EFFECTS OF DIFFERENT GATE LENGTH FOR N-GATE DEVICE

In this section, the electrical properties of the proposed n-gate NMOSFET are analyzed and discussed for various gate lengths at L_g = 0.11, 0.12 and 0.13 μm respectively. Figure 5.6 compares the drain saturation current in a number of n-gate NMOS transistors with different gate lengths, as a function of the gate overdrive (V_g-V_{th}). A larger current is observed when shorter gate length, L_g, is considered. At a gate overdrive of 1.2 V, the 0.11μm gate length NMOS present an 8% and 17% current improvement over the 0.12 μm and 0.13 μm gate length NMOS structure respectively.

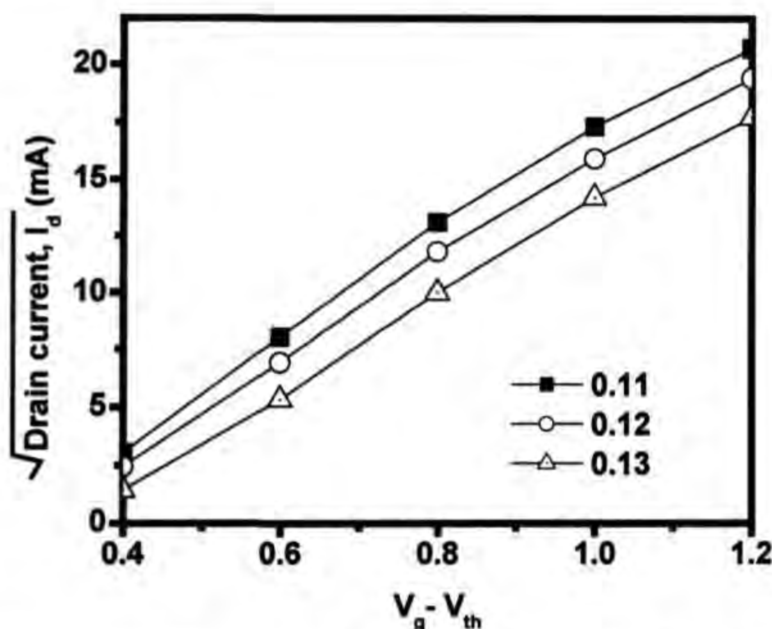

Figure 5.6: Drive current characteristics at different gate length for n-gate NMOS transistor.

As demonstrated in Figure 5.7a, the maximum transconductance, G_m of all gate lengths is comparable at the linear region. However, the maximum G_m for a 0.11 μm L_g is better than the 0.12 μm and 0.13 μm L_g structures by 9.2% and 23% in the saturation region. In Figure 5.7b, the off-state leakage current obtained at V_g = 0 V and V_d = 1.2 V is depicted. The measured I_{off} for L_g = 0.11μm is 740 nA/μm whereas at L_g = 0.13 μm, the I_{off} = 468 nA/μm. However, it is unexpected that the I_{off} for L_g = 0.12 μm is 1.67 μA/μm, which is higher than the rest. Theoretically, one with a shorter gate

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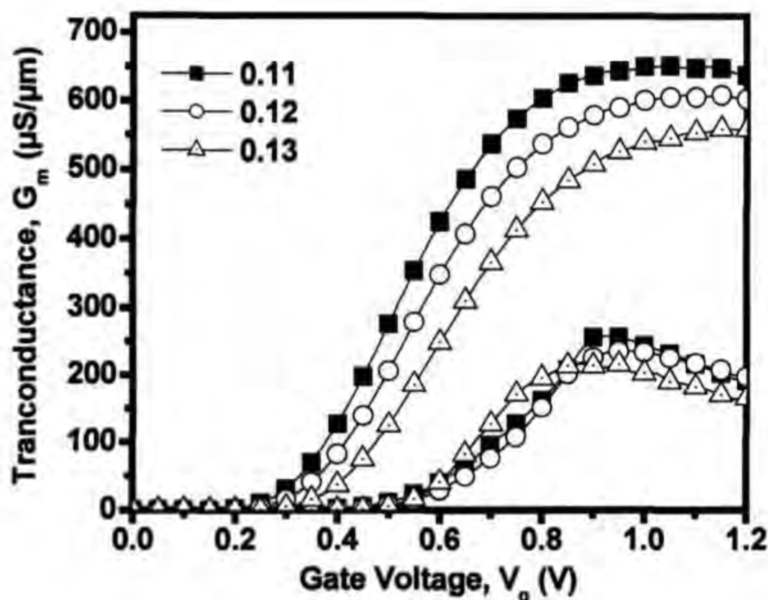
length will tend to cause higher leakage due to the lower threshold voltage and higher electric field that is induced under strong drain biasing. In fact, this phenomenon actually happens for the L_g = 0.11 μm and 0.13 μm only. We suspect that the leaky characteristic of L_g = 0.12 μm NMOS transistor is most likely caused by poor gate oxide integrity, which creates additional leakage paths between the source to drain.



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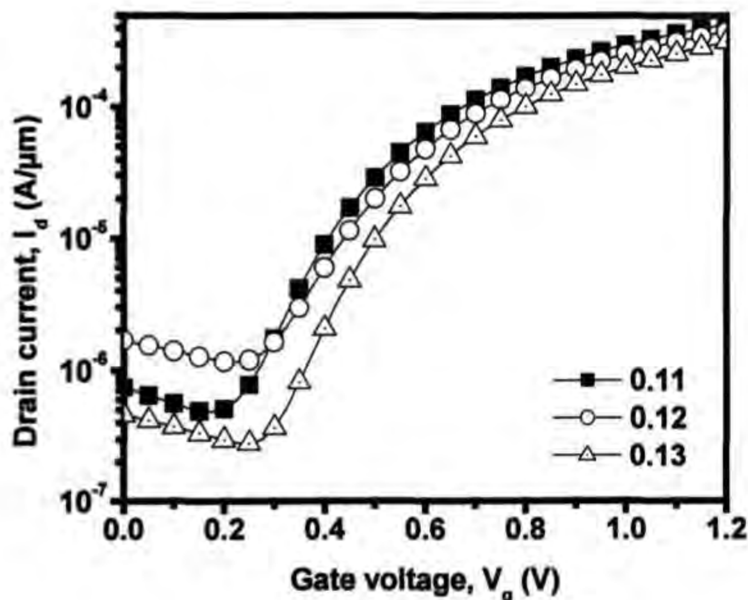

(b)

Figure 5.7: n-gate electrical characteristics for different gate length (a) transconductance and (b) subthreshold slope and off-state leakage current.

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The effect of higher I_{off} incurred in 0.12 μm NMOS transistor has certainly affected the subthreshold slope. A similar subthreshold slope close to about 140 mV/dec, operating in saturation region is illustrated in Figure 5.7b for both the 0.11 μm and 0.13 μm NMOS devices. The subthreshold slope is slightly more than 160 mV/dec for the 0.12 μm device

Table 5.1 summarizes the electrical properties on different gate lengths for the proposed n-gate structure. It is observed that the 0.11 μm n-gate NMOS transistor offers the best current drive and transconductance at a lower threshold voltage. It also exhibits better short channel behaviour such as excellent subthreshold behaviour during linear operation.

Table 5.1: Electrical characteristics on different gate length for n-gate NMOSFET.

Gate Length, L_g (μm)	0.11	0.12	0.13
Drive current, Id_{sat} (μA/μm)	463	433	395
Threshold voltage, V_{th} (V)	0.525	0.554	0.602
Transconductance, Gm_{max} (μS/μm)	652	609	559
Subthreshold slope (mV/dec)	70	-	84
DIBL (mV/V)	275	329	256
Off-state current, I_{off} (nA/μm)	740	-	468

5.1.4 EFFECTS OF DIFFERENT CHANNEL WIDTH FOR N-GATE DEVICE

The effect of different channel widths for the n-gate NMOSFET are also studied to investigate on the various basic electrical properties. Two sets of different channel widths are compared, namely the long 20 μm and short 0.12 μm L_g n-gate NMOS transistors. Figure 5.8 provides a comparison of the drive current for different

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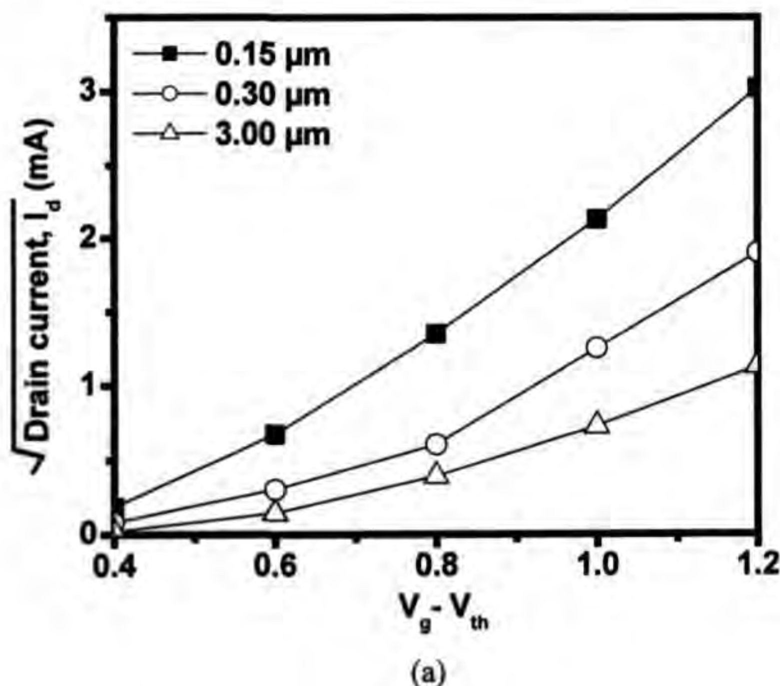
channel widths. For the 20 μm L_g n-gate device, an increasing current trend is noted, whereby a wider spread is observed over a higher overdrive gate voltage (V_g- V_{th}). Under a strong overdrive of 1.2 V, the 0.15 μm channel width device exhibits the highest current drive amongst the rest. A 59% and 167% improvement in current drive is recorded over the 0.3 μm and 3.0 μm channel width respectively. A similar trend is also observed for short channel n-gate NMOSFET (see Figure 5.8b).

The 0.15 μm channel width device yields 52.5 % enhancement in drive current when compared to the large 20 μm channel width device. This current enhancement signifies that the construction of a gate electrode that extends into some depth of the buried oxide will play an important role in improving the current drive performance as well. Most probably, multiple inversions or conduction have taken place at the channel surface, sidewalls or even beneath the silicon channel due to the extended gate electrode, contributing to the eventual improved current drive performance.



(a)

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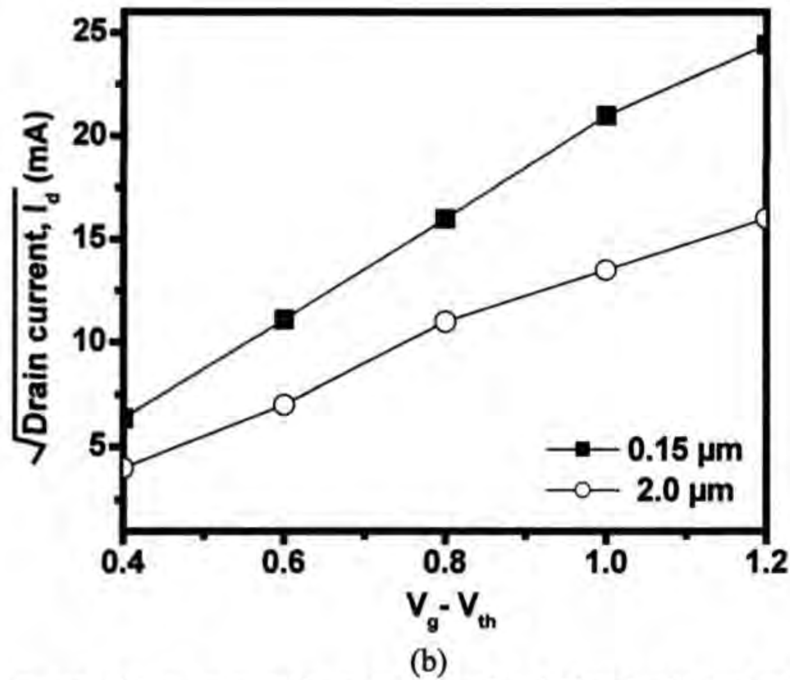

(b)

Figure 5.8: n-gate drive current characteristics for different channel width (a) long L_g (20 µm) and (b) short L_g (0.12 µm).

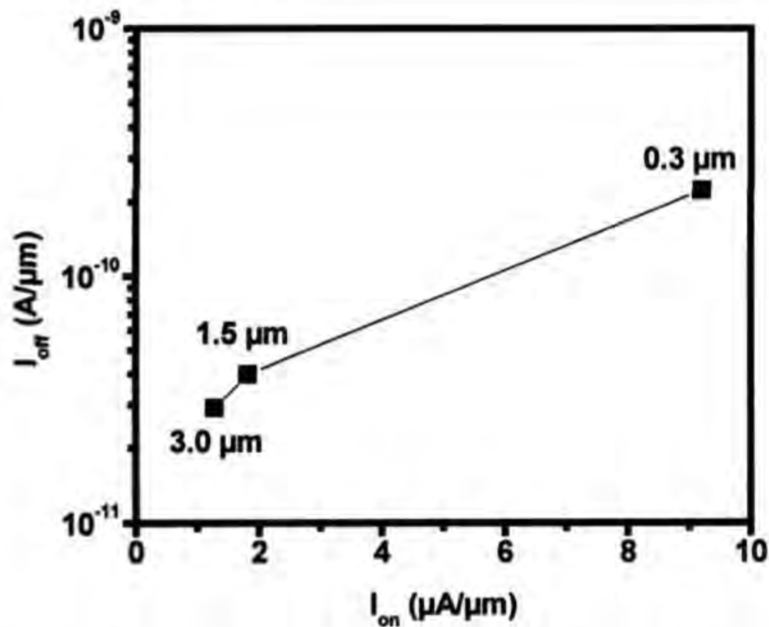

Figure 5.9: n-gate drive current characteristics for different channel width (a) long L_g (20 µm) and (b) short L_g (0.12 µm).

The I_{on}-I_{off} characteristics of the n-gate NMOS device with different channel widths are summarized in Figure 5.9. At a fixed gate length of 20 µm, the on-state current of 9.2 µA/µm is obtained at a leakage current of about 220 pA for the 300 nm device. The leakage current increase rapidly as the channel width is scaled down.

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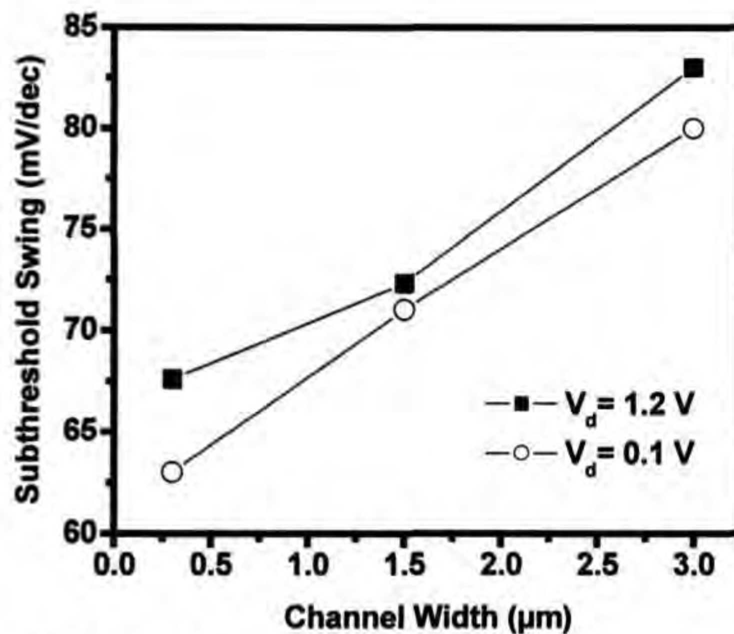

Figure 5.10: Subthreshold slope of the n-gate NMOS device as a function of channel width.

Dependence of the subthreshold slope of the n-gate NMOS device on the channel width is demonstrated in Figure 5.10. From the graph, it is worth noting that the subthreshold slope at $V_d = 0.1$ V decreases from 80 mV/dec to 62 mV/dec when the channel width is scaled from 0.3 μm to 3.0 μm. At low biasing condition where $V_d = 0.1$ V, the overall subthreshold behaviour for all the devices are improved slightly. This is a clear indication that the excellent value of the subthreshold value in small channel width n-gate transistor permits the usage of smaller threshold voltage than that of bulk devices without increasing the leakage current. As a result, better speed performance can be attained, especially at low supply voltages.

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5.2 PROPOSED GAA NMOS TRANSISTOR CHARACTERISTICS

In this section, the electrical behaviour of the GAA transistor is presented. The GAA transistor offers multiple surface inversions where the inversion charge spreads throughout the entire surface of the ultrathin silicon body (see Figure 5.11). The device characteristics can be enhanced tremendously. The GAA is well known for suppressing short channel effect (SCE) such as Drain Induced Barrier Lowering (DIBL) and subthreshold slope degradation. GAA designed with a bottom gate extended into the buried oxide underneath the active silicon film, will effectively shield the back of the channel region from the electric field lines directed from the drain. Thus, it is capable of suppressing the DIBL effect and reducing the subthreshold current. Different gate configurations due to the silicon channel undercutting are also inspected.

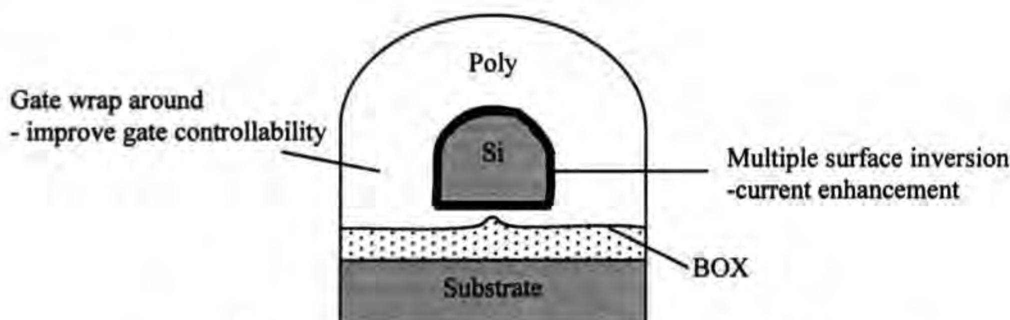

Figure 5.11: The device characteristic of a GAA MOSFET.

5.2.1 0.12 μm GATE-ALL-AROUND (GAA) NMOS TRANSISTOR

Figure 5.12 features the Gate-All-Around of narrow width (0.12 μm) structure MOSFET device (I_d-V_d characteristics). This novel GAA device with the gate coverage extending to the beneath the silicon channel exhibits a substantial current drive of 1200 μA/μm. No kink effect has been observed. The slope of the I_d-V_d curve in the linear region reflects a considerably low series resistance. Note that cobalt silicidation has been employed in the NMOS devices discussed in this thesis.

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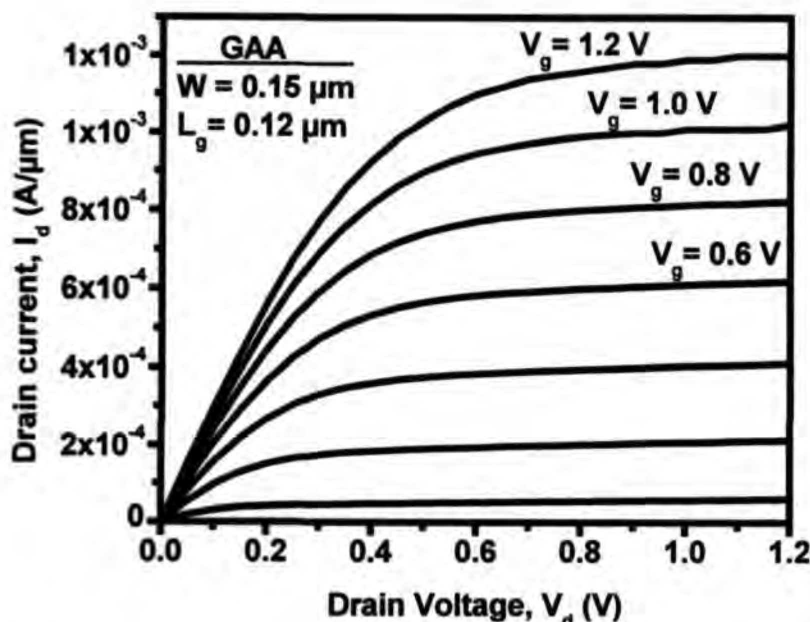

Figure 5.12: The I_d- V_d characteristics of the narrow width 0.11 μm GAA NMOSFET.

The graphically extracted threshold voltage is of a negative value at 0.194 V (see Figure 5.13a). This is because of the low n+ poly gate work functions (Φ_m) of 4.17 eV that is insufficient to achieve the desired positive threshold voltage. In order to obtain a proper V_{th}, the submicron device requires a range of gate work functions of say 4.4 ~5.0 eV. This precludes the deployment of poly-Si as a gate material. Hence, midgap metal gates maybe suitable for use to attain the desired V_{th} for the GAA NMOSFET. Besides, the metal gate offers lower gate sheet resistance, and the retardation of boron penetration and poly depletion in deep submicron MOSFET. Despite the fact that the proposed GAA fabrication process is limited to the used of n+ poly gate material for the NMOS device, different gate materials are analysed so as to evaluate the shifting of the Id-Vg characteristics along the Vg axis with respect to the corresponding work function difference.

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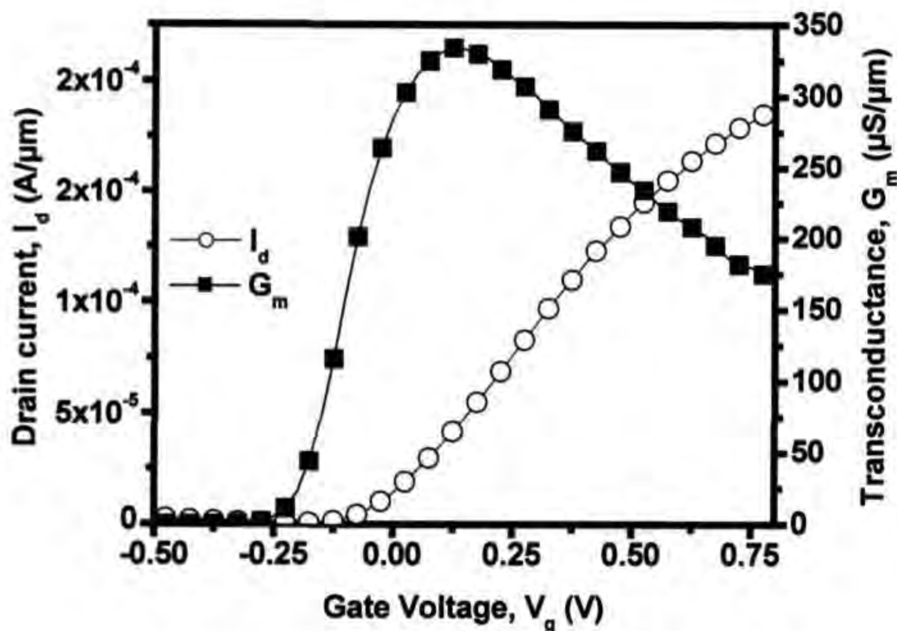
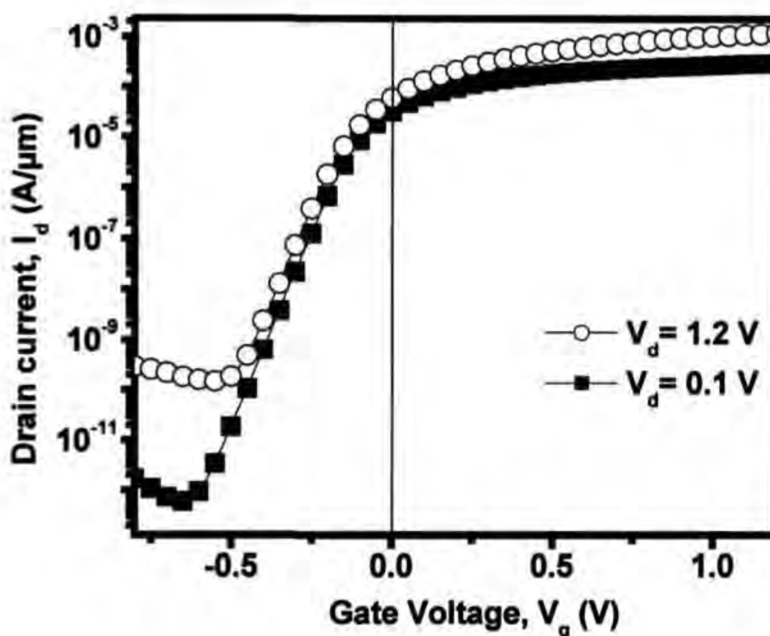


(a)



(b)

Figure 5.13: A narrow width 0.11 µm GAA-gate NMOSFET (a) I_d- V_g characteristics and (b) Subthreshold slope and off state leakage current characteristic.

The of the negative threshold voltage in GAA device has resulted in a very leaky, I_{off} of 55 µA/µm at V_g = 0 V. This reading is however not a true reflection of the I_{off} value since the device is conducting appropriately at the point of time. In the case

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of a metal gate, the I_{off} falls onto the nanometer regime. Nevertheless, the GAA NMOSFET still demonstrated excellent DIBL properties of 32 mV/V. A near-ideal subthreshold slope behaviour of 65 mV/dec and 69.5 mV/dec at both the linear and saturation operating region, independent of the gate material used are also observed.

5.2.2 EFFECTS OF DIFFERENT GATE ELECTRODE EXTENSION

Figures 5.14 (a) to (d) present different gate configurations fabricated in the project so as to understand and analysis the effect of gate electrode extension on the GAA NMOS transistor electrical behaviour. The first figure illustrates a basic n-gate design with the gate electrode extends into the buried oxide without any undercut beneath the silicon channel. As for the rest of the structure (see Figure 5.14 (b) – (d)), the gate configuration have been exposed to different etch timing at: b)100 seconds; c)125 seconds and d)150 seconds respectively. Narrow width transistors of 0.12-µm gate length are used as reference for device comparison on the drive current capability and the short channel properties such as subthreshold slope and DIBL behaviour.

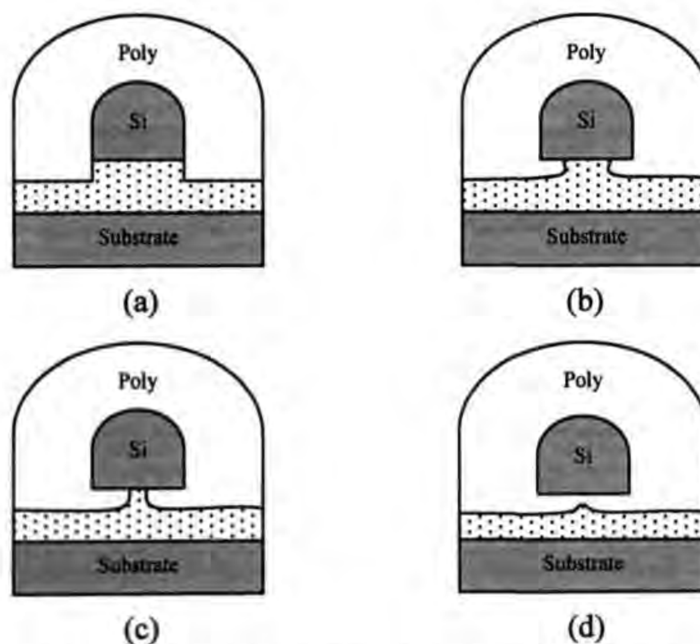

Figure 5.14: Cross sectional view of different gate configurations: a) no etch, b) 100 sec, c) 125 sec and d) 150 sec undercut beneath the silicon channel.

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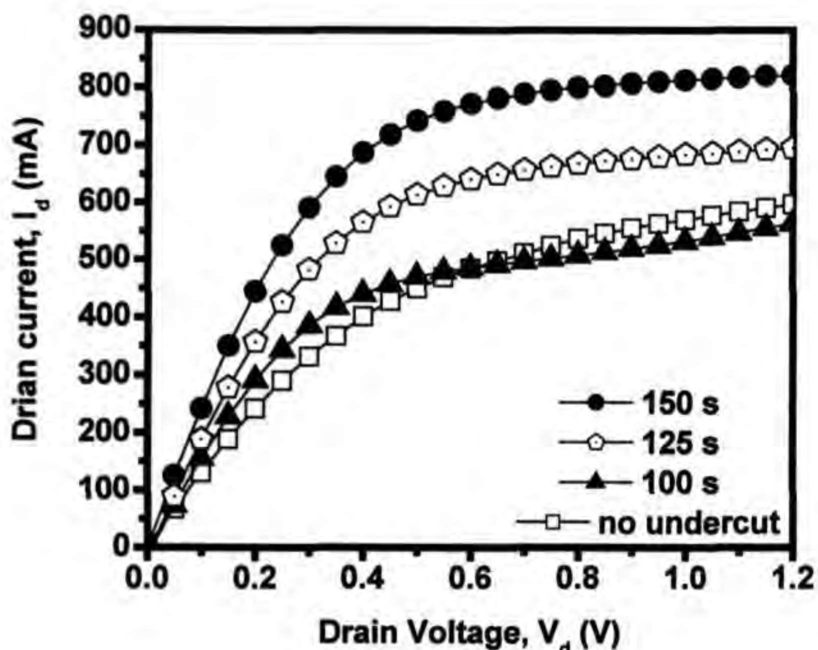
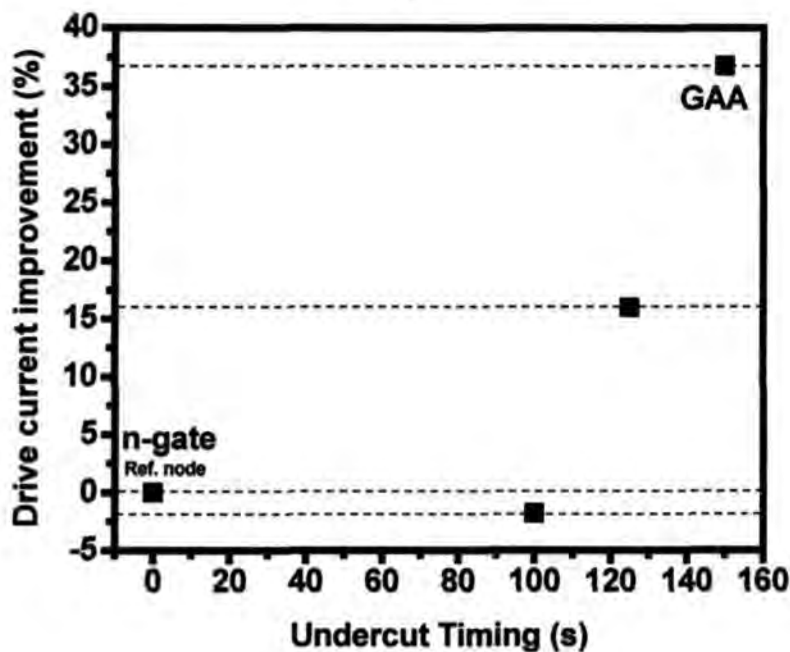


(a)



(b)

Figure 5.15: Drive current characteristics for different silicon channel undercut duration.

In Figure 5.15(a), a comparable drive current of approximately 600 μA/μm is obtained between the device structures: with an undercut timing of 100 seconds and without undercut beneath the silicon channel. It can be seen that the highest drive current of 820 μA/μm is achieved in the optimised GAA device structure with an

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undercut timing of 150 seconds. This timing actually corresponds to the time necessary to completely remove the buried oxide underneath the silicon channel so as to have the gate electrode wraps around the silicon channel. The overall current drive capability in percentage is plotted in Figure 5.15(b) for different NMOS devices against the undercut timings. For this case, n-gate with no undercut is taken as a reference node to compare the drive current performance as a function of different etch timings. Generally, the result indicates a rising trend, where the drive current performance increases with the amount of undercut beneath the silicon channel. GAA device displays an amazing improvement of 37% in the drive current over the n-gate device. This result clearly shows that there is a close relationship between the effect of gate electrode extension into the bottom silicon channel and its electrical behaviour. However, a linear relationship between the current drive and the etch timing cannot be established. This is because upon the buried oxide beneath the silicon channel being totally y removed (after 150 seconds), further undercutting will probably only yield similar drive current performance.

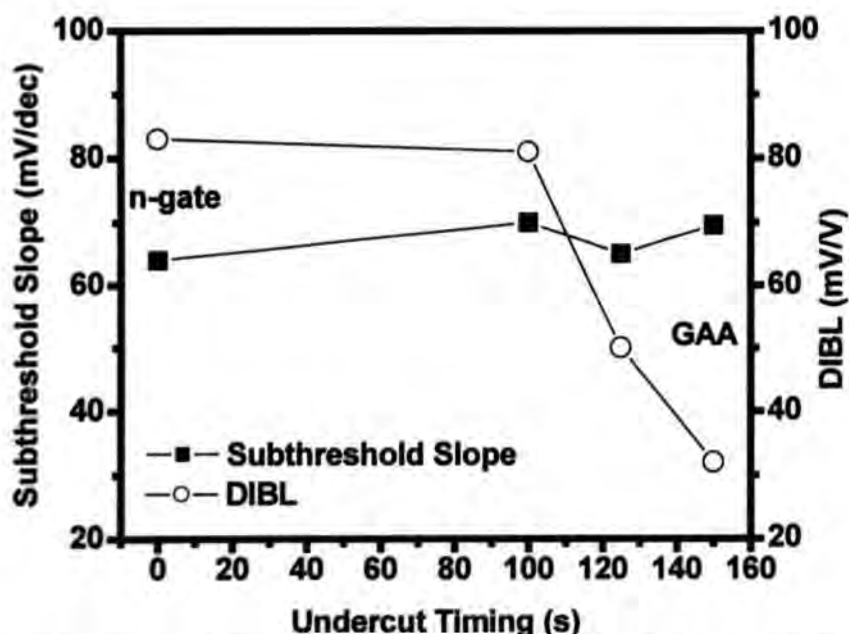

Figure 5.16: Subthreshold behaviour and DIBL characteristics for different undercut beneath the silicon channel.

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Figure 5.16 shows the subthreshold slope and the DIBL in device structure with differing gate electrode extensions beneath the silicon channel. It can be observed that the subthreshold slope is quite consistent and are all very close to ideal theoretical value of 60 mV/dec for all devices. Similarly, the DIBL for all device are well kept at below 100 mV/V. The DIBL is most effectively suppressed by the GAA gate structure.

In summary, the effect of gate electrode extension beneath the silicon channel has been studied. Results show that the transistor characteristics generally improved with larger gate extension beneath the silicon channel. For instance, the GAA NMOS device clearly exhibits higher drive current and excellent short channel effects over the n-gate device. These advantages include an increment of 36% in drive current, near ideal subthreshold slope of 69 mV/dec and a low DIBL of 32 mV/V. These findings are consistent with some of the recently published work [1][5][23], whereby GAA is found to be the most suitable device structure for effective drive current improvement and for suppressing short channel effects.

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CHAPTER 6: CONCLUSION AND SUGGESTION FOR FUTURE WORK

6.1 CONCLUSION

The project aims to make a significant contribution towards the search for advanced SOI MOSFETs for continuous scaling into the deep submicron regime, for down to 0.1-μm gate length. First, a general introduction concerning the trend of device miniaturization and VLSI technology towards the end of silicon roadmap is given. The advantages of the SOI technology have been identified and various applications have been presented in this thesis. The methods for producing SOI structures with emphasis on its suitability for CMOS applications have been described. At the present stage of technological maturity, the few techniques that are considered serious contenders for VLSI CMOS SOI application in the near future are the separation-by-implanted-oxygen (SIMOX) method and the wafer-bonding approach. In this project, the SOI wafers prepared via SIMOX approach have been ultilised. The electrical properties of the SOI MOSFETs have been outlined, especially in connection with the basic transistor design choice, i.e, thick or thin film, partially or fully depleted SOI film. The advantages and drawbacks of each approach as well as the SOI inherent floating body effect have all been discussed in section 2.2.3.

Considering the different kinds of three dimensional (3D) SOI MOSFET characteristics, the n-gate and Gate-All-Around (GAA) structure are proposed to enhance the performance of both the conventional triple-gate and the quadruple-gate designs. In brief, the n-gate NMOSFET is introduced to eliminate the early turn on effect due to the corners that are inherent to the transistors, which appear in the triple-gate structure (see section 3.2.1). On the other hand, the GAA structure is proposed to

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offer an optimum electrical performance for deep-submicron SOI transistors. The process optimisation for fabricating such multiple-gates SOI device structures has been clearly described. For the first time, the novel surface rounding technique and the replacement gate mask process are finely demonstrated to achieve rounded silicon channel and to create a cavity beneath the silicon channel respectively using the conventional bulk processing tools. The proposed narrow-width 0.12-μm n-gate and GAA NMOS transistors are successfully fabricated using a compatible 0.13-μm bulk fabrication process. Though many process issues such recipe mismatches and measurement errors are encountered during fabrication (due to the use of SOI substrate), the issues have all been resolved to attain the final desired structural profile.

The experimental results obtained from the fabricated multiple gates SOI MOSFET such as the n-gate and the GAA NMOS device have been presented. Comparisons of the experimental findings with different gate lengths, channel widths and even gate extension beneath the silicon channel have all been established. The proposed n-gate device demonstrates possible elimination of "early turn-on" effect and excellent short channel behaviour. It is interesting to note that the 20-μm channel-width n-gate transistor shows a kink effect during strong drain biasing. This phenomenon gives rise to the lowering of V_{th} and hence, the increased drive current. Base on the study carried out to investigate the effect of gate electrode extension beneath the silicon channel, the GAA device exhibits a most suitable transistor design to improve on the current drive and for effective suppression of the short channel effects. However, the choice of gate material for the GAA devices may have to be switched to metal gates for attaining suitable threshold voltage for optimum transistor performance.

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In summary, two new types of advance SOI structures have been demonstrated. They offer excellent electrical properties to sustain the pace-quickening trend in submicron silicon technology and beyond.

6.2 SUGGESTION FOR FUTURE WORK

Taking into account the results obtained so far, an outlook on the future development and perspective of the advanced SOI device are given as follows:

Although the 0.11-μm SOI transistors fabricated in this project show better switching characteristics, they tend to exhibit very high off-state leakage. In order to alleviate the high parasitic leakage problem, two suggestions are made. Upon the completion of the surface rounding process, the silicon surface shall undergo thermal oxidation to smoothen the surface roughness prior to gate dielectric growth. This is to allow better transconducance behavior and to minimise on the current leakage paths. Alternatively, a high-k gate oxide can be used to replace the conventional oxide, so as to provide low leakage current while maintaining good gate controllability over the silicon channel.

The featured n-gate and GAA NMOS devices require the replacement of poly gate with metal gate so as to obtain proper threshold voltages. In this case, midgap metal gates such as Molybdenum [1], Titanium nitride [2], Nickel Silicide [3], are desirable for attaining correct V_{th} for the GAA NMOSFET. Furthermore, metal gate also gives the advantages of lower gate sheet resistance, elimination of boron penetration and poly depletion in deep submicron MOSFET.

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A smaller physically gate length dimension as low as below 60 nm is preferred in advanced 0.13-μm SOI devices, to provide a significantly improved current drive for more complex future circuitries. In reality, this can be achieved by incorporating poly trimming process to further reduce the gate length through etching instead of using lithography where the exposure margin is very tight and the final profile may not be guaranteed.

As the devices continue to scale down aggressively, the formation in thin silicided source/drain region may be a prime concern since the silicidation process becomes very difficult to control precisely. It is worth suggesting that another way of fabricating thin SOI device without compromising the source/drain resistance by using different silicon film thicknesses for the channel and source/drain regions. This technique uses the raised-source/drain to improve the salicide formation which will also reduce the parasitic resistance problem at the same time [4][5]. This process shall be considered in the future fabrication to ensure proper silicidation while the channel thickness can scales down accordingly to the gate length to provide better electrical behaviour such as lower leakage current and enhanced gate controllability.

Lastly, the justification for investing in a new CMOS device technology such as the proposed advanced SOI must be found not only on its present attributes but also on its ability to favourably scale device features through future generations of lithograph and voltage.

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PATENT

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PROJECT CONTRIBUTION LIST

The names of the respective engineers that are involved in the project development are listed below.

	Description	
1	GAA Process Flow/ Runsheet	James Lee
2	Project Lot Start/ Execution	Dr. Lap Chan Tee Kheng Chok Timothy Phua
3	Active Definition	Li Fang
4	STI CMP	Wang Sim Kit
5	Poly Gate	Li Fang
5	Oxide Film Deposition	Zeng Meng
6	Reverse Gate Mask	Fadhillwati Alixes Fermo
7	Clean Technology	Lee Chin San
8	Cavity Etch	Jason Wong
9	BEOL Execution	Ho Mun Yee
10	Contact Etch	Zhu Yeqing
11	Metal Layers Alignment	Koo Chee Kiong Teddy Johan
12	Project Partner	Tee Kian Meng