Chip-Package Codesign of 5 GHz RF Receiver Front End

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2006

ACKNOWLEDGMENTS

I would like to express my gratitude to my supervisor, Professor Zhang Yue Ping, without whose motivation and encouragement I would not have considered a graduate career in RF research area, his expertise, understanding, and patience, added considerably to my graduate experience. I appreciate his vast knowledge and skill in many areas (e.g., antenna, packaging, EM modeling, RF circuit design, interaction with participants), and his assistance in writing reports (i.e., first year report, second year scholarship applications and this thesis), which have on occasion made me "GREEN" with envy. Again, a very special thanks goes out to Professor Zhang, he gave me the freedom to pursue this research, it was under his tutelage that I developed a focus and became interested in antenna area and chip-package codesign of RF receivers. He provided me with direction, technical support and became more of a mentor and friend, than a professor. It was through his persistence, understanding and kindness that I was encouraged to pursue my Ph.D degree. I doubt that I will ever be able to convey my appreciation fully, but I owe him my eternal gratitude.

My sincere thanks to Dr. Lu Chee Wai, Albert, my co-supervisor, who provided great help from technical and industrial support to life inspire. I would like to thank the other members of SIMTech, Mr. Chua Kai Meng and Miss Wai Lai Lai, they helped a lot in antenna fabrication in LTCC technology.

I must also acknowledge the other colleagues of our research group, Mr. Wang Wei, Mr. Li Qiang, Mr. Aaron Do, Mr. Xue Yang, Mr. Lin Wei and Miss. Sun Mei for the assistance they provided at all levels of my research project.

Thanks also goes out to those friends who provided me with good advice at times of critical need and for our exchanges of knowledge, skills, and venting of frustration during my graduate program, which helped to enrich the experience.

Finally, my great appreciate to my family for the support they provided me through my entire life and in particular, I must acknowledge my parents, without whose love and encouragement, I would not have finished this thesis.

SUMMARY

Nowadays, the demand for smaller and lighter portable electronics is driving both the semiconductor and packaging industries to increase integration density for radio frequency (RF) transceivers. Chip-package codesign opens a new era for integration, as the package is now part of the circuit. However, there are many problems to be solved for chip-package codesign.

In this project, a concept of integrated circuit package antenna (ICPA) has been further developed, which can be viewed as a kind of integrated antenna solution for single-chip RF transceivers. The major contributions are listed as follows.

Firstly, the development of a circuit model for the ICPA is of great importance. A circuit model for the ICPA in a CLGA package format has been proposed with an emphasis on verifying existing or deriving analytical formulas. The circuit model is validated with the high-frequency structural simulator (HFSS) simulations and measurements. Defining the resonant frequency as where the imaginary part of the input impedance is zero, the difference between our modeled and the simulated resonant frequencies is only 0.077 GHz (0.077/5.745 = 1.34%). The difference of the modeled and simulated resonant resistances is 0.8 Ω (0.8/25.7 = 3.1%).

Secondly, a novel feeding technique has been demonstrated for the ICPA. The effects of these feeding components on the performance of the ICPA have been investigated. It has been found that they mainly affect the impedance characteristics but not the radiation

properties of the ICPA. Utilizing the via shorting scheme of the ICPA, a band selection ICPA is designed and fabricated using the low temperature cofired ceramic (LTCC) technology. The frequency band selection capability greatly enhances the ICPA applications in wireless communications.

Thirdly, the interface between the antenna and the LNA has been explored. A 50-Ω input impedance single-ended LNA, which is designed in CSM 0.18 μm CMOS on-chip technology as a comparison reference, achieves a voltage gain of 20.7 dB and a noise figure of 2.3 dB at 5.8 GHz. While with the concept of antenna-chip codesign using a new interface between the LNA and the antenna, we can completely remove the usage of the large matching inductor and utilize the package components as well as the antenna's characteristics to further improve the performance of the LNA. The voltage gain is 28.7 dB and the noise figure is 1.6 dB with the optimized "codesign" implementation.

Fourthly, the improved theory of single-ended microstrip antennas based on the cavity model is expanded to analyze the input impedance and radiation characteristics of the differentially-driven microstrip antennas and ICPA. The differentially-driven microstrip antennas are fabricated using Taconic TLY-5. Theoretical and experimental results are found to be in acceptable agreement. It is found that the differentially-driven microstrip antennas have a lower cross-polar radiation component compared with the single-ended counterpart. In addition, we have developed a novel differentially-driven ICPA for single-chip RF transceivers. The differentially-driven ICPA fabricated in LTCC technology of Dupont 951-AX is experimentally verified. Results show that the differentially-driven ICPA of size 15 x 15 x 1.6 mm^3 achieves impedance bandwidth of 2.2%, radiation efficiency of 84%, and gain of 3.2 dBi at 5.8 GHz.

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LIST OF ACRONYMS

ADS-- Advanced Design System

ATM-- Asynchronous Transfer Mode

AUT-- Antenna Under Test

BPSK-- Binary Phase Shift Keying

BRAN-- Broadband Radio Access Network

CAD-- Computer Aided Design

CBGA-- Ceramic Ball Grid Array

CLGA-- Ceramic Land Grid Array

CMOS-- Complementary Metal Oxide Semiconductor

CW-- Continuous Wave

DSB-- Double SideBand

ETSI-- European Telecommunications Standards Institute

FCC-- Federal Communications Commission

FDTD-- Finite Difference Time Domain

FEM-- Finite Element Method

GDE-- Gate-Distributed Effect

GPS-- Global Positioning System

HFSS-- High Frequency Structural Simulator

HIPERLAN-- High Performance European Radio LAN

IC-- Integrated Circuit

ICPA-- Integrated Circuit Package Antenna

IF-- Intermediate Frequency

ISM-- Industrial, Scientific and Medical

LAN-- Local Area Network

LNA-- Low Noise Amplifier

LTCC-- Low Temperature Cofired Ceramic

MAC-- Medium Access Control

MAN-- Metropolitan Area Network

MCM-- Multi-Chip Module

MCM-D-- thin film MCM

MLO-- Multi-Layered Organic

MoM-- Method of Moments

MOSFET-- Metal Oxide Semiconductor Field Effect Transistor

NF-- Noise Figure

NQS-- Non Quasi-Static

OFDM-- Orthogonal Frequency Division Multiplexing

PA-- Power Amplifier

PCS-- Personal Communication System

QAM-- Quadrature Amplitude Modulation

QPSK-- Quadrature Phase Shift Keying

RF--Radio Frequency

SiP-- System-in-a-Package

SoC-- System-on-Chip

UNII-- Unlicensed National Information Infrastructure

VCO -- Voltage Controlled Oscillator

WAN-- Wide Area Network

CHAPTER ONE

INTRODUCTION

1.1 The trend towards higher frequencies of wireless communications

The wireless era was started by two European scientists, James Clerk Maxwell and Heinrich Rudolf Hertz [1]. In 1864, Maxwell presented Maxwell's equations by unifying the works of Lorentz, Faraday, Ampere, and Gauss. He predicted the propagation of electromagnetic waves in free space at the speed of light. He postulated that light was an electromagnetic phenomenon of a particular wavelength and predicted that radiation would occur at other wavelengths as well. His theory was not well accepted until 20 years later, after Hertz validated the electromagnetic wave propagation in 1887. Hertz demonstrated RF generation, propagation, and reception in the laboratory, for his work, Hertz is known as the father of radio, and frequency is described in units of hertz (Hz). Guglielmo Marconi successfully transmitted wireless signals across the Atlantic Ocean in 1900. The following decades, wireless communication systems have developed rapidly.

Wireless communications systems require high frequency signals for the efficient transmission of information [2]. Higher operating frequency has several advantages: larger instantaneous bandwidth for greater transfer of information; higher resolution for radar,

greater Doppler shift for continuous wave (CW) radar, and more detailed imaging and sensing; reduced dimensions for antennas and other components; less interference from nearby applications; fast speed for digital system signal processing and data transmission; less crowded spectrum; difficulty in jamming (military applications), etc. For example, an antenna radiates efficiently if its size is comparable to the signal wavelength, since the signal frequency is inversely related to its wavelength, antennas operating at radio frequencies and microwaves have higher radiation efficiencies. Further, their size is relatively small and hence convenient for mobile communications.

Wireless technology has been expanding very fast, with new applications reported every day. Besides the traditional applications in communication, such as radio and television, RF and microwave signals are being used in cordless phones, cellular communication, local area network (LAN), wide area network (WAN), metropolitan area network (MAN), and personal communication system (PCS). Among which, the wireless LANs (WLANs) have continual growth due to their benefits and applications.

1.2 Introduction to WLANs

The growth of WLANs commenced in the mid-1980s and was triggered by the US Federal Communications Commission (FCC) decision to authorize the public use of the Industrial, Scientific and Medical (ISM) bands [3]. The first attempt to define a standard was made in the late 1980s by IEEE Working Group 802.4, which was responsible for the development of the token-passing bus access method. The group decided that token passing was an inefficient method to control a wireless network and suggested the development of an

alternative standard. As a result, Working Group IEEE 802.11 was established to be responsible for the definition of physical and medium access control (MAC) sublayer standards for WLANs. The first 802.11 standard was finalized in 1997, it offered data rates up to 2 Mbps using spread spectrum modulation in the ISM bands. In September 1999, two supplements to the original standard were approved by the IEEE Standards Board. The first standard, 802.11b, extends the performance of the existing 2.4 GHz physical layer, with potential data rates up to 11 Mbps. The second, 802.11a, aims to provide a new, higher data rate (from 20 up to 54 Mbps) physical layer in the 5 GHz band.

In additional to IEEE 802.11, another WLAN standard, High Performance European Radio LAN (HIPERLAN), was developed by group RES10 of the European Telecommunications Standards Institute (ETSI), as a Pan-European standard for high speed WLANs. The HIPERLAN1 standard, like 802.11, covers the physical and MAC layers, offering data rates between 2 and 25 Mbps by using traditional radio modulation techniques in the 5.2 GHz band. Upon completion of the HIPERLAN1 standard, ETSI decided to merge the work on Radio Local Loop and Radio LANs through the formation of Broadband Radio Access Networks (BRAN). This project aims to specify standards for wireless asynchronous transfer mode (ATM) (HIPERLAN Types 2, 3, 4).

The growth in the area of WLANs can be partly attributed to the need to support mobile networked applications. Many jobs nowadays require people to physically move while using an appliance, such as a hand-held PC, which exchanges information with other user appliances or a central computer. Thus, WLANs are the technology of choice for such applications. Another benefit of using WLAN is the reduction in infrastructure and operating costs. A wireless LAN needs no cabling infrastructure, significantly lowering its

overall cost. Moreover, in situations where cabling installation is expensive or impossible (e.g. historic buildings, monuments or the battlefield) WLANs appear to be the only feasible means to implement networking. Therefore, the use of WLANs helps reduce the downtime of the network and eliminates the costs associated with cable replacement. The four major areas for WLAN applications are LAN extension, cross-building interconnection, nomadic access and ad hoc networking.

1.3 Specifications for 5 GHz WLAN

In this dissertation, we focus on the standards for wide-band WLANs in the 5-6 GHz band [4, 5]. IEEE 802.11a specifies operation in the 5-GHz unlicensed national information infrastructure (UNII) band recently allocated in the U.S. and employs orthogonal frequency division multiplexing (OFDM) in order to contend more effectively with the vagaries of indoor propagation. To complicate an already complex situation, a competing 5-GHz standard, HIPERLAN2, is nearing ratification, with many adherents in Europe. HIPERLAN2 specifies OFDM, bringing it much closer to 802.11a. OFDM is a multicarrier modulation technique that efficiently manages intersymbol interference and multipath distortions, making it very suited for indoor wireless communications. The standards foresee several data rates up to 54 Mbps, using different modulation schemes at different coding rates. The modulation schemes can be binary phase shift keying (BPSK), quadrature phase shift keying (QPSK) and quadrature amplitude modulation with 16 (16-QAM) and 64 points (64-QAM).

Although HIPERLAN2 and 802.11a do share some superficial similarities, there are important differences, particularly in the MAC protocol used to give multiple users access to a shared medium. HIPERLAN2 drives its MAC largely from ATM and possesses a mechanism for guaranteeing quality of service (QoS) by tagging packets with priority data. By contrast, 802.11's MAC uses a contention resolution mechanism that traces its heritage to that of 802.3 Ethernet.

The IEEE 802.11a standard defines three frequency bands that can be used. The first band extends from 5.15 to 5.25 GHz, the second from 5.25 to 5.35 GHz and the third from 5.725 to 5.825 GHz. These three equal domains are distinguished by allowable transmit powers. The bottom 100 MHz domain is restricted to a maximum power output of 50 mW, the next 100 MHz to 250 mW, and the top 100 MHz to a maximum of 1 W (this last domain is largely intended to support outdoor communications). HIPERLAN2 specifies two bands: from 5.15 to 5.35 GHz and from 5.470 to 5.725 GHz. That is why the researches are always focused on 5.2 GHz or 5.8 GHz for 5-GHz wireless LAN transceivers.

Strictly speaking, the required noise figure for HIPERLAN2 and 802.11a receivers is a function of data rate. 802.11a recommends a noise figure of 10 dB, with a 5 dB implementation margin to accommodate the worst-case situation. A 10-dB maximum noise figure is the design goal for the present work both for HIPERLAN2 and IEEE 802.11a. IEEE 802.11a specifies the receiver should be able to receive a signal between –85 dBm and –30 dBm at the antenna, whereas HIPERLAN1 specifies –25 dBm as the maximum input signal. Consequently, -25 dBm is the target maximum input level. Converting these specifications into a precise IIP3 target or 1-dB compression requirement is nontrivial. However, as a conservative rule of thumb, the 1-dB compression point of the receiver

should be about 4-dB above the maximum input signal power level that must be tolerated successfully. Based on this approximation, we target a worst-case input-referred 1-dB compression point of -21 dBm.

1.4 Chip-package codesign implementation for wireless communications

Designing analog front ends for these WLAN applications is quite challenging. Next to the high operating frequency, critical aspects are the wide bandwidth, large dynamic range, and a good linearity [6]. Fig. 1-1 shows the typical RF receiver front-end architectures for both single-ended and differential operations.

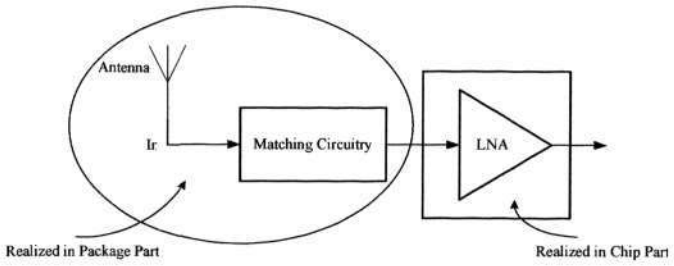


Fig. 1-1(a) Typical RF receiver front-end for single-ended architecture

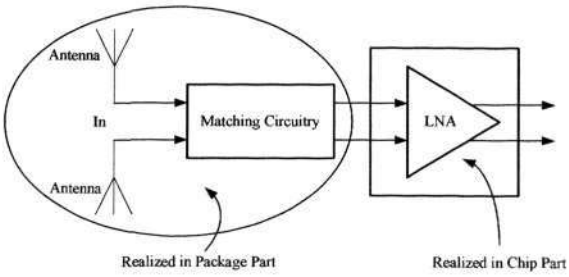


Fig. 1-1(b) Typical RF receiver front-end for differential architecture

Transceivers are now required to be wireless and to lower the cost, at the same time with an increase of the performance and a reduction of the power consumption. Higher integration density is in need for smaller and lighter portable RF transceivers. The ultimate goal would be a single-chip solution and the integration of different blocks of an RF transceiver into a single chip in deep submicron complementary metal oxide semiconductor (CMOS) technology has been continuously attempted [7-10]. T. H. Lee, et al introduced a low-power 5-GHz wireless LAN receiver consisting an image-reject low noise amplifier (LNA), an image-reject downconverter and a complete frequency synthesizer in [9], which achieved an overall noise figure of 5 dB, power consumption of approximately 37 mW and input referred third-order intercept of –2 dBm. Razavi developed a 5.2 GHz CMOS receiver which employed a double downconversion heterodyne architecture and realized in a 0.25-μm digital CMOS technology [10]. The circuit exhibited a noise figure of 6.4 dB and a voltage conversion gain of 43 dB, while draining 29 mW from a 2.5-V supply. But due to the substrate coupling between on-chip digital circuits and the RF blocks [11], and the frequency of self resonance of passive components [5], the single-chip systems still require many off-chip components, such as the antenna, the RF bandpass filters, the antenna switches and the power amplifier. That is, the largest problem of the single-chip solution is the integration of the passive components for high frequency. Therefore, several architectures that eliminate the need for bandpass filters at intermediate frequencies (IF) have been reported, such as the zero-IF and low-IF architectures [12-15]. Incorporating the zero-IF (direct-conversion) architecture, a 5-GHz band radio transceiver front-end chipset for wireless LAN applications was implemented in a 0.25-μm CMOS technology [14]. The receiver IC integrated an LNA, a set of I/Q down-

conversion mixers, an integrated quadrature voltage controlled oscillator (VCO) and a pair of local oscillator (LO) buffers. The transmitter IC was composed of a quadrature modulator, a driver amplifier and an on-chip quadrature VCO as well as buffers. The receiver achieved 3-dB double sideband (DSB) noise figure (NF), 18-dB voltage gain and -11-dBm input IP3 while dissipating 114 mW. The transmitter delivered -2.5-dBm power to a 50-Ω load at the 1-dB compression point and attained -33.4-dB sideband rejection, all at 5.7 GHz and 120-mW power consumption. But it still needs external RF band-select filters, a frequency synthesizer and a power amplifier (PA) to complete the radio front-end. Another fully integrated transceiver was built in 0.18-μm CMOS including the power amplifier, the phase-locked loop filter, and the antenna switch, as well as the complete baseband physical layer and the MAC sections [15]. The transceiver introduced in [15] had significantly high level of integration and achieved a good performance at lower power consumption, but the on-chip inductor is the critical problem, its quality factor is quite low compared to the discrete one and its area in RF integrated circuits is very large. Since the cost per square millimeter of deep submicron silicon processes is increasing rapidly with technology scaling and the size of inductors does not scale, the cost of these integrated on-chip inductors will become more and more important in fully integrated RF front-ends. What's more, the maximum allowable supply voltage decreases with CMOS technology scaling. As a result, analog front-end blocks realized in deep submicron digital CMOS technologies suffer from smaller dynamic ranges, which may not be allowable in future digital communication applications. Anyway, no absolutely true single-chip solution is available, a package is necessary in order to connect the antenna or external filters. The integration of the passive components in technologies other than IC-technologies, that are

still included in the same package, solves these problems. This leads to the concept of system-in-a-package (SiP) [16].

Several researches have been done about SiP [5-6, 16-19]. Most of these works are focused on multiple chips and use a thin film multichip module technology (MCM-D) to interconnect these different chips. The MCM technology is an interconnection technology on a common substrate with low losses and can be used to integrate a large number of required passive components with very good quality factors, it is clear that this technology opens a perspective for integration of a complete system into a single package. Therefore, a complete system integration of a transceiver, from the antenna until the digital baseband circuitry, which cannot be achieved with a single chip for high-performance applications, can now be realized. The advantages compared to a single-chip solution are obvious [6]: higher performance for RF solutions that benefit from high-Q inductors; a clever partitioning of the system into its subsystems, each realized in the most suitable technology, will lead to lower cost, increase of manufacturing yield and optimal performance; no coupling between different components through the common substrate; different supply voltage levels can easily be used; the MCM technology also opens a perspective for single-package mixed analog-digital integrated systems. It allows to have low-cost digital and high-performance analog in the same package, thereby retaining a high level of system integration as well as offering a good combination of cost, performance and functionality. For example, in [5], a 5-GHz WLAN receiver, which incorporated two 5-GHz bandpass filters, a LNA and a down-conversion mixer, was demonstrated. The SiP technology allows the integration of high quality passive components. With these passives, low-loss filters can be implemented. The use of passives,

filters and off-the-shelf, active, bare die components opens the way to successful system integration. The complete receiver in [5] had a measured conversion gain of 22 dB and noise figure of 7.5 dB. The 1-dB compression point was –3.6 dBm, referenced to the output. The whole structure measured 6.5 × 7 mm^2. The design of single-package integrated RF front ends requires a good knowledge of the features and limitations of different IC technologies and of interconnection technologies. It is essential to "co-design" the chips and package.

Chip-package codesign opens another dimension for integration, as the package is now part of the circuit [6, 20-25]. Chip-package codesign optimizes the integration of circuits and systems more effectively than traditional design methods and has more advantages to high-frequency circuit design, such as the elimination of the 50-Ω constraints if this leads to a higher performance or a lower power consumption for the active blocks [6, 20], the 50-Ω standard was optimized for minimum loss and maximum power in coaxial cable, not for IC design; a reduced number of design iterations because global optimization of both chip and package improves the design accuracy and the process variation of package-integrated passive elements is under better control than in active chips. For consumer electronics demanding quick time to market, this is a great advantage. For a 5 GHz WLAN front end, the LNA, mixer and VCO, "single-chip" version and chip-package codesign version were designed in [6]. And of course, there are varieties of challenges for chip-package codesign. For example, designers must combine chip and package designs into one circuit design platform [20]. Depending on computer aided design (CAD) tools and component models, codesign can extend from either the chip or the package designs. Assuming that it extends from chip design, using a CAD tool capable of both lump-

element and distributed models is not a problem. For a CAD tool that can only handle a lump-element model, designers need a conversion from a distributed-package model to a lump-element model. If it extends from package design, designers must use a CAD tool capable of simulating both active and passive circuits, and the active device models must be available; for certain structures without standard models available, designers will need to use electromagnetic simulators to generate models. Chip-package codesign involves several different tasks and mutual interactions among them. These different tasks need different types of knowledge. Managing these different tasks effectively is a challenge.

Although MCM technology allows chips manufactured by different technologies, such as silicon and Gallium Arsenide (GaAs), to be integrated in a common packge, designing an MCM for high frequency applications remains challenging due to cross-talk coupling and grounding. A greater challenge for MCMs lies in testing and production. This is usually referred to as the known-good-die issue which still bottlenecks MCM technology [20]. Single-chip package will give a better solution in this aspect. The packaged circuits can be tested as a single-chip package. It is more suitable for chip-package codesign with smaller package area. In our work, we propose such a solution with the integration of the antennas which will be demonstrated in details in the following chapters.

1.5 Achievements

For our research, there are four main achievements we have accomplished. First, a suitable circuit model of the integrated circuit package antenna has been developed for the feeding components of integrated circuit package antenna (ICPA) in a CLGA package format,

which is a critical step for chip-package codesign under current limited CAD tools. Second, a proper feeding technique suitable for ICPA has been investigated, which emphasizes particularly on impedance and radiation characterizations. Third, a new interface for LNA and the antenna has been explored so as to achieve a better performance for the chip-package. The single-ended LNA architecture is utilized for demonstration, which is consistent with the above two chapters using single-ended ICPA designs. Fourth, the improved theory on differentially-driven microstrip antennas and ICPA has been developed to suit the current and future development of RF transceivers. Meanwhile, differentially-driven microstrip antennas can well match to differential RF circuits without the needs of using bulky and lossy baluns. Due to time limitation, no differential circuitry has been designed and illustrated.

The study and the ultimate outcome of this project are worthwhile mentioning. The project bases on a novel package format for integrating the antenna into the package, and studies a particular feeding technique for the ICPA. A proper circuit model of the ICPA will give more convenience in the circuit simulation using current CAD tools. The reason is in that driving and robust CAD software allowing chip-package codesign is not available until now. Elimination of the 50-Ω constraint has been brought forward with the appearance of the concept of chip-package codesign, however, there has no final realization in current publications. We can investigate the optimized interface for LNA and antenna so as to optimize the whole performance of chip-package, such as the reduction of passive on chip or off chip inductors, which can economize the chip area. It is well known that a differential circuit is somewhat immune to electro-magnetic interference (EMI) and cross coupling than that of the single-ended counterpart, differentially-driven microstrip

antennas have found wide applications. Informative improved theory has been achieved to analyze the differential operation of microstrip antennas and ICPA.

1.6 Organization of this dissertation

This chapter has presented the background and main achievements of the project. The following chapters will be organized as below.

The concept and configuration of ICPA will be presented in chapter two. The circuit model of the ICPA in CLGA package format will be described in chapter three, and theoretical, High Frequency Structural Simulator (HFSS) simulated and measured results will be presented. The novel feeding technique for ICPA will be illustrated in chapter four. A brief introduction of Finite Difference Time Domain (FDTD) method will also be summarized. It will mainly demonstrate and explain the effects of the feeding network on ICPA performance. A band selection ICPA will also be shown utilizing the via shorting scheme of the ICPA. Chapter five will touch on the architecture of a single-ended LNA in different implementation techniques. A new interface between the RF receiver front-end and the antenna will be studied, which utilized the advantages of antenna-chip codesign. Improved cavity model theory on differentially-driven microstrip antennas and ICPA will be detailed in chapter six. Finally, chapter seven will give conclusions of the whole work and some recommendations.

CHAPTER TWO

CONCEPT OF ICPA AND METHODOLOGIES

2.1 Motivation for Integrated Circuit Package Antenna (ICPA)

We have discussed in chapter one that most works about chip-package codesign use MCM technology. Both the advantages and disadvantages are listed. Although they said that MCM technology could integrate the full system, few of them have integrated antenna into their RF transceivers. Researches only cited a work in [26] to demonstrate the possibility of integrating the antenna in MCM technology.

Antennas and RF front-ends are key components that often control the overall performance of wireless communication systems [27]. Many antenna researchers nowadays are devoted to the development of compact antennas that can be integrated well in portable devices while keeping a good antenna performance in spite of their small physical size. At microwave frequencies, material properties and manufacturing tolerances are becoming more important and cost-effective design becomes more challenging. The first planar antenna dates from 1950s, but only from the 1970s was it really used for the integration of circuits and antennas [27]. Planar antennas are the favorite antenna type for integrated antennas because of their clear advantages in terms of weight, manufacturability, compatibility with microwave circuits and cost.

It should be noted that several researches have integrated the antenna directly on the package [17, 27-29]. In [17], the cavity-backed patch antenna has been developed in the low temperature co-fired ceramic package and fabricated directly on the top of the module. A band-pass filter was embedded inside the package. The RF transceiver was consisted of a power amplifier (PA), an LNA, mixers and a VCO. Antenna, filter and RF transceiver were connected using via structures. The antenna had advantages over the conventional patch in terms of larger bandwidth, smaller size and less interference with other components. However, we should be reminded that they still utilized the multi-chip solution [27] or the RF transceivers were for mm-wave frequency band [29]. Several configurations using different layers of the multi-layered organic (MLO) package were studied [28], the MLO package consisted of three metal layers of copper separated by two dielectric layers. The most desirable configuration was the antenna and its feed line on the top metal layer with the second metal layer removed and the bottom layer serving as ground. To reduce the coupling of noise to the antenna part, a grounded tuning strip was placed next to the radiating edge of the antenna. But in MLO package technology, the material has poor loss tangent value (0.02-0.05). The challenge here is that the substrate thickness of each layer of the MLO package is electrically extremely small at high frequency.

To parallel with the single-chip solution trend, Chan, et al implemented integrated antennas in silicon semiconductor technology on both conventional low-resistivity and proton-implanted high-resistivity silicon substrates [30]. As expected, the integrated antennas on the low-resistivity silicon have a rather poor radiation efficiency because of the high loss of the silicon substrate, while the integrated antennas on the high-resistivity

silicon have acceptable radiation properties. A planar inverted-F antenna of size 3.5 x 9.4 mm^2 integrated on the high-resistivity silicon substrate exhibited a sharp resonance, a lower return loss, and a symmetrical radiation pattern at 5.7 GHz. The integration of antennas on the high-resistivity silicon substrate has deviated from the mainframe silicon process, which undoubtedly will increase the fabrication cost and degrade the gate oxide integrity. Furthermore, these integrated antennas are too large to be feasible from the economical viewpoint of very large-scale integrated circuits.

To overcome the problems associated with the integrated antennas and to provide a low-cost antenna solution, miniature surface-mountable chip-scale antennas have received attention recently [31-36]. Great efforts have been made involving the development of new dielectric materials [31, 32], the application of novel fabrication technologies [33, 34], and the optimization of various radiator structures [35, 36]. Tanikodoro, et al demonstrated a chip antenna in the thick film process. This chip antenna of volume 17.5 x 17.5 x 8.3 mm^3 grounded on a big copper plate was measured. The results showed that the chip antenna resonated at 1.765 GHz and had impedance bandwidth of 1.02% and gain of 4.79 dBi [32]. Using the optimized mounting condition of the chip multilayer antenna to take the distribution of the current on the ground plane into account, Dakeya et al investigated antenna of size 9 x 9 x 2 mm^3 working for 2.4 GHz applications in LTCC technology, with bandwidth of more than 100 MHz [33]. In [35], a ceramic chip antenna using meander conductor lines of size 11.5 x 4 x 1 mm^3 has been proposed with measured impedance bandwidth of 9.8% at 190 MHz and gain of 1.5 dBi. These chip antennas are physically small, however, they are still discrete.

Hence, antennas on multilayer substrates have been proposed in which RFICs can be embedded [37, 38]. In [38], a circularly polarized antenna was designed for global positioning system (GPS) applications. The LTCC multilayer technology has been applied to realize the soft-and-hard surface (SHS) structure by surrounding the patch antenna with a number of rings of metal vias. They left a cavity beneath the patch antenna for burying the GPS RF front-end IC chipset. It's been found that a 14-dB improvement of the front-to-back (F/B) ratio can be achieved for an SHS width of less than half of the patch length.

Ball grid array (BGA) packaging technology is one of the advanced technologies emerging in response to the challenge for higher integration. As a single-chip package format, BGA package is like chip-scale package with a much smaller package area, which can overcome the known-good-die problem and the packaged circuits can be treated as a single-chip package [18]. To better suit the innovative development of single-chip solutions of RF transceivers and the trend of chip-package codesign, Zhang has recently proposed to integrate antennas on chip packages. Microstrip antennas have been integrated on both cavity-up and cavity-down ceramic chip packages for applications at 2 to 5 GHz [22-24, 39]. Ceramic BGA (CBGA) packages have been widely used to carry highly integrated RF transceivers because of their excellent performance [40, 41]. A compact integrated circuit package antenna (ICPA) has been demonstrated in a CBGA package format in Zhang's works. The antennas realized in this manner enjoy economical advantage of mass production and automatic assembly and have potential benefit to the system-level board miniaturization and the system-level manufacturing facilitation. This is because they offer the possibility to combine antennas and single-chip RF transceivers into standard surface mounted devices.

2.2 Configuration of the ICPA

Fig. 2-1 shows the configuration of the ICPA in a thin CBGA package format. The ICPA consists of three cofired laminated ceramic layers, with a bare chip cavity formed at the middle layer. There are two buried layers and one top-layer metallization in the construction. The lower buried layer provides the metallization for the signal traces, while the upper buried layer provides the metallization for the ground plane of the ICPA. The radiating element of the ICPA, which can take any form of a printed circuit antenna, is realized with top-layer metallization. It should be noted that only two of the three laminated layers are used as the effective substrate for the ICPA, which is different from the design of conventional multilayer antennas where all layers are used as the substrates of the antennas [37, 38]. There are 48 signal traces in the ICPA. These 48 signal traces follow the current designs of single-chip RF transceivers where 48 input/output pads are often adopted [42, 43]. The outer ends of 48 signal traces are connected to 48 solder balls through 48 vias, while the inner ends of 48 signal traces are connected to the single-chip RF transceiver through 48 bond wires. The single-chip RF transceiver is attached upside down to the ground plane of the ICPA in the chip cavity. The ground plane of the ICPA shields the single-chip RF transceiver from the radiating-element of the ICPA. The feed of the radiating element of the ICPA from the carried single-chip RF transceiver is realized with a bond wire, a signal trace, and a via through an aperture on the ground plane of the ICPA. This feeding technique is compatible with the integrated circuit package technology and can be easily implemented.

In the next chapters, studies will be carried on surrounding the ICPA, either in CLGA or in CBGA package format.

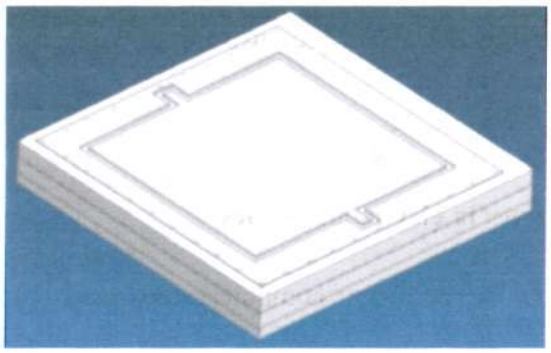


Fig. 2-1(a) Top view of the ICPA

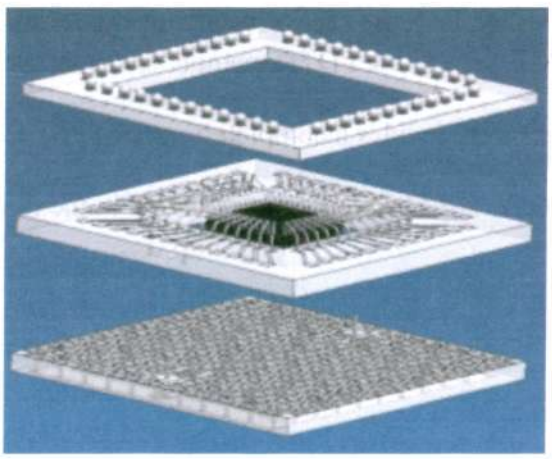


Fig. 2-1(b) Three laminated layers of the ICPA

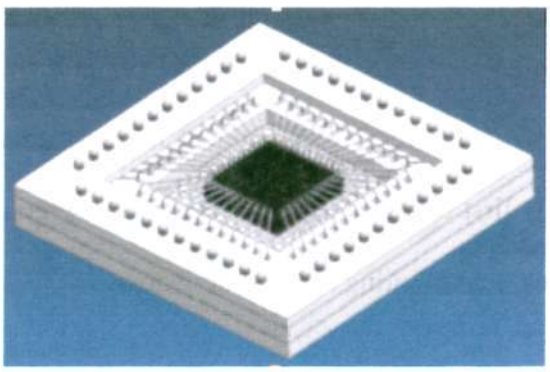


Fig. 2-1(c) Bottom view of the ICPA

2.3 Methodologies in the thesis

In this Section, the theories and techniques used in the subsequent chapters are briefly described.

2.3.1 Numerical techniques in electromagnetics

At high frequency operation, the use of computers facilitates the utilization of numerical techniques such as the FDTD method, finite-element method (FEM), and method of moments (MoM) to evaluate the field distribution in practical, yet complicated, geometries. Originally introduced by Yee [44], the FDTD method has been applied to a wide variety of problems. The FDTD method provides a completely general formulation which consists of a discretization and a solution of Maxwell's curl equation in the time domain [45].

$$\nabla \times E = -\mu \frac{\partial H}{\partial t} \tag{2-1}$$

$$\nabla \times H = \varepsilon \frac{\partial E}{\partial t} \tag{2-2}$$

In Cartesian coordinate system (x, y, z), equations (2-1) and (2-1) can divide E and H into six scalar equations [46]. In the space and time, E and H are computed half a time increment and space increment at a time. Every E component is surrounded by four circulating H components, and every H component is surrounded by four circulating E components. Yee was the first to introduce the scheme of discretization, which consists of using a Taylor development and writing the first derivative as [45],

$$\frac{\partial f}{\partial x}(x_0)=\frac{f\left(x_0+\frac{\Delta}{2}\right)-f\left(x_0-\frac{\Delta}{2}\right)}{\Delta}+\theta\left(\Delta^2\right) \tag{2-3}$$

where x_0 is the derivative calculation point and Δ is the space increment. Space and time derivatives are then second-order accurate in Δ and a central differencing scheme reduces the round-off error.

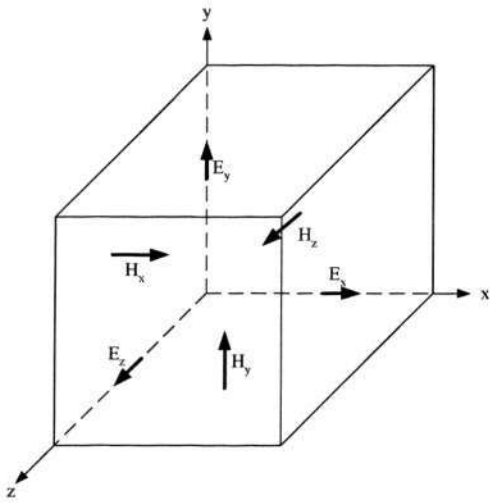


Fig. 2-2 Six components of the electromagnetic field

Δx, Δy and Δz are the space increment of x, y, z direction respectively. Δt is the time increment. The increment Δ should at least satisfy $\Delta \le \frac{\lambda_{min}}{10}$, where $\frac{\lambda_{min}}{10}$ is the minimum wavelength of electromagnetic wave [46]. To avert the numerical divergence in calculations, Δ t needs to satisfy stability conditions. The rule used for time step calculation is called "Courant stability criterion" [47] and for three dimension space it is expressed as [46],

$$\Delta t \le \frac{1}{V_{max}\sqrt{\left(\frac{1}{\Delta x}\right)^2+\left(\frac{1}{\Delta y}\right)^2+\left(\frac{1}{\Delta z}\right)^2}} \tag{2-4}$$

where V_{max} is the maximum electromagnetic wave phase velocity within the media.

The FDTD method basically divides the solution domain into some finite number of discrete points, and replaces the partial differential equations with a set of difference equations. The mesh size of the discretized solution domain is a measure of the solution accuracy. The FDTD method is suitable for structural analysis, but it always requires a partial differential equation and a series of boundary conditions as a starting point [48]. It is sometimes very difficult to bring forward a partial differential equation for a complex structural problem.

The FEM is an optimization method that basically minimizes the total energy stored in the system subject to some constraints dictated by the boundary conditions. The most important advantage of the FEM is that it almost has no difficulties to model configurations which may have complicated geometries and many arbitrarily shaped dielectric regions [48].

In problems with open boundaries, the MoM appears to the best choice to determine the electric and magnetic fields, which basically employs the equations of unknown fields in integral form to determine the field distribution in a given medium. So we do not really need to solve the solution with finite boundaries. This technique requires the knowledge of the charge or current distribution on the existing boundaries of the problem, which usually is not available. However, when the potential is given on the boundary, we can predict the distribution of the charge or the current on the boundary numerically by dividing the boundary into a number of elements, sometimes referred to as boundary elements. Then we can determine the field distribution everywhere in the system [48]. However, MoM techniques applied to integral equations are not very effective to arbitrary configurations

with complex geometries or inhomogeneous dielectrics. They also are not well-suited for analyzing the interior of conductive enclosures or thin plates with wire attachments on both sides.

All the numerical techniques have their advantages and disadvantages, respectively. We can apply these techniques for their suitable applications. In our work, we have utilized all the above-mentioned techniques to facilitate our study.

2.3.2 Antenna radiation pattern basics

The radiation pattern gives the angular variation of radiation (far field) at a fixed distance from an antenna when the antenna is transmitting [49, 50]. When calculations of electromagnetic fields radiated from antenna are required, the distant point at which the field is to be calculated is expressed in terms of spherical coordinates (r, θ, φ). This common hybrid arrangement is illustrated in Fig. 2-3 [50].

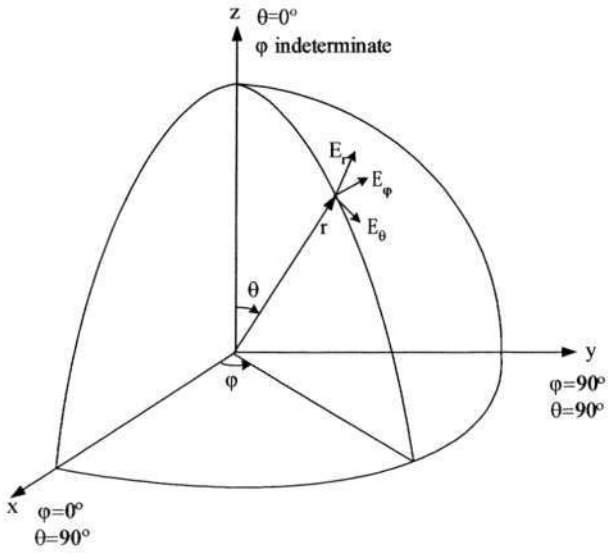


Fig. 2-3 Spherical coordinate system used with antennas

It is rarely feasible to measure or calculate the absolute amplitude, phase and polarization of the radiated fields over the surface of a sphere at every frequency of operation. So in practice, relative amplitude and phase is sampled at a number of points and the absolute amplitude level is calibrated by a measurement of power gain in the direction of the peak radiated field [50].

For example, with the frequency of operation and polarization fixed, a value of angle φ could be chosen, at the same time the relative field is measured for increments of angle θ. The angle φ is then incremented, and the above-mentioned process repeated. The calibration of this relative distribution would then be performed by a single measurement of power gain typically in the $\theta = \varphi = 0$ direction. Each two dimensional radiation pattern taken at an increment of φ is called a "pattern cut", referred to the test antenna. If the radiation pattern is taken along the $\varphi = 0$ or $\varphi = 90$ planes it is described as a "principle-plane cut" [50]. The fields radiated from an ideal dipole are shown in Fig. 2-4 for better understanding [49]. The E-plane contains the electric field vector and the direction of maximum radiation, while H-plane is the plane contains the magnetic field vector and the direction of the maximum radiation. Obviously, E-plane and H-plane are perpendicular to each other.

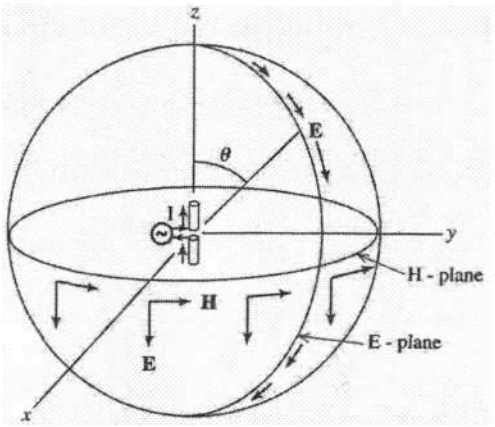


Fig. 2-4 Radiation field components from an ideal dipole

2.3.3 Far-field radiation pattern measurement

The radiated electric field (the magnetic field behavior follows directly) is both a vector and a phasor. In general, it has two orthogonal components, E_θ and E_φ, as shown in Fig. 2-3. In practice, measurement of the radiation pattern is conceptualized by rotating the test antenna or antenna under test (AUT) to vary the observation angle and maintaining a constant large distance to the source reference antenna. The AUT orientation is maintained parallel to E_θ or E_φ. Usually the AUT is used as a receiving antenna. The fields from the motionless source antenna provide a constant illumination of the AUT whose output varies with its angular position [49].

A facility used to measure antenna radiation characteristics is referred to as an antenna range. In our measurement, we use anechoic chamber, which is a room lined with absorber material to suppress reflections. Frequently the absorber is pyramidal-shaped to eliminate flat surfaces that reflect rays toward the test antenna. The entire measurement facility consists of the space (indoor) for the source and test antennas, antenna positioners, a

transmitter, a receiving system, and data display/recording equipment. The AUT is located in the far field of the source antenna. The source antenna and the AUT are approximately the same height. More details please refer to [49, 51].

We have no available facilities to measure the gain and efficiency of the antenna, therefore, we do not mention the measurement setting up here.

CHAPTER THREE

CIRCUIT MODEL OF ICPA ON CLGA PACKAGE

3.1 Urgent call for circuit model for ICPA in antenna-chip codesign

The ICPA offers the possibility of the antenna-chip codesign of an RF transceiver without the constraint of 50-Ω common impedance interface between the antenna and the chip. As we have mentioned, the 50-Ω standard was optimized for interconnect with a coaxial cable. Whereas in chips and packages, signal traces, vias, and bond wires are utilized for interconnection. In addition, MOS transistors are capacitive devices and inductors are employed to match MOS transistors to 50-Ω for acceptable RF performance. Inductors consume a larger die area and have a poor quality factor. The moving of the large on-chip inductor to the package is rather desirable. In the antenna-chip codesign, at least two on-chip inductors for matching the LNA to the 50-Ω antenna can be eliminated. We can determine the feed location of the antenna to be inductive (rather than 50-Ω) so as to resonate with the capacitive impedance of the MOS transistors in the LNA of the receiver [52]. The antenna-chip codesign has to be made in a circuit simulator, say, Cadence RF

Spectra. All circuit simulators rely on circuit models. Thus, the development of a circuit model for the ICPA is of great importance.

Under the circumstance of chip-package codesign, if available, standard element models will be used, if not, electromagnetic simulation will be performed, the electromagnetic analysis of nonstandard passive elements presents the most challenging task to designers, since the electromagnetic simulation is quite time consuming. They should be able to simulate the whole circuit, from antenna to chip and package, and predict the performance. Therefore, a circuit model for our ICPA is in urgent need.

The circuit model that consists of *RLC* lumped elements of both microstrip patch antenna and feeding interconnect components has been developed in this chapter with an emphasis on verifying existing or deriving analytical formulas. The *RLC* values of the microstrip patch antenna are calculated with our improvements to existing computer-aided design formulas, while the *RLC* values of the feeding interconnect components are calculated with more efforts. In particular the *C* values related to the vias and signal traces require to be calculated numerically and they are calculated here with the MoM and the conformal mapping method, respectively.

3.2 ICPA in CLGA package and its circuit model

CLGA packages reduce the integrated circuit mounted height by eliminating the solder balls that are used for mounting CBGA packages to printed circuit boards. CLGA packages are designed for enhanced thermal operation, improved RF performance and resistance to mechanical stress failures.

Any printed circuit antenna can be used for the ICPA. A microstrip patch antenna is chosen in our modeling study because the rich knowledge on the antenna is available and the microstrip patch enhances the ICPA thermal performance. For the microstrip patch antenna, it is usually modeled as a simple parallel resonant *RLC* circuit. A lot of work have been done to calculate the *RLC* values in the circuit model [53-57]. In [53-55], they presented a simple model for the input impedance of a rectangular microstrip patch antenna based on the classical cavity model, which is well suited to the computed aided design. They used the cavity model to determine the frequency and the input resistance at resonance. They took into account the influence of the fringing field at the edges of the patch antenna by exploring the dynamic permittivity. The circuit model they adopted was resonant parallel *RLC* circuit. They have achieved a fast computation time. However, the results were still not so comprehensive because they neglected some important effects in their analysis. Martin [56] further improved the previous work by adding the frequency dispersion effects to the effective dielectric constant. But it still not completed. Therefore, their models were not so accurate especially in the calculation of the resonant resistance. Among these studies, [53] is a representative work, which is utilized as the reference for comparison with our work in the following sections. In our investigation, more accurate improvements to the existing calculations have been made.

3.2.1 ICPA in CLGA package

The architecture of the ICPA in CLGA package format is almost the same as described in Chapter Two except the balls are substituted by lands. It is seen from Fig. 3-1 that the

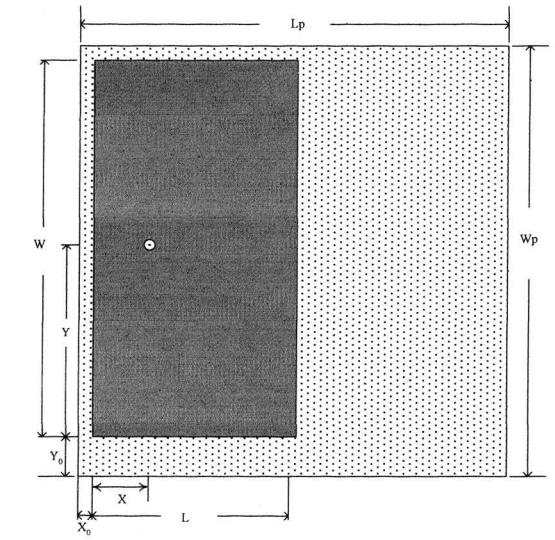
microstrip patch antenna of the ICPA is fed by packaging interconnect components such as bond wires, signal traces, and vias in a G-S-G configuration from the carried chip. The proposed equivalent circuit model of the ICPA feeding network is shown in Fig. 3-2. As shown in Fig. 3-2, the microstrip patch antenna, the feeding via under the ground plane, the G-S-G signal traces, the G-S-G bond wires, the vias to lands and the lands are represented with the corresponding equivalent *RLC* subcircuits.

3.2.2 Circuit model of microstrip patch antenna

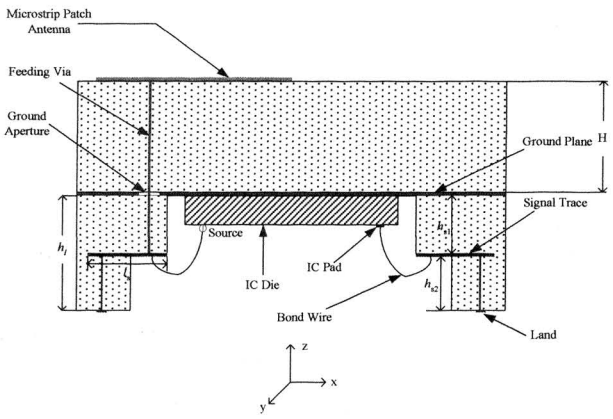
The *RLC* values in the circuit model of the microstrip patch antenna are calculated below. The feeding via above the ground plane is represented by an inductive reactance term [53]

$$XL = \frac{377 f_r H}{c_0} \ln\left(\frac{c_0}{\pi f_r d_v \sqrt{\varepsilon_r}}\right) \tag{3-1}$$

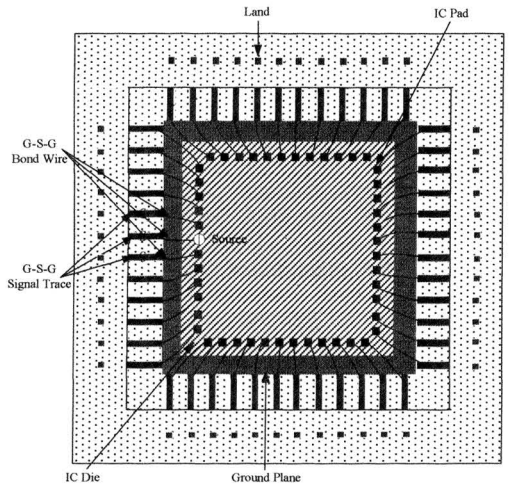
where c_0 is the velocity of light, d_v is the diameter of the feeding via, H is the thickness of the substrate between the microstrip patch and ground plane, ε_r is the relative permittivity of the substrate, and f_r is the resonant frequency of the ICPA. The L_{XL} in Fig. 3-2 is the equivalent inductance of the reactance XL for the feeding via between the antenna and ground plane.



(a)



(b)



(c)

Fig. 3-1 ICPA in CLGA package format
(a) top view; (b) cross section; (c) bottom view

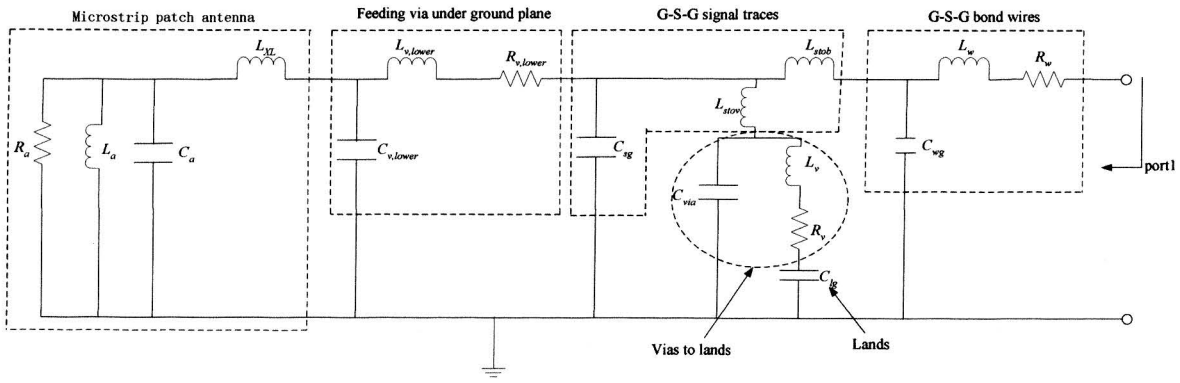


Fig. 3-2 Equivalent circuit for the ICPA feeding network

The resonant resistance R_a of the parallel RLC circuit is given by

$$R_a = \frac{Q_{total} H}{\pi f_r \varepsilon_{dyn} \varepsilon_0 W L_{eff}} \cos^2\left(\frac{\pi X_{eff}}{L_{eff}}\right) \tag{3-2}$$

where we propose an effective length L_{eff} of the antenna to take into account the influence of the fringing field at the corners and the dielectric inhomogeneity of the ICPA. Accordingly, the distance from the feeding point to the patch edge X is replaced by

$$X_{eff} = X + (L_{eff} - L)/2 \tag{3-3}$$

In equation (3-2), ε_{dyn} is the dynamic permittivity, which is a function of the dimensions of the ICPA and the relative permittivity ε_r as well as the different modes field distribution [53].

$$\varepsilon_{dyn} = C_{dyn}(\varepsilon)/C_{dyn}(\varepsilon_0) \tag{3-4}$$

where $C_{dyn}(\varepsilon)$ represents the total dynamic capacitance of the patch in the presence of a dielectric of relative permittivity $\varepsilon_r = \varepsilon/\varepsilon_0$ and $C_{dyn}(\varepsilon_0)$ represents the total dynamic capacitance of the patch in the presence of air. $C_{dyn}(\varepsilon)$ can be written as

$$C_{dyn}(\varepsilon) = C_{0,dyn}(\varepsilon) + 2C_{e1,dyn}(\varepsilon) + 2C_{e2,dyn}(\varepsilon) \tag{3-5}$$

where $C_{0,dyn}(\varepsilon)$ is the dynamic main field of the patch capacitance without considering the fringing field. It is calculated by

$$C_{0,dyn}(\varepsilon) = C_{dyn}(\varepsilon)\frac{\varepsilon_0\varepsilon_r WL}{H\gamma_n\gamma_m} = \frac{C_{0,stat}(\varepsilon)}{\gamma_n\gamma_m} \tag{3-6}$$

where $C_{0,stat}(\varepsilon)$ represents the static main capacitance of the patch without considering the fringing field and γ_n and γ_m are in the form

$$\gamma_i = \begin{cases} 1 & \text{for } i = 0 \\ 2 & \text{for } i \neq 0 \end{cases} \tag{3-7}$$

Then, a dynamic edge capacitance for each side of the patch taking into account the influence of the fringing field is calculated. Assuming that the edge field of the resonator has an X- and Y-dependent field distribution, the dynamic fringing capacitances are then given in the general form by

$$C_{e1,dyn}(\varepsilon) = \frac{1}{L}\int_0^L C_{e1,stat}(\varepsilon)\cos^2\left(\frac{n\pi x}{L}\right)dx = \frac{C_{e1,stat}(\varepsilon)}{\gamma_n} \tag{3-8}$$

and

$$C_{e2,dyn}(\varepsilon) = \frac{1}{W}\int_0^W C_{e2,stat}(\varepsilon)\cos^2\left(\frac{m\pi y}{W}\right)dy = \frac{C_{e2,stat}(\varepsilon)}{\gamma_m} \tag{3-9}$$

where $C_{e1,stat}(\varepsilon)$ represents the edge capacitance on one side of a patch length L and $C_{e2,stat}(\varepsilon)$ represents the edge capacitance on one side of a patch width W.

$C_{e1,stat}(\varepsilon)$ is given by

$$C_{e1,stat}(\varepsilon) = \frac{1}{2}\left[C_t(W,H,\varepsilon_r) - \frac{\varepsilon_o\varepsilon_r W}{H}\right]L \tag{3-10}$$

where $C_t\left(W,H,\varepsilon_r\right)$ is the total capacitance of the microstrip patch of width W, which is traditionally calculated from some approximation equations just as in [57]. In order to get a more accurate value of $C_t\left(W,H,\varepsilon_r\right)$, it is calculated as follows [58].

Fig. 3-3 shows the original structure for the microstrip patch and the conformal mapping structures in different planes.

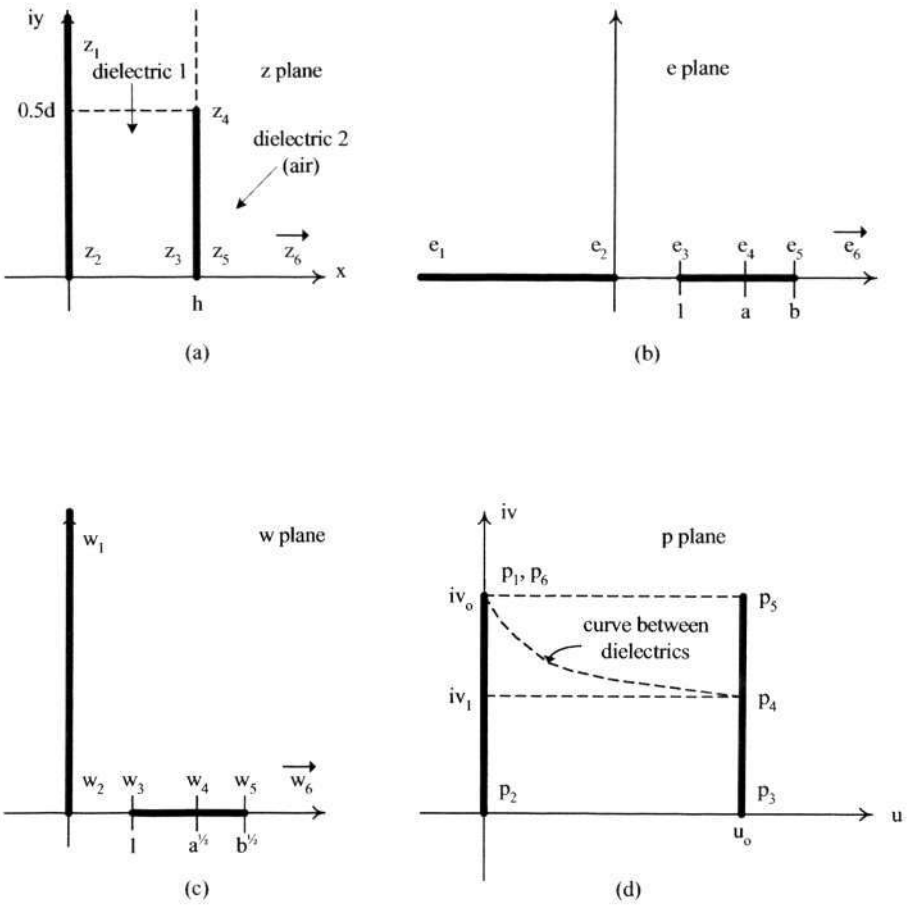


Fig. 3-3(a) z-plane geometry; (b) e-plane geometry; (c) w-plane geometry; (d) p-plane geometry

Firstly, the modulus of the integrals m is calculated as below.

$$\frac{W}{2H}=\frac{2}{\pi}K'(m)Z_n\left(\phi_1/\alpha_1\right) \tag{3-11}$$

where

$$Z_n(\phi_1/\alpha_1) = E(\phi_1/\alpha_1) - E(\alpha_1)F(\phi_1/\alpha_1)/K(\alpha_1) \tag{3-12}$$

$$\phi_1 = \sin^{-1}\sqrt{\frac{b-a}{b-1}} \tag{3-13}$$

$$\alpha_1 = \cos^{-1}\left(1/\sqrt{b}\right) \tag{3-14}$$

$$a = b\frac{E'(m)}{K'(m)} \tag{3-15}$$

$$m = 1/b \tag{3-16}$$

$$K'(m) = K(1-m) \tag{3-17}$$

$$E'(m) = E(1-m) \tag{3-18}$$

where $K(m)$ is the complete elliptic integral of the first kind; $E(m)$ is the complete elliptic integral of the second kind; $F(\phi_1/\alpha_1)$ is the incomplete elliptic integral of the first kind and $E(\phi_1/\alpha_1)$ is the incomplete elliptic integral of the second kind.

Secondly, the equation of the curve *v(u)*, which separates the two dielectrics, is given by the following equations.

$$\mathrm{sn}(v/m_1) \equiv g(u/m_1) = \left\{ \frac{m\,\mathrm{sn}(u/m)\,\mathrm{cn}(u/m)\,\mathrm{dn}(u/m)}{\frac{\pi}{2K'(m)} - \frac{\pi u}{2K(m)K'(m)} - Z_n(u/m)} + \mathrm{dn}^2(u/m) \right\}^{-1/2} \tag{3-19}$$

where $m_1 = 1-m$

$$v(u) = \mathrm{sn}^{-1}(v/m_1) = F(\phi_3/m_1) \tag{3-20}$$

here $\phi_3 = \sin^{-1}\left[g(u/m_1)\right]$

A number of values of u between 0 and $K(m)$ is selected, and the respective values of v can be calculated.

Thirdly, by using the Finite Difference method to solve for the Laplace equation and apply the following boundary conditions for dielectric 1 (the substrate between radiating element and ground plane) and dielectric 2 (air), the voltages at all nodes can be determined.

$$\nabla^2 V_1 = 0 \tag{3-21}$$

$$\nabla^2 V_2 = 0 \tag{3-22}$$

$$V_1(0, v') = 0 \tag{3-23}$$

$$V_1(1, v') = V_2(1, v') = 1 \tag{3-24}$$

$$\nabla^{\perp} V_1(u', 0) = \nabla^{\perp} V_2(u', 1) = 0 \tag{3-25}$$

$$\left.\begin{aligned} V_1 &= V_2 \\ \varepsilon_1 \nabla^{\perp} V_1 &= \varepsilon_0 \nabla^{\perp} V_2 \end{aligned}\right\} \text{ which are for the curve between dielectrics} \tag{3-26}$$

where $u' = u/K(m)$, $v' = v/K'(m)$.

Fourthly, once the voltages at all nodes in the column next to a conductor plate are known, the capacitance of the microstrip line can be obtained through the calculation of total surface charge Q_s.

$$Q = \oint_S \mathrm{D} \cdot ds \tag{3-27}$$

$$Q_s \approx \sum_{k=1}^{N} D_k \Delta v \approx \sum_{k=1}^{N} \varepsilon_k E_k \Delta v \approx \sum_{k=1}^{N} \varepsilon_k \left(-\frac{\Delta V_k}{\Delta u} \right) \Delta v \approx -\sum_{k=1}^{N} \varepsilon_k \Delta V_k \tag{3-28}$$

where $D_k = \varepsilon_k E_k$, $E_k = \left(-\dfrac{\Delta V_k}{\Delta u} \right)$ and we set $\Delta u = \Delta v$.

Here, Q is the total volume charge; Q_s is the total surface charge; **D** is the vector electric flux and **E** is the vector electric field. D_k is the scalar electric flux at k subsection; E_k is the scalar electric field at k subsection; ε_k is the permittivity at k subsection; ΔV_k is the difference scalar potential at k subsection between the node next to the conductor plate and node at the conductor plate; Δu is the single subsection size of the axis perpendicular to the metal plate; Δv is the single subsection size of the axis parallel to the metal plate.

The relative effective permittivity ε_{eff} can be calculated as

$$\varepsilon_{eff}(W) = \sum_{k=1}^{N} \varepsilon_{rk} \Delta V_k \tag{3-29}$$

where ε_{rk} is the permittivity at k subsection, N is the number of subsections.

Finally, the capacitance of the microstrip line with width W will be calculated as

$$C_t(W, H, \varepsilon_r) = 2\varepsilon_{eff}(W)\varepsilon_o \frac{K'(m)}{K(m)} \tag{3-30}$$

Similarly, $C_{e2,stat}(\varepsilon)$ is given by the following equation, in which we should exchange L with W.

$$C_{e2,stat}(\varepsilon) = \frac{1}{2}\left[C_t(L, H, \varepsilon_r) - \frac{\varepsilon_o \varepsilon_r L}{H}\right]W \tag{3-31}$$

To obtain $C_{dyn}(\varepsilon_0)$, ε should be replaced by ε_0 in above equations.

The advantage of utilizing the above method is the exact determination of the curve that separates the two dielectrics in the transformed plane.

Q_{total} is the quality factor associated with system losses, which include radiation from the walls (Q_r), losses in the dielectric (Q_d) and losses in the conductor (Q_c).

$$1/Q_{total} = 1/Q_r + 1/Q_c + 1/Q_d \tag{3-32}$$

where Q_r, Q_d and Q_c are given by [41]

$$Q_r = \frac{c_0\sqrt{\varepsilon_{dyn}}}{4f_r H} \tag{3-33}$$

$$Q_d = \frac{1}{T_g} \tag{3-34}$$

where T_g is the dielectric loss tangent;

$$Q_c = \frac{7860\sqrt{f_r}\times Za_0(W)\times H_{eq}}{P_a(W)} \tag{3-35}$$

where f_r is in GHz, $Za_0(W)$ is the impedance of an air filled microstrip line of width W and thickness H, which is evaluated from $Za(W)$ by setting $\varepsilon_r = 1$. The impedance of the dielectric filled microstrip line of width W is given as follow

$$Za(W) = \frac{\sqrt{\varepsilon_{eff}(W)}}{c_0 C_t(W,H,\varepsilon_r)} \tag{3-36}$$

and

$$P_a(W) = \frac{2\pi\left[\frac{W}{H} + \frac{W/(\pi H)}{W/(2H)+0.94}\right]\left[1+\frac{H}{W}\right]}{\left\{\frac{W}{H} + \frac{2}{\pi}\ln\left[2\pi e\left(\frac{W}{2H}+0.94\right)\right]\right\}^2} \tag{3-37}$$

where $\varepsilon_{eff}(W)$ is the effective permittivity of the dielectric filled line of width W and thickness H.

As mentioned before, f_r is the resonant frequency of the radiating element, here the resonant frequency corresponds to the frequency for which the real part of the input impedance is maximum, the additive reactance term XL does not modify the value of the resonant frequency.

$$f_r = \frac{c_0}{2\sqrt{\varepsilon_{dyn}}}\sqrt{\left(\frac{m}{W_{eff}}\right)^2 + \left(\frac{n}{L_{eff}}\right)^2} \tag{3-38}$$

The effective width W_{eff} and length L_{eff} are calculated from the following relation.

$$L_{eff} = L + \left(\frac{W_{eq} - W}{2}\right)\frac{\varepsilon_{eff}(W) + 0.3}{\varepsilon_{eff}(W) - 0.258} \tag{3-39}$$

where W_{eq} is the equivalent width calculated from the planar waveguide model.

$$W_{eq} = \frac{120\pi H}{Za(W)\sqrt{\varepsilon_{eff}(W)}} \tag{3-40}$$

Similarly, we can calculate W_{eff} by replacing L_{eff}, L, W_{eq}, W and $\varepsilon_{eff}(W)$ with W_{eff}, W, L_{eq}, L and $\varepsilon_{eff}(L)$, respectively.

Then, the capacitance and inductance of the microstrip patch antenna are calculated by

$$C_a = \frac{Q_{total}}{2\pi f_r R_a} \tag{3-41}$$

$$L_a = \frac{R_a}{2\pi f_r Q_{total}} \tag{3-42}$$

The dispersion effect of ε_{eff} in frequency domain is considered in this work, because it was found that ε_{eff} is a changing function of frequency [59].

An accurate equation for evaluating the dispersion effect in frequency domain is given below [60].

$$\varepsilon_{eff}(W, f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}(W, 0)}{1 + P} \tag{3-43}$$

where

$$P = (H / Za(W))^{1.33}\left[0.43 f^2 - 0.009 f^3\right] \tag{3-44}$$

here H is in mm and f in GHz.

Similarly, we can calculate $\varepsilon_{eff}(L,f)$ by replacing $\varepsilon_{eff}(W,0)$ and $\varepsilon_{eff}(W,f)$ with $\varepsilon_{eff}(L,0)$ and $\varepsilon_{eff}(L,f)$, respectively.

3.2.3 Circuit model of feeding via under ground plane

$L_{v,lower}$ and $R_{v,lower}$ are the inductance and resistance of the feeding via under ground plane. The inductance is calculated by [61]

$$L_{v,lower} = 20l_{v,lower}\left[\ln(2l_{v,lower}/r_{v,lower})-1\right] \text{ nH} \tag{3-45}$$

where $l_{v,lower}$, $r_{v,lower}$ are the length and the radius of the feeding via (in mm) under the ground plane.

$$R_{v,lower} = \frac{l_{v,lower}}{\sigma S_{v,lower}} \tag{3-46}$$

where $l_{v,lower}$, $S_{v,lower}$ and σ are the length, the cross-section area, and the conductivity of the feeding via under the ground plane.

$C_{v,lower}$ is the capacitance between the feeding via under the ground plane and the ground plane as well as the shorting vias. It is calculated by the MoM [62].

3.2.4 Circuit model of G-S-G signal traces

C_{sg} is the capacitance of the signal traces, which is a CPW structure and calculated by the conformal mapping method [63]:

$$C_{sg} = 2\varepsilon_0 \varepsilon_{s,eff} \left[\frac{K\left(k_{1,s}\right)}{K\left(k_{1,s}^{'}\right)} + \frac{K\left(k_{0,s}\right)}{K\left(k_{0,s}^{'}\right)} \right] \times l_s \tag{3-47}$$

where $K\left(k_i\right)$ is the complete elliptic integrals of the first kind.

$$\varepsilon_{s,eff} = 1 + q_{1,s}(\varepsilon_r - 1) + q_{2,s}(\varepsilon_r - 1) \tag{3-48}$$

$$q_{1,s} = \frac{K\left(k_{1,s}\right)}{K\left(k_{1,s}^{'}\right)} \left[\frac{K\left(k_{1,s}\right)}{K\left(k_{1,s}^{'}\right)} + \frac{K\left(k_{0,s}\right)}{K\left(k_{0,s}^{'}\right)} \right]^{-1} \tag{3-49}$$

$$q_{2,s} = \frac{K\left(k_{2,s}\right)}{K\left(k_{2,s}^{'}\right)} \left[\frac{K\left(k_{1,s}\right)}{K\left(k_{1,s}^{'}\right)} + \frac{K\left(k_{0,s}\right)}{K\left(k_{0,s}^{'}\right)} \right]^{-1} \tag{3-50}$$

$$k_{0,s} = \frac{s_s}{s_s + g_s} \tag{3-51}$$

$$k_{1,s} = \frac{\tanh\left(\frac{\pi s_s}{2h_{s1}}\right)}{\tanh\left[\frac{\pi(s_s + g_s)}{2h_{s1}}\right]} \tag{3-52}$$

$$k_{2,s} = \frac{\sinh\left(\frac{\pi s_s}{2h_{s2}}\right)}{\sinh\left[\frac{\pi(s_s + g_s)}{2h_{s2}}\right]} \tag{3-53}$$

where l_s is the length of the signal trace, h_{s1} and h_{s2} are the height from the signal trace to the ground plane and the land, respectively, g_s is the signal trace gap, s_s is half the signal trace width.

The signal trace inductance L_{sg} is calculated by the following equation [64]:

$$L_{sg} = \frac{\mu_0 l_s}{2\pi}\left\{ \begin{array}{l} ar\sinh\left(\frac{l_s}{w_s+t}\right)+\frac{l_s}{w_s+t}ar\sinh\left(\frac{w_s+t}{l_s}\right)+\frac{w_s+t}{3l_s} \\ -\frac{1}{3}\left(\frac{l_s}{w_s+t}\right)^2\left[\left(1+\frac{(w_s+t)^2}{l_s^2}\right)^{3/2}-1\right] \end{array} \right\} \quad (3\text{-}54)$$

where w_s is the width of the signal trace, t is the thickness of the signal trace, l_s is the length of the signal trace. In Fig. 3-2, L_{stob} and L_{stov} represent the inductances of the signal trace, the lengths of which are the signal trace to the bond wire and the signal trace to the via connecting the land, respectively.

3.2.5 Circuit model of G-S-G bond wires

The inductance and capacitance of the bond wire are given as follows [65]:

$$L_w = 2l_w \ln\left(\frac{4h_w}{d_w}\right) \text{ nH} \quad (3\text{-}55)$$

$$C_w = \frac{0.5563 l_w}{\ln\left(\frac{4h_w}{d_w}\right)} \text{ pF} \quad (3\text{-}56)$$

where l_w, d_w and h_w are in cm, l_w, d_w and h_w are the length of the bond wire, the diameter of the bond wire, and the distance from the bond wire to the ground plane, respectively. Here it should be mentioned that the grounded bond wires slightly reduces the inductance of the signal bond wire as calculated by (3-54) and the encapsulant slightly increases the capacitance of the signal bond wire as calculated by (3-55). The resistance of the bond wire also approximates using the same formula as the feeding via under the ground plane.

3.2.6 Circuit model of lands

C_{via}, R_v and L_v are the capacitance, resistance and inductance of the vias connecting the lands. C_{via} is also obtained using Method of Moments. R_v and L_v are calculated as the same equations for the feeding via under ground plane.

C_{lg} is the capacitance of the lands. It is again calculated using the conformal mapping method [63].

$$C_{lg} = 2\varepsilon_0 \varepsilon_{l,eff} \left[\frac{K(k_{0,l})}{K(k'_{0,l})} + \frac{K(k_{1,l})}{K(k'_{1,l})} \right] \times l_l \tag{3-57}$$

where

$$\varepsilon_{l,eff} = 1 + q_{1,l}(\varepsilon_r - 1) \tag{3-58}$$

$$q_{1,l} = \frac{K(k_{1,l})}{K(k'_{1,l})} \left[\frac{K(k_{0,l})}{K(k'_{0,l})} + \frac{K(k_{1,l})}{K(k'_{1,l})} \right]^{-1} \tag{3-59}$$

$$k_{0,l} = \frac{s_l}{s_l + g_l} \tag{3-60}$$

$$k_{1,l} = \frac{\tanh\left(\frac{\pi s_l}{2h_l}\right)}{\tanh\left(\frac{\pi(s_l + g_l)}{2h_l}\right)} \tag{3-61}$$

where l_l is the length of the land, h_l is the height from land to ground plane, g_l is the gap between lands, and s_l is half the land width.

3.3 Validation of the circuit model

In this section, we will validate the proposed model with HFSS simulations, as well as discuss the modeled results and measurements for a typical ICPA.

The ICPA is designed using the Ferro-A6 LTCC material system with the dielectric constant of 5.9 and loss tangent of 0.002 at 6 GHz. Fig. 3-4 shows the photo of the fabricated antenna part of the ICPA that measures 17 x 17 x 1.6 mm^3. The thickness of the top, middle, and bottom layers of the ICPA are 0.8, 0.4, and 0.4 mm, respectively. The vias have the same diameter of 100 μm. The signal traces have the same size of 2 × 0.4 mm^2. The lands are squares with a length of 0.34 mm. The feeding via to the microstrip patch is 1.2 mm long, while the other vias to the ground plane and lands are 0.4 mm long. The aperture on the ground plane for the feeding via to pass through is 0.6 mm in diameter. The feeding and grounded bond wires with a diameter of 32.5 μm are 1.22 mm long. Referring to Fig. 3-1, the sizes of the microstrip patch antenna are: L = 9.9 mm, W = 15 mm, X_0 = 0.9 mm, Y_0 = 1.4 mm, X = 2.35 mm, and Y = 7.5 mm.

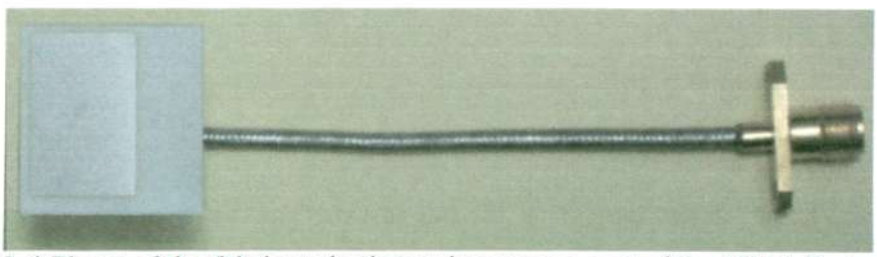


Fig. 3-4 Photo of the fabricated microstrip antenna part of the ICPA for testing

3.3.1 Microstrip patch antenna results

Fig. 3-5 shows the HFSS setting up and Fig. 3-6 shows the advanced design system (ADS) circuit model setting up for the microstrip patch antenna part. Fig. 3-7 shows the measured, modeled, and simulated return loss of the microstrip patch antenna. The result calculated by the method in [53] is also included for comparison purpose. As can be seen from Fig. 3-7, the center frequencies of the impedance bandwidth are 5.9 GHz, 5.83 GHz, 5.84 GHz, and 6.24 GHz for the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is only 0.07 GHz (0.07/5.9 = 1.19%), while the difference between the measured and calculated from the method in [53] is 0.34 GHz (0.34/5.9 = 5.76%).

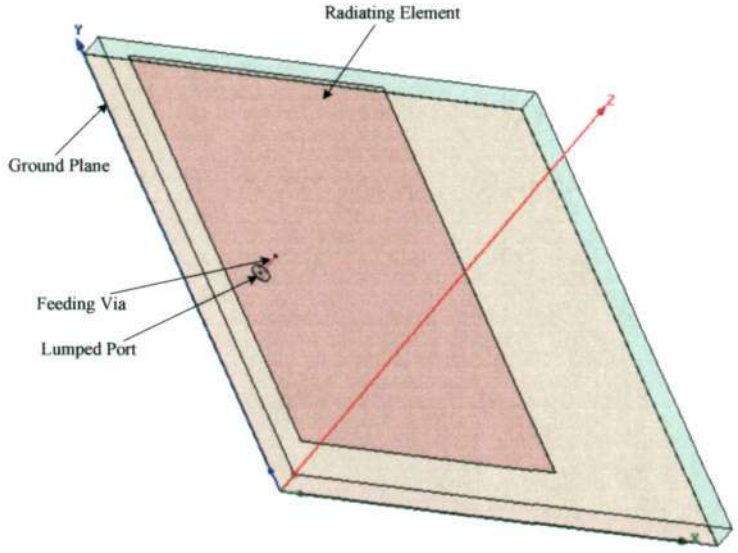


Fig. 3-5 HFSS setting up for the microstrip antenna

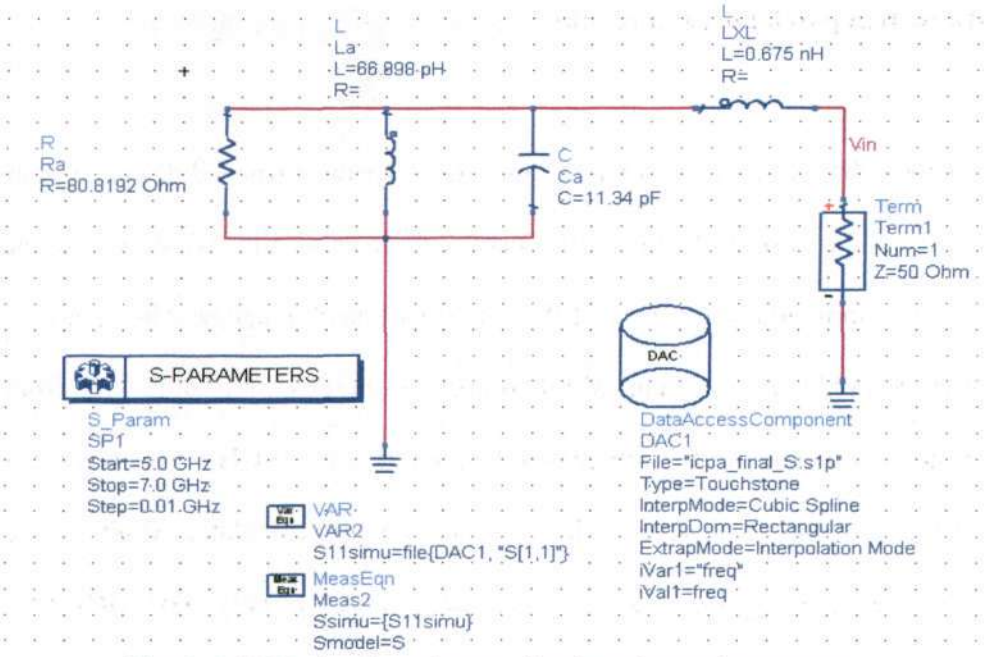


Fig. 3-6 ADS circuit setting up for the microstrip antenna

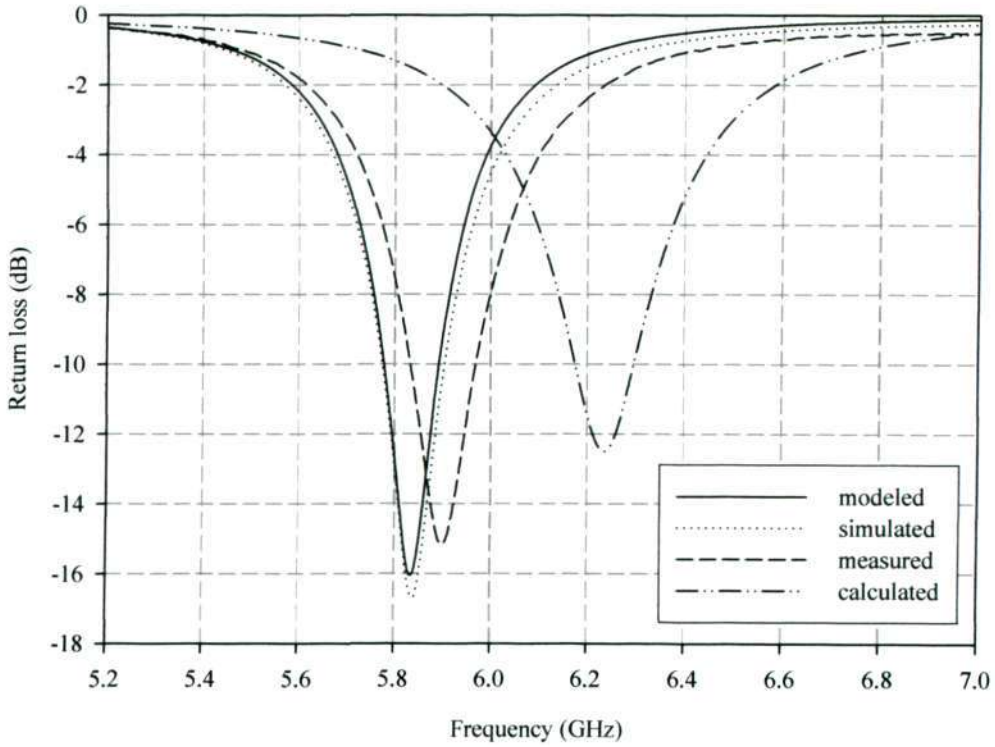


Fig. 3-7 Return loss of the microstrip antenna

Fig. 3-8 shows the measured, modeled, simulated, and calculated input impedance. The resonant frequencies are 5.83 GHz, 5.7 GHz, 5.77 GHz, and 6.15 GHz from the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is only 0.13 GHz (0.13/5.83 = 2.2%), while the difference between the measured and calculated from [53] is 0.32 GHz (0.32/5.83 = 5.5%).

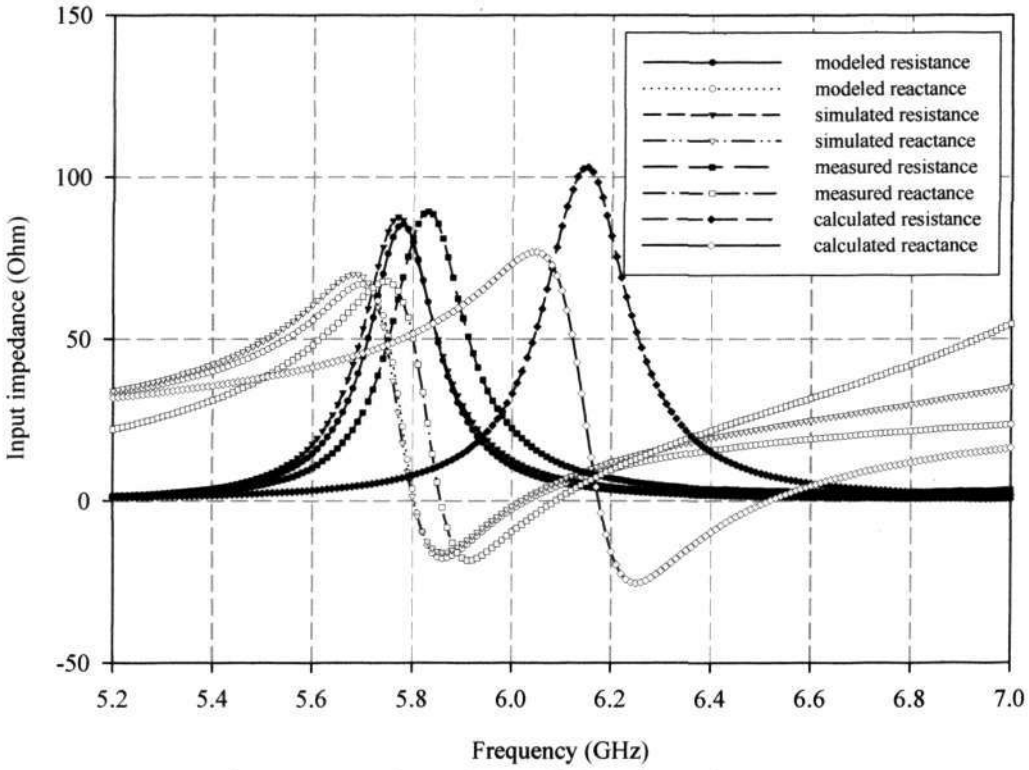


Fig. 3-8 Input impedance of the microstrip antenna

The resonant resistance of the *RLC* parallel circuit is 89.3 Ω, 85.45 Ω, 87.7 Ω, and 103.05 Ω from the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is 3.85 Ω (3.85/89.3 = 4.3%), while the difference between the measured and calculated from [53] is 13.75 Ω (13.75/89.3 = 15.4%).

3.3.2 ICPA results

Fig. 3-9 shows the HFSS setting up and Fig. 3-10 shows the ADS circuit model setting up for the ICPA. The measurement of the feeding network of the ICPA cannot be done with our existing facilities. Therefore, we have to validate our circuit model with the HFSS simulations. This validation is supported from the above comparison shown in Figs. 3-7 and 3-8. It is evident from them that the simulated results from the HFSS are closely matched with the measured results of the microstrip patch antenna.

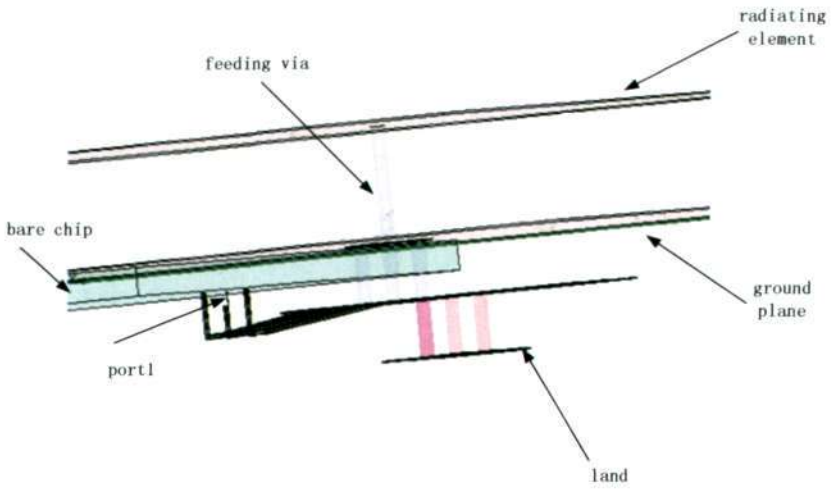


Fig. 3-9 HFSS setting up for the ICPA

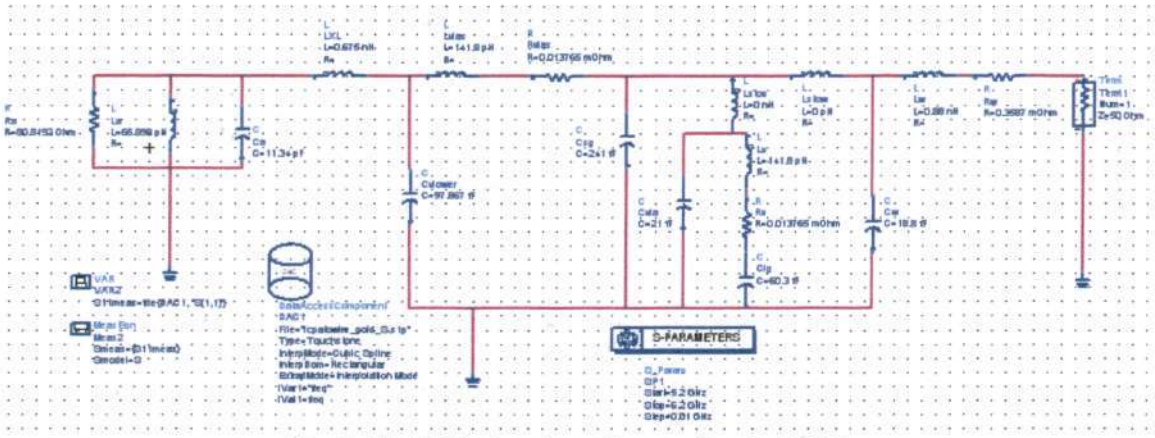


Fig. 3-10 ADS circuit setting up for the ICPA

To extract the element parameters of the circuit model from the HFSS simulations, the ADS is utilized for optimization and matching. It is found that the extraction is quite time-consuming. The modeled and extracted element parameters of the circuit model are listed below for comparison.

For the resistance values of the feeding via under ground plane, vias to lands and bond wires are trivial parts of the whole circuit model, they are not compared here. From Tables 3-I, 3-II, and 3-III, the differences between the modeled and extracted parameters are acceptable.

Table 3-I Parameters for microstrip patch antenna

	R_a (Ω)	L_a (pH)	C_a (pF)	L_{XL} (nH)
Extracted	89.97	73.80	10.59	0.71
Modeled	85.48	66.90	11.34	0.68

Table 3-II Parameters for feeding via under ground plane and G-S-G signal traces

	$L_{v,lower}$ (nH)	$C_{v,lower}$ (fF)	C_{sg} (fF)	L_{stow} (nH)	L_{stov} (nH)
Extracted	0.16	119.99	319.98	0.43	0.17
Modeled	0.14	98.00	300.00	0.41	0.19

Table 3-III Parameters for G-S-G vias to lands, lands and bondwires

	C_{via} (pF)	L_v (nH)	C_{lg} (fF)	C_{wg} (fF)	L_w (nH)
Extracted	24.00	0.16	30.37	23.00	0.72
Modeled	21.00	0.14	26.50	18.90	0.88

Finally, the modeled and simulated center frequencies of impedance bandwidth for the ICPA occur at 5.78 GHz and 5.694 GHz, respectively. The difference between our modeled and the simulated is only 0.086 GHz (0.086/5.694 =1.5%). Defining here the resonant frequency as at which the imaginary part of the input impedance is zero, we have 5.822 GHz and 5.745 GHz from the modeled and simulated results, respectively. The difference between our modeled and the simulated is only 0.077 GHz (0.077/5.745 = 1.34%). The modeled and simulated resonant resistance are 26.5 Ω and 25.7 Ω, respectively. The difference is 0.8 Ω (0.8/25.7 = 3.1%).

3.4 Summary of the chapter

A circuit model of a microstrip patch antenna on a CLGA package is developed with an emphasis on verifying existing or deriving analytical formulas. The circuit model considers the microstrip patch antenna fed by packaging interconnects such as bond wires, signal traces, and vias in a G-S-G configuration from the carried chip. The model is validated with the HFSS simulations and measurements, it is well suitable for the antenna-chip codesign of a highly integrated RF transceiver. The modeled center frequency of impedance bandwidth for the ICPA is 5.78 GHz while the simulated one is 5.694 GHz. The difference is only 0.086 GHz (0.086/5.694 =1.5%). The resonant frequencies are 5.822

GHz and 5.745 GHz from the modeled and simulated results, respectively. The difference between our modeled and the simulated is only 0.077 GHz (0.077/5.745 = 1.34%). The corresponding modeled and simulated resonant resistance are 26.5 Ω and 25.7 Ω, respectively. The difference is 0.8 Ω (0.8/25.7 = 3.1%).

CHAPTER FOUR

CHARACTERISTICS OF THE PACKAGING INTERCONNECT COMPONENTS FOR THE ICPA

We have introduced the architecture of the ICPA, and have investigated the ICPA from the view point of the circuit model.

In this chapter, we focus on the study of the feeding network for the ICPA on a CBGA package, from the viewpoint of the impedance and radiation patterns. The ICPA in a thin 48-ball cavity-down ceramic ball grid array integrated circuit package format has been designed for applications at 5.8 GHz using the FDTD method. The ICPA has been fed by a bond wire, a signal trace and a via through an aperture on the ICPA ground plane. The effects of these feeding components on the performance of the ICPA have been investigated. What's more, we study the ICPA by a strategic via for frequency band selection.

4.1 Design of the ICPA and FDTD analysis

The following design parameters will be treated as the basic parameters for our study in this chapter. The radiating element in our design is a microstrip patch of size 7.75 x 12.09 mm^2. The signal traces have the same size of 2.17 x 0.62 mm^2, the solder balls have the same volume of 0.03 mm^3, and the bond wires have different lengths from 3.434 to 5.294 mm. The bare CMOS chip is adhered to the cavity base. The chip cavity has the volume of 11.47 x 11.47 x 0.636 mm^3, which can accommodate the bare chip of size up to 9.0 x 9.0 x 0.318 mm^3. The ground plane of the ICPA provides good shielding to the bare chip from the radiating-element of the ICPA. The feed of the radiating element of the ICPA from the single-chip RF transceiver is realized with a bond wire of length 3.744 mm, a signal trace of size 2.17 x 0.62 mm^2, and a via of length 1.91 mm through an aperture of size 0.62 x 0.62 mm^2 on the ground plane of the ICPA. The ICPA ceramic and metallic layers are alumina and copper, respectively. Alumina has a dielectric constant of 9.8 and copper has a conductivity of 3.7×10^7 S/m. The whole ICPA measures 17 x 17 x 2.544 mm^3.

The design of the ICPA was done with an in-house CAD code and a commercial FDTD simulator [66, 67]. The CAD code first calculates the basic physical properties of the rectangular microstrip patch and then outputs its results such as the patch dimensions and the feeding location as initial values to the FDTD engine for fine design. The spatial step sizes Δx, Δy, and Δz in the FDTD computation must be properly chosen so that an integral number of Yee cells can fit the ICPA. Furthermore, the spatial step sizes should be much less than the smallest guided wavelength λ_g for accuracy. In our design the spatial step sizes were chosen to be $\Delta x = \Delta y = 0.31$mm and $\Delta z = 0.318$ mm. Thus, the ICPA was fitted with 55 x 55 x 6 cells and also the spatial step sizes were much smaller than the smallest guided wavelength λ_g = 16.52 mm, which corresponds to free space wavelength λ_o=51.7

mm at 5.8 GHz. The chip cavity consumed 37 x 37 x 2 cells. The single-chip RF transceiver was modeled by a piece of silicon of size 29 x 29 x 1 cells. A signal trace was treated to be a thin microstrip line of $7\Delta x$ long and $2\Delta y$ wide, a via to be a thin conductor of $4\Delta z$ long, and a bond wire to be a thin conductor of length varying from $(8\Delta y+3\Delta z)$ to $(6\Delta x+8\Delta y+3\Delta z)$. A solder ball was approximately represented by 2 x 2 x 1 cells. To calculate the far-field patterns, the additional free space mesh cells were added to all six sides of the ICPA. The total computational space was 85 x 85 x 40 cells. The outer boundary was second order stabilized. A Gaussian pulse was used to energize the radiating element of the ICPA. The Gaussian pulse was applied to feed the radiating element of the ICPA through the feeding bond wire, signal trace, via, and aperture. The feeding bond wire was $(8\Delta x+1\Delta y+3\Delta z)$ long. The feeding via had diameter of 0.1 mm and length of $6\Delta z$. The aperture size on the ground plane of the ICPA was $2\Delta x$ x $2\Delta y$. The time step in our design was $\Delta t = 614.3$ fs, which satisfies the Courant stability criterion. The Gaussian pulse width was 32 time steps. The source resistance was set to 50 Ω to reduce the time steps needed for FDTD calculations. It was found that 20000 time steps were sufficient for our simulations.

4.2 ICPA results for the basic parameters

Fig. 4-1 illustrates the simulated and measured return loss of the ICPA. The return loss indicates how well the ICPA is matched to a signal source and how wide the impedance bandwidth is. The impedance bandwidth is defined as the difference between the upper

and lower frequencies for which the return loss is less than or equal to -10 dB. The percentage bandwidth is defined here as the difference between the upper and lower frequencies for which the return loss is less than or equal to - 10 dB divided by the average of the upper and lower frequencies. It is observed from the figure that there is a reasonable agreement between the simulated and measured results. The return loss below -10 dB at the frequency of operation indicates acceptable matching between the ICPA and the 50-Ω signal source is achieved. The simulated and measured impedance bandwidths of the ICPA are 81 MHz (0.079/5.775=1.37%) and 105 MHz (0.105/5.76=1.823%), respectively. The narrow impedance bandwidth is an inherent disadvantage of microstrip antennas. We did not attempt to improve the impedance bandwidth of the ICPA because we focused on the feeding technique of the ICPA.

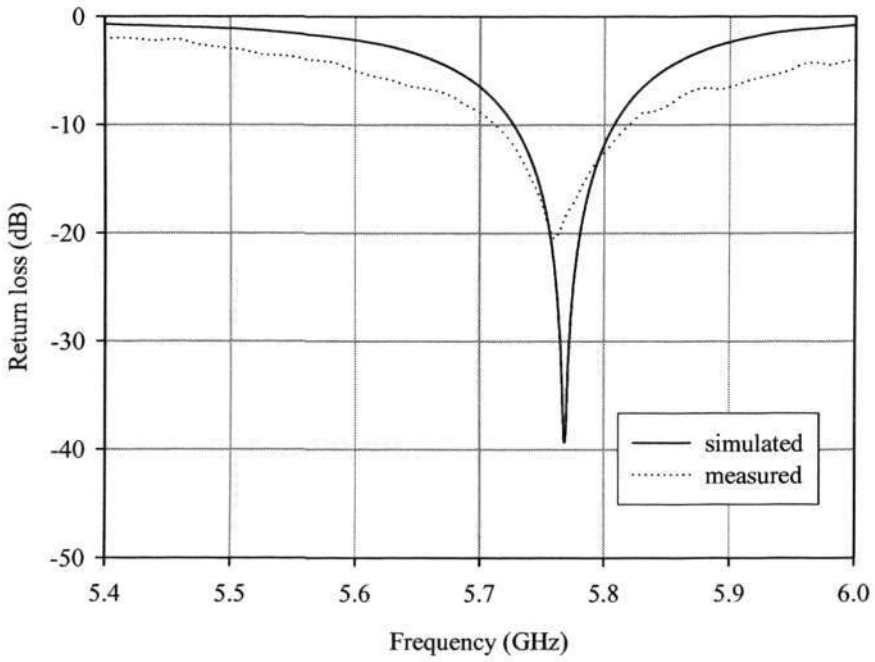


Fig. 4-1 Return loss of the ICPA

Fig. 4-2 exhibits the simulated and measured radiation patterns of the ICPA. In general, the simulated co-polarization patterns agree with the measured results in the main beam. The ripples of the measured radiation patterns in E-plane and H-plane are caused by the edge diffraction around the finite ground plane. The efficiency of the antenna is used to take into account losses at the input terminals and within the structure of the antenna. The high antenna efficiency is desired particularly for personal RF transceiver antennas. The calculated efficiency of the ICPA is 88% by XFDTD. The calculated gain of the ICPA is 6.4 dBi, which is almost 5 dB higher than the gain of most conventional dielectric chip antennas.

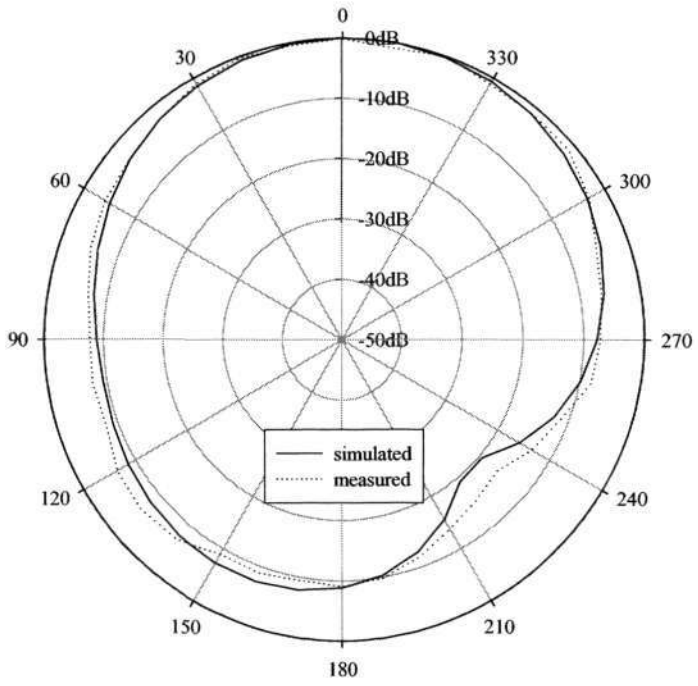


Fig. 4-2(a) Radiation patterns in E-plane

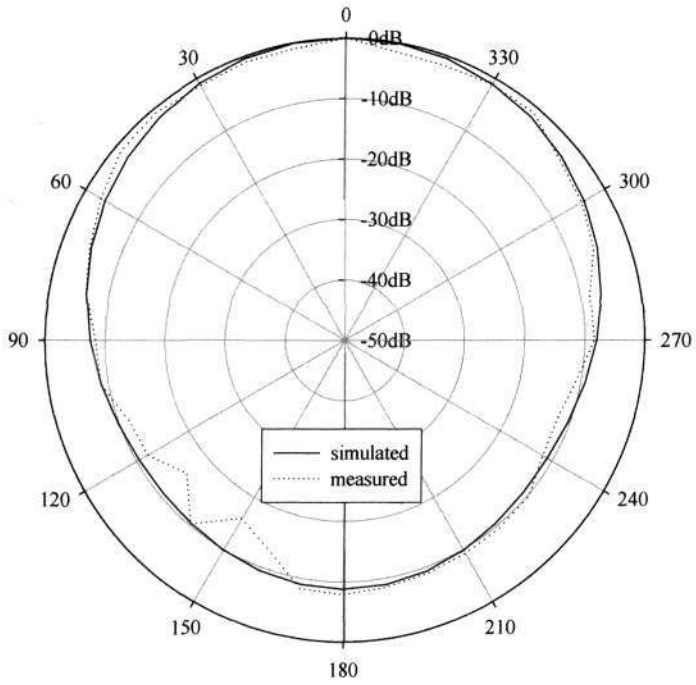


Fig. 4-2(b) Radiation patterns in H-plane

Fig. 4-3 compares near-field intensity distribution for E_z component of the electric field on the substrate middle plane between patch metallization and ground plane with that on the cavity middle plane perpendicular to the ICPA at 5.764 GHz. E_z component is along incident direction. It is strongly confined in incinity of near-field of the antenna. It has higher intensity and dominates enhancement energy in near-field zone [68]. These plots provide useful information on the shielding of the single-chip RF transceiver from the radiating element by the ground plane of the ICPA. Note that the electric field becomes quite weak in the bare chip cavity indicating that good shielding has achieved.

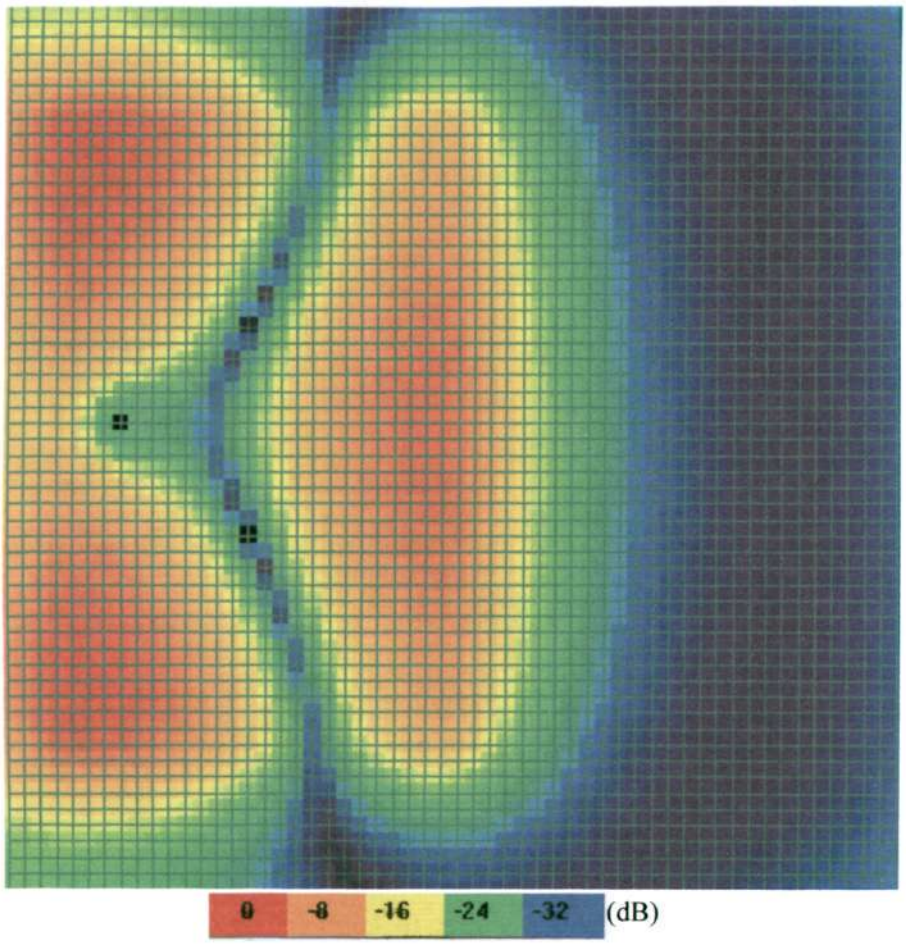


Fig. 4-3(a) Ez on the substrate middle plane between the microstrip patch and ground plane

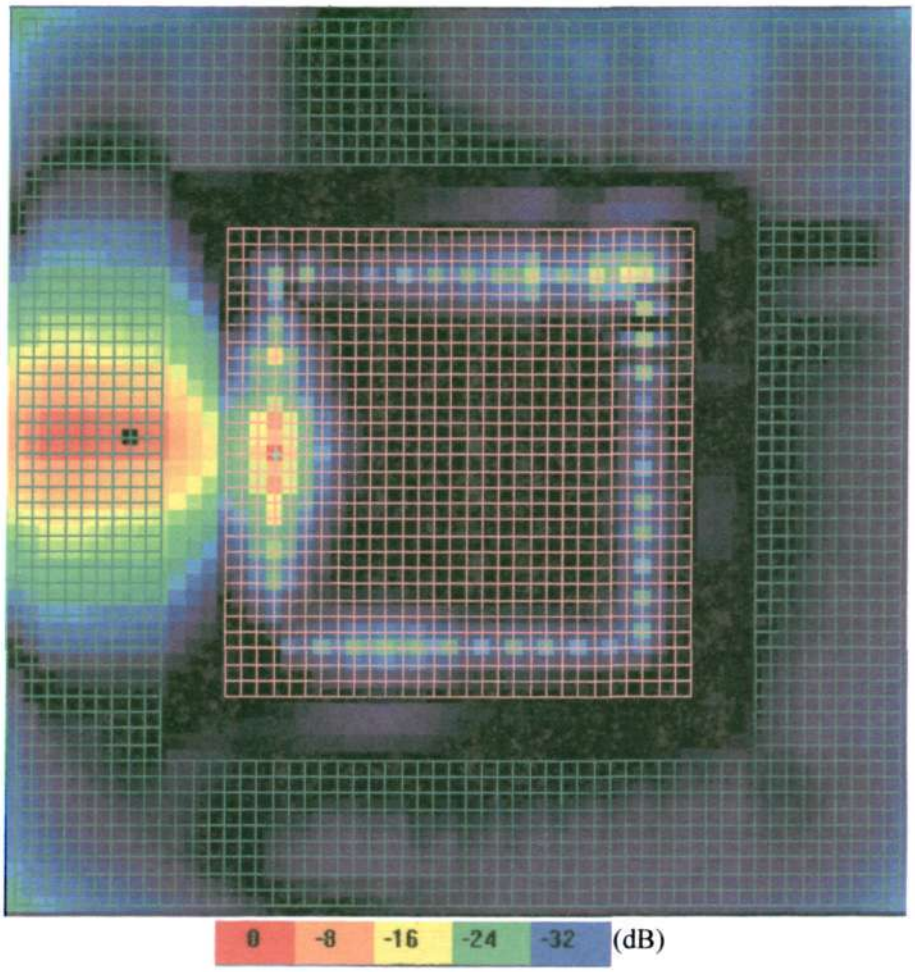


Fig. 4-3(b) Ez on the cavity middle plane perpendicular to the ICPA

4.3 Effects of the feeding components on the ICPA performance

As illustrated above, the feed of the ICPA is realized with a bond wire, a signal trace, and a via through an aperture on the ground plane of the ICPA. In this section, the effects of these feeding components on the performance of the ICPA are determined and discussed.

4.3.1 Effects of feeding via diameter

Vias connecting metallic layers in chips and their packages have been employed to feed microstrip antennas for radio-system-on-package applications recently [17]. A via is an essential part of the feeding network to the ICPA. Fig. 4-4(a) shows the ICPA input impedance versus frequency for three typical via diameters of 100 μm, 120 μm and 150 μm. Note that the resonant frequency at which the reactance is equal to zero increases with the via diameter. The resonant frequency increases from 5.764 GHz for the via diameter of 100 μm, to 5.799 GHz for 120 μm then to 5.824 GHz for 150 μm. The increase in the resonant frequency is due to the decrease of the equivalent inductance of the ICPA by the thick via. Also note that the resistance at the resonant frequency decreases with the via diameter. The resonant resistance decreases from 54 Ω for the via diameter of 100 μm, to 50 Ω for 120 μm and to 48 Ω for 150 μm. This is because the larger the via diameter, the lower the via resistance. Fig. 4-4(b) shows the return loss versus frequency for the three via diameters. The impedance bandwidths are all around 81 MHz, 1.23% (0.081/5.712) for the via diameter of 100 μm, 1.37% (0.081/5.775) for 120 μm, and 1.31% (0.081/5.82) for 150 μm. The far-field radiation patterns of the ICPA were calculated for the principal planes. Fig. 4-5 shows the far-field radiation patterns in the E-plane and H-plane for different via diameters. Obviously, the radiation patterns will be insensitive to the via diameter. They all take the typical patterns of a conventional microstrip patch antenna on a small ground plane. The radiation efficiency and the gain of the ICPA are calculated to be 88% and 6.4 dBi for the three typical via diameters.

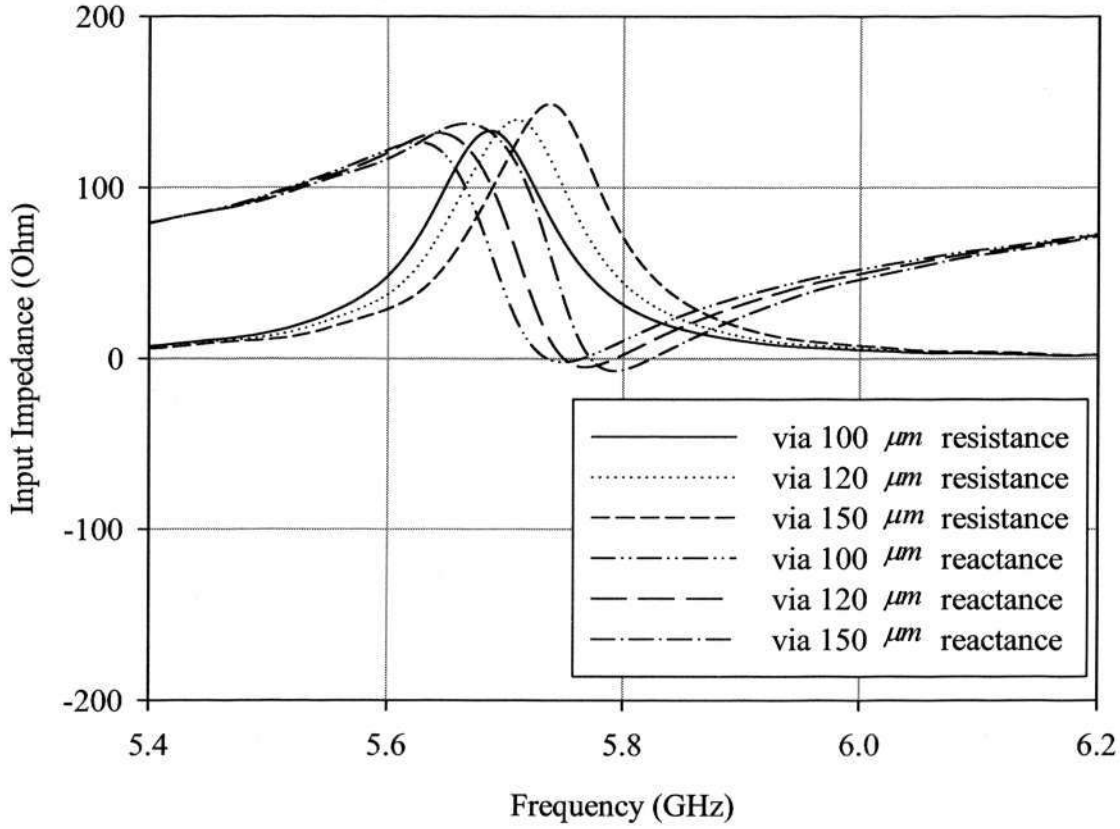


Fig. 4-4(a) Input impedance of the ICPA for three via diameters

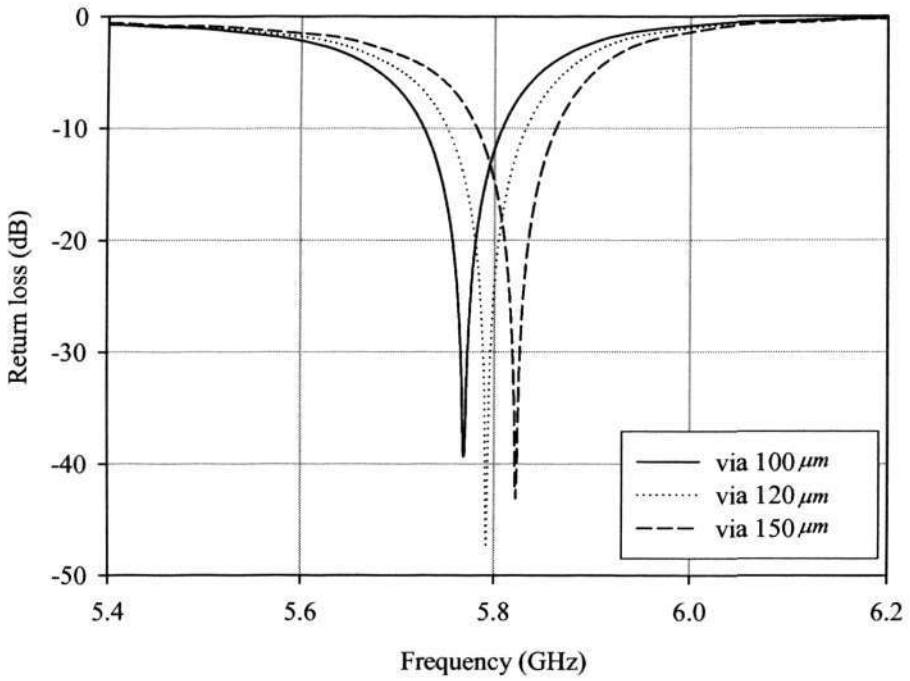


Fig. 4-4(b) Return loss of the ICPA for three via diameters

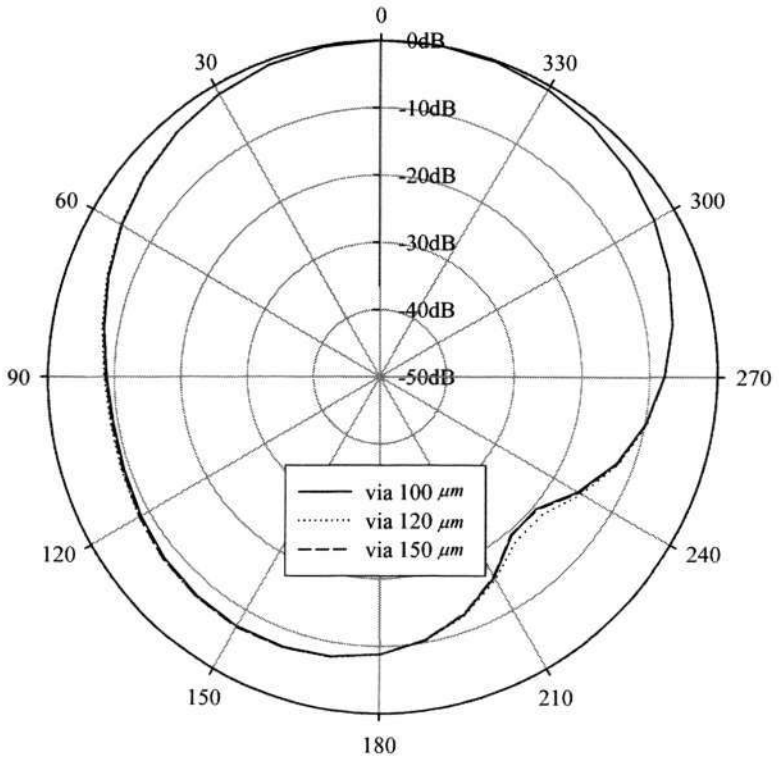


Fig. 4-5(a) Co-polar radiation patterns in E-plane for three via diameters

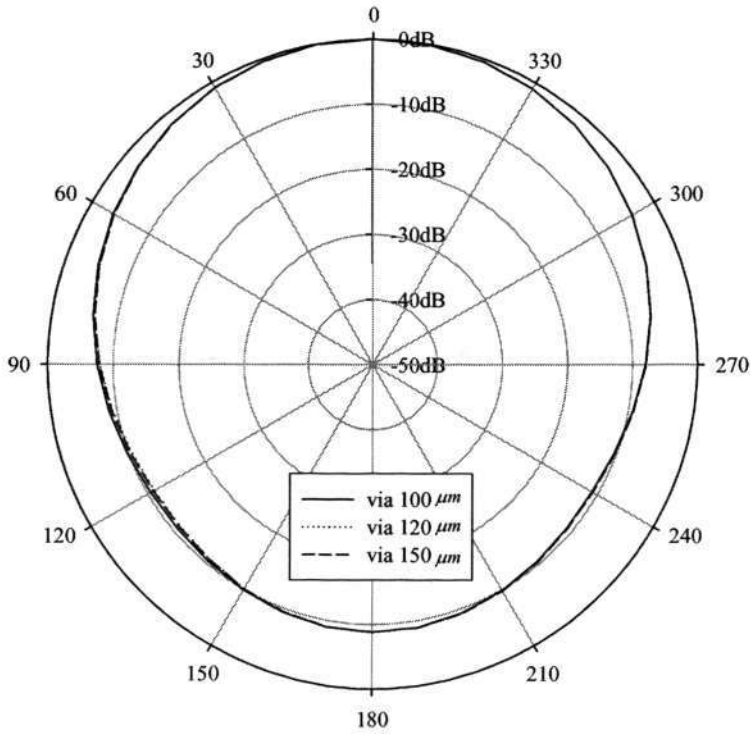


Fig. 4-5(b) Co-polar radiation patterns in H-plane for three via diameters

4.3.2 Effects of ground aperture size

Apertures in chip packages appear on the power and ground planes to reduce the mechanical stress. The aperture on the ground plane of the ICPA avoids short circuit of the feeding via. Fig. 4-6(a) shows the ICPA input impedance versus frequency for three aperture sizes of 0.62 x 0.62 mm^2, 1.24 x 1.24 mm^2, and 1.86 x 1.86 mm^2. Note that the resonant frequency increases from 5.764 GHz to 5.806 GHz and further to 5.841 GHz, while the resonant resistance decreases from 54 Ω to 35 Ω and further to 27 Ω as the aperture size increases from 0.62 x 0.62 mm^2 to 1.24 x 1.24 mm^2 and further to 1.86 x 1.86 mm^2. The increase in the resonant frequency is due to the decrease of the equivalent

capacitance of the ICPA by the larger aperture size. The larger aperture size also enhances the fringe field in the vicinity of the aperture, which increases the effective dielectric permittivity, consequently, the resonant resistance decreases [53]. Fig. 4-6(b) shows the return loss versus frequency for the three aperture sizes. The -10 dB impedance bandwidths are 81 MHz (0.081/5.7675 = 1.404%) for the aperture size of 0.62 x 0.62 mm^2, 83 MHz (0.083/5.7855 = 1.435%) for the aperture size of 1.24 x 1.24 mm^2 and 83 MHz (0.083/5.8045 = 1.43%) for the aperture size of 1.86 x 1.86 mm^2. As expected, the radiation patterns are slightly altered by the ground aperture size which will not be shown. The radiation efficiency and the gain of the ICPA are still calculated to be 88 % and 6.4 dBi for the three aperture sizes.

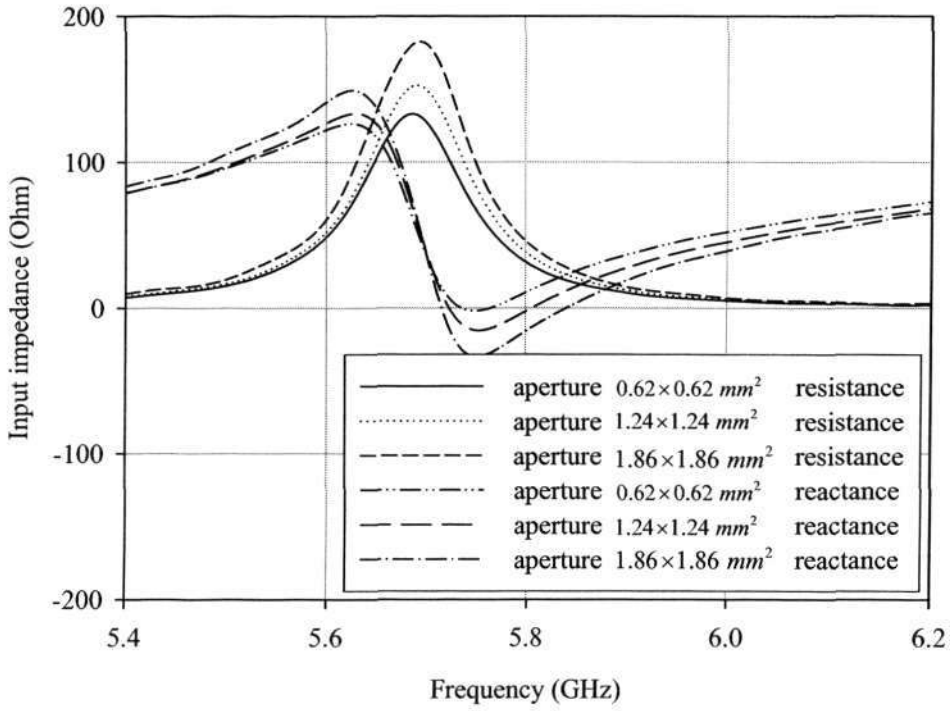


Fig. 4-6(a) Input impedance of the ICPA for three aperture sizes

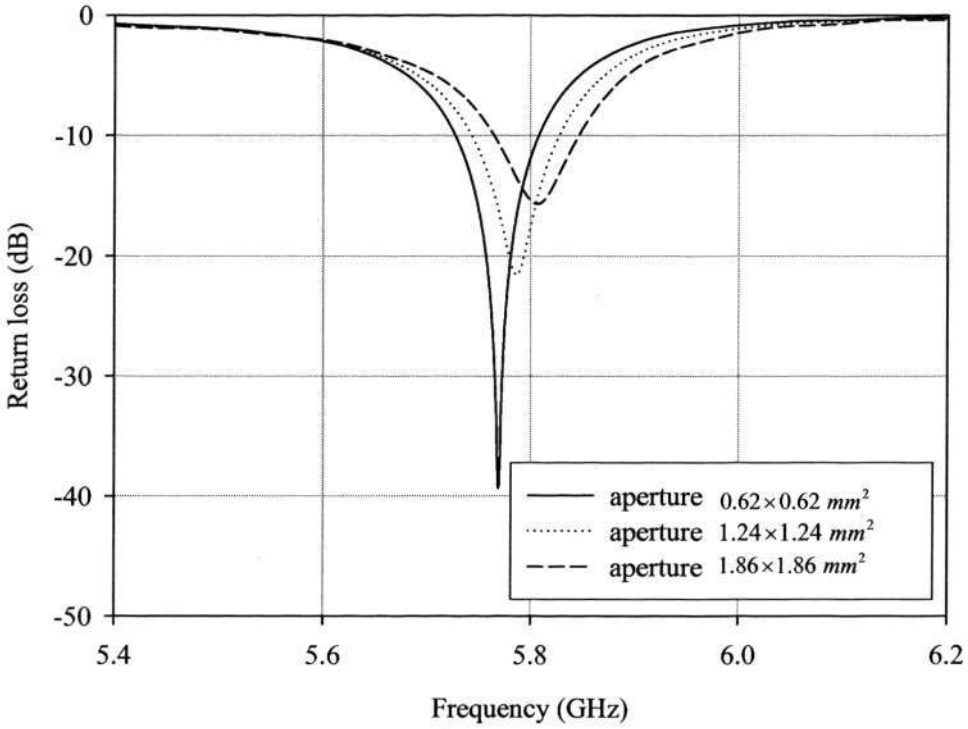


Fig. 4-6(b) Return loss of the ICPA for three aperture sizes

4.3.3 Effects of signal trace size

Signal traces are often symmetrically embedded in chip packages. A signal trace in the ICPA bridges the via and the bond wire to energize the radiating element. Fig. 4-7(a) shows the ICPA input impedance versus frequency for three signal trace sizes of 1.86 x 0.62 mm^2, 2.17 x 0.62 mm^2, and 2.48 x 0.62 mm^2. It can be seen from the figure that the resonant frequency decreases and the resonant resistance increases with the signal trace size. The resonant frequency decreases from 5.85 GHz for signal trace size of 1.86 x 0.62 mm^2 to 5.764 GHz for signal trace of size 2.17 x 0.62 mm^2, while the resonant resistance increases from 27.5 Ω to 54 Ω as the signal trace size increases from 1.86 x 0.62 mm^2 to

2.17 x 0.62 mm^2. The decrease of the resonant frequency is because the longer signal trace increases the capacitance of the whole ICPA. Fig. 4-7(b) shows the ICPA return loss versus frequency for the three signal trace sizes. The impedance bandwidths are 74 MHz (0.074/5.814 = 1.44%), 81 MHz (0.081/5.7675 = 1.404%) and 75 MHz (0.075/5.7365 = 1.31%), respectively. The radiation patterns are insensitive to the signal trace size. The radiation efficiency and the gain of the ICPA are again calculated to be 88% and 6.4 dBi.

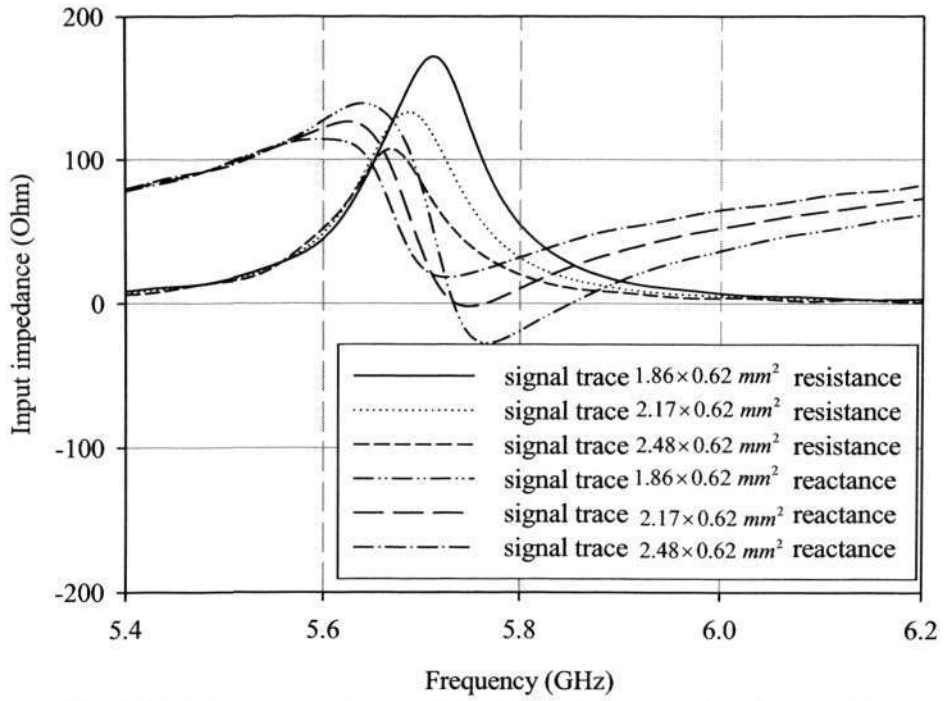


Fig. 4-7(a) Input impedance of the ICPA for three signal trace sizes

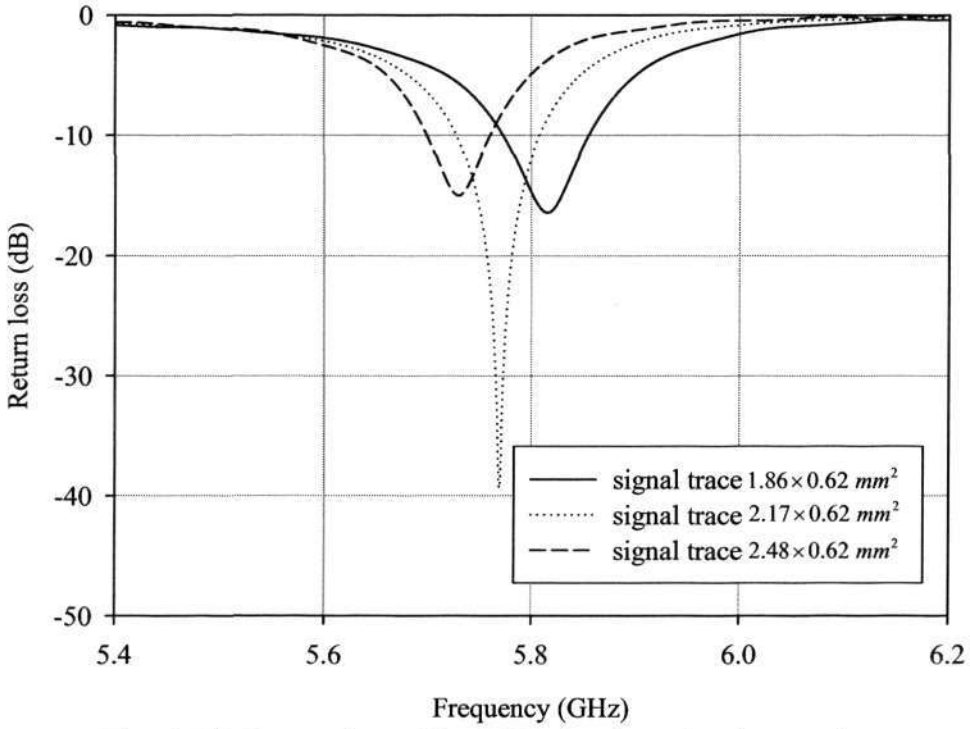


Fig. 4-7(b) Return loss of the ICPA for three signal trace sizes

4.3.4 Effects of bond wire length

Bond wires interconnecting integrated circuits with their packages have recently been used to feed chip antennas at 2.4 and 5.8 GHz [69]. A bond wire was used in the ICPA to connect the 50-Ω signal source to the signal trace. The typical diameter of a bond wire is 32.5 μm, therefore, in our simulation, the diameter of the bond wire was set as 32.5 μm. Figs. 4-8(a) and (b) show the ICPA input impedance and the return loss versus frequency for three bond wire lengths of 3.74 mm, 4.36 mm, and 4.98 mm, respectively. The lengths of the bond wire are longer than common bond wire used in RF applications, the reason is that in our architecture, the distance from the signal trace to the IC pad on the IC chip is a

little long. The resonant frequency decreases from 5.764 GHz to 5.762 GHz and further to 5.756 GHz, while the resonant resistance increases from 54 Ω to 57 Ω and further to 63 Ω. These are because the longer bond wire induces more inductance and resistance of the whole structure. The impedance bandwidths are 81 MHz (0.081/5.7675 = 1.404%), 78 MHz (0.078/5.769 = 1.35%) and 77 MHz (0.077/5.7695 = 1.32%), respectively. The radiation patterns are not sensitive to the bond wire length either. The radiation efficiency and the gain of the ICPA are maintained to be 88% and 6.4 dBi for the three bond wire lengths.

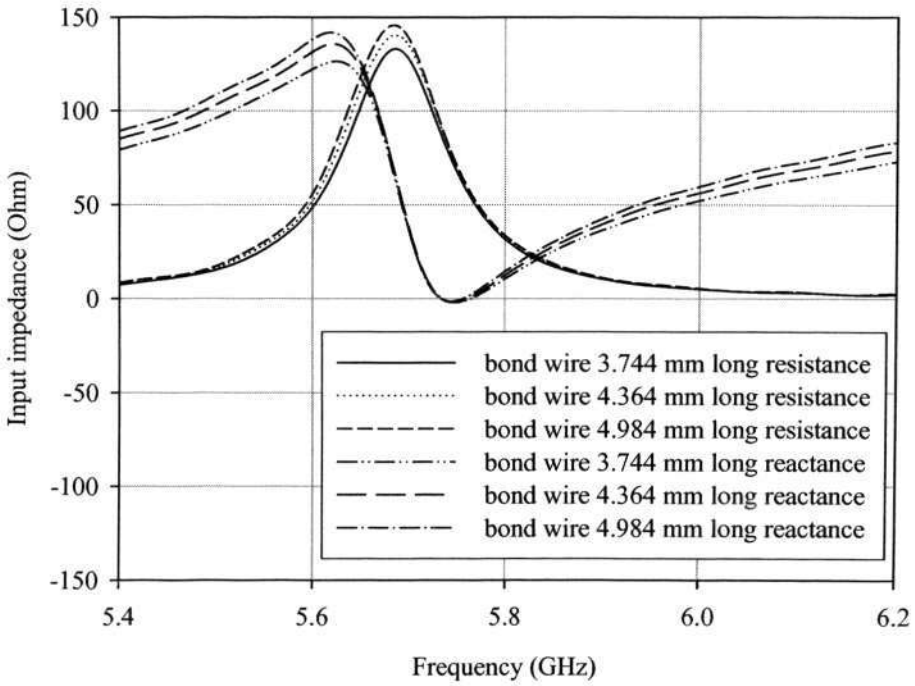


Fig. 4-8(a) Input impedance of the ICPA for three bond wire lengths

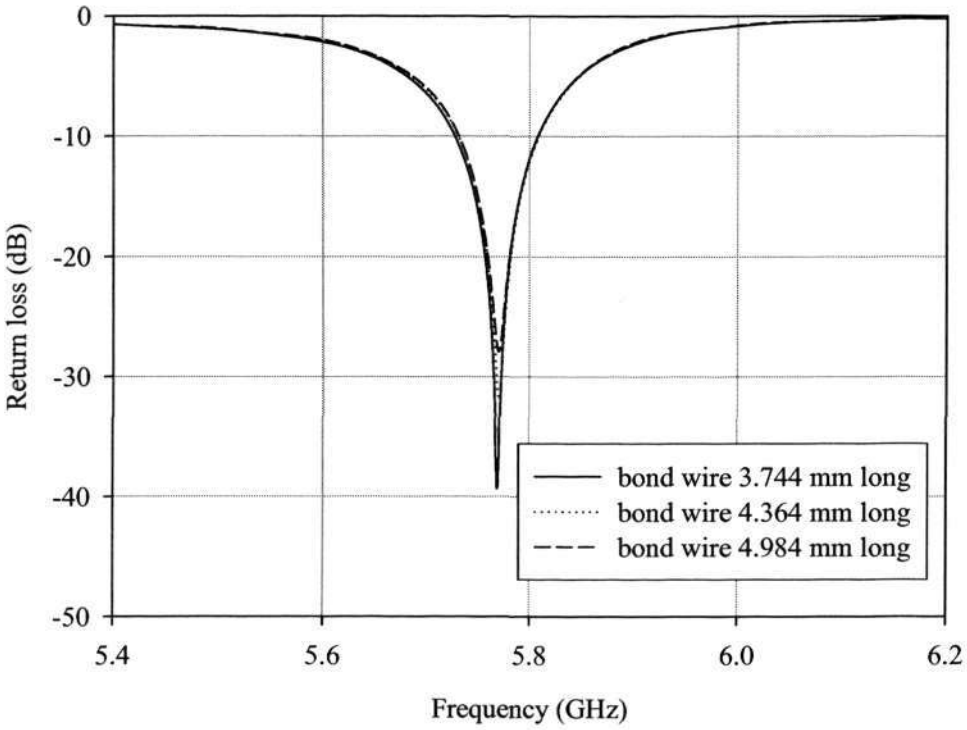


Fig. 4-8(b) Return loss of the ICPA for three bond wire lengths

Based on the studies above, a further noticeable achievement we can see is that in our simulation results, the reactive part of the input impedance presents more inductive than capacitive characteristics, which is desirable when studying the matching interface between the radiating element and the LNA, because the MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) have intrinsic capacitive property, which will be demonstrated in details in the following chapter.

4.4 Band selection characterization of the ICPA

In this section, we study the ICPA that features a via shorting scheme. The via can be easily shorted to ground or left open at the board-level to achieve frequency band selection.

In addition, this ICPA offers the possibility to achieve shorting using a simple diode circuit in the RF transceiver for frequency band selection purpose [22, 39]. The ability to select different frequency bands greatly enhances the ICPA applications in wireless communications. What's more, this ICPA will be treated as a sample to illustrate the antenna measurement equipment and setting up.

4.4.1 Band selection ICPA

The fabricated prototype ICPA is assembled on a test board as shown in Fig. 4-9 and Fig. 4-10. The ICPA is fabricated with FERRO A6-M in LTCC material system, which has a dielectric constant of 5.9 and a dissipation factor of 0.0012 at 5 GHz. The ICPA is designed in a cavity-down CBGA package structure with nine tape layers. The microstrip patch radiator is printed on the top surface of the ICPA with two vias linked to the microstrip patch radiator. One via is used for antenna excitation and the other via is utilized for frequency band selection. The ground plane of the ICPA is printed on the bottom surface of the third layer. A guard ring is employed, and is shorted to the ground plane to reduce the interference of the antenna to the RF transceiver. A multi-tier cavity is formed in the centre of the ICPA, and it can accommodate a $4 \times 4 \times 0.5$ mm^3 CMOS single-chip RF transceiver die. The ICPA is designed to have 88 I/Os with a JEDEC standard ball pitch of 1.27 mm. The prototype ICPA size is $17 \times 17 \times 2$ mm^3 with the microstrip patch radiator size of 10.5×10.5 mm^2.

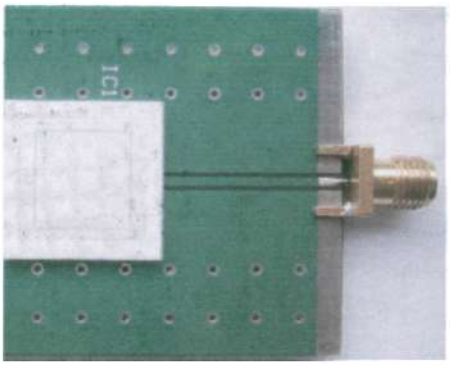


Fig. 4-9 Mounted band selection ICPA on the test board

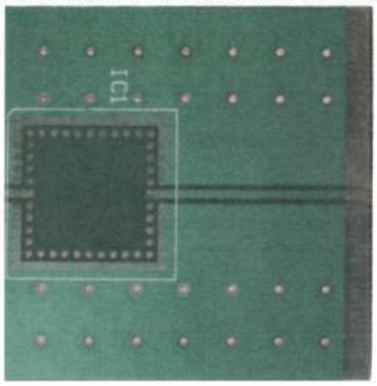


Fig. 4-10 Bare test board

4.4.2 Measurement results of the band selection ICPA

Measurements were carried out in an anechoic chamber using a HP 8510C network analyzer. The setting up for radiation patterns and s-parameters are shown in Fig. 4-11 and Fig. 4-12, respectively. The return loss characteristic is shown in Fig. 4-13 whilst the radiation patterns for opening and shorting of the band-select via are shown in Fig. 4-14 and Fig. 4-15 respectively.

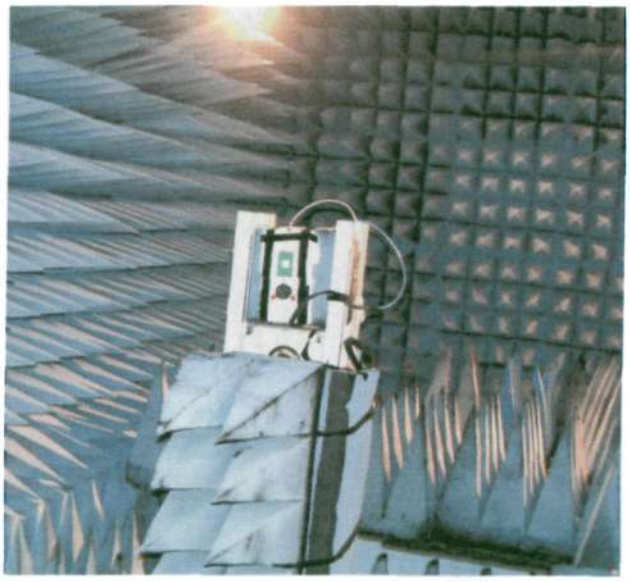


Fig. 4-11 Anechoic chamber room setting up for measuring radiation patterns

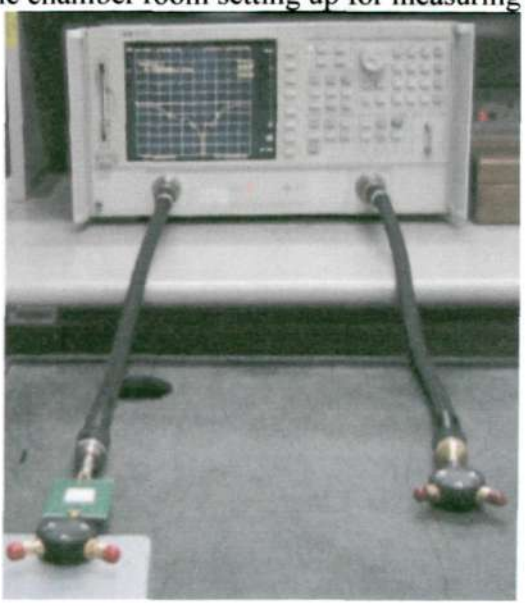


Fig. 4-12 Setting up for measuring s-parameters

Fig. 4-13 illustrates the measured return loss when the band-select via is shorted and opened on the board-level. The minimum return loss occurs at 5.37 and 5.67 GHz for the short and open cases, respectively. The shorted case has a 6 dB return loss and bandwidth of 80 MHz, while the opened case has a 10 dB return loss and bandwidth of 120 MHz. Fig.

4-14 shows the measured far-field radiation patterns at 5.37 GHz when the band-select via is shorted, while Fig. 4-15 indicates the measured far-field radiation patterns at 5.67 GHz when the band-select via is opened. As shown in both Fig. 4-14 and Fig. 4-15, the far-field radiation patterns for both cases are similar to those of a conventional microstrip antenna on a small ground plane. Similar behavior can be observed for the antenna gain characteristics.

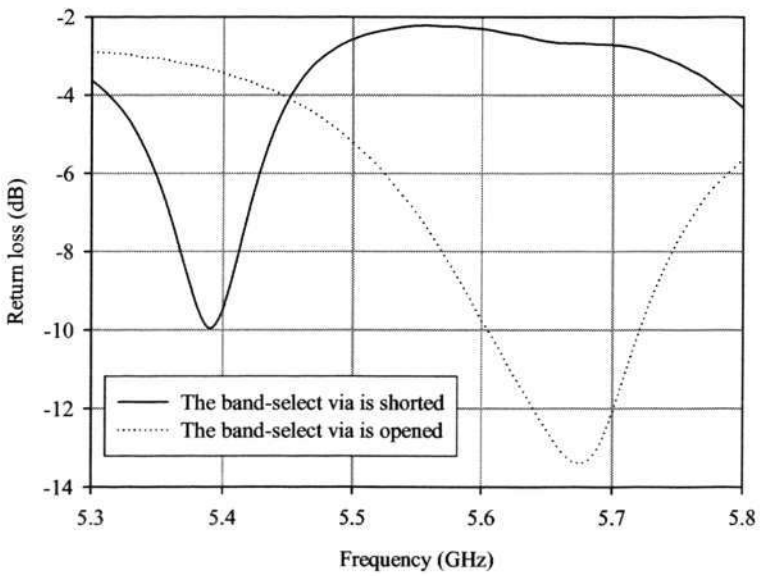


Fig. 4-13 Measured return loss of the band selection ICPA

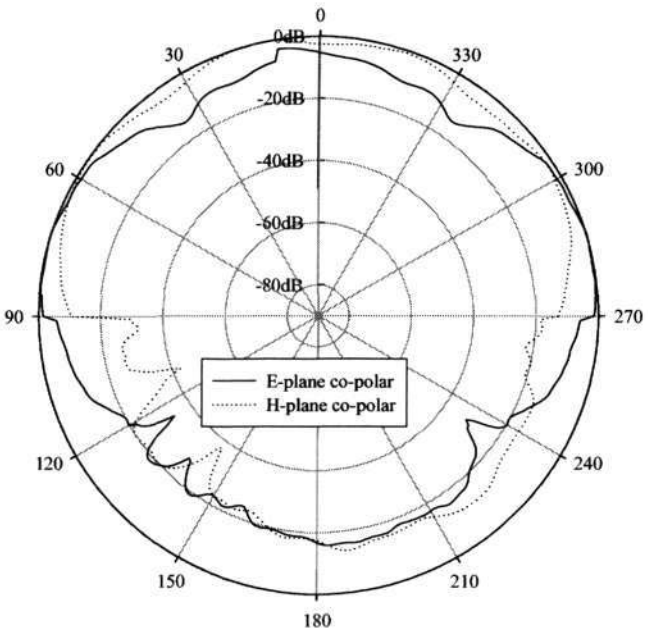


Fig. 4-14 Measured E- and H-plane patterns when the band-select via is shorted

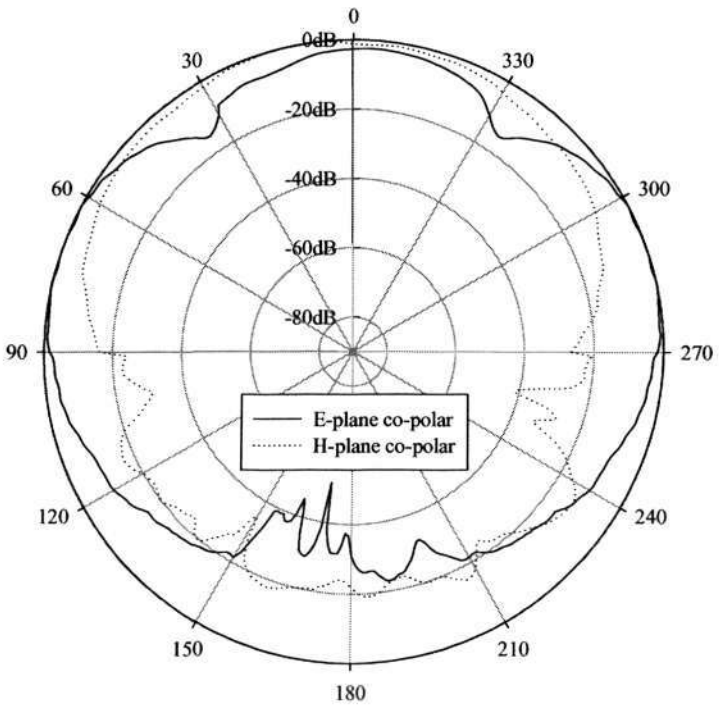


Fig. 4-15 Measured E- and H-plane patterns when the band-select via is opened

4.5 Summary of the chapter

This chapter has focused on the development of the feeding technique to integrated circuit package antennas for single-chip wireless transceivers. A compact ICPA has been designed and fabricated in a cavity-down CBGA package format. Results show that the ICPA achieved impedance bandwidth of 1.4% and radiation efficiency of 88%, and gain of 6.4 dBi at 5.764 GHz. The effects of the different physical feeding components of the ICPA on the antenna performance have been investigated using the FDTD method. It has been found that they mainly affect the impedance characteristics but not the radiation properties of the ICPA. The bandwidth of the ICPA can be improved by adopting different forms of the radiating element.

A further noticeable achievement is that in our simulation results, the reactive part of the input impedance presents more inductive than capacitive characteristics, which is desirable when studying the matching interface between the radiating element and the LNA, because the MOSFETs have intrinsic capacitive property.

The technique for frequency band selection of ICPA, which is designed and fabricated using LTCC technology, has been experimentally verified. The prototype ICPA operates at 5.37 and 5.67 GHz when the band-select via is shorted and opened, respectively. The frequency band selection capability greatly enhances the ICPA applications in wireless communications.

CHAPTER FIVE

ANTENNA-CHIP CODESIGN

5.1 Antenna-chip codesign interface

LNA is one of the key components in typical RF receiver designs. A stable 50-Ω input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier should be provided on a traditional LNA design. In CMOS LNA circuits, matching is often done with a source-degenerative inductor. When referring back to the gate input, the source-degenerative inductance is transformed into a real impedance. The advantage of using this architecture is that it ideally does not introduce any extra noise source [70]. The inductive source degeneration method offers the possibility of achieving the best noise performance among current architectures, although it's a narrow-band approach [71].

SiP has been brought forward as a possible better option than SoC in improving RF performance and decreasing total implementation cost [72]. Moving the expensive, low-quality on-chip passive components off the chip and integrating them in SiP substrate can achieve the high performance and low cost for RF applications [6, 16, 73]. The argument still exists that if passive components are moved off the chip, a package interface will be

inserted which will consequently induce unwanted parasitic effects to RF circuits and thus degrade the circuit performance. Researchers have demonstrated chip-package codesign solution with trade-offs for on-chip versus off-chip passive integration. Studies in [6] and [16] primarily focused on off-chip passive components design while no trade-offs were performed for on-chip versus off-chip passives. In [72], it improved the above work. Duo et al developed co-designed and co-optimized methods for the optimal solution between on-chip and off-chip components design. Unfortunately, the early work did not report any real architecture utilizing package components to gain the whole system optimization, although chip-package codesign methodology has been proposed in many reports as a milestone in RF transceiver design.

We have stated in previous chapters that chip-package codesign offers the advantage of removing the 50-Ω constraints so that a higher performance can be achieved. It is also desirable in LNA design to eliminate the "huge" inductors occupying large die areas. As the first active stage of an RF receiver front-end, the LNA plays a critical role in chip-package codesign for providing the interface between the antenna and the chip, which is named antenna-chip codesign interface in this chapter. In the antenna-chip codesign study, the large passive matching inductor will be realized into the antenna part, both cost and area of the RF transceiver will be saved.

In our study, a traditional source-degenerated LNA using on-chip architecture with 50-Ω input impedance will be presented as a reference architecture. The key inductors will be moved out of the chip and integrated into the package, which uses the in-package architecture. These two methods are popularly used in current LNA designs. The purpose we describe them is to compare with our proposed new interface, so we can validate our

anticipation that our new interface will improve the critical performance of the LNA. Finally, as the main point of the study in this chapter, the 50-Ω matching inductor of the LNA will be removed and the antenna will be designed as an inductive element to directly match the capacitive MOS transistor of the LNA circuit. Package interconnect components will be utilized in this matching technique to put the antenna-chip codesign concept into realization.

5.2 LNA design with 50-Ω interface

5.2.1 CMOS LNA and noise analysis

In the design of the LNA, several common goals must be considered, which include minimizing the noise figure of the amplifier, providing the desired gain with sufficient linearity, providing a 50-Ω input impedance to connect with external components, and minimizing the power consumption. Since the primary role of the LNA is to lower the overall noise figure of the entire receiver, noise optimization is one of the crucial steps in the LNA design procedure [74, 75].

Fig. 5-1 shows the cascade topology for the input stage of the LNA, which has been widely used for its low NF and high input-output isolation [71], at the same time, the input and output matching can be done separately. The design involves essential tradeoffs between gain, noise, power, impedance matching, stability and linearity.

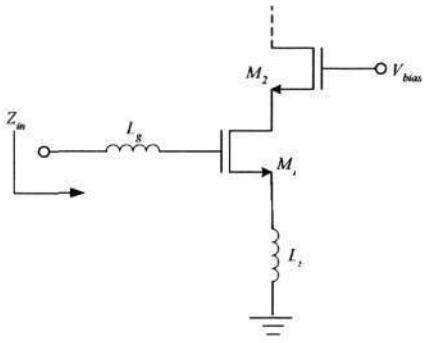


Fig. 5-1 LNA with inductive degeneration input stage

The noise factor (F) of an LNA represents how much the given system degrades the signal-to-noise ratio [74].

$$F \triangleq \frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}} = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power by Source Impedance}} \tag{5-1}$$

The input impedance can be calculated as [71]

$$Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s$$

$$\approx \omega_T L_s \qquad \text{(at resonance).} \tag{5-2}$$

$$\omega_o^2 = \frac{1}{\left(L_g + L_s\right)C_{gs}} \tag{5-3}$$

$$\frac{g_m L_s}{C_{gs}} = \omega_T L_s = R_s \tag{5-4}$$

where g_m is the device transconductance.

Fig. 5-2 shows the small signal circuit used to obtain the noise factor of the LNA shown in Fig. 5-1 [76].

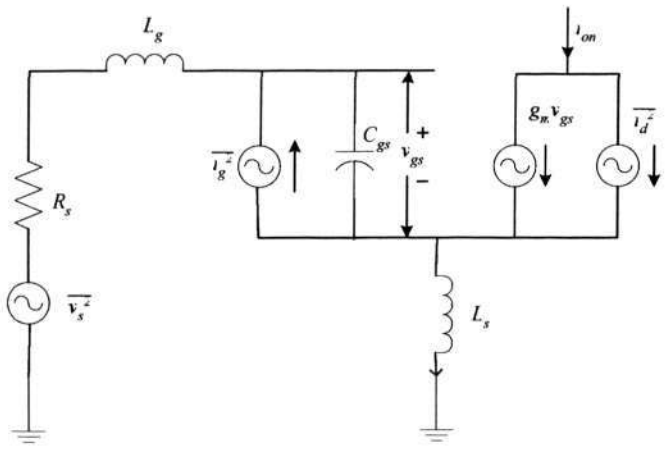


Fig. 5-2 Small signal circuit of the LNA for noise analysis

The simplified expression for the noise factor reads as follows [76], which corrects the widely cited equation in [71]. The corrected noise figure is shown as below.

$$F = 1 + \frac{\gamma}{\alpha}\frac{\omega_o}{\omega_T}\frac{1}{Q}\left(1 + \frac{\delta\alpha^2}{5\gamma}\left(1+Q^2\right) - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right) \tag{5-5}$$

$$Q = \frac{1}{\omega_o R_s C_{gs}} \tag{5-6}$$

where R_s is the source resistance, γ is the coefficient of channel thermal noise, $\alpha \triangleq \frac{g_m}{g_{d0}}$, and g_{d0} is the zero-bias drain conductance. δ is the coefficient of gate noise, and the gate noise is partially correlated with the drain noise, with a correlation coefficient c defined as $c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}$.

5.2.2 Noise factor optimization

F is rearranged for optimization purpose [76], which also corrects the corresponding equation in [71].

$$F = 1 + \frac{\gamma \omega_o L}{3 v_{sat}} P(\rho, P_d) \tag{5-7}$$

$$P(\rho, P_d) = \frac{\frac{P_d}{P_o} P_1(\rho) + \frac{P_o}{P_d} P_2(\rho)}{\rho^3 (1+\rho/2)^2 (1+\rho)} \tag{5-8}$$

$$P_1(\rho) = (1+\rho)^6 + \frac{\delta}{5\gamma}(1+\rho)^2 \left(1+\frac{\rho}{2}\right)^2 - 2|c| \sqrt{\frac{\delta}{5\gamma}(1+\rho)^4 \left(1+\frac{\rho}{2}\right)} \tag{5-9}$$

$$P_2(\rho) = \frac{\delta}{5\gamma}\left(1+\frac{\rho}{2}\right)^2 \rho^4 \tag{5-10}$$

5.2.2.1 Optimization for a fixed transconductance

The overall transconductance of the first stage of the LNA can be derived as [71]

$$G_m = \frac{3\rho\left(1+\frac{\rho}{2}\right)}{2R_s \omega_o L (1+\rho)^2} \tag{5-11}$$

In [76]

$$Q_{opt,G_m} = \sqrt{1 + \frac{5\gamma}{\delta\alpha^2} - 2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}} \tag{5-12}$$

the noise factor reaches a minimum.

$$F_{\min,optG_m} = 1 + \left(\frac{\omega_o}{\omega_T}\right)\left(\frac{2\delta\alpha}{5}\right)\sqrt{1 + \frac{5\gamma}{\delta\alpha^2} - 2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}} \tag{5-13}$$

But the popular derivation for the noise figure in [71] is incorrect.

5.2.2.2 Optimization for a fixed DC power dissipation

It is proved that at [76]

$$Q_{opt,P_d} = \sqrt{\frac{15\gamma}{\delta}}\sqrt{1+\frac{\delta}{5\gamma}-2|c|\sqrt{\frac{\delta}{5\gamma}}} \tag{5-14}$$

and the noise factor reaches a minimum as given in [76].

$$F_{\min,optP_d} = 1+\frac{\gamma}{\delta}\frac{\omega_o}{\omega_T}\left(\frac{1+3\alpha^2+\frac{4\delta\alpha^2}{5\gamma}-2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}-6|c|\sqrt{\frac{\delta\alpha^4}{5\gamma}}}{\sqrt{3+\frac{15\gamma}{\delta}-30|c|\sqrt{\frac{\gamma}{5\delta}}}}\right) \tag{5-15}$$

The popular derivation for the noise figure in [71] is incorrect either.

Note that [71] is wrong and we can validate it by deriving the equations ourselves, please refer to reference [76].

The optimum Q is a constant for any DC power dissipation, the unique value for the device width corresponding to (5-14) is obtained.

$$W_{opt,\min F} = \frac{3}{2\omega_o R_s L C_{ox} Q_{opt,P_d}} \tag{5-16}$$

5.2.3 Source-degenerated CMOS LNA in on-chip implementation

In this part, we design an LNA using the CSM 0.18 μm CMOS technology with a 50-Ω input impedance, whose performance will be treated as a reference to our following study.

Fig. 5-3 shows the topology of the source-degenerated LNA at 5.8 GHz in our design. It should be noted that we focused on the comparison analysis among different design technologies, the performance of our designed LNA may not be the best compared with that of the other topologies in the same technology.

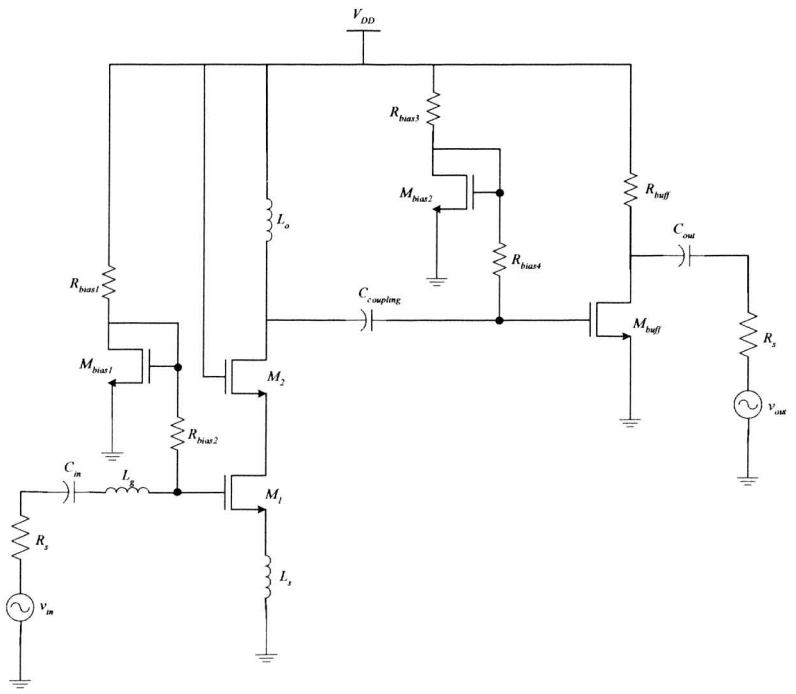


Fig. 5-3 Source-degenerated LNA circuitry

Using the power-constrained simultaneous noise and input matching technique, the design process for the key components of the LNA circuit can be calculated as follows. Since the size of the transistor will have the most significant effect on the circuit, the size of the transistor should be determined first. Using (5-14) and (5-16), we can obtain the device width for M_1. We choose the same width for M_2 at first; set the DC power dissipation P_d as

10 mW, then calculate the bias voltage V_{GS}, thus ω_T can be calculated, hence L_s using (5-4) and L_g using (5-3) can be obtained.

Finally, we fixe the parameters of the circuit components based on the above process and optimization. They are listed as below.

$W_1 = 300\ \mu m$; $W_2 = 210\ \mu m$; $W_{bias1} = 120\ \mu m$; $W_{bias2} = 120\ \mu m$.

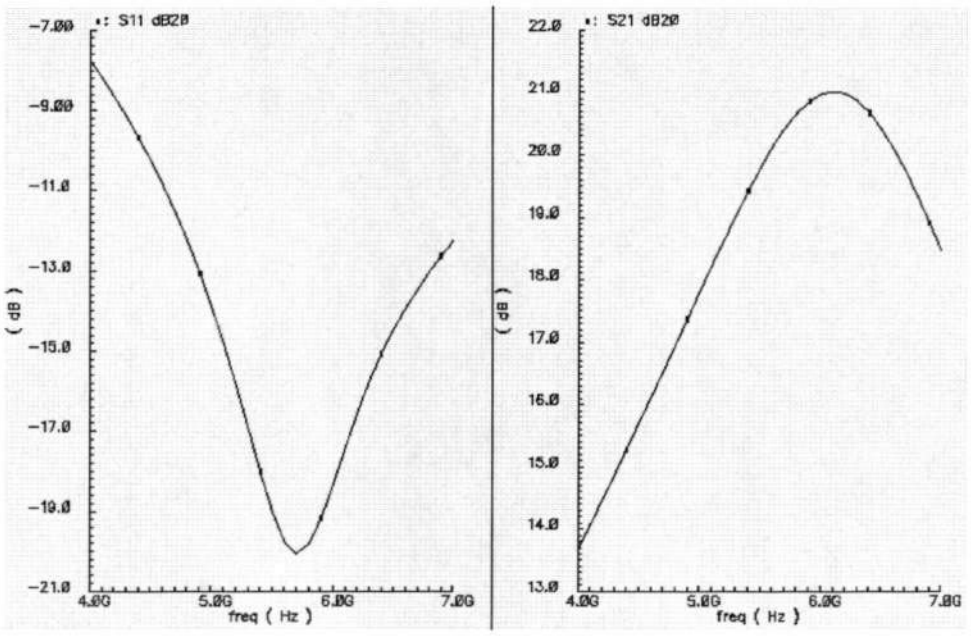
$R_{bias1} = 800\ \Omega$; $R_{bias2} = 500\ \Omega$; $R_{bias3} = 800\ \Omega$; $R_{bias4} = 500\ \Omega$.

$L_s = 0.34\ nH$; $L_g = 1.43\ nH$; $L_o = 2.39\ nH$.

$C_{in} = C_{coupling} = C_{out} = 0.5\ pF$.

$W_{buff} = 120\ \mu m$; $R_{buff} = 50\ \Omega$.

A 1.8 V supply voltage is used and the total DC power dissipation is 18.8 mW. The simulated voltage gain of the LNA is 20.7 dB, and the noise figure is 2.3 dB at 5.8 GHz. The input return loss is -19.8 dB at 5.8 GHz. Fig. 5-4 shows the S_{11} and S_{21} in dB and Fig. 5-5 shows the noise figure in dB, respectively. It should be noted that the LNA is an on-chip design; all passive components are integrated on the RF chip. Fig. 5-6 shows the layout of the designed LNA with bonding pads.



(a) (b)

Fig. 5-4 Simulated s-parameters for the on-chip LNA (a) S_{11}; (b) S_{21}

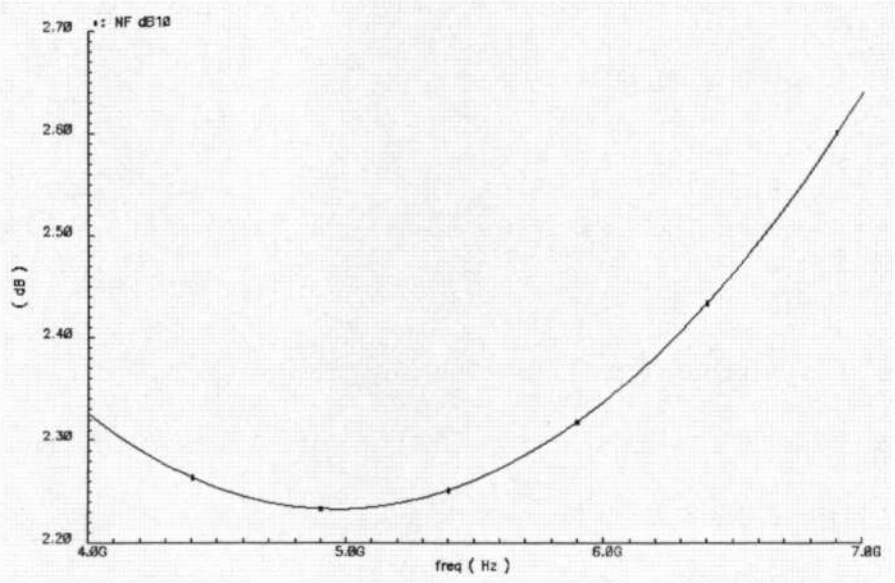


Fig. 5-5 Simulated noise figure for the on-chip LNA

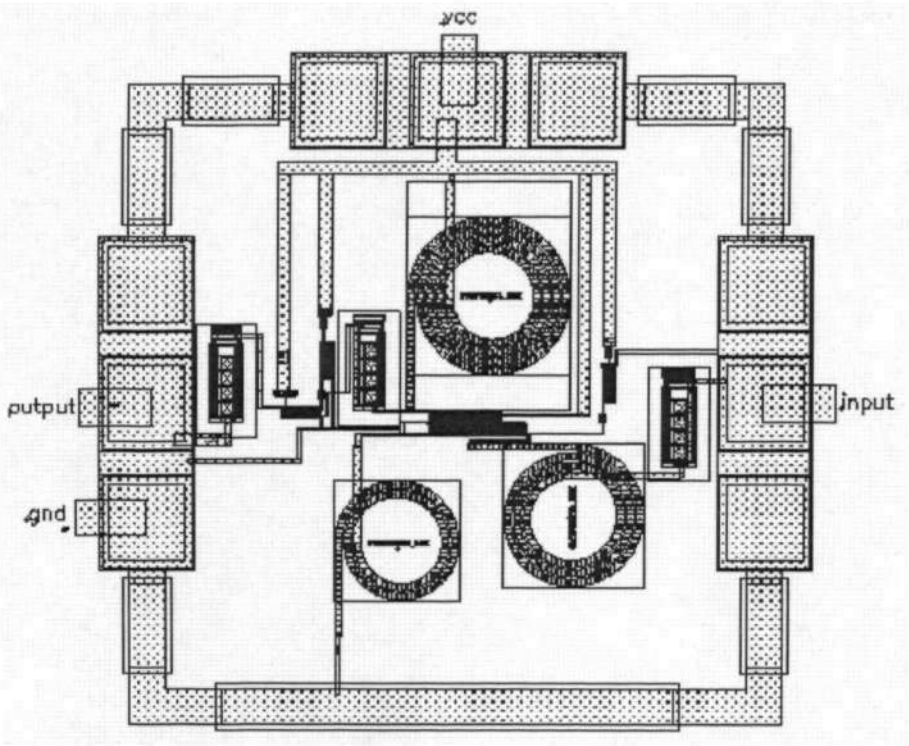
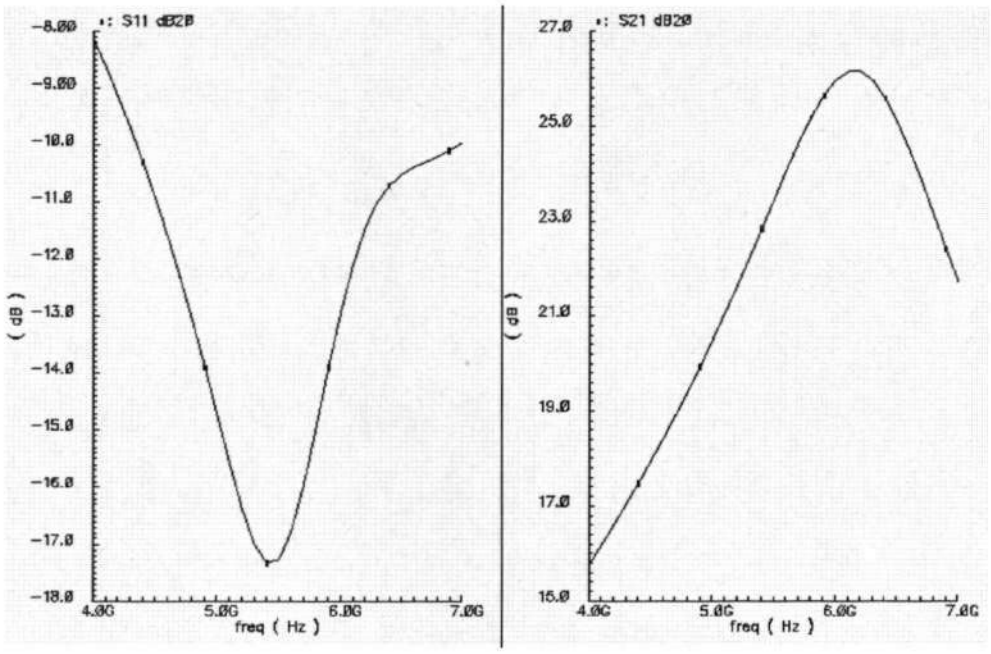


Fig. 5-6 Layout for the on-chip LNA

5.2.4 LNA in in-package implementation

With the development of SiP concept, we can move the inductors (L_g, L_s and L_o) of the LNA off the chip and into the package.

With the in-package inductors, the LNA achieves voltage gain of 25.2 dB, and noise figure of 2.0 dB at 5.8 GHz. The input return loss is -15 dB at 5.8 GHz. Fig. 5-7 shows the S_{11} and S_{21} in dB and Fig. 5-8 shows the noise figure in dB, respectively. The performance of the LNA is improved as expected when the inductors are moved off the chip and integrated with the package.



(a) (b)

Fig. 5-7 Simulated s-parameters for LNA using in-package architecture (a) S_{11}; (b) S_{21}

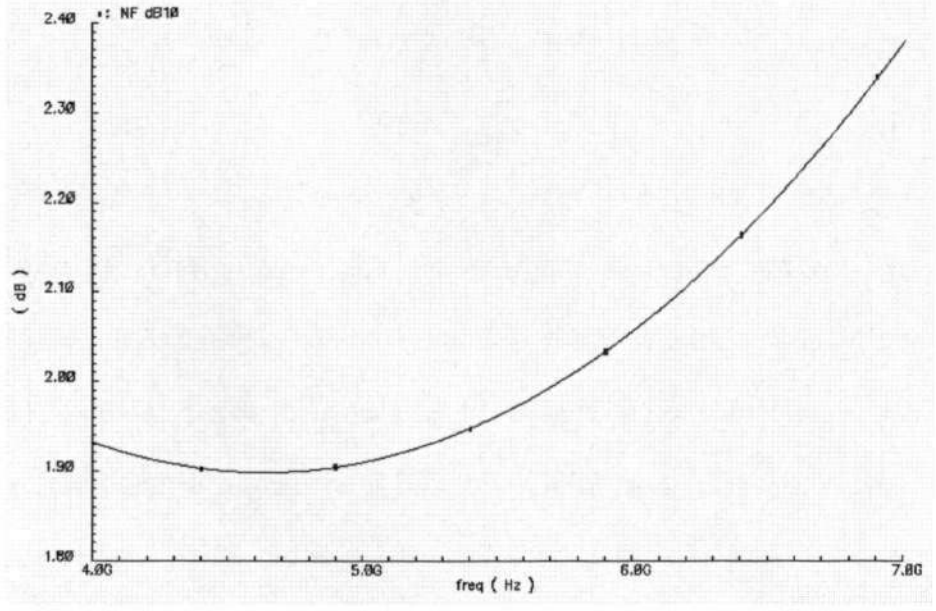


Fig. 5-8 Simulated noise figure for LNA using in-package architecture

5.3 New interface in antenna-chip codesign

The designs in this section will realize the concept of antenna-chip "codesign". It is well known that L_g and L_s are used to match the MOS transistor to obtain purely real input impedance, for instance 50-Ω, so as to connect the LNA with other components. By codesigning the antenna and the RF chip, presumably the removal of the troublesome inductors will improve the performance of the RF transceivers. We have stated in chapter three that we can calibrate the feeding location of the antenna to be inductive, therefore, the antenna can connect directly to the MOS transistors of the LNA.

5.3.1 Gate resistance and capacitance of RF MOSFET

Because in our design, the antenna connects directly with the gate of the MOSFET of the LNA, the resistance of the antenna should be the gate resistance R_G of the RF MOSFET, which is the sum of the gate electrode resistance and non quasi-static (NQS) distributed channel resistance; while the inductance of the antenna should be resonant with the RF MOSFET gate capacitance C_{gg} which includes the capacitive effects from the source, drain and substrate to the gate. The characterization of the gate resistance and capacitance of the RF MOSFET should be necessarily demonstrated here.

Although it is always possible to have a detailed equivalent circuit that accounts for all the physical elements of the RF MOS transistor, it is often too complex to be implemented as a compact model or a subcircuit for circuit simulation purposes. Moreover, many of the

component values are difficult or even impossible to extract and the subcircuit would contain too many internal nodes which significantly increases simulation time. A good compromise is obtained by simplifying the complete detailed equivalent circuit to the one expressed in Fig.5-9 [77, 78].

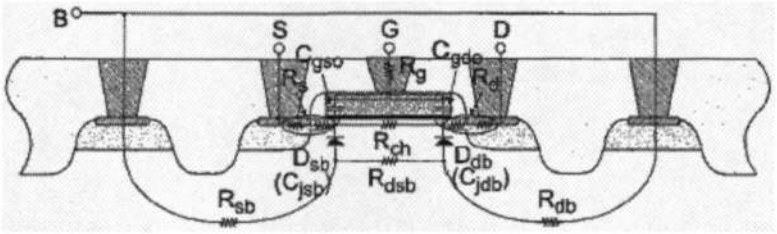
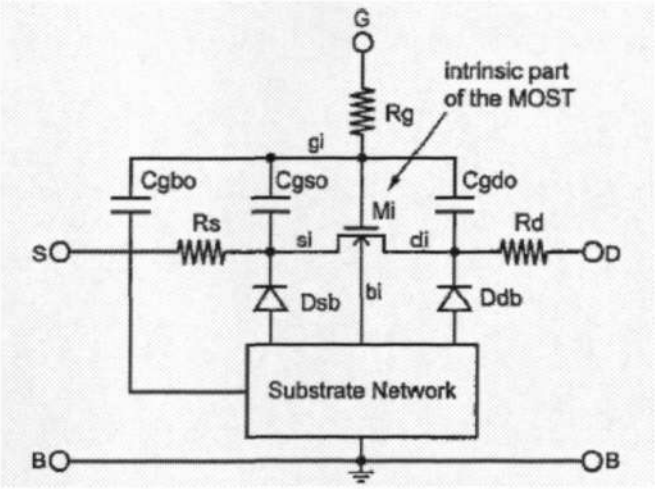


Fig. 5-9(a) MOS transistor cross section



(b)

Fig. 5-9(b) MOS transistor equivalent subcircuit

The gate resistance at DC and low frequency consists mainly of the polysilicon sheet resistance, at high frequency two effects will affect the effective gate resistance: one is gate-distributed effect (GDE), so the distributed gate electrode resistance R_g, and the other one is the non-quasistatic (NQS) effect in the channel, so the NQS distributed channel resistance R_{ch} seen from gate and is a function of both biases and geometry [79]. So $R_G = R_g + R_{ch}$.

No matter how R_g and R_{ch} are computed, the representative value of R_G is from 10-Ω to 20-Ω [80-83]. In spite of the various derivations for gate capacitance, C_{gg} typically ranges from 0.15 pF to 0.25 pF [78, 80].

5.3.2 Removal of L_g for 50-Ω interface

Here, we still design using the traditional 50-Ω interface, but now the L_g will be realized at the antenna, which means that we will design the antenna with an impedance of (R_s + sL_g) Ω, while the real inductor L_g will not exist. R_s can be a 50-Ω or non-50-Ω source resistance. In this section, R_s = 50 Ω. The bond wires, signal traces and vias supply some inductance included in the antenna part. For the calculation and equivalent circuit of the inductance and capacitance induced by these package components, we can refer to chapter three. Fig. 5-10 demonstrates that L_g is part of the antenna.

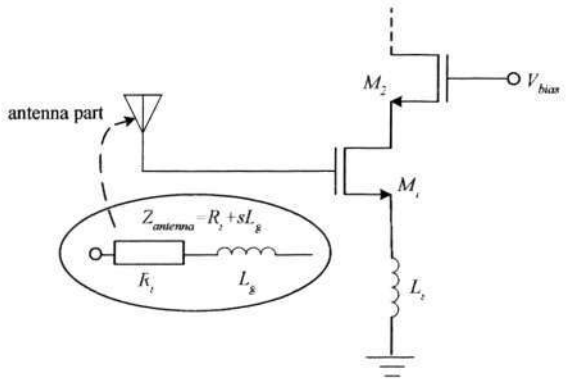
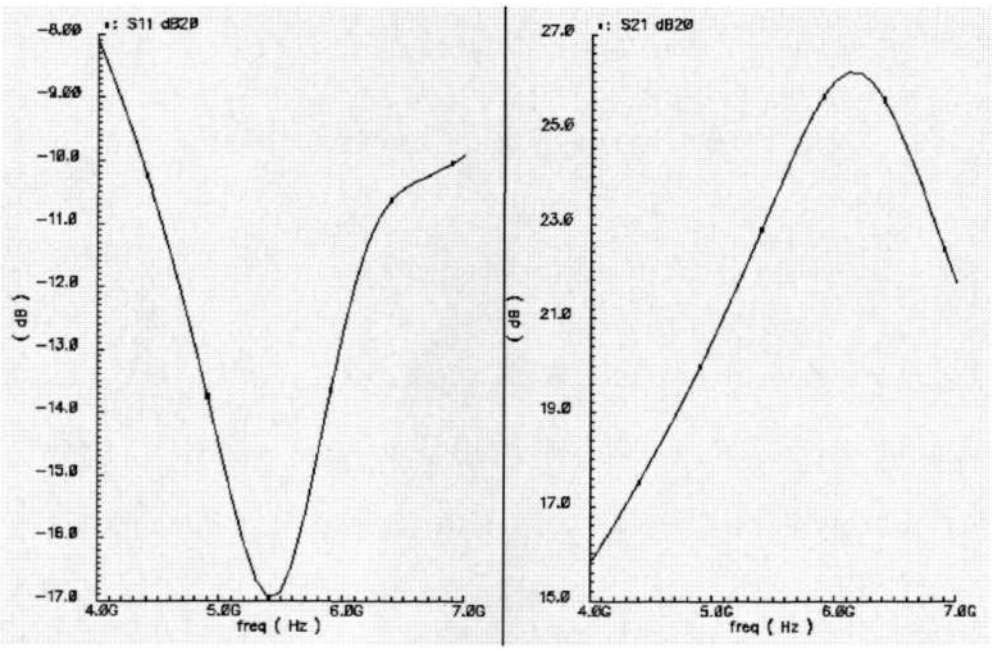


Fig. 5-10 Realizing the role of L_g into the antenna part

Keeping all the other parameters unchanged from the in-package implementation, this architecture achieves a voltage gain of 25.2 dB, and a noise figure of 1.9 dB at 5.8 GHz.

The input return loss of the LNA is -15 dB at 5.8 GHz. Fig. 5-11 shows S_{11} and S_{21} in dB and Fig. 5-12 shows the noise figure in dB, respectively.



(a) (b)

Fig. 5-11 Simulated s-parameters for codesigned LNA with 50-Ω interface (a) S_{11}; (b) S_{21}

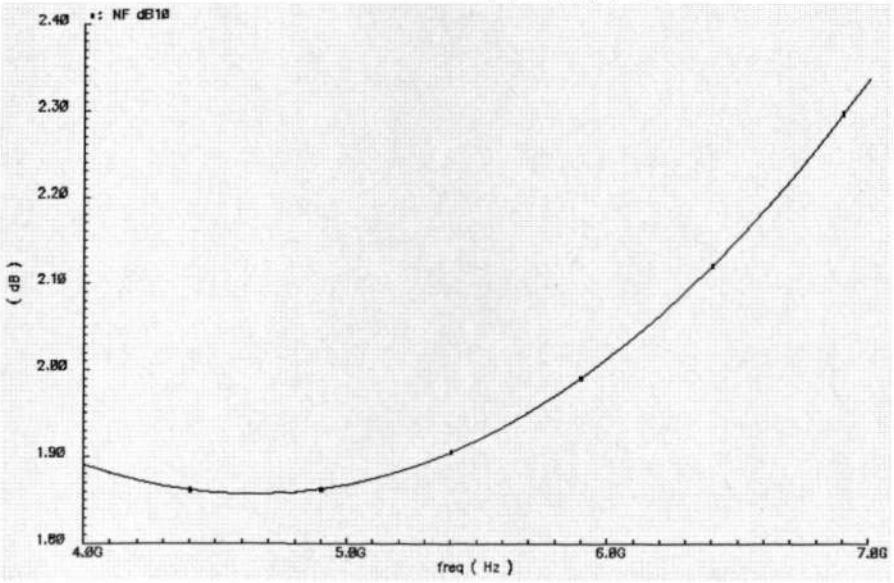
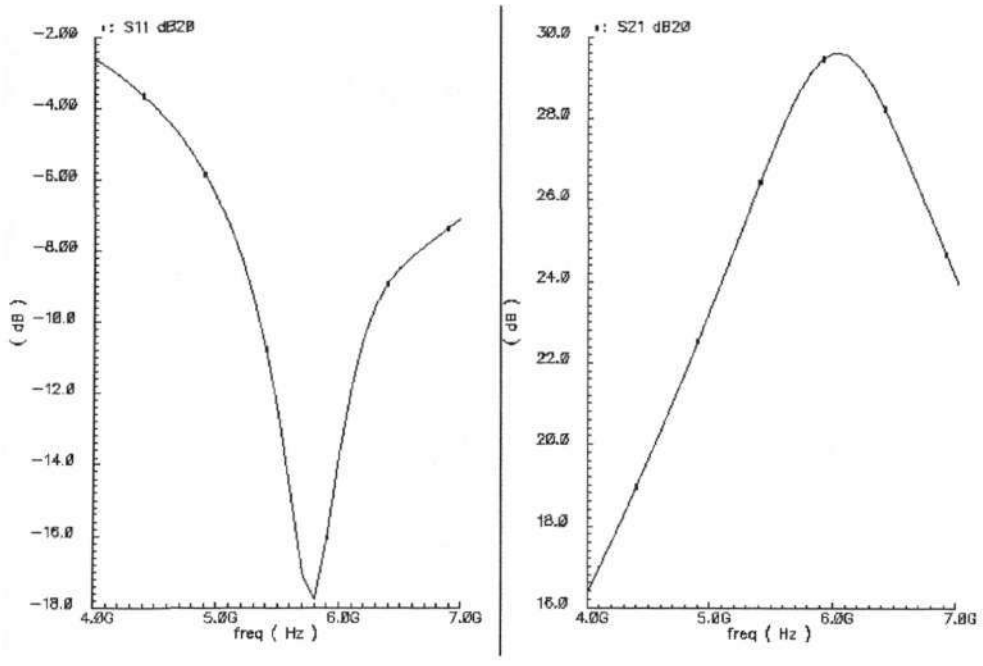


Fig. 5-12 Simulated noise figure for codesigned LNA with 50-Ω interface

5.3.3 Removal of L_g for non-50-Ω interface

In section 5.3.1, we have studied that the input impedance of the pure RF MOSFET is around $(R_G + \frac{1}{sC_{gg}})$ Ω. The antenna can be directly designed as $(R_G + sL_g)$ Ω. From Fig. 5-10, $R_s = R_G$, and $\omega_o^2 = \frac{1}{L_g C_{gg}}$. To be consistent with the previous section, we will not change the other parameters except the matching inductors L_g and L_s. This time L_g is 1.25 nH and L_s is 0.1 nH. The real part of the input impedance is set as 20-Ω.

The voltage gain of the LNA designed in this method is 29.1 dB, and the noise figure is 2.1 dB at 5.8 GHz. The input return loss is now -17.8 dB at 5.8 GHz. Fig. 5-13 shows S_{11} and S_{21} in dB. Fig. 5-14 shows the noise figure in dB.



(a) (b)

Fig. 5-13 Simulated s-parameters for codesigned LNA with non-50-Ω interface (a) S_{11}; (b) S_{21}

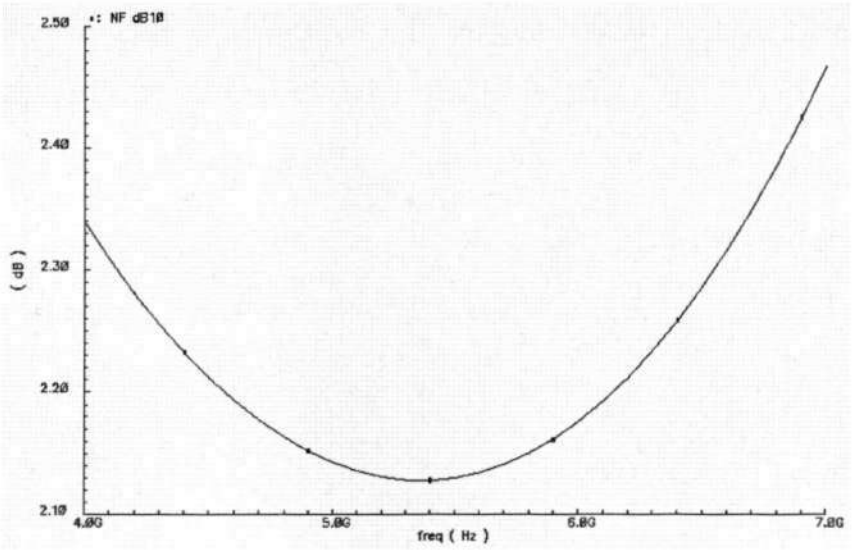


Fig. 5-14 Simulated s-parameters for codesigned LNA with non-50-Ω interface

5.3.4 Codesigned and optimized LNA in new interface implementation

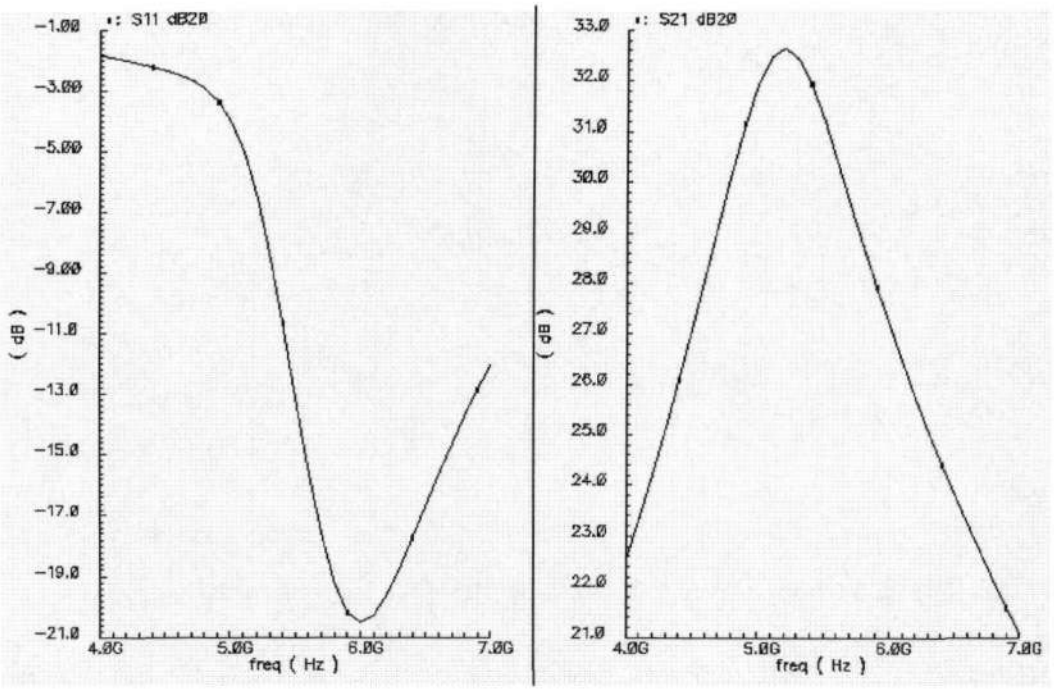
The above codesigned LNA may not be the optimized design considering the tradeoff between the gain and the noise figure. We redesigned an LNA by adjusting the sizes of the RF transistors and the values of the inductors. L_g is still realized at the antenna part. L_s and L_o keep the in-package implementation. The changed parameters are listed below.

$W_1 = 450\ \mu m;$ $W_2 = 360\ \mu m.$

$L_s = 0.05\ nH;$ $L_g = 0.75\ nH;$ $L_o = 2.6\ nH.$

The optimized LNA with antenna-chip codesign achieves the following performance. Due to the enlargement of the transistors' size, the power dissipation is 23.5 mW at supply voltage of 1.8 V. The voltage gain of the optimized antenna-chip codesigned LNA is 28.7

dB, and the noise figure is improved to 1.6 dB at 5.8 GHz. The input return loss is -19.2 dB at 5.8 GHz. Fig. 5-15 shows the S_{11} and S_{21} in dB and Fig. 5-16 shows the noise figure in dB, respectively.



(a) (b)

Fig. 5-15 Simulated s-parameters for codesigned LNA with optimization (a) S_{11}; (b) S_{21}

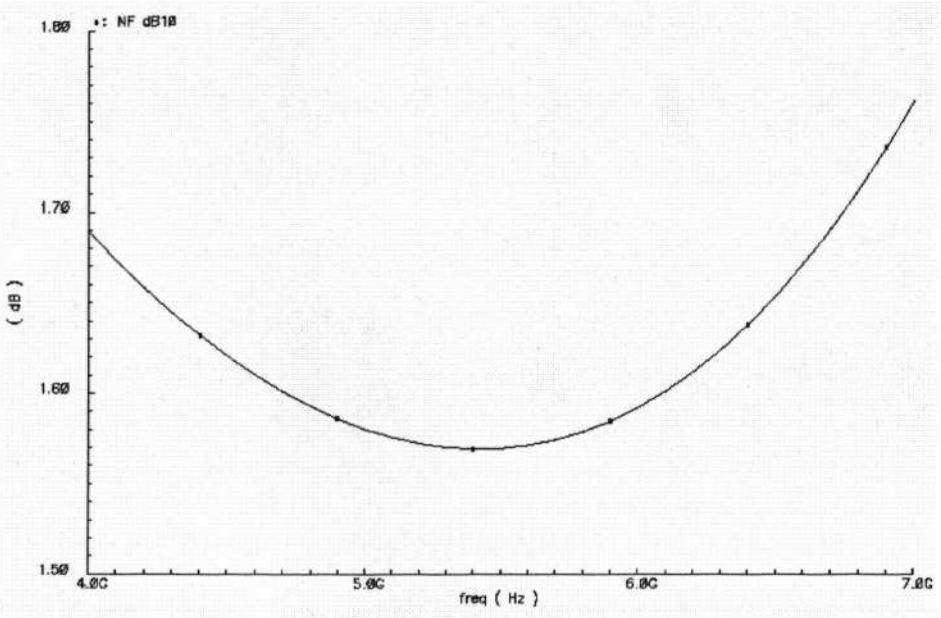


Fig. 5-16 Simulated noise figure for codesigned LNA with optimization

Table 5-I Comparison of the LNA performance

	On-chip LNA with 50-Ω interface	In-package LNA with 50-Ω interface	Codesigned LNA with 50-Ω interface	Codesigned LNA with non-50-Ω interface	Codesigned and optimized LNA
NF (dB)	2.3	2.0	1.9	2.1	1.6
Voltage gain (dB)	20.7	25.2	25.2	29.1	28.7
IIP3 (dB)	-25.6	-19.6	-20.2	-25.7	-30.7
1-dB compression Point(dB)	-18.9	-19.5	-55.7	-24.1	-24.7

Table 5-I lists the performance of the LNA designed by different technologies. The improvements and tradeoffs are expected. We have verified that in antenna-chip codesign technology, 50-Ω interface is not necessary. In the on-chip version of the LNA, the inductors are put on the chip together with the transistors. In the in-package version of the LNA, the inductors are put into the LTCC package substrate. In the antenna-chip codesign version we proposed, the large matching inductance is introduced by the antenna. Area and cost of the package are saved. Package interconnect components are fully utilized as elements of the interface for the RF receiver front-end, the real "codesign" has been implemented theoretically.

5.4 Summary of the chapter

This chapter has proposed a new interface for antenna-chip codesign through the performance demonstration of the single-ended LNA with different input impedance interface and different technologies. For the traditional on-chip LNA with 50-Ω input impedance which is designed in CSM 0.18 μm, the voltage gain is 20.7 dB and noise figure is 2.3 dB at 5.8 GHz. By integrating the critical inductors into the package and keep the other parameters unchanged, the voltage gain could improve to 25.2 dB and noise figure could decrease to 2.0 dB. While utilizing the antenna-chip codesign conception, we can completely eliminate the usage of the large matching inductors and 50-Ω interface. By deliberate design of an inductive antenna for connecting with the LNA, the voltage gain is

28.7 dB and noise figure is 1.6 dB at 5.8 GHz for the new scenario with less area and cost of the RF chip.

CHAPTER SIX

THEORY AND ANALYSIS OF DIFFERENTIALLY-DRIVEN ICPA

6.1 Theory and analysis of differentially-driven microstrip antennas

As introduced before, microstrip antennas have many unique and attractive properties – low in profile, light in weight, compact and conformable in structure, and easy to fabricate and to be integrated with solid-state devices. Microstrip antennas have found wide applications in radio systems with single-ended signal operation. Aforementioned chapters focused on the single-ended ICPA studies, in this chapter, differentially-driven antennas will be studied.

Recently, microstrip antennas have been used in radio systems with differential signal operation as well [25, 84-86]. For example, a differentially-driven microstrip antenna integrated with a push-pull power amplifier in Gallium Arsenide semiconductor technology is reported in [84]. The differentially-driven microstrip antenna acts also as an output balun, which makes the push-pull power amplifier more compact and efficient. A second differentially-driven microstrip antenna integrated with a push-pull power amplifier in complimentary metal oxide semiconductor technology is presented in [25]. The

differentially-driven microstrip antenna takes full advantages of the standard surface-mounted CBGA package; consequently, the system-level board space and the system-level assembly can be reduced and facilitated, respectively. A third differentially-driven microstrip antenna integrated with an oscillator including a buffer amplifier in Silicon Germanium semiconductor technology is proposed in [85]. The differentially-driven microstrip antenna introduces a virtual ground; accordingly, there is no need for connecting the ground of the solid-state devices and the ground plane of the antenna, the parasitic effect caused by interconnect is eliminated. Besides these differentially-driven microstrip antennas, a differential receiving microstrip antenna integrated with a differential LNA in Gallium Arsenide semiconductor technology is described in [86].

The differential receiving microstrip antenna acts also as an input balun, which offers a new possibility to build small, robust and cost-effective smart antenna arrays. The above works focus on integration with solid-state devices and indeed provide little information on the design of differential microstrip antennas. Furthermore, the state of the art single-chip and single-package solutions of radio systems call for differential antennas to reduce the bill of materials and to improve the receiver noise performance and transmitter power efficiency [52, 87].

In this chapter, the theory of microstrip antennas based on the cavity model is expanded to analyze the input impedance and radiation characteristics of the differentially-driven microstrip antennas. The gained physical insights from the theory then guide the integration of the differentially-driven microstrip antenna on the CBGA package into the differentially-driven ICPA. The integration emphasizes on the feeding and shielding of the

antenna from the transceiver. The differentially-driven microstrip antennas and ICPA were fabricated. Their performances were experimentally verified.

6.1.1 Theory of differentially-driven microstrip antennas

A microstrip antenna and a coordinate system are illustrated in Fig. 6-1.

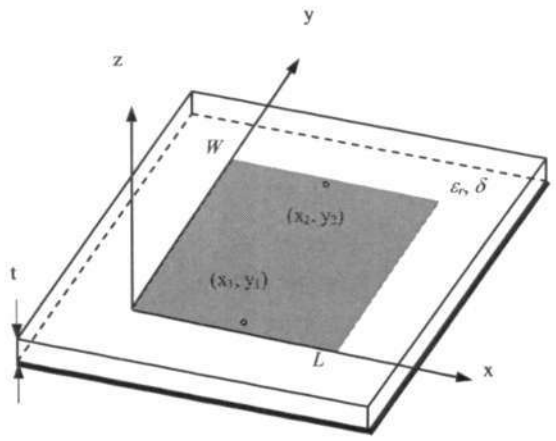


Fig. 6-1 A microstrip antenna and its coordinate system

The microstrip antenna that has dimensions L along x-axis and W along y-axis located on the surface of a grounded dielectric substrate with thickness H, dielectric constant ε_r, and dielectric loss tangent δ is differentially driven at points (x_1, y_1) and (x_2, y_2).

The differentially-driven microstrip antenna can be treated as a two-port network. With reference to the ground plane, the driving point at (x_1, y_1) is defined as port 1 and the driving point at (x_2, y_2) as port 2. The Z_{11} and Z_{22} refer to the input impedance for the port 1 and port 2 respectively, and Z_d refers to the differential input impedance for the differentially-driven microstrip antenna. The two ports relate to each other and form the

single port, for which Z_d was defined. Using the Z parameters for ports 1 and 2, one can express the differential voltage V_d as

$$V_d = V_1 - V_2 = (Z_{11} - Z_{21})I_1 - (Z_{22} - Z_{12})I_2 \tag{6-1}$$

where V_1 and V_2 are the driving point voltages and I_1 and I_2 are the driving point currents of ports 1 and 2, respectively. Since for the differentially-driven microstrip antenna,

$$I_1 = -I_2 = I \tag{6-2}$$

Equation (6-1) simplifies to

$$Z_d = \frac{V_d}{I} = 2(Z_{11} - Z_{21}) = 2(Z_{22} - Z_{12}) \tag{6-3}$$

where Z_d is the input impedance of the differentially-driven microstrip antenna. The Z parameters for the microstrip antenna shown in Fig. 6-1 can be calculated with the improved theory based on the cavity model as follows [88].

$$Z_{11} = j\omega\mu_o H \sum_{m,n=0}^{\infty} \frac{\phi_{mn}^2(x_1, y_1)\, j_o^2\left(\frac{m\pi d_e}{2L_{eff}}\right)}{k_{mn}^2 - k_e^2} \tag{6-4}$$

$$Z_{12} = j\omega\mu_o H \sum_{m,n=0}^{\infty} \frac{\phi_{mn}(x_1, y_1)\phi_{mn}(x_2, y_2)\, j_o^2\left(\frac{m\pi d_e}{2L_{eff}}\right)}{k_{mn}^2 - k_e^2} \tag{6-5}$$

where ω is angular frequency, μ_o is the permeability of vacuum, d_e is the effective width of a uniform strip of z directed source current of one amp,

$$k_e^2 = \varepsilon_r(1 - j\delta_e)k_o^2 \tag{6-6}$$

$$k_o = \omega / v \tag{6-7}$$

$$k_{mn}^2 = \left(m\pi / L_{eff}\right)^2 + \left(n\pi / W_{eff}\right)^2 \tag{6-8}$$

$$j_o(x) = \sin(x)/x \tag{6-9}$$

$$\phi_{mn}(x,y) = \sqrt{\varepsilon_{0m}\varepsilon_{0n}/L_{eff}W_{eff}}\cos(m\pi x/L_{eff})\cos(n\pi y/W_{eff}) \tag{6-10}$$

$\varepsilon_{0m} = 1$ for $m = 0$ and 2 for $m \neq 0$, m and n are the mode indices in the x and y directions, respectively, δ_e is the effective loss tangent, v is the speed of light, L_{eff} and W_{eff} are the effective dimensions, taking into account the fringing fields at the edges of the microstrip patch [53]. Similarly, Z_{21} and Z_{22} can be computed. L_{eff} may be approximated as follows.

$$L_{eff} = L + \left(\frac{W_{eq} - W}{2}\right)\frac{\varepsilon_{eff}(W) + 0.3}{\varepsilon_{eff}(W) - 0.258} \tag{3-38}$$

where $\varepsilon_{eff}(W)$ is the effective dielectric constant and W_{eq} is the equivalent width calculated from the planar waveguide model . $\varepsilon_{eff}(W)$ can be written as

$$\varepsilon_{eff}(W) = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 10\frac{H}{W}\right)^{-1/2} \tag{6-11}$$

and W_{eq} as

$$W_{eq} = \frac{120\pi H}{Za(W)\sqrt{\varepsilon_{eff}(W)}} \tag{3-39}$$

here $Za(W)$, the impedance of a microstrip line of width W and thickness H, is given by

$$Za(W) = \frac{60\pi}{\sqrt{\varepsilon_r}}\left\{\frac{W}{2H} + 0.441 + 0.082\left[\frac{\varepsilon_r - 1}{\varepsilon_r^2}\right] + \frac{(\varepsilon_r + 1)}{2\pi\varepsilon_r}\left[1.415 + Ln\left(\frac{W}{2H} + 0.94\right)\right]\right\}^{-1} \tag{6-12}$$

Similarly, W_{eff} can be calculated by replacing L, W_{eq}, W, $Za(W)$ and $\varepsilon_{eff}(W)$ in equations (6-11), (3-29) and (6-12) with W, L_{eq}, L, $Za(L)$ and $\varepsilon_{eff}(L)$, respectively.

Next, let's examine the radiation characteristics of the differentially-driven microstrip antenna. It is known that the radiation of the microstrip antenna originates from two slots

and each slot can be thought of as radiating the same field as a magnetic dipole with a magnetic current of

$$M = 2\hat{n} \times \hat{z} E_z \tag{6-13}$$

where the factor of 2 comes from the image of the magnetic current in the ground plane, $\hat{n}$ is the outward normal to the magnetic wall, $\hat{z}$ is the unit vector in the z-direction, and E_z is the z component of electric field in the cavity region. For the differentially-driven microstrip antenna, E_z can be written as

$$E_z = j\mu_o \sum_{m,n=0}^{\infty} I \frac{\phi_{mn}(x,y)}{k_e^2 - k_{mn}^2} j_o\left(\frac{m\pi d_e}{2L_{eff}}\right)\left[\begin{matrix}\phi_{mn}(x_1,y_1)\\ -\phi_{mn}(x_2,y_2)\end{matrix}\right] \tag{6-14}$$

where I is the source current of one amp in our calculation. Equation (6-14) reveals that the differentially-driven microstrip antenna introduces the cancellation mechanism, which can be explored to suppress some higher-order modes to reduce the cross polarization radiation. The electric vector potential of M is given by

$$F(r) = \frac{\varepsilon_o}{4\pi} \int \frac{M(r')}{|r - r'|} \exp\left(-jk_o|r - r'|\right) dl(r') \tag{6-15}$$

where ε_o is the permittivity of vacuum and integration is over the perimeter of the patch. The far field radiation components at a point $P(r, \theta, \phi)$ can be expressed as

$$E_\theta = j\omega\eta_o H\left(-F_x \sin\phi + F_y \cos\phi\right), \tag{6-16}$$

$$E_\phi = -j\omega\eta_o H\left(F_x \cos\theta\cos\phi + F_y \cos\theta\sin\phi\right) \tag{6-17}$$

where $\eta_o = 377\ \Omega$.

In the implementation of the improved cavity model, the determination of the effective loss tangent δ_e is critical. If the dielectric substrate is thin so that surface wave loss can be negligible, δ_e is given by

$$\delta_e = \frac{P_r}{2\omega W_e} + \delta + \frac{s}{H} \tag{6-18}$$

where P_r is power radiated by the space wave, W_e is electric energy stored in the cavity under the patch at resonance, and $s = 0.029\sqrt{\lambda_0 / \sigma}$ is the skin depth in the metal cladding with conductivity σ (with units of Siemens per meter). The power radiated by the space wave is

$$P_r = \frac{1}{2\eta_o}\int_0^{2\pi}\int_0^{\pi/2}\left(\left|E_\theta\right|^2 + \left|E_\phi\right|^2\right) r^2 \sin\theta d\theta d\phi \tag{6-19}$$

The stored electric energy is

$$W_e = \frac{\varepsilon_o \varepsilon_r}{4}\iiint_{cavity}\left|E_z\right|^2 dV \tag{6-20}$$

The calculation of δ_e in equation (6-18) requires an iterative procedure. It is found that the final value of δ_e is quite sensitive to the value chosen at the start of the iterative process [89]. We begin by setting $\delta_e = \delta_0$ instead of usual δ to shorten the iterative procedure. δ_0 is given by

$$\delta_0 = \frac{P_{r0}}{2\omega W_{e0}} + \delta + \frac{s}{H}. \tag{6-21}$$

where P_{r0} can be expressed as [90]

$$P_{r0} = \frac{V_d^2 A\pi^4}{20340}\left[(1-B)\left(1 - \frac{A}{15} + \frac{A^2}{420}\right) + \frac{B^2}{5}\left(2 - \frac{A}{7} + \frac{A^2}{189}\right)\right] \tag{6-22}$$

with $A=(\pi L/\lambda_0)^2$ and $B=(2W/\lambda_0)^2$. While working from the approximations indicated in [90], one obtains 40680 instead of 20340, there appears to be an algebraic error in [90]. W_{e0}, the electric energy stored for dominant mode at resonance, can be derived to be

$$W_{e0}=\frac{\varepsilon_0\varepsilon_r LWV_d^2}{8H}. \tag{6-23}$$

6.1.2 Validation of the theory for the differentially-driven microstrip antennas

Theoretical calculations, numerical simulations, and physical experiments were made for a differentially-driven microstrip antenna. The antenna was constructed using Taconic TLY-5 with a relative dielectric constant of 2.2 ± 0.02 and a loss tangent of approximately 0.0009. It had dimensions L = 17.2 mm, W =16.7 mm, and H = 0.635 mm. The substrate size is 25 × 25 mm^2. The antenna was driven differentially at both radiating edges at (x_1, y_1) = $(0.0054L, 0.5W)$ and $(x_2, y_2) = (0.9946L, 0.5W)$ to excite TM_{10} mode. Fig. 6-2 shows the fabricated microstrip antenna. This differentially-driven scheme was used in [25, 84]. The calculations of the antenna parameters were performed in Matlab, the simulations were executed using the HFSS, and the measurements were conducted with an HP 8510C network analyzer. The measured S parameters were converted to the differential input impedance by

$$Z_d=2Z_o\frac{(1-S_{11}^2+S_{21}^2-2S_{21})}{(1-S_{11})^2-S_{21}^2} \tag{6-24}$$

where Z_o is the reference impedance of 50 Ω.

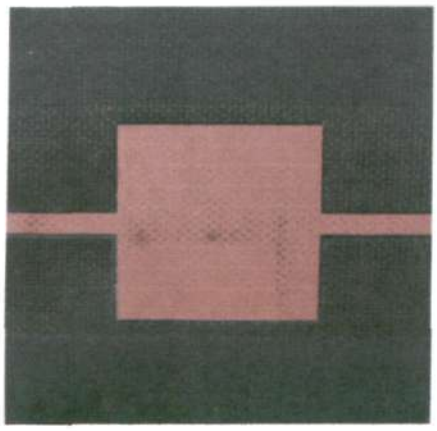


Fig. 6-2 Microstrip antenna driven at both radiating edges

Fig. 6-3 compares the calculated, simulated, and measured input impedance of the differentially-driven microstrip antenna. The impedance characteristics give insight on how the antenna must be modified to achieve a specified resonant frequency. Here the resonant frequency is defined as where the reactance of the input impedance is equal to zero. According to this definition, one can see that both calculated and simulated resonant frequencies are at 5.77 GHz and the measured resonant frequency is at 5.74 GHz. One also can see that the agreement between the calculated and simulated input impedance is excellent. The agreement between theory and experiment is in general acceptable. The discrepancy is likely due to the fabrication tolerance and the experimental error of our measuring system. It was found that any small phase difference in measured S_{11} and S_{21} would cause a large error in the measured Z_d.

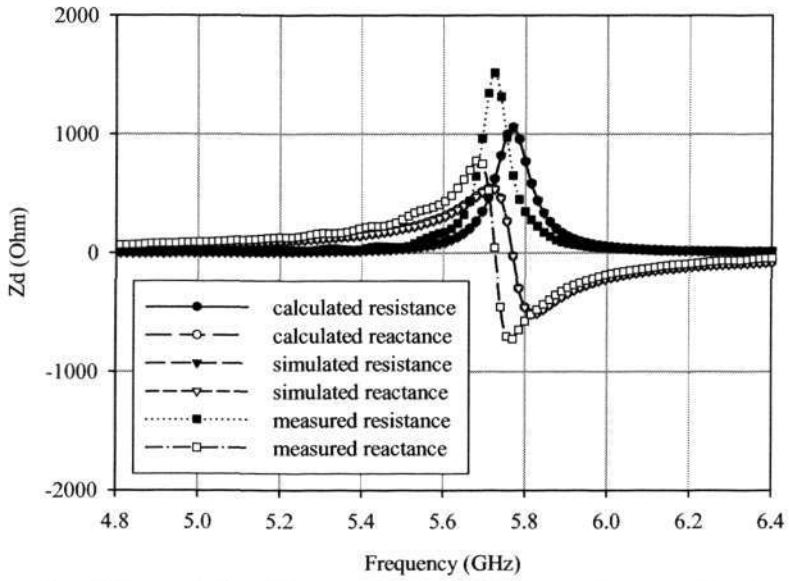


Fig. 6-3 Z_d for the differentially-driven microstrip antenna driven at both radiating edges

Fig. 6-4 compares the calculated, simulated, and measured co-polar radiation patterns of the differentially-driven microstrip antenna at 5.75 GHz. The comparison shows that excellent agreement is obtained between the theory, simulation, and experiment in the broadside direction of the forward region. The difference in the side lobe region is because the radiation pattern is calculated for an infinite ground plane while the simulation and experiment are performed on a finite ground plane. We do not compare the cross-polar radiation patterns because the cross-polar radiation is quite weak and hard to measure accurately due to the cancellation mechanism introduced by the differentially-driven technique.

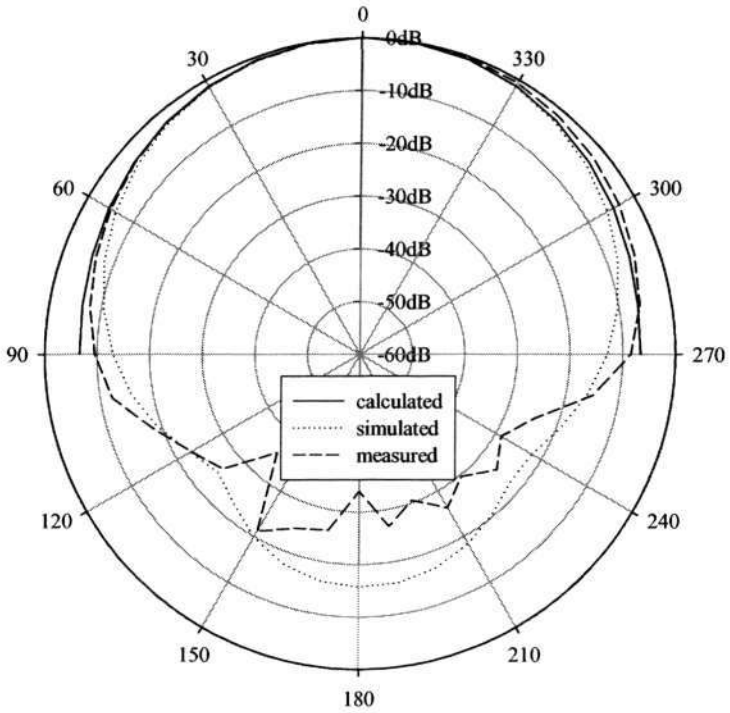


Fig. 6-4(a) Co-polar radiation patterns in E-plane for differentially-driven microstrip antenna driven at both radiating edges

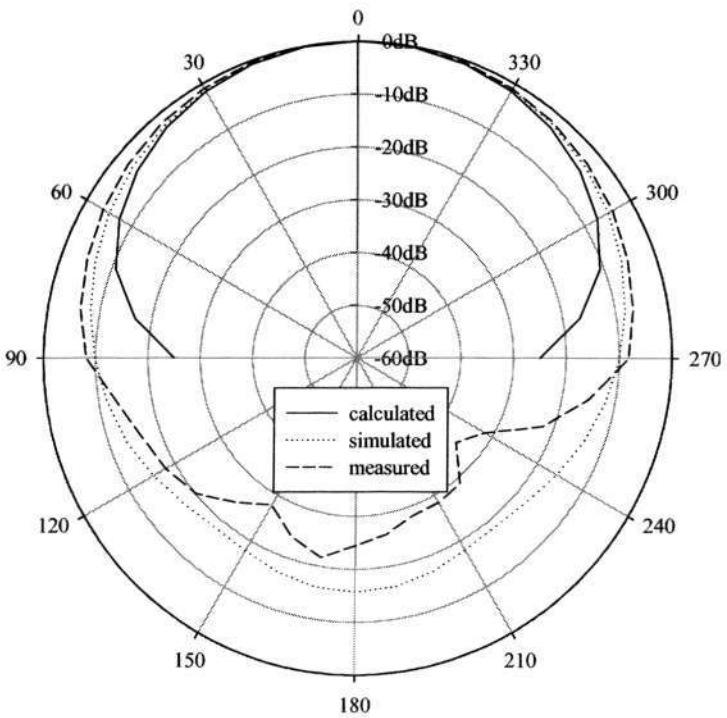


Fig. 6-4(b) Co-polar radiation patterns in H-plane for differentially-driven microstrip antenna driven at both radiating edges

Fig. 6-5 shows the calculated radiation patterns of the microstrip antenna driven for differential and single-ended operations at 5.75 GHz. It is evident from the figure that the cross-polar radiation from the differentially-driven microstrip antenna is weaker than that of the single-ended microstrip antenna.

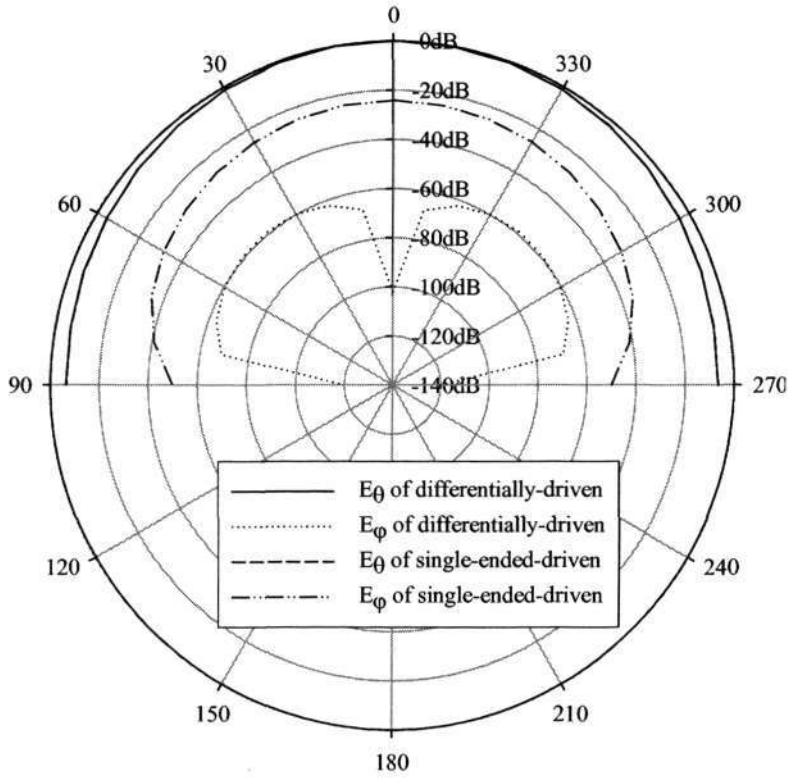


Fig. 6-5(a) Radiation patterns in E-plane for differentially-driven and single-ended microstrip antenna

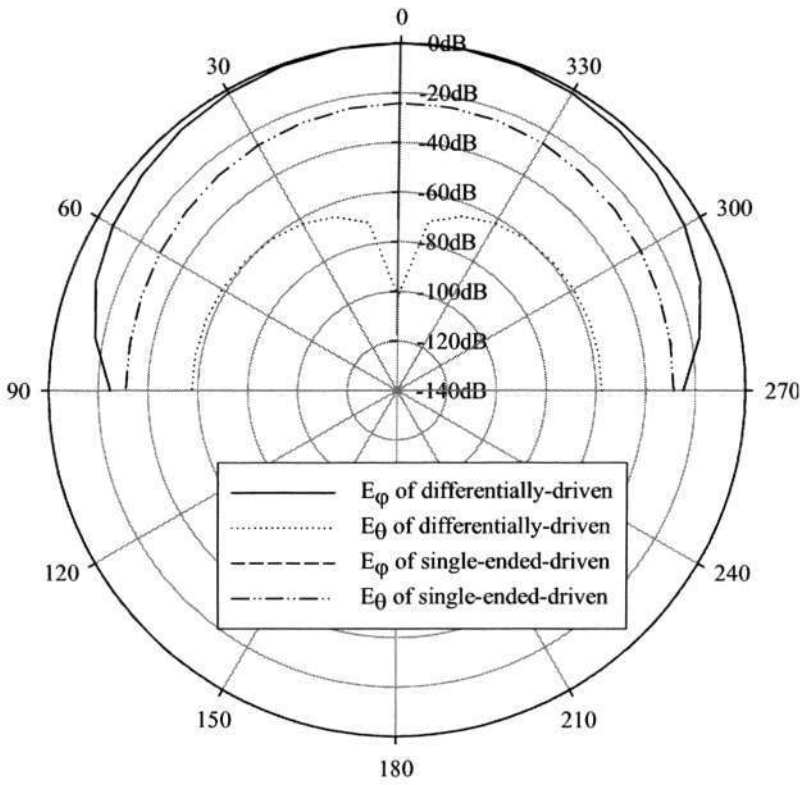


Fig. 6-5(b) Radiation patterns in H-plane for differentially-driven and single-ended microstrip antenna

For the differentially-driven microstrip antenna, there are two feeds. The isolation between them is guaranteed by the virtual ground in the middle of the patch, which we will give detailed illustration in the analysis of the differentially-driven ICPA.

6.1.3 Theoretical analysis of the differentially-driven microstrip antennas

Having validated the theory, we now proceed to apply it to analyze the microstrip antenna to gain deep insight into its differential operation in this section.

First, consider the differentially-driven points at one radiating edge: $(x_1, y_1) = (0.0054L, 0.0056W)$ and $(x_2, y_2) = (0.0054L, 0.9944W)$ to excite the TM_{01} mode. This differentially-driven scheme was used in [85]. Fig. 6-6 shows the fabricated microstrip antenna for this driven scheme.

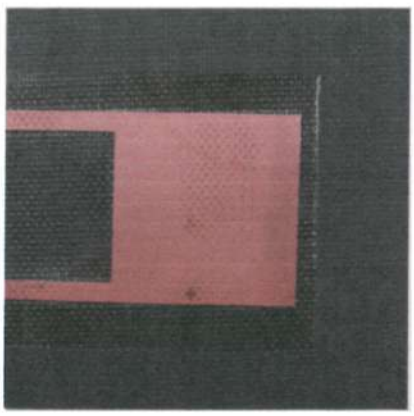


Fig . 6-6 Microstrip antenna driven at one radiating edge

Fig. 6-7 shows the calculated and simulated input impedance of the differentially-driven microstrip antenna. It is evident from the figure that the microstrip antenna resonates at 5.8 GHz and excellent agreement is obtained between the theory and simulation. Fig. 6-8 illustrates the calculated and simulated co-polar radiation patterns of the differentially-driven microstrip antenna at 5.75 GHz. Once again, the cross-polar radiation is negligible.

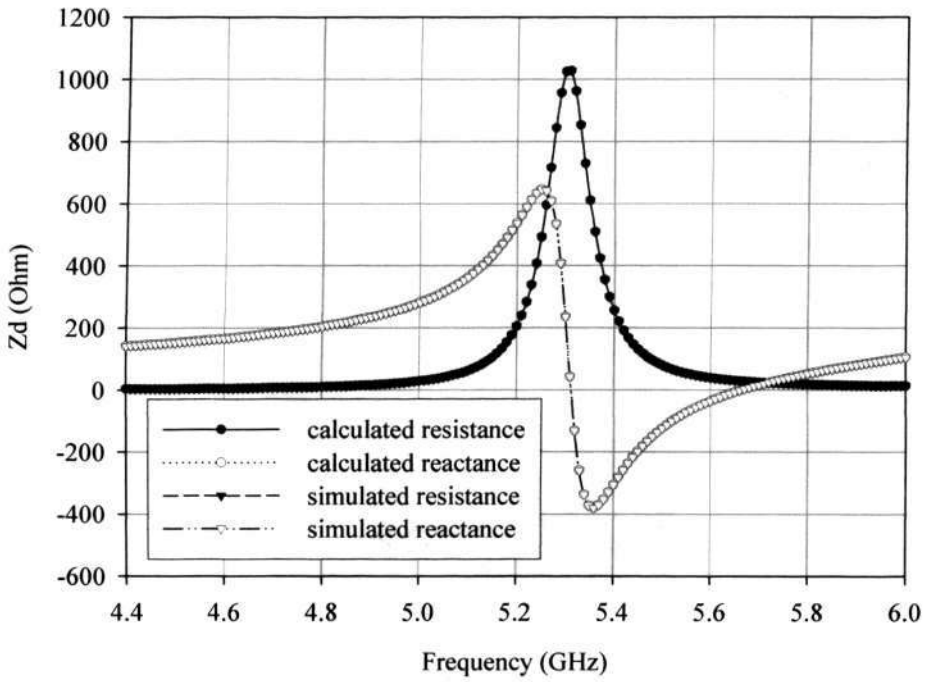


Fig. 6-7 Z_d for differentially-driven microstrip antenna driven at one radiating edge

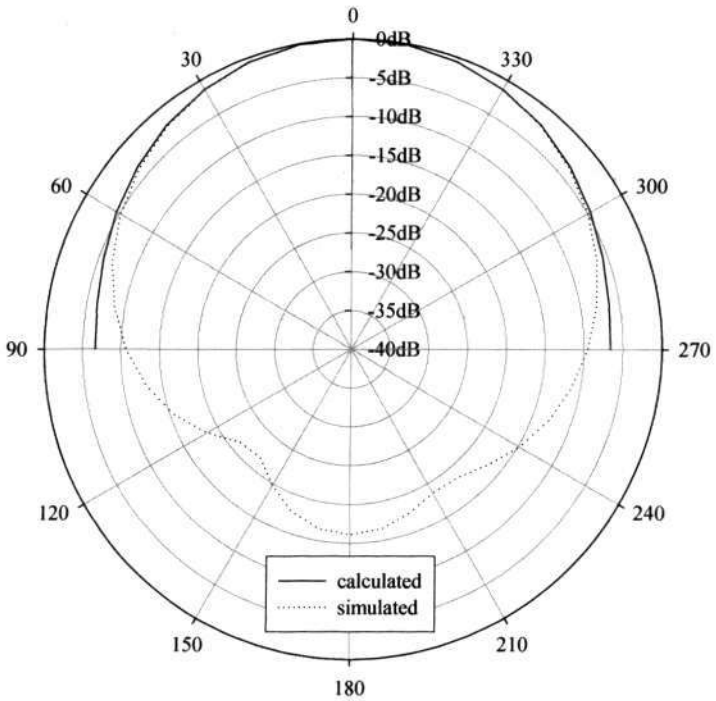


Fig. 6-8(a) Co-polar radiation patterns in E-plane for differentially-driven microstrip antenna driven at one radiating edge

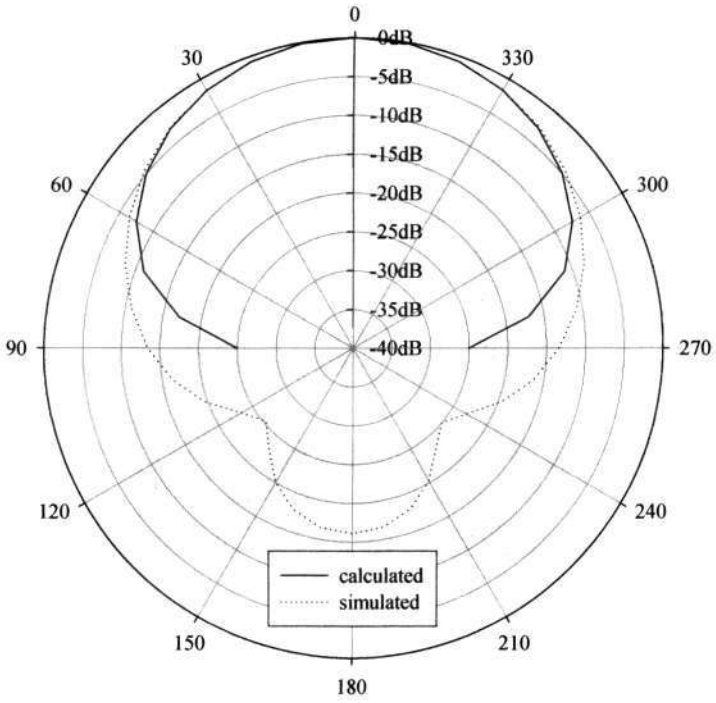


Fig. 6-8(b) Co-polar radiation patterns in H-plane for differentially-driven microstrip antenna driven at one radiating edge

Secondly, consider the differentially-driven points at $(x_1, y_1) = (0.0054L, 0.0056W)$ and $(x_2, y_2) = (0.9946L, 0.9944W)$ to excite both TM_{10} and TM_{01} modes to realize circular polarization. This differentially-driven scheme has never been used. Fig. 6-9 shows the fabricated antenna for this driven scheme. Fig. 6-10 shows the calculated and simulated input impedance of the differentially-driven microstrip antenna. It is evident from the figure that the microstrip antenna resonates at 5.67 GHz of the TM_{10} mode and 5.8 GHz of the TM_{01} mode and excellent agreement is obtained between the theory and simulation. Left-Hand circular polarization (LHCP) occurs at 5.75 GHz. Fig. 6-11 illustrates the calculated and simulated co-polar radiation patterns of the differentially-driven microstrip antenna at 5.75 GHz. It should be pointed out that for this case the radiation level of the

cross-polar component is the same as that of the co-polar component. It is found that the 3-dB axial ratio bandwidth is 0.96%.

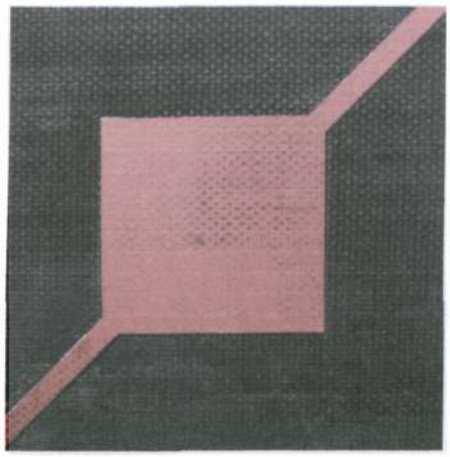


Fig . 6-9 Microstrip antenna driven for circular polarization

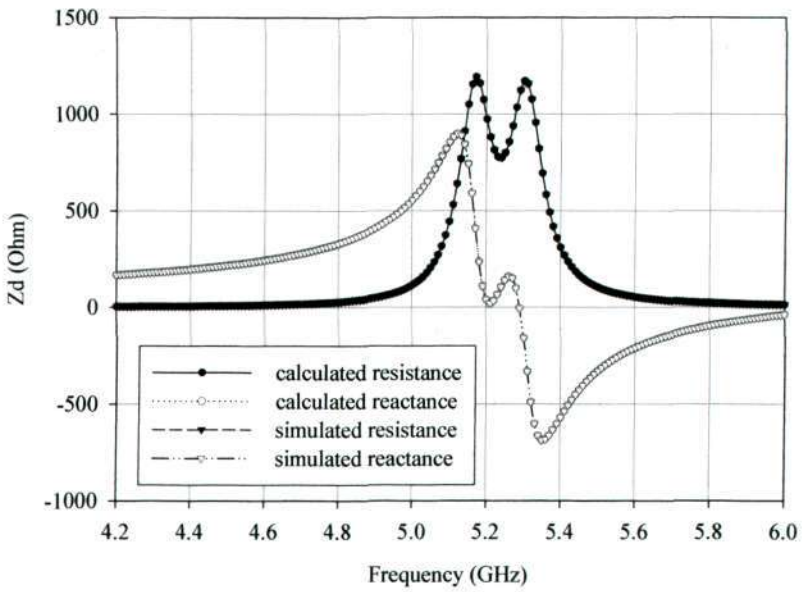


Fig. 6-10 Z_d for differentially-driven microstrip antenna driven for circular polarization

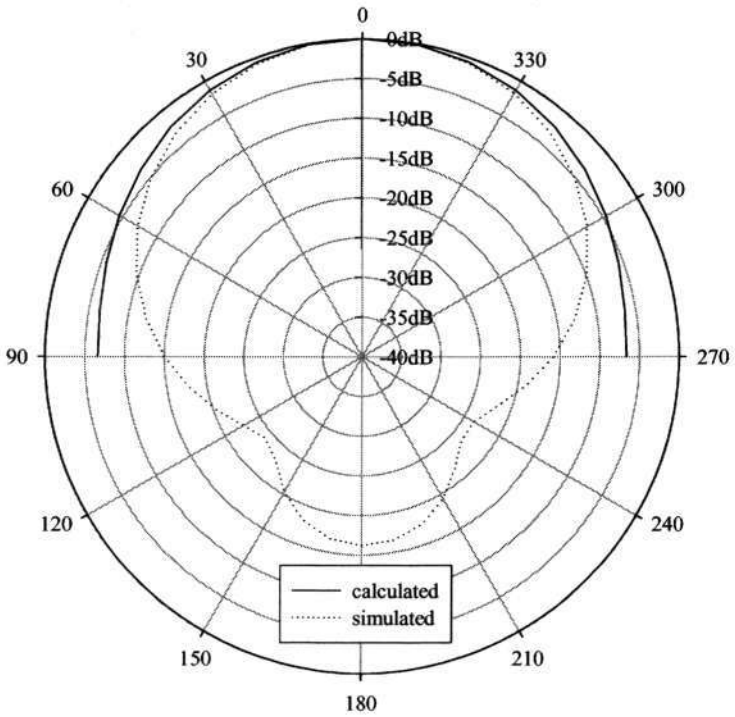


Fig. 6-11(a) Co-polar radiation patterns in E-plane for differentially-driven microstrip antenna driven for circular polarization

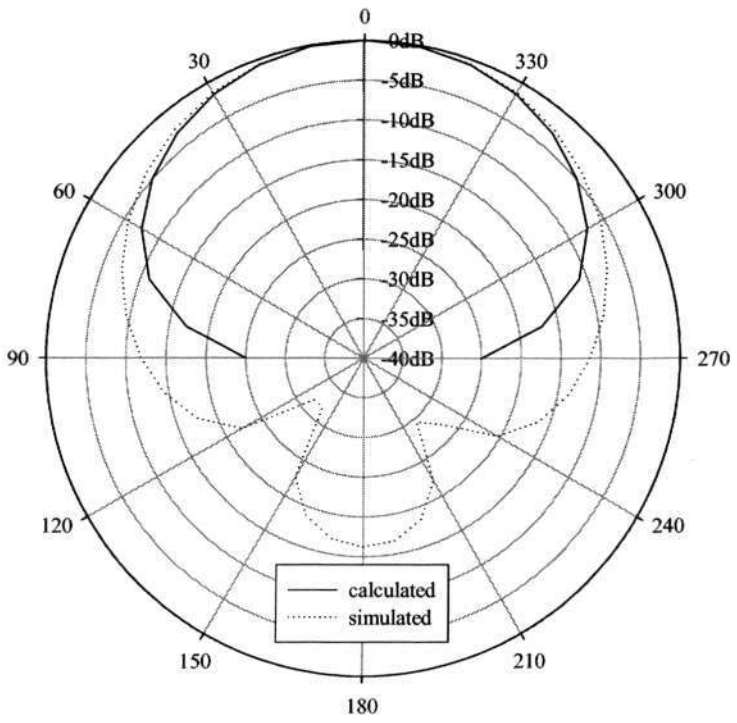


Fig. 6-11(b) Co-polar radiation patterns in H-plane for differentially-driven microstrip antenna driven for circular polarization

As in microstrip antennas for single-ended signal operation and shown in the above three driven cases, the radiation patterns of differentially-driven microstrip antennas are not sensitive to the locations of the driven points. However, the physical symmetry of the locations of the driven points should be maintained for better differential performance.

Finally, we analyze the differential resonant resistance as a function of ξ/λ_o for the above three differentially-driven schemes to excite the TM_{10}, TM_{01}, and both TM_{10} and TM_{01} modes, respectively. ξ is the seperation between the two feeds, and λ_o is the free space wavelength of the microstrip antenna. The resonant resistance for the single-ended signal operation is included for comparison. For single-ended operation, the microstrip antenna is fed at (x_1, y_1), ξ is calculated with respect to a virtual feed located at (x_2, y_2). Fig. 6-12 shows the resonant resistance for the first scheme to excite the TM_{10} mode. It is seen that the resonant resistance increases with ξ/λ_o and the differential resonant resistance is larger than the single-ended one. It is found that when ξ/λ_o is smaller than 0.1, no resonance for differential operation will occur any more, the differential input impedance is inductive. Fig. 6-13 shows the resonant resistance for the second scheme to excite the TM_{01} mode. Similarly, the resonant resistance increases with ξ/λ_o and the differential resonant resistance is also larger than the single-ended resonant resistance. Fig. 6-14 shows the resonant resistance for the third scheme to excite both the TM_{10} and the TM_{01} modes for circular polarization. As can be seen from the figure, the resonant resistance increases with ξ/λ_o and the differential resonant resistance is larger than the single-ended one. It is also found that when ξ/λ_o is smaller than 0.1, no resonance for differential operation will occur any more, the differential input impedance is inductive. The dependence of resonance for

the differentially-driven microstrip antennas on the separation of the dual feeds can be explained as follows. When the dual feeds are located near to each other $\xi/\lambda_o < 0.1$, the differential signal applied to the dual feeds cancels, hence the resonance does not occur and the feeds themselves make the differential input impedance exhibit inductive.

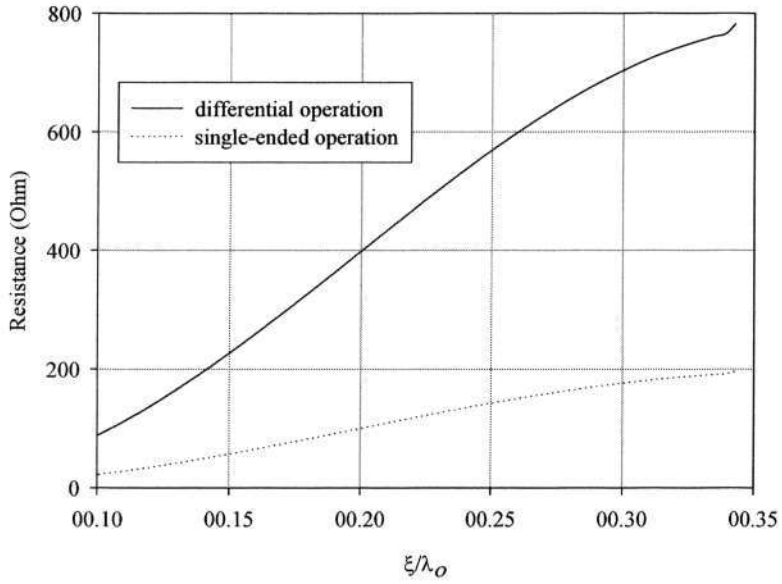


Fig. 6-12 Resonant resistance for the first scheme

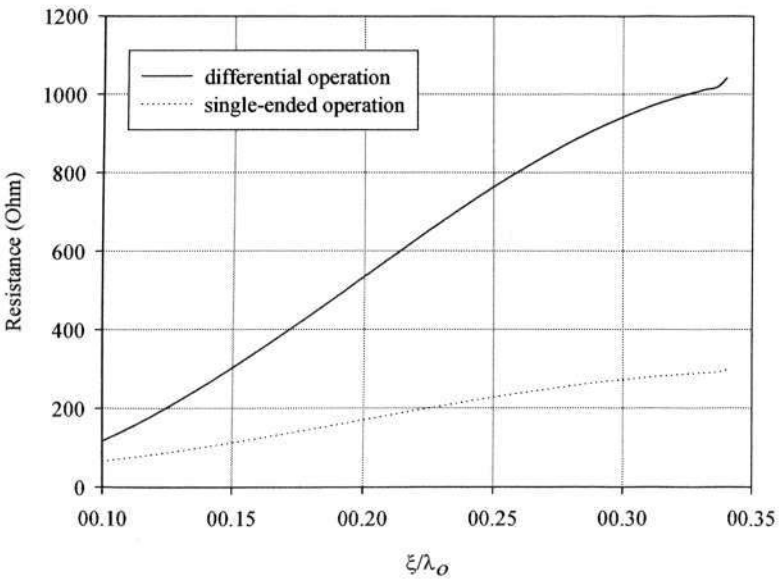


Fig. 6-13 Resonant resistance for the second scheme

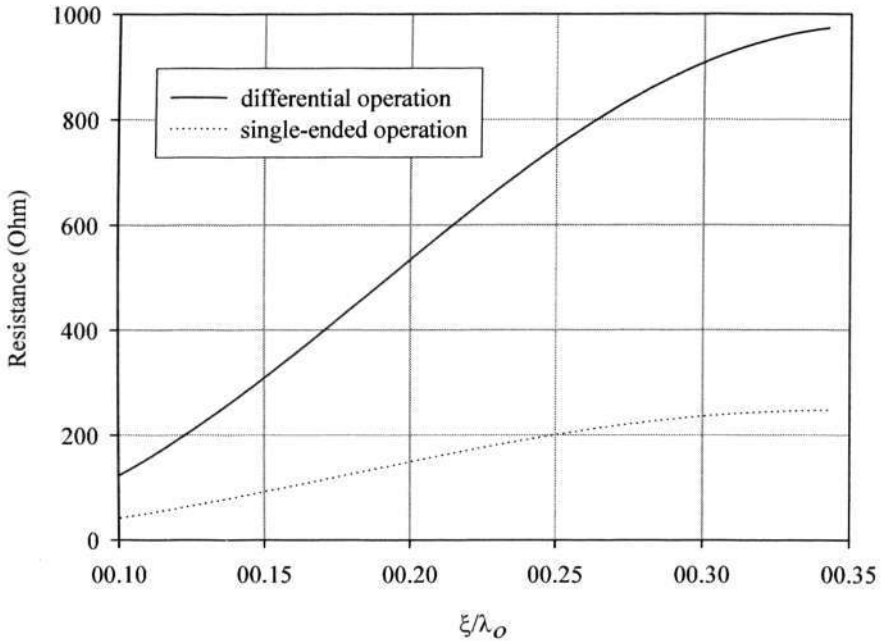


Fig. 6-14 Resonant resistance for the third scheme

6.2 Theory and analysis of differentially-driven ICPA

As in the aforementioned chapters, single-chip RF transceivers in CMOS technology for wireless LAN applications at 5-GHz bands have been successfully demonstrated. Single-chip RF transceivers have the benefit of cost reduction and system reliability and therefore represent the trend of implementing radio systems. Fig. 6-15 shows a simplified architecture from current designs of single-chip RF transceivers in CMOS technology [71, 91-92]. Note that the direct conversion architecture is adopted to circumvent the difficulty of the integration of different high-Q analog bandpass filters in CMOS technology. Also note that a fully differential signal path is employed to reduce local oscillator feedthrough

and leakage and to achieve higher linearity, lower offset and better immunity to common-mode noise due to power supply variations or substrate coupling. Further note that off-chip components such as one antenna, one T/R switch, and two baluns are required to construct a functional RF transceiver.

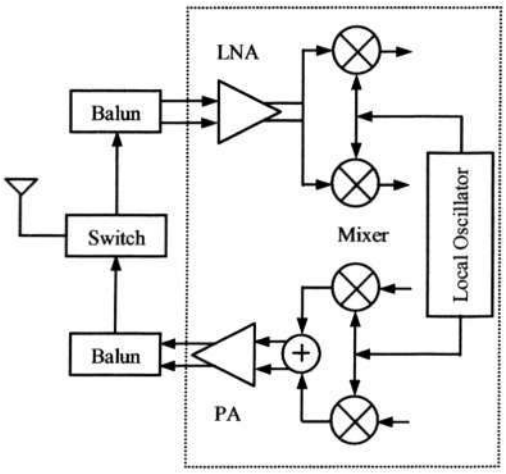


Fig. 6-15 Simplified architecture of single-chip RF transceivers

The antenna appears currently impossible to be integrated into a single-chip RF transceiver for efficient radiation. Consequently, it is left external to the single chip (or chips) in virtually all solutions of highly integrated radio systems. A T/R switch is another key component of the RF transceiver. The T/R switch connects the antenna to the receiver and transmitter alternatively following the command of time domain depluxing. The T/R switch can be easily integrated into the single-chip RF transceiver because it only needs a few transistors and resistors. For example, the world first differential T/R switch in 0.18-μm CMOS technology uses six transistors and four resistors. It has proven feasible for differential signal operation up to 6 GHz [93]. With the differential T/R switch and the differential antenna to be proposed in this work, one can avoid using baluns as shown in

Fig. 6-15. This will not only translate into the reduction of material cost but also the improvement of the receiver noise performance and transmitter power efficiency.

The results in [22-24] on the ICPA show: (1) the cavity-up package makes the shielding between the radiator and the RF transceiver chip complicated; (2) the unbalanced radiator for single-ended signal operation deviates from the mainstream of single-chip RF transceivers where differential signal operation is preferred. Here we present an ICPA in a cavity-down package format to facilitate the shielding issue and choose a balanced radiator for differential signal operation.

6.2.1 Design of the differentially-driven ICPA

The design of the ICPA must consider its fabrication in large quantity, which requires novel manufacturing technologies. The LTCC technology that uses noble metals and specific ceramic materials and has the flexibility in realizing an arbitrary number of metallic and ceramic layers, is suitable for the mass production of the ICPA. There are a few LTCC material systems in the market. The LTCC material system from Dupont is used in this demonstration. The physical design rules recommended by Dupont are obeyed [94]. The Dupont 951-AX ceramic type has a dielectric constant of 7.8 and a loss tangent of 0.002 at 5 GHz. Two metallization options are available: silver and gold, of which silver metallization is chosen for the ICPA implementation. The design of the ICPA must also consider the package of the single-chip RF transceiver die and the automatic assembly of the ICPA to the printed circuit board. In this regard, the ICPA should be designed as the JEDEC standard compliant. The ICPA has a standard body size 15 x 15 mm^2 and 48

signal traces and solder balls with a pitch of 0.48 mm. The ICPA holds the stepped cavity that is large enough to accommodate a single-chip RF transceiver die of current size. Fig. 6-16 shows the differentially-driven ICPA.

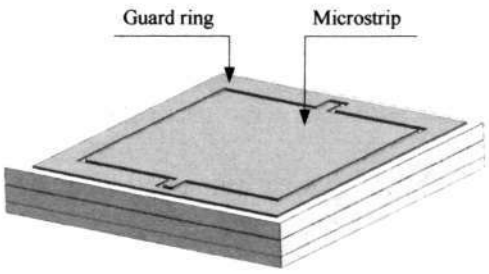


Fig. 6-16(a) Top view of the differentially-driven ICPA

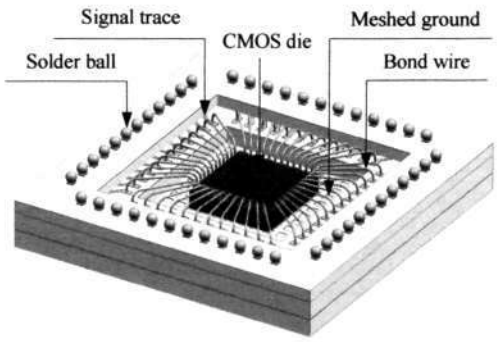


Fig. 6-16(b) Bottom view of the differentially-driven ICPA

Using the theory described in section 6.1.1, we studied a microstrip antenna in Dupont design rule, which has L = 10.04 mm and W = 10.176 mm, H = 0.8 mm, d = 0.2 mm. First, we analyze the microstrip antenna differentially driven at both radiating edges: $(x_1, y_1) = (\Delta, 0.5W)$ and $(x_2, y_2) = (L - \Delta, 0.5W)$ where Δ = 0.1 mm. Fig. 6-17 shows the numerical results of Z_d against frequency from the theory. It is evident from the figure that the microstrip antenna resonates at 5 GHz (reactance is zero at resonance). The microstrip

antenna is usually operated near resonance to obtain a smaller resistance to match the source. Fig. 6-18 shows the far field radiation patterns in the *E*- and *H*-planes at 5.8 GHz. It is seen that the co-polar E_φ component dominates the cross-polar component E_θ in the *E*-plane and the co-polar E_θ component dominates the cross-polar component E_φ in the *H*-plane. Second, we analyze the microstrip antenna differentially driven at one radiating edge: $(x_1, y_1) = (0, 0.5W-\Delta)$ and $(x_2, y_2) = (0, 0.5W+\Delta)$ where $\Delta = 0.5$mm. Fig. 6-19 shows the numerical results of Z_d against frequency from the theory. It is interesting to note that the microstrip antenna does not resonate but exhibits an inductive property. As mentioned in previous chapters, the inductive property is useful in the codesign of antenna and transceiver because it can be explored to resonate with the capacitive nature of the transistors in the LNA and PA [44].

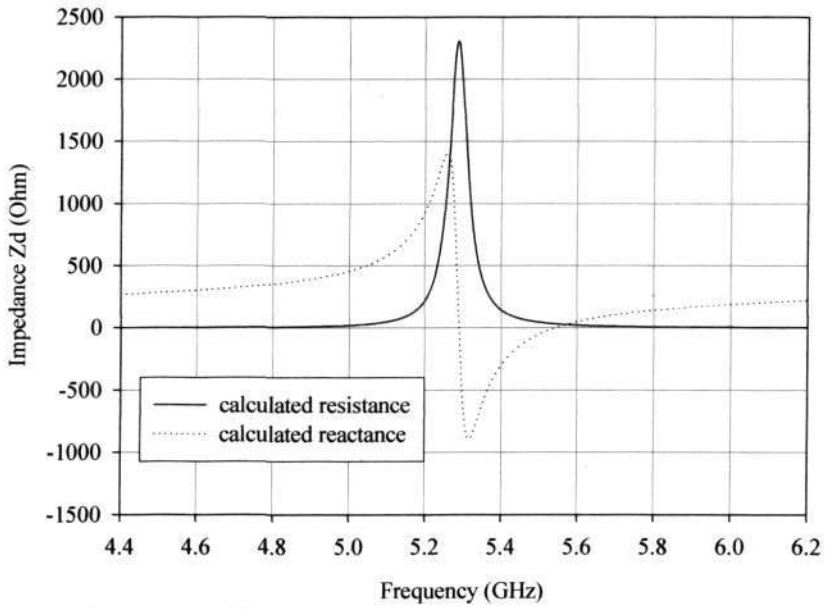


Fig. 6-17 Z_d for the ICPA driven at both radiating edges

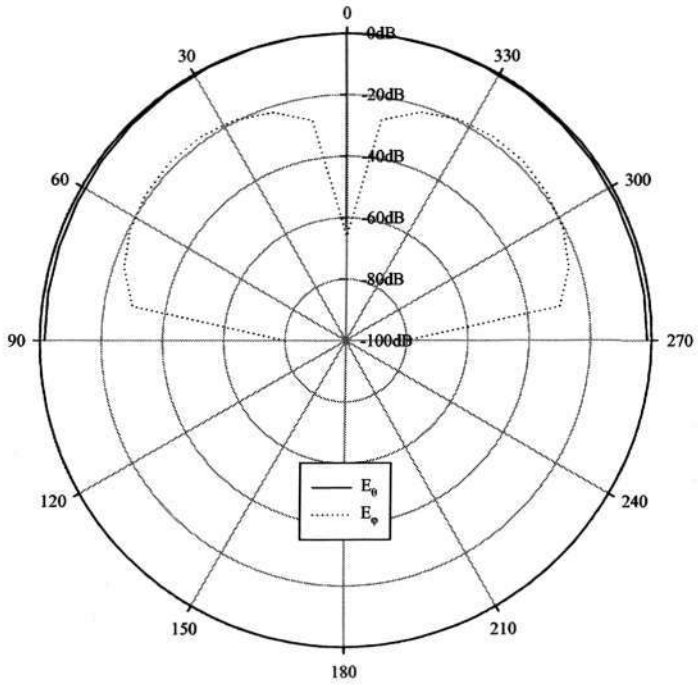


Fig. 6-18(a) Radiation patterns in E-plane for the ICPA driven at both radiating edges

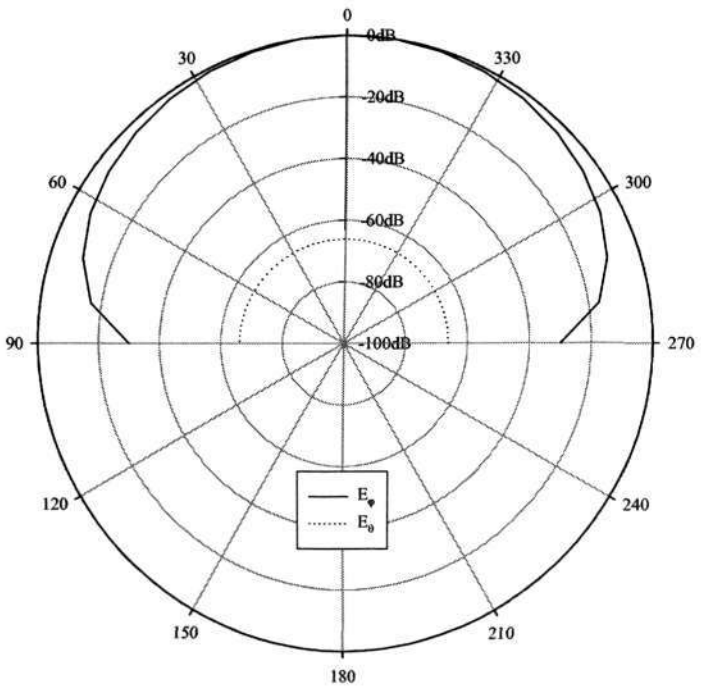


Fig. 6-18(b) Radiation patterns in H-plane for the ICPA driven at both radiating edges

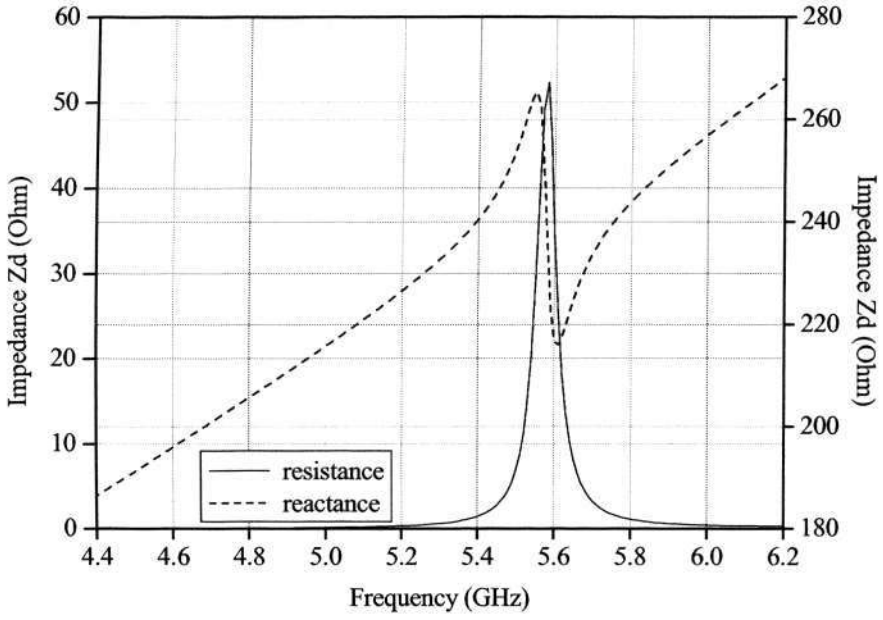


Fig. 6-19 Z_d for the ICPA feeding at one radiating edge

6.2.2 Integration

The integration of the differentially-driven microstrip antenna on the CBGA package into the differentially-driven ICPA is a challenging task. It requires a versatile numerical tool that can simulate both antenna and package structures. The HFSS and XFDTD from Ansoft and Remcom were chosen as our primary design tools. There are many integration issues for the ICPA. In this section, we emphasizes on such issues as feeding and shielding of the antenna from the transceiver using the packaging techniques. Fig. 6-20 is the explored view of differentially-driven ICPA, where the packaging elements for feeding and shielding can be clearly seen. The feeding to the antenna from the transceiver die is

through two identical packaging element networks. A packaging element network includes three bond wires, three signal traces, and three vias in the G-S-G fashion. A bond wire has a loop height of 0.2 mm and a length of 1.3 mm. A signal trace has a width of 0.32 mm and a length of 3 mm. The gap between the two adjacent signal traces is 0.48 mm. A via has a diameter of 0.2 mm. It is of interest to evaluate each of their impact on the overall electrical performance: bond wire, signal trace, and via. The bond wire presents high impedance; it has high inductance and low capacitance. Keeping the length of the bond wire to a minimum is critical to minimize its disruptive effect on the electrical signal. Using the largest diameter wire possible is also important, in this work we are using 32.5 μm wire. We place a ground wire on each side of the signal wire. This improves the situation by providing a return path in close proximity to the wire and thus reducing inductance slightly. The signal trace can provide the best electrical performance of the feeding network. It is primarily a coplanar waveguide. The signal integrity is well preserved. However, there is some level of loss due to dielectric material that is surrounding the conductor. As such, the length of this part does have an effect on the overall electrical behaviour but it is much less damaging than the bond wire is. The via is a transition from the signal trace to the microstrip line through an aperture on the ground plane. The diameter of the aperture has the potential to impact the electrical signal and is 0.3 mm.

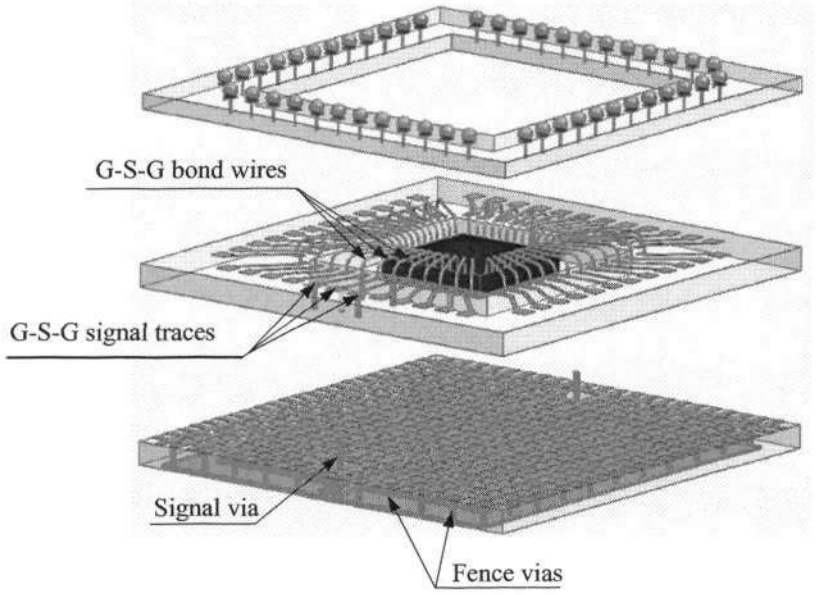


Fig. 6-20 Explored view of the differentially-driven ICPA

To model the effect of the single-chip transceiver die, a dummy CMOS silicon with dimensions of $4 \times 4 \times 0.4$ mm^3 is attached to the meshed ground in the cavity.

The results of the differentially-driven ICPA were compared with Fig. 6-17 for the differentially-driven microstrip antenna fed at both radiating edges which has L = 10.04 mm, W = 10.176 mm, H = 0.8 mm and d = 0.2 mm. Fig. 6-21 shows the simulated input impedance of differentially-driven ICPA fed from the signal traces and bond wires. It is seen that the resonant frequency shifts down to 4.41 GHz from 5.28 GHz when it is fed from the signal traces and further shifts down to 4.33 GHz when it is fed from the bond wires. The shift is mainly caused by the increased inductance from the feeding network. This shifting characteristic is helpful in miniaturizing the microstrip patch size of the ICPA. One can use a smaller microstrip patch to bring up the resonant frequency. Of course, due

to increased inductance, the bandwidth may become narrower and the impedance mismatch may become severer. We need to consider the tradeoffs.

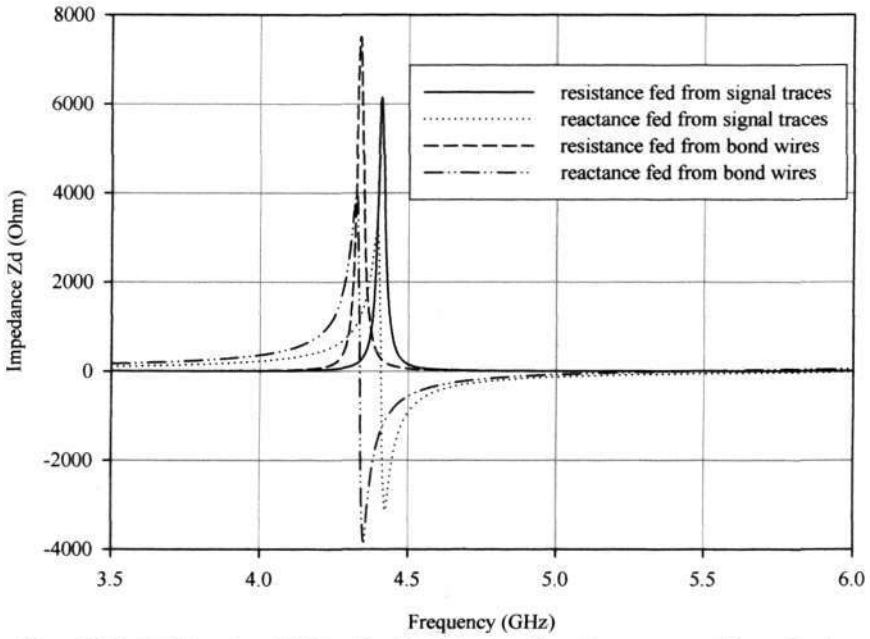


Fig. 6-21 Zd for the ICPA feeding from signal traces and bond wires

The shielding of the antenna from the transceiver is realized with the meshed ground. To enhance the shielding, a guard ring with fence vias shorted to the meshed ground is added. The width of the guard ring is 1.5 mm, and the gap between the guard ring and the microstrip patch is 0.4 mm. There are 8 fence vias on each side of the guard ring. The diameter of a fence via is 0.2 mm. Fig. 6-22 compares the simulated E_z components of the electric field on the middle plane between the microstrip patch and the meshed ground at 5.8 GHz with and without the guard ring. It is evident from the figure that the guard ring improves the shielding by 3 dB. Fig. 6-22 also shows that there exists a virtual AC ground in the middle of the patch, which is due to the ICPA fed differentially. The virtual ground

improves the isolation between the two feeding networks and also can be used to introduce a DC supply without affecting the ICPA operation.

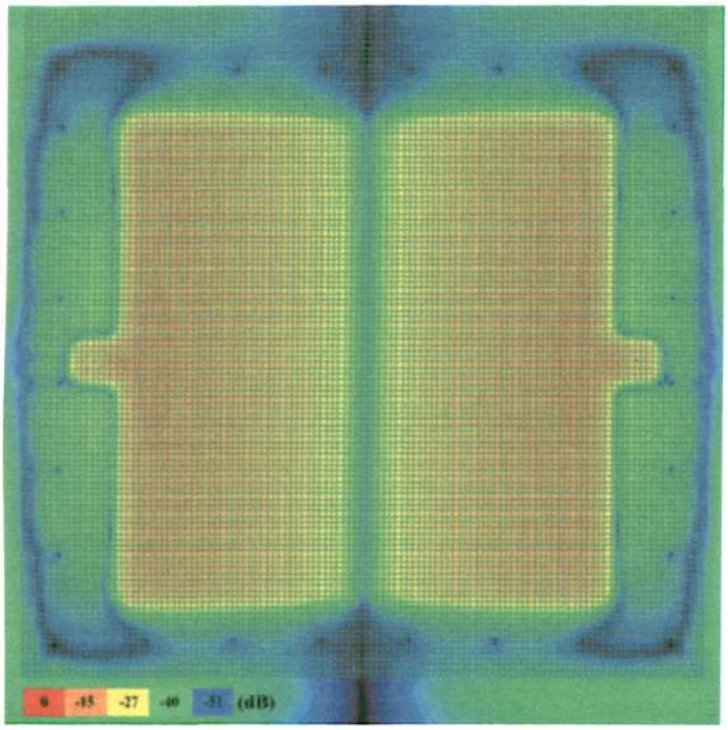


Fig. 6-22(a) E_z on the middle plane between the microstrip patch and the meshed ground with guard ring

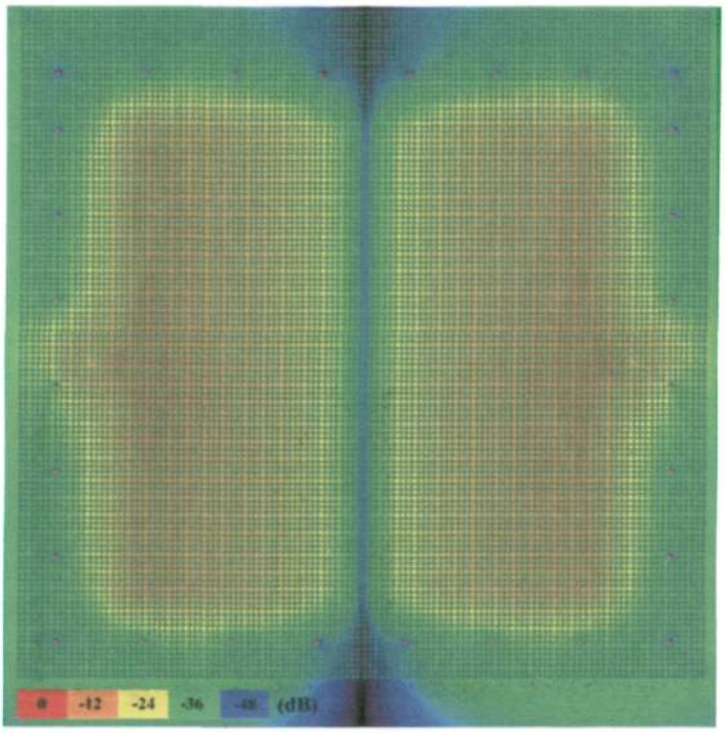


Fig. 6-22(b) Ez on the middle plane between the microstrip patch and the meshed ground without guard ring

6.2.3 Measured results for the ICPA

The designed differentially-driven ICPA was fabricated in Dupont 951-AX LTCC. Fig. 6-23 shows the photo. It measures 15 x 15 x 1.6 mm^3 with the microstrip patch of size 10.04 × 10.176 mm^2. Fig. 6-24 shows the ICPA surface-mounted on the middle of a test board. The test board of size 60 × 40 × 0.8 mm^3 is FR4 substrate. The ICPA feeds are soldered on two 50-Ω CPW lines for impedance and radiation tests. The differentially-driven ICPA was measured with an HP 8510C network analyzer in the NTU anechoic chamber. The measured S parameters were converted to the measured input impedance of the differentially-driven ICPA by eqn. (6-24). While the measured return loss calculated from Z_d is given by

$$RL = 20\log 10\left(\frac{Z_d - Z_o}{Z_d + Z_o}\right) \tag{6-25}$$

here Z_o is of typical value 100 Ω, 300 Ω or 600 Ω. In the study in this section, we chose 100 Ω to calculate the corresponding return loss.

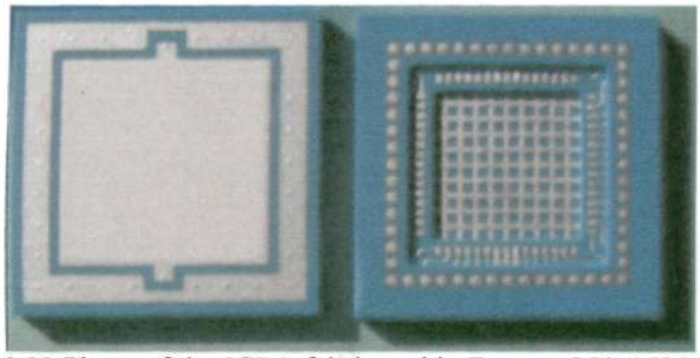


Fig. 6-23 Photo of the ICPA fabricated in Dupont 951-AX LTCC

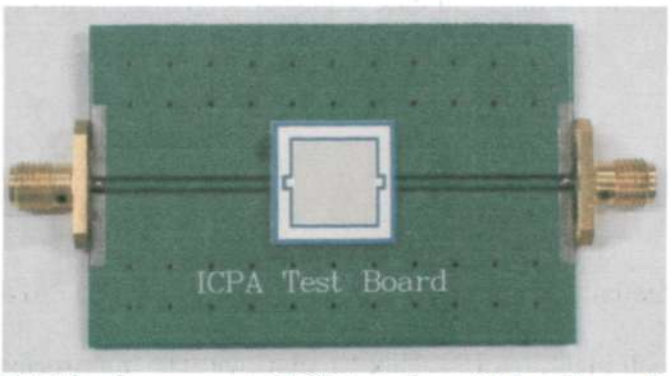


Fig. 6-24 Surface-mounted ICPA on the middle of a test board

Fig. 6-25 shows the measured input impedance of the differentially-driven ICPA. The impedance characteristics give insight on how the ICPA must be modified to achieve a specified resonant frequency. Here the resonant frequency is again defined as where the reactance of the input impedance is equal to zero. According to this definition, there are two resonant frequencies for the ICPA over the frequency range of interest from 5.6 to 6.2 GHz. It is evident that the impedance characteristics at the frequency of operation exhibit a

small peak in the resistance and a gentle swing in the reactance from inductive to capacitive.

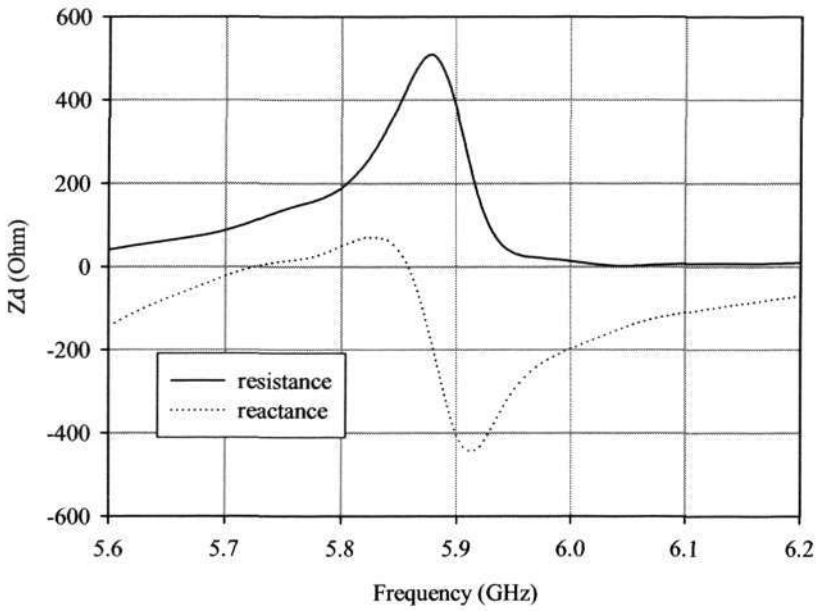


Fig. 6-25 Measured Z_d of the differentially-driven ICPA driven at both radiating edges

Fig. 6-26 shows the measured return loss of the ICPA. The percentage bandwidth is also defined as the difference between the upper and lower frequencies for which the return loss is less than or equal to - 10 dB divided by the average of the upper and lower frequencies. The return loss below - 10 dB at the frequency of operation indicates acceptable matching between the ICPA and the 100-Ω signal source is achieved. The measured impedance bandwidth of the ICPA is 120 MHz (0.12/5.52= 2.2%).

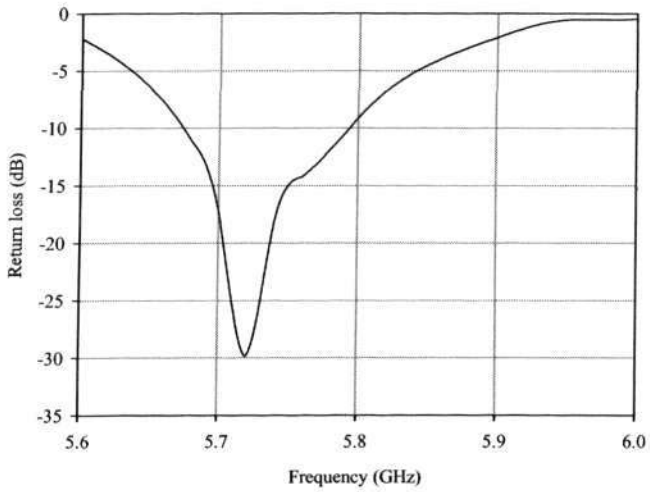


Fig. 6-26 Measured return loss of the ICPA driven at both radiating edges

Fig. 6-27 illustrates the measured radiation patterns of the ICPA at 5.8 GHz. In order to obtain differential signals to feed the differentially-driven ICPA, a 50-Ω balun designed at 5.8 GHz is used, the setting up is shown in Fig. 6-28. Due to the interaction between the radiation from the ICPA and the feeding cable, the measured radiation patterns show fluctuations particularly in the *E*-plane. The radiation is stronger in the upper hemisphere, i.e., in the direction normal to the ICPA. This feature of the radiation patterns is desirable because it not only helps improve the efficiency of the ICPA but also reduces the interaction of the ICPA with the human body. As shown in Fig. 6-27, the cross-polar components are at least 20 dB lower than the co-polar components. The efficiency of the ICPA is calculated to be 84%. In addition, it should be mentioned that the ICPA has much shorter distance to the RF output of the wireless transceiver than a conventional dielectric chip antenna; this implies a smaller transmission loss, which can be translated as an improvement to the ICPA efficiency by a few percent. The gain of the ICPA i found to be

3.2 dBi, which is almost 3 dB higher than the gain of most conventional dielectric chip antennas.

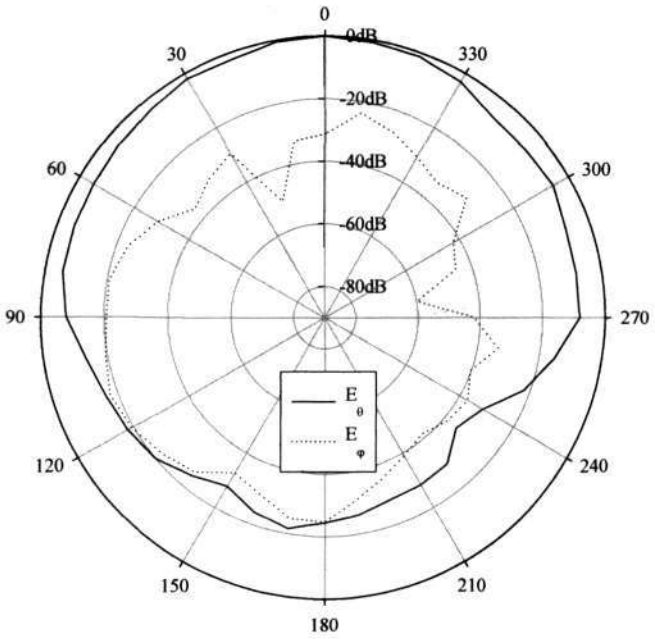


Fig. 6-27(a) Measured radiation patterns in E-plane driven at both radiating edges

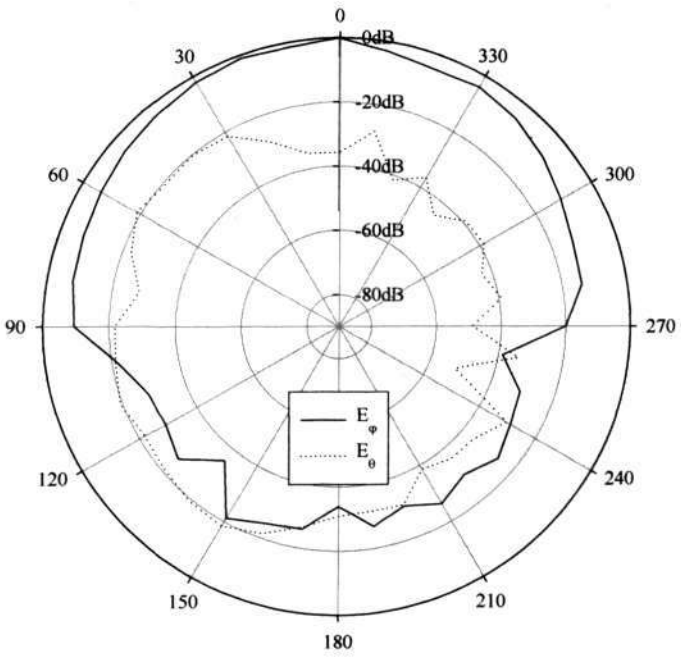


Fig. 6-27(b) Measured radiation patterns in H-plane driven at both radiating edges

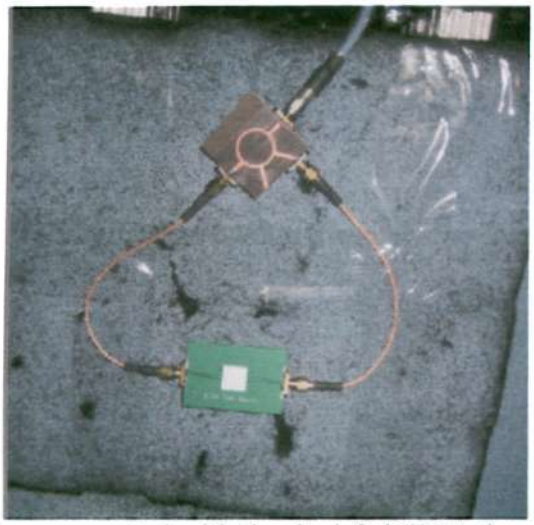


Fig. 6-28 Balun connected with the dual-fed ICPA for measurement

6.3 Summary of the chapter

We have studied differentially-driven microstrip antennas theoretically and experimentally in this paper. The improved theory of single-ended microstrip antennas based on the cavity model is expanded to analyze the input impedance and radiation characteristics of the differentially-driven microstrip antennas. The differentially-driven microstrip antennas are fabricated using Taconic TLY-5 and measured with the HP 8510C network analyzer. Theoretical and experimental results are found to be in acceptable agreement. It is shown from the analysis that the occurrence of resonance for the differentially-driven microstrip antennas also depends on the ratio of the separation ξ of the dual feeds to the free-space wavelength λ_o. When the dual feeds are located far from each other $\xi/\lambda_o > 0.1$, the resonance occurs, and the input resistance at resonance is rather large. However, when the dual feeds are located near to each other $\xi/\lambda_o < 0.1$, the resonance does not occur, the input

resistance is quite small, and the input impedance is inductive. The comparison with single-ended microstrip antennas is made. It is found that the differentially-driven microstrip antennas have larger resonant resistance, similar co-polar radiation patterns, and lower cross-polar radiation component.

What's more, we have developed a novel differentially-driven ICPA for single-chip radio transceivers. The ICPA designed in a cavity-down CBGA package format uses a differentially-driven microstrip antenna to better match the single-chip solution of radio transceivers. The gained physical insights from the theory then guide the integration of the differentially-driven microstrip antenna on the CBGA package into the differentially-driven ICPA. The integration is emphasized on the feeding and shielding of the antenna from the transceiver. The performance of the differentially-driven ICPA fabricated in LTCC technology is experimentally verified. Results show that the differentially-driven ICPA of size 15 x 15 x 1.6 mm^3 achieves impedance bandwidth of 2.2%, radiation efficiency of 84%, and gain of 3.2 dBi at 5.8 GHz.

CHAPTER SEVEN

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

We have emphasized on the necessity of the emergence of this project. Because this project should consider from the system level for chip-package codesign, the package format has been chosen firstly. This project solves the problem of integrating the antennas into the single-chip RF transceivers and a series of studies have been developed based on the ICPA concept.

A circuit model for the ICPA in a CLGA package format has been proposed. The model consideres the microstrip patch antenna fed by packaging interconnects such as bond wires, signal traces, and vias in a G-S-G configuration from the carried chip. 0.086 GHz (0.086/5.694 =1.5%) difference of center frequencies of impedance bandwidth between our modeled and the simulated one has been achieved. The difference between our modeled and the simulated resonant frequencies is only 0.077 GHz (0.077/5.745 = 1.34%) and the difference of the modeled and simulated resonant resistances is 0.8 Ω (0.8/25.7 = 3.1%).

A novel feeding technique suitable for the ICPA has been demonstrated, the ICPA in a thin 48-ball cavity-down CBGA package format has been designed for study. And the effects

of these feeding components on the performance of the ICPA have been investigated. It has been found that they mainly affect the impedance characteristics but not the radiation properties of the ICPA. What's more, a band selection ICPA is designed and fabricated using LTCC technology, which utilizes the via shorting scheme of the ICPA. The prototype ICPA operates at 5.37 GHz and 5.67 GHz when the band-select via is shorted and opened by measurement, respectively, whose capability greatly enhances the ICPA applications in wireless communications.

The voltage gain is 28.7 dB and noise figure is 1.68 dB of the antenna-chip codesigned LNA at 5.8 GHz, which is the critical component as the first active stage for the interface between antenna and the RF chip. The performance has obviously been improved using our proposed interface by the removal of the large matching inductor and utilization of the package components as well as the antenna's characteristics, which is compared with the 50-Ω input impedance single-ended on-chip LNA which achieves voltage gain of 20.7 dB and noise figure of 2.3 dB as well as the LNA using in-package architecture which achieves voltage gain of 25.2 dB and noise figure of 2.0 dB. Consequently, the area and cost of the RF chip are saved.

The improved theory of single-ended microstrip antennas based on the cavity model is expanded to analyze the input impedance and radiation characteristics of the differentially-driven microstrip antennas and ICPA. Theoretical and experimental results are found to be in acceptable agreement for the differentially-driven microstrip antennas. It is found that the differentially-driven microstrip antennas have larger resonant resistance, similar co-polar radiation patterns, and lower cross-polar radiation component compared with the single-ended counterpart. The differentially-driven ICPA fabricated in LTCC technology

of Dupont 951-AX is experimentally verified. Results show that the differentially-driven ICPA of size 15 x 15 x 1.6 mm^3 achieves impedance bandwidth of 2.2%, radiation efficiency of 84%, and gain of 3.2 dBi at 5.8 GHz.

7.2 Recommendations

In this project, we have mainly investigated the chip-package codesign of single-ended RF receiver front-end; while for the chip-package codesign of the differential RF receiver front-end, we have investigated only the antenna package part. To suit the development of differential RF receivers, the circuit model for the differentially-driven ICPA should be developed, the differential LNA should be designed and the interface between the antenna and LNA should be investigated in the future study for chip-package codesign of differential RF receiver front-end.

We have explored the antenna-chip co-design only by simulation. The RF chip could be fabricated and co-tested with the antenna part to further validate the proposed methods in the future. The RF receiver front-end may also include the mixer and VCO parts. Further circuits design for mixers and VCOs may be investigated for better completeness of the receiver system.

The connection between the single chip and the package in our work uses wire bonding. In the future study, flip-chip connections may be a better solution for RF and high speed packaging since they improve both electrical and thermal performance. Electrical performance improves by reducing bond wire inductance to a much smaller flip-chip bump inductance. With much smaller parasitic inductance, flip-chips also improve the ground

connection in both analog and digital circuits [20]. Besides electrical performance improvement, thermal performance also improves by direct heat dissipation through solder bumps from the front side of the chip. Studies on the flip-chip circuit model have been developed in [95], combining the circuits into the ICPA package model should be a good research work.

AUTHOR'S PUBLICATIONS

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1. **J. J. Wang**, Y. Xue, Y. P. Zhang, K. M. Chua, A. C. W. Lu and L. L. Wai, "Frequency-band selection for an integrated-circuit package antenna using LTCC technology," *Microwave and Optical Tech. Letters*, Vol. 44, No. 5, pp. 439-441, Mar. 2005.

2. **J. J. Wang**, Y. P. Zhang, K. M. Chua and A. C. W. Lu, "Circuit Model of Microstrip Patch Antenna on Ceramic Land Grid Array Package for Antenna-Chip Codesign of Highly Integrated RF Transceivers," *IEEE Trans. Antennas and Propagat.*, Vol. 53, No. 12, pp. 3877-3883, Dec. 2005.

3. **J. J. Wang**, A. C. W. Lu and K. M. Chua, "ICPA fed with packaging interconnect components for single-chip wireless transceivers," *RF and Microwave Computer Aided Engineering*, Vol. 16, No. 3, pp. 259-267, Feb. 2006.

4. Y. P. Zhang and **J. J. Wang**, "Theory and analysis of differentially-driven microstrip antennas," *IEEE Trans. Antennas and Propagat.*, Vol. 54, No. 4, pp. 1092-1099, Apr. 2006.

5. Y. P. Zhang, **J. J. Wang** and Y. Xue, "Differentially-driven integrated circuit package antenna for single-chip radio transceivers," submitted to *IEEE Trans. Antennas and Propagat.*.

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1. **J. J. Wang** and Y. P. Zhang, "Characterization of a feeding technique for integrated circuit package antenna," *Asia Pacific Microwave Conference*, Korea, Jun. 2003.
2. **J. J. Wang**, A. C. W. Lu and Y. P. Zhang, "Hybrid technique modeling of a generic feeding network for highly-integrated RF transceivers," *Electronics Packaging Technology Conference*, Singapore, Dec. 2004.
3. A. C. W. Lu, K. M. Chua, L. L. Wai, **J. J. Wang** and Y. P. Zhang, "Integrated antenna module for broadband wireless applications," *Electronics Packaging Technology Conference*, Singapore, Dec. 2004.

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