



**Millimeter-Wave CMOS Front-End  
Components Design**

**Huang Nan**

**SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING**

**2016**

**Millimeter-Wave CMOS Front-End  
Components Design**

**Huang Nan**

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

A thesis submitted to Nanyang Technological University  
in partial fulfillment of the requirement for the degree of  
Doctor of Philosophy

**2016**

# Acknowledgements

This is the place, where I tend to acknowledge all the people, who have helped me. Also note that there is a difference between thanking, which means to show of gratitude, and acknowledging, which means to recognize a contribution. This is to say that, I do not prosper or survive, because of my own strength or skill alone. The front page contains only one name, but that author would not have been able to do much of anything without the following people.

Here they are ——

I acknowledge Dr. Boon Chirn Chye, my supervisor, a man who adores and understands the circuit. He is knowledgeable, erudite, friendly, generous and all the while as a nice supervisor can be. His advocacy, support, candor and encouragement make me brave, and want to be brave when confronting the unpredictable challenges.

I acknowledge Dr. Yi Xiang, Dr. He Xiaofeng, Dr. Zhu Xi, for inspiring me with their passion and for their reading my circuits and drafts at critical times, offering wise, thoughtful and expansive feedback.

I acknowledge Mr. Feng Guangyin, for helping and teaching me on various software tools, with his patience, proficient computer skills.

I acknowledge Mr. Lim Wei Meng, for his commitment and his professional, meticulous work on my chip measurement.

I acknowledge Miss Zhu Di, for sharing with me her sheer mastery of concepts on analogue circuitry, benefiting me so much.

I acknowledge Mr. Bai Xiaoyin, Mr. Yang Yongkui, Miss Chen Zihao, and Miss Wang Bo, who sit near to me, for their best wishes always steadily accompanying me throughout all these years, leaving me priceless mementos.

I acknowledge Mr. Liang Zhipeng, Mr. Liu Bei, Mr. Yang Kaituo, Mr. Li Chengyang, Mr. Mao Mengda, Mr. Sun Junyi, Mr. Lin Jiafu, Mr. Liu Hang and other team members, for their myriad forms of support.

I acknowledge God, for giving me these sweet people, who help me, care me and mend me, with their overwhelming knowledgeability, humanity and personality.

# Contents

Abstract .....	1
Chapter 1 Introduction .....	4
1.1 Motivation.....	4
1.2 Overview of Intended Component Designs .....	6
1.3 Contributions.....	18
1.4 Organization.....	21
Chapter 2 Literature Review of Millimeter-Wave Applications on Automotive Radar and 94 GHz Passive Imaging .....	23
2.1 Overview of Automotive Radar .....	23
2.2 Overview of Millimeter-Wave Application at 94 GHz .....	25
2.3 Low-Noise Amplifiers for Automotive Radars .....	27
2.4 Low-Noise Amplifier at 94 GHz .....	32
2.5 W-band Mixer Design.....	35
2.6 Summary .....	37
Chapter 3 Fundamentals of LNA and Mixer Designs.....	38
3.1 Thermal Noise.....	38
3.2 Shot Noise .....	42
3.3 Flicker Noise .....	43
3.4 Classical Two-Port Noise Theory .....	45
3.5 Noise Figure of Cascade of Stages .....	48

3.6 LNA Configurations.....	49
3.7 Mixer Configurations.....	53
3.8 Discussions on Existing Refinement Works for Millimeter-Wave LNA and Mixer Designs .....	57
3.9 Summary.....	70
Chapter 4 Formulas for Analyzing Effects of Feedback on Noise Performance .....	71
4.1 Introduction.....	71
4.2 Formula Deduction Procedure .....	72
4.3 Summary.....	84
Chapter 5 A Dual-Band 24/77 GHz CMOS LNA for Automotive Radar Application.....	85
5.1 Introduction.....	86
5.2 Design of a Dual-Band Loading Network .....	88
5.3 Design of LNAs Operating at 24 GHz and 77 GHz .....	89
5.4 Noise Matching Technique .....	92
5.5 Design Flow of 77 GHz LNA.....	98
5.6 Switch Design .....	98
5.7 Layout Consideration and Simulation Results.....	99
5.8 Measurement Results .....	102
5.9 Summary.....	107
Chapter 6 Design of a Dual-Band Wilkinson Power Divider .....	108

6.1 Introduction.....	108
6.2 Theory and Design Equations .....	109
6.3 Layout and Simulation Results .....	116
6.4 Summary .....	120
Chapter 7 A 65-nm CMOS LNA for Bolometer Applications .....	121
7.1 Introduction.....	121
7.2 Design Considerations and Analysis.....	124
7.2.1 Device Sizing .....	125
7.2.2 First Stage Configuration.....	127
7.2.3 Configurations of Following Stages .....	141
7.3 Circuit Implementation and Measurement Results.....	145
7.4 Summary .....	153
Chapter 8 A CMOS W-band $4\times$ Quasi-Subharmonic Mixer .....	155
8.1 Introduction.....	155
8.2 Circuit Design .....	157
8.3 Measurement Results .....	165
8.4 Summary .....	169
Chapter 9 Conclusions and Future Work .....	170
9.1 Conclusions.....	170
9.2 Future Work .....	172
Reference .....	176
Publication List .....	186

# List of Figures

Figure 1.1 The architecture of a single channel transceiver used for an FMCW radar. ....	8
Figure 1.2 Noise Figure versus Link Budget for $d=50m$ . ....	10
Figure 1.3 (a) a photo of a patch antenna array, (b) building blocks of the patch array. ....	11
Figure 1.4 Noise Figure versus Link Budget for $d=150m$ . ....	13
Figure 1.5 The prototype of a passive imaging receiver. ....	16
Figure 1.6 Plot of the system noise temperature ( $T_s$ ) versus the noise equivalent temperature difference ( $NETD$ ) for different bandwidths. .	17
Figure 2.1 Illustration of an automotive radar's working principles. [5], [14]. ....	24
Figure 2.2 (a) The plot of atmosphere windows; (b) attenuation versus frequency. [6]. ....	26
Figure 2.3 The plot of the commended noise figure versus frequency [14]. ....	28
Figure 2.4 (a) The configuration of the proposed LNA and its corresponding layout, and (b) the plot of the noise figure and gain versus frequency [14]. ....	29
Figure 2.5 A BJT LNA proposed by [18]. ....	30
Figure 2.6 The schematic of a BJT dual-band LNA proposed by [19]. ....	32

Figure 2.7 The principle of the staggered tuning amplification. [21].	34
Figure 2.8 Illustration of the distributed amplification [22].	35
Figure 2.9 An example of the subharmonic mixer (N=2) [22].	37
Figure 3.1 Illustration of the definition of available noise power.	39
Figure 3.2 Illustration of gate noise.	41
Figure 3.3 A noisy two-port network represented by two noise generators and a noiseless two-port network.	45
Figure 3.4 A matching method by directly placing a resistor at input.	49
Figure 3.5 An amplifier configured by series-shunt feedback.	50
Figure 3.6 The configuration of a common-gate LNA.	51
Figure 3.7 A common-source amplifier with a source degenerated inductor.	52
Figure 3.8 A dual-gate mixer [22].	54
Figure 3.9 (a) A typical CMOS subharmonic mixer, and (b) the working principle of a CMOS subharmonic mixer. [37].	56
Figure 3.10 A shunt inductor used to extend the bandwidth of a cascode amplifier. [38]	59
Figure 3.11 Noise and bandwidth refinements for a cascade of cascode amplifiers. [39].	61
Figure 3.12 A folded cascode amplifier. [40].	62
Figure 3.13 Figure 3.13 A W-band Gilbert-cell mixer. [41].	63
Figure 3.14 A conventional subharmonic mixer implemented by diodes. [42]	

.....	64
Figure 3.15 A subharmonic mixer by the pumping method. [43].....	65
Figure 3.16 Die photo of a subharmonic consisting of a quadrature coupler. [44].....	66
Figure 4.1 Shunt-series feedback represented by two two-port networks ..	73
Figure 4.2 The noise equivalent circuit of Figure 4.1.....	74
Figure 5.1 The proposed topology for the dual-band LNA. ....	87
Figure 5.2 The structure of the dual-band loading network.....	88
Figure 5.3 The effect of $C_{gd}$ on the input impedance of a common source amplifier. ....	90
Figure 5.4 Schematic of the proposed dual-band LNA: (a) the 77 GHz LNA, (b) the 24 GHz LNA, and (c) the final schematic.....	92
Figure 5.5 The simplified schematic of the first stage circuit in Figure 24(a) and (b). ....	96
Figure 5.6 The structure of the binary-switch.....	99
Figure 5.7 The final layout of the proposed dual-band LNA.....	100
Figure 5.8 Simulated results of (a) the voltage gain, (b) $s_{11}$ and (c) the noise figure.....	102
Figure 5.9 Die photograph of the 24/77 GHz receiver.....	103
Figure 5.10 Measured output power gain and the 1-dB-compression point (a) 24- and (b) 77-GHz modes. ....	105
Figure 5.11 Measured FMCW modulation frequency and its time-domain	

frequency error. ....	105
Figure 5.12 Measured input reflection coefficients of the receiver at the 24- and 77-GHz input ports. ....	106
Figure 6.1. A conventional Wilkinson power divider. ....	110
Figure 6.2. The structure of the proposed dual-band Wilkinson power divider. .....	111
Figure 6.3. The odd-mode analysis: (a) the halved circuit for the odd-mode analysis, (b) the proposed method to reduce the chip area by combining $L_1$ and $L_2$ in one planar inductor. ....	113
Figure 6.4. The halved circuit for the even-mode analysis. ....	114
Figure 6.5. The illustration of the decomposition of the fifth order filter. ....	114
Figure 6.6. 3-D view of the dual-band Wilkinson power divider ....	117
Figure 6.7. Simulated results of (a) the return loss and isolation, and (b) insertion loss. ....	119
Figure 7.1 The conventional configuration of the cascode amplifier. ....	127
Figure 7.2 The modified cascode amplifier aiming for the gain enhancement. .....	129
Figure 7.3 The small-signal model for analyzing the gate inductive feedback. .....	130
Figure 7.4 The small-signal model of the circuit shown in Fig. 7.2. ....	133
Figure 7.5 (a) A practical circuit example given to demonstrate $L_3$ 's impact on the input reflection coefficient; (b) the plot of the input reflection	

coefficient versus the increase of $L_3$ . .....	137
Figure 7.6 The circuit model to analyze the impact of the input matching on the noise figure.....	139
Figure 7.7 The frequency domain illustration of the conventional amplification scheme. ....	142
Figure 7.8 The equivalent circuit model of $M_4$ and $M_6$ 's loading networks.....	143
Figure 7.9 The proposed LNA structure (biasing circuits are not shown).....	145
Figure 7.10 The die photo of the proposed LNA.....	146
Figure 7.11 The illustration of the implementation of the circuit model shown in Fig. 7.8. ....	147
Figure 7.12 Simulated AC responses at outputs of each stage. ....	148
Figure 7.13 Simulated (dashed line) and measured (solid line) results of the input and output reflection coefficients. ....	151
Figure 7.14 Simulated (dashed line) and measured (solid line) results of the transducer gain and noise figure. ....	151
Figure 7.15 Measured output power versus input power. ....	152
Figure 8.1 (a) The schematic of the tandem-switch, (b) detailed waveforms at point A and (b) at point B.....	159
Figure 8.2 (a) The snapshot captured when $\omega_{in}$ is a multiple of $\omega_{LO}$ , and (b) details on LO. ....	160

Figure 8.3 Time domain waveforms used to explain the output waveform. ....	161
Figure 8.4 The plot of $A_{out}/A_{in}$ versus $\Delta T/T_{in}$ . ....	162
Figure 8.5 The schematic of the proposed $4\times$ quasi-subharmonic mixer. ....	163
Figure 8.6 (a) $\Delta T$ and $T_{hold}$ effects on gain, and (b) the plot of $V_{bias}$ versus $v_B$ -at-1-GHz. ....	165
Figure 8.7 The die photo of the proposed mixer and its corresponding DC bias. ....	166
Figure 8.8 Measured power conversion gain (CG) and the input reflection coefficient ( $\Gamma$ ) versus RF frequency with LO power set to 10 dBm. ....	167
Figure 8.9 Measured NF (DSB), CG versus the frequency offset. ....	168
Figure 8.10 Measured $P_{1dB}$ , with LO power set to 10dBm. ....	168

# List of Tables

Table 1.1 Design Specifications of the LNAs.....	144
Table 1.2 Design Specifications of the Dual-Band Power Divider.....	155
Table 1.3 Design Specifications of the LNA and Mixer for Passive Imaging Application.....	188
Table 3.1 Performance Summary of Some Millimeter-Wave LNAs and Mixers .....	677
Table 5.1 Comparison of the State-of-the-Art Receivers for Automotive Radar Applications.....	106
Table 6.1 Performance Summary of the Wilkinson Power Divider.....	118
Table 7.1 Inductance and Capacitance Summary.....	148
Table 7.2 Performance Comparison of Millimeter-Wave LNAs .....	153
Table 8.1 Performance Comparison of W-band Mixers .....	169

# Acronyms

AC	Alternating Current
ACC	Adaptive Cruise Control
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BW	Bandwidth
CG	Conversion Gain
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FMCW	Frequency Modulated Continuous Wave
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LB	Link Budget
MOS	Metal Oxide Semiconductor
NEP	Noise-Equivalent Power
NETD	Noise-Equivalent Temperature Difference
NF	Noise Figure
NMOS	n-channel MOS
PA	Power Amplifier
PDK	Process Design Kit
PMOS	p-channel MOS
RF	Radio Frequency
SiGe	Silicon-Germanium

# Abstract

Ranging from 30 to 300 GHz, millimeter-waves are whipping up flames of interest for all sorts of uses. They take the pressure off the lower frequencies and expand wireless communications into the outer limits of radio technology; they provide atmosphere windows upon the extremely high frequencies and benefit the bolometer-arrays seeking for smaller dimensions. At one time, this part of the spectrum was essentially unused, simply because few if any electronic components could generate or receive the millimeter-waves. All that has changed in the past decade or so. Millimeter-waves now gradually become practical and affordable, thanks to the development of CMOS technologies. Once implemented in CMOS, blocks that handle the millimeter-waves fit in perfectly with the digital ones, making the chip readily available for massive production. Although such integration capacity could overcome the bottleneck of compatibility, the millimeter-wave block yet remains as a stumbling block. MOS transistor's insufficient intrinsic gain and lossy substrate limit the circuit performance. Therefore, the W-band CMOS circuits strongly need some refinement work in order to undertake two important millimeter-wave applications. The first important application is for the 76-77 GHz automotive radar. The second is the passive imaging, which utilizes an atmosphere window centered at 94 GHz. The scope of this thesis focuses on the millimeter-wave receiver's front-end design. Based on a 65-nm CMOS technology, the following refinement works further

stretches the CMOS limits, aiming to fulfill its potential in aforesaid millimeter-wave applications. The first two concentrate on the millimeter-wave application for automotive radars. There are frequency bands opened for vehicle radars to use. One is centered at the millimeter-wave frequency range, i.e. 77 GHz, which is known as the long-range radar. Another is centered at 24 GHz, known as the short-range radar. In order to make the best possible use of those two bands, a dual-band 24/77 GHz CMOS low-noise amplifier (LNA) is designed. It is the first time that a 24- and a 77-GHz LNA are combined using a CMOS technology. The proposed topology of the dual-band LNA greatly saves the chip area and the LNA consumes very little dc power, which is particularly suitable for the electric vehicle to use. In order to improve the sensitivity and the angular resolution, the single channel receivers should be combined as an array. The conventional combining method uses specific power dividers operating in only one frequency band. Moreover, a conventional Wilkinson power divider occupies a large chip area. In order to address these issues, a dual-band Wilkinson power divider is presented in this thesis. The proposed divider consists of lumped elements instead of quarter-wavelength transmission lines, which has greatly reduced the chip size. Its performance is as effective as that of a single-band power divider. The second two works are dedicated to the millimeter-wave application for passive imaging. An LNA and a mixer are designed. By properly applying positive feedback, the noise figure of the proposed LNA is minimized at 5.1 dB, and the bandwidth is extended to 30 GHz. The proposed LNA achieves the lowest noise figure among

all reported 65 nm CMOS LNAs. The proposed mixer is developed from subharmonic mixers. Down-conversion process is achieved by capturing the phase difference between two sine waves at every half cycle of the local oscillator. The significant advantage of the presented mixer is that it saves one's great trouble in designing phase-shifters. Moreover, the mixer covers a wide frequency band. Its conversion gain is above 3.5 dB across the entire W-band. In turn, it can also be used in a 77-GHz automotive radar.

# Chapter 1

## Introduction

### 1.1 Motivation

CMOS millimeter-wave systems have gained increasing attention in recent years. With continuous efforts in scaling down the feature size of MOS transistors, it seems more promising than ever to implement a millimeter-wave system, which is all made up of CMOS components. A fully integrated CMOS millimeter-wave system brings numerous benefits. Best of all, it makes the millimeter-wave more practical and affordable. [1]–[4]

The work presented in this thesis is motivated by following applications.

First, the Federal Communications Commission has licensed two frequency bands, i.e. the 22 GHz-29 GHz band and the 76-77 GHz band, which are both opened for automotive radars [5]. Vehicle manufacturers are quite interested in these radars, because vehicle injuries and bills can be henceforth reduced. The radar that operates at 77 GHz is a long-range radar, called the Adaptive Cruise Control radar (ACC). It measures the distance between the driver's car and its nearest front car. If the measured distance is too short, ACC will automatically trigger a slow down or a brake signal. Similarly, if the front car starts to speed up or change a lane, ACC will accordingly accelerate the speed of the driver's car. Price for an ACC radar is around 1,500 to 3,000 US dollars. In order to promote the ACC market, such a high price should be further reduced. One benefit offered

by CMOS is its lower cost. Therefore, it is desirable to fabricate the ACC radar in a CMOS technology. Another type of vehicle radars is called the short-range radar. Its operating frequency range is from 22 GHz to 29 GHz. This type of radar prevents side impacts and can assist with parking. As can be seen, the combination of short- and long-range radars makes an automotive radar more powerful.

Second, it is well known that millimeter-waves can help with navigating and surveilling under poor weather conditions [6]. In addition, their ability to penetrate textile and plastic materials let themselves become as a green technology, thus serving as an alternative solution for security scanning [2]. All these applications depend on the atmosphere windows, which ease the transmission of millimeter-waves. For a 65-nm CMOS technology, its operating frequency-range contains two atmosphere windows [7]. One is centered at 35 GHz and another is centered at 94 GHz. The 94 GHz atmosphere window is more preferable for CMOS imaging-arrays, because the antenna dimension is inversely proportional to the operating frequency [8]. However, such a high operating frequency is difficult for a 65-nm CMOS circuitry to get by [9] [10]. Therefore, the performance of a CMOS circuit, supposed to operate at the extremes of frequency, has to be improved [11].

Currently, it yet remains as a challenge task to design a millimeter-wave CMOS front-end. The low-noise amplifier (LNA) and mixer are two important components in the front-end. The low-noise amplifier is the first active device

that handles the incoming millimeter-wave. Its performance directly determines how sensitive the receiver can detect out a millimeter-wave signal. The mixer is the second active device, which is used to down-convert the millimeter-waves to baseband. Its performance is also critical. For example, it should possess a relatively low noise figure such that the gain of the preceding LNA can easily minimize its noise figure. It should be of low loss and high linearity as well; otherwise, the noise figure would be deteriorated therefrom. [12]

As motivated by the above mentioned opportunities and challenges, this thesis continues the refinement work on the front-end components designs, aiming to improve the performance of CMOS components in a millimeter-wave front-end.

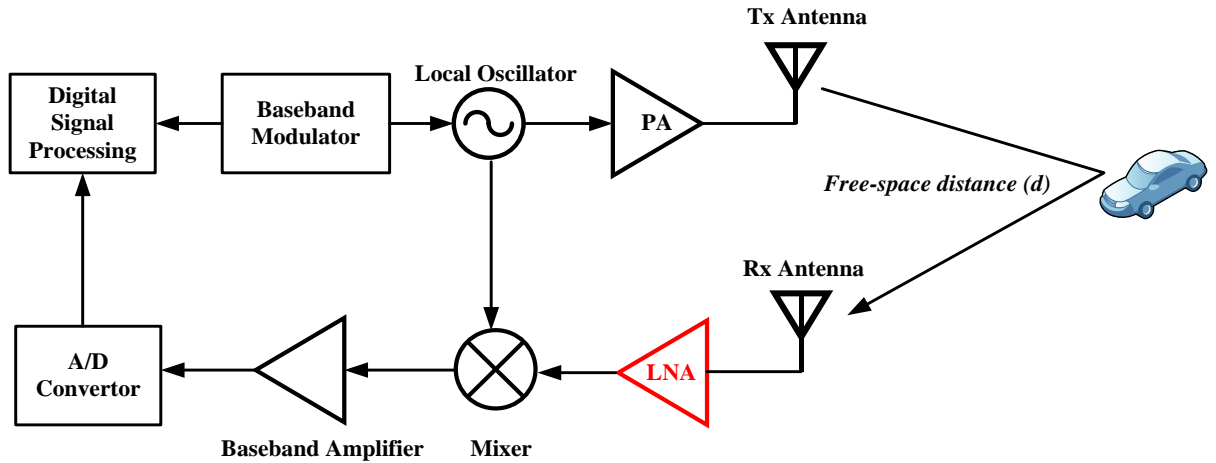
## **1.2 Overview of Intended Component Designs**

The motivation and the intended component designs have been briefly introduced in section 1.1. As described in section 1.1, this thesis focuses on components in a receiver's front-end. Topics on LNAs, mixers and power dividers are within its coverage. This section is to link and to investigate these individual components from a system-level perspective such that one can clearly know the design issues as well as the specifications at the very beginning. After outlining the main features of this thesis, a more detailed explanation and description with respect to the design theory and principles is provided in Chapter 2 and 3.

The first application to look at is the millimeter-wave automotive radars. The

Frequency Modulated Continuous Wave (FMCW) radars at 77-GHz in the millimeter-wave frequency range and 24-GHz in the K-band, when combined together, can help the driver either to drive or to park the car. One important reason of choosing the FMCW radar is that it has a simple architecture. Unlike pulse radars, such a radar does not depend on the high voltage circuitry. The architecture of an FMCW radar is illustrated in Fig. 1.1, which is basically a homodyne radio. Taken the 77-GHz FMCW radar as an example. As shown in Fig. 1.1, the baseband signal after being modulated to the 77-GHz band is then sent to the power amplifier (PA). The antenna helps the PA to radiate a continuous wave so as to examine the traffic condition. At the receiver side, the transmitted power, which might be heavily attenuated, should be received by the LNA in the receiver. The received signal is then downconverted to the baseband by the mixer.

The first intended design is an LNA, which is used to help the radar to accurately receive the transmitted signal, as highlighted in red in Fig 1.1. Before starting the component design, the design specifications should be determined first. Based on the scenario illustrated in Fig. 1.1, the link budget with respect to the receiver can be estimated. Then, the design specifications can be specified based on the estimation.



**Figure 1.1** The architecture of a single channel transceiver used for an FMCW radar.

In order to estimate the link budget (LB) for a receiver's front-end, following conditions, according to the state-of-the-art technologies, are set ahead: [13] [14]

1.  $d=50\text{m}$  (The initial value for the distance is set at 50m. Later on, as one will see, after some refinements, this receiver's detection range can be extended.)
2.  $G_{\text{TX}}=G_{\text{RX}}=30\text{dBi}$  (The gain of an antenna is normalized to the gain of an isotropic antenna. It is assumed that the transmitter's and receiver's antennas share the same gain and they are implemented as patch antennas.)
3.  $\sigma=15\text{m}^2$  (The radar cross-section is evaluated to be  $15\text{ m}^2$ , a typical value for a car's area.)
4.  $P_{\text{TX}}=20\text{dBm}$  ( $P_{\text{TX}}$  is the power radiated at the output of the transmitter.)
5.  $\text{SNR}=6\text{dB}$  (According to existing works, the signal to noise ratio, SNR, is set at 6dB.)

With these known variables, the link budget can be calculated as follows.

The first step is to calculate the radiated power at the receiver side. At the input of the receiver, the received radiated power ( $P_{RX}$ ) is described by the radar equation.

$$P_{RX}(dBm) = 10\log_{10}\left(\frac{\lambda^2\sigma P_{TX}G_{TX}G_{RX}}{(4\pi)^3 r^4}\right)$$

$$= -48 + 12 + 20 + 30 + 30 - 100 = -56 (dB). \quad (1.1)$$

Next, the expression of the minimum detectable signal needs be obtained. Assume that the receiver's noise figure is determined by the LNA. The minimum detectable signal ( $S_i$ ) then can be expressed as the sum of the LNA's noise figure (NF) plus the noise power within a bandwidth of  $\Delta f$  and the SNR:

$$S_i(dBm) = NF + 10\log_{10}(kT\Delta f) + SNR = NF - 174dBm + 90dBm + 6dB = NF - 78dB. \quad (1.2)$$

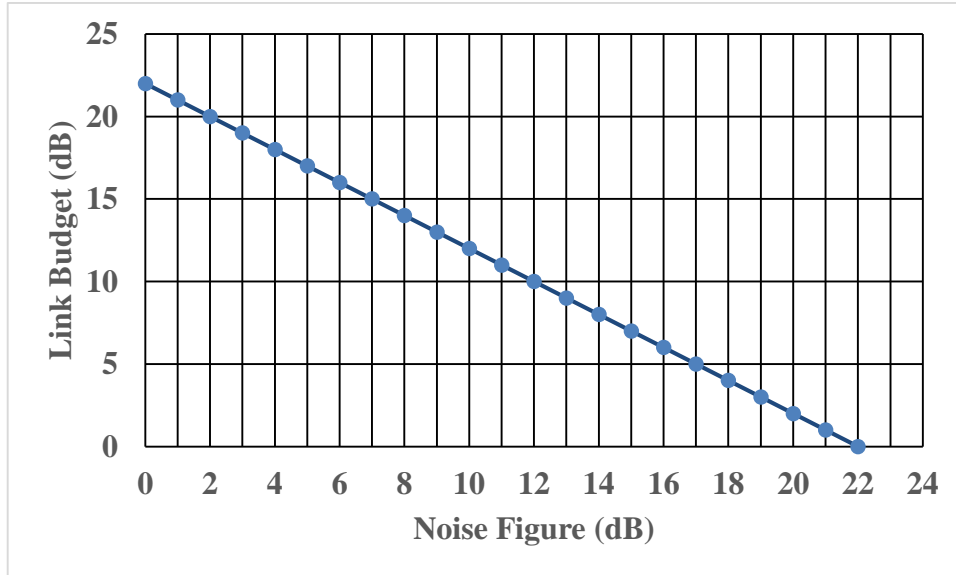
Based on (1.1) and (1.2) the expression of the link budget (LB) can be finally obtained:

$$LB(dB) = P_{RX}(dBm) - S_i(dBm) = 22dBm - NF. \quad (1.3)$$

Based on (1.3), the specification of the LNA's noise figure can be estimated. To help the estimation, one can plot the curve of “NF vs.LB” to directly inspect

how the noise figure affects the room of the link budget. The plot is shown in Fig.

1.2.

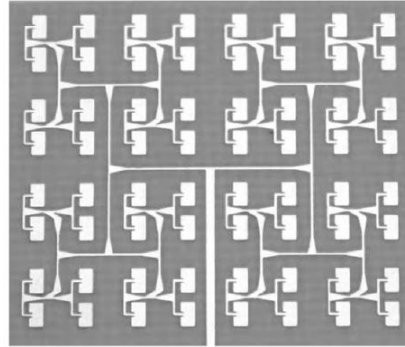


**Figure 1.2 Noise Figure versus Link Budget for  $d=50m$ .**

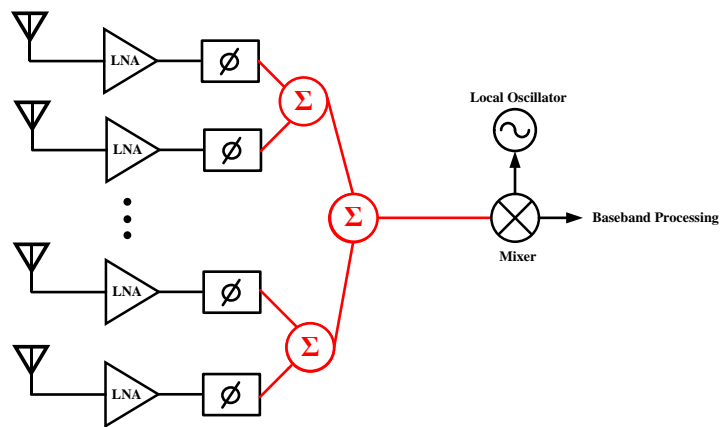
As seen in Fig. 1.2, the link budget reduces if the noise figure increases. This means that the noisier the LNA is, the less room the link budget would have. For the link budget, a larger link budget can leave enough room for various unexpected realistic problems such as the cable and the probe losses. However, for a single channel receiver as shown in Fig. 1.1, in order to obtain a link budget greater than 20dB, the noise figure should not exceed 2dB. For a 65 nm CMOS LNA, such a requirement is impractical.

Nevertheless, the link margin requirement can be relaxed if the single channel receiver can be grouped as an array, as shown in Fig. 1.2(a). Fig. 1.2(a) is a photo of an array consisting of  $8 \times 8$  patch antennas. Fig. 1.2(b) illustrates the building

blocks inside the patch array. As seen in Fig. 1.2(b), the patch array is a combination of multiple single channel receivers which are grouped in pairs.



(a)



(b)

**Figure 1.3 (a) a photo of a patch antenna array, (b) building blocks of the patch array.**

The patch array is superior to a single channel receiver for the following reasons. In regard to a patch antenna array consisting of  $N$  antennas, expressions of (1.1) and (1.2) then become as:

$$P_{RX}(dBm) = 10 \log_{10} \left( \frac{\lambda^2 \sigma N P_{TX} G_{TX} G_{RX}}{(4\pi)^3 r^4} \right), \quad (1.4)$$

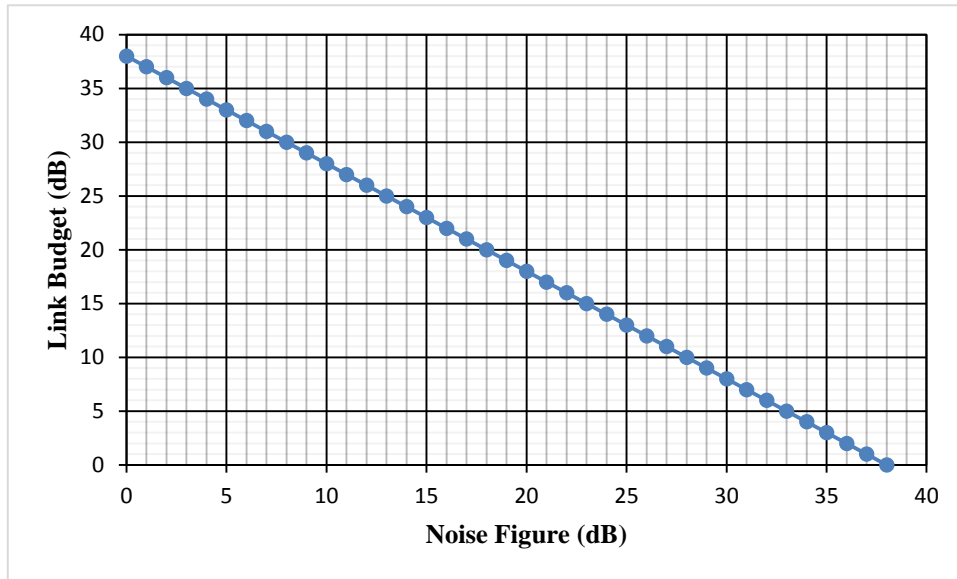
and

$$LB(dB) = P_{RX}(dBm) - S_i(dBm) + 10\log_{10}N. \quad (1.5)$$

Consider an  $8 \times 8$  array and assume the noise figure of the LNA is 8dB, the new link budget is:

$$LB(dB) = P_{RX}(dBm) - S_i(dBm) + 10\log_{10}N = 50 (dB) \quad (1.6)$$

Compared to the previous single channel receiver whose noise figure is also 8 dB, this array can increase the link budget by 36 dB for the same given distance of 50 m. Moreover, for the same noise figure, the array can extend the detecting distance. If the free space distance is increased to 150m, the “*Noise Figure vs. Link Budget*” curve can be replotted, as shown in Fig. 1.4.



**Figure 1.4 Noise Figure versus Link Budget for  $d=150m$ .**

As seen in Fig. 1.4, a noise figure of 8 dB corresponds to a link budget of 30 dB. Therefore, for a 77-GHz LNA design, the specification of the noise figure is selected to be 8 dB. The bandwidth is set to be 1 GHz as earlier mentioned. The specification of the gain is determined based on the following judgement. The gain of the LNA is used to minimize the overall noise figure of the receiver. Given that the mixer and its following stages normally contribute a noise figure around 20 dB, the gain of the LNA is thereby targeted at 25dB. Similarly, for the 24-GHz LNA, the specification can be decided in the same manner. Table 1.1 summarizes the specifications of the LNAs.

**Table 1.1 Design Specifications of the LNAs**

<i>Name</i> <i>Spec.</i>	<i>Gain</i>	<i>Noise Figure</i>	<i>Bandwidth</i>
<b>24-GHz LNA</b>	<i>25 dB</i>	<i>5 dB</i>	<i>4 GHz</i>
<b>77-GHz LNA</b>	<i>25 dB</i>	<i>8 dB</i>	<i>1 GHz</i>

Although it has been proven that the antenna array can create additional room for the link budget, it brings some problems as well. One big problem is the large area occupied by the power divider. Power dividers are passive microwave components used for power division or power combining. In power division, an input signal is divided into two (or more) output signals of lesser power, while a power combiner accepts two or more input signals and combines them at an output port. Referring to Fig. 1.3(a), the combination of power is realized by the Wilkinson power dividers. The Wilkinson power divider is widely used nowadays, because it can have its three ports simultaneously well matched to 50  $\Omega$  while maintains a high isolation. The Wilkinson power divider normally occupies a large chip area, because it is conventionally implemented by bulky transmission lines. For a dual-band system, if each frequency band needs its own divider, it can be imagined that the chip size will become unacceptably large. Therefore, in order to relieve the space constraints, a dual-band Wilkinson power divider which employs the lumped elements instead of the transmission lines is designed.

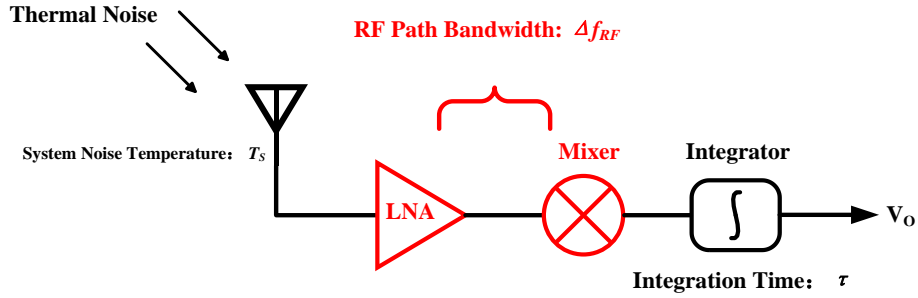
The specifications of the dual-band Wilkinson power divider are summarized in Table 1.2. Firstly, at each frequency band, the power loss should be kept below 1.5 dB. Secondly, the three ports should be well matched to 50  $\Omega$ . Therefore, the input reflection coefficient at each port should be suppressed below -10 dB. Thirdly, the isolation should be as high as 20 dB, which corresponds to a power leakage less than 1%.

**Table 1.2 Design Specifications of the Dual-Band Power Divider**

<i>Frequency Bands</i>	$S_{11}$	$S_{22}$	$S_{33}$	$S_{23}$	$S_{21}$	$S_{31}$
<i>Centered at 24 GHz</i>	-10 dB	-10 dB	-10 dB	-20 dB	-4.5 dB	-4.5 dB
<i>Centered at 77 GHz</i>	-10 dB	-10 dB	-10 dB	-20 dB	-4.5 dB	-4.5 dB

Above discussions have determined the design specifications for components dedicated to the application for automotive radars. Design specifications of the millimeter-wave application for passive imaging are determined based on the following analysis.

The millimeter-wave passive imaging receivers are designed to receive the thermal radiation emitted from a “black-body”. The thermal noise is their incoming signal. As can be conceived, in order to receive such weak power, the receiver should have a very low noise figure. In addition, its bandwidth should be wide enough in order to receive more noise power from a much wider frequency range. The prototype of a passive imaging receiver is simple, as illustrated in Fig. 1.5. The focused components are highlighted in red.



**Figure 1.5 The prototype of a passive imaging receiver.**

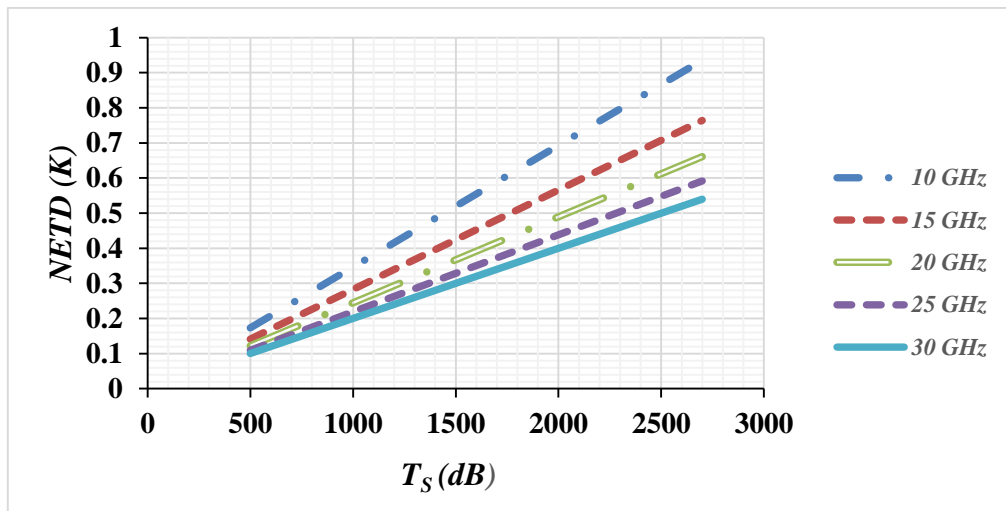
Similar to the foregoing discussion, the design specifications can be determined through the link budget calculation. In this case, the link budget refers to the thermal resolution. The thermal resolution of a passive receiver is quantified by the noise equivalent temperature difference. The noise equivalent temperature difference (NETD) is a measure that indicates the minimum thermal difference the receiver can distinguish. A simple form of NETD can be expressed as:

$$NETD = 6 \cdot T_s \cdot \sqrt{\frac{1}{\Delta f_{RF} \cdot \tau}}, \quad (1.7)$$

where the weighting factor, 6, is estimated for power losses due to the passive components in front of the LNA such as the antenna and the switch losses.

Based on the expression of NETD and referred to Fig. 1.5, design specifications can be quantitatively decided. In order to improve the thermal

resolution, firstly, the LNA should have a low noise figure and high gain. Such that the overall noise figure can be controlled by the LNA. Secondly, both the LNA and the mixer should have a large bandwidth. Thirdly, a longer integration time is also desired, and the typical value for the integration time is 30ms. Based on (1.7), Fig. 1.6 plots the “ $T_s$  vs.  $NETD$ ” curves for each given bandwidth. From such a plot, one can select a targeted specification to ensure an  $NETD$  less than 0.5 K.



**Figure 1.6 Plot of the system noise temperature ( $T_s$ ) versus the noise equivalent temperature difference ( $NETD$ ) for different bandwidths.**

As seen in Fig. 1.6, a  $T_s$  of 1000 K can make all the  $NETD$ s stay below 0.4 K. This outcome is quite satisfactory. It seems that as long as  $T_s$  is kept at 1000 K, even a bandwidth of 10 GHz can yield an  $NETD$  of 0.34 K. However, in a more realistic case, unwanted losses caused by the passive components and the gain fluctuation may add additional noise temperature. Therefore, in order to create enough room for the link budget, for  $T_s$  of 1000 K, the bandwidth is

selected to be 30 GHz. This yields a 0.2 K NETD, which means it creates a 0.3 K link budget. The gain of the LNA should be large enough in order to minimize the noise figure of the following stages. Therefore, the gain of the LNA is targeted at 20 dB. Correspondingly, the noise figure of the mixer should be less than 20 dB. Additionally, to ensure that the output power of the LNA does not saturate the mixer's input and to avoid unwanted noise being folded to the baseband, the linearity of the mixer, quantified by 1-dB compression point, is targeted at -5 dBm. Table 1.3 summarizes the design specifications for components used for the passive imaging application.

**Table 1.3 Design Specifications of the LNA and Mixer for Passive Imaging Application**

<i>Component</i>	<i>Bandwidth</i>	<i>Gain</i>	<i>Noise Figure</i>	<i>1-dB Compression Point</i>
<i>LNA</i>	<i>30 GHz</i>	<i>25 dB</i>	<i>6.5 dB</i>	<i>-5 dBm</i>
<i>Mixer</i>	<i>30 GHz</i>	<i>0 dB</i>	<i>15 dB</i>	<i>-10 dBm</i>

### **1.3 Contributions**

1. One of the subjects that this thesis focuses on is the analysis and design of millimeter-wave LNAs. Based on the classical noise theory, formulas for analyzing the feedback effect on noise performance have been derived. This is the first time that one completely summarizes and derives such formulas. The deducing procedure is elegant and simple. The deduced formulas further expand

the classical two-port network noise theory to more practical cases. This work was presented in the International Conference on Electronics, Information and Communication 2013.

2. Based on theoretical analysis, a dual-band LNA designed for automotive radars has been proposed. The dual-band LNA achieves a relatively low noise figure and consumes very little dc power. More importantly, the proposed combination method makes the best possible use of the two frequency-bands, thus further expanding the functionality for the radar receiver. As the first reported dual-band CMOS LNA, its attributes of low power and compact size outstand itself as a new green solution for electric vehicles. This work was presented in the International Conference on Electronics, Information and Communication 2013.
3. As discussed in section 1.2, the dual-band system seeks for high performance dual-band power dividers. The 24/77- GHz dual-band system sets a stringent requirement for its corresponding dividers. For passive devices, it is difficult for them to cover such a wide bandwidth. Therefore, in order to achieve a better integration, higher sensitivity and angular resolution for the dual-band receiver, a novel design of a dual-band lumped Wilkinson power divider is proposed. As well known, a conventional Wilkinson power divider normally occupies a large chip area. Developed from conventional Wilkinson power divider, a miniaturized Wilkinson power divider is proposed. The compact power divider works effectively at the two frequency bands. This work was presented in the IEEE

Midwest Symposium on Circuits and Systems, 2013. It is the first reported 24-/77-GHz Wilkinson power divider.

4. For millimeter-wave applications on passive imaging, the system requires the LNA to attain a wide operating frequency range and to possess a small noise figure. A 94 GHz LNA is designed to meet such a demand. It focuses on the refinement work for the first stage of the LNA, regarding the first stage as the LNA's LNA. The conventional stagger tuning method has been modified in order to achieve a broad operating bandwidth. As a result, the bandwidth is extended to 30 GHz, within which the gain is kept above 22 dB. The noise figure is minimized to 5.1 dB. According to the discussion in section 1.2, the proposed LNA has more competence than other CMOS LNAs to help a bolometer achieve an NETD of 0.5 K. This work has been accepted by the Journal of Infrared, Millimeter, and Terahertz Waves, Springer, January 2016 (IF=1.942).
5. Directly down-converting a millimeter-wave frequency requires the local oscillator to supply the same high frequency signal with enough output power, which is impractical. To relax the stringent requirement on the local oscillator side, a subharmonic mixer is usually used in a millimeter-wave front-end. However, subharmonic mixers normally need a coupler, which occupies a large chip area. In addition, subharmonic mixers have poor gain performance, which potentially increases the noise figure. To address the preceding issues, a novel design of a W-band mixer is proposed in this thesis. The proposed mixer has satisfactory performance over the entire W-band. Moreover, it does not need a

coupler, which greatly saves the chip area and reduces the design periods. This work has been published in the IEEE Microwave and Wireless Component Letter, June 2015 (IF=1.703).

## **1.4 Organization**

The thesis is organized as follows.

Chapter 2 is an overview part. Selected works on automotive radars and passive imaging are reviewed.

Chapter 3 prepares the fundamentals for front-end components designs.

Chapter 4 is an extension of the fundamentals given in Chapter 3. It provides useful formulas to analyze the noise performance of an LNA which is connected to a feedback network. The work introduced in this chapter has been presented in the International Conference on Electronics, Information and Communication, 2013.

Chapter 5 proposes a narrow-band LNA. The LNA operates at 24/77 GHz, which can be used in an automotive radar. The work introduced in this chapter has been presented in the International Conference on Electronics, Information and Communication, 2013.

Chapter 6 proposes a dual-band Wilkinson power divider, and its topology is inspired by the loading network of the LNA presented in Chapter 5. The work introduced in this chapter has been presented in the IEEE 56th International Midwest Symposium on Circuits and Systems, 2013.

Chapter 7 continues refinement work on the millimeter-wave front-end. This chapter proposes a method for wideband millimeter-wave LNA designs. A 94 GHz LNA is presented in this chapter. The work introduced in this chapter has been accepted by the Journal of Infrared, Millimeter, and Terahertz Waves, Springer, January 2016.

Chapter 8 focuses on another important component in a millimeter-wave front-end, i.e. the mixer. The mixer is the second and the last active device in a front-end chain. Without the mixer, the millimeter waves received by the LNA cannot be processed by the baseband. In this regards, a design of a W-band mixer is proposed. The mixer adopts a new topology, which lends the mixer satisfactory performance over the entire W-band. The proposed mixer could either be used for a 77 GHz radar or a bolometer operating at 94 GHz. The work introduced in this chapter has been published in the IEEE Microwave and Wireless Components Letters, June, 2015.

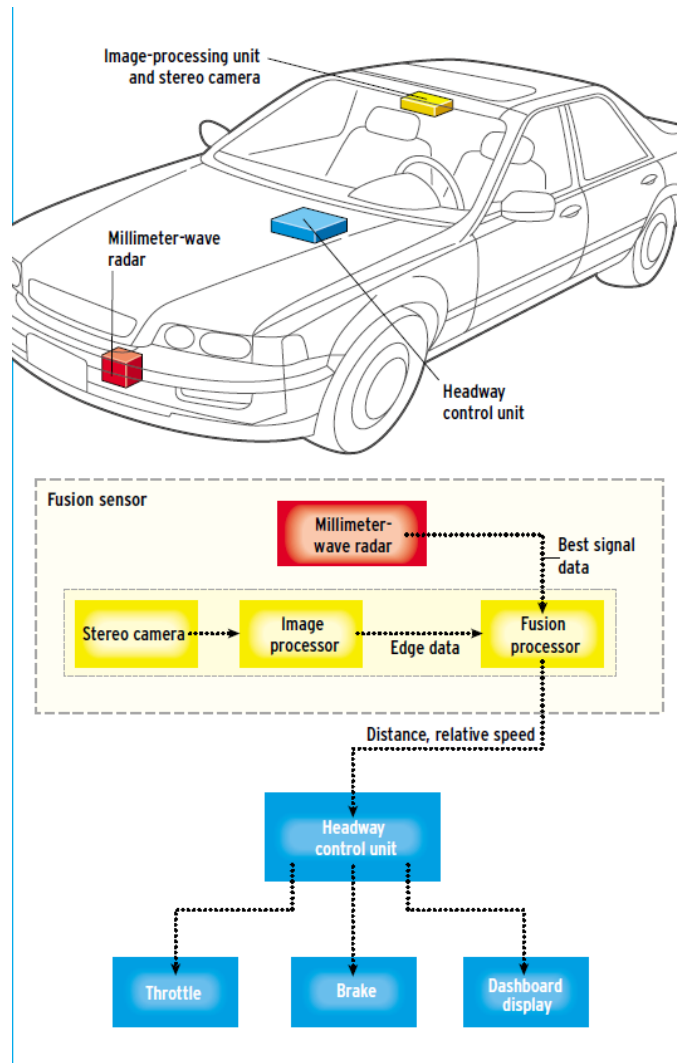
## **Chapter 2**

# **Literature Review of Millimeter-Wave Applications on Automotive Radar and 94 GHz Passive Imaging**

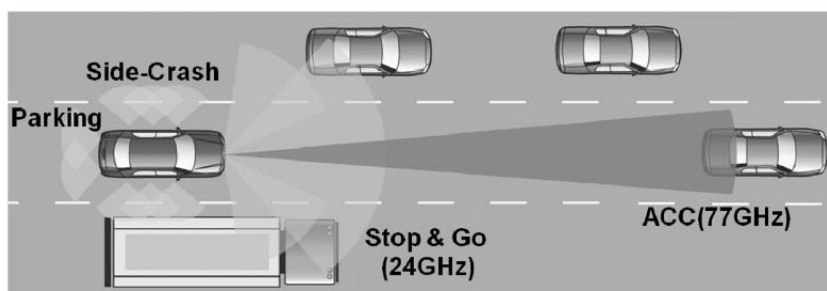
This chapter provides a literature review on two specific millimeter-wave applications introduced in Chapter 1. First, detailed working principles of the two applications are explained. Next, selected works corresponding to each specific application are discussed.

### **2.1 Overview of Automotive Radar**

In September 2011, IEEE Spectrum shared an interesting article [5]. The content can be a good starting point to render an overall picture of working principles of the automotive radar. [5] introduces the development history of the automotive radar and provides examples of commercialized automotive radars. Fig. 2.1, cited from [5] and [14], illustrates how an automotive radar works.



(a)



(b)

Figure 2.1 Illustration of an automotive radar's working principles. [5] [14]

Referring to Fig. 2.1(a) and (b), imagine that one is driving in bad weather

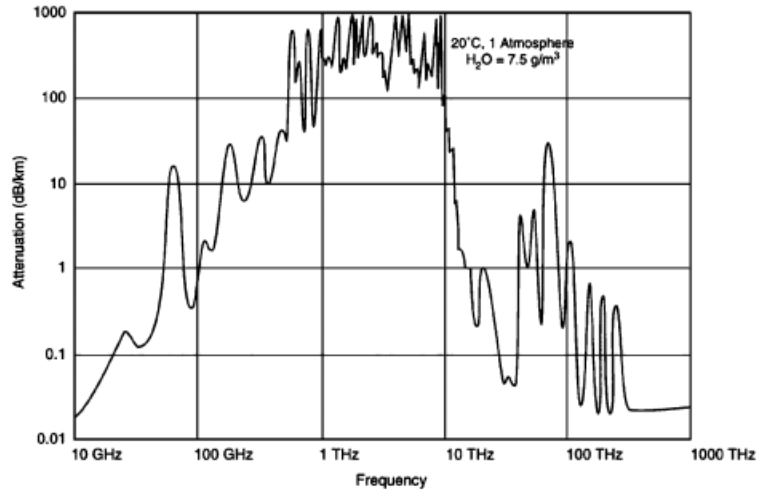
conditions, e.g. in fog or heavy rain. In such conditions, by transmitting and receiving a continuous millimeter-wave, the automotive radar can "see" at least 100-150 meters. The millimeter-wave, after being processed by the baseband, will command the car either to open the throttle (accelerate) or to slow down the speed (brake). As mentioned in [5], the advantage of an automotive radar implemented in CMOS is that the millimeter-wave front-end and the baseband circuitry can henceforth be combined together, thus saving on cost.

[14] provides a more detailed description on an automotive radar's working principle. As shown in Fig. 2.1(b), the short-range radar operating at 24 GHz helps with parking and parallel driving. It avoids impacts to the sides of a car. The long-range radar operating at 77 GHz measures the distance and the speed of the car in front. Correspondingly, as determined by the received signals, the car can either accelerate or decelerate, automatically.

## **2.2 Overview of Millimeter-Wave Application at 94 GHz**

Section 2.1 introduced one millimeter-wave application for vehicles. Another important millimeter-wave application includes the passive imaging [2] [15]. Millimeter-waves provide two atmosphere windows, which are well under the coverage of a 65-nm MOS transistor's transition- frequency range. The atmosphere window refers to those frequency ranges where the transmission attenuation is relatively low, compared to their adjacent frequencies [6]. As shown in Fig. 2.2(a) and (b), around the frequencies of 35 GHz and 94 GHz, the

attenuation seems suitable for the millimeter-wave transmission. Therefore, these two frequency ranges are referred to as atmosphere windows.



(a)

Frequency THz	Attenuation db/km
0.035	0.15
0.094	0.6
0.140	2
0.220	8
1	500
10	100

(b)

**Figure 2.2 (a) The plot of atmosphere windows; (b) attenuation versus frequency. [6]**

The 94 GHz atmosphere window is more suitable for passive imaging applications, mainly because the antenna dimension is inversely proportional to the operating frequency [8]. Regarding the large-scale arrays in an imaging system, an antenna with a small dimension can help to increase pixels for a given

area, thus partially improving the resolution of the imaging system.

Unlike automotive radars, passive imaging systems do not need transmitters. This may sound good at first, since it effortlessly solves the millimeter-wave generation problem. Millimeter-waves, in this case, are all provided by nature. At such high frequencies, lightweight materials such as cloths, plastics and smoke become transparent to millimeter-waves. Therefore, the millimeter-wave imaging can help with security scanning and surveillance. Moreover, at the millimeter-wave frequency range, materials radiate a fixed pattern known as the resonance signature. As a result, by using a millimeter-wave receiver, materials can be identified

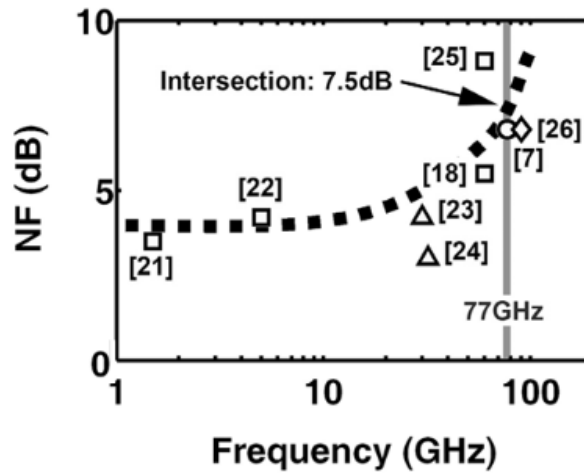
It seems as though millimeter-wave passive imaging avoids the trouble of designing high frequency local oscillators (LO), and it is also very useful in many respects, as pointed out earlier, however, such applications set high standards on the receiver's front-end performance [16]. The receiver must possess high performance regarding the noise figure and operating frequency- range.

## **2.3 Low-Noise Amplifiers for Automotive Radars**

Section 2.2 and 2.3 have provided an overview of two millimeter-wave applications. This section and the following provide an overview of individual component designs. It first begins with the LNAs in automotive radars.

The recommended specifications for an LNA operating at 77 GHz are given in Chapter 1.2. Additionally, as evaluated by [14] shown in Fig. 2.3, the noise figure

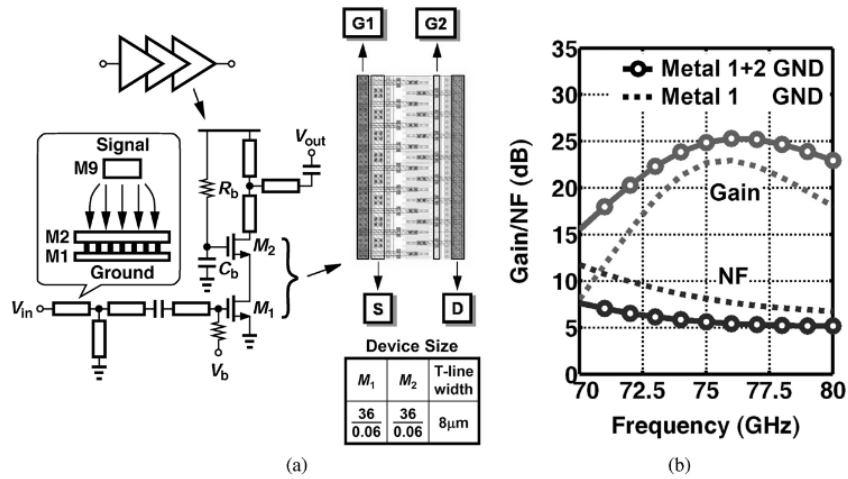
(NF) of an LNA operating at 77 GHz should be kept below 10 dB. In addition, in [14], the gain of the LNA should be greater than 18 dB.



**Figure 2.3** The plot of the commended noise figure versus frequency. [14]

There are already some 77-GHZ-LNA designs. The following section provides a review of three typical designs.

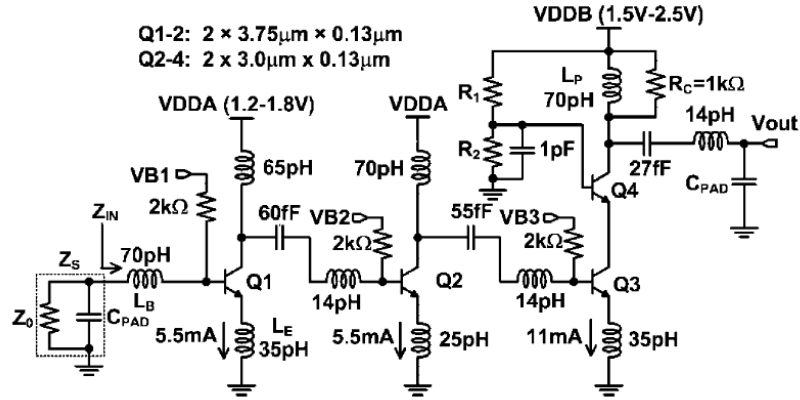
The first selected design was proposed in [14] and has been implemented in a 65-nm CMOS technology. The topology is redrawn in Fig. 2.4(a).



**Figure 2.4. (a) The configuration of the proposed LNA and its corresponding layout, and (b) the plot of the noise figure and gain versus frequency. [14]**

As shown in Fig. 2.4(a), the LNA consists of three stages, all in cascode configurations. Its input and output ports are both conjugatively matched. Transmission lines replace inductors as parts of the matching network. However, a transmission line with a relatively long length suffers from substrate-loss issues. For example, at 77 GHz, the skin depth is about 0.25  $\mu$ m, but the thickness of the ground metal is 0.07  $\mu$ m smaller than the skin depth. Regarding such an issue, the ground metal and its neighbor metal are thereby combined together to reduce the loss, as shown in Fig. 2.4(a). By using such a combination, the noise figure could be significantly reduced, as plotted in Fig. 2.4(b). The cascode amplifier in [14] adopts a layout topology known as the multi-interdigital-gate transistor [17]. It claims that this configuration can greatly reduce the parasitic capacitance. Source degeneration is not used in [14], because it decreases the gain.

The second selected design was proposed by [18]. It was implemented in a 0.13- $\mu\text{m}$  SiGe HBT technology. Fig. 2.5 depicts the schematic.



**Figure 2.5. A BJT LNA proposed by [18].**

The first two stages are common-emitter amplifiers. The cascode structure is not adopted for the first two stages, because [18] fears that this might increase the noise figure. [18] finds a way to achieve the noise- and source-matching simultaneously. Moreover, in order to reduce the power consumption, the power supply is scaled to a minimum value by properly choosing the resistance of  $R_1$  and  $R_2$ . The ratio of  $R_1$  and  $R_2$  is given by

$$\frac{R_1}{R_2} \leq \frac{V_{DDB-MIN}}{V_{BE-ON} + V_{CE-SAT}} - 1 \quad (2.1)$$

When designing the input matching network, [18] shows that the pad capacitance cannot be neglected. The capacitance of the pad has been extracted.

[18] demonstrates that the pad capacitance is comparable to the input capacitance.

Consequently, the source impedance should be more accurately expressed as:

$$Z_S = \frac{Z_O}{k} - j \frac{\omega C_{PAD} Z_O^2}{k}, \quad (2.2)$$

$$k = 1 + \omega^2 C_{PAD}^2 Z_O^2. \quad (2.3)$$

The expression of the input impedance is given by (2.4) ~ (2.6):

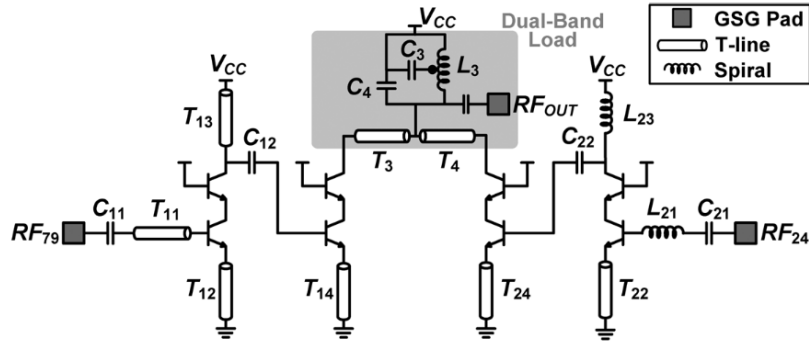
$$Z_{IN} = R_{B1} + R_{E1} + \omega_T L_E + j(\omega L_E + \omega L_B - \frac{\omega_T}{\omega^2 g_{m1}}), \quad (2.4)$$

$$L_E = \frac{1}{\omega_T} \left( \frac{Z_O}{k} - R_{B1} - R_{E1} \right), \quad (2.5)$$

$$L_B = \frac{Z_O^2 C_{PAD}}{k} - L_E + \frac{\omega_T}{\omega^2 g_{m1}}. \quad (2.6)$$

According to the expression of the source and input impedance, it becomes possible to achieve noise and source matching at the same time, by properly adjusting the emitter length.

The third selected design was proposed by [19] and is a dual-band LNA, implemented in a 0.18- $\mu\text{m}$  SiGe HBT technology, as shown in Fig. 2.6. For the first time, LNAs in the short- range and long-range radars are combined together on a single chip.



**Figure 2.6. The schematic of a BJT dual-band LNA proposed by [19].**

As shown in Fig. 2.6, the dual-band LNA consists of two LNAs. One is for the short-range radar and another for the long-range radar. The two LNAs are combined together by one loading network designed as a dual-band filter. It provides two peaks at 24 GHz and 77 GHz. The LNA's design method is similar to previous examples given in [14], [18].

## 2.4 Low-Noise Amplifier at 94 GHz

As mentioned in section 2.2, the millimeter-wave front-end for passive imaging highly depends on the performance of noise and bandwidth. This increases one's pressure on designing high performance LNAs. Additionally, the design method is different from the preceding examples. In this regard, this section provides a macroscopic description of 94 GHz LNAs. Later chapters provide detailed discussions.

Before delving into details, a parameter that judges the performance of a passive-imaging receiver is best revisited first. Since passive imaging systems are used to measure the thermal radiation, its thermal resolution is considered to

be the most important specification.

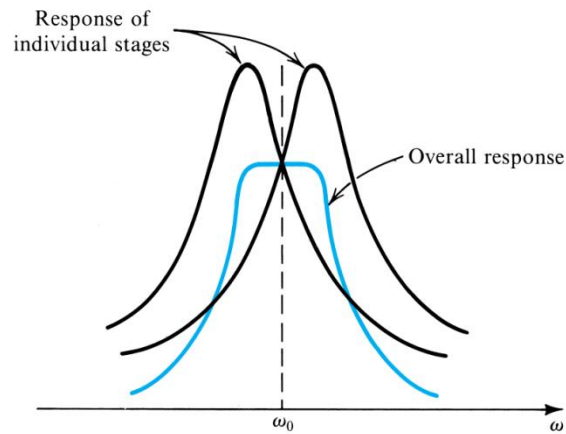
NETD quantifies the thermal resolution, as introduced in Chapter 1. A more complete form of NETD could be defined as:

$$\text{NETD} = T_S \sqrt{\frac{1}{B\tau} + \left(\frac{\Delta G}{G}\right)^2}, \quad (2.7)$$

where  $B$  depends on the bandwidth of the LNA,  $\tau$  is integration time depending on the video-rate, and  $T_S$  refers to the system noise temperature which relies on the noise performance of the LNA.  $G$  is the gain of the LNA, and  $\Delta G$  is the fluctuation of the gain, which can be alleviated using a Dicke Switch [16] [20]. As discussed in Chapter 1, the LNA should cover a wideband and have a very low noise figure.

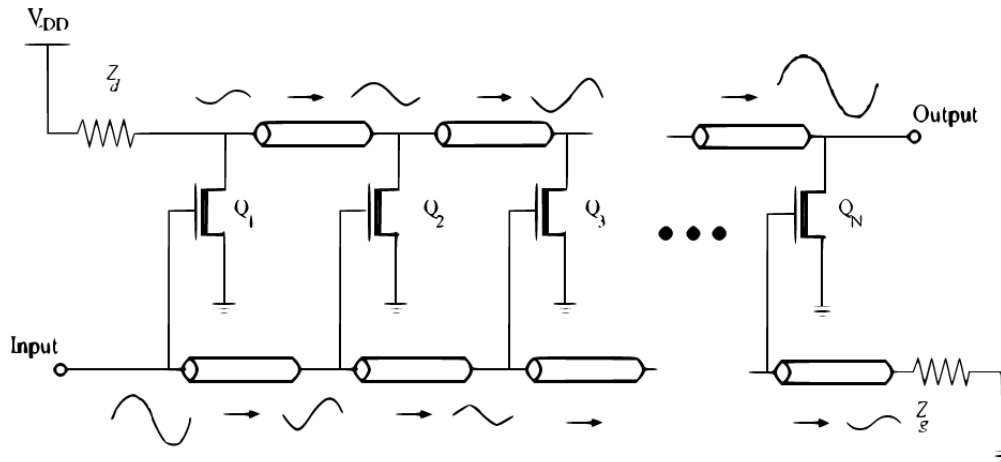
The following sections provide two typical topologies adopted by 94 GHz LNAs. Both consist of multi-stage amplifiers. Configurations of an individual amplifier is similar to the ones in section 2.3.

The first topology that a 94 GHz LNA can adopt is called a staggered tuning. Regarding the frequency at 94 GHz, hardly any MOS transistor can cover such a high frequency point with its cut-off frequency. Therefore, in order to achieve a broadband frequency response, the amplifier always consists of several tuned-amplifiers. Each tuned amplifier resonates at a different frequency point. When combined together, the cascaded amplifier could hence achieve a broadband frequency response, as illustrated in Fig. 2.7 [21].



**Figure 2.7 The principle of the staggered tuning amplification. [21]**

The second topology is referred to as a distributed configuration, as shown in Fig. 2.8. Referring to Fig. 2.8, imagine that a sinusoid wave is applied at the input terminal. That wave then propagates along the input transmission lines. Consequently, a succession of sinusoidal waves is imposed at the gate terminal of each MOS transistor. That gate voltage is then transformed to a drain current. Ultimately, these currents are accumulated in time coherence, providing an amplified signal at output.



**Figure 2.8 Illustration of the distributed amplification [22].**

Distributed topology is not currently commonly used, probably due to the elaborate procedure of transmission-line designs and the Miller effect caused by the drain to gate capacitor. [22]

## 2.5 W-band Mixer Design

Previous sections have provided overviews of the LNA's topologies. As mentioned earlier, the mixer is also a critical component for a front-end. At the millimeter-wave frequency range, especially when it comes to the frequencies above V-band, CMOS mixers are practically configured in a subharmonic topology. After all, subharmonic is often the only option available at extremely high frequencies, due to the millimeter-wave generation problems with respects to the LO side.

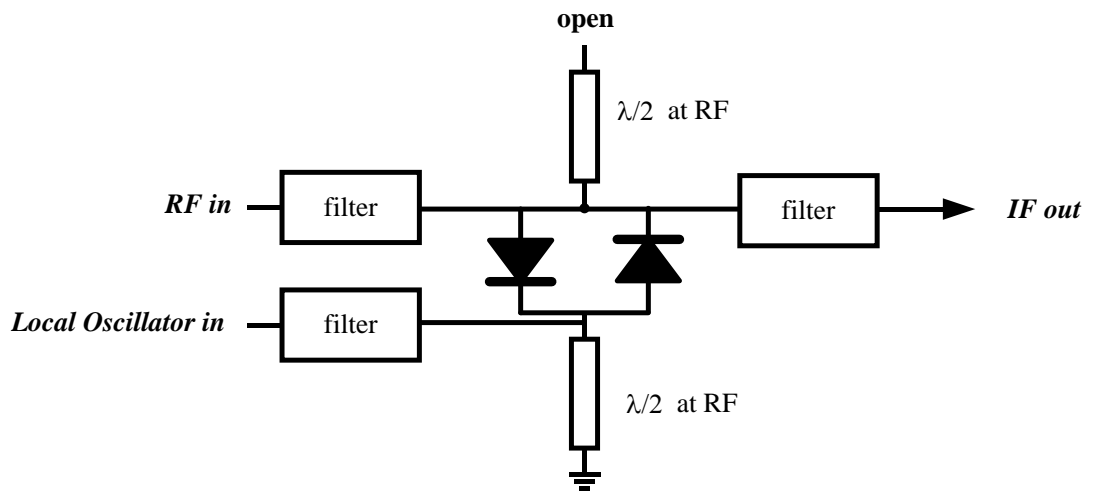
Working principles of the subharmonic mixer are summarized below [22] [23]. More details are provided in later chapters.

There are two common ways to realize a subharmonic mixer. One solution is

to take advantage of nonlinearities. After all, nonlinearities are hard to avoid, so it is much better to exploit them. For example, suppose the mixer needs an LO drive with a frequency  $f_l$ , but it turns out to be impractical or inconvenient to acquire this. One could use a nonlinear element to generate harmonics of that frequency, then use a filter to select the harmonic desired, and use that signal to drive a mixer.

An alternative method is to take advantage of the spur modes, which are generally present in practical mixer circuits. In this case, the LO port is driven at a frequency  $f_l/N$ . The spur mode corresponding to the LO's  $N$ th harmonic is then selected.

The usual goal of the mixer's design is to suppress spur modes, but in subharmonic mixers the spur mode is enhanced. An example is shown in Fig. 2.9. Assume that the RF input signal and the desired LO frequency are so close that they may be treated as equal. Furthermore, assume that the LO actually supplied is at half this frequency, so that the subharmonic's order  $N=2$ . The open-circuited transmission line in the upper portion of the circuit thus presents an open circuit for the desired RF signal but a short circuit to the LO drive that is supplied. The voltage across the diodes is thus the sum of the RF input signal and the LO drive. The use of two diodes connected in inverse parallel fashion assures an enhancement of even-mode spurs. The low-pass IF filter does its best to remove undesired hash, but its ability to do so is limited, precisely because of the spur-mode enhancement inherent in this architecture.



**Figure 2.9** An example of the subharmonic mixer ( $N=2$ ). [22]

## 2.6 Summary

This chapter first provides a brief overview of two millimeter-wave applications followed by a brief explanation of their working principles.

Secondly, critical components have been briefly introduced.

# Chapter 3

## Fundamentals of LNA and Mixer Designs

Previous chapters discussed how the LNA and mixer are critical components for a millimeter-wave front-end. The LNA determines the overall noise performance. The mixer, followed by the LNA, translates the frequency to baseband for further processing. This chapter illustrates fundamentals for LNA and mixer designs.

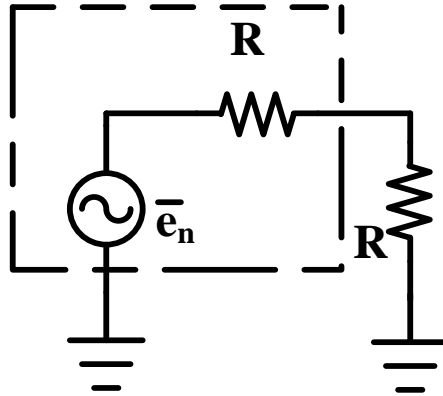
### 3.1 Thermal Noise

Before delving into the specific LNA designs, it is better to study the noise behaviors at first. After all, the LNA is supposed to deal with noise. The most commonly seen noise is the thermal noise [24]. Therefore, in this section, thermal noise basics are summarized mainly based on the work done by Dr. Aldert van der Ziel [24].

Thermal noise is the most commonly seen noise. It is a result of Brownian motion, i.e. thermally agitated charge-carriers in a conductor constitute a randomly varying current, which gives rise to a random voltage. This type of noise is also called Johnson noise or Nyquist noise, in recognition of its finders. The thermal noise's power is in proportion to temperature, as described by (3.1):

$$P_{NA} = kT\Delta f, \quad (3.1)$$

where  $k$  is Boltzmann's constant and  $\Delta f$  is the noise bandwidth. The subscription,  $NA$ , is short for the available noise power. The available noise power is the maximum power that can be delivered to the load, as illustrated in Fig. 3.1.



**Figure 3.1 Illustration of the definition of available noise power.**

As shown in Fig. 3.1, a noise voltage generator is enclosed by the dashed box, which is in series with a resistor. The available noise power is the amount of power that can be delivered to another resistor outside the dashed box, as given by:

$$P_{NA} = kT\Delta f = \frac{\overline{e_n^2}}{4R}, \quad (3.2)$$

where  $\overline{e_n^2}$  is the open-circuit rms noise voltage. It is generated by the resistor  $R$

in the dashed box, and covers a bandwidth of  $\Delta f$  at a given temperature,  $T$ .

Based on (3.2), the following relationship holds:

$$\overline{e_n^2} = 4kT\Delta f. \quad (3.3)$$

Additionally, dividing (3.3) by  $\Delta f$  could yield the expression of the noise spectral density.

Furthermore, it is noteworthy that the thermal noise is always considered “white”, which suggests that its spectrum is always a flat line, as implied by (3.3). However, more accurately speaking, its spectral density increases with frequency [24]. A more accurate expression of (3.3) is as follows.

$$\overline{e_n^2} = \frac{h\omega R\Delta f}{\pi} \coth\left(\frac{h\omega}{4\pi kT}\right), \quad (3.4)$$

where  $h$  is Plank’s constant.

The good news is that there is hardly any difference between (3.4) and  $4kT\Delta f$ , if the frequency is below 80 THz. Therefore, (3.3) is valid for most cases.

Additionally, thermal noise does not exist in pure reactive elements. It is only associated with resistors. The next section covers the topic on noise sources in MOS transistors.

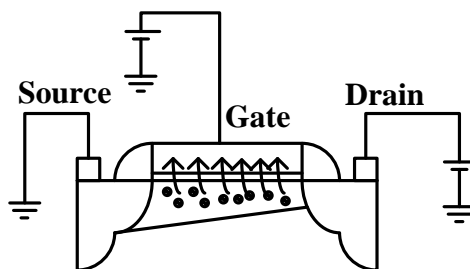
There are two thermal-noise sources dominating in an MOS transistor. Their mechanisms are introduced respectively as follows.

As earlier mentioned, thermal noise only exists in resistors. This section deals with noise in MOS transistors. MOS transistors are known as active devices. In addition, they could also be treated as voltage-controlled resistors. Therefore, MOS transistors exhibit noise. Especially when operating in the triode region, MOS transistors are more like a resistor in that case. Thus, it can be postulated that, its noise behavior is similar to what (3.3) describes. As revealed in [37], the drain noise current is expressed as:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \quad (3.5)$$

where  $g_{d0}$  is the drain-source conductance when the drain to source voltage is zero. The parameter  $\gamma$  roughly equals 1 to 2 for the short channel MOS transistor.

The drain noise current is not the only noise source in an MOS transistor. The MOS transistor's gate terminal exhibits noise, too. The gate noise is agitated by the channel charges. As shown in Fig. 3.2, the thermal agitation causes the charge to fluctuate. The fluctuation, in turn, capacitively couples to the gate terminal, forming a noisy current.



**Figure 3.2 Illustration of gate noise.**

Gate noise can be expressed as [37]:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f, \quad (3.6)$$

where  $\delta$  is called the gate noise coefficient, with an empirical value of 2 to 4 for short channel MOS transistors, and  $g_g$  is called the gate noise resistance and is expressed as:

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}. \quad (3.7)$$

Equation (3.6) implies that the spectral density of the gate noise is not “white”. It increases with frequency. To make the expression simpler, (3.6) can be expressed in terms of voltage, as given in (3.8). When expressed in volts, the spectral density of the noise voltage becomes “white” as well.

$$\overline{v_{ng}^2} = 4kT\delta r_g \Delta f, \quad (3.8)$$

where  $r_g$  approximately equals  $1/5g_{d0}$ .

## 3.2 Shot Noise

Apart from the thermal noise, another type of noise called shot noise was first identified and explained by Schottky in 1918. For this reason, sometimes it is

also called Schottky noise. [26]

Two conditions have to be satisfied in order to make this type of noise happen: (1) a DC flow, and (2) a potential barrier, which could enable the electrons to hop over. The second condition implies that shot noise does not exist in devices that do not transport electrons via the pn junction. The expression for the shot noise is given by

$$\overline{i_n^2} = 2qTI_{DC}\Delta f, \quad (3.9)$$

where  $\overline{i_n}$  is the rms noise current,  $q$  is the electron charge,  $I_{DC}$  is the DC current. For MOS transistors, only the gate leakage current causes shot noise, concerning the two conditions mentioned above. The leakage is negligible. Therefore, shot noise is not a significant noise source.

### 3.3 Flicker Noise

Flicker noise, also known as the  $1/f$  noise, remains the most mysterious type of noise. Therefore, this section describes flicker noise empirically. [24]

Flicker noise can be found in resistors. It is also known as  $1/f$  noise or the “excess noise”, because the flicker noise is in addition to the thermal noise. The resistor exhibits  $1/f$  noise only when there is a DC current, therefore, passive mixers usually have a low noise figure. The empirical expression for flicker noise in resistors is:

$$\overline{e_n^2} = \frac{K}{f} \cdot \frac{R_{sheet}^2}{A} \cdot V^2 \Delta f, \quad (3.10)$$

where  $A$  is the area of that resistor,  $R_{sheet}$  is the sheet resistivity,  $V$  is the voltage across the resistor and  $K$  is a constant defined by the material property.

MOS transistors exhibit  $1/f$  noise, too. They are surface devices. As a result, the possibility of charge-trapping tends to be very high, which means that the  $1/f$  noise is much stronger in MOS transistors than in BJT transistors. One way to ameliorate the  $1/f$  noise issue for an MOS transistor is to increase its size, because a larger capacitance can smooth the fluctuation of the noise current. Therefore, in order to achieve good  $1/f$  noise performance, the device size should be larger.

The expression of mean-square  $1/f$  drain noise current is:

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{W_L g C_{OX}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f, \quad (3.11)$$

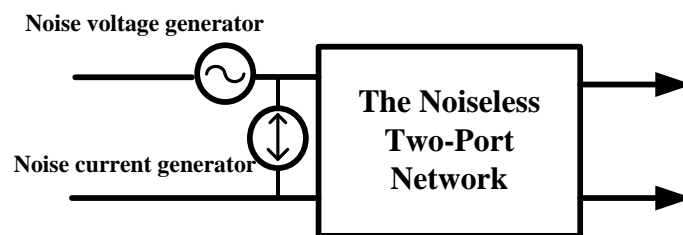
where  $A$  is the gate area and  $K$  is a constant. It suggests that the larger gate area, the smaller the noise. For PMOS devices,  $K$  is typically 50 times smaller than NMOS devices.

In sum, flicker noise has less impact on a millimeter-wave LNA. Regarding mixer designs, it is better not to directly down-convert the millimeter-wave to DC which exhibits a large amount of  $1/f$  noise.

### 3.4 Classical Two-Port Noise Theory

Previous sections reviewed noise sources in MOS transistors. This section examines noise behavior more broadly with a noise model in a two-port network. Noise sources within the network are all simplified to two equivalent noise generators. Such an analysis can offer useful design insights. [39]

The analysis begins with the definition of the noise figure. Noise figure is used to judge the noise performance or the sensitivity. Its definition is as follows.



**Figure 3.3. A noisy two-port network represented by two noise generators and a noiseless two-port network.**

As shown in Fig. 3.3, the net effect of all internal noise sources are represented by a pair of external generators: a noise voltage generator and a noise current generator. Thanks to this simplification, the extent to which the source admittance could affect the overall noise performance can henceforth be readily estimated.

The noise figure,  $NF$ , is the ratio of the total output noise power to the output noise power due to the input source:

$$NF \equiv \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad (3.12)$$

where the source is at a temperature of 290 K.

Noise figure is a measure of the degradation of the signal-to-noise ratio. The larger the degradation, the larger the noise figure. Regarding Fig. 3.3, its noise figure is:

$$F = \frac{\overline{i_s^2 + |i_n + Y_s e_n|^2}}{i_s^2}, \quad (3.13)$$

where  $i_n$  is

$$i_n = i_c + i_u. \quad (3.14)$$

In (3.14),  $i_c$  is correlated with the noise voltage generator, and  $i_u$  is uncorrelated with the noise voltage generator.

Since  $i_c$  and  $e_n$  are correlated with each other, the following expression holds.

$$i_c = Y_c e_n, \quad (3.15)$$

where  $Y_c$  is the correlated admittance which links  $i_c$  and  $e_n$ .

Based on (3.12) ~ (3.14), (3.13) can be expressed as

$$F = \frac{\overline{i_s^2 + |i_u + (Y_c + Y_s)e_n|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2 + |(Y_c + Y_s)|^2 e_n^2}}{\overline{i_s^2}}. \quad (3.16)$$

Equation (3.16) contains three independent noise sources. Each can be treated as a resistor:

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f}, \quad (3.17)$$

$$G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f}, \quad (3.18)$$

$$G_s \equiv \frac{\overline{i_s^2}}{4kT\Delta f}. \quad (3.19)$$

Substituting (3.17) ~ (3.19) for (3.16), (3.16) could be rewritten as,

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s}. \quad (3.20)$$

In (3.20), the admittance is summed by two elements, e.g. the conductance  $G$  and the susceptance  $B$ . Taking the first derivative of (3.19) with respect to the source admittance, and equaling that derivative to zero, yields

$$B_c = -B_s = B_{opt}, \quad (3.21)$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt}. \quad (3.22)$$

Therefore, to minimize the noise figure, the source susceptance should be made equal the inverse of the correlation susceptance, and the source conductance should be made equal  $\sqrt{\frac{G_u}{R_n} + G_c^2}$ .

If conditions set by (3.21) and (3.22) are both satisfied, the minimum noise figure can be acquired, as given by:

$$F_{min} = 1 + 2R_n[G_{opt} + G_c] = 1 + 2R_n \left[ \sqrt{\frac{G_u}{R_n} + G_c^2} + G_c \right]. \quad (3.23)$$

### 3.5 Noise Figure of Cascade of Stages

Section 3.4 has described the noise performance with regard to a single stage. This section describes the noise performance with respect to a cascade of stages. As well known, LNA is located at the first stage in a front-end chain. Its performance directly determines the overall noise figure of a receiver. The overall noise figure of a receiver can be calculated using Friis' noise formula [12]. For example, if there is an  $m$ -stage receiver, the overall noise figure is

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \dots + \frac{NF_m - 1}{A_{p1}A_{p2}\dots A_{pm}}, \quad (3.24)$$

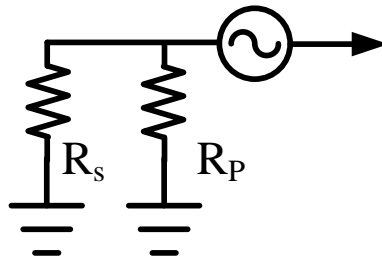
where  $A_{pi}$  denotes the available power gain of the  $i^{th}$  stage. As obviously shown in (3.24), the LNA is a critical element, since noise figures of subsequent stages

are all divided by its gain. Therefore, the gain of the LNA should be high enough, in order to minimize noise figures of following stages. This suggests that, for millimeter-wave LNA designs, where the MOS transistors normally lack sufficient intrinsic gain, some gain-boosting techniques have to be employed.

### 3.6 LNA Configurations

Previous sections have introduced some basic noise sources revealing that the noise limits the sensitivity of a millimeter-wave front-end. Therefore, one uses an LNA to optimize the front-end's noise performance. This section reviews fundamental LNA configurations.

The first topology, proposed by [40], uses a resistor to match the source impedance at input. Using this method, the input impedance could be easily matched to  $50\ \Omega$ . However, the noise performance could drastically deteriorate with this method. The reason is as follows. Fig. 3.4 shows the input stage of an LNA terminated by a resistor  $R_p$ . The following calculations show that this topology should be avoided for the millimeter-wave LNA design.



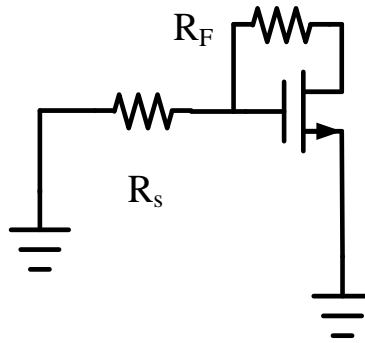
**Figure 3.4.** A matching method by directly placing a resistor at input.

According to (3.12), the noise figure at the input stage is,

$$NF = 1 + \frac{R_S}{R_P}. \quad (3.25)$$

As seen in (3.25), if  $R_S = R_P$ , the noise figure would be at least 3 dB. Since the input stage alone has contributed a noise figure of 3 dB, the overall noise figure could be in excess of 11 dB [28].

The second topology is a common-source amplifier with a resistive feedback network, as shown in Fig. 3.5 [29]–[31]. Instead of terminating a resistor at the input, this topology employs a series-shunt feedback network.



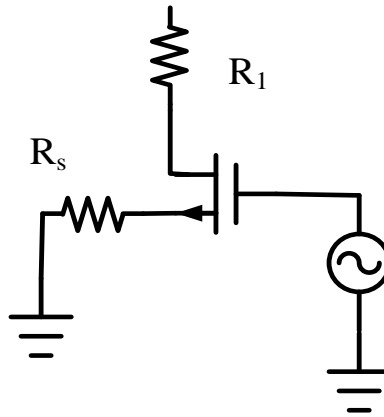
**Figure 3.5. An amplifier configured by series-shunt feedback.**

The noise figure of this topology is:

$$NF \approx 1 + \frac{4R_S}{R_F} + \gamma + \gamma g_{m2} R_S. \quad (3.26)$$

By observing (3.26), one can find that even when  $\gamma \approx 1$ , the first two terms have already contributed a noise figure greater than 3 dB. Therefore, this configuration is also not suitable for a millimeter-wave LNA.

The third topology is based on a common-gate amplifier [32]–[34]. It is suitable for the ultra-wide-bandwidth applications, but its noise figure still remains high. The simplified structure of the common-gate stage is shown in Fig. 3.6.



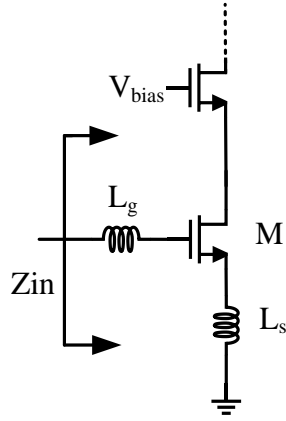
**Figure 3.6 The configuration of a common-gate LNA.**

The noise figure can be calculated, as given by:

$$NF = 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1} \left(1 + \frac{1}{g_m R_S}\right)^2 = 1 + \gamma + 4 \frac{R_S}{R_1}. \quad (3.27)$$

Unfortunately, its noise figure is still undesirably high.

The fourth topology [47], shown in Fig. 3.7, is a common-source amplifier with a source degenerated inductor.



**Figure 3.7. A common-source amplifier with a source degenerated inductor.**

Referring to Fig. 3.7, its input impedance  $Z_{in}$  is:

$$Z_{in} = s(L_S + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_S. \quad (3.28)$$

Equation (3.28) provides a design insight for input matching. At resonance,  $s(L_S + L_g) + \frac{1}{sC_{gs}}$  is zero. It turns out that the input impedance at such resonance is only determined by the term  $\left(\frac{g_{m1}}{C_{gs}}\right)L_S$ . Therefore, by properly choosing the inductance of  $L_S$ , the input impedance can be set to  $50 \Omega$ . After a little labored calculation, the noise figure can be found by:

$$NF = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2, \quad (3.29)$$

where  $R_l$  and  $R_g$  represent resistance loss in the inductor.

Equation (3.29) indicates that this topology offers the lowest noise figure among all topologies.

### 3.7 Mixer Configurations

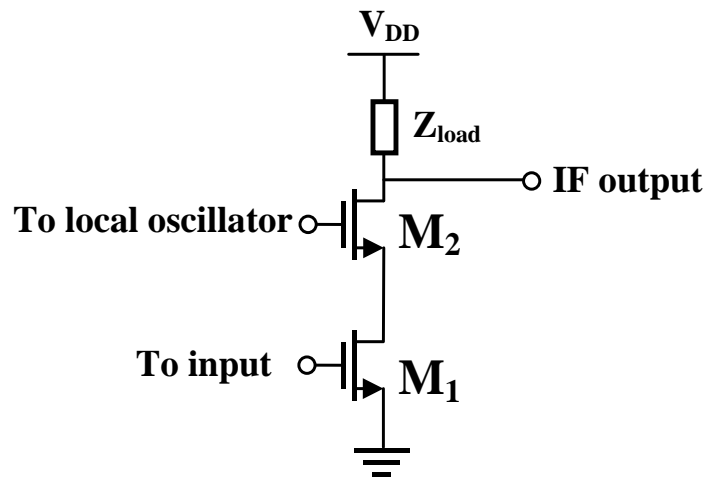
Previous sections covered topics on linear, time-invariant designs. Additionally, the high performance of a millimeter-wave front-end depends critically on the presence of one time-variant component, i.e. the mixer. After being amplified by the LNA, millimeter-waves need a mixer to perform the important frequency translation. This section describes some typical mixer configurations in the millimeter-wave frequency range.

At the core of all mixers presently in use is a multiplication of two signals in the time domain. The fundamental usefulness of multiplication may be understood by examine the following trigonometric identity:

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2} [\cos(\omega_1 - \omega_2) t + \cos(\omega_1 + \omega_2) t]. \quad (3.30)$$

The multiplication in (3.30) yields a result which contains the sum and difference frequencies of the input. Therefore, if  $\omega_1 \geq \omega_2$ , such a multiplication can be treated as a down-conversion process. MOS transistor's fast-and-low-resistance switching-potential can be exploited to realize such a multiplication [36]. However, as mentioned in Chapter 2, the LO performance limits the

practical use of conventional CMOS mixers at the millimeter-wave frequencies. As a result, subharmonic mixers prevail in this frequency range. As mentioned in Chapter 2, the subharmonic mixer exploits the MOS transistor's nonlinearity. The enhanced spur mode in turn relaxes the stringent requirement on the LO side. Before introducing the subharmonic mixer, it is best to review a configuration referring to another type of mixer, i.e. the dual-gate mixer. Most CMOS subharmonic mixers evolve from this. An example of a CMOS dual-gate mixer is given in Fig. 3.8 [22].

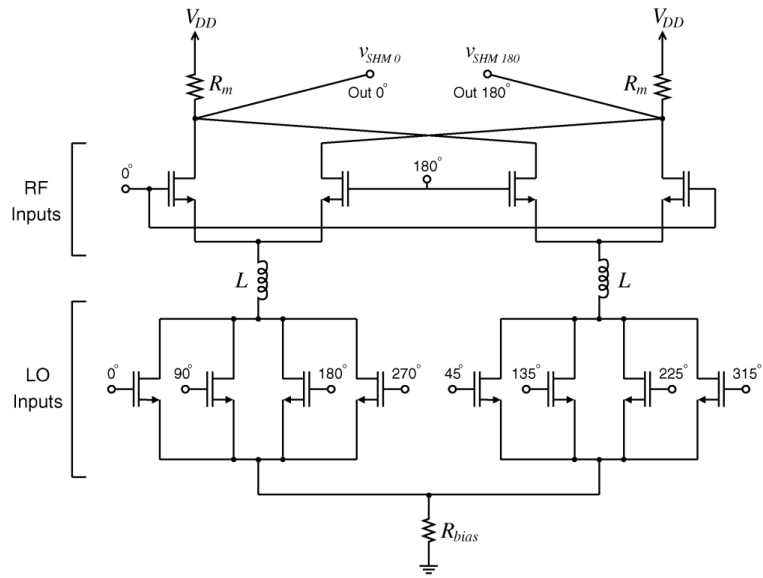


**Figure 3.8 A dual-gate mixer [22].**

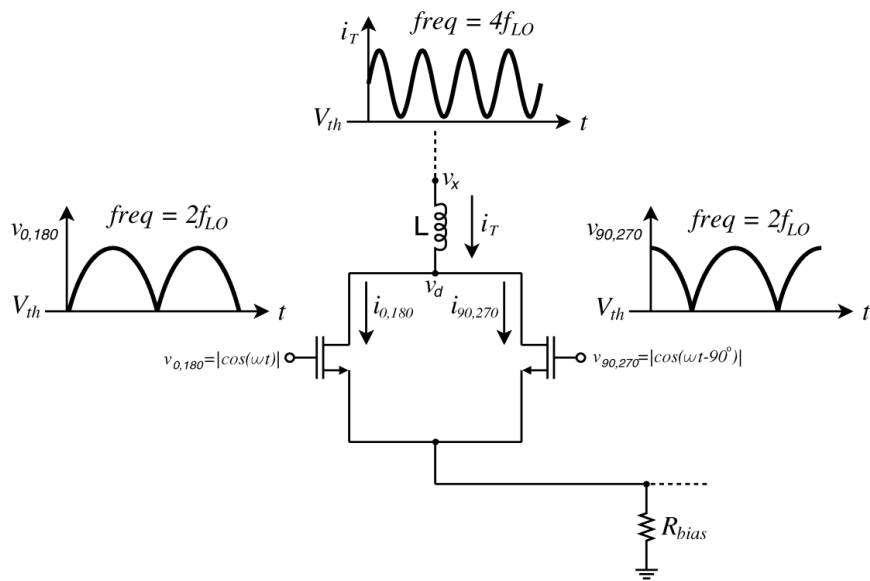
In the circuit given in Fig. 3.8,  $M_1$  functions as a transconductor with deliberately poor output resistance; it is generally biased to operate in the triode region. With that choice of bias, the LO drive applied to  $M_2$  causes the drain current, and resistance, of  $M_1$  to vary at the LO rate. The drain current of  $M_1$  (and

hence of  $M_2$ ) thus contains components at the sum and difference frequencies, thus implementing the multiplication expressed by (3.30).

One typical configuration of a CMOS subharmonic mixer evolves from the dual-gate mixer, as shown in Fig. 3.9 [37]. Similar to a dual-gate mixer, in Fig. 3.9(a), the drain current of the LO transistors deliberately disturbs the biasing condition of the input transistors. As a result, the output current carries a difference frequency of the input and the LO frequency. The configuration shown in Fig. 3.9(b) explains how such a configuration could free the LO drive from supplying a very high frequency. By applying quadrature signals to the gate terminals, as shown in Fig. 3.9(b), at the output, a current component is created, whose frequency is four times higher than the LO rate. Therefore, in such a configuration, the LO rate only needs to be one fourth of that input frequency. The disadvantage of this type of mixer is obvious. Since the 4x frequency rate is achieved by superposing the harmonics, its gain is usually poor.



(a)



(b)

Figure 3.9 (a) A typical CMOS subharmonic mixer, and (b) the working principle of a CMOS subharmonic mixer. [37]

### **3.8 Discussions on Existing Refinement Works for Millimeter-Wave LNA and Mixer Designs**

The sections in this chapter and Chapter 2 have reviewed the fundamentals for LNA and mixer designs. During the course of study, following design considerations for millimeter-wave LNA and mixer designs can be observed.

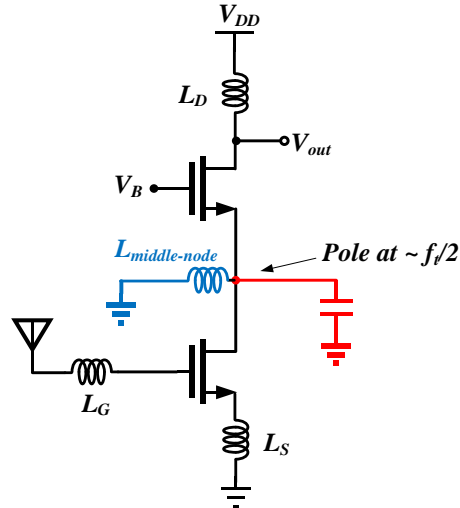
1. According to the Friis formula, the LNA must present little noise. However, this requirement becomes difficult to satisfy for the millimeter-wave designs. Because the operating frequency is approaching a transistor's transition frequency, which will aggressively deteriorate the transistor's minimum noise figure. Therefore, for the millimeter-wave LNA design, how to minimize the noise figure becomes one of the primary concerns.
2. To help the LNA achieve a satisfactory gain performance is another primary concern. For an NMOS transistor fabricated in a CMOS 65nm technology, it is conceivable that the poles caused by the parasitic capacitors will start to worsen the gain performance.
3. Regarding the application on passive imaging, the LNA's bandwidth plays a critical role in determining the thermal resolution. However, for an NMOS transistor fabricated in a 65nm CMOS technology, its cut-off frequency is much lower than the W-band frequencies. Therefore, how to extend the bandwidth becomes one's another primary concern.
4. A millimeter-wave mixer suffers from the noise issue as well, which is even worse than what the LNA suffers. As the nature of mixing, noise at undesired

frequencies can be downconverted to the baseband. If the mixer has a poor linearity, the noise figure will be increased. The lack of a high performance commercial LO drive above the V-band limits the mixer performance as well. For example, regarding a Gilbert-cell mixer, the insufficient output power of the LO drive will prolong the period where both of the NMOS switches are turned on. Consequently, it causes the conversion gain to fall and increases the noise figure at the same time.

These observations are based on the design philosophy and theory introduced in previous chapters. To deepen the understanding of the millimeter-wave circuit design techniques, typical solutions to address the aforementioned issues are critically reviewed in the following parts.

The design examples of LNA are introduced first. As discussed in section 3.6, in high frequency amplifier designs, the common-source topology is more widely used if low noise is one's prime goal.

The schematic shown in Fig. 3.10 extends the bandwidth of a conventional cascode amplifier by placing an additional inductor in its middle node [38]. This is because at such high frequencies the gate to drain parasitic capacitance is comparable to the gate to source capacitance. Correspondingly, a pole at half of the transistor's transition frequency will be created. The shunt inductor is thus used to tune out the parasitic capacitors in order to extend the bandwidth.



**Figure 3.10 A shunt inductor used to extend the bandwidth of a cascode amplifier. [38]**

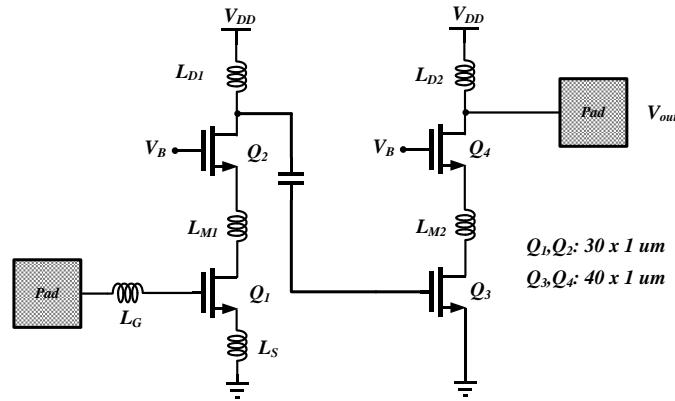
Although the method in Fig. 3.10 can extend the bandwidth, its effect is limited and it suffers from the noise issue at the extremes of frequencies. This is because the bandwidth of the resonance is narrow. Additionally, the single stage LNA cannot provide enough gain. Thus, it may not fully suppress the noise figure of subsequent stages. In order to significantly broaden the bandwidth and suppress the noise figure of the following stages, the stagger tuning method introduced in Chapter 2 can be applied. [39] shows a two-stage LNA in a 90nm CMOS technology. The schematic is reproduced in Fig. 3.11. To minimize the noise figure, the bias current is set to an optimum point. To achieve a simultaneously noise and power match, the transistors have been resized. It emphasizes that in the millimeter-wave frequency range, the effect of parasitic passives, especially the pad capacitance, must be included in the design consideration. Otherwise, the results would seriously deviate from the true values. Unlike [38], it places the inductor in series with the transistors. As a result, the

inductor and the parasitic capacitors can form a lumped transmission line. It is known that the transmission line covers a wider frequency range than the inductor does. Therefore, compared to the previous method, such a modification further improves the bandwidth. All in all, its design procedure can be summarized as follows and such a method can be either frequency scaled to higher frequencies or can be ported to another technology node.

1. Choose an optimum size for the transistor.
2. Find an optimum current density which can yield the minimum noise figure.
3. Use inductors to resonate out parasitic capacitors and insert the inductor at the middle node to further broaden the bandwidth.
4. Cascade the cascode amplifiers to achieve a wide frequency response.

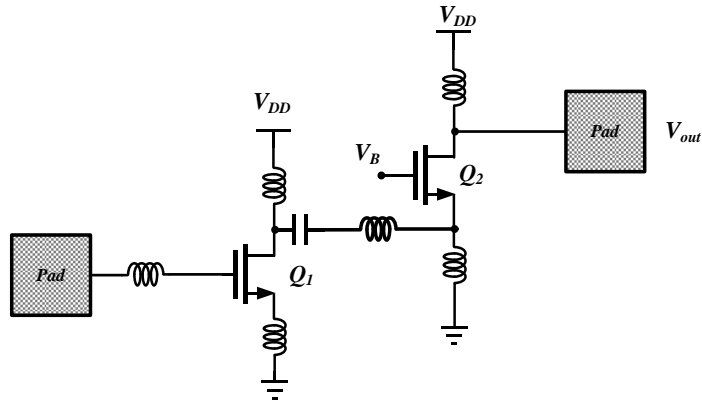
Although such a method is simple in configuration and can achieve a simultaneous noise and power match, it still has potential drawbacks and room for refinement. Firstly, once the transistor is resized, the gate width then becomes unchangeable. According to the device theory, the larger the size, the higher the minimum noise figure [26]. Secondly, it neglects that the matching network corresponding to the optimum gate width may significantly deteriorate the noise performance. For example, if one blindly aims at noise matching, the corresponding matching network may incur an even bigger noise figure. Thirdly, the series inductor used to broaden the bandwidth can also be used to improve the noise performance. As a load of the common-source transistor, the series inductor can boost the gain of the common-source transistor. Consequently, noise

figure of subsequent stages can be further minimized.



**Figure 3.11 Noise and bandwidth refinements for a cascade of cascode amplifiers. [39]**

As mentioned above, referring to Fig. 3.11, improving the gain of  $Q_1$  can further suppress the noise figure of the following stages. Therefore, another topology shown in Fig. 3.12 can be adopted to boost the gain of the common-source transistor [40]. This topology is originally proposed to address the issue of low power supply in more advanced technology node. In this topology, the cascode configuration is decomposed to two single stages. Since the common-source stage now becomes a standalone amplifier, its gain can be fully used to suppress the noise figure of subsequent stages. The drawback of this topology is obvious. Because many passives are involved in the design, the chip size will become unwillingly large.

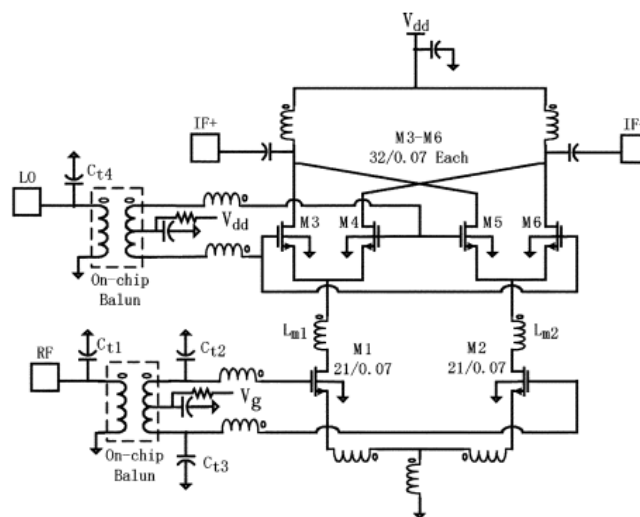


**Figure 3.12 A folded cascode amplifier. [40]**

The circuit examples of the millimeter-wave LNA discussed above can provide the following design insights. Firstly, the noise performance of the LNA can be optimized by properly resizing the transistor's gate width. Secondly, in order to achieve a wideband frequency response, the stagger tuning method is found to be more useful at the millimeter-wave frequency range. If one needs a wideband frequency response down to DC and the noise issue is not the primary goal, the common-gate topology can be employed. Thirdly, the issue of lack of gain becomes serious as the frequency increases. The lack of gain not only decreases the output power but also increases the noise figure according to the Friis noise formula. For completeness, Table 3.1 summarizes more works pertaining to millimeter-wave LNA designs.

After reviewing the millimeter-wave LNA examples, the following part selects some refinements done for the millimeter-wave mixer designs. As earlier mentioned, the mixer needs refinements at the millimeter-wave frequencies as well.

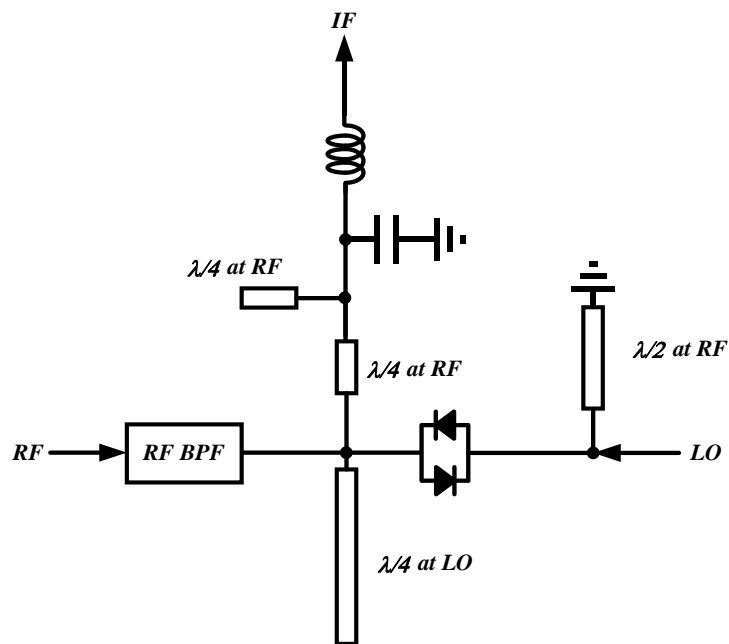
The first example is a conventional Gilbert-cell mixer as shown in Fig. 3.13 [41]. This work is the first work that demonstrates how to frequency scale the design of a Gilbert-cell mixer from low frequencies to the W-band. It is conceivable that at such a high-frequency band, the local oscillator cannot provide enough power to fully turn on or off the switch pairs in the Gilbert-cell. Consequently, the gain and noise performance become mediocre. Also note that since the active mixer naturally possesses a higher noise figure than the passive ones due to the bias current, in Fig. 3.13,  $M_1$  and  $M_2$  are constructed as a low-noise amplifier. However, such a refinement requires seven inductors to implement: not only does it prolong the design iteration, but also the chip area increases.



**Figure 3.13 A W-band Gilbert-cell mixer. [41]**

The second design refers to a conventional subharmonic mixer as shown in Fig. 3.14 [42]. Its working principle is similar to the one shown in Fig. 2.9. The

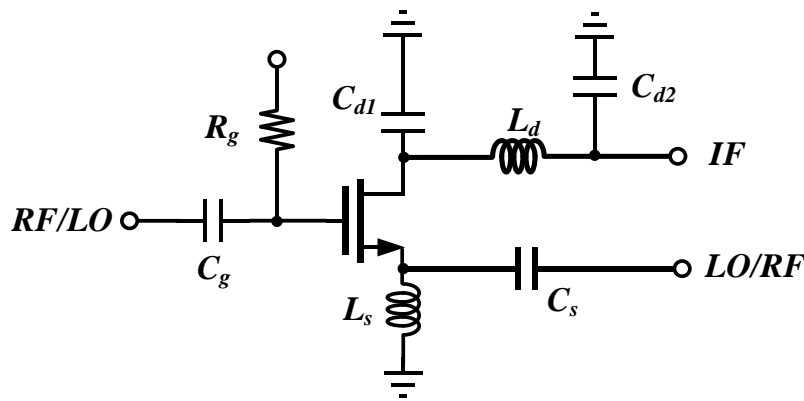
circuit is simple and can easily suppress RF even harmonics without any DC power. However, for a commercial CMOS technology, it is impractical to implement a high performance Schottky diode. Moreover, the quarter- and half-wavelength transmission lines occupy a large chip area. In recent years, the pumped resistive CMOS mixers have gained increasing attention. Compared to the diode subharmonic mixer, the pumped resistive CMOS mixer occupies a smaller chip area and can operate in a wider frequency range.



**Figure 3.14 A conventional subharmonic mixer implemented by diodes.**  
[42]

[43] proposes an NMOS subharmonic mixer. The schematic is reproduced in Fig. 3.15. As shown in Fig. 3.15, the RF and the LO signals can be applied either at the gate terminal or at the source terminal. For example, when the LO signal is injected at the source terminal, the gate to drain transconductance varies

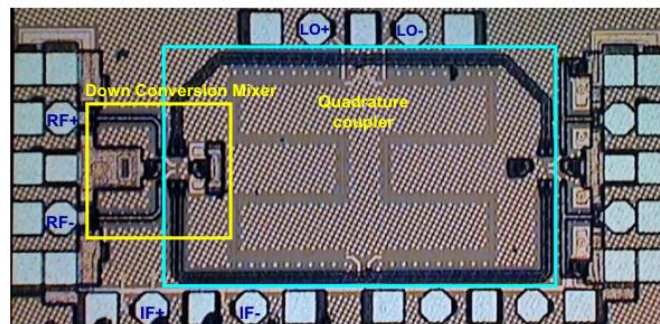
accordingly. Consequently, the desired subharmonic component will be pumped out at the drain terminal. The IF signal then can be selected out by the  $\pi$ -network,  $L_D$ ,  $C_{D1}$  and  $C_{D2}$ . Although this type of mixer can operate in a wide frequency range and achieve good linearity, it still has some potential drawbacks. Firstly, it cannot maintain a relatively low conversion loss, because the IF signal depends on the pumped harmonic, which normally has a poor amplitude. Secondly, since the RF, LO and IF signals are all applied to a single transistor, it may have very poor port-to-port isolations.



**Figure 3.15 A subharmonic mixer by the pumping method. [43]**

To overcome the aforementioned issues, the subharmonic mixer [37] introduced in section 3.7 can be frequency scaled to the millimeter-wave frequencies. [44] proposes a 4x CMOS subharmonic mixer. The working principle is similar to the one in [37]. The 4x harmonic frequency component is generated by the quadrature LO signals. In [37] where the operating frequency is relatively low, the quadrature LO signals are obtained by the RC poly phase shifters. The frequency response of an RC phase shifter is narrow and the loss is

high when the operating frequency increases. To achieve a broadband frequency response and to reduce the power loss, a coupler is needed at the millimeter-wave frequencies. However, as shown in Fig. 3.16, because the size of the coupler is proportional to the wavelength, it usually occupies a large chip area [44]. In Table 3.1, more existing millimeter-wave mixer designs have been summarized.



**Figure 3.16 Die photo of a subharmonic consisting of a quadrature coupler.**  
[44]

**Table 3.1 Performance Summary of Some Millimeter-Wave LNAs and**

**Mixers**

Reference	Device Name	Peak Gain (dB)	Operating Freq. (GHz)	NF (dB)	OP <sub>1dB</sub> (dBm)	Technologies
[14]	LNA <sup>1</sup>	17.5	73.5-77.1	6.8	-5.5	65-nm CMOS
[18]	LNA <sup>2</sup>	25	82-89	4.8	N/A	0.13-um SiGe
[45]	LNA <sup>2</sup>	14.6	72-84	6.2	N/A	90-nm CMOS
[46]	LNA <sup>1</sup>	18.5	43-53	2.9	3	45-nm SOI CMOS
[47]	LNA <sup>1</sup>	32	89-92	5.1	-12.8	28-nm CMOS
[48]	LNA <sup>1</sup>	16.3	77	15.6	N/A	90-nm CMOS
[7]	LNA <sup>1</sup>	27	83-93	6.8	N/A	65-nm CMOS
[49]	LNA <sup>1</sup>	45	77-101	6	0.2	0.13-um SiGe
[23]	Mixer <sup>3</sup>	0	30-100	N/A	-9.6	90-nm CMOS
[50]	Mixer <sup>4</sup>	20.7	10-67	16.5	-8.8	65-nm CMOS
[51]	Mixer <sup>3</sup>	-4.7	85-92	N/A	N/A	GaAs HEMT
[52]	Mixer <sup>4</sup>	24	65-90.8	7	-4	0.18-um SiGe
[53]	Mixer <sup>3</sup>	0.7	75-81	20	-8	0.8-um SiGe
[43]	Mixer <sup>3</sup>	11	9-31	N/A	-3	90-nm CMOS
[54]	Mixer <sup>4</sup>	5	25-75	N/A	-4	65-nm CMOS
[41]	Mixer <sup>4</sup>	-1.5	76-77	8.3	-7	65-nm CMOS
[55]	Mixer <sup>4</sup>	6	74-98	8	-16.5	65-nm CMOS

*Notes: The superscripts refer to the following configurations: “1” denotes the cascode configuration. “2” denotes the common source configuration. “3” denotes the subharmonic mixer. “4” denotes the Gilbert-cell configuration.*

Regarding the LNA designs, although [14] reduces the noise figure by

increasing its ground thickness, it seems that this method has not been widely adopted. This may be due to two reasons. Firstly, this method increases the layout complexity. Secondly, its improvement on the noise figure is limited. In contrast, the substrate loss can be significantly reduced by employing a silicon-on-insulator technology [46]. Regarding the gain performance, the listed LNAs accumulate the power gain via the staggering method. As seen in Table 3.1, for most LNA designs, the gain is above 20 dB, in order to fully suppress the noise figure of the mixer. If the gain-enhancement is not applied in the first stage, following stages then can have some effects on the overall noise figure. Regarding the mixer designs, although conventional Gilbert-cell mixers, as shown by [41] and [55], provide limited power gain, it is difficult to implement a corresponding high-performance LO at such a high frequency range. Although subharmonic mixers solve the millimeter-wave generation problem, as shown by [51] and [53], the gain performance is poor and the indispensable phase-shifters of a subharmonic mixer increases the design burden.

As seen in Table 3.1, with respect to LNA designs, the common-source and cascode configurations are widely adopted. Compared to other configurations, such configurations provide higher intrinsic gain and maintain a relatively low noise figure for the millimeter-wave LNAs [1] [12]. Linearity performance (measured by the output 1-dB compression point,  $OP_{1dB}$ ) deteriorates when the gain increases. Such an issue, however, has limited effects on the overall performance of a millimeter-wave LNA. Recall that in (1.7), as for the passive

imaging application, NETD is not determined by the linearity performance. Moreover, for the millimeter-wave communication, the communication interference is unlikely to happen [4] [55]. Regarding the mixer designs, subharmonic types usually have a higher loss. Gilbert-cell mixers, on the other hand, possess relatively higher gain, due to the amplification transistor connected to the switching pair. For mixer designs, linearity performance matters. As seen in Table 3.1, good linearity performance tends to benefit the noise performance. This is because good linearity can further reduce the unwanted harmonic spurs, and as a result, there is a lower amount of thermal noise being carried to the baseband [22].

In conclusion, regarding the LNA design for the automotive application, there have not yet been any reported CMOS LNA that can both cover the 24-/77-GHz frequency band. One can conceive a loading network that has two resonance peaks at 24- and 77-GHz. The dual-band receiver introduced in the previous chapter employs a transformer to construct a dual-band loading [19]. However, the design of a transformer will add more design iterations. Since it is a narrowband LNA, a fourth-order filter is competent enough to provide two resonance peaks. As seen in Table 3.1, it is not a stringent requirement for a CMOS LNA to have a noise figure of 8 dB. Therefore, the configuration of the LNA can be a conventional cascode amplifier similar to the one proposed in [14]. Moreover, [18] proposed the noise matching technique for a BJT LNA. One can employ such a technique and applies it to a dual-band CMOS LNA design.

Regarding the LNA design for passive imaging. In order to extend the bandwidth, it is best employs the stagger tuning method as adopted by all the LNAs listed in Table 3.1. To further minimize the noise figure, the first stage of the LNA should be well optimized. Regarding the mixer design, although there are reported Gilbert-cell mixers operating in the W-band, as mentioned earlier, it is impractical to design a high performance CMOS LO. Therefore, the intended mixer should be a subharmonic mixer. It is best to be a passive mixer so as to improve the noise and linearity performance.

### **3.9 Summary**

This chapter outlined the basics of millimeter-wave front-end designs. Firstly, common types of noise sources were reviewed. In conclusion, in an MOS transistor, drain noise dominates the overall noise performance. Gate noise has some impact on the millimeter-wave frequency range and its noise resistance has to be taken in to account when performing the noise-matching technique. Flicker noise exists at very low frequencies, therefore, regarding the mixer designs, the IF frequency should be kept away from the DC frequencies. Secondly, typical topologies commonly adopted by LNAs and mixers were reviewed. Thirdly, it specifically discussed the design issues for the millimeter-wave LNAs and mixers. With respect to components in a millimeter-wave CMOS front-end, additional refinement work is needed in order to achieve higher performance.

# Chapter 4

## Formulas for Analyzing Effects of Feedback on Noise Performance

Chapter 3 introduced noise models in two ways. One was to focus on the individual device, and another from a macroscopic angle, i.e. the classical two-port noise theory. The individual noise model provides guidance on deciding the dimension of an MOS transistor. The classical two-port network noise theory simplifies circuit analysis, and in turn, offers useful design insight for a specific design. This chapter continues the study on the two-port network noise theory, relating it to a more practical situation.

### 4.1 Introduction

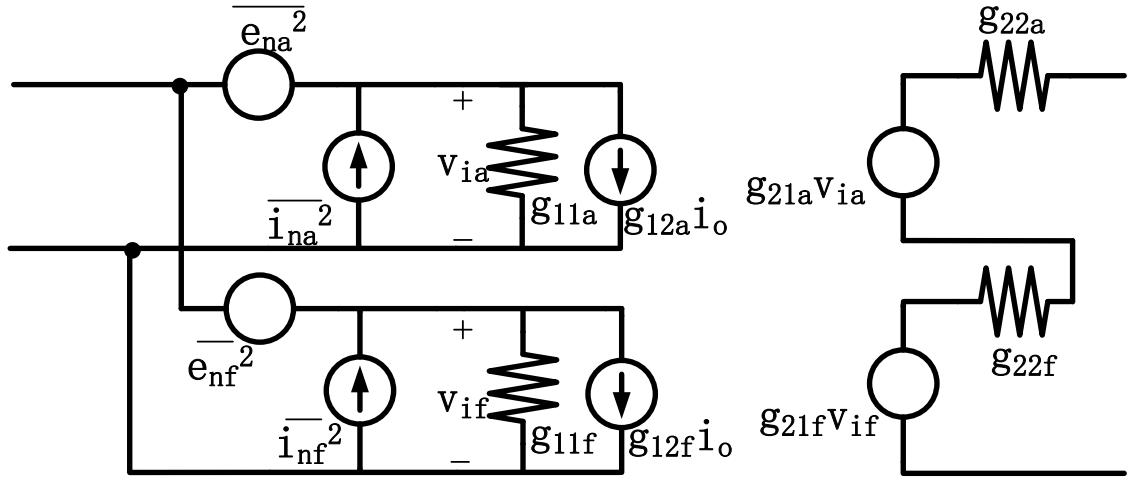
Formulas that can be used to analyze noise behaviors of a two-port network were given in Chapter 3. However, in most cases, the situation may be a little more complicated, because the two-port network is usually associated with a feedback network. For this reason, concerning the effect of feedback on noise performance, this chapter provides formulas along with a detailed deducing procedure. Feedback of all configurations is taken into consideration, i.e. the shunt-series, series-shunt, series-series, and shunt-shunt feedback.

The deduced formulas are useful. As mentioned in Chapter 3, noise sources inside any two-port network can be represented by two noise generators at the

input. Such simplification offers design insights from a system-view. For example, the expression of the minimum noise figure is obtained from this. However, few if any articles have concentrated on the situation where the two-port network is combined with a certain type of feedback. Although [55]–[58] covers this subject a little bit, their analysis is either hard to understand or lacks completeness. The purpose of this chapter is thus to provide formulas for measuring the noise performance of a two-port network with all types of feedback, from the inside out. Moreover, the formulas are deduced in a simpler and more explicit way.

## 4.2 Formula Deduction Procedure

First, consider the case of a shunt-series feedback. In this case, there are two two-port networks. One is a basic amplifier, which is subscripted by “ $a$ ”. Another is the feedback network, which is subscripted by “ $f$ ”. The two networks are connected in a shunt-series topology, as depicted in Fig. 4.1.



**Figure 4.1. Shunt-series feedback represented by two two-port networks**

Since the two networks share a common input voltage and output current, hybrid- $g$  parameters can be used to analyze such a configuration.

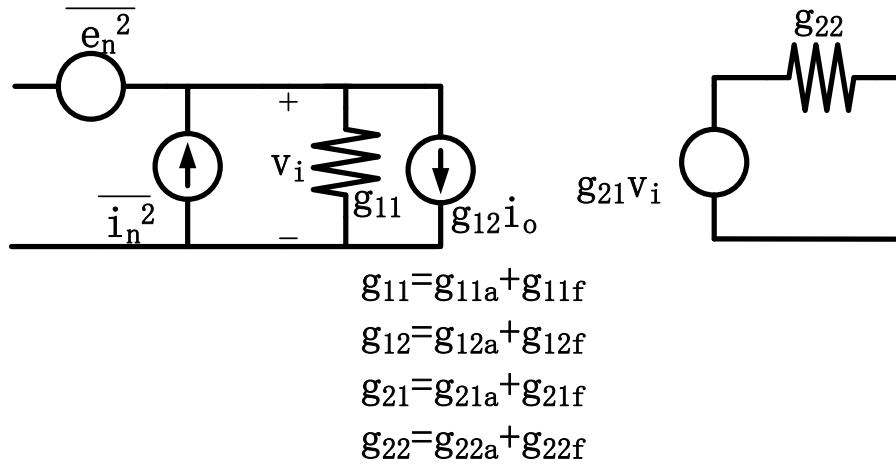
The two networks shown in Fig. 4.1 can be combined, by applying the hybrid- $g$  parameters to each network, as shown in Fig. 4.2. The hybrid- $g$  parameters are given in (4.1) ~ (4.4).

$$g_{11} = g_{11a} + g_{11f}, \quad (4.1)$$

$$g_{12} = g_{12a} + g_{12f}, \quad (4.2)$$

$$g_{21} = g_{21a} + g_{21f}, \quad (4.3)$$

$$g_{22} = g_{21a} + g_{21f}. \quad (4.4)$$



**Figure 4.2.** The noise equivalent circuit of Figure 4.1.

The circuit in Fig. 4.2 is similar to the circuit in Fig. 3.3. This suggests that all the noise sources inside the two-port network shown in Fig. 4.2, can also be simplified to two equivalent noise generators at the input, i.e.  $\bar{e}_n$  and  $\bar{i}_n$ . The value of  $\bar{e}_n$  can be found by short-circuiting the input of each circuit in Fig. 4.1 and 4.2, and then equating their output currents, as described in (4.5)~(4.8). When the input terminals in Fig. 4.1 and 4.2 are shorted, both noise current generators,  $\bar{i}_{na}$  and  $\bar{i}_{nf}$ , are shorted as well. Consequently, in Fig. 4.1, the output current is excited by the noise voltage generators, i.e.  $\bar{e}_{na}$  and  $\bar{e}_{nf}$ . The expressions of the output current are:

$$i_{out \text{ in Fig. 14}} \Big|_{\text{input-shortcd}} = \frac{g_{21f}\bar{e}_{nf} + g_{21a}\bar{e}_{na}}{g_{22a} + g_{22f}}, \quad (4.5)$$

and,

$$i_{out \text{ in Fig.15}} \Big|_{\text{input-shortcd}} = \frac{g_{21}\bar{e}_n}{g_{22}}. \quad (4.6)$$

Equating the output currents expressed by (4.5) and (4.6), yields the following equation:

$$\frac{g_{21f}\bar{e}_{nf}+g_{21a}\bar{e}_{na}}{g_{22a}+g_{22f}} = \frac{g_{21}\bar{e}_n}{g_{22}}. \quad (4.7)$$

The expression of  $\bar{e}_n$  thereby can be found by solving (4.7) and its final expression is:

$$\bar{e}_n = \frac{g_{21f}\bar{e}_{nf}+g_{21a}\bar{e}_{na}}{g_{21}}. \quad (4.8)$$

After obtaining the expression of  $\bar{e}_n$ , the next step is to find the expression of  $\bar{v}_n$ . The expression of  $\bar{v}_n$  could be found by forcing the voltages of the two circuits to be equal to each other, when the input terminals are left open-circuited. Care must be taken, because even the input terminal in Fig. 4.1 is left open-circuited, either  $\bar{e}_{na}$  or  $\bar{e}_{nf}$  no longer has a floating terminal. Instead, they form a loop with  $g_{11a}$  and  $g_{11f}$ . This is in contrast to the situation described in Chapter 3, where opening the input terminals means that the voltage generators are both disabled. Therefore, in this case, the output voltage comprises two parts,

i.e. the one by the current generators i.e.  $\bar{i}_{na}$  and  $\bar{i}_{nf}$ , and another by the voltage generators, i.e.  $\bar{e}_{na}$  or  $\bar{e}_{nf}$ .

Firstly, consider the part contributed by the current generator, i.e.  $\bar{i}_{na}$  and  $\bar{i}_{nf}$ .

Since the output is open-circuited, there is no current at the output, which means  $i_o$  is zero. The current generators,  $\bar{i}_{na}$  and  $\bar{i}_{nf}$ , generate currents through  $g_{11a}$ , thus creating a voltage drop across  $g_{11a}$ . The voltage drop can then be referred to the output, by multiplying a factor of  $g_{21a}$ . The current generators also provide a certain amount of current which flows through  $g_{11f}$ , thus developing a voltage drop across  $g_{11f}$  as well. The voltage drop across  $g_{11f}$  is then also referred to the output, by multiplying a factor of  $g_{21f}$ . The two voltage components are given on the left hand side of (4.9), and can further be simplified to  $(\bar{i}_{nf} + \bar{i}_{na}) \cdot \frac{g_{21}}{g_{11}}$ , as expressed by (4.9):

$$\begin{aligned} & (\bar{i}_{nf} + \bar{i}_{na}) \cdot \frac{g_{11a}}{g_{11a} + g_{11f}} \cdot \frac{1}{g_{11a}} \cdot g_{21a} + (\bar{i}_{nf} + \bar{i}_{na}) \cdot \frac{g_{11f}}{g_{11a} + g_{11f}} \cdot \frac{1}{g_{11f}} \cdot g_{21f} \\ & = (\bar{i}_{nf} + \bar{i}_{na}) \cdot \frac{g_{21}}{g_{11}}. \end{aligned} \quad (4.9)$$

Secondly, consider the output voltage due to  $\bar{e}_{na}$  or  $\bar{e}_{nf}$ .

As mentioned earlier,  $\bar{e}_{na}$  and  $\bar{e}_{nf}$  could also generate currents flowing through  $g_{11a}$  and  $g_{11f}$ . Therefore, the voltage drops across  $g_{11a}$  and  $g_{11f}$  are:

$$\frac{(\bar{e}_{na} - \bar{e}_{nf})}{\frac{1}{g_{11a}} + \frac{1}{g_{11f}}} \cdot \frac{1}{g_{11a}}, \quad \frac{(\bar{e}_{nf} - \bar{e}_{na})}{\frac{1}{g_{11a}} + \frac{1}{g_{11f}}} \cdot \frac{1}{g_{11f}}. \quad (4.10)$$

Equating the output voltage in Fig. 4.1 and the output voltage in Fig. 4.2 yields the following equation:

$$\begin{aligned} g_{21}(\bar{i}_n g_{11}) \\ = (\bar{i}_{nf} + \bar{i}_{na}) \cdot g_{21} + \frac{(\bar{e}_{na} - \bar{e}_{nf})}{\frac{1}{g_{11a}} + \frac{1}{g_{11f}}} \cdot \frac{1}{g_{11a}} \cdot g_{21a} + \frac{(\bar{e}_{nf} - \bar{e}_{na})}{\frac{1}{g_{11a}} + \frac{1}{g_{11f}}} \cdot \frac{1}{g_{11f}} \cdot g_{21f} \end{aligned} \quad (4.11)$$

$\bar{i}_n$  thus could be solved, as given by

$$\bar{i}_n = \bar{i}_{nf} + \bar{i}_{na} + \frac{g_{11a}g_{21f} - g_{21a}g_{11f}}{g_{21}} \bar{e}_{nf} + \frac{g_{11f}g_{21a} - g_{21f}g_{11a}}{g_{21}} \bar{e}_{na} \quad (4.12)$$

Before proceeding to the final expression of  $\bar{e}_n$  and  $\bar{i}_n$ , some simplification can be made in order to make the deducing process easier. Note that the amplifier has a large gain and the feedback is usually made up of lossy elements. Also, note that the signal power fed back by the feedback network is much stronger than that fed back by the basic amplifier, due to the isolation of the amplifier. Therefore, the following assumptions can be made:

$$|g_{21a}| \gg |g_{21f}|, |g_{12a}| \ll |g_{12f}|, \quad (4.13)$$

which implies:

$$g_{21} \approx g_{21a}, g_{12} \approx g_{12f}. \quad (4.14)$$

Therefore, (4.8) and (4.12) can then be further simplified as:

$$\bar{e}_n \approx \bar{e}_{na}, \quad (4.15)$$

$$\bar{i}_n = \bar{i}_{nf} + \bar{i}_{na} + g_{11f}(\bar{e}_{na} - \bar{e}_{nf}). \quad (4.16)$$

Assuming that all noise sources are independent, the noise current power is:

$$\bar{i}_n^2 = \bar{i}_{nf}^2 + \bar{i}_{na}^2 + g_{11f}^2(\bar{e}_{na}^2 + \bar{e}_{nf}^2), \quad (4.17)$$

where

$$\bar{i}_{nf} = \bar{i}_{uf} + Y_{cora}\bar{e}_{nf}; \quad (4.18)$$

and

$$\bar{i}_{na} = \bar{i}_{ua} + Y_{corf} \bar{e}_{na}. \quad (4.19)$$

Substituting (4.15), (4.18) and (4.19) into (4.17), yields:

$$\bar{i}_n^2 = \bar{i}_{nf}^2 + \bar{i}_{na}^2 + (Y_{corf}^2 + g_{11f}^2) \bar{e}_{nf}^2 + (Y_{cora}^2 + g_{11f}^2) \bar{e}_n^2. \quad (4.20)$$

Recall that in Chapter 3, the noise generator could be treated as thermal noise produced by equivalent resistance or conductance, therefore,

$$R_n \equiv \frac{\bar{e}_n^2}{4kT\Delta f}, \quad (4.21)$$

and

$$G_u \equiv \frac{\bar{i}_u^2}{4kT\Delta f}. \quad (4.22)$$

Comparing (4.21), (4.22) with (4.20), the following relationships hold:

$$R_n \approx R_{na}, \quad (4.23)$$

$$G_u = G_{uf} + G_{ua} + |Y_{corf} - g_{11f}|^2 R_{nf}, \quad (4.24)$$

$$Y_{cor} = Y_{cora} + g_{11f}. \quad (4.25)$$

The optimum source admittance,  $Y_{sopt}$ , is

$$Y_{sopt} = G_{sopt} + jB_{sopt} = \sqrt{\frac{G_u}{R_n} + G_{cor}^2} + j(-B_{cor}), \quad (4.26)$$

where  $G_{cor}$  and  $B_{cor}$  represent the conductance and the susceptance of  $Y_{cor}$  [26]:

$$Y_{cor} = G_{cora} + jB_{cora} + Re(g_{11f}) + Im(g_{11f}). \quad (4.27)$$

Substituting (4.17) ~ (4.19) into (4.20), the final expression for the optimum source admittance is derived as:

$$Y_{sopt} = \sqrt{G_{sopta}^2 + \frac{G_{uf}}{R_{na}} + 2G_{cora}Re(g_{11f}) + Re^2(g_{11f}) + \frac{|Y_{corf} - g_{11f}|^2 R_{nf}}{R_{na}}} + j[B_{sopta} - Im(g_{11f})]. \quad (4.28)$$

The minimum noise figure,  $NF_{min}$ , is

$$NF_{min} = 1 + 2R_n(G_{sopt} + G_c) = 1 + 2R_{na}[G_{cora} + G_{sopt} + Re(g_{11f})]. \quad (4.29)$$

At this point, several conclusions can be made based on the results deduced above.

1. The shunt-series feedback network can increase  $Y_{SOPT}$  by the noise current stemming from the feedback network, as indicated by (4.21).
2. According to 1, if the shunt-series feedback network is associated with resistive elements, such a topology will increase  $Y_{SOPT}$ . This means that if the noise impedance of an amplifier is higher than the source impedance, a shunt-series lossy feedback network can be used to decrease  $Z_{SOPT}$ .
3. As implied by (4.28), the feedback network can extend the bandwidth of  $Y_{SOPT}$ .
4. If the feedback network is lossless, the noise parameters of the amplifier will not be changed.

The remaining feedback configurations can be analyzed in the same way. The results are summarized below:

**1. Shunt-shunt feedback:**

$$Y_{sopt} \Big|_{\text{shunt-shunt feedback}} = \sqrt{G_{sopta}^2 + \frac{G_{uf}}{R_{na}} + 2G_{cora} \text{Re}(y_{11f}) + \text{Re}^2(y_{11f}) + \frac{|Y_{corf} - y_{11f}|^2 R_{nf}}{R_{na}}} + j[B_{sopta} - \text{Im}(y_{11f})], \quad (4.30)$$

$$NF_{min}|_{\text{shunt-shunt feedback}} = 1 + 2R_{na}[G_{cora} + G_{sopt} + Re(y_{11f})]. \quad (4.31)$$

The shunt-shunt feedback shares similar characteristics with that of the shunt-series feedback. Therefore, such a topology can be applied to the case where the noise impedance of an amplifier is higher than the source impedance. Moreover, based on the deduced formulas, it can be proven that if a network is combined with  $n$  identical networks in a shunt-shunt topology, the optimum noise impedance will be decreased correspondingly. Therefore, for the noise matching technique introduced in Chapter 2 and 3, the deduced formulas, by using the two-port network analyzing method, can theoretically prove that the optimum noise impedance of a transistor can be adjusted by paralleling multiple gate fingers.

## 2. *Series-series feedback:*

$$Z_{sopt}|_{\text{series-series feedback}} = \sqrt{R_{sopta}^2 + \frac{R_{uf}}{G_{na}} + 2R_{cora}Re(z_{11f}) + Re^2(z_{11f}) + \frac{|z_{corf} - z_{11f}|^2 G_{nf}}{G_{na}}} + j[X_{sopta} - Im(z_{11f})], \quad (4.32)$$

$$NF_{min}|_{\text{series-series feedback}} = 1 + 2R_{na}[R_{cora} + R_{sopt} + Re(z_{11f})].$$

(4.33)

The series-series feedback can refer to a topology where the main amplifier is being inductively source degenerated as shown in Fig. 3.7. Similarly to above analysis, the deduced formulas prove that if the feedback network is purely reactive, the noise parameters of the main amplifier will remain unchanged. Additionally, as can be noticed from (4.32), the optimum source impedance,  $Z_{SOPT}$ , can be increased if the feedback network is lossy. Therefore, if the main amplifier has a relatively lower optimum noise impedance, such a feedback network can be used to increase  $Z_{SOPT}$ .

### 3. Series-shunt feedback:

$$Z_{sopt} \Big|_{\text{series-shunt feedback}} = \sqrt{R_{sopta}^2 + \frac{R_{uf}}{G_{na}} + 2R_{cora} \operatorname{Re}(h_{11f}) + \operatorname{Re}^2(h_{11f}) + \frac{|Z_{corf} - h_{11f}|^2 G_{nf}}{G_{na}}} + j[X_{sopta} - \operatorname{Im}(h_{11f})], \quad (4.34)$$

$$NF_{min} \Big|_{\text{series-shunt feedback}} = 1 + 2R_{na} [R_{cora} + R_{sopt} + \operatorname{Re}(h_{11f})]. \quad (4.35)$$

The series-shunt feedback shares similar characteristics with that of the series-series feedback. A practical example of such a topology is referred to a negative feedback through a transformer. It can be concluded that the series-shunt feedback can be applied to the situation where the main amplifier has a lower noise impedance.

### **4.3 Summary**

The classical noise theory based on a two-port network was applied to a more practical situation. These formulas can offer useful design insights. Based on the formulas, the real part of the optimum noise impedance will not be affected by a lossless feedback network. It thus allows one to further exploit the noise matching technique with more configurations.

## **Chapter 5**

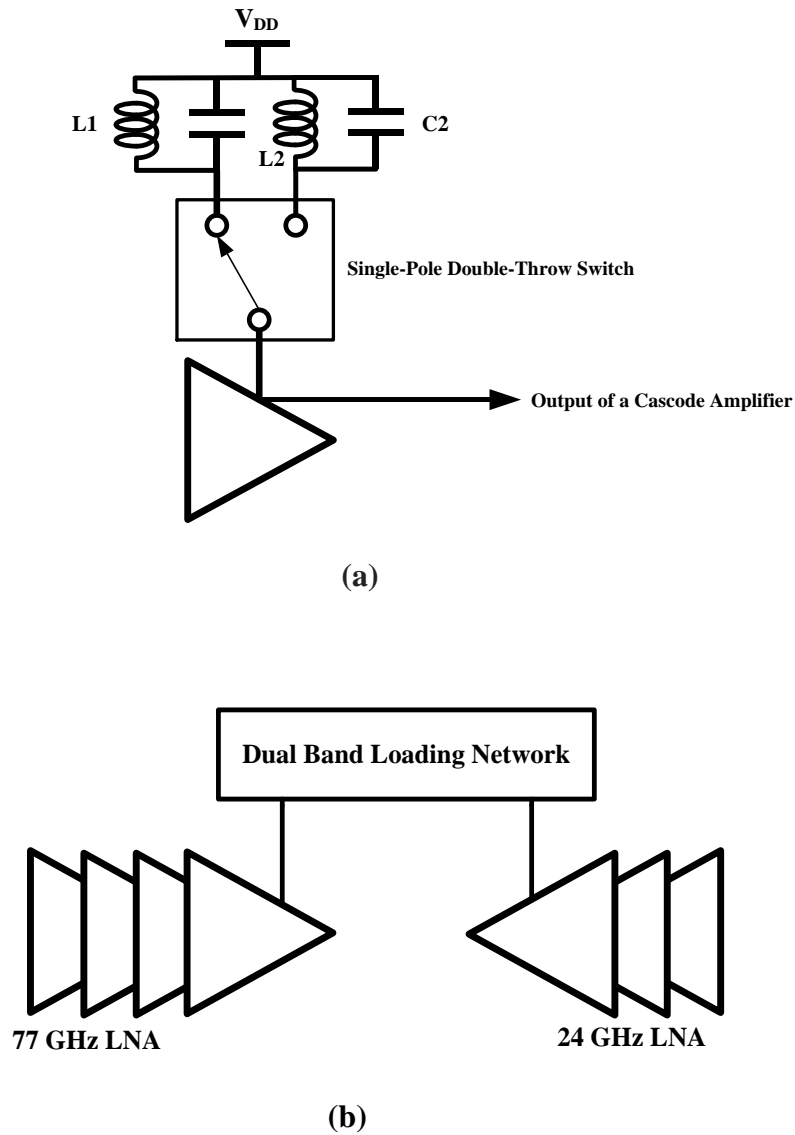
# **A Dual-Band 24/77 GHz CMOS LNA for Automotive Radar Application**

In previous chapters, the noise behavior in MOS transistors and the macroscopic description of it based on a two-port network were examined. This chapter explores how theory can be put into practical use. A dual-band LNA is proposed. As mentioned in Chapter 1, CMOS millimeter-wave circuits have demonstrated a great potential in handling millimeter-waves, as evidenced by various W-band CMOS LNAs [46]–[48]. In 2009, the first BiCMOS dual-band transceiver for automotive applications was proposed by [19]. As introduced in Chapter 2, the dual-band radar incorporates two sub-radars [5]. The K-band radar is used to transceive parking, stop and go signals. The W-band radar is used for the auto-cruise purpose. LNA plays an important role in receiving the millimeter-waves. As mentioned in Chapter 3, its performance directly determines the sensitivity of a receiver. Without LNA, the millimeter-waves would be submerged in noise. This chapter proposes a dual-band LNA in a 65-nm CMOS technology for automotive applications. As mentioned in Chapter 1, realizing the integration of such multi-mode multi-band transceivers in CMOS technologies could improve the radar's functionality and further lower its fabrication cost.

## 5.1 Introduction

The automotive radar uses two frequency bands to transmit and receive millimeter-waves [19]. Consider the case when implementing such a dual-band receiver in a conventional way [59] [60]. In this case, conventionally, one has to design two LNAs with two separate loading networks. Loading networks normally occupy a large chip area. This is contrary to the wish for a small chip area. The dual-band switchable LNA can be used to address such an issue. However, as shown in Figure 5.1(a), the conventional dual-band LNA has following drawbacks. Firstly, the switch is located at the signal path. The headroom of the cascode amplifier is thereby limited by that switch and biasing becomes difficult if  $V_{DD}$  is low. Secondly, because the switch is at the signal path, it will add additional noise and thus degrades the noise performance. For this reason, a dual-band LNA structure is proposed, as shown in Fig. 5.1(b). As illustrated in Fig. 5.1(b), compared to Fig. 5.1(a), the loading network has two resonance peaks for each of the dual-band, and the switches no longer exist in the signal path. Instead, the switches are relocated at the gate-terminal. By adjusting the gate biasing voltage, one can easily turn on one LNA and shut down another at the same time, thus avoiding contaminating the signal path. Compared to conventional ones, this structure benefits the LNA in the following aspects. Firstly, the chip area previously reserved for one loading network can henceforth be saved. Secondly, the signal will not be contaminated by the noise current in the switch and its headroom increases. Thirdly, compared to Fig. 5.1(a), the

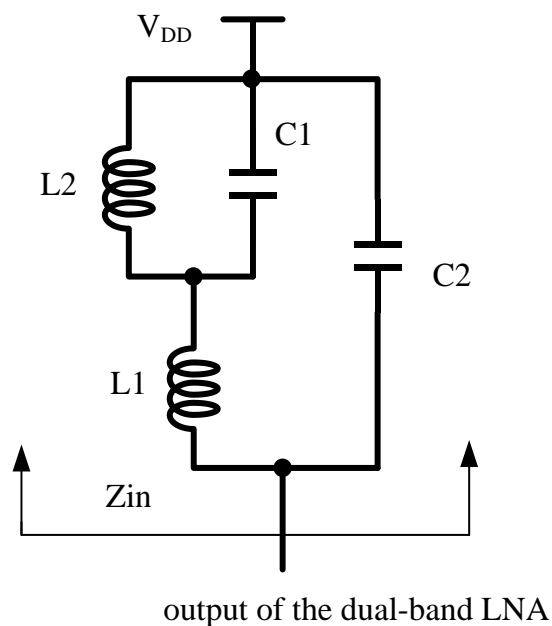
proposed topology allows more freedom when designing an LNA for a specific frequency band. Fourthly, the mixer now has only one RF input port, thus comforting the layout designer when making the floor plan. [19]



**Figure 5.1. The proposed topology for the dual-band LNA.**

## 5.2 Design of a Dual-Band Loading Network

Regarding the application field, the dual-band loading network should resonate at 24 GHz and 77 GHz. This observation leads to a loading network which is similar to a dual-band filter [61]. Once the loading network is designed as a dual-band filter, it then can provide two resonance peaks at 24 GHz and 27 GHz, in its two passbands. Besides providing two peaks, the loading network should also provide the biasing path. With these concerns taken into account, the proposed structure for the loading network is shown in Fig. 5.2.



**Figure 5.1. The structure of the dual-band loading network.**

As shown in Fig. 5.2, the input impedance of the dual-band loading network is equivalent to the output impedance of the dual-band LNA. The input impedance of the dual-band loading network is

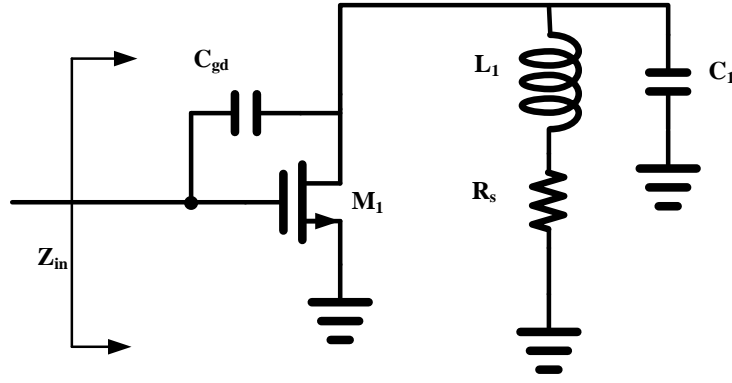
$$Z(s) = \frac{s(L_1+L_2)(1+s^2 \cdot L_1/L_2 \cdot C_1)}{s^4 L_1 L_2 C_1 C_2 + s^2 (L_1 C_1 + L_1 C_2 + L_2 C_2) + 1}. \quad (5.1)$$

Based on (5.1), the inductance of  $L_1$  and  $L_2$  and the capacitance of  $C_1$  and  $C_2$  can be determined, by forcing the denominator of (5.1) to zero.

### 5.3 Design of LNAs Operating at 24 GHz and 77 GHz

After introducing the passive loading network design, this section focuses on active devices, i.e. the amplifier design. Recall that, in Chapter 3, it seems that with fewer active devices, the noise figure will be smaller. Therefore, common-source amplifier sounds like a good choice. However, at the millimeter-wave frequency range, instability issues arise. Common-source topology suffers from instability issues. Referring to Fig. 5.3, the input impedance of a common source amplifier is:

$$Z_{in}(j\omega) = \frac{1 - L_1(C_1 + C_F)\omega^2 + jR_S(C_1 + C_F)\omega}{[-(R_S C_1 + g_m L_1)\omega + j(g_m R_S - L_1 C_1 \omega^2 + 1)]C_F \omega}. \quad (5.2)$$



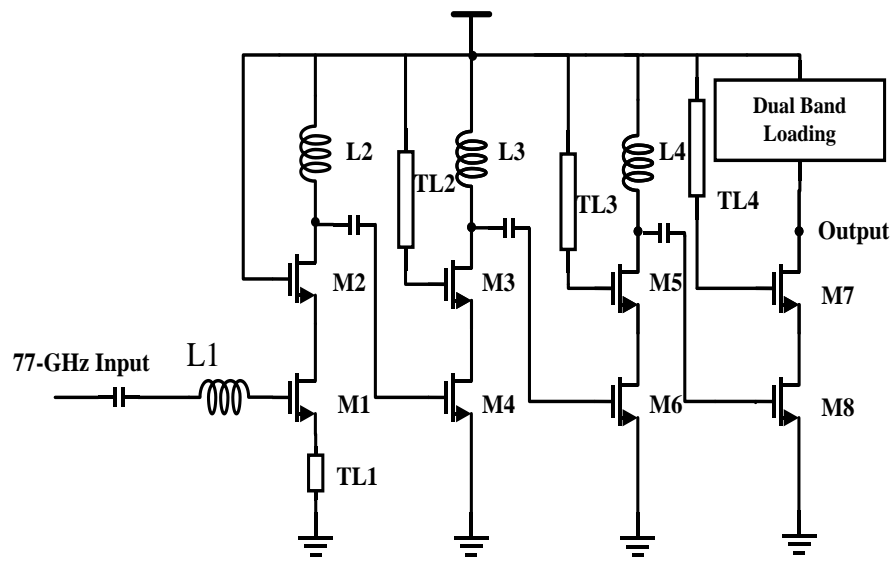
**Figure 5.2. The effect of  $C_{gd}$  on the input impedance of a common source amplifier.**

As implied by (5.2), the drain to gate capacitor  $C_{gd}$  may create a negative input resistance at a certain frequency point, thus potentially leading to an instability issue. This frequency point refers to the moment when the numerator drops to zero, as denoted by  $\omega_1$ :

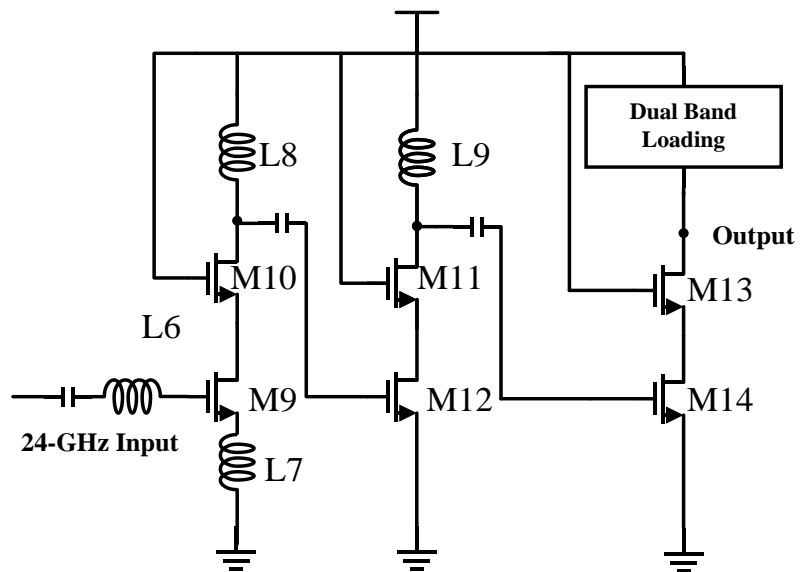
$$\omega_1^2 = \frac{R_S C_1 + g_m L_1 - (1 + g_m R_S) R_S (C_1 + C_F)}{g_m L_1^2 (C_1 + C_F)}. \quad (5.3)$$

Therefore, if the frequency is higher than  $\omega_1$ , the sign of the input impedance  $Z_{in}(j\omega)$  will be reversed.

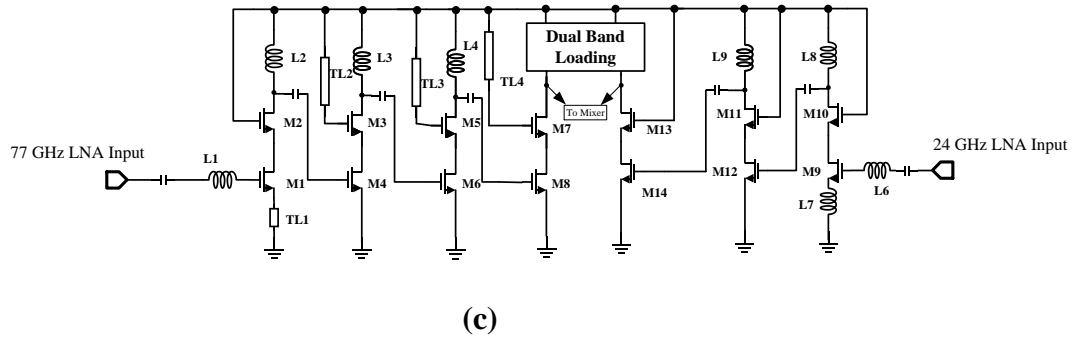
Concerning the instability issue, the cascode structure can be applied to all stages. The proposed structures for the 24 GHz and 77 GHz LNA are given in Fig. 5.4.



(a)



(b)



**Figure 5.3. Schematic of the proposed dual-band LNA: (a) the 77 GHz LNA, (b) the 24 GHz LNA, and (c) the final schematic.**

As seen in Fig. 5.4(a), transmission lines are placed at the gate of M<sub>3</sub>, M<sub>5</sub> and M<sub>7</sub>. A technique called gain-boosting is used here. Once an inductor with proper inductance is placed at the gate terminal of a common-gate amplifier, feedback is formed by the gate to the source capacitor. The feedback in turn could potentially boost the gain, if the waveforms at the two sides of the capacitor are out of phase [62]. Referring to the design of the 24 GHz LNA, since this frequency band is far below the transition frequency of a 65-nm MOS transistor, the gain-boosting technique is not adopted.

## 5.4 Noise Matching Technique for the Input Terminal in Series-Series Feedback

This section focuses on the refinement work on noise performance. As examined in Chapter 3, the noise figure of the LNA has a great impact on overall noise performance. In the millimeter-wave frequency range, without any

refinement, MOS transistors normally exhibit a large amount of noise. Therefore, the refinement work is needed in order to optimize the noise performance of a MOS transistor operating in the millimeter-wave frequency range. The noise matching technique described in Chapter 2 is thereby applied to the first stage of the LNA. The noise matching technique helps the transistor to achieve its minimum noise figure. The minimum noise figure,  $NF_{min}$ , is achieved by matching the input impedance to optimum noise impedance, as already discussed in Chapter 2. This optimum noise impedance may cancel a certain amount of noise currents, thus reducing the noise figure [24]. Therefore, if the input impedance of  $M_1$  and  $M_9$  is matched to the optimum noise source impedance,  $Z_{sopt}$ , the output noise could be minimized to a maximum extent. The procedure of applying the noise matching technique is as follows.

Firstly, recall that there are two dominant types of noise in an MOS transistor. One is the drain noise current, as given by

$$\bar{i}_{nd}^2 = 4kT\gamma g_{d0}\Delta f; \quad (5.4)$$

Another is the gate current noise:

$$\bar{i}_{ng}^2 = 4kT\delta g_g\Delta f, \quad (5.5)$$

where

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}. \quad (5.6)$$

The two noise sources are correlated, and their relationship is described by a correlation coefficient, which is

$$c \equiv \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}}. \quad (5.7)$$

Secondly, by applying the two-port noise theory, the expression of the equivalent input noise voltage generator could be computed as:

$$\bar{e}_n^2 = \frac{\bar{i}_{nd}^2}{g_m^2} = \frac{4kT\gamma g_{d0}\Delta f}{g_m^2}. \quad (5.8)$$

Besides the equivalent noise voltage generator  $\bar{e}_n$ , as indicated in Chapter 3, an equivalent noise current generator also exists at the input too, since the noise voltage generator itself alone cannot fully represent the overall noise current, i.e.  $\bar{i}_{nd}$ . The equivalent noise current generator is a necessary element. Imagine that the gate terminal is left open-circuited. In this case, the equivalent noise voltage generator is disabled. In order to represent the output noise current, the existence of the equivalent noise current generator thereby becomes necessary.

When the gate terminal is left open-circuited, the MOS transistor could also produce a certain amount of noise current which flows across the gate to the source capacitor,  $C_{gs}$ . Note that the voltage drop across the capacitor equals the

amount of noise current divided by the transconductance. Therefore, the equivalent input noise current generator can be partly expressed as

$$\bar{i}_{n1}^2 = \bar{e}_n^2 (j\omega C_{gs})^2. \quad (5.9)$$

Accurately speaking, besides  $\bar{i}_{n1}$ , the overall expression of the equivalent current noise generator contains another element, i.e. the induced gate noise current,  $\bar{i}_{ng}$ , as discussed in Chapter 3. The induced gate noise current,  $\bar{i}_{ng}$ , consists of two items. The first item,  $i_{ngc}$ , is correlated with  $\bar{i}_{nd}$ . Another item,  $i_{ngu}$ , is uncorrelated with  $\bar{i}_{nd}$ . Therefore, in the end, the expression of the correlation admittance is obtained as:

$$Y_C = j\omega C_{gs} + g_m \cdot \frac{i_{ngc}}{i_{nd}} = j\omega C_{gs} + \frac{g_m}{g_{d0}} \cdot c \sqrt{\frac{\delta}{5\gamma}} \cdot \omega C_{gs} = j\omega C_{gs} \left( 1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right), \quad (5.10)$$

where

$$\alpha = \frac{g_m}{g_{d0}}. \quad (5.11)$$

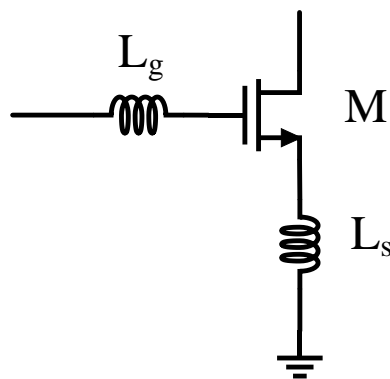
$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma} (1 - |c|^2)}. \quad (5.12)$$

Equation (5.12) implies that by properly sizing the transistor, the optimum

source resistance can be set to  $50 \Omega$ .

After setting the optimum source resistance to  $50 \Omega$  by sizing the transistor, the next step is to match the input impedance of the MOS transistor to  $50 \Omega$ . As mentioned in Chapter 3, the source degeneration method could provide a  $50 \Omega$  input impedance. Therefore, by placing inductors at the source terminals of  $M_1$  and  $M_9$ , the input impedance of both 24 GHz and 77 GHz LNAs can be made equal to  $50 \Omega$ .

At this point, regarding the preceding noise matching technique, a question may be raised. Since the size of the MOS transistor has already been fixed to an optimum value, it seems that the source inductor, if added, may change the input condition, and thus change the optimum point. However, based on the formulas given in Chapter 4, the optimum point will not be changed.



**Figure 5.4. The simplified schematic of the first stage circuit in Figure 24(a) and (b).**

Firstly, referring to (5.12) and Fig. 5.5, and assuming that the inductor is lossless, the optimum noise impedance is given by:

$$Z_{sopt} \Big|_{\text{series-series feedback}} = \sqrt{R_{sopta}^2 + \frac{R_{uf}}{G_{na}} + 2R_{cora} \operatorname{Re}(z_{11f}) + \operatorname{Re}^2(z_{11f}) + \frac{|z_{corf} - z_{11f}|^2 G_{nf}}{G_{na}}} + j[X_{sopta} - \operatorname{Im}(z_{11f})], \quad (5.13)$$

where, referring to Fig. 5.5, the Z-parameters are:

$$G_{nf} = R_{uf} = Z_{corf} = 0, Z_{11f} = j\omega(L_s + L_g), Z_{12a} = 0, Z_{12f} = jL_s. \quad (5.14)$$

By substituting (5.14) into (5.13), it clearly reveals that the optimum noise resistance remains the same even if an inductor is placed at the source terminal. For more discussions on the noise matching technique, one can refer to [63].

Biasing has an impact on noise figure, too, for the following reason. Referring to Fig. 5.4, when the gate to source biasing voltage,  $V_{gs}$ , is small, the transconductance of  $M_1$ ,  $g_{m1}$ , is proportional to  $V_{gs}$ . When  $V_{gs}$  increases,  $g_{m1}$  increases as well. At the same time, the noise current also increases but at a slower rate compared to the transconductance. When  $V_{gs}$  increases to a certain point, the mobility of the electrons becomes saturated. At this time, the transconductance stops increasing, since it is proportional to the mobility. Consequently, the current noise grows faster than the signal current. This implies that the signal to noise ratio begins to worsen. In other words, the foregoing analysis shows that an optimum biasing point exists. At this point, the

transconductance is at its maximum value, and after such a point, the mobility begins to decrease, thus bringing down the signal-to-noise ratio. [64]

## 5.5 Design Flow of 77 GHz LNA

The design flow is as follows. Take the design of the 77 GHz LNA as an example.

The first step is to decide the optimum biasing current. Referring to [55], the current density is found to be 0.15 mA/ $\mu\text{m}$ .

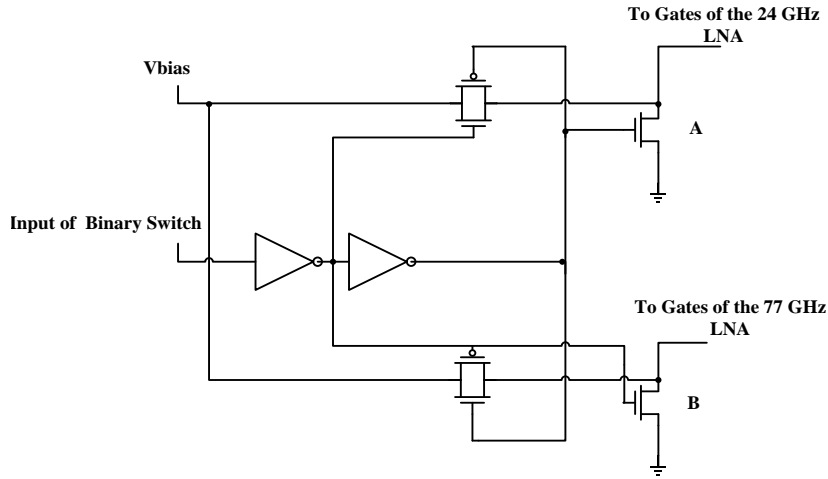
The second step is to size the transistor such that the optimum noise source resistance of the input transistor equals 50  $\Omega$ . This is done by adjusting the number of fingers.

The third step is to decide the inductance of the source inductor in  $M_1$ . This is done by using (3.28). Note that, as mentioned in Chapter 2, the pad capacitance should be taken into account at this step.

The fourth step is to place an inductor at the gate of  $M_1$ . Due to the gate and source inductors, the imaginary part of the input impedance is cancelled.

## 5.6 Switch Design

The LNA employs a binary switch to turn each LNA “on” and “off”. The schematic of the binary switch is shown in Fig. 5.6.



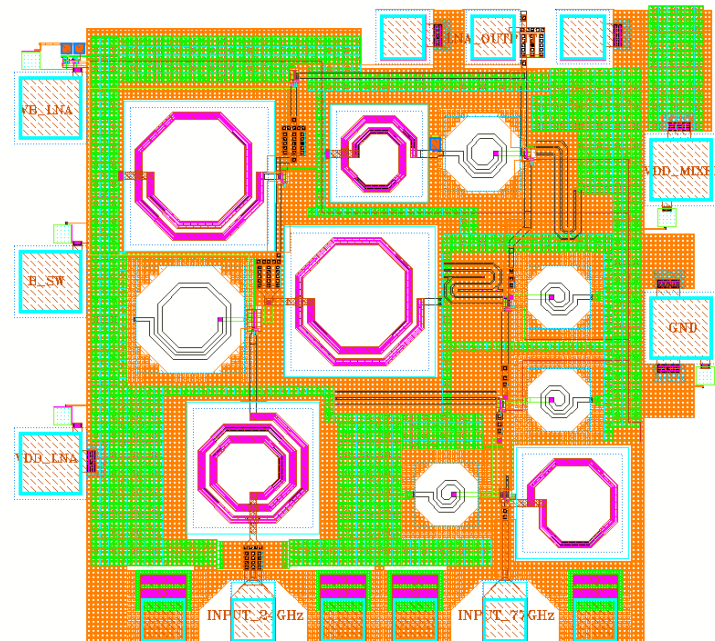
**Figure 5.5. The structure of the binary-switch.**

The working principle of the binary switch is as follows. When the binary switch is set to “1”, the bottom NMOS-PMOS switch pair will be triggered on. As a result, the gate voltage of Transistor B becomes zero. Since Transistor B does not have enough gate voltage to be turned on,  $V_{bias}$  is then all applied on its drain.

## 5.7 Layout Consideration and Simulation Results

The final layout of the dual-band LNA is shown in Fig. 5.7. The chip area including the pads is  $560\text{-}\mu\text{m} \times 600\text{-}\mu\text{m}$ . The pad is  $50\text{-}\mu\text{m} \times 50\text{-}\mu\text{m}$  large, and they are located around the layout. The pads for the millimeter-wave inputs are placed at the bottom. The input pad for the 77 GHz LNA is placed at the right corner. Regarding the distance from pads to output, this pad lends a shorter distance than

the left corner one does. Therefore, the power loss in the transmission line can be reduced. Metal 2 is used by the power supply, and Metal 1 is the ground plane. Pink inductors are automatically generated through the process design kit (PDK).



**Figure 5.6. The final layout of the proposed dual-band LNA**

The white inductors, whose inductance is too small to be made in the PDK, are designed in Ansoft HFSS. They are octagonal symmetrical inductors. The inductors are created on the top copper layer which has a thickness of  $3.3 \mu\text{m}$ . A high impedance layer is placed under the inductor in order to minimize the substrate loss.

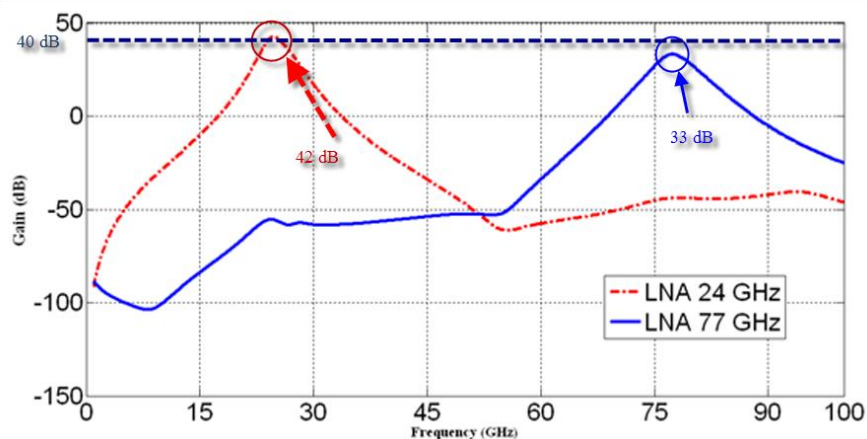
The design procedure is as follows.

- (1) First calculate the inductance based on preceding analysis, and then use the

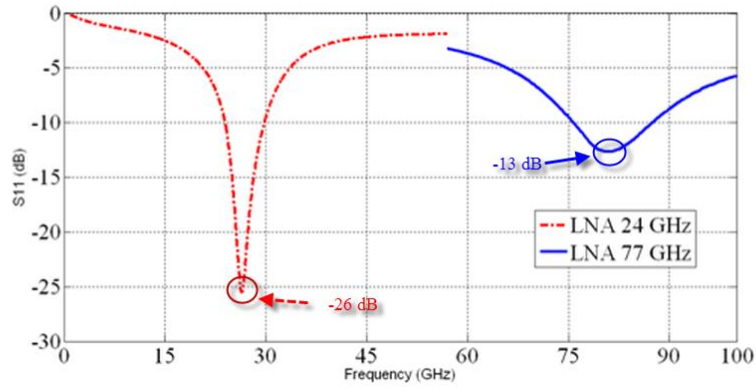
simulation tool to create an inductor with the theoretical value.

- (2) Based on the inductor created in the first step, change its radius more or less. At this step, additional inductors whose inductance is around the theoretical value are obtained.
- (3) Substitute each inductor designed in the first and second steps into the circuit, until one of them achieves a good result.

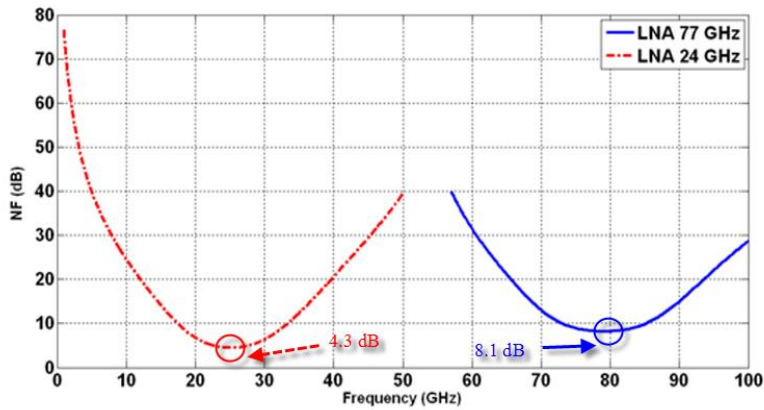
The simulated results are plotted in Fig. 5.8. The input return loss at 77 GHz is 13 dB, and is 26 dB at 24 GHz. At 77 GHz, the voltage peak gain is 33 dB, and at 24 GHz it is 42 dB. The input reflection coefficient at 24 GHz is -26 dB and at 77 GHz, it is -13 dB. The noise figure at 24 GHz is 4.3 dB and is 8.1 dB at 77 GHz. The dc power consumption at the 24 GHz mode is 7.1 mW and it is 9.5 mW at the 77 GHz mode.



(a)



(b)



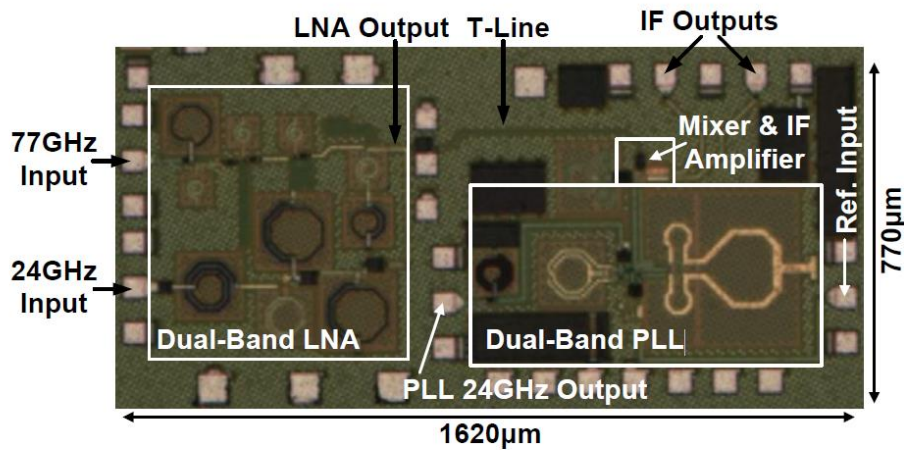
(c)

**Figure 5.7. Simulated results of (a) the voltage gain, (b)  $S_{11}$  and (c) the noise figure.**

## 5.8 Measurement Results

The proposed LNA has been integrated into a 24/77-GHz single-channel receiver. The die photo is shown in Fig. 5.9. The LNA is designed to be combined and measured with a broadband mixer. An on-chip dual-band PLL is used to provide the LO signal [65]. The circuit is implemented in GlobalFoundries 65 nm CMOS technology. The area of the receiver including the pads is 1620- $\mu\text{m}^2$

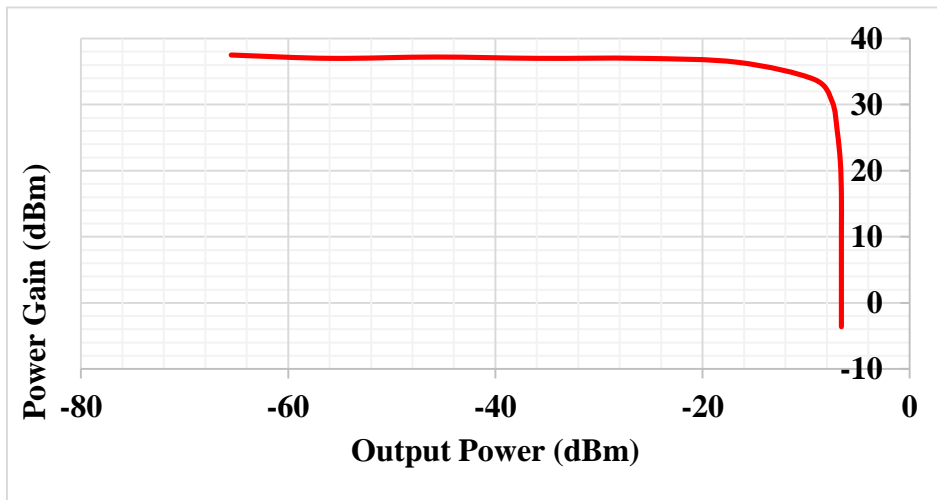
× 770- $\mu\text{m}$ . The power consumption of the receiver is 52- and 60-mW for 24 and 77 GHz modes, respectively.



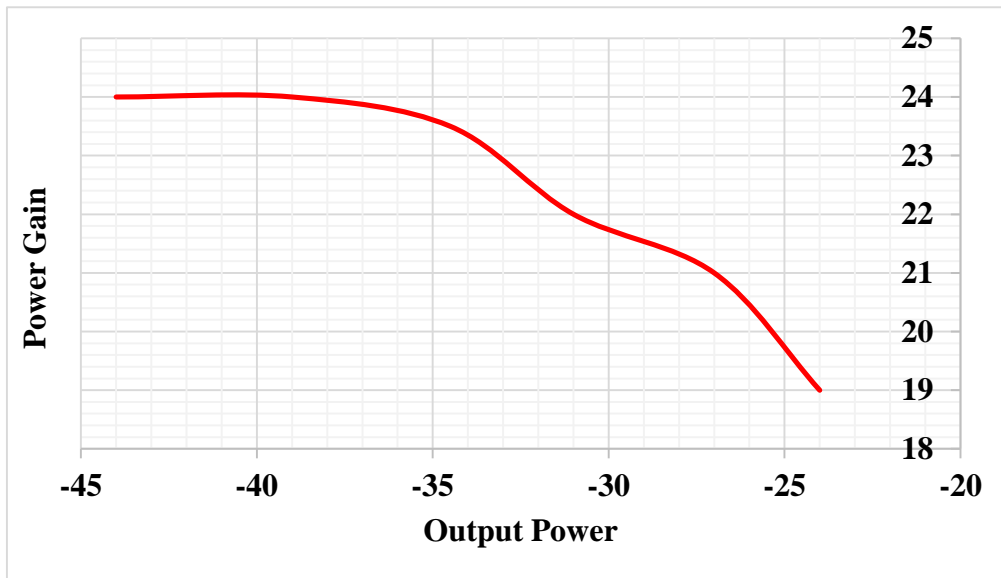
**Figure 5.8 Die photograph of the 24/77 GHz receiver.**

The RF measurement is conducted in the same manner introduced by [14]. Fig. 5.10 illustrates the output power gain at 24 and 77 GHz, respectively. In the 24-GHz mode, the conversion gain is 37 dB and in the 77-GHz mode the conversion gain is 23 dB. Fig. 5.10 also shows that the 1-dB compression point for the 24 GHz mode is -11.5 dBm. For the 77 GHz mode, it is -33 dBm. The noise figure referred to the noise floor is 16 dB at the 24-GHz modulation mode and 23 dB for the 77-GHz modulation mode. The discrepancy between the measured and simulated results is caused by the inaccurate EM simulation of the transmission lines (T-line). The measured FMCW modulation frequency and its time-domain frequency error in 77 GHz mode is shown in Fig. 5.11. To measure its frequency error, a chirp signal is applied from a signal generator SMF100A, and down-

convert the output to low frequency. As shown in Fig. 5.11, the frequency error is less than 1 MHz and the RMS value is only 290 kHz. The measured input reflection coefficients are plotted in Fig. 5.12. For both ports, the input reflection coefficients are suppressed under -10 dB. Table 5.1 summarizes and compares the measured results with other receivers designed for the automotive radar application. To the best of the author's knowledge, it is the first 24/77 GHz dual-band CMOS receiver and it achieves the lowest power consumption among all of the reported receivers in the same application field. The circuit can be regarded as a green technology, which is especially suited for the electric vehicles. As discussed in Chapter 1, when uniformed as an antenna array, the performance of the receiver can be further improved. In order to implement such a combination, Chapter 6 proposes a 24/77 GHz dual-band Wilkinson power divider.



(a)



(b)

Figure 5.9 Measured output power gain and the 1-dB-compression point

(a) 24- and (b) 77-GHz modes.

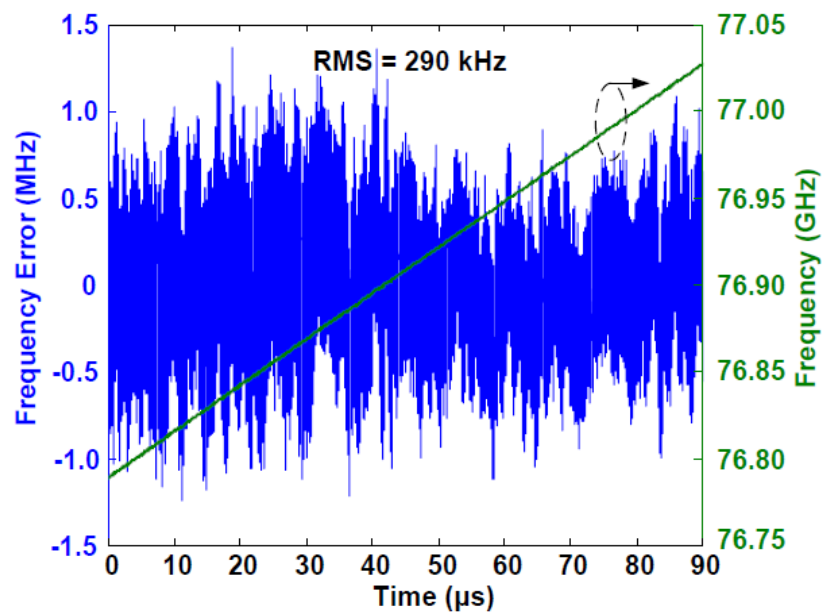
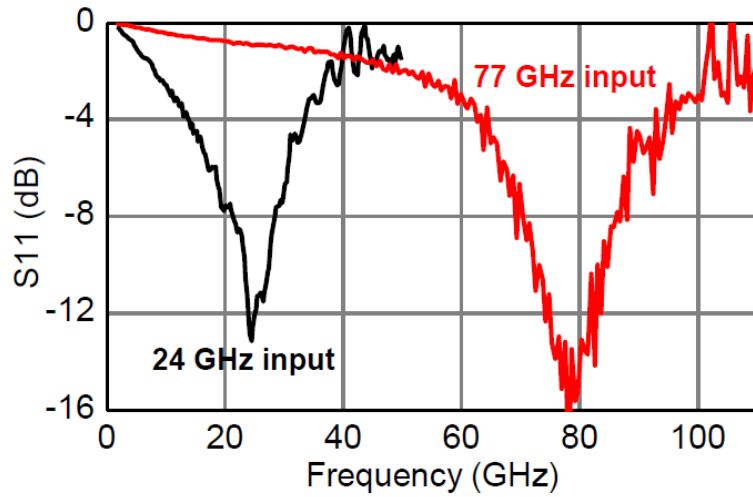


Figure 5.10 Measured FMCW modulation frequency and its time-domain frequency error.



**Figure 5.11 Measured input reflection coefficients of the receiver at the 24- and 77-GHz input ports.**

**Table 5.1 Comparison of the State-of-the-Art Receivers for Automotive Radar Applications**

Reference	Technology	Frequency Band	Conversion Gain (dB)	NF (dB)	Power Consumption (mW)	Chip Area (mm <sup>2</sup> )
[19]	0.18μm BiCMOS	24 GHz 77 GHz	35 31	4.5 8	197.5 282.5	3.6
[48]	90nm CMOS	77 GHz	23.1	15.6	212	4.7
[14]	65nm CMOS	77 GHz	38.7	30	128	0.95
<b>This Work</b>	65nm CMOS	24 GHz 77 GHz	37 24	16 23	52 60	1.25

## **5.9 Summary**

This chapter has presented a dual-band CMOS LNA for application on automotive radars employing the noise matching technique. Simulated results demonstrated that the proposed LNA meets the specification described in Chapter 1.

## **Chapter 6**

# **Design of a Dual-Band Wilkinson Power Divider**

Wilkinson power divider plays an important role in the receiver and transmitter. As wireless systems become more and more complex, dual-band systems can be seen everywhere nowadays [19] [66] [67]. As analyzed in Chapter 1, once combined by the power dividers, a receiver array can have a higher sensitivity and angular resolution than a single channel receiver. In this chapter, a design for a dual-band Wilkinson power divider is presented.

### **6.1 Introduction**

Since its first invention in 1960, the Wilkinson power divider [68] has attracted increasing attention, attributed to its highly ingenious matching and isolation methods. Various improved dividers based on Wilkinson's prototype have since then been reported. Nowadays, compact sized circuits are usually desired, thus how to embed the Wilkinson power divider on a single silicon chip becomes a critical challenge. The reason is that the conventional Wilkinson power divider occupies a large area due to its two relatively long arms, albeit it is much smaller compared to its counterparts such as coil dividers in the past [69]. Furthermore, the conventional Wilkinson power divider could operate only with one single frequency band. Regarding its large size, using meander lines to reconfigure the

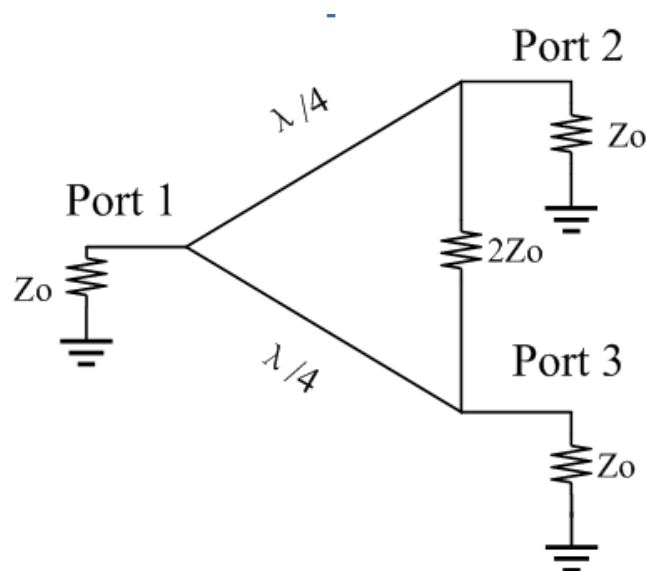
arms remains three times larger than bulky on-chip inductors if at best, not to speak of its suitability to be integrated into dual-band operation systems such as automotive cruise control systems [70]. Various solutions have been proposed to address these issues. [71] demonstrated a dual-band Wilkinson power divider using transmission lines with different line impedances and  $R$ ,  $L$ ,  $C$  components. However, due to the transmission lines, the divider is still considerably large. [72] and [73] replace the transmission lines with two inductors. The overall area was indeed decreased, but it cannot be directly fitted into a dual-band operating system. [74] proposed a dual-band divider implemented using lumped  $LC$ s. The problem for [74] was: firstly, it uses four inductors, meaning it almost occupies the same area as the meander-line-type ones do; secondly, the structure lacks symmetry, which is a potential cause of phase errors at the outputs. This chapter presents a novel design of a Wilkinson power divider, with a compact size and functionality to operate in two frequency-bands.

## 6.2 Theory and Design Equations

In a conventional Wilkinson power divider, as shown in Fig. 6.1, there are two  $\lambda/4$  transmission lines where the line impedances are  $\sqrt{2}Z_0$ . These lines split the input power evenly, so signals at port 2 and port 3 are equally split and are in phase. As for the impedance behavior, each  $50\ \Omega$  termination at port 2 and port 3 is up transformed by the two  $\lambda/4$  transmission lines to  $100\ \Omega$ . The two transformed impedances are connected in parallel, so the input impedance at port

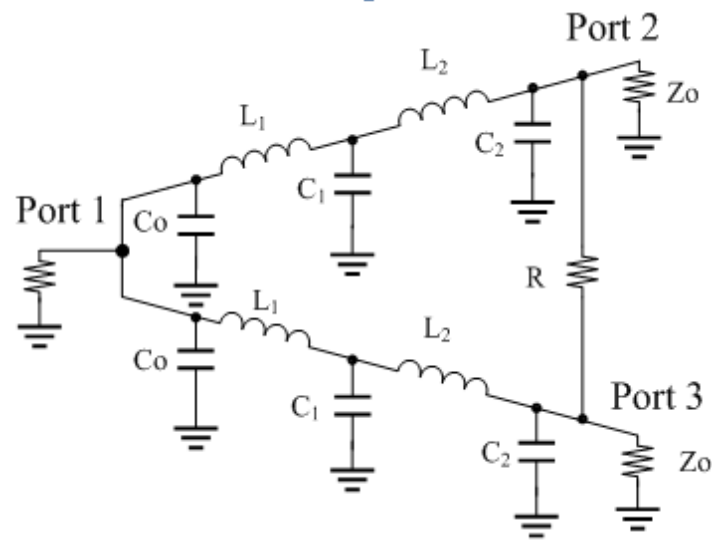
1 is  $50 \Omega$ , which means port 1 is well matched. Applying the nodal analysis, one can prove that port 2 and port 3 are also matched. The isolation method Wilkinson proposed can be simply stated in the following way. If the signal power is coming back at port 2 and travels through the two  $\lambda/4$  transmission lines, it will be 6 dB attenuated and since it travels through the half wave length long line, the shifted phase will be  $180^\circ$ . The signal also travels through the resistor which is  $2Z_0$ . Therefore it gets attenuated by 6 dB too. But the ideal resistor has no phase shifting effect upon the signal. So the two signals meeting at port 3 have the same magnitude but are out of phase and thus get cancelled.

In short, the Wilkinson power divider can be described as follows: it appears lossless when all the output ports are matched, which implies that only reflected power from the output ports is dissipated. [75]



**Figure 6.1. A conventional Wilkinson power divider.**

In our proposed structure,  $\lambda/4$  transmission lines are replaced by two  $LC$  networks as illustrated in Fig. 6.2. Due to its symmetrical structure, odd- and even-mode analysis can be applied to exploit the operation of the dual-band Wilkinson power divider.

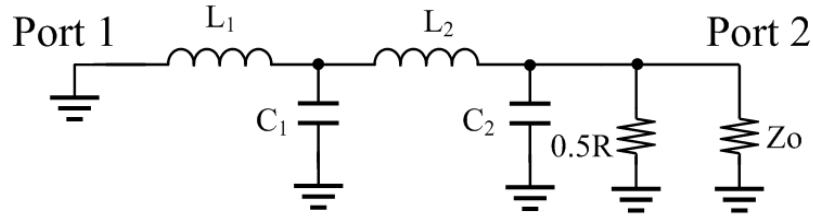


**Figure 6.2. The structure of the proposed dual-band Wilkinson power divider.**

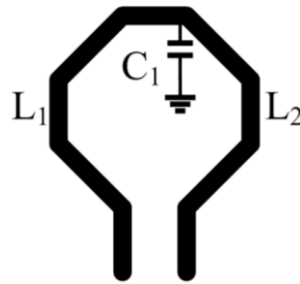
In regards to the odd-mode analysis, in Fig. 6.2, imagine driving port 2 and port 3 with differential voltages, because of the voltages along the upper and lower halves being a mirror image of each other, there is a voltage null along the middle of the circuit in Fig. 6.2. Consequently, the upper and lower part can be bisected and redrawn as shown in Fig. 6.3(a). The halved circuit, which consists

of a fourth order filter, conveys complete information on the odd-mode response of the dual-band Wilkinson power divider.

When the fourth order filter in the half-circuit shown in Fig. 6.3(a) resonates at two frequencies, the impedance looking from  $C_2$  (including  $C_2$ ) towards port 1 approaches infinity. This is “almost” similar in the case if we replace the filter by a  $\lambda/4$  transmission line, inserting it between port 1 (now terminated at a virtual ground in this case) and port 2. The qualifier “almost” applies because  $\lambda$  is specified only for one frequency, which means one has to design two  $\lambda/4$  transmission lines for the purpose of transforming impedance from zero to infinity. An advantage of using the fourth order filter lies in: it simultaneously transforming the impedance from zero to infinity at two frequencies, which realizes the dual-band operation. Additionally, referring to Figure 6.3(b), not only does it fulfill the dual-band operation demand, but also further reduces the size of the divider in the following way. As one may notice,  $L_1$  and  $L_2$  can be in series in a single inductor, distinct by a capacitor which refers to  $C_1$  in this design. As for the matching condition at port 2, since the impedance looking from  $C_2$  towards port 1 is infinite, the only loading at port 2 is the halved resistor whose value is  $0.5R$ . It is chosen to be  $50 \Omega$  so that port 2 could be matched. As in this mode of excitation, all power is delivered to the halved resistor, with none going to port 1.



(a)



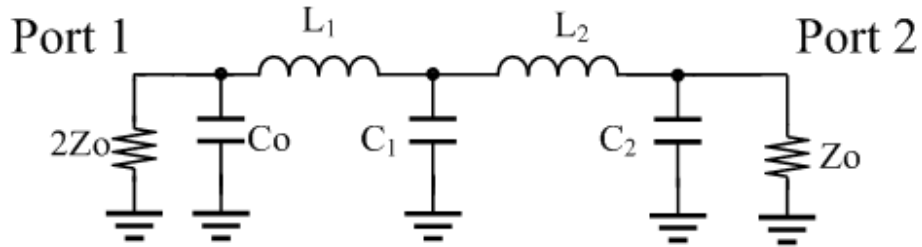
(b)

**Figure 6.3. The odd-mode analysis: (a) the halved circuit for the odd-mode analysis, (b) the proposed method to reduce the chip area by combining  $L_1$  and  $L_2$  in one planar inductor.**

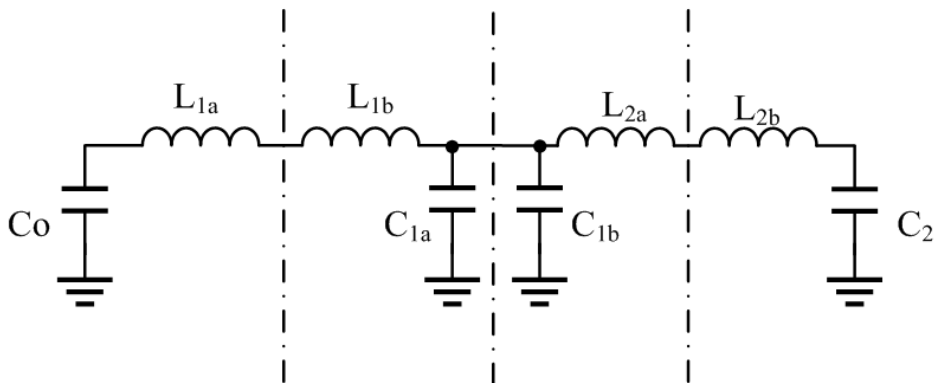
In regards to the even-mode analysis, referring to Fig. 6.2, imagine driving port 2 and port 3 with identical voltages, due to the symmetry, the lower and upper halves of the dual-band Wilkinson power divider behave identically and no current would flow through the resistor. One can bisect the divider and the new circuit is shown in Fig. 6.4.

For the even-mode excitation, a  $70.7 \Omega$  impedance line is required to transform port 2's impedance to  $100 \Omega$  at port 1. A  $\lambda/4$  transmission line of  $70.7 \Omega$  line impedance can do this, so does the LC network. To explain how it works in a simple way, the new filter network with  $C_o$  added is decomposed to four sections

as shown in Fig. 6.5.



**Figure 6.4. The halved circuit for the even-mode analysis.**



**Figure 6.5. The illustration of the decomposition of the fifth order filter.**

The characteristic impedance of the filter thus can be set to  $70.7 \Omega$  once the square root of the ratio of the inductance and capacitance in each section is  $70.7 \Omega$ . The order of the capacitance values is usually  $10^4$  smaller than that of inductors, so the effect of the additional pole introduced by  $C_o$  on the desired

peaks can be neglected. Thus, the new fifth order filter can still be deemed as a quasi- $\lambda/4$  transmission line and the “line” impedance which is actually the characteristic impedance of the LC network has been adjusted to 70.7  $\Omega$ .

After finishing the principle analysis, equations for determining the parameters can be derived as follows.

The first step is to determine the values of  $L_1$ ,  $L_2$ ,  $C_1$  and  $C_2$ . As earlier mentioned in the even-mode analysis, the impedance looking towards  $C_2$  is infinite at resonant frequencies. The expression for this impedance is given by

$$Z(s) = \frac{s(L_1+L_2)(1+s^2 \cdot L_1/L_2 \cdot C_1)}{s^4 L_1 L_2 C_1 C_2 + s^2 (L_1 C_1 + L_1 C_2 + L_2 C_2) + 1} \quad (6.1)$$

Forcing the denominator in (6.1) to zero at 24 and 77 GHz respectively, two equations and four unknowns are obtained. One can assign values to two of the unknowns and then solve the rest.

The next step is to determine the value of  $C_o$ . The procedure is as follows:

In Figure 6.2, the value of  $C_2$  is fixed due to the calculation from the previous step. The relationship between  $C_2$  and  $L_{2b}$  is held by

$$\sqrt{\frac{L_{2b}}{C_2}} = 70.7 \Omega. \quad (6.2)$$

After knowing the value of  $L_2$ ,  $L_{2a}$  can be determined since  $L_2$  is already solved from (6.1). Subsequently, the values of  $C_{1b}$ ,  $C_{1a}$ ,  $L_{1b}$  and  $L_{1a}$  can all be readily

calculated in such an iterative way. Finally, the value of  $C_o$  can now be decided which is governed by

$$\sqrt{\frac{L_{1a}}{C_o}} = 70.7 \ \Omega. \quad (6.3)$$

Note that if  $L_{1a}$  happens to be a negative value, which means that  $C_2$  has been assigned a larger value, one needs to go back to reassign a relatively small value to  $C_2$ .

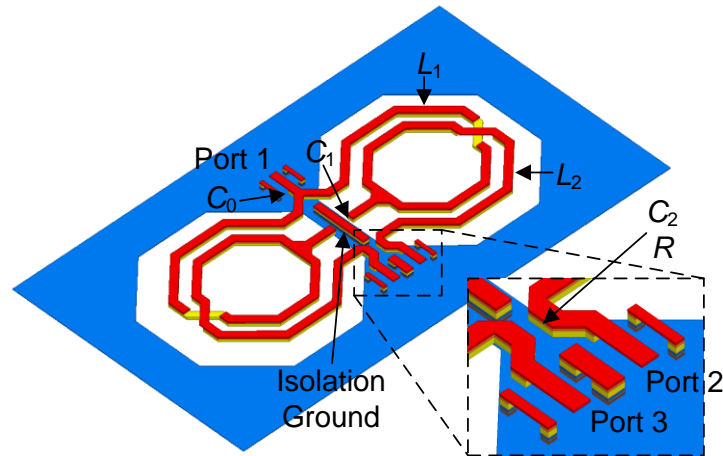
The value of  $R$  has been described in the even-mode analysis.

Thus, all the parameters needed for designing the dual-band Wilkinson power divider have been determined. Strict simulations are needed after acquiring the results by hand, because issues such as coupling has not been considered in the hand calculation.

### **6.3 Layout and Simulation Results**

The dual-band Wilkinson power divider is designed in the GLOBALFOUNDRIES 65 nm CMOS technology. The 1.325- $\mu\text{m}$  thick top aluminum metal and the 3.3- $\mu\text{m}$  thick copper metal are combined together so as to reduce the ohmic loss of the inductors. The ports are fed through 50- $\Omega$  grounded-CPW transmission lines. Metal one and two are used as the ground plane since the skin depth is larger than the thickness of metal one at 77 GHz. The isolation ground is inserted along the horizontal line as a way to reduce the

coupling. The dual-band Wilkinson power divider was simulated using Ansoft HFSS to take into account the electromagnetic interaction. The design model is shown in Fig. 6.6. The overall size for the dual-band Wilkinson power divider is  $200 \mu\text{m} \times 450 \mu\text{m}$ .



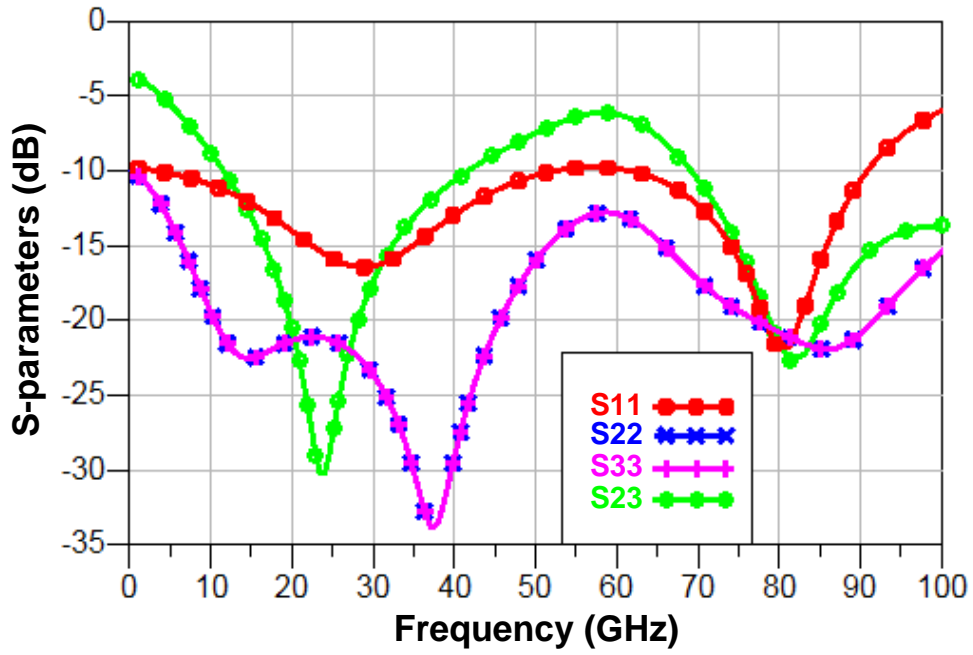
**Figure 6.6. 3-D view of the dual-band Wilkinson power divider**

The simulation results of return losses at each port, isolation between port 2 and port 3, and insertion losses are plotted in Fig. 6.7. As plotted in Fig 6.7(a),  $S_{11}$ ,  $S_{22}$  and  $S_{33}$  represent the input reflection coefficients at Port 1, 2 and 3, respectively, and they are all suppressed below -10 dB. This means that the proposed method can effectively achieve a simultaneous match at all the ports. The input coefficient at Port 1 is higher than those at Port 2 and Port 3, because the quality factor determined by the section of  $L_{1a}$  and  $C_o$  is slightly lower at low frequencies. This can be adjusted by further shrinking the size of  $L_{1a}$ . Nevertheless, the return loss at each port is quite satisfactory. The input reflection coefficients at Port 2 and Port 3 are overlapped. This means that the proposed

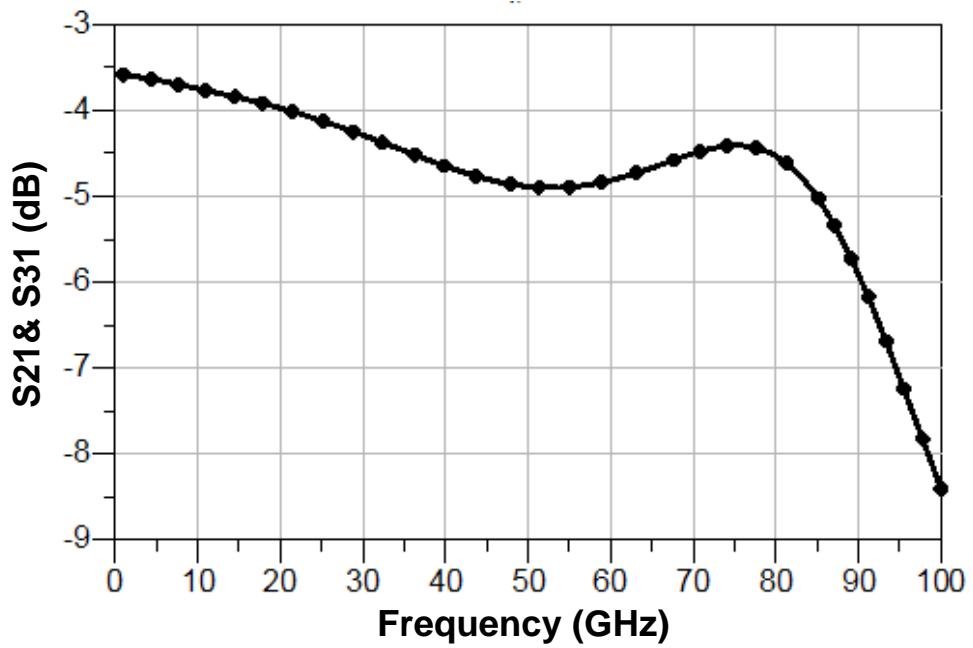
divider is highly symmetrical.  $S_{23}$  represents the isolation. As seen from Fig. 6.7(a), the leakage power at 24- and 77-GHz is negligible. The insertion loss is plotted in Fig. 6.7(b). Because of the highly symmetrical structure, the insertion losses from Port 1 to 2 and Port 1 to 3 are overlapped. Excluding the -3 dB loss due to the even power splitting, the insertion loss at 24 GHz is 1.2 dB and at 77 GHz is 1.5 dB. It means that more than 70% power has been preserved. The performance of the dual-band Wilkinson power divider is summarized in Table 6.1. As shown in Table 6.1, all the ports are well matched at both desired frequencies with adequate isolation between the output ports. By inspecting Fig. 6.7, one may also notice that this dual-band Wilkinson power divider works across a wide frequency range, e.g. from 10 GHz to 40 GHz and 70 GHz to 85 GHz.

**Table 6.1 Performance Summary of the Wilkinson Power Divider**

<b>Frequency Bands</b>	$S_{11}$	$S_{22}$	$S_{33}$	$S_{23}$	$S_{21}$	$S_{31}$
<b>K-band (centered at 24 GHz)</b>	-16 dB	-22 dB	-22 dB	-30 dB	-4.1 dB	-4.1 dB
<b>W-band (centered at 77 GHz)</b>	-20 dB	-20 dB	-20 dB	-21 dB	-4.3 dB	-4.3 dB



(a)



(b)

Figure 6.7. Simulated results of (a) the return loss and isolation, and (b) insertion loss.

## **6.4 Summary**

A new method to design a Wilkinson power divider was discussed in this chapter. Parameters of the dual-band Wilkinson power divider can be well determined by theory and equations discussed in section 6.2. The positive results demonstrated that this dual-band Wilkinson power divider is suitable for multiband operation, and not limited to two bands.

# Chapter 7

## A 65-nm CMOS LNA for Bolometer

### Applications

Previous chapters focused on the millimeter-wave application up to 77 GHz. This chapter starts to concentrate on another important application which is set at a higher frequency, i.e. the 94 GHz passive imaging. The passive imaging normally employs a radiometry receiver, known as the bolometer. Modern bolometers generally consist of large-scale arrays of detectors. Implemented in conventional technologies, such bolometer arrays suffer from integrability and productivity issues. Recently, the development of CMOS technologies has presented an opportunity for the massive production of high-performance and highly integrated bolometers. This chapter presents a 65-nm CMOS LNA, designed for a millimeter-wave bolometer's pre-amplification stage. By properly applying some positive feedback, the noise figure of the proposed LNA is minimized to at under 6 dB, and the bandwidth is extended to 30 GHz.

### 7.1 Introduction

Bolometric detectors are used to measure thermal radiation energies [76]. They have many applications, especially those conducted beyond the millimeter-wave and infrared frequencies [77]–[80]. The circuitry of a bolometric detector generally consists of a square-law detector, the output of which is directly

proportional to the incident power. In most cases, incident power is broadband thermal noise, which is at quite a low power level [81]. Therefore, in order to detect slight nuances of noise fluctuations, detectors must demonstrate fine thermal resolution. Noise-equivalent temperature difference (NETD) is such a measure used to describe the minimum resolvable temperature that a detector could differentiate. One desirable value for NETD is of the order of 0.5 K. In order to achieve such high resolution, a low noise amplifier (LNA) is generally located in front of a bolometric detector. As mentioned in [81], an LNA with a large RF bandwidth could greatly refine a detector's temperature resolution. Previously, LNAs operating in the millimeter-wave frequencies were mainly implemented in III-V semiconductor technologies [82][83]. Transistors of III-V semiconductor technologies have higher intrinsic gain and lower substrate loss, but such technologies are expensive and difficult to integrate with CMOS digital blocks. Silicon-germanium heterojunction bipolar transistors also demonstrate positive performance [16], [49], [84]–[86]. However, compared to CMOS technologies which are known for their cost-efficiency and small feature size, the foregoing issues still exist. More recently, as the feature size of CMOS technologies is continuously shrinking to the deep nanoscale, the performance of CMOS RF circuits operating at the millimeter-wave frequencies has become acceptable [55], [87]–[89]. As can be imagined, efforts devoted to improving CMOS technologies will ultimately make CMOS the best option for the fabrication of bolometer array. At present, however, designing a CMOS

millimeter-wave LNA that possesses both a low noise figure and a wide bandwidth with high gain is a challenging task. Among existing reported results, the bandwidth of a millimeter-wave CMOS LNA can hardly be greater than 20 GHz, and the noise figures are all larger than 6 dB. Therefore, there still leaves a lot of design room.

An LNA in a 65-nm CMOS technology, which aims to address the preceding issues, is presented in this Chapter. It has a low noise figure and can operate in a large frequency range. The design specifications are as follows. The topology of the LNA is a cascade of narrowband amplifiers, each resonating at a certain frequency point. The highest resonance frequency is targeted at 100 GHz and the lowest resonance frequency is targeted at 70 GHz, creating a sufficiently wide bandwidth with the aim of achieving an NETD of less than 0.5 K. The selected power supply is 1.8 V, regardless of the perception that CMOS is low power. CMOS might be regarded as a low power solution for digital blocks, but for RF amplifiers, in order to compete with those implemented in other advanced technologies, additional cost has to be paid, i.e. the power consumption.

This chapter is organized as follows. Design considerations and circuit analysis are discussed in section 7.2. Firstly, as earlier mentioned, the noise performance of a single transistor is determined by its size, i.e. the gate-width. The first stage can be regarded as the LNA's LNA, because according to the Friis formula given by (3.24), the noise figure of the first stage has the most impact on the overall noise figure. However, a transistor with a small gate-width normally has less gain

than a wider one. For this reason, in section 7.2.1, the design consideration on size selection discusses the balance between the gain and noise performance of a single transistor. Next, for the first stage consisting of transistors with a relatively small size, section 7.2.2 proposes a method to boost its gain. As indicated by the Friis formula, the noise figure of the following stages is balanced by the gain of the first stage. Followed by section 7.2.2, section 7.2.3 proposes a method which modifies the conventional stagger tuning method. The method helps the following stages to accumulate enough gain over a wide frequency-range, thus achieving a balance between the gain and the bandwidth. Section 7.3 describes and summarizes the circuit implementation and experimental results. A conclusion is drawn in section 7.4.

## 7.2 Design Considerations and Analysis

In Chapter 1, a general equation that defines the thermal resolution of a bolometric detector has been given. For completeness, (7.1) gives a more accurate expression [85]:

$$\text{NETD} = T_{\text{SYS}} \sqrt{\frac{2B_{\text{IF}}}{B} + \left(\frac{\Delta G}{G}\right)^2 + \frac{1}{2\tau} \cdot \left(\frac{\text{NEP}}{k_B \cdot G \cdot \text{BW} \cdot T_{\text{SYS}}}\right)^2}, \quad (7.1)$$

where  $B_{\text{IF}}$  is the IF bandwidth,  $B$  is the RF bandwidth,  $G$  is the gain before the detector,  $\Delta G$  is the gain fluctuation which can be eliminated using a Dicke Switch,  $\tau$  is the integration time,  $k_B$  is Boltzmann's constant,  $\text{NEP}$  is short for

the noise-equivalent power, and  $T_{SYS}$  is the noise temperature of the detector system.

If the performance of the LNA can dominate NETD, (7.1) can be further reduced to:

$$NETD = T_{SYS} \sqrt{\frac{1}{BW \cdot \tau}}. \quad (7.2)$$

As can be seen from (7.2),  $T_{SYS}$  serves as a weighting factor for NETD. Additionally, its magnitude is determined by the noise figure of the LNA, and in turn, the device size of the LNA has a considerable impact on the noise figure. Therefore, prior to the circuit design, sizes of transistors have to be determined at the outset. Section 7.2.1 describes the consideration of size selection.

### 7.2.1 Device Sizing

As introduced in Chapter 2, transistors in an LNA generate a large amount of noise, which increases the noise figure. Referring to Chapter 5, the minimum noise figure that an MOS transistor can achieve is expressed as follows [26]:

$$NF_{min} = 1 + 2 \left( \frac{\omega_o}{\omega_T} \right) \sqrt{\frac{\gamma \delta}{\kappa} (1 - |c|^2)}, \quad (7.3)$$

where  $\sqrt{\frac{\gamma \delta}{\kappa} (1 - |c|^2)}$  can be treated as a constant,  $\omega_o$  denote the operating

frequency, and  $\omega_T$  is the transition frequency, which is determined by the transconductance and the gate-length and -width of the MOS transistor. Given the fact that for most LNA designs, the gate-length is generally the minimum channel length,  $NF_{min}$  depends on the transconductance and gate-width only. This implies that for a fixed transconductance, a narrow device possesses a lower noise figure than a wide one does. In other words, with the same amount of drain current, a smaller transistor generates a smaller amount of noise than a larger one does. In short, if the noise figure is one's primary concern, then the selected gate-width of the MOS transistor should not be too wide.

The gate-width is the sum of the total finger-width. For the proposed LNA, the finger-width is selected as 1  $\mu\text{m}$ , based on the evaluation carried out in [55]. The selection of the total finger-width, i.e. the gate-width, is based on following judgment. As can be inferred from (3), the smaller the size is, the smaller the noise figure would be. The noise figure, on the other hand, is related to the gain of the first stage, which will be discussed later in Chapter 7.2.2. Note that the gain of the first stage in [55]'s LNA has not been boosted by any gain-enhancement techniques, in which a cascode amplifier, consisting of 20- $\mu\text{m}$ -gate-width transistors, provides a gain about 5 dB at 90 GHz. Additionally, note that the maximum available gain of a 15- $\mu\text{m}$ -gate-width NMOS transistor configured in a common-source topology is about 10 dB. Therefore, an estimation can be quickly made. If once the gain be enhanced, the transistor with a gate-width of 15  $\mu\text{m}$  can possess an even smaller noise figure, say less than 6 dB, compared to

the noise figure reported in [55]. Based on the foregoing judgment, in the proposed LNA, the gate-width of the transistors used in the first stage is selected to be 15  $\mu\text{m}$ . As will be discussed later, following stages have less impact on overall noise figure. Therefore, their device size can be set to a larger value.

## 7.2.2 First Stage Configuration

At this stage, cascode configuration as illustrated in Fig. 2.4(a) is adopted [14]. The cascode configuration is a common-source-common-gate amplifier, as redrawn in Fig. 7.1.  $L_1$  and  $L_2$  in Fig. 7.1 are used to tune out parasitic capacitors. The common gate transistor,  $M_2$ , is used to increase the output impedance by a factor of  $g_{m2} \cdot r_{o2}$ , where  $g_{m2}$  is the transconductance of  $M_2$ , and  $r_{o2}$  stands for the drain to source resistance of  $M_2$ .  $M_2$  does not provide much gain, due to its limited output impedance. Actually,  $M_2$  is only used to improve the reverse isolation of the cascode amplifier.

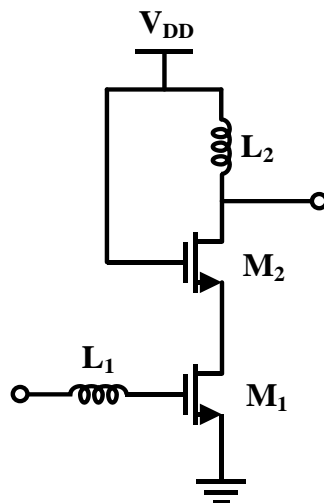


Figure 7.1 The conventional configuration of the cascode amplifier.

If the operating frequency is located far below the transition frequency, then the performance of the cascode amplifier can be as effective as it is supposed to be. However, in the millimeter-wave frequency range, the noise issue caused by low intrinsic gain starts to arise.

Prior to describing the noise issue from which a cascode amplifier may suffer, it is worth revisiting Friis's noise formula [81]. As introduced in Chapter 3, Friis's noise formula is used to estimate the total noise figure of a system consisting of a cascade of stages. For a cascade of common-source and common-gate stages, the total noise figure is

$$NF_{total} = NF_{common-source} + \frac{NF_{common-gate}-1}{G_{M1}} + \frac{NF_L-1}{G_{M1} \cdot G_{M2}}, \quad (7.4)$$

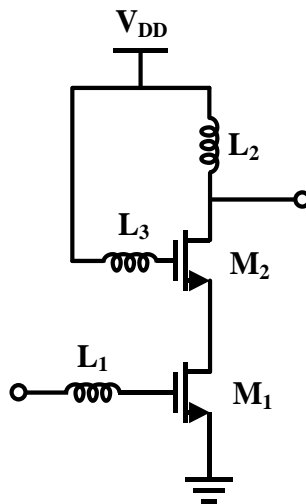
where  $NF_{common-source}$  and  $NF_{common-gate}$  denote the noise figure of the common-source and common-gate amplifier, respectively.  $NF_L$  is the noise figure of the following stage.  $G_{M1}$  and  $G_{M2}$  stand for the available power gain provided by  $M_1$  and  $M_2$ , respectively.

Equation (7.4) provides two design insights. The first one is that, the total noise figure largely depends on  $M_1$ , because no preceding gain is available there to minimize the noise figure of  $M_1$ . The second one is that if  $M_1$  and  $M_2$  lack sufficient gain, then the noise stemming from  $M_2$  and its following stages may not be minimized, and thus the total noise figure will increase.

For an NMOS transistor operating in the millimeter-wave frequency range, the

intrinsic gain is generally low. Consequently, when operating at such high frequencies, this low intrinsic gain may not be able to minimize the noise figure of the following stages. Noise issues therefore start to arise, as just pointed out.

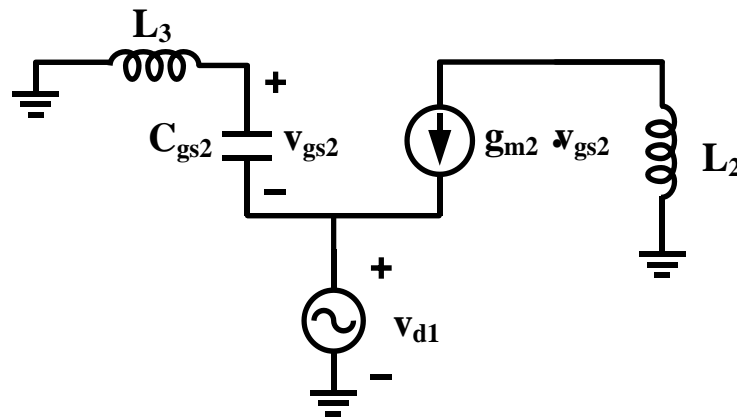
The noise issue can be alleviated nevertheless. First, the noise contributed by  $M_1$  can be minimized simply by decreasing its gate-width, as mentioned in section 7.2.1. Second, in order to minimize the second and third terms in (7.4), both the gain of  $M_1$  and  $M_2$  should be enhanced. A structure aiming to boost the gain of  $M_1$  and  $M_2$  is proposed in Fig. 7.2.



**Figure 7.2 The modified cascode amplifier aiming for the gain enhancement.**

Compared to a conventional cascode amplifier, an inductor,  $L_3$ , is inserted between the gate terminal of  $M_2$  and its power supply terminal,  $V_{DD}$ . This type of

configuration is known as gate inductive feedback [62] [90], as briefly introduced in Chapter 5. Gate inductive feedback can be applied to enhance the gain of  $M_2$ . Its working principle is as follows. After the insertion of  $L_3$ , a voltage is correspondingly developed at the gate terminal, and its amplitude equals that of the voltage drop across  $L_3$ . The voltage drop across  $L_3$  is flexible, because its amplitude is determined by another flexible value, the current strength flowing through  $L_3$ . A design insight to enhance the transconductance of  $M_2$  is enlightened therefrom. Since the voltage drop across  $L_3$  can be used to vary the amplitude of  $v_{gs2}$ , it seems possible that the output current,  $g_{m2} \cdot v_{gs2}$ , could be enhanced accordingly. In order to gain more design insight, a circuit model for small-signal analysis is shown in Fig. 7.3.



**Figure 7.3** The small-signal model for analyzing the gate inductive feedback.

As shown in Fig. 7.3, without  $L_3$ , the amplitude of the voltage drop across the gate to source capacitor,  $C_{gs2}$ , simply equals to the drain voltage of  $M_1$ , i.e.  $v_{d1}$ . Due to the insertion of  $L_3$ , voltage drop across the capacitor starts to vary. The new expression for the voltage drop across  $C_{gs2}$  can be obtained based on the small-signal model in Fig. 7.3:

$$v_{gs2} = -\frac{v_{in}}{1-\omega^2 L_3 C_{gs2}}, \quad (7.5)$$

According to (7.5), when the denominator becomes less than one,  $v_{gs2}$  can be greater than  $v_{in}$ . The output current thereby gets increased. This is to say that,  $L_3$  can be served as one degree of design freedom. With the increase of  $L_3$ , the amplitude of the output current can be enhanced. Although it seems that  $v_{gs2}$  could be raised to an infinite value, this scheme suffers from instability issues. In fact, such configuration is supposed to create a negative impedance for oscillators. Specifically to say that, referring to Fig. 7.3, the newly added inductor,  $L_3$ , is in series with  $C_{gs2}$ . If  $L_3$  increases continuously, then at a certain point, it will start to resonate with  $C_{gs2}$ . The resonance frequency is given by the following:

$$\omega_r = \frac{1}{\sqrt{L_3 C_{gs2}}}. \quad (7.6)$$

At such resonance, the input impedance at the source of  $M_2$  drops to zero. Consequently, if  $L_3$  increases continuously, for  $M_2$ , such an increase may create

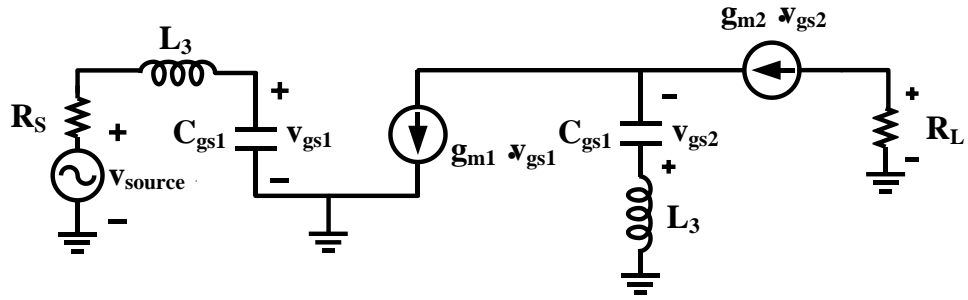
a negative impedance at its source terminal. Therefore, care must be taken in order to keep  $M_2$  from oscillating.

At the moment when  $\frac{1}{\sqrt{L_3 C_{gs2}}}$  becomes infinitely close to  $\omega_r$ , the inductive feedback can provide its highest current gain. At this moment, all of the current generated by  $M_1$  flows to  $C_{gs2}$  and  $L_3$ . The relationship between the drain currents in  $M_1$  and  $M_2$  can be found based on the small-signal model shown in Fig. 7.3:

$$i_{d2} = \frac{g_{m2}}{C_{gs2}\omega_0} \cdot \frac{i_{d1}}{j} = \frac{\omega_{T2}}{\omega_0} \cdot \frac{i_{d1}}{j}, \quad (7.7)$$

where  $i_{d1}$  and  $i_{d2}$  denote the drain currents of  $M_1$  and  $M_2$ , respectively and  $\omega_{T2}$  is the transition frequency of  $M_2$ . Recall that for a 65-nm CMOS technology,  $\omega_T$  is about 200G rad/s. This implies that, when gate inductive feedback is applied, the magnitude of the output current can be doubly enhanced.

The foregoing discussion shows that gate inductive feedback boosts transconductance. In addition, its noise behavior should be also taken into the consideration. In order to calculate the noise figure of the circuit shown in Fig. 7.2, a small-signal model is redrawn in Fig. 7.4.



**Figure 7.4** The small-signal model of the circuit shown in Fig. 7.2.

Applying nodal analysis, the expression for the voltage gain can be obtained as follows:

$$A_v = \frac{R_L}{R_S} \cdot \frac{\omega_{T1}}{\omega_o} \cdot \frac{1}{1 + \frac{1}{g_{m2}(\frac{1}{j\omega C_{gs2}} + j\omega L_3)}}. \quad (7.8)$$

For the sake of simplicity, assume that in each transistor, the drain noise current is the only noise source. Dividing the output noise by the gain calculated in (7.8), the expression of the noise figure can be obtained.

$$NF = 1 + \gamma_1 g_{d1} R_S \left( \frac{\omega_o}{\omega_{T1}} \right)^2 \left( 1 + \frac{\gamma_2 r_{o1}}{\gamma_1 r_{o2}} \cdot \left( 1 + \frac{\omega_{T1} L_3}{R_S} \right)^2 \left( \frac{\omega_o C_{gs2}}{g_{m2}} \right)^2 \right). \quad (7.9)$$

Assuming that  $M_1$  and  $M_2$  share the same device size, (7.9) can be further simplified to the following:

$$NF = 1 + \gamma_1 g_{d1} R_S \left( \frac{\omega_o}{\omega_{T1}} \right)^2 \left( 1 + \left( 1 + \frac{\omega_{T1} L_3}{R_S} \right)^2 \left( \frac{\omega_o C_{gs2}}{g_{m2}} \right)^2 \right). \quad (7.10)$$

Equation (7.10) shows that  $L_3$  does contribute some noise. However, from a close look at (7.10), it is discernible that  $L_3$  merely increases the noise figure. Referring to (7.10), the term  $\frac{\omega_{T1} L_3}{R_S}$  is multiplied by a weighting factor,  $\left( \frac{\omega_o C_{gs2}}{g_{m2}} \right)^2$ . If  $L_3$  is of the order of 100 pH and  $\omega_{T1}$  is about 200G rad/s,  $\frac{\omega_{T1} L_3}{R_S}$  then roughly equals 1 and  $\left( \frac{\omega_o C_{gs2}}{g_{m2}} \right)^2$  is of the order of 1/4. This means that the weighing factor could scale down  $\frac{\omega_{T1} L_3}{R_S}$  by a factor of 75%.

In order to further minimize the noise caused by the insertion of  $L_3$ , additional gain has to be provided by  $M_1$ . Moreover, the demand for additional gain is not only due to the noise incurred by  $L_3$  but also mainly due to the fact that the gain of  $M_1$  is critical for the overall noise figure. This is because, as discussed earlier, referring to (7.4), the gain of  $M_1$  is used to minimize the noise figure of  $M_2$ .

Fortunately, without any modification,  $M_1$  itself can be used to enhance its own gain. The gate to drain capacitor associated with  $M_1$  naturally boosts the gain in a small frequency range; albeit, it is notorious for its Miller effect. Although the Miller effect can potentially reduce the bandwidth, for wideband LNAs consisting of multi-stages, the frequency response of each stage is not meant to be wide. This is to say one can fully take advantage of such a gain boosting ability and apply it to a small frequency range.

That the gain can be boosted is due to the decrease in the phase-margin. Referring to  $M_1$  as shown in Fig. 7.2, where  $C_{gd}$  is a Miller capacitor, the

voltage gain from the drain terminal to the gate is given by [58]:

$$A_{V-M1} = \frac{a(s)}{1+e^{-j\varphi}} \quad , \quad (7.11)$$

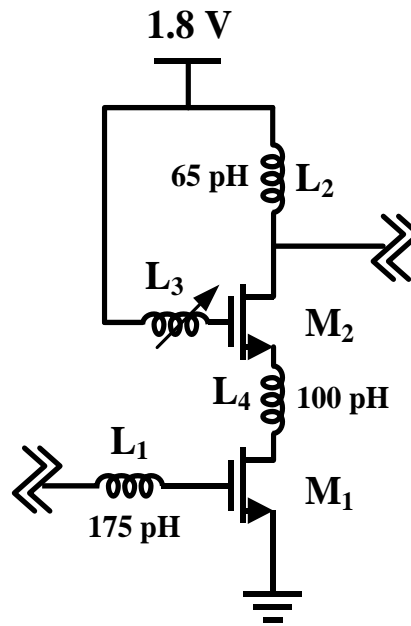
where  $a(s)$  is the open loop gain of  $M_1$ , and  $\varphi$  is the phase of the loop gain. As shown in (7.11), once the denominator becomes less than one,  $A_{V-M1}$  gets increased. In other words, the gain can be boosted at the expense of a decrease in the phase-margin.

The decrease of the phase-margin means that the amplifier requires more settling time. Although this is usually the case for operational amplifiers, the settling time is not considered as a critical parameter for LNAs. Moreover, for a bolometric detector, the integration time,  $\tau$ , which is typically about 30 ms, is long enough for the amplifier to settle. The real issue associated with the phase-margin decreasing is stability. Therefore, care must be taken when the phase-margin decreases.

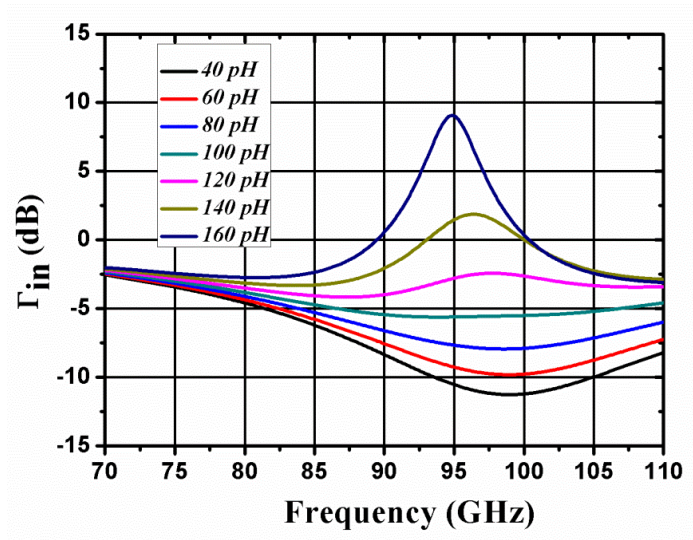
The decrease of the phase-margin also means that the phase difference between the input and output is getting larger. In fact,  $L_3$  accelerates such a decreasing trend. As can be noticed in (7.7), under this circumstance, the phase difference between  $i_{d1}$  and  $i_{d2}$  can be as large as  $90^\circ$ . Therefore, as long as the amplifier is unconditionally stable, by increasing  $L_3$ , both the gain of  $M_1$  and  $M_2$  can be enhanced simultaneously.

The instability issues can be avoided by checking the stability factor back and

forth during each design iteration. However, the decrease of the phase-margin can cause another problem. The magnitude of the input reflection coefficient may become seriously distorted. In order to illustrate this phenomenon, a practical example is given in Fig. 7.5(a). As shown in Fig. 7.5(a), the conventional cascode amplifier is modified by the gate inductive feedback. By sweeping the inductance of  $L_3$  from 40 pH to 120 pH, the corresponding input reflection coefficients are found and summarized in Fig. 7.5(b). Here,  $L_4$  is used to resonate out the capacitors distributed along the current path and to compensate for some frequency-shifts which can also be noticed in Fig. 7.5(b).



(a)



(b)

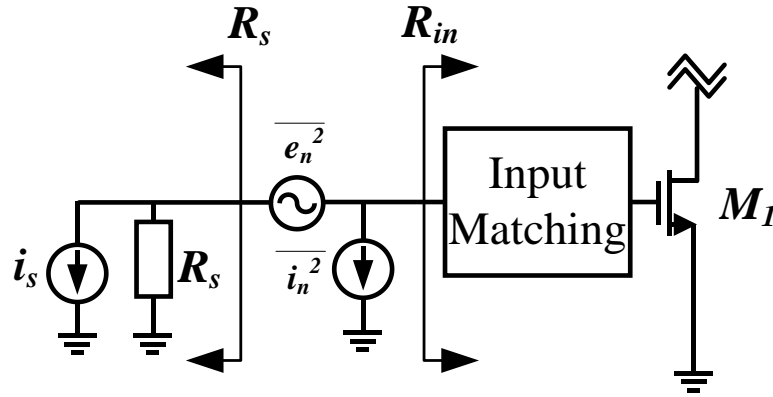
**Figure 7.5 (a) A practical circuit example given to demonstrate  $L_3$ 's impact on the input reflection coefficient; (b) the plot of the input reflection coefficient versus the increase of  $L_3$ .**

As can be clearly seen from Fig. 7.5(b), the increase of  $L_3$  increases the input reflection coefficient significantly. When the input reflection coefficient is raised to above 0 dB, at the input port, the received power surmounts the incident. This means that the LNA becomes an oscillator.

Given the fact that  $L_3$  can have a large impact on the input reflection coefficient, it seems that there is a tradeoff between the strength of the gain-enhancement and the magnitude of the input reflection coefficient. This tradeoff appears to be reasonable since a good source matching seems necessary for a high gain. However, this is not the case given the fact that the gain-enhancement can already improve the gain on its own. In other words, as long as the gain stays satisfactory, the input reflection coefficient can be of any magnitude unless it exceeds 0 dB. It is also worth mentioning that the peaking phenomenon observed in Fig. 7.5(b)

is caused by the output power leakage through the feedback capacitor  $C_{gd}$ . Even when the input reflection coefficient equals to 0 dB, it is by no means possible to say that all the incident power has been reflected. In fact, this just suggests that the positive feedback brings additional power from the output to the input port.

The distortion of the input reflection coefficient may also lead to another concern. It seems plausible that a good source matching is a prerequisite for a satisfactory noise performance. However, it is not true. In order to reinforce the view that the input matching network has no impact on the noise performance, consider a general case. The common source amplifier breakout is drawn in Fig. 7.6. All the noise sources associated with  $M_1$  are referred to input, as represented by two equivalent noise sources. Focusing on the input port, for simplicity's sake, noise stemming from  $M_2$  and its following is neglected. The two equivalent noise sources are assumed to be irrelevant to each other, for simplicity's sake as well. The gate noise is included, since its noise resistance influences the input impedance in this case.



**Figure 7.6 The circuit model to analyze the impact of the input matching on the noise figure.**

Firstly, consider that the input impedance at the gate terminal of  $M_1$  has been perfectly matched to source, i.e.  $R_S = R_{in}$  and no reflection happens. It can be shown that, when  $R_S = R_{in}$ , the expression of the noise figure is

$$NF = 1 + (F_d - 1) + (F_g - 1) , \quad (7.12)$$

where  $(F_d - 1)$  is:

$$F_d - 1 = \gamma \left( \frac{\omega_o}{\omega_T} \right)^2 \frac{g_m}{R_S} (R_S + r_g)^2 , \quad (7.13)$$

and  $(F_g - 1)$  is:

$$F_g - 1 = \frac{r_g \alpha \delta}{R_S} . \quad (7.14)$$

The full expression of (7.12) is

$$NF = 1 + \gamma \left( \frac{\omega_o}{\omega_T} \right)^2 \frac{g_m}{R_S} (R_S + r_g)^2 + \frac{r_g \alpha \delta}{R_S}. \quad (7.15)$$

Secondly, consider the case when  $R_S \neq R_{in}$ . Under this case, due to the mismatch, reflection occurs. To derive the expression of the noise figure in this case, assume that  $R_S$  is a variable parameter and  $R_{in}$  is a fixed one. At the plane inserted between  $R_S$  and  $R_{in}$ , incident power bounces back and forth, as represented by the input reflection coefficient  $\Gamma$ . The new expression of the noise figure as a function of  $\Gamma$  is given by

$$NF = 1 + \frac{1+\Gamma}{1-\Gamma} \left( \frac{R_S+r_g}{R_{in}+r_g} \right)^2 (F_d - 1) + \frac{1+\Gamma}{1-\Gamma} (F_g - 1), \quad (7.16)$$

where  $\Gamma$  is defined as follows:

$$\Gamma = \frac{R_{in}-R_S}{R_{in}+R_S}. \quad (7.17)$$

Substituting (7.13), (7.14) and (7.17) into (7.18), yields

$$NF = 1 + \gamma \left( \frac{\omega_o}{\omega_T} \right)^2 \frac{g_m}{R_S} (R_S + r_g)^2 + \frac{r_g \alpha \delta}{R_S}. \quad (7.18)$$

Since (7.15) and (7.18) share the same expression, a conclusion can be drawn.

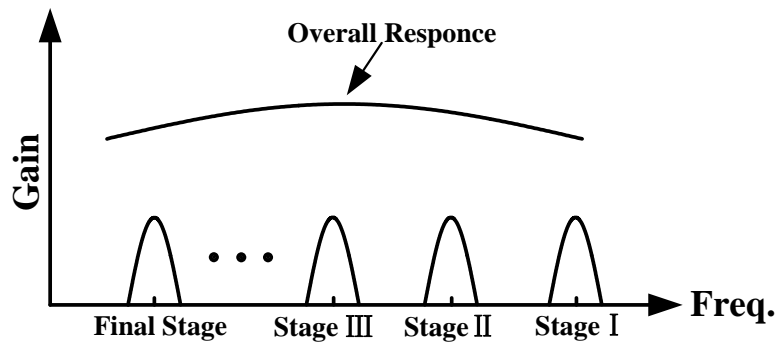
The noise figure under the unmatched case is the same noise figure as when  $R_S = R_{in}$ . It can also be proven that when noise from following stages is included in the calculation, this conclusion still holds true [64]. Moreover, referring to Chapter 3, expressions associated with the noise figure have no items related to the input coefficient [26].

All in all, the peaking phenomenon observed in Fig. 7.5(b) barely affects the noise performance. Moreover, this suggests that for a wideband LNA consisting of multi-stages of narrowband amplifiers, the bandwidth of the input reflection coefficient is not necessarily wide. For example, as can be seen in [87], only within a limited frequency range does the input reflection coefficient fall below -10 dB, but the noise performance still does not deteriorate in the frequency range where the magnitude of the input reflection coefficient is larger than -10 dB.

### **7.2.3 Configurations of Following Stages**

The following stages are designed to provide gain for remaining frequency points so that when combined together with the first stage, the LNA can provide a flat gain over a large frequency range. Staggered tuning amplification introduced in Chapter 2 is adopted here.

Conventionally, as shown in Fig. 7.7, the first stage resonates at the highest frequency, and the resonance frequencies of the following stages are placed in descending order [20].

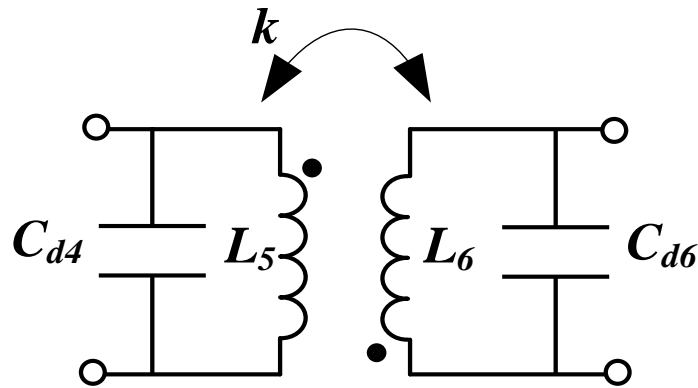


**Figure 7.7 The frequency domain illustration of the conventional amplification scheme.**

However, if the gain of the first stage is enhanced too aggressively, then the conventional amplification scheme might not work so well. As can be imagined, before being amplified by the final stage, the lowest resonance frequency barely receives any gain. This means it is a laborious job for the final stage to drag up the gain at the lowest resonance frequency. Therefore, in the proposed LNA, the second stage is designed to provide gain for the lowest resonance frequency before it is too late to do so at the final stage.

As given by the design specifications, the lowest resonance frequency is located relatively far from the highest. In order to enhance the gain at the lowest resonance frequency while not diminishing the gain at the highest, the loading of the second and third stage can be designed as a dual-band filter on account of its dual peaking ability. The principle of the dual-band loading is as follows. Assuming that the output impedance of the cascode amplifier is high, the loading networks of the second and third stages can be treated as a transformer that is combined in parallel with two lumped parasitic capacitors at the drain of  $M_4$  and

$M_6$ , as shown in Fig. 7.8. Note that the phases of the second and third stages are  $180^\circ$  out of phase. Therefore, in order to enhance the voltage amplitude at each winding, the polarity of the transformer is reversed. The reversal of polarity imposes positive feedback between the two windings, which efficiently enhances the gain at the lowest resonance frequency.



**Figure 7.8** The equivalent circuit model of  $M_4$  and  $M_6$ 's loading networks.

The working principle of the transformer loading shown in Fig. 7.8 is as follows. The input impedance seen at the primary side is

$$Z_{primary-in} = \frac{(j\omega)^3(1-k^2)L_5L_6C_1+j\omega L_5}{1+(j\omega)^4(1-k^2)L_5L_6C_{d4}C_{d6}+(j\omega)^2(L_5C_{d4}+L_6C_{d6})} \quad (7.19)$$

Similarly to (6.1) in Chapter 6, forcing the denominator of (7.19) to become zero can yield the expressions of the highest and lowest resonance frequencies, as given by the following expressions:

$$f_{lowest} = \sqrt{\frac{2}{f_1^2 + f_2^2 + \sqrt{4k^2 f_1^2 f_2^2 + (f_2^2 - f_1^2)^2}}} \cdot f_1 f_2 , \quad (7.20)$$

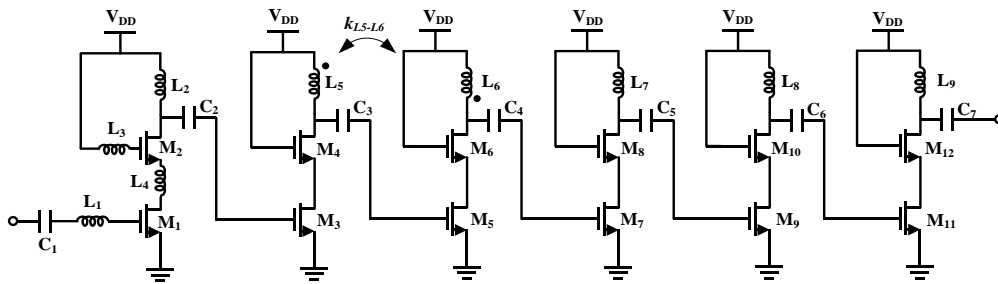
$$f_{highest} = \sqrt{\frac{2}{f_1^2 + f_2^2 - \sqrt{4k^2 f_1^2 f_2^2 + (f_2^2 - f_1^2)^2}}} \cdot f_1 f_2 . \quad (7.21)$$

where  $f_1^2 = \frac{1}{4\pi^2 L_5 C_{d4}}$  and  $f_2^2 = \frac{1}{4\pi^2 L_6 C_{d6}}$ .

The coupling-factor  $k$  can be treated as a degree of design freedom. It provides (7.20) and (7.21) two different denominators. The larger the difference, the wider the bandwidth. However, a strong coupling may also make the LNA unstable. In view of this, design iterations become necessary as to find a suitable value for  $k$ . The recommended iteration is as follows. The initial value of  $k$  can be set to 0.15, which produces moderate positive feedback. Note that the highest and lowest resonance frequencies are already given by the design specifications. Also note that the capacitances of  $C_{d4}$  and  $C_{d6}$  can be treated as known quantities as well.  $L_5$  and  $L_6$  can then be solved using (7.20) and (7.21). If the solved results returns an unstable LNA, then  $k$  has to be reset to a smaller value, which leads to another round of design.

Subsequent stages are all made up of conventional cascode amplifiers. They are designed to raise the gain between the highest and lowest resonance frequencies. Since subsequent stages do not have much impact on the overall

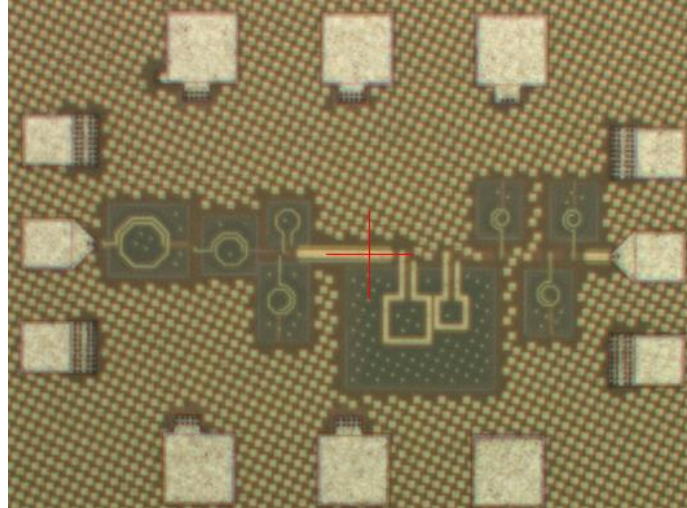
noise figure, their gate-width can be set to be larger in order to provide more gain. Also note that several instability factors have already hidden in the design, therefore, additional cost at the expense of stability should be avoided. Therefore, gate inductive feedback is not applied to the following stage designs. Combined with the first stage, the final structure for the proposed LNA is shown in Fig. 7.9.



**Figure 7.9** The proposed LNA structure (biasing circuits are not shown).

### 7.3 Circuit Implementation and Measurement Results

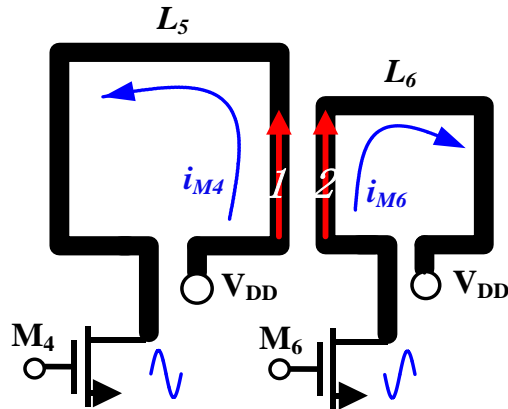
The circuit is implemented in GlobalFoundries standard 65-nm low-power CMOS technologies. The die photo is shown in Fig. 7.10. The chip area is 660  $\mu\text{m} \times 490 \mu\text{m}$ . Total power consumption is 83.3 mW.



**Figure 7.10 The die photo of the proposed LNA.**

The transformer is designed in Ansoft HFSS. It consists of two rectangular inductors as shown in Fig. 7.11. The primary and secondary windings are placed on the same top metal layer. Instead of stacking the primary and secondary windings vertically on different layers, such a placement can limit the coupling strength and also improve the quality factor. Segments 1 and 2 are placed close to each other, providing a moderate mutual coupling. The strength of the mutual coupling is adjustable and it is determined by the distance between the two segments. Recall that polarities of the primary and secondary windings are  $180^\circ$  out of phase. This means that if the current in one winding flows inwards to the power supply, then the current in the other winding flows outwards. In order to achieve the positive feedback, both Segment 1 and Segment 2 should carry currents in the same direction. As shown in Fig. 7.11, the power supply is inserted in between the drain terminals such that although the current directions are different with respects to the power terminals, in Segments 1 and 2 the currents

flow in the same direction.



**Figure 7.11 The illustration of the implementation of the circuit model shown in Fig. 7.8.**

All the inductors and interconnections that are longer than 5  $\mu\text{m}$  are simulated in Ansoft HFSS. Their inductance and quality factors are summarized in Table 7.1. Parasitic capacitors are also treated as part of the matching network. Capacitors  $C_1 \sim C_7$  are all finger capacitors, on account of the poor quality factors associated with MIM capacitors above 60 GHz. The corresponding capacitance is summarized in Table 7.1 as well. The simulated ac responses at each drain terminal of the common-gate amplifiers are plotted in Fig. 7.12. The final stage is designed as a buffer, which provides a voltage gain around 0 dB. The simulated power consumption of the final stage is 14.8 mW.

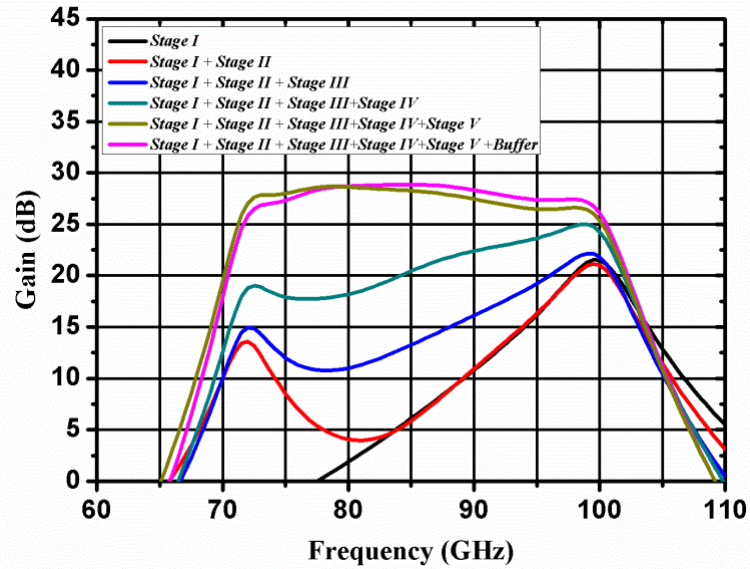


Figure 7.12 Simulated AC responses at outputs of each stage.

Table 7.1 Inductance and Capacitance Summary

Component	Value	Remark
$L_1$	242 pH	$Q=15$
$L_2$	39 pH	$Q=22$
$L_3$	99 pH	$Q=20$
$L_4$	141 pH	$Q=17$
$L_5$	90 pH	$Q=21, k=0.08$
$L_6$	59 pH	$Q=22, k=0.08$
$L_7$	63 pH	$Q=17$
$L_8$	80 pH	$Q=16$
$L_9$	64 pH	$Q=17$
$C_1$	59 fF	Metal Finger Capacitors
$C_2$	90 fF	Metal Finger Capacitors
$C_3$	59 fF	Metal Finger Capacitors
$C_4$	128 fF	Metal Finger Capacitors
$C_5$	128 fF	Metal Finger Capacitors
$C_6$	128 fF	Metal Finger Capacitors
$C_7$	64 fF	Metal Finger Capacitors

The circuit is measured via on-wafer probing. S-parameters are measured based on Agilent's N5260 extenders for millimeter-wave applications. Noise figure measurement is done with a Rohde & Schwarz's SNF-110 noise-figure test-suit. In measuring the 1-dB power compression point, a Rohde & Schwarz's SMF 100A signal generator is combined with a 6×multiplier and two attenuators, to provide calibrated output power ranging from -35 dBm to -25 dBm.

Measurement results are plotted below. The discrepancy of the measured and simulated results can be attributed to the process variation and the model accuracy. The simulated and measured input and output reflection coefficients ( $s_{11}$  and  $s_{22}$ ) are plotted in Fig. 7.13. Both  $\Gamma_{in}$  and  $\Gamma_{out}$  are smaller than 0 dB, meaning that the LNA is unconditionally stable. The simulated and measured results of transducer gain ( $s_{21}$ ) and noise figure are plotted in Fig. 7.14. The -3-dB bandwidth ranges from 69 GHz to 99 GHz, with a peak gain of 25 dB at 85 GHz. The minimum noise figure is 5.1 dB at 98 GHz. As can be seen from Fig. 7.14, the location of the minimum noise figure is associated with the highest resonance frequency, because gain at the first stage has suppressed the noise stemming from the following stages. This may probably reduce some design iterations, because the location of the minimum noise figure and the highest resonance frequency has henceforth become one design variable. The measured output 1-dB compression point ( $OP_{1-dB}$ ) is -8 dBm, as marked in Fig. 7.15. It is noteworthy that bolometers do not quite demand on the linearity performance. Even if the input 1-dB compression point degrades to as low as -50 dBm,

according to bolometer standards, that is still not yet an unacceptable result, because it still far exceeds the noise power-level. Moreover, at such a high frequency range, communication interferences are unlikely to happen [55]. Comparison results are summarized in Table 7.2. As can be noticed in Table 7.2, the proposed LNA achieves the lowest noise figure. This is for two reasons. Firstly, the gain-enhancement applied to the first stage further minimizes the noise stemming from the following stages. Secondly, as discussed in Chapter 3 and section 7.2, the amount of thermal noise from the transistors of  $M_1$  and  $M_2$  has been reduced due to the smaller gate width. The linearity performance is in trade-off with the noise performance. The gain-enhancement boosts the gain of the first stage, and at the same time, the linearity performance deteriorates. However, such a trade-off improves the noise performance. As mentioned in [85], empirically, the second and the following stages of an LNA may contribute a noise figure about 2 dB to the overall noise figure. The gain-enhancement further minimizes the effect of the following stages on the overall noise figure. Alternatively, if linearity is one's primary concern, the noise figure can be traded off, as shown by [91] listed in Table 7.2.

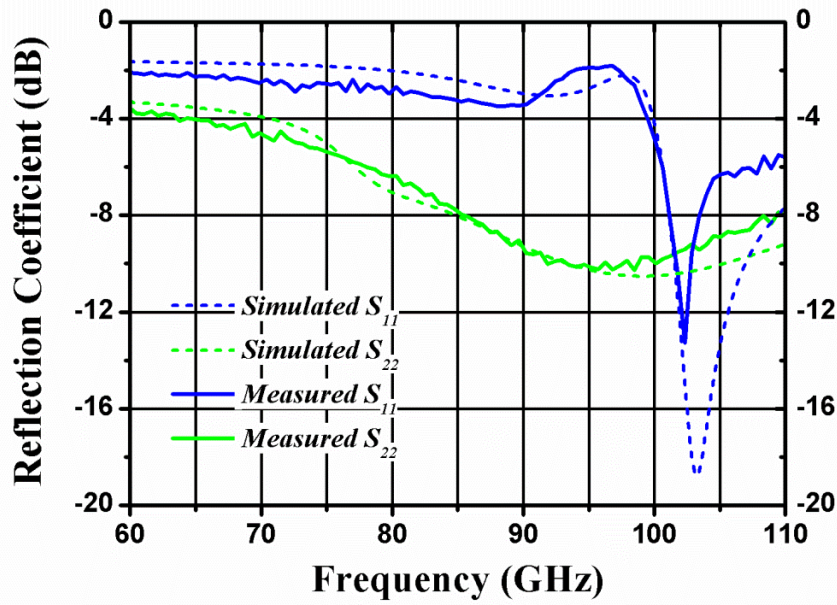


Figure 7.13 Simulated (dashed line) and measured (solid line) results of the input and output reflection coefficients.

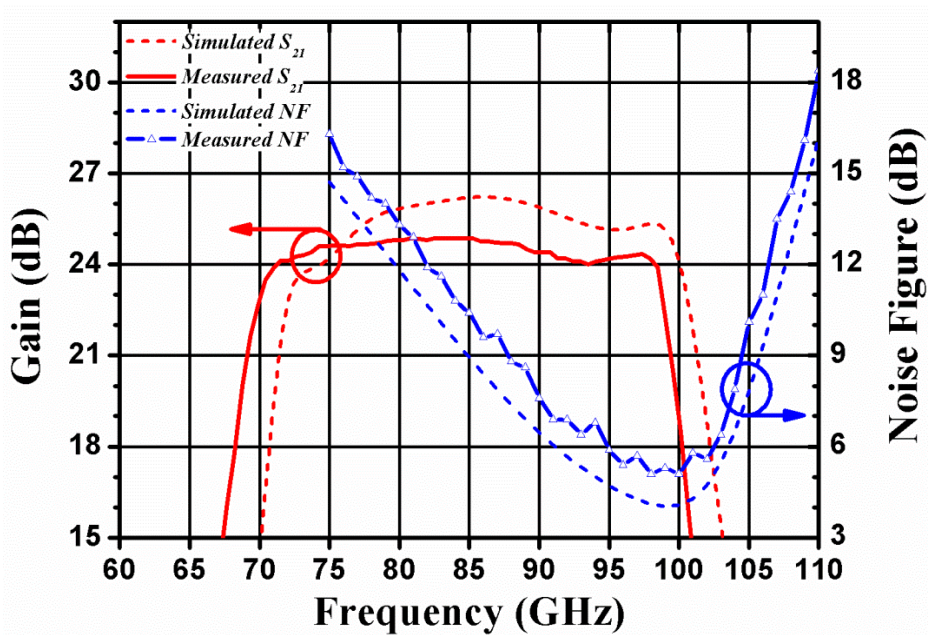


Figure 7.14 Simulated (dashed line) and measured (solid line) results of the transducer gain and noise figure.

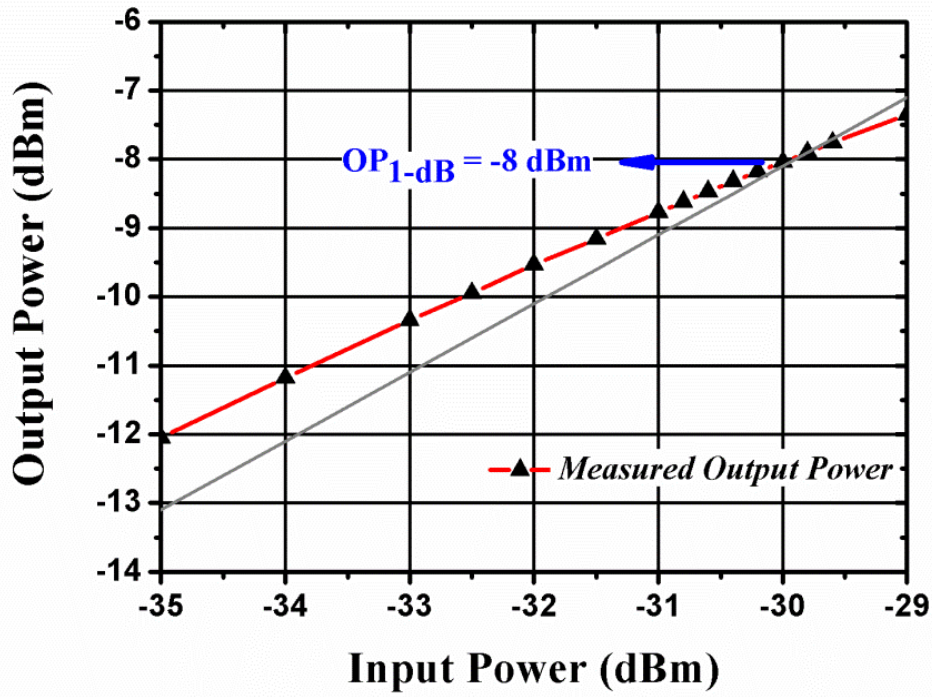


Figure 7.15 Measured output power versus input power.

**Table 7.2 Performance Comparison of Millimeter-Wave LNAs**

Ref.	-3-dB BW (GHz)	Noise Figure (dB)	Peak Gain (dB)	OP <sub>1dB</sub> (dBm)	Technology
[85]	70—92	9 @ 86 GHz	19	N/A	180 nm SiGe
[49]	77—101	6 @ 92 GHz	45	0.2	90 nm SiGe
[92]	75—105	5.1 @ 90 GHz	19	-3	90 nm SiGe
[93]	75—110	3.5 @ 95 GHz	34	12	90 nm SiGe
[94]	75—81	9 @ 79 GHz	12	-10	65 nm CMOS
[91]	82—103	7.5 @ 100 GHz	13	10	65 nm CMOS
[55]	72—92	6.4 @ 84 GHz	15	-1.6	65 nm CMOS
[95]	81—92	7 @ 90 GHz	15	N/A	65 nm CMOS
[7]	83—93	6.8 @ 81 GHz	27	N/A	65 nm CMOS
<b>This work</b>	69—99	5.1 @ 98 GHz	25	-8	65 nm CMOS

## 7.4 Summary

A millimeter-wave LNA implemented in a 65-nm CMOS technology was presented in this chapter. Gain-enhancement techniques, aiming at improving the noise figure and bandwidth, have been discussed and employed. Some misconceptions that constrain the practical usage of the gain-enhancement have been clarified by theoretical analysis. As a result, of being granted full play in

terms of gain-boosting, the LNA has demonstrated comparable performance to those implemented in other advanced technologies. Additionally, the noise figure is the lowest, compared to hitherto known results of the millimeter-wave CMOS LNAs. To sum up, based on the performance, it is possible to implement low cost bolometer-arrays in a CMOS technology, with which comparable performance to state-of-the-art bolometer-arrays can be achieved.

## Chapter 8

# A CMOS W-band $4\times$ Quasi-Subharmonic Mixer

So far, this thesis has introduced techniques for designing the narrow- and wideband millimeter-wave LNAs. As in a front-end, millimeter waves will finally be translated to lower frequencies by another important component, i.e. the mixer. This chapter presents a  $4\times$  W-band quasi-subharmonic down-conversion mixer in a 65 nm CMOS technology. Developed from subharmonic mixers, this mixer saves trouble in designing phase-shifters and works well within W-band. Down-conversion is accomplished by capturing the phase difference between two sine waves at every half cycle of the LO rate. The mixer presents a satisfactory performance. The power gain is above 3.5 dB over the entire W-band. The minimum noise figure is 12.5 dB, and the 1-dB compression point is -1.2 dBm.

### 8.1 Introduction

At this point, there should be no doubt that the millimeter-wave systems would prevail in our daily life. As mentioned earlier, millimeter-wave radiometers can be used for many application fields, but unlike X-ray scanners, they pose no risk of harm to humans [95]. Communication systems are also expanding their frontiers to the millimeter-wave range, as evidenced by IEEE 802.15.3c, IEEE

802.11ad and the impending 5G cellular networks [4] [96]. As is well known, the receiver plays an important role. It demodulates the received millimeter-wave frequency to a lower frequency,  $\Delta\omega$ , by using a mixer driven by an LO. In practice, however, as described in Chapter 2 and 3, it is difficult to build an LO at the extremes of frequency, especially for CMOS technologies. To address such an issue, a subharmonic mixer could be used in lieu of conventional mixers. Compared with conventional mixers driven at an LO frequency,  $\omega_{LO}$ , the subharmonic mixer only needs one-half or even less of that LO frequency. [37] explains the working principle of a conventional  $4\times$  CMOS subharmonic mixer. The mixer in [37] is driven by LO signals with quadrature-phases. The quadrature-phases are generated by phase-shifters. However, the phase-shifter, typically a coupler, becomes a new burden for designers, because it occupies a large chip area and requires many EM simulation iterations [44] [97]. Another issue associated with some subharmonic mixers is their low conversion gain [51], [98], [99] because the enhanced amplitudes of higher harmonics are normally smaller than the fundamental's. The subsampling mixer [26] could be used to relax the requirement on the LO side as well. Its scheme is based on the observation that the information bandwidth of modulation is necessarily lower than the carrier frequency. One may satisfy the Nyquist criterion with a sampling rate that is lower than the carrier frequency to down-convert the input signal. However, a train of impulses is created in the frequency domain as well, which simultaneously folds the noise at the multiples of the sampling rate into the

baseband during the sampling process.

This chapter presents a design of a W-band  $4\times$  CMOS quasi-subharmonic mixer. The design method is based on the general description for subharmonic mixers. The topology and LO driving signals are similar to conventional ones. However, the down-conversion process is completed by trimming the input signal rather than by superposing or pumping the higher order of harmonics, wherein lies the reason for the prefix, “quasi-”. Section 8.2 describes the design method. Section 8.3 exhibits the experimental results. A summary is drawn in Section 8.3.

## 8.2 Circuit Design

As described in Chapter 3, the core of a mixer is to realize a multiplication between two frequency components. From a mathematical view, a  $4\times$  subharmonic mixer could be described as:

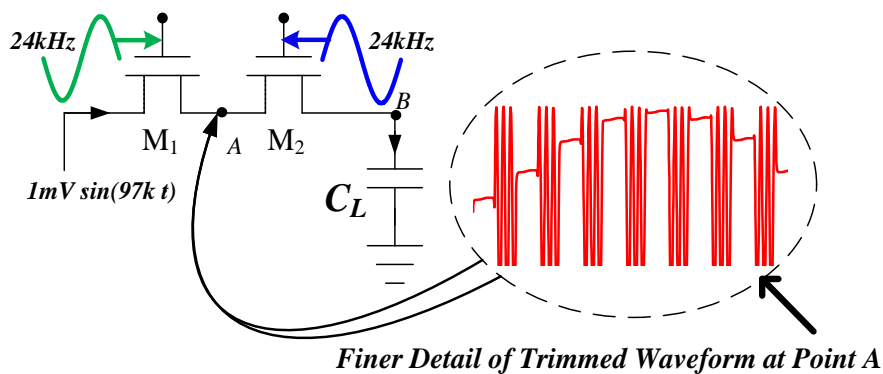
$$v_{out} = A_{out} \sin[(\omega_{in} - 4 \cdot \omega_{LO}) \cdot t] = A_{out} \sin(\Delta\omega \cdot t), \quad (8.1)$$

where  $v_{out}$  is the output voltage, and  $A_{out}$  is its amplitude. Similarly, the input voltage can be expressed as:

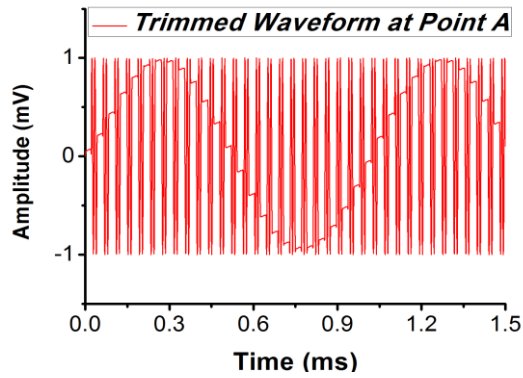
$$v_{in} = A_{in} \sin\left(4 \cdot \frac{2\pi}{T_{LO}} \cdot t + \Delta\omega \cdot t\right), \quad (8.2)$$

where  $T_{LO}$  is the time-period of the LO rate. Equation (8.2) carries useful information, from which the design inspiration is derived.

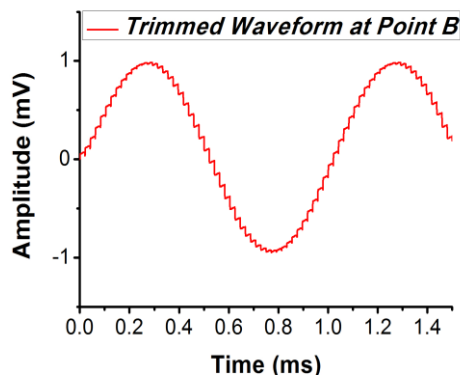
Assuming that  $A_{in}$  is a constant, the value of  $v_{in}$  at each time  $t$  is determined by its phase change. The phase change is due to two parts, i.e.  $4 \cdot \frac{2\pi}{T_{LO}} \cdot t$  and  $\Delta\omega \cdot t$ . Interestingly, once  $t$  is a multiple of  $\frac{T_{LO}}{2}$ , the value of  $v_{in}$  is only decided by the latter part, because  $4 \cdot \frac{2\pi}{T_{LO}} \cdot t$ , at that time, is just a multiple of  $2\pi$ . In other words, the value of  $v_{in}$  is modulated by  $\sin(\Delta\omega \cdot t)$  at every half LO-cycle. Therefore, if  $v_{in}$  can be properly trimmed, a loss-less mixer becomes possible by tracking the values of  $v_{in}$  at the moment when  $t$  is a multiple of  $\frac{T_{LO}}{2}$ . A circuit consisting of two NMOS transistors in tandem could meet such an expectation. For the sake of developing an intuitive feel, a specific example from the simulation is given in Fig. 8.1.



(a)



(b)

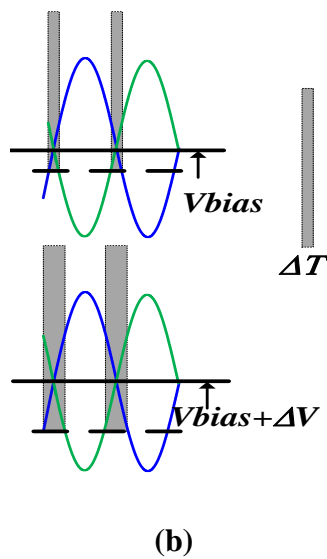
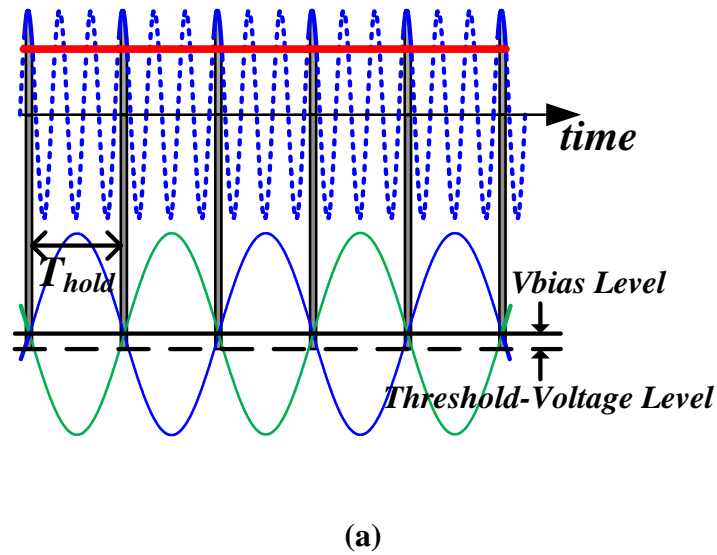


(c)

**Figure 8.1 (a) The schematic of the tandem-switch, (b) detailed waveforms at point A and (c) at point B.**

In the particular case shown in Fig. 8.1, the tandem-switch trims a 1-mV sinusoid alternately, which yields a 1-mV demodulated-sinusoid at the output. Its working principle can be analyzed as follows. As shown in Fig. 8.2(a), the differential LO applied to each gate creates a time-interval,  $\Delta T$ .  $\Delta T$  repeats itself by every half LO-cycle. Within  $\Delta T$ , both switches are “on”. The current can charge the capacitor. Outside  $\Delta T$ , the current stops charging, because at least one of the switches is turned off. The capacitor will hold the stored charge for a

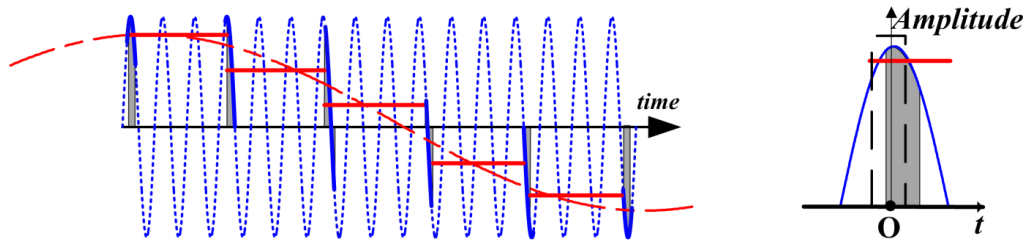
period of  $T_{hold}$ . The  $T_{hold}$  and  $\Delta T$  depend on the bias voltage,  $V_{bias}$ . As shown in Fig. 8.2(b), a high bias voltage reduces  $T_{hold}$  but increases  $\Delta T$ .



**Figure 8.2 (a) The snapshot captured when  $\omega_{in}$  is a multiple of  $\omega_{LO}$ , and (b) details on LO.**

If the frequency of  $\omega_{in}$  is a multiple of  $\omega_{LO}$ , charges stored by the capacitor remain the same. The voltage on the capacitor is the area of the shadowed region

divided by  $\Delta T$ , as represented in Fig. 8.2(a) by a straight line in red. When  $\omega_{in}$  is no longer a multiple of  $\omega_{LO}$ , the charge stored by the capacitor starts to vary in a sinusoidal form, as shown in Fig. 8.3.



**Figure 8.3 Time domain waveforms used to explain the output waveform.**

An intuitive way to think about this is as follows. Imagine that one is at point B in Fig. 8.1 and starts to record the values of  $v_{in}$ , which are on the other side of the tandem-switch. The value change of  $v_{in}$  can be monitored only at every half LO-cycle, when both switches are turned on. Otherwise, nothing could be recorded, since at least one switch is placed in the “off” state, which cuts off the path from the input to the output. Therefore, referring to (8.2), the recorded points belong to  $\sin(\Delta\omega \cdot t)$  only. The principle can be analyzed in the frequency domain as well. The repeating pattern of  $\Delta T$  is similar to a Dirac comb [100]. The Fourier transform of ditto is also a Dirac comb, spaced at intervals of  $\frac{2}{T_{LO}}$  in the frequency domain. The down-conversion process is accomplished by utilizing its second harmonic component at the frequency of  $4\omega_{LO}$ . At this point, it is worth noting that the proposed scheme differs from a subsampling mixer in

the following ways.

Fig. 8.3 helps with estimating the amplitude of the demodulated signal,  $A_{out}$ . Neglecting the frequency-offset and assuming that the center of  $\Delta T$  is at the origin, one can have,

$$A_{out} \approx \frac{\int_{-\frac{\Delta T}{2}}^{\frac{\Delta T}{2}} A_{in} \sin(\omega_{in} \cdot t + \frac{\pi}{2}) dt}{\Delta T} = \frac{\int_{-\frac{\Delta T}{2}}^{\frac{\Delta T}{2}} A_{in} \sin(\frac{2\pi}{T_{in}} t + \frac{\pi}{2}) dt}{\Delta T}, \quad (8.3)$$

where  $T_{in}$  is the time-period of the input. Fig. 8.4 plots (8.3) as a function of  $\Delta T/T_{in}$ . As one may notice, in the extreme cases where  $\Delta T$  is just a few instants of  $T_{in}$ , there is almost no difference between  $A_{out}$  and  $A_{in}$ . However, synchronization suffers at the same time.

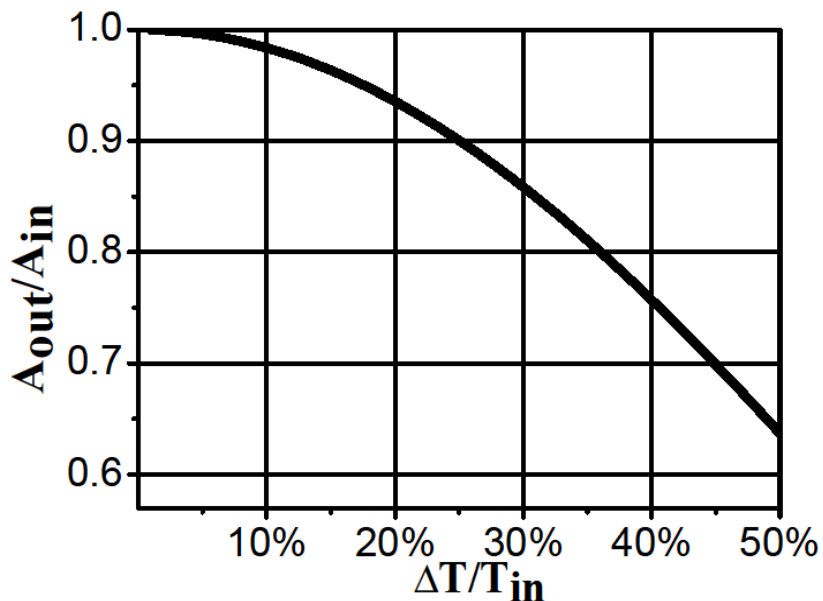
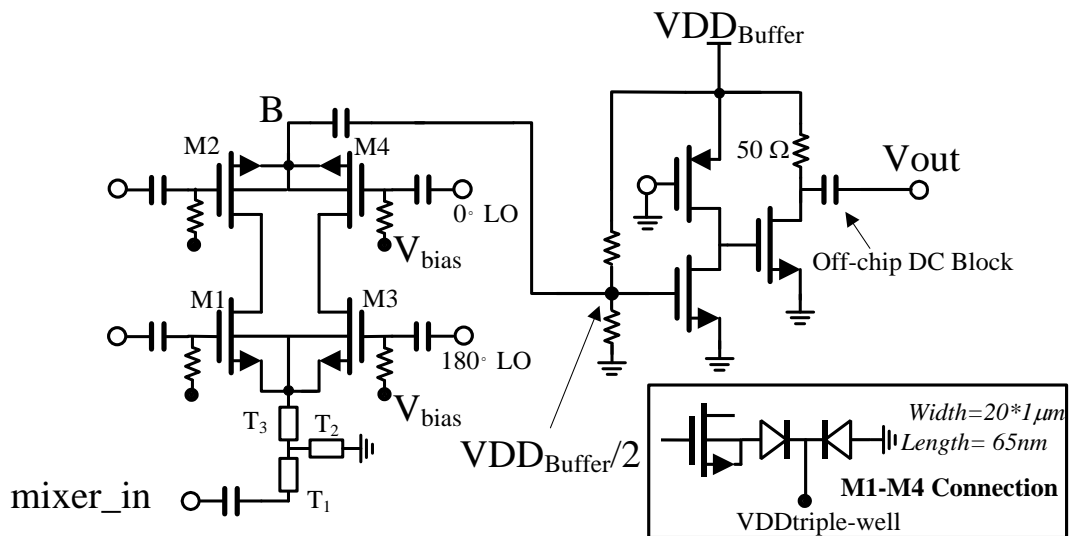


Figure 8.4 The plot of  $A_{out}/A_{in}$  versus  $\Delta T/T_{in}$ .

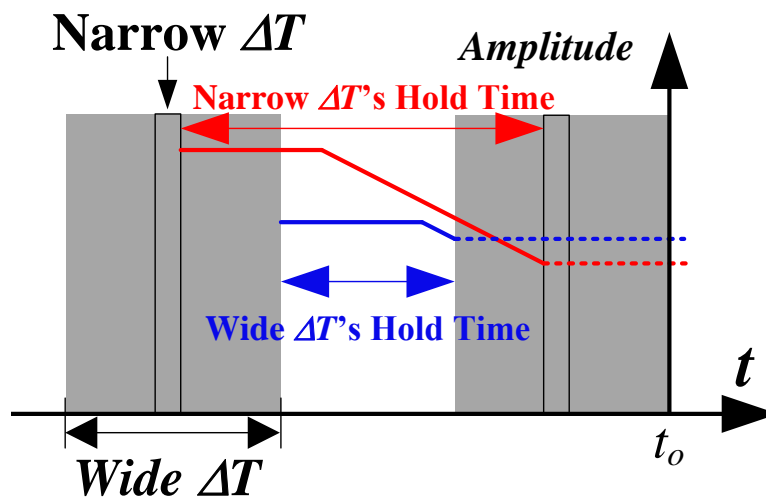
Fig. 8.5 shows the schematic of the proposed mixer. A balanced topology is adopted in order to cancel the leakage current from LO at point B in Fig. 8.5. To relieve the issue of unequal threshold-voltages caused by body-effect, triple-well transistors are used. Conductance for a  $20 \times 1 \mu\text{m}$ -gate-width is about 1/20-Siemens. An IF amplifier, also used as a buffer, matches the output to  $50 \Omega$ . Its -3-dB bandwidth is from DC to 12 GHz. A PMOS transistor is used here, mainly because as mentioned in Chapter 3, it suffers less from the  $1/f$  noise issues. The AC gain-level falls below 10 dB thereafter. The LO power is chosen to be 10 dBm.



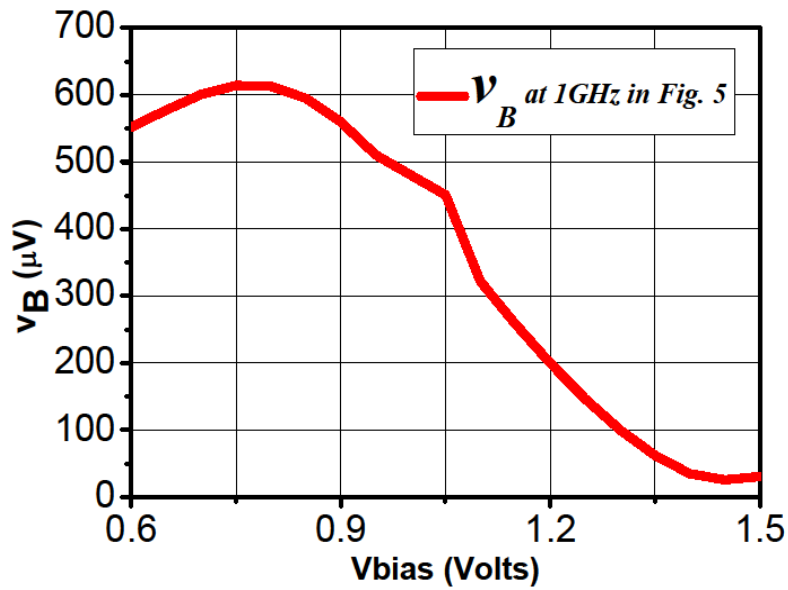
**Figure 8.5 The schematic of the proposed  $4 \times$  quasi-subharmonic mixer.**

The values of  $\Delta T$  and  $T_{hold}$  are controlled by the bias condition. As mentioned earlier, a small  $\Delta T$  yields a high average value. Additionally,  $T_{hold}$

also has effects on gain. Practically, the capacitor can only hold the charge for a limited duration, since the amount of stored charges would decrease exponentially within  $T_{hold}$ . As sketched in Fig. 8.6(a), a small  $\Delta T$  averages a high value for (8.3) but increases  $T_{hold}$ , aiding the leakage. A large  $\Delta T$  reduces  $T_{hold}$  but lowers the average value of (8.3). An optimized point for biasing thereby exists. As can be seen from Fig. 8.6(b), referring to the circuit in Fig. 8.5, when  $V_{bias}$  is 750 mV, for a 1 mV, 97 GHz input at the input node “mixer\_in”,  $v_B$  at 1 GHz is 615  $\mu$ V. In other words, the loss from point B to the input node “mixer\_in” is 4.2 dB.



(a)

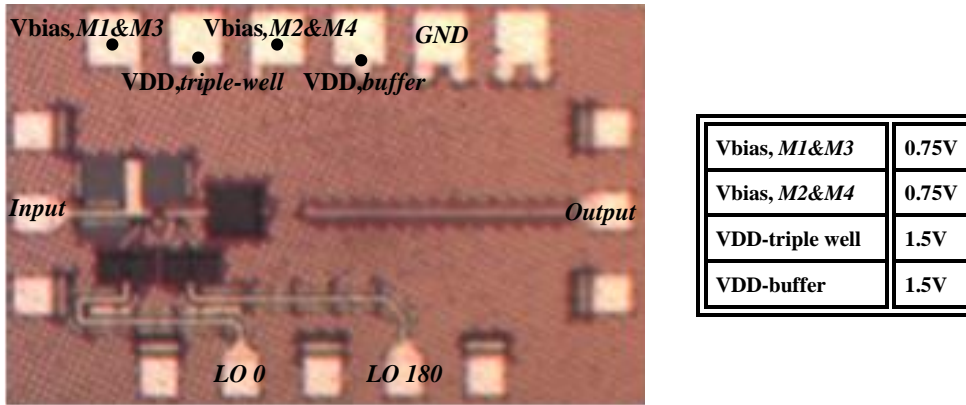


(b)

Figure 8.6 (a)  $\Delta T$  and  $T_{hold}$  effects on gain, and (b) the plot of  $V_{bias}$  versus  $v_B$ -at-1-GHz.

### 8.3 Measurement Results

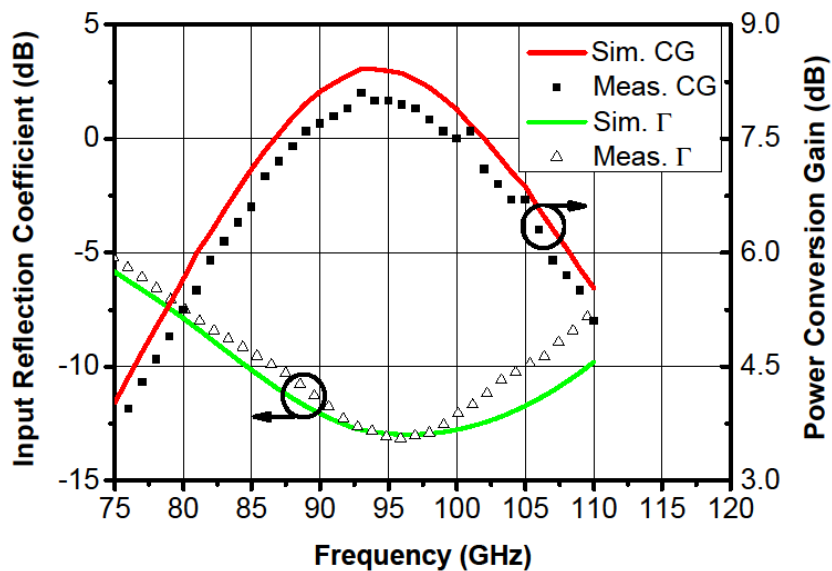
Fig. 8.7 shows the die photo of the proposed mixer using the GlobalFoundries 65-nm CMOS technology. The area including the pads is  $0.78 \times 0.48 \text{ mm}^2$ . The W-band signal fed into the mixer comes from an R&S SMF100A signal generator. It is connected by a 6x frequency multiplier and an attenuator. An R&S ZVA67 network analyzer is used to generate the differential LO drive. The noise source is an ELVA ISSN-10, which covers the entire W-band. The passive mixer consumes a DC-power of 17 mW to drive the buffer stage.



**Figure 8.7** The die photo of the proposed mixer and its corresponding DC bias.

The measured results agree well with the simulated. As shown in Fig. 8.8, the mixer can operate over a wide frequency range. The -3-dB bandwidth is from 79 GHz to 110 GHz. The mixer keeps its gain-level above 3.75 dB over the entire W-band. The peak gain is 8.1 dB at 93 GHz. Its noise performance is satisfactory as well. As shown in Fig. 8.9, the minimum double-sideband (DSB) noise figure (NF) is 12.5 dB at IF=2 GHz. Noise could be further suppressed, if a gain stage is applied at the input [35]. Fig. 8.9 also plots the effect of the frequency offset when it is applied to the mixer. In reality, a fading channel or an LO mismatch between the transmitter and the receiver may cause such a problem. To evaluate this effect, the LO frequency is fixed at 24 GHz, and the input frequency is swept from 97 GHz to 110 GHz. As plotted in Fig. 8.9, the gain of the mixer stays above 0 dB when the frequency offset is increased to 5.5 GHz. The measured output power-compression-point ( $OP_{1dB}$ ) is -1.2 dBm when the input frequency is 97 GHz, as shown in Fig. 8.10. The measured LO-to-RF/LO-to-IF/RF-to-IF isolations are 55/63/34 dB when the frequency of LO/RF is 24/97 GHz. The

proposed mixer is not intended to strengthen the fourth harmonic at the LO-port. Moreover, its passive nature suppresses the current-growth at the frequency of 2LO or 4LO. Therefore, 2LO-RF and 4LO-RF are not considered as measures to judge the mixer performance. Taken as a supplement, the measured power, at 48 GHz (2LO) and 96 GHz (4LO), at the RF-port, is -31 dBm and -53 dBm, respectively. Table 8.1 summarizes and compares the designed mixer's performance with other CMOS mixers in W-band. As summarized in Table 8.1, compared to other mixers, the proposed mixer demonstrates a balanced performance, and there is no obvious disadvantages. Moreover, this type of mixer saves trouble in designing the phase-shifters.



**Figure 8.8 Measured power conversion gain (CG) and the input reflection coefficient ( $\Gamma$ ) versus RF frequency with LO power set to 10 dBm.**

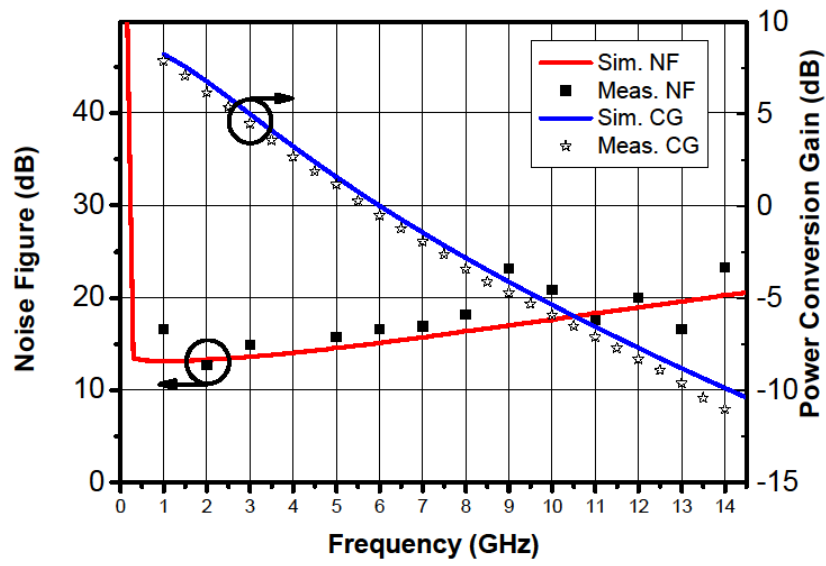


Figure 8.9 Measured NF (DSB), CG versus the frequency offset.

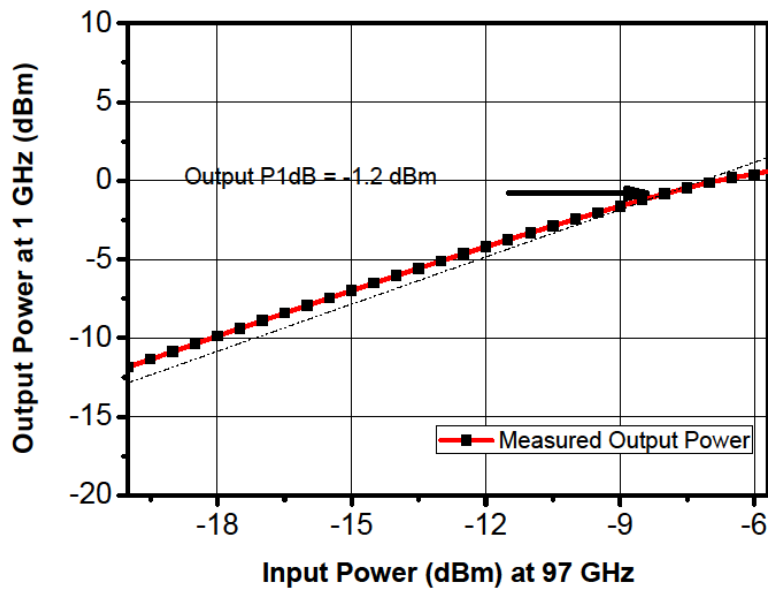


Figure 8.10 Measured  $P_{1dB}$ , with LO power set to 10dBm.

**Table 8.1 Performance Comparison of W-band Mixers**

<b>Ref.</b>	<b>Process</b>	<b>Freq. (GHz)</b>	<b>Gain (dB)</b>	<b>NF (dB)</b>	<b>OP<sub>1dB</sub> (dBm)</b>	<b>Power (mW)</b>
[44]	CMOS 65 nm	5-75	>3	14.6	N/A	3
[55]	CMOS 65 nm	74-98	6	8	-16.5	N/A
[101]	CMOS 90 nm	40-108	-1.5	11	-14.5	2
[102]	CMOS 90 nm	35-83	0.5	N/A	-0.5	6.5
<b>This work</b>	CMOS 65 nm	79-110	8	12.5	-1.2	17

## 8.4 Summary

A W-band mixer in a CMOS 65 nm technology has been presented. It is of low loss, high linearity, and has a moderate noise figure. The principle is simple and straightforward, and it saves trouble in designing the phase-shifters. Moreover, by expanding the proposed method, it is possible to design a subharmonic mixer of higher orders, which could be a potential solution for down-converting Terahertz frequencies.

# Chapter 9

## Conclusions and Future Work

### 9.1 Conclusions

This thesis has covered topics on: (1) noise analysis based on a two-port network; (2) circuit designs of active CMOS components in the millimeter-wave front-ends; (3) methods to miniaturize bulky CMOS elements.

Chapter 1 and 2 have introduced the motivation and outlined the scope of this work. Design specifications are provided in Chapter 1.

Chapter 3 has provided fundamentals with respects to individual component designs. Configurations of LNAs and mixers have been carefully reviewed. Noise behaviors have been extensively studied.

Chapter 4 expands the classical two-port noise theory, to make it be more practical. Formulas that describe the feedback effect on noise performance have been derived in a simple and straightforward way. The formulas are believed to be useful when one needs to design an input matching network or estimate the effect of parasitic components at input.

Chapter 5 starts the circuit design. A method for designing a narrow-band millimeter-wave LNA has been proposed. It employs the noise matching technique described in Chapter 3 and 4. The LNA achieves a noise figure of 8.1 dB at 77 GHz and a voltage gain of 33 dB at 77 GHz. The power consumption is kept below 10 mW for both bands' function. Although the results meet the

specification set in Chapter 2, the noise matching technique has not significantly improved the overall noise performance. This may be due to two reasons. Firstly, for the noise matching technique, empirically, at high frequencies, it improves the noise figure by an order of 0.5 dB to 1 dB [26]. Secondly, according to Chapter 3.5, the input transistor of an LNA has the most impact on the overall noise figure. The proposed LNA in this Chapter has not optimized the gain at the first stage. Therefore, when designing LNAs used for passive imaging, additional refinement work is needed.

Chapter 6 has presented a dual-band lumped Wilkinson power divider. Its working principle is inspired by the work done in Chapter 5. Simulated results show that the return loss at each port has been kept above 15 dB. The insertion loss is kept below 1.5 dB. The divider can save a large chip area and the design method could be potentially applied to higher-order-mode designs. The proposed design demonstrate that passive elements implemented in a CMOS technology could also have sound performance.

Chapter 7 has presented a wideband millimeter-wave CMOS LNA for applications on 94 GHz passive imaging. Based on the design experience gained in Chapter 6, in order to optimize the noise performance, gain-enhancement has been properly introduced. The proposed circuit yields satisfactory performance. The peak gain is 25 dB along with a noise figure of 5.1 dB. The presented LNA thus is suitable for the millimeter-wave application at 94 GHz.

Chapter 8 has presented a millimeter-wave CMOS mixer. Developed from

subharmonic mixers, this mixer saves trouble in designing phase-shifters and works well within W-band. Down-conversion is achieved by capturing the phase difference between two sine waves at every half cycle of the LO rate. The power gain is above 3.5 dB over the entire W-band. The minimum noise figure is 12.5 dB, and the 1-dB compression point is -1.2 dBm. The operating frequency range of the mixer has covered two important millimeter-wave applications. Additionally, the proposed method could be potentially expanded to Terahertz range.

## **9.2 Future Work**

Previous refinement works have showed that, once properly refined, the millimeter-wave CMOS circuit would demonstrate satisfactory performance. The following merits of CMOS circuits at the millimeter-wave frequency range can be found. Firstly, because of the continuous efforts in scaling down the feature size of MOS transistors, once properly designed, the CMOS LNA can also provide acceptable gain at the millimeter-wave frequency range. Secondly, compared to BJT LNAs, the proposed dual-band LNA does not depend on a constant biasing current. Thus, it significantly reduces the power consumption, which can greatly benefit the commercial applications. Thirdly, even though the substrate loss associated with CMOS technologies may potentially limit the performance of passive elements, there are still remedies to overcome such an issue. For example, in the proposed CMOS Wilkinson power divider, in order to

reduce the substrate loss, the inductors and the ground plane have been thickened. As a result, the proposed Wilkinson power divider has a power loss of only 1.5 dB at the extremes of frequencies. Fifthly, if the power consumption is not one's primary concern, by increasing the power consumption and by gain-enhancement techniques, CMOS LNAs can achieve comparable performance compared to other advanced technologies. Sixthly, an NMOS transistor can be naturally regarded as a switch. Therefore, such a characteristic can be exploited for the mixer design. Compared to BJT mixers, CMOS mixers normally consume less power while still can yield high performance, as demonstrated by the proposed mixer. Therefore, because of these merits, expectation for higher performance arises. This section suggests some topics for future work.

Firstly, for the dual-band LNA in Chapter 5, following refinement work can be considered. The LNA possesses a noise figure of 8 dB, which leaves a lot to be desired. As discussed in Chapter 8, subsequent stages would contribute significant noise if the first stage lacks sufficient gain. Therefore, gain-enhancement can be applied to the first stage. The layout of the multi-interdigital-gate transistor proposed in Chapter 2 could also deteriorate the noise performance. As can be noticed from Fig. 2.4(a), contacts and vias at each gate terminal are combined in series. Consequently, compared to double-gate transistors, this type of layout leads to a higher noise figure. Therefore, other configurations can be considered for future designs [103] [104].

Secondly, for the wideband LNA presented in Chapter 8, there still leaves some

room for improvement. The power consumption can be optimized. Although the power consumption is in trade-off with other performance, high consumption can cause heat radiation issues. To meliorate such issues, the number of stages can be reduced. Methods for broadband amplifier designs should be future investigated for future work [105] [106].

Thirdly, for the mixer presented in Chapter 9, its IF bandwidth can be improved. One possible way is to place an inductor at the output of the mixer core. Note that the inductor may increase the noise figure. Therefore, a gain stage can be placed in front of the mixer core, to make the mixer become a low-noise mixer.

Finally, the LNA presented in Chapter 8 and the mixer presented Chapter 9 shall be combined together as a fully integrated radiometry receiver. Regarding this type of receiver, Dicke switch is usually an indispensable part, which is used to alleviate the gain fluctuation issue. [85] and [107] have proposed a method, where Dicke switch is embedded in a balanced LNA topology using phase shifters. This method greatly improves sensitivity and worth the effort for a further study. As evidenced in Chapter 6, the CMOS passive component can achieve a low insertion power loss. In the future work, it is possible to implement a Dicke switch with an insertion loss less than 1.5 dB at 94 GHz.

To sum up, the millimeter-wave application benefits people life from many aspects. At the same time, it also brings in its own challenges. However, as it goes that, there is always a way out. There are always more solutions than difficulties. With the efforts in continuously refining CMOS circuits and

continuously improvement on CMOS technologies [108] [109], there is no doubt that the future for the millimeter-wave CMOS IC is bright.

## Reference

- [1] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–154, 2005.
- [2] L. Yujiri, M. Shoucri, and P. Moffa, "Passive millimeter wave imaging," *Microw. Mag. IEEE*, vol. 4, no. 3, pp. 39–50, 2003.
- [3] B. Razavi, "Design of millimeter-wave CMOS radios: A tutorial," *Circuits Syst. I Regul. Pap. IEEE Trans.*, vol. 56, no. 1, pp. 4–16, 2009.
- [4] T. S. Rappaport, R. Mayzus, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi, and F. Gutierrez, "Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!," *IEEE Access*, vol. 1, pp. 335–349, 2013.
- [5] W. D. Jones, "Keeping cars from crashing," *IEEE Spectr.*, vol. 38, no. 9, pp. 40–45, 2001.
- [6] R. Appleby and R. N. Anderton, "Millimeter-wave and submillimeter-wave imaging for security and surveillance," *Proc. IEEE*, vol. 95, no. 8, pp. 1683–1690, 2007.
- [7] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981–1991, 2010.
- [8] T. A. Milligan, *Modern Antenna Design*, 2nd ed. Wiley-IEEE Press, 2005.
- [9] M. Varonen, M. Kärkkäinen, M. Kantanen, and K. A. I. Halonen, "Millimeter-wave integrated circuits in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1991–2002, 2008.
- [10] K. H. K. Yau, M. Khanpour, M. T. Yang, P. Schvan, and S. P. Voinigescu, "On-die source-pull for the characterization of the W-band noise performance of 65 nm General Purpose (GP) and Low Power (LP) n-MOSFETs," in *IEEE Microwave Symposium Digest*, 2009, pp. 773–776.
- [11] B. Razavi, "A millimeter-wave circuit technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2090–2098, 2008.

- [12] B. Razavi, *RF Microelectronics*, 2nd ed. Prentice Hall, 2011.
- [13] E. A. Firouzaei, *PhD thesis: mm-Wave Phase Shifters and Switches*, University of California at Berkeley, 2010.
- [14] J. Lee, Y. A. Li, M. H. Hung, and S. J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, 2010.
- [15] J. A. Nanzer and R. L. Rogers, "Human presence detection using millimeter-wave radiometry," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2727–2733, 2007.
- [16] J. W. May and G. M. Rebeiz, "Design and characterization of W-band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1420–1430, 2010.
- [17] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Wiley-IEEE Press, 2010.
- [18] S. T. Nicolson, K. H. K. Yau, S. Pruvost, V. Danelon, P. Chevalier, P. Garcia, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A low-voltage SiGe BiCMOS 77-GHz automotive radar chipset," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1092–1104, 2008.
- [19] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22-29-GHz/77-81-GHz BiCMOS transceiver for automotive radars," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, 2009.
- [20] R. H. Dicke, "The measurement of thermal radiation at microwave frequencies," *Rev. Sci. Instrum.*, vol. 17, no. 7, pp. 268–275, 1946.
- [21] A. Sedra and K. Smith, *Microelectronic Circuits*, 7th ed. Oxford University Press, 2014.
- [22] T. H. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits*. Cambridge University Press, 2004.
- [23] J. H. Tsai, H. Y. Yang, T. W. Huang, and H. Wang, "A 30-100 GHz wideband sub-harmonic active mixer in 90 nm CMOS technology," *IEEE Microw. Wirel. Components Lett.*, vol. 18, pp. 554–556, 2008.
- [24] V. der Ziel, *Noise in Solid State Devices and Circuits*, 1st ed. Wiley, 1986.

- [25] A. van der Ziel, "Thermal Noise in Field-Effect Transistors," *Proc. IRE*, vol. 50, no. 8, pp. 1808–1812, 1962.
- [26] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge University Press, 2003.
- [27] J. A. Dobrowolski, *Microwave Network Design Using the Scattering Matrix*. Artech House, 2010.
- [28] J. Y. C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2- $\mu\text{m}$  CMOS RF amplifier," *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 246–248, 1993.
- [29] R. Benton, M. Nijjar, C. Woo, A. Podell, G. Horvath, E. Wilson, and S. Mitchell, "GaAs MMICs for an integrated GPS front-end," in *IEEE 14th Gallium Arsenide Integrated Circuit Symposium Technical Digest*, 1992, pp. 123–126.
- [30] N. H. Sheng, W. J. Ho, N. L. Wang, R. L. Pierson, P. M. Asbeck, and W. L. Edwards, "A 30 GHz bandwidth AlGaAs-GaAs HBT direct-coupled feedback amplifier," *IEEE Microw. Guid. Wave Lett.*, vol. 1, no. 8, pp. 208–210, 1991.
- [31] J.-H. C. Zhan and S. S. Taylor, "A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," in *IEEE Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, 2006, pp. 721–730.
- [32] A. Rofougaran, J. Y. C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 880–889, 1996.
- [33] K. W. Kobayashi and A. K. Oki, "Low-noise baseband 5-GHz direct-coupled HBT amplifier with common-base active input match," *IEEE Microw. Guid. Wave Lett.*, vol. 4, no. 11, pp. 373–375, 1994.
- [34] X. Li, S. Shekhar, and D. J. Allstot, "Gm-booster common-gate LNA and differential Colpitts VCO/QVCO in 0.18- $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2618, 2005.
- [35] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, 1997.
- [36] D. Soo and R. Meyer, "A four-quadrant NMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. 17, no. 6, pp. 1174–1178, 1982.

- [37] B. R. Jackson and C. E. Saavedra, "A CMOS Ku-band 4x subharmonic mixer," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1351–1359, 2008.
- [38] B. Razavi, "A 60GHz direct-conversion CMOS receiver," in *IEEE Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, 2005, pp. 400–402.
- [39] T. Yao, M. Gordon, K. Yau, M. T. Yang, and S. P. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006, pp. 1–4.
- [40] S. T. Nicolson, a. Tomkins, K. W. Tang, a. Cathelin, D. Belot, and S. P. Voinigescu, "A 1.2V, 140GHz receiver with on-die antenna in 65nm CMOS," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2008, pp. 229–232..
- [41] N. Zhang, H. Xu, H. T. Wu, and K. O. Kenneth, "W-band active down-conversion mixer in bulk CMOS," *IEEE Microw. Wirel. Components Lett.*, vol. 19, no. 2, pp. 98–100, 2009.
- [42] S. Raman, F. Rucky, and G. M. Rebeiz, "A high-performance w-band uniplanar subharmonic mixer," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 6, pp. 955–962, 1997.
- [43] M. Bao, H. Jacobsson, L. Aspemyr, G. Carchon, and X. Sun, "A 9-31-GHz subharmonic passive mixer in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2257–2263, 2006.
- [44] F. Zhang, B. Yang, and E. Skafidas, "A low-power 5-75-GHz common-gate subharmonic mixer in 65-nm CMOS," in *2011 IEEE 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Digest of Papers*, 2011, pp. 133–136.
- [45] Y.-S. Lin, G.-L. Lee, and C.-C. Wang, "Low-power 77–81 GHz CMOS LNA with excellent matching for automotive radars," *Electron. Lett.*, vol. 50, no. 3, pp. 207–209, Jan. 2014.
- [46] M. Parlak and J. F. Buckwalter, "A 2.9-dB noise figure, Q-band millimeter-wave CMOS SOI LNA," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2011, pp. 1–4.
- [47] D. Pepe and D. Zito, "32 dB Gain 28 nm Bulk CMOS W-Band LNA," *IEEE Microw. Wirel. Components Lett.*, vol. 25, no. 1, pp. 55–57, Jan. 2015.

- [48] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, 2010.
- [49] X. et al. Bi, "A 19.2 mW, > 45 dB gain and high-selectivity 94 GHz LNA in 0.13 um SiGe BiCMOS," *IEEE Microw. Wirel. Comp. Lett.*, vol. 23, no. 5, pp. 261–263, 2013.
- [50] C. C. Boon, S. Member, X. Yi, and G. S. Member, "A 10–67 GHz 1.44 mW 20.7 dB Gain VGA-Embedded Downconversion Mixer With 40 dB Variable Gain Range," *IEEE Microw. Wirel. Components Lett.*, vol. 24, no. 7, pp. 466–468, 2014.
- [51] Y. J. Hwang, H. Wang, and T. H. Chu, "A W-band subharmonically pumped monolithic GaAs-based HEMT gate mixer," *IEEE Microw. Wirel. Components Lett.*, vol. 14, no. 7, pp. 313–315, 2004.
- [52] W. Perndl, H. Knapp, M. Wurzer, K. Aufinger, T. F. Meister, T. F. Bock, W. Simburger, and A. L. Scholtz, "A low-noise, and high-gain double-balanced mixer for 77 GHz automotive radar front-ends in SiGe bipolar technology," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2004, pp. 47–50.
- [53] J. J. Hung, T. M. Hancock, and G. M. Rebeiz, "A 77 GHz SiGe sub-harmonic balanced mixer," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2167–2173, Nov. 2005.
- [54] J. H. Tsai, P. S. Wu, C. S. Lin, T. W. Huang, J. G. J. Chern, and W. C. Huang, "A 25-75 GHz broadband Gilbert-cell mixer using 90-nm CMOS technology," *IEEE Microw. Wirel. Components Lett.*, vol. 17, no. 4, pp. 247–249, 2007.
- [55] M. Khanpour, K. W. Tang, P. Garcia, and S. P. Voinigescu, "A wideband W-band receiver front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717–1730, 2008.
- [56] A. Allam, *PhD Thesis: Noise and quadrature signal generation problems in CMOS Radio Frequency*. University of Alberta, 2008.
- [57] S. Iversen, "The effect of feedback on noise figure," *Proc. IEEE*, vol. 63, no. 3, pp. 540–542, 1975.
- [58] P. Gray, *Analysis and Design of Analog Integrated Circuits*. Wiley Press, 2001.

- [59] D. Saunders, S. Bingham, G. Menon, D. Crockett, J. Tor, R. Mende, M. Behrens, N. Jain, A. Alexanian, and Rajanish, "A single-chip 24 GHz SiGe BiCMOS transceiver for FMCW automotive radars," in *IEEE Radio Frequency Integrated Circuits(RFIC) Symposium*, 2009, pp. 459–462.
- [60] S. T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A 77-79-GHz Doppler Radar Transceiver in Silicon," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2007, pp. 1–4.
- [61] G. Matthaei, E. M. T. Jones, and L. Young, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*. Artech House, 1980.
- [62] H. H. Hsieh, P. Y. Wu, C. P. Jou, F. L. Hsueh, and G. W. Huang, "60GHz high-gain low-noise amplifiers with a common-gate inductive feedback in 65nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, 2011, pp. 1–4.
- [63] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M. T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1056, 2007.
- [64] J. Janssens and M. Steyaert, *CMOS cellular receiver front-ends: from specification to realization*. Boston, MA: Kluwer, 2002.
- [65] X. Yi, C. C. Boon, J. Sun, N. Huang, and W. M. Lim, "A low phase noise 24/77 GHz dual-band sub-sampling PLL for automotive radar applications in 65 nm CMOS technology," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2013, pp. 417–420.
- [66] T. Maeda, N. Matsuno, S. Hori, T. Yamase, T. Tokairin, K. Yanagisawa, H. Yano, R. Walkington, K. Numata, N. Yoshida, Y. Takahashi, and H. Hida, "A low-power dual-band triple-mode WLAN CMOS Transceiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2481–2489, 2006.
- [67] I. Nasr, B. Laemmle, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "A 70-90-GHz high-linearity multi-band quadrature receiver in 0.35-um SiGe Technology," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 12, pp. 4600–4612, 2013.
- [68] E. J. Wilkinson, "An n-way hybrid power divider," *IEEE Trans. Microw. Theory Tech.*, vol. 8, no. 1, pp. 116–118, 1960.

- [69] G. Features, "Aircraft Transformers — Small and Light," *Electr. Eng.*, vol. 63, no. 3, pp. 84–88, 1943.
- [70] N. Huang, C. C. Boon, and X. Yi, "A dual-band 24 and 77 GHz CMOS LNA for automotive radars," in *International Conference on Electronics, Information and Communication*, 2013, pp. 44–45.
- [71] X. Wang, I. Sakagami, K. Takahashi, and S. Okamura, "A planar three-way dual-band power divider using two generalized open stub Wilkinson dividers," in *IEEE Microwave Conference Proceedings (APMC)*, 2010, pp. 714–717.
- [72] L.-H. L. L.-H. Lu, P. Bhattacharya, L. P. B. Katehi, and G. E. Ponchak, "X-band and K-band lumped Wilkinson power dividers with a micromachined technology," in *IEEE Microwave Symposium Diges*, 2000, vol. 1, pp. 287–290.
- [73] J. G. Kim and G. M. Rebeiz, "Miniature four-way and two-way 24 GHz wilkinson power dividers in 0.13  $\mu\text{m}$  CMOS," *IEEE Microw. Wirel. Components Lett.*, vol. 17, no. 9, pp. 658–660, 2007.
- [74] T. Kawai, I. Ohta, and A. Enokihara, "Design method of lumped-element dual-band Wilkinson power dividers based on frequency transformation," in *IEEE Microwave Conference Proceedings (APMC), Asia-Pacific*, 2010, pp. 710–713.
- [75] D. M Pozar, *Microwave Engineering*, 3rd ed. Wiley, 2005.
- [76] P. L. Richards, "Bolometers for infrared and millimeter waves," *J. Appl. Phys.*, vol. 76, no. 1, pp. 1–24, 1994.
- [77] T. May, V. Zakosarenko, E. Kreysa, W. Esch, S. Anders, H. P. Gemuend, E. Heinz, and H. G. Meyer, "Design, realization, and characteristics of a transition edge bolometer for sub-millimeter wave astronomy," *Rev. Sci. Instrum.*, vol. 83, no. 11, 2012.
- [78] M. Devlin, A. E. Lange, T. Wilbanks, and S. Sato, "DC-coupled, high sensitivity bolometric detector system for the infrared telescope in space," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 2, pp. 162–165, 1993.
- [79] A. Alessandrello, C. Brofferio, O. Cremonesi, A. Giuliani, M. Pedretti, A. Nucciotti, M. Pavan, G. Pessina, and E. Previtali, "A front-end for an array of  $\mu$ -bolometers for the study of the neutrino mass," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 1851–1856, 2000.

- [80] J. J. Lynch, H. P. Moyer, J. H. Schaffner, Y. Royter, M. Sokolich, B. Hughes, Y. J. Yoon, and J. N. Schulman, "Passive millimeter-wave imaging module with preamplified zero-bias detection," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 7, pp. 1592–1600, 2008.
- [81] M. E. Tiuri, "Radio Astronomy Receivers," *IEEE Trans. Mil. Electron.*, vol. 8, no. 3, pp. 264–272, 1964.
- [82] E. D. Cohen, "The MMIC program—a retrospective," *IEEE Microw. Mag.*, vol. 13, no. 4, pp. 77–88, 2012.
- [83] N. J. Koliass, "MMIC pioneers: A historical review of MMIC development at Raytheon," in *IEEE Microwave Symposium Digest*, 2009, pp. 1405–1408.
- [84] W. M. L. Kuo, Y. Lu, B. A. Floyd, B. M. Haugerud, A. K. Sutton, R. Krithivasan, J. D. Cressler, B. P. Gaucher, P. W. Marshall, R. A. Reed, and G. Freeman, "Proton radiation response of monolithic millimeter-wave transceiver building blocks implemented in 200 GHz SiGe technology," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3781–3787, 2004.
- [85] L. Gilreath, V. Jain, and P. Heydari, "Design and analysis of a w-band sige direct-detection-based passive imaging receiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2240–2252, 2011.
- [86] S. Ickhyun, S. Jung, N. E. . Lourenco, U. S. . Raghunathan, Z. E. . Fleetwood, S. . Zeinolabedinzadeh, T. B. . Gebremariam, F. . Inanlou, N. J.-H. . Roche, A. . Khachatryan, D. . McMorro, S. P. . Buchner, J. S. . Melinger, J. H. . Warner, P. . Paki-Amouzou, and J. D. Cressler, "Design of radiation-hardened RF low-noise amplifiers using inverse-mode SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3218–3225, 2014.
- [87] Y. S. Jiang, Z. M. Tsai, J. H. Tsai, H. Te Chen, and H. Wang, "A 86 to 108 GHz amplifier in 90 nm CMOS," *IEEE Microw. Wirel. Components Lett.*, vol. 18, no. 2, pp. 124–126, 2008.
- [88] X. Yi, C. C. Boon, H. Liu, J. F. Lin, and W. M. Lim, "A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with In-phase injection-coupled QVCO in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 347–359, 2014.
- [89] D. R. Lu, Y. C. Hsu, J. C. Kao, J. J. Kuo, D. C. Niu, and K. Y. Lin, "A 75.5-to-120.5-GHz, high-gain CMOS low-noise amplifier," in *IEEE Microwave Symposium Digest*, 2012, pp. 1–3.

- [90] C. Inui, I. C. H. Lai, and M. Fujishima, “60GHz CMOS current-reuse cascade amplifier,” in *IEEE Microwave Conference, Asia-Pacific*, 2007, pp. 1–4.
- [91] D. Sandström, M. Varonen, M. Kärkkäinen, and K. Halonen, “W-band CMOS amplifiers achieving +10dBm saturated output power and 7.5dB NF,” in *IEEE Solid-State Circuits Conference Digest of Technical Papers*, 2009, pp. 486–487.
- [92] Y. Yang, S. Cacina, and G. M. Rebeiz, “A SiGe BiCMOS W-Band LNA with 5.1 dB NF at 90 GHz,” in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2013, no. c, pp. 1–4.
- [93] P. Song, A. C. Ulusoy, R. L. Schmid, and J. D. Cressler, “A high gain, W-band SiGe LNA with sub-4.0 dB noise figure,” in *IEEE Solid-State Circuits Conference Digest of Technical Papers*, 2009, pp. 486–487.
- [94] N. Zhang, C. M. Hung, and K. O. Kenneth, “80-GHz tuned amplifier in bulk CMOS,” *IEEE Microw. Wirel. Components Lett.*, vol. 18, no. 2, pp. 121–125, 2008.
- [95] L. Zhou, C. C. Wang, Z. Chen, and P. Heydari, “A W-band CMOS receiver chipset for millimeter-wave radiometer systems,” *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 378–391, 2011.
- [96] T. Luo, C. Wu, and Y. Chen, “A 77-GHz CMOS automotive radar transceiver with anti-interference function,” *Circuits Syst. I Regul. Pap. IEEE Trans.*, vol. 60, no. 12, pp. 3247–3255, 2013.
- [97] V. Le, H. Duong, and A. Huynh, “A CMOS 77-GHz receiver front-end for automotive radar,” *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 10, pp. 3783–3793, 2013.
- [98] Z. Liu and R. M. Weikle, “High-order subharmonically pumped mixers using phased local oscillators,” *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 7, pp. 2977–2982, 2006.
- [99] Y. J. Hwang, C. H. Lien, H. Wang, M. W. Sinclair, R. G. Gough, H. Kanoniuk, and T. H. Chu, “A 78-114 GHz monolithic subharmonically pumped GaAs-based HEMT diode mixer,” *IEEE Microw. Wirel. Components Lett.*, vol. 12, no. 6, pp. 209–211, 2002.
- [100] A. V. Oppenheim, A. S. Willsky, and S. Hamid, *Signals and Systems*, 2nd ed. Prentice Hall, 1996.

- [101] J. Tsai, "Design of 40 – 108-GHz Low-Power and High-Speed CMOS Up-/Down-Conversion Ring Mixers for," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 670–678, 2012.
- [102] H. Chiou, H. Chou, and C. Liang, "A 35-to-83 GHz Multiconductor-Lines Signal Combiner for High Linear and Wideband Mixer," *IEEE Microw. Wirel. Components Lett.*, vol. 23, no. 10, pp. 548–550, 2013.
- [103] A. M. Niknejad, S. Emami, B. Heydari, M. Bohsali, and E. Adabi, "Nanoscale CMOS for mm-wave applications," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2007, pp. 1–4.
- [104] S. Pellerano, Y. Palaskas, and K. Soumyanath, "A 64GHz 6.5 dB NF 15.5 dB gain LNA in 90nm CMOS," in *IEEE European 33<sup>rd</sup> Solid State Circuits Conference*, 2007, pp. 352–355.
- [105] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Prentice Hall, 1996.
- [106] C. F. Liao and S. I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, 2007.
- [107] D. C. W. Lo, H. Wang, B. R. Allen, G. S. Dow, K. W. Chang, M. Biedenbender, R. Lai, S. Chen, and D. Yang, "Novel monolithic multifunctional balanced switching low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 12, pp. 2629–2634, 1994.
- [108] M. Uzunkol and G. M. Rebeiz, "A 65 GHz LNA/phase shifter with 4.3 dB NF using 45 nm CMOS SOI," *IEEE Microw. Wirel. Components Lett.*, vol. 22, no. 10, pp. 530–532, 2012.
- [109] P. Wambacq, B. Verbruggen, K. Scheir, J. Borremans, M. Dehan, D. Linten, V. De Heyn, G. Van der Plas, A. Mercha, B. Parvais, C. Gustin, V. Subramanian, N. Collaert, M. Jurczak, and S. Decoutere, "The potential of FinFETs for analog and RF circuit applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 11 SPEC. ISS., pp. 2541–2551, 2007.

# Publication List

1. **N. Huang**, C. C. Boon, and X. Yi, “A dual-band 24 and 77 GHz CMOS LNA for automotive radars,” in *International Conference on Electronics, Information and Communication*, 2013, pp. 44–45.
2. **N. Huang**, C. C. Boon, and X. Yi, “Formulas for the analysis of effect of feedback on noise performance,” in *International Conference on Electronics, Information and Communication*, 2013, pp. 54–55.
3. **N. Huang**, X. Yi, C. C. Boon, X. Zhao, J. Sun, G. Y. Feng, “Design of a fully integrated CMOS dual K- and W- band lumped Wilkinson power divider,” in *IEEE 56th International Midwest Symposium on Circuits and Systems*, 2013, pp. 788-791.
4. **N. Huang**, X. Yi, C. C. Boon, X. He, G. Y. Feng, W. M. Lim, X. Zhu, “A CMOS W-band 4x quasi-subharmonic mixer,” *IEEE Microwave and Wireless Components Letters*, vol.23, no.10, pp.548–550, 2015. (IF= 1.703)
5. **N. Huang**, C. C. Boon, X. Zhu, X. Yi, X. He, G. Y. Feng, W. M. Lim, B. Liu., “A 65-nm CMOS LNA for Bolometer Applications,” *Journal of Infrared, Millimeter, and Terahertz Waves*, Springer, January 2016. (Accepted) (IF=1.942)
6. X. Yi, C. C. Boon, J. Sun, **N. Huang**, W. M. Lim, “ A Low Phase Noise 24/77 GHz Dual-Band Sub-Sampling PLL for Automotive Radar Applications in 65 nm CMOS Technology,” in *IEEE Asian Solid-State Circuits Conference*, 2013, pp.417-420.