The shuttle nano-electro-mechanical non-volatile memory

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***Abstract*—Non-volatile memories (NVM) based on storage layers, pn junctions and transistors, like FLASH, suffer from poor retention at high temperature, high voltage writing, and wear out while cycling. This paper presents the structure, operation, and modeling of a nano-electro-mechanical (NEM) non-volatile memory based on the switching of a free electrode between two stable states. This electrode, called the shuttle, has no mechanical anchors and commutes between two positions. It is guided inside an insulator pod. Adhesion forces between the shuttle and fixed electrodes serve to hold the shuttle in stable positions. Smooth metal layers give strong Van der Waals stiction between two surfaces in contact. Memory detection is obtained by probing the conductance between two fixed contacts, the shuttle acting as a moveable bridge between these electrodes. Electro-mechanical contacts have an ideally large resistance ratio between ON and OFF levels. At micro-scale, gravity is found to be negligible compared to adhesion forces, which motivates the anchorless design for high-temperature data storage.**

The model proposed is based on charge induction over the surface of metal electrodes, and is validated by finite element method (FEM). Kinematic equations and energy transfers of the shuttle device are explored. Due to its unique anchorless design, the scalability of the anchorless shuttle memory is found to be excellent.

***Index Terms*—Non-volatile memory, MEMS, NEMS, high-temperature electronics, electrostatic actuation.**

I. Introduction

THE continuous scaling in MOSFET channel length has led to a significant increase in CMOS static energy consumption due to the increase in sub-threshold leakage current (I_{OFF}) [1]. Typically, scaling of memory cells such as SRAM, DRAM, or FLASH is made difficult because of their tight requirements on static leakage, immunity to process variations, and noise.

Emerging devices that can achieve zero standby leakage and low turn-on voltage have been proposed to alleviate this issue. However, any silicon *"CMOS-like"* devices such as tunnel-FET [2], impact-ionization MOSFET [3], and suspended-gate FET [4] also suffer from I_{OFF} leakage. To overcome this limit, nano-electro-mechanical (NEM) devices with air gaps and resistive electro-mechanical contacts have been investigated for digital applications [5]–[6] because they ideally have both zero I_{OFF} and abrupt switching. Similarly, non-volatile memories based on micro-electro-mechanical systems (MEMS) have been proposed for high temperature (HT) data storage [7]. MEMS memories can be categorized as either *storage-layer-based* devices, where data are typically stored as a charge [8], or *storage-layer-free* devices, where non-volatility is obtained either by adhesion forces [7] or by a bistable mechanical design (zippering [9], buckling [10]).

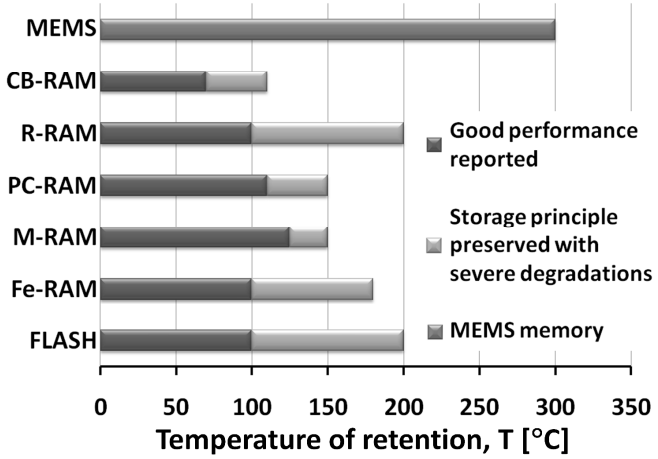

Fig. 1. Maximum temperature of operation for various types of non-volatile memories. This review is based on recently published papers, constrains are more stringent for commercial memories.

Review of HT performances for various types of NVM is summarized in Fig. 1. The actual mainstream for NVM integration is FLASH technology [11]-[12]. Emerging NVM typically include resistive RAM (R-RAM) [13], magnetic RAM (M-RAM) [14], phase-change RAM (PC-RAM) [15], conductive-bridge RAM (CB-RAM) [16], and ferroelectric RAM (Fe-RAM) [17]. Different physical mechanisms (FLASH: floating gate, M-RAM: free magnetic layer, Fe-

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RAM: ferroelectric polarization) are exploited to store data, but all suffer from poor retention at HT. However, adhesion-based NEM memories can potentially offer seamless SET/RESET/READ/HOLD cycles over an extremely wide temperature range for industrial or defense electronics.

The observation of metal-metal adhesion increase with temperature is reported in various studies focusing on electro-mechanical contacts [7]-[18]-[19]. This effect can be explained by metal softening with temperature increase. Therefore, the data storage principle in adhesion-based NEM memories is strengthened with temperature, which is an opposite trend compared to all storage-layer-based NVM.

The shuttle memory presented in this paper is a novel type of NVM. Using an anchorless design [20] is advantageous for compactness. It is also suggested that a floating electrode offers unique performance in terms of low actuation voltage and reliability. An analytical model based on Newton's motion equation is developed and validated by FEM simulation. Finally, energy transfers during a switching cycle are given.

II. The Anchorless Shuttle Memory

A. Structure and operating principle

Geometrical and material related parameters are summarized in Table I. For this study, the use of tantalum nitride (TaN) as a shuttle and contacts metal is proposed.

TABLE I
INDEX OF MODEL PARAMETERS.

Symbol	Quantity	Value
ε_0	dielectric constant of vacuum	$8.854 \cdot 10^{-12}$ F/m
g	gravitational acceleration	9.81 m/s^2
A	shuttle surface	2µm x 2µm = 4µm^2
L	shuttle length	2µm
$d_{shuttle}$	shuttle thickness	300nm
ρ	shuttle metal density (TaN)	$16.6 \cdot 10^3$ kg/m^3
m	shuttle mass	$2 \cdot 10^{-14}$ kg
d_{gap}	vacuum actuation gap	100nm
d_{DS}	drain-source slit gap	200nm
d_{metal}	drain-source metal thickness	300nm
d_{vdw}	Van der Waals distance	5nm
x	shuttle displacement	$0<x<2d_{gap}$
A_{TaN}	Hamaker constant of TaN	$20 \cdot 10^{-20}$ J
Γ	TaN-TaN adhesion energy	33mJ/m^2
α	real/apparent contact area	0.1%

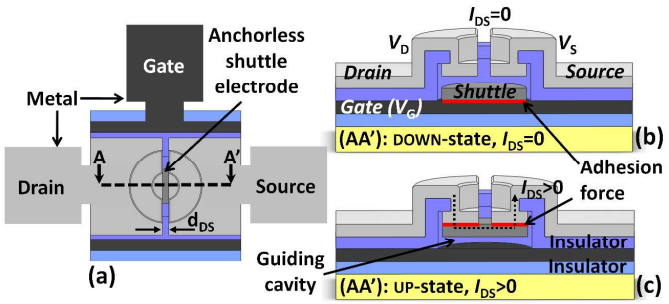

Fig. 2. (a) Top-view layout of the 3-terminal NEM memory. AA' 3D cross sections in the DOWN (b) and UP (c) states. Memory reading is done by V_{DS} bias and current reading: I_{DS}=0 in DOWN-state, and I_{DS}>0 in UP-state.

Figure 2 illustrates the structure of the proposed 3-terminal (D: Drain, S: Source, G: Gate) NEM shuttle memory. Permanent retention is obtained by adhesion forces between the shuttle and the fixed electrodes in contact. A guiding cavity ensures that the free-flying shuttle electrode is actively switched and has only two stable positions (UP and DOWN).

Memory reading is achieved by probing the resistance between drain and source electrodes, with an ideally large ratio between ON (resistance: R_{ON}) and OFF (resistance: R_{OFF}) states. In the OFF-state, no current can flow, and the isolation is only determined by surface leakage currents (typically R_{OFF}>10GΩ). In the ON-state, source and drain electrodes are shorted by the shuttle electrode. The value of R_{ON} is determined by $R_{ON}=2 \cdot R_{contact}$, where $R_{contact}$ is the electro-mechanical contact resistance between the shuttle and fixed electrodes (access and shuttle resistance are negligible). Values of metal-metal electro-mechanical contacts are typically in the range of 5Ω to 50Ω for hard metals having a smooth surface [21]. That means a R_{OFF}/R_{ON} ratio as large as 10^8 is achievable, without degradation at high temperature.

The associated parasitic drain to source C_{DS} capacitance is estimated by:

$$C_{DS} = \varepsilon_0 \cdot \frac{L \cdot d_{metal}}{d_{DS}} \quad (1)$$

where d_{metal} is the thickness of source/drain electrodes and d_{DS} is the gap between electrodes (see Fig. 2). Typical values (L=2µm, d_{metal}=300nm, d_{DS}=200nm) result in C_{DS}~27aF. Such a small value does not impact memory reading.

An anchorless design has unprecedented advantages in terms of reliability and low variability. The absence of flexural (or torsional) anchors makes the scalability of this NEM structure ($9F^2$) remarkable compared to most NEM devices. For example, using a 200nm ½-pitch lithography system results in a density of $700 \cdot 10^3$ devices/mm^2. A proper NEMS/CMOS addressing scheme must be developed to control shuttle-based NVM arrays, integrated on top of a CMOS chip for cost and density efficiency.

The main challenge to get a small footprint and low-voltage actuation (V_{DD}<1V) resides in the ability to release nanoscale gaps. Anchorless structures have not been widely explored so far. Some noteworthy reports include radio-frequency (RF) switches [20], [22] and a conceptual non-volatile memory based on the free displacement of a guided carbon nanotube [23]. Gravity and shocks are found to be negligible at sub-micron scale, with a shuttle electrode being immune to accelerations up to 10^5g. A disk-shape shuttle is ideal, as it prevents any risk of shuttle gripping inside its cavity.

Only three materials are needed for the integration of the shuttle memory: metal, insulator and a sacrificial material. The whole integration process can be done with a very minimum number of lithographic steps, and at moderate temperature to preserve any underlying CMOS stacks. It is also suggested [6] to properly package under vacuum the device, to make sure air damping does not slow down the shuttle during transitions; and to protect metal contacts from oxidation, dust and humidity.

Shuttle memory bias conditions are listed in Table II.

TABLE II
INDEX OF STIMULUS AND MODEL PARAMETERS.

Symbol	Quantity	Value
V_D	applied drain voltage	0
V_S	applied source voltage	0
$V_{D/S}$	applied drain and source voltage	$V_{D/S}=V_D=V_S=0$
$V_{shuttle}$	shuttle voltage	floating
V_G	applied gate voltage amplitude (pulsed-mode)	10V
V_P	pull-out voltage	
V_R	reading voltage	$V_R<<V_P$
$R_{contact}$	metal-metal contact resistance	
R_{ON}	drain-to-source resistance (shuttle in the up-state)	$R_{ON}=2\cdot R_{contact}$
R_{OFF}	drain-to-source resistance (shuttle in the down-state)	
$Q_{shuttle}$	fixed shuttle charge	$-1.78\cdot10^{-15}$ C
q_{top}	induced charge on shuttle top interface	
q_{bottom}	induced charge on shuttle bottom interface	
q_D	induced drain charge	
q_S	induced source charge	
q_G	induced gate charge	
F_{up}	electrostatic force shuttle → drain/source	
F_{down}	electrostatic force shuttle → gate	
T_{pulse}	gate voltage pulse duration	
t_0	gate voltage turn-on time $0\rightarrow V_G$	$t_0=0$
t_1	gate voltage turn-off time $V_G\rightarrow0$	$t_1=T_{pulse}$
t_2	shuttle landing time	

The shuttle NVM is based on the commuting of a floating (mechanical and electrical) electrode between a bottom fixed electrode (G) and two anchored electrodes (D/S). Forces acting on the shuttle are (i) electrostatic forces, (ii) adhesion forces between the shuttle and fixed electrodes, (iii) damping forces during transients, and (iv) shuttle gravity. Damping is negligible, as the device operates under vacuum.

TABLE III
OPERATING PRINCIPLE OF THE NVM DEVICE.

Logic	Applied voltage	Effect
Switching down	$V_D=V_S=0$ $V_G=V_P$ (pulse)	V_P: Pull-out voltage $F_{down}>F_{adhesion}$
Switching up	$V_D=V_S=V_P$ (pulse) $V_G=0$	Switching to both drain and source. $F_{up}>F_{adhesion}$
Read	$V_D=V_R$, $V_S=0$ $V_G=0$	V_R: Read voltage ($V_R<<V_P$) down-state: $I_{DS}=0$ up-state: $I_{DS}>0$ $I_{DS}\cong V_{DS}/2\cdot R_C$
Hold	$V_D=V_S=V_G=0$	Non-volatility: adhesion increases with temperature

Switching occurs when the electrostatic force applied to the shuttle overcomes adhesion forces. A pulsed voltage ($V_G>0$) applied to the gate electrode moves the shuttle down (assuming $V_D=V_S=0$), while a pulsed voltage applied to both drain and source ($V_D=V_S>0$) moves the shuttle up (assuming $V_G=0$). Logic states are shown in Table III. The pulsed mode is needed to avoid the shuttle to operate as an electrostatic oscillator. Drain and source are symmetric to ease circuit design. The stability and switching thresholds of the shuttle memory are presented in Fig. 3. A hysteresis ideally centered at $V_G=V_D=V_S=0$ ensures the non-volatility of the memory, *i.e.* data retention when the chip is powered off.

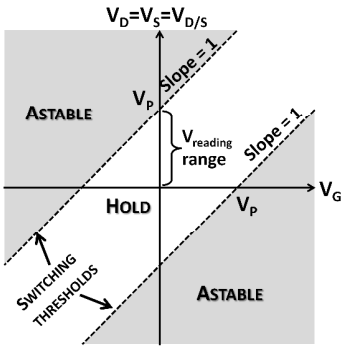

Fig. 3. Stability and switching thresholds of the shuttle NVM. A hysteresis ideally centered at $V_D=V_S=V_G=0$ ensures that data are properly stored when the device is powered off.

B. Adhesion forces and switching threshold

The model presented describes a transition from the UP-state (the shuttle being stuck to both drain and source) to the DOWN-state (the shuttle being stuck to the gate). The separation slit between drain and source electrodes is negligible, compared to the shuttle area. Similarly, fringing fields are neglected in the analytical model. Therefore, the electrostatic force applied to the shuttle (UP-state) towards the gate is expressed as:

$$F_{elec}(x=0)=\frac{1}{2}\cdot\frac{\varepsilon_0\cdot A\cdot(V_G-V_{D/S})^2}{(2d_{gap})^2}=\frac{1}{8}\cdot\frac{\varepsilon_0\cdot A\cdot V_G^2}{d_{gap}^2} \quad (2)$$

The parameter A represents the shuttle planar area, $2d_{gap}$ the vacuum gap (double-air gap structure, see Fig. 2), ε_0 the permittivity of vacuum, and x=0 the initial position of the shuttle ($0<x<2d_{gap}$). When the shuttle is stuck to drain and source, $V_{shuttle}=V_D=V_S=0$. Adhesion forces between the shuttle and fixed electrodes in Eqn. (3) are given in terms of adhesion energy Γ and distance x between the two surfaces in contact, where $F_{adh}=0$ if $x>d_{vdw}$ and d_{vdw} is approximated to 5nm [24]. The parameter α represents the ratio between real to apparent contact area; this approximation being valid for smooth surfaces. The exact *Force–Energy* adhesion plot is highly experimental and usually extracted from atomic force microscopy (AFM) *Force–Stiction* plots [24].

$$F_{adh}(0<x<d_{vdw})=\frac{2\Gamma\cdot A\cdot\alpha}{d_{vdw}}\cdot\frac{d_{vdw}-x}{d_{vdw}} \quad (3)$$

To confirm this value, AFM scan of a physical vapor deposition (PVD) of tantalum nitride (TaN) layer was conducted. The surface is very smooth (D_{rms}=0.4nm) and ideal for electro-mechanical contacts. Adhesion energy of $\Gamma=33mJ/m^2$ is extracted from the AFM scan, where A_{TaN} is the Hamaker constant of TaN:

$$\Gamma = \frac{A_{TaN}}{12 \cdot \pi \cdot D_{rms}^2} \quad (4)$$

This corresponds to $F_{adh}(x=0,\alpha=1)=13\cdot10^3$ [N/m^2], in good accordance with other published reports, see for example [25]. The force is $F_{adh}(x=0,\alpha=1)=52\cdot10^{-9}$ [N] for a shuttle area of A=4μm^2.

Gravity (weight) of the shuttle is shown in Eqn. (5), where $d_{shuttle}$ represents the thickness of the shuttle, and ρ is the density of metal. Using metrics in Table I, $F_{gravity}=2\cdot10^{-13}$ [N].

$$F_{gravity} = (\rho \cdot A \cdot d_{shuttle}) \cdot g \quad (5)$$

From Eqns. (2) to (4), the minimum switching voltage V_P needed to pull the shuttle out of adhesion can be extracted. First, gravity is at least 4 to 5 order of magnitude smaller than the adhesion force needed to initiate switching, demonstrating the robustness of the anchorless design. Second, adhesion force very quickly decreases (contact opening) after pull-out, while electrostatic actuation increases (gap reduction). Last, all three forces (electrostatic, adhesion, and gravity) have similarly a linear dependence with the shuttle surface A. That means the switching voltage V_P does not depend from the actuation area A. This is an unusual result for most electrostatic MEMS devices, but of great interest for device scaling. The switching voltage V_P expression is in Eqn. (6) and plotted in Fig. 4.

$$V_P = 4d_{gap} \cdot \sqrt{\frac{\Gamma \cdot \alpha}{d_{vdw} \cdot \varepsilon_0}} \quad (6)$$

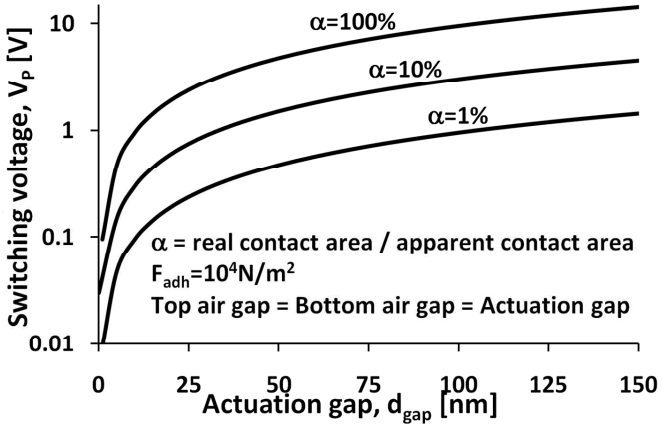

Fig. 4. Switching pull-out voltage V_P (log-scale) *vs.* actuation gap d_{gap}. Sub-25nm actuation gaps are typically needed for low-voltage actuation. Switching voltage does not depend on shuttle area A.

C. Shuttle static analysis

This section describes the static analysis of the shuttle electrode in vacuum. Once the shuttle has lifted off, it *flies* until it eventually reaches the opposite electrode. The study is conducted for a transition from drain/source side towards the gate. When a positive bias V_G is applied to the gate ($V_{D/S}$=0), the shuttle is charged. If the applied voltage V_G is higher than the pull-out (switching) voltage V_P, then the shuttle lifts off and carries a net charge $Q_{shuttle}$ until it reaches the opposite electrode. Gate voltage actuation needs to be turned off during the shuttle flight, or the shuttle would be charged by an opposite charge -$Q_{shuttle}$ when landing and rebound towards its initial position. This effect, which is not desirable for memory application, is reported as *electrostatic pendulum* [26].

The model is based on charge distribution over the surface of metal electrodes, as shown in Fig. 5. The net charge on the shuttle splits between the top and bottom interface, and its redistribution depends on both the external applied voltages and the shuttle position (0<x<2d_{gap}).

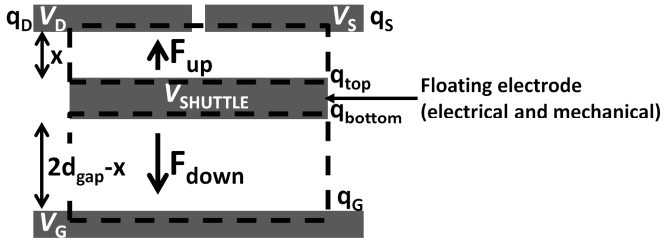

Fig. 5. Double air gap capacitor divider with charge distribution. While switching, the shuttle electrode carries a constant charge.

From the charge conservation on the shuttle and the electrostatic law of a capacitor Q=C·V (in this case, two air-gap capacitors), the charge equilibrium system is:

$$\begin{cases} q_D = q_S \\ q_D + q_S + q_{top} = 0 \\ q_{bottom} + q_G = 0 \\ q_{top} + q_{bottom} = Q_{shuttle} \\ q_G = -q_{bottom} = \dfrac{\varepsilon_0 \cdot A}{(2d_{gap} - x)} \cdot (V_G - V_{SHUTTLE}) \\ q_{top} = -q_D - q_S = \dfrac{\varepsilon_0 \cdot A}{x} \cdot (V_{SHUTTLE} - V_{D/S}) \end{cases} \quad (7)$$

The net charge on the shuttle depends on its initial charging, as written in Eqn. (8).

$$Q_{shuttle} = Q = \frac{\varepsilon_0 \cdot A}{2 \cdot d_{gap}} \cdot V_G \quad (8)$$

The model was verified by FEM simulation [27], with a charged shuttle placed between fixed electrodes, see Fig. 6(a). Both charge induction over surfaces and shuttle charge splitting between top and bottom interfaces are observed. A charge distribution cross-section is extracted in Fig 6(b).

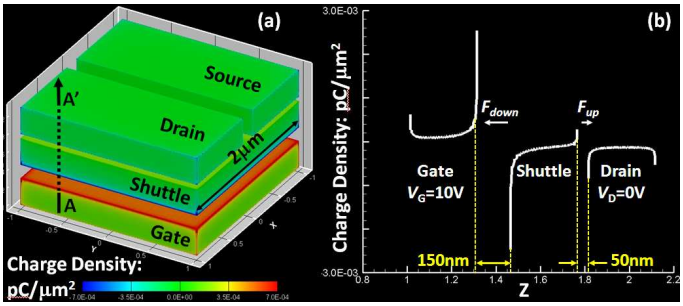

Fig. 6 (a) FEM charge density simulation of a charged conductive shuttle placed between fixed drain, source, and gate electrodes. Bias conditions are V_D=V_S=0 and V_G=10V, and shuttle position is x=50nm ($2d_{gap}$-x=150nm). Corner effects inducing extra charges are visible on electrode edges. (b) AA' cross section of the charge density distribution. The surface charge distribution inducing electrostatic forces F_{down} and F_{up} are visible.

As a result, two electrostatic forces, named F_{up} (towards D/S) and F_{down} (towards gate) build up during the switching, see Eqn. (9). One force (F_{up}) operates as a *break*, while the other (F_{down}) acts as a *motor* for switching.

$$\begin{cases} F_{up} = \dfrac{q_{top}^2}{2\cdot\varepsilon_0\cdot A} = \dfrac{(q_D+q_S)^2}{2\cdot\varepsilon_0\cdot A} \\ F_{down} = \dfrac{q_{bottom}^2}{2\cdot\varepsilon_0\cdot A} = \dfrac{q_G^2}{2\cdot\varepsilon_0\cdot A} \end{cases} \quad (9)$$

From Eqns. (7) to (9), the evolution of the two electrostatic forces (F_{up} and F_{down}) as a function of the shuttle position is extracted and plotted (see Fig. 7). The difference between the analytical solution and FEM results (8%) is due to corner/edge effects, which are not captured by the analytical model. This discrepancy induces a higher FEM charge density than predicted by equations, therefore increasing both F_{up} and F_{down}.

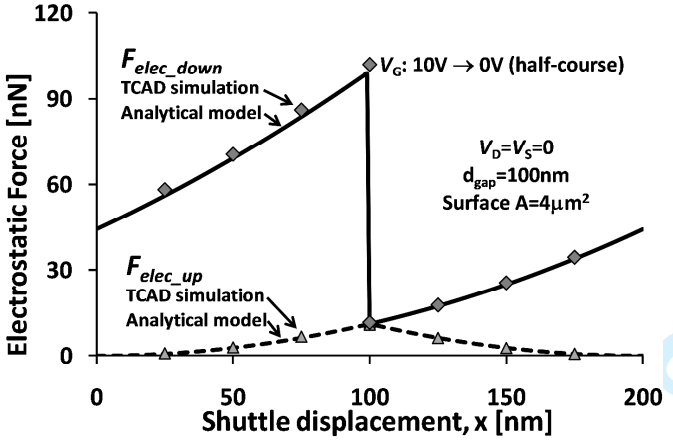

Fig. 7. Analytical modeling of electrostatic forces F_{down} (shuttle → gate) and F_{up} (shuttle → drain/source) *vs.* shuttle displacement. V_G-pulse turn-off is applied after shuttle ½-course. Solid markers represent TCAD solutions.

In this static analysis example, V_G pulse is turned-off at x=100nm, which corresponds to the middle of the course. We observe from Fig. 7, that even with the condition $V_G=V_D=V_S=0$, F_{up} and F_{down} forces are non-zero, due to the fixed shuttle charge. Figure 8 shows the evolution of the induced shuttle voltage, with an abrupt change at x=100nm.

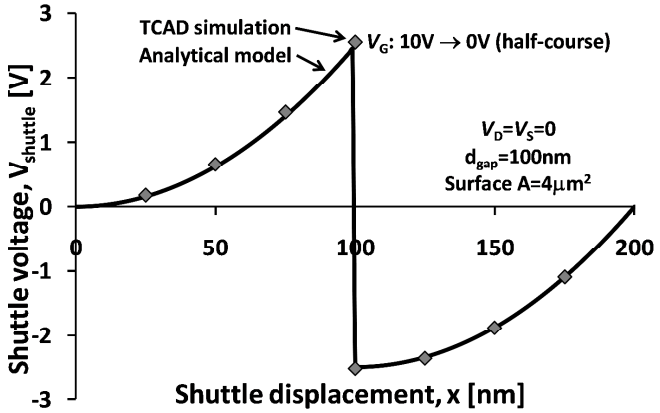

Fig. 8. Evolution of the shuttle voltage during switching. V_G-pulse turn-off is applied after shuttle ½-course. Solid markers represent TCAD solutions.

D. Shuttle dynamic analysis

The time-dependent control of the gate voltage follows the time diagram shown in Fig. 9. To avoid an electrostatic rebound of the shuttle, the switching is divided between an *accelerated flight (V_G>0, V_D=V_S=0)* and a *free flight (V_G=0, V_D=V_S=0).*

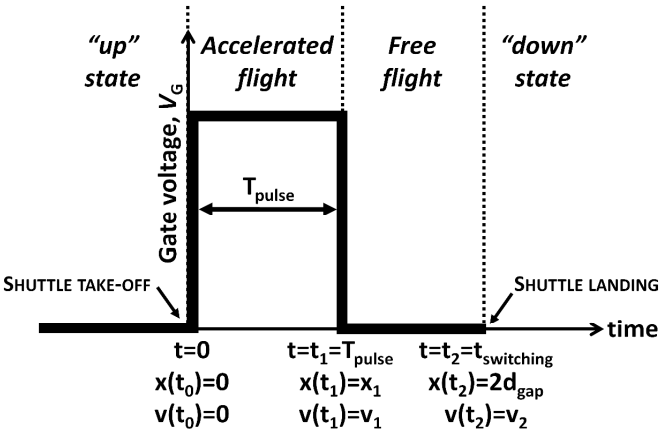

Fig. 9. Transient details of the pulsed-mode switching, simulating a transition from the "UP" state to the "DOWN" state. In order to avoid rebound of the shuttle, the switching of the electrode must be divided into an "accelerated" flight phase and a "free" flight phase.

Dynamic equation is solved from Newton's second law of motion. The two forces applied to the shuttle are F_{up} and F_{down}, and the resulting equation is as followed, where m is the shuttle mass:

$$m\cdot\frac{d^2x(t)}{dt^2} = \frac{q_{bottom}^2}{2\cdot\varepsilon_0\cdot A} - \frac{q_{top}^2}{2\cdot\varepsilon_0\cdot A} \quad (10)$$

Using values from Eqn. (7), Eqn. (10) can be solved analytically. Eqn. (10) is a 2nd order differential equation and has a single physical solution. In Eqn. (11), a K-factor is used as a substitution coefficient. Motion equation (12) is valid for any value of applied voltages, including $V_{D/S}\neq 0$. Eqn. (13) is the first derivative of Eqn. (12) and represents the shuttle speed. Initial conditions for position and speed are $x(t_0)$ and $v(t_0)$, respectively.

$$K = \sqrt{2\cdot A\cdot\varepsilon_0\cdot d_{gap}\cdot m} \quad (11)$$

$$x(t) = \frac{1}{Q}(d_{gap}\cdot Q + A\cdot\varepsilon_0(-V_{D/S}+V_G) + [-d_{gap}\cdot Q + A\cdot\varepsilon_0(V_{D/S}-V_G) + Q\cdot x(t_0)]\cdot Cosh(\frac{Q\cdot t}{K}) + K\cdot v(t_0)\cdot Sinh(\frac{Q\cdot t}{K})) \quad (12)$$

$$\frac{dx(t)}{dt} = v(t) = v(t_0)\cdot Cosh(\frac{Q\cdot t}{K}) + \frac{-d_{gap}\cdot Q + A\cdot\varepsilon_0(V_{D/S}-V_G) + Q\cdot x(t_0)}{K}\cdot Sinh(\frac{Q\cdot t}{K}) \quad (13)$$

As shown in Fig. 9, shuttle flight is divided into two phases. At $t=t_1=T_{pulse}$, gate voltage must be switched off. Therefore, the relation between landing time t_2 and turn-off time t_1 is solved and presented in Eqn. (15), with Eqn. (14) as substitution. $x_1=x(t_1)$ and $v_1=v(t_1)$ represent shuttle position and speed at $t=t_1$, respectively.

$$\kappa = \frac{d_{gap} \cdot Q^2 \cdot (-d_{gap} + x_1) + \sqrt{K^2 v_1^2 (K^2 v_1^2 + Q^2 \cdot (2d_{gap} - x_1) \cdot x_1)}}{d_{gap}^2 \cdot Q^2 + K^2 \cdot v_1^2} \quad (14)$$

$$t_2 = t_1 - \frac{K}{Q} \cdot Arc\sec h(\kappa) \qquad 0 < \kappa \le 1 \quad (15)$$

From Eqn. (12), the position of the shuttle as a function of time is plotted. Curves are shown in Fig. 10. There is a given range for proper V_G pulse duration. If the pulse is too short, then the shuttle would go back to its initial position; if the pulse is too long, then the shuttle would experience an electrostatic rebound.

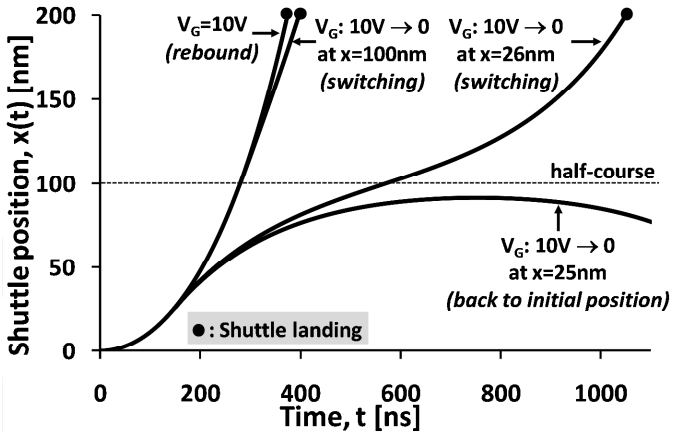

Fig. 10. Position of the shuttle electrode as a function of time. Depending on the duration of the V_G pulse, three cases could happen: (i) the shuttle back to its initial position if pulse duration is too short, (ii) proper switching or (iii) shuttle electro-mechanical rebound if the pulse is too long.

The dynamic analysis is done with the assumption that charge redistribution over various surfaces of the shuttle electrode is faster than its own mechanical displacement.

E. Switching speed and switching energy

Switching time and switching energy, as a function of T_{pulse} duration are reported in Fig. 11.

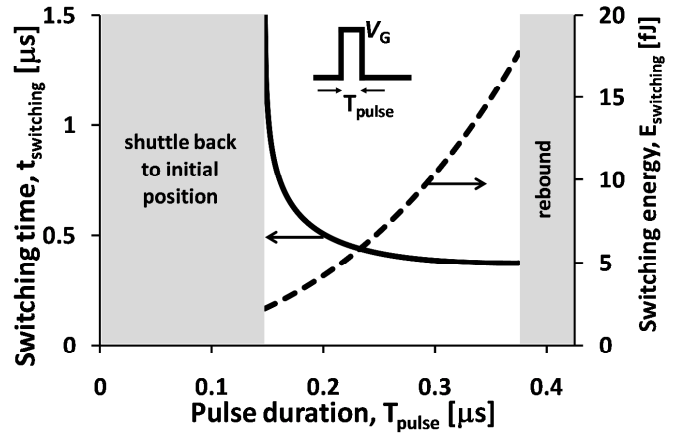

Fig. 11. Switching time and switching energy plots, as a function of V_G pulse duration.

The switching energy corresponds to the kinetic energy of the shuttle $1/2mv^2$, where m is the shuttle mass, and $v=v(t_2)$ the shuttle speed on landing ($v(t_2)$=1.3nm/ns if no V_G turn-off is applied). Without V_G turn-off, the calculated kinetic energy equals the initial charging energy of the shuttle-to-gate capacitor:

$$\frac{1}{2} m \cdot v(t_2)^2 = \varepsilon_0 \cdot \frac{A}{2d_{gap}} \cdot V_G^2 \quad (16)$$

If V_G is turned-off during switching, then a part of the initial charging energy is returned to power supplies (S, D, G).

III. Conclusion

This paper presents a new non-volatile NEM memory device, called the shuttle memory. It consists of a floating metal electrode guided inside a pod cavity, which is actuated by electrostatic forces and has two stable positions. Permanent data retention is obtained by adhesion forces only, which eliminates leakage current and predicts good reliability at high temperature. Furthermore, the anchorless geometry provides better compactness compared to planar MEMS memories, and does not suffer from elastic fatigue or thermal drifts.

A complete analytical model based on Newton's equation of motion is derived, and validated by FEM simulations. This memory must be controlled by a pulsed mode to avoid a pendulum effect. Further development should include MEMS/CMOS NVM arrays design and detailed analysis of shuttle fabrication parameters.

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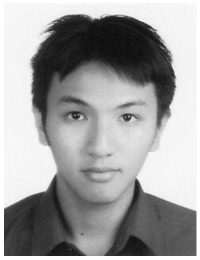
Dr Pott serves as reviewer in various IEEE journals and (co-)authored around 60 publications. His current research interests include micro and nano technology fabrication, MEMS, NEMS, nanowires and hybrid technologies.



Geng Li Chua was born in Singapore in Jan. 1987. He is currently pursuing a Bachelor Degree in Electrical & Electronics Engineering at National University of Singapore. He was on Industrial Attachment programme with the Institute of Microelectronics (IME), Agency for Science, Research, and Technology (A*STAR), Singapore, from January to June 2011. He is involved in research activities that focus on high temperature operating nano-electro-mechanical devices.

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Prof. Kim is the recipient of the 2008 AMD/CICC Student Scholarship Award, 2008 DAC/ISSCC Student Design Contest Award, 2008 Departmental Research Fellowship from University of Minnesota, 2008 Samsung Humantec Thesis Award (2008, 2001, and 1999), and 2005 ETRI Journal Paper of the Year Award.

Dear Dr. Yen-Hao Shih

We would like to thank you, as well as T-ED reviewers, for considering our abstract entitled: "The shuttle nano-electro-mechanical non-volatile memory" - TED-2011-08-0843-R. In this document, we address point-by-point latest concerns raised by one reviewer, and reflect these comments in the final version of our manuscript.

As mentioned in your e-mail, we also had to reduce the size of the abstract. In order to keep a good readability, we decided (as suggested by one reviewer) to remove the circuit-related section (this part to be published in a separated abstract) and to focus on the key message we would like to share with TED readers.

Sincerely,
Vincent Pott (and co-authors)

Reviewer: 1

No comments

Reviewer: 2

The authors answered all the comments satisfactorily. I recommend this manuscript is ready for publication. Thank you.

Reviewer: 3

No comments

Reviewer: 4

A. The revised manuscript is too long for a regular T-ED paper.
My suggestions are
(i) Merge III-(A) into II.
(ii) Completely remove III- (B) and -(C), and the last sentence in the abstract/conclusion.
These paragraphs are not the core of the NEM device so they can be discussed in the next paper.

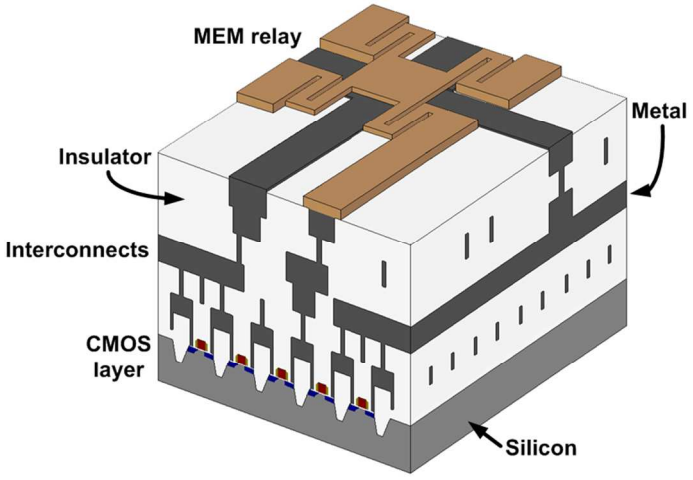
We reduced the size of the paper according to reviewer's suggestions. We also deleted non-cited references and slightly simplified the introduction/conclusion. The core modeling + FEM parts have not been changed, as they represent the key message of the paper.

B. Page 32, you didn't explain how you get the number, $9F^2$ in the revised manuscript, to readers (only for reviewers). Please revise. Actually, $9F^2$ is only for the memory element. The unit cell size, including 2 access transistors is much bigger than $9F^2$.

There are 2 points we would like to mention:

- *Concerning the shuttle device only: due to the limited size of the abstract, we don't believe that a floorplan (layout) figure will add a significant value to the paper. The value $9F^2$ represents the best achievable footprint. However, this footprint will be dependent to the fabrication process (i.e. dependent on the way the device is designed with litho masks). Therefore, we believe it is fair to mention the value $9F^2$ (checked by reviewers) to give TED readers a first estimation value of the achievable footprint (so they can compare this value with other published reports).*

- *Concerning the shuttle cell integrated on top of CMOS: The same planar area is used for both 2 access NMOS transistors and 1 NVM shuttle device (the section: 2NMOS/1MEMS had to be removed due to size limitation). Please see the picture[1] below.*
  In future abstracts, I fully agree a precise study must be conducted, and the 2 access NMOS transistors require to control the device will consume more than $9F^2$. Therefore, we will split the analysis between "footprint per MEMS device" and "footprint per bit cell".
  Again, we don't believe a precise design layout (MEMS/CMOS) is needed in this report. The goal is to emphasize the reasonable size consumption of the shuttle cell, compared to most anchored structures. The text has been amended accordingly. Thank you.



C. About English:
1. Page 31, line 30, "Emerging NVM typically" --> "Emerging NVMs typically"
2. Page 33, line 36, "Pulsed mode is needed" --> "The pulsed mode is needed"
3. Page 34, line 34, "ρ the density" --> "ρ is the density"
4. Page 34, line 52, "simulation plots in Fig. 5" --> "simulation plots are in Fig. 5"
5. page 35, line 12, "otherwise the shuttle" --> "or the shuttle"
6. page 35, line 14, "initial position, which is not" --> "initial position. This is not"

[1] **Picture reproduced from: V. Pott, T.-J. King Liu, *et al.*, *Proceedings of the IEEE*, vol. 98 (12), pp. 2076-2094, Dec. 2010.**

7. page 35, line 20, "and bottom interface, and its redistribution dependent on both external applied voltages and shuttle" --> "and bottom interfaces, and its redistribution depends on both the external applied voltages and the shuttle"
8. page 35, line 53, "(..) as a motor for switching" --> "(..) acts as a motor for switching"
9. page 36, lines 12-14, " results in reasonable, with a maximum error of 8% for FEM simulation. This discrepancy is due to corner/edges effects, which are not captured by the analytical model, and which induce..."--> " results (8%) is due to corner/edges effects, which are not captured by the analytical model. The corner/edges effect induce..."
10. page 36, line 55, please put the label "(12)" at the end of the equation.
11. Page 37, line 26, "way faster than" --> "faster than"
12. Page 38, line 1, "metrics, for example if..." --> "metrics. For example, if..."
13. Page 38, line 29, " in the previous reports, it is... rebound [29]." --> " in the previous report [29], it is ..."
14, Page 38, line 42, "Even if this value ... [28] and solving the ..." --> "Even though this value ... [28] for solving the ..."
15, page 38, line 59, " ...), divided between an accelerated..." --> "...". for an accelerated".
16, Page 39, line 13, "excellent reliability, as it has..." --> "excellent reliability because it has..."
17, Page 40, line 42, "S-slope degradation" --> "subthreshold swing degradation"
18, Page 41, line 1, " above-IC, this means..." --> "above-IC, which" (although I suggest removing this session).

I'm highly grateful for helping us improving the quality of our abstract. Mistakes have been corrected (some sections have been deleted in the final abstract).

The shuttle nano-electro-mechanical non-volatile memory

Vincent Pott, *Member, IEEE,* Geng Li Chua, Ramesh Vaddi, *Member, IEEE,*
Julius Tsai Ming Lin, *Member, IEEE,* and Tony T. Kim, *Member, IEEE*

***Abstract*—Non-volatile memories (NVM) based on storage layers, pn junctions and transistors, like FLASH, suffer from poor retention at high temperature, high voltage writing, and wear out while cycling. This paper presents the structure, operation, and modeling of a nano-electro-mechanical (NEM) non-volatile memory based on the switching of a free electrode between two stable states. This electrode, called the shuttle, has no mechanical anchors and commutes between two positions. It is guided inside an insulator pod. Adhesion forces between the shuttle and fixed electrodes serve to hold the shuttle in stable positions. Smooth metal layers give strong Van der Waals stiction between two surfaces in contact. Memory detection is obtained by probing the conductance between two fixed contacts, the shuttle acting as a moveable bridge between these electrodes. Electro-mechanical contacts have an ideally large resistance ratio between ON and OFF levels. At micro-scale, gravity is found to be negligible compared to adhesion forces, which motivates the anchorless design for high-temperature data storage.**

The model proposed is based on charge induction over the surface of metal electrodes, and is validated by finite element method (FEM). Kinematic equations and energy transfers of the shuttle device are explored. Due to its unique anchorless design, the scalability of the anchorless shuttle memory is found to be excellent.

***Index Terms*—Non-volatile memory, MEMS, NEMS, high-temperature electronics, electrostatic actuation.**

I. Introduction

THE continuous scaling in MOSFET channel length has led to a significant increase in CMOS static energy consumption due to the increase in sub-threshold leakage current (I_{OFF}) [1]. Typically, scaling of memory cells such as SRAM, DRAM, or FLASH is made difficult because of their tight requirements on static leakage, immunity to process variations, and noise.

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Emerging devices that can achieve zero standby leakage and low turn-on voltage have been proposed to alleviate this issue. However, any silicon *"CMOS-like"* devices such as tunnel-FET [2], impact-ionization MOSFET [3], and suspended-gate FET [4] also suffer from I_{OFF} leakage. To overcome this limit, nano-electro-mechanical (NEM) devices with air gaps and resistive electro-mechanical contacts have been investigated for digital applications [5]–[6] because they ideally have both zero I_{OFF} and abrupt switching. Similarly, non-volatile memories based on micro-electro-mechanical systems (MEMS) have been proposed for high temperature (HT) data storage [7]. MEMS memories can be categorized as either *storage-layer-based* devices, where data are typically stored as a charge [8], or *storage-layer-free* devices, where non-volatility is obtained either by adhesion forces [7] or by a bistable mechanical design (zippering [9], buckling [10]).

Review of HT performances for various types of NVM is summarized in Fig. 1. The actual mainstream for NVM integration is FLASH technology [11]-[12]. Emerging NVM typically include resistive RAM (R-RAM) [13], magnetic RAM (M-RAM) [14], phase-change RAM (PC-RAM) [15], conductive-bridge RAM (CB-RAM) [16], and ferroelectric RAM (Fe-RAM) [17]. Different physical mechanisms (FLASH: floating gate, M-RAM: free magnetic layer, Fe-RAM: ferroelectric polarization) are exploited to store data, but all suffer from poor retention at HT. However, adhesion-based NEM memories can potentially offer seamless SET/RESET/READ/HOLD cycles over an extremely wide temperature range for industrial or defense electronics.

The observation of metal-metal adhesion increase with temperature is reported in various studies focusing on electro-mechanical contacts [7]-[18]-[19]. This effect can be explained by metal softening with temperature increase. Therefore, the data storage principle in adhesion-based NEM memories is strengthened with temperature, which is an opposite trend compared to all storage-layer-based NVM.

The shuttle memory presented in this paper is a novel type of NVM. Using an anchorless design [20] is advantageous for compactness. It is also suggested that a floating electrode offers unique performance in terms of low actuation voltage and reliability. An analytical model based on Newton's motion equation is developed and validated by FEM simulation. Finally, energy transfers during a switching cycle are given.

II. THE ANCHORLESS SHUTTLE MEMORY

A. Structure and operating principle

Geometrical and material related parameters are summarized in Table I. For this study, the use of tantalum nitride (TaN) as a shuttle and contacts metal is proposed.

Figure 2 illustrates the structure of the proposed 3-terminal (D: Drain, S: Source, G: Gate) NEM shuttle memory. Permanent

retention is obtained by adhesion forces between the shuttle and the fixed electrodes in contact. A guiding cavity ensures that the free-flying shuttle electrode is actively switched and has only two stable positions (UP and DOWN).

Memory reading is achieved by probing the resistance between drain and source electrodes, with an ideally large ratio between ON (resistance: R_{ON}) and OFF (resistance: R_{OFF}) states. In the OFF-state, no current can flow, and the isolation is only determined by surface leakage currents (typically R_{OFF}>10GΩ). In the ON-state, source and drain electrodes are shorted by the shuttle electrode. The value of R_{ON} is determined by $R_{ON}=2\cdot R_{contact}$, where $R_{contact}$ is the electro-mechanical contact resistance between the shuttle and fixed electrodes (access and shuttle resistance are negligible). Values of metal-metal electro-mechanical contacts are typically in the range of 5Ω to 50Ω for hard metals having a smooth surface [21]. That means a R_{OFF}/R_{ON} ratio as large as 10^8 is achievable, without degradation at high temperature.

The associated parasitic drain to source C_{DS} capacitance is estimated by:

$$C_{DS} = \varepsilon_0 \cdot \frac{L \cdot d_{metal}}{d_{DS}} \qquad (1)$$

where d_{metal} is the thickness of source/drain electrodes and d_{DS} is the gap between electrodes (see Fig. 2). Typical values (L=2µm, d_{metal}=300nm, d_{DS}=200nm) result in C_{DS}~27aF. Such a small value does not impact memory reading.

An anchorless design has unprecedented advantages in terms of reliability and low variability. The absence of flexural (or torsional) anchors makes the scalability of this NEM structure ($9F^2$) remarkable compared to most NEM devices. For example, using a 200nm ½-pitch lithography system results in a density of $700\cdot10^3$ devices/mm^2. A proper NEMS/CMOS addressing scheme must be developed to control shuttle-based NVM arrays, integrated on top of a CMOS chip for cost and density efficiency.

The main challenge to get a small footprint and low-voltage actuation (V_{DD}<1V) resides in the ability to release nanoscale gaps. Anchorless structures have not been widely explored so far. Some noteworthy reports include radio-frequency (RF) switches [20], [22] and a conceptual non-volatile memory based on the free displacement of a guided carbon nanotube [23]. Gravity and shocks are found to be negligible at sub-micron scale, with a shuttle electrode being immune to accelerations up to 10^5g. A disk-shape shuttle is ideal, as it prevents any risk of shuttle gripping inside its cavity.

Only three materials are needed for the integration of the shuttle memory: metal, insulator and a sacrificial material. The whole integration process can be done with a very minimum number of lithographic steps, and at moderate temperature to preserve any underlying CMOS stacks. It is also suggested [6] to properly package under vacuum the device, to make sure air damping does not slow down the shuttle during transitions; and to protect metal contacts from oxidation, dust and humidity.

Shuttle memory bias conditions are listed in Table II.

The shuttle NVM is based on the commuting of a floating (mechanical and electrical) electrode between a bottom fixed electrode (G) and two anchored electrodes (D/S). Forces acting on the shuttle are (i) electrostatic forces, (ii) adhesion forces between the shuttle and fixed electrodes, (iii) damping forces during transients, and (iv) shuttle gravity. Damping is negligible, as the device operates under vacuum.

Switching occurs when the electrostatic force applied to the shuttle overcomes adhesion forces. A pulsed voltage (V_G>0) applied to the gate electrode moves the shuttle down (assuming V_D=V_S=0), while a pulsed voltage applied to both drain and source (V_D=V_S>0) moves the shuttle up (assuming V_G=0). Logic states are shown in Table III. The pulsed mode is needed to avoid the shuttle to operate as an electrostatic oscillator. Drain and source are symmetric to ease circuit design. The stability and switching thresholds of the shuttle memory are presented in Fig. 3. A hysteresis ideally centered at V_G=V_D=V_S=0 ensures the non-volatility of the memory, *i.e.* data retention when the chip is powered off.

B. Adhesion forces and switching threshold

The model presented describes a transition from the UP-state (the shuttle being stuck to both drain and source) to the DOWN-state (the shuttle being stuck to the gate). The separation slit between drain and source electrodes is negligible, compared to the shuttle area. Similarly, fringing fields are neglected in the analytical model. Therefore, the electrostatic force applied to the shuttle (UP-state) towards the gate is expressed as:

$$\boldsymbol{F_{elec}(x=0)=\frac{1}{2}\cdot\frac{\varepsilon_0\cdot A\cdot(V_G-V_{D/S})^2}{(2d_{gap})^2}=\frac{1}{8}\cdot\frac{\varepsilon_0\cdot A\cdot V_G^2}{d_{gap}^2}} \quad (2)$$

The parameter A represents the shuttle planar area, $2d_{gap}$ the vacuum gap (double-air gap structure, see Fig. 2), ε_0 the permittivity of vacuum, and x=0 the initial position of the shuttle ($0<x<2d_{gap}$). When the shuttle is stuck to drain and source, $V_{shuttle}$=V_D=V_S=0. Adhesion forces between the shuttle and fixed electrodes in Eqn. (3) are given in terms of adhesion energy Γ and distance x between the two surfaces in contact, where F_{adh}=0 if $x>d_{vdw}$ and d_{vdw} is approximated to 5nm [24]. The parameter α represents the ratio between real to apparent contact area; this approximation being valid for smooth surfaces. The exact *Force–Energy* adhesion plot is highly experimental and usually extracted from atomic force microscopy (AFM) *Force–Stiction* plots [24].

$$\boldsymbol{F_{adh}(0<x<d_{vdw})=\frac{2\Gamma\cdot A\cdot\alpha}{d_{vdw}}\cdot\frac{d_{vdw}-x}{d_{vdw}}} \quad (3)$$

To confirm this value, AFM scan of a physical vapor deposition (PVD) of tantalum nitride (TaN) layer was conducted. The surface is very smooth (D_{rms}=0.4nm) and ideal for electro-mechanical contacts. Adhesion energy of Γ=33mJ/m^2 is extracted from the AFM scan, where A_{TaN} is the Hamaker constant of TaN:

$$\Gamma = \frac{A_{TaN}}{12 \cdot \pi \cdot D_{rms}^2} \quad (4)$$

This corresponds to $F_{adh}(x=0,\alpha=1)=13\cdot10^3$ [N/m^2], in good accordance with other published reports, see for example [25]. The force is $F_{adh}(x=0,\alpha=1)=52\cdot10^{-9}$ [N] for a shuttle area of A=4μm^2.

Gravity (weight) of the shuttle is shown in Eqn. (5), where $d_{shuttle}$ represents the thickness of the shuttle, and ρ is the density of metal. Using metrics in Table I, $F_{gravity}=2\cdot10^{-13}$ [N].

$$F_{gravity} = (\rho \cdot A \cdot d_{shuttle}) \cdot g \quad (5)$$

From Eqns. (2) to (4), the minimum switching voltage V_P needed to pull the shuttle out of adhesion can be extracted. First, gravity is at least 4 to 5 order of magnitude smaller than the adhesion force needed to initiate switching, demonstrating the robustness of the anchorless design. Second, adhesion force very quickly decreases (contact opening) after pull-out, while electrostatic actuation increases (gap reduction). Last, all three forces (electrostatic, adhesion, and gravity) have similarly a linear dependence with the shuttle surface A. That means the switching voltage V_P does not depend from the actuation area A. This is an unusual result for most electrostatic MEMS devices, but of great interest for device scaling. The switching voltage V_P expression is in Eqn. (6) and plotted in Fig. 4.

$$V_P = 4d_{gap} \cdot \sqrt{\frac{\Gamma \cdot \alpha}{d_{vdw} \cdot \varepsilon_0}} \quad (6)$$

C. Shuttle static analysis

This section describes the static analysis of the shuttle electrode in vacuum. Once the shuttle has lifted off, it *flies* until it eventually reaches the opposite electrode. The study is conducted for a transition from drain/source side towards the gate. When a positive bias V_G is applied to the gate ($V_{D/S}$=0), the shuttle is charged. If the applied voltage V_G is higher than the pull-out (switching) voltage V_P, then the shuttle lifts off and carries a net charge $Q_{shuttle}$ until it reaches the opposite electrode. Gate voltage actuation needs to be turned off during the shuttle flight, or the shuttle would be charged by an opposite charge $-Q_{shuttle}$ when landing and rebound towards its initial position. This effect, which is not desirable for memory application, is reported as *electrostatic pendulum* [26].

The model is based on charge distribution over the surface of metal electrodes, as shown in Fig. 5. The net charge on the shuttle splits between the top and bottom interface, and its redistribution depends on both the external applied voltages and the shuttle position ($0<x<2d_{gap}$).

From the charge conservation on the shuttle and the electrostatic law of a capacitor Q=C·V (in this case, two air-gap capacitors), the charge equilibrium system is:

$$\begin{cases} q_D = q_S \\ q_D + q_S + q_{top} = 0 \\ q_{bottom} + q_G = 0 \\ q_{top} + q_{bottom} = Q_{shuttle} \\ q_G = -q_{bottom} = \dfrac{\varepsilon_0 \cdot A}{(2d_{gap} - x)} \cdot (V_G - V_{SHUTTLE}) \\ q_{top} = -q_D - q_S = \dfrac{\varepsilon_0 \cdot A}{x} \cdot (V_{SHUTTLE} - V_{D/S}) \end{cases} \quad (7)$$

The net charge on the shuttle depends on its initial charging, as written in Eqn. (8).

$$Q_{shuttle} = Q = \frac{\varepsilon_0 \cdot A}{2 \cdot d_{gap}} \cdot V_G \quad (8)$$

The model was verified by FEM simulation [27], with a charged shuttle placed between fixed electrodes, see Fig. 6(a). Both charge induction over surfaces and shuttle charge splitting between top and bottom interfaces are observed. A charge distribution cross-section is extracted in Fig 6(b).

As a result, two electrostatic forces, named F_{up} (towards D/S) and F_{down} (towards gate) build up during the switching, see Eqn. (9). One force (F_{up}) operates as a *break*, while the other (F_{down}) acts as a *motor* for switching.

$$\begin{cases} F_{up} = \dfrac{q_{top}^2}{2 \cdot \varepsilon_0 \cdot A} = \dfrac{(q_D + q_S)^2}{2 \cdot \varepsilon_0 \cdot A} \\ F_{down} = \dfrac{q_{bottom}^2}{2 \cdot \varepsilon_0 \cdot A} = \dfrac{q_G^2}{2 \cdot \varepsilon_0 \cdot A} \end{cases} \quad (9)$$

From Eqns. (7) to (9), the evolution of the two electrostatic forces (F_{up} and F_{down}) as a function of the shuttle position is extracted and plotted (see Fig. 7). The difference between the analytical solution and FEM results (8%) is due to corner/edge effects, which are not captured by the analytical model. This discrepancy induces a higher FEM charge density than predicted by equations, therefore increasing both F_{up} and F_{down}.

In this static analysis example, V_G pulse is turned-off at x=100nm, which corresponds to the middle of the course. We observe from Fig. 7, that even with the condition V_G=V_D=V_S=0, F_{up} and F_{down} forces are non-zero, due to the fixed shuttle charge. Figure 8 shows the evolution of the induced shuttle voltage, with an abrupt change at x=100nm.

D. Shuttle dynamic analysis

The time-dependent control of the gate voltage follows the time diagram shown in Fig. 9. To avoid an electrostatic rebound of the shuttle, the switching is divided between an *accelerated flight* (V_G>0, V_D=V_S=0) and a *free flight* (V_G=0, V_D=V_S=0).

Dynamic equation is solved from Newton's second law of motion. The two forces applied to the shuttle are F_{up} and F_{down}, and the resulting equation is as followed, where m is the shuttle mass:

$$m \cdot \frac{d^2x(t)}{dt^2} = \frac{q_{bottom}^2}{2 \cdot \varepsilon_0 \cdot A} - \frac{q_{top}^2}{2 \cdot \varepsilon_0 \cdot A} \quad (10)$$

Using values from Eqn. (7), Eqn. (10) can be solved analytically. Eqn. (10) is a 2nd order differential equation and has a single physical solution. In Eqn. (11), a K-factor is used as a substitution coefficient. Motion equation (12) is valid for any value of applied voltages, including $V_{D/S} \neq 0$. Eqn. (13) is the first derivative of Eqn. (12) and represents the shuttle speed. Initial conditions for position and speed are $x(t_0)$ and $v(t_0)$, respectively.

$$K = \sqrt{2 \cdot A \cdot \varepsilon_0 \cdot d_{gap} \cdot m} \quad (11)$$

$$x(t) = \frac{1}{Q}(d_{gap} \cdot Q + A \cdot \varepsilon_0(-V_{D/S} + V_G) + [-d_{gap} \cdot Q + A \cdot \varepsilon_0(V_{D/S} - V_G) + Q \cdot x(t_0)] \cdot Cosh(\frac{Q \cdot t}{K}) + K \cdot v(t_0) \cdot Sinh(\frac{Q \cdot t}{K})) \quad (12)$$

$$\frac{dx(t)}{dt} = v(t) = v(t_0) \cdot Cosh(\frac{Q \cdot t}{K}) + \frac{-d_{gap} \cdot Q + A \cdot \varepsilon_0(V_{D/S} - V_G) + Q \cdot x(t_0)}{K} \cdot Sinh(\frac{Q \cdot t}{K}) \quad (13)$$

As shown in Fig. 9, shuttle flight is divided into two phases. At $t=t_1=T_{pulse}$, gate voltage must be switched off. Therefore, the relation between landing time t_2 and turn-off time t_1 is solved and presented in Eqn. (15), with Eqn. (14) as substitution. $x_1=x(t_1)$ and $v_1=v(t_1)$ represent shuttle position and speed at $t=t_1$, respectively.

$$\kappa = \frac{d_{gap} \cdot Q^2 \cdot (-d_{gap} + x_1) + \sqrt{K^2 v_1^2 (K^2 v_1^2 + Q^2 \cdot (2d_{gap} - x_1) \cdot x_1)}}{d_{gap}^2 \cdot Q^2 + K^2 \cdot v_1^2} \quad (14)$$

$$t_2 = t_1 - \frac{K}{Q} \cdot Arc\sec h(\kappa) \qquad 0 < \kappa \leq 1 \quad (15)$$

From Eqn. (12), the position of the shuttle as a function of time is plotted. Curves are shown in Fig. 10. There is a given range for proper V_G pulse duration. If the pulse is too short, then the shuttle would go back to its initial position; if the pulse is too long, then the shuttle would experience an electrostatic rebound.

The dynamic analysis is done with the assumption that charge redistribution over various surfaces of the shuttle electrode is faster than its own mechanical displacement.

E. Switching speed and switching energy

Switching time and switching energy, as a function of T_{pulse} duration are reported in Fig. 11.

The switching energy corresponds to the kinetic energy of the shuttle $1/2mv^2$, where m is the shuttle mass, and $v=v(t_2)$ the shuttle speed on landing ($v(t_2)$=1.3nm/ns if no V_G turn-off is applied). Without V_G turn-off, the calculated kinetic energy equals the

initial charging energy of the shuttle-to-gate capacitor:

$$\frac{1}{2} m \cdot v(t_2)^2 = \varepsilon_0 \cdot \frac{A}{2d_{gap}} \cdot V_G^2 \qquad (16)$$

If V_G is turned-off during switching, then a part of the initial charging energy is returned to power supplies (S, D, G).

III. Conclusion

This paper presents a new non-volatile NEM memory device, called the shuttle memory. It consists of a floating metal electrode guided inside a pod cavity, which is actuated by electrostatic forces and has two stable positions. Permanent data retention is obtained by adhesion forces only, which eliminates leakage current and predicts good reliability at high temperature. Furthermore, the anchorless geometry provides better compactness compared to planar MEMS memories, and does not suffer from elastic fatigue or thermal drifts.

A complete analytical model based on Newton's equation of motion is derived, and validated by FEM simulations. This memory must be controlled by a pulsed mode to avoid a pendulum effect. Further development should include MEMS/CMOS NVM arrays design and detailed analysis of shuttle fabrication parameters.

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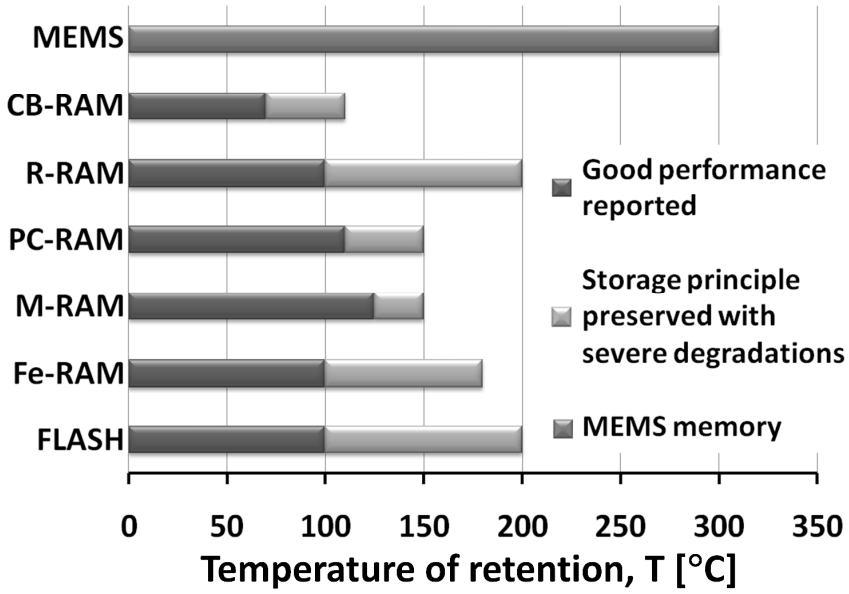


Fig. 1. Maximum temperature of operation for various types of non-volatile memories. This review is based on recently published papers, constrains are more stringent for commercial memories.

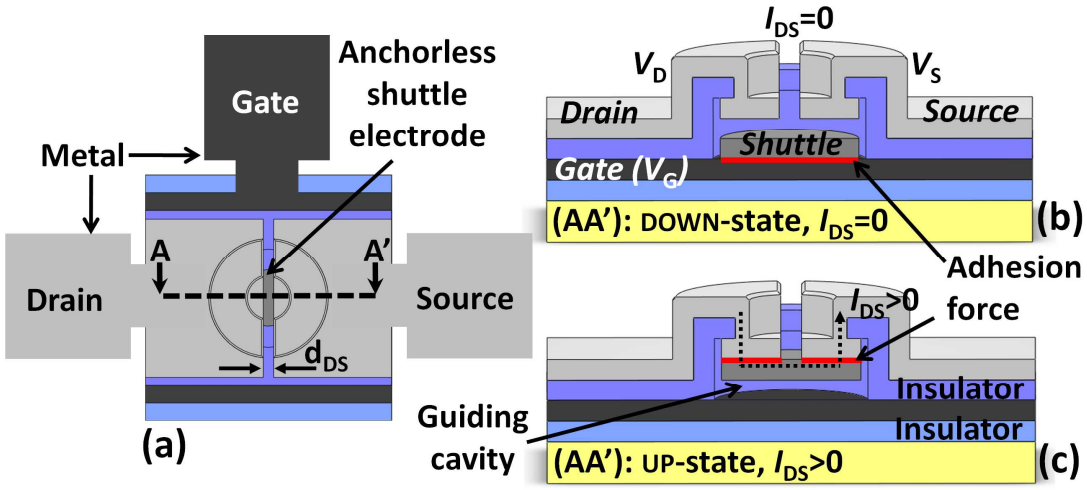


Fig. 2. (a) Top-view layout of the 3-terminal NEM memory. AA' 3D cross sections in the DOWN (b) and UP (c) states. Memory reading is done by V_{DS} bias and current reading: I_{DS}=0 in DOWN-state, and I_{DS}>0 in UP-state.

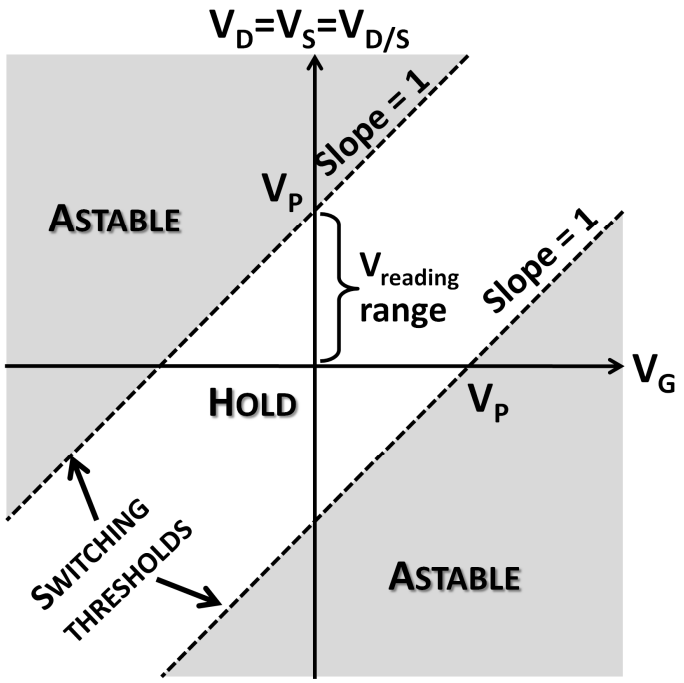


Fig. 3. Stability and switching thresholds of the shuttle NVM. A hysteresis ideally centered at $V_D=V_S=V_G=0$ ensures that data are properly stored when the device is powered off.

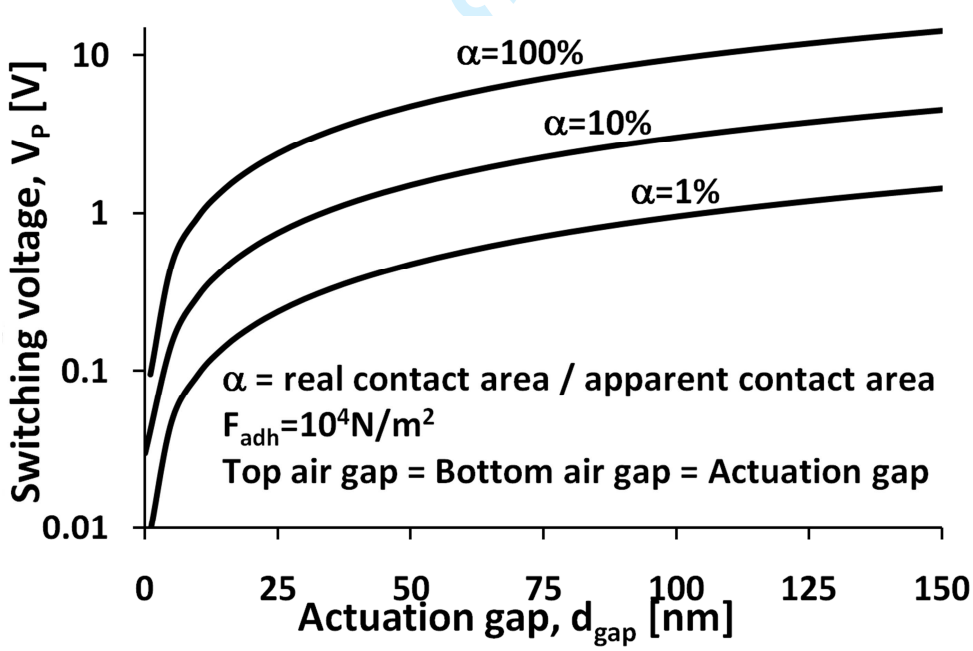


Fig. 4. Switching pull-out voltage V_P (log-scale) *vs.* actuation gap d_{gap}. Sub-25nm actuation gaps are typically needed for low-voltage actuation. Switching voltage does not depend on shuttle area A.

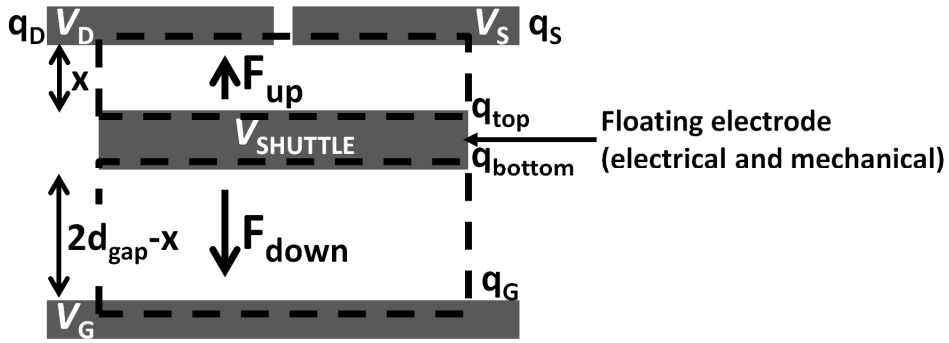


Fig. 5. Double air gap capacitor divider with charge distribution. While switching, the shuttle electrode carries a constant charge.

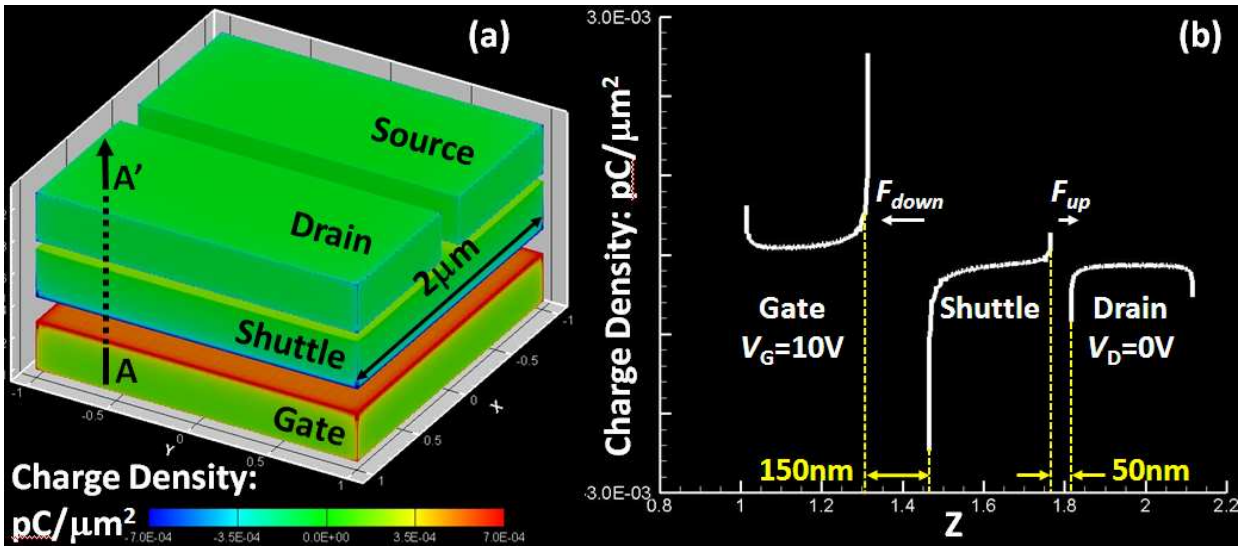


Fig. 6 (a) FEM charge density simulation of a charged conductive shuttle placed between fixed drain, source, and gate electrodes. Bias conditions are V_D=V_S=0 and V_G=10V, and shuttle position is x=50nm ($2d_{gap}$-x=150nm). Corner effects inducing extra charges are visible on electrode edges. (b) AA' cross section of the charge density distribution. The surface charge distribution inducing electrostatic forces F_{down} and F_{up} are visible.

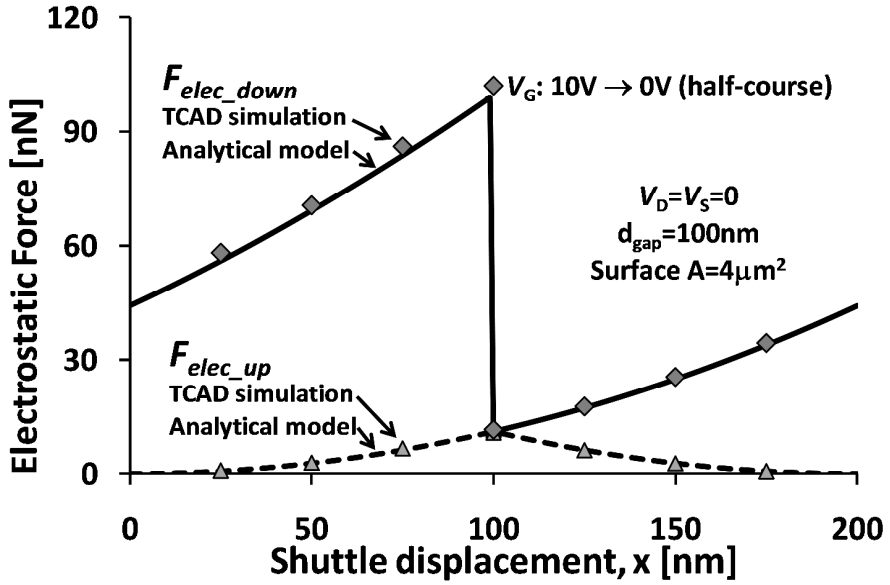


Fig. 7. Analytical modeling of electrostatic forces F_{down} (shuttle → gate) and F_{up} (shuttle → drain/source) *vs.* shuttle displacement. V_G-pulse turn-off is applied after shuttle ½-course. Solid markers represent TCAD solutions.

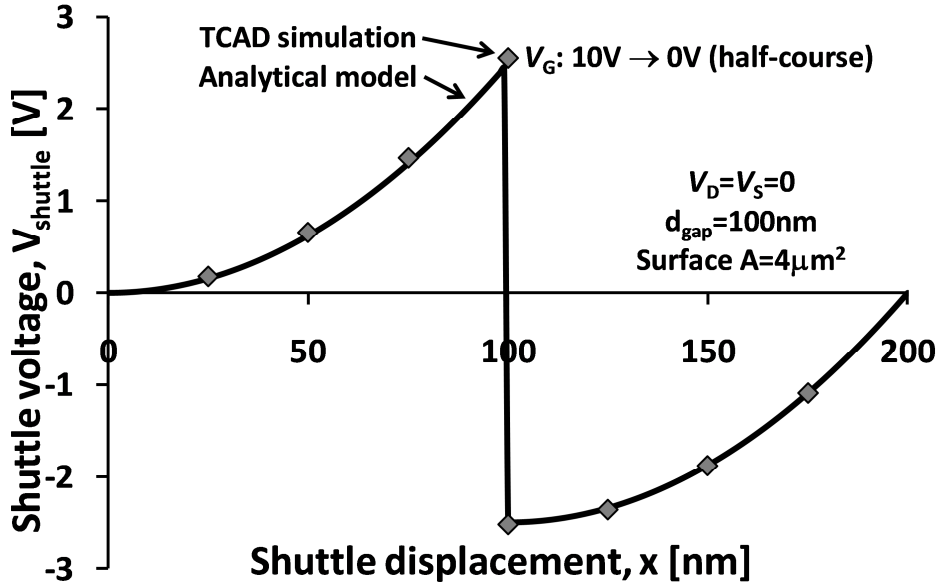


Fig. 8. Evolution of the shuttle voltage during switching. V_G-pulse turn-off is applied after shuttle ½-course. Solid markers represent TCAD solutions.

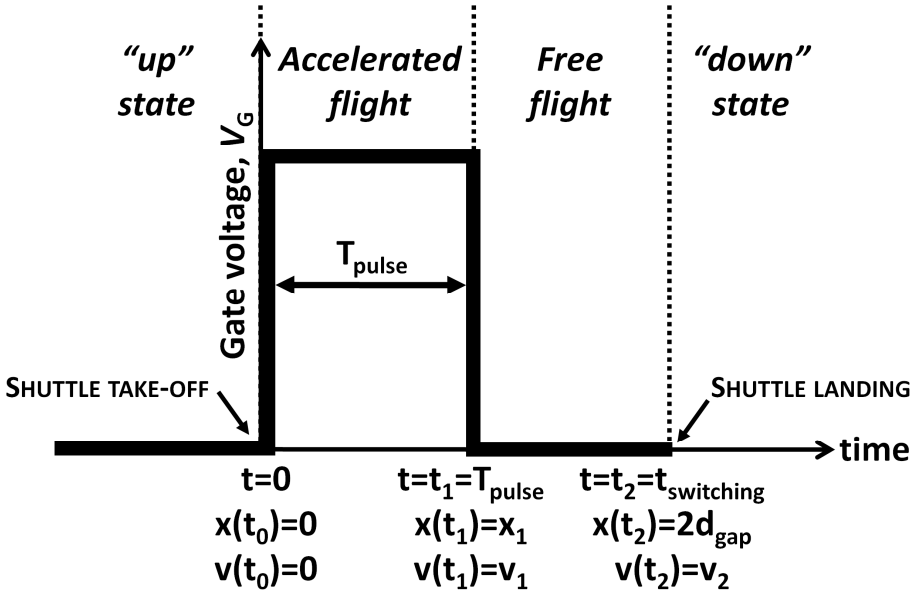


Fig. 9. Transient details of the pulsed-mode switching, simulating a transition from the "UP" state to the "DOWN" state. In order to avoid rebound of the shuttle, the switching of the electrode must be divided into an "accelerated" flight phase and a "free" flight phase.

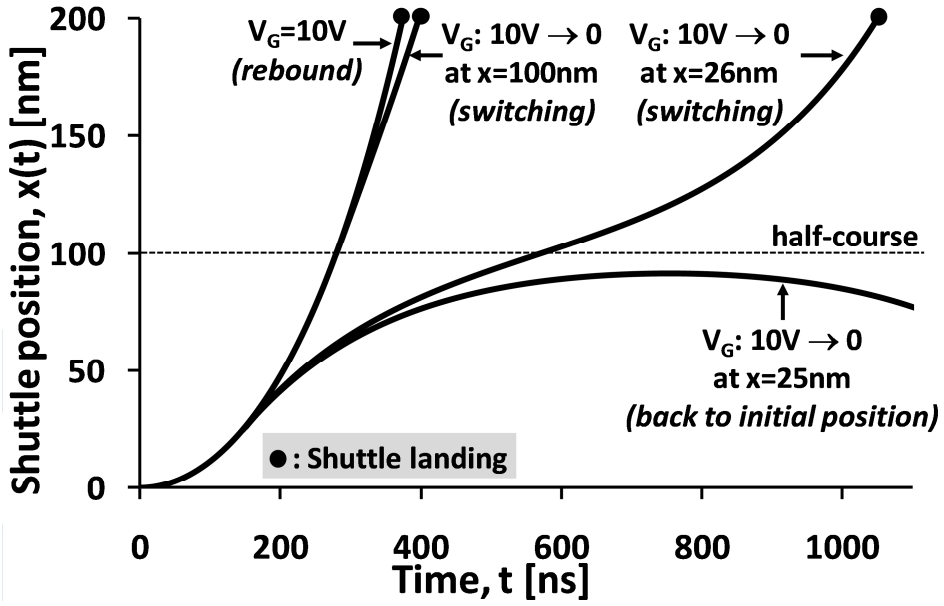


Fig. 10. Position of the shuttle electrode as a function of time. Depending on the duration of the V_G pulse, three cases could happen: (i) the shuttle back to its initial position if pulse duration is too short, (ii) proper switching or (iii) shuttle electro-mechanical rebound if the pulse is too long.

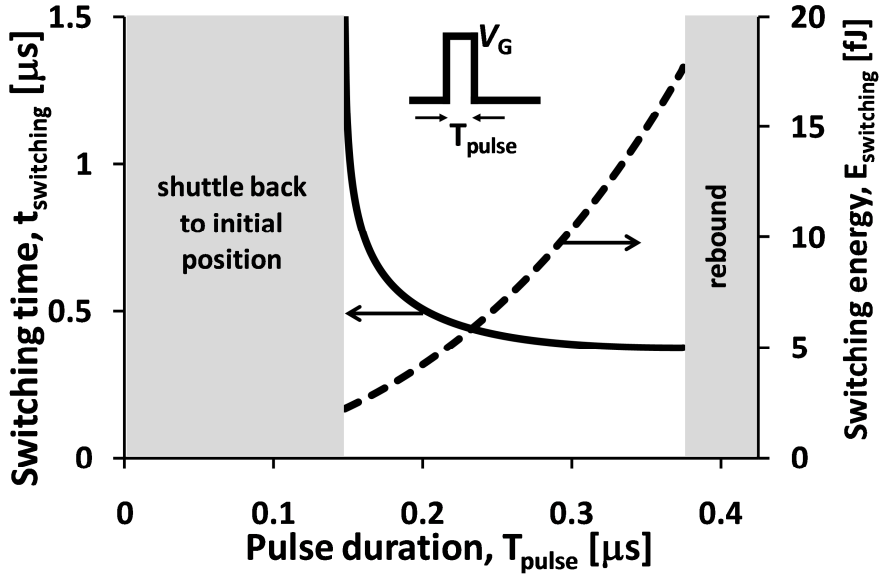


Fig. 11. Switching time and switching energy plots, as a function of V_G pulse duration.

TABLE I
INDEX OF MODEL PARAMETERS.

Symbol	Quantity	Value
ε_0	dielectric constant of vacuum	$8.854 \cdot 10^{-12}$ F/m
g	gravitational acceleration	9.81 m/s^2
A	shuttle surface	2µm x 2µm = 4µm^2
L	shuttle length	2µm
$d_{shuttle}$	shuttle thickness	300nm
ρ	shuttle metal density (TaN)	$16.6 \cdot 10^3$ kg/m^3
m	shuttle mass	$2 \cdot 10^{-14}$ kg
d_{gap}	vacuum actuation gap	100nm
d_{DS}	drain-source slit gap	200nm
d_{metal}	drain-source metal thickness	300nm
d_{vdw}	Van der Waals distance	5nm
x	shuttle displacement	$0<x<2d_{gap}$
A_{TaN}	Hamaker constant of TaN	$20 \cdot 10^{-20}$ J
Γ	TaN-TaN adhesion energy	33mJ/m^2
α	real/apparent contact area	0.1%

TABLE II
INDEX OF STIMULUS AND MODEL PARAMETERS.

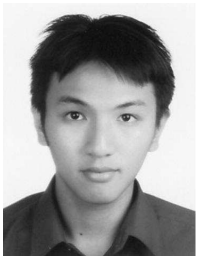
Symbol	Quantity	Value
V_D	applied drain voltage	0
V_S	applied source voltage	0
$V_{D/S}$	applied drain and source voltage	$V_{D/S}=V_D=V_S=0$
$V_{shuttle}$	shuttle voltage	floating
V_G	applied gate voltage amplitude (pulsed-mode)	10V
V_P	pull-out voltage	
V_R	reading voltage	$V_R<<V_P$
$R_{contact}$	metal-metal contact resistance	
R_{ON}	drain-to-source resistance (shuttle in the up-state)	$R_{ON}=2\cdot R_{contact}$
R_{OFF}	drain-to-source resistance (shuttle in the down-state)	
$Q_{shuttle}$	fixed shuttle charge	$-1.78\cdot10^{-15}$ C
q_{top}	induced charge on shuttle top interface	
q_{bottom}	induced charge on shuttle bottom interface	
q_D	induced drain charge	
q_S	induced source charge	
q_G	induced gate charge	
F_{up}	electrostatic force shuttle → drain/source	
F_{down}	electrostatic force shuttle → gate	
T_{pulse}	gate voltage pulse duration	
t_0	gate voltage turn-on time $0\rightarrow V_G$	$t_0=0$
t_1	gate voltage turn-off time $V_G\rightarrow0$	$t_1=T_{pulse}$
t_2	shuttle landing time	

TABLE III
OPERATING PRINCIPLE OF THE NVM DEVICE.

Logic	Applied voltage	Effect
Switching down	$V_D=V_S=0$ $V_G=V_P$ (pulse)	V_P: Pull-out voltage $F_{down}>F_{adhesion}$
Switching up	$V_D=V_S=V_P$ (pulse) $V_G=0$	Switching to both drain and source. $F_{up}>F_{adhesion}$
Read	$V_D=V_R$, $V_S=0$ $V_G=0$	V_R: Read voltage ($V_R<<V_P$) down-state: $I_{DS}=0$ up-state: $I_{DS}>0$ $I_{DS}\cong V_{DS}/2\cdot R_C$
Hold	$V_D=V_S=V_G=0$	Non-volatility: adhesion increases with temperature

Vincent Pott obtained both the M.S. degree in micro-technology and the Ph.D. degree in electrical engineering from the Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland, in 2002 and 2008, respectively. From 2008 to 2010, he was with the University of California, Berkeley, as post-doctoral associate. In 2010, he joined the Institute of Microelectronics (IME), Agency for Science, Research, and Technology (A*STAR), in Singapore. He currently holds a project leader position and works on various projects related to energy-efficient computing and high-temperature data storage.

Dr Pott serves as reviewer in various IEEE journals and (co-)authored around 60 publications. His current research interests include micro and nano technology fabrication, MEMS, NEMS, nanowires and hybrid technologies.



Geng Li Chua was born in Singapore in Jan. 1987. He is currently pursuing a Bachelor Degree in Electrical & Electronics Engineering at National University of Singapore. He was on Industrial Attachment programme with the Institute of Microelectronics (IME), Agency for Science, Research, and Technology (A*STAR), Singapore, from January to June 2011. He is involved in research activities that focus on high temperature operating nano-electro-mechanical devices.

Mr. Chua interests include novel computation and data storage systems for tomorrow sustainability of information technology.

Ramesh Vaddi received the B.Tech degree in Electronics and Communication Engineering from M. V. G. R. College of Engineering, Vizianagaram (Affiliated to J.N.T.U Hyderabad), India in 2002 and M. Tech degree in Energy Engineering from Maulana Azad National Institute of Technology, Bhopal, India in 2004. He has obtained his Ph.D. degree in Electronics and Computer Engineering (Microelectronics and VLSI Group) from Indian Institute of Technology Roorkee, India in 2011.

From 2004 to 2005, he was as a Lecturer in MANIT, Bhopal, India and 2005-2007, he was an Assistant Professor in the Department of ECE, GITAM University, Visakhapatnam, India. He is currently working as a Postdoctoral Fellow with Nanyang Technological University, Singapore. He has been involved in the design of ultra-low power interface circuits for energy harvesting sources and NEMS based NVM.

Dr Ramesh Vaddi serves as reviewer in various IEEE journals and (co-) authored around 25 publications.

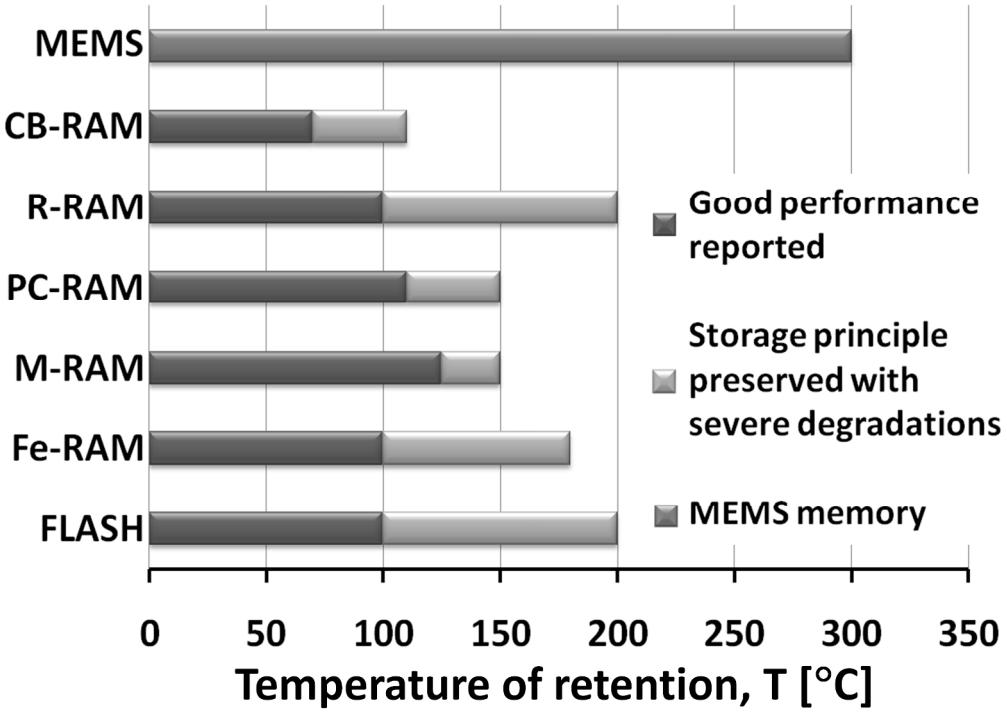
Julius Ming-Lin Tsai received the B.S. and Ph.D. degrees in power mechanical engineering from National Tsing Hua University, Hsin-Chu, Taiwan, in 1995 and 2004, respectively. From June 2003 to April 2004, he was a visiting scholar with Carnegie–Mellon University, Pittsburgh, PA, where he was involved with low-noise CMOS accelerometers. From 2004 to 2009 he joined VIA Technologies, where he was involved with high-frequency small-signal modeling.

He is now a principle investigator in Institute of Microelectronics (IME), Singapore and an adjunct assistant professor with the National University of Singapore. His main research interests are in RF-MEMS, NEMS switches and MEMS ultrasound transducers.

Tony T. Kim received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He received the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, Minnesota, USA, in 2009.

He joined the Device Solution Network Division, Samsung Electronics, Yong-in, Korea, in 2001. From 2001 to 2005, he performed research on the design of high-speed SRAM memories. In summer 2007 and 2008, he was with IBM T. J. Watson Research Center, Yorktown Heights, NY, where he worked on NBTI/PBTI-induced circuit reliability measurement circuits. In summer 2009, he was an intern at Broadcom where he performed research on ultra-low power SRAM design. Since November 2009, he has been an assistant professor with Nanyang Technological University, Singapore. His research interests include ultra-low power and high performance integrated circuits including low voltage circuits, silicon and non-silicon memories, and energy efficient circuits and systems.

Prof. Kim is the recipient of the 2008 AMD/CICC Student Scholarship Award, 2008 DAC/ISSCC Student Design Contest Award, 2008 Departmental Research Fellowship from University of Minnesota, 2008 Samsung Humantec Thesis Award (2008, 2001, and 1999), and 2005 ETRI Journal Paper of the Year Award.



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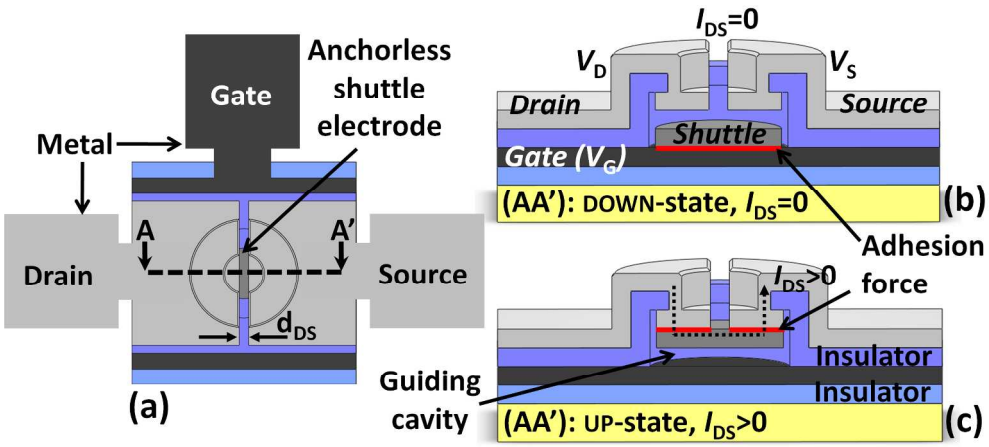

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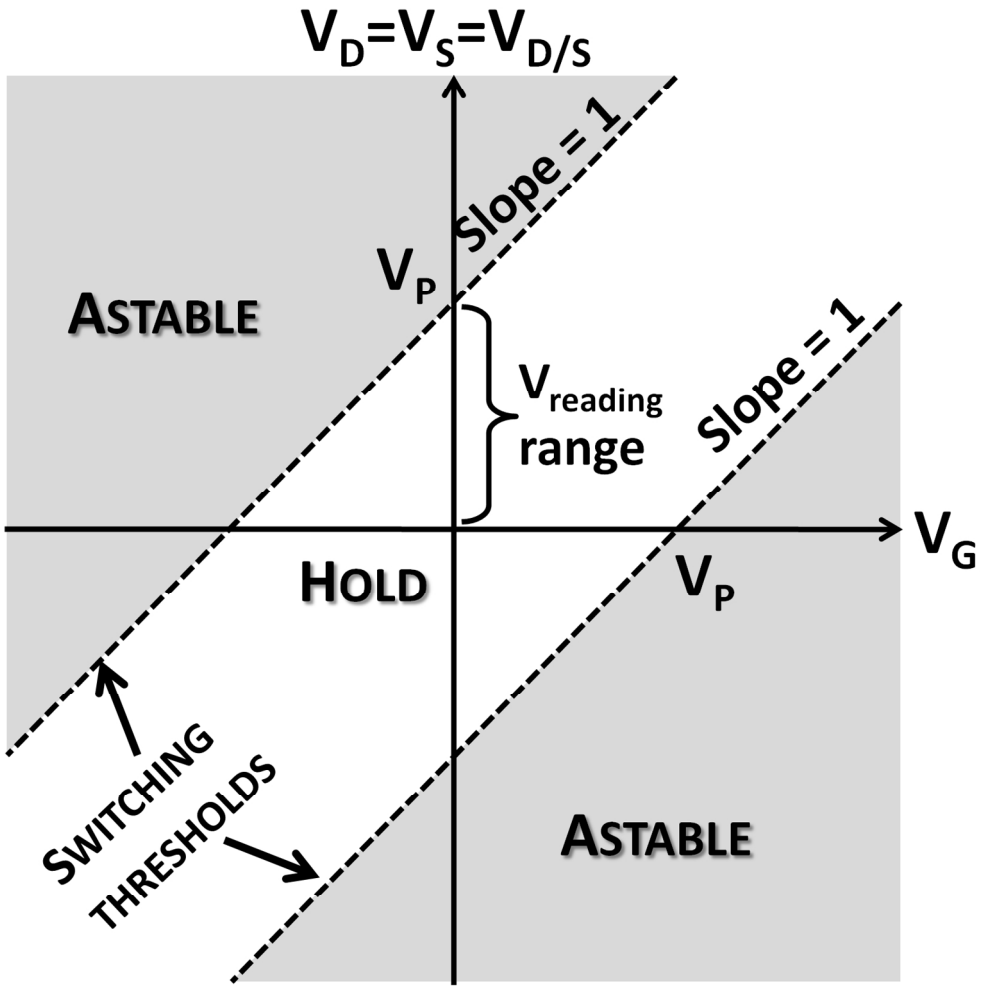

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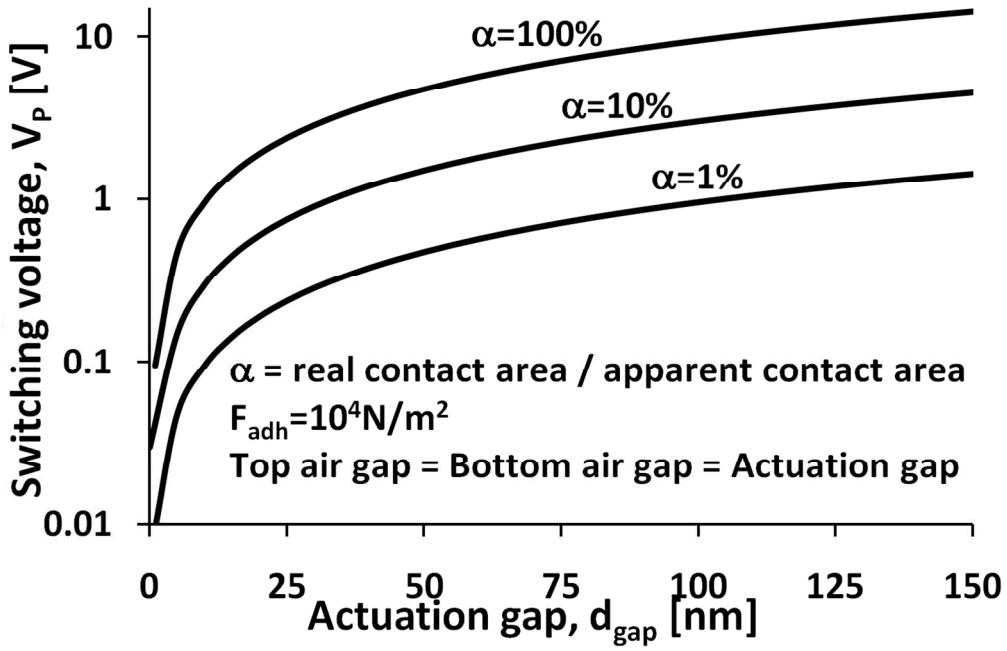

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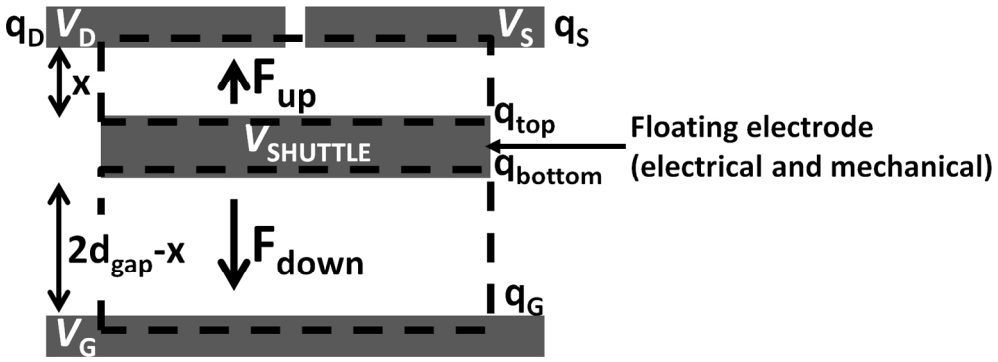

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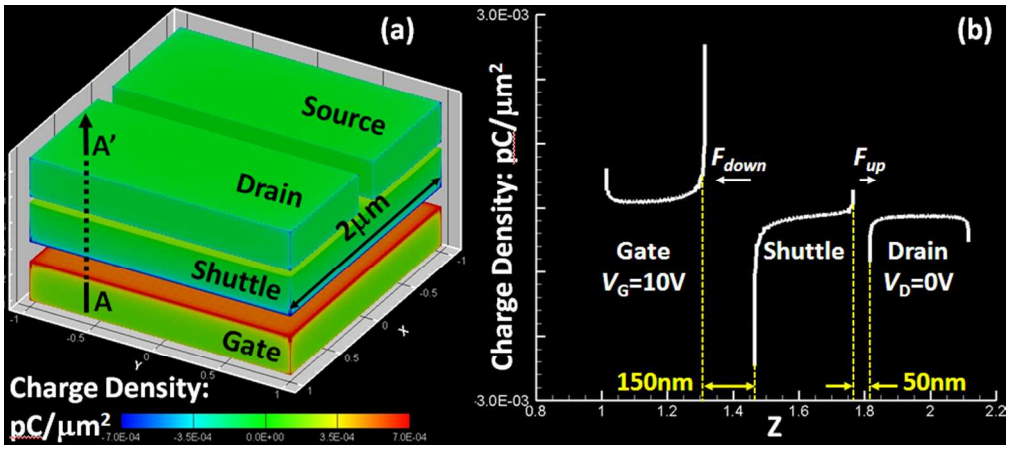

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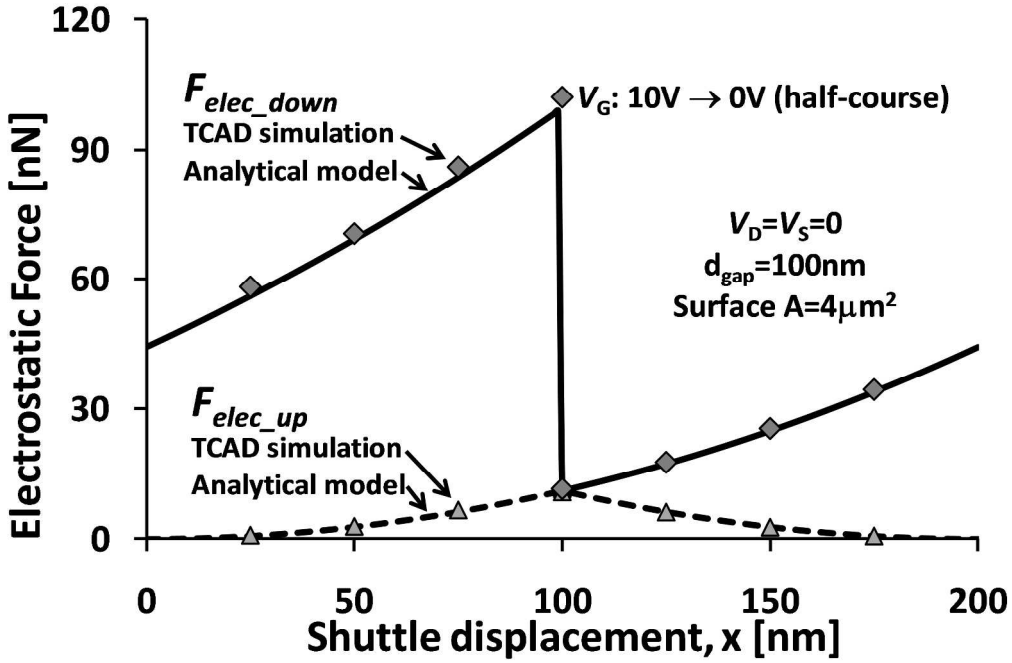

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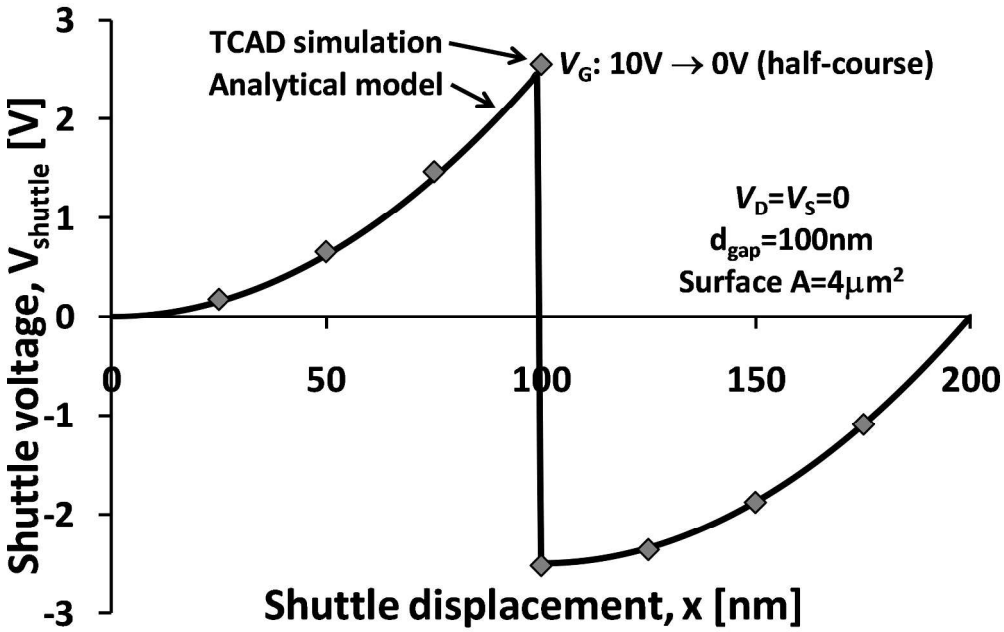

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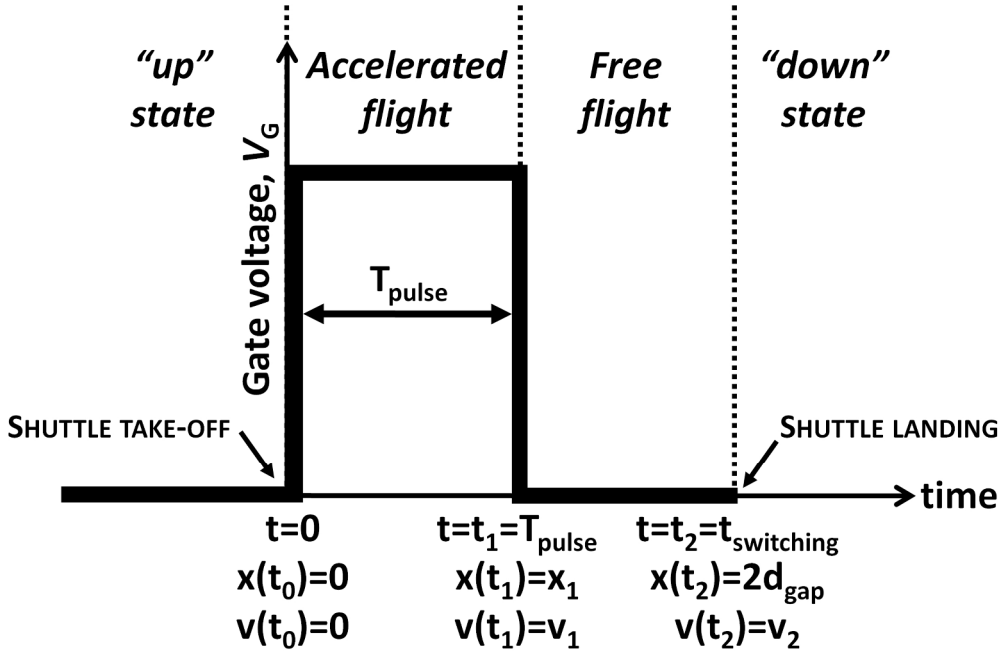

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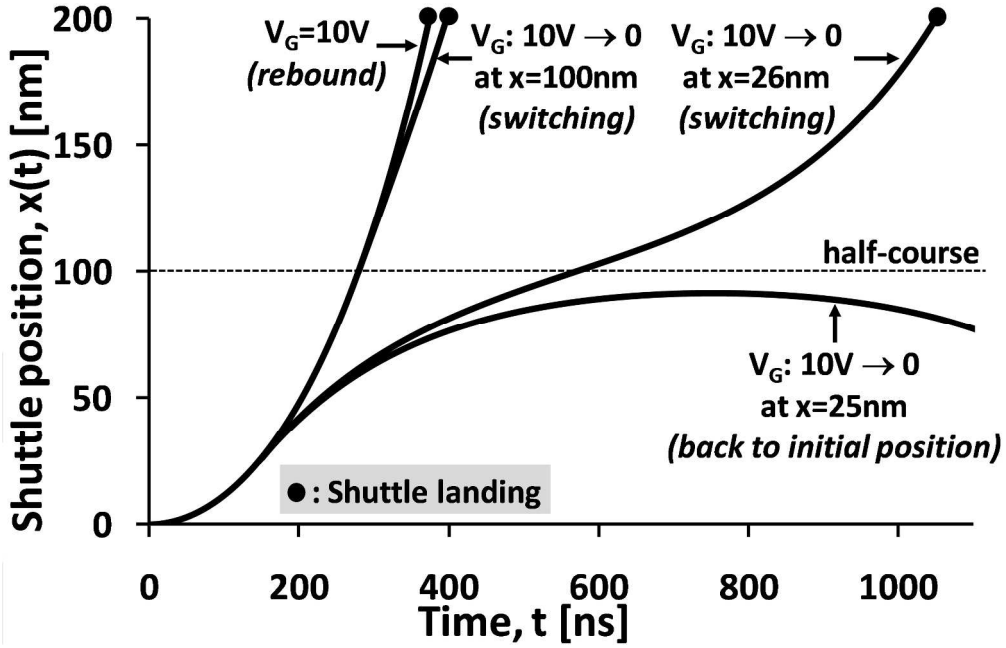
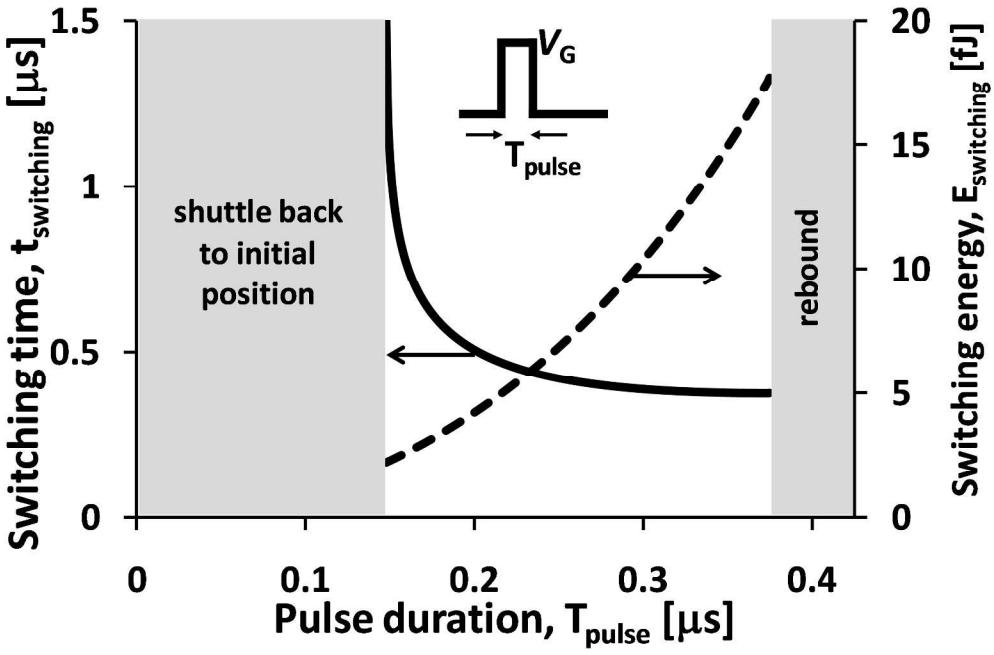


249x159mm (284 x 284 DPI)



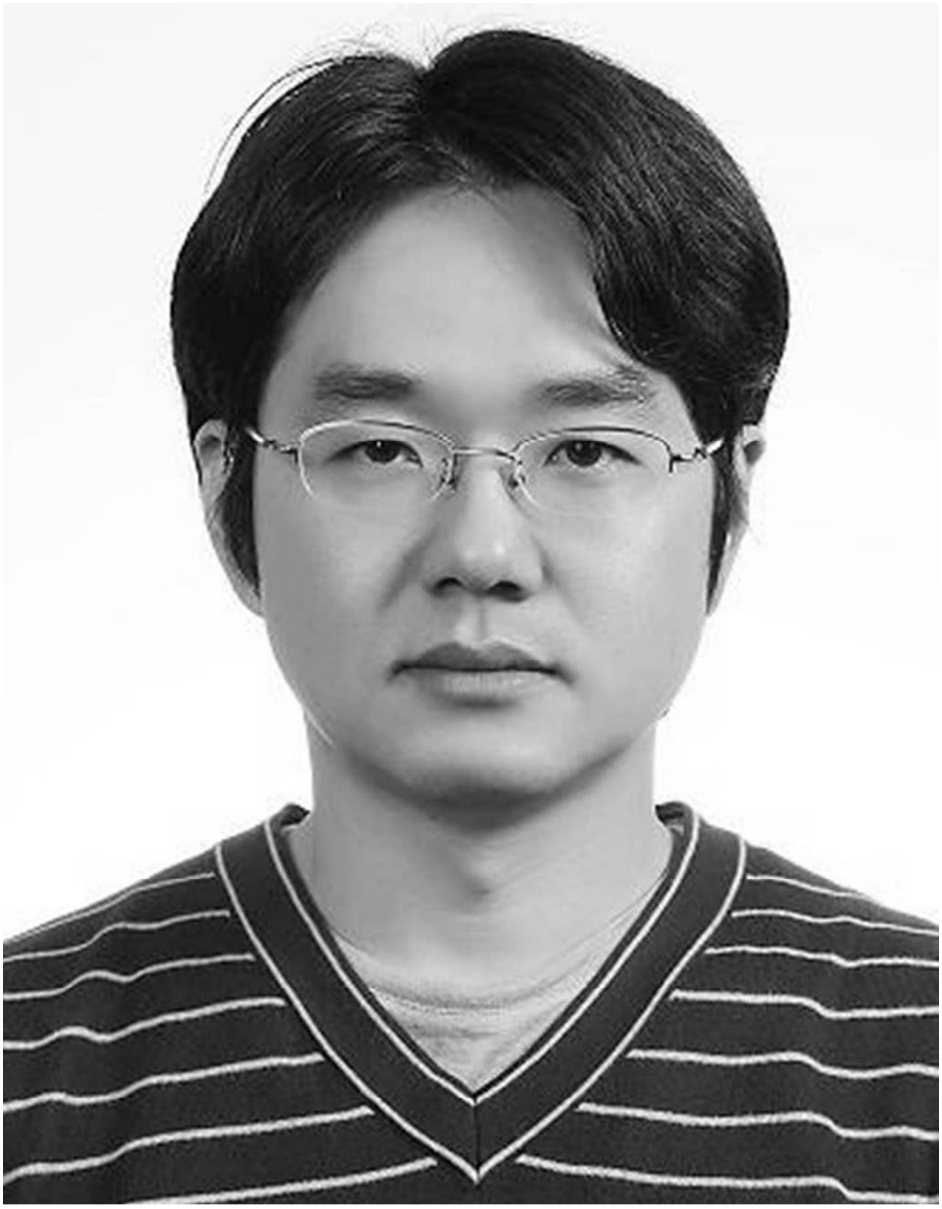
231x154mm (300 x 300 DPI)

46x63mm (300 x 300 DPI)

96x126mm (96 x 96 DPI)

90x112mm (300 x 300 DPI)

41x52mm (300 x 300 DPI)



87x111mm (300 x 300 DPI)