OPERATION AND EFFICIENCY IMPROVEMENTS OF A HYBRID DUAL-ACTIVE-BRIDGE CONVERTER FOR ENERGY STORAGE SYSTEMS

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in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Prof. Josep Pou

Authorship Attribution Statement

This thesis contains material from one paper published in the following peer-reviewed journal, and from three papers accepted at conference in which I am listed as an author.

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The contributions of the co-authors are as follows:

- Prof Josep Pou provided invaluable guidance in defining the initial project direction.
- I prepared the manuscript drafts. The manuscript was revised by Prof. Josep Pou, Dr. Changjiang Sun and Dr. Zhan Li.
- I designed the experiment and performed all the laboratory work at the Rolls Royce @ NTU corporate lab. Additionally, I thoroughly analyzed the resulting data.
- Assist. Prof. Xin Zhang assisted in the implementation of controller algorithm into FPGA based model.
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The contributions of the co-authors are as follows:

- Prof. Josep Pou played a crucial role in providing invaluable guidance to establish the initial project direction.
- I took responsibility for drafting the manuscript and carried out revisions in collaboration with Prof. Josep Pou and Dr. Xinze Li.
- I managed all communication and correspondence related to the article and represented all authors in the process of signing the publishing agreement.
- Dr. Xinze Li actively contributed by co-designing the experiments and conducting laboratory work at the Rolls Royce @ NTU corporate lab.
- Mr. Yu Zeng made significant contributions by offering valuable suggestions and enhancing the project's methodology, particularly in addressing controllability issues.
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- Prof Josep Pou provided invaluable guidance in defining the initial project direction.
- Dr Xinze Li prepared the manuscript drafts. I revised the manuscript with Prof. Josep Pou and Dr. Fanfan Lin.
- I handled all correspondence related to the article and represented all authors in signing the publishing agreement.
- I co-designed the experiment and performed the laboratory work at the Rolls Royce @ NTU corporate lab.
- Prof Changyun Wen offered suggestions and enriched the project's methodology specifically on controllability issues.
- Dr. Suvajit Mukherjee provided support in acquiring the required measurement equipment.
- Assist Prof. Xin Zhang assisted in the placement of hardware within the Rolls Royce @ NTU corporate lab.

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Their support and encouragement have been instrumental in my success, and I dedicate this thesis to them with love and appreciation.

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Summary

This thesis focuses on optimizing the operation and efficiency of the dual-active-bridge (DAB) converter for high-power energy storage systems.

A novel DAB-based topology and some modulation strategies are proposed and thoroughly investigated in Chapter 2. The hybrid neutral-point-clamped (NPC) modules in the DAB converter topology utilize Si IGBTs and SiC MOSFETs to reduce power losses while maintaining a cost-efficiency balance.

A new modulation method is introduced in Chapter 3, applying different switching schemes for the SiC MOSFETs and the Si IGBTs in the hybrid NPC DAB converter. This design effectively utilizes the neutral current path and significantly reduces conduction and switching losses. Experimental comparisons demonstrate higher efficiency of the proposed hybrid duty ratio phase-shifted modulation (PSM) .

To address modelling challenges, a novel data-driven modelling with experimental augmentation (D^2EA) is proposed in Chapter 4, combining simulation and experimental data to improve accuracy. The D2EA achieves an efficiency modelling accuracy of 99.92% and is validated in 2-kW hardware experiments, reaching a peak efficiency of 98.45%.

Chapter 5 presents an artificial intelligent- (AI-) based control method to optimize zero-voltage zero-current (ZVZCS) operation and improved efficiency performance. The hybrid NPC DAB converter demonstrates superior efficiency under various load conditions compared to conventional triple-phase-shifted (TPS) modulation.

This research offers valuable insights into optimizing DAB converters, introducing novel strategies and control methods. The proposed D2EA approach and AI-based optimization show promise in advancing power converter modeling and efficiency, paving the way for future high-power energy storage system applications.

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Nomenclature

AC	alternating current
ANPC	active neutral point clamped
BESS	battery energy storage systems
CDOF	control dimensions of freedom
DAB	dual active bridge
DC	direct current
D^2EA	data-driven modeling with experimental augmentation
DPS	dual phase shift
DRM	duty ratio modulation
EPS	extended phase shift
ESS	energy storage systems
FM	frequency modulation
NPC	neutral point clamped
PSM	phase-shift modulation
PSO-SAVL	particle swarm optimization with state-based adaptive velocity limit
PWM	pulse width modulation
Si	silicon
SiC	silicon-carbide
SoC	state of charge
SPS	single phase shift
SPWM	sinusoidal pulse width modulation
SVM	space-vector modulation

THD	total harmonic distortion
TPS	triple phase shift
XGBoost	extreme gradient boosting
ZVS	zero-voltage switching
ZVZCS	zero-voltage-zero-current switching

1 Introduction

1.1 Research Background

1.1.1 Renewable Energy Systems

In recent times, the energy sector is experiencing a great change due to the undeniable urgency surrounding global environmental issues, most notably the impact of global warming. As a result, there has been a concerted endeavor to diminish our dependency on fossil fuels, while simultaneously promoting the extensive integration of renewable energy sources. Fig. 1.1 visually captures the remarkable increase in renewable energy sources, including solar power, wind energy, hydropower, and various other sustainable alternatives, since 2010 [1]. Notably, the installed capacity of solar energy in 2020 has witnessed a magnificent doubling compared to its 2010 counterpart, showcasing the substantial progress in this field.

Nevertheless, the development of renewable energy systems poses significant stability challenges to the power grids. Additionally, renewable energy sources such as wind, solar, and biomass, exhibit decentralized characteristics, lack continuous generation, and possess a relatively low level of inherent inertia. Consequently, they are less responsive to fluctuations in grid frequency. Conventional power grids have predominantly relied on alternating current (AC), necessitating a subtle balance between generation and load, to maintain the system frequency and avert stability concerns [2], [3]. The integration of renewable energy sources diminishes system inertia and presents a formidable obstacle in managing power grid stability.

Energy storage systems (ESSs) play a pivotal role in addressing grid stability issues. ESSs, such as batteries, supercapacitors, and flywheels, effectively address the challenges arising from imbalances between power generation and demand [4]-[6]. During periods of high demand, these ESSs provide a valuable resource by supplementing the active power supply. Conversely, during periods of low demand, these ESSs store excess active power. By facilitating this

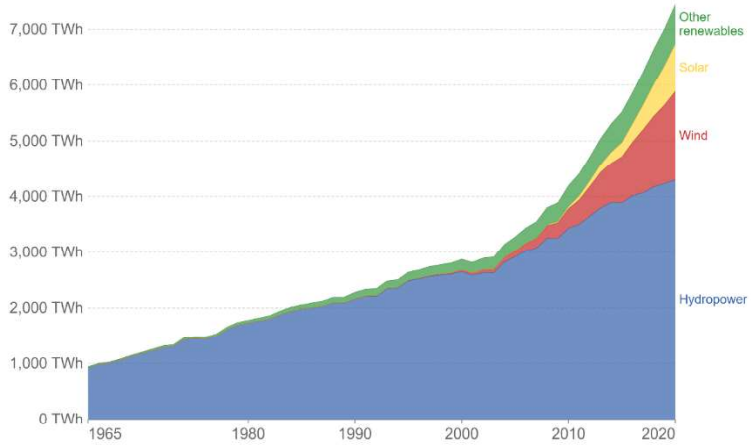


Fig. 1.1 Global renewable energy consumption, terawatt-hours [1].

dynamic balance between load and generation, ESSs alleviate the burden placed on grid stability management.

1.1.2 High-Power Dual-Active-Bridge Topology

The dual-active-bridge (DAB) DC-DC converter has emerged as a promising topology for battery ESSs (BESSs), thanks to its impressive array of features, including galvanic isolation, bidirectional power flow, high efficiency, and enhanced power density. In the realm of high-voltage medium-power applications, DAB-based topologies have gained more attraction compared to non-DAB-based modular multilevel topologies [7]. Some research papers have been dedicated to exploring the potential of the DAB topology for BESSs [8]–[13].

Reference [8] introduces a matrix topology on the AC power side for the single-stage DAB-based topology. However, its efficiency remains quite low, even with the incorporation of a soft-switching scheme. In [9], a combination of NPC rectifier and DAB dc-dc converter is utilized to design a fast charger. Nevertheless, the dc-dc stage of the converter consists of two cascaded DAB converters, resulting in increased system cost due to the higher number of switches.

Another cascaded DAB topology is discussed in [10] to charge three battery stacks. Nonetheless, the two battery stacks across the dc-link are non-isolated,

posing the risk of circulating current in case of certain failures. In [11], the secondary side of the DAB is split into two parts—one for fast charging and the other one for slow charging. Unfortunately, this setup may give rise to circulating power between the two ports, as they share a single magnetic core, leading to coupled power flow.

To improve the performance of the single-stage matrix DAB converter, [12] employs a combination of pulse-width modulation (PWM) and sinusoidal PWM (SPWM). However, this introduces low-frequency harmonics in the input current, negatively impacting the power factor. While [13] offers a solution for reducing the total harmonic distortion (THD), the bulky volume of the matrix DAB converter becomes a concern when cascaded for high-power applications, as it hampers the overall converter's high-power density.

Although there are already many different DAB topologies being discussed for BESSs, the practical implementation of DAB converters in high-power applications faces certain challenges that need to be addressed. Firstly, the heightened power and voltage levels pose a significant obstacle for power electronic converters as the semiconductor devices may not be able to reach such demanding ratings [14].

1.1.3 High Power SiC MOSFETs

It is well-known that Si IGBTs experience considerable power losses because of the tailing current effect, which occurs during the turn-off phase when the semiconductor is carrying the peak current. These power losses significantly diminish the overall system efficiency, especially when the output power is high.

Moreover, Si IGBTs are unsuitable for high switching frequencies, particularly when increasing the switching frequency beyond 20 kHz. Additionally, the utilization of bulkier magnetic components in Si IGBT-based DAB topologies further diminishes power density, limiting the overall compactness and efficiency of the system.

In contrast, SiC MOSFETs exhibit significantly lower power losses, thereby enabling notable improvements in power efficiency and power density. The design of the heatsink and cooling system can be simplified and downsized. Thus, SiC MOSFETs are more suitable and a preferable option for DAB topologies in high-power applications. A performance evaluation from Cree Inc. states that a dc-dc boost converter with SiC MOSFET had a 99.3% efficiency at 100 kHz, reducing the losses by 18% from the best Si IGBT solution at 20 kHz [15].

To investigate the progress of high-power SiC MOSFETs, a comprehensive market survey was conducted in October 2020, and the findings are presented in Table I. The table highlights the presence of eight manufacturers offering a total of eighteen distinct SiC modules with voltage ratings surpassing 1200 V. After excluding devices that are not commercially available, and factoring in a 50% derating consideration, only four viable options remain for a high-power system operating at a nominal voltage of approximately 1500 V. Regrettably, the cost implications pose a significant challenge as the two devices with the lowest current ratings among the remaining four options are priced above 1000 SGD. This cost factor significantly impacts the practical implementation of the entire power converter system.

TABLE I

MARKET SURVEY OF HIGH-POWER SIC MOSFETS

Manufacture	Model	Voltage Rating (V)	Current Rating (A)	Price (SGD)
Cree Wolfspeed	CAS300M17BM2	1700	225 (Tc 90 ˚C)	1,178
	CAB450M12XM3	1200	409 (Tc 90 ˚C)	1,159
	CAS300M12BM2	1200	300(Tc 90 ˚C)	755
Infineon	FF4MR20KM1	2000	370	-
	FF2MR12KM1	1200	500(Tc 85˚C)	-
	FF3MR12KM1	1200	375 (Tc 80˚C)	-
	FF6MR12W2M1P_B11	1200	200 (TH 10 ˚C)	400
Mitisubishi	FMF800DX2-24A	1200	800 (Tc 30℃)	-
	FMF400BX-24A	1200	400 (Tvj 25℃)	-
Powerex	QJD1760SB1	1700	540 (Tc 25°C)	-
Semikron	SKM350MB120SCH17	1200	541(Tc 25°C) 416 (Tc 80℃)	725
Rohm	BSM250D17P2E004	1700	250(Tc=60°C)	1,283
	BSM600D12P3G001	1200	576(Tc=60°C)	2,328
	BSM400D12P3G002	1200	358 (Tc=60°C)	1,744
	BSM180D12P2C101	1200	204(Tc 60°C)	556
Hitachi	MSM900FS17ALT	1700	900	Under development
ON Semiconductor	NXH200T120H3Q2F2SG	1200/650	256/128	131.02
	NXH350N100H4Q2F2	1000	300	157.96

1.1.4 SiC MOSFET-Based DAB Topologies for High-Power Applications

To overcome the mentioned problems and make the DAB-based topologies available for high-power BESSs, the voltage stress for the SiC MOSFETs should be reduced. There are mainly two approaches.

One potential solution for addressing the high-voltage stress lies in distributing the voltage stress by employing multiple series-connected DAB modules and

sharing the output current through parallel-connected DAB modules [14],[16]. Ideally, the power should be equally shared among these modules. However, due to practical limitations such as unequal inductance and slight variations in turn ratios of high-frequency transformers, power sharing between the modules may become imbalanced. This imbalance in input voltage poses a significant control challenge and has the potential to induce semiconductor failures. To address these issues and optimize overall efficiency performance, an input voltage sharing control and output current sharing control can be implemented [17]-[19]. Nonetheless, it is important to acknowledge that such control schemes introduce complexity to the overall control system. Additionally, the adoption of cascaded topologies introduces additional electromagnetic components, including transformers, leakage inductors, and capacitors. And to maintain the dc-link voltage, two input capacitors and one output capacitor are required. The addition of these extra components significantly increases the overall size and weight of the system. Furthermore, the presence of these components contributes to a reduction in system efficiency due to substantial iron losses incurred.

An alternative solution to address these challenges is the implementation of multilevel topologies, the neutral-point-clamped (NPC)-based DAB topology stands out as a promising candidate. The concept of the NPC structure was introduced for DAB design, as documented in [20]. A half-bridge NPC structure was discussed. However, while the half-bridge NPC DAB converter effectively tackles the issue of high voltage, it falls short in achieving high output power due to its limited voltage utilization. To enhance the performance, a full-bridge NPC DAB converter configuration is proposed in [21]. In this topology, both the primary and secondary sides employ Si IGBT-based NPC modules, featuring four switches in one phase leg. As a result, the voltage stress imposed on the semiconductors is halved compared to that in the conventional two-level DAB topology. Efficiency optimization is achieved through the application of DPS modulation. However, the use of Si IGBT-based NPC modules leads to significant switching losses. Moreover, there is potential for further optimization

by extending the DPS modulation method to triple-phase-shift. Another avenue of investigation involves the integration of a hybrid active-NPC (ANPC) structure within the inverter, combining Si and SiC switches, as elaborated in reference [22]. Specifically, SiC devices are utilized for the inner switches. This proposed topology has demonstrated effectiveness in improving inverter efficiency. However, it should be acknowledged that the ANPC structure necessitates the inclusion of two additional Si IGBTs for active control, thereby increasing both cost and control complexity. To summarize, the NPC DAB topology is a promising converter topology for high-power applications. Nonetheless, further research is required to explore the utilization of SiC MOSFETs to enhance the efficiency performance.

These challenges call for innovative solutions and further advancements to unlock the full potential of DAB converters in high-power scenarios.

1.2 Research Objectives

The primary objectives of this thesis are outlined as follows:

Firstly, conducting an extensive investigation and analysis of the existing literature and research on DAB converters utilized in high-power applications. This comprehensive review aims to gain a profound understanding of the subject matter and identify research gaps, such as topology issues and semiconductor limitations.

Secondly, addressing the identified research gaps by developing a novel multilevel topology for the DAB converter. This conceptual framework will serve as the foundation for subsequent analyses, with the goal of achieving optimal efficiency performance.

Thirdly, introducing a modulation and control method based on the analysis of the proposed topology, aiming to maximize the utilization of SiC MOSFETs.

Fourthly, designing and constructing a functional prototype of the proposed topology, providing a tangible platform for verification and experimentation.

Fifthly, performing rigorous hardware experiments and gather pertinent data to validate the proposed approach. The collected data will be compared with benchmark results obtained from the literature review.

Sixthly, analyzing and interpreting the collected data, drawing comparisons and insights from the benchmark results. Furthermore, efforts will be made to explore and elucidate any new findings that emerge from the experimental results, thereby facilitating design optimization.

Seventhly, drawing conclusions based on the research findings, establishing a clear connection to the initial research questions and objectives.

Eighthly, offering practical recommendations based on the research findings, proposing actionable steps for achieving zero switching features.

Lastly, to present the research findings, conclusions, and recommendations in a coherent, organized manner through the thesis, ensuring clarity and accessibility for the intended audience.

1.3 Major Contributions

According to the objectives of this thesis, the main contributions can be summarized as follows are:

Introducing a pioneering hybrid topology for high-power applications, combining Si IGBTs and SiC MOSFETs in an NPC DAB topology. The efficiency of this novel hybrid NPC DAB topology is compared against the full Si IGBT NPC DAB topology, full SiC MOSFET NPC DAB topology, and another hybrid topology, providing valuable insights into their respective performances.

A new modulation method is introduced to achieve enhanced efficiency for the proposed hybrid NPC DAB topology. The novel modulation technique, namely hybrid duty ratio phase-shift modulation (hybrid duty ratio PSM), is specifically designed to harness the advantages offered by SiC MOSFETs. The effectiveness of this hybrid modulation method is compared to the performance achieved with traditional triple-phase-shift (TPS) modulation.

Optimization efforts are undertaken to enhance the zero-voltage-zero-current switching characteristics of the proposed hybrid NPC DAB topology. Utilizing the power of AI technology, an optimization process is employed to fine-tune the hybrid modulation method, and hence further improving its overall performance.

Leveraging the same hybrid topology, a data-driven approach is employed for the TPS modulation method. The model is trained and tuned with experimental augmentation, leading to an optimized efficiency performance using the data-driven methodology.

Overall, these contributions significantly advance the field by proposing a novel hybrid topology, designing an innovative modulation method, optimizing efficiency through AI technology, and utilizing a data-driven approach for further enhancements in performance.

1.4 Organization of the Thesis

The thesis is organized as follows:

Chapter 1 begins with a concise overview of the research background, providing a comprehensive understanding of the existing knowledge and literature review. It briefly highlights the challenges encountered in practical applications, followed by a detailed description of the research objectives. Additionally, this chapter elucidates the contributions made by the thesis.

Chapter 2 encompasses a thorough literature review focusing on the topologies of grid-connected converters, as well as the fundamental characteristics of the DAB converter. Furthermore, it offers a comprehensive parameter design for the NPC DAB converter. In addition, the chapter includes a discussion on SiC switches, providing a brief overview of their characterization.

Chapter 3 centers on the modulation method for the hybrid NPC DAB converter. It analyzes the limitations associated with TPS modulation and

proposes a hybrid duty ratio PSM to address these challenges. Detailed modulation modes and switching sequences are provided, alongside simulation results comparing switching losses and conduction losses under TPS modulation and hybrid duty ratio PSM. Hardware experiments are conducted to validate the effectiveness of the proposed hybrid duty ratio PSM.

Chapter 4 specifically focuses on the switching characteristics of the hybrid NPC DAB converter, with a detailed analysis of zero-voltage-zero-current switching. AI technology is applied, and hardware experiments are conducted to validate the control method.

Chapter 5 introduces a data-driven approach for the hybrid NPC DAB with TPS modulation. The experimental results are utilized to enhance the trained model, and the outcomes are presented within this chapter.

Chapter 6 concludes the thesis by summarizing the findings and proposing future directions for research. It is followed by a list of publications, author biography, and an appendix section.

2 Hybrid Neutral-Point-Clamped Dual-Active-Bridge Converter for High-Voltage Battery Energy Storage Systems

2.1 Literature Review of Existing Grid-Connected Converter Topologies

With the increasing interest in clean energy, electrical devices are experiencing a surge in popularity. Within the realm of renewable energy systems, the power electronic converter assumes a pivotal role, thanks to its distinct features. Power electronic converters provide a solution to connect DC sources to the AC grid. There are many converter topologies existing to cater to diverse applications. Some topologies are single-stage DC-AC converters, which usually integrate a DC-AC stage alongside filters, and others are multi-stage DC-AC converters, which usually combine with not only a DC-AC stage and filters, but also a DC-DC stage to accommodate varying requirements.

Single-stage topologies enable direct connection between the DC source to the AC grid, offering the advantage of eliminating intermediate stages. By removing the need for DC-link capacitors, these topologies can enhance system reliability compared to multi-stage converters [23]–[25]. Several studies have explored the use of single-stage converters in electric vehicle chargers [26]–[28]. However, their popularity in high-power applications is limited due to switch constraints, and their power density is limited by the operating frequency. The soft-switching characteristics of the single-stage DAB converter is explored to further enhance system efficiency compared to multi-stage converters [29]–[33]. Specifically, [33] presents a DAB-based matrix converter as a single-stage DC-AC converter for electric vehicle chargers. While this design requires a total of 16 switching devices, leading to significant conduction losses, it operates at high frequencies with no switching losses. In [8] a 1.5-kW prototype is presented, which achieves a maximum efficiency of 82%. However, the output current exhibits low-frequency harmonic components, which may introduce stability

concerns when connected to the grid. An alternative single-stage DC-AC topology is presented [20], [34]. The modulation method for this topology is single-phase-shift (SPS) control, which is the same as the DAB DC-DC converter. However, it should be noted that achieving zero-voltage-switching (ZVS) throughout the entire power range is not attainable in this design. The absence of ZVS can impact the overall efficiency of the system, as the switching devices will experience switching losses when ZVS is not achieved.

In addition to the single-stage DC-AC converter, multi-stage converters can also be used to convert DC power into AC power. These multi-stages can be classified into two distinct stages, namely the DC-DC stage and the DC-AC stage. The DC-DC stage can be further divided based on its inclusion of galvanic isolation. Considering the need for galvanic isolation in energy storage systems to ensure system reliability and, taking into account the limitations of the research scope, this discussion will focus solely on the isolated DC-DC stage.

The concept of isolated bidirectional DC-DC converter was initially introduced in 1991 [35]. Its remarkable features, including galvanic isolation and high-power density, hold significant importance in high-voltage medium-power applications [36]-[38]. Nowadays, the DAB-based DC-DC topologies are increasingly popular compared to modular multilevel DC-DC topologies for high-voltage medium-power applications [39]. However, in the case of DAB-based DC-DC converters, certain passive components such as transformer leakage inductance and power transfer inductors might impose limitations on their ability to achieve soft-switching. Numerous studies have been dedicated to addressing this issue [40], [41]. The topology depicted in [40], as illustrated in Fig. 2.1, incorporates a division of the inductor and capacitor into two distinct sections, thereby expanding the soft-switching range. On the other hand, [41] proposes an alternative topology for mitigating the usage of capacitors (depicted in Fig. 2.2). With an equal number of switches, this topology offers advantages such as fewer capacitors and smaller leakage inductor current. Additionally, it presents an approach to reduce the voltage stress on the single switch, which

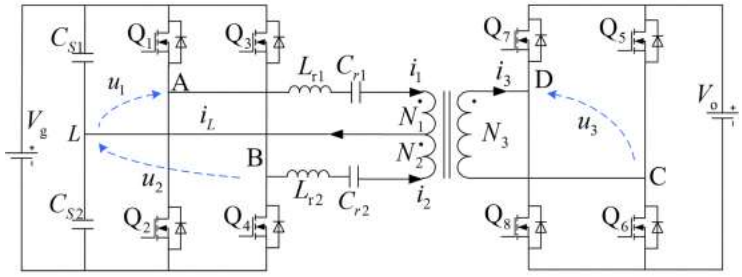


Fig. 2.1 Dual tank dual-bridge-series-resonant-converter topology [40].

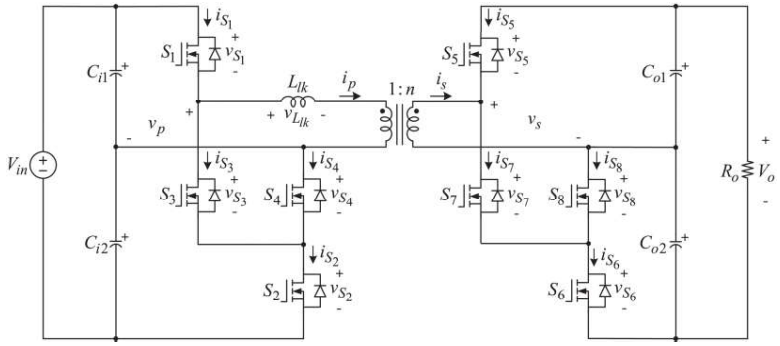


Fig. 2.2 Split-capacitor DAB topology [41].

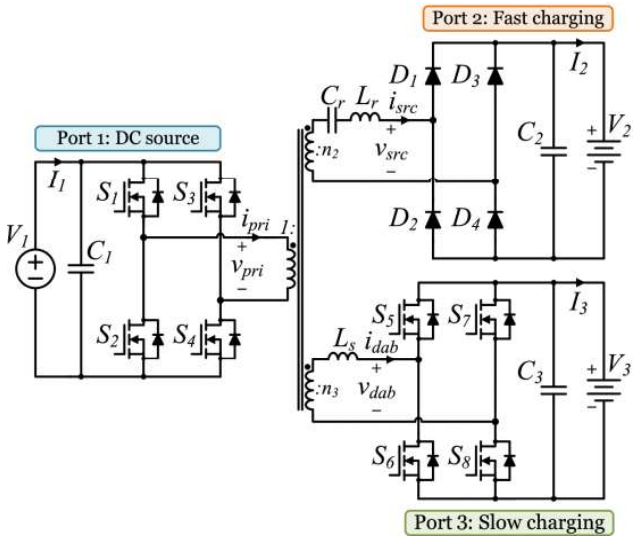


Fig. 2.3 Optimized three-port dc-dc converter [42].

proves to be beneficial for high-voltage applications without imposing extra requirements on semiconductor switches.

In recent years, there has been a growing focus on topologies specifically designed for high-power battery chargers, driven by the development of the electric vehicle industry. One example of such a topology, optimized for electric

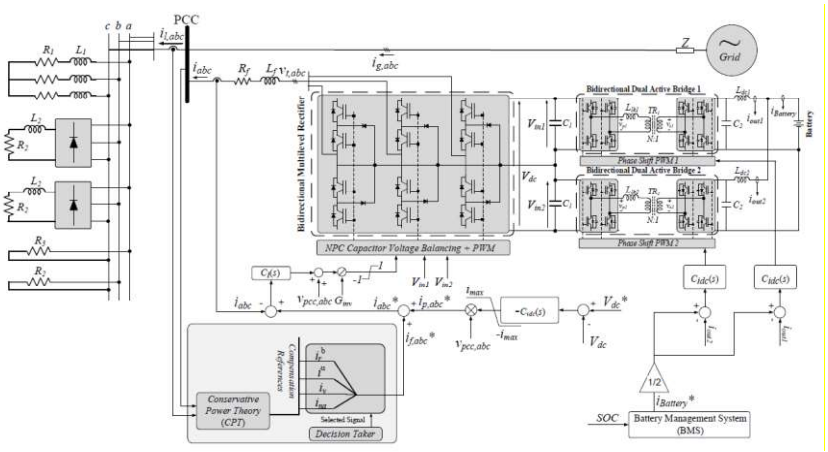


Fig. 2.4 NPC DAB converter for battery chargers [43].

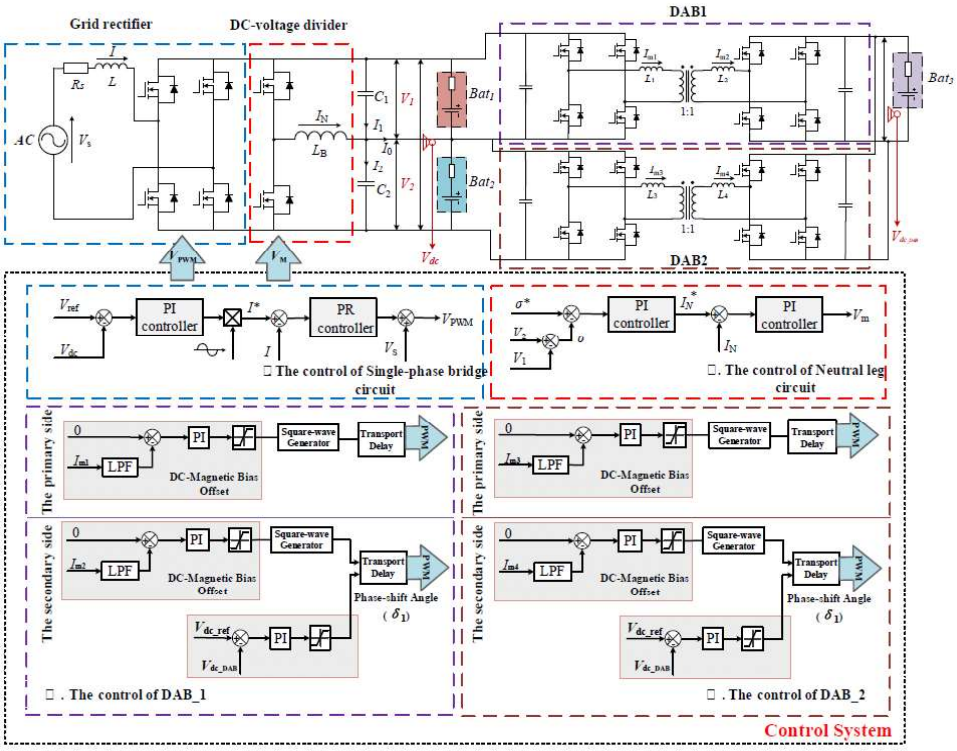


Fig. 2.5 Multi-port energy storage converter [44].

vehicle chargers, is discussed in [42] and depicted in Fig. 2.3. However, only one output port is capable of bidirectional operation, while the other output port is designed exclusively for fast charging from the grid to the built-in battery stack in a unidirectional manner.

Another DAB-based topology, incorporating Si IGBT-based NPC bridges, is explored in [43]. This topology, shown in Fig. 2.4, serves as both a power factor

correction mechanism and a battery charger, adjusting its operation based on the state of charge of the battery. To enhance the flexibility of input and output voltage levels, [44] presents a modular topology, as depicted in Fig. 2.5. However, due to its modular structure, an additional half-bridge and a neutral inductor are employed to balance the output voltages.

2.2 System Configuration

The system configuration for this study is shown in Fig. 2.6. the system integrates several battery stacks, each battery stack is rated at 373 kWh. And each battery is connected with three parallel-connected 150-kW power converter. The battery specifications are fixed by the manufacturers. The minimum and maximum input voltage is 1165 V and 1498 V, respectively. The nominal input voltage is 1368 V.

In terms of the literature review, an extensive comparison of various state-of-the-art topologies has been compiled, and the findings are succinctly presented in Table II. This table juxtaposes six different topologies across three key aspects: switches, voltage stress, and leakage inductance. Among these topologies, the NPC three-level-to-two-level configuration emerges as the preferred choice due to its adeptness in managing high input voltages, coupled with its reduced number of switches and reduced leakage inductance. These

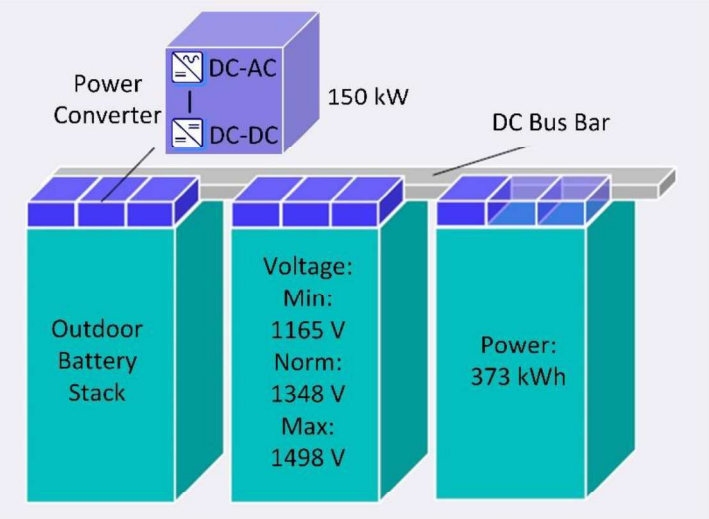


Fig. 2.6 System configuration of BESS.

attributes significantly enhance the power efficiency and power density of the system.

TABLE II

TOPOLOGIES COMPARISON FOR HIGH POWER APPLICATIONS

Topology	Switches	Voltage Stress	Leakage Inductance	Features
Two-level DAB	8	V_{in}, V_{out}	L_{lk}	Simple structure
NPC three-level to three-level DAB	16	$\frac{1}{2}V_{in}$, $\frac{1}{2}V_{out}$	L_{lk}	Suitable for high-voltage applications
NPC three-level to three-level DAB	12	$\frac{1}{2}V_{in}$, V_{out}	L_{lk}	Less complexity compared to the NPC 3L-3L topology.
Four-switch three-level to three-level	8	$\frac{1}{2}V_{in}$ for 3 V_{in} for 1, $\frac{1}{2}V_{out}$ for 3 V_{out} for 1	$\frac{1}{4}L_{lk}$	Suitable for high-frequency applications.
Input-series-output-series DAB	16	$\frac{1}{2}V_{in}$, $\frac{1}{2}V_{out}$	$\frac{1}{2}L_{lk} \times 2$	Suitable for high-voltage applications.
Input-series-output-parallel DAB	12	$\frac{1}{2}V_{in}$, V_{out}	$\frac{1}{2}L_{lk} \times 2$	Suitable for high-voltage applications.

2.3 Research Problems

2.3.1 Three-Level DAB Topology

Regarding the 150-kW 1500-V Battery Energy Storage Systems, bidirectional power flow is essential for both charging and discharging the battery. The DAB topology is well-suited for such applications due to its bidirectional power flow capability, high power density, and excellent efficiency. However, the conventional two-level DAB is not suitable for this specific application due to the absence of suitable semiconductor devices.

While both cascaded and multilevel topologies offer effective ways to reduce voltage stress on semiconductors, it is worth noting that cascaded topologies come with a limitation: they require separate transformers. This aspect is not conducive to achieving high-power density and optimal efficiency.

Therefore, to address this challenge and effectively mitigate the voltage stress experienced by semiconductors, the three-level NPC DAB topology is introduced. By implementing this three-level DAB configuration, the voltage stress imposed on semiconductors is notably reduced, precisely by half. This strategic reduction in voltage stress makes the three-level NPC DAB topology an excellent choice for high-power applications.

2.3.2 Hybrid NPC Modules

There are several options available for NPC modules. Traditionally, these modules have employed a single type of semiconductor device, such as full Si IGBT-based NPC modules or full SiC MOSFET-based NPC modules. SiC MOSFETs are preferred for their potential to achieve higher efficiency. However, their elevated cost limits their use in high-power applications.

To address the cost concerns associated with NPC modules, hybrid modules have been introduced. In the context of inverters, hybrid modules typically incorporate SiC MOSFETs for the inner switches. While previous ANPC hybrid modules replaced the inner IGBTs with SiC MOSFETs primarily to reduce inverter switching losses, this configuration is not well-suited for NPC-based DAB converters. This is because the primary switching losses in NPC-based DAB converters occur in the outer switches, rendering the previous approach less effective.

2.4 Topology Description and Circuit Design

2.4.1 Circuit Description

Fig. 2.7 showcases the proposed hybrid Si + SiC NPC-based DAB converter. The input and output voltages are denoted as U_1 and U_2, respectively. The primary side of the DAB is connected to a battery stack, complemented by two hybrid half-bridge NPC modules. The outer switches of the NPC module employ SiC MOSFETs, while the inner switches utilize Si IGBTs. On the primary side, the switches are represented as $S_{1\sim8}$, where S_1, S_4, S_5 and S_8 correspond to SiC MOSFETs, while the remaining switches are Si IGBTs. The NPC modules also incorporate clamped diodes defined as $D_{c1\sim c4}$. The secondary side consists of two SiC half-bridge modules denoted as $Q_{1\sim4}$. The central component of the converter is a high-frequency transformer, featuring a leakage inductance L_s. The transformer has a turns ratio of n:1.

The converter can facilitate bidirectional power flow, making it suitable for both charging and discharging the battery stack. The power direction can be controlled by adjusting the phase shift ratio between the primary and secondary sides. When employing SPS control, if the phase shift ratio exceeds zero, the battery stack releases power to the grid. Conversely, when the phase shift ratio falls below zero, the battery stack is charged. The fundamental principles of control remain consistent for both power directions, with the divergence lying in the specific requirements for battery stack charging and discharging. Therefore, for the sake of simplicity, this chapter will solely focus on elucidating the discharging procedure, wherein the power flows from the battery stack to the grid.

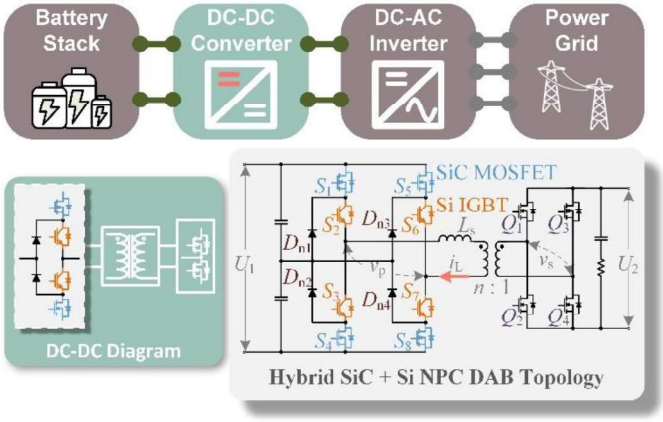


Fig. 2.7 Proposed hybrid SiC + Si NPC DAB topology.

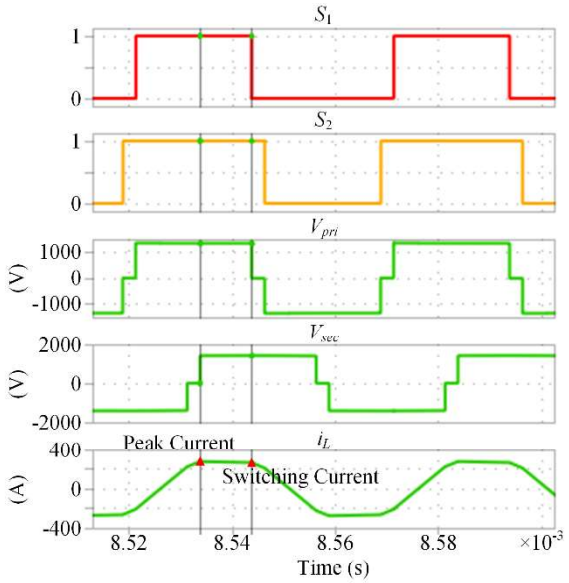


Fig. 2.8 Switching transitions for the outer switches in the NPC modules.

As previously mentioned, the primary power loss in the NPC-based DAB lies in the switching process. Within the NPC modules of this converter, ZVS can be naturally achieved across a wide power range, resulting in minimal turn-on loss compared to the overall power losses. The dominant losses within the NPC module are due to the turn-off processes. For Si IGBTs, the turn-off period involves a two-stage process. The first stage involves swiftly halting the inner MOSFET channel, leading to a significant drop in current to a specific level. The second stage entails ceasing the tail current, which arises from the recombination of minority carriers. As the second stage is time-consuming, the

overall turn-off process for Si IGBTs takes a considerable amount of time (approximately 0.5 μs). High switching currents result in substantial switching losses for these devices. However, SiC MOSFETs exhibit smaller switching losses since they do not experience tail current, requiring only around 0.05 μs for the turn-off process.

To provide a clearer demonstration of the intended purpose of the proposed DAB converter, Fig. 2.8 illustrates the switching transitions. When the outer switch S_1 is turned off, the switching current approaches the peak current (indicated by the left cursor representing peak current and the right cursor indicating switching current for the outer switches). Consequently, if IGBTs are employed as the outer switching devices, the switching loss can be substantial. One approach to address this issue is by reducing the peak current, but the potential improvement is limited. Another idea is to replace the IGBTs with SiC MOSFETs, which can significantly reduce switching losses at the same current level. In this chapter, a novel hybrid structure for the DAB converter is proposed, as depicted in Fig. 2.7 In this proposed configuration, the outer switches of the NPC modules are substituted with SiC MOSFETs, while the inner switches remain as Si IGBTs to limit cost escalation.

2.4.2 Control Scheme and Modulation Method

The primary modulation method employed in the DAB converter is SPS control, which utilizes a single control degree, *D*, to modify the phase shift ratio between the primary and secondary sides. This control method is the most straightforward for the DAB converter, allowing the output power to be regulated by adjusting the phase shift ratio, *D*. However, optimizing performance metrics such as peak current, switching loss, and conduction loss cannot be achieved with just one control degree.

To address this limitation, the TPS control was introduced in [45], offering three control degrees to enhance system efficiency across a wide range of loads. Several studies have investigated this control method for various optimization objectives [46]. Additionally, there have been a few studies on the

3L-DAB converter. In [47], TPS control is applied to the half-bridge NPC DAB converter, while [48] proposes a full-bridge NPC DAB converter with TPS control. However, [48] is not suitable for diode-clamped NPC modules, as the switches within the NPC modules may experience overvoltages. The detailed illustration will be shown in Chapter 3.

In order to enhance the performance of the proposed hybrid three-level DAB converter, this study incorporates an additional control method that incorporates three control degrees of freedom (CDOF). The definition of CDOF is depicted in Fig. 2.9, while the switching sequence within the NPC modules is illustrated in Fig. 2.10. The parameter T_h represents half of the switching period. The three CDOF, namely $D_{1\sim3}$, are identified as follows: D_1T_h represents the pulse width during which S_1 conducts, and D_2T_h denotes the duration in which Q_1 and Q_4 are simultaneously open. As indicated in the Fig. 2.10, the period of D_2T_h commences at the termination of the rising edge of Q_4 and concludes at the onset of the falling edge of Q_1. Points a-b and c-d signify the boundary points of the highest voltage on the primary side and the secondary side, respectively. Subsequently, the third control degree, D_3, denotes the phase-shift ratio between X (the midpoint between a and b) and Y (the midpoint between c and d). Similar to the phase-shift ratio D in the SPS control method, D_3 serves a comparable function. The control degrees D_1 and D_2 provide the controller with additional functionality to optimize performance indicators such as peak current.

As illustrated in Fig. 2.9, the voltage waveforms on both the primary and secondary sides exhibit three levels. In the three-level structure, the voltage stress experienced by the switches is only half of that in the two-level structure. This reduction in voltage stress expands the range of available commercial semiconductor options. Furthermore, high-voltage devices often suffer from increased conduction losses due to their higher on-resistance. By employing lower-rated switches, the total power losses can be reduced, and efficiency can be improved. It is possible to modify the three-level voltage waveforms by adjusting the CDOF D_1 and D_2 for the primary and secondary sides, respectively.

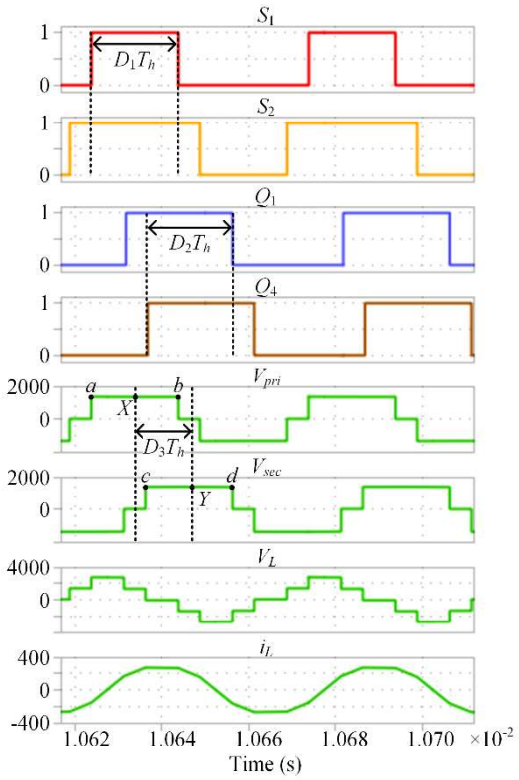


Fig. 2.9 Definition of CDOF for the proposed NPC-based DAB converter.

t	S_1	SD_1	S_2	SD_2	S_3	SD_3	S_4	SD_4	S_5	SD_5	S_6	SD_6	S_7	SD_7	S_8	SD_8	D_{c1}	D_{c2}	D_{c3}	D_{c4}
t_1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
t_2	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
t_3	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
t_4	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1
t_5	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
t_6	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Fig. 2.10 Switching sequence in the NPC modules.

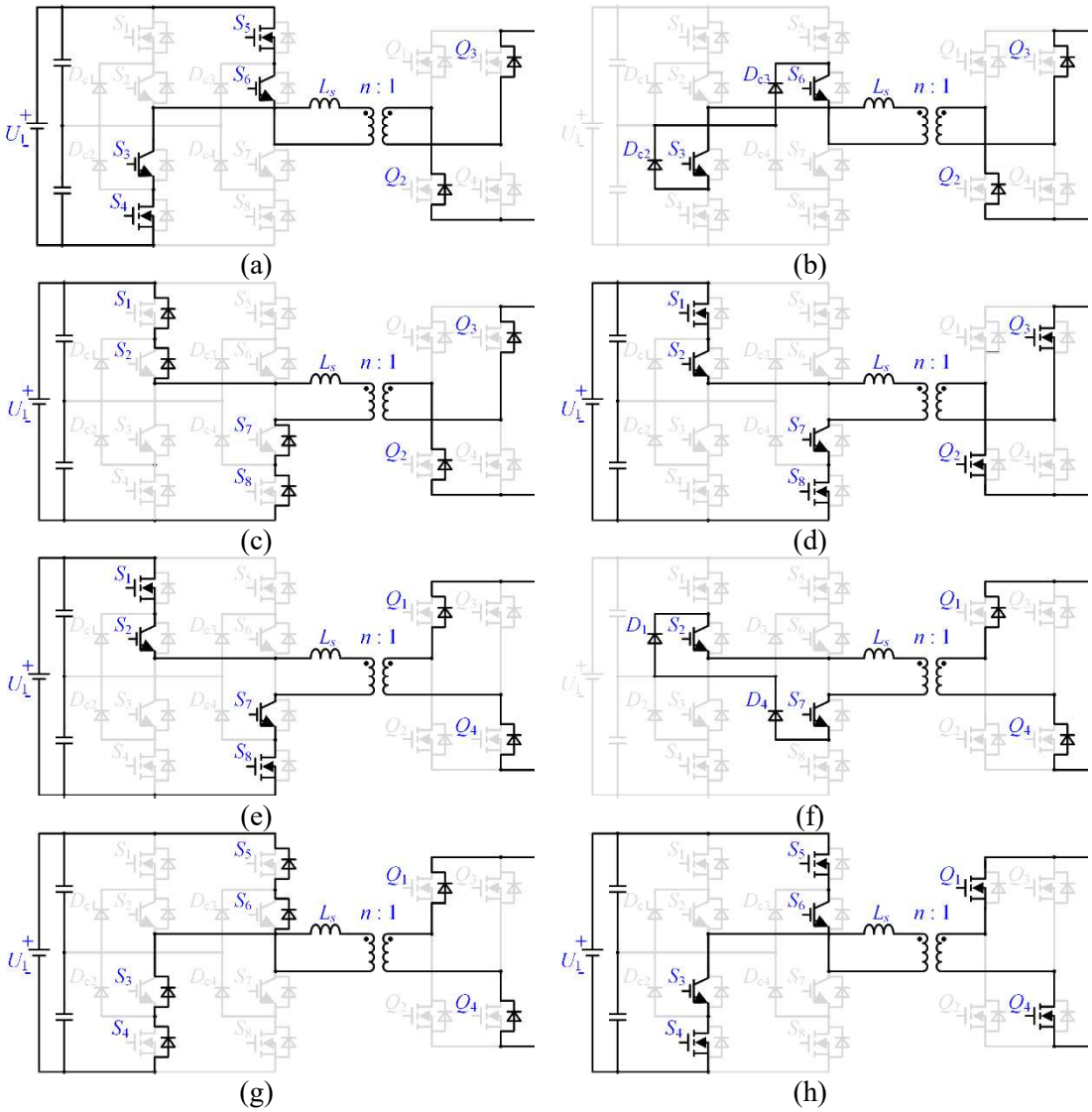


Fig. 2.11. Current commutation loops with the control method in the proposed NPC DAB converter.

However, there are certain drawbacks that accompany the efficiency advantages. The three-level structure, while offering efficiency benefits, leads to a reduction in voltage utilization due to the zero-voltage duration, consequently impacting the power transfer capability. In order to achieve the same output power, a larger phase-shift angle between the primary and secondary sides is generally required to compensate for the reduced voltage utilization. This, in turn, necessitates a higher value of D_3 for the same output power when incorporating D_1 and D_2. Furthermore, the overload capability of

the three-level structure is not as robust as that of the two-level structure, as D_3 may easily exceed the upper limit of 0.5 in the three-level configuration.

The proposed NPC modules adhere to stringent rules for semiconductor switching. The switching sequence is illustrated in Fig. 2.10. During the turn-on phase, all the switches achieve automatic ZVS, ensuring synchronous turn-on for both the inner and outer switches of the NPC modules. However, it is crucial for the outer switches to turn off before their corresponding inner switches to prevent overvoltage damage. For instance, in Fig. 2.7, S_1 is an outer switch that must turn off prior to its corresponding inner switch, S_2. Simultaneously, S_1 and S_2, can be turned on together. The detailed commutation loops based on this operating principle are depicted in Fig. 2.11. Both the primary and secondary sides achieve ZVS during the turn-on period, aided by the body diodes.

Chapter 3 will delve into the control method and derive various relationships related to it. The current section provides only a brief introduction to this aspect. As mentioned previously, the transformer turns ratio is denoted as n:1. The voltage conversion ratio of the converter is expressed as $k = nU_2/U_1$. When k = 1, the converter can achieve the optimal ZVS range. In practical designs, the transformer turns ratio is typically selected to match the nominal operating point of the converter, ensuring that the voltage conversion ratio under nominal conditions equals one. However, during the discharging process, the voltage of the battery stacks decreases with the state of charge (SoC), resulting in an increase in the voltage conversion ratio. Consequently, during discharging, the value of k exceeds 1. Since the two conditions are symmetrical, this study focuses solely on the situation where $k > 1$. For the case of $k > 1$, the peak current of the inductor, i_p, can be derived using equation (1), and the output power, P, can be calculated based on equation (2), where U_1 and U_2 represent the input and output voltages, respectively. The variable f_s denotes the switching frequency of the switches, and L_s indicates the leakage inductance of the high-frequency transformer. The control method involves three control degrees, $D_{1\sim3}$, which will be discussed further in the chapter.

As mentioned before, reducing the peak current can help decrease switching losses, especially for the inner IGBTs, despite the outer switches being replaced by SiC MOSFETs. However, if D_2 decreases too much, it will lead to a drop in power transfer capability. There exists a minimum value for D_2, below which the converter will lose its ability to output maximum power. Similarly, when k is less than 1, D_1 can affect the peak current. As an initial control strategy, monitoring the value of D3 is suggested. If D_3 approaches the upper limit of 0.5, modifying D_2 should be avoided to ensure maximum power output.

2.5 Comparisons of Different Modules

Simulations of a 1500-V, 150-kW NPC DAB converter application are conducted on PLECS. The detailed simulation setting is shown in Table III. The input side is the battery stack, and the output side is the dc bus of the system. The input and output voltages in the simulations are set as nominal values 1348 V and 750 V, respectively. The maximum output power of the proposed converter is 150 kW. Four different NPC modules are compared, and the results are shown in Figs. 2.12 and 2.13. The maximum output power of the proposed converter is 150 kW. Four different NPC modules are compared, and the results are shown in Figs. 2.12 and 2.13.

2.5.1 Performance Comparison for Different Types of NPC Modules

Fig. 2.12 illustrates the efficiency curves for four distinct types of NPC modules, namely full Si IGBT-based NPC modules (marked with blue color), full SiC MOSFET-based NPC modules (marked with orange color), hybrid NPC modules with SiC MOSFET inner switches (marked with grey color), and the proposed novel hybrid NPC modules with SiC MOSFET outer switches (marked with yellow color). Among these configurations, the full Si IGBT-based NPC modules exhibit the lowest efficiency. The maximum efficiency of full Si IGBT-based NPC modules is 98.29% at 40 kW. The lowest efficiency is 96.68% at 150 kW. The full SiC MOSFET-based modules achieve best efficiency performance, whose highest efficiency is 99.83% at 40 kW and lowest efficiency

is 99.03% at 150 kW. Comparing two hybrid NPC modules. The hybrid modules with inner-SiC-outer-Si structure achieve a better efficiency than full Si IGBT-based modules but the improvement is trivial. Its efficiency ranges from 97.51% to 98.47%, at power 150 kW and 40 kW, respectively. The proposed hybrid modules with inner-Si-outer-SiC structure achieve a significant improvement in efficiency performance compared to another hybrid modules. The highest efficiency reaches up to 99.70% at 40 kW, and lowest efficiency maintain at 98.01%. When the output power ranges from 40 kW to 100 kW, the hybrid modules proposed exhibit nearly identical performance to that of the full SiC modules, with a mere difference of 0.13%. In contrast, the efficiency of the other hybrid NPC modules is comparable to that of the full Si modules, displaying a lower efficiency. The simulation results reinforce the theoretical analysis and underscore the effectiveness of the proposed hybrid NPC DAB converter.. It is noteworthy that the proposed hybrid NPC modules demonstrate significant efficiency improvement, even though they are not as efficient as the full SiC MOSFET-based NPC modules. In fact, the proposed hybrid modules outperform other hybrid NPC modules and achieve efficiencies that closely approach those of the full SiC MOSFET-based NPC modules.

TABLE III

SIMULATION SETTINGS FOR DIFFERENT NPC MODULES

Parameters		Values
Battery voltage, U_1		1348 V
DC-bus voltage, U_2		750 V
Turns ratio, n		1.8
Resistance, R		3.75 Ω
Inductance, L_s		63.7 μF
Switching frequency, f_s		20 kHz
Primary side IGBTs	FF600R12KE4P	$V_{ce,sat}$ = 2.00 V @ T_{vj} = 125℃
Primary side MOSFETs	FF3MR12KM1	$R_{ds(on)}$ = 3.92 mΩ @ T_{vj} = 125℃
Secondary side MOSFETs	FF2MR12KM1	$R_{ds(on)}$ = 2.94 mΩ @ T_{vj} = 125℃

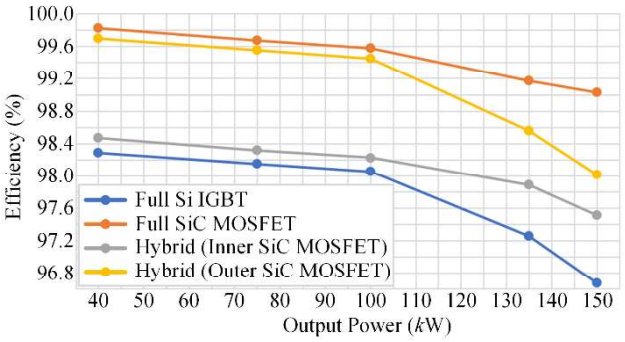


Fig. 2.12 Efficiency comparison for four types of NPC modules.

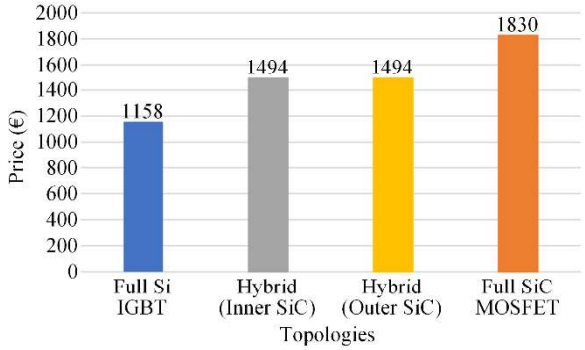


Fig. 2.13 Cost comparison for the four types of NPC modules.

The hybrid curves exhibit a notable decline beyond 100 kW output power, primarily due to the constrained voltage utilization resulting from the introduction of control degrees D_1 and D_2. As the output power increases, D_3 also rises in tandem. The significant growth of D_3 leads to a linear increase in peak current, but only a marginal boost in output power. In particular, as D_3 approaches its upper limit of 0.5, the increase of D_3 results in higher peak current As previously mentioned, the substantial increase in peak current leads to heightened switching losses in the Si devices. Additionally, the conduction losses are also impacted by the amplified peak current. Consequently, the higher losses incurred by the inner switches contribute to a more pronounced reduction in efficiency. To address this issue for high output power scenarios, the controller should make slight adjustments to the control degrees in order to maintain both D_3 and power loss within acceptable ranges. Further investigations could be

conducted to explore optimized control degree pairs for specific power ranges, thereby aiding in the reduction of losses in the inner switches.

2.5.2 Cost Estimation for Different Types of NPC Modules

In order to assess the proposed topology for commercial applications, this study conducts a cost comparison of four distinct NPC modules. Given that the majority of components, such as the leakage inductor, transformer, and passive components, remain consistent across all four topologies, the primary cost discrepancy arises from the pricing of the semiconductors. With the market pricing in 2019, each half-bridge Si IGBT module FF600R12KE4P costs €193 and each half-bridge SiC MOSFET module €305. Fig. 2.13 illustrates the obtained results. While the secondary side remains consistent across the four designs, they differ in terms of the NPC modules employed on the primary side. Specifically, the four NPC module types are: full Si IGBT-based NPC modules, full SiC MOSFET-based NPC modules, hybrid NPC modules with SiC MOSFET inner switches, and the proposed novel hybrid NPC modules with SiC MOSFET outer switches. The proposed hybrid NPC modules exhibit a comparable cost to the alternative hybrid topology, but attains higher efficiency, as previously discussed in the preceding sections.

As illustrated in Fig. 2.13, the full Si IGBT-based NPC modules exhibit the lowest cost, approximately €1158 for switching devices. However, this configuration also exhibits the lowest efficiency. In comparison, the proposed hybrid module demonstrates a 1.4% efficiency increase with an additional cost of €336. On the other hand, the other hybrid module only achieves a modest 0.18% improvement in efficiency. The full SiC MOSFET-based NPC modules, while costing an additional €672, achieves a similar efficiency improvement of approximately 1.5%. Consequently, the proposed hybrid solution is a trade-off between efficiency improvement and cost.

2.6 Summary

This chapter has introduced a novel hybrid Si + SiC NPC DAB converter that addresses the requirements of high efficiency and power density in high-voltage medium-power battery applications. The proposed hybrid converter exhibits a remarkable ability to operate at a high switching frequency while maintaining high efficiency. Through simulation results, the effectiveness of the hybrid structure and the proposed control strategy, which incorporates three control degrees, has been verified. This strategy aids in reducing peak currents. It is crucial to consider power transfer capability and power loss, particularly in scenarios involving high output power. Simulation experiments using PLECS have been conducted on a 150-kW converter application. When compared to other hybrid NPC modules, the proposed converter achieves higher efficiency at the same cost. Furthermore, in comparison to a full SiC MOSFET-based NPC modules, the proposed hybrid structure offers cost savings in switch components while delivering nearly identical efficiency levels. Further analysis can be conducted on phase-shift pairs to strike a balance between minimizing switching losses and optimizing voltage utilization. The control method can be further optimized in the prototype to achieve the highest efficiency across a wide power range.

3 Hybrid Duty Ratio Phase-Shift Modulation for a Si + SiC Neutral-Point-Clamped Dual-Active-Bridge Converter

3.1 Review of Modulation Methods

The modulation techniques employed in DAB-based topologies can be categorized into various methods, including PSM, duty ratio modulation (DRM), frequency modulation (FM), space-vector modulation (SVM), and hybrid modulation.

Under the PSM technique, the two bridges within the DAB are modulated with a phase-shift angle, allowing control over the output power. Among the PSM methods, SPS modulation is widely adopted due to its simplicity [49]. However, extended-phase-shift and dual-phase-shift methods have been introduced to enhance performance by introducing an additional degree of control [50], [51]. TPS modulation, which allows independent tuning of phase-shift angles for the primary and secondary sides, can be considered the general PSM method [52]. With TPS modulation, optimization of the primary and secondary sides at different operating points can be achieved, resulting in superior performance compared to other PSM methods. The peak current performance can be optimized with the TPS modulation [53], [54]. Besides, ZVS range [55], and overall efficiency performance [56] also can be optimized with TPS. However, the primary concern with PSM methods is that their efficiency under light load conditions may not be as favorable as their efficiency at rated power [57].

In DRM, the amplitude of the carrier signal for the modulation varies to achieve the desired output power [58]. Compared to PSM, DRM offers cost reduction by alleviating the need for high-precision sensors, while maintaining satisfactory performance under light load conditions. However, it is unsuitable for high-frequency applications and typically necessitates a bulky filter, thereby inevitably diminishing the power density of the converter.

The FM technique is capable of achieving ZVS over a broad operating range, although its dynamic response is comparatively limited [59]. Moreover, the utilization of a bulky capacitor is necessary for effective filtering. On the other hand, SVM receives considerable acclaim for its exceptional precision and minimal THD [60]. However, the complex implementation requirements of SVM in DAB topologies restrict its widespread adoption.

Hybrid modulation has garnered attention due to its ability to amalgamate the benefits of different modulation techniques [61]. This approach enhances efficiency, particularly in light load conditions, while also necessitating a smaller filter, which is crucial for the effective implementation of DRM.

In a hybrid Si + SiC NPC DAB topology, the primary side combines Si IGBTs and SiC MOSFETs. However, certain challenges arise with this configuration. When operating with a fixed duty ratio and synchronized switching command under PSM, the Si IGBTs turn off at the peak of the current, leading to significant switching losses due to the tail current effect of the IGBTs [62]. Additionally, the SiC MOSFETs experience high conduction losses due to their high on-resistance [63].

Research presented in [66] reveals that high-power SiC MOSFET modules, despite having a consistently low resistance ($R_{ds(on)}$), exhibit diminished conduction loss performance when the current exceeds 50% of the rated current, falling short of the performance demonstrated by equivalent-rated Si IGBT modules. In the NPC DAB topology, the absence of a neutral current path under PSM results in high conduction losses on SiC body diodes [64]. Moreover, since Si and SiC devices have different switching rates, the synchronized gate signals in PSM may lead to overvoltage failure. Therefore, employing a fixed duty ratio is not suitable for hybrid semiconductor topologies. For a more comprehensive analysis, please refer to Section 3.2.

A pioneering approach, known as the hybrid duty ratio PSM method, is introduced for the hybrid NPC DAB converter, aiming to address the limitations of conventional PSM techniques. In this method, the primary side NPC bridges

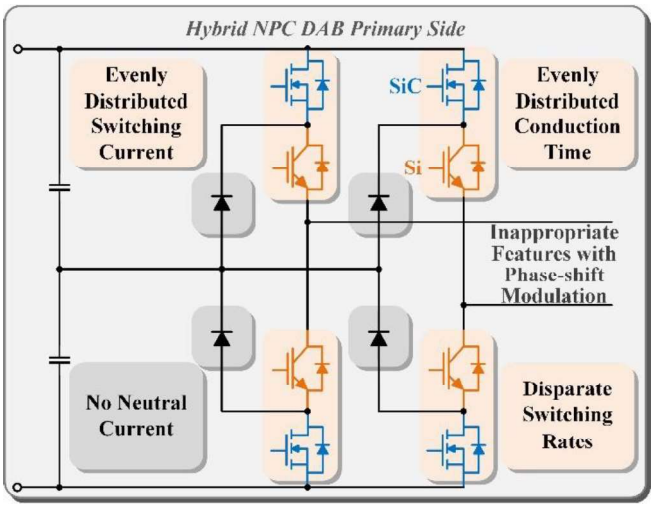


Fig. 3.1 Inappropriate features with PSM.

employ distinct duty ratios coupled with a staggered switching sequence for the Si IGBTs and SiC MOSFETs. This configuration allows the Si IGBTs to avoid high turn-off currents, while the SiC MOSFETs achieve reduced conduction time through the proposed hybrid modulation scheme. Additionally, the neutral current path is utilized to alleviate conduction stress on the SiC MOSFET body diodes. By employing a staggered switching time for different semiconductor devices, the potential for overvoltage failure is effectively mitigated. Comparatively, the proposed hybrid modulation method surpasses conventional PSM in terms of efficiency. A comprehensive theoretical analysis is presented, and experimental results from a 2-kW hardware prototype extensively validate the viability of the hybrid duty ratio PSM approach.

3.2 Challenges in the Existing Phase-Shift-Modulation for the Hybrid NPC DAB Converter

3.2.1 Challenges in the Existing PSM for the Hybrid NPC DAB Converter

The hybrid topology is not suitable for the conventional PSM due to the differing characteristics of Si IGBTs and SiC MOSFETs. There are four main reasons for this:

1) High switching loss due to evenly distributed switching current

Under PSM on the primary side, the evenly distributed switching current leads to high switching losses and a significant overvoltage spike in the Si IGBTs. In the hybrid topology with TPS modulation, both the Si and SiC devices are in the same bridge arm (e.g., S_1 and S_2 in Fig. 2.7) and switch simultaneously. The switching currents for both devices are the same. However, due to the tail current, the Si device experiences higher losses during the turn-off process, which is directly proportional to the switching current. The Si devices (S_2 and S_7) turn off the positive peak current of the leakage inductor, while the Si devices (S_3 and S_6) turn off the negative peak current. Consequently, the switching losses of the Si device are excessive. Furthermore, the high switching current results in a high di/dt, leading to a large overvoltage spike that could potentially damage the device.

2) High conduction loss due to evenly distributed conduction time

PSM on the primary side, with its evenly distributed conduction time, results in high conduction losses in the SiC MOSFETs. As mentioned earlier, conventional PSM methods do not allow for changing the duty ratio of the primary side in the hybrid NPC DAB converter. All switches share an equal conduction time. However, the on-state resistances of Si IGBTs and SiC MOSFETs differ. Generally, at higher working currents, Si IGBTs exhibit better conduction loss performance than SiC MOSFETs due to the lower voltage drop across Si switches. These differences become more pronounced at higher temperatures [64]. Additionally, the long conduction time under high temperature is more detrimental to SiC MOSFETs, as it may cause die-attach deterioration [65]. Consequently, applying the same duty ratio to both Si IGBTs and SiC MOSFETs in PSM is not a suitable strategy.

3) Body diodes conduction loss due to no neutral current paths

The full potential of neutral current paths is not fully realized when using pure PSM methods like TPS. While TPS modulation can generate three-level waveforms across the transformer, the zero-level voltage plateau is achieved

by turning on either all upper switches or all lower switches in different NPC bridges. This configuration eliminates the current commutation loop that would pass through the clamping diodes. Consequently, continuous current can only flow through the body diodes of the Si and SiC switches when the commutation state changes. However, as highlighted in [64], the current flowing through the body diode of the SiC device results in high conduction losses.

4) Potential overvoltage failure due to disparate switching rates

The dissimilar switching rates between Si and SiC devices introduce a heightened risk of overvoltage in semiconductor switches. In the case of PSM, despite providing simultaneous gate signals to switches within the same bridge arm, the switches do not complete their state transitions at the same time due to the varying switching rates of Si and SiC switches. This discrepancy amplifies **the potential overvoltage risk.**

3.2.2 Proposed Solutions: Hybrid Duty Ratio PSM

In this chapter, a hybrid duty ratio PSM with a staggered switching sequence is introduced to resolve the four aforementioned issues. This approach provides three control parameters: one degree of control for adjusting the duty ratio of the primary side switches, and two degrees of control for managing the inner phase angle among secondary side switches and the outer phase angle between the primary and secondary sides. These control freedoms facilitate the regulation of power transfer.

Under the hybrid modulation method, the switching sequence for the primary side of the hybrid NPC DAB topology undergoes modifications to optimize performance. By employing duty ratio modulation on the primary side, the hybrid NPC DAB converter achieves its utmost potential.

Firstly, the staggered switching sequence of Si and SiC devices mitigates switching losses by evenly distributing the switching stress. The proposed hybrid modulation assigns a narrower driving signal to SiC MOSFETs S_1, S_4, S_5, and S_8, while employing a wider signal to drive Si IGBTs S_2, S_3, S_6, and S_7.

Consequently, Si devices experience lower current during commutation, helping to alleviate excessive switching losses caused by prolonged tail current duration. On the other hand, SiC devices handle peak current with reduced switching losses.

Secondly, under the hybrid modulation method, the SiC MOSFETs on the primary side operate with a duty ratio of less than 50%, effectively reducing total conduction losses.

Thirdly, thanks to the staggered switching sequence, the Si devices remain closed when the adjacent SiC devices are turned off. This allows continuous current to flow through the neutral clamped diodes rather than the SiC MOSFETs body diodes, leading to smoother state transitions on the primary side switches.

Finally, due to the non-concurrent switching of Si and SiC devices, the potential overvoltage failure resulting from differing switching rates is avoided.

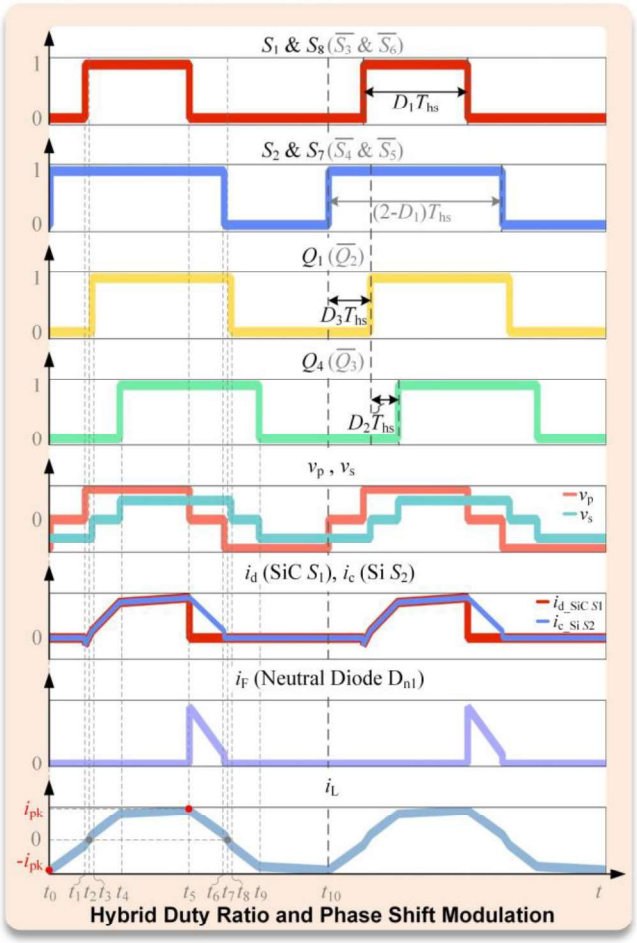


Fig. 3.2 Waveforms of proposed hybrid duty ratio PSM.

3.3 Hybrid Duty Ratio Phase-Shift-Modulation

3.3.1 Waveforms of the Proposed Hybrid Modulation

Fig. 3.2 illustrates the waveforms of the proposed modulation technique. On the primary side, the duty ratio modulation is applied to the SiC MOSFET S_1 and Si IGBT S_2, as well as to S_4 and S_3, S_5 and S_6, and S_8 and S_7. During the on-state duration of S_2, the switching process of the SiC MOSFET S_1 is completed. Consequently, the on-state of S_2 is longer than that of S1. On the secondary side, the gate driving signals for Q_1 and Q_4 (or Q_2 and Q_3) follow the phase shift rules. Furthermore, the signals driving S_2 and Q_1 are phase-shifted. The switching cycle commences with the activation of the Si IGBT S_2. After S_2 is

turned on, the SiC switches Q_1 and Q_4 sequentially turn on, conducting half of the switching cycle.

Fig. 3.2 also presents the definition of three control degrees. The time that equals half of the switching time is denoted as T_{hs}. The control freedom D_1 represents the duty ratio of the SiC MOSFET S_1. The on-state duration for S_1 is D_1T_{hs}, which is less than or equal to T_{hs}. Meanwhile, the Si IGBT S_2 in the same arm remains conducting for $(2\text{-}D_1)T_{hs}$. On the primary side, the SiC MOSFET S_1 and the Si IGBT S_3 receive complementary driving signals, as do SiC S_4 and Si S_2, SiC S_5 and Si S_7, and SiC S_8 and Si S_6. Thus, the switching sequences for Si and SiC devices are staggered. The second control degree, D_2, defines the inner phase angle between the secondary devices Q_1 and Q_4. The third control degree, D_3, adjusts the outer phase shift angle between the primary S_2 and the secondary Q_1. The phase shift between the rising edge of S_2 and the rising edge of Q_1 is defined as D_3T_{hs}.

3.3.2 Operation Mode Analysis

Under the hybrid modulation method with three control degrees, D_1, D_2, and D_3, there are six different modes, as depicted in Fig. 3.3. These modes represent various operating points and are distinguished by the boundary conditions of the modulation parameters D_1, D_2, and D_3, summarized in Table IV. Each of the six modes corresponds to a different power range, with Mode IV covering the entire range from zero to the maximum power. Given the similarity in analysis methods and processes, only Mode IV will be analyzed in the following sections for illustrative purposes.

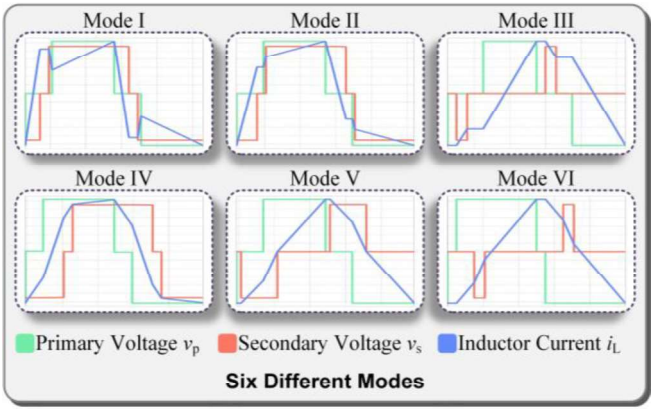


Fig. 3.3 Six different modes under the hybrid modulation.

TABLE IV

CONTROL PARAMETERS AND POWER RANGE WITH DIFFERENT MODES

MODE	RANGE OF D_1, D_2, D_3	MAXIMUM POWER OUTPUT
MODE I	$0<D_3<1-D_1<1$ $0<D_3+D_2<1-D_1<1$	$(-0.5P_{MAX}, 0.5P_{MAX})$
MODE II	$0<D_3<1-D_1<1$ $0<1-D_1<D_3+D_2<1$	$(0, 2/3P_{MAX})$
MODE III	$0<D_3<1-D_1<1$ $1<D_3+D_2<2-D_1<2$	$(0, 0.5P_{MAX})$
MODE IV	$0<1-D_1<D_3<1$ $1-D_1<D_3+D_2<1$	$(0, P_{MAX})$
MODE V	$0<1-D_1<D_3<1$ $1<D_3+D_2<2-D_1$	$(0, 2/3P_{MAX})$
MODE VI	$0<1-D_1<D_3<1$ $1<2-D_1<D_3+D_2<2$	$(-0.5P_{MAX}, 0.5P_{MAX})$

To better understand the relationship between the transferred power and three modulation parameters under Mode IV, voltages and currents are analyzed segment-by-segment using piecewise approach. Specifically, the voltage and current waveforms shown in Fig. 3.3 for Mode IV are divided into smaller segments, and the power transferred during each segment is analyzed separately. Based on the analyzed segments, the peak inductor current can be derived using equation (1), which is defined as follows:

$$i_p = U_1[D_1 + k(D_2 + 2D_3 - 1)]/(4f_sL_s), \qquad (1)$$

where U_1, f_s, L_s, and k represent the input voltage, switching frequency, leakage inductance and voltage conversion ratio respectively, and $D_{1\text{-}3}$ are the modulation parameters.

As the output power P is the average of the instantaneous inductor voltage and current u_L and i_L integrated over time, P can be calculated by:

$$P = \int_0^{2T_{hs}} u_L(t)i_L(t)dt/2T_{hs}. \qquad (2)$$

From (4), the equation for the output power under Mode IV is:

$$P = kU_1^2\left[D_3(1-D_3) - \frac{1}{2}(1-D_1)^2 - \frac{1}{2}D_2(D_1 + D_2 + 2D_3 - 2)\right]/(2f_sL_s). \qquad (3)$$

3.3.3 Commutation State Analysis

The detailed commutation states under Mode IV are shown in Fig. 3.4 The current passing through the inductor from left to right is defined as positive. The first switching cycle starts at the time t_0 and ends at the time t_{10}.

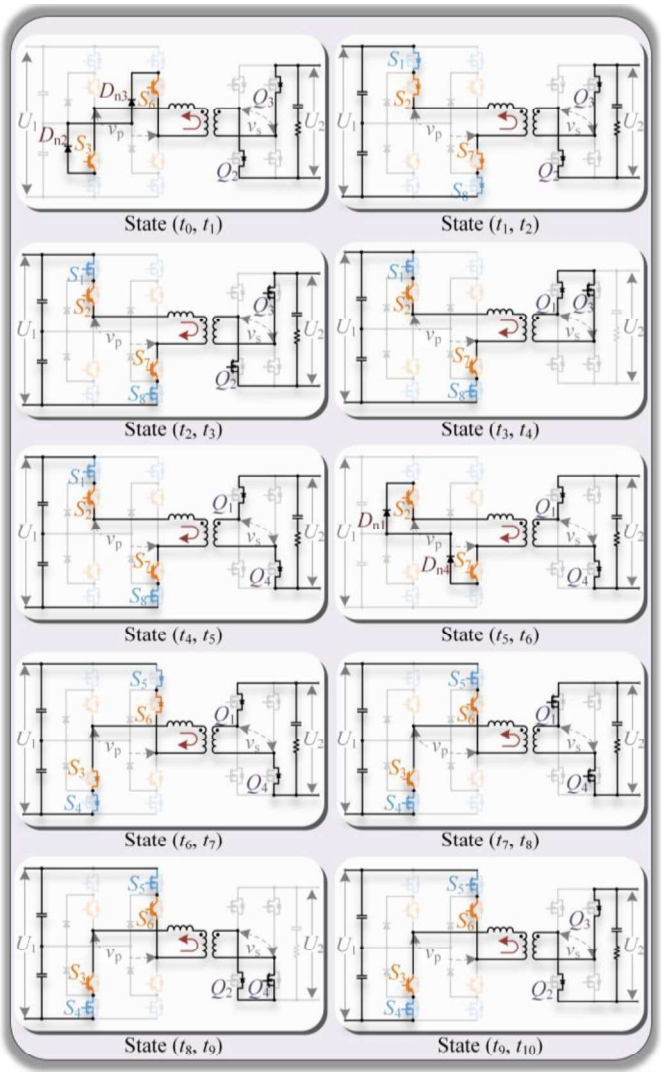


Fig. 3.4 Commutation states under Mode IV.

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is nU_2, hence the negative current reduces. But it still reversely flows through the inductor. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. There is no current running through the SiC MOSFET body diodes during this

time. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBT S_3 and S_6 turn off, and the SiC MOSFET S_1 and S_8 turn on. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is U_1+nU_2, hence the negative current reduces sharply. On the primary side, the current path changes to the body diodes of S_1, S_2, S_7, and S_8 for a short time. The voltages of S_1, S_2, S_7, and S_8 are clamped to zero with the negative current flowing through the body diodes. Therefore, ZVS of S_1, S_2, S_7 and S_8 is achieved. On the secondary side, the current flows through the body diodes of Q_2 and Q_3 so that ZVS is also ensured.

Commutation state t_2: At the time t_2, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_2, and Q_3 are activated at this time.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the current direction changes to positive. The voltage across the inductor is U_1+nU_2. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, SiC MOSFETs S_1, and S_8. On the secondary side, the current flows through Q_2 and Q_3.

Commutation state t_3: At the time t_3, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2, and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, while Q_3 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1, and the current increases. On the primary side, the current path is made by S_1, S_2, S_7, and S_8. On the secondary side, the current flows through Q_3 and the body diode of Q_1. The drain-to-source voltage of Q_1 is clamped to zero. ZVS of Q_1 is achieved.

Commutation state t_4: At the time t_4, on the primary side, the SiC MOSFETs S_1 and S_8, and the Si IGBTs S_2 and S_7 are in the on state. On the secondary side, Q_3 turns off, Q_4 turns, and Q_1 is activated.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1-nU_2. The current continues rising but slowly. On the primary side, the current path is still made by S_1, S_2, S_7, and S_8. On the secondary side, the current changes to the body diodes of Q_1 and Q_4. The voltage across Q_4 is zero. Hence, ZVS for Q_4 is achieved.

Commutation state t_5: At the time t_5, the inductor current reaches the maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is -nU_2. The current drops from the peak. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. There is no current passing through the SiC body diodes during this time. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_1 and Q_4 are in the on state.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is -(U_1+nU_2). Hence, the current decreases. On the primary side, the current path changes to the body diodes of S_3, S_4, S_5, and S_6 for a short time. The voltages of S_3, S_4, S_5, and S_6 are clamped to zero with the negative current passing through the body diodes so that ZVS of S_3, S_4, S_5, and S_6 is achieved.

Commutation state t_7: At the time t_7, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_1, and Q_4 are active at this time.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the current direction becomes negative. The voltage across the inductor is $-(U_1+nU_2)$. The negative current increases. On the primary side, the current path changes to Si IGBTs S_3, S_6, SiC MOSFETs S_4, and S_5. On the secondary side, the current flows through Q_1 and Q_4.

Commutation state t_8: At the time t_8, on the primary side, the SiC MOSFETs S_4 and S_5, and the Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_1 turns off, Q_2 turns on, while Q_4 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$. The negative current increases. On the primary side, the current path is made by S_3, S_4, S_5, and S_6. On the secondary side, the current flows through Q_4 and the body diode of Q_2.

Commutation state t_9: At the time t_9, on the primary side, the SiC MOSFETs S_4 and S_5, and the Si IGBTs S_3 and S_6 are in the on state. On the secondary side, Q_4 turns off, Q_3 turns on, while Q_2 is active.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is $-(U_1-nU_2)$. The negative current continues increasing but slowly. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is still made by S_3, S_4, S_5, and S_6. On the secondary side, the current changes to the body diodes of Q_2 and Q_3.

3.3.4 ZVS Range Analysis of the Hybrid Modulation Method

Similar to the analysis of ZVS range under TPS modulation method, a piecewise method has been employed for the investigation of the ZVS range pertaining to the hybrid duty ratio PSM. The switching cycle is partitioned into ten segments under Mode IV, consistent with the segmentation used for the commutation state analysis in subsection 3.3.3.

Ensuring the ZVS range demands certain conditions at various time points. At

time t_1, it is imperative for the inductor current to remain below zero to guarantee the ZVS operation of switches S_1, S_2, S_7, and S_8. Subsequently, at the time t_3, when the switch Q_1 turns on, the current must exceed zero, allowing it to pass through the body diode of Q_1, thereby ensuring the ZVS of Q_1. At time t_4, the current should surpass zero to ensure that it passes through the body diodes of Q_4 first, thus guaranteeing the ZVS. it must traverse zero between times t_5 and t_9 to ensure the ZVS of switches S_3, S_4, S_5, S_6, and Q_2. Finally, at time t_9, the current should be negative to secure the ZVS of Q_3.

To provide a succinct overview of the criteria for the six different modes, we have summarized them in Table V.

TABLE V

ZVS CRITERIA UNDER DIFFERENT MODES

MODE	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
MODE I	0	+	+	-	+	0	-	-	+	-
MODE II	0	+	+	+	+	0	-	-	-	-
MODE III	-	-	-	0	+	+	+	+	0	-
MODE IV	-	0	+	+	+	+	0	-	-	-
MODE V	-	-	0	+	+	+	+	0	-	-
MODE VI	-	-	-	0	+	+	+	+	0	-

3.3.5 Features of the Hybrid Modulation Method

The proposed hybrid duty ratio PSM method overcomes the four challenges in the existing TPS modulation shown in Fig. 3.1.

Firstly, the duty ratio modulation on the primary side facilitates uneven switching stress, which significantly reduces switching loss and prevents large overvoltages. As shown in Fig. 3, the peak currents at t_0 and t_5 (indicated by red dots) are both handled by the SiC MOSFETs. Due to the semiconductor topological structure, the SiC devices do not suffer the tail current, resulting in minimal switching-off losses even at high switching currents. Furthermore,

thanks to the staggered switching sequence, the adjacent Si IGBTs do not turn off at the same time. Instead, they continue conducting and only turn off the current at t_1 (S_3 and S_6) and t_6 (S_2 and S_7). At time t_5, the peak current is switched by the SiC MOSFETs S_1 and S_8, while the negative peak current is handled by the SiC MOSFETs S_4 and S_5 at t_0. As the current at t_1 (t_6) is close to zero, the switching losses for the Si IGBTs are minimized. Compared to conventional TPS modulation, the switching stress for the SiC MOSFETs remains unchanged, while the switching stress for the Si IGBTs is reduced. Consequently, the overall switching losses are reduced. Moreover, the reduced switching current results in low di/dt, which mitigates overvoltage spikes during the turn-off process and enhances the reliability of the NPC DAB converter.

Secondly, the duty ratio modulation on the primary side enables uneven conduction stress, leading to significant reductions in conduction losses. By assigning different duty ratios to the Si IGBTs and SiC MOSFETs, their respective conduction times can be varied. As discussed above, the on-state durations for S_1 and S_2 are D_1T_{hs} and $(2\text{-}D_1)T_{hs}$, respectively. Since the control degree D_1 is less than one, the conduction time of the Si IGBT S_2 is longer than that of the SiC MOSFET S_1 When operating at elevated temperatures caused by high load currents, the Si IGBTs are better suited for longer conduction times due to their lower voltage drop in high-temperature conditions. are better suited for longer conduction times due to their lower voltage drop in high-temperature conditions.

Thirdly, the hybrid modulation scheme incorporates a neutral current path that effectively mitigates conduction losses arising from the body diodes of the SiC MOSFETs. For example, during the commutation state (t_5, t_6), the inductor current flows through the neutral diodes due to the continued activation of Si IGBTs S_2 and S_7 are still activated. This neutral current path bypasses the SiC body diodes, preventing them from experiencing high currents. Moreover, the inductor current experiences a significant drop during this period. Hence, when the IGBTs S_2 and S_7 on the verge of turning off, the current is nearly zero, thereby greatly reducing the switching-off losses of the IGBTs. Moreover,

although there is a possibility of positive current flowing through the body diodes of the SiC switches during the commutation state (t_6, t_7), the conduction losses caused by the SiC MOSFETSs body diodes can be neglected due to the low current magnitude and short duration.

Fourthly, the duty ratio modulation on the primary side effectively eliminates disparate switching rates by employing a staggered switching sequence for the Si IGBTs and the SiC MOSFETs. Specifically, the SiC MOSFETs S_1 and S_8 switch on and off at t_1 and t_5, respectively, while the adjacent Si IGBTs S_1 and S_8 switch at t_0 and t_6, respectively. This staggered timing arrangement ensures that different semiconductor devices do not switch at different rates, thereby safeguarding both the Si and SiC switches against potential overvoltage failures.

Moreover, as shown in Figs. 3.2 and 3.4, the hybrid modulation method enables ZVS for all the switching devices. On the primary side, during the time interval (t_1, t_2), the current passes through the body diodes of S_1, S_2, S_7, and S_8. This ensures that the drain-to-source voltage of the MOSFETs and the collector-to-emitter voltage of the IGBTs are clamped to zero. At t_2, the IGBTs and MOSFETs are activated, achieving ZVS for S_1, S_2, S_7 and S_8. Similarly, during (t_6, t_7), the current flows through the body diodes of S_3, S_4, S_5, and S_6, while the drain-to-source voltage and collector-to-emitter voltage are clamped to zero. Hence, the IGBTs and MOSFETs turn on at t_7 with ZVS. On the secondary side, ZVS is also guaranteed. The MOSFETs turn on with zero drain-to-source voltage as their body diodes are active before the switches are activated. As a result, ZVS is achieved for all the switches in the analyzed operation mode.

Additionally, the hybrid duty ratio PSM does not introduce any additional transformer losses than TPS modulation. This is due to the fact that the hybrid modulation is capable of generating an inductor voltage waveform that is equivalent to that of TPS modulation. The detailed waveforms illustrating the operation under hybrid modulation can be observed in Fig. 3.3.

3.4 Power Loss Comparison between Phase-Shift-Modulation and Hybrid Duty Ratio Phase-Shift-Modulation

The hybrid modulation method offers significant advantages over TPS modulation, primarily due to reduced switching and conduction stresses on the power semiconductors. To validate the earlier analysis, simulation results were obtained using the PLECS platform, and these results are presented in this section. The simulation parameters and settings are outlined in Table VI. Considering the easy implementation of the hardware experiments within the research lab and the main contributions of this chapter is the hybrid duty ratio PSM rather than the topology validation, which has been discussed with simulation results in Chapter 2, the high-power systems were downscaled for the simulations and experimental trials for the validations of hybrid duty ratio modulation. However, it is worth noting that the validation of the hybrid NPC topology at higher power levels has been conducted, and the corresponding results can be found in Chapter 2.

TABLE VI
SIMULATION SETTINGS FOR HYBRID MODULATION

Parameters	Values
Battery voltage, U_1	300 V
DC-bus voltage, U_2	140 V
Turns ratio, n	2
Inductance, L_s	236 µF
Switching frequency, f_s	20 kHz
Primary side IGBT	IKW40N65ES5
Primary side MOSFET	UF3C065030K4S
Primary side neutral diode	APT30DQ60B
Secondary side MOSFET	UF3C065030K4S

3.4.1 Simulation Waveforms of the Proposed Hybrid TPS Modulation

The simulation waveforms depicted in Fig. 3.5 provide validation for the improvements achieved by the hybrid modulation in terms of switching stress,

conduction stress, and switching sequence for Si and SiC devices on the primary side, as compared to TPS modulation.

The drain-to-source voltage v_{ds} illustrates that the turn-on time of the SiC devices is delayed under the proposed hybrid modulation, creating a differentiation in the turn-on process between Si and SiC devices. The collector-to-emitter voltage v_{ce} waveform reveals that the Si devices under hybrid modulation exhibit a delayed turn-off compared to TPS modulation, resulting in

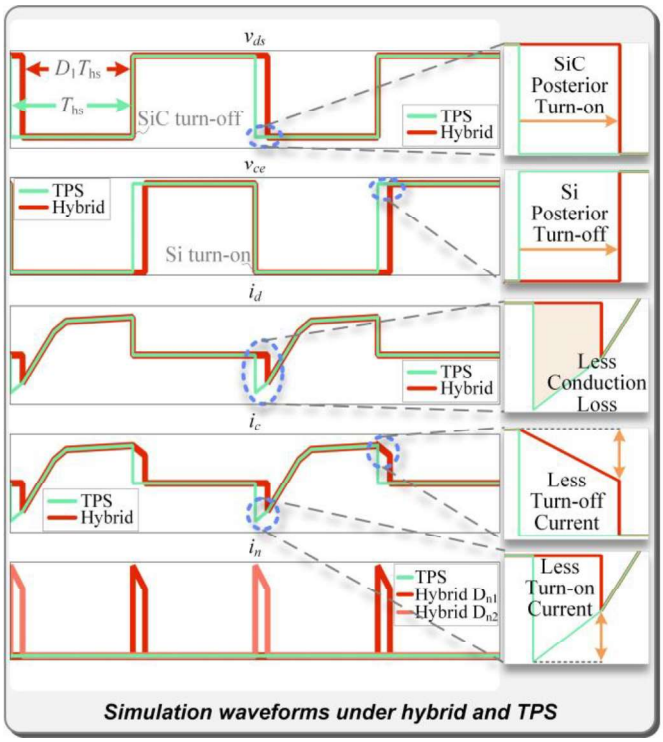


Fig. 3.5 Simulation waveforms under the proposed hybrid modulation and TPS modulation.

a staggered turn-off process for Si and SiC devices. The staggered switching sequence, achieved through the hybrid modulation method, avoids potential overvoltage failures arising from dissimilar switching rates among different semiconductor devices.

The third waveform records the drain-to-source current i_d. Compared to the TPS modulation, the proposed hybrid modulation benefits from the reduced conducting time of SiC devices, thereby decreasing conduction losses caused

by negative current i_d, as shown in Fig. 3.5. Besides, the turn-on current for the SiC devices also decrease, contributing to a reduction in turn-on losses.

The collector-to-emitter current i_c waveform highlights two advantages brought about by the hybrid modulation method for Si devices. Firstly, the turn-on losses for Si devices are minimized compared to TPS modulation due to lower turn-on currents. Secondly, the turn-off current of the Si IGBT is notably lower than that under TPS modulation, resulting in a reduced turn-off voltage spike and lower turn-off losses.

At the bottom of Fig. 3.5, the neutral current is displayed for both hybrid modulation and TPS modulation. This depiction showcases the presence of a neutral current path under hybrid modulation, whereas no such path exists under TPS modulation.

3.4.2 Switching Loss Comparison between the Proposed Hybrid Modulation and TPS Modulation

The simulation results presented in Fig. 3.5 demonstrate a reduction in switching losses under the proposed modulation due to the lower switching current. A comparison between the switching losses of the proposed hybrid modulation and TPS modulation is conducted through simulation. Practical semiconductor models with thermal and loss behavior, as described in the respective datasheets, are employed to construct the NPC DAB topology. As discussed in Subsection 3.2, during the time interval [t_5, t_6], the current descent rate is $-nU_2/L_s$, and the duration of this state is equal to (1-D_1)T_{hs}. The peak current under Mode IV is shown in Subsection 3.3.2. Furthermore, the IGBT switching-off current varies with changes in the control parameters D_1, D_2, and D_3, as shown in equation (3).

The switching loss at 2 kW, 1 kW, and 200 W is compared in Fig. 3.6 For each output power, four different pairs of (D_1, D_2) are considered. Category I represents (D_1, D_2) = (0.96, 0.96), while Categories II to IV correspond to (0.90, 0.90), (0.80, 0.90), and (0.76, 0.84), respectively. As illustrated in Figure 7, the proposed hybrid modulation significantly reduces switching losses. When the

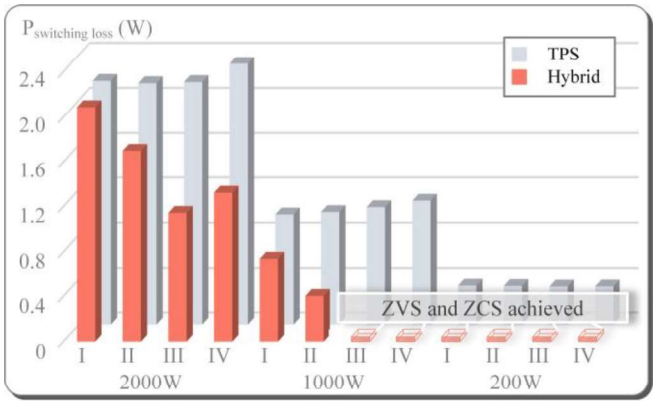


Fig. 3.6 Switching loss of Si IGBT devices under the hybrid modulation and TPS modulation.

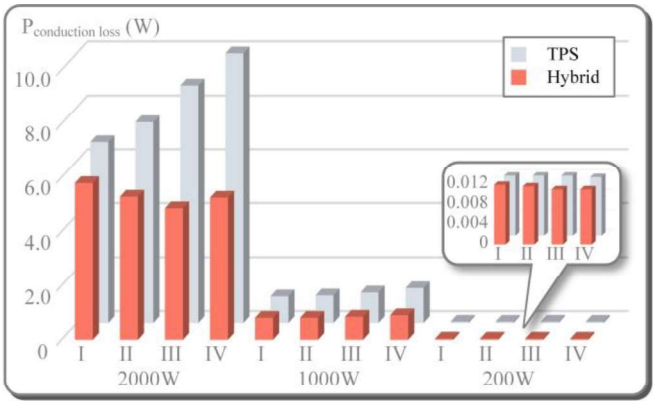


Fig. 3.7 Conduction loss of primary SiC MOSFET devices under the hybrid modulation and TPS modulation.

output power is 2 kW with Category IV, the switching losses in the IGBTs are reduced by 42.94%. Similarly, for the same output power, applying Category III results in a 46.92% reduction in switching losses compared to TPS modulation. Additionally, under light load conditions, the hybrid modulation achieves both ZVS and ZCS simultaneously, leading to a reduction of more than 0.8 W in each IGBT switching loss. Providing Category IV and P=1 kW, ZCS can be achieved during the turn-off process of the IGBT, highlighting the superiority of the proposed hybrid modulation.

Throughout all load conditions, the switching losses of the proposed hybrid modulation consistently outperform those of TPS modulation, primarily due to the absence of high switching currents. Moreover, if the control parameters are

appropriately adjusted, ZVS can be ensured for the entire power range under the hybrid modulation.

3.4.3 Conduction Loss Comparison between the Proposed Hybrid Modulation and TPS Modulation

In Subsection 3.2, it is explained that the proposed hybrid modulation method effectively reduces the conduction loss of the SiC devices. This reduction is achieved by shortening the duty ratio of the SiC MOSFET and providing a neutral current path to bypass the body diode of the SiC device. The conduction loss, which is primarily determined by the on-resistance of the SiC MOSFET, is directly proportional to the integral of the drain-to-source current over time. As depicted in Fig. 3.5, the conduction time of the MOSFET corresponds to $D_1 T_{hs}$. Therefore, by reducing the value of D_1, the conduction loss can be lowered.

Furthermore, during the zero-voltage stage of v_p, the conduction loss caused by the body diode of the SiC devices is mitigated by employing neutral clamped diodes to establish a neutral current path. This enables the high current to flow through the neutral diodes instead of the SiC body diodes, resulting in minimized conduction losses.

Fig. 3.7 illustrates the comparison of conduction losses at different operating points. The categories defined in Fig. 3.6 are used for this comparison. At the rated power of 2 kW, the hybrid modulation achieves a reduction of more than 5 W in total conduction loss when using Category IV. Similarly, at 1 kW, the conduction loss is reduced by over 20% under the hybrid modulation compared to the TPS modulation. When operating under light load conditions, the performance improvement achieved by the hybrid modulation is 8% better than that of the TPS modulation.

3.5 Experimental Results

3.5.1 Hardware Settings

To validate the proposed hybrid modulation method, a prototype of a 2-kW NPC-based DAB converter was constructed using SiC MOSFETs and Si IGBTs. The hardware platform employed for the experiments is depicted in Fig. 3.8, and the experimental settings are summarized in Table VI. The control system is based on the dSPACE 1202 platform, providing precise and reliable control capabilities. The converter's input voltage is supplied by a Chroma programmable DC power supply model 62150H-600S. On the output side, a Chroma programmable AC/DC electric load model 6304 is connected as the DC load. To measure the converter efficiency, a Yokogawa precision power analyzer model WT3000 is utilized. Additionally, a Teledyne LeCroy WaveRunner 8058HD oscilloscope is employed to capture the waveforms for analysis and evaluation purposes.

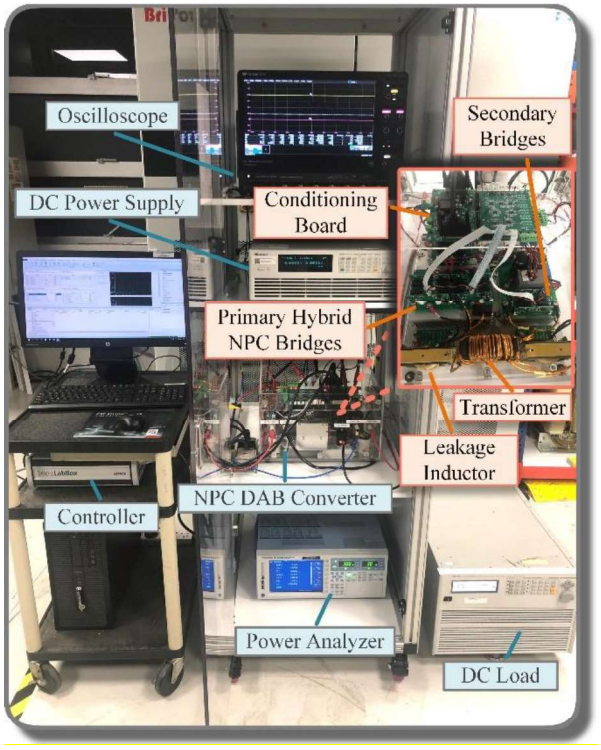


Fig. 3.8 Hardware setup of the NPC DAB converter.

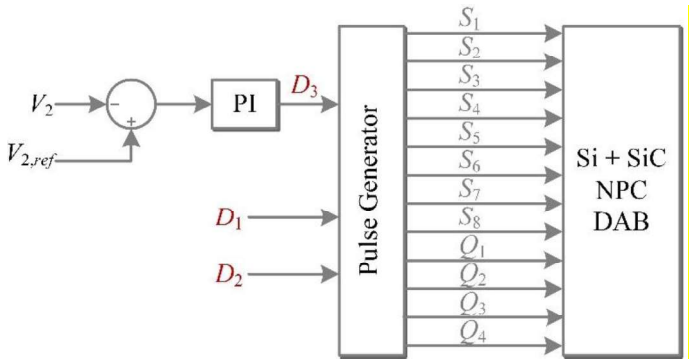


Fig. 3.9 Control diagram of Si + SiC NPC DAB under the proposed hybrid duty ratio PSM.

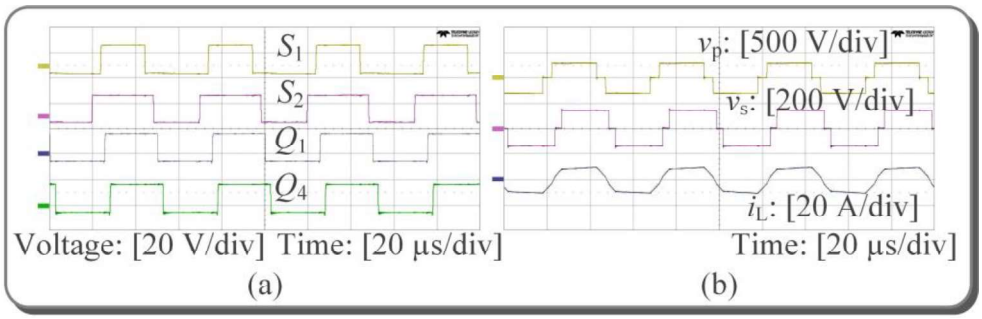


Fig. 3.10 Hardware experiments of the proposed hybrid modulation at 2 kW with (D1, D2) = (0.84, 0.90). (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

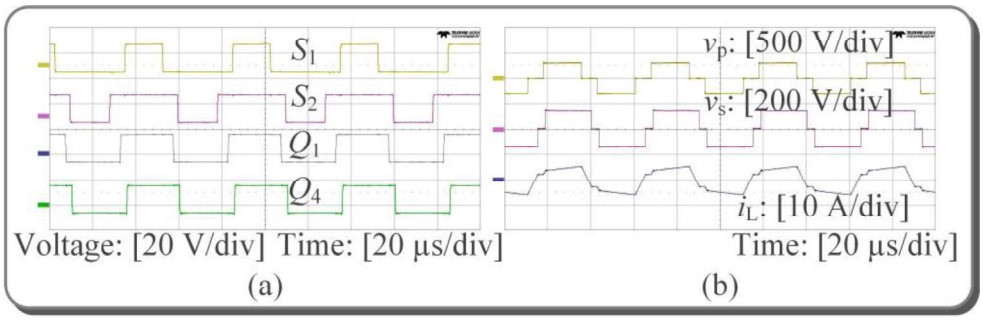


Fig. 3.11 Hardware experiments of the proposed hybrid modulation at 1 kW with (D1, D2) = (0.72, 0.88). (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

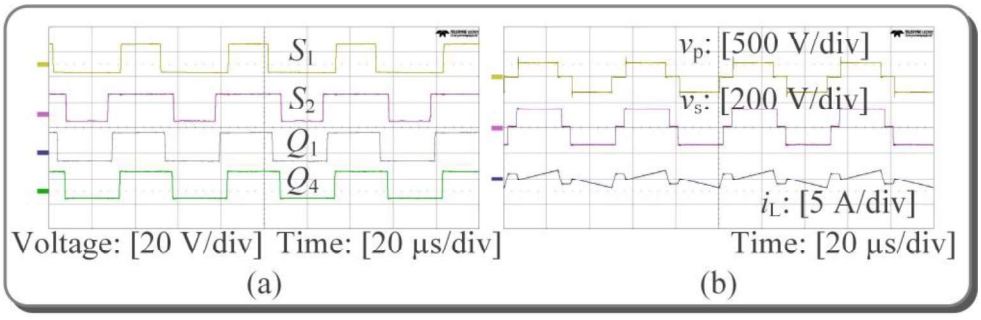


Fig. 3.12 Hardware experiments of the proposed hybrid modulation at 200 W with (D1, D2) = (0.76, 0.86). (a) Gate signal waveforms and (b) v_p, v_s, and i_L waveforms.

3.5.2 Control Diagram

The control diagram, depicted in Fig. 3.9, showcases the control strategy employed in the system. In order to ensure the stability of the output voltage and regulate the power transfer, the third parameter, D_3, is governed by a PI controller. On the other hand, the modulation parameters D_1 and D_2 are manually determined, meaning they are set based on predetermined values or specific requirements. This combination of manual parameter selection and PI control enables effective management of the system's output voltage and power transfer.

3.5.3 Modulation Waveforms in the Steady State

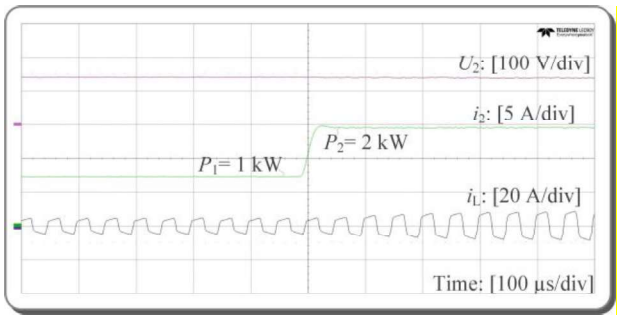
The experimental results presented in Figs 3.10 to 3.12 validate the effectiveness of the proposed hybrid modulation method at different output powers. Fig. 3.10 illustrates the waveforms at 2 kW with (D_1, D_2) = (0.84, 0.90), Fig. 3.11 shows the waveforms at 1 kW with (D_1, D_2) = (0.72, 0.88), and Fig. 3.12 displays the waveforms at 200 W with (D_1, D_2) = (0.76, 0.86). These figures demonstrate the different operating modes achieved under the proposed hybrid modulation as the output power varies from 200 W to 2 kW. Specifically, Mode IV corresponds to the hybrid modulation at 2 kW, Mode II corresponds to the hybrid modulation at 1 kW, and Mode I corresponds to the hybrid modulation at 200 W.

The experimental waveforms align well with the theoretical analysis presented in Section III. It can be observed from Fig. 3.10 to 3.12 that the proposed hybrid modulation effectively adjusts the duty ratio of the primary side SiC MOSFET S_1 and Si IGBT S_2, resulting in a reduction in the on-state time of S_1 and the prevention of high switching-off current in S_2. Additionally, the hybrid modulation introduces a shift in the inner phase angle between the secondary bridges and the outer phase angle between the primary and secondary sides. These experimental results provide empirical validation for the proposed hybrid duty ratio PSM.

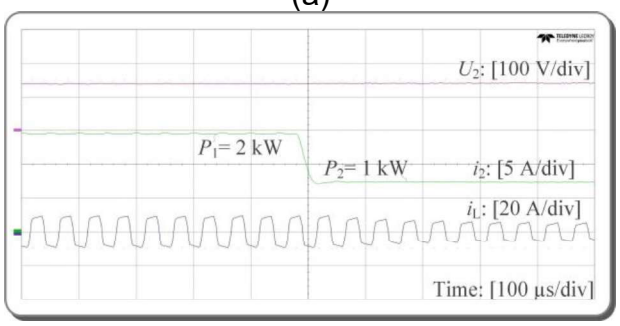
3.5.4 Transition Performance of the Proposed Hybrid Modulation

Fig. 3.13 illustrates the transition performance of the proposed hybrid modulation method when subjected to load changes. It displays the waveforms of the output voltage U_2, output current i_2, and inductor current i_L during transitions from 1 kW to 2 kW and from 2 kW to 1 kW. The experimental results highlight the fast dynamic response of the hybrid modulation method, as it quickly recovers from the load step.

The waveforms demonstrate that the proposed hybrid modulation method effectively adapts to changes in the output power, maintaining stable and well-controlled output voltage and current. The rapid response and recovery observed in the experimental results validate the ability of the hybrid modulation method to handle load variations efficiently, ensuring reliable and consistent performance in dynamic operating conditions.



(a)



(b)

Fig.3.13 Hardware experiments of a transition performance with the proposed hybrid modulation method. (a) Load changes from 1 kW to 2 kW and (b) load changes from 2 kW to 1 kW

3.5.5 Soft Switching Analysis of Proposed Hybrid Modulation

Figs. 3.14-3.16 depict the ZVS operation of the primary Si IGBTs, primary SiC MOSFETs, and secondary SiC MOSFETs under different operating modes. The ZVS operation ensures efficient and reliable switching with reduced switching losses and improved overall converter performance.

In Fig. 3.14, when the output power is 2 kW and the converter operates under Mode IV, ZVS is achieved for all the Si IGBTs and SiC MOSFETs. The intervals where the current passes through the corresponding body diodes are marked, indicating ZVS operation. Specifically, the Si devices S_2, S_7, SiC S_1, and S_8 achieve ZVS simultaneously, while the devices S_3, S_6, S_4, and S_5 also achieve ZVS at the same moment.

In Fig. 3.15, under Mode II, which corresponds to an output power of 1 kW, the primary side Si IGBTs and the secondary side SiC MOSFETs can achieve ZVS conditions. This demonstrates that ZVS operation is maintained for these devices, ensuring efficient switching and minimizing switching losses.

Fig. 3.16 examines ZVS operation under Mode I, corresponding to an output power of 200 W. The waveform shows that ZVS is satisfied for all the SiC MOSFETs and Si IGBTs. The primary Si devices S_2 and S_7 achieve ZVS when they receive the gate signals, while ZVS is ensured for the primary SiC devices S_1 and S_8 due to the inductor current dropping to negative values. Consequently, ZVS conditions are met for all the primary Si IGBTs and secondary SiC MOSFETs under Modes I, II, and IV. For the primary SiC MOSFETs, ZVS can be achieved under both Modes I and IV.

The experimental results confirm the successful implementation of the proposed hybrid modulation method in achieving ZVS operation for the different semiconductor devices involved in the NPC DAB converter. This ensures optimal performance, reduced losses, and enhanced converter efficiency across a range of operating conditions.

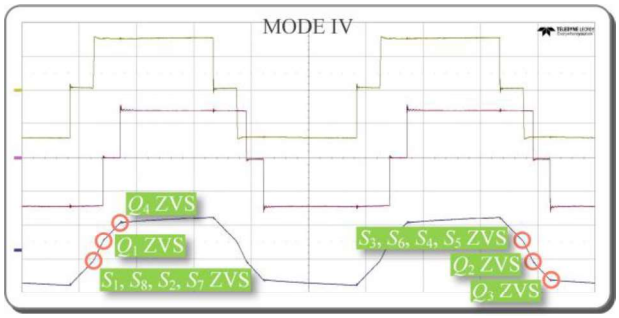


Fig. 3.14 ZVS analysis at 2 kW with modulation Mode IV (0.84, 0.90).

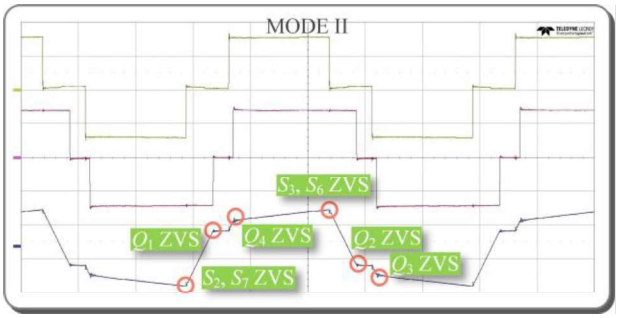


Fig. 3.15 ZVS analysis at 1 kW with modulation Mode II (0.72, 0.88).

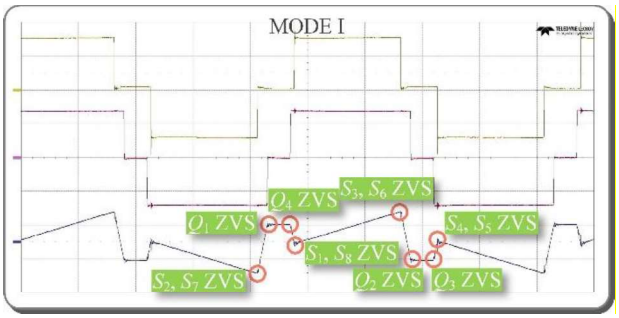


Fig. 3.16 ZVS analysis at 200 W with modulation Mode I (0.76, 0.86).

3.5.6 Efficiency Comparison with TPS Modulation under Different Voltage Gains

The comparison in Fig. 18 demonstrates that the hybrid modulation method outperforms TPS modulation in terms of efficiency. At 2 kW output power, the hybrid modulation achieves an efficiency of 96.7%, while TPS modulation achieves 96.4%. Similarly, at 1 kW output power, the hybrid modulation achieves a higher efficiency of 97.9% compared to TPS modulation.

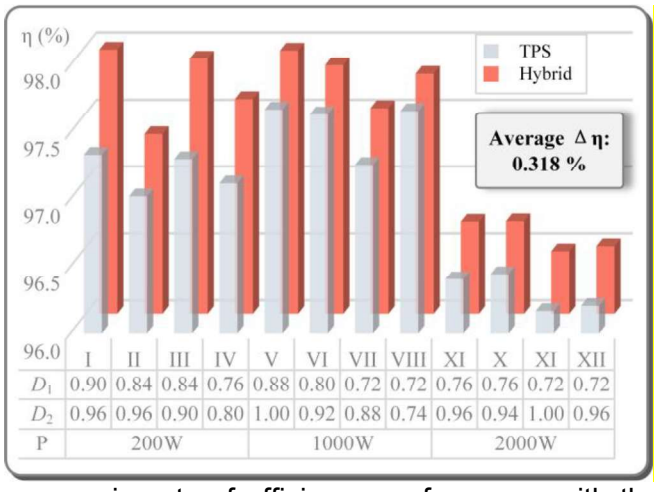


Fig. 3.17 Hardware experiments of efficiency performance with the proposed hybrid modulation and TPS modulation (Input: 300 V; Output:140 V).

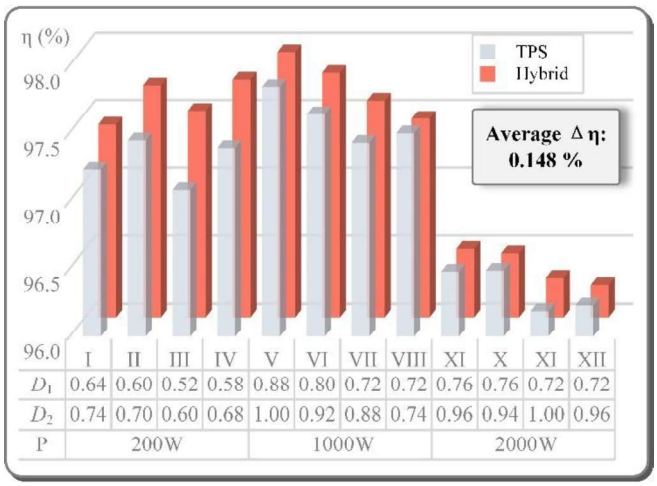


Fig. 3.18 Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 140V).

These findings highlight the advantage of utilizing different duty ratios for the Si IGBTs and SiC MOSFETs in the proposed hybrid modulation. By optimizing the duty ratios, higher efficiency is achieved, surpassing the performance of TPS modulation with fixed duty ratio.

Furthermore, the experimental results demonstrate that the hybrid modulation maintains the highest efficiency even under light load conditions, reaching 97.9%. This efficiency level is 0.5% higher than TPS modulation, indicating the superior performance of the proposed hybrid modulation method.

Overall, these experimental results comprehensively validate the effectiveness of the proposed hybrid modulation method in achieving higher efficiency and support the earlier observation of an average efficiency improvement of 0.318% across all load conditions compared to TPS modulation.

The additional experimental data presented in Figs. 3.18-3.20 provide valuable insights into the relationship between voltage gain and efficiency in the DAB-based topology under both TPS modulation and the proposed hybrid modulation.

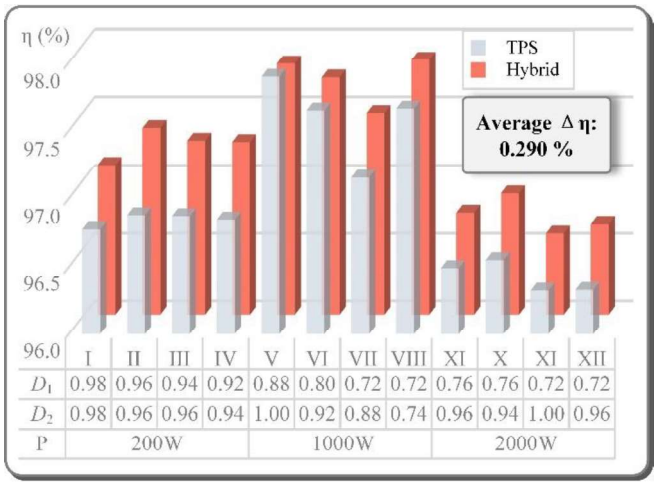


Fig. 3.19 Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 150V).

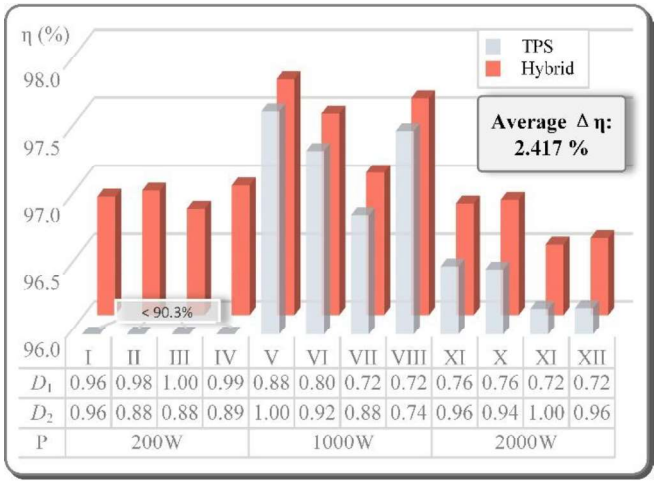


Fig. 3.20 Hardware experiments of the efficiency performance with the proposed hybrid modulation and TPS modulation (Input:300V; Output: 160V).

In Fig. 3.18, the efficiency performance is compared for a 300-V input voltage and 140-V output voltage. The results clearly demonstrate that the hybrid modulation method surpasses TPS modulation in terms of efficiency. At 200 W, the hybrid modulation achieves an efficiency of 97.7%, while TPS modulation achieves 97.4%. At 1 kW, the hybrid modulation reaches the highest efficiency of 98.0% with (D_1, D_2) = (0.88, 1.00). At 2 kW, the hybrid modulation maintains the highest efficiency at 96.5%. The average efficiency improvement across all load conditions is 0.148% compared to TPS modulation.

Similarly, in Fig. 3.19, the efficiency performance is compared for a 300-V input voltage and 150-V output voltage. The results once again confirm the superiority of the hybrid modulation method over TPS modulation in terms of efficiency. At 200 W, the hybrid modulation achieves an efficiency of 97.4%, while TPS modulation achieves 96.8%. At 1 kW, the hybrid modulation reaches the highest efficiency of 97.9% with (D_1, D_2) = (0.88, 1.00). At 2 kW, the hybrid modulation maintains the highest efficiency at 96.9%. The average efficiency improvement across all load conditions is 0.290%.

Fig. 3.20 compares the efficiency performance for a 300-V input voltage and 160-V output voltage. The results further reinforce the effectiveness of the hybrid modulation method. At 200 W, the hybrid modulation achieves an efficiency of 96.9%, while TPS modulation only achieves 90.2%. At 1 kW, the hybrid modulation reaches the highest efficiency of 97.7% with (D_1, D_2) = (0.88, 1.00). At 2 kW, the hybrid modulation maintains the highest efficiency at 96.8%. The average efficiency improvement across all load conditions is a substantial 2.417% compared to TPS modulation.

In conclusion, the experimental results across different voltage gains consistently demonstrate that the hybrid modulation method outperforms TPS modulation in terms of efficiency. The higher efficiency achieved by the hybrid modulation validates the effectiveness of the hybrid duty ratio PSM in optimizing the performance of the DAB-based topology.

3.6 Summary

The proposed hybrid duty ratio PSM method for a Si + SiC NPC DAB topology addresses several issues associated with conventional PSM, such as TPS modulation, and aims to improve the efficiency of the converter. The hybrid modulation approach introduces different duty ratios for the primary Si IGBTs and SiC MOSFETs, resulting in improved performance.

Specifically, the primary Si IGBTs (S_2, S_3, S_6, and S_7) are assigned larger duty ratios, while the primary SiC MOSFETs (S_1, S_4, S_5, and S_8) have shorter duty ratios. This duty ratio optimization reduces the switching loss of the Si devices by minimizing the turn-off current and decreases the conduction loss of the SiC devices by reducing their conduction time.

Additionally, the hybrid modulation enables the adjustment of the outer and inner phase shift angles. The outer phase shift angle controls the phase relationship between the primary side (e.g., S_2) and the secondary side (e.g., Q_1), while the inner phase shift angle governs the inner phase shift angle on the secondary Q_1 and Q_4. By modifying these phase shift angles, the switching behavior can be optimized to reduce losses and improve overall performance.

Furthermore, the hybrid modulation makes full use of the neutral current path for current commutation, which helps minimize losses. The staggered switching time implemented in the hybrid modulation approach prevents potential overvoltage failures that could occur due to disparate switching rates.

The hybrid modulation method has been extensively analyzed and validated using PLECS simulation results. Additionally, experimental results obtained from a 2-kW prototype have demonstrated higher efficiencies across all tested operating conditions. These experimental findings highlight the effectiveness and superiority of the hybrid duty ratio PSM method, showcasing its potential to improve the performance of the Si + SiC NPC DAB topology.

4 Data-Driven Modeling with Experimental Augmentation for the Modulation Strategy of the Dual-Active-Bridge Converter

To alleviate model discrepancy and improve accuracy in practice, this chapter proposes a novel data-driven modeling with experimental augmentation (D2EA), leveraging both simulation data and experimental data.

For the performance modeling of power converters, the mainstream approaches are essentially knowledge-based, suffering from heavy manpower burden and low modeling accuracy. Recent emerging data-driven techniques greatly relieve human reliance by automatic modeling from simulation data. However, model discrepancy may occur due to unmodeled parasitic, deficient thermal and magnetic models, unpredictable ambient conditions, etc. These inaccurate data-driven models based on pure simulation cannot represent the practical performance in the physical world, hindering their applications in power converter modeling.

In D2EA, simulation data aims to establish basic functional landscape, and experimental data focuses on matching actual performance in the real world. The D2EA approach is instantiated for the efficiency optimization of a hybrid modulation for the NPC-DAB converter. The proposed D2EA approach realizes 99.92% efficiency modeling accuracy, and its feasibility is comprehensively validated in 2-kW hardware experiments, where the peak efficiency of 98.45% is attained. Overall, D2EA is data-light and can achieve highly accurate and highly practical data-driven models in one shot, and it is scalable to other applications, effortlessly.

4.1 Introduction

In this chapter, the three-level NPC-DAB converter adopted in [74] is the research target, which consists of two NPC bridge legs integrated by Si and SiC switches in the primary side, and a secondary SiC-based full bridge. For the sake of readability, the circuit diagram presented in Fig. 2.7 is reproduced again in Fig. 4.1. The hybrid switch choice of the NPC-DAB attains high efficiency while still maintaining cost effectiveness [74]. Aiming at enhancing the efficiency performance of the NPC-DAB converter under different circumstances, a hybrid modulation strategy with three degrees of control freedom is investigated to optimize the modulation parameters. As shown in Fig. 4.2, the hybrid modulation

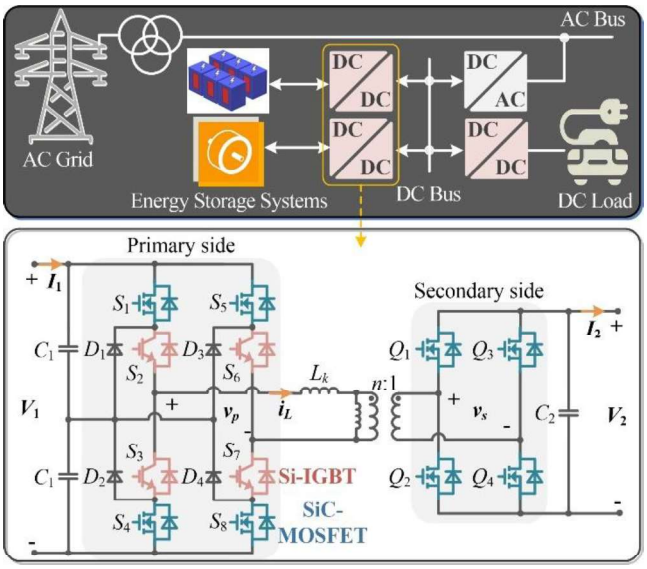


Fig. 4.1 NPC-DAB converters in ESSs.

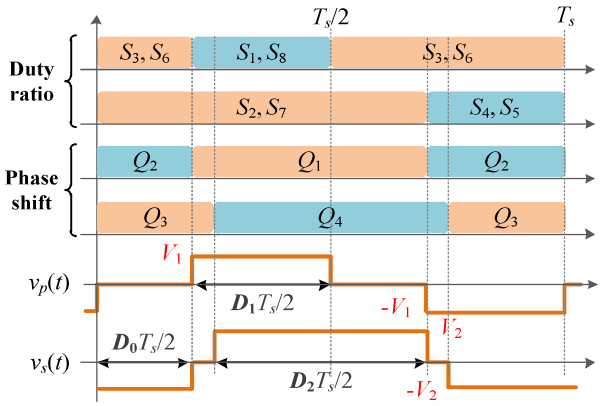


Fig. 4.2 Hybrid modulation for the NPC-DAB converter.

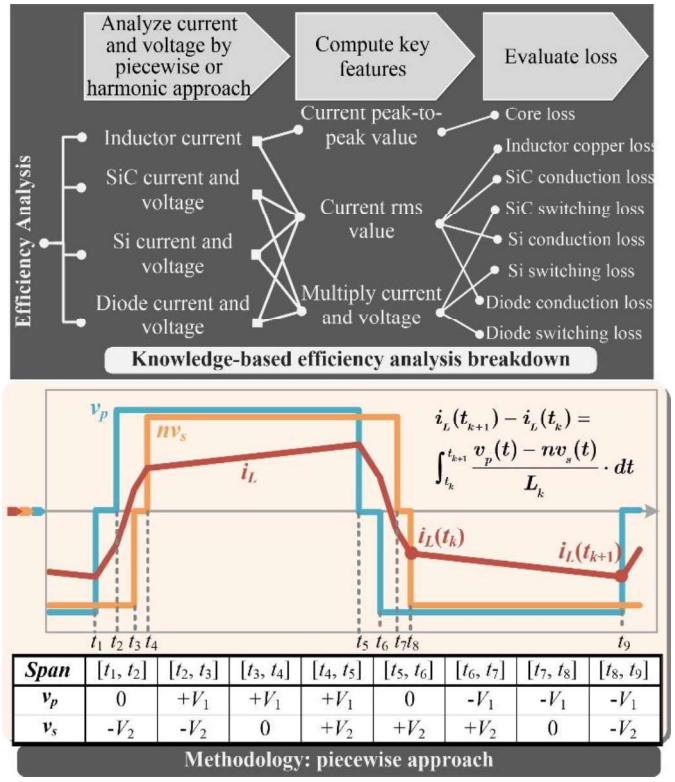


Fig. 4.3 Knowledge-based approach for the efficiency analysis.

employs the duty ratio strategy in the primary NPC bridge and the phase shift strategy in the secondary bridge, including: the outer phase shift D_0 between S_2 and Q_1, the duty ratio D_1 of S_1, and the inner phase shift D_2 between Q_1 and Q_4. The switches in the primary bridge are regulated with variable duty ratio to reduce the turn-off loss [74].

In this respect, the modulation objective should be modeled with the expectation of high modeling accuracy to precisely gauge the operating performance of DAB converters. Generally, the existing modeling approaches can be classified into two main categories, the conventional knowledge-based approach and the emerging data-driven approach.

The knowledge-based modeling method relies on expert knowledge for a thorough understanding of the converter working principles and the modulation behaviors, the human-dependent feature of which leads to low modeling accuracy and heavy manual burden. For example, the piecewise approach adopted in [75]-[77] deduced the ac inductor current segment-by-segment for

all working modes, the high order of which indicates a time-consuming derivation process. The accuracy in [77], [78] was reduced due to the negligence of the inductor resistance and other parasitic parameters. In addition, the harmonic method for the efficiency analysis in [79], [80] smoothed out high-order harmonics to alleviate deduction complexity but sacrificing the modeling accuracy.

The time-consuming efficiency analysis of the NPC-DAB converter under the hybrid modulation with knowledge-based approaches is given in Fig. 4.3. Initially, the current and voltage waveforms of the inductor and switches are analyzed with either piecewise approach or harmonic analysis, based on which some keys features are computed. Detailed losses are then evaluated [81]: the peak-to-peak inductor current evaluates magnetic core losses; inductor copper and device conduction losses are calculated with the current rms value; the voltage and current of devices are multiplied and averaged to evaluate switching losses. This derivation process should be repeated for all working modes, so is undoubtedly tedious considering the complex NPC-DAB topology and the intricate modulation. Moreover, the knowledge-based efficiency modeling can be inaccurate due to the inevitable model simplification and mathematical approximation.

As a step further, latest data-driven approaches for building the models of modulation objectives are the most advanced techniques. Compared to knowledge-based approaches, it can significantly relieve manpower burden, free engineers from tedious and repetitive works, and improve the modeling accuracy [82], [83]. To automatically analyze the current stress of DAB converters under TPS modulation, Li *et al.* trained neural networks (NNs) on the performance data obtained from simulation software [84]. In the efficiency-oriented optimization of TPS modulation, efficiency models have been built with NNs [85]. Besides, data-driven models for ZVS conditions under the hybrid extended phase shift modulation were trained to optimize ZVS range [86]. Outlier detection algorithm has been integrated in the data-driven modeling of the current stress under a hybrid phase shift modulation [87]. The data-driven models in [84]-[87] can realize

higher accuracy since the considerations of switching behavior and more precise circuit components contribute to more realistic simulation. These data-driven approaches, which achieve automation in modeling, are the future tendency to accelerate industrial design cycle.

However, as shown in Fig. 4.4, the existing data-driven methods suffer from two nontrivial drawbacks: data-intensive and model discrepancy. First, the commonly adopted data-driven methods such as neural networks for performance modeling are data-intensive, which require large datasets for training [82], [84]. However, it can be infeasible to acquire such large datasets in the power electronics domains. Second, the data-driven methods that are trained purely on simulation data suffer from model discrepancy, which induces nonnegligible deviations from the actual performance in real-world situations because of the following factors: unmodeled parasitic parameters, imprecise thermal modeling, disregarded physical phenomenon, deficient magnetic modeling, unforeseeable environmental disturbances, fluctuating ambient conditions, etc. For example, the effect of inductance fluctuations can cause divergence in the analysis of gain margin and phase margin in a cascaded power converter system [88]. [89], [90] discussed the negative influence of unmodeled parasitic resistance and capacitance on the state-space model accuracy. Besides, the nonlinearity of magnetic hysteresis loop, the skin and proximity effects under high switching frequency, and poor thermal modeling can bring about deviated loss modeling [91], [92]. In some other research fields, the various sources of data for data-driven modeling has shown the feasibility and superiority in speeding up the modeling process and increase the modeling accuracy [113], [114]. In power engineering field, the simulation data shows the basic function of the circuit design. And experimental data includes the parasitic parameters effect and provide a more precise result, So the simulation data and experimental results can be taken as various sources for data-driven modeling.

Aiming at the shortcomings of the existing approaches, a data-driven modeling with experimental augmentation (D^2EA) is proposed for performance modeling and optimization. The essential idea of D^2EA is to combine both

simulation data and experimental results in the data-driven modeling. It is applied in the efficiency-oriented optimization of the NPC-DAB converter under the hybrid modulation. Generally, D^{2}EA includes three main steps. In Step 1, simulation is built, and hardware experiments are conducted to collect sufficient simulation data and experimental results. Provided the hybrid data pool, Step 2 adopts an ensemble learning algorithm, the extreme gradient boosting (XGBoost) algorithm, to train accurate data-driven models for efficiency. In Step 3, the latest particle swarm optimization with state-based adaptive velocity limit (PSO-SAVL) algorithm is applied to find the best modulation parameters that achieve the optimal efficiency. In D^{2}EA modeling, the simulation data obtained from simulation software and experimental data collected in practice from a hybrid data pool, both of which are indispensable for the data-light and accurate performance modeling. First, the simulation data constructs the basic functional landscape of the modulation objectives, which serves as a time-efficient and cost-effective data source to reduce the amount of experimental data required. Furthermore, the experimental data bridges the gap between the simulation data and real-life implementation, enhancing the practicality of the proposed D^{2}EA approach. The comparisons of different modeling approaches are summarized in Table VII and Fig. 4.4, and the major contributions of this chapter are summarized as follows:

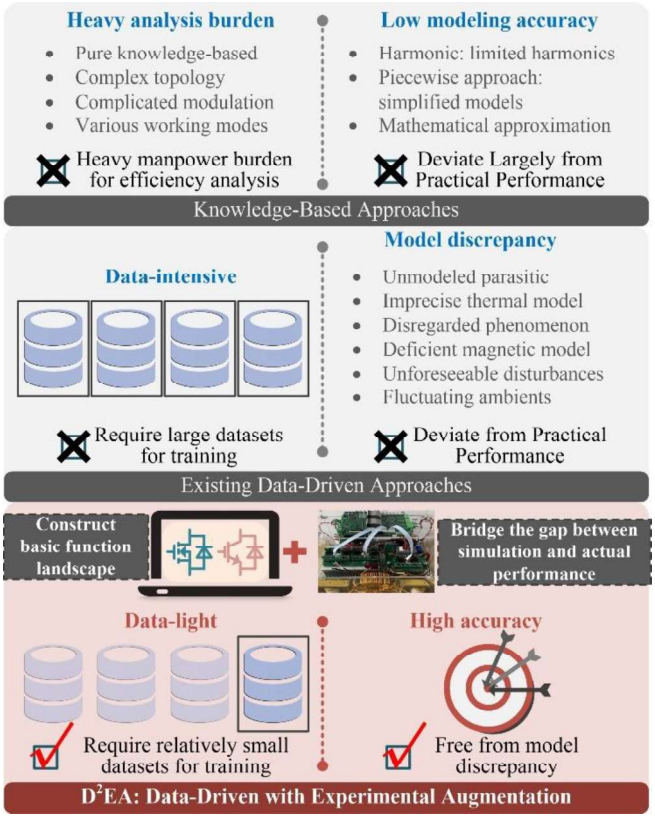


Fig. 4.4 Comparisons among the existing knowledge-based approaches, data-driven approaches, and the proposed D^{2}EA modeling approach.

- The proposed D^{2}EA promotes the existing data-driven approaches for performance modelling in two aspects: First, the D^{2}EA approach is data-light, since both data sources are contributing to the performance modelling, and the adopted XGBoost algorithm requires less training data compared with other data-driven algorithms; Second, the D^{2}EA approach can achieve accurate and practical modeling in one shot, mitigating the needs for repetitive tuning of simulation and data-driven models to match practical situations.

- In terms of the contribution for the application background, with the D^{2}EA approach, the complicated efficiency modeling is automated and high accuracy can be realized. Besides, this chapter initiates the efficiency optimization for the NPC-DAB converter under the hybrid modulation.

TABLE VII

COMPARISONS OF DIFFERENT MODELING APPROACHES

CATEGORY	REFERENCE	MANPOWER BURDEN	DATA SIZE	DEVIATION FROM PRACTICE
Knowledge-Based: Piecewise	[75]–[77], [93]	Large	-	Large
Knowledge-Based: Harmonics	[78]–[80], [94]	Medium	-	Large
Existing Data-Driven	[84]–[87]	Low	Data-intensive	Medium
Proposed D²EA	**This chapter**	**Low**	**Data-light**	**Low**

The organization of this chapter is as follows. Section 4.2 elaborates the methodologies of the proposed D²EA modeling in detail. Section 4.3 studies a design case in a comprehensive way. Hardware experiments presented in Section 4.4 verify the feasibility of the proposed D²EA. In Section 4.5, the conclusion of the chapter is summarized.

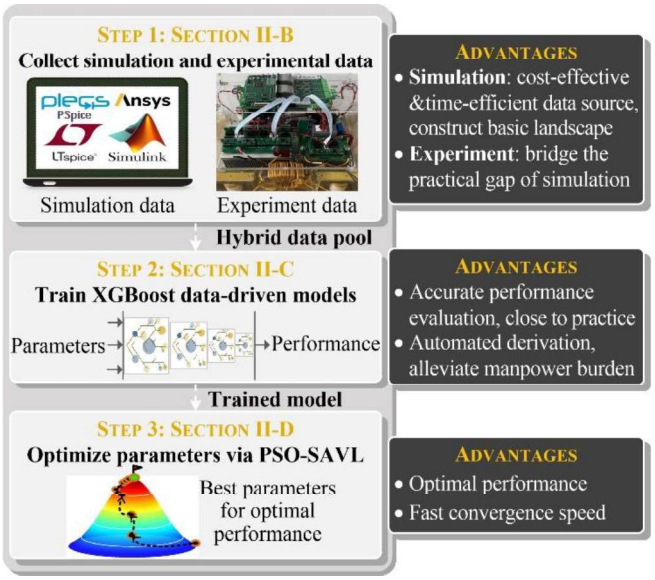


Fig. 4.5 Flowchart of the proposed D²EA modeling approach.

4.2 Methodology of Proposed D^{2}MA Modeling

In this section, the methodology of the proposed D^{2}EA modeling is comprehensively illustrated. D^{2}EA is a universal modeling approach which can be extensively applied to various converter circuits, modulation strategies, and applications. For illustrative purposes, the proposed D^{2}EA approach is applied to shed lights on the efficiency-oriented optimization for the NPC-DAB converter under the hybrid modulation.

4.2.1 The Proposed D^{2}EA Modelling Approach

The design process is shown in Fig. 4.5, which consists of three main steps. First, simulation models are run, and hardware experiments are carried out to collect sufficient simulation data and experimental performance, respectively. Second, utilizing the hybrid data pool of simulation data and experimental data, two XGBoost-based data-driven models are consecutively trained to deliver accurate evaluation of actual efficiency performance in the physical world. In Step 2, one initial XGBoost model constructs a basic functional landscape, and a subsequent XGBoost model bridges the accuracy gap to compensate for the simulation model discrepancy. Third, the PSO-SAVL algorithm interacts with the trained XGBoost models to achieve the optimal efficiency over the entire working ranges.

Generally, the proposed D^{2}EA modeling is implemented in a high level of design automation, freeing human experts from complicated, time-consuming, and error-prone process of performance derivation and parameter optimization.

4.2.2 Step 1: Collect Simulation and Experimental Data

As a preliminary preparation, the design specifications such as the performance to optimize, parameters to consider, and working conditions are determined. In this chapter, the values of duty ratio (D_1) and inner phase shift (D_2) should be designed under various load conditions (P_L) to optimize efficiency. Hence, the parameters incorporate D_1, D_2, and P_L, and the modulation objective is the optimal efficiency.

Thereafter, in Step 1, simulation models are built and run for sufficient number of times to collect performance data. The simulation data is responsible for establishing the basic functional relationships between design parameters and performance.

To mitigate the negative impact brought by mismatched simulation models, experimental data is collected in real-world situations, which is used in the D^2EA data-driven modeling for approaching practical performance. The experimental data contributes to a more complete data pool.

Both simulation data and experimental data are necessary to guarantee the satisfactory modeling accuracy. Simulation results reduce the number of experiments required through generating a basic functional landscape, fostering the data-light merit of the proposed D^2EA approach. Experimental data further improves the modeling accuracy. Another merit of D^2EA is that the repetitious tuning of models to match practical situations in the existing approaches based on pure simulation is avoided, and promising data-driven models with high accuracy and high practicality can be trained in one shot. After Step 1 of the proposed D^2EA modeling, a hybrid data pool is generated.

4.2.3 Step 2: Train Data-Driven Models of Efficiency via the XGBoost Algorithm

Step 2 of the proposed D^2EA modeling automatically learns the functional relationships between the considered parameters and the modulation objective through the XGBoost algorithm. XGBoost is a popular ensemble learning algorithm [95], which utilizes a set of weak decision trees to learn the target. In the power electronics domain of performance modeling in this chapter, XGBoost algorithm is chosen because of its easily scalable structure, fast computation speed, simple implementation, etc. First, XGBoost model is flexible structure-wise, and its learning capacity can increase by simply stacking more base models, which is more powerful than conventional machine learning algorithms such as support vector machine [86]. Second, XGBoost model can be parallelly applied during the inference stage, justifying its fast inference speed.

Furthermore, XGBoost algorithm is simple to implement since it has few hyperparameters to adjust to find the optimal structure.

To attain high accuracy and high practicality and coordinate with the hybrid data pool, two XGBoost models are consecutively trained. XGBoost-I model forms landscape basis, and XGBoost-II model bridges the accuracy gap between simulation and experiments to avoid model discrepancy.

The training of the XGBoost models is accomplished with the sequential gradient boosting strategy shown in Fig. 4.6, where there are L_1 and L_2 decision trees in XGBoost-I and XGBoost-II, respectively. For the training of XGBoost-I, the subsequent decision tree is trained on the residual $o_{l,sim}^*$, as expressed in (4) and (5). $o_{l,sim}^*$ represents the difference between the ground-truth objective o_{sim}^* (simulation efficiency η_{sim}) and the aggregate sum of all the previous decision trees from 1 to l-1. For the l^{th} tree, it receives $o_{l\text{-}1,sim}^*$ to calculate the l^{th} residual $o_{l,sim}^*$, and its adjustable weights $\theta_{l,sim}$ are tuned to minimize the difference between $o_{l,sim}^*$ and the output $y_{l,sim}$, as shown in Fig. 4.5 and (4). Afterwards, the resulting error between $o_{l,sim}^*$ and $y_{l,sim}$ is provided to the next $(l+1)^{th}$ tree for training. This recurrent boosting-based training process is repeated for L_1 decision trees. Thereafter, the XGBoost-II model is similarly trained as formularized in (6) and (7), where the ground-truth objective o_{gap}^* denotes the gap between experimental efficiency η_{exp} and the results from XGBoost-I to mitigate model discrepancy.

Besides, the performance evaluation utilizes the trained XGBoost-I and XGBoost-II models to infer the efficiency of the given input parameters (D_1, D_2, P_L), as expressed in (8).

In this chapter, the inputs of XGBoost models include D_1, D_2, and P_L, which can be extended to consider other impactful parameters, and the key point is to acquire training data which can properly represent the considered application scenarios. As shown in Fig. 4.7, the input variables of the D^{2}EA modeling can be extended to incorporate modulation parameters, operating conditions, and circuit parameters. For instance, the effects of output power P_L, voltage

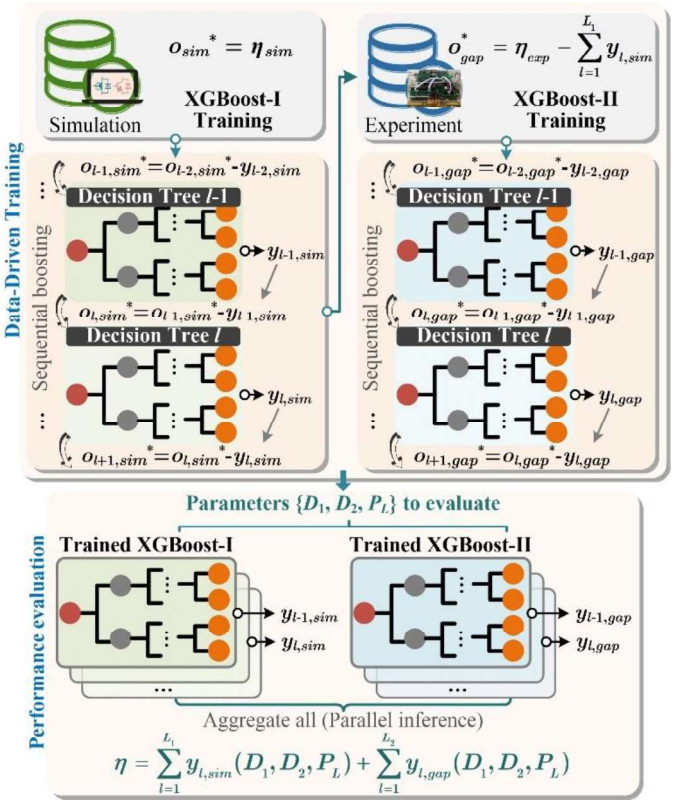


Fig. 4.6 Training and inference of the XGBoost algorithm.

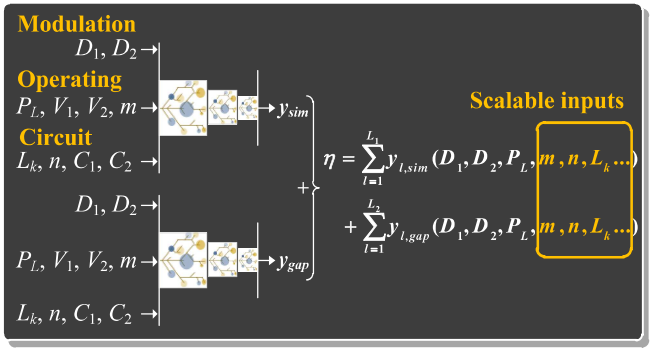


Fig. 4.7 XGBoost models considering other impactful parameters.

conversion ratio *m*, and the fluctuation of circuit parameters can be considered in the efficiency modeling.

With Step 2 of the proposed D^{2}EA modeling, data-driven XGBoost models are properly trained, serving as the surrogate models for the efficiency of the NPC-DAB converter under the hybrid modulation. Being informed of both simulation data and experimental performance in practice, the XGBoost models can provide accurate and practical efficiency evaluation, which improves the utility

of the proposed D^{2}EA approach.

$$\min_{\theta_{l,sim}}\left(obj_{l,sim}\right)=\min_{\theta_{l,sim}}\left(o^{*}_{l,sim}-y_{l,sim}\right)^{2},l=1,\ldots,L_1 \tag{4}$$

$$o^{*}_{l,sim}=o^{*}_{l-1,sim}-y_{l-1,sim}=o^{*}_{sim}-\sum_{i=1}^{l-1}y_{i,sim}=\eta_{sim}-\sum_{i=1}^{l-1}y_{i,sim} \tag{5}$$

$$\min_{\theta_{l,gap}}\left(obj_{l,gap}\right)=\min_{\theta_{l,gap}}\left(o^{*}_{l,gap}-y_{l,gap}\right)^{2},l=1,\ldots,L_2 \tag{6}$$

$$o^{*}_{l,gap}=o^{*}_{l-1,gap}-y_{l-1,gap}=o^{*}_{gap}-\sum_{i=1}^{l-1}y_{i,gap}=\eta_{exp}-\sum_{i=1}^{L_1}y_{i,sim}-\sum_{i=1}^{l-1}y_{i,gap} \tag{7}$$

$$\eta=y_{sim}+y_{gap}=\sum_{l=1}^{L_1}y_{l,sim}(D_1,D_2,P_L)+\sum_{l=1}^{L_2}y_{l,gap}(D_1,D_2,P_L) \tag{8}$$

4.2.4 Step 3: Search for Optimal Modulation Parameters via the PSO-SAVL Algorithm

In Step 3, a latest PSO variant, PSO-SAVL, is chosen to search for the optimal modulation parameters to reach the best efficiency over the entire operating ranges. Compared with the conventional PSO algorithm, PSO-SAVL adaptively adjusts the velocity limit of particles to match the evolutionary state of population, which improves the global exploration capability and the convergence speed. The superiority of the adopted PSO-SAVL is theoretically and empirically validated in [96].

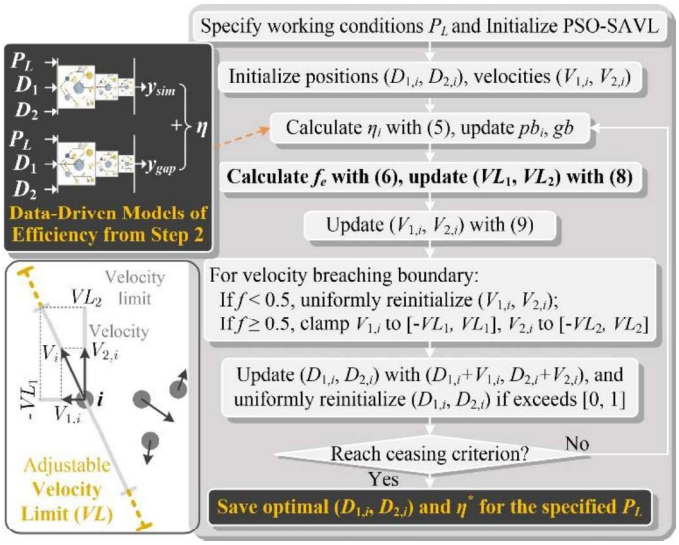


Fig. 4.8 Flowchart of the PSO-SAVL algorithm for optimizing modulation parameters to achieve the best efficiency.

$$f_e = (d_g - d_{min})/(d_{max} - d_{min}) \tag{9}$$

$$d_i = \sum_{j=1, j\neq i}^{N} \sqrt{\left(D_{1,i} - D_{1,j}\right)^2 + \left(D_{2,i} - D_{2,j}\right)^2} /(N-1) \tag{10}$$

$$VL = X_{max}/(1 + (1/vl_{min} - 1)\exp\left(\ln((1/vl_{min} - 1)/(1/vl_{min} - 1))f_e\right)) \tag{11}$$

$$V_i = \omega V_i + c_1 r_1 (pb_i - X_i) + c_2 r_2 (gb - X_i) \tag{12}$$

The flowchart of PSO-SAVL is shown in Fig. 4.8. In the beginning, the load conditions P_L and the algorithm hyperparameters including particle number N, velocity inertia ω, velocity limit coefficients vl_{max}, vl_{min}, and learning factors c_1, c_2 are initialized. Position X_i (i.e., $D_{1,i}$, $D_{2,i}$) and velocity V_i (i.e., $V_{1,i}$, $V_{2,i}$) are uniformly initialized. Practical efficiency performance η in physical world is evaluated through interfacing the trained XGBoost models from Step 2, and the global best position gb and historical best position pb_i are updated. Hereafter, f_e which measures the evolutionary state of particles is computed to tune the velocity limit VL (i.e., VL_1, VL_2), as shown in (9), (10), and (11), where X_{max} is

the position boundary, d_g is the d_i value of the best particle, and d_{min}, d_{max} are the minimum and maximum d_i values. The velocity V_i of each particle is then adjusted with (12) and restricted by the new VL, and the adjusted V_i is used next for relocating the particles. This process repeats until the maximum iteration is met.

In summary, with the assistance of PSO-SAVL algorithm, Step 3 finds the optimal modulation parameters to achieve the best efficiency over the entire load range.

4.2.5 Strategies to Tune the Hyperparameters of XGBoost Models and the PSO-SAVL Algorithm

The strategies and insights in selecting the hyperparameters of the XGBoost models and the PSO-SAVL algorithm are revealed. To tune the hyperparameters of XGBoost for high modeling accuracy, the collected data is partitioned into training, test, and validation sets. The potential hyperparameter values are enumerated and the ones with the highest accuracy on the test set are selected as the optimal hyperparameters. In terms of PSO-SAVL algorithm, the hyperparameters discussed in Subsection 4.2.4 are adjusted to achieve a proper balance between global exploration and local exploitation [96].

4.3 Design Case with Proposed D^{2}MA Modeling

Section 4.3 discusses a design case given by the proposed D^{2}EA modeling approach in a step-by-step manner. Subsections 4.3.1, 4.3.2, and 4.3.3 elaborate the settings and results of Step 1, Step 2, and Step 3, respectively. Subsections 4.3.4 sheds light on the computational costs required for the D^{2}EA modeling.

4.3.1 Step 1: Collect Simulation and Experimental Data

Design specifications that provide operating boundaries for simulation and experiments are summarized in Table VIII. In this chapter, considering the application of ESSs shown in Fig. 4.1, the input and output voltages are fixed,

which are regulated by the ESSs and DC bus, respectively. Other design specification such as the switching frequency is not limited to the selected value 20 kHz, and other values can be adopted with slight modifications in the initial data acquisition step.

TABLE VIII

DESIGN SPECIFICATIONS

Working Conditions			
Input voltage V_{1R}	300 V	Output voltage V_{2R}	140 V
Rated power P_{LR}	2 kW	Frequency f_s	20 kHz
Semiconductor Switches			
Si-IGBT	IKW40N65ES5	SiC-MOSFET	UF3C065030K4S
Clamping diode	APT30DQ60BG	Dead time	400 ns
Magnetics			
Duty ratio n:1	2:1	External inductance L_k	236 μH
Ranges of Parameters			
Primary duty ratio D_1	[0, 1]	Inner phase shift D_2	[0, 1]
Outer phase shift D_0	[0, 1]	Output power P_L	[200 W, 2 kW]

In Step 1, a closed-loop simulation model is built in PLECS, as shown in Fig. 4.9. The output of the PI controller is the outer phase shift D_0 between the primary side and the secondary side, which regulates the power transfer. To generate sufficient simulation data, within the ranges of three parameters D_1,

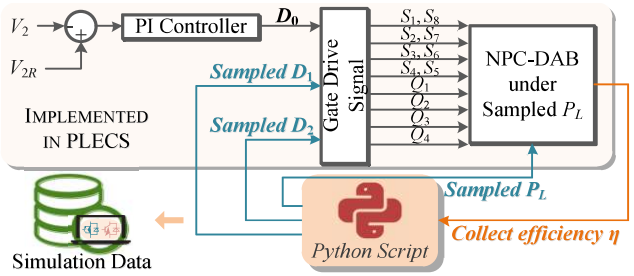


Fig. 4.9 Closed-loop simulation conducted by python script for all sampled D_1, D_2, and P_L.

D_2, and P_L, 25, 25, and 20 number of samples are evenly selected, respectively. Hence, the PLECS simulation is repetitively run for the chosen parameter values to collect 12,500 simulation data automatically using python scripts.

During the automated running of simulation, hardware experiments are conducted to collect practical efficiency performance for mitigating the deviation between simulation and practice in step 2. The experimental platform and the built hardware prototype are shown in Fig. 3.8. In the design case, there are totally 1000 experimental data collected for various values of D_1, D_2, and P_L.

4.3.2 Step 2: Train Data-Driven Models of Efficiency via the XGBoost Algorithm

Given the hybrid pool of simulation data and experimental data, Step 2 of the proposed D^{2}EA approach trains XGBoost models to learn the underlying relationships between the design parameters (D_1, D_2, P) and the efficiency η to be optimized.

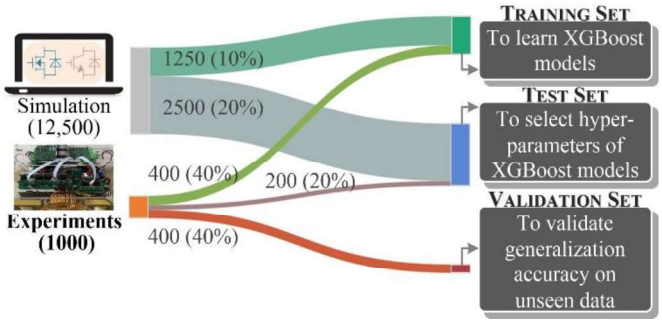


Fig. 4.10 Partitions of simulation and experimental data.

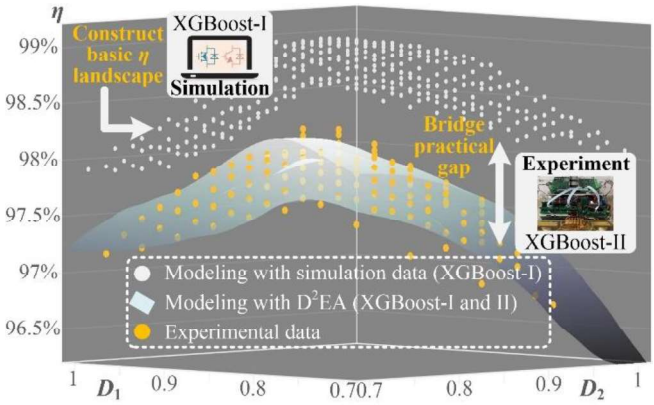


Fig. 4.11 Modeling with D^{2}EA under 1 kW output power.

By following the training process in Fig. 4.6, XGBoost surrogate models for efficiency are automatically trained, the settings of which are summarized in Table IX. The collected 12,500 simulation data and 1000 experimental data are partitioned into three datasets for training the XGBoost models, refining modeling accuracy, and validating the generalization capability, respectively, as displayed in Fig. 4.10.

The modeling results of Step 2 are intuitively shown in Fig. 4.11, verifying the utility of both simulation data and experimental data. In Fig. 4.11, the yellow scattered dots are the experimental results captured in hardware experiments, the white scatted dots are the efficiency predictions of XGBoost-I (trained purely on simulation data), and the transparent surface indicates the accurate efficiency modeling of D^2EA, which combines both XGBoost-I and XGBoost-II. As can be seen, XGBoost-I constructs a basic functional landscape of the efficiency, the shape and trend of which are similar to the actual performance behavior. However, XGBoost-I suffers from model discrepancy, as the average

TABLE IX

SETTINGS OF EXTREME GRADIENT BOOSTING MODELS

	Training Set	Test Set	Validation Set
Simulation data	1250 (10%)	2500 (20%)	8750 (70%)
Experimental data	400 (40%)	200 (20%)	400 (40%)
XGBoost Specifications			
Inputs	D_1, D_2, P	Outputs	Efficiency η
Hyperparameters of XGBoost-I			
Max tree height	11	Number of trees	140
L2 regularization	1.0	Learning rate	0.05
Hyperparameters of XGBoost-II			
Max tree height	9	Number of trees	94
L2 regularization	0.01	Learning rate	0.1

difference between the modeling with only simulation data and the experimental data is around 1.1%, which is a nontrivial gap. XGBoost-II, which is trained on experimental data, significantly bridges the gap between the simulation results and the experimental performance. With both XGBoost-I and XGBoost-II, the data-driven models with D^{2}EA can precisely evaluate the practical efficiency of the NPC-DAB converter in the physical world.

Furthermore, to quantitatively validate the high accuracy and practicality of the proposed D^{2}EA, Fig. 4.12 compares the modeling accuracy of three approaches on experimental data. If only simulation data is used for modeling, the average percentage difference is more than 1%, which is a nonnegligible gap for efficiency modeling. Although the efficiency modeling with only experimental data can decrease the error to 0.58%, the D^{2}EA approach attains 99.92% average percentage accuracy on validation dataset by leveraging both simulation and experimental data.

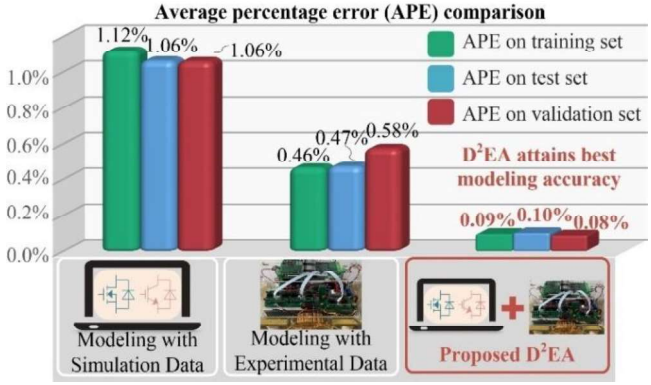


Fig. 4.12 Accuracy comparison (on experimental data) among three modeling approaches: Modeling with only simulation data, modeling with only experimental data, and modeling with the proposed D^{2}EA.

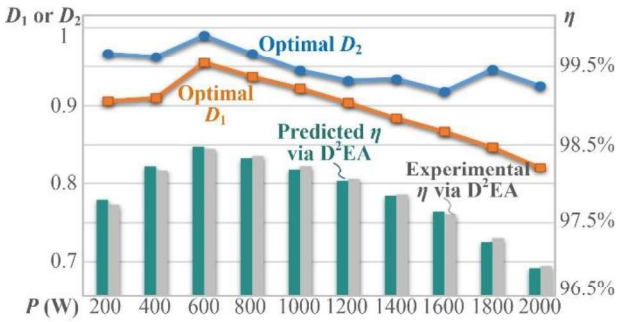


Fig. 4.13 Optimal D_1 and D_2 for the entire load range and accuracy comparison on optimal points.

4.3.3 Step 3: Search for Optimal Modulation Parameters via the PSO-SAVL Algorithm

Utilizing the PSO-SAVL algorithm in Fig. 4.8, Step 3 finds the optimal values of D_1 and D_2 to achieve the best efficiency for various load conditions P. Configurations of the adopted PSO-SAVL are summarized in Table X. The outcomes of Step 3 are shown in Fig. 4.13, based on which D_1 and D_2 are adjusted in real time to achieve optimal efficiency under varying load conditions. The difference between the predicted efficiency via D^{2}EA and the experimental efficiency in physical world is trivial, validating the high modeling accuracy and high practicality of the proposed D^{2}EA modeling approach.

TABLE X
Settings of PSO-SAVL Algorithm

Inputs	Trained data-driven surrogate models XGBoost-I $y_{sim}(D_1, D_2, P)$ and XGBoost-II $y_{gap}(D_1, D_2, P)$ from Step 2
Outputs	Optimal D_1, D_2 and the highest efficiency η^* for given P
Population size	10
Total number of iterations	50
Velocity limit coefficients	vl_{min} = 0.05; vl_{max} = 0.2
Learning factors	$c_1 = c_2 = 2.05$
Weight inertia factor	ω decreases from 0.9 to 0.1

4.3.4 Computational Costs of the Proposed D^{2}EA Modeling

One major merit of the proposed D^{2}EA approach is that the model building process and modulation optimization are automated with computer platforms, which greatly alleviates human involvements and largely accelerates design cycle. To disclose the computational costs, the average implementation time and CPU utilization of each step of D^{2}EA are recorded in Table XI, where the

TABLE XI

COMPUTATIONAL COSTS OF EACH STEP OF D^{2}EA

Main Step	Average CPU Time	CPU Utilization
Step 1: Collect simulation and experimental data	9 hours and 17 minutes	20.2%
Step 2: Train data-driven models of efficiency	1 minute 54.7 seconds	68.9%
Step 3: Search for Optimal Modulation Parameters	12 minutes 25 seconds	43.9%

workstation configures a 4-core Intel Xeon processor E5-1630 with 16 gigabytes RAM. The collection of simulation and experimental data occupies the majority of implementation time, while the training of data-driven models exhibits the highest average CPU utilization.

4.3.5 Comparison of Modelling Accuracy

The data-light merit of the proposed D^{2}EA approach is empirically verified. The comparison results between D^{2}EA and other popular data-driven algorithms are summarized in Fig. 4.14. All the compared algorithms are run 30 times on experimental data, where the dotted lines represent the average modeling accuracy of different algorithms, and the areas denote the variation of modeling accuracy. From Fig. 4.14, the D^{2}EA approach achieves the highest and the most robust modeling accuracy in all data sizes, and the accuracy reaches 99.88% with only 10% of data, justifying the data-light merit.

4.4 Design Case with the Proposed D^{2}EA Modeling

This section holistically presents hardware experimental results to verify the feasibility of the proposed D^{2}EA modeling approach. The operating conditions are given in Table VIII, and the hardware platform is shown in Fig. 3.8.

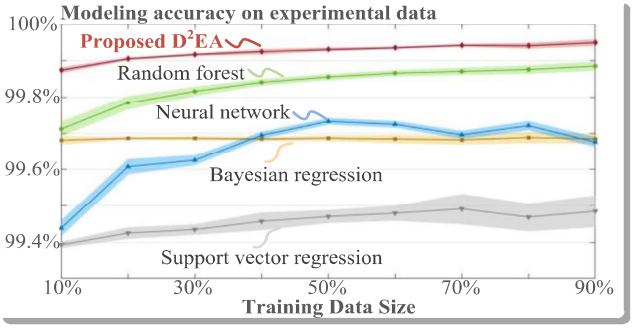
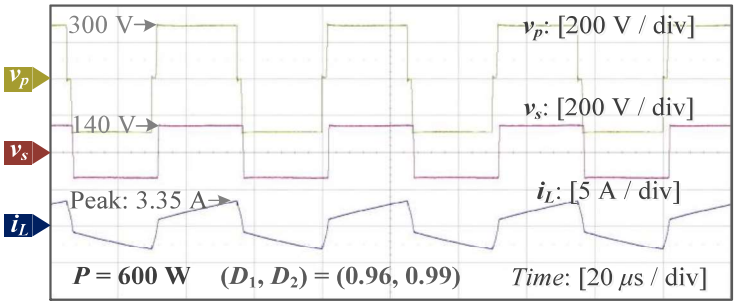


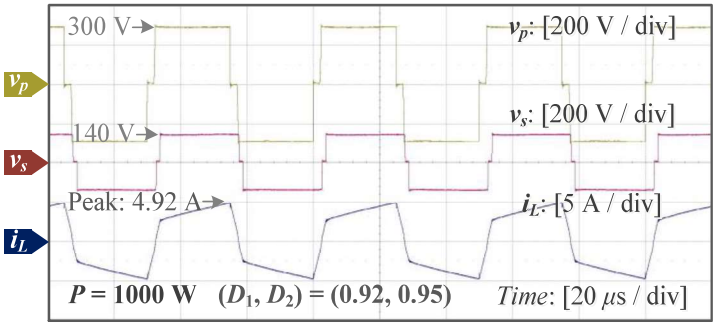
Fig. 4.14 Comparison of the modeling accuracy on experimental data among the proposed D²EA approach, SVR, BR, RF, and NN.

4.4.1 Steady-State Waveforms

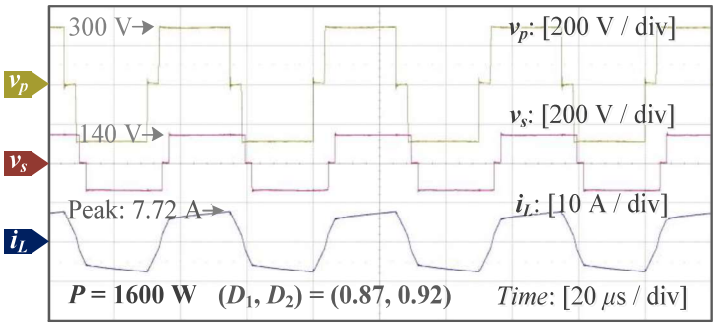
To comprehensively validate the steady-state operations over the entire load range, 600 W (30% load), 1000 W (50% load), and 1600 W (80% load) are analyzed as examples, which represent light, medium, and heavy load levels, respectively. As high-frequency ac voltages v_p, v_s and current i_L shown in Fig. 4.15, D_1 and D_2 values are adjusted to the optimal values in Fig. 4.13 to reduce reverse current and improve efficiency by introducing adequate amount of zero-level voltage plateaus.



(a)

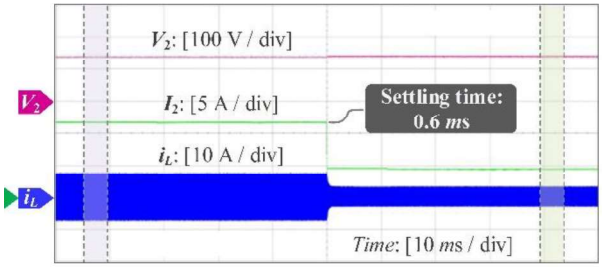


(b)

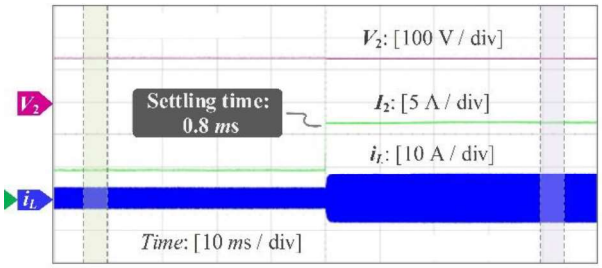


(c)

Fig. 4.15 Steady-state waveforms of: (a) 600 W, (b) 1000 W, (c) 1600 W.



(a)



(b)

Fig. 4.16 Dynamic response waveforms when: (a) *P* changes from 1600 W to 600 W, (b) *P* changes from 600 W to 1600 W.

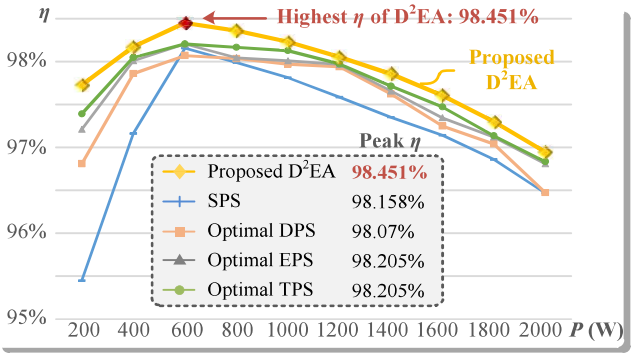


Fig. 4.17 Efficiency comparisons among the D²EA, SPS, optimal DPS, optimal EPS, and optimal TPS.

4.4.2 Dynamic Response of Load Step

Fig. 4.16 shows the dynamic response of the optimal hybrid modulation when load steps are injected. The output voltage is robustly controlled, and the transient settling time is less than 1 ms.

4.4.3 Comparison of Efficiency Performance

The superiority of the proposed D^{2}EA approach compared with other modulation strategies is experimentally validated, as shown in Fig. 4.17. The proposed D^{2}EA approach achieves the highest efficiency 98.45% at P = 600 W, and it is significantly better than SPS and optimal DPS modulation by 0.293% and 0.381%, respectively. Compared with the advanced strategies, optimal EPS and optimal triple TPS modulation, D^{2}EA achieves higher efficiency consistently, and the peak efficiency is improved by 0.246%.

To demonstrate the high efficiency obtained with the D^{2}EA approach, detailed loss breakdown charts are provided in Fig. 4.18. Under light load conditions of P = 600 W, the switching and conduction losses of the secondary bridge are the main losses. With the increasing power level, the percentage of the losses of secondary bridge decreases, while that of inductor and transformer losses increase. The percentage of the losses of the primary NPC bridge is less than that of the secondary bridge.

Besides, benefiting from the high accuracy and practicality of the D^{2}EA modeling, the optimized modulation values D_1 and D_2 from D^{2}EA will achieve better efficiency compared with those from the modeling with simulation data only and the modeling with experimental data only. Fig. 4.19 presents the comparison results, where D^{2}EA attains higher efficiency than the optimized hybrid modulation with simulation-based modeling and experiment-based modeling by 0.243% and 0.236%, respectively.

4.4.5 Verification of Optimality

Aiming at proving the optimality of the modulation values obtained from the proposed D^{2}EA approach, the experimental efficiency results of adjacent D_1 and D_2 values near the optimized values are measured, as shown in Fig. 4.20 Under various load conditions, D^{2}EA can precisely locate the optimal efficiency areas, validating the optimality.

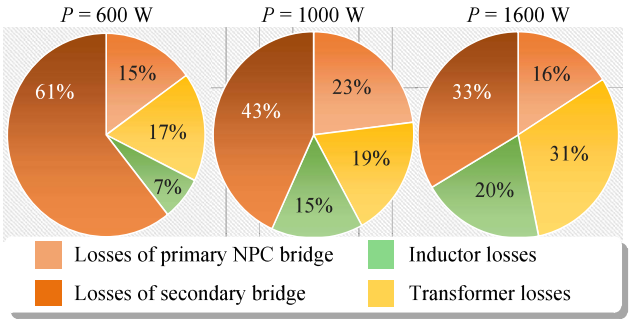


Fig. 4.18 Loss breakdown when load power is 600 W, 1000 W, and 1600 W.

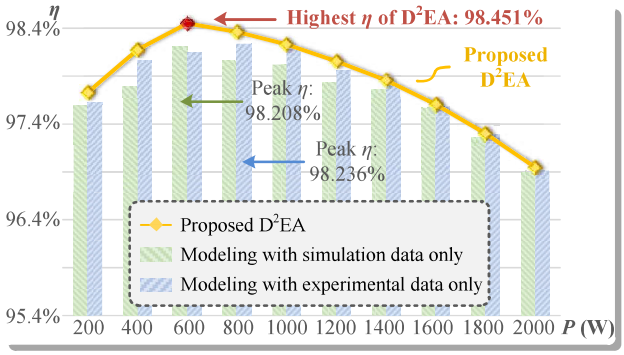
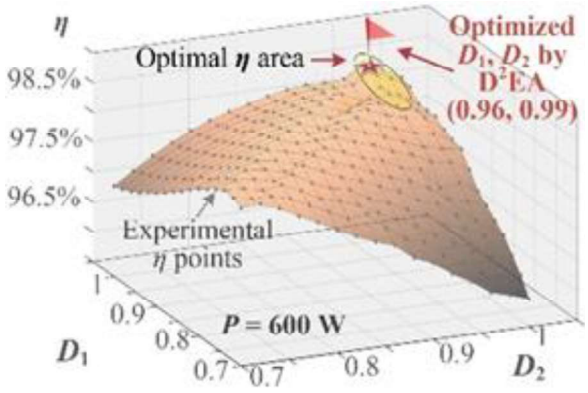
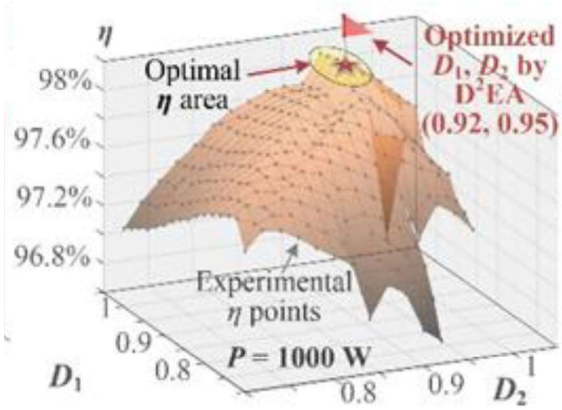


Fig. 4.19 Efficiency comparisons among the D^{2}EA, the optimized hybrid modulation via simulation-based modeling, and the optimized hybrid modulation via experiment-based modeling.



(a)



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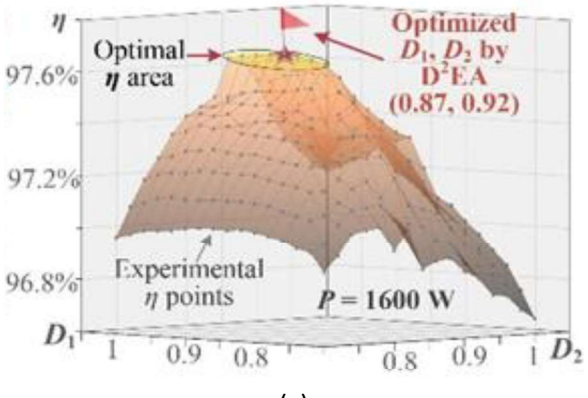


(c)

Fig. 4.20 Validation of optimality under different output power. (a) 600 W; (b) 1000 W; (c) 1600 W.

With the comprehensive experiments in Subsection 4.4, the feasibility of the proposed D^{2}EA method is verified.

4.5 Summary

Striving to conquer the challenges in the mainstream knowledge-based and latest data-driven approaches for performance modeling, this chapter has proposed a novel D^{2}EA. In D^{2}EA, the simulation data serves as cost-effective and time-efficient data source to construct basic functional landscape. While the augmentation of experimental data contributes to bridging the gap between the data-driven surrogate models and practical performance in physical world, alleviating model mismatch. In comparison with the existing data-driven approaches, the proposed D^{2}EA approach is data-light, and the built performance models are highly accurate and practical, free from model discrepancy.

The application of D^{2}EA focuses on the efficiency-oriented optimization of a hybrid modulation for NPC-DAB converters in energy storage systems. D^{2}EA can be effortlessly extended to other application scenarios. Overall, it consists of three steps. In Step 1, simulation is automatically run, and hardware experiments are conducted to collect both simulation and experimental data. In Step 2, the advanced extreme gradient boosting algorithm trains accurate data-driven models for the design performance. Two XGBoost data-driven models are consecutively trained by leveraging residuals to produce practical efficiency evaluation. In Step 3, a latest PSO variant searches for the optimal modulation parameters to realize the best efficiency over the entire load range.

Experiments on a 2-kW hardware prototype comprehensively validate the high modeling accuracy and high practicality and thus prove the effectiveness of the proposed D^{2}EA modeling method. In the design case, via the proposed D^{2}EA approach, the modeling accuracy for efficiency achieves 99.92%. Moreover, the efficiency performance optimized via the D^{2}EA is consistently better than other advanced modulation strategies, and the highest efficiency reaches 98.45%.

5 Data-driven Optimization for Neutral-Point-Clamped Dual-Active-Bridge Converter with Zero-Voltage-Zero-Current Switching

5.1 Introduction

The hybrid SiC + Si NPC DAB converter introduced by Dong et al. in [74], presents a compelling advantage by striking a favorable balance between cost and efficiency when compared to Si IGBT-based NPC DAB and full SiC MOSFET-based NPC DAB converters. Despite its promising characteristics, the optimization of the hybrid NPC DAB converter has not been thoroughly explored.

For optimization purposes, two popular objectives in converter modeling are achieving ZVZCS and improving efficiency performance. Attaining ZVZCS is crucial as it ensures minimal switching losses in semiconductors, which is particularly important for high-frequency and high-power applications. Increasing efficiency of power converter can help simplify the thermal system design and make the converter more cost friendly. Moreover, both these objectives contribute to the reduction of electromagnetic interference noise, ultimately enhancing the reliability of the controller and gate driver circuit.

To achieve optimized performance, the proposed hybrid duty-ratio PSM helps to reduce the conduction time for SiC MOSFETs and alleviates current stress on Si IGBTs [102], it is essential to model the converter accurately. Currently, most of the research in converter modeling focuses on two main approaches: time-domain analysis and frequency-domain analysis.

For time-domain analysis, the research [103], [104] has been extensively discussed. This approach involves splitting the current and voltage waveforms into multiple segments based on the switching times of the semiconductor switches. However, if there are numerous modulation indices, such as in the

case of TPS modulation, the complexity and computation burden significantly escalate.

On the other hand, frequency-domain analysis [105], [106] is another method that necessitates transforming the voltage and current waveforms into the time-domain using Fourier series. This method ensures accuracy when all harmonic components of the waveforms are considered. Nevertheless, as the number of harmonic components increases, the complexity and computation burden also grow accordingly.

To expedite and cost-effectively model the converter, AI has recently emerged as a viable third option. Several researchers have explored the application of AI-based technology for converter modelling [107], [108]. However, one of the drawbacks of AI technology modelling is the delicate balance required for learnable parameters—having too few or too many can impact the model's accuracy in mapping input to output. Insufficient parameters may lead to an underfitting issue, while an excess of parameters may result in overfitting.

To overcome these challenges, this chapter suggests the use of XGBoost algorithm, a novel approach that enables the training of an accurate model even with a limited dataset in a short amount of time [109]. Furthermore, with the help of PSO-SAVL algorithms, this approach achieves the optimization of current stress with ZVZCS operation for hybrid NPC DAB converter with hybrid duty ratio PSM modulation.

The chapter’s organization is as follows. Section 5.2 presents the challenges and research gaps in the field. Section 5.3 illustrates the methodology and flowchart, outlining the XGBoost algorithm in detail. Section 5.4 describes the design case used to demonstrate the application of XGBoost algorithm in converter modelling. Section 5.5 presents the results of the optimization, along with experimental comparison results, showcasing the effectiveness of the proposed approach.

5.2 Challenge and Research Gap

For the sake of readability, the circuit diagram presented in Fig. 2.7 is reproduced again in Fig. 5.1. The hybrid NPC DAB configuration features two NPC modules on the primary side. In this arrangement, the outer switch is implemented using SiC MOSFETs, while the inner switch utilizes Si IGBTs.

5.2.1 The Hybrid Modulation Method for Hybrid NPC DAB

The innovative hybrid duty ratio PSM method for the hybrid NPC DAB converter is introduced to unveil the concealed potential of this configuration. As depicted in Fig. 5.2, this method incorporates three distinct control parameters. Firstly, D_1 is applied to the Si and SiC switches within the NPC modules,

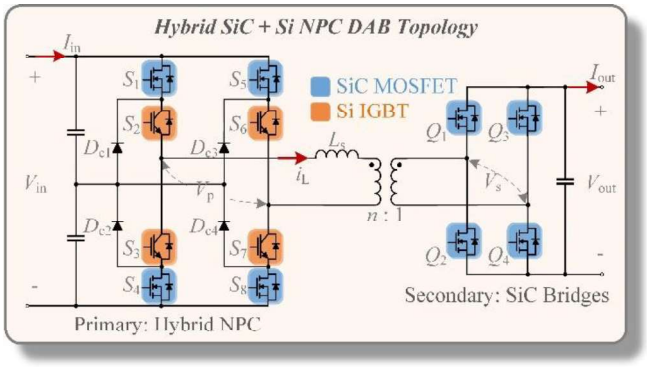


Fig. 5.1 Hybrid SiC + Si NPC DAB topology.

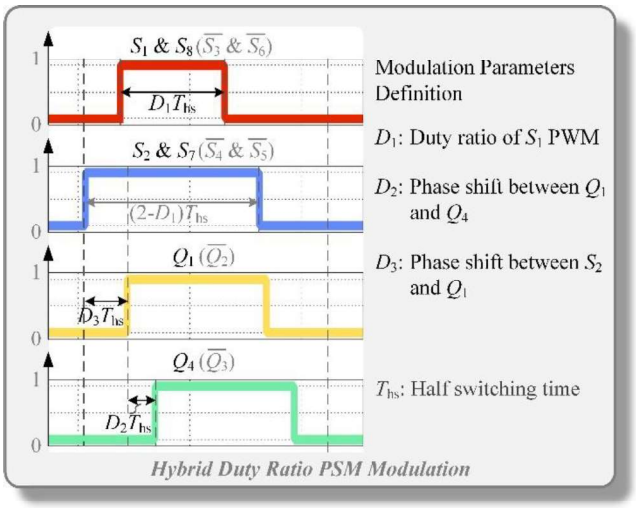


Fig. 5.2 Hybrid duty ratio PSM modulation method.

effectively altering the duty ratio of these two disparate semiconductor types, thereby preventing simultaneous switching of different semiconductors. Secondly, D_2 denotes the phase shift among the secondary side phase legs. Lastly, D_3 is implemented to modify the phase shift between the primary side and secondary side, enabling enhanced control and efficiency.

5.2.2 Challenges for the ZVZCS modelling

Traditionally, two distinct modeling methods are employed for the analysis of ZVZCS. The first one is the time-domain method, and the second one is the frequency-domain method.

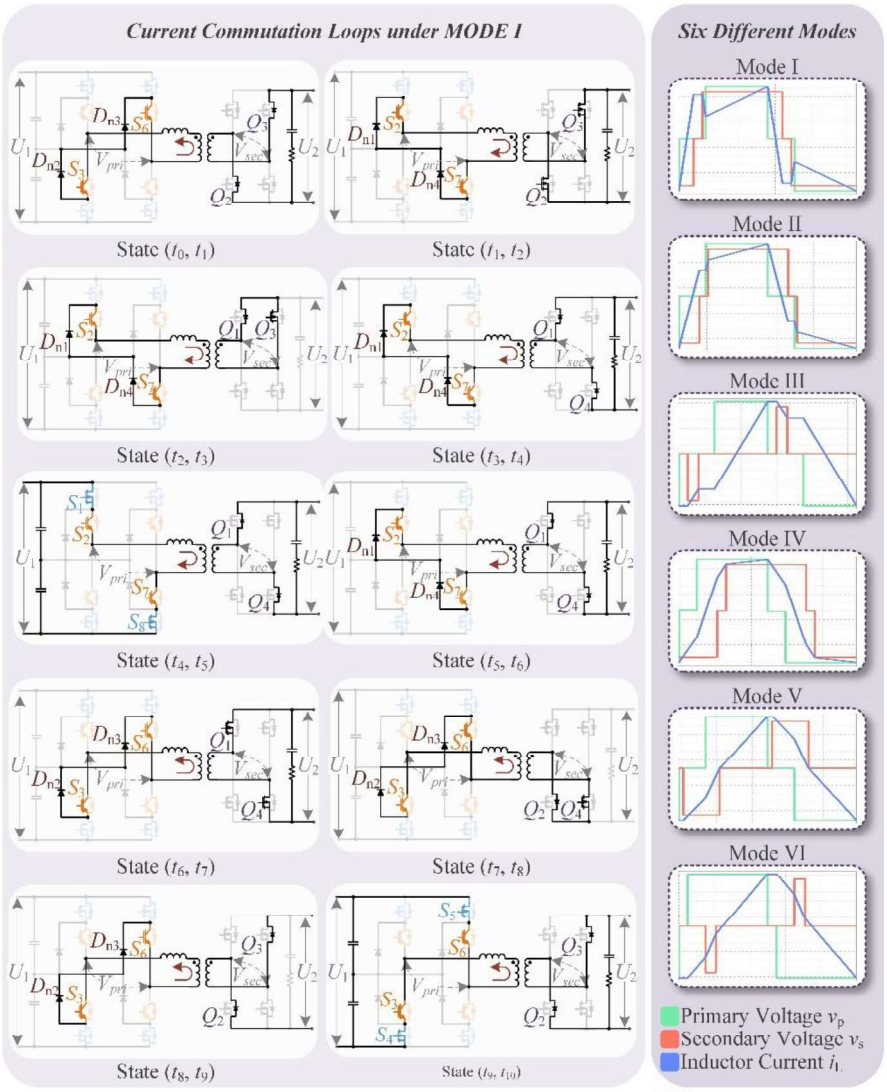


Fig. 5.3 Commutation loop analysis for different modulation modes.

The time-domain approach involves a meticulous examination of the voltage waveforms on both the primary and secondary sides, as well as the inductor current waveforms. Due to the generation of multilevel voltage waveforms across the high-frequency transformer under hybrid duty ratio PSM, six different modes are applicable for different operating points. However, the segment-by-segment analysis in the time-domain method can prove to be excessively time-consuming. Specifically, for the ZVZCS phenomenon, a comprehensive understanding of the commutation loops is essential. An example of the commutation loop with hybrid duty ratio PSM modulation is illustrated in Fig. 5.3. The commutation loop for six different modes can be found in Appendix A.

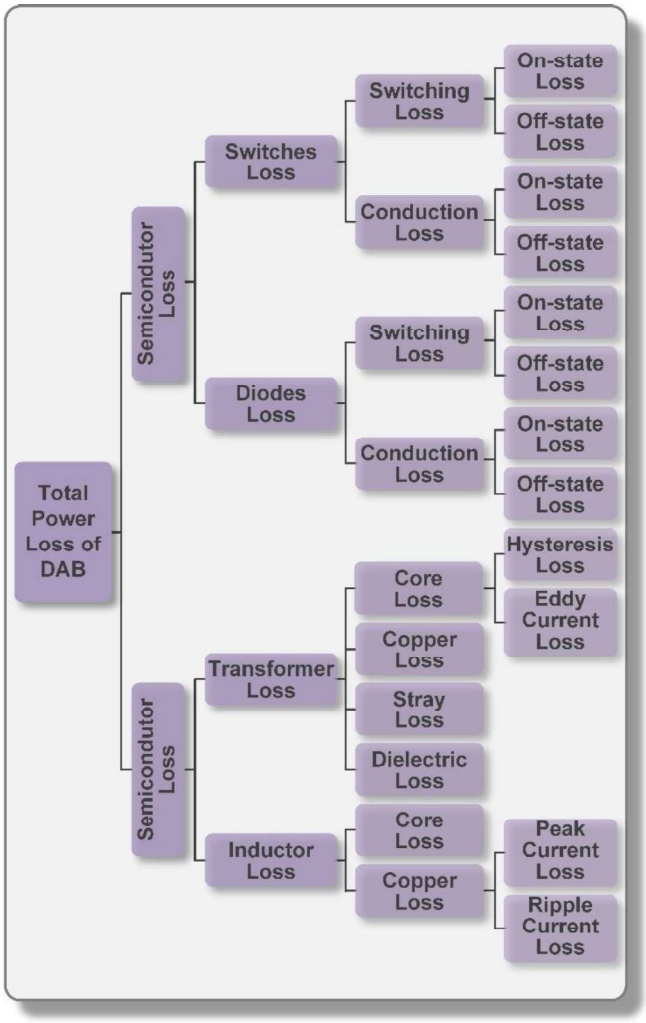


Fig. 5.4 Power losses components for DAB based topologies.

To analyze ZVZCS at a specific operating point and modulation method, the following steps are taken. Firstly, the modulation modes need to be determined based on the chosen operating point. Then, in the next step, one switching cycle is divided into 10 different segments, considering the switching behavior of the semiconductors according to the identified modulation modes. The analysis will be repeated as necessary when the operating conditions change.

This level of detailed analysis is necessary to fully comprehend and optimize the performance of the system under the hybrid duty ratio PSM modulation, but it requires significant computational effort due to its time-domain nature and the consideration of various operating points and modulation scenarios.

On the other hand, the frequency-domain method employs Fourier series to consider voltage and current waveforms, thereby reducing complexity by not taking modulation modes and switching patterns into account [50]. Nevertheless, the accuracy of this method heavily depends on the number of harmonics considered. If numerous harmonic components are taken into consideration, the calculations for ZVZCS conditions can become overly intricate. Conversely, if only a few harmonics are considered, the accuracy may not be sufficient.

Both time-domain and frequency-domain analyses rely on knowledge-based methods. There are three concerns associated with such approaches. Firstly, both methods necessitate a comprehensive understanding of circuit waveforms to determine boundary conditions, which requires a high-performance control unit due to the computational burden. Secondly, if multiple optimization objectives need to be simultaneously considered, the analysis process can become exceedingly time-consuming. Lastly, the existence of nonlinear components in the circuit means that real-world situations may not align perfectly with theoretical analyses, potentially leading to suboptimal fulfillment of the optimization objectives.

5.2.3 Challenges for the Efficiency Modelling

Efficiency modeling poses challenges due to numerous nonlinear components contributing to power losses in the system. As depicted in Fig. 5.4, the power losses in DAB converters consist of 16 different types of losses. Some of these losses are independent of the load condition and solely dependent on their own characteristics, such as transformer core losses. However, others are closely related to the operating points, which are influenced by factors like topology, modulation, control, thermal management, and more.

While there exist some analytical equations and experimental assumptions for estimating these power losses [110], [111], accurately modeling the power losses for the entire power converter is intricate. This complexity makes efficiency estimation across the entire power range challenging. The interplay of multiple variables and the nonlinear nature of the losses require sophisticated models and comprehensive data to achieve precise efficiency predictions. As a result, efficiency analysis for DAB converters demands careful consideration and often necessitates a combination of theoretical models and experimental validations to attain accurate results.

This chapter centers around the optimization of the hybrid NPC DAB converter under the hybrid duty ratio PSM. The study encompasses two primary optimization objectives: ZVZCS, and high efficiency. To achieve these goals, an innovative AI-based modeling approach will be employed to accurately characterize the converter's behavior. Subsequently, the optimization control parameters will be determined and implemented to achieve the desired outcomes.

5.3 Methodology

5.3.1 Data-Driven Modelling of ZVZCS and Efficiency

The data-driven method proves to be a valuable approach in simplifying the modeling of the intricate behavior of the hybrid NPC DAB converter. However, traditional data-driven methods demand an extensive dataset to ensure accurate training of neural networks. Unfortunately, obtaining such a vast amount of data poses a challenge in the power converter domain.

To address this issue, a novel data-driven approach is proposed in [112], specifically for ZVS optimization, to enhance the efficiency performance. In this section, the data-driven models of ZVZCS and efficiency for hybrid NPC DAB converter under hybrid duty ratio PSM is discussed.

The flowchart for the modelling is shown in Fig. 5. There are totally 3 steps.

The initial step involves selecting input parameters for the model. These input parameter pairs consist of (P, V_{out}, D_1, D_2). Power P varies within the range (P_{min}. P_{max}) with N_1 steps, and output voltage V_{out} varies within the range (V_{out_min}. V_{out_max}) with N_2 steps. D_1 and D_2 represent modulation indices with hybrid duty ratio PSM, both varying in the range [0, 1] M_1 and M_2 samples. Consequently, the input sets comprise $N_1 \times N_2 \times M_1 \times M_2$ different combinations.

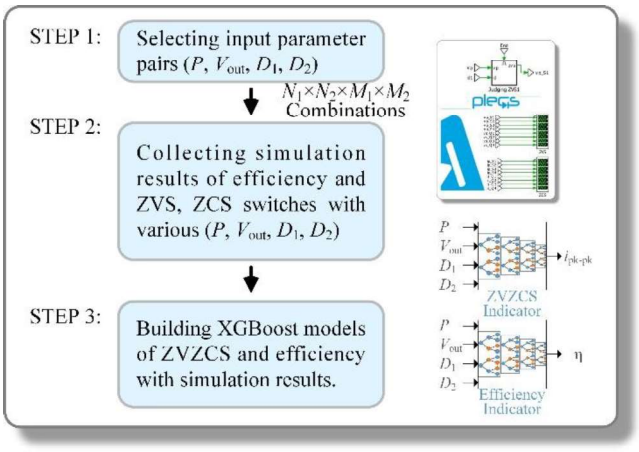


Fig. 5.5 Flowchart of Stage I of the proposed AI-based optimization method.

In the second step, simulation data is gathered for all possible input combinations using PLECS. Python automatic codes facilitate swift and highly accurate simulations.

Finally, based on the simulation data collected, the data is utilized to train a model using the XGBoost algorithm. The inputs for the XGBoost models are P, V_{out}, D_1, and D_2. The outputs of these models are the efficiency η and the number of switches satisfying ZVS and ZCS constraints N_{ZVS}, N_{ZCS} respectively. The collected simulation data is divided into training set (70%), validation set (15%), and testing set (15%). The training set is used to train the data-driven model, the validation set helps in selecting the optimal XGBoost structure, and the testing set is used to evaluate the trained XGBoost model's performance on new and unseen data points. As a result, the trained XGBoost models serve as data-driven surrogate models for current stress and ZVZCS. These models enable the evaluation of current stress and ZVZCS performance under any unforeseen operating and modulation parameters.

5.3.2 ZVZCS and Efficiency Optimization

Utilizing the trained XGBoost models, the optimization process aims to achieve minimum current stress and ZVZCS operation through the application of the PSO-SAVL algorithm. The optimization targets can be mathematically expressed as follows:

$$\eta^* = \max_{D_1, D_2} \left(\eta(P, V_{out}, D_1, D_2) \right) \tag{13}$$

Subject to the following constraints:

$$\begin{cases} N_{\mathrm{ZVS}}(P, V_{out}, D_1, D_2) = 12 \\ N_{\mathrm{ZCS}}(P, V_{out}, D_1, D_2) = 8 \\ 0 \le D_1 \le 1 \\ 0 \le D_2 \le 1 \end{cases} \tag{14}$$

The optimization process can be succinctly summarized into two steps. In the first step, the operating conditions are determined, wherein the required output power P and output voltage V_{out} are specified. Subsequently, in the second step,

the PSO-SAVL algorithm is employed to solve the optimization equations, leading to the selection of operating points that achieve both the efficiency optimization and ZVZCS operation, while adhering to the given values of P and V_{out}.

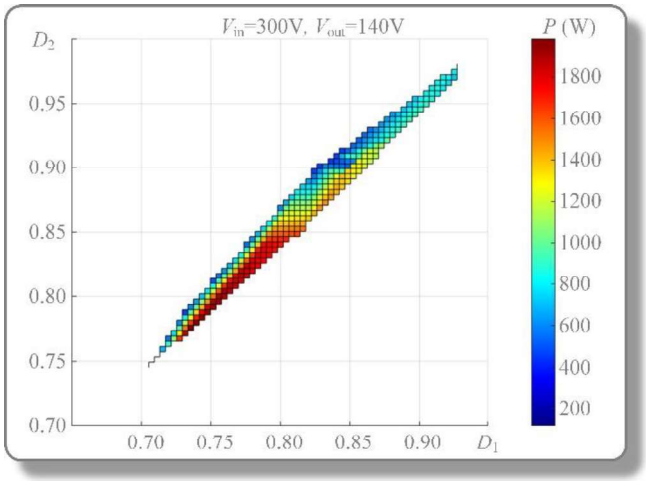
5.4 Design Case for ZVZCS and Efficiency Optimization with Hybrid Duty Ratio PSM

The design for the ZVZCS operation and efficiency optimization for the hybrid NPC DAB converter with hybrid duty ratio PSM is given in this section.

5.4.1 Data-Driven Modelling of ZVZCS and Efficiency with XGBoost Algorithm

In the context of the hybrid duty ratio PSM for the hybrid NPC DAB converter, the inputs necessary for modeling the ZVZCS and efficiency are outlined in Table XII. The system's rated output power is 2 kW, with a minimum output power of 100 W. The input voltage is set at 300 V, and the output power is rated at 140 V. Additionally, variable values of 150 V and 160 V are chosen to study both buck and boost modes. The leakage inductance is denoted as 230 μH.

Following the same flowchart as described in Subsection 5.3.1, data-driven models for ZVZCS and efficiency are constructed using the XGBoost algorithm. In the first step, a total of 20×3×20×20=24000 combinations of P, V_{out}, D_1, and D_2 are uniformly sampled. Then, in the second step, PLECS simulations are executed to gather data on the efficiency and the number of switches N_{ZVZCS} that meet the ZVZCS requirements. The collected data is organized and utilized to train the XGBoost models for ZVZCS and efficiency. The specific configurations used in this process are detailed in Table XIII.



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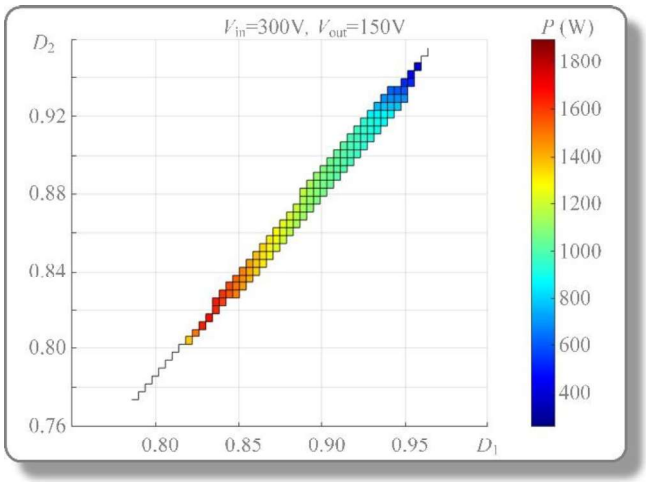

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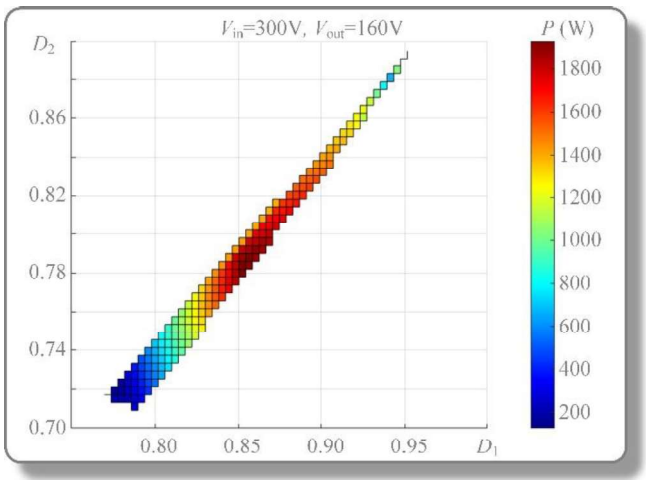

(c)

Fig. 5.6 Optimal modulation parameters for the whole power range (from 200W to 2 kW) at different modes. (a) Buck mode: V_{out} = 140 V, (b) unit gain mode: V_{out} = 150 V. and (c) boost mode: V_{out} = 160 V.

TABLE XII

SPECIFICATIONS OF DESIGN CASE

	Parameters		Values
Rated Conditions	Rated Output Power	P_{rate}	2000 W
	Rated Input Voltage	V_{in_rate}	300 V
	Rated Output Voltage	V_{out_rate}	140 V
	Switching Frequency	f_{sw}	20 kHz
Switching Device	Primary Side IGBT	S_2, S_3, S_6, S_7	IKW40N65ES5
	Primary Side MOSFET	S_1, S_4, S_5, S_8	UF3C065030K4S
	Primary Side Neutral Diode	$D_{n1\text{-}n4}$	APT30DQ60B
	Secondary Side MOSFET	$Q_{1\text{-}4}$	UF3C065030K4S
Transformer	Turns ratio	n	2
	Inductance	L_s	230 μH
Ranges of Operation Parameters	Output Power	P_{out}	[200 W, 2000 W]
	Output Voltage	V_{out}	[140 V, 160 V]

TABLE XIII

CONFIGURATIONS OF XGBOOST MODELS OF ZVS AND EFFICIENCY

	Parameters	Values
General setting	Inputs	P_{out}, V_{out}, D_1, D_2
	Learning Rate	0.08
	Output	Total Power loss P_{loss}
Structure of XGBoost-1 for ZVZCS	Maximum Tree Depth	9
	Regularization Coefficient	0.1
	Number of Base Tree Models	1930
Structure of XGBoost-2 for efficiency	Output	Number of ZVZCS switches N_{ZVZCS}
	Maximum Tree Depth	6
	Regularization Coefficient	1
	Number of Base Tree Models	189

5.4.2 Efficiency Optimization with ZVZCS Operation

The optimal modulation parameters D_1 and D_2 have been successfully determined across a wide range of power P and output voltage V_{out} values. The PSO-SAVL algorithm was employed, and the specific parameters used in this optimization process are listed in Table XIV. The resulting optimal modulation parameters D_1 and D_2 are depicted in Fig. 5.6.

TABLE XIV

CONFIGURATIONS OF CONFIGURATIONS OF PSO-SAVL

Parameters	Values
Inputs	P_{out}, V_{out}, D_1, D_2, XGBoost-1 $P_{loss}(P_{out}, V_{out}, D_1, D_2)$, XGBoost-2 $N_{ZVZCS}(P_{out}, V_{out}, D_1, D_2)$
Output	Optimal D_1, D_2 and optimal P_{loss} * for given P_{out}, V_{out}, D_1, D_2
Number of particles	5
Maximum iterations	50
Weight inertia ω	Linearly decrease from 0.9 to 0.4
ZVZCS weight factor	$c_{ZVZCS} = 100$
Velocity limit factors	$vl_{max} = 0.7$; $vl_{min} = 0.4$

As observed in the figure, the optimal modulation parameters are clustered within a slender and elongated region. Notably, for different operating modes, namely buck, boost, and unit modes, the optimal regions vary, particularly noticeable under light load conditions. However, as the power approaches the rated power level, the optimal modulation parameters tend to converge around the range of 0.8 to 0.85. These findings demonstrate that the PSO-SAVL algorithm successfully identifies the most effective modulation parameters based on the specific power and output voltage conditions. The clustered nature of the optimal regions implies that certain modulation settings perform optimally

within defined ranges of power and voltage, which can significantly impact the overall efficiency and performance of the system under different load conditions.

5.5 Experimental Results

The hardware configuration is depicted in Fig. 3.8, and the experimental parameters are tabulated in Table XII.

In this section, steady-state experimental waveforms obtained for various power P and output voltage V_{out} values are presented. The power levels considered range from 200 W to 2000 W, with a step size of 200 W, encompassing high, medium, and low power conditions. Moreover, the V_{out} voltage is explored at three distinct values: 160 V for boost mode, 150 V for unit gain mode, and 140 V for buck mode. Fig. 5.1 provides the notation and directions for the waveforms.

To investigate the ZVZCS results under light load conditions, where typically the efficiency is extremely low, the power P is set to 200 W and V_{out} to 140 V. In this scenario, the primary and secondary voltage waveforms, V_p and V_s, exhibit

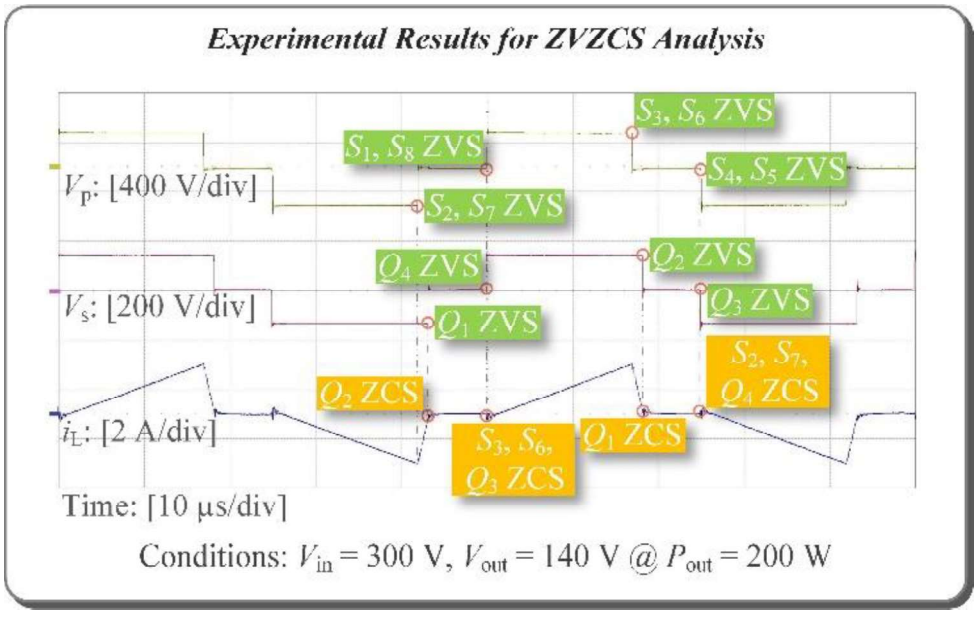

Fig. 5.7 Experimental waveforms under buck mode when V_{out} = 140 V and P = 200 W.

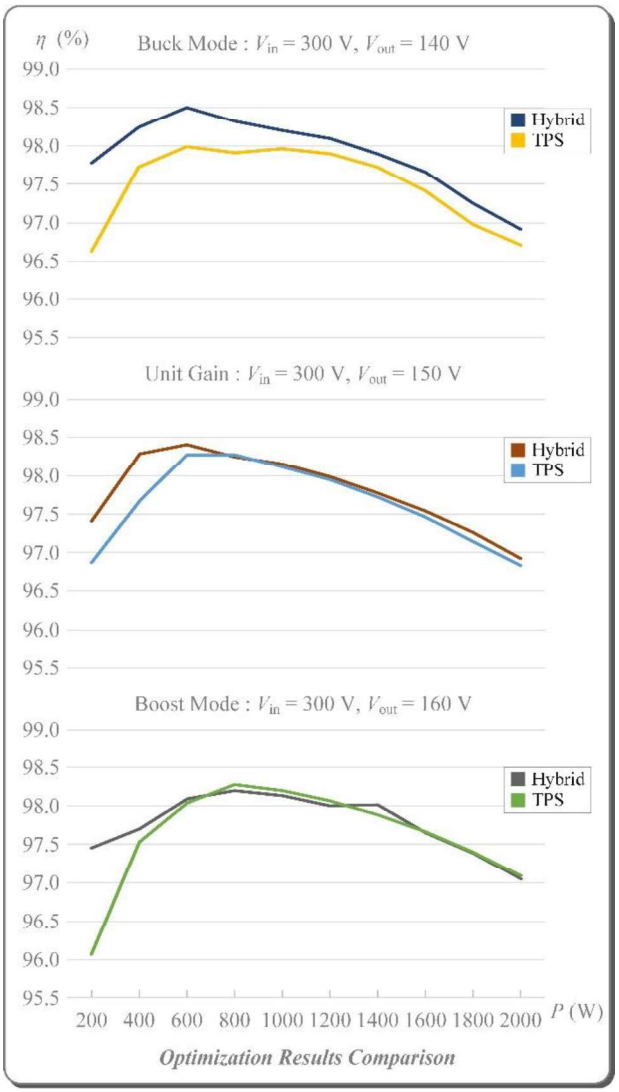

Fig. 5.8 Comparison for the optimized performance between hybrid duty ratio PSM and TPS.

three-level waves, as illustrated in Fig. 8. Notably, all 12 switches comply with the ZVS constraints, and eight switches, excluding the SiC MOSFETs inside NPC modules, also meet the ZCS constraints, as evident from the inductor current waveform, i_L, displayed in Fig. 5.7.

Fig. 5.8 presents an efficiency comparison with the TPS modulation. It is evident from the figure that, in buck mode, the optimization achieved with the hybrid modulation is significantly better than that of TPS. In unit gain and boost modes, the performance at heavy load conditions is comparable to that of TPS. However, under light load conditions, the advantages of hybrid duty ratio PSM are fully realized, showcasing superior optimization capabilities.

5.6 Summary

This chapter has proposed an AI-based optimization method for the hybrid duty ratio PSM in a hybrid NPC DAB converter. The primary objective is to optimize efficiency while ensuring all-switch ZVS operation and maximizing ZCS operation for all Si IGBT switches. By integrating simulation software and the XGBoost algorithm, the ZVZCS and efficiency models of the hybrid duty ratio PSM have been developed automatically, eliminating the cumbersome and often inaccurate model-building process in conventional approaches.

The optimization process involves two stages. In Stage I, performance data generated through simulations is used to build data-driven models of ZVZCS and efficiency using the XGBoost algorithm. In Stage II, the cutting-edge PSO-SAVL algorithm is employed to optimize the modulation strategy and parameters for achieving the best efficiency and ZVZCS operation. Experimental validation is conducted on a 2-kW hardware prototype of a hybrid NPC DAB converter. The results demonstrate the optimized efficiency, full ZVS range, real-time operating capability, and overall effectiveness of the proposed AI-based optimization approach.

This research leverages the application of AI techniques to the field of power electronics to achieve efficient and reliable operation of the hybrid NPC DAB converter. By automating the modelling and optimization processes, the proposed method offers an efficient and accurate solution for designing and controlling power converters with improved performance.

6 Conclusion and Recommendations

6.1 Conclusion

This thesis has explored the optimized operation and efficiency of a DAB converter for high-power energy storage system applications. To meet the demanding requirements of such applications, a novel DAB-based topology and modulation strategies have been proposed and thoroughly investigated. Through comprehensive analysis and experimental verification, the following conclusions are drawn:

In the design of the DAB converter topology, the integration of hybrid NPC modules proves to be advantageous for high-power DAB converters. By capitalizing on the benefits of SiC MOSFETs, the proposed hybrid SiC + Si NPC-based DAB converter effectively reduces power losses while maintaining a favourable balance between cost and efficiency. The simulation results obtained from PLECS demonstrate that the proposed hybrid multilevel topology achieves nearly the same efficiency performance as a full SiC-based topology, but with a cost advantage due to integrating some cheaper Si-based semiconductor components. This innovation in hybrid multilevel topology offers a promising new solution for high-power energy storage system applications.

In pursuit of further enhancing efficiency, a novel modulation method is introduced in Chapter 3. In conventional PSM for the DAB converter, switches within the same phase leg exhibit synchronized switching. However, in the case of the NPC DAB topology, especially the hybrid NPC DAB converter discussed in Chapter 2, where outer switches in the NPC module are SiC MOSFETs and adjacent inner switches are Si IGBTs, employing conventional PSM may lead to significant power losses and risks of damaging the semiconductors.

To fully leverage the advantages of the topology proposed in Chapter 2, a new modulation method is devised, wherein different switching schemes are applied to SiC MOSFETs and Si IGBTs. The duty ratio of adjacent SiC MOSFETs and Si IGBTs is designed to be unequal but complementary. While maintaining

phase-shift control for primary and secondary voltages, an inner phase shift is applied to the secondary side SiC MOSFETs. This design effectively utilizes the neutral current path, enabling maximum utilization of the clamping diodes. As a result, the conduction losses of SiC MOSFETs and the switching losses of Si IGBTs are significantly reduced.

Experimental comparisons between the efficiency performance under the proposed hybrid duty ratio PSM and the conventional TPS modulation have been conducted on a 2-kW prototype. The hybrid duty ratio PSM proves to be highly effective, achieving higher efficiency with a maximum value of 97.9%.

To address the challenges encountered when modelling the DAB converter, Chapter 4 introduces a novel data-driven modelling method. Traditional performance modelling of power converters relies on knowledge-based approaches, which can be labour-intensive and suffer from lower modelling accuracy. In contrast, emerging data-driven techniques automate the modelling process using simulation data. However, inaccuracies may arise due to unaccounted parasitic, incomplete thermal and magnetic models, and unpredictable real-world conditions, limiting the practical application of pure simulation-based data-driven models.

To bridge this gap and enhance practical accuracy, the chapter proposes a novel approach called D^2EA. D^2EA harnesses the strengths of both simulation data and experimental data to create robust and accurate models. Simulation data lays the foundation by establishing a basic functional landscape, while experimental data ensures the models match the actual performance in real-world scenarios. By combining these data sources, D2EA significantly improves the accuracy of data-driven models for power converters.

The D2EA approach is applied to optimize the efficiency of a hybrid modulation for the NPC-DAB converter. Remarkably, D2EA achieves an efficiency modelling accuracy of 99.92%. Extensive validation through 2-kW hardware experiments further demonstrates its effectiveness, achieving a peak

efficiency of 98.45%. This confirms the feasibility and reliability of the D2EA approach in practical applications.

Overall, D2EA offers a data-light and scalable solution, generating highly accurate and practical data-driven models that effectively combine simulation and experimental data. This pioneering approach holds immense potential for enhancing power converter modelling and optimization across diverse applications.

Chapter 5 delves deeper into the improvement of the proposed NPC DAB converter through the application of an AI-based control method to optimize the ZVZCS operation and efficiency performance. Due to the complexity of the converter's topology and modulation strategies, conventional knowledge-based modelling is challenging to implement for the NPC DAB converter. To overcome this, a data-driven method is proposed for modelling the ZVZCS and efficiency of the converter. The optimization process is then carried out using the PSO-SAVL algorithm.

Through this approach, the hybrid NPC DAB converter is ensured to achieve optimized efficiency while maintaining ZVZCS switching, as confirmed by experimental results. Notably, at buck mode, the optimized efficiency performance consistently outperforms that of the conventional TPS modulation. At unit gain and boost mode, the superiority of the optimized efficiency is particularly evident under light load conditions. However, even at heavy load conditions, the efficiency performance remains comparable to that of TPS. The results demonstrate the efficacy of the AI-based control method in enhancing the efficiency and ZVZCS operation of the hybrid NPC DAB converter. By utilizing data-driven modelling and AI-based optimization, the converter's performance is significantly improved, providing a promising solution for high-power energy storage system applications.

6.2 Recommendations for Further Research

Within the realm of dual active bridge converter design for high-power energy storage systems, there are several other intriguing topics worth investigating. Two potential directions are outlined below:

6.2.1 Neutral Point Voltage Control for Hybrid NPC DAB Converter

Under the hybrid duty ratio PSM modulation, the current passes through the clamping diodes during the zero-voltage stage. However, in practical applications, the neutral point voltage is not precisely zero due to the voltage drop across the clamping diodes. This discrepancy may lead to an imbalance in the output voltage levels and inductor current waveforms, subsequently affecting the overall performance of the converter.

To address this issue, three steps can be considered. Firstly, the neutral voltage can be monitored using either conventional voltage sensors or through reliable neutral voltage prediction using data-driven modeling. Next, a compensating voltage can be generated to eliminate the effects of clamping diode voltage drops. Finally, the controller can implement the compensating voltage on the corresponding switches, thereby ensuring a balanced and optimized converter performance.

6.2.2 Cascaded Hybrid NPC DAB Converter Design for Large Scale System Applications with Data-Driven Methods.

For large-scale system applications, a single topology may not be sufficient to handle the extremely high-power requirements. In such cases, cascaded topologies offer a viable solution. The modular structure of cascaded converters provides the flexibility to customize the converter for different system scales. However, designing the control for cascaded DAB converters requires careful consideration to ensure equal voltage sharing, current sharing, and voltage balancing among the capacitors.

Indeed, while research has been conducted on cascaded two-level DAB converters, the exploration of cascaded hybrid NPC DAB converters remains

largely unexplored. The unique advantages of the hybrid NPC DAB converter offer a promising solution for cascaded systems. By leveraging the hybrid topology, it becomes possible to reduce the number of modules in cascaded converters while maintaining the same power level when compared to conventional two-level DAB cascaded systems. This reduction in modules results in fewer magnetic components and leads to improved system efficiency.

However, to fully realize the potential benefits of cascaded hybrid NPC DAB converters, the development of advanced control methods is crucial. Voltage and current balancing control among different cascaded modules becomes more complex with the addition of the hybrid NPC DAB topology. To achieve seamless integration and optimal performance of the cascaded system, precise control of each module is essential.

Data-driven techniques offer a promising approach to design these converters efficiently. By using data-driven modeling and optimization methods, the control strategies for cascaded hybrid NPC DAB converters can be finely tuned to ensure effective voltage and current balancing among modules. Data-driven techniques can facilitate the development of adaptive control algorithms that can adapt to varying operating conditions and ensure stable and efficient operation of the cascaded converter system.

By exploring and advancing the control methods for cascaded hybrid NPC DAB converters using data-driven techniques, researchers can unlock the full potential of this topology for high-power energy storage systems. The efficient and reliable operation of cascaded converters can contribute significantly to the implementation of large-scale energy storage systems and support the transition to a more sustainable and energy-efficient future.

By exploring these areas, further advancements can be made in the design and control of DAB converters for high-power energy storage systems, opening up new possibilities for efficient and reliable power conversion in various applications.

Author's Publications

Published

[1] Jiaxin Dong, Josep Pou, Xinze Li, Suvajit Mukherjee, Amit K. Gupta, and Yu Zeng, "Hybrid Duty Ratio Phase-Shift Modulation for a Si + SiC Neutral-Point-Clamped Dual-Active-Bridge Converter," IEEE Access, vol. 11, pp. 129866-129881, 2023, doi: 10.1109/ACCESS.2023.3332764.

[2] Xinze Li, Josep Pou, **Jiaxin Dong**, Fanfan Lin, Changyun Wen, Suvajit Mukherjee, and Xin Zhang, "data-driven modeling with experimental augmentation for the modulation strategy of the dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, early access, doi: 10.1109/TIE.2023.3265027.

[3] **Jiaxin Dong**, Josep Pou, Suvajit Mukherjee, Amit Kumar Gupta and Yu Zeng, "efficiency optimization for hybrid Si + SiC neutral-point-clamped dual-active-bridge converter for energy storage systems," in *Proc. IEEE PES Innov. Smart Grid Technol. – Asia, ISGT-Asia 2022,* pp. 345-348, Singapore, Nov. 2022.

[4] **Jiaxin Dong**, Josep Pou, Changjiang Sun, Zhan Li, Xin Zhang, Suvajit Mukherjee, Amit Kumar Gupta, and Yu Zeng, "hybrid Si + SiC neutral-point-clamped dual-active-bridge converter for high-voltage battery energy storage systems," in *Proc. IEEE Energy Convers. Congr. Expo. - Asia, ECCE-Asia 2021*, pp. 632-637, Singapore, May 2021.

[5] Yu Zeng; Josep Pou; Changjiang Sun; Suvajit Mukherjee; Xu Xu; Amit Kumar Gupta; and **Jiaxin Dong**, "autonomous input voltage sharing control and triple phase shift modulation method for ISOP-DAB converter in dc microgrid: a multiagent deep reinforcement learning-based method," *IEEE Trans Power Electron.*, vol. 38, no. 3, pp. 2985-3000, Mar. 2023.

[6] Yu Zeng, Ali Iftekhar Maswood, Josep Pou; Xin Zhang, Zhan Li, Changjiang Sun; Suvajit Mukherjee; Amit Kumar Gupta; and **Jiaxin Dong**, “active disturbance rejection control using artificial neural network for dual-active-bridge-based energy storage system,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 11, no. 1, pp. 301-311, Feb. 2023.

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[10] **Jiaxin Dong**, Josep Pou, Xinze Li, Yu Zeng, Janardhana Kotturu, Marco Cupelli, and Amit Kumar Gupta, “switching characteristics analysis for hybrid neutral point clamped dual active bridge with hybrid duty ratio PSM modulation,” in *Proc. IEEE Ind. Electron. Conf. (IECON) 2023*, pp., Singapore, Oct. 2023.

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[11] **Jiaxin Dong**; Aritra Basu; Smita Barua; Xinze Li; and Suvajit Mukherjee “grid-tied converter design document,” Rolls-Royce@NTU Corporate Laboratory, Tech. Report, Dec. 2022

Bibliography

Jiaxin Dong, Student Member, IEEE,] received his B.S. degree in Electrical Engineering from Southeast University, China, in 2016. Currently, he is in the final year of his Ph.D. program in the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore. In January 2020, he was awarded a Ph.D. scholarship by Rolls-Royce @ NTU corporate lab.

Jiaxin has made significant contributions to the field, with 10 published technical papers and active involvement in various industrial projects related to high-power power electronics. His research interests encompass a wide range of areas, including modulation and control of power converters, multilevel converters, renewable energy, energy storage, more-electrical aircraft, and fuel cell systems.

In recognition of his academic achievements, Jiaxin received the Rolls-Royce @ NTU scholarship in 2021. Additionally, he was awarded in the Nanyang Technological University 3-minute presentation competition in 2023. These accolades highlight his exceptional abilities and dedication to his field. Also, he was selected as a finalist for the PhD dissertation challenge in the 2023 IEEE IAS Industrial and Commercial Power System Asia Conference.

Awards

[1] Rolls-Royce @ NTU Corporate Lab Scholarship	Aug-2020
[2] Certificate of appreciation on hosting the ISGT-Asia 2022 Technical Tour at the Rolls-Royce@NTU Corporate Lab	Nov-2022
[3] Audience Favorite Award at 3-minute-thesis (3MT) EEE Finals	Mar-2023
[4] 1st Prize at First Let's Talk Research – NTU Graduate Student Research Conference Series	Mar-2023
[5] Finalist at Ph.D. Dissertation Challenge in 2023 IEEE IAS Industrial and Commercial Power System Asia (IEEE I&CPS Asia 2023)	Jul-2023

Appendices

A Current Commutation Loops under Modulation Modes with Hybrid Duty Ratio PSM

This appendix aims to analyze the various modes associated with the hybrid duty ratio PSM. To facilitate this analysis, the circuit diagram from Fig. 2.7 has been reproduced in Fig. A.1, and the modulation method presented in Fig. 3.2 is replicated in Fig. A.2. In total, there are six distinct modes, each of which will be discussed in detail on the following pages.

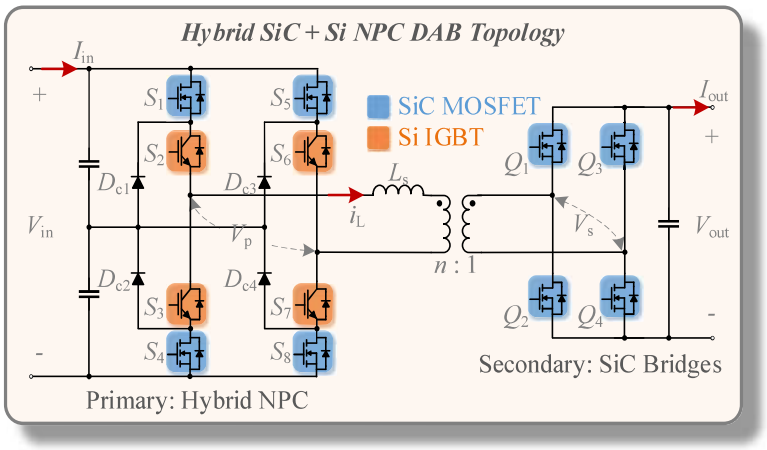

Fig. A.1 Circuit diagram of hybrid NPC DAB converter

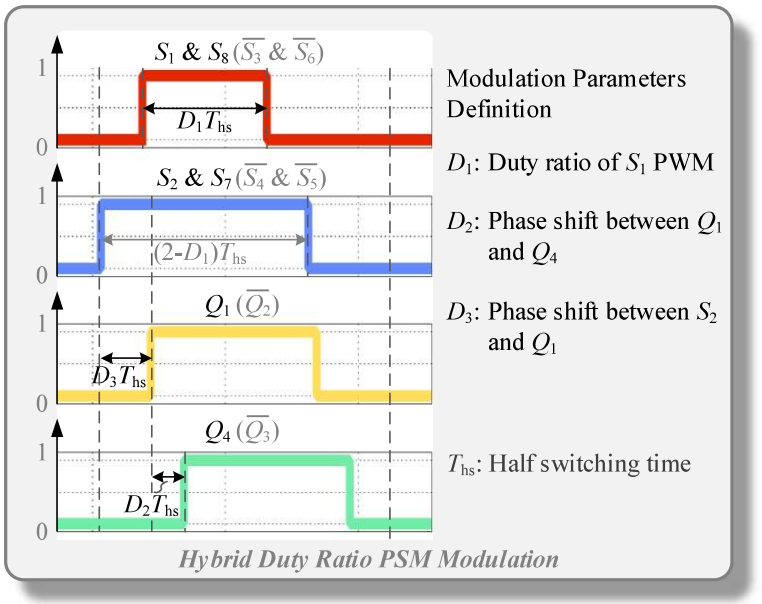

Fig. A.2 Hybrid duty ratio PSM

Mode I:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is nU_2 so the negative current reduces sharply. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_1: At the time t_1, the negative inductor current reduces to zero. The switches S_2, S_3, S_6, S_7, Q_2, and Q_3 are activated at this time.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the current direction changes to positive. The voltage across the inductor is nU_2. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, neutral diode D_{n1}, and neutral diode D_{n4}. On the secondary side, the current flows through Q_2 and Q_3.

Commutation state t_2: At the time t_2, on the primary side, the Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diodes of body diodes of Q_1 and switch Q_3.

Commutation state t_3: At the time t_3, on the primary side, the Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_3 turns off and Q_4 turns on, and Q_1 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is $-nU_2$. The positive current drops. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_4: At the time t_4, on the primary side, the Si IGBTs S_3 and S_6 turn off, and the SiC MOSFETs S_1 and S_8 turn on. On the secondary side, Q_1 and Q_4 are in the on state.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1-nU_2, and the current increases. On the primary side, the current path is made by S_1, S_2, S_7, and S_8. On the secondary side, the current flows through body diodes of Q_1 and Q_4.

Commutation state t_5: At the time t_5, the inductor current reaches the positive maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, The current drops from the peak. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_6: At the time t_6, the positive inductor current reduces to zero. The switches S_2, S_7, Q_1, and Q_4 are active at this time.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the current direction becomes negative. The voltage across the inductor is $-nU_2$. The negative current increases. On the primary side, the current path changes to Si IGBTs S_3, S_6, neutral diode D_{n2}, neutral diode D_{n3}. On the secondary side, the current flows through Q_1 and Q_4.

Commutation state t_7: At the time t_7, on the primary side, the Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_1 turns off and Q_2 turns on, and Q_4 is still active.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_8: At the time t_8, on the primary side, the Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_4 turns off and Q_3 turns on, and Q_2 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is nU_2. The negative current drops. On the primary side, the current path is combined with the Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_9: At the time t_9, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is $-(U_1\text{-}nU_2)$, and the negative current increases. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is made by S_3, S_4, S_5, and S_6. On the secondary side, the current flows through body diodes of Q_2 and Q_3.

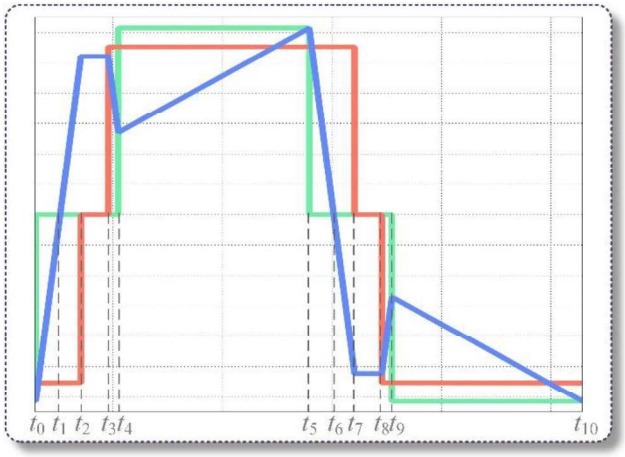

Fig. A.3 Voltage and current waveforms under mode I.

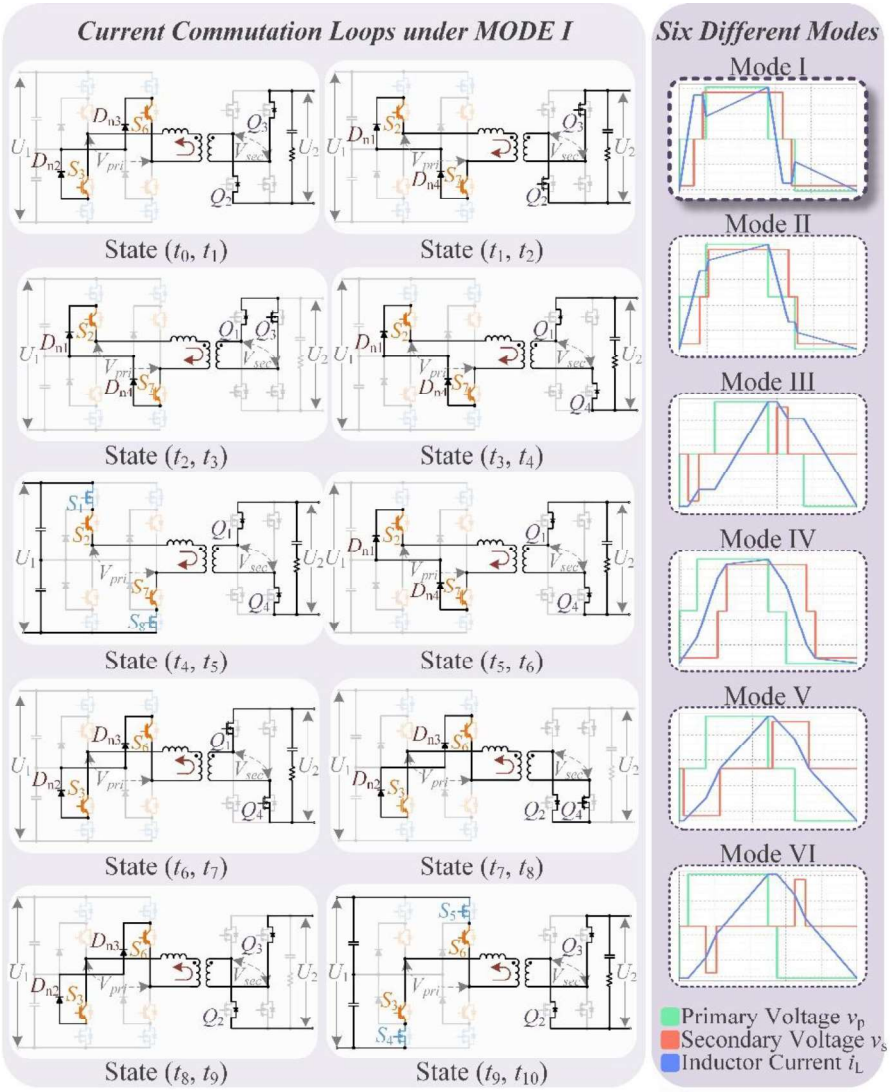

Fig. A.4 Current commutation loops under mode I.

Mode II:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is nU_2 so the negative current reduces sharply. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_1: At the time t_1, the negative inductor current reduces to zero. The switches S_2, S_3, S_6, S_7, Q_2, and Q_3 are activated at this time.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the current direction changes to positive. The voltage across the inductor is nU_2. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, neutral diode D_{n1}, and neutral diode D_{n4}. On the secondary side, the current flows through Q_2 and Q_3.

Commutation state t_2: At the time t_2, on the primary side, the Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_3: At the time t_3, on the primary side, the Si IGBTs S_3 and S_6 turn off, and the SiC MOSFETs S_1 and S_8 turn on. On the secondary side, Q_1 and Q_3 are in the on state.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1. The positive current increases. On the primary side, the current path is combined with the SiC MOSFET S_1, Si IGBT S_2, Si IGBT S_7, and SiC MOSFET S_8. On the secondary side, the current flows through the body diodes of Q_1 and Q_3.

Commutation state t_4: At the time t_4, on the primary side, the SiC MOSFET S_1, S_8 Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_3 turns off and Q_4 turns on, and Q_1 is still active.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1-nU_2, and the current increases. On the primary side, the current path is made by S_1, S_2, S_7, and S_8. On the secondary side, the current flows through body diodes of Q_1 and Q_4.

Commutation state t_5: At the time t_5, the inductor current reaches the positive maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is $-nU_2$ so the positive current reduces sharply. On the primary side, the current path consists of Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_6: At the time t_6, the positive inductor current reduces to zero. The switches S_2, S_3, S_6, S_7, Q_1, and Q_4 are activated at this time.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the current direction changes to negative. The voltage across the inductor is $-nU_2$. The negative current keeps increasing. On the primary side, the current path changes to Si IGBTs S_3, S_6, neutral diode D_{n2}, and neutral diode D_{n3}. On the secondary side, the current flows through Q_1 and Q_4.

Commutation state t_7: At the time t_7, on the primary side, the Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_1 turns off and Q_2 turns on, and Q_4 is still active.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_8: At the time t_8, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$. The positive current increases. On the primary side, the current path is combined with the SiC MOSFET S_4, Si IGBT S_3, Si IGBT S_6, and SiC MOSFET S_5. On the secondary side, the current flows through the body diodes of Q_2 and Q_4.

Commutation state t_9: At the time t_9, on the primary side, the SiC MOSFET S_4, S_5 Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_4 turns off and Q_3 turns on, and Q_2 is still active.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is $-(U_1-nU_2)$, and the negative current increases. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is made by S_3, S_4, S_5, and S_6. On the secondary side, the current flows through body diodes of Q_2 and Q_3.

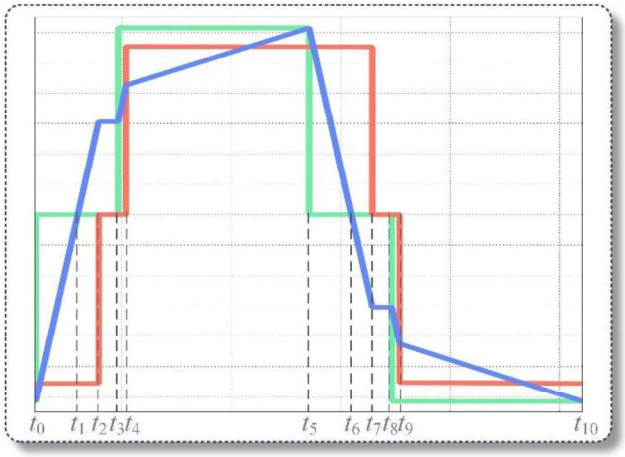

Fig. A.5 Voltage and current waveforms under mode II.

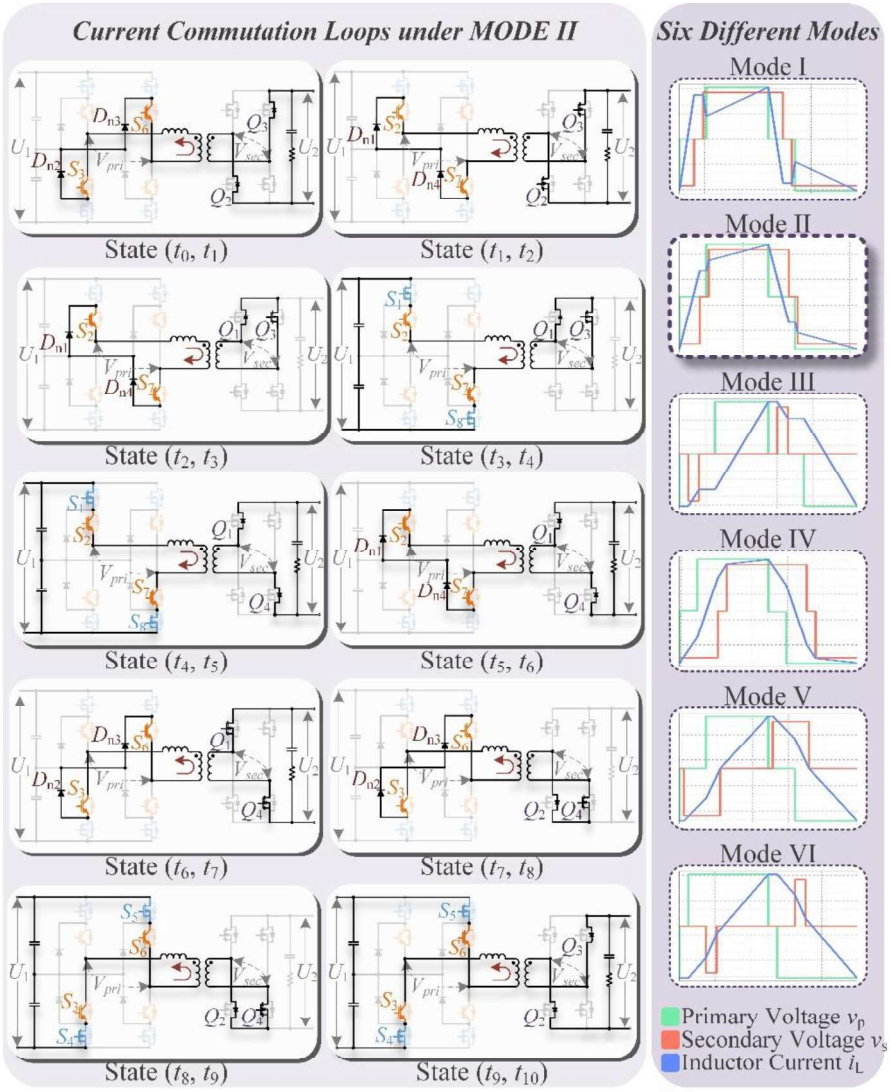

Fig. A.6 Current commutation loops under mode II.

Mode III:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is 0 so the negative current remains. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBTs S_2, S_3, S_6 and S_7 are in conduction. On the secondary side, Q_4 turns off and Q_3 turns on, and Q_2 is still active.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is nU_2, and the negative current decreases. On the primary side, the current path is made by Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through body diodes of Q_2 and Q_3.

Commutation state t_2: At the time t_2, the Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_3, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_6. On the secondary side, the current flows through the body diode of Q_3 and switch Q_1.

Commutation state t_3: At the time t_3, on the primary side, the Si IGBTs S_3 and S_6 turn off, and the SiC MOSFETs S_1 and S_8 turn on. On the secondary side, Q_1 and Q_3 are in the on state.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1 so the negative current reduces sharply. On the primary side, the current path consists of SiC MOSFETs S_1, S_8, Si IGBT S_2 and S_7. On the secondary side, the current flows through the body diode of Q_3 and switch Q_1.

Commutation state t_4: At the time t_4, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_1, and Q_3 are activated at this time.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1. The positive current increases. On the primary side, the current path is combined with the SiC MOSFET S_1, Si IGBT S_2, Si IGBT S_7, and SiC MOSFET S_8. On the secondary side, the current flows through the body diode of Q_3 and switch Q_1.

Commutation state t_5: At the time t_5, the inductor current reaches the positive maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_3 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is 0 so the negative current remains. On the primary side, the current path consists of Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2, S_3, S_6 and S_7 are in conduction. On the secondary side, Q_3 turns off and Q_4 turns on, and Q_1 is still active.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is $-nU_2$, and the positive current decreases. On the primary side, the current path is made by Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through body diodes of Q_1 and Q_4.

Commutation state t_7: At the time t_7, on the primary side, the Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_1 turns off and Q_2 turns on, and Q_4 is still active.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the voltage across the inductor is 0. The current remains unchanged. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_4 and switch Q_2.

Commutation state t_8: At the time t_8, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$ so the positive current reduces sharply. On the primary side, the current path consists of SiC MOSFETs S_4, S_5, Si IGBT S_3 and S_6. On the secondary side, the current flows through the body diode of Q_4 and switch Q_2.

Commutation state t_9: At the time t_9, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_2, and Q_4 are activated at this time.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is $-U_1$. The negative current increases. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is combined with the SiC MOSFET S_4, Si IGBT S_3, Si IGBT S_6, and SiC MOSFET S_5. On the secondary side, the current flows through the body diode of Q_4 and switch Q_2.

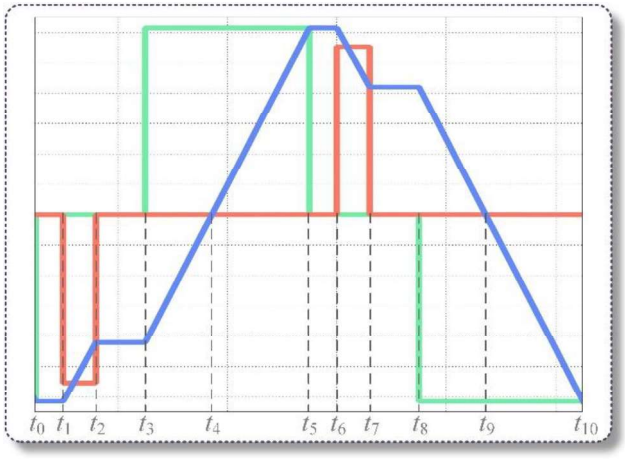

Fig. A.7 Voltage and current waveforms under mode III.

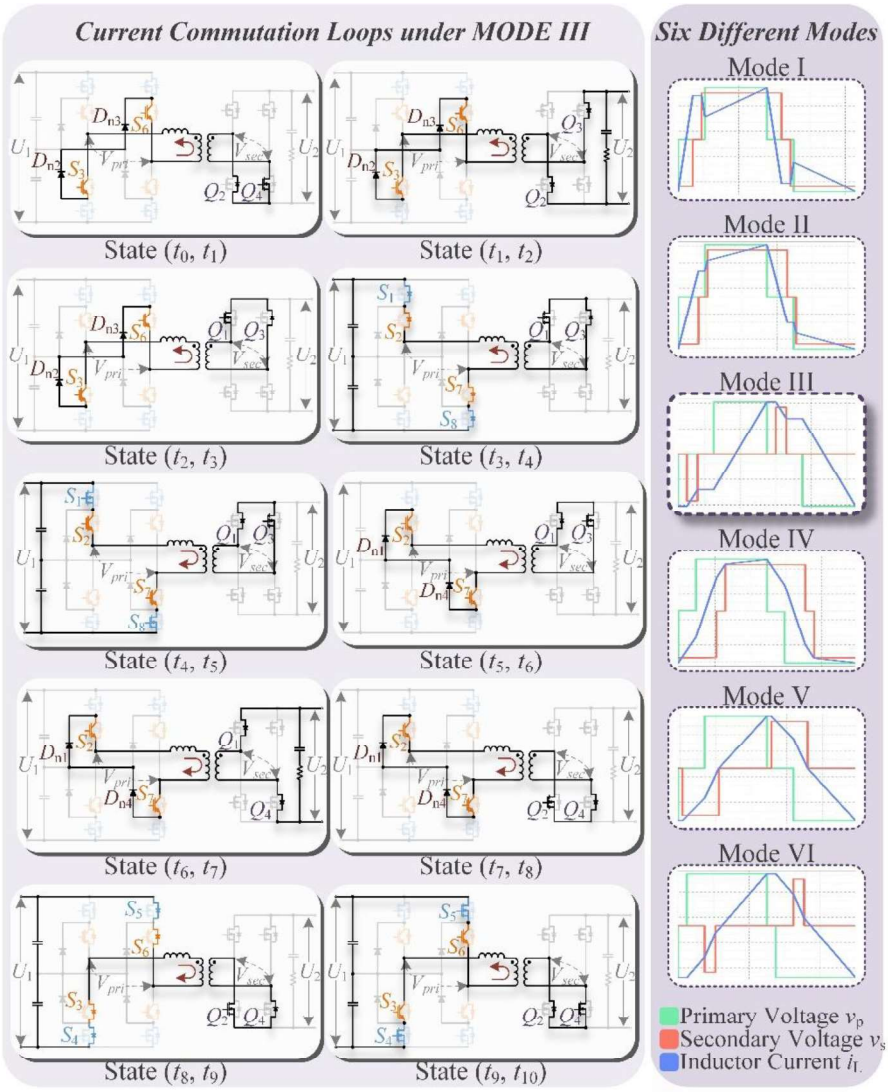

Fig. A.8 Current commutation loops under mode III.

Mode IV:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is nU_2, hence the negative current reduces. But it still reversely flows through the inductor. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBT S_3 and S_6 turn off, and the SiC MOSFET S_1 and S_8 turn on. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is U_1+nU_2 so the negative current reduces sharply. On the primary side, the current path changes to the body diodes of S_1, S_2, S_7, and S_8 for a short time. The voltages of S_1, S_2, S_7, and S_8 are clamped to zero with the negative current flowing through the body diodes. On the secondary side, the current flows through the body diodes of Q_2 and Q_3 so that ZVS is also ensured.

Commutation state t_2: At the time t_2, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_2, and Q_3 are activated at this time.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the current direction changes to positive. The voltage across the inductor is U_1+nU_2. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, SiC MOSFETs S_1, and S_8. On the secondary side, the current flows through Q_2 and Q_3.

Commutation state t_3: At the time t_3, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2, and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1, and the current increases. On the primary side, the current path is made by S_1, S_2, S_7, and S_8. On the secondary side, the current flows through Q_3 and the body diode of Q_1.

Commutation state t_4: At the time t_4, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2 and S_7 are in the on state. On the secondary side, Q_3 turns off, Q_4 turns, and Q_1 is activated.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the voltage across the inductor is U_1-nU_2. The current continues rising but slowly. On the primary side, the current path is still made by S_1, S_2, S_7, and S_8. On the secondary side, the current changes to the body diodes of Q_1 and Q_4.

Commutation state t_5: At the time t_5, the inductor current reaches the maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is -nU_2. The current drops from the peak. On the primary side, the current path is combined with the Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_1 and Q_4 are in the on state.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is -(U_1+nU_2). Hence, the current decreases. On the primary side, the current path changes to the body diodes of S_3, S_4, S_5, and S_6 for a short time.

Commutation state t_7: At the time t_7, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_1, and Q_4 are active at this time.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the current direction becomes negative. The voltage across the inductor is $-(U_1+nU_2)$. The negative current increases. On the primary side, the current path changes to Si IGBTs S_3, S_6, SiC MOSFETs S_4, and S_5. On the secondary side, the current flows through Q_1 and Q_4.

Commutation state t_8: At the time t_8, on the primary side, the SiC MOSFETs S_4, S_5, Si IGBTs S_3, and S_6 are in conduction. On the secondary side, Q_1 turns off, Q_2 turns on, and Q_4 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$. The negative current increases. On the primary side, the current path is made by S_3, S_4, S_5, and S_6. On the secondary side, the current flows through Q_4 and the body diode of Q_2.

Commutation state t_9: At the time t_9, on the primary side, the SiC MOSFETs S_4, S_5, Si IGBTs S_3, and S_6 are in the on state. On the secondary side, Q_4 turns off, Q_3 turns on, and Q_2 is active.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the voltage across the inductor is $-(U_1-nU_2)$. The negative current continues increasing but slowly. It will reach the negative peak current and start another switching cycle. On the primary side, the current path is still made by S_3, S_4, S_5, and S_6. On the secondary side, the current changes to the body diodes of Q_2 and Q_3.

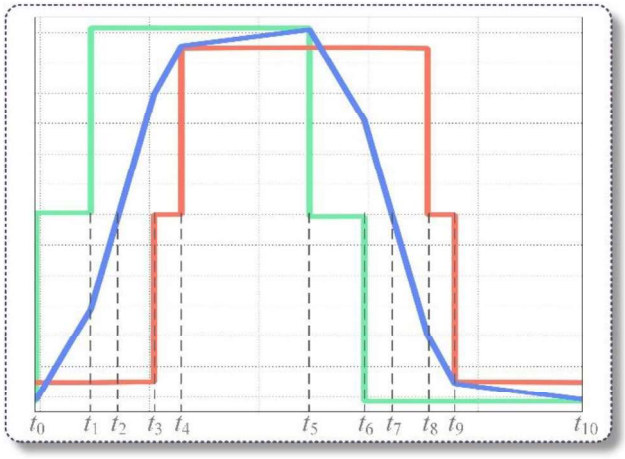

Fig. A.9 Voltage and current waveforms under mode IV.

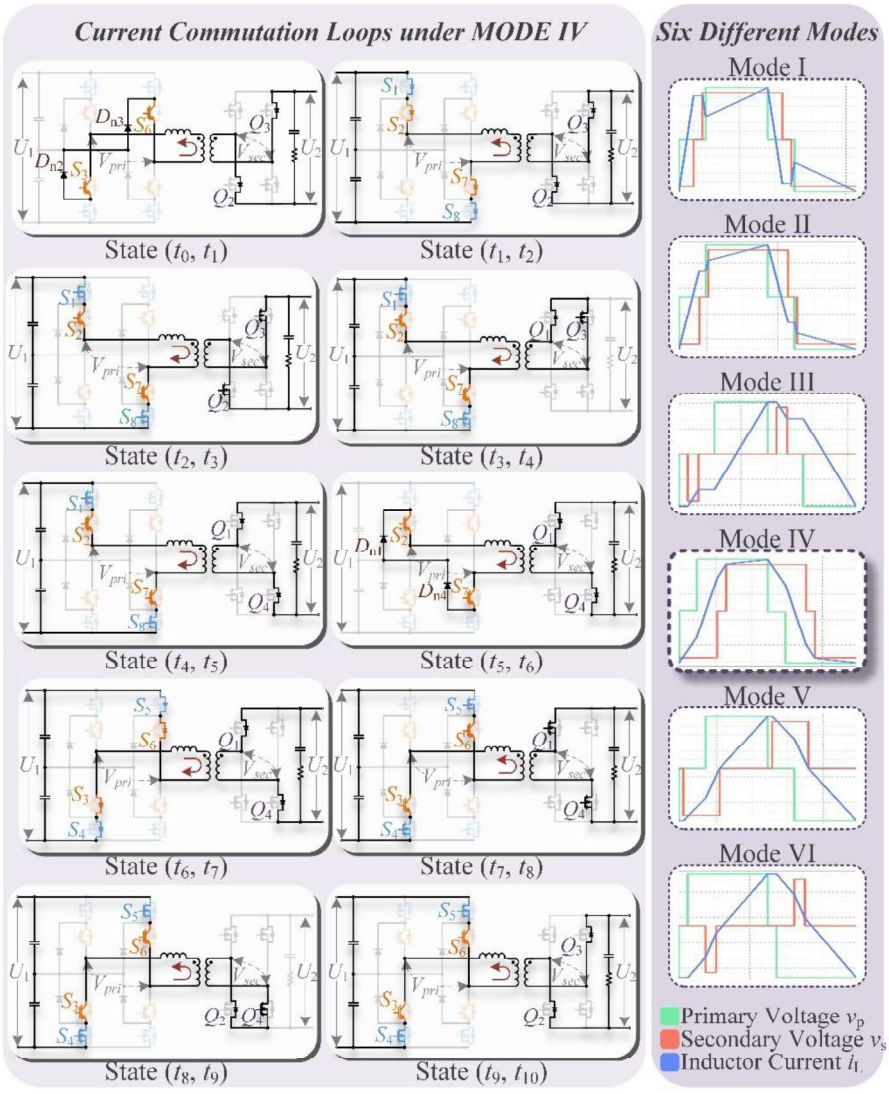

Fig. A.10 Current commutation loops under mode IV.

Mode V:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is 0 so the negative current remains. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBTs S_2, S_3, S_6 and S_7 are in conduction. On the secondary side, Q_4 turns off and Q_3 turns on, and Q_2 is still active.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is nU_2, and the negative current decreases. On the primary side, the current path is made by Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through body diodes of Q_2 and Q_3.

Commutation state t_2: At the time t_2, on the primary side, the Si IGBTs S_3 and S_6 turn off, and the SiC MOSFETs S_1 and S_8 turn on. On the secondary side, Q_2 and Q_3 are in the on state.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the voltage across the inductor is U_1+nU_2 so the negative current reduces sharply. On the primary side, the current path consists of body diodes of SiC MOSFETs S_1, S_8, Si IGBT S_2 and S_7. On the secondary side, the current flows through the body diodes of Q_2 and Q_3.

Commutation state t_3: At the time t_3, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2, and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1. The negative current decreases. On the primary side, the current path is combined with the body diodes of SiC MOSFET S_1, Si IGBT S_2, Si IGBT S_7, and SiC MOSFET S_8. On the secondary side, the current flows through the body diode of Q_3 and switch Q_1.

Commutation state t_4: At the time t_4, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_1 and Q_3 are activated at this time.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the current direction changes to positive. The voltage across the inductor is U_1. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, SiC MOSFETs S_1 and S_8. On the secondary side, the current flows through body diode of Q_1 and switch Q_3.

Commutation state t_5: At the time t_5, the inductor current reaches the maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_4 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is 0 so the positive current remains. On the primary side, the current path consists of Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2, S_3, S_6 and S_7 are in conduction. On the secondary side, Q_3 turns off and Q_4 turns on, and Q_2 is still active.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is $-nU_2$, and the negative current decreases. On the primary side, the current path is made by Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through body diodes of Q_1 and Q_4.

Commutation state t_7: At the time t_7, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_1 and Q_4 are in the on state.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the voltage across the inductor is $-(U_1+nU_2)$ so the negative current reduces sharply. On the primary side, the current path consists of body diodes of SiC MOSFETs S_4, S_5, Si IGBT S_3 and S_6. On the secondary side, the current flows through the body diodes of Q_1 and Q_4.

Commutation state t_8: At the time t_8, on the primary side, the SiC MOSFETs S_4, S_5, Si IGBTs S_3, and S_6 are in conduction. On the secondary side, Q_1 turns off and Q_2 turns on, and Q_4 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$. The positive current decreases. On the primary side, the current path is combined with the body diodes of SiC MOSFET S_4, Si IGBT S_3, Si IGBT S_6, and SiC MOSFET S_5. On the secondary side, the current flows through the body diode of Q_4 and switch Q_2.

Commutation state t_9: At the time t_9, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_2 and Q_4 are activated at this time.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the current direction changes to negative. The voltage across the inductor is $-U_1$. The negative current keeps increasing. It will reach the negative peak current and start another switching cycle. On the primary side, the current path changes to Si IGBTs S_3, S_6, SiC MOSFETs S_4 and S_5. On the secondary side, the current flows through body diode of Q_2 and switch Q_4.

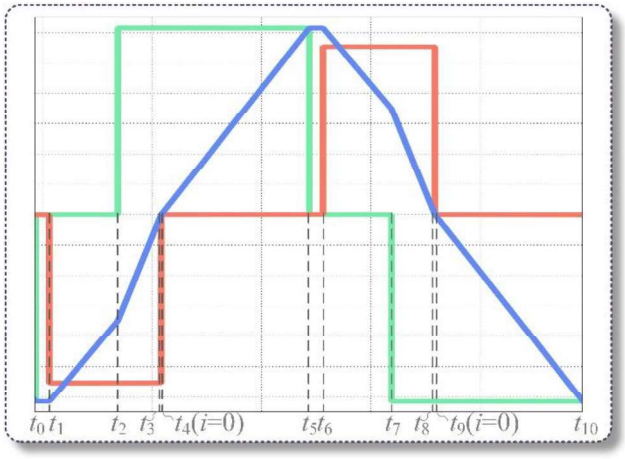

Fig. A.11 Voltage and current waveforms under mode V.

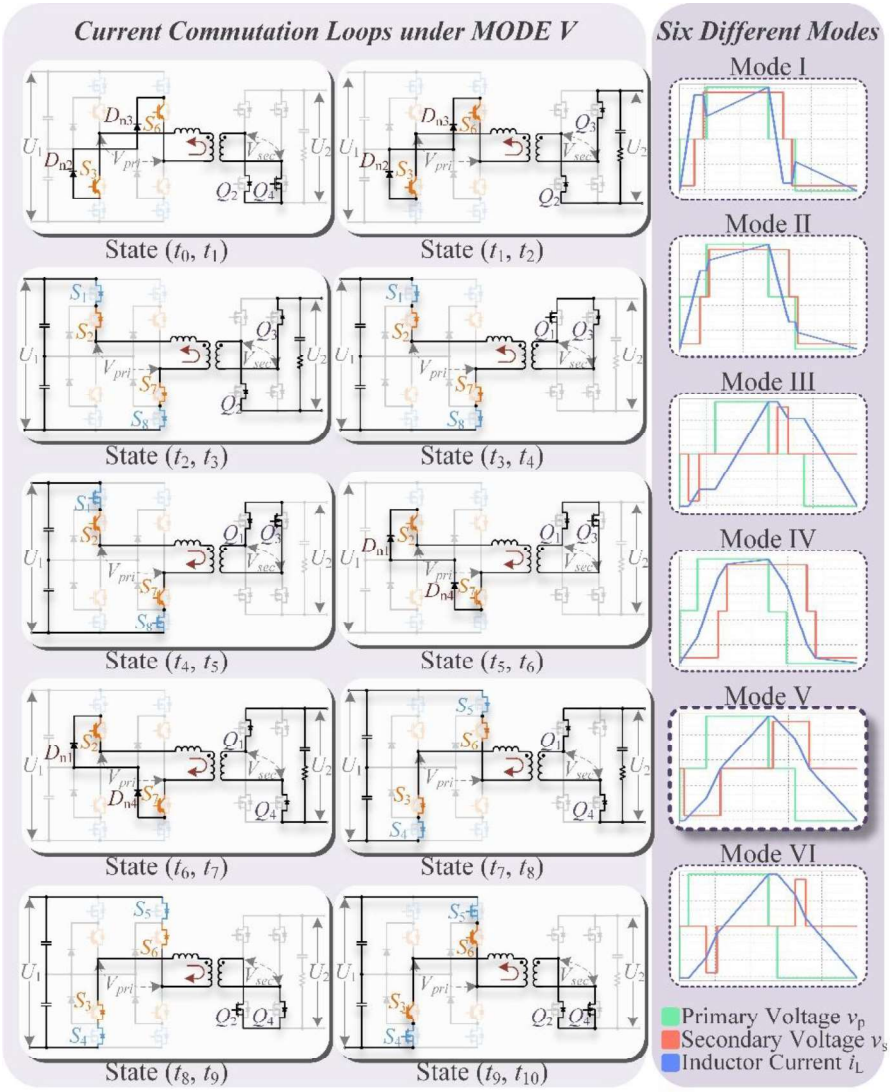

Fig. A.12 Current commutation loops under mode V.

Mode VI:

Commutation state t_0: At the time t_0, the inductor current reaches the negative maximum value. The SiC MOSFETs S_4 and S_5 on the primary side turn off the negative peak current, and the Si IGBTs S_2 and S_7 turn on at the same time. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_0, t_1): During the time between t_0 and t_1, the voltage across the inductor is 0 so the negative current remains. On the primary side, the current path consists of Si IGBT S_3, neutral diode D_{n2}, neutral diode D_{n3}, and Si IGBT S_6. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_1: At the time t_1, on the primary side, the Si IGBTs S_3 and S_6 turn off, and the SiC MOSFETs S_1 and S_8 turn on. On the secondary side, Q_2 and Q_4 are in the on state.

Commutation state (t_1, t_2): During the time between t_1 and t_2, the voltage across the inductor is U_1 so the negative current reduces. On the primary side, the current path consists of body diodes of SiC MOSFETs S_1, S_8, Si IGBT S_2 and S_7. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

Commutation state t_2: At the time t_2, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2 and S_7 are in conduction. On the secondary side, Q_4 turns off and Q_3 turns on, and Q_2 is still active.

Commutation state (t_2, t_3): During the time between t_2 and t_3, the voltage across the inductor is U_1+nU_2, and the negative current decreases sharply. On the primary side, the current path is made by body diodes of SiC MOSFETs S_1, S_8, Si IGBT S_2 and S_7. On the secondary side, the current flows through body diodes of Q_2 and Q_3.

Commutation state t_3: At the time t_3, on the primary side, the SiC MOSFETs S_1, S_8, Si IGBTs S_2, and S_7 are in conduction. On the secondary side, Q_2 turns off and Q_1 turns on, and Q_3 is still active.

Commutation state (t_3, t_4): During the time between t_3 and t_4, the voltage across the inductor is U_1. The negative current decreases. On the primary side, the current path is combined with the body diodes of SiC MOSFET S_1, Si IGBT S_2, Si IGBT S_7, and SiC MOSFET S_8. On the secondary side, the current flows through the body diode of Q_3 and switch Q_1.

Commutation state t_4: At the time t_4, the negative inductor current reduces to zero. The switches S_1, S_2, S_7, S_8, Q_1 and Q_3 are activated at this time.

Commutation state (t_4, t_5): During the time between t_4 and t_5, the current direction changes to positive. The voltage across the inductor is U_1. The positive current keeps increasing. On the primary side, the current path changes to Si IGBTs S_2, S_7, SiC MOSFETs S_1 and S_8. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_5: At the time t_5, the inductor current reaches the maximum value. On the primary side, the SiC MOSFETs S_1 and S_8 turn off the positive peak current, and the Si IGBTs S_3 and S_6 receive the driving signals at the same time. On the secondary side, Q_1 and Q_3 are active.

Commutation state (t_5, t_6): During the time between t_5 and t_6, the voltage across the inductor is 0 so the negative current remains. On the primary side, the current path consists of Si IGBT S_2, neutral diode D_{n1}, neutral diode D_{n4}, and Si IGBT S_7. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_6: At the time t_6, on the primary side, the Si IGBTs S_2 and S_7 turn off, and the SiC MOSFETs S_4 and S_5 turn on. On the secondary side, Q_1 and Q_3 are in the on state.

Commutation state (t_6, t_7): During the time between t_6 and t_7, the voltage across the inductor is $-U_1$ so the positive current reduces. On the primary side, the current path consists of body diodes of SiC MOSFETs S_4, S_5, Si IGBT S_3 and S_6. On the secondary side, the current flows through the body diode of Q_1 and switch Q_3.

Commutation state t_7: At the time t_7, on the primary side, the SiC MOSFETs S_4, S_5, Si IGBTs S_3 and S_6 are in conduction. On the secondary side, Q_3 turns off and Q_4 turns on, and Q_1 is still active.

Commutation state (t_7, t_8): During the time between t_7 and t_8, the voltage across the inductor is $-(U_1+nU_2)$, and the positive current decreases sharply. On the primary side, the current path is made by body diodes of SiC MOSFETs S_4, S_5, Si IGBT S_3 and S_6. On the secondary side, the current flows through body diodes of Q_1 and Q_4.

Commutation state t_8: At the time t_8, on the primary side, the SiC MOSFETs S_4, S_5, Si IGBTs S_3, and S_6 are in conduction. On the secondary side, Q_1 turns off and Q_2 turns on, and Q_4 is still active.

Commutation state (t_8, t_9): During the time between t_8 and t_9, the voltage across the inductor is $-U_1$. The positive current decreases. On the primary side, the current path is combined with the body diodes of SiC MOSFET S_4, Si IGBT S_3, Si IGBT S_6, and SiC MOSFET S_5. On the secondary side, the current flows through the body diode of Q_4 and switch Q_2.

Commutation state t_9: At the time t_9, the positive inductor current reduces to zero. The switches S_3, S_4, S_5, S_6, Q_2 and Q_4 are activated at this time.

Commutation state (t_9, t_{10}): During the time between t_9 and t_{10}, the current direction changes to negative. The voltage across the inductor is $-U_1$. The negative current keeps increasing. It will reach the negative peak current and start another switching cycle. On the primary side, the current path changes to Si IGBTs S_3, S_6, SiC MOSFETs S_4 and S_5. On the secondary side, the current flows through the body diode of Q_2 and switch Q_4.

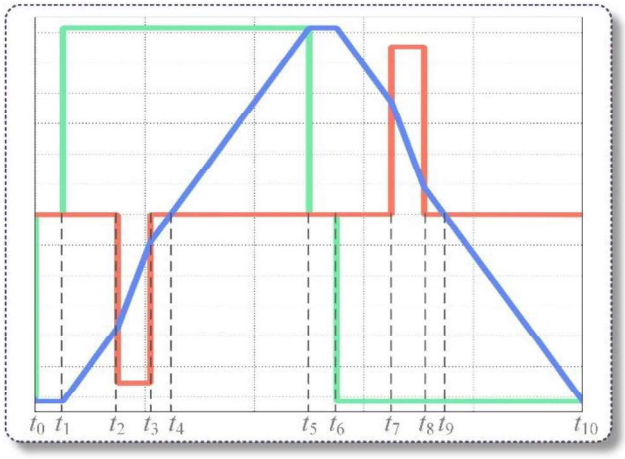

Fig. A.13 Voltage and current waveforms under mode VI.

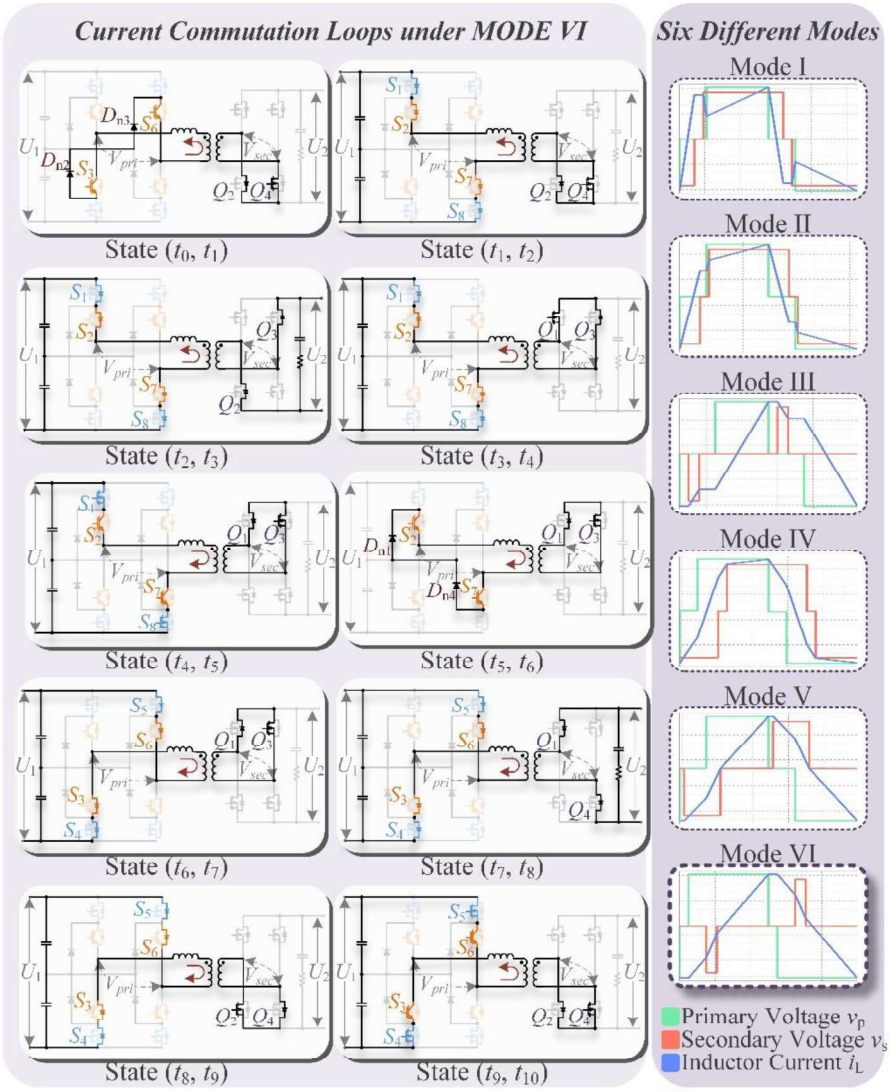

Fig. A.14 Current commutation loops under mode VI.

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