Transient Electrical Thermal Analysis of ESD Process using 3-D Finite Element Method

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***Abstract*—In this work, the transient electrical-thermal response of a simple ESD protection circuit to excessive current during an electrostatic discharge (ESD) event is investigated numerically, using 3-D finite element analysis (FEA). The 3-D transient temperature distribution in the circuit can be revealed and the fusing phenomenon of interconnection is captured during the ESD process using human body model (HBM). The method in this work provides a quantitative approach to study the ESD damaging process in the future.**

***Index Terms*—electrostatic discharge, finite element method**

I. INTRODUCTION

As microelectronics technology continues to shrink in device dimensions, the dimensions of the transistors, interconnects, and insulation layers are decreasing, resulting in breakdown damage at lower energy levels. This, together with the changing application environment especially toward increasing portable applications, renders electrostatic discharge (ESD) damage in integrated circuits as one of the major reliability issues [1].

Duration an ESD event, large amount of electrostatic charge is discharged within duration in the order of tens of nanoseconds. This current spike can lead to an instantaneous rise in the device temperature that often results in thermal damages. ESD failure modes are in the form of gate oxide rupture, junction filamentation and spiking, charge injection as well as interconnect and poly-silicon burn-out [1]. Transient electrical-thermal behavior of various ESD protection elements in 2-D has been reported in literature using various simulators, e.g. MEDICI[@] [2], [3], LIAGAMENT[@] [4], etc.

The modeling of ESD process in 3-D finite element model is very difficult due to its fast rise time, short duration as well as the size of the model. On the other hand, 3-D FEA is necessary as all integrated circuits are 3-D in their physical implementation, and thermal dissipation is critically dependent on the surrounding materials and structure. So far, there are very few studies on the transient thermal effect of ESD and its corresponding physical damage process to the integrated circuit [5].

In this work, we present a first attempt to model the transient thermal response of the protection circuit during ESD event using finite element analysis (FEA) and examine how the temperatures of the different parts of an ESD protection circuit evolve during the short ESD process (~200 ns). In particular, we focus on the interconnects as ESD failure in interconnects has been reported experimentally [1], but it is rarely studied. The melting phenomenon is also taken into consideration through the phase change analysis.

II. ESD MODEL

There are 3 basic models for ESD used in electronic industry today, namely the human body model (HBM), machine model (MM), and charged device model (CDM). The HBM has a 100 pF capacitor charged to a given ESD voltage, and then discharged into the device in series with a 1500 Ω resistor, resulting in transient current flowing through the device. With the ESD protection circuit, it can divert this potentially damaging charge away from the sensitive circuitry and protect the system from permanent damage. In this work, we choose the diode protection circuit as the ESD protection circuit together with an inverter for illustration. Diode protection circuit is frequently used as ESD protection circuit, especially in RF applications [6].

The circuit schematic is shown in Fig. 1. D1 and D2 are large-area diodes with direct connections to Vcc and GND rails. M1 and M2 form a simple inverter. The current pulse based on HBM will be the input load for the subsequent finite element analysis. A positive ESD voltage of 1 kV is assumed in this work. The parasitic lumped elements in the HBM are found to have small effect on the HBM current pulse, and will not be included in our modeling for simplicity. The current peak is calculated to be 667 mA based on the HBM. The rise time tr is chosen to be 10 ns and the decay time constant is 150 ns. All these values are typical for HBM [7].

The input ESD pulse is shown in Fig. 2 and it will be shunt through D1 to Vcc during ESD process. The input ESD pulse can be divided into two load steps. Load step one is a linearly increasing current spike with 10 ns rise time. In load step two, the current pulse decays exponentially with a time constant of 150 ns. The two loads will be applied sequentially in our FEA. It is noted that the input ESD pulse is dependent on the ESD models and it can be modified in the future for the specific ESD simulations.

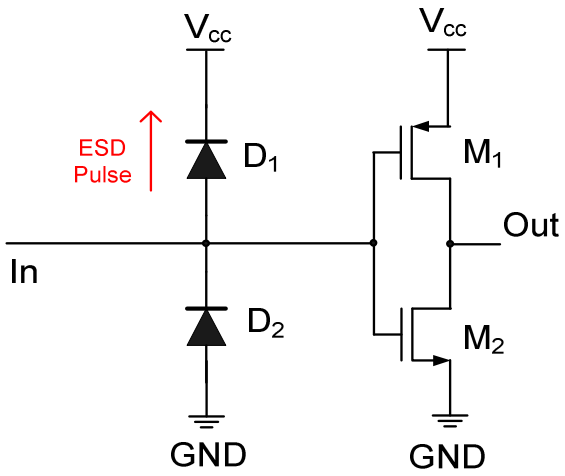

Figure 1. Schematic of an ESD protection circuit with an inverter.

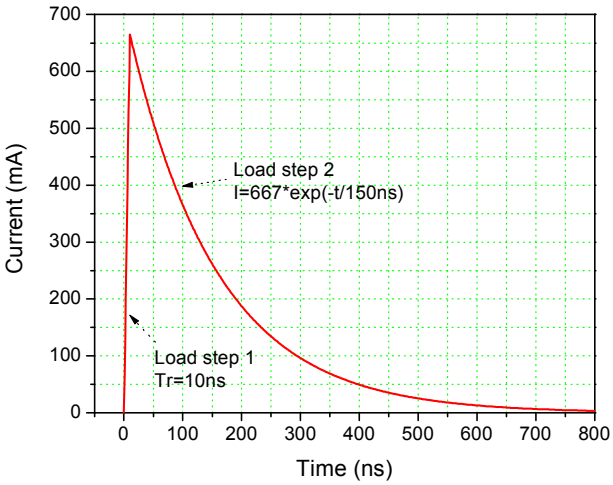

Figure 2. Input ESD pulse based on HBM.

III. FINITE ELEMENT ANALYSIS

The corresponding 3-D physical model of the ESD protection circuit is drawn using Design Modeler@ in ANSYS Workbench@ as shown in Fig. 3. The Si substrate and the surrounding dielectrics (SiO_2) are not shown for clear illustration. The model is then meshed using Meshing@ with 4-node tetrahedral elements in ANSYS Workbench@. The meshed finite element model is transferred to ANSYS Classic@ through ANSYS input file for the simulation. There are 22485 nodes and 123192 elements in the finite element model. The meshed model is shown in Fig. 4 with the whole circuit on Si substrate. The Si substrate has a dimension of $15\times20\times5$ μm^3. Interconnects are drawn according to Chartered 0.18 µm/5V design rule. The meshing density for the ESD protection circuit is higher than that of the substrate and the surrounding dielectrics for simulation accuracy with reasonable simulation time.

During an ESD event, D_1 is in the forward bias region for a positive ESD pulse. For a diode in forward bias, its I-V characteristic can be represented by two piecewise linear I-V curves. Since the ESD current pulse is high and its rise time is short, the diode can be represented by the small resistance as obtained from the piecewise linear I-V curve with larger current, and a typical value of 1 Ω is used in this work.

Therefore, we can model D_1 and D_2 as rectangular thin layer with appropriate resistivity models (doped-Si) in the finite element model in Fig. 3 and Fig. 4. It is worth mentioning that the layout of the ESD protection circuit can always be modified to meet the specific needs of ESD modeling in the future.

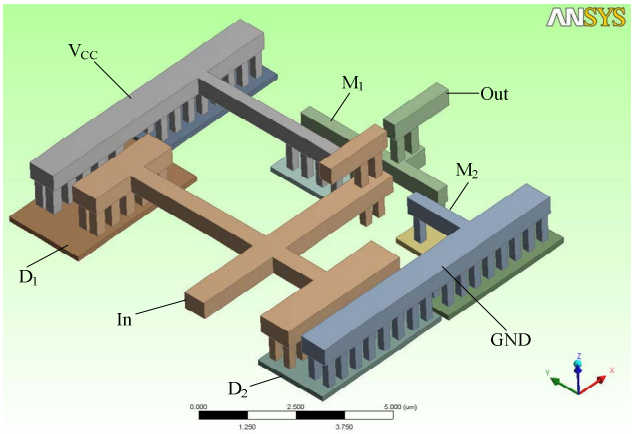

Figure 3. 3-D ANSYS geometry model for the ESD protection circuit.

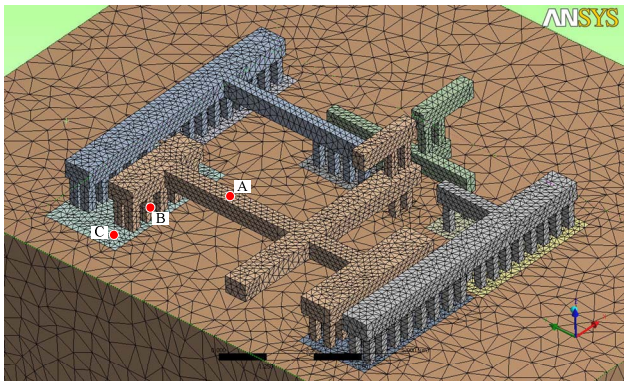

Figure 4. Finite element model for the ESD protection circuit.

As ESD is a transient nonlinear electrical-thermal problem in nature, it is important to take the nonlinear temperature dependent electrical and thermal properties of the materials into consideration. For example, the resistivity of Cu will increase with increasing temperature due to a positive temperature coefficient of resistivity (TCR) while its thermal conductivity drops at high temperature. Doped-Si for the protection diode and Cu may melt during ESD process if the local temperature is above their melting points. The phase change is implemented by defining the enthalpy in ANSYS. The enthalpy for Cu and doped-Si is shown in Fig. 5. Their values are calculated based on density, specific heat, heat of fusion, heat of vaporization, melting point and boiling point. Therefore, complicated time-dependent non-uniform self-heating in the ESD structure will be expected in the simulations.

ANSYS element *solid69* is chosen for the coupled field electrical-thermal analysis. Since simulation results are dependent on the boundary conditions, it is crucial to apply the

correct boundary conditions to represent the actual ESD test conditions. In this work, we assume that ESD test is conducted at ambient temperature with natural convection on the side surfaces of the chip, and hence in our simulation, the substrate bottom is fixed at an ambient temperature of 25 °C. The top and side surfaces are subject to natural convection with a convection coefficient of 10 W/mm^2·K [8].

ESD current pulse in Fig. 2 is forced to the end nodes on the Cu input surface with the voltage coupled, and the nodes on the lower surface of D_1 side are grounded. In the simulation, the time step size is chosen to be 1 ns for the solution to converge without unwanted oscillations. To include the phase change effect in the simulation, automatic time stepping option is activated with Euler backward difference scheme used for the transient time integration [9]. To save the simulation time, simulation terminates at 160 ns.

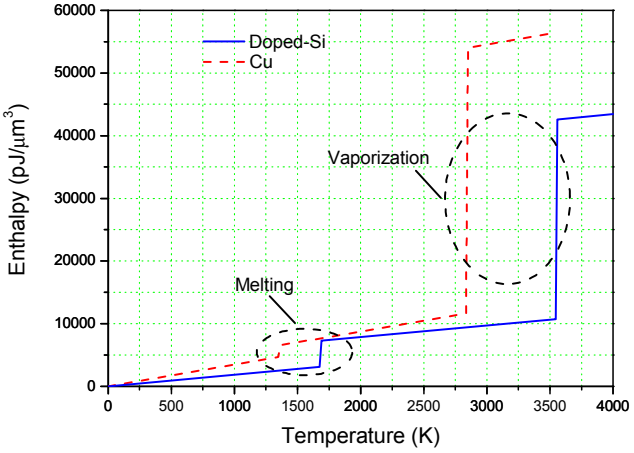

Figure 5. Computed Enthalpy for Cu and doped-Si.

IV. Results and Discussion

The simulated temperature profile at different locations in the ESD protection circuit during the load history is shown in Fig. 6. Location A, B, C is taken from the Cu line, Cu via, and doped-Si (Diode D1) respectively as shown in Fig. 4. Compared with input current pulse with the maximum at 10 ns in Fig. 2, the temperature reaches maximum around 40 ns for via and doped-Si. For Cu line, the temperature peaks around 100 ns. The phase change (melting) for Cu can be observed clearly from the temperature profile of Cu in Fig. 6 and the melting process lasts around 10 ns. This phenomenon can be explained as follows.

As the resistivity for doped-Si is higher than that of Cu when temperature is low, the temperature increasing rate for doped-Si and via is much faster than Cu line as high current is passing through them as shown in Fig. 6. The melting of the doped-Si and via is very fast and it is not obvious from the graph. This can be resolved by imposing a smaller time step (e.g. 0.1 ns), resulting in much longer simulation time. The temperature profile decays gradually after 100 ns due to the decaying input current pulse. Therefore, 160 ns simulation time is sufficient for the present work.

The temperature distribution at different time during the transient ESD process is shown in Fig. 7. As shown in Fig. 7(a), local heating starts in the doped-Si at the initial stage. At the time around 30 ns in Fig. 7(b), both via and Cu line are heated to a high temperature with the maximum temperature remaining in doped-Si. Finally, the maximum temperature site moves to the Cu line. The change of maximum temperature location during the ESD process is expected due to the nonlinear temperature dependent electrical properties of Cu and doped-Si.

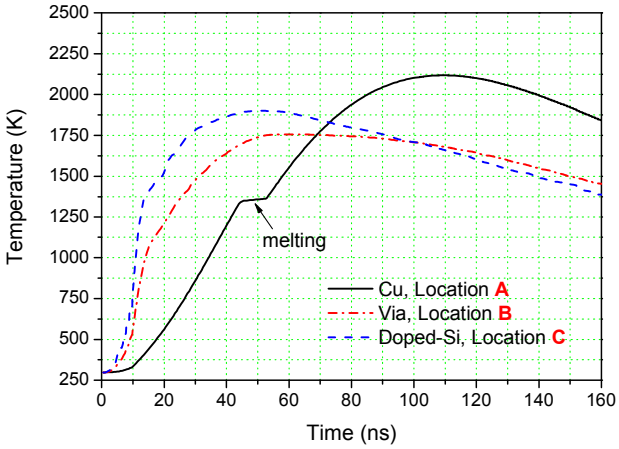

Figure 6. Temperature profile at different location of the ESD protection circuit.

The observed change in temperature distribution in Fig. 7 is attributed to the opposite electrical characteristic between Cu and poly-Si. Cu resistivity increases with temperature while the opposite is for poly-Si. As temperature increases, Joule heat by Cu increases while that by Poly-Si decreases, shifting the hot spot from poly-Si to Cu as the heating continues due to the high current from ESD.

At the time of 80 ns in Fig. 7(c), we can also see that the adjacent inverter circuit remains at the ambient temperature. This shows that in the short duration of ESD process, the surrounding sensitive circuitry is not affected by high current pulse through the ESD protection circuit, indicating the effectiveness of the protection circuit against HBM ESD pulse.

It is also noted that vaporization is not observed in Fig. 6 even the vaporization has been included in the enthalpy definition in Fig. 5. This is due to the relatively low ESD voltage (1 kV) chosen for the current simulation. Such vaporization is indeed observed by Vinson et al. [10] who performed experiments with HBM, MM and CDM.

V. Conclusion

In this work, the transient electrical-thermal response of a simple ESD protection circuit to excessive current during an ESD event is investigated numerically, using a three-dimensional finite element analysis (FEA). The transient temperature distributions during the short ESD process have been revealed with 3-D FEA. The method in this work provides a quantitative approach to study the ESD damaging process in the future.

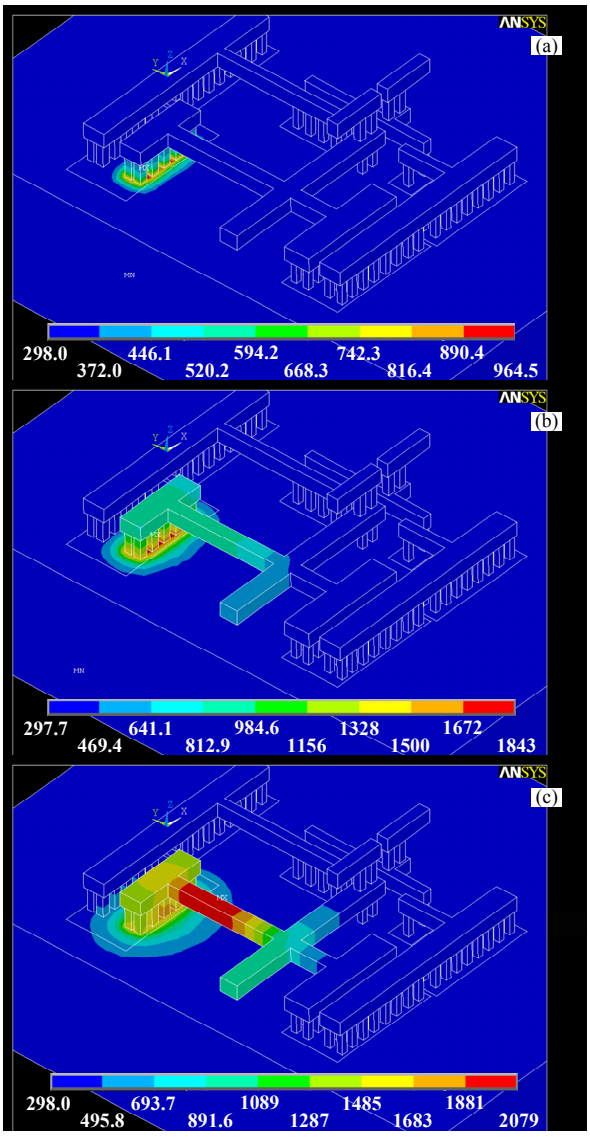

Figure 7. Temperature distributions at different time during the transient ESD process. (a) 10 ns (b) 30 ns (c) 80 ns (Unit: K)

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