Formation of periodic interfacial misfit dislocation array at the InSb/GaAs interface via surface anion exchange

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The relationship between growth temperature and the formation of periodic interfacial misfit (IMF) dislocations via the anion exchange process in InSb/GaAs heteroepitaxy was systematically investigated. The microstructural and electrical properties of the epitaxial layer were characterized using atomic force microscope, high-resolution x-ray diffraction, transmission electron microscopy, and Hall resistance measurement. The formation of interfacial misfit (IMF) dislocation arrays depended on growth temperature. A uniformly distributed IMF array was found in a sample grown at 310 °C, which also exhibited the lowest threading dislocation density. The analysis suggested that an incomplete As-for-Sb anion exchange process impeded the formation of IMF on sample grown above 310 °C. At growth temperature below 310 °C, island coalescence led to the formation of 60° dislocations and the disruption of periodic IMF array. All samples showed higher electron mobility at 300 K than at 77 K. *Published by AIP Publishing.*
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I. INTRODUCTION

The monolithic integration of highly mismatched material has received much attention due to its benefit in new combinations of high performance microelectronic, photonic devices, and established substrates such as Si, Ge, and GaAs.[1] Due to high electron mobility (77 000 $cm^2/V\ s$) and narrow room temperature band gap energy (0.18 eV), InSb is widely considered as an ideal candidate for channel material in high electron mobility transistor (HEMT)[2] applications and for photon absorbers in mid-infrared photonic applications.[3] However, unlike the semi-insulating GaAs substrates, a semi-insulating InSb substrate is not commercially available. Integrating InSb on GaAs will not only provide a semi-insulating substrate but also enable the co-existence of InSb-based and GaAs-based devices on a single platform.

Despite all benefits, it is extremely challenging to integrate InSb on a GaAs platform due to the considerable lattice mismatch between InSb and GaAs (14.6%). The conventional direct growth method of InSb on GaAs resulted in high threading dislocation density (TDD) and other defects in the InSb layer.[4] The application of various buffer layer technologies has been reported to reduce the TDD in InSb grown on GaAs.[5,6] Lattice strain was accommodated by a thick ($>1\ \mu m$) buffer layer grown on a GaAs layer. This thick buffer layer was shown to effectively reduce TDD and other defect densities in the InSb layer.[7]

Utilizing uniform 90° misfit dislocations to accommodate the lattice mismatch between the epilayer and substrate is another way to accommodate the mismatch. The 90° dislocations relax more strain than 60° dislocations. Furthermore, the 90° dislocations do not glide on a (111) lattice plane to form detrimental threading dislocations. This technology can be considered as a "buffer layer free" technology as the deposition of a thick buffer layer to relax lattice strain is no longer required. Maree *et al.* used transmission electron microscopy (TEM) to investigate the diamond-type semiconductor heteroepitaxy and suggested the majority of the interfacial misfit (IMF) dislocations is 90° type when the lattice mismatch is above 6%.[8] Some researchers attempted to form uniform 90° misfit dislocations in mismatched heterogeneous structures.[9,10] Huang *et al.* showed that a perfect 90° IMF dislocations array was formed at the hetero-interface under specific growth conditions.[11,12]

A theoretical calculation shows that TDD can be minimized and strain can be fully relaxed by the IMF array.[13] Huang *et al.* successfully decreased TDD in the GaSb layer grown on GaAs from $10^9\ cm^{-2}$ to $10^5\ cm^{-2}$ using the IMF method[14]. The type of misfit dislocation formed at the interface is dependent on the magnitude of the lattice mismatch induced strain. A strain induced by the lattice mismatch $>7\%$ favors the formation of 90° dislocations compared to 60° dislocations.[15] However, the mechanism of IMF formation in the heteroepitaxy of InSb on GaAs remains unclear. Furthermore, no relationship between IMF formation and growth temperature has been reported yet for InSb/GaAs heteroepitaxy.

In this study, four samples with an InSb layer grown on a GaAs substrate were grown using a molecular beam epitaxy (MBE) system at different growth temperatures (350 °C, 310 °C, 270 °C, and 220 °C) to investigate the IMF formation in heteroepitaxial InSb on GaAs. In contrast to previous studies[14,16] where a monolayer of Sb atoms was formed by depositing Sb atoms on a Ga-rich GaAs surface, this study utilized an As-for-Sb anion exchange process to form a monolayer of Sb atoms on the GaAs surface. The advantage of this process is that it occurs at a lower temperature than the former process which relies on the formation of a Ga-rich GaAs surface. The formation of a Ga-rich GaAs surface requires a substrate temperature of 560 °C or higher,

which may lead to a rough GaAs surface.[17] The microstructures and electrical properties of the InSb layer were investigated using high-resolution x-ray diffraction (HR XRD), transmission electron microscopy (TEM), atomic force microscope (AFM), and a Hall-effect measurement system. A well-suited growth temperature for an InSb layer with the lowest TDD is worked out. Furthermore, the relationship between IMF formation and growth temperatures is analyzed. The formation of 90° and 60° misfit dislocations at different temperatures is also discussed.

II. EXPERIMENTAL PROCEDURES

All experiments were carried out in a solid source molecular beam epitaxy (MBE) equipped with arsenic (As) and antimony (Sb) valved cracker sources which can provide As_2 and Sb_2 dimers. The substrate temperature was measured by a tungsten/rhenium alloy thermocouple, which was placed at the back of the molybdenum substrate holder. The oxide desorption temperature of the GaAs substrate (580 °C) was used to calibrate the thermocouple reading. The onset of oxide desorption was detected by *in-situ* reflection high-energy electron diffraction (RHEED) observation. After the oxide desorption, 200 nm GaAs was grown on the substrate in 12 min at a growth rate of 17 nm/min to smoothen the surface. The RHEED pattern exhibited a clear (2×4) As-terminated surface reconstruction after the buffer growth. Subsequently, the As valve was closed, and the substrate temperature was lowered to 540 °C and maintained at this temperature for 10 min to reduce the As background pressure. The RHEED pattern remained the same throughout this period.

Thereafter, the substrate temperature was lowered to the respective growth temperature for each of the four samples (350 °C, 310 °C, 270 °C, and 220 °C), and the conditioned substrate was exposed to Sb flux with a beam equivalent pressure (BEP) of $\sim 1.2 \times 10^{-6}$ Torr. The As atoms at the surface were gradually replaced by Sb atoms via anion exchange process during this Sb supply step. After 4 min of Sb supply, a streaky (1×3) Sb-rich surface reconstruction was observed with RHEED. Following the occurrence of this (1×3) reconstruction, 0.7 μm InSb layers were grown at set temperatures with a Sb/In beam equivalent pressure ratio of 4 and a growth rate of 15 nm/min. During the initial stage of growth, the streaky (1×3) pattern rapidly changed to a bright spotty pattern. This observation indicated that there was an island-like growth mode occurring at this stage. Subsequently, the RHEED patterns slowly recovered to a streaky (1×3) pattern. The recovery time increased with the decreasing substrate temperature, and the longest time is about 2 min which was observed in the sample grown at 220 °C. In the following, RHEED patterns kept streaky (1×3) which indicated that all samples kept layer by layer growth mode until the end of growth.

III. RESULTS AND DISCUSSION

Table I lists the degree of strain relaxation of the InSb layers, the full-width at half-maximum (FWHM) of the x-ray diffraction (XRD) rocking curves, the root mean square (RMS) roughness in the AFM measurements, and charge carrier concentrations for each sample. The degree of relaxation in the InSb layers was derived from symmetric and asymmetric ω-2θ XRD scans from (004) and (115) reflexes in the XRD measurements. All samples were close to fully relaxed (>98% of relaxation), and the degree of relaxation increased with decreasing growth temperature. As the presence of threading dislocations in an epilayer could result in significant broadening of the symmetric rocking curve,[18] the FWHMs obtained from the (004) rocking curves can be used to qualitatively compare the TDD in the samples.[19,20] From the FWHM comparison in Table I, it is evident that the changes in growth temperature can influence the TDD of the samples. The (004) rocking curve FWHM analysis suggests that TDD is the lowest in the InSb sample grown at 310 °C.

Figure 1 shows the AFM images for the four samples with InSb layers grown at (a) 350 °C, (b) 310 °C, (c) 270 °C, and (d) 210 °C, respectively. The RMS roughness for each sample is listed in Table I. Samples 1–3 show a smooth surface with a RMS roughness below 1.3 nm. However, the sample with an InSb layer grown at 210 °C (Sample 4 in Figure 1(d)) exhibits a high RMS roughness of 8.8 nm, and a high density of steps was observed on the surface of the epilayer. This comparatively high RMS roughness can be attributed to the limited adatom diffusivity at a very low temperature.[21] Moreover, craters are observed on the surface of Sample 4. These craters exhibited random size distribution and shape. This was in contrast to the previous reported pinhole defects shown in a highly mismatched epilayer, where the pinhole defects had been caused by threading dislocations and low atomic migration rate.[22] These pinhole defects have a uniform size and are hexagonal in shape. The origin of the craters shown in Sample 4 will be discussed later in conjunction with microstructural information.

To further understand the possible mechanism for growth temperature influence on the IMF array, we studied the InSb/GaAs interface of the samples using cross-sectional TEM. Sample 2 exhibited the narrowest FWHM in XRD rocking curves and implied the lowest TDD among all samples. In the bright field TEM image of Sample 2, as shown in Figure 2(a), a smooth and abrupt InSb/GaAs interface with

TABLE I. Overview of XRD, AFM, and Hall resistance measurement results for InSb/GaAs heteroepitaxy at different growth temperatures.

Sample No.	Growth temperature (°C)	Strain Relaxation (%)	XRD rocking curve FWHM (arcsec)	RMS Roughness (nm)	300 K charge carrier concentration (10^{16} cm^{-3})	77 K charge carrier concentration (10^{16} cm^{-3})
1	350	98.7	454	0.9	1.852	1.056
2	310	98.9	415	1.1	1.647	0.849
3	270	99.1	462	1.3	2.278	1.435
4	220	99.9	650	8.8	3.374	2.074

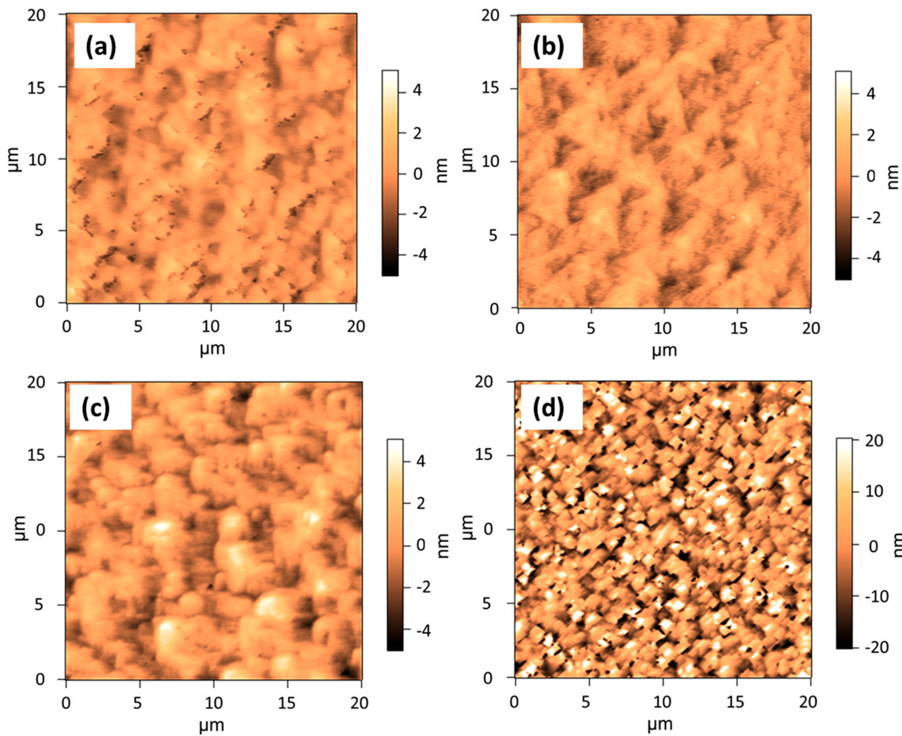

FIG. 1. AFM images (20 μm × 20 μm) of 0.7 μm InSb grown on GaAs (100) substrate at (a) 350 °C, (b) 310 °C, (c) 270 °C, and (d) 210 °C.

no obvious threading dislocations arising from the interface is observed. Under higher magnification, uniformly distributed black dots along the InSb/GaAs interface are illustrated in Figure 2(b), and these dots indicated interfacial misfit dislocations. A high-resolution image about the detail of these interfacial dislocations is shown in the inset of Figure 2(b). In this inset, the separation of two adjacent interfacial misfit dislocations cis is measured to be 3.1 ± 0.2 nm. It is clear that long-range uniform 90° misfit interfacial dislocation array has been formed on InSb/GaAs interface. Based on the atomic model of the IMF method, if the entire lattice mismatch induced strain is relaxed by 90° interfacial misfit dislocations, the distances between two adjacent dislocations, S, can be calculated by the following equation:

$$s = \frac{b}{f}, \tag{1}$$

where b is the Burgers vector of the 90° misfit dislocation in the InSb layer and f is the lattice mismatch between InSb and GaAs. Inserting $|b| = 4.58$ Å and $f = 14.6\%$ into Eq. (1), the theoretical value of S is 3.14 nm, which matches the measurement result of 3.1 ± 0.2 nm.

The InSb/GaAs interface of Sample 1 is shown in Figure 2(c). Unlike Sample 2, threading dislocations arising from the interface were observed. To investigate the origin of the threading dislocations, a high-resolution TEM image (shown in Figure 2(d)) was taken at the InSb/GaAs interface where the threading dislocations arise (marked by a white dotted box in Figure 2(c)). Clear and distinct contrasts in the InSb layer and GaAs layer indicate an abrupt InSb/GaAs interface. A discontinuous V-shaped region (two bifurcate lines arising from interface and marked by two opposed white arrows) is found at the left of Figure 2(d). A previous study suggested that these dots indicate 90° misfit dislocation nucleation areas.[23]

Since the details of the interfacial atomic arrangement in the image are too noisy to confirm the type of dislocations, a Fourier mask filter was applied on two selected areas (marked E and F) in Figure 2(d) to reduce the noise and investigate the atomic arrangement around the InSb/GaAs interface. The results are shown in Figures 2(e) and 3(f). Figure 2(e) shows the interface at the V-shaped regions where two 90° and two 60° misfit dislocations are found. A 90° misfit dislocation is associated with two extra lattice planes symmetrically located at the interface, while a 60° misfit dislocation is only associated with one extra lattice plane. The distance between the two adjacent 60° misfit dislocations is 5.3 nm. Due to the fact that 60° misfit dislocations only relax half the strain compared to the 90° misfit dislocations,[15] the separation distance between two adjacent 60° dislocations should be half of the distance between two 90° dislocations[24] if the strain is to be fully relaxed by the 60° dislocations. Therefore, 60° dislocations with a separation distance of 5.3 nm on an InSb/GaAs interface are insufficient to fully relax the strain energy.

Since the degree of relaxation in Sample 1 is ~98.7%, the residual strain has to be relaxed through other mechanisms such as the formation of threading dislocations.[25] Figure 2(f) shows a uniform 90° misfit dislocation array with a separation of 3.2 nm in Area F. There are no other visible defects around that area, and the strain is fully relaxed. Compared with Area F, the formation of a 90° misfit dislocations array has been obstructed in Area E.

Figure 3(a) shows a bright-field TEM image of Sample 3 at the InSb/GaAs interface. No visible threading dislocations arising from the interface are observed. At the top

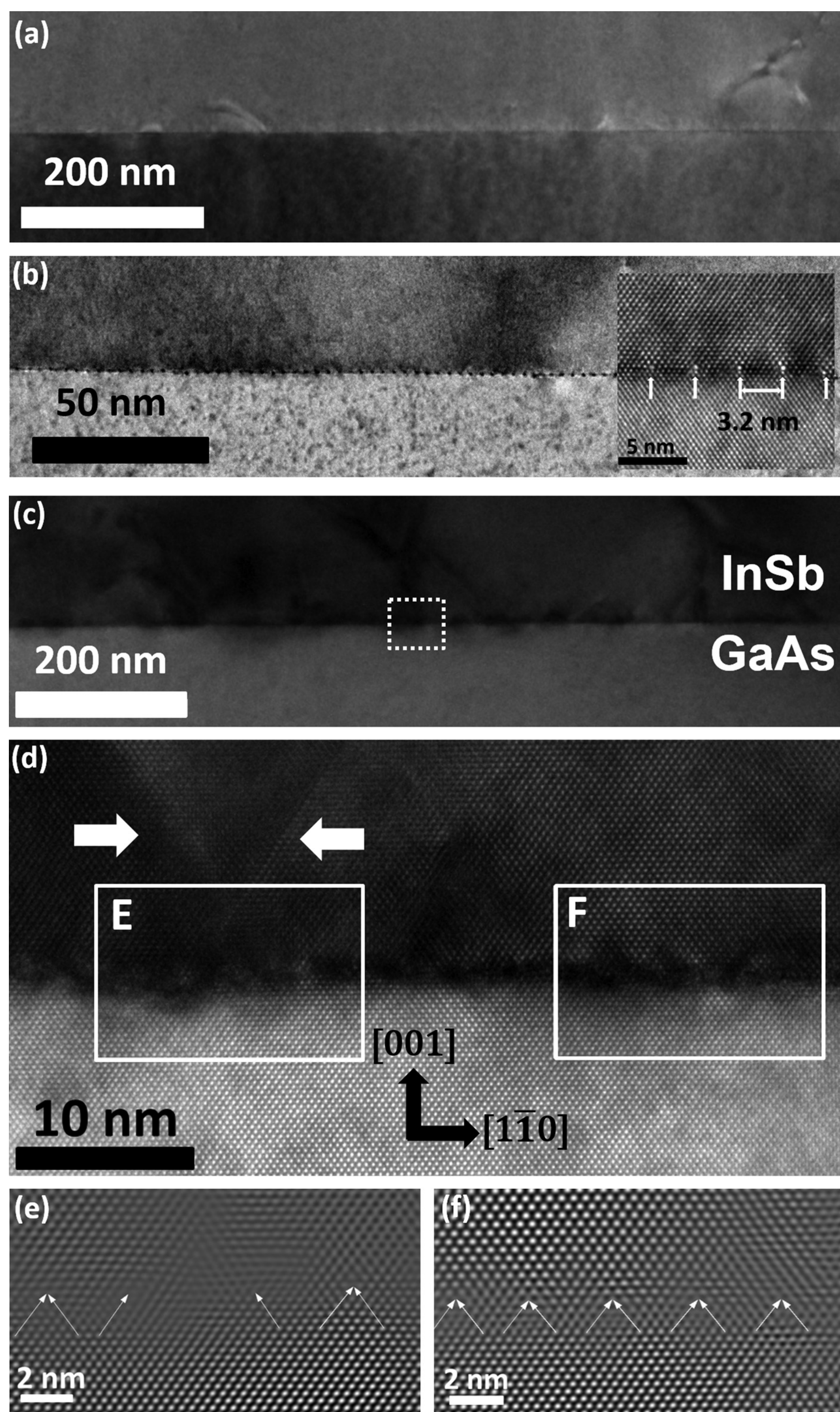

FIG. 2. Cross-sectional TEM images of InSb layer on GaAs (100) substrate grown at 350 °C and 310 °C. (a) Bright-filed image for sample grown at 310 °C; (b) bright-field image of highly periodic misfit dislocations array with high-resolution inset of interfacial dislocations at the InSb/GaAs interface; (c) bright-filed image for sample grown at 350 °C; (d) high resolution image along the [1$\bar{1}$0] zone axis for the sample grown at 350 °C; (e) and (f) phase contrast images of selected areas E and F in (d) by using Fourier mask filtering technique. At the InSb/GaAs interface, 60° misfit dislocations are indicated by one arrow and 90° misfit dislocations are indicated by a pair of arrows.

of the film, two threading dislocations (marked by white arrows) are observed. At the InSb/GaAs interface, there are a few arc-shaped features with different image contrasts. Figure 3(b) shows a high-resolution TEM image taken at the edge of an arc-shaped feature (indicated by the dotted box). In that area, one dislocation line, which is nucleated at the InSb/GaAs interface, is found. By applying a Fourier filter to the TEM image, the arrangements of the atoms in Areas C and D are presented in Figures 3(c) and 3(d). In Figure 3(c), three 90° misfit dislocations and one 60° misfit dislocation are observed. The separations for these dislocations are not uniform. From left to right, the space between two adjacent dislocations is 3.8 nm, 4.7 nm, and 2 nm, respectively. With a 60° misfit dislocation and wider distances between two adjacent dislocations, this IMF was not capable of fully relaxing the entire lattice strain, and thus, the formation of threading dislocations to relax the remaining strain was promoted. In contrast to the dislocations in Figure 3(c), uniformly distributed 90° misfit dislocations with a separation of 3.2 nm, which are capable of relieving the entire lattice strain, are

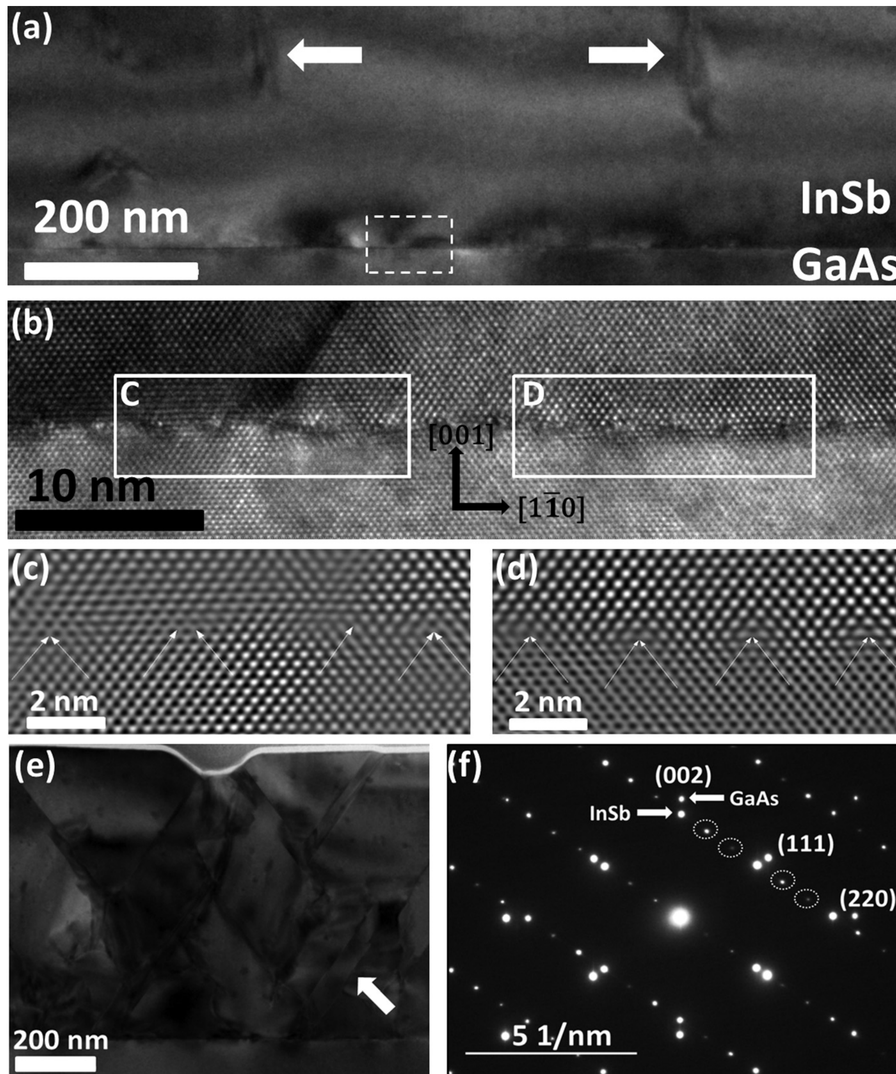

FIG. 3. (a) Bright-filed TEM image for InSb on GaAs grown at 270 °C. A box indicates the area shown in (b); (b) high resolution image along the [1$\bar{1}$0] zone axis for InSb on GaAs grown at 270 °C; (c) and (d) phase contrast images of selected area C and D in (b) by using Fourier mask filtering technique. At the InSb/GaAs interface, 60° misfit dislocations are indicated by one arrow and 90° misfit dislocations are indicated by a pair of arrows; (e) bright-field image for sample grown at 220 °C indicates one of the microtwins in the InSb layer; (f) selected area electron diffraction (SAED) pattern taken from the sample grown at 210 °C. Spots belong to InSb and GaAs have been marked by white arrows. White dotted circles mark extra diffraction spots caused by microtwins in InSb layer.

observed in Area D as shown in Figure 3(d). No threading dislocations are observed in that area.

Figure 3(e) contains a bright-field cross-sectional TEM image taken from Sample 4. In contrast to Figures 2(a), 2(b), and 3(a) obtained from Samples 1, 2, and 3, respectively, various defects were observed in this TEM image obtained from Sample 4. In addition to the threading dislocations, a microtwin defect is observed in the heteroepitaxial InSb layer, which is marked by a white arrow in Figure 3(e). In Figure 3(f), a selected area electron diffraction (SAED) taken at the InSb/GaAs interface of Sample 4 illustrates two sets of separate diffraction spots, which are associated with two different lattice constants from InSb and GaAs, respectively. The SAED also shows additional microtwin spots (circled by a white dotted line). These spots confirm the presence of microtwin defects, which have different crystal orientations than the remaining InSb layer and could be the cause of the formation of craters at the surface of the epilayer (craters are observed in TEM image, Figure 4(e), and in AFM image, Figure 1(d)). In a strongly mismatched heteroepitaxy, the formation of microtwin defects is normally linked to the introduction of a stacking fault during the island growth phase.[26]

This study reveals the influence of growth temperature on the IMF formation in the heteroepitaxy of InSb on GaAs.

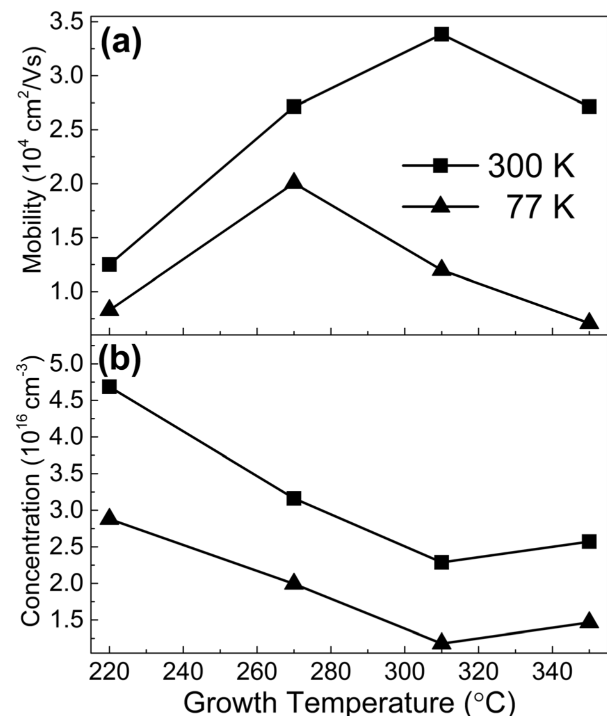

FIG. 4. Dependence of (a) charge carrier mobility and (b) charge carrier concentration on growth temperature for InSb on GaAS (100) at 300 K and 77 K.

A growth temperature of 310 °C (Sample 2) resulted in the lowest observed TDD in the epilayer, as suggested by the trend from TEM observation in conjunction with the FWHM of the XRD rocking curve. In Samples 1 and 3, 60° dislocations and a shorter distance between two adjacent dislocations disrupt the uniformly distributed 90° IMF array. The existence of 60° misfit dislocations is commonly associated with the formation of threading dislocations in an antimonide compound semiconductor on GaAs.[27]

A previous TEM study revealed that 90° dislocations start to nucleate at the interface during the phase of island growth.[28] Each island has its own 90° dislocation network. When two islands coalesce, their dislocation networks can merge to form a larger network. Usually, a small shift between two networks can be accommodated by an elastic deformation. However, in the case of coalescence between two islands, where the shift between two networks is roughly half of the dislocation separation (S), a 60° dislocation will be formed.[29] Although a quantitative relationship between the density of islands and TDD is difficult to establish, a higher InSb island density can be qualitatively associated with a higher rate of island coalescence, and thus, leads to a higher TDD. A study on the heteroepitaxy of GaSb on GaAs revealed that GaSb grown at a low temperature exhibited higher island nucleation site density compared to GaSb grown at a high temperature.[30] Thus, the higher TDD in Sample 3 could be due to the higher island coalescence, as Sample 3 was grown at a temperature lower than the growth temperature of Sample 2.

The island coalescence mechanism does not explain the high TDD found in Sample 1 which was grown at a higher temperature than Sample 2. Huang *et al.* showed that a Ga-rich GaAs surface before Sb supply is essential to form a uniform 90° interfacial misfit dislocation array. In their report, using contrast test, one 5 μm GaSb epilayer was grown on a Ga-rich GaAs surface and the other 5 μm GaSb epilayer was grown on the As-terminated GaAs surface. Plan-view TEM revealed the threading dislocations densities for the sample grown on the Ga-rich GaAs of about 5×10^5 cm^{-2}, and for the sample grown on the As-terminated GaAs of about 10^9 cm^{-2}.[23] A theoretical calculation[13] predicted that Ga-Sb bonds, which resulted from the deposition of a monolayer of Sb atoms on the Ga-rich GaAs surface, are stretched and bent due to a different covalent radius between the Sb and As atom. The stretching and bending of these Ga-Sb bonds result in lattice strain. The formation of periodic IMF array is driven by the minimization process of this strain.[13] The existence of Ga-As bonds changes the distribution of strain and obstructs the formation of 90° misfit dislocations.

In this study, the formation of Ga-Sb bonds was done not through deposition of Sb on Ga-rich surface but through the As-for-Sb anion exchange process at the GaAs surface. This As-for-Sb anion exchange process can be expressed as

$$\mathrm{GaAs(s)} + \frac{1}{2}\mathrm{Sb_2(g)} \rightleftharpoons \mathrm{GaSb(s)} + \frac{1}{2}\mathrm{As_2(g)}. \quad (2)$$

The change of enthalpy for this reaction is 47.6 kJ/mol at 350 °C, which yields an equilibrium constant of 0.138.[31] Under a Sb flux with a BEP of 1.2×10^{-6} Torr, less than 5% As on the GaAs surface can be replaced by Sb atoms. This indicates an inefficient As-for-Sb anion exchange process, which may lead to residual Ga-As bonds at the surface. However, the situation differs for low substrate temperatures. Arsenic released from the substrate forms arsenic tetrameric (As_4) on the surface of the substrate when the substrate temperature is below 350 °C.[32] The As-for-Sb exchange reaction with As_4 has an equilibrium constant of up to 148.[32] Under the same Sb flux (BEP of 1.2×10^{-6} Torr), the As-for-Sb conversion is nearly 100% on the GaAs surface, which indicates that As atoms can be replaced efficiently by Sb atoms. Complete As-for-Sb anion exchange on As-terminated GaAs surface has the same effect as depositing As on Ga-rich GaAs surface as mentioned in the introduction. Strain caused by Ga-Sb bonds stretching and bending plays an important role on the formation of uniform IMF array, while Ga-As bonds are unable to result in lattice strain because the substrate is GaAs which impedes IMF array's formation. The higher substrate temperature during the Sb absorption step in Sample 1 (350 °C) resulted in an inefficient As-for-Sb anion exchange process, which did not occur on the other three samples grown at 310 °C or lower. The higher growth temperature in Sample 4 has led to a higher density of Ga-As bonds on the surface and suppressed the formation of a periodic IMF array in the InSb layer.

Threading dislocations can influence charge carrier mobility in semiconductors, especially for heteroepitaxy. Based on the model proposed by Dexter *et al.*, the mobility of charge carrier is suppressed by 90° dislocations and is inversely proportional to the density of dislocations.[33] In GaN/sapphire heterogeneous structures with lattice mismatch >12%, the mobility in an undoped GaN epilayer depends on dislocation density, and the dislocations act as acceptor-like traps.[34] For InSb grown on GaAs, a strong relationship between threading dislocations and charge carrier mobility was reported.[5] Using different buffer layers, 600 nm thick InSb epilayers with different threading dislocation densities were grown on the GaAs substrate. The highest charge carrier mobility was achieved in the sample with lowest threading dislocation density. Sato *et al.* prepared InSb layers with a different thickness on the GaAs substrates and found that charge carrier mobility in the InSb layer was limited by threading dislocations.[35] This limitation is prominent for InSb epilayer thickness below 1 μm.[36]

In this study, although most of the threading dislocations can be avoided by forming IMF array, high density 90° misfit dislocations still existed on InSb/GaAs interface as shown in TEM images. Their influence on the charge carrier mobility in InSb layer was investigated by Hall resistance measurement. Figures 4(a) and 4(b) illustrate the growth temperature-dependent charge carrier mobility and charge carrier concentration for an unintentional doped InSb grown on GaAs measured at 300 K and 77 K. The detailed charge carrier concentrations are listed on Table I. The influence of GaAs substrate can be negligible because the substrate is a semi-insulator with a resistivity of 10^7 Ωcm.

All samples exhibited unintentional n-type doping. At 300 K, the highest charge carrier mobility value was

observed in Sample 2. This is consistent with XRD and TEM results. However, all samples exhibited decreasing mobility as the temperature is lowered. Furthermore, this decrease of charge carrier mobility with the decrease of temperature from 300 K to 77 K is unusual. Typically, higher charge carrier mobility at low temperature measurement is expected due to suppression of phonon scattering at low temperature and this behavior is consistently reported in bulk InSb.[37] A reduced charge carrier mobility was reported[38] in the n-type bulk InSb, which was measured at very low temperature (20 K–80 K). The charge carrier mobility increased with an increasing measurement temperature and reached the maximum mobility value around 60 K. This phenomenon was attributed to the scattering of ionized impurity.[39] Below 80 K, the effect of phonon scattering on charge carrier mobility was very weak and can be ignored. In this low temperature conditions, the charge carrier mobility was significant limited by the Coulomb interaction between the ionized impurities and charge carriers. At higher measurement temperature, the increasing thermal velocities of charge carriers weaken the influence of ionized impurities, and the value of charge carrier mobility was increased in proportion to $T^{3/2}$, where T was the temperature based on Brooks–Herring formula.[40] However, it should be noted that the influence of ionized impurities on the charge carriers mobility in the n-type bulk InSb material was only significant in the <80 K measurements. Charge carrier mobility in the n-type InSb bulk decreased with an increasing measurement temperature from 60 K to 600 K, due to effect of phonon scattering.[37] Therefore, the effect of ionized impurities could not explain the reduced charge carrier mobility observed in InSb epilayers on GaAs measured at 77 K. Another possible explanation is related to the effect of dislocations in InSb epilayers. Lower charge carrier mobility at 77 K has been reported in some InSb/GaAs heteroepitaxy grown below 2 μm thick.[41,42] Although the mechanism of this deviation is still not fully understood, the reports attributed it to the influence of dislocations in InSb layer. For all samples, the charge carrier concentration at 300 K was higher than $2 \times 10^{16}\,\mathrm{cm}^{-3}$, which is the intrinsic charge carrier concentration of InSb at 300 K.[43] Moreover, all samples showed charge carrier concentrations between 1×10^{16} and $3 \times 10^{16}\,\mathrm{cm}^{-3}$ at 77 K, which is at least two orders of magnitude higher than the intrinsic charge carrier concentration of InSb ($\sim 10^{14}\,\mathrm{cm}^{-3}$).[43] The charge carrier concentration also depends on threading dislocation density in the InSb layer. Moreover, a higher dislocation density, as suggested by the XRD FWHM, seems to result in a higher charge carrier concentration. This phenomenon suggests the presence of extrinsic charge carriers in the unintentional doped InSb layer at both 300 K and 77 K, and these extrinsic charge carriers may be related to defects (threading dislocations and microtwins) in epilayers. Background unintentional doping concentration of MBE system used in this was in the range of $10^{14}\,\mathrm{cm}^{-3}$, and these extrinsic charge carriers observed in the samples are above $10^{16}\,\mathrm{cm}^{-3}$. Therefore, background unintentional doping makes little contribution to extrinsic carries in InSb layer.

Because interfacial misfit dislocation arrays and threading dislocations are in the region close to InSb/GaAs interface, this region is named "dislocation region" in this study. Although the accurate thickness and clear boundary of this region are difficult to be extracted from the available experimental data, TEM images in Figures 2 and 3 clearly show high density dislocations exist near the interface, and the previous research demonstrated that the dislocation density decreased rapidly with increasing thickness in heteroepitaxy.[44] Beside dislocations, microtwins are also found in sample 4, and the influence of microtwins on the charge carrier mobility is similar to the influence of dislocation.[45] In the dislocation region, most of the charge carriers are extrinsic and excited from dislocations.[41] These charge carriers are inevitably scattered by dislocations, leading to low charge carrier mobility. The region above the "dislocation region" where dislocations density is low is named as "bulk region" in this study. The charge carriers (electrons) in this region are intrinsic and directly excited from the valence band of the InSb. Due to the minimum of the dislocation-induced scattering, the charge carrier mobility in this region is relatively higher compared to that in the dislocation region.

At 300 K, charge carrier concentration in each sample is slightly higher compared to the intrinsic charge carrier concentration of bulk InSb material. A small fraction of charge carriers could be extrinsic charge carriers located in the dislocation region, while most charge carriers were intrinsic charge carriers located in the bulk region. At 77 K, charge carrier concentrations in samples were at least two orders higher than the intrinsic charge carrier concentration of InSb at 77 K, which indicated the dominance of extrinsic for electric current and, thus, most of the conductance originating from the dislocation region. Therefore, the anomalous decrease in charge carrier mobility at 77 K could be attributed to the presence of the dislocation region and different conduction paths of carriers at different temperatures.

The extent of decrease in charge carrier mobility from 300 K to 77 K varied between different samples as shown in Figure 4(a). It can be seen that the extent of decrease in charge carrier mobility of samples 3 and 4 is much smaller compared to that of samples 1 and 2. A similar observation was reported for undoped and Sn-doped InSb layers grown on the GaAs substrate.[41] While the undoped InSb layer showed a large decrease in charge carrier mobility in the 77 K Hall resistance measurement, the Sn doped InSb showed only a small decrease value in charge carrier mobility in the low temperature Hall resistance measurement. In Sn doped InSb, extrinsic charge carriers exist in both bulk region and dislocation region due to the donor impurity of Sn.[41] At low temperature, extrinsic charge carriers were not confined in the dislocation region and can be found in the bulk region as well, resulting in higher charge carrier mobility compared to low temperature charge carrier mobility in the undoped InSb layer on the GaAs substrate.

In this study, samples 3 and 4 were grown at lower temperatures compared to the optimal growth temperature of InSb. The optimal growth temperature of InSb is above 300 °C,[46] and samples 3 and 4 were grown at 270 °C and 220 °C. When compound semiconductors were grown below their optimal growth temperature, native point defects (anti-site, vacancy, and interstitial defects) were known to

occur readily.[47] Höglund *et al.* calculated that these defects act as n-type donors in an InSb epilayer using density-functional theory.[48] Due to the low growth temperature of samples 3 and 4, it is possible that native point defects contributed to the extrinsic charge carrier in the InSb layer of both samples. At 77 K, these defect-generated extrinsic charge carriers were responsible for the charge carrier transport in the bulk region, leading to the smaller decrease in charge carrier mobility of samples 3 and 4 compared to that of samples 1 and 2, where electric current at low temperatures occurred primarily through the dislocation region.

IV. CONCLUSIONS

We systematically investigated the growth temperature dependence of the formation of IMF dislocations array in the highly mismatched InSb/GaAs heteroepitaxy system. In this work, the formation of Ga-Sb bonds, which is an essential step to form a uniform IMF array, was achieved through an As-for-Sb anion exchange process. The sample grown at 310 °C (Sample 2) exhibited the lowest surface roughness, smallest FWHM in the rocking curve, a uniformly distributed IMF array, and the lowest threading dislocation density. Higher and lower growth temperatures introduced 60° misfit dislocations interrupting the uniformity of the IMF array resulting in the development of threading dislocations. The possible origins of these 60° misfit dislocations have also been analyzed. The samples showed higher charge carrier mobility at 300 K than at 77 K. This observation was explained by the presence of "dislocation region" and "bulk region" in the InSb layer. The "dislocation region" is defined as the region where the charge carrier transport is dominated by the misfit dislocation-induced charge carrier scattering.

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