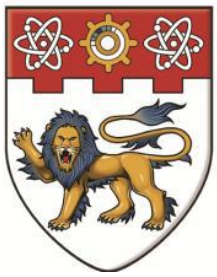

NANYANG TECHNOLOGICAL UNIVERSITY

DESIGN OF HIGH SPEED HIGH RESOLUTION ADC WITH INNOVATIVE ARCHITECTURE AND CIRCUITS

QIU LEI

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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SUMMARY

Nowadays, the demand for high performance Analog-to-Digital Converter (ADC) is growing rapidly. The high-speed high-resolution ADCs play important role in many systems, such as wireless base station, software-defined-radio (SDR), test system, etc. Due to the development of process technology, low power and high performance ADC design becomes more attractive. Therefore, there is continuous interest in designing the high-speed high-resolution and low power ADCs.

The mismatches between channels in multi-channel architecture degrade the linearity of overall ADC systems. In this research work, the mismatches calibration for two kinds of multi-channel ADCs, time-interleaved ADCs (TI-ADCs) and frequency-interleaved ADCs (FI-ADCs), are proposed. The time skew estimation technique adopts the correlation between channels, which indicates the value of time skew. And the time skew correction techniques are divided into two categories: analog trimming and digital compensation. In addition, the analysis of frequency-interleaved ADCs is addressed. An efficient calibration method for frequency-interleaved ADCs is proposed to compensate the analog analysis filter mismatches and gain mismatches, which could promote the FI-ADCs as a competitive multi-channel ADC alternative to TI-ADCs.

It is known that SAR ADCs are more energy efficient than pipeline ADCs. However, the typical structure of SAR ADC is difficult to operate at high speed (>250MHz). To increase the sampling rate of single channel SAR ADC. A 10-bit 300MS/s SAR ADC with interpolated 2b/cycle architecture is proposed. By using the asynchronous timing, less time is needed for the conversion cycles. In addition, the conventional shift register based successive approximation algorithm has been optimized, which reduces the settling time for the DAC array. A background offset calibration technique is presented

to eliminate of effect of the offsets between comparators. The ADC chip was fabricated in a 40nm CMOS low power technology. The measurement results show that the ADC achieves a SNDR of 51.5dB and with a figure of merit (FoM) of 58fJ/conversion-step when operating at 300MS/s and 147MHz Nyquist input. The ADC core achieves a small area of 0.032mm^2.

Time-interleaving is a popular approach to extend ADC speed. A 10-bit 1GS/s 4-way time-interleaved (TI) SAR ADC is presented. Each channel exploits a 250MS/s SAR ADC with high speed non-binary searching approximation that allows the conversion to obtain settling error tolerance. The non-binary DAC associated with adders based encoding circuit are custom designed, which eliminates multiplier based encoding logic and thus, simplifies the digital circuitry and reduces the digital power. To suppress the time skew among the TI SAR ADC, the sampling instant of the sub-ADC channels are synchronized to the full rate master clock, which reduces the time skew spurs below -52 dB at Nyquist input. Moreover, a digital background low computational time skew calibration technique with interpolation FIR filters is proposed, which further suppresses the timing mismatch spurs to be less than -70dB. The prototype was fabricated in a 65nm CMOS technology. The measurement results show that the ADC achieves a SNDR of 49.6dB and with a figure of merit (FoM) of 37fJ/conversion-step when operating at 1GS/s and 458.1MHz Nyquist input. The ADC core achieves a small area of 0.03mm^2.

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Chapter 1. INTRODUCTION

In this Chapter, a brief introduction of the high performance analog-to-digital converter ADC implementations is provided to show the emerging demands of high-speed high-resolution ADCs in section 1.1. Here, high-speed high-resolution means that the ADCs with sampling rate larger than 100MS/s and resolution larger than 8 bits are addressed in this thesis. As the data capacity of communication requirement significantly increases in the past decades, the implementations of high-speed and high-resolution ADCs trend to grow up dramatically. For the wireless communication such as 3G/4G base stations, software-defined radio, the bandwidth and dynamic range are required to higher level. Also, the bandwidth of optical network faces an explosive growth, due to the coming of big data time. To valid or debug the new electronic system with higher bandwidth, the real-time oscilloscope also is driven to higher bandwidth design range.

Then the research motivation and major contribution of this thesis is introduced in Section 1.2 and Section 1.3 respectively.

1.1 Background

In this section, the implementation of the high-speed high-resolution ADCs is introduced.

1.1.1 Software defined radio

A software defined radio (SDR) system is a kind of radio system that combines the analog front end and post digital processor, allowing the reconfiguration of wireless communication protocols [1]. As the developments of advanced technologies and devices, the SDR faces a rebirth. The main component that enables SDR is in the analog domain of high-speed high-resolution data converter. In a software defined radio

receiver, the ADC is used to digitize the analog signal as close to the antenna as possible. The system diagram is shown in Figure 1.1. After the digitization, the signals are filtered, demodulated, and separated into individual channels in digital domain.

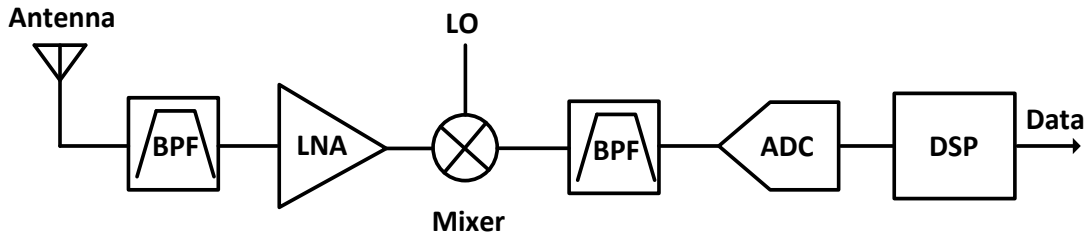


Figure 1.1 Software defined radio receiver.

The high speed high resolution ADC plays an important role in an SDR system. In general, the sampling rate and the resolution determine the bandwidth and dynamic range of the SDR system, respectively. If the bandwidth required for communication is large, it most likely involves strong interfering signals in the spectrum of interest. For instance, for a 200MHz bandwidth system with 50dB dynamic range, a 10-bit ADC with 500MS/s could satisfy the system requirements.

The bandwidth to be converted in SDR systems could be divided into different Nyquist zones. The most common one is the first Nyquist zone, which is from DC to half of the sampling rate. Also, for some high intermediate frequency (IF) systems, the ADC operates in higher Nyquist zones, where the ADC works as a mixer and digitizer. The requirement on SFDR and SNR are challenging.

1.1.2 Optical communication

Over the last two decades the capacity of optical communication has increased by more than three orders of magnitude [2]. And essentially, the trends continue to increase

to meet the future bandwidth demand. Today, a popular technical approach to boost the communication capacity adopts the coherent technique, in which the signal carrier and local oscillator are coherently mixed. The technique along with digital signal processing implemented in CMOS technology features low-power and low-cost solutions. Nowadays, the optical communication systems employing coherent receivers with channel capacity of 40Gbps are widely deployed.

To design a 100Gbps optical network with maximum communication distance and immunity to non-ideal factors of fiber, the dual-polarization quadrature phase-shift keying (DP-QPSK) is employed as a modulation method, which means the coherent receiver is needed. The most challenged design part is the low-power high-speed ADC. Without low power ADCs, it is extremely difficult to realize a 100G coherent receiver for optical network.

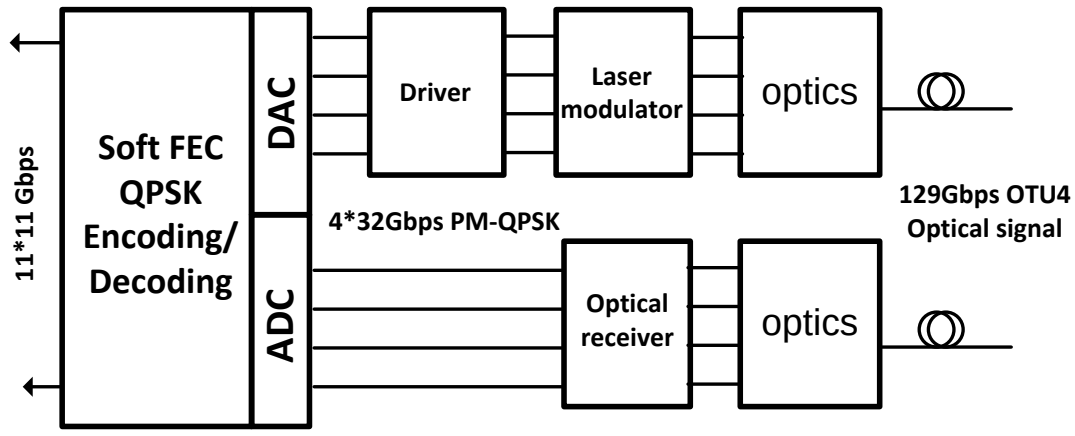


Figure 1.2 System with DAC-based transceiver IC.

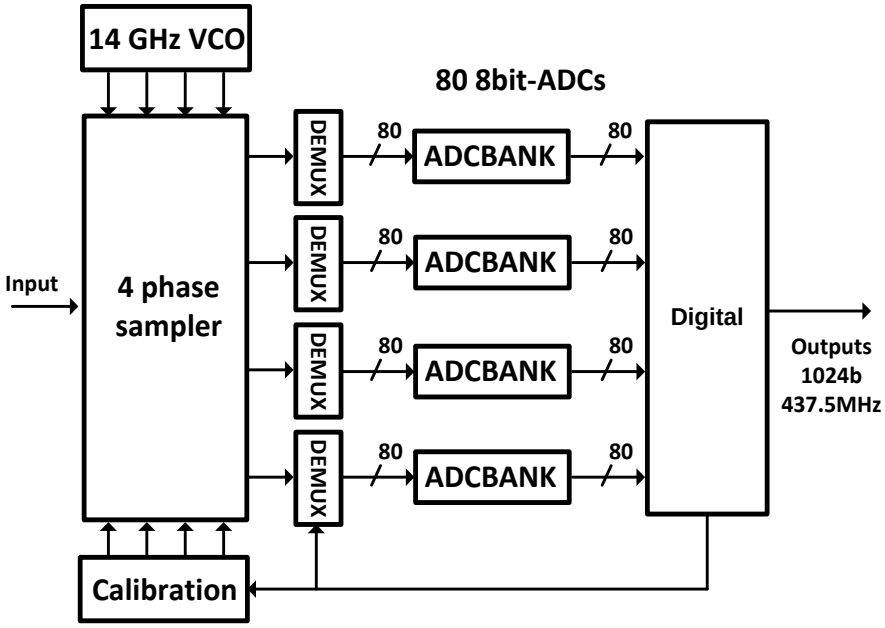


Figure 1.3 Block diagram for a 56GS/s ADC.

Compared with conventional optical transceiver IC architecture, greater integration can be realized by interfacing high speed DAC and ADC to the DSP. The system diagram of a 100Gbps optical transceiver [3] is shown in Figure 1.2. It can be seen that only optical devices and driver for transmission are required in analogue part. Among the optical transceiver, the four-channel 56GS/s 8-bit is designed as shown in Figure 1.3 [3]. Due to the power target, the power consumption of the whole ADC is limited to 10W or less. Therefore, low-power time-interleaved SAR ADC architecture instead of Flash ADC is adopted. As shown in Figure 1.3, in each channel ADC bank there are 80 175MS/s SAR ADCs. In addition, SAR ADCs also scale well with advanced CMOS technologies (e.g. 65nm, 40nm, 28nm), since most of the building blocks are digital.

1.1.3 High bandwidth oscilloscope

Over the past decade, data communication rates have increased by a factor over 10X. The requirement of data rates that was 1Gb/s and below is now up to 10Gb/s. Therefore,

the high bandwidth oscilloscopes used for validation, certification, and debugging are highly demanded. For example, the designers have extended the bandwidth of high performance oscilloscope up to the 60GHz-70GHz range and beyond.

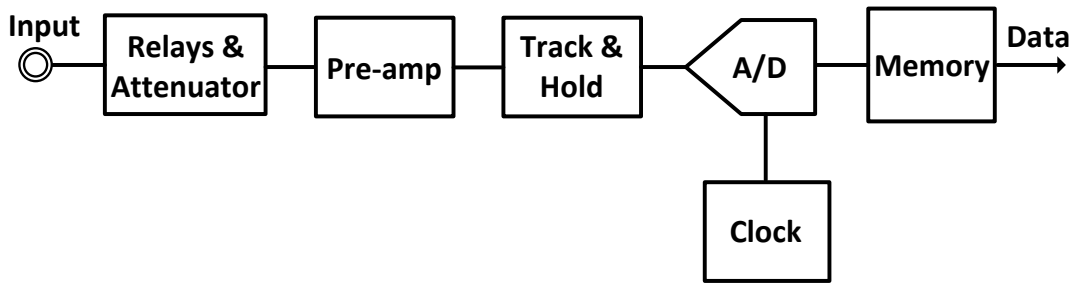


Figure 1.4 Block diagram of digital oscilloscope.

For the conventional architecture of digital oscilloscope as shown in Figure 1.4, it usually includes an analog front-end, analog-to-digital converter, memory and digital signal processing (DSP) included [4]. The analog front-end consists of a preamp or attenuation for signal conditioning, a track-and-hold to obtain the amplitude of signal periodically. The following A/D block digitizes the sampled signal amplitude. If the analog front-end can support the full bandwidth of the input signal, then the sampling rate of the ADC becomes the primary constraint of system bandwidth. According to Nyquist sampling rule, the input signal bandwidth should be less than half sampling rate. For example, a 5GHz input bandwidth will require a sampling rate greater than 10GHz.

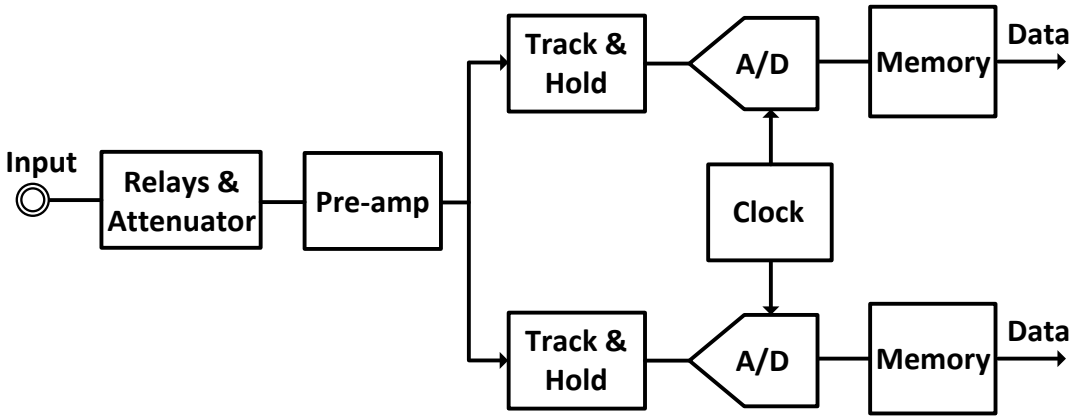


Figure 1.5 Block diagram of time-interleaved sampling architecture of digital oscilloscope.

Once the bandwidth requirements extend beyond the sampling rate limitation of the existed ADCs, time interleaving is a popular technique to extend the system sampling rate. In this way, the architecture of oscilloscope adopting the time-interleaved technique is shown in Figure 1.5. The analog front-end is designed to pass the entire bandwidth of interest. And the following two ADCs sample in parallel with 180 degree out of phase. The sampled data are demultiplexed in digital back end. Theoretically, there is no limitation to how many ADCs can be interleaved, though it become difficult to control the sampling time of interleaved devices as the number of ADC increases. The time-interleaved technique has been used by nearly all the major oscilloscope manufactures to get bandwidth up into GHz range.

1.2 Research motivations

Although there has been dramatic research progress in the high-speed SAR ADCs and time-interleaved ADCs domain, some limitations are still to be solved to further push these emerging techniques for real clinical applications:

The first limitation of the existing high-speed SAR ADCs is that the sampling rate of single-channel 10-bit SAR ADC is limited to 100MS/s [5], due to the serial conversion

characteristic and accuracy requirement for each comparison. Hence, it is necessary to analysis and design multi-bit per cycle SAR ADC architecture and successive approximation algorithm with redundancy.

The second limitation is the digital time skew calibration scheme existed in time-interleaved ADCs. The reported works on time skew calibration suffer from long-tap FIR introduced cost and fixed coefficients, which cannot track the change of environment variations. Therefore, low-computational background digital time skew calibration is required. Also, another multi-channel architecture is studied to avoid time skew existed in time-interleaved ADCs.

1.3 Major contributions

To overcome these limitations, this thesis conducts a comprehensive analysis and design on three aspects: analysis and design of calibration techniques for time-interleaved ADCs and frequency-interleaved ADCs, design of 2b/cycle 10-bit SAR, design of 1GS/s 10-bit 4-channel time-interleaved SAR ADC:

Analysis and design of calibration techniques for time-interleaved ADCs and frequency-interleaved ADCs: In Chapter 3, two time skew calibration methods are proposed. The time skew estimation technique adopts the correlation between channels, which indicates the value of time skew. And the time skew correction techniques are divided into two categories: analog trimming and digital compensation. In addition, the analysis of frequency-interleaved ADCs is addressed. An efficient calibration method for frequency-interleaved ADCs is proposed to compensate the analog analysis filter mismatches and gain mismatches, which could promote the FI-ADCs as a competitive multi-channel ADC alternative to TI-ADCs.

Design of 2b/cycle 10-bit high speed SAR: In Chapter 4, a 10-bit high speed asynchronous 2b/cycle SAR ADC is proposed. The interpolation technique is employed to reduce the size of DAC array, relaxing the trade-off between input bandwidth and resolution. Therefore, the sampling rate could be boosted up to several MHz.

Design of 1GS/s 10-bit 4-channel time-interleaved SAR ADC: In chapter 5, a 10-bit 1GS/s 4-way time-interleaved (TI) SAR ADC is proposed. Each channel exploits a 250MS/s SAR ADC with high speed non-binary searching approximation that allows the conversion to obtain settling error tolerance. To suppress the time skew among the TI SAR ADC, the sampling instant of the sub-ADC channels are synchronized to the full rate master clock. Moreover, digital background time skew calibration technique is utilized, which further suppresses the timing mismatch spurs.

Chapter 2. HIGH-SPEED HIGH RESOLUTION ADCS

In this Chapter, several ADC architectures, which are potential candidates for high speed high resolution ADCs designs are presented and analyzed. Pipeline ADCs convert the sampled signals with pipelined low-resolution stages, which is quite suitable for high speed high resolution ADCs design. Unfortunately, the high performance amplifiers used to resample and amplify the residue signals could not scale well with advanced CMOS technology, which limits the implementation of pipelined ADCs. Also, the employment of amplifiers lowers the power-efficiency of pipeline ADCs. It is known that successive approximation register (SAR) ADCs have a higher power-efficiency. Since most of building blocks are digital-oriented, SAR ADCs could scale very well as the modern CMOS technology.

2.1 Single-channel high-speed high-resolution ADCs

In this section, single-channel high-speed high-resolution ADCs are introduced first. The operation and non-ideal factors in the design of pipeline ADCs are addressed. The architecture of SAR ADC is presented, along with the source of errors needed to be considered during the design process. To cancel or compensate the errors, numerous calibration techniques have been reported. In this section, some selected non-ideal factor calibration techniques are reviewed and discussed.

2.1.1 Pipeline ADCs

Pipeline ADCs are long proven candidates for high-speed high-resolution ADCs design. The principle of pipelined ADCs is that it uses a series of low resolution of flash ADCs stages to build a high resolution converter shown in Figure 2.1 [6]. Each stage in pipelined ADCs quantizes the input signal with low resolution and amplifies the residue

signal before passing to next stage. Finally, the output digital bits of each stage are combined to generate a high resolution digital output.

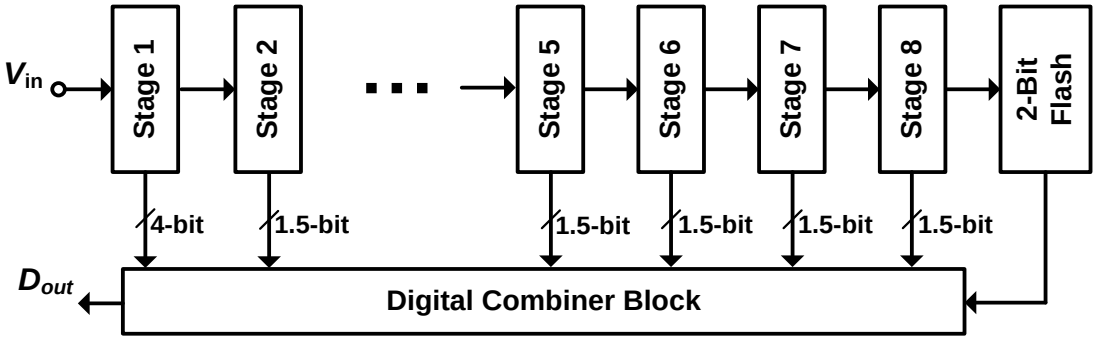


Figure 2.1 Architecture of pipeline ADCs.

2.1.1.1 Stage operation

A typical stage in pipelined ADC is shown in Figure 2.2 [7]. One notable feature of the stage architecture is the sub-ADC, which generates the approximation D_{out} for the stage, and the DAC block translates the D_{out} to the corresponding V_{ref}, which is subtracted by input signal. Then the residue voltage V_{res} is amplified by a factor of G to be processed by next stage. The transfer function of the stage is

$$V_{res} = G \cdot (V_{in} - D_{out} \cdot V_{ref}) \tag{2.1}$$

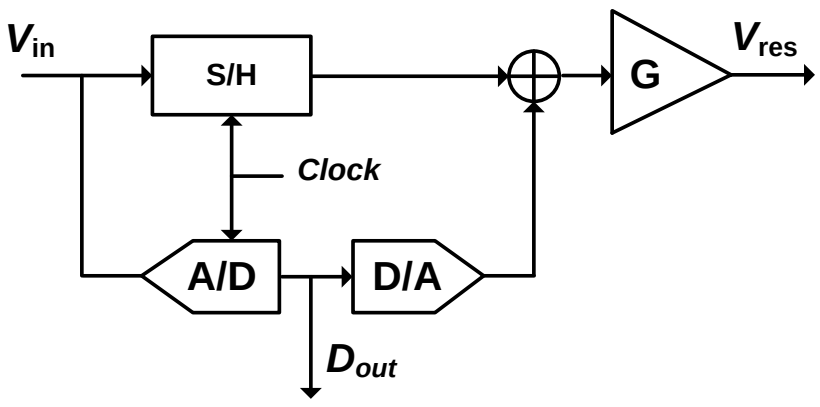


Figure 2.2 Block diagram of a typical stage in pipelined ADCs.

2.1.1.2 Source of errors

Each stage suffers from non-ideal errors that degrade the system performance. These errors [8] are 1) comparator offset error, 2) Op-amp offset and finite gain, 3) Capacitor mismatch and 4) Op-amp gain nonlinearity.

The comparator offset is caused by the threshold voltage mismatch and dimension mismatch of the input differential pair and differential output load in comparator. The mismatch in residue amplifier results in the op-amp offset and finite gain of op-amp that cause the gain error, change the stage gain and affect the system linearity. Due to the fabrication variation and imperfect layout, mismatch of capacitors occurs, which affects the stage gain and degrades ADC linearity. The nonlinearity gain of op-amp is also reflected in the stage gain, resulting linearity degradation.

2.1.1.3 Error Calibration

In order to overcome the errors and achieve the required performance, a number of calibration techniques have been published [9]-[11]. These calibration approaches are divided into two categories: foreground calibration [9] and background calibration [10], [11]. For the foreground calibration, it needs to interrupt the regular conversion of ADC, which is a drawback compared with background calibration. And it has been summarized in [10] that the approaches of the reported background calibration techniques can be categorized into mainly three types: statistics-based approach, correlation-based approach and equalization-based ones.

2.1.1.4 Source follower based residue amplifier

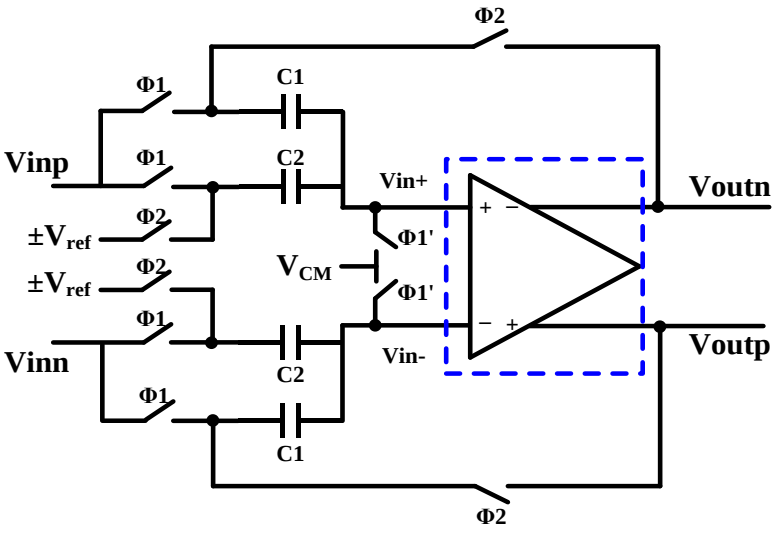
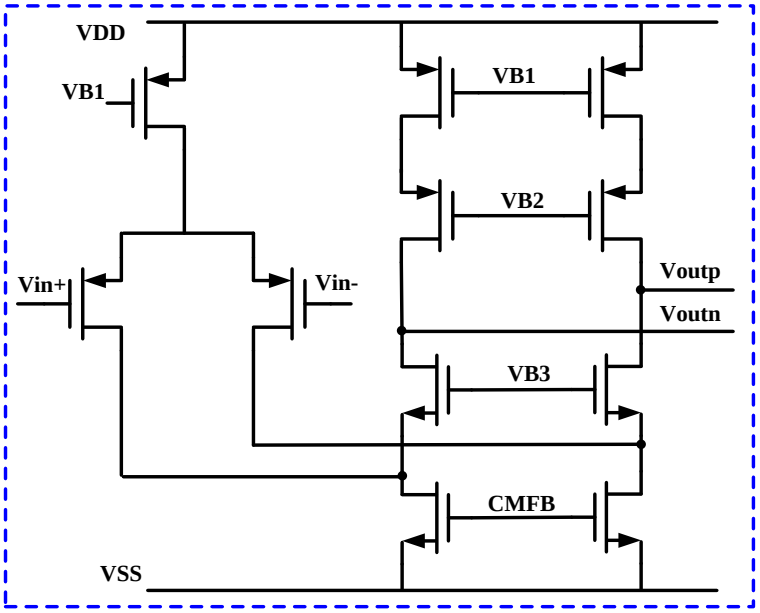
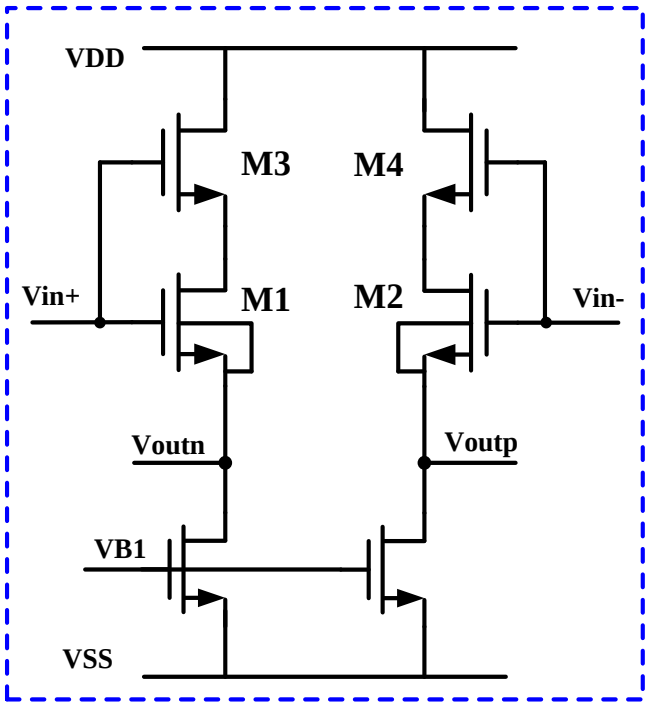


Figure 2.3 A residue amplifier in pipelined ADCs.



(a)



(b)

Figure 2.4 Two different amplifier cores for residue amplifier. (a) Conventional op-amp core. (b) Proposed source follower based core.

Pipeline architecture is suitable for high-speed high-resolution ADCs design. However, the power efficiency is limited when using conventional op-amp based residue amplifier [12] shown Figure 2.3, as the traditional op-amp, shown in Figure 2.4(a), is power hungry when targeting high bandwidth and high gain. Recently, several novel techniques have been developed to supersede the power hungry residue amplifiers. In [13], an open-loop amplifier is adopted to replace the op-amp, leading to low power consumption. And in [14], a dynamic source follower amplifier based pipelined ADC is presented, which achieves low power. Unfortunately, it is limited to run at low speed (<100MS/s) and without employing bottom plate sampling, the linearity of the ADC is

limited. Here, a source follower based SC amplifier, of which the V_{gs} of following transistor is nearly constant with given bias current, achieves 250MS/s and linearity of 65.9dB with consuming 1.4mW [15]. The structure of proposed source follower based SC amplifier is depicted in Figure 2.4(b). M1 and M2 are the pseudo differential input pairs, which work as source followers. M3 and M4 duplicate the input signal respectively to the drain of M1 and M2 to suppress channel-length modulation effect and the bulk of M1 and M2 are connected to their source for eliminating bulk effect, both effects of which can degrade the linearity of SC amplifier. To make M1-M4 work in saturation region, the $V_{in}+$ and $V_{in}-$ should be larger than $V_{th1,2}+V_{ov3,4}+V_{ov1,2}+V_{ov,bias}$. The proposed SC amplifier uses a two phase clocking scheme. During the sample phase Φ_1, both C_1 and C_2 are connected to input and the gate of M1 is connected to common mode voltage V_{CM}, which can be voltage supply V_{dd}. The output common mode voltage is V_{dd}-$V_{gs1,2}$. In the amplification phase Φ_2, the bottom plate of C_2 is connected to reference voltage V_{ref} ($V_{ref,cm}+V_{ref,diff}$) and the bottom plate of C_1 is connected to output. Hence, the transfer function of the SC amplifier can be derived according to charge conservation. The charge on the gate of M1 or M2 during the sample phase is:

$$Q_{\Phi 1} = (C_1 + C_2) \cdot (V_{CM} - V_{in,cm} - \frac{V_{in,diff}}{2}) . \tag{2.2}$$

For the amplification phase,

$$Q_{\Phi 2} = C_1 \cdot V_{gs1,2} + C_2 \cdot (V_{out} + V_{gs1,2} - V_{ref,cm} - V_{ref,diff}) + C_{gd3,4} \cdot (V_{out} + V_{gs1,2} - V_{dd}) \tag{2.3}$$

Since the charge is conserved, setting the equations (2.2) and (2.3) equal gives the output common mode

$$V_{\text{out,cm}} = \frac{(C_1 + C_2) \cdot (V_{CM} - V_{in,cm} - V_{gs1,2}) + C_2 \cdot V_{ref,cm} - C_{gd3,4} \cdot (V_{gs1,2} - V_{dd})}{C_2 + C_{gd3,4}} . \tag{2.4}$$

It can be seen in (2.4) that there is a common mode gain in the SC amplifier. Therefore, common mode feedback block is needed for further implementation in pipelined ADC. The differential output is

$$V_{out,diff} = \frac{C_1 + C_2}{C_2 + C_{gd3,4}} \cdot V_{in,diff} + \frac{C_2}{C_2 + C_{gd3,4}} \cdot V_{ref,diff} \,. \tag{2.5}$$

In the case of $C_{gd3,4} << C_{1,2}$, the gain of proposed SC amplifier is

$$G = \frac{V_{out,diff}}{V_{in,diff}} \approx \frac{C_1 + C_2}{C_2} \,. \tag{2.6}$$

Actually, a small variation of $V_{gs1,2}$ can be caused by different input voltage, which means $V_{gs1,2}$ is input signal dependent, leading to the nonlinearity of the SC amplifier. Assuming a variation of $\Delta V_{gs1,2}$ in $V_{gs1,2}$, the differential output is now

$$V_{out,diff} = \frac{C_1 + C_2}{C_2 + C_{gd3,4}} \cdot V_{in,diff} \pm \frac{C_2}{C_2 + C_{gd3,4}} \cdot (V_{ref+} - V_{ref-}) + \frac{C_1 + C_2 + C_{gd3,4}}{C_2 + C_{gd3,4}} \cdot \Delta V_{gs1,2} \,. \tag{2.7}$$

2.1.2 Successive approximation ADCs

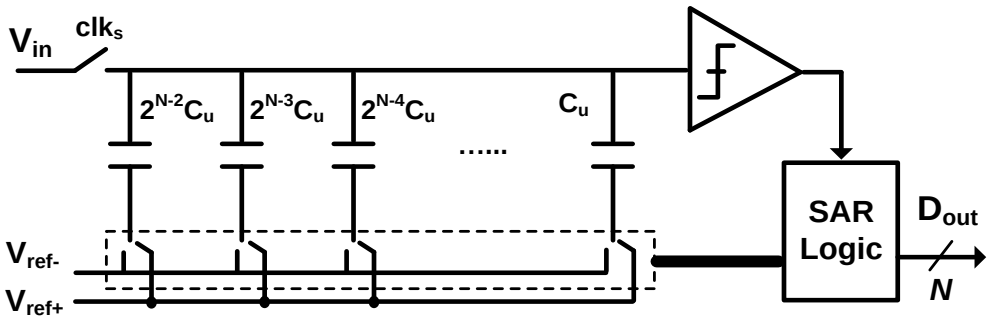


Figure 2.5 Block diagram of a typical SAR ADC.

The conventional structure of successive approximation register (SAR) ADCs is shown Figure 2.5. The operation procedure is as the following. Firstly, the input signal

is sampled on the whole DAC array. Then, the sampled signal is compared with $1/2V_{ref}$ by connecting the first capacitor to V_{ref} while the other capacitors connect to ground. And if the results of first comparison is positive, input signal compares with $3/4V_{ref}$, else the input signal compares with $1/4V_{ref}$. Same process continues until all the N bits are determined.

Since most of the blocks in SAR ADCs are dynamic circuits, the FOM value of SAR ADCs is usually smaller compared with other ADC architectures, which means that the SAR ADCs can achieve higher power efficiency [16].

2.1.2.1 High speed design considerations

Recent development of advanced CMOS technology has provided opportunities for SAR ADCs to operate at high frequency (>100MS/s). To design a SAR ADC with sampling rate in hundreds of MS/s range, the following approaches are considered:

1. To reduce the number of steps per conversion, multi-bit per step architecture is adopted.

2. Small customized capacitive DAC array, to increase the input bandwidth and DAC settling bandwidth.

3. Asynchronous timing, to shorten the total conversion time.

4. Redundant searching algorithm, to relax the settling time requirement of DAC array.

5. Delay improved control logic, to reduce the delay between output of comparator and DAC array.

6. High speed comparator design, to reduce the time of residue regeneration.

2.1.2.2 Error and calibration

Similar to pipelined ADCs, SAR ADCs also suffer from non-ideal errors that degrade the system performance. These errors are 1) Incomplete settling, 2) Comparator offset, 3) Capacitor mismatch and 4) Hysteresis in comparator.

For the issue caused by incomplete settling, the DAC array with redundancy [5] could solve this problem. And the approach in [17] is an effective background offset calibration scheme. Additionally, special attention must be paid on the layout of capacitor DAC array to reduce the system linearity degradation as much as possible. As an example, a well floor plan of the capacitor DAC array is presented in [18]. For the SAR ADC design with resolution larger than 12 bits, the mismatch calibration for capacitive DAC array is usually needed. As mentioned in [19], a per-turbation based digital calibration method could compensate the mismatch among the capacitive DAC, enabling it to downsize the DAC to save power and silicon area.

2.2 Time-interleaved high-speed high-resolution ADCs

In this section, a brief review of time-interleaved high-speed high-resolution ADCs is presented. Firstly, the mismatches in time-interleaved ADCs (TI-ADCs) is reviewed and analyzed. Then, the reported mismatches calibration methods are summarized and discussed.

2.2.1 Mismatches between channels

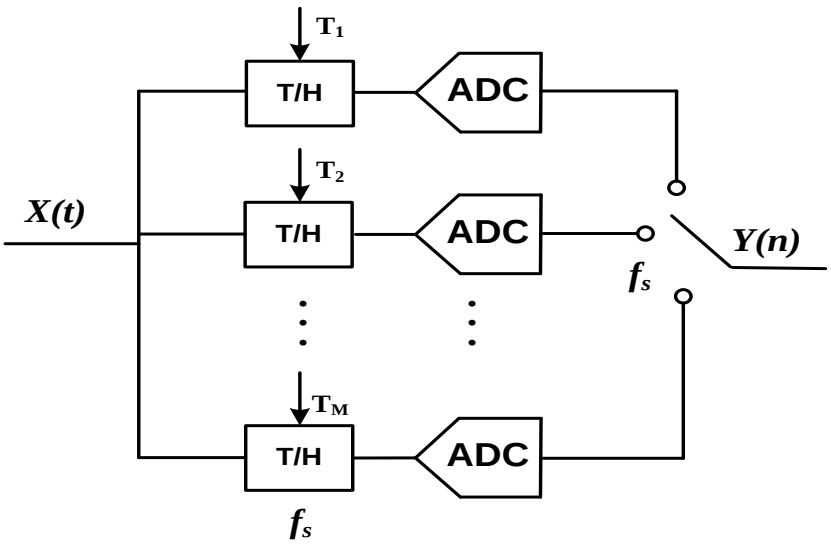


Figure 2.6 The structure of time-interleaved ADCs.

For the design of high-speed and high-resolution ADCs, multi-channel ADC structures are adopted in numerous implementations. TI-ADCs are the most frequently used multi-channel ADC structure. However, due to manufacturing variation, there are mismatches between the channels, such as offset mismatch, gain mismatch, time skew and bandwidth mismatch, which result in the performance degradation. Figure 2.6 presents the block diagram of *M*-channel TI-ADCs. The input signal is sampled by multi-phase clock with period T_s and multiplexed in digital domain with a digital clock with period T_s/M.

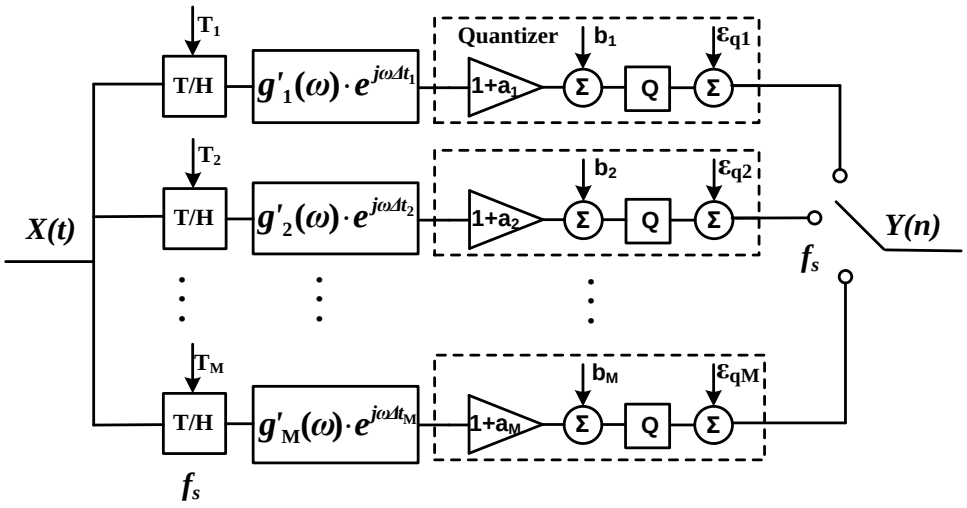


Figure 2.7 The structure of time-interleaved ADCs.

The model of *M*-channel TI-ADCs is shown in Figure 2.7, including quantization noise ε_{qm}, offset mismatch b_m, gain mismatch a_m, bandwidth mismatch $g'_m(\omega)$ and time skew Δt_m. Detailed discussion of mismatches can be found in [20], [21]. For normal priority of calibration, offset mismatch is compensated first. It is then followed sequentially by the gain mismatch, bandwidth mismatch calibration, and finally the time skew calibration. The bandwidth mismatch will affect the phase the signal, therefore, the bandwidth mismatch calibration is prior to time skew calibration.

2.2.2 Calibration for mismatches

Numerous publications are targeted to solve the time skew issue [22]-[25]. For the calibration techniques of time-interleaved ADCs, there are foreground and background calibration. Background calibration means that it does not interrupt normal ADC operation and can track environmental (e.g., temperature) and process aging. The background calibration can be categorized into mainly two types: Nyquist sampling frequency based and distributed clocking based approach.

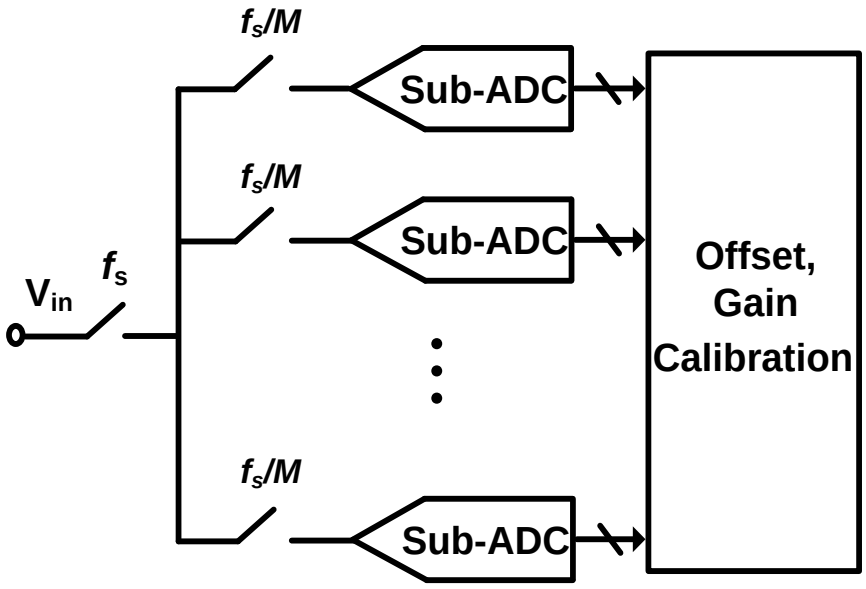


Figure 2.8 Time-interleaved ADCs with serial sampling switches to avoid time skew.

In Figure 2.8, a switch at Nyquist sampling rate is placed in front of all sub-channels to avoid the effect of the time skew error in sub-channel sampling switches [22]. In this technique, non-overlap sub-sampling clock signals are required to alleviate input load. Also, certain time margin is required to ensure the settling after master sampling switch turning off, which may limit this technique applied in ultra-high-speed TI-ADCs. In Figure 2.9, an alternative Nyquist sampling frequency based time skew cancellation technique is depicted [26]. The differential Nyquist rate clock signal is feed into each sub-channel. The potential issue is the threshold voltage mismatch of sampling transistors in sampling circuit may introduce significant time skew error.

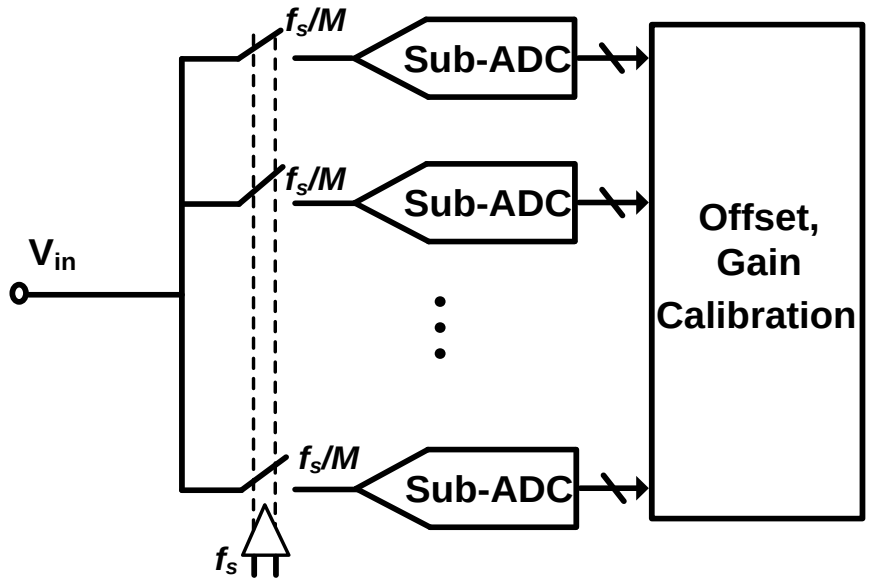


Figure 2.9 Time-interleaved ADCs with full rate sampling clock embedded into each channel.

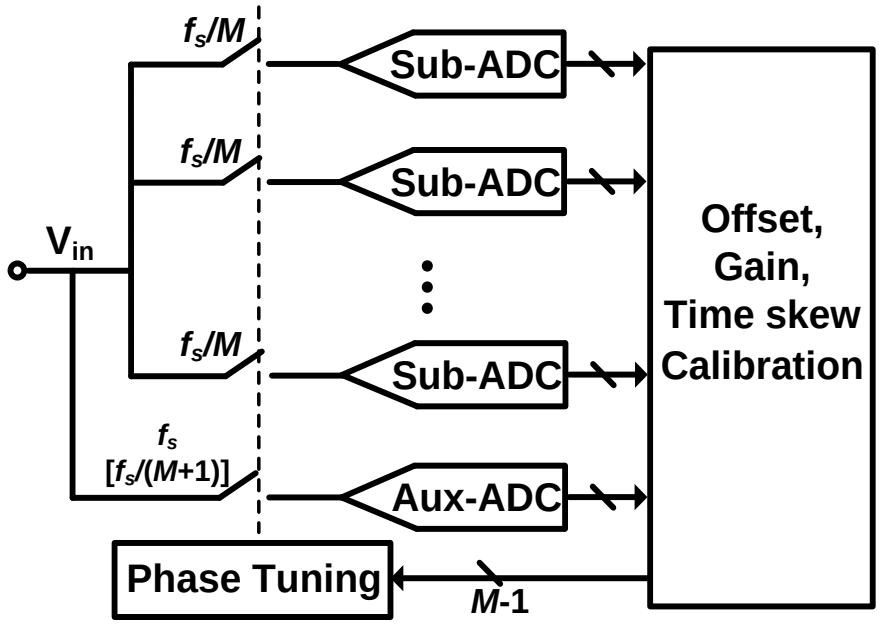


Figure 2.10 Time-interleaved ADCs with an auxiliary ADC branch to adjust the time skew.

An auxiliary ADC, which is the reference channel for all sub-channels, is needed for the time skew cancellation in Figure 2.10. In digital domain, the time skew can be extracted

from the correlation between sub-channels and the auxiliary-channel [27], [28]. In [28], the reference channel works at Nyquist sampling rate. While frequency of $f_s/(M+1)$, where f_s is the overall sampling rate and M is the number of channels, is selected as the reference frequency in [27].

Without the Nyquist rate sampling switch, the time skew existed in sub-sampling clocks can be calibrated as shown in Figure 2.11. By replicating the sampling switches of each sub-channel and sampling a known signal with the replicated sampling switches [24], the time skew could be estimated by analyzing the sampled digitized signal [30]. However, to achieve the expected time skew cancellation, the threshold mismatch

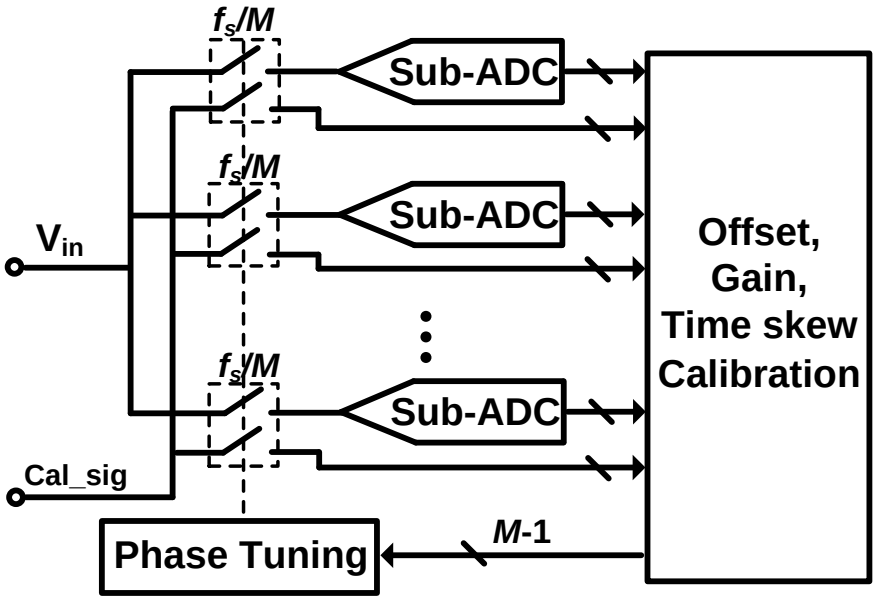


Figure 2.11 Time-interleaved ADCs with an auxiliary ADC branch to adjust the time skew.

sub-channel sampling switch and its replication must be considered, which potentially induces additional time error.

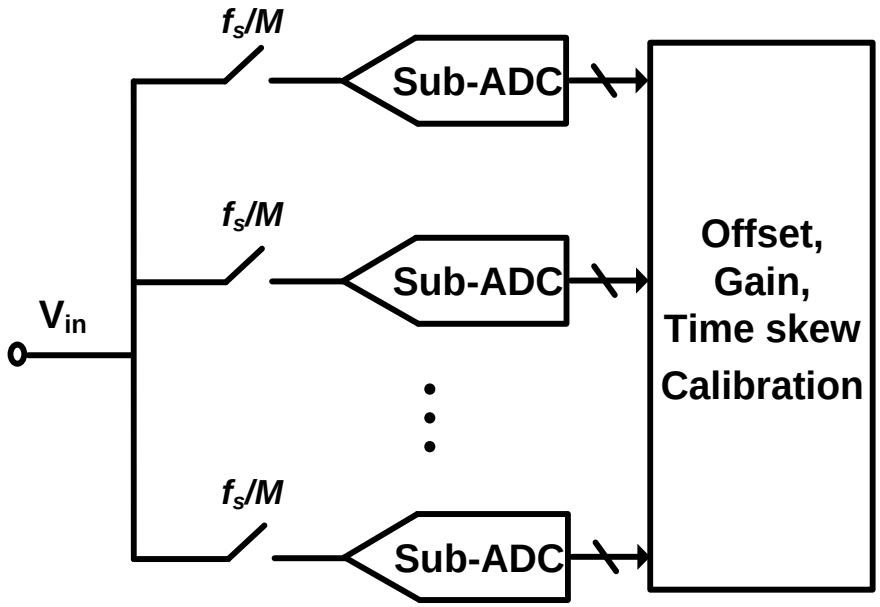


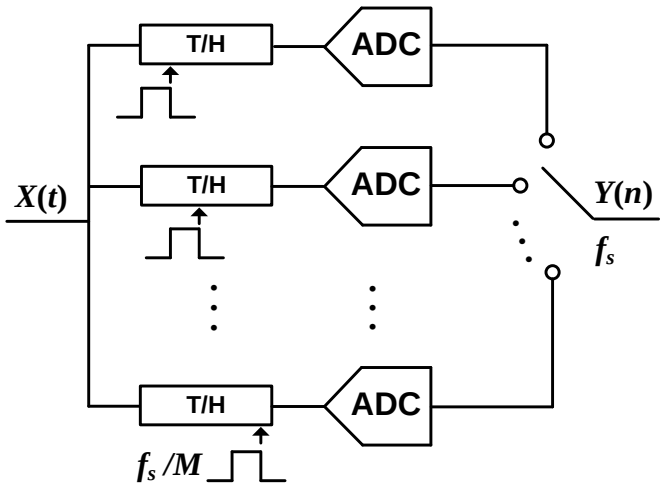
Figure 2.12 Fully digital calibration architecture for time skew.

Time skew also can be estimated and compensated purely in digital domain [23], [25], [31] as shown in Figure 2.12. However, the disadvantage of digital calibration is that the efficiency of time skew compensation becomes lower as the input frequency approaching Nyquist frequency, with oversampling ratios of 1.1 [25] or 1.3 [31]. In addition, with fixed optimized filter coefficients, the calibration could not be able to track environmental variation. Moreover, long-tap FIR filters adopted in prior works [25], [31] increase the computational complexity and considerable power consumption.

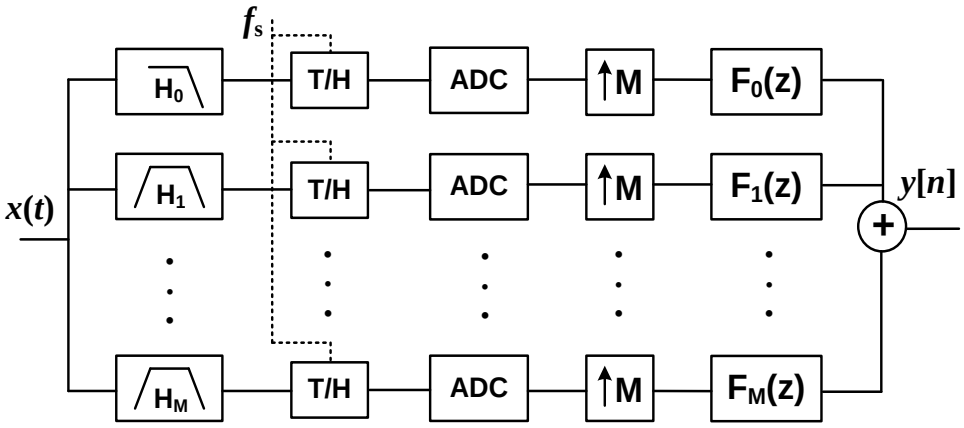
Chapter 3. CALIBRATION OF MULTI-CHANNEL ADCS

In this Chapter, we divide the multi-channel ADCs into two types: time-interleaved ADCs (TI-ADCs) and frequency-interleaved ADCs (FI-ADCs). Actually, from the perspective of signal processing, TI-ADCs are special cases of FI-ADCs. The mismatches among multiple channels always degrade the linearity of the entire ADC system. To compensate the non-linearity spurs caused by channel mismatches, the calibration methods for TI and FI ADCs are discussed in this Chapter.

3.1 Introduction



(a)



(b)

Figure 3.1 Architecture of ADCs. (a) Time-interleaved ADC. (b) Frequency-interleaved ADC.

In many mixed-signal systems, analog-to-digital converters (ADCs) play an important role for digitizing analog signal. To design high-speed and high-resolution ADCs, multi-channel ADC structure is adopted in numerous applications [50], [55]. And time-interleaved ADCs (TI-ADCs) shown in Figure 3.1(a) are the most frequently used multi-channel ADC structure, as the sampling rate of TI-ADCs can be boosted multiple times. However, due to process variation, there are mismatches between the channels, such as offset mismatch, gain mismatch, time skew and bandwidth mismatch, which result in the performance degradation. Many approaches have been published to mitigate the mismatches in timed-interleaved ADCs [66]-[71]. In [66], a multi-channel filter was utilized to compensate time skew and bandwidth mismatch. However, no mismatch parameter estimation block is used and the filter coefficients are fixed. It therefore cannot be adjusted with environmental changing. It was presented in [72] that the reported background calibration techniques can be categorized mainly into three types: the correlation-based approach [25], the equalization-based approach and statistics-based ones.

Besides TI-ADCs, there is another multi-channel architecture ADC as shown in Figure 3.1(b), named frequency-interleaved ADCs (FI-ADCs), which samples the input signal with unique clock signal f_s, avoiding therefore the time skew error in TI-ADCs. The analysis filter bank in front of sub-ADCs split the input signal in frequency domain instead of time domain. Earlier research work on this architecture included applications based on filter bank in communication and signal processing [73], with some applications thereafter using hybrid filter bank (HFB) to design multi-channel ADC [74]-[76].

3.2 Time-interleaved ADCs

3.2.1 Mismatches of TI-ADCs

Offset mismatch and gain mismatch can be calibrated easily [48], [78]. A digital compensation filter based bandwidth mismatch calibration approach is proposed in [78]. However, due to correlation between channels, time skew cannot be calibrated easily. Though it can be compensated by digital post processing [25], the performance cannot satisfy the SFDR requirement at high input frequency. In [79], a digital filter bank is adopted to compensate all the mismatches in TI-ADCs, but it does not propose channel mismatches estimation techniques, instead obtaining the mismatches through instruments. There is also a background time skew calibration method published in [67], which, however, is only suitable for input signals with wide bandwidth and extra slicers are needed for the sample time error estimation. In [69], an average value calculation of all the channels is employed. Unfortunately, it is not feasible for large number of channels implementation.

3.2.2 Statistic calibration method for TI-ADCs

3.2.2.1 Time skew extraction using clock signal

In this section, the proposed time skew calibration technique is introduced. The clock signal goes through a divider, which is normally a periodic square wave, will be adopted as input signal to carry out time skew calibration. The expression of square wave is

$$x(t) = \frac{4A}{\pi} \sum_{k=1}^{I} \frac{\sin(2\pi(2k-1) f_0 t)}{2k-1}, \tag{3.1}$$

where A is the amplitude of square wave. And f_0 is the fundamental frequency, which equals $K/N \cdot f_s$. K/N is the division ratio. I represents number of harmonics consisting of the square wave. The sampled and quantized $x(t)$ with a period T_s is

$$x[n] = \frac{4A}{\pi} \sum_{k=1}^{I} \frac{\sin(2\pi(2k-1) f_0 n T_s)}{2k-1} + q_B[n], \tag{3.2}$$

where $q_B[n]$ is the noise caused by B-bit quantization, and k=1, 2, …I. It should be mentioned that the gain and offset error will not affect the time skew calibration, as long as the errors are controlled below one LSB level. The multiplication of two adjacent sub-ADC channel outputs, $x_m[n]$ and $x_{m+1}[n]$, is represented as

$$\begin{aligned} M_{m,m+1}[n] &= x_m[n] \cdot x_{m+1}[n] \\ &= [\frac{4A}{\pi} \sum_{k_m=1}^{I} \frac{\sin(2\pi(2k_m-1) f_0 n T_s)}{2k_m-1} + q_B[n]] \cdot [\frac{4A}{\pi} \sum_{k_{m+1}=1}^{I} \frac{\sin(2\pi(2k_{m+1}-1) f_0 (nT_s + T_s/M + \Delta t_{m,m+1}))}{2k_{m+1}-1} + q_B[n]] \\ &= \frac{8A^2}{\pi^2} \sum_{k=1}^{I} \frac{\cos(2\pi(2k-1) f_0 (T_s/M + \Delta t_{m,m+1}))}{2k-1} + o[n] + e_B[n] \quad , \end{aligned} \tag{3.3}$$

where $\Delta t_{m,m+1}$ is the time skew between channel m and channel m+1 and M is the number of channels. $e_B[n]$ indicates the components related with quantization noise $q_B[n]$, whose mean value is zero. $o[n]$ represents the components related with n, of which mean value is zero if

$$\begin{cases} n[(2k_m-1) \pm (2k_{m+1}-1)] \neq gN \\ 2n(2k_{m,m+1}-1) \neq gN \end{cases} \quad g = 1,\ 2,\ 3\ \ldots. \tag{3.4}$$

Taking N =7 as an example, number of harmonics must be less than 7 so that I<4 in order to satisfy (3.4). Here, the division ratio N is selected as odd number, satisfying (3.4). Then the mean value of $M_{m,m+1}(n)$ is

$$E[M_{m,m+1}] = \frac{8A^2}{\pi^2} \sum_{k=1}^{I} \frac{\cos(2\pi(2k-1) f_0 (T_s / M + \Delta t_{m,m+1}))}{(2k-1)^2} \quad . \tag{3.5}$$

It can be seen from (3.5) that $E[M_{m,m+1}]$ is related with time skew $\Delta t_{m,m+1}$, of which the relation is drawn in Figure 3.2.

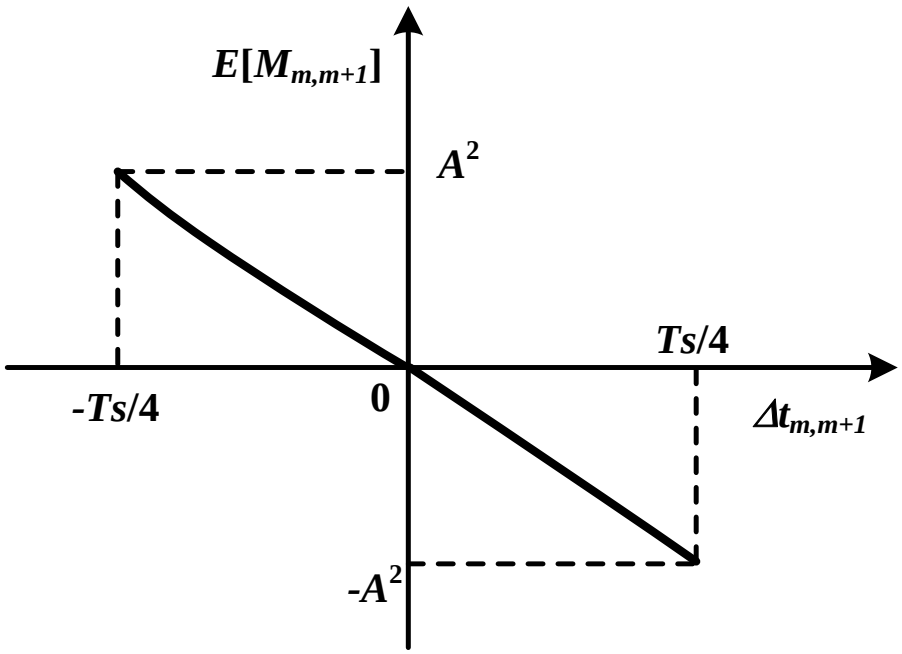


Figure 3.2 The monotonic relation between Δtm,m+1 and E[Mm,m+1] with *f*0/*f*s= 48/49, *M*=4, *A*=1.

Within the range of [$-T_s/4$, $T_s/4$], the relation is monotonic, which is necessary for calibration. For a given required time accuracy ε, the mean value $E[M_{m,m+1}]$ should be less than $4A^2\varepsilon/T_s$ approximately. The time skew calibration range is up to [$-T_s/4$, $T_s/4$], which is large enough for normal implementation. The mean value is estimated by averaging large number of samples, suppressing the effect of $o[n]$ and $e_B[n]$ in (3.3).

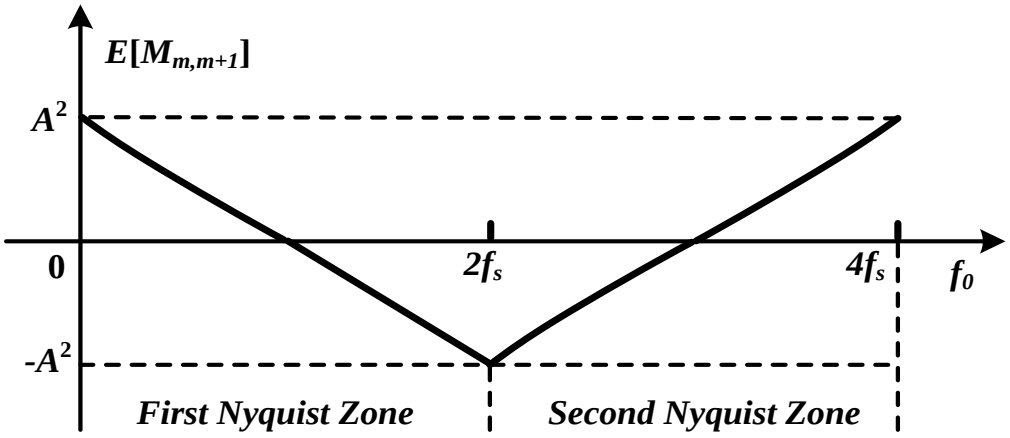
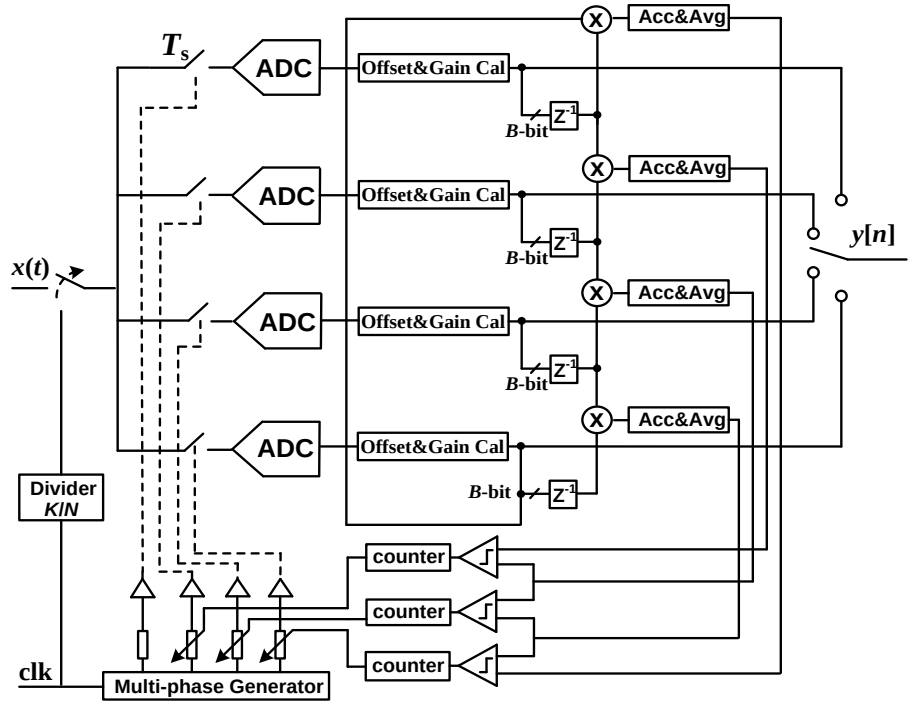


Figure 3.3 The relation between f_0 and $E[M_{m,m+1}]$ with $\Delta_{tm,m+1}$ =0, M=4, A=1.

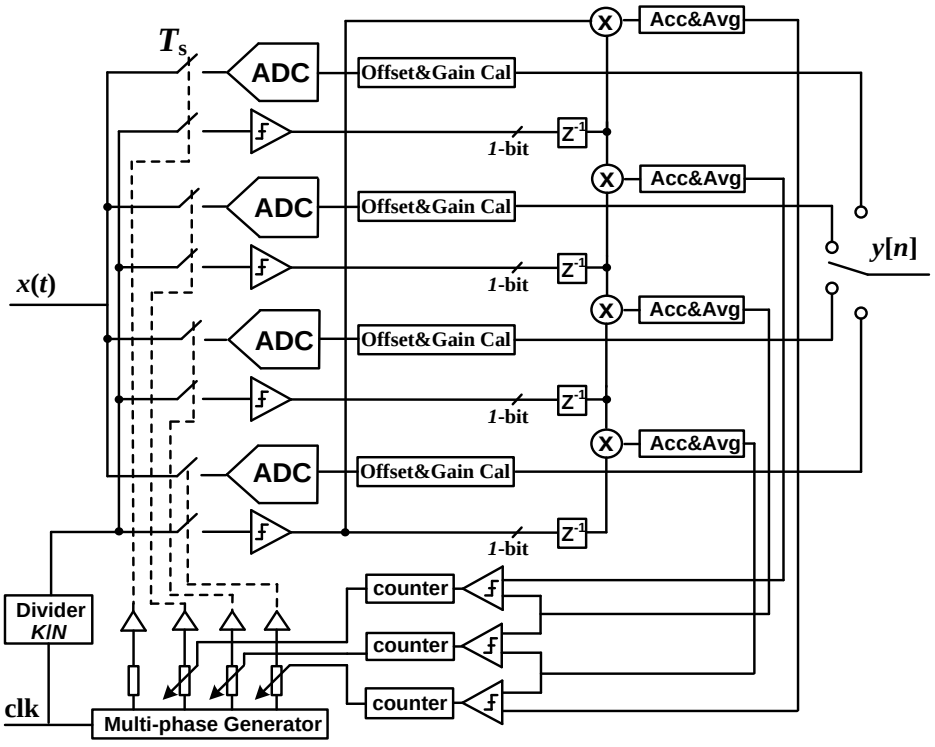
In Figure 3.3, it shows the relationship between $E[M_{m,m+1}]$ and fundamental frequency f_0. It can be seen that the polarity is opposite for different Nyquist zones. Fortunately, it is monotonic in one Nyquist zone. Additionally, it can be concluded from (3.3) that it is always monotonic in one Nyquist zone regardless of the number of channels M, which means the calibration technique can be used for TI-ADCs with arbitrary number of channels.

3.2.2.2 Calibration algorithm

To illustrate the calibration operation, two block diagrams of 4-channel TI-ADCs, including foreground calibration and background calibration, are shown in Figure 3.4.



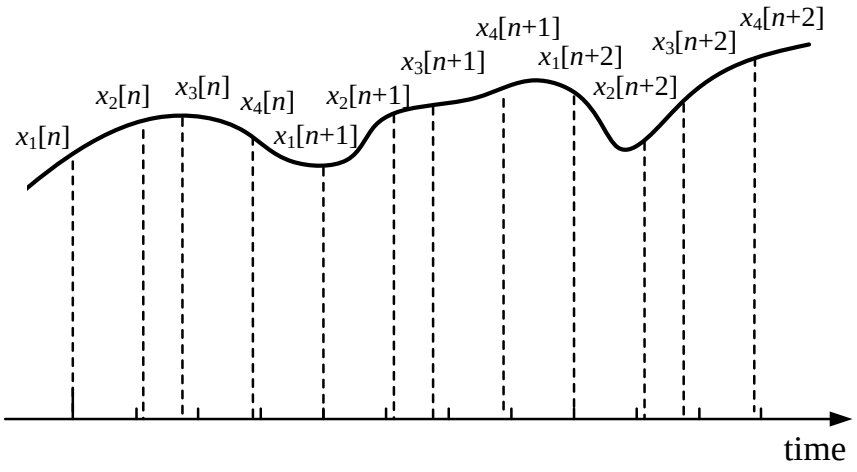
(a)



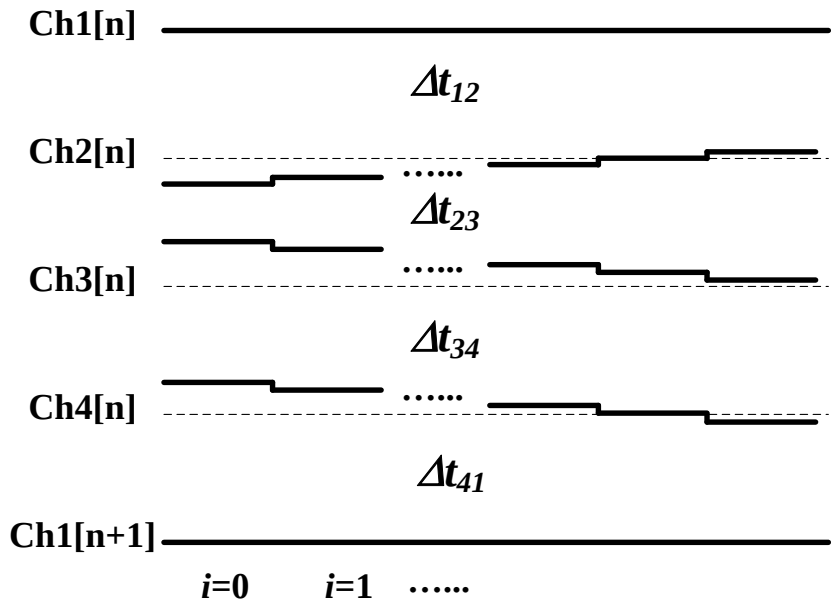
(b)

Figure 3.4 The proposed calibration structure for 4-channel TI-ADCs. (a) Foreground architecture. (b) Background architecture.

The calibration structure is a closed-loop iterative system. In Figure 3.4(a), during the calibration, the input is switched to the clock signal after divider with a frequency $K/N \cdot f_s$. The samples from sub-ADC of each channel go through offset and gain calibration block first, followed by a truncation block, where the remaining B-bit is multiplied with adjacent channels. If B equals 1, the multiplier can be replaced by a NAND gate, which reduces the hardware cost. Then the output value of the accumulator and average block is the approximation of mean value $E[M_{m,m+1}]$. After the estimation of $E[M_{m,m+1}]$, every two adjacent mean values $E[M_{m-1,m}]$ and $E[M_{m,m+1}]$ are compared to generate one bit output, tuning the time skew of mth channel by making the counter add or subtract one T_{step}, which is the adjustment resolution of digital controlled delay block. In Figure 3.4(b), the background calibration architecture is shown. The basic idea is using a duplicated sampling switch [69] to sample divided clock signal and extracting time skew in the same way as in Figure 3.4(a). This technique poses no constraint on input signal and does not interrupt normal ADC operation. And it can also track the temperature and other environmental variation. However, the threshold mismatch between sampling switches is not covered and calibrated, leading to degradation of ADC performance. To alleviate the threshold mismatch effect, the size of sampling transistor could be made large, and clock edge could be sharp enough. There is a non-ideal sampling case of a 4-channel TI-ADC in Figure 3.5(a), where channel 1 is the reference channel. Time skew between channel m and m+1is represented as $\Delta t_{m,m+1}$.



(a)



(b)

Figure 3.5 Illustration of calibration process. (a) Input signal with time skew. (b) The process of convergence.

It can be seen from Figure 3.5(a) that $\Delta t_{12}>0$, $\Delta t_{23}<0$, $\Delta t_{34}>0$ and $\Delta t_{41}>0$. The operation process of calibration is illustrated in Figure 3.5(b), where i is number of iterations. When $i=0$, $\Delta t_{12}>\Delta t_{23}$, after first iteration, the phase of channel 2 decreases by one T_{step}. The same operations are done in channel 3 and channel 4. And if $\Delta t_{12}=\Delta t_{23}$, the delay of

channel will be unchanged until next iteration. In addition, to ensure that the algorithm works, the process of calibration should be demonstrated to be convergent. First, defining the $\Delta t_{\max}$ and $\Delta t_{\min}$ as

$$\Delta t_{\max} = \max_{m,m+1} | \Delta t_{12}, \Delta t_{23}, \Delta t_{34}, \Delta t_{41}) | \tag{3.6}$$

and

$$\Delta t_{\min} = \min_{m,m+1} | \Delta t_{12}, \Delta t_{23}, \Delta t_{34}, \Delta t_{41}) |, \tag{3.7}$$

respectively. According to the algorithm illustrated in Figure 3.5(b), the value of $\Delta t_{\max}$ will always be decreased (or unchanged), and $\Delta t_{\min}$ will always be increased (or unchanged). In other words, it means $\Delta t_{\max}(i+1) \leq \Delta t_{\max}(i)$ and $\Delta t_{\min}(i+1) \geq \Delta t_{\min}(i)$. Therefore, the conclusion can be drawn as

$$\lim_{i\to\infty} \Delta t_{\max}(i) = \lim_{i\to\infty} \Delta t_{\min}(i), \tag{3.8}$$

which means as i approaches infinity, all the time skew between two adjacent channels become the same, meaning there is no time skew. The time needed for convergence T_{con} depends on the maximum variation of time skew $\Delta t_{\max}$ and the number of samples N_s for estimation of mean value. It can be represented as

$$T_{con} = \frac{\max | \Delta t_{\max} |}{T_{step}} \cdot N_s \cdot T_s, \tag{3.9}$$

where T_s and N_s are sampling period and number of samples for mean value estimation, respectively. The selection of N_s is based on the calibration accuracy ε and number of bits B used for estimation. The relationship between ε and T_{con} with fixed B is linear. And the relation between B and T_{con} with fixed ε is also linear.

3.2.2.3 Digitally controlled delay block

After the detection of time skews, some techniques can be employed to compensate the time error. Basically, there are two kinds of calibration methods, analog compensation [28] and digital tuning [25]. For the digital calibration, variable fractional delay filter can be adopted to take advantage of its stability and robustness. However, to maintain the high resolution calibration, the required filter length will be long, which increases the power consumption and hardware overhead. Also, as the calibration range increases, the accuracy will be reduced. On the other hand, benefiting from scaling of the process, high accuracy and large range analog calibration become feasible. To achieve both above simultaneously, the proposed calibration method is based on accurate capacitor array tuning.

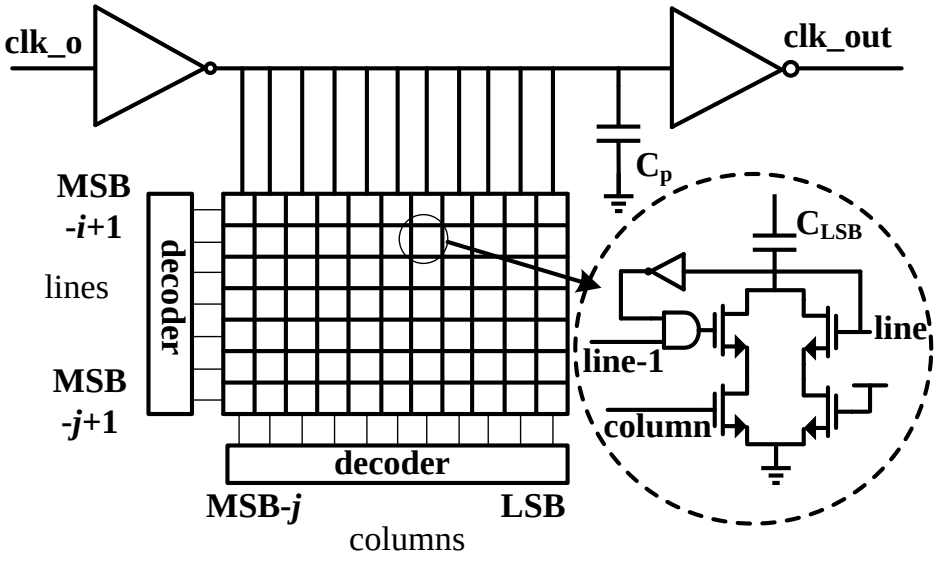


Figure 3.6 The digitally controlled delay block.

As shown in Figure 3.6, there is a capacitor array based digitally-controlled delay block. The number of C_{LSB} connected to the output of clock buffer is controlled by a binary code, of which the MSBs bits control the lines and LSBs control the columns. With this

arrangement, the time delay will be monotonic, which is more important than linearity of the capacitor array. C_p is the parasitic capacitor. The number of bit N_c required for calibration should larger than $\log_2(T_{max}/T_{step})$. T_{max} is the maximum time skew error. Nowadays, because of the monotonic adjustment of time delay and small metal capacitor (~50aF) used in advanced technology [55], the tough requirement of time skew calibration accuracy (~90fs) [80] for high performance time-interleaved ADC design could be satisfied.

3.2.2.4 Simulation results

In this section, a 4-channel 1GS/s 12-bit TI-ADC system is designed to validate the proposed calibration technique. The simulation is based on the system level model. The division ratio K/N is set as 64/81, which is easily realized by frequency doubler and divider. The time skew is set so that $[\Delta t_1, \Delta t_2, \Delta t_3, \Delta t_4]$ = [40ps, 5.1ps, 28.3ps, 38.4ps] and the resolution of the digitally controlled delay array is 0.1ps. The number of samples N needed for accumulation and average is set to 10000. The simulation results are obtained by using the block diagram in Figure 3.4(a). The same results are obtained through the block diagram in Figure 3.4(b). According to Figure 3.4(a), the delay of channel 1 is fixed as reference channel. And the delay of channel m (m=2, 3, 4) can be adjusted accordingly.

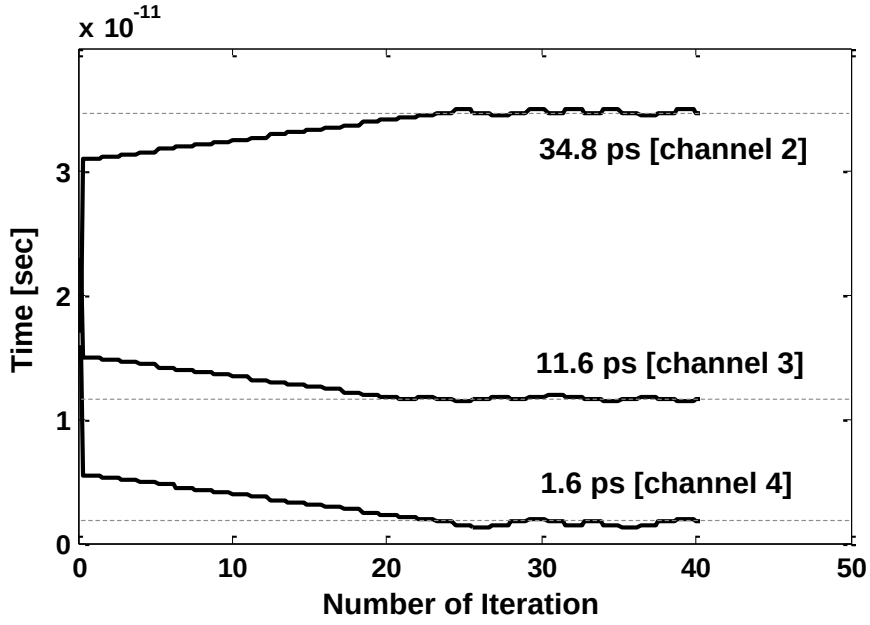
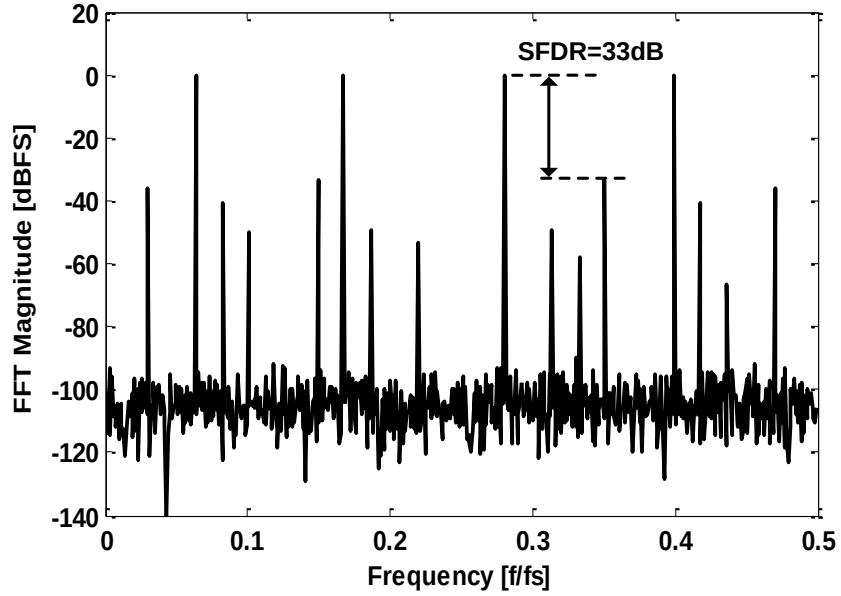
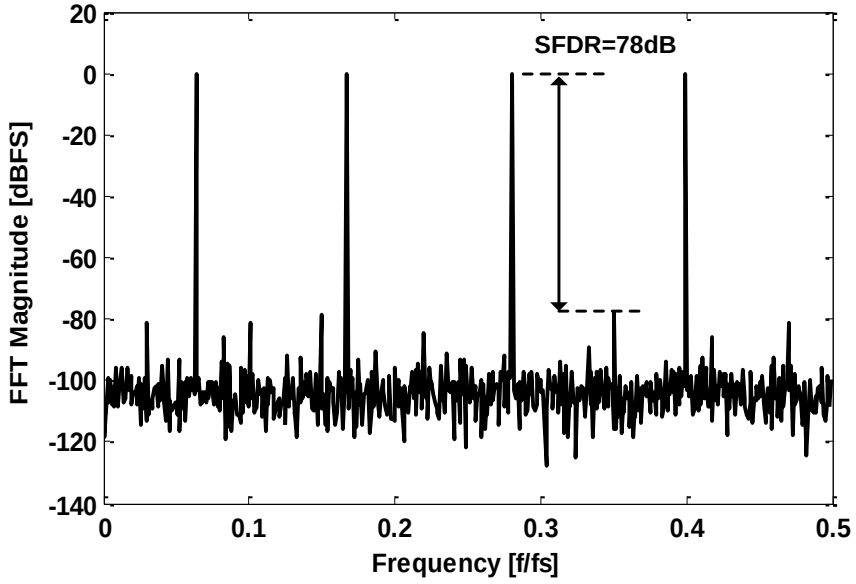


Figure 3.7 Convergence of the optimized time delay values.

The convergence performance of calibrated delay values in digitally controlled delay array is presented in Figure 3.7, where the calibration is finished after about 26 iterations. Finally, the optimized variable time delay values of channel 2, 3, 4 equal [34.8ps, 11.6ps, 1.6ps], making total delay of each channel same as 40ps approximately. Before and after the calibration using divided clock signal, the input signal containing 63.48MHz, 166.9MHz, 280.3MHz and 399.4MHz, is input to proposed TI-ADC. The 1024-point Fast Fourier Transform (FFT) of output signal before calibration is shown in Figure 3.8(a), while Figure 3.8(b) shows FFT of output signal after calibration. It can be seen from Figure 3.8 that the SFDR is improved to 78dB after calibration, satisfying the request of a 12-bit ADC system.



(a)



(b)

Figure 3.8 The 1024-point FFT of output signal. (a) Before calibration. (b) After calibration.

3.2.2.5 Summary

A statistic based calibration technique for M-channel TI-ADC is proposed. Compared with the previous published techniques, it provides an effective time skew detection method, and with the digitally controlled delay block, the precision of the calibration can be further improved by decreasing the size of unit capacitor in the delay block. In addition, the calibration technique can be readily extended to TI-ADCs with more than four-channels. The summary and comparison table is listed in Table 3.1.

Table 3.1 Comparison Table.

Calibration Techniques	Pros.	Cons.
[67]	Background calibration.	Only for wideband input signal.
[69]	Background calibration.	Not suitable for large number of channels. Residual time skew due to threshold mismatch.
This work (Background)	Background calibration. Less hardware overhead.	Residual time skew due to threshold mismatch.

3.2.3 Fully digital calibration method for TI-ADCs

In this section, a digital time skew calibration technique for time-interleaved (TI) ADCs is presented. The time skew calibration for TI-ADCs in analog domain suffers from limited correction accuracy and additional jitter. The proposed digital time skew calibration method estimates the polarity of the time skew through correlation of adjacent channels and corrects the time error by adopting adaptive fractional delay filters iteratively. Simulation results show that, in a 4-channel 1GS/s 12-bit TI-ADC system,

the SFDR can be improved to 78dB by 5-order FIR filters within a calibration range of [-0.005/f_s, +0.005/f_s].

3.2.3.1 Digital fractional delay filter design

In this section, the design of digital fractional delay filter is proposed. Supposing T as clock period, and $T_d=\alpha T$ is the fractional delay time, where α is the delay parameter. Prior works [61], [62] on fractional delay filter optimized the filter coefficients in entire delay range -0.5< α <0.5, which results in polynomial approximation with order larger than 2 in order to achieve expected linearity. For time skew calibration, the range of α is usually within -0.02<α <0.02 [68]. Optimization for α in a small range reduces the order of polynomial approximation and FIR filter length, and equivalently, reducing hardware overhead and power consumption. The ideal transfer function of a filter with delay (α+β)T is given by

$$D(\omega, a) = e^{-j\omega(\alpha+\beta)T}, \tag{3.10}$$

where α is the fractional delay and β is the integer delay. Here, the coefficients of FIR filter are approximated by the linear polynomial of fractional delay α. Therefore, the transfer function of the FIR filter is

$$F(\omega, a) = \sum_{n=0}^{N-1} (c_{n,0} + \alpha c_{n,1}) e^{-j\omega nT}, \tag{3.11}$$

where N is the number of taps. The difference between ideal transfer function and the real transfer function, namely, the approximation error, is given by

$$e(\omega, \alpha) = F(\omega, a) - D(\omega, a). \tag{3.12}$$

The approximation error should be minimized by using certain criterion. The FIR filter coefficients $C_{n,m}$=[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, …, $c_{N-1,0}$, $c_{N-1,1}$], whose length is 2N, are to be optimized. The transfer function of $F(\omega,\alpha)$ can be rewritten as

$$F(\omega,a)=C_{n,m}\cdot(c(\omega)-js(\omega))^{\mathrm{T}},$$

where $\boldsymbol{c}(\omega)$=[1, 1, cos(ω), cos(ω),…, cos((N-1)ω), cos((N-1)ω)], and $\boldsymbol{s}(\omega)$=[0, 0, sin(ω), sin(ω),…, sin((N-1)ω), sin((N-1)ω)]. To minimize the approximation error, the following min-max problem needs be solved:

$$\min_{C_{n,m}}\{\max|e(\omega,\alpha)|\},\qquad \omega\in\Omega,\ \alpha\in A, \tag{3.13}$$

where $C_{n,m}$ contains all the filter coefficients to be optimized. Ω and A are the frequency band and time delay range of optimization respectively. The objective in (3.12) can be written as

$$\begin{aligned}&|e(\omega,\alpha)|\\&=|F(\omega,\alpha)-D(\omega,\alpha)|\\&=\left\|\begin{bmatrix}R^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha)\\ I^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha)\end{bmatrix}\right\|_2\\&=[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\end{aligned}$$

where

$$\begin{aligned}&R^D(\omega,\alpha)=[D(\omega,\alpha)]_R,\ \ I^D(\omega,\alpha)=[D(\omega,\alpha)]_I\\&R^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_R\\&I^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_I\\&R^{FD}(\omega,\alpha)=R^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha)\\&I^{FD}(\omega,\alpha)=I^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha)\end{aligned}$$

Here $[\cdot]_R$ and $[\cdot]_I$ represent the real and imaginary parts of a complex number or vector respectively. Therefore, the min-max problem can be reformulated as

$$\min_{C_{n,m}}\quad \delta$$

$$\text{subject to} \quad \delta - [R^{FD}(\omega,\alpha)^2 + I^{FD}(\omega,\alpha)^2]^{1/2} \geq 0. \tag{3.14}$$

And the above optimization problem within a certain range of frequency ω and fractional delay value α could be solved by a standard SOCP solver [76], which is

$$\min_{x} \quad c \cdot x$$

$$\text{subject to} \quad c \cdot x \geq \left\| Fx - d \right\|_2, \tag{3.15}$$

where c=[1, zeros(1,$2N$)], x=[δ, $C_{n,m}$]$^{\mathrm{T}}$, F=[0, $R^{\mathrm{F}}(\omega_i,a_j)$; 0, $I^{\mathrm{F}}(\omega_i,a_j)$], d=[$R^{\mathrm{D}}(\omega_i,a_j)$, $I^{\mathrm{D}}(\omega_i,a_j)$]$^{\mathrm{T}}$, i=0, 1,…, I, j=0, 1,…, J. And I and J are the number of frequency points and fractional delay points for computation respectively.

3.2.3.2 Time skew calibration for TI-ADCs

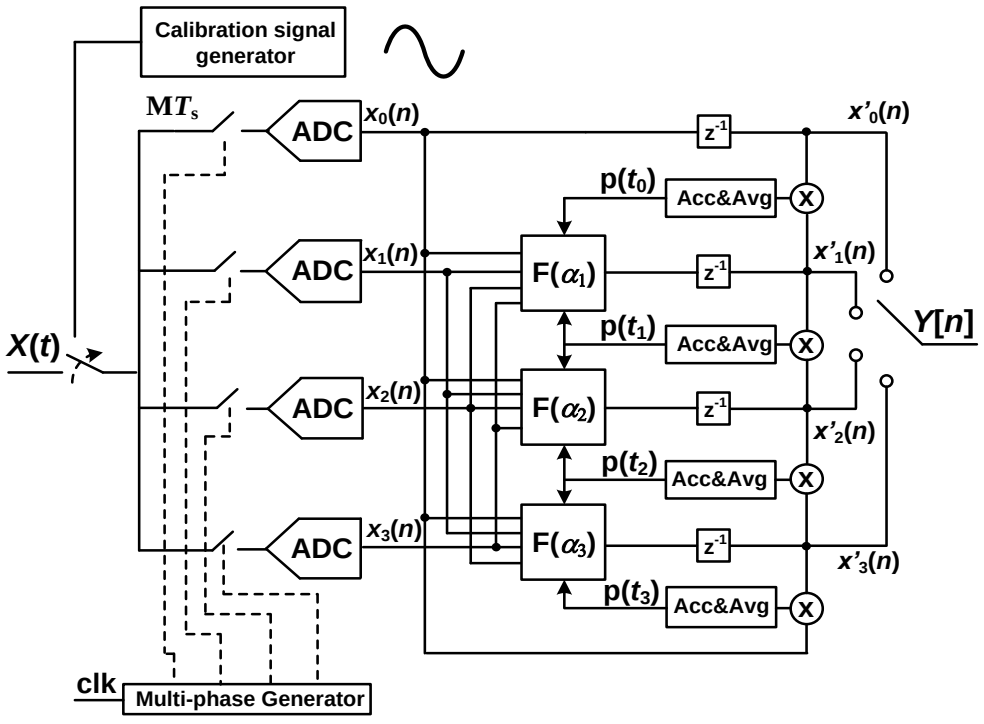


Figure 3.9 The proposed calibration architecture.

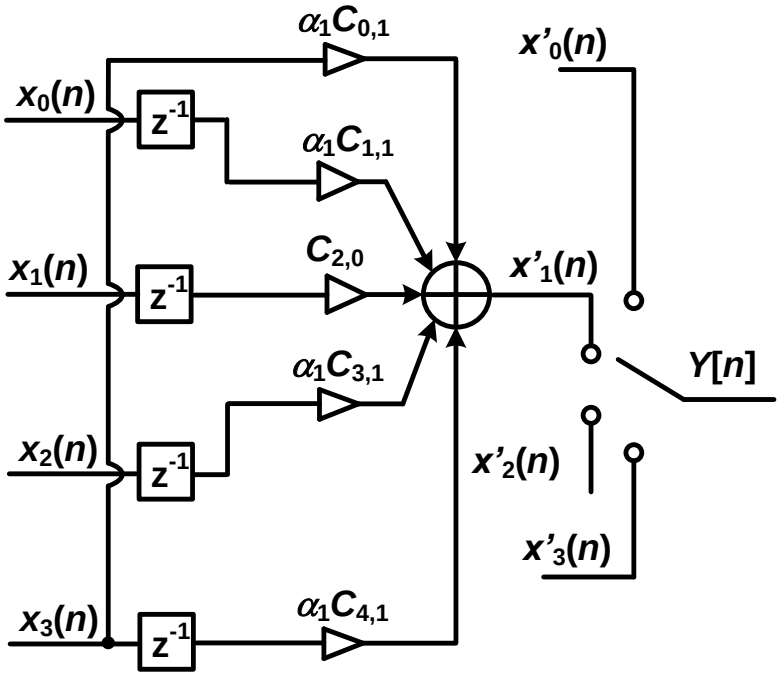
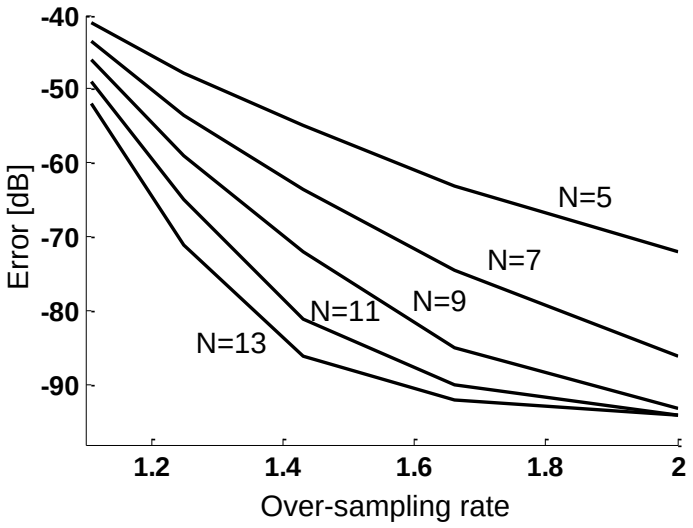


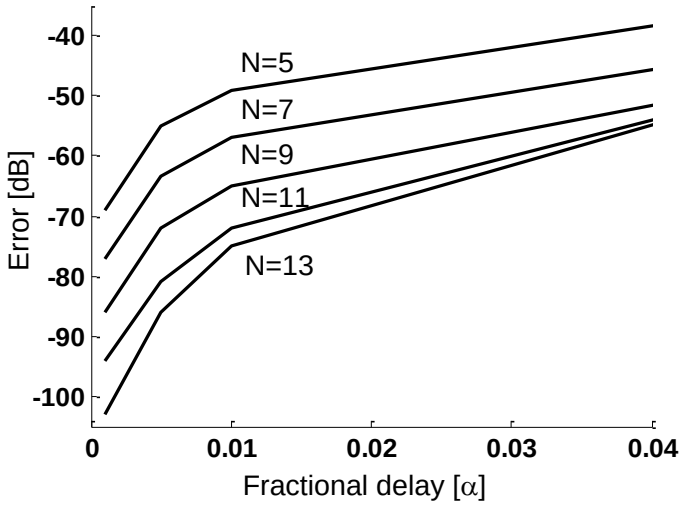
Figure 3.10 Implementation structure for $F(\alpha_1)$ with 5-tap FIR filter with coefficient using linear polynomial of fractional delay α_1.

The block diagram of a 4-channel TI-ADC depicting the proposed calibration technique is shown in Figure 3.9. The calibration structure is a closed-loop iterative system. The proposed calibration scheme has no stringent requirement on the reference input. Setting the first sub-channel as the reference channel, the delay of other 3 channels are tunable through variable fractional delay filters $F(\alpha_m)$ (m=1, 2, 3). The time skew estimation approach in [63] is adopted, and multiplication is conducted between every two adjacent channels, then the output value $p(t_m)$ (m=0, 1, 2, 3) of the accumulator and average unit is the approximation of the mean value $E_N[M]$. Then, every two adjacent $E_N[M]$ are compared. The delay parameter $\alpha_{m,m+1}$ of the delay filter $F(\alpha_{m,m+1})$ add or subtract one time step t_{step} according to the $E_N[M]$ comparison result. The convergence of the closed-loop system has been proven in [63]. Figure 3.10 depicts an implementation structure of a 5-tap fractional delay FIR filter. The coefficients use linear polynomial approximation. The α_m in Figure 3.10 represents the time skew of

$x_1(n)$. Since the range of fractional delay for time skew calibration is comparatively small, 20ps time skew for 1GS/s ADC system is reasonable. Therefore, the linearity could be calibrated to be 80dB by using the proposed short-tap FIR filter calibration technique. The number of taps of the fractional FIR filter is not necessarily long and 5~13 taps could satisfy most implementations. The relations of over-sampling rate, fractional delay, number of taps *N* and error suppression are illustrated in Figure 3.11.



(a)



(b)

Figure 3.11 (a) Error level versus over sampling rate with different *N* and α=[-0.005, 0.005]. (b) Error level versus fractional delay range with different *N* and oversampling rate=1.4.

3.2.3.3 Simulation results

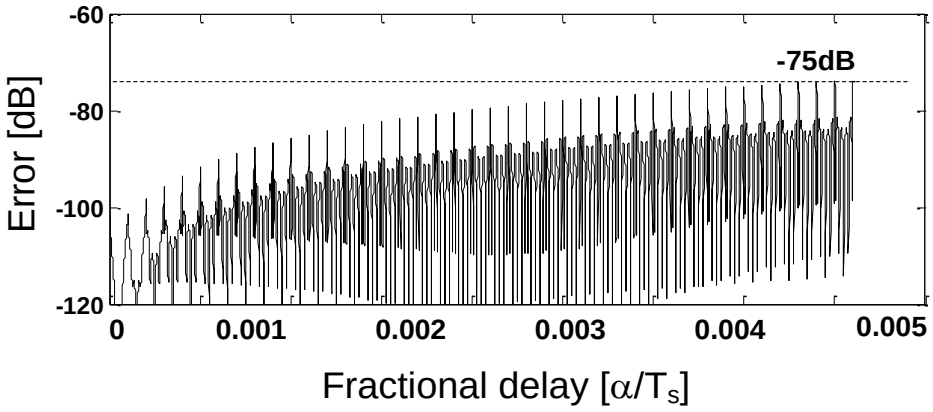


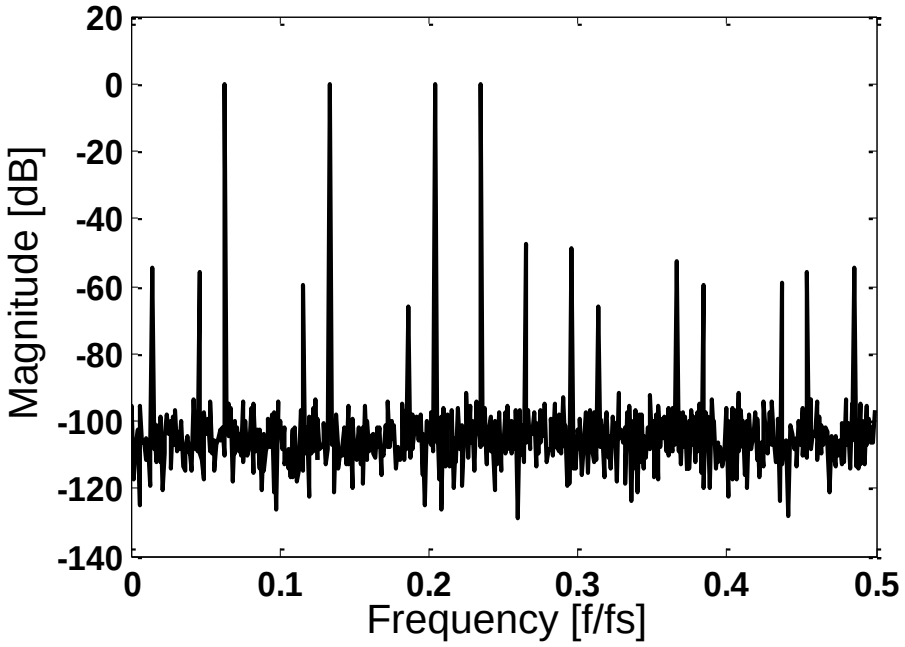
Figure 3.12 Convergence of the optimized time delay values.

Table 3.2 Optimized filter coefficients

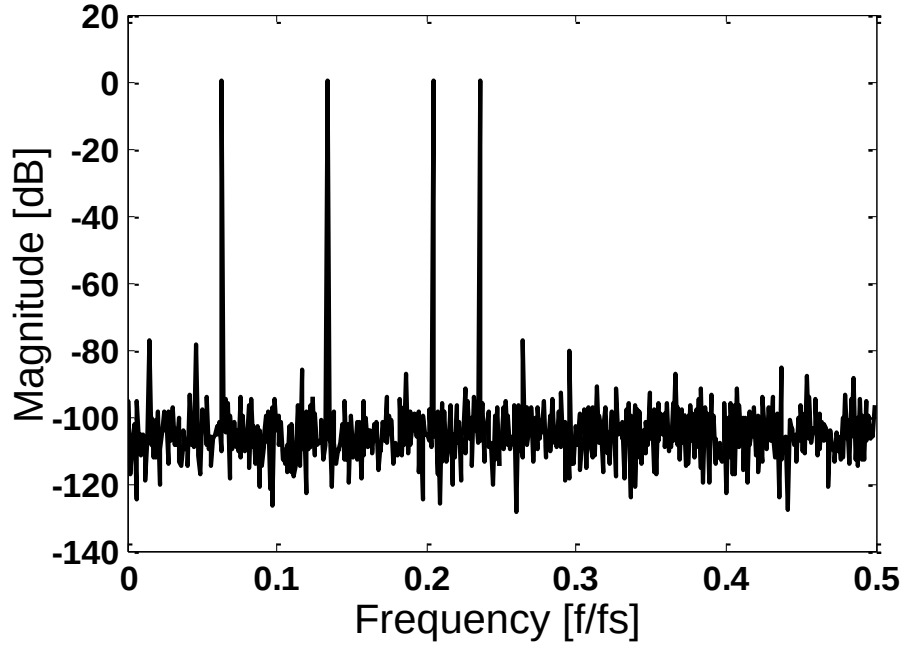
$C_{n,m}$	m=0	m=1
n=0	-5.6e-7 (0)	0.1453
n=1	6.3 e-6 (0)	-0.7602
n=2	1	-1.3e-13 (0)
n=3	6.3 e-6 (0)	0.7602
n=4	-5.6e-7 (0)	-0.1453

In this section, a 4-channel 1GS/s 12-bit TI-ADC system is designed to demonstrate the proposed calibration technique. The over sampling rate is 2. The fractional delay range for optimization is α=[-0.005, 0.005]. Using the SOCP solver, the optimization result for a 5-tap fractional FIR filter is shown in Figure 3.12. And the corresponding optimized coefficients of FIR filter are listed in Table 3.2. The small coefficients are set to 0. The input signal for calibration $x(t)$ =sin($2\pi f_{i1}t$)+sin($2\pi f_{i2}t$)+sin($2\pi f_{i3}t$)+ sin($2\pi f_{i4}t$), f_{i1}=63.5MHz, f_{i2}=133.8MHz, f_{i3}=204.1MHz, f_{i4}=235.3MHz. The reference channel is channel 1. Setting the time skew of the other three channels to [Δt_1, Δt_2, Δt_3] = [2ps, -3ps, 5ps]. The tuning time step is 0.1ps. The number of samples needed to accumulate and average N is set to 20,000. The 1024-point fast Fourier transform (FFT) of output signal before calibration is shown in Figure 3.13(a), while Figure 3.13(b) shows the FFT

of output signal after calibration. It can be seen from Figure 3.13(b) that the SFDR can be improved from 48dB to 78dB. The convergence process of calibration is presented in Figure 3.14, which shows that the calibration is terminated after iterating about 20 times and the optimized time delay value is [α_1, α_2, α_3]= [1.9ps, -3.1ps, 5.0ps].



(a)



(b)

Figure 3.13 Calibration results. (a) Before calibration. (b) After calibration.

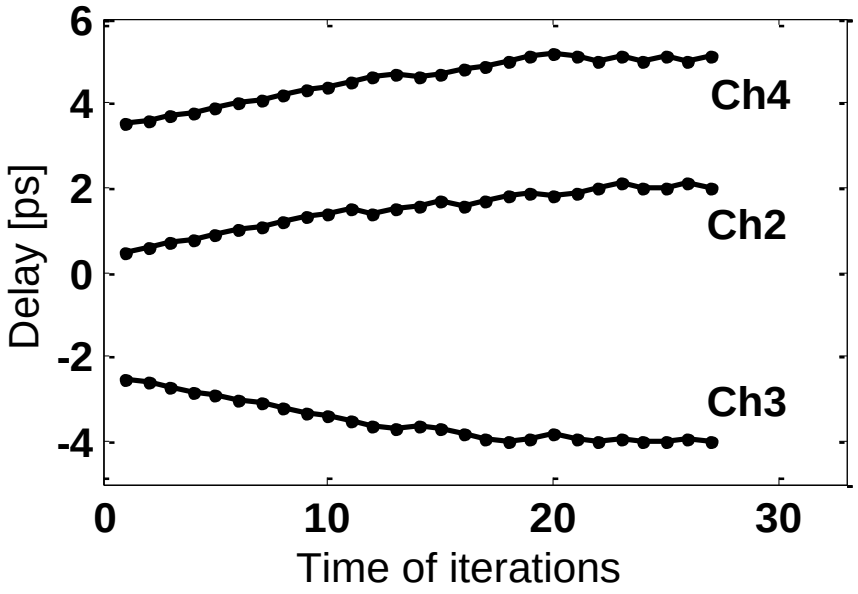


Figure 3.14 Convergence process.

3.2.4.4 Summary

An adaptive fractional delay FIR filter based calibration technique for *M*-channel TI-ADCs is proposed. Compared with previous published techniques, it provides a fully digital time skew calibration technique with less computational complexity. And the variable delay filter could also be extended to high-order approximation for better accuracy. In addition, the calibration technique is extendable to TI-ADCs with more channels. The summary and comparison is listed in Table 3.3:

Table 3.3 Optimized filter coefficients

Calibration Techniques	Pros.	Cons.
[23]	Background calibration	Long-tap FIR filter for compensation.
[79]	Large compensation time skew range.	Need measure the frequency response.

This work (Background)	Short-tap FIR filter for compensation.	Small compensation time skew range.

3.3 Frequency-interleaved ADCs

The filter bank mismatch of analog analysis filters in frequency-interleaved ADCs (FI-ADCs) degrades the system's spurious-free dynamic range (SFDR) significantly. In this section, a calibration approach for compensating such mismatch is presented. By modeling the parameter mismatches of the analysis filters, the filter bank mismatch compensation is divided into a coarse trimming and a fine tuning process. After the coarse compensation by trimming the resistors and capacitors in analog domain, fine tuning on the coefficients of synthesis filters is further carried out in digital domain to achieve high precision calibration. A design example of 10GS/s 8-bit four-channel FI-ADC is built in MATLAB. The simulation results show that 25-tap synthesis filters can satisfy the reconstruction requirement of 8-bit ADC. And the proposed calibration technique improves the SFDR to 51 dB, compensating the filter mismatch effectively.

3.3.1 Introduction of FI-ADCs

In the field of ultra high speed and medium resolution ADC design, where the work for calibration of time skew and multiphase clock distribution become costly, the FI-ADCs could overcome the drawbacks of TI-ADCs. Different from TI-ADCs, there is analysis filter bank in front of sampling circuits in FI-ADCs, which may introduce much mismatch degrading the ADC system performance. However, for the design of ADCs with medium resolution (6~8 bits) of which the SFDR is from 32dB to 50dB, the performance degradation caused by filter bank mismatch is limited. And with the help of mismatch calibration technique, the filter bank mismatch could be fully covered.

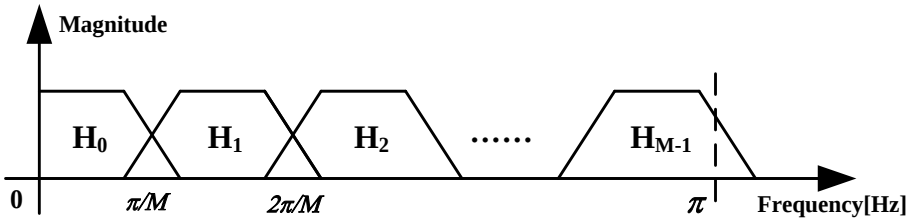


Figure 3.15 Frequency distribution of M-channel analysis filter bank.

In FI-ADCs , the input signal $X(j\Omega)$ is split into M equal frequency bands as shown in Fig. 2. After the zero-order sample and hold, sub-ADCs and interpolation, the signal is filtered by digital synthesis filters. The output signal is given by

$$Y(e^{j\omega}) = \frac{1}{M}\sum_{p=0}^{M-1} X(j\frac{\omega}{T} - j\frac{2\pi p}{MT})T_p(e^{j\omega}), \tag{3.16}$$

where T is the sample period of the system, p indicates the frequency-shifted versions of input signal. $T_p(e^{j\omega})$ is the system transfer function of FI-ADC given as

$$T_p(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m(j\frac{\omega}{T} - j\frac{2\pi p}{MT})F_m(e^{j\omega}), \tag{3.17}$$

where m represents the number of sub-channel ADC, $H_m(j\omega/T)$ is the analog analysis filter of mth channel, and $F_m(e^{j\omega})$ is mth digital synthesis filter. The system can be regarded as a perfect-reconstruction system if $T_p(e^{j\omega})$ satisfies the following condition

$$T_{ideal}(e^{j\omega}) = \begin{cases} c\cdot e^{-j\omega d}, & p = 0 \\ 0, & p = 1,...,M-1 \end{cases} \tag{3.18}$$

where c is a non-zero constant and d is the system delay.

In TI-ADCs, some mismatches has been discussed in numerous publications [25], [48], [81], such as bandwidth mismatch [78], gain mismatch, offset mismatch [21], [48]

and time skew [27], [69], [70]. For FI-ADCs, besides the filter bank mismatch, the other mismatches between channels mentioned in TI-ADCs also exist.

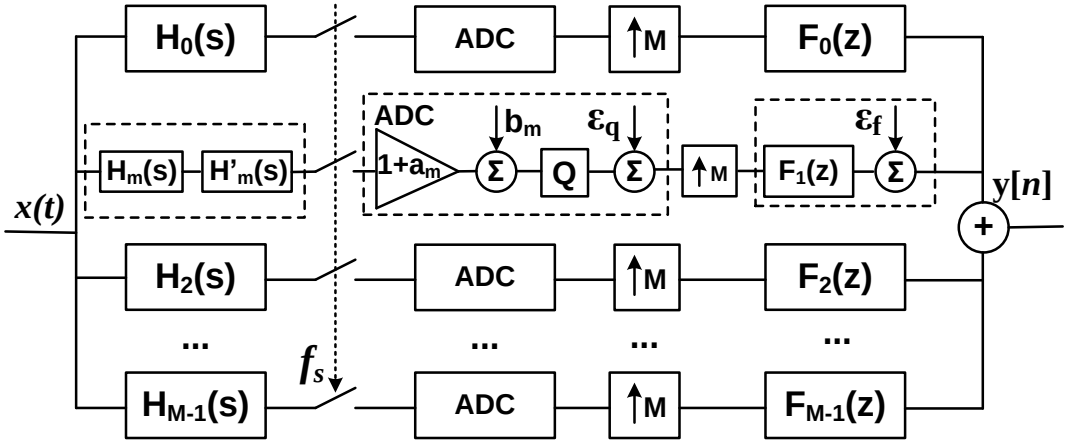


Figure 3.16 Architecture of FI-ADC with mismatch model.

The model of FI-ADC is shown in Fig. 3.16, including gain mismatch a_m, offset mismatch b_m, filter mismatch and bandwidth mismatch $H'_m(s)$ expressed as

$$H'_{\mathrm{m}}(s) = H_{Afb}{}'_{m}(s) \cdot H_{Bw}{}'_{m}(s) \tag{3.19}$$

In (3.19), $H_{Afb}{}'_m(s)$ and $H_{Bw}{}'_m(s)$ represent the analog analysis filter bank mismatch and bandwidth mismatch, respectively. The bandwidth of the sample circuit in each channel is modeled under a first-order approximation with c_{m} indicating the bandwidth mismatch and ω_0 denoting the reference bandwidth of each channel. In addition, the quantization in sub-ADC and limited word length in FIR synthesis filters are added as sources of noise ε_{q} and ε_{f}. With all the mismatches mentioned above taken into account, the output signal in (1) can be rewritten as

$$Y'(e^{j\omega}) = \frac{1}{M}\sum_{p=0}^{M-1} X(j\frac{\omega}{T} - j\frac{2\pi p}{MT})T_p'(e^{j\omega}) + O(e^{j\omega}), \tag{3.20}$$

where

$$T_p'(e^{j\omega}) = \sum_{m=0}^{M-1} H_m \cdot H_{Afb}'_m(j\frac{\omega}{T_s} - j\frac{2\pi p}{MT_s})F_m(e^{j\omega}) \cdot \frac{1}{1+s/c_m\omega_0} \cdot (1+a_m)$$

and

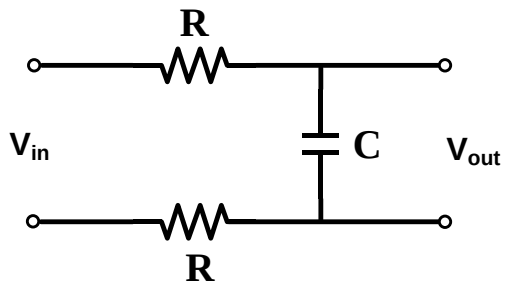
$$O(e^{j\omega}) = \frac{1}{M}\sum_{p=0}^{M-1}\sum_{m=0}^{M-1} b_m \cdot F_m(e^{j\omega})\delta(j\frac{\omega}{T_s} - j\frac{2\pi p}{MT_s}).$$

It can be seen in (3.20) that the $T_p'(e^{j\omega})$ includes the coefficient variation of analysis filters $H_{\mathrm{Afb}}'_m(j\omega)$, bandwidth mismatch c_{m} and gain mismatch a_{m}, which cause both distortion (p=0) and aliasing (p=1, 2, ... , M-1). The offset mismatch multiplied by $F_m(e^{j\omega})$ generates spectral components at $2\pi pf_s/M$. Given the analysis filter bank, the coefficients of synthesis filter bank can be obtained through optimization program. The error of perfect reconstruction described in (3) is

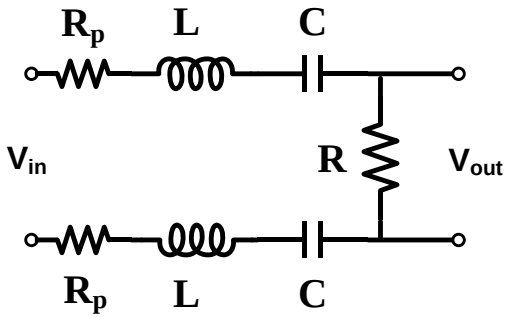
$$e_p(\omega) = |T_p'(e^{j\omega}) - T_{ideal}(e^{j\omega})|. \tag{3.21}$$

For the sequence of mismatch calibration in FI-ADC, the offset mismatch is calibrated first. Then, the gain mismatch, which may be caused by the analysis filter bank and sub-ADC, is compensated. Finally, filter bank mismatch calibration is done. For the bandwidth mismatch, which normally results from asymmetric layout routing and mismatch between track and hold block [78], could be alleviated by careful layout and increasing the bandwidth of track and hold block.

3.3.2 Design of analog analysis filters



(a)



(b)

Figure 3.17 Schematic of 2nd order passive filter. (a) Lowpass. (b) Bandpass.filter.

As mentioned above, the analog analysis filters split the input signal into *M* equal frequency bands. Here 1st order lowpass and 2nd order bandpass passive filters shown in Fig. 3.17 are adopted. R_p is parasitic resistor. The transfer function of analog filters are given by

$$\begin{cases} H_{LP}(s) = \dfrac{1/RC}{s+1/RC} \\ H_{BP}(s) = \dfrac{sR/L}{s^2+s(R+R_p)/L+1/LC} \end{cases}. \tag{3.22}$$

In (3.22), the locations of poles are assigned at frequency points that divide the input band into equal sub-bands. This means that the resistors *R* and inductors *L* can be

designed with same value. In this design, since all the resistors R are identical, the temperature variation on absolute value of R has no effect. Only the relative error of R is critical, this could be minimized by sufficient layout consideration. The corner frequency testing could calibrate all the R to the same value.

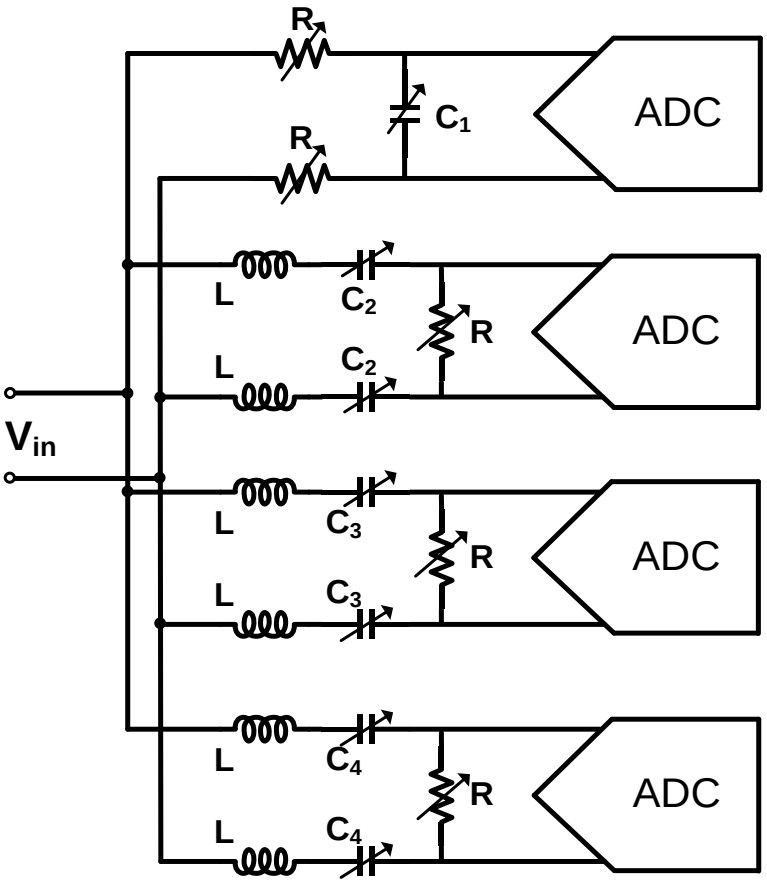


Figure 3.18 Schematic of analysis filter bank.

The schematic of a four-channel analysis filter bank is shown in Figure 3.18. The ratio of the capacitors is C1: C2: C3: C4= 12: 6: 2: 1. The mismatch between capacitors can be described as

$$\sigma^2_{\Delta C/C} = \frac{A^2}{W \cdot L} + B^2 \ , \qquad (3.23)$$

where A is the mismatch coefficient and B is the offset mismatch. W and L are the width and length of capacitor, respectively. With deep sub-micron technology (e.g. 65nm, 40nm), the value of A could be less than 0.5% and B is around 0.01%. Therefore, an accurate ratio of C_1, C_2, C_3 and C_4 can be obtained, meeting the requirement of medium resolution. Although the absolute value of capacitors may vary much due to process variations, the ratio of C_1/C_2 is accurate enough so that its influence on frequency response of analysis filter bank is predictable.

3.3.3 Filter bank mismatch calibration

Before explain the calibration scheme, the modeling of process variation of passive devices is considered first. Assuming that the variation factors of capacitor, resistor and inductor are is α_C, α_R and α_L, respectively. And also considering the gain mismatch α_m between channels, the equation (7) can be rewritten as

$$\begin{cases} H'_{LP}(s) = \dfrac{1/\omega_c}{s+\omega_c} \\ H'_{BP}(s) = \dfrac{sk_m(1+a_m)/LC}{s^2 + sk_m(\omega_c + R_pC)/LC + k_m/LC}, \\ \omega_c = \dfrac{1}{a_R a_C RC} \\ k_m = 1/a_C a_L \end{cases} \tag{3.24}$$

where $H_{LP}'(s)$ and $H_{BP}'(s)$ represent the transfer function containing mismatch. And ω_c is -3dB bandwidth of the low pass filter $H_{LP}'(s)$. Parameter k_m indicates the total variation of C and L. Based on the above analysis, the system transfer function in (2) can be rewritten as

$$T_p'(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m'(j\frac{\omega}{T} - j\frac{2\pi p}{MT})F_m(e^{j\omega}) \ , \tag{3.25}$$

where $H'(s)$ contains filter mismatch and gain mismatch. From (3.24), it is concluded that the calibration in analog domain can be realized by adjusting k_m (R) and ω_c (C). The calibration precision of analog trimming shown in Figure 3.18 is constrained by process limitations. Nevertheless, its calibration range is large. Digital calibration, on the other hand, can achieve high calibration precision whereas its calibration range is limited by linearity requirement of the calibration algorithm. Therefore, by combining analog and digital calibration methods, large calibration range and high precision tuning can be attained simultaneously.

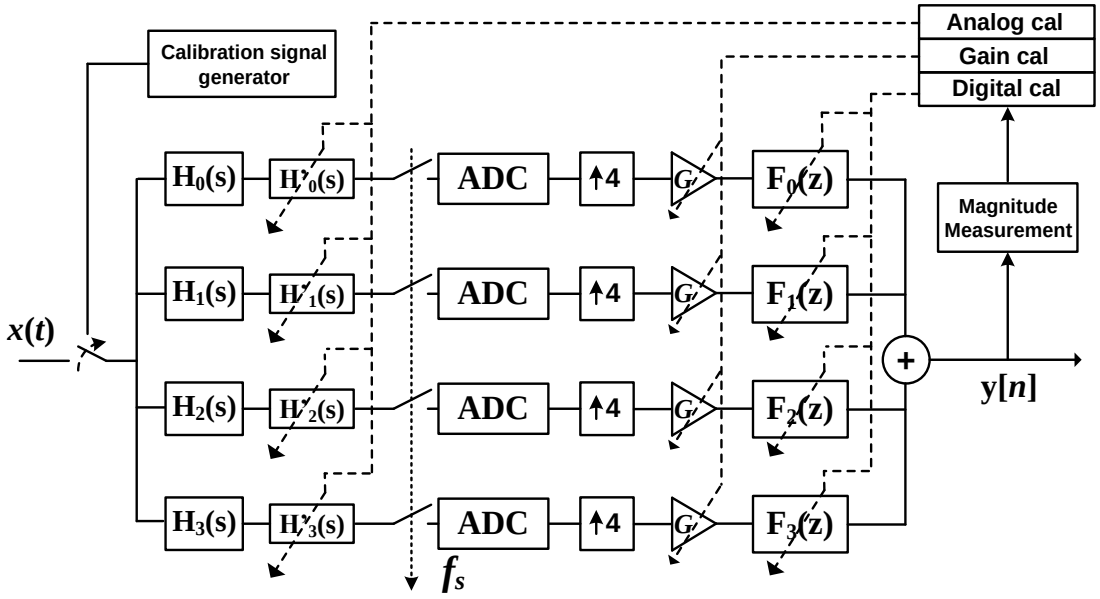


Figure 3.19 Block diagram of filter bank and gain mismatch calibration.

As an example, a 4-channel FI-ADC system is illustrated in Figure 3.19, which contains analog trimming, gain mismatch calibration and look-up-table (LUT) based digital filter coefficients tuning. $H_m(s)$ and $F_m(z)$ (m=0, 1, 2, 3) are the ideal analysis filters and digital synthesis filters, respectively. $H'_m(s)$ (m=0, 1, 2, 3) contains the mismatch factor

caused by parameter variations of the analysis filters, which will be compensated coarsely by resistor and capacitor trimming in analog domain as shown in Figure 3.18. After the coarse calibration, the system transfer function is changed to

$$T_p^{(\text{coarse})}(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m(j\frac{\omega}{T} - j\frac{2\pi p}{MT}) H_m^{(\text{coarse})}(j\frac{\omega}{T} - j\frac{2\pi p}{MT}) F_m(e^{j\omega}), \qquad (3.26)$$

with

$$|e_p(\omega)| = |T_{\text{ideal}}(e^{j\omega}) - T_p^{(\text{coarse})}(e^{j\omega})| \le \varepsilon_{\text{coarse}}. \qquad (3.27)$$

The error k_{m} of $H_m^{(\text{coarse})}(s)$ in (3.26) is controlled to be less than one coarse calibration step with its reconstruction error $e_p(\omega)$ being smaller than $\varepsilon_{\text{coarse}}$. Then, the remaining mismatch is fine compensated by the LUT based adaptive synthesis filter $F_m(z)$. In Figure 3.19, the pre-calculated synthesis filter coefficients corresponding to different filter bank mismatch with fine tuning step are stored in the LUT. And relation of stored coefficients and k_{m} is $f(\text{k}_0, \text{k}_1, \text{k}_2, \text{k}_3)$, in which k_{m} is the mismatch of analysis filter in mth channel. The min-max criterion is employed to calculate the coefficients of synthesis filters with given analog analysis filters $H_m(s)$, and the optimization problem is solved by standard second-order cone program (SOCP) solver [76]. After fine calibration the system transfer function becomes

$$T_p^{(\text{fine})}(e^{j\omega}) = \frac{1}{M}\sum_{m=0}^{M-1} H_m(j\frac{\omega}{T} - j\frac{2\pi p}{MT}) H_m^{(\text{coarse})}(j\frac{\omega}{T} - j\frac{2\pi p}{MT}) \cdot F_m(e^{j\omega}) F_m^{(\text{fine})}(e^{j\omega}) \qquad (3.28)$$

with reconstruction error

$$|e_p(\omega)| = |T_{\text{ideal}}(e^{j\omega}) - T_p^{(\text{fine})}(e^{j\omega})| \le \varepsilon_{\text{fine}}. \qquad (3.29)$$

Similar to coarse tuning, the error k_m of $H_m^{(\text{fine})}(s)$ caused is less than one fine tuning step and its associated reconstruction error $e_p(\omega)$ are trimmed to be less than one fine

calibration step and $\varepsilon_{\text{fine}}$, respectively. As a result, the SFDR of system after fine calibration is

$$SFDR^{(\text{fine})} = 20\log\frac{|T_0^{(\text{fine})}(e^{j\omega})|}{\max\{|T_1^{(\text{fine})}(e^{j\omega})|,|T_2^{(\text{fine})}(e^{j\omega})|,|T_3^{(\text{fine})}(e^{j\omega})|\}} \quad . \tag{3.30}$$

It can be seen in Figure 3.19 that there is a filter mismatch detector following the output signal $y[n]$ to measure the magnitude of calibration signal, which is generated from the calibration signal generator. By comparing the magnitude of several specific frequency points, the polarity of variation parameter k_m and a_{m} (m=0, 1, 2, 3) can be detected. Subsequently, the k_m error can be iteratively reduced, by trimming the R and C or updating coefficients of synthesis filters $F_m(z)$. And the a_{m} can be compensated in digital domain.

3.3.4 Calibration algorithm

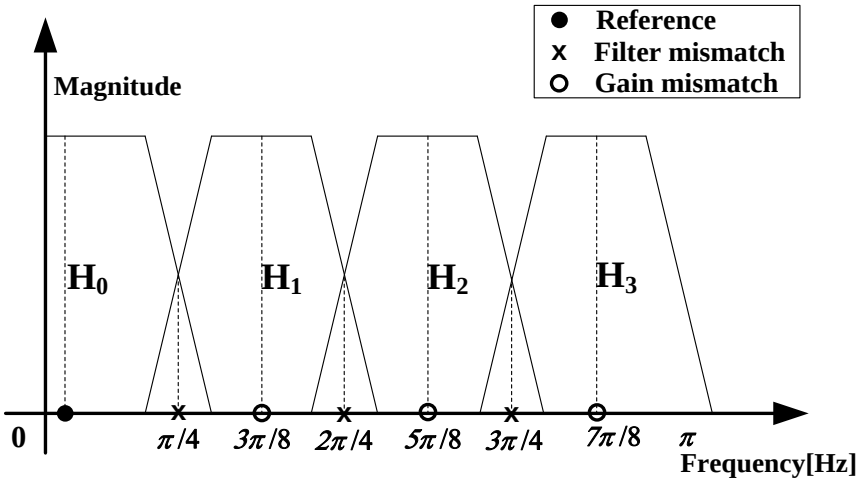


Figure 3.20 Illustration of magnitude comparison between certain frequency points.

Continuing with the 4-channel FI-ADC system example, the magnitude measurement at certain frequency points can be seen in Figure 3.20, where they are located near 0,

π/4, 3π/8, 2π/4, 5π/8, 3π/4 and 7π/8. Without filter bank and gain mismatch, the measured magnitude of these points should be the same. Since the frequency point at low frequency near DC point is not affected by filter parameter variation, the magnitude of $Y(0)$ can be chosen as a reference value. And magnitude of frequency points at π/4, 2π/4 and 3π/4 reflect the polarity of parameter k_m, which is expressed as

$$\begin{cases} Y(\frac{m\pi}{4}) > Y(0) > Y(\frac{(m+1)\pi}{4}), & k_m < 1 \\ Y(\frac{m\pi}{4}) < Y(0) < Y(\frac{(m+1)\pi}{4}), & k_m > 1 \end{cases} \quad (m=1, 2, 3). \tag{3.31}$$

It is observed in Figure 3.20 that if k_1 is smaller than 1, which means the shape of $H_1(s)$ is shifted to the left. Therefore, $Y(\pi/4)$ is larger than $Y(0)$ and $Y(2\pi/4)$ is smaller than $Y(0)$. By calculating and comparing magnitudes of the frequency points, k_m can be adjusted step by step until it converges to 1. Independently, the magnitude of frequency points at 3π/8, 5π/8 and 7π/8 indicate the gain difference between channels.

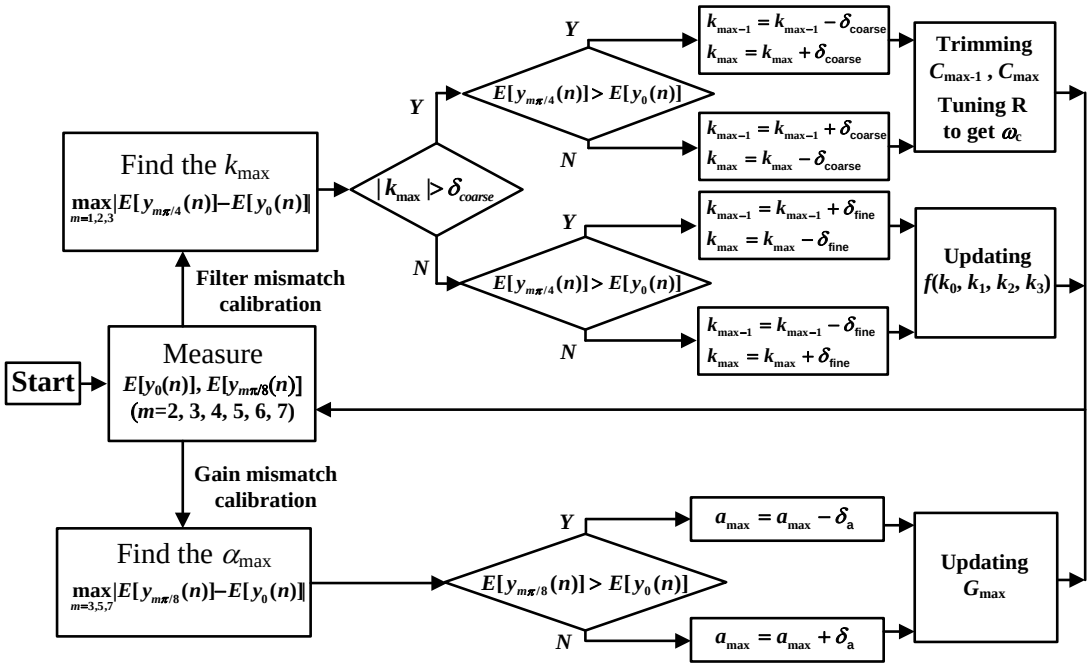


Figure 3.21 Reconstruction results without filter bank mismatch.

The calibration algorithm is summarized in the flow chart given in Figure 3.21. Filter bank mismatch calibration is divided into coarse trimming and fine tuning mode. Firstly, the maximum magnitude difference between the $Y(0)$ and $Y(m\pi/4)$ is obtained. Then, the corresponding parameter k_m is adjusted by one step. At the beginning, the calibration works at coarse trimming mode with step δ_{coarse}. Once the coarse trimming is done, the calibration is switched to fine tuning mode by updating coefficients of synthesis filter with step δ_{fine}. The accuracy of gain mismatch calibration is δ_{a}. In this way, the maximum magnitude difference is smaller than previous one after each trimming operation. Therefore, it can be found that

$$\max_{m=1,2,3}^{(i+1)} |Y(\frac{m\pi}{4}) - Y(0)| \leq \max_{m=1,2,3}^{(i)} |Y(\frac{m\pi}{4}) - Y(0)| \tag{3.32}$$

and

$$\max_{m=3,5,7}^{(i+1)} |Y(\frac{m\pi}{8}) - Y(0)| \leq \max_{m=3,5,7}^{(i)} |Y(\frac{m\pi}{8}) - Y(0)| , \tag{3.33}$$

where i is number of iteration. The calibration process stops when the variation parameters k_m and a_m (m=0, 1, 2, 3) fluctuate around one fine tuning step. Depending on the sum of the variation k_m, gain mismatch a_m, number of samples N for magnitude measurement and tuning size δ_{coarse} and δ_{fine}, the convergence time of filter bank mismatch calibration T_{con} is estimated as

$$T_{con} \approx (\frac{\sum_{m=0}^{3} |k_m - 1|}{\delta_{coarse}} + \frac{\sum_{m=0}^{3} |k_m - 1| \bmod \delta_{coarse}|}{\delta_{fine}}) \cdot N \cdot T_s \tag{3.34}$$

or

$$T_{con} \approx \left(\frac{\sum_{m=0}^{3} |\alpha_m - 1|}{\delta_a}\right) \cdot N \cdot T_s \tag{3.35}$$

where T_s is the sampling period of the FI-ADC system.

3.3.5 Simulation results

To demonstrate the proposed calibration method, a 4-channel 10GS/s 8-bit FI-ADC system is designed as an example.

Table 3.4 Parameters of analysis filter bank

	Value
R	50 Ohm
L	6.36 nH
C_1 (=12C_4)	2.546 pF
C_2 (=6C_4)	1.273 pF
C_3 (=2C_4)	0.424 pF
C_4	0.212 pF

Table 3.4 shows the values of components for analysis filter bank in Figure 3.18. According to Table I, all the resistors R are 50 Ohm and all the L are 6.36 nH in Figure 3.18. Firstly, the initial coefficient calculation of digital synthesis filters without filter bank mismatch is done. The target SFDR is larger than 50 dB according to satisfy 8-bit resolution. To achieve this with short-tap FIR filters, the idea of weighted filter design [9, 14] is applied here, which results in smaller aliasing error in the majority of frequency band (larger than 90%) at a cost of a small "don't care" band (no more than 10%). In the example, the "don't care" band is [0.9π, π]. As mentioned in (3), the target c and d are set to 1 and 12 respectively. The number of tap of synthesis filters $F_m(z)$ is set to 25.

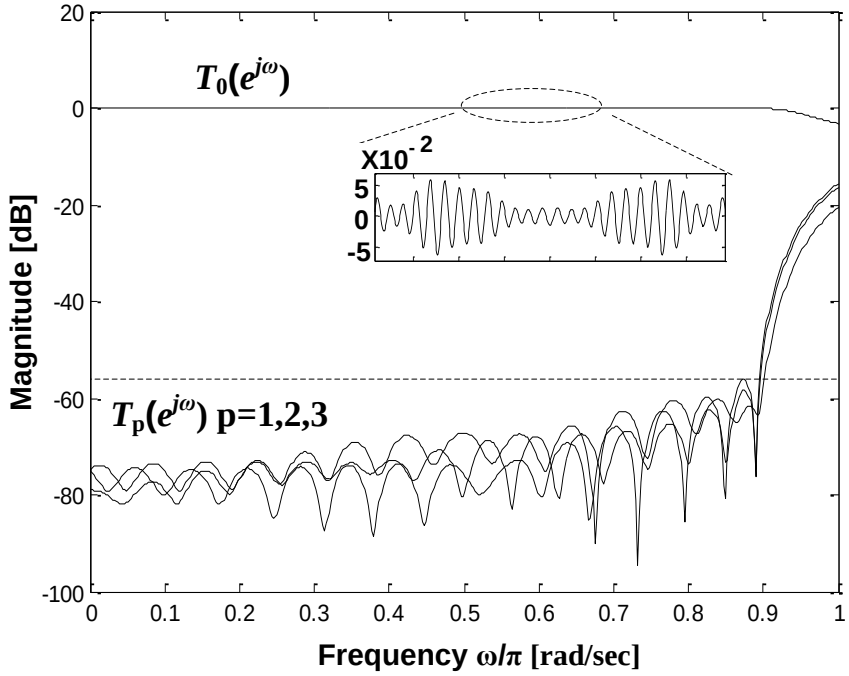


Figure 3.22 Reconstruction results without filter bank mismatch.

Conducting the optimization by SOCP solver, the results are shown in Figure 3.22 where maximum distortion of the original signal $T_0(e^{j\omega})$ is around 0.05 dB, while the attenuation is below -56 dB in frequency range [0, 0.9π]. Secondly, the calculation of the synthesis filter coefficients in LUT is based on same optimization criterion. Supposing the variation parameters k_m in $H'_m(s)$ (m=0, 1, 2, 3) and gain mismatch a_m (m=1, 2, 3) are listed in Table 3.5 along with the specifications of the given analog analysis filters.

Table 3.5 Specifications of analysis filters

m	Analysis filter type	Bandwidth (GHz) (-3dB)	Parameter variation (k_m)	Gain mismatch (a_m)
0	Low pass	[0,1.25]	1.102	-
1	Band pass	[1.25,2.50]	0.901	-0.04

2	Band pass	[2.50,3.75]	1.050	0.015
3	Band pass	[3.75,5.00]	0.950	-0.01

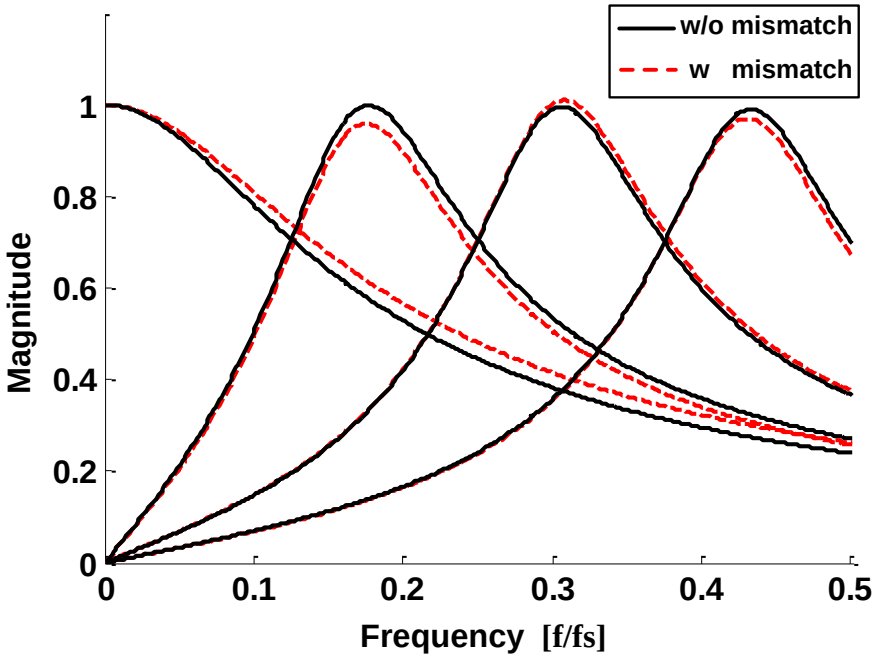
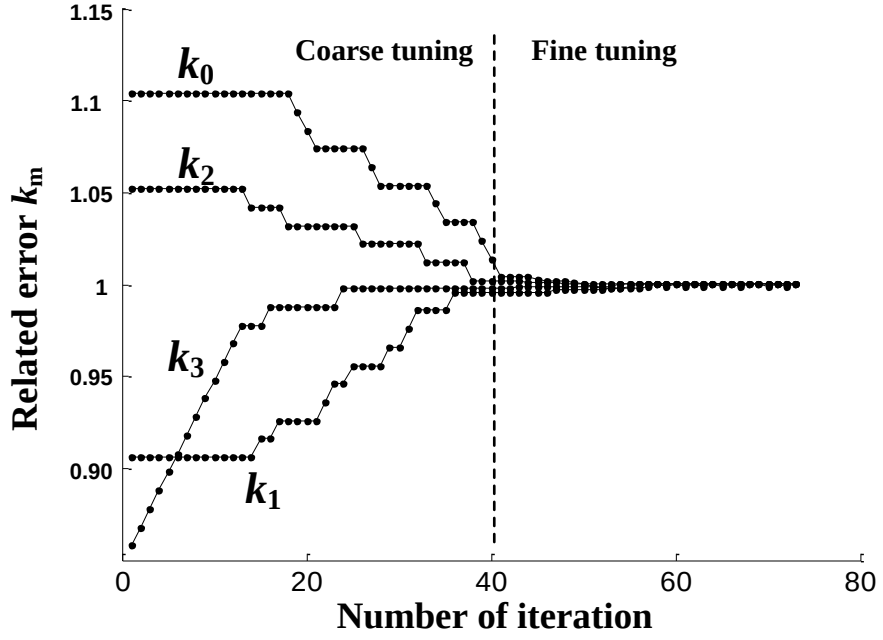
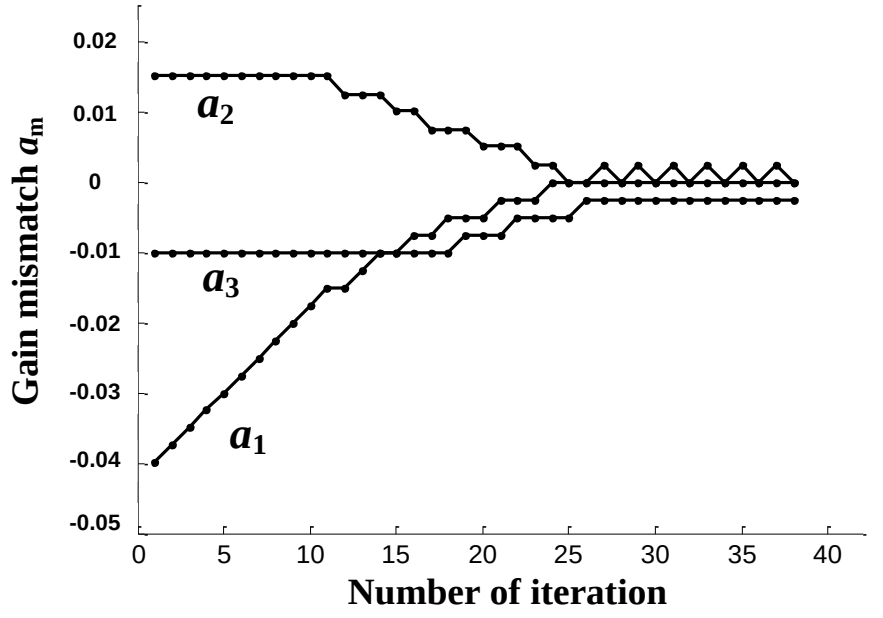


Figure 3.23 Magnitude responses of analog analysis filters $H_m(s)$ (m=0, 1, 2, 3).

The corresponding magnitude responses, with and without mismatches of analog analysis filters, are illustrated in Figure 3.23. To calculate the magnitude of the test points effectively, a small deviation in frequency needs to be added. In this case, magnitude measurement points are set at 5MHz (0), 1.249GHz ($\pi/4$), 1.874GHz ($3\pi/8$), 2.499GHz ($2\pi/4$), 3.124GHz ($5\pi/8$), 3.749GHz ($3\pi/4$) and 4.374GHz ($7\pi/8$). The coarse tuning step δ_{coarse} and fine tuning step δ_{fine} are set to 0.02 and 0.002, respectively. The tuning accuracy of gain mismatch calibration δ_a is set to 0.002.



(a)



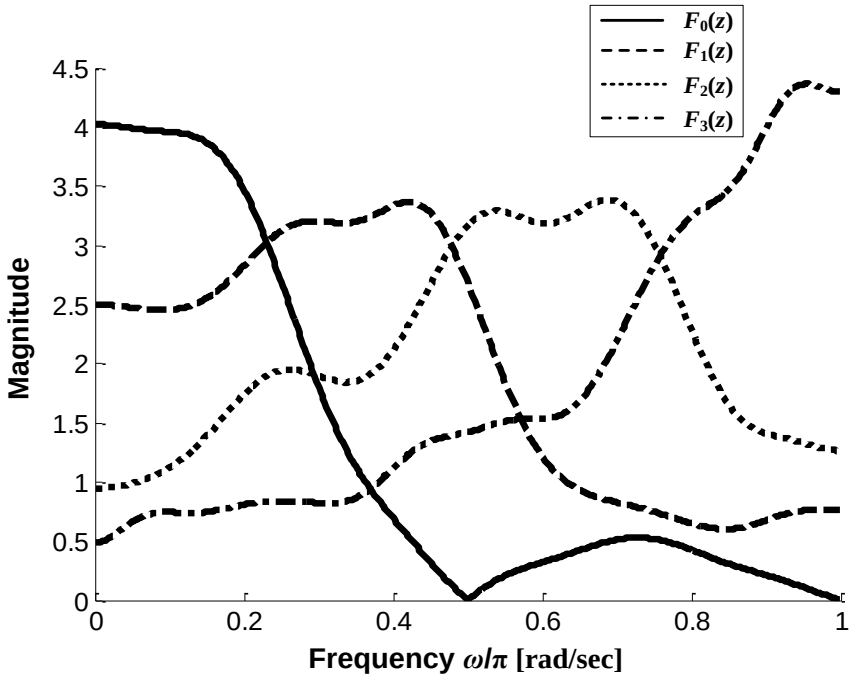
(b)

Figure 3.24 Convergence process of calibration. (a) Filter bank tuning. (b) Gain mismatches calibration.

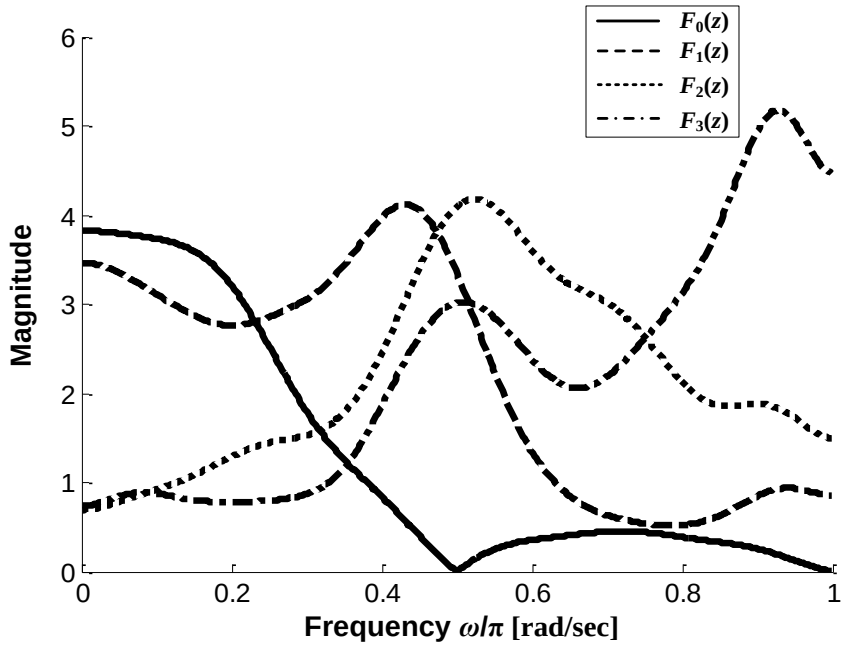
The convergence process is shown in Figure 3.24. In Figure 3.24(a), the process includes coarse tuning and fine tuning. Once the k_m error is smaller than δ_{coarse} after 40 iterations, the system calibration is switched to fine tuning mode for further calibration until k_m error falls within one fine tuning step δ_{fine}. The convergence process of gain error is shown in Figure 3.24(b). After calibration, the optimized coefficients of synthesis filters $F_m(z)$ are listed in Table 3.6.

Table 3.6 Filter coefficients

n	$F_0(z)$	$F_1(z)$	$F_2(z)$	$F_3(z)$
0	0.00448	-0.01497	0.020055	-0.02169
1	-0.00118	0.009622	-0.01855	0.014946
2	0.003713	-0.00697	0.01869	-0.01856
3	-0.00389	0.01809	-0.03423	0.050091
4	0.012694	-0.06048	0.10314	-0.16631
5	-0.00569	0.031808	-0.0577	0.102929
6	0.003525	-0.02341	0.047802	-0.09403
7	-0.01245	0.066512	-0.12005	0.214446
8	0.107781	-0.41476	0.628677	-0.83836
9	0.782867	-1.93656	1.650737	-0.58098
10	0.994587	-1.01989	-1.19989	1.160053
11	1.103542	0.211805	-0.33023	-1.04925
12	0.952235	0.595907	0.451968	0.861627
13	0.296371	-0.08872	-0.27037	-0.60893
14	0.034333	-0.21627	-0.1888	0.47004
15	-0.08349	-0.05243	0.137051	-0.22121
16	-0.11522	0.144345	-0.0235	0.174714
17	-0.0821	-0.08125	0.158179	-0.17839
18	-0.03765	-0.07845	-0.07024	0.181006
19	-0.00027	-0.0084	-0.03668	-0.14074
20	0.041274	0.058328	0.039472	0.141468
21	0.014328	0.011326	-0.01844	-0.06379
22	0.005961	-0.01038	-0.01724	0.035421
23	0.000835	-0.01103	0.011873	-0.01512
24	0.000655	0.002232	-0.0008	0.017647



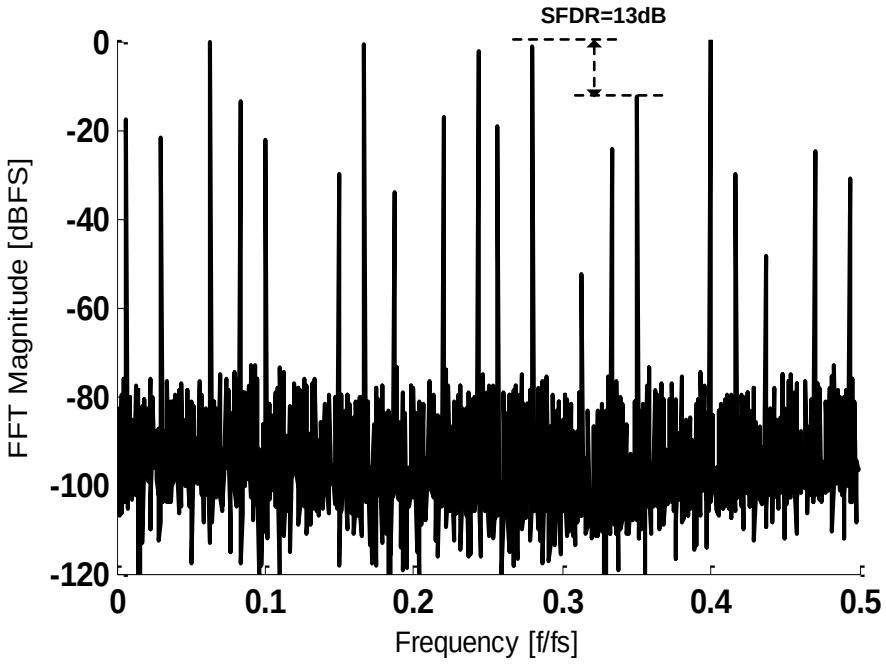
(a)



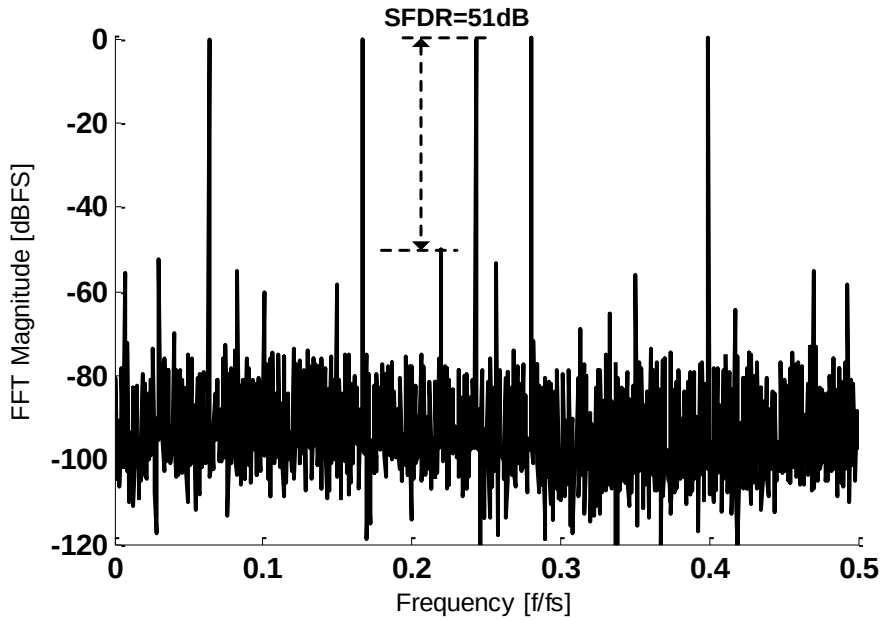
(b)

Figure 3.25 Frequency responses. (a) Initial response before calibration. (b) Response after calibration.

And the corresponding frequency response of $F_m(z)$ before and after calibration are shown in Figure 3.25. To observe the SFDR improvement of proposed calibration technique, giving the input signal $x(t) = \sin(2\pi f_{i1}t+\theta_1)+ \sin(2\pi f_{i2}t+\theta_2)+ \sin(2\pi f_{i3}t+\theta_3)+ \sin(2\pi f_{i4}t+\theta_4) +\sin(2\pi f_{i5}t+\theta_5)$, where $\theta_k=0$ (k=1,2,3,4,5), f_{i1}=635MHz, f_{i2}=1.67GHz, f_{i3}=2.43GHz, f_{i4}=2.80GHz and f_{i5}=3.99GHz, the output results of the system before and after calibration are given in Figure 3.26, which shows that the SFDR of the system is improved from 13dB to 51dB, satisfying the 8-bit ADC requirement.



(a)



(b)

Figure 3.26 The 2048-point FFT of output signal. (a) Before calibration. (b) After calibration.

Table 3.7 Performance Comparison

	Robust design in [76]	Proposed calibration
Mismatch tolerance (σ^2)	0.001	0.01
Filter length	81	25
Aliasing error	-62 dB	-51 dB
Tuning precision (δ)	-	0.002

Finally, the performance comparison with the robust design method in [76] is given in Table 3.7. In the simulation, the range of variation parameter k_m is [0.9 1.1], resulting in an equivalent variance around 0.01.

3.4 Summary

In this section, an efficient calibration method is proposed to compensate the analog analysis filter mismatches and gain mismatches existed in FI-ADCs, which could promote the FI-ADCs as a competitive multi-channel ADC alternative to TI-ADCs. Moreover, the calibration method is independent on number of channels, and the optimization algorithm is suitable for FI-ADCs with more than four channels. Therefore, the proposed calibration technique is extendable to M (M>4) channels FI-ADC.

Chapter 4. DESIGN OF 10-BIT 300MS/S SAR ADC

In this chapter, a 10-bit 300MS/s asynchronous 2b/cycle successive approximation register (SAR) analog-to-digital converter (ADC) is proposed. The interpolation technique is employed to reduce the size of DAC array, relaxing the trade-off between input bandwidth and resolution. The background offset calibration technique is presented after every data conversion to compensate the offset of each comparator. Moreover, a fast SAR control logic is proposed to shorten the delay between comparator outputs to DAC array.

This Chapter is organized as follows. An introduction of the high-speed SAR ADC is given in Section 4.1. Section 4.2 presents the design considerations of 2-bit/cycle SAR ADC. The proposed SAR ADC structure, including SAR algorithm with interpolation and asynchronous timing generation blocks is described in Section 4.3. The detailed circuit implementations are described in Section 4.4. And Section 4.5 shows the measurement results. Finally, the Charter summary is drawn in Section 4.6.

4.1 Introduction

The increasing demand of multimedia and communication is making the design of ADCs facing higher resolution and speed with low power consumption, which is even important for portable instrumentation. The trend of 802.11 standards is for higher bandwidth (80~160MHz for 802.11ac) and higher SNR requirement. As technology scales down, it is possible to design a low power high performance analog-to-digital converter (ADC). It has been proven that successive approximation register (SAR) ADCs is one of the most power efficient architecture [32]-[38]. With the scaling of the advanced technologies, it is possible for SAR ADCs to achieve high speed implementations with high resolution. However, the state-of-the-art high-speed high-

resolution (>=10-bit) single-channel SAR ADCs [5], [39], [82] are approaching the speed limitation, which is around 200MS/s.

For the previous design of 2b/cycle SAR ADC [33], [37], [38], [40], the mainstream of achievable resolution is around 8 bits. In [17], the employed capacitor DAC array for 2b/cycle structure makes the size of total capacitors three times as large as single-bit/cycle DAC array in SAR ADC, which decreases the input bandwidth and increases the power consumption. Using the split capacitor can reduce the switching energy [33], however, it increases the capacitor matching requirement and layout complexity. In the proposed 2b/cycle SAR ADC, asynchronous structure is employed to shorten the conversion time. By using 2-bit interpolation, only 8-bit capacitive DAC array is required. As a result, the proposed SAR ADC can achieve 10-bit 300MS/s with power consumption less than 6mW.

4.2 Design considerations

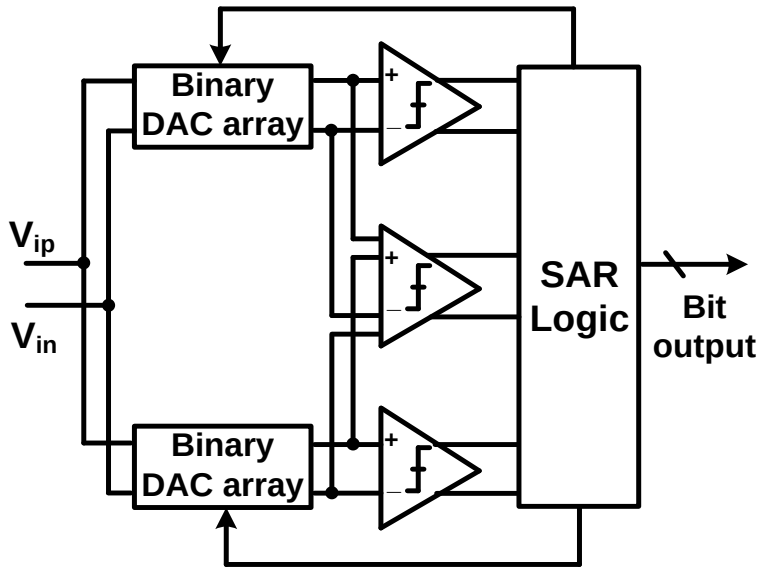


Figure 4.1 Proposed 2b/cycle SAR ADC with binary DAC array.

To design a 10-bit SAR ADC with 300MS/s sampling rate, there is not much headroom to realize using single-bit/cycle SAR ADC structure. Therefore, 2-bit/cycle SAR architecture is employed. However, three 10-bit DAC arrays are required according to the SAR structure in [17]. Actually, in other words, the 2-bit/cycle SAR ADC also can be regarded as 2-bit flash ADC with feedback. And interpolation could be used to reduce the size of DAC array. The block diagram of proposed ADC is presented in Figure 4.1.

To design such a high-speed high-resolution SAR ADC, some key points should be considered. To supply a clear reference voltage, one way is to design a reference buffer with high output bandwidth. And another way is putting a large decoupling capacitor between the positive and negative reference voltage, which can decouple the large ringing caused by bonding wire during switching. Unlike the comparator offset in single-bit/cycle SAR ADCs, which is the system offset not affecting the system linearity. For the 2-bit/cycle SAR ADCs, it usually contains three comparators with different offset voltages, which introduces unexpected spurs. To achieve high speed operation in SAR ADCs, the logic must be optimized to reduce the delay between comparator outputs and DAC array. Although the control logic has been minimized in [39], there is still at least a D flip-flop (DFF) delay in the path from comparator output to DAC array, which limited the sampling rate at 100MS/s.

4.3 Proposed ADC architecture

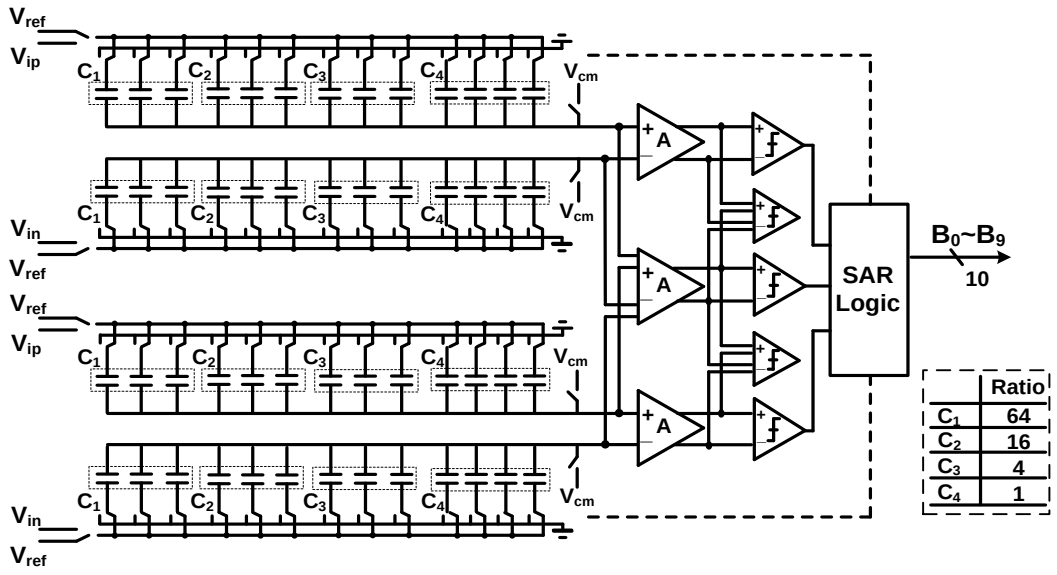


Figure 4.2 Proposed 2b/cycle SAR ADC architecture.

Figure 4.2 shows the proposed 2-bit/cycle architecture, as well as the weights of each capacitor. In addition, asynchronous timing proved in [41] is applied to further reduce the conversion time, avoiding high frequency conversion clock generator. The interpolation is employed between two DAC arrays, which reduce one DAC array compared with [17]. The operational principle of the proposed 2b/cycle SAR ADC is depicted in Figure 4.2. One feature is that the size of DAC array is only 8-bit, which means there are 256 unit capacitors for one DAC array rather than 1024 unit capacitors. The DAC array generates the first 8 bits outputs, the last 2 bits are generated through interpolated comparators following the pre-amplifiers. Totally, the sum of the two DAC arrays is equal to a 9-bit DAC array. All the blocks are fully differential implemented so that they can suppress the common mode noise from input, power supply and ground. To prevent charge injection effect, the bottom plate sampling technique is used. And the bootstrapped switches, which can increase sampling speed and linearity, are applied for

sampling the input signal. Another benefit of using bootstrapped switches is that they can achieve a large input voltage range. In this design, the differential input range is almost twice of voltage supply.

4.3.1 SAR algorithm with interpolation

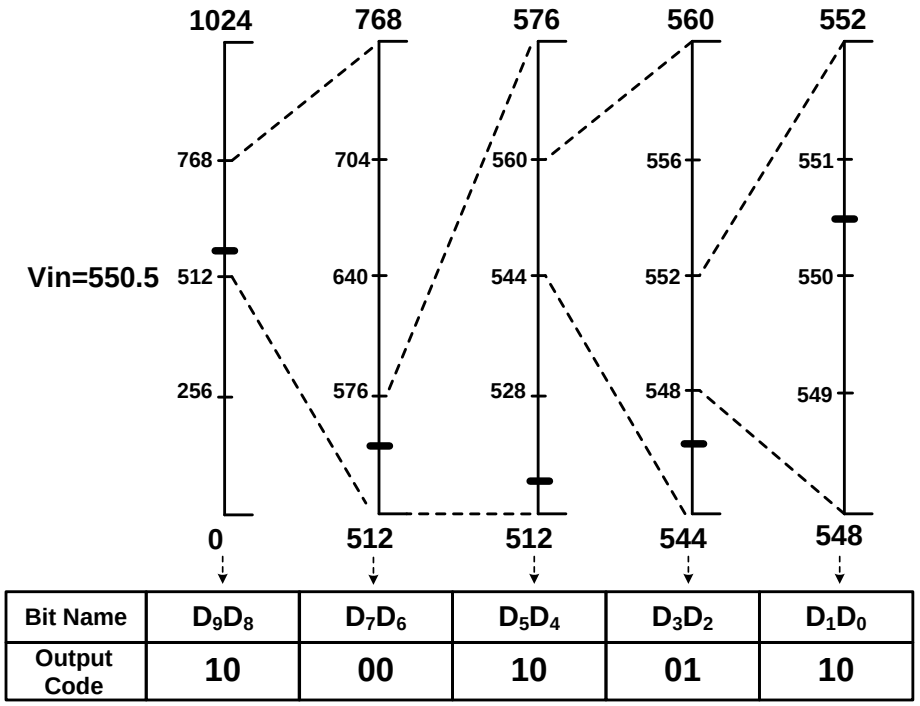
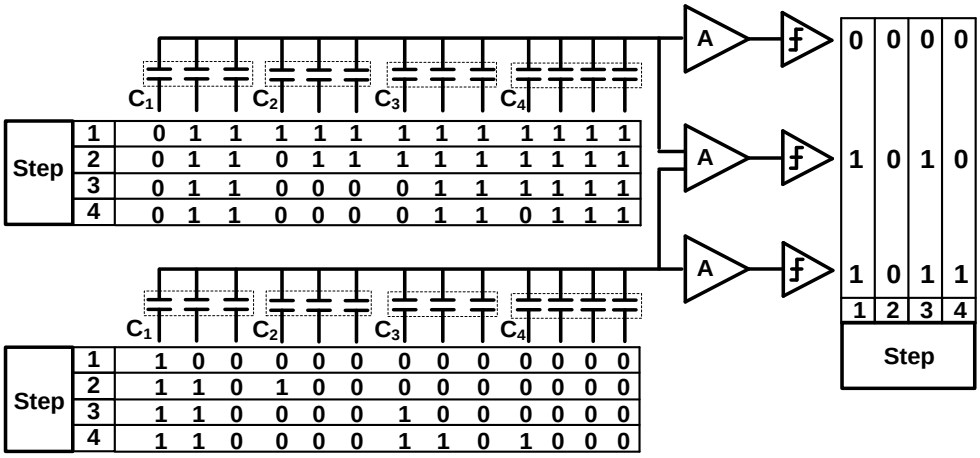
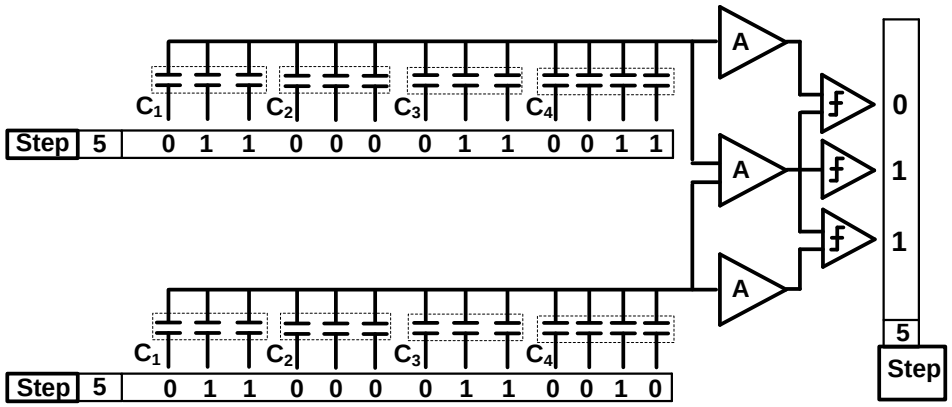


Figure 4.3 Illustration of the 2b/cycle searching algorithm.

In Figure 4.3, the 2-bit/cycle algorithm is explained with input as 550.5 LSBs. And the operation of the first four cycles is shown in Figure 4.4(a). Figure 4.4(b) shows the last two bits generated by interpolated comparators. Different from the 2b/cycle algorithm in [17], which employs three DAC arrays, the switching energy of the DAC array in Figure 4.4 is less.



(a)



(b)

Figure 4.4 Operation of DAC array with input 550.5 LSBs. (a) First four step without interpolation. (b) Last step with interpolation.

4.3.2 Asynchronous conversion

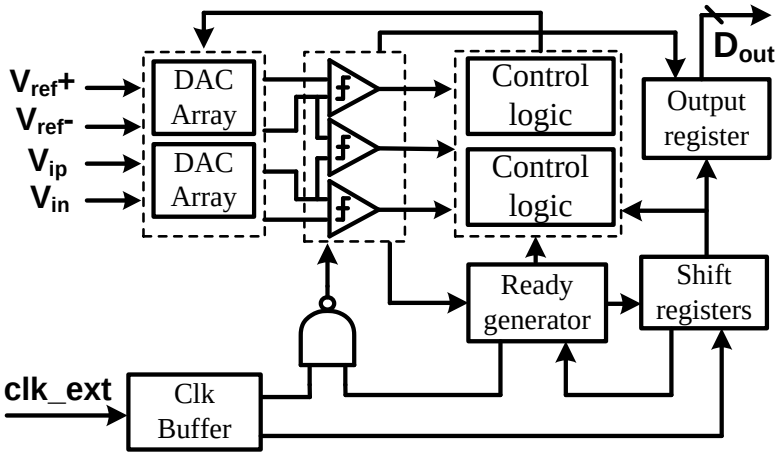


Figure 4.5 Block diagram of asynchronous structure.

It has been proved in [41] that asynchronous processing makes the average conversion time shorter than using synchronous processing, which is suitable for high speed applications. Figure 4.5 illustrates the operation of proposed asynchronous conversion. In essence, the proposed asynchronous processing circuit is a positive feedback loop. In Figure 4.5, when the enable signal clk_i generated from clock generator is '1', the comparators are waked up ('clk_c'=1) from reset state ('clk_c'=0), conducting the first time comparison. When the comparators generate the results, at the same time, the ready signal generator output a '0' (rdn='0') to indicate finish of comparison. If the meta-stability occurs, which means the 'rdn' equals '1' lasts a long time, the 'time_out' block that is a meta-stability detector, will generate an alternative signal to make the loop continue to work. Additionally, by insert a variable delay line, the delay of the loop can be adjusted to meet the settling time requirement.

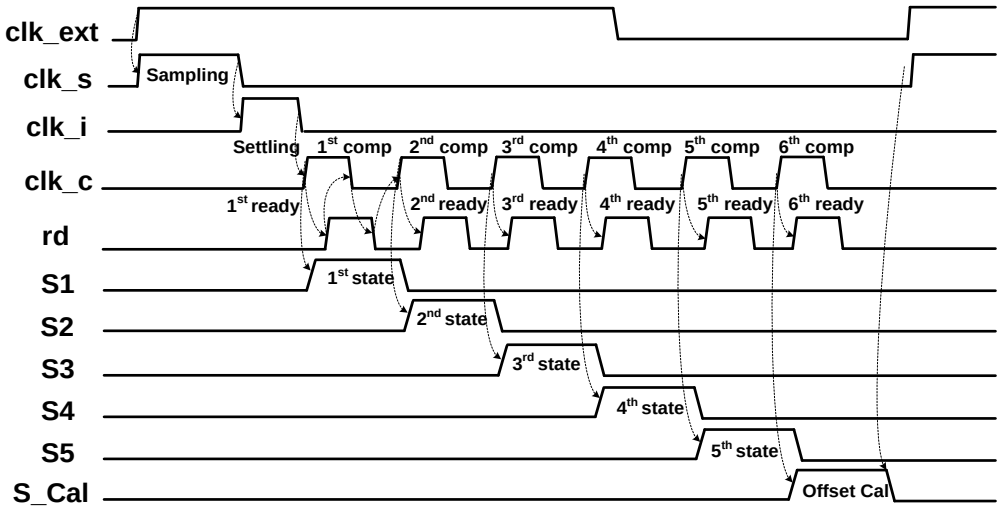


Figure 4.6 Asynchronous timing diagram, including sampling phase, conversion phase and calibration phase.

The asynchronous timing is figured in Figure 4.6, consisting of sampling phase, conversion phase and offset calibration phase. The pulse duration of signal 'clk_s' is created by inverter chain delay, which is allocated to sampling phase. The falling edge of 'clk_s' triggers the first comparison. After five asynchronous conversions, all the comparators calibrate the offset separately. And the time occupied by calibration phase equals roughly one conversion.

4.4 Building blocks

4.4.1 Comparator

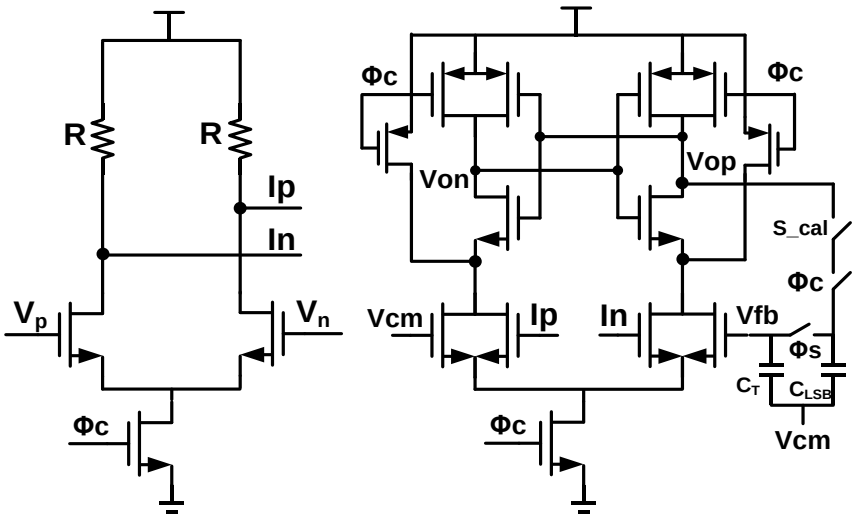


Figure 4.7 Schematic of pre-amplifier and comparator.

The schematic of dynamic comparator is shown in Figure 4.7. When ϕ_c is low, the comparator is in reset phase. And comparator is in conversion phase when ϕ_c is low. The pre-amplifier is placed prior to comparator to suppress the effect of kick back noise on floating gate during the conversion phase. The offset calibration is realized by placing an auxiliary differential pair with the gate voltage of one fixed and the other one adjusted by negative feedback loop. To decouple the switching caused wave on the 'Vcm', which is generated by comparison switching, the bottom plate is connected to 'Vcm'. Additionally, a latch follows the *Vop* and *Von* to store the results of comparison. The calibration phase is placed following the last comparison cycle, which is illustrated in Figure 4.6.

4.4.2 Shift register and control logics

Unlike the traditional SAR logic [39], which always contains a comparable delay between comparator output and DAC array, the proposed control logic eliminates the

delay of DFF and the equivalent delay just equals to transmission delay of several inverters. Since asynchronous timing is employed in this design, and the settling of DAC array before each conversion is triggered by *rdn* signal. The proposed control logic is a state machine based shift register, which selects the corresponding unit capacitors before the *rdn* signals coming during every conversion. In this way, the delay from comparator output to DAC array just equals to the delay of two or three transmission gates. Figure 4.8 presents the state machine based shift register. And the schematic of DAC control logic is shown in Figure 4.9.

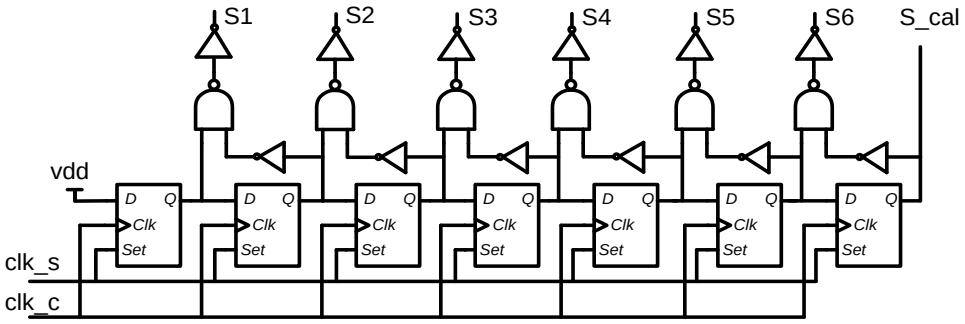


Figure 4.8 Schematic of state machine based shift register.

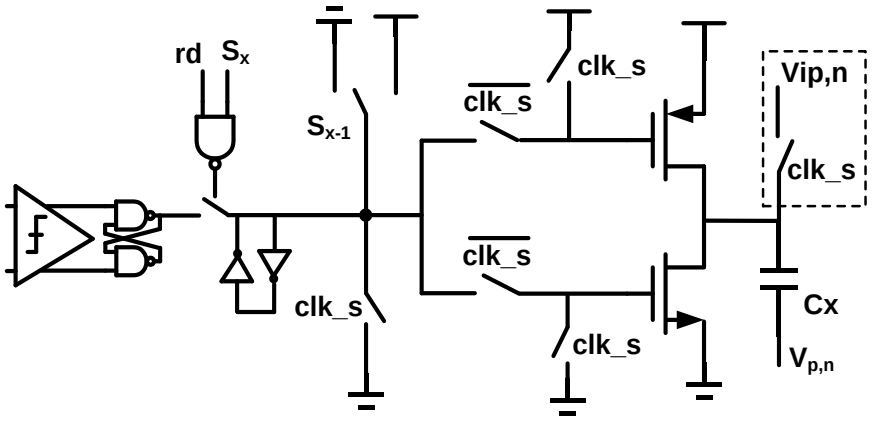


Figure 4.9 Schematic of control logic for DAC array.

4.4.3 DAC array

Figure 4.10 shows the floor plan of capacitor DAC array in which the size of unit capacitor is 1.2fF, which is comparable with unit capacitor in [42]. According to [42], the variation should satisfy

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u} LSB$$
$$\sigma_{INL,MAX} = \sqrt{2^{N-1}}\frac{\sigma_u}{C_u} LSB \quad (4.1)$$

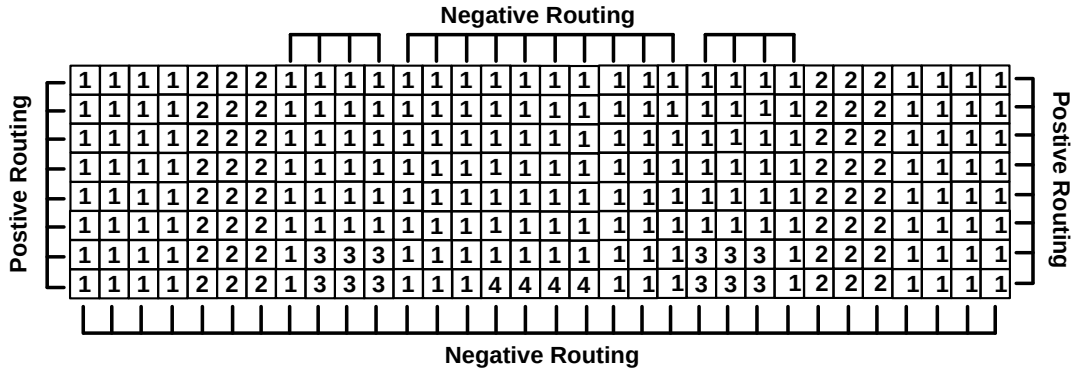


Figure 4.10 Floor plan of the capacitive DAC array.

And with a 1.2fF unit capacitor, of which the size is 1μm^2, the mismatch can be tolerated is 0.1%. The structure of unit capacitor is drawn in Figure 4.11. The positive terminal is connected horizontally and the negative terminal is connected vertically.

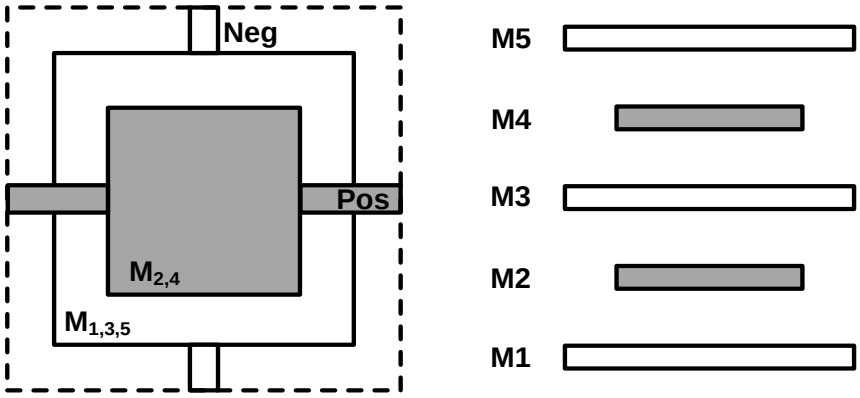


Figure 4.11 Structure of unit capacitor.

Unlike the previous placement of unit capacitors [5], for which the extra wiring are necessary for different unit capacitor groups, introducing unexpected parasitic capacitors between positive and negative of DAC array. In [42], the unit capacitors are placed in one line, suffering from more serious gradient effect horizontally. Since the small unit capacitor is used, the routing the DAC array should be placed very carefully.

4.4.5 Sample switches

It can be seen in Figure 4.12 that the bottom plate sampling is applied in this design. And a bootstrapped switch [43] with multiple outputs is needed. Figure 4.12 shows the schematic of bootstrapped switch. A potential issue is that the bandwidth mismatch may degrade the linearity of the sampled signal. However, by benefiting from advanced CMOS process with large transition frequency f_T and careful layout, the bandwidth mismatch can be ignored.

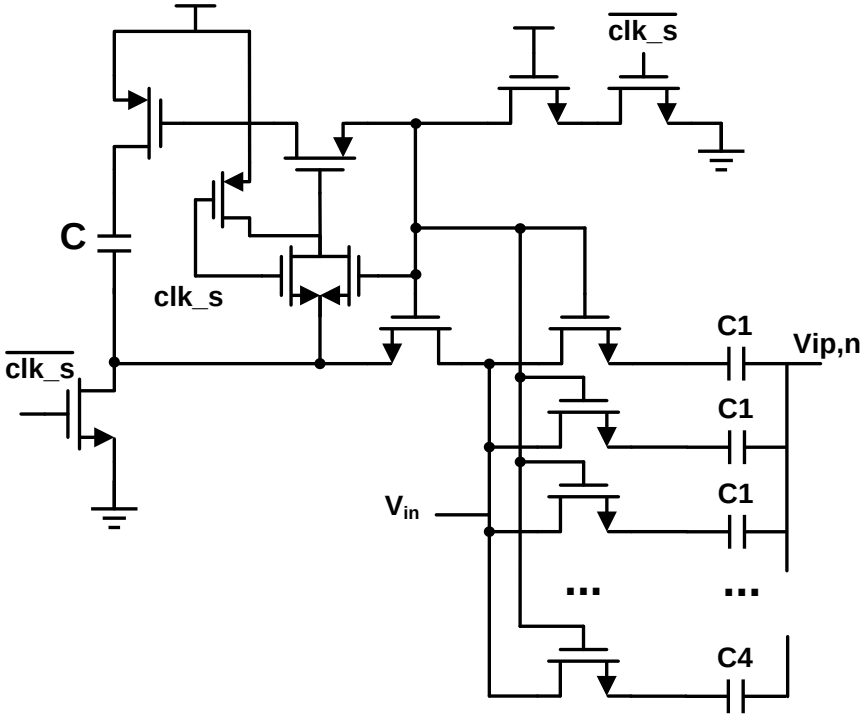
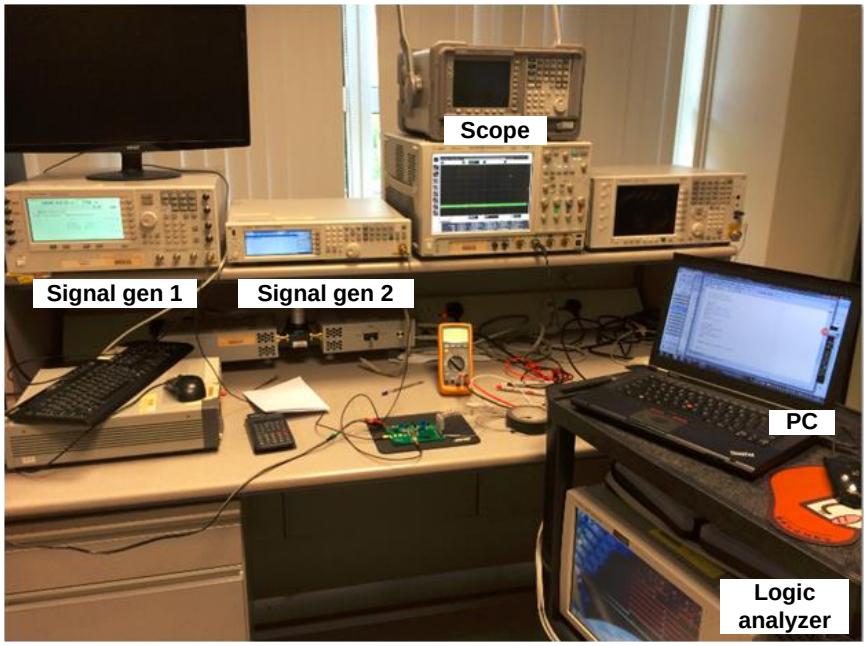


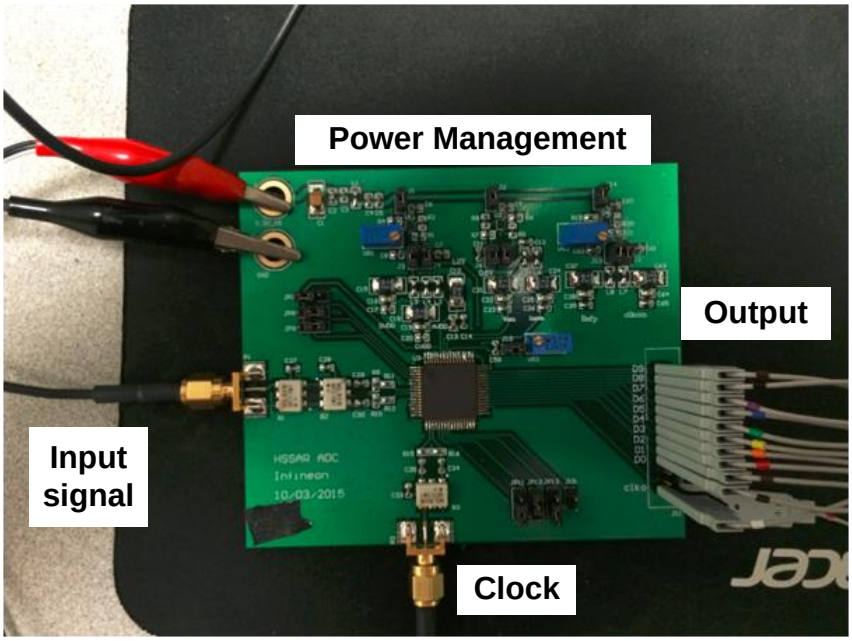
Figure 4.12 Schematic of bootstrapped switch.

4.5 Measurement results

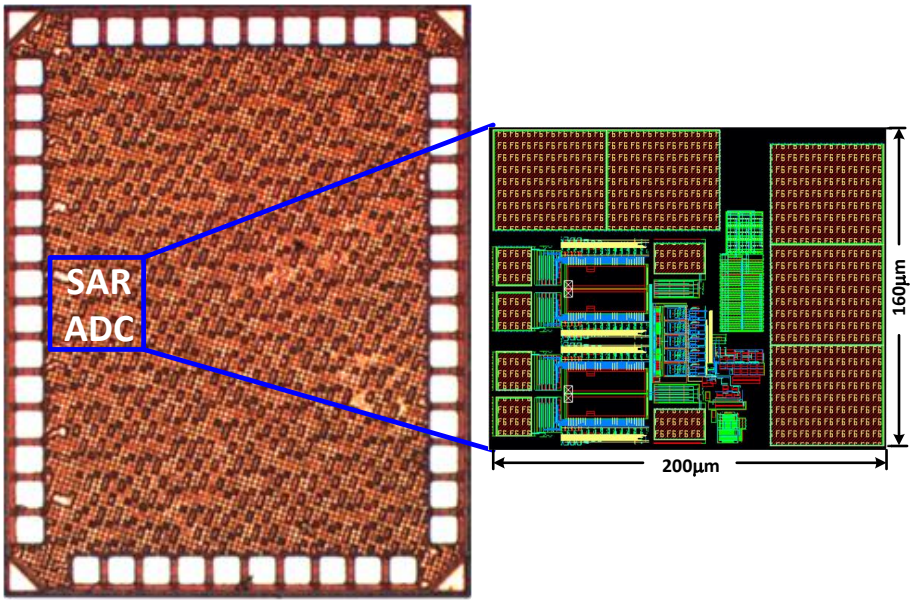
The ADC chip is fabricated in 40nm CMOS low power technology. The testing setup is shown in Figure 4.13 (a). Two RF signal generator are required for clock and input signal generation, respectively. The testing board is shown in Figure 4.13 (b). The die photo and layout are shown in Figure 4.13 (c), and ADC core occupied 160 x 200μm^2. The performance is measured at 1.2V power supply and normal temperature. The measured peak differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Figure 4.14. The peak DNL and INL are -1.0/2.1 and -1.9/2.3 respectively. It could be concluded from the DNL plot that the settling of MSB comparison is incomplete. Therefore, the peak values of DNL are located at code 1011111111 (767) and 0100000000 (256).


Scope
Signal gen 1
Signal gen 2
PC
Logic analyzer

(a)


Power Management
Output
Input signal
Clock

(b)



(c)

Figure 4.13 (a) Testing setup. (b) Testing board. (c) Die photo and layout.

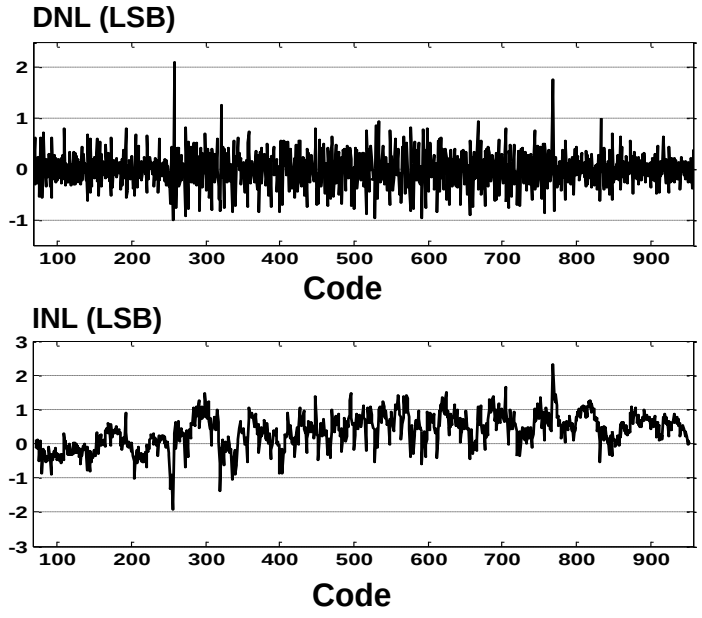


Figure 4.14 Measurement results of DNL and INL.

The digital output is decimated by a factor 8. All the dynamic performance testing is conducted with -1dBFS input. At a 300MHz sampling frequency, Figure 4.14 shows the measured SFDR and SNDR at 4.5MHz input are 62dB and 53.5dB, respectively. The

measured SFDR and SNDR at 147MHz shown in Figure 4.15 are 59dB and 51.5dB respectively. The corresponding effective number of bit (ENOB) is 8.3 bits at Nyquist input. The SFDR and SNDR versus input frequency is shown in Figure 4.16. It can be seen in Fig. 16 that the effective resolution bandwidth (ERBW) is up to 360MHz. Figure 4.17 illustrates the measured SFDR and SNDR versus sampling frequency at 15MHz input.

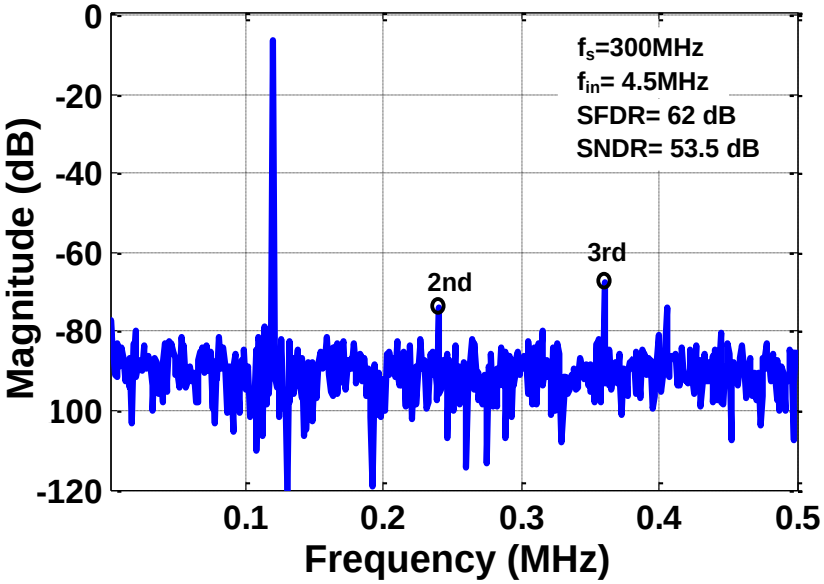


Figure 4.15 Measured SFDR and SNDR (digital output is decimated by 8) with f_{in}=4.5MHz.

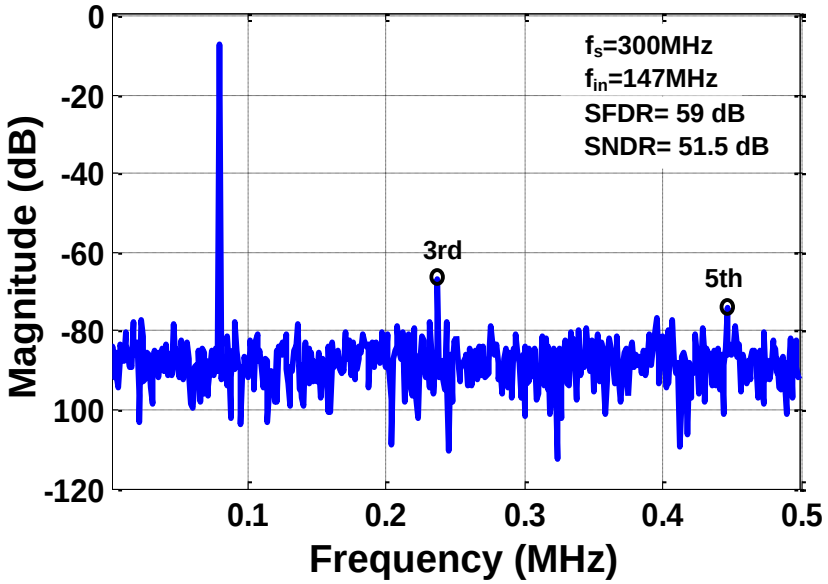


Figure 4.16 Measured SFDR and SNDR (digital output is decimated by 8) with f_{in}=147MHz.

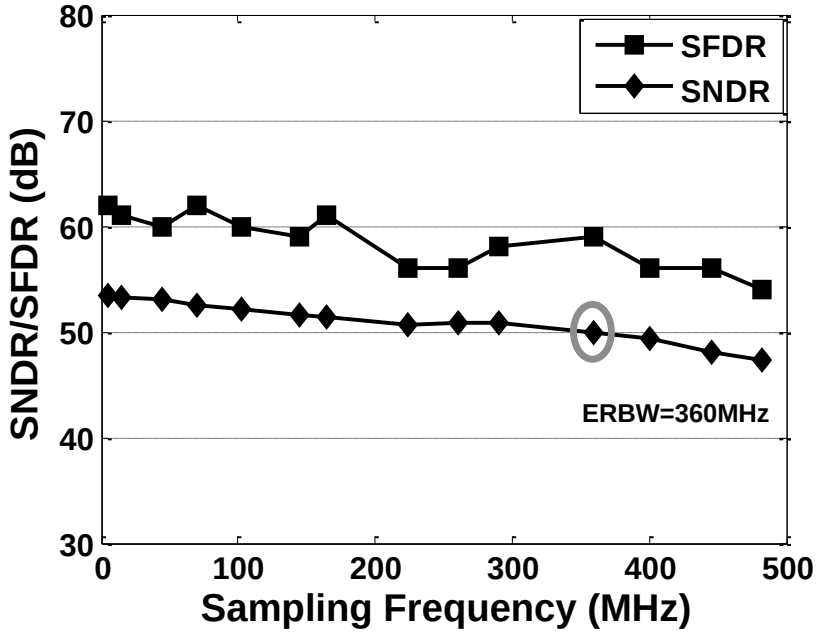


Figure 4.17 SFDR and SNDR versus input frequency at f_s=300MHz and V_{dd}=1.2V.

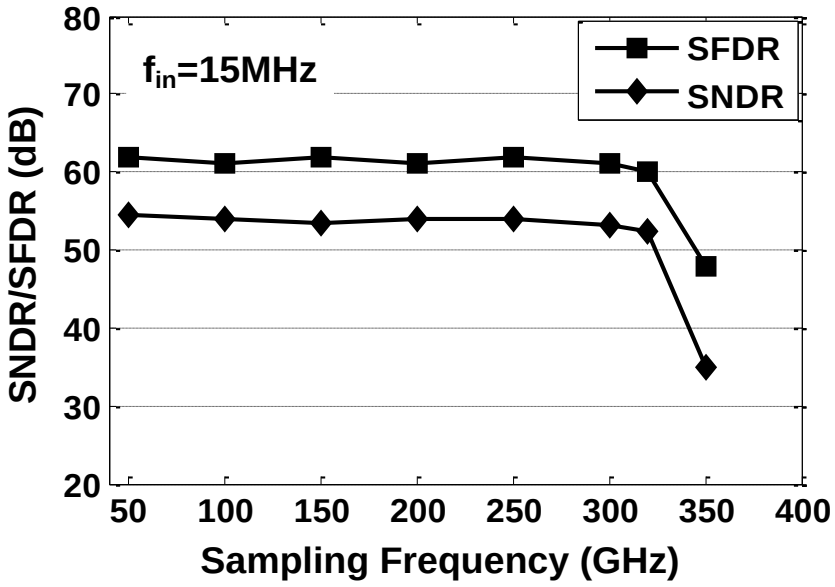


Figure 4.18 SFDR and SNDR versus sampling frequency at f_{in}=15MHz and V_{dd}=1.2V.

The performance summary is listed in Table 4.1. The power consumption of the ADC core is 5.8mW. Since the size of unit capacitor utilized in this work is only 1.2fF, the power contribution is limited. The proposed ADC achieves a FoM value of 61fJ/conversion-step and smaller ADC core size of 0.032mm^2. The performance comparison with the state-of-the-art ADCs up to 300MS/s is listed in Table 4.2. Compared with single-channel SAR ADC [5], the comparator and digital logic consumes more power due to the parallel conversion, which is similar to flash-ADCs.

Table 4.1 Performance Summary

Technology	40nm LP CMOS
Supply Voltage (V)	1.2
Input Common Mode (V_{cm})	0.6
Differential Input Range (V_{p-p})	2.4
Input Capacitive Load (pF)	0.6
Sampling Rate (MS/s)	300

Active Area (mm^2)		0.032
DNL		-1.0/2.1
INL		-1.9/2.2
SFDR(dB) @Nyquist-freq		59
SNDR(dB) @Nyquist-freq		51.5
ENOB		8.3
Power	Preamp+Comparator	2.5mW
	DAC array	0.3mW
	Digital logic	3mW
	Total	5.8mW
Figure of Merit (fJ/conv-step)		61

Table 4.2 Comparison of state-of-the-art works up to 300MS/s

	JSSC 2010 [39]	ISSCC 2010 [5]	JSSC 2015 [82]	ISSCC 2012 [45]	JSSC 2012 [46]	JSSC 2013 [47]	**This Work**
Amplifier Architecture	SAR	SAR	SAR	Pipeline	Pipeline	Pipeline	**SAR**
Technology (nm)	90	65	28	65	90	65	**40**
Supply voltage (V)	1.2	1.2	1.0	1	-	1	**1.2**
Power (mW)	3	1.13	0.68	5.37	40	26.6	**5.8**
Sampling Rate (MS/s)	100	100	240	200	320	300	**300**
Resolution	10	10	10	10	10	10	**10**
DNL(LSB)	+0.79/-0.27	+0.58/-0.53	+0.5/-0.5	+0.08/-0.38	+0.7/-0.6	+0.52/-0.4	+2.1/-1.0
INL(LSB)	+0.86/-0.78	+0.69/-0.61	+1.0/-1.0	+1.36/-1.29	+0.8/-0.9	+0.99/-1.65	+2.2/-1.9
SNDR(dB) **@Nyquist freq**	53.5	56	53.6	55	51.2	52.9	**51.5**
ENOB (bit) @Nyquist freq	8.6	9.0	8.6	8.8	8.2	8.5	**8.3**
FOM (fJ/conv-step)	77	22	7.8	59	396	245	**61**
Area (mm^2)	0.09	0.026	0.003	0.19	0.46	0.36	**0.032**

4.6 Summary

A test chip of a single channel 10-bit 2b/cycle SAR ADC with sampling rate of 300MS/s, which extends the speed limitation of SAR ADC, is proposed. The proposed redundancy algorithm of 2b/cycle structure improves the error tolerance capability for conversions and reference settling. Additionally, to further reduce the conversion time, a state machine based shift register structure is introduced to the proposed SAR ADC. Benefiting from advanced technology and special layout, the value of unit capacitor can be reduced to 1.2fF without affecting the system linearity. The offset existed in comparators are calibrated in the background through feedback loop, which will not influent regular conversion of the ADC. Different from traditional SAR ADC, the power consumption of DAC array is only 0.5mW and the digital logic costs 3mW, which is dominant in the total power consumption and can be further decreased by optimized the dynamic logics.

Chapter 5. DESIGN OF A 1GS/S 10-BIT TIME-INTERLEAVED SAR ADC

In this Chapter, a 10-bit 1GS/s 4-way time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC) is proposed. Each channel exploits a 250MS/s SAR ADC with high speed non-binary searching approximation that allows the conversion to obtain settling error tolerance. The non-binary DAC associated with adders based encoding circuit are custom designed, which eliminates multiplier based encoding logic and thus, simplifies the digital circuitry and reduces the digital power. To suppress the time skew among the TI SAR ADC, the sampling instant of the sub-ADC channels are synchronized to the full rate master clock, which reduces the time skew spurs below -52 dB at Nyquist input. Moreover, based on the fully digital time skew calibration technique in Section 3.2.2, an improved digital background time skew calibration technique with interpolation FIR filters is proposed, which further suppresses the timing mismatch spurs to be less than -70dB. The prototype was fabricated in a 65nm CMOS technology. The measurement results show that the ADC achieves a SNDR of 49.6dB and with a figure of merit (FoM) of 37fJ/conversion-step when operating at 1GS/s and 458.1MHz Nyquist input. The ADC core achieves a small area of 0.03mm^2.

This Chapter is organized as follows. An introduction of the time-interleaved SAR ADC is given in Section 5.1. Section 5.2 introduces the proposed TI SAR ADC architecture, including the sampling scheme, non-binary high speed SAR sub-ADC and the proposed digital background time skew calibration technique. The detailed circuit implementations are described in Section 5.3. Section 5.4 shows the measurement results. Finally, the conclusion is drawn in Section 5.5.

5.1 Introduction

The aggressive scaling CMOS technology has fuelled the emergence of high performance analog-to-digital converters (ADCs) with lower power consumption and smaller silicon area [32]-[38]. The power and area efficient high-speed high-resolution ADCs, instead of traditional power hungry ADCs [48]-[50], facilitate software defined radio (SDR) and wideband communication implementations. Besides, portable testing instruments (e.g., portable oscilloscopes, spectrum analyzers) could be further developed by leveraging such low power high performance ADC solutions.

Since the residue amplification and buffering operations rely on high performance operational amplifier design, which requires large intrinsic device gain and high power supply, pipelined ADCs are facing design challenges in technology scaling (e.g. 65nm, 40nm, 28nm). It is known that pipelined ADCs are suitable for high resolution and high speed sampling at gigahertz frequencies [6], [51], [52]. However, to achieve low power consumption, power efficient amplifiers are needed. Some techniques have been published [14], [53] to overcome the design challenges (low intrinsic device gain and low power supply). However, the calibrations for offset, gain and linearity of operational amplifier will introduce complicated circuits that consumes considerable silicon area and power consumption [53]. Due to the lessened requirement of residue amplification for two-step pipelined ADCs, they could achieve high resolution high speed and low power consumption with necessary calibrations [51]. Nowadays, the two-step pipeline ADCs could lead the trend of low power pipelined ADCs design [51], [54].

SAR ADCs are power and area efficient [32]-[38]. However, the sampling rates of prior high speed SAR ADCs [5], [32] are limited to be around 100MS/s, due to the serial comparison characteristic and accuracy requirement for each comparison cycle. To achieve high sampling rate with SAR architecture, time-interleaved (TI) SAR ADCs are

presented in previous publications [23], [28], [37], [48]-[50]. The sampling rate increases proportionally with the number of sub-channels. However, the mismatches of offset, gain, time skew and bandwidth between sub-channels cause the non-linearity. In spite of the reported low power designs on high speed high resolution TI SAR ADCs [28], [37], the power consumption and silicon area overhead in terms of time skew calibration and clock distribution, however, are comparable with that of sub-channel. The power consumption of 24-way TI SAR ADC in [55] was reduced as compared with traditional TI ADCs [49], [50]. However, the time-interleaving overhead is still considerable, including those of time skew calibration and clock distribution. Another 8-way TI SAR ADC in [28] consumes large area of 0.78mm^2 with off-chip timing calibration, with one flash ADC and eight identical SAR ADCs sampling at 125MS/s.

In this section, we present a 1GS/s 10-bit four-channel time-interleaved SAR ADC. The 4×TI SAR ADC consumes only 7.8mW power and 0.03mm^2 core area, resulting in a FoM of 37fJ/conversion-step at Nyquist input. To reduce the time skews, a time skew suppressed sampling technique with full rate clock for TI ADCs is presented, which facilitates the clock distribution and reduces hardware overhead. Additionally, this work implements an adders based non-binary encoding scheme in sub-channel SAR ADC for high speed conversion. The solution provides maximum 25% and 4% error tolerance range during the MSBs and the LSBs conversion, respectively, which speeds up the conversion to 250MS/s in each sub-SAR ADC with 10-bit resolution. To further compensate the time skew, a low computational short-tap FIR correction filter is designed, along with low accurate interpolation FIR filters, to calibrate the time skew spurs to be lower than -70dB.

5.2 Proposed TI SAR ADC architecture

As mentioned above, power and area efficient TI SAR ADCs, which are the popular candidates for low power high speed ADC designs, were proposed in numerous prior works [28], [49], [50], [55]. To reduce the hardware overhead of time-interleaved ADCs, this work presents power and area efficient high speed SAR sub-ADCs, facilitating the clock routing and distribution. Also, a time skew suppressed sampling technique is presented, which makes only the full rate sampling clock jitter sensitive. Further, an off-chip digital background time skew calibration technique with interpolation FIR filters is introduced.

5.2.1 Sampling network

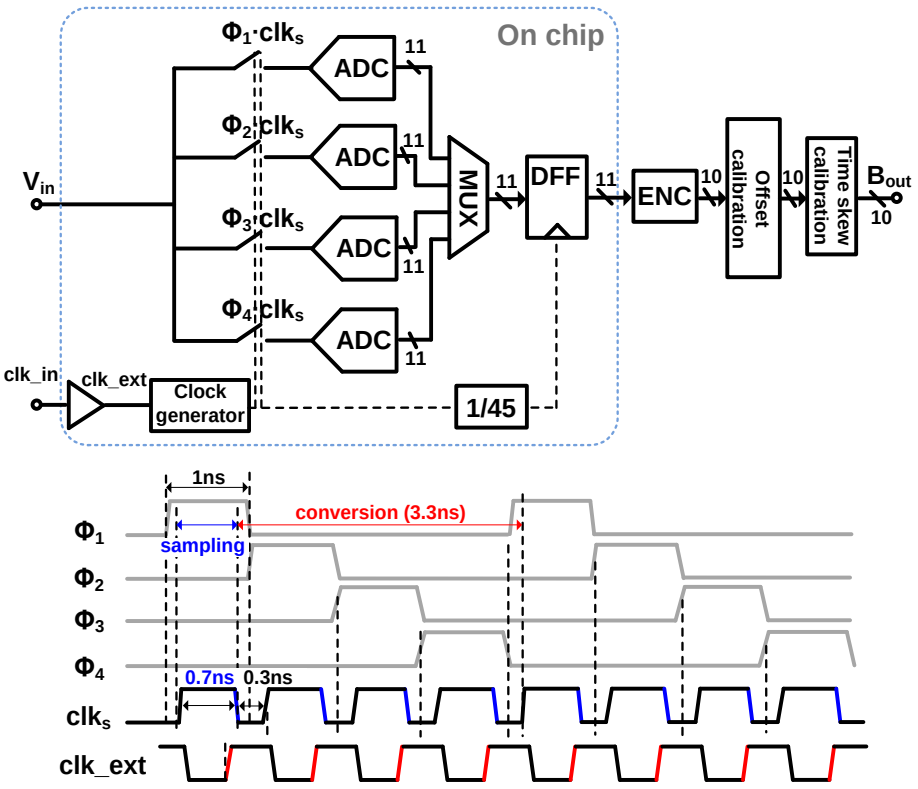


Figure 5.1 Proposed architecture of the four-channel TI-ADC with sampling rate of 1GS/s.

The overall ADC architecture is shown in Figure 5.1, which consists of four TI sub-SAR ADCs operating at 250MS/s with total 1GS/s. To reduce the time skew, the sampling instant of each channel is only determined by the falling edge of the 1GS/s master clock clk_s, while the corresponding TI clock signals Φ_i (i=1, 2, 3, 4) are used to perform the channel selection [51]. The sampling switches in the TI channels are bootstrapped, where the symmetrical routing of the clk_s to the bootstrapped terminals is considered. According to the measurement results, the spurs due to time skew are suppressed below 52dB at Nyquist input. After multiplexing, the digital outputs are decimated by a factor of 45 for testing purpose. And the selection of decimation factor should equal $N \cdot M+1$, of which the N is an integer and the M is the number of channels. One bit redundancy is implemented for the proposed non-binary searching scheme. The decimated outputs of ADC are followed by an encoding circuit (ENC) to encode the outputs from 11b to 10b. The offset errors are extracted by average and accumulation in digital domain [48].

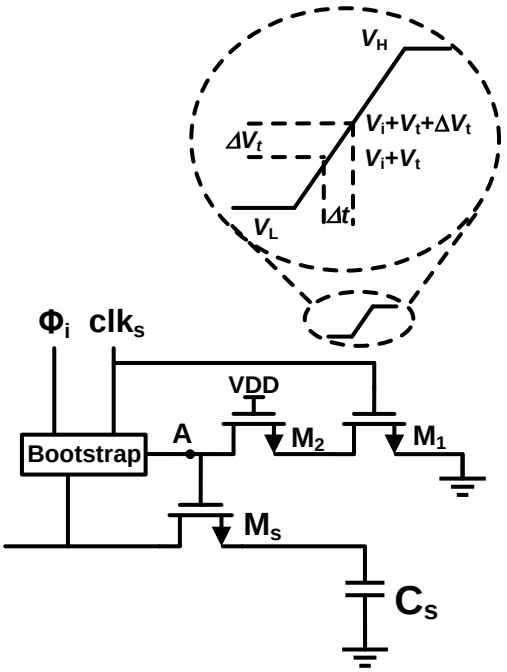


Figure 5.2 Effect of threshold mismatch on time skew.

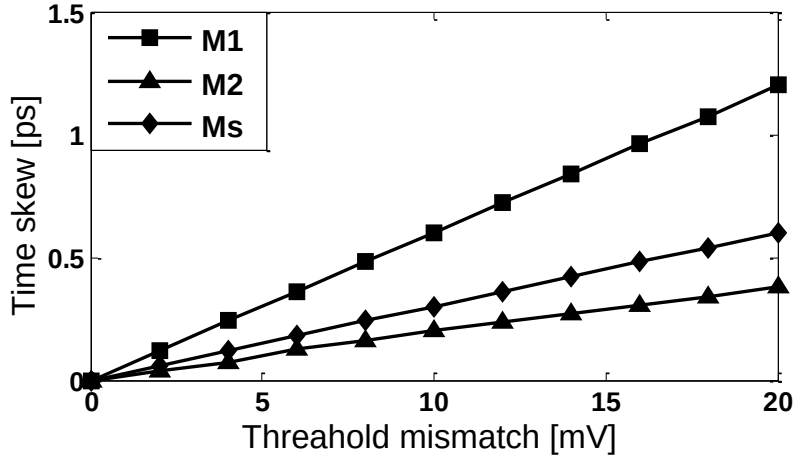
Although every channel is sampled by the master clock signal clk_s, there are still some time skew error sources, including threshold mismatch of the sampling switches (transistor M_1, M_2, Ms) and unmatched layout after fabrication. The effect of threshold mismatch of transistor M_1 is explained in Figure 5.2. The time skew Δt can be derived as

$$\Delta t = \frac{t_{fall}}{V_H - V_L} \Delta V_t , \tag{5.1}$$

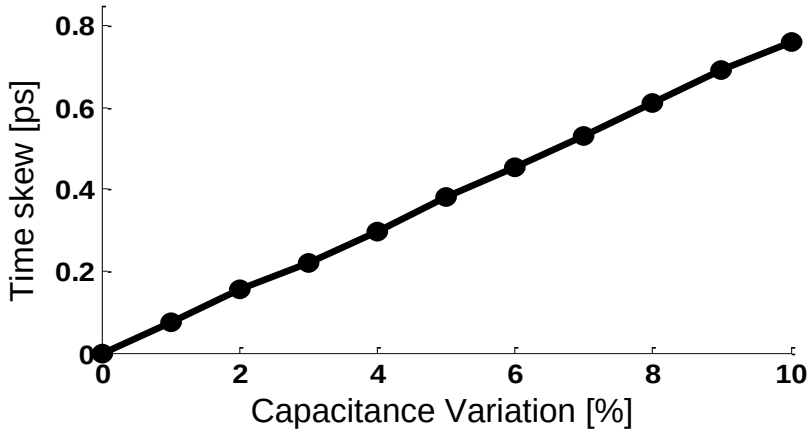
where t_{fall} is the falling time of clock. From (5.1), it can be concluded that making the falling edge sharper and reducing threshold mismatch ΔV_t of transistor M_1 could decrease the time skew. To reduce threshold mismatch of sampling switches (transistor M_1, M_2, Ms) shown in Figure 5.2, the size of sampling switch could be increased properly according to [56], which states that the standard deviation of threshold mismatch is

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} , \tag{5.2}$$

where A_{Vt} is the matching constant. To simulate the effect of process variation on time skew, we set the falling time of clk_s as 70ps, the size of M_1 and M_2 as 4μm/60nm and the size of the Ms as 15μm/60nm.



(a)



(b)

Figure 5.3 The relation between time skew and (a) offset of transistors M1, M2 and Ms (b) capacitance variation at node A.

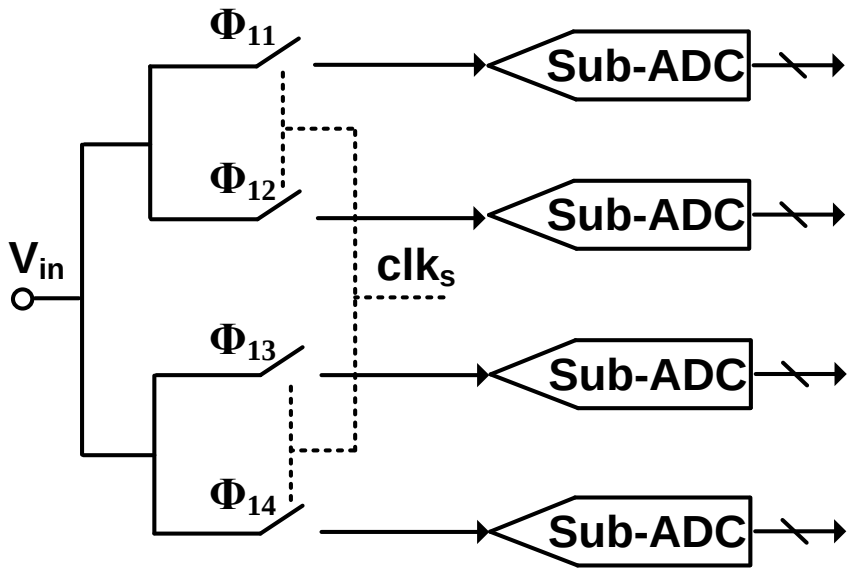


Figure 5.4 Layout illustration of input and clock signal for a four-channel TI ADC.

The simulation results of threshold mismatch and capacitance mismatch at node A (Figure 5.2) versus time skew are illustrated in Figure 5.3. To suppress the error caused by unmatched layout, the layout of clock signal clk_s and input signal V_{in} are illustrated in Figure 5.4, where it utilizes "binary tree" connection to guarantee the routings of input and clock signal to each channel identical. Compared with the identical routing in [26], the "binary tree" routing is comparatively symmetric. Assuming that the time skew error is treated as Gaussian distributed variable, the relation between SNDR and time skew standard deviation σ_t with given input frequency f_{in} is [57]

$$SNDR = 20\log\frac{1}{2\pi f_{in}\sigma_t} - 10\log(1-\frac{1}{M}), \tag{5.3}$$

where M is the number of interleaved channels. To satisfy an SNDR of 60dB at a 500MHz input frequency, the time skew deviation σ_t between channels should be less than 0.28ps, which is difficult to achieve without additional calibration even after necessary matching.

5.2.2 Non-binary high speed SAR ADC

To design a 10-bit SAR ADC with 250MS/s sampling rate, there is not much headroom for improvement by using conventional binary SAR ADC structure, which requires ten conversion cycles with each cycle satisfying the same accuracy as

$$V_{\text{ref}} \cdot e^{-t/\tau} < V_{\text{ref}} / 2^{M}, \tag{5.4}$$

where M is the resolution of the ADC. τ is RC time constant of the settling switch resistor and capacitor to be charged. It means the settling time required for 10-bit resolution is

$$t_{settling} > 6.9\tau. \tag{5.5}$$

Otherwise, the comparison error occurs. With the presence of custom designed non-binary DAC, the accuracy requirements for the MSBs are significantly relieved. Taking a 4% redundancy range as an example, the required settling time for each cycle is

$$V_{\text{ref}} \cdot e^{-t/\tau} < 4\% \cdot V_{\text{ref}} \Rightarrow t_{\text{settling}} > 3.2\tau \tag{5.6}$$

Therefore, the settling time allocated to DAC settling could be shorter. Additionally, the redundancy algorithm also can cover the error caused by incomplete reference voltage settling in the conversion phase.

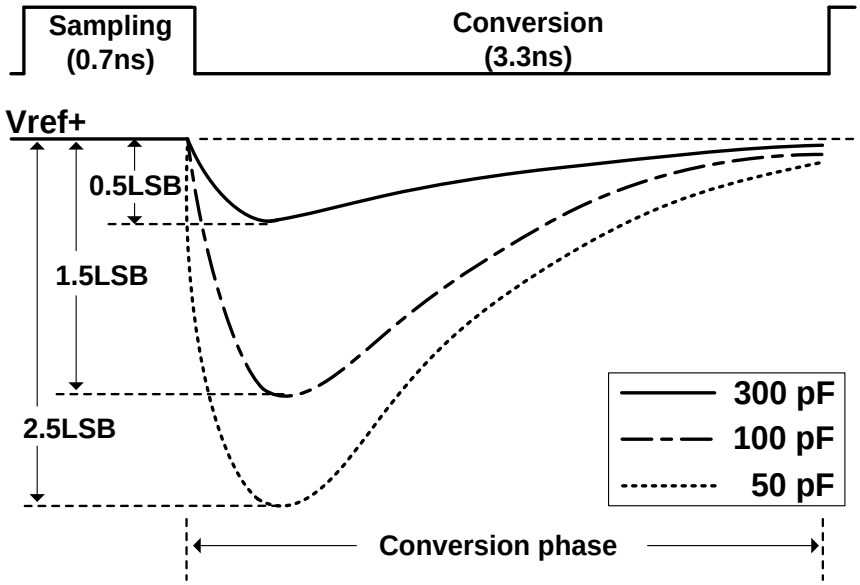


Figure 5.5 Illustration of reference voltage settling in conversion phase with different sizes of decoupling capacitors.

For a DAC array with 0.25pF capacitance and conversion time of 3.3ns, it can be seen in Figure 5.5 that to satisfy the precision requirement of reference voltage settling, the decoupling capacitance between positive and negative of reference voltage should be around 300pF. With the presence of non-binary successive approximation, the size of decoupling capacitor could be much reduced.

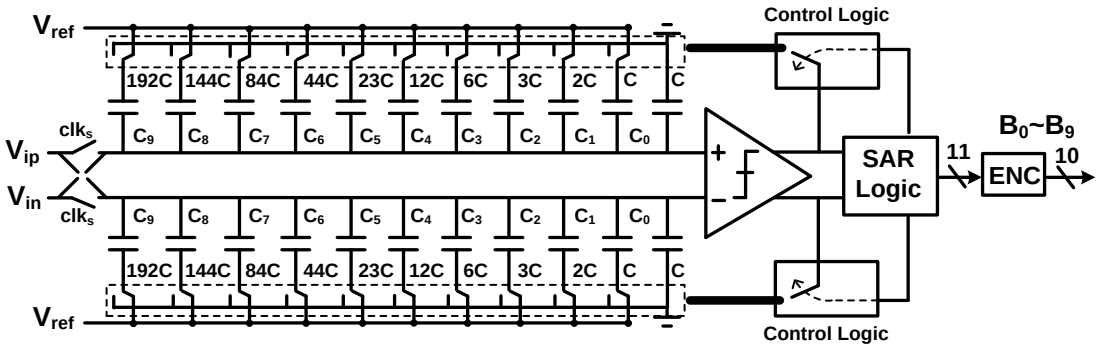
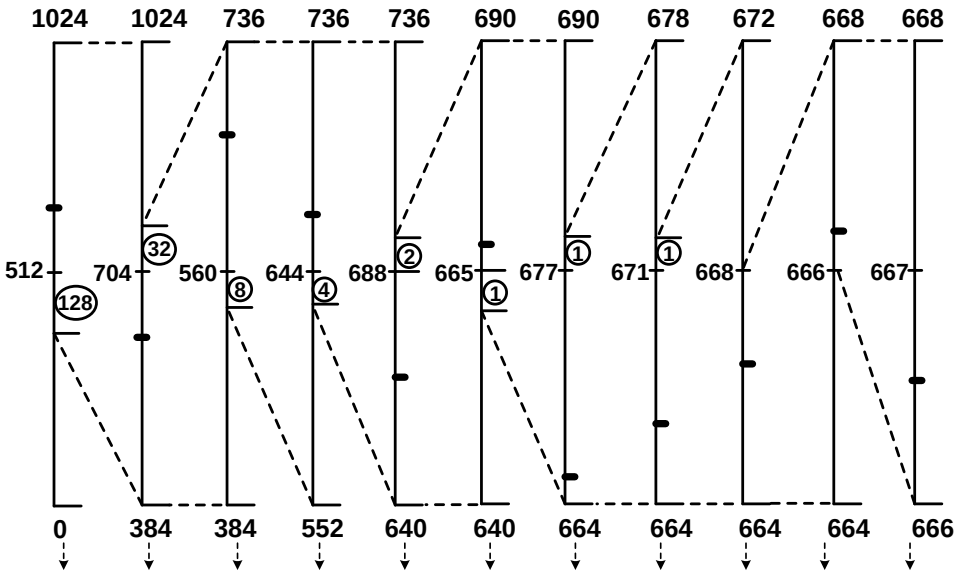


Figure 5.6 Proposed non-binary single-channel SAR ADC architecture.

Complex arithmetical units based non-binary algorithm has been discussed in [58], [59], which could not satisfy high speed implementations due to the delay of algorithm computation units. In this design, the non-binary threshold voltage generations are embedded into DAC array directly, resulting in high speed SAR operations without extra delay and additional unit capacitors [5], [37]. The architecture of the non-binary SAR ADC is shown in Figure 5.6, and 11 conversion cycles are needed with one bit redundancy. The non-binary weights D_{10}~D_0 are

$$\begin{aligned} D_{10} &= 2^9 - R_1 \\ D_9 &= 2^8 + \frac{R_1}{2} - R_2 \\ &\cdots\cdots \\ D_0 &= 2^{-1} + \frac{R_1}{2^{10}} + \frac{R_2}{2^9} + \ldots + \frac{R_{10}}{2} - R_{11} \end{aligned} \quad (5.7)$$

The numbers of redundant LSB R_i (i=1, 2, …11) for each cycle are 128, 32, 8, 4, 2, 1, 1, 1, 0, 0, 0. The corresponding bit weights of the non-binary DAC array D_{10}~D_0 are 384, 288, 168, 88, 46, 24, 12, 6, 4, 2, 1. To cover the error caused by incomplete reference voltage settling, the redundancy values of first two MSB comparisons are set as 25% (128 LSB) and 10% (32 LSB), respectively. And the redundancy ratios of the following cycles are set at around 4% to tolerate errors caused by the incomplete settling of the control logic buffers. The last two redundancy values are set to 1 LSBs to adjust the number of unit capacitors to be integers, which facilitate the floor planning of the DAC array.



Redundancy Range(LSB)	128	32	8	4	2	1	1	1	0	0	0
Redundancy Ratio	25%	10%	4.5%	4.3%	4.2%	4%	7.7%	15%	0	0	0
Bit Name	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output Code	1	0	1	1	0	1	0	0	0	1	0

Figure 5.7 Illustration of the non-binary algorithm operation with 666.5 LSB input.

In Figure 5.7, the non-binary operation is illustrated with a 666.5 LSB input. The monotonic switching technique [18] is employed in this design, and the dynamic offset caused by common mode voltage variation is tolerated within the non-binary search algorithm. The synchronous timing is adopted. Moreover, the feedback delay from the comparator output to DAC array is shortened by using the state machine based pre-settling control logic. The summary and comparison of DAC settling time are listed in Table 1. The total settling time requirement is shortened to 35.2τ by using the proposed non-binary algorithm. The time allocation for one SAR conversion is depicted in Table 2.

Table 5.1 Comparison of binary and non-binary algorithm

	Each settling time	Number of Step	Total settling time
Traditional binary	**6.9τ**	**10**	**69τ**
Non-binary in [58]	**2.8τ**	**11**	**31τ**
Non-binary in this work	**3.2τ**	**11**	**35.2τ**

Table 5.2 Time allocation for one SAR conversion

	Each step	Number of step
DAC settling time	**100 ps**	**10**
Logic delay	**50 ps**	**10**
Comparison time	**150 ps**	**11**
Sampling	**700 ps**	
Total	**3.85 ns**	

Weight	512	256	128	64	32	16	8	4	2	1
		D_{10}	D_{10}	D_7	D_9	D_7	D_8	D_6	D_6	D_0
		D_9	D_8		D_8	D_5	D_7	D_4	D_3	
					D_6		D_6	D_3	D_1	
							D_5	D_2		
+							D_4			
Binary out	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

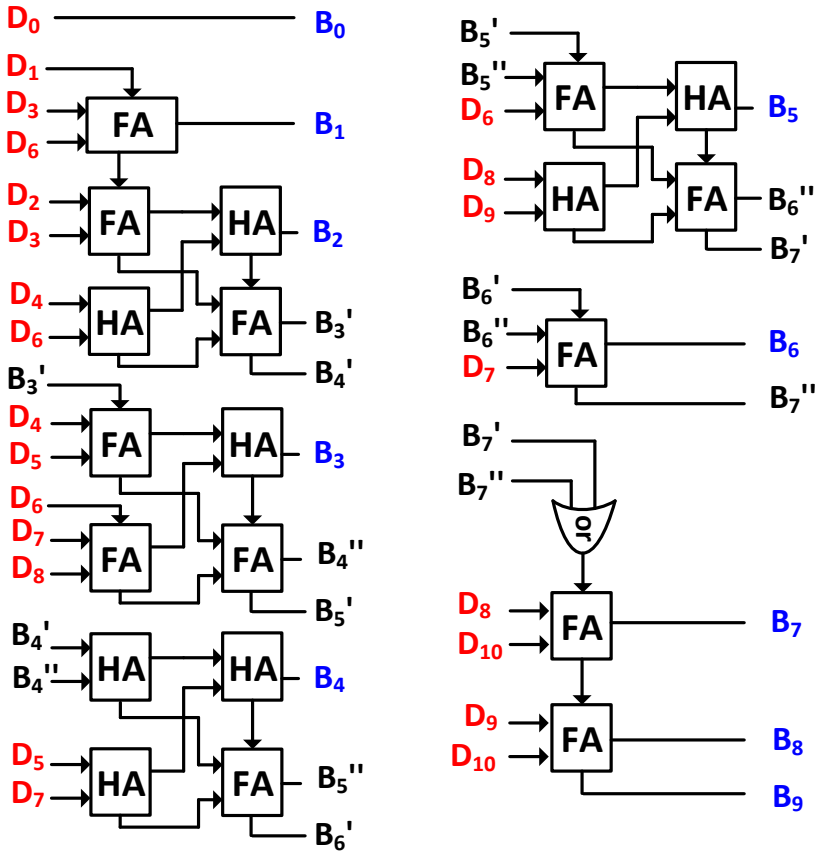


Figure 5.8 Schematic of encoding circuit from D_i (i=0~10) to B_j (j=0~9).

To convert the ADC output codes with redundancy to binary codes, the adder based encoding circuit illustrated in Figure 5.8 is adopted. The conversion table is also shown in Figure 5.8. D_{10}~D_0 represent the redundant outputs and B_9~B_0 represent the binary codes. The encoding operation is realized by adders instead of complex arithmetical units [58] or FIR filters [60]. To build the encoding circuit, only 12 full adders (FA), 8

half adders (HA) and 1 OR gate are used, resulting in low power consumption. Compared with [5], no subtraction and extra unit capacitors are required.

5.2.3 Background time skew calibration

Fractional delay filters [61], [62] could be utilized to compensate the time skew error in digital domain. Supposing T is the overall ADC sampling period, and $T_d=\alpha T$ represents the fractional delay. For conventional fractional delay filter based time skew calibration technique [25], the input signal bandwidth for calibration is limited to sub-channel sampling rate and the range of α could not be small due to large time skew introduced by the front-end sampling. Benefiting from the presented time skew suppressed sampling technique, the range of fractional delay in this design could be constrained into [-0.002T, +0.002T]. The calibration of time skew is divided into two parts: detection and correction. The time skew detection technique in [63] is employed, which compares the mean value (through accumulation and average) of the multiplication of signals $x_m(n)$ in two adjacent channels to detect the polarity of time skew error $p(t_m)$ and updates the coefficients of FIR filter $F(a_m)$ adaptively as shown in Figure 5.9.

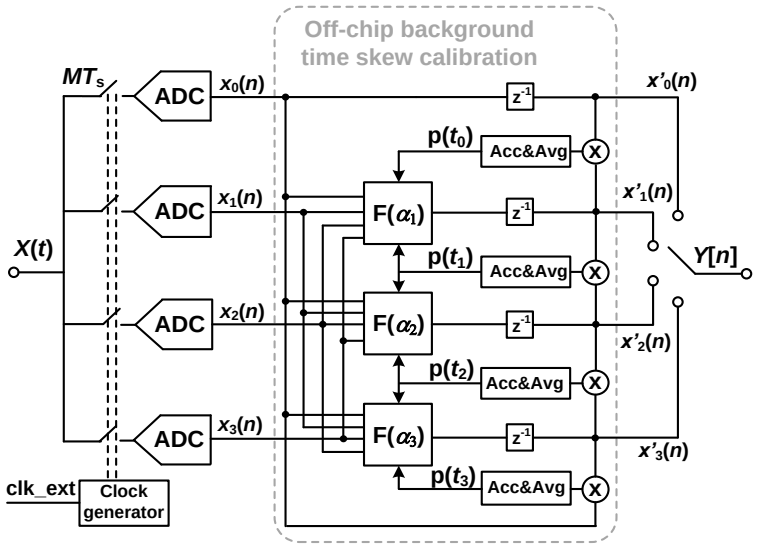


Figure 5.9 The architecture of the proposed digital background time skew calibration.

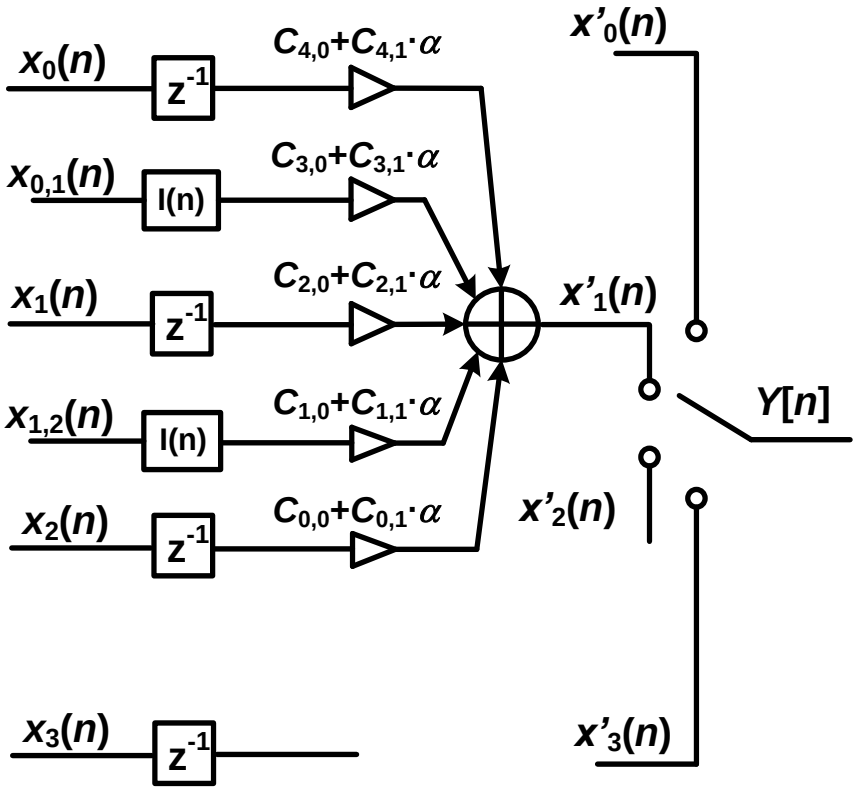


Figure 5.10 Proposed digital time skew calibration architecture of a four-channel TI-ADC, where only the second-channel is illustrated and N=2.

For time skew correction, the proposed correction FIR filter architecture is shown in Figure 5.10, where only the second-channel (m=1) is illustrated and the length of FIR correction filter is $2N$+1 (N=2, 4, …) (N=2 in Figure 5.10). The α indicates the time error to be calibrated. C =[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, $c_{2,0}$, $c_{2,1}$, $c_{3,0}$, $c_{3,1}$, $c_{4,0}$, $c_{4,1}$] are the coefficients of correction filters. $I_{m,m+1}(n)$ is the interpolation filter between channel m and channel m+1. M is number of interleaved channels. To achieve a nearly full Nyquist band (95%) calibration with short-tap FIR filters, the interpolation after sampling is presented, making an equivalent oversampling ratio of 2.

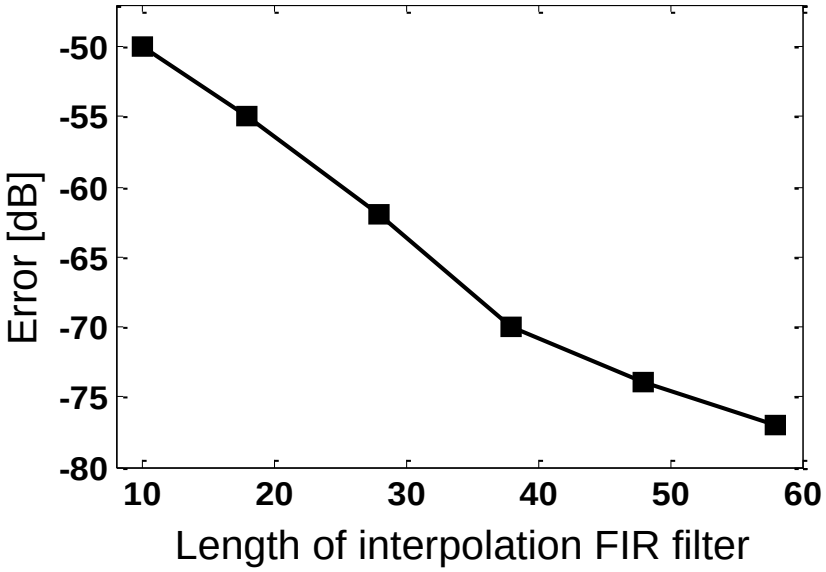


Figure 5.11 With 5-tap time skew correction filter, error level versus the length of interpolation FIR filters.

To evaluate the effect of length of interpolation filter on calibration accuracy, Figure 5.11 shows the error level under different lengths of interpolation FIR filters, with the length of FIR correction filters being 5-tap (N=2). The advantage of the proposed calibration technique is that it can achieve background time skew error calibration with shorter tap FIR correction filters and less bandwidth penalty compared with those in [25] and [64]. The comparison is shown in Table 5.3.

Table 5.3 Time allocation for one SAR conversion

	Number of taps	Bandwidth penalty	Error Level (dB)	Adaptive
[25]	60	10%	-72	No
[64]	75+30	33%	-72	Yes
This work	38+5	5%	-70	Yes

The correction filter coefficients are approximated by linear polynomial of time skew

error α. The approximation error is

$$e(\omega,\alpha) = F(\omega,a) - D(\omega,a)\,, \tag{5.8}$$

where

$$\begin{aligned} F(\omega,a) = &\sum_{n=0}^{N}(c_{2n,0} + \alpha c_{2n,1})e^{-j\omega(n+\frac{K-N}{2})T} \\ &+ \sum_{n=0}^{N-1}(c_{2n+1,0} + \alpha c_{2n+1,1})\sum_{k=0}^{K-1}e^{-j\omega(k+n)T} \end{aligned} \tag{5.9}$$

and

$$D(\omega,a) = e^{-j\omega(\alpha+\frac{K}{2})T}\,. \tag{5.10}$$

$F(\omega,\alpha)$ and $D(\omega,\alpha)$ are the transfer function of the correction FIR filter and the ideal fractional delay function, respectively. Variable K (K=2, 4, …) is the length of interpolation FIR filter. α and K/2 are the factional and integral delay respectively. The optimization of correction FIR filter coefficients $C_{n,m}$=[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, …, $c_{2N,0}$, $c_{2N,1}$] is to be done.

The time skew correction FIR filter coefficients $C_{n,m}$=[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, …, c_{2N},0, $c_{2N,1}$], whose length is 4N+2, are to be optimized. The transfer function $F(\omega,\alpha)$ of the FIR filter can be rewritten as

$$F(\omega,a) = C_{n,m}\cdot(c(\omega) - js(\omega))^{\mathrm{T}}\,, \tag{5.11}$$

where $c(\omega)$=[cos((K/2-1) ω), cos((K/2-1) ω), $\sum_{k=0}^{K-1}$ cos($k\omega$), $\sum_{k=0}^{K-1}$ cos($k\omega$), …, $\sum_{k=0}^{K-1}$ cos((k+N-1)ω), $\sum_{k=0}^{K-1}$ cos((k+N-1)ω), cos((K/2-1+N) ω), cos((K/2-1+N) ω)], and $s(\omega)$=[sin((K/2-1) ω), sin((K/2-1) ω), $\sum_{k=0}^{K-1}$sin($k\omega$), $\sum_{k=0}^{K-1}$sin($k\omega$), …, $\sum_{k=0}^{K-1}$sin((k+N-1)ω), $\sum_{k=0}^{K-1}$ sin((k+N-1)ω), sin((K/2-1+N) ω), sin((K/2-1+N) ω)]. To minimize the approximation error, the following min-max problem need be solved:

$$\min_{C_{n,m}}\{\max|e(\omega,\alpha)|\}, \qquad \omega\in\Omega,\ \alpha\in\mathrm{A} \tag{5.12}$$

where $C_{n,m}$ contains all the filter coefficients to be optimized. Ω and A are the frequency band and time delay range of optimization respectively. The objective in (5.8) can be written as

$$\begin{aligned} &|e(\omega,\alpha)| \\ &=|F(\omega,\alpha)-D(\omega,\alpha)| \\ &=\left\| \begin{bmatrix} R^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha) \\ I^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha) \end{bmatrix} \right\|_2 \\ &=[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2} \end{aligned} \tag{5.13}$$

where

$$\begin{aligned} &R^D(\omega,\alpha)=[D(\omega,\alpha)]_R,\ \ I^D(\omega,\alpha)=[D(\omega,\alpha)]_I \\ &R^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_R \\ &I^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_I \\ &R^{FD}(\omega,\alpha)=R^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha) \\ &I^{FD}(\omega,\alpha)=I^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha) \end{aligned}$$

Here $[\cdot]_R$ and $[\cdot]_I$ represent the real and imaginary parts of a complex number or vector respectively. Therefore, the min-max problem can be reformulated as

$$\begin{aligned} &\min_{C_{n,m}} \quad \delta \\ &\text{subject to} \quad \delta-[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\geq 0. \end{aligned} \tag{5.14}$$

And the above optimization problem within a given range of frequency ω and fractional delay value α could be solved by a standard SOCP solver [76], which is

$$\begin{aligned} &\min_{x} \quad c\cdot x \\ &\text{subject to} \quad c\cdot x\geq \left\|Fx-d\right\|_2, \end{aligned} \tag{5.15}$$

where c=[1, zeros(1, 4N+2)], x=[δ, $C_{n,m}$]$^{\mathrm{T}}$, F=[0, $R^{\mathrm{F}}(\omega_i,\alpha_j)$; 0, $I^{\mathrm{F}}(\omega_i,\alpha_j)$], d=[$R^{\mathrm{D}}(\omega_i,\alpha_j)$, $I^{\mathrm{D}}(\omega_i,\alpha_j)$]$^{\mathrm{T}}$, i=0, 1,…, I, j=0, 1,…, J. Here I and J are the number of frequency points and fractional delay points for computation respectively.

5.3 Circuit implementation

5.3.1 Internal clock generator

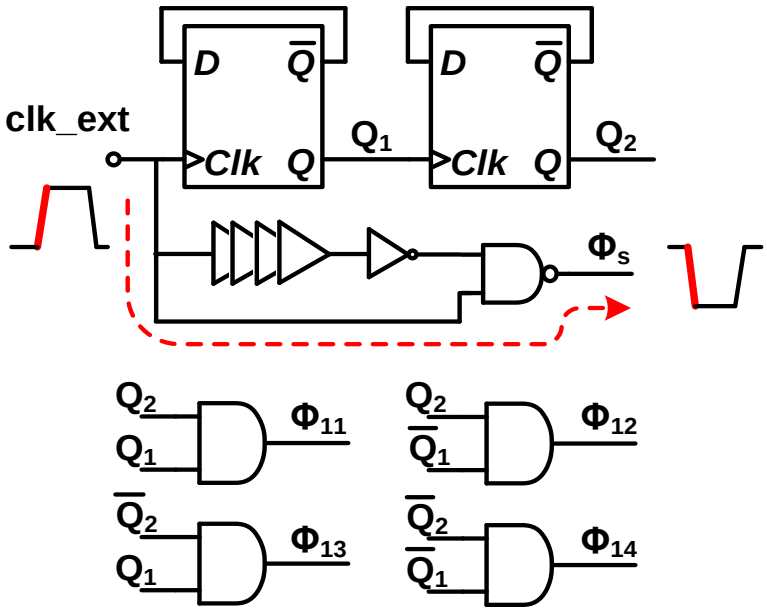


Figure 5.12 Schematic of internal clock generator.

For the presented sampling technique of TI SAR ADCs, a clock signal with Nyquist sampling rate is needed. The schematic of internal clock generator is shown in Figure 5.12, where *clk_ext* is the external clock input. Signal Q_1 and Q_2 are generated by divide-by-2 and divide-by-4, respectively. The signal clk_s is obtained from *clk_ext* with duty cycle changed. When clk_s is high, one of four sub-channels operates in sampling phase. Using Q_1 and Q_2, the Φ_i (i=1, 2, 3, 4) can be generated through AND gates shown in Figure 5.12. In addition, since the falling edge of clk_s determines the end of each sampling, attention should be paid regarding to the jitter performance of clk_s. The relationship between SNR and jitter Δt_{jitter} is [26]

$$SNR = 20\log\frac{1}{2\pi f_{in}\Delta t_{jitter}}. \tag{5.16}$$

Where f_{in} is the input frequency. To maintain the SNR as 50dB at a 500MHz input frequency, the jitter of signal after internal clock buffer should be much lower than 0.7ps *rms*. In this design, the rising edge of the buffered *clk_ext* goes through only one NAND gate to generate the falling edge of clk_s (shown in Figure 5.12), introducing less additional jitter from digital logic. The power supply of the circuit generating clk_s is separated with other logic circuit to reduce power supply noise introduction. The schematic of bootstrapped switch for proposed sampling technique is drawn in Figure 5.13. Φ_i is the control signal mentioned before. When Φ_i is high, the corresponding bootstrapped switch is activated. clk_s is the full rate sampling clock, dominating the sampling instant.

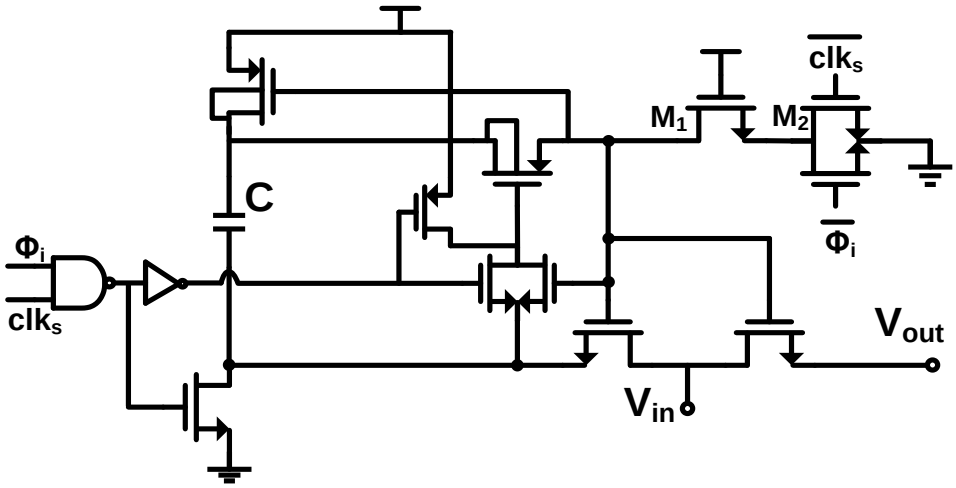


Figure 5.13 Schematic of sampling switch.

5.3.2 Single-channel SAR ADC

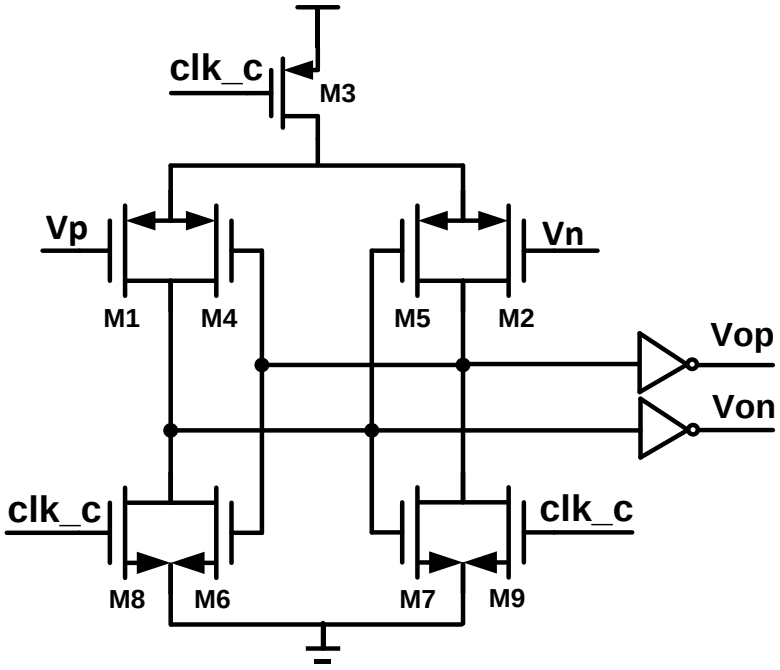


Figure 5.14 Schematic of comparator circuit.

The schematic of dynamic comparator is shown in Figure 5.14. The PMOS transistors are adopted as the input pair. An extra p-type cross-couple transistors M_4 and M_5 are added to obtain larger output scale. When *clk_c* is high, the comparator is in reset phase. And it is in comparison phase when *clk_c* is low. Additionally, two inverters follow the *Vop* and *Von* to prevent hysteresis effect caused by the following latch circuit.

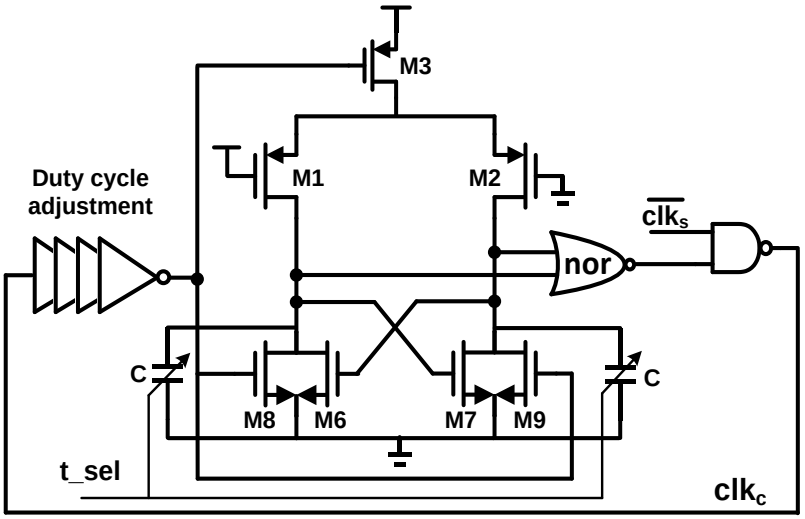


Figure 5.15 Schematic of local synchronous timing generator.

The programmable synchronous timing generator providing local timing with process corner sensing function is shown in Figure 5.15. Unlike the traditional SAR logic [39], there always exists considerable delay between comparator output and DAC array. The proposed dynamic control logic shortens the delay, which just equals to the delay of one transmission gate and inverter.

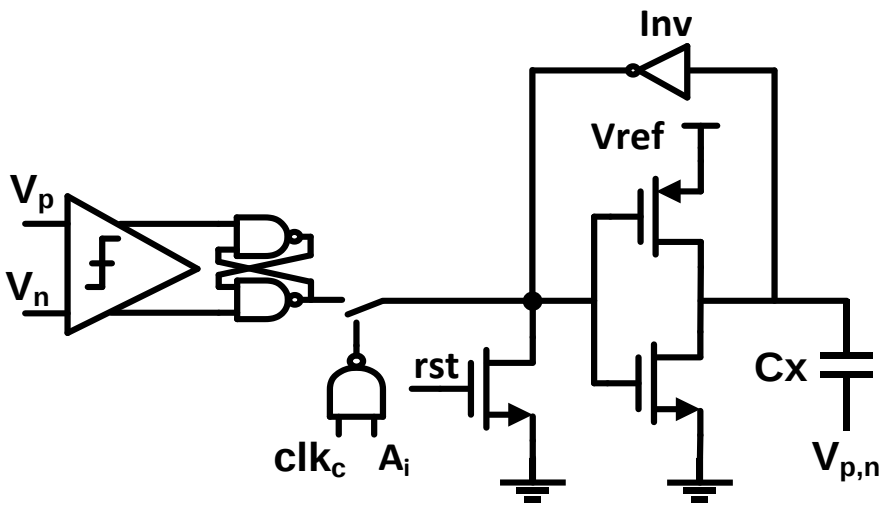


Figure 5.16 Schematic of control logic circuit.

The schematic of DAC control logic is shown in Figure 5.16. In the sampling phase, the reset signal *rst* is high, and all the unit capacitors in DAC array are connected to V_{ref}. During the conversion phase, the DAC array is controlled by *clk_c* under certain state A_i. The inverter *inv* in Figure 5.16, whose driving capacity is quite weak, is used to prevent logic error caused by leakage or unnecessary interference.

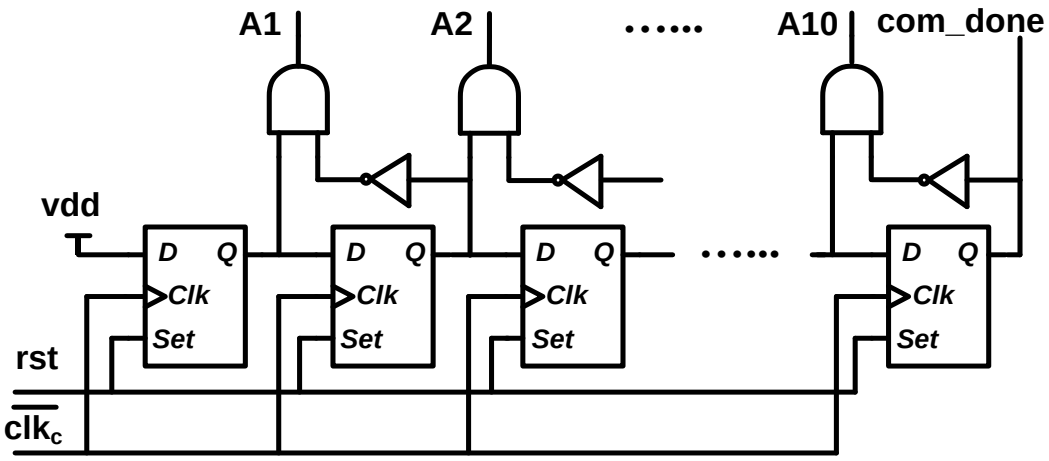


Figure 5.17 Schematic of shift register.

The control logic is controlled by a state machine based shift register shown in Figure 5.17, which selects the corresponding unit capacitors before the rising edge of *clk_c* coming. According to [42], the process variation of unit capacitor should satisfy

$$3\sigma_{\mathrm{DNL}} < \frac{1}{2}\mathrm{LSB}\ . \tag{5.17}$$

Due to the implemented non-binary DAC array, the MSB code transition switches 766 (2·(192+191)) unit capacitors for a differential DAC array. Therefore, with the given nominal value of C_{u}, the σ_{DNL} is

$$\sigma_{\mathrm{DNL}} = \frac{\sqrt{766}\sigma_u}{2C_u} \Rightarrow \frac{\sigma_u}{C_u} < 1.2\%\,. \tag{5.18}$$

In the proposed DAC array, a 1.3μm x 1.3μm unit capacitor with a capacitance of 0.47fF is employed.

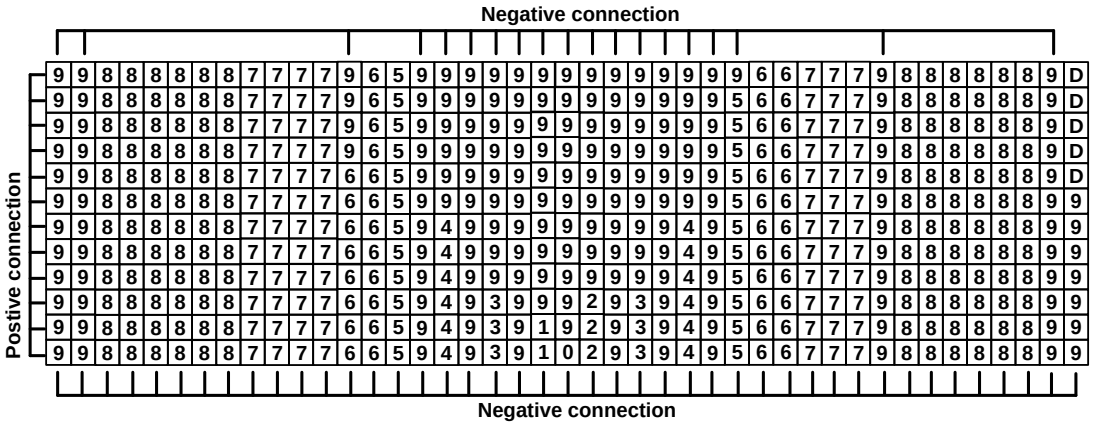
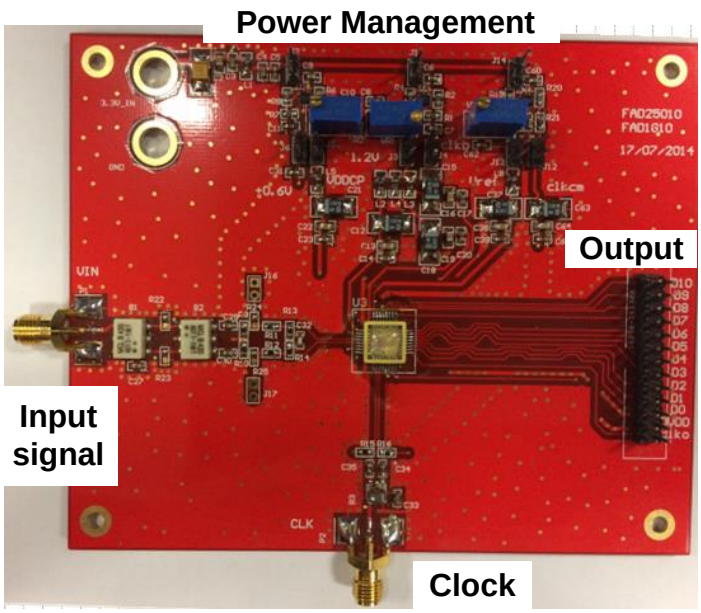


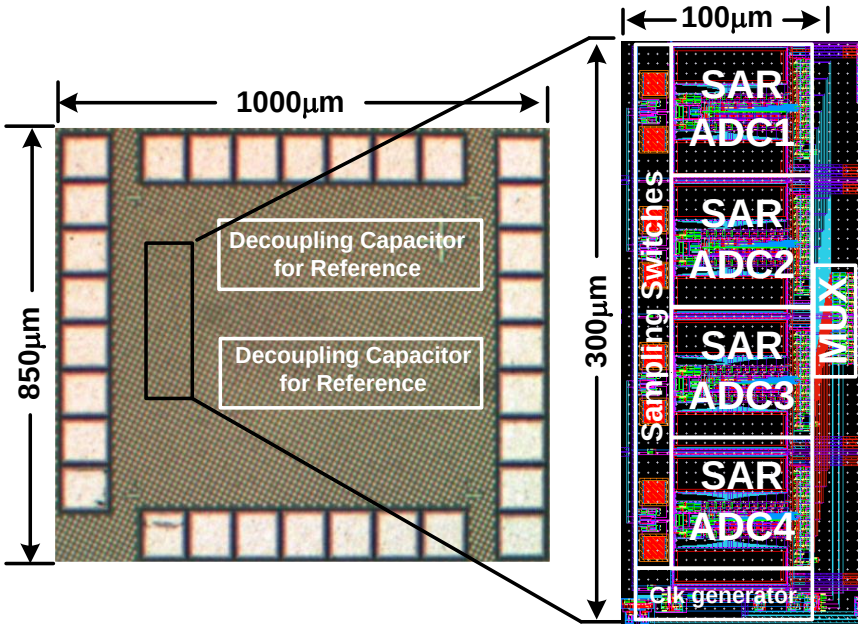
Figure 5.18 Floor plan of the capacitor DAC array.

Figure 5.18 shows the floor plan of capacitor DAC array. The positive is connected horizontally and the negative is connected vertically. Unlike the previous placement of unit capacitors [18] , for which the extra wiring are necessary for different unit capacitor groups, introducing unexpected parasitic capacitors between positive and negative of DAC array. In [42], the unit capacitors are placed in one line, suffering from more serious gradient effect in horizontal and larger area.,

5.4 Measurement results



(a)



(b)

Figure 5.19 (a) Testing board. (b) Chip micrograph and layout.

The ADC chip is fabricated in a 1P9M 65nm CMOS process with low-V_{th} option. The testing board is shown in Figure 5.19(a). The die photo is shown in Figure 5.19 (b). The ADC core occupied 300µm x 100µm (0.03mm^2). Instead of using power hungry reference buffer, a decoupling capacitor of 50pF is used to guarantee a sufficient error coverable range for the SA comparisons. The measurement is conducted in room temperature. The total power consumption is 7.8mW (excluding off-chip mismatch calibration) at 1.2V power supply when operating at 1GS/s, with each sub-channel SAR ADC consuming 1.85mW, and 0.4mW for the clock generation (excluding CML-to-CMOS converter) and multiplexing. The ENC block is designed off-chip, of which the estimated power is 0.15mW and its area is 110µm^2. The offset mismatch and background time skew calibration are done off-chip, of which the estimated power consumption is 8mW and area is 0.012mm^2. The capacitance of each single-end input sampling DAC array is 240fF (512C, each unit capacitor C of 0.47fF) excluding

parasitic capacitance. To reduce the effect of parasitic inductor of bonding wire, double input pads are used with the parasitic capacitance of 2pF. The impedance of input is matched to be 50Ω on board, resulting in a 3GHz input bandwidth. In this design, the differential input range is $2.0V_{p\text{-}p}$ at 1.2V supply.

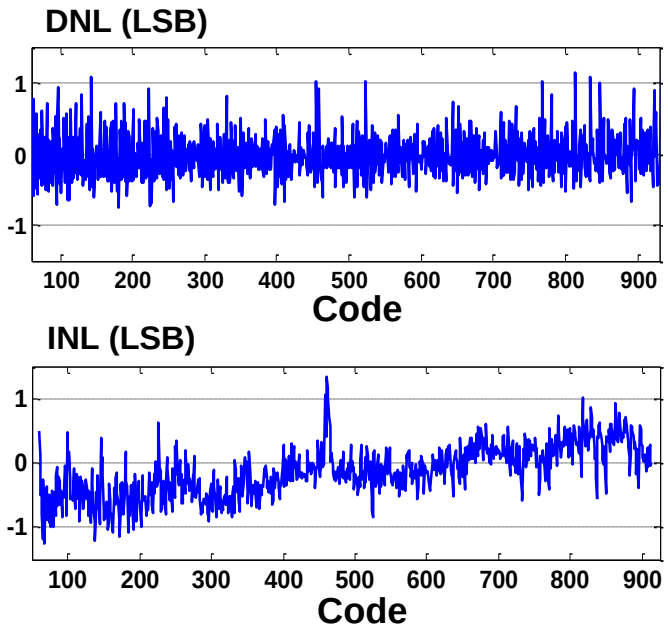


Figure 5.20 Measurement results of DNL & INL.

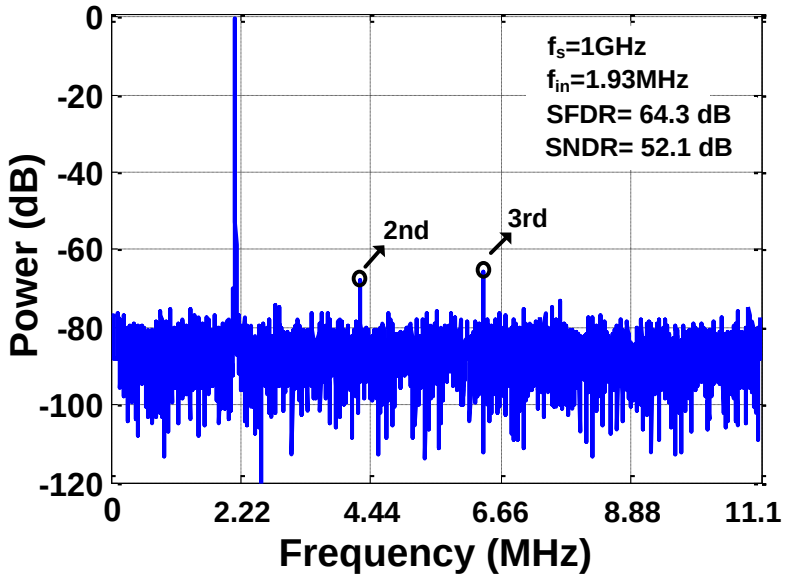
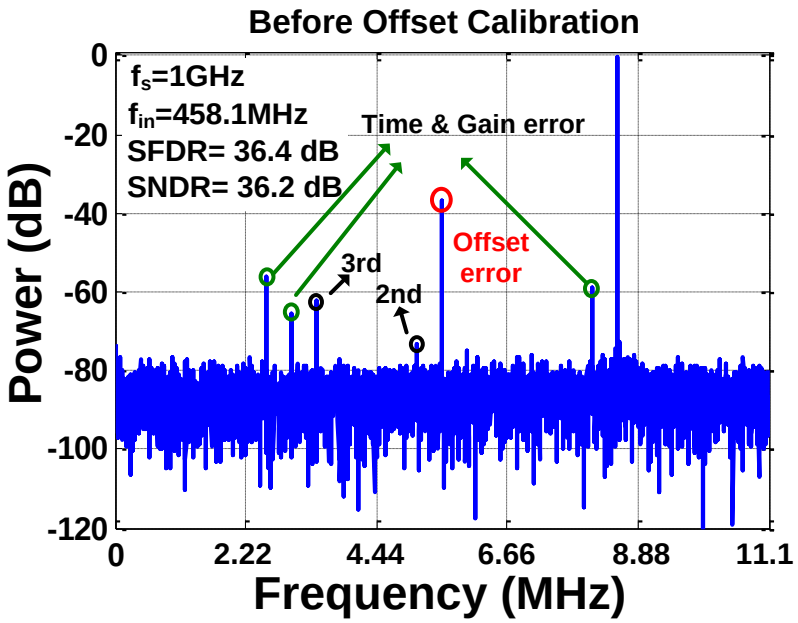
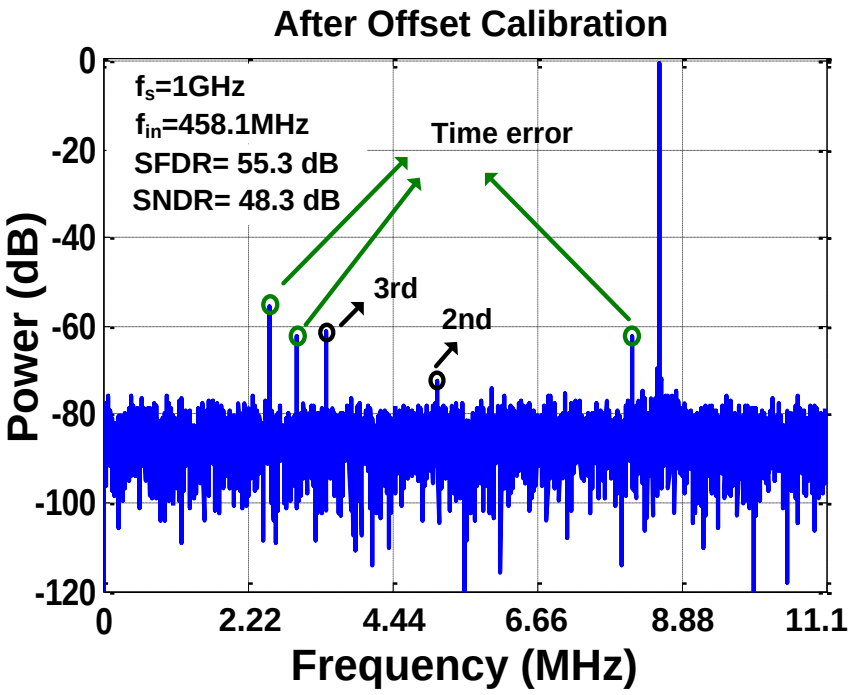


Figure 5.21 Measured 8192-point FFT (digital output is decimated by 45) with f_{in}=1.9MHz.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Figure 5.20. The peak DNL is +1.2/-0.7 LSB and peak INL is +1.3/ -1.2 LSB. Before offset calibration, the SNDR and SFDR are degraded mainly by offset mismatch, which is removed after calibration. Figure 5.21 shows the measured output spectrum of 1.9MHz. In Figure 5.22, after calibration the measured SFDR and SNDR at a 458.1MHz input are 55.3dB and 48.3dB respectively. The corresponding effective number of bit (ENOB) is 7.76 bits at Nyquist input frequency. The summary of measurement for the three sample chips is listed in Table 5.4.



(a)



(b)

Figure 5. 22 Measured 8192-point FFT (digital output is decimated by 45) with f_{in}=458.1MHz before and after offset calibration.

Table 5.4 Mismatch of three tested chips

Chip sample	Time error (SFDR @497.4 MHz)	Offset error (Average)	Gain error (Average)
No.1	52.1 dB	26mV	0.0008
No.2	55.3 dB	17mV	0.0005
No.3	53.4 dB	28mV	0.0006

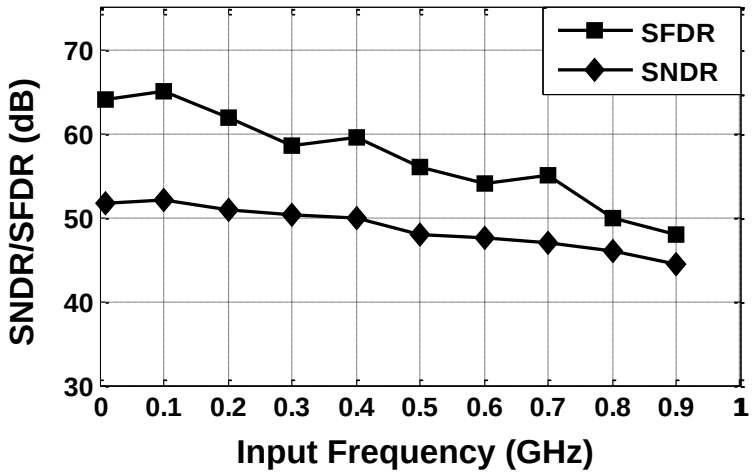


Figure 5.23 SFDR and SNDR versus input frequency at f_s=1GHz and V_{dd}=1.2V.

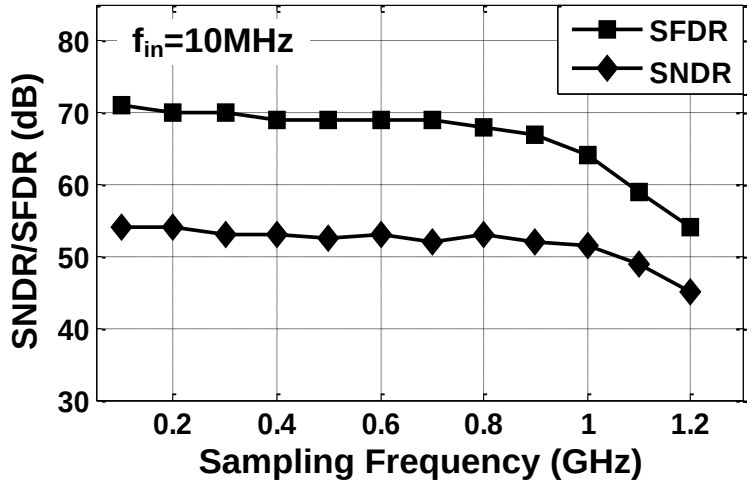


Figure 5.24 SFDR and SNDR versus sampling frequency at f_{in}=10MHz and V_{dd}=1.2V.

It is found that the gain mismatch is comparatively small with negligible effect on the SNDR and SFDR. Without time skew calibration, the SFDR caused by time error at 458.1MHz input is around 52~55dB (0.6ps *rms* equivalently, Table 5.4 Mismatch of three tested chips) with *W/L* of M_2 in the fabricated chip around 4um/60nm. Figure 5.23 shows the SFDR and SNDR versus input frequency from 10MHz to 900MHz. Figure

5.24 depicts the SFDR and SNDR versus sampling frequency at 10MHz input frequency. A summary of the measured performance is shown in Table 5.5.

To reduce the effect of time skew error, the proposed digital background time skew compensation technique is adopted off-chip. The length of time skew correction filter and interpolation filter are set as 5 and 38 respectively, which calibrates the time skew spurs to be lower than -70dB. The coefficients of correction filter are listed in Table 5.6.

Table 5.5 Performance summary

Technology		65nm CMOS	
Supply Voltage (V)		1.2	
Input Common Mode (V_{cm})		0.6	
Differential Input Range (V_{p-p})		2.0	
Input Capacitive Load Single-end (pF)		0.25	
Sampling Rate (GS/s)		1.0	
Active Area (mm^2)		0.03	0.042
SFDR(dB) @Nyquist-freq		55.3	61.6
SNDR(dB) @Nyquist-freq		48.3	49.6
ENOB		7.76	7.96
Power	Sub-channel (mW)	1.85	1.85
	Clock distribution and Multiplexing (mW)	0.4	0.4
	Binary encoding	0.15	0.15
	Time skew calibration	0	8
	Total (mW)	7.95	15.95
Figure of Merit (fJ/con-step)		36.7	63

Table 5.6 Optimized filter coefficients

$C_{n,m}$	m=0	m=1
n=0	-3.5e-7 (0)	0.2674
n=1	4.1e-6 (0)	-1.4923
n=2	1	-7.3e-13 (0)
n=3	4.1e-6 (0)	1.4923
n=4	-3.5e-7 (0)	-0.2674

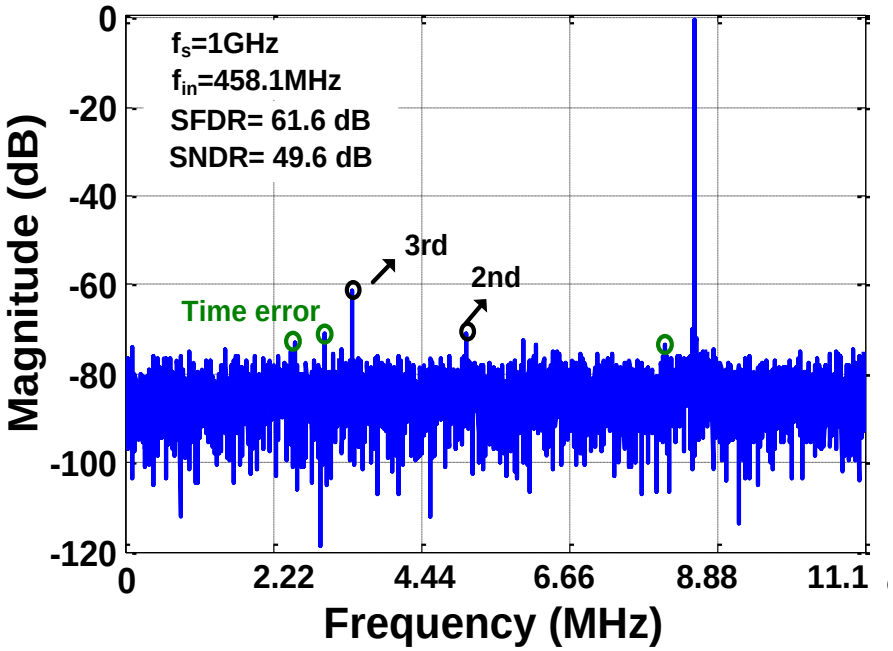


Figure 5.25 Measured 8192-point FFT (digital output is decimated by 45) with f_{in}=458.1MHz after off-chip time-skew calibration.

Assuming channel 1 as the reference channel, the measured time skew of other 3 channels in one chip are -0.6ps, 0.1ps and -1.5ps. The iterative calibration time step T_{step} is set to 0.1ps. After time skew calibration, the SFDR and SNDR are improved to 61.6dB and 49.6dB respectively shown in Figure 5.25. Compared with the state-of-the-art ADCs (Table 5.6), the proposed ADC achieves a low FoM value of 36.7fJ/conversion-step (lowest 31.6fJ/conversion-step after time skew compensation) and a die size of 0.03mm^2. In term of energy per conversion, this work achieves 7.8pJ per conversion. A comparison with the prior state-of-the-arts ADCs faster than 1GS/s published at ISSCC and VLSI conference from 1997 to 2014 [65] is shown in Figure 5.7.

Table 5.7 Comparison of State-of-the-Art GHz ADCs

	JSSC 2013 [55]	JSSC 2013 [52]	JSSC 2014 [51]	ISSCC 2013 [37]	ISSCC 2014 [23]	ISSCC 2014 [28]	This Work	This Work (w time skew cal.)
Architecture	TI-SAR	Pipe-line	Pipe line	TI-SAR	TI-SAR	TI-SAR	TI-SAR	
Technology (nm)	65	65	65	40	40	65	65	
Supply voltage(V)	1.2	1.0	1.0	1.2	1.1	1.0	1.2	
Power (mW)	44.6	19.0	7.1	10.8	93	18.9	7.95	15.95
Fs (GS/s)	2.8	0.8	1.0	0.9	1.6	1.0	1.0	
Resolution(bit)	11	10	9	9	9	10	10	
DNL (LSB)	-	+1.0/-1.0	+0.8/-0.87	0.21	-	+1.0/-1.0	+1.2/-0.7	
INL(LSB)	-	+2.0/-2.0	+1.8/-1.6	0.31	-	+1.0/-1.0	+1.3/-1.2	
SNDR@ Nyquist(dB)	48.2	52.2	47.7	51.2	48.0	51.4	48.3	49.6
ENOB(bit)	7.7	8.36	7.6	8.2	7.65	8.2	7.7	7.94
FoM (fJ/con-step)	75.8	71.4	35.6	40.5	283	62.3	36.7	63
Active Area (mm^2)	1.7	0.18	0.1	0.038	0.83	0.78	0.03	0.042

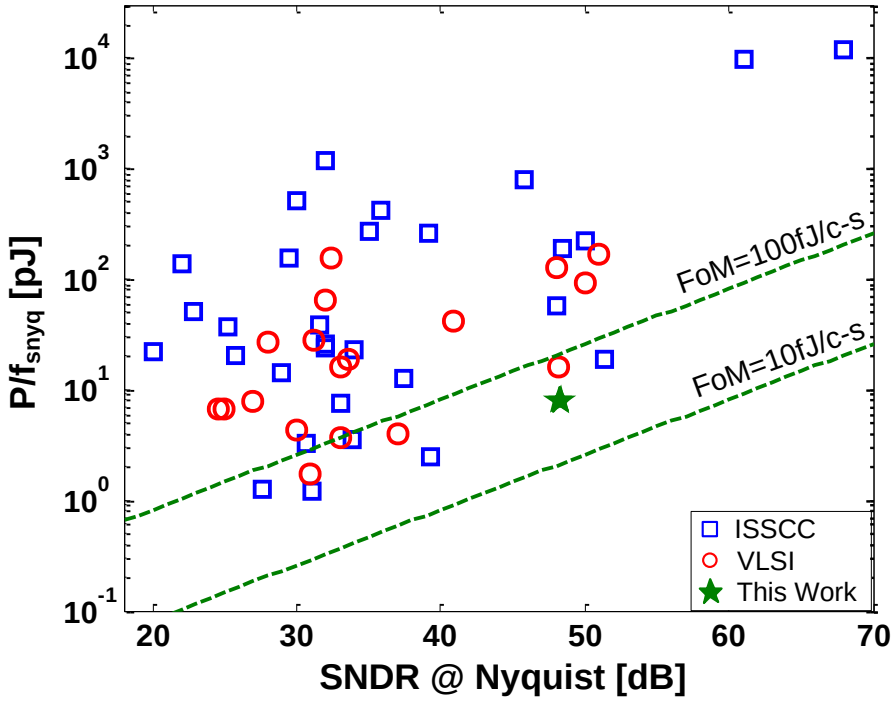


Figure 5.26 Energy per conversion for all ADCs with published at ISSCC and VLSI conferences from 1997 to 2014.

5.5 Summary

A test chip of a four-channel 10-bit SAR ADC with sampling rate up to 1GS/s, adopting time skew suppressed sampling technique, is proposed. By utilizing the power and area efficient non-binary high speed sub-SAR ADCs, the TI-ADC achieves low power consumption (7.8mW) at 1GS/s and smaller silicon area of 0.03mm^2, compared with the prior state-of-the-art works. Without time skew calibration, a SFDR of 55 dB can be obtained at 458MHz input. Moreover, the remaining time skew error could be compensated readily by digital background calibration with low computational FIR filters. The custom designed non-binary DAC array improves the error tolerance capability during conversion mode and reference settling phase. Additionally, the adders based encoding logic for non-binary SAR ADC ensures that less hardware overhead is required to implement the error-tolerant SAR ADC architecture. Further, the proposed silicon area efficient TI SAR ADC is potential for designing TI ADCs with tens of sub-channels.

Chapter 6. CONCLUSION AND FUTURE WORK

This chapter will conclude the thesis and shed light on the possible improvement and update of the high-speed high-resolution ADCs for future work.

6.1 Conclusion

This thesis conducted a comprehensive study of high-speed high-resolution ADCs covering single-channel high-speed SAR ADC design, time-interleaved SAR ADC design and calibrations for multi-channel ADCs:

Power-efficient switched-capacitor amplifier: In Section 2.1.1.4, a low power high speed source follower based switched-capacitor amplifier for pipelined ADCs is proposed. By using the source follower as the core of the SC amplifier, the power consumption can be significantly reduced whilst obtaining the same linearity and bandwidth. Meanwhile, through replicating the input signal to the drain of input transistor, the channel-length modulation effect can be suppressed, achieving a high linearity (> 60dB).

Calibrations for multi-channel ADCs: Two time skew calibration techniques for time-interleaved ADCs are presented in Section 3.2. First, a statistic based time skew calibration method for time-interleaved ADCs is presented. By comparing the mean value of the multiplication of signals in two adjacent channels, the time skew can be estimated. Subsequently, a capacitor array based digitally controlled delay block placed in sampling clock path is adopted to compensate the time skew. In addition, the precision of calibration is further improved through using a monotonic small capacitor array. Second, a digital time skew calibration technique for time-interleaved (TI) ADCs is presented. The time skew calibration for TI-ADCs in analog domain suffers from limited correction accuracy and additional jitter. And the proposed digital time skew

calibration method estimates the polarity of the time skew through correlation of adjacent channels and corrects the time error by adopting adaptive fractional delay filters iteratively. The calibration scheme of filter bank mismatches for frequency-interleaved ADCs is depicted in Section 3.3. The filter bank mismatch of analog analysis filters in frequency-interleaved ADCs (FI-ADCs) degrades the system's spurious-free dynamic range (SFDR) significantly. In this paper, a calibration approach for compensating such mismatch is presented. By modelling the parameter mismatches in the analysis filters, the filter bank mismatch compensation is divided into a coarse trimming mode and a fine tuning mode. After the coarse trimming mode by trimming the resistors and capacitors in analog domain, the fine tuning mode by updating coefficients of synthesis filters is further carried out in digital domain to achieve high precision calibration. A design example of 10GS/s 8-bit four-channel FI-ADC is built in MATLAB.

Single-channel high-speed SAR ADC: In Chapter 4, a 10-bit 300MS/s asynchronous 2b/cycle successive approximation register (SAR) analog-to-digital converter (ADC) is proposed. The interpolation technique is employed to reduce the size of DAC array, relaxing the trade-off between input bandwidth and resolution. The background offset calibration technique is presented after every data conversion to compensate the offset of each comparator. Moreover, a fast SAR control logic is proposed to shorten the delay between comparator outputs to DAC array.

Time-interleaved high-speed SAR ADC: In Chapter 5, a four-channel 10-bit SAR ADC with sampling rate up to 1GS/s, adopting time skew suppressed sampling technique, is proposed. By utilizing the power and area efficient non-binary high speed sub-SAR ADCs, the TI-ADC achieves low power consumption (7.95mW) at 1GS/s and smaller silicon area of 0.03mm^2, compared with the prior state-of-the-art works. Without time skew calibration, a SFDR of 55 dB can be obtained at 458MHz input. Moreover,

the remaining time skew error could be compensated readily by digital background calibration with low computational FIR filters. The custom designed non-binary DAC array improves the error tolerance capability during conversion mode and reference settling phase. Additionally, the adders based encoding logic for non-binary SAR ADC ensures that less hardware overhead is required to implement the error-tolerant SAR ADC architecture. Further, the proposed silicon area efficient TI SAR ADC is potential for designing TI ADCs with tens of sub-channels.

In summary, this thesis introduced some techniques for low-power high-speed high-resolution ADCs designs.

6.2 Future work

Although some progress has been achieved in this thesis, there is still much space to be improved for a better high-speed high-resolution ADC:

Single-channel ADC designs: In this part, a two-step ADC structure with background offset and gain calibration could further increase the speed and resolution of the ADC. To make the ADC system design more completed, the design of input buffer and reference buffer should be considered.

Time-interleaved ADCs: In this part, by employing power efficient wide band input buffer, the input bandwidth of ADC system could be extends up to ten GHz. Also, the background calibration algorithm should be integrated into the ADC system to further verify the function in details.

Calibration for multi-channel ADCs: In this part, the limitations of the proposed calibration techniques should be fully investigated. For example, the speed limitation for the proposed digital background time skew calibration technique should be studied.

AUTHOR'S PUBLICATIONS

Journal papers:

1. **Q. Lei**, Y. Zheng, S. Liter, " Design of frequency interleaving ADC with mismatch compensation," ***Electronics Letters***, vol. 50, issue. 9, pp. 659-661, 2014.
2. Kuojun yang, Shulin Tian, Hao Zeng, **Lei Qiu**, Lianping Guo, "A seamless acquisition digital storage oscilloscope with three-dimensional waveform display," ***Review of Scientific Instruments***, vol.85, No.4, 2014.
3. Guo, Lianping, Shulin Tian, Zhigang Wang, Kuojun Yang, **Lei Qiu**, "Analysis of Channel Mismatch Errors in Frequency-Interleaved ADC System." ***Circuits, Systems, and Signal Processing*** (2014): 1-16.
4. **Q. Lei**, Y. Zheng, S. Liter, " A source follower based high-speed switched capacitor amplifier for pipelined ADCs," ***Electronics Letters***, vol. 51, issue 1, pp. 21-23, 2015.
5. **Lei Qiu**, Yuanjin Zheng, Siek Liter, " Multichannel Time Skew Calibration for Time-Interleaved ADCs Using Clock Signal," ***Circuits, Systems and Signal Processing***, pp. 1-14, 2015.
6. **Lei Qiu**, Yuanjin Zheng, Siek Liter, " A Filter Bank Mismatch Calibration Technique for Frequency-Interleaved ADCs," ***Circuits, Systems and Signal Processing***, pp. 1-16, 2016.
7. **Lei Qiu**, Kai Tang, Yuanjin Zheng and Liter Siek, " A Low Computational Non-binary Searching Technique for High Speed SAR ADCs," ***IEEE Trans. Very Large Scale Integration Systems***, accepted.

8. **Lei Qiu**, Kai Tang, Yuanjin Zheng, Liter Siek, Yan Zhu, and Seng-Pan U, " A 10-bit 1GS/s 7.8mW 0.03mm^2 Four-Way Time-Interleaved SAR ADC in 65nm CMOS," ***IEEE J. Solid-State Circuits***, under review.
9. **Lei Qiu**, Kai Tang, Yuanjin Zheng, Liter Siek, ChinYeong Goh, " A 10-bit 300MSs Asynchronous 2b/cycle SAR ADC with 2-bit Interpolation in 40nm CMOS," in preparation.
10. **Lei Qiu**, Kai Tang, Menghan Guo, Yuanjin Zheng, Liter Siek, " A 8-bit 5GS/s 50mW 8-channel Time-Interleaved SAR ADC with meta-stability cancellation in 65nm CMOS," in preparation.

Conference papers:

11. **Q. Lei**, Kai Tang, Y. Zheng, S. Liter, " A Digital Time Skew Calibration Technique for Time-Interleaved ADCs," in ***Proc. IEEE International Symp. Circuits and System* (*ISCAS*)**, 2015, Accepted.
12. **Q. Lei**, Y. Zheng, D. Zhu, S. Liter, "A Statistic Based Time Skew Calibration Method for Time-Interleaved ADCs," in ***Proc. IEEE International Symp. Circuits and System* (*ISCAS*)**, 2014, pp. 2373–2376.
13. **Q. Lei**, Y. Zheng, S. Liter, " Analysis and Design of High Performance Frequency-Interleaved ADC," in ***Proc. IEEE International Symp. Circuits and System* (*ISCAS*)**, 2013, pp. 2022- 2025.
14. Zhu Di, Wang Jiacheng, Siek Liter, Kok Chiang Liang, **Qiu Lei,** Zheng, Yuanjin, "High Accuracy Time-Mode Duty-Cycle-Modulation-Based Temperature

Sensor for Energy Efficient System Applications.” ***International Symposium on Integrated Circuits* (*ISIC*)**, 2014, pp. 400- 403.

BIBLIOGRAPHY

[1] S. Pithadia, “Smart Selection of ADC/DAC Enables Better Design of Software-Defined Radio,” [online]. Available: http://www.ti.com/lit/an/slaa407/slaa407.pdf .

[2] K. Roberts, D. Beckett, D. Boertjes, J. Berthold,C. Laperle, “100 G and beyond with digital coherent signal processing,” *IEEE Commun. Mag*., vol. 48, no. 7, pp. 62–69, 2010.

[3] P. Bower, I. Dedic, “High speed converters and DSP for 100 G and beyond,” *Opt. Fiber Technol.*, vol. 17, no. 17, pp. 464–471, 2011.

[4] Tektronix, “Techniques for Extending Real-Time Oscilloscope Bandwidth [white paper]” [online]. Available: http://www.tek.com/document/whitepaper /techniques-extending-real-time-oscilloscope-bandwidth.

[5] C. C. Liu, S. J. Chang, G. Y Huang, Y. Z. Lin, C. M. Huang, C. H. Huang, L. Bu, C. C. Tsai, “A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation,” in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 386-387.

[6] B. D. Sahoo, B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 48, no.6, pp. 1442-1452, Apr. 2013.

[7] C. Y. Chen, J. Wu, J. J. Hung, T. Li, W. Liu, W. Shih, " A 12-Bit 3 GS/s Pipeline ADC With 0.4mm^2 and 500mW in 40 nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no.4, pp. 1013-1021, Apr. 2012.

[8] A. Verma, B. Razavi, "A 10-Bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no.11, pp. 3039-3049, Nov. 2009

[9] A. N. Karanicolas, H. S. Lee and K. L. Barcrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1207-1215, Dec 1993.

[10] C. Tsang, Y. Chiu, J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen and B. Nikolic, "Background ADC calibration in digital domain," in *Proc. IEEE CICC*, 2008, pp.301-304.

[11] H. Wang, X. Wang, P. Hurst and S. H. Lewis, "Nested Digital Background Calibration of a 12-bit Pipelined ADC Without an Input SHA," *IEEE J. Solid-State Circuits*, vol. 44, no.10, pp. 2780-2789, Oct. 2009.

[12] Ishii, H., Tanabe, K., and Iida, T., "A 1.0V 40mW 10b 100MS/s Pipeline ADC in 90nm CMOS," in *Proc. IEEE CICC*, 2005, pp. 395-398.

[13] Murmann, B., and Boser, B. E., "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid-State Circuit*, vol. 38, no. 12, pp. 2040-2050, 2003.

[14] J. Hu, N. Dolev and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1057-1066, Apr. 2009.

[15] L. Qiu, Y. Zheng, L. Siek, "Source follower-based high-speed switched capacitor amplifier for pipelined ADCs," *Electronics Letters*, vol. 51, no. 1, pp.21-23, 2015.

[16] M. Elzakker, E. Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink and B. Nauta, "A 10-bit Charge-Redistribution ADC Consuming 1.9uW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1014, May. 2010.

[17] Z. Cao, S. Yan. Y. Li, "A 32mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13um CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp.862-873, 2009.

[18] C. C. Liu, S. Chang, G. Huang and Y. Ling, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, Apr. 2010.

[19] W. Liu, P. Huang and Y. Chiu, “A 12-bit, 45-MS/s, 3-mW Redundant Successive Approximation-Register Analog-to-Digital Converter With Digital Calibration,” *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 1-12, 2011.

[20] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara and K. Kobayashi, “Explicit analysis of channel mismatch effects in time-interleaved ADC systems,” *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, no. 3, pp. 261–271, Mar. 2001.

[21] T. H. Tsai, Hurst, P.J., Lewis, S.H., "Correction of Mismatches in a Time-Interleaved Analog-to-Digital Converter in an Adaptively Equalized Digital Communication Receiver," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol.56, no.2, pp.307-319, Feb. 2009.

[22] S. K. Gupta, M. A. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC With 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture," *IEEE J. Solid-State Circuits,* vol. 41, no.12, pp. 2650-2657, Dec. 2006.

[23] N. L. Dortz, *et al.*, “A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS,” *IEEE ISSCC Dig. Tech. Papers*, pp. 386-387, 2014.

[24] C. C. Huang, C. Y. Wang and J. T. Wu, “ A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques," *IEEE J. Solid-State Circuits*, vol. 46, no.4, pp. 848-858, Apr. 2011.

[25] L. Chi Ho, P. J. Hurst, and S. H. Lewis, "A Four-Channel Time-Interleaved ADC with Digital Calibration of Inter-channel Timing and Memory Errors," *IEEE Journal of Solid-State Circuit,* vol. 45, pp. 2091-2103, 2010.

[26] S. M. Louwsma, A. J. M. van Tuijl, M. Vertregt and B. Nauta, " A 1.35 GS/s, 10b, 175mW Time-Interleaved AD Converter in 0.13 μm CMOS," *IEEE J. Solid-State Circuits,* vol. 43, no.4, pp. 778-786, Apr. 2008.

[27] M. E. Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC With Background Timing Skew Calibration," *IEEE J. Solid-State Circuits*, vol. 46, no.4, pp. 838-847, Apr. 2011.

[28] S. Lee, A. P. Chandrakasan, H. S. Lee "A 1GS/s 10b 18.9mW Time-Interleaved SAR ADC with Background Timing-Skew Calibration," *IEEE ISSCC Dig. Tech. Papers*, pp. 384-385, 2014.

[29] C. C. Huang, C. Y. Wang and J. T. Wu, " A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques," *IEEE J. Solid-State Circuits*, vol. 46, no.4, pp. 848-858, Apr. 2011.

[30] H. Wei, P. Zhang, B. D. Sahoo and B. Razavi, "An 8Bit 4GS/s 120mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 47, no.11, pp. 2763-2772, Nov. 2014.

[31] V. Divi and G. Wornell, "Blind Calibration of Timing Skew in Time-Interleaved Analog-to-Digital Converters," *IEEE J. Selected Topics in Signal Processing*, vol.3, no.3, pp.509-522, June 2009.

[32] G. Y. Huang, S. J. Chang, Y. Z. Lin, C. C. Liu and C. P. Huang, "A 10b 200MS/s 0.82mW SAR ADC in 40nm CMOS," in *IEEE ASSCC Dig. Tech. Papers*, 2013, pp. 289-292.

[33] C. H. Chan, Y. Zhu, S. W. Sin, S. P. U and R. Martins, "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure," *IEEE Symp. VLSI Circuits*, pp. 86-87, June 2012.

[34] B. Verbruggen, M. Iriguchi, J. Craninckx, “A 1.7mW 11b 250MS/s 2× Interleaved Fully Dynamic Pipelined SAR ADC in 40nm Digital CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 466-467.

[35] S. S. Wong, U. F. Chio, Y. Zhu, S. W. Sin, S. P. U and Rui Paulo Martins, “A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC,” *IEEE J. Solid-State Circuits*, vol. 48, no.8, pp. 1783-1794, Aug. 2013.

[36] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Brändli, M. Kossel, T. Morf, T. M. Andersen and Y. Leblebici, “A 3.1 mW 8b 1.2 GS/s Single-Channel Asynchronous SAR ADC With Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS,” *IEEE J. Solid-State Circuits*, vol. 48, no.12, pp. 3049-3058, Dec. 2013.

[37] H. K. Hong, H. W. Kang, B. Sung, C. H. Lee, M. Choi, H. J. Park and S. T. Ryu, “An 8.6 ENOB 900MS/s Time-Interleaved 2b/cycle SAR ADC with a 1b/cycle Reconfiguration for Resolution Enhancement,” in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 470-471.

[38] Y. C. Lien, “A 4.5-mW 8-b 750-MS/s 2-b/step asynchronous subranged SAR ADC in 28-nm CMOS technology,” *IEEE Symp. VLSI Circuits*, pp. 88-89, June 2012.

[39] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, F. Maloberti, “A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 45, no.6, pp. 1111-1121, Jun. 2010.

[40] H.-K. Hong, et al., “A 7b 1GS/s 7.2mW Non binary 2b/cycle SAR ADC with Register-to-DAC Direct Control,” *IEEE CICC*, Sept. 2012.

[41] S. W. Chen and R. W. Brodersen, “A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, 2006.

[42] P. Harpe, C. Zhou, Y. Bi, N. Meijs, X. Wang, K. Philips, G. Dolmans and H. Groot, "A 26μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585-1595, Jul. 2011.

[43] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no.5, pp. 599–606, May 1999.

[44] Y. C. Huang and T. C. Lee, "A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 300-301.

[45] Y. Chai and J. T. Wu, "A 5.37mW 10b 200MS/s Dual-Path Pipelined ADC," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 462-463.

[46] C. J. Tseng, H. W. Chen, W. T. Shen, W C. Cheng and H. S. Chen, "A 10-b 320-MS/s Stage-Gain-Error Self-Calibration Pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1334-1343, Jun. 2013.

[47] B. N. Fang and J. T. Wu, "A 10-Bit 300-MS/s Pipelined ADC With Digital Calibration and Digital Bias Generation," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 670-683, Mar. 2013.

[48] C. C. Hsu, F. C. Huang, C. Y. Shih, C. C. Huang, Y. H. Lin, C. C. Lee, and B. Razavi, "An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 464-465.

[49] K. Doris, et al., "A 480mW 2.6GS/s 10b 65nm CMOS Time-Interleaved ADC with 48.5dB SNDR up to Nyquist," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 180-181.

[50] E. Janssen, K. Doris *et al.*, "An 11b 3.6GS/s Time-Interleaved SAR ADC in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp.464-465.

[51] S. Hashemi, B. Razavi, “A 7.1 mW 1 GS/s ADC With 48 dB SNDR at Nyquist Rate,*" IEEE Custom Integrated Circuits Conference*, Sept, 2013, pp. 1–4.

[52] S. H. W. Chiang, H. Sun and B. Razavi, “A 10-Bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no.4, pp. 935-949, Apr. 2014.

[53] E. Iroaga and B. Murmann, “A 12-Bit 75-MS/s Pipelined ADC Using Incomplete Settling,” *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 748-756, Apr. 2007.

[54] Y. Zhu, C. H. Chan, S. W. Sin, S. P. U and R. P. Martins, “A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC,” *IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 90-91.

[55] D. Stepanović and B. Nikolić,” A 2.8GS/s 44.6mW Time-Interleaved ADC Achieving 50.9dB SNDR and 3dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no.4, pp. 971-982, Apr. 2013.

[56] M. J. M. Pelgrom et al., “Matching properties of MOS transistors,” *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.

[57] Y. C. Jenq, “Digital Spectra of Nonuniformly Sampled Signals: Fundamentals and High-Speed Waveform Digitizers”, *IEEE Trans. on Instrumentation and Measurement*, vol. 37, no. 2, pp. 245-51, Jun. 1988.

[58] F. Kuttner, “A 1.2-V 10-b 20-Msample/s non binary successive approximation ADC in 0.13-µm CMOS,” *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 176-177.

[59] Ogawa, T *et al*, "SAR ADC that is configurable to optimize yield," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Dec. 2010, pp.374-377.

[60] S. W. Chen and R. W. Brodersen, “A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13µm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 2350-2359.

[61] G. D. Cain, N. P. Murphy, A. Tarczynski, "Evaluation of several variable FIR fractional-sample delay filters," in *IEEE Acoustics, Speech, and Signal Processing*, vol.3, pp. 621-624, Apr. 1994.

[62] C. W. Farrow, "A continuously variable digital delay element," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol.3, Jun. 1988, pp.2641-2645.

[63] Q. Lei, Y. Zheng, D. Zhu, S. Liter, "A Statistic Based Time Skew Calibration Method for Time-Interleaved ADCs," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2014, pp. 2373–2376.

[64] V. Divi and G. Wornell, "Blind Calibration of Timing Skew in Time-Interleaved Analog-to-Digital Converters," *IEEE J. Selected Topics in Signal Processing*, vol.3, no.3, pp.509-522, June 2009.

[65] B. Murmann, ADC Performance Survey 1997–2012 Stanford Univ. [Online]. Available: http://www.stanford.edu/ ~murmann/adcsurvey.html.

[66] Y. C. Lim, Y. X. Zou, J. W. Lee, S. C. Chan, "Time-Interleaved Analog-to-Digital-Converter Compensation Using Multichannel Filters," *IEEE Trans. Circuit and Syst. I: Regular papers*, vol.56, no.10, pp.2234-2247, Oct. 2009.

[67] A. Haftbaradaran, K.W. Martin, "A Background Sample-Time Error Calibration Technique Using Random Data for Wide-Band High-Resolution Time-Interleaved ADCs," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol.55, no.3, pp.234-238, March 2008.

[68] Camarero, D, Ben Kalaia, K, J. F. Naviner, P. Loumeau, "Mixed-Signal Clock-Skew Calibration Technique for Time-Interleaved ADCs," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol.55, no.11, pp.3676-3687, Dec. 2008.

[69] Chung-Yi Wang, Jieh-Tsorng Wu , "A Multiphase Timing-Skew Calibration Technique Using Zero-Crossing Detection," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol.56, no.6, pp.1102-1114, June 2009.

[70] Chung-Yi Wang; Jieh-Tsorng Wu; , "A background timing-skew calibration technique for time-interleaved analog-to-digital converters," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol.53, no.4, pp. 299- 303, April 2006.

[71] H. Jin and E. K. F. Lee, "A digital-background calibration technique for minimizing timing-error effects in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 47, no. 7, pp. 603–613, Jul. 2000.

[72] C. Tsang, Y. Chiu, J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen and B. Nikolic, "Background ADC calibration in digital domain," in Proc. *IEEE CICC*, 2008, pp.301-304.

[73] P. Vaidyanathan, "Theory and design of M-channel maximally decimated quadrature mirror filters with arbitrary M, having the perfect-reconstruction property," *IEEE Trans. Acoustics, Speech and Signal Processing*, vol. 35, pp. 476-492, 1987.

[74] A. Petraglia and S. K. Mitra, "High-speed A/D conversion incorporating a QMF bank," *IEEE Trans. Instrumentation and Measurement*, vol. 41, pp. 427-431, 1992.

[75] S. R. Velazquez, T. Q. Nguyen, and S. R. Broadstone, "Design of hybrid filter banks for analog/digital conversion," *IEEE Trans. Signal Processing*, vol. 46, pp. 956-967, 1998.

[76] S. H. Zhao and S. C. Chan, "Design and Multiplierless Realization of Digital Synthesis Filters for Hybrid-Filter-Bank A/D Converters," *IEEE Trans. Circuit and Syst. I Regular papers*, vol. 56, pp. 2221-2233, 2009.

[77] T. H. Tsai, Hurst, P.J., Lewis, S.H., "Correction of Mismatches in a Time-Interleaved Analog-to-Digital Converter in an Adaptively Equalized Digital Communication Receiver," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol.56, no.2, pp.307-319, Feb. 2009.

[78] T. H. Tsai, P. J. Hurst, and S. H. Lewis, "Bandwidth Mismatch and Its Correction in Time-Interleaved Analog-to-Digital Converters," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol.53, no.10, pp.1133-1137, Oct. 2006.

[79] S. Munkyo, M. J. W. Rodwell, and U. Madhow, "Comprehensive digital correction of mismatch errors for a 400-Msamples/s 80-dB SFDR time-interleaved analog-to-digital converter," *IEEE Trans. on Microwave Theory and Techniques*, vol. 53, pp. 1072-1082, 2005.

[80] B. Setterberg, K. Poulton, S. Ray, D. J. Huber, V. Abramzon, G. Steinbach, J. P. Keane, B. Wuppermann, M. Clayson, M. Martin, R. Pasha, E. Peeters, A. Jacobs, F. Demarsin, A. Al-Adnani, P. Brandt, "A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 466-467.

[81] S.M. Jamal, D. Fu, N.C-J Chang, P.J. Hurst and S.H. Lewis, "A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration," *IEEE J. Solid-State Circuits*, pp. 1618-1627, December 2002.

[82] J.-H. Tsai, et al., "A 0.003mm^2 10b 240MS/s 0.7mW SAR ADC in 28nm CMOS with digital error correction an correlated-reversed switching," *IEEE J. Solid-State Circuits*, vol 50, no. 6, pp. 1382-1398, June, 2015.