

A CMOS EQUIVALENT-TIME SAMPLING DIGITIZER FOR A DIRECT-MILLIMETER-WAVE UWB PULSE DOPPLER RADAR RECEIVER IMPLEMENTATION

GIBRAN LIMI JAYA

School of Electrical and Electronic Engineering

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research,
is free of plagiarised materials, and has not been submitted for a higher degree to
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Boon Chirn Chye

Authorship Attribution Statement

This thesis contains material from 1 paper published in the following peer-reviewed journal and material from 1 paper accepted at a conference in which I am listed as an author.

Section 2.2.1 is published as a chapter in G. L. Jaya, S. Chen, and L. Siek, "The design of clocked-comparator-based time-interval measurement circuit for pulse ToF measurement," *IEEE Sensors J.*, vol. 17, no. 20, pp. 6699 - 6706, Oct. 2017.

The contributions of the co-authors are as follows:

- A/Prof Chen provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by A/Prof Siek.
- I co-designed the study with A/Prof Chen and A/Prof Siek and performed all the measurement work at VIRTUS, IC Design Centre of Excellence, School of Electrical and Electronic Engineering, Nanyang Technological University. I also came out with the circuit study and analysis.

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The contributions of the co-authors are as follows:

- A/Prof Chen provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I designed and layout the circuit presented in the paper.
- I characterized the circuit and analyzed the results of the characterization.

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Summary

In the past ten years, various radar integrated circuits (IC) have been proposed in the literature, with some already been commercialized. While a radar IC designed to operate in the 3.1 - 10.6 GHz ultra-wideband (UWB) band has low cost and power consumption advantages, crowded spectrum usage in the band gives rise to various constraints in the radar IC's design and usage. In contrast, because of the directional operation of millimeter-wave (mm-wave) radio devices, spectrum crowding is less of an issue for a mm-wave radar device. Additionally, the radar cross sections (*RCS*) of radar targets, in general, increase with frequency. Together with the typically higher effective isotropic radiated power limits in mm-wave frequency bands, a mm-wave radar device can potentially be realized with a small antenna and, hence, a small form factor compared to its sub 10.6 GHz counterparts.

This work aims to design a low-power digitizer capable of digitizing a mm-wave radar pulse signal in bulk complementary metal-oxide-semiconductor (CMOS) technology. The digitizer design is meant to be used to implement a CMOS mm-wave UWB pulse-Doppler radar transceiver with a direct radio frequency (direct-RF) receiver. The receiver in such a radar transceiver must process narrow pulses and allow for adequately sensitive Doppler-shift measurements. Designing the radar transceiver with a direct-RF receiver allows for it to be designed with lower power consumption because a direct-RF receiver suffers less from flicker noise than its traditional super-heterodyne or homodyne counterparts. Additionally, without an explicit down-converter circuit, a direct-RF receiver does not need a mm-wave local oscillator (LO) signal, whose generation and distribution consume a lot of power.

In this work, a novel equivalent-time sampling analog-to-digital converter (ADC) architecture that can be used to design such a digitizer with acceptable attenuation level, low power consumption, and reduced input capacitance is proposed. The novel architecture is proposed assuming that the targets that are of interest to the pulse-Doppler radar under design have the characteristics of either a type I or type III Swerling target whose RCS does not fluctuate significantly within the radar's acquisition time.

At the heart of the proposed digitizer is a comparator bank whose comparators are designed for sampling and comparing a mm-wave frequency signal to some direct-current (DC) threshold values. In this work, each of these comparators is implemented as a 'bare' StrongARM latch circuit. Thus, a StrongARM latch circuit design capable of working with mm-wave input signals is analyzed in this work considering the circuit's linearity, noise, input range, and input capacitance.

A 4 GSa/s prototype of the proposed digitizer is designed and fabricated in a 40 nm low-power (LP) CMOS technology. The prototype is measured to be capable of digitizing signals with frequencies of up to 64 GHz while maintaining an effective number of bits ($ENOB$) of >3.2 bits. This performance is achieved with a power consumption of <20 mW and a modest figure of merit without needing the digitizer to be fabricated in a much more advanced CMOS technology node. It is also shown that the 60 GHz tuned amplifier circuit that is to drive the digitizer circuit can be designed with a gain that is more than enough to overcome the digitizer's 9 dB attenuation at 60 GHz while consuming <10 mW of power.

Lastly, the power consumption of a power-cycled 60 GHz UWB pulse-Doppler radar transceiver designed using the proposed digitizer is estimated assuming that the transceiver's end-use is for implementing a radar system whose uses are for monitoring human targets located at distances of less than 3 m from the radar system with a range resolution of <3.5 cm. The prospective design is then compared with some prior-art CMOS UWB pulse radar transceiver designs reported in the literature. It is shown that the transceiver design can consume <1.75 mW when the transceiver is power cycled with a duty cycle ratio of 0.35% for a radar scan update rate of 1 kHz. The energy usage efficiency of the prospective 60 GHz UWB pulse radar transceiver design is comparable to that of prior-art UWB pulse radar transceivers that operate at a much lower frequency band.

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List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DLL	Delay-Locked Loop
DNL	Differential Nonlinearity
EIRP	Effective Isotropic Radiated Power
ENOB	Effective Number of Bits
ESD	Electrostatic Discharge
ETS	Equivalent-Time Sampling
FMCW	Frequency-Modulated Continuous-Wave
IC	Integrated Circuits
INL	Integral Nonlinearity
ISF	Impulse Sensitivity Function
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low-Power
LSB	Least Significant Bit
LTV	Linear Time-Varying

mm-wave	millimeter-wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NF	Noise Figure
PA	Power Amplifier
PLL	Phase-Locked Loop
PRF	Pulse Repetition Frequency
PRI	Pulse Repetition Interval
Q-factor	Quality factor
RCS	Radar Cross Section
RF	Radio Frequency
RMS	Root Mean Square
RX	Receiver
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
T/H	Track-and-Hold
TDC	Time-to-Digital Converter
THD	Total Harmonic Distortion
TOF	Time-of-Flight
TX	Transmitter
UWB	Ultra-Wideband

Chapter 1

Introduction

1.1 Background and Motivation

Various radar integrated circuits (IC) have been proposed in the literature in the past ten years. These include those operating in the 3.1 - 10.6 GHz ultra-wideband (UWB) band [1-13], K/Ka-band [14-18], V-band [19-23], W-band [16, 24-27], and even the G-band [28, 29] with [2] and [7] already in commercialization. These radar ICs are designed for use in various applications, including healthcare, industrial monitoring and automation, building security and automation, automotive applications, and even applications in the consumer electronics market (such as the 60 GHz radar IC used to implement the touchless user interface in Google's Pixel 4 smartphone). Radar IC usage has lately become increasingly popular.

While a radar IC designed to operate in the 3.1 - 10.6 GHz band has the advantages of low cost and power consumption, crowded spectrum usage in the band gives rise to various constraints in the design and usage of the radar IC. In contrast, because of the directional operation of millimeter-wave (mm-wave) radio devices, spectrum crowding is less of an issue for a mm-wave radar device [30, 31]. Additionally, the radar cross sections (*RCS*) of radar targets, in general, increase with frequency [32-35]. Coupled with the typically higher effective isotropic radiated power (*EIRP*) limits in mm-wave frequency bands [36], a mm-wave radar device can potentially be realized with a small antenna and, hence, a small form factor as compared to that of its sub 10.6 GHz counterparts. Basically, if the targeted

application of a radar device requires a target that can stay within the radar's field of view to be monitored and requires the device to have a small form factor, it can be said that a mm-wave implementation of the device is a more suitable implementation for the device. An example of such an application is the portable monitoring of the breathing activity of a target that can be pinpointed beforehand (by the radar device's user, for example).

If the targeted application of a radar device requires both the distance to and Doppler shift of an object to be measured, the type of radar employed is usually either a pulse-Doppler radar or a frequency-modulated continuous-wave (FMCW) radar. Both radar types have their advantages and disadvantages. FMCW radars whose transceivers are realized in IC forms, even with their worse receiver noise figures (NF), typically have higher maximum ranging distances than the typical pulse radar designs. This is because, for the same integration duration, the amount of radio signal energy that an FMCW radar IC transmits to probe its surroundings can be several orders of magnitude higher than what a pulse radar IC can practically transmit [37, 38]. On the other hand, unintentional interferences between pulse radars are simpler to manage [38-40], which helps in the radars' usage proliferation. This work is interested in the design of a pulse-Doppler radar.

One of the main challenges in designing a mm-wave UWB pulse-Doppler radar IC is its circuitries' high power consumption. First, the generation and distribution of local oscillator (LO) signals in a mm-wave radio IC are very power-hungry. Figure 1-1 shows the results of our survey on the power used by the LO generation and distribution circuitries of prior-art 60 GHz Complementary Metal-Oxide-Semiconductor (CMOS) transceiver and stand-alone receiver ICs [41-47]. As shown in Figure 1-1, the amount of power used by the transceivers (in receive mode) or

receivers for the said purpose is typically more than 50% of their overall power consumption. Second, a UWB pulse-Doppler radar receiver must process narrow pulses and allow for adequately sensitive Doppler-shift measurements. If the receiver adopts the traditional superheterodyne or homodyne architecture (see Figure 1-2a), its power consumption will be very high due to the heavy design trade-offs between the power consumption, bandwidth, and flicker noise performance of its baseband circuitries. The flicker noise can significantly degrade the sensitivity of the radar's Doppler-shift measurements since the frequency of interest can be very low after down-conversion (for example, when human-related motions cause the Doppler shifts of interest) [33, 48].

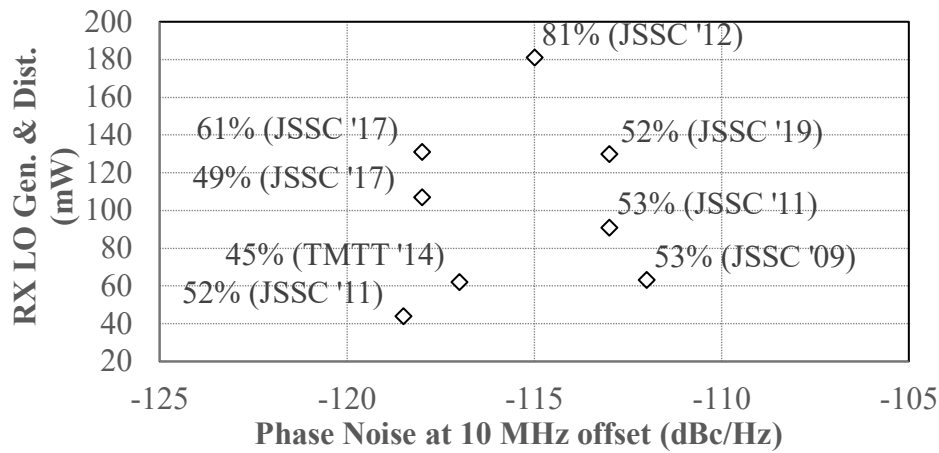


Figure 1-1 Percentage of power used for LO signals' generation and distribution in prior-art 60 GHz CMOS transceivers (in receive mode) or receivers [41-47]

The usual way to realize a UWB pulse radar IC with lower power consumption is by designing it with a non-coherent receiver [4, 6, 11] or a time-to-digital converter-based (TDC-based) receiver [1, 18]. However, a non-coherent UWB pulse radar (see Figure 1-2b) is incapable of measuring Doppler shifts since its receiver foregoes to process the phase of the carrier of the received radar echo signal. Meanwhile, a TDC-based UWB pulse radar (see Figure 1-2c) typically has a limited maximum ranging distance since, by its operating principle, it cannot employ averaging.

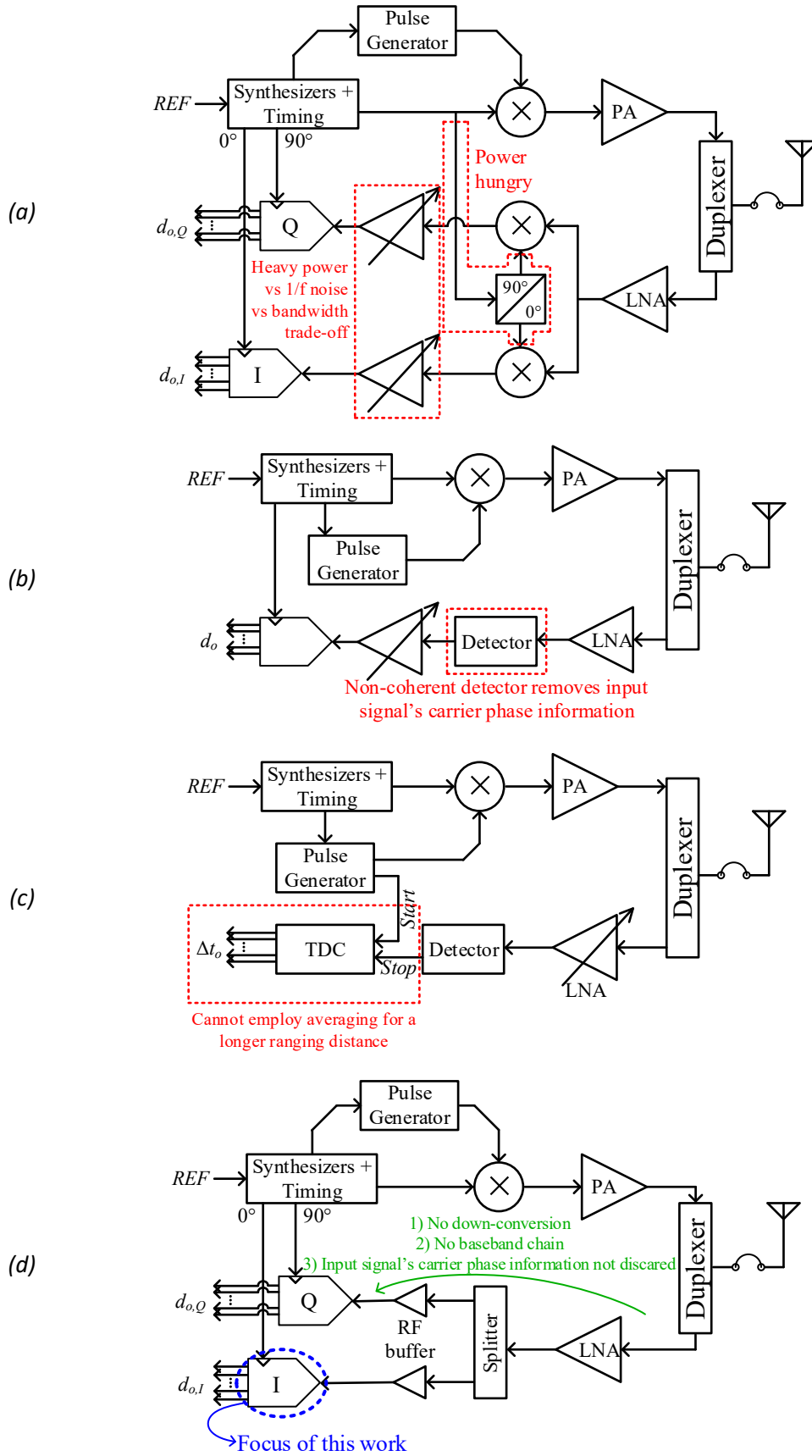


Figure 1-2 Block diagrams of mm-wave UWB pulse radar transceivers with a (a) homodyne receiver, (b) non-coherent receiver, (c) TDC-based receiver, and (d) direct-RF receiver with the advantages of the design that utilizes a direct-RF receiver highlighted

In this work, the use of direct radio frequency (direct-RF) receiver architecture for the implementation of a mm-wave UWB pulse-Doppler radar IC is proposed (see Figure 1-2d). A direct-RF receiver suffers less from the aforesaid power-hungry flicker noise versus bandwidth trade-off since it has no baseband circuit chain. The only flicker noise contributor in a direct-RF receiver is its digitizer. Since a digitizer is located at the end of a receiver chain, the effect of its flicker noise is reduced by the receiver's total gain. In contrast, in a non-direct-RF receiver, the effect of the receiver's major flicker noise contributor is reduced only by a portion of the receiver's total gain. Secondly, without a down-converter, the receiver does not require a mm-wave *LO* signal. Instead, it only requires a clock signal to clock a digitizer whose frequency is only in the low GHz range. Therefore, direct-RF receiver architecture allows a mm-wave UWB pulse-Doppler radar IC to be designed with reduced power consumption. The major hurdle in realizing this approach is in designing a digitizer that can directly digitize mm-wave UWB radar pulses with no prior down-conversion. As a note, the general-purpose analog-to-digital converters (ADC) in the literature are rarely reported with an input frequency range of >20-30 GHz [49, 50].

1.2 Objectives

This work focuses on the design of a digitizer that is capable of digitizing a mm-wave UWB radar pulse signal without a prior down-conversion. The digitizer must be of the "coherent" type to allow for the implementation of pulse-Doppler processing [51]. The radar's targets are assumed to have the characteristics of either type I or type III Swerling targets [32]. That is, their movements are assumed to be slow relative to the radar's scan update rate. Hence, their *RCS* are assumed to not fluctuate significantly within the radar's integration time.

Some considerations in the digitizer design are, first, the digitizer's parallel-equivalent input impedance at around the carrier frequency of the signal to be digitized should not be too low. Primarily, the digitizer's parallel-equivalent input resistance should effectively be more than approximately $300\ \Omega$ so that the mm-wave radio-frequency (RF) buffer driving the digitizer (see Figure 1-2d) can be designed with a power consumption of $<10\ \text{mW}$. Second, to be competitive, the digitizer's figure-of-merit (FoM) should not be much worse than that of a general-purpose ADC, whose value is typically in the hundreds of fJ/c-s . Third, the digitizer's maximum sampling rate must be at least several GSa/s so that a radar designed using the digitizer can be power-cycled with a low duty-cycle ratio ($<1\ \%$) while maintaining several hundred Hz to 1 kHz of radar scan update rate. Power cycling is essential for battery-operated radar implementations [1, 10]. Lastly, since a CMOS implementation of a radar IC is favored due to cost and integration considerations [52], the digitizer must be implementable in CMOS technology.

1.3 Major Contributions of the Thesis

This work adds the following contributions to the literature:

- 1) In this work, a novel flash-ADC-like equivalent-time sampling ADC architecture whose working principle is based on the concept of multi-pass analog-to-digital conversion [53] is presented. The novel ADC architecture allows for a mm-wave UWB radar pulse digitizer to be implemented in bulk CMOS technology with acceptable attenuation, low power consumption, and reduced input capacitance. Basically, unlike in a flash-ADC, the direct-current (DC) offsets of the comparators in a digitizer that is implemented based on the novel ADC architecture do not cause distortion and do not need to be reduced to less than

- a few least significant bits (*LSB*). That is, unlike in the case of a flash-ADC, the DC offsets calibration of the digitizer does not need to be highly accurate. Therefore, the practical range of the DC offsets calibration of the digitizer can be much wider compared to that of a typical flash-ADC design. In turn, this allows for the spread in the DC offsets of the comparators in the digitizer to be large. In addition, the digitizer can be implemented without its calibration-related circuitries causing an increased loading at the input signal path of the digitizer.
- 2) At the heart of the proposed mm-wave UWB radar pulse digitizer is a comparator bank whose comparators must be designed with the capability to sample and compare a mm-wave frequency signal to some DC threshold values. Along with this capability, the comparators must also be designed considering the linearity, noise, input range, and input capacitance of the digitizer. In this work, the design and analysis of such a comparator in bulk CMOS technology are presented. As a note, an ADC's sampling bandwidth is typically designed to be much higher than the frequency of the signal that the ADC must digitize. This is so that the linearity of the ADC is not degraded by the ADC's input-dependent sampling aperture delay [54, 55]. In the proposed digitizer's case, since the frequency of the signal of interest is in the mm-wave frequency range, the digitizer's sampling bandwidth is expected to be comparable to or even lower than the digitizer's input signal frequency. As a note, the digitizer's attenuation of its input signal, by itself, is not a problem since this can be compensated by some pre-amplification (as illustrated in Figure 1-3) or by reducing the full-scale input range of the digitizer. These, however, must be done while considering their effects on the linearity and noise performance of the digitizer.

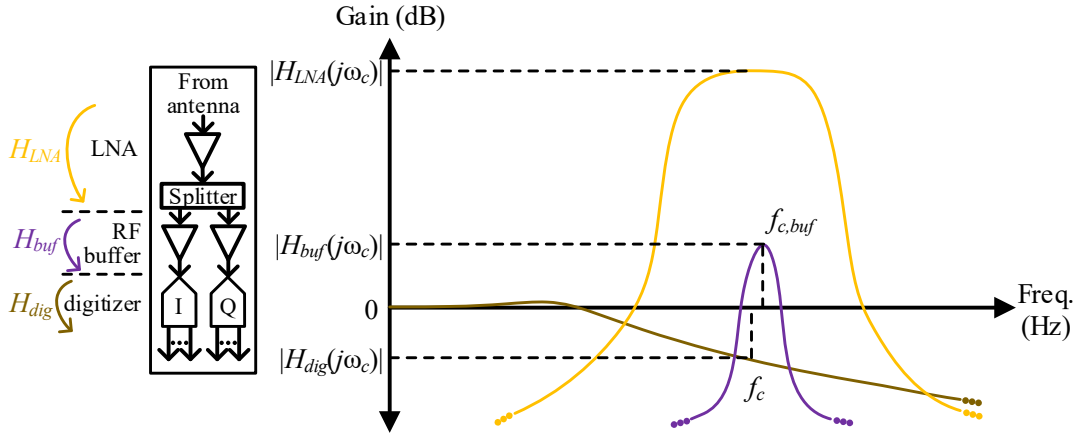


Figure 1-3 An illustration showing the transfer functions across the stages in the mm-wave UWB radar pulse receiver the proposed digitizer is meant to be used in; here, f_c is the carrier frequency of the radar pulse signal that must be processed, and $f_{c,buf}$ is the midpoint of the transfer function of the resonant-type RF buffer that drives the proposed digitizer; to compensate for $|H_{dig}|$'s slope at around f_c , $f_{c,buf}$ must be slightly higher than f_c

3) The proposed digitizer is meant to be used in the implementation of a mm-wave UWB pulse-Doppler radar IC. This work discusses how such a radar IC can be implemented using the proposed digitizer. This work then envisages the advantages of a 60 GHz UWB pulse-Doppler radar design implemented using the proposed digitizer compared to the more traditional radar designs found in the literature. In this way, this work promotes a direct-RF receiver to be used for a UWB pulse-Doppler radar IC implementation.

1.4 Organization of the Thesis

Following this chapter, this thesis is organized as follows.

Chapter 2 reviews the theory of quadrature under-sampling and coherent equivalent-time sampling to explain why the proposed mm-wave UWB radar pulse digitizer can be designed with a sampling rate lower than both the bandwidth and the frequency of the signal that must be digitized. The chapter then reviews the theory of impulse sensitivity function, which is essential to the design of sampling

circuits that need to work with a very high frequency input signal. The chapter also presents a literature survey on sampling circuits that work with signals whose frequencies are in the tens of GHz range. The discussions presented in the chapter lead to the proposal for the CMOS low-power equivalent-time sampling mm-wave UWB radar pulse digitizer design presented in a later chapter.

Chapter 3 discusses the working principle and calibration of the proposed flash-ADC-like equivalent-time sampling ADC architecture that allows for the design of a low-power and low-input-capacitance mm-wave UWB radar pulse digitizer in CMOS technology. The design of the digitizer's building blocks, especially its bank of comparators (which is the core of the digitizer), are then discussed in detail. The chapter concludes by discussing the implementation and measurements of a prototype of the digitizer, which is implemented in a Low-Power (LP) 40nm CMOS technology.

Chapter 4 discusses how a mm-wave UWB pulse-Doppler radar transceiver can be implemented with a direct-RF receiver using the proposed digitizer. The chapter also discusses how a 60 GHz UWB pulse-Doppler radar transceiver design implemented with the direct-RF receiver approach compares to the various UWB radar transceivers reported in the literature. The comparisons use an estimate of the proposed radar's performance as the proposed radar is not implemented in this work.

Lastly, chapter 5 concludes the works presented in this report. The chapter also discusses the future works ensuing from the works reported.

Chapter 2

Review of Direct Millimeter-Wave UWB Signal Sampling

In this chapter, the sub-Nyquist sampling theories used to reduce the sampling rate requirement of the proposed mm-wave UWB radar pulse digitizer design are discussed. The chapter then reviews the theory of impulse sensitivity function essential to the design of a sampling circuit that needs to work with a mm-wave frequency signal. The challenges in designing such a circuit in CMOS technology with low power consumption are then highlighted. All these lead to the proposal for the CMOS mm-wave UWB radar pulse digitizer design presented in chapter 3.

2.1 Sub-Nyquist Sampling

The Nyquist theorem mandates that a signal is sampled at a sampling rate that is more than double the maximum frequency component in the signal's spectrum. Whereas sub-Nyquist sampling relies on the information in which the signal's spectrum does not necessarily occupy the whole frequency range from DC until the highest frequency component in the signal's spectrum.

Under-sampling (or band-pass sampling) is one sub-Nyquist sampling technique that is usable when the spectrum of the signal of interest spans not from DC but only between a particular frequency range, e.g., between f_l and f_h . If a quadrature sampler is used, the signal can be sampled without aliasing at a rate that is equal to $(f_h - f_l)$. Therefore, if quadrature under-sampling is employed, the sampling rate required to sample the signal without aliasing can be reduced from $2 \bullet f_h$ to $(f_h - f_l)$.

Equivalent-time sampling is another sub-Nyquist sampling technique, which is the sub-Nyquist sampling technique used in sampling oscilloscopes and some sampler-based pulse radar receivers. Equivalent-time sampling is usable when the signal of interest is periodic (or approximately so), allowing it to be sampled at time $t + k \cdot T$ as if it is sampled at time t (T is the signal's period and k is an integer number).

Coherent equivalent-time sampling, which is a specific equivalent-time sampling implementation, can (or cannot) be done based on the value of i defined below:

$$i = \frac{f_s}{1/T - f_s} \quad (2-1)$$

in which f_s is the rate at which the periodic signal of interest is sampled. The most straightforward coherent equivalent-time is done by choosing f_s so that i is an integer. If i is an integer, no sample rearrangement is needed in reconstructing the sampled signal. If i is not an integer but still a rational number, a sample rearrangement is needed to reconstruct the sampled signal in the correct sequence. Lastly, if there is no way that i can be made a rational number, coherent equivalent-time sampling cannot be used.

In equivalent-time sampling, the effective sampling timing resolution ($\Delta t_{s,eff}$) and its inverse (i.e., the equivalent sampling rate, $f_{s,eff} = 1/\Delta t_{s,eff}$) can be defined. In either coherent equivalent-time sampling case (whether sample rearrangement is required or not required), $\Delta t_{s,eff}$ can be calculated as follows:

$$\Delta t_{s,eff} = \frac{(1/f_s) \cdot (1/T)}{LCM((1/f_s) \cdot (1/T))} \quad (2-2)$$

in which LCM is the least common multiple operator [56].

As a note, since the signal of interest is periodic, its spectrum will be discrete, and the distance between any adjacent spectral lines in the spectrum will always be equal to the inverse of T .

In the proposed mm-wave UWB radar pulse digitizer implementation, we combine quadrature under-sampling with coherent equivalent-time sampling to reduce the sampling rate required of the digitizer in digitizing a mm-wave UWB radar pulse signal without a prior down-conversion. Assuming that the radar's target object is moving very slowly, the echo signal that the radar receives will approximately be periodic. Since the echo signal originates from the radar system, the radar system has control over both the $1/T$ (i.e., the radar's pulse repetition frequency or PRF) and the f_s . Figure 2-1 illustrates how a mm-wave UWB radar pulse signal can be sampled using both quadrature under-sampling and equivalent-time sampling. As illustrated, the required sampling rate can be reduced substantially.

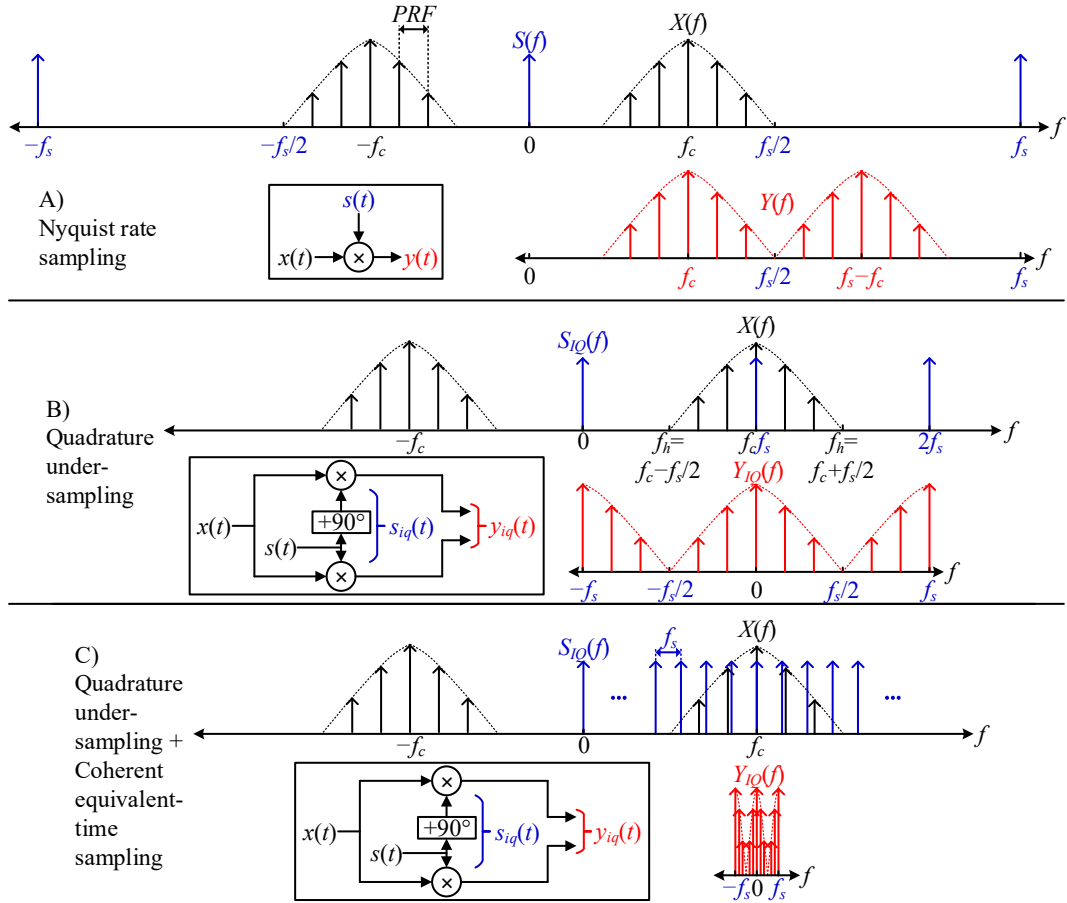


Figure 2-1 Employing quadrature under-sampling and coherent equivalent-time sampling to reduce the frequency of the clock signal, $s(t)$, of a digitizer that digitizes a mm-wave UWB radar pulse signal, $x(t)$; f_c here is the radar pulse signal's carrier frequency

2.2 Millimeter-Wave Sampling Circuits

Sampling circuits can broadly be categorized into two major categories, i.e., those whose outputs track their input signals before sampling the signals and those that do not. An example of a sampling circuit that tracks its input signal before sampling the signal is the simple NMOS track-and-hold (T/H) circuit shown in Figure 2-2a. Meanwhile, an example of a sampling circuit that does not track its input signal before sampling the signal is the StrongARM latch comparator shown in Figure 2-2b.

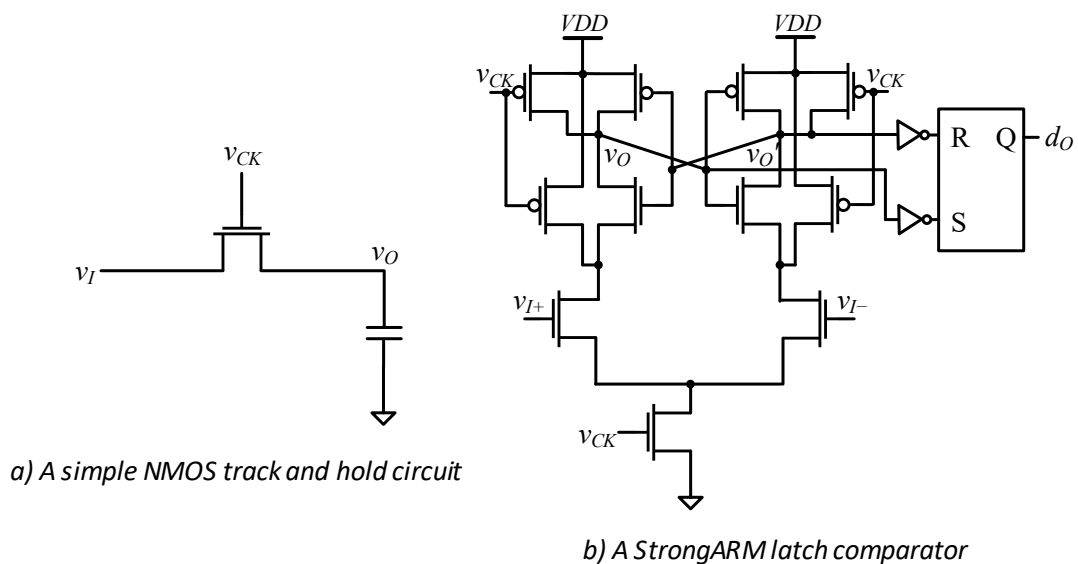


Figure 2-2 Example of a sampling circuit that (a) tracks (b) does not track its input signal before sampling the signal

For both types of sampling circuits, if the circuits are designed for sampling signals whose frequencies are very high, the assumption that the circuits can sample their input signals instantaneously is no longer valid. In the case of the simple NMOS track and hold circuit shown in Figure 2-2a, the circuit's sampling bandwidth is no longer determined solely by the circuit's R-C time constant during its tracking phase. The reason is that the clock signal controlling the NMOS switch in the circuit does not have an infinite slew rate [57].

The non-instantaneous sampling process of a sampling circuit manifests in a low-pass filter effect in which the sampling circuit applies a weighted averaging process across time on its input signal as the circuit is sampling the signal. The duration within which this weighted averaging process is occurring is usually called the aperture time. Meanwhile, the function that describes how the weight factor in the weighted averaging process varies across time is usually called the impulse sensitivity function (ISF) of the sampling circuit.

Section 2.2.1 further discusses the ISF of a sampling circuit. Since this work, later on, deals with the design of a clocked comparator circuit, the sampling circuit used in the discussion is a clocked comparator circuit (clocked comparators are also called dynamic comparators in the literature).

2.2.1 Impulse Sensitivity Function (of a Clocked Comparator Circuit)

Figure 2-3 shows a model that describes the operation of a clocked comparator circuit [58, 59]. The model substitutes the clocked comparator circuit with a subtractor, a linear time-varying (LTV) filter, an ideal sampler, and a slicer. The model assumes that the clocked comparator circuit processes the difference between the voltage values of its input signals, $v_i(t) = v_{i+}(t) - v_{i-}(t)$, linearly before the circuit decides on a logic “1”/“0” output.

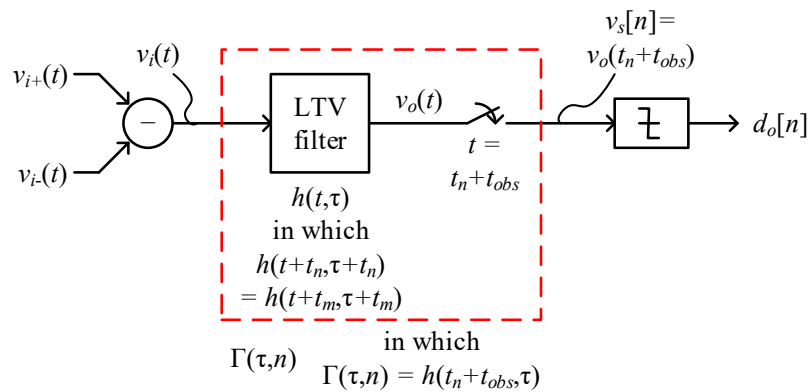


Figure 2-3 A model describing the operation of a clocked comparator circuit [58, 59]

$h(t, \tau)$ in Figure 2-3 is the impulse response function of the LTV filter block in the clocked comparator circuit model. Two time-domain variables are needed to describe the impulse response function since the filter's response to an impulse input depends on the impulse signal's arrival time, τ , relative to the instant at which the comparator circuit that the model represents is strobed, t_n . Therefore, the output of the LTV filter block, $v_o(t)$, can be described by the following equation:

$$v_o(t) = \int_{-\infty}^{+\infty} v_i(\tau) \cdot h(t, \tau) \cdot d\tau \quad (2-3)$$

The output of the LTV filter block, $v_o(t)$, is subsequently instantaneously sampled by the ideal sampler block in the model t_{obs} seconds after the comparator circuit that the model represents is strobed at t_n . Therefore, $v_s[n]$, which is the output of the ideal sampler block, is basically v_o 's value at $t_n + t_{obs}$, in which n is an integer index.

The overall output of the clocked comparator circuit model, $d_o[n]$, is either a logic "1"/"0" depending on $v_s[n]$'s value. $d_o[n]$ is a logic "1" if $v_s[n]$ is >0 and vice versa. Hence, $d_o[n]$'s value depends on whether the result of the following integration is >0 or <0 :

$$v_s[n] = v_o(t_n + t_{obs}) = \int_{-\infty}^{+\infty} v_i(\tau) \cdot \Gamma(\tau, n) \cdot d\tau \quad (2-4)$$

in which $\Gamma(\tau, n) = h(t_n + t_{obs}, \tau)$.

As a note, the above assumes that the LTV filter in the model always responds the same way every time the clocked comparator circuit that the model represents is strobed. Therefore, if the clocked comparator circuit is strobed at, say, $t = t_n$ and $t = t_m$ (n and m are integer indexes), $h(t + t_n, \tau + t_n)$ will always be equal to $h(t + t_m, \tau + t_m)$ for any n and m because the LTV filter's responses related to these strobes have entirely died down first before a subsequent strobe is applied. This assumption is valid if the clocked comparator circuit is not clocked at too high of a rate.

Figure 2-4 and Figure 2-5 illustrate the clocked comparator circuit's sampling process discussed earlier.

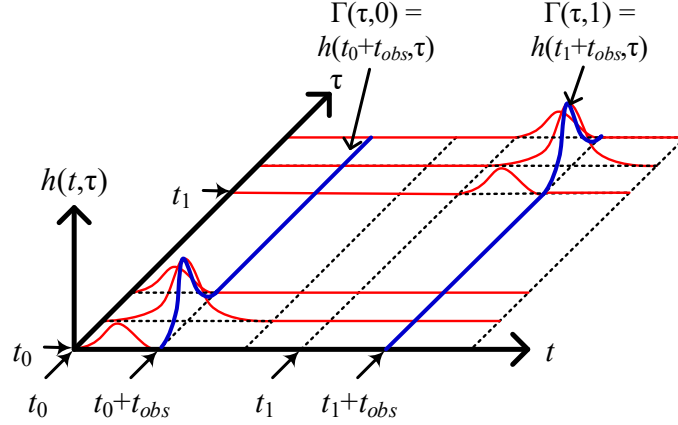


Figure 2-4 The time-varying impulse response function of the LTV filter block in the clocked comparator circuit model given in Figure 2-3; here, the comparator is strobed at $t=t_0$ and t_1

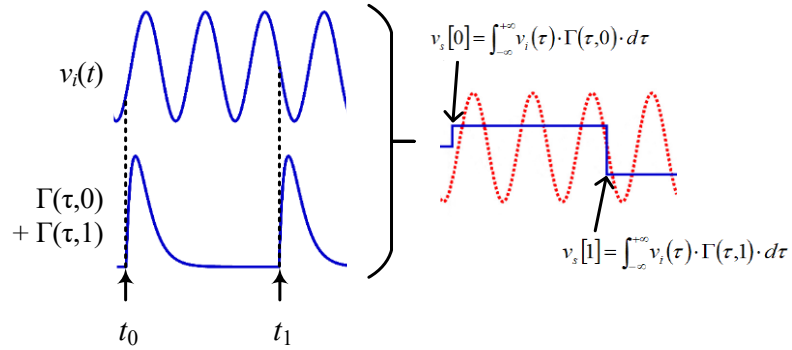


Figure 2-5 An illustration of how $v_s[n]$ comes about every time the clocked comparator circuit that is represented by Figure 2-3 is strobed

Assuming that $\Gamma(\tau) = \Gamma(\tau, n) = \Gamma(\tau, m)$, $\Gamma(\tau)$ here is the ISF of the clocked comparator circuit, that is, it is the circuit's weighting factor function which the circuit applies to its input signal every time the circuit is strobed to sample the signal. If we can slide the strobing position of the comparator with infinitesimal time increment and record the corresponding v_s value for each strobe position, the resulting continuous-time waveform is the cross-correlation between v_i and Γ . In frequency domain:

$$V_s(j\omega) = V_I(j\omega) \cdot \Gamma^*(j\omega) \quad (2-5)$$

in which $*$ is the complex conjugate unary operator and $V_s(j\omega)$, $V_I(j\omega)$, and $\Gamma(j\omega)$ are the Laplace transform of $v_s(t)$, $v_i(t)$, and $\Gamma(\tau)$, respectively.

2.2.2 Literature Survey

This work aims to design a low-power digitizer capable of digitizing mm-wave frequency signals (signals whose frequencies are >30 GHz) in CMOS technology. The maximum sampling rate of the digitizer is of secondary concern since, as discussed in section 2.1, quadrature under-sampling and coherent equivalent-time sampling can be used to reduce the sampling rate required of the circuit given the nature of the signal that requires digitization in the digitizer's targeted application. Nevertheless, the digitizer's sampling rate still needs to be at least several GSa/s.

Table 2-1 reports the results of our literature survey on sampling circuits designed for sampling signals whose frequencies are >10 GHz. As shown in Table 2-1, such a sampling circuit is typically designed with a sampling rate of >10 GSa/s and consumes much more than 10 mW of power. The bandwidths of some of these circuits are <30 GHz, which is not a problem if the circuits can maintain their signal-to-noise and distortion ratio (*SNDR*) performance when they sample a >30 GHz signal. Input signal attenuation can be compensated, for example, by digital post-processing, as mentioned in [60].

Table 2-1 Survey of prior-art sampling circuit designs with >10 GHz of input signal frequency

	IMS '14 [61]	JSSC '14 [62]	TCASII '16 [63]	JSSC '18 [60]	JSSC '19 [64]	BCICTS '18 [65]	APMC '19 [66]	RFIC '19 [67]	ICECS '20 [68]	ISCAS '20 [69]
Fabrication Technology	65 nm CMOS	65 nm CMOS	28 nm CMOS	14 nm FinFET CMOS	28 nm CMOS	55 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS
f_s (GS/s)	32.5	12.8	25	72	56	16 32	5	112	32	10
Interleaving?	Yes, 2 ways	Yes, 32 ways	No	Yes, 64 ways	Yes, 64 ways	No	No	Yes, 4 ways	No	No
Large-Signal -3 dB Bandwidth (GHz)	-	25	55	21	31.5	19 9	70 (-1 dB)	-	58	61
Input Range (V_{pk-pk})	0.16	0.3	0.8 0.4	0.65	0.6	2	0.35	0.5	1	0.45
$THD @ f_{in}$ (dB @ GHz)	-25 @ 16	-	-28 -32 @ 50	-45.7 ⁺ @ 36	-	-38 -32 @ 18.5	-23 @ 60	-	-18 @ 58	-41 @ 61
$SNDR @ f_{in}$ (dB @ GHz)	-	26.4 ⁺ @ 25	27 30 @ 50	30.4 ⁺ @ 36	33 ⁺ @ 27	-	22 @ 60	28 @ 43	-	40 @ 61
Power (mW)	192	125 [#] 43.5 [^]	73	77 [#]	493 [#] 291 [^]	1020 284 [*]	1,100	3,340 2,280 [^]	1,800 685 [*]	375

[#] Without ADC's power consumption
of the whole ADC circuit

[^] Interleaver's power consumption only
^{*} Track and hold circuit's power consumption only

[66] and [69] present sampling circuit designs whose electrical performances are suitable given the targeted application of the digitizer design discussed in this work. Each has >60 GHz of bandwidth, >20 dB of *SNDR* at around 60 GHz, and can operate at a sampling rate of more than several GSa/s. However, these sampling circuits are designed in SiGe BiCMOS technology and consume more than several hundreds of mW of power. A sampling circuit must not consume much more than 10 mW of power in a low-power direct mm-wave receiver design.

Meanwhile, the 28 nm CMOS sampling circuit whose design is reported by [63] achieves a large-signal –3dB bandwidth of 55 GHz and maintains an *SNDR* of around 30 dB as it samples a signal with up to 67 GHz of frequency. The circuit consumes 73 mW and operates with a sampling rate of 25 GSa/s. However, redesigning this circuit for operation at $1/5^{\text{th}}$ the quoted maximum sampling rate may not result in the circuit consuming <20 mW of power. A significant portion of the circuit's power consumption is static power consumption that does not scale with the circuit's sampling rate.

Lastly, some of the CMOS sampling circuits listed in Table 2-1 are interleavers used in time-interleaved ADC designs [60, 62, 64]. Each is capable of sampling >20 GHz signals while maintaining an *SNDR* of >25 dB. Arguably, after stripping off their interleaving-related circuitries (since the digitizer design discussed in this work does not require interleaving), the resulting sampling circuit may perform better than the original design reported in the corresponding literature while consuming a sufficiently low amount of power. However, as will be discussed in section 2.2.2.1, 2.2.2.2, and 2.2.2.3, the power consumption of some of these sampling circuits can be improved, and an architectural level optimization can be done to reduce the overall digitizer power consumption further.

2.2.2.1 CMOS Sampling circuit with a cascaded T/H stage

The CMOS high-frequency sampling circuits presented in [60, 63, 64] all have a similar basic structure. Their general architecture is illustrated in Figure 2-6 below.

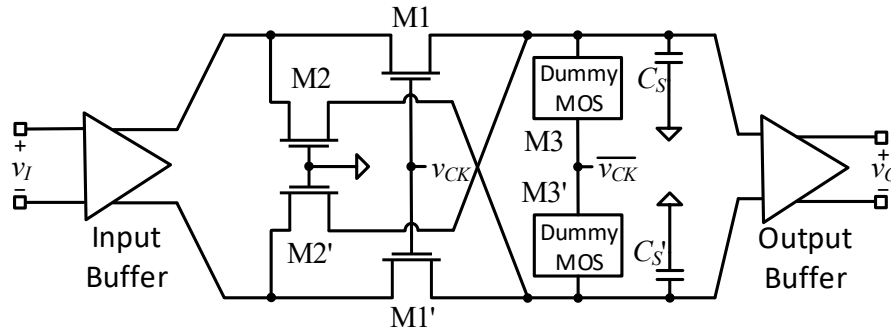


Figure 2-6 The general architecture of the high-frequency sampling circuits presented in [60, 63, 64]

The T/H switches in the sampling circuits are implemented as bare NMOS transistors, shown as M1 and M1' in Figure 2-6. The T/H switches avoid the use of PMOS transistors (to realize transmission gates) in their implementations because PMOS transistors are “slow”. Moreover, the T/H switches also avoid the use of bootstrapping in their designs because bootstrapping implementation is significantly challenging when the input signal frequency of interest is very high.

Since the frequencies of the input signals that are of interest to the sampling circuits are very high, one of the circuits' design aims is to maximize their tracking bandwidths. The on-resistances of the T/H switches in the circuits must thus be minimized. In the sampling circuit presented in [63], the on-resistances are minimized by having the v_{CK} signal in the circuit swings above the maximum allowed supply voltage level. Meanwhile, the input buffer in the sampling circuit presented in [64] is powered using a dual $\pm$ supply voltage so that the buffer can have a near-ground output common-mode level. Lastly, the sampling circuit presented in [60] avoids the use of an input buffer altogether in its design and requires that the common-mode level of the signal input into the circuit is near ground level.

On top of having their T/H switches designed with low on-resistances by maximizing the overdrive voltages of the switches, the T/H stages in the sampling circuits presented in [60, 63, 64] are also designed with small output capacitances. Thus, clock feedthroughs through the T/H switches in the T/H stages may be enough to cause the voltage levels at the outputs of the T/H stages to fall lower than the gate voltage levels of the T/H switches in hold mode, causing hold-mode leakages. Therefore, the dummy switches M3 and M3' shown in Figure 2-6 are added to the sampling circuits' designs to compensate for the output voltage drops caused by the feedthroughs.

Lastly, as illustrated in Figure 2-6, each of the sampling circuits presented in [60, 63, 64] has a cross-coupled transistor pair (shown as M2 and M2' in Figure 2-6) added across the T/H switch pair in the circuit. The cross-coupled transistor pair's function is to cancel the input signal feedthrough corrupting the voltage values held at the output nodes of the T/H stage in the circuit. The size of these transistors must be matched to that of the T/H switches in the circuit. Therefore, these transistors add substantial parasitic capacitances to both the input and output nodes of the T/H stage in the circuit.

With the addition of the dummy switches and the use of an input and output buffer, the sampling circuits presented in [60, 63, 64] are not very power efficient. The buffers and dummy switches in the designs consume some static power and add sizeable dynamic power consumptions. Moreover, the signal feedthrough compensation transistors in the circuits also load the input buffers in the circuits. The additional loading can pose a challenge in the buffer circuit's design since the pole caused by the capacitances at the output of the buffer should ideally not significantly affect the bandwidth of the sampling circuit under design.

2.2.2.2 CMOS Sampling circuit with cascoded T/H switch

The CMOS sampling circuit presented in [62] addresses some of the CMOS sampler design challenges discussed in section 2.2.2.1. The sampling circuit's general architecture is given in Figure 2-7. As shown, the sampling operation in the sampling circuit is merged into the circuit's input buffer. This configuration also allows for the sampling circuit to be designed with a higher sampling bandwidth [62].

In the sampling circuit whose general configuration is shown in Figure 2-7, the common-mode voltage level at the top plate of the sampling capacitor in the circuit, C_S , can be more flexibly chosen. Therefore, this circuit requires no clock feedthrough compensation. It is noted in [62] that clock feedthrough and charge injection are not significant sources of non-linearities for a sampling circuit design whose targeted effective-number-of-bits (*ENOB*) performance is only around 5 bits. Also, since the common-mode voltage level at the input of the output buffer in the sampling circuit can be chosen more flexibly, the buffer can be implemented without utilizing a folded-cascode structure, which helps to lower the buffer's design complexity and, ultimately, power consumption. Lastly, as discussed in [62], the sampling circuit can be implemented without employing the signal feedthrough compensation transistors needed in the sampling circuit implementations discussed in section 2.2.2.1, further improving the circuit's power efficiency.

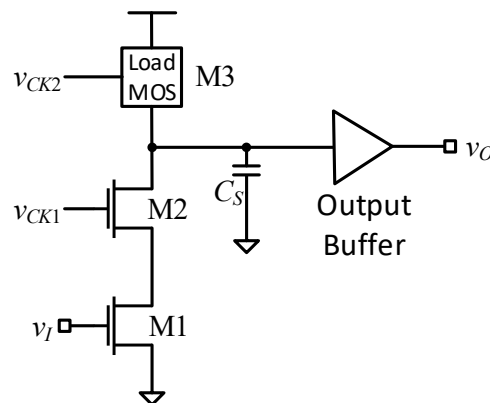


Figure 2-7 The general architecture of the high-frequency sampling circuit presented in [62]

2.2.2.3 *The proposed approach*

In this work, we perform some further optimizations compared to the optimizations done in the CMOS high-frequency sampling circuit design discussed in the previous section (i.e., section 2.2.2.2). In the mm-wave UWB radar pulse digitizer design proposed in this work, the sampling function of the digitizer is merged into the input signal comparators of the digitizer, which are each implemented as a StrongARM latch circuit. Therefore, the digitizer circuit, architecturally, does not have an explicit sampling circuit. This approach is possible if the StrongARM latch circuit used in the digitizer's design is designed to work with a mm-wave input signal. The design of such a StrongARM latch circuit is discussed in section 3.2.1 of this work.

In pursuing this approach, the digitizer circuit cannot be designed based on some traditional ADC architecture. In a flash-ADC circuit, for example, the comparators in the ADC typically share a track-and-hold circuit. One of the track-and-hold circuit's primary functions is to mitigate the distortions caused by the sampling timing skews among the comparators in the ADC. The distortions caused by these skews worsen as the input signal frequency of interest increases. Therefore, in this work, we propose a novel flash-ADC-like equivalent-time sampling ADC architecture whose operating principle is based on the concept of multi-pass analog-to-digital conversion [53], which is immune to the effect of said sampling timing skews. The discussions on the novel ADC architecture are presented in section 3.1.3 of this work.

Lastly, the signals that are of interest to the digitizer design proposed in this work are modulated pulse signals whose spectrums occupy some frequency ranges away from 0 Hz. Therefore, the digitizer's input buffer does not need to be designed with a very wide and flat frequency response starting from 0 Hz. Instead, the input buffer can be implemented as an RF buffer whose transfer function is tuned for operation with a particular center frequency.

Table 2-2 below summarizes the differences between the CMOS high-frequency sampling circuit design approaches reviewed in this work, including the approach adopted in the mm-wave UWB radar pulse digitizer design proposed in this work. As shown in the table, the proposed approach requires the least overhead compared to the other approaches.

Table 2-2 Comparisons between the different CMOS high-frequency sampling circuit design approaches reviewed in this work

	Input Buffer	Sampling Function	Input Signal Feedthrough Compensation	Clock Feedthrough Compensation	Output Buffer
Sampling Circuit with Cascaded T/H Stage [60, 63, 64]	Requires a high-frequency buffer design that is capable of operating with a suitable output common-mode voltage level	Implemented as a separate T/H stage	A cross-coupled transistor pair must be added across the circuit's T/H switch pair	Sizeable dummy switches that are clocked by the inverse of the circuit's T/H switches' clock signal must be added to the output of the T/H stage in the circuit	Requires a buffer design that is capable of operating with a suitable input common-mode voltage level
Sampling Circuit with Cascode T/H Switch [62]	T/H function is merged into the circuit's high-frequency input buffer's design		Not required		Possibly implemented as a simple buffer stage
Proposed approach*	Implemented as an RF buffer that is tuned for operation with a particular center frequency	Merged into each StrongARM latch comparator in the digitizer circuit	Not required		

* Digitization function included

Chapter 3

A CMOS Equivalent-Time Sampling Digitizer for Millimeter-Wave Ultra-Wideband Radar Pulse Signal Digitization

One of the challenges in designing a mm-wave UWB pulse-Doppler radar IC is the high power consumption of its circuitries. As discussed in chapter 1, the use of direct-RF architecture in the radar's receiver design (see Figure 1-2d) can reduce the radar's power consumption. The major hurdle in realizing this approach is in designing the digitizer in the receiver, which must be capable of digitizing a mm-wave UWB radar pulse signal directly without a prior down-conversion.

This chapter presents the design of a CMOS equivalent-time sampling mm-wave UWB radar pulse digitizer with low power consumption and reduced input capacitance. In the digitizer, several multi-pass ADCs, which are each an equivalent-time sampling flash ADC implemented using only 1 comparator, are operated together. The digitizer requires neither a complicated nor a time-consuming calibration. Also, the circuitries needed to implement the calibration do not load the digitizer's input signal path.

On top of its architecture, this chapter also discusses the design of the digitizer's building blocks—particularly the digitizer's bank of comparators, which needs to work with a mm-wave input signal. The chapter ends with a discussion on the implementation and measurements of a prototype of the digitizer. The prototype is designed and fabricated in an LP 40nm CMOS technology.

3.1 ADC Architecture for Mm-Wave UWB Radar Pulse Signal Digitization

3.1.1 Motivation

In general, the thresholds of the comparators in a flash ADC must not be away from their intended values by more than a fraction of the least significant bit (*LSB*) size of the ADC. This requirement is so that the ADC's linearity is acceptable for the design's intended resolution. Conventionally, this is achieved by sizing up the devices that make up the comparators in the ADC until the variation in the DC offsets of the comparators is sufficiently low. If the requirement is so that the ADC has "no missing codes", the following equation must then be fulfilled:

$$C \cdot \sqrt{2} \cdot \sigma(V_{OFF}) < V_{FS} \cdot 1/2^B \quad (3-1)$$

in which C is some constant that is related to the yield target of the design, $\sigma(V_{OFF})$ is the standard deviation of the random DC offsets of the comparators in the ADC, and $V_{FS} \cdot 1/2^B$ is equal to the *LSB* size of the ADC (V_{FS} is the ADC's full-scale input range and B is its resolution). If $C = 3$, for example, the chance for the ADC to miss a particular output code is equal to $\sim 0.135\%$ (assuming that the offsets are normally distributed). Now, the standard deviations of the random mismatches that give rise to a comparator's DC offset are typically inversely proportional to the square root of the area usages of the devices that make up the comparator [55]:

$$\sigma(V_{OFF}) = \sqrt{A_1/Area_1 + A_2/Area_2 + \dots + A_U/Area_U} \quad (3-2)$$

in which $A_u = \{A_1, A_2, \dots, A_U\}$ are some constants and $Area_u = \{Area_1, Area_2, \dots, Area_U\}$ are the corresponding area usages of the devices. Basically, in designing a flash ADC, if the conventional approach of upsizing the devices that make up the ADC is used, the resulting devices' sizes may cause the ADC to fall short in terms of its area, power consumption, sampling rate, and input capacitance.

Instead of sizing up the devices that make up their comparators, modern high-speed flash ADCs typically rely on some form of calibration to reduce [70-73] or compensate for [74-77] the mismatches of their comparators so that their threshold errors variation can be reduced. However, a practical implementation of the calibration can only correct for a limited range of offsets and never eliminate the threshold errors. The range and accuracy of the DC offsets calibration of a flash ADC typically trade with the ADC's input capacitance and area usage.

In the flash ADC designs that are reported in [70] and [72] (whose DC offsets calibration approach is illustrated by Figure 3-1a), the number of redundant comparators in the ADCs must be increased to lower the ADCs' post-calibration threshold errors variation. Similarly, in the flash ADC designs that are reported in [71] and [73] (whose DC offsets calibration approach is illustrated by Figure 3-1b),

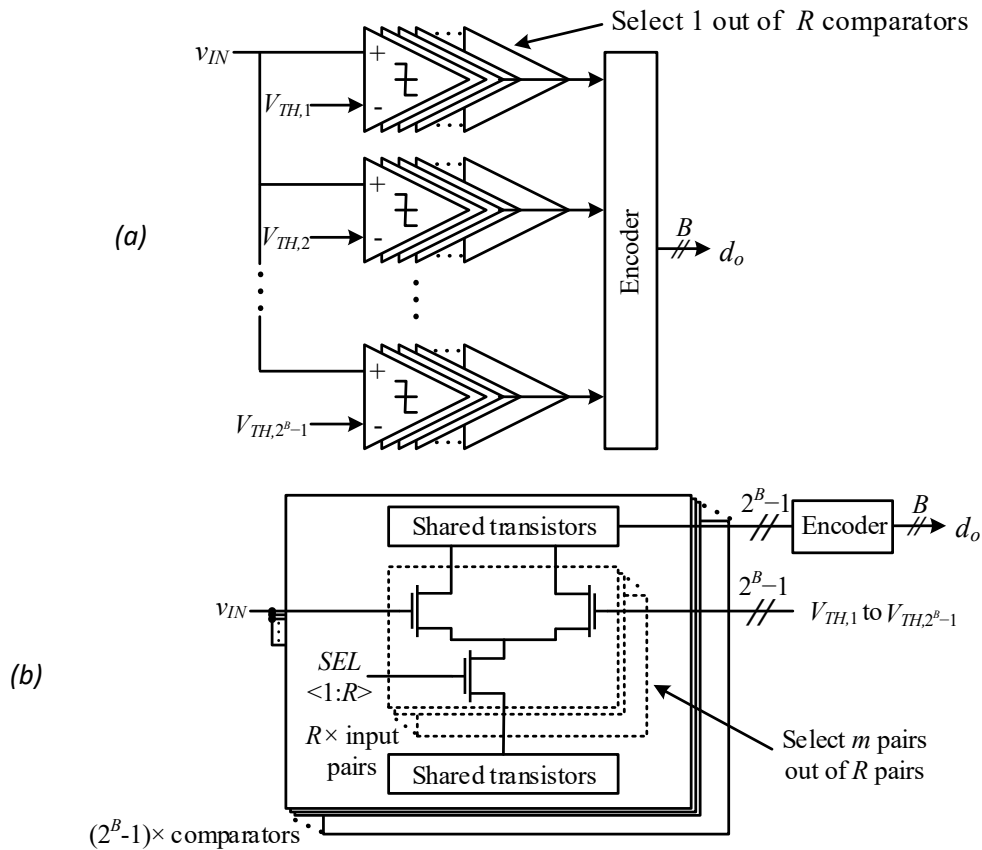


Figure 3-1 Flash ADC designs with (a) redundant comparators [70, 72] and (b) redundant sub-selectable comparator input pairs [71, 73]

the number of redundant input pairs in each comparator in the ADCs must be increased to lower the ADCs' post-calibration threshold errors variation.

In the flash ADC whose design is reported in [74], a pair of binary-weighted capacitor banks are added to the internal nodes of each comparator in the ADC for DC offsets calibration purposes, as shown in Figure 3-2. These capacitors increase the total capacitance that the comparators must toggle in each conversion. Besides increasing the ADC's total power consumption, these capacitors will also indirectly increase the ADC's input capacitance, especially if the ADC's sampling rate requirement is high.

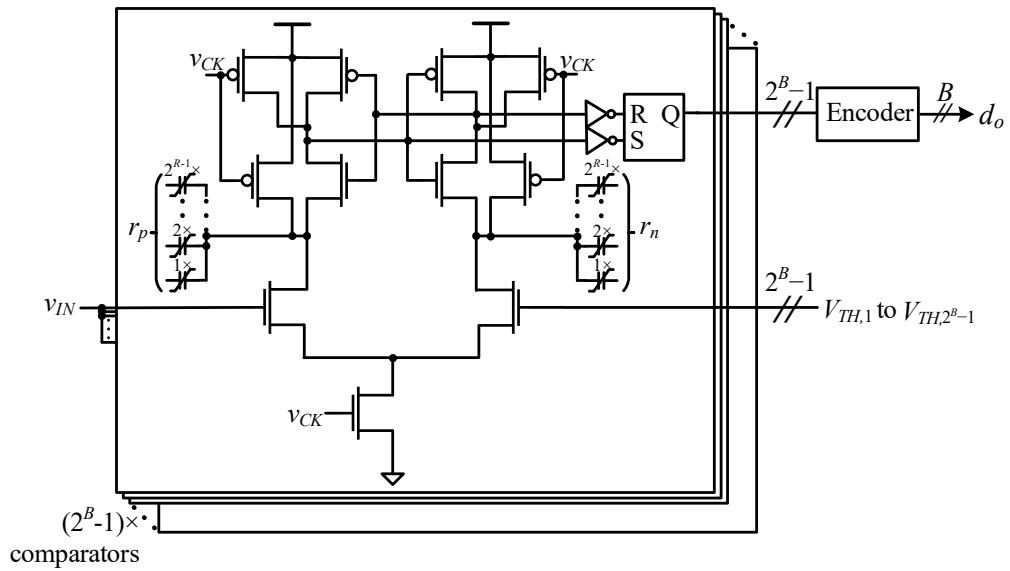


Figure 3-2 A flash ADC design whose StrongARM-latch-based comparators are calibrated using pairs of binary-weighted capacitor banks [74]

The thresholds of the flash ADCs whose designs are reported in [76] and [77] are corrected by adjusting the back-gate biases of some transistors in their comparators, as illustrated by Figure 3-3. This method, however, can only correct for a limited range of threshold errors. Therefore, the DC offsets of the comparators in the ADCs must still be relatively low. This limits the minimum transistors' size in the comparators.

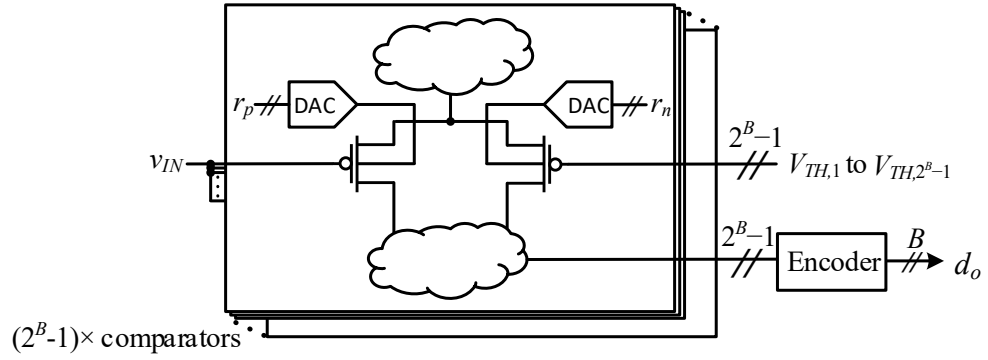


Figure 3-3 A flash ADC design whose thresholds are adjustable from the back-gates of some transistors in its comparators [76, 77]

The DC offsets of the comparators in the flash ADC whose design is reported in [75] are compensated by shifting the threshold reference levels of the comparators, as shown in Figure 3-4. However, the reference voltage multiplexers needed to implement the adjustments require a lot of silicon area to implement. Therefore, the ADC's DC offsets calibration range and resolution, which dictate the width of the multiplexers, must be determined prudently. This eventually limits the minimum size of the transistors in the comparators.

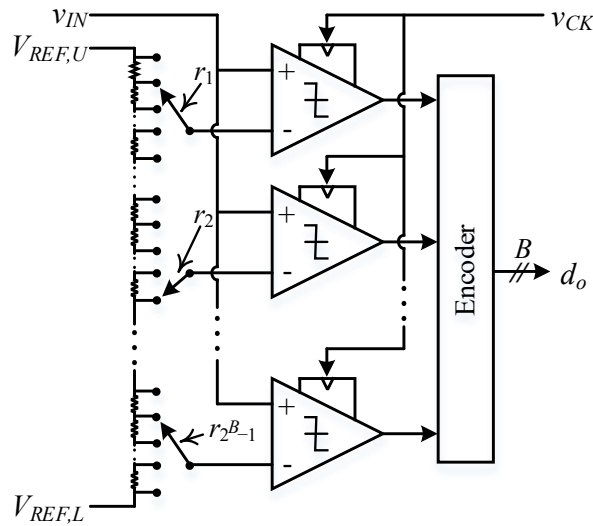


Figure 3-4 A flash ADC design with shift-able threshold reference levels [75]

Besides the trade-offs discussed earlier, a flash ADC's thresholds calibration implementation typically requires that a multiplexer is added at the input signal path of the ADC. The multiplexer is needed to provide a way to input a calibration stimulus signal into the ADC. This multiplexer is undesirable since it increases the ADC's input signal attenuation when the ADC's input signal frequency is very high.

Lastly, the time required by an ADC to complete its calibration routine may also be of concern. In the flash ADC design reported in [73], each of the comparators in the ADC is calibrated by performing a search for an input pair combination among around a thousand possible combinations that will result in the comparator having a sufficiently low DC offset. In [73], this search can only be done one comparator at a time due to the complexity of the circuitries required to execute the calibration. The ADC's long calibration time mandates that an extra copy of the ADC is incorporated in the design if the overall ADC circuitries must still be operable while a calibration is being executed in the background.

3.1.2 The Multi-Pass ADC

A multi-pass ADC [53] is a flash ADC that is implemented using only 1 comparator. The ADC works with either a DC or a periodic input signal. Figure 3-5 illustrates how a multi-pass ADC digitizes a periodic input signal, v_{IN} . As shown in Figure 3-5, the ADC digitizes the v_{IN} by comparing it to one threshold value, V_{TH} , at a time. The comparisons result in a stream of data, $d[l, b]$, in which:

$$d[l, b] = \begin{cases} 1 & \text{if } v_{IN}(t_l) > V_{FS} \cdot b/2^B \\ 0 & \text{if } v_{IN}(t_l) \leq V_{FS} \cdot b/2^B \end{cases} \quad (3-3)$$

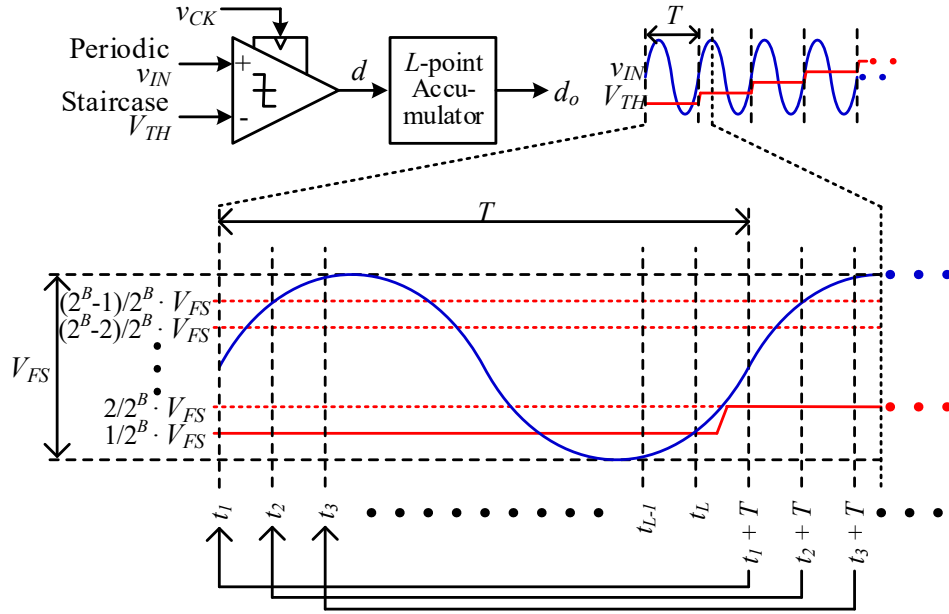


Figure 3-5 The operation of a multi-pass ADC with a periodic input signal; the ADC's input range is between 0 V and V_{FS} here

where $l = \{1, 2, \dots, L\}$, $b = \{1, 2, \dots, 2^B-1\}$, L is the number of points in a period of the periodic v_{IN} the ADC is digitizing, B is the ADC's resolution, and V_{FS} is the ADC's full-scale input range at a low input signal frequency. For simplicity, the ADC's V_{TH} value ranges between $1/2^B \cdot V_{FS}$ and $[2^B-1]/2^B \cdot V_{FS}$ here. In practice, these values will most likely be on top of a DC bias value.

Since the v_{IN} is periodic here, $v_{IN}(t_l)$ can equivalently be sampled at $t_l + k \cdot T$. That is, a multi-pass ADC is an equivalent-time sampling system. Therefore, the following equation is valid here:

$$v_{IN}(t_l) = v_{IN}(t_l + k \cdot T) \quad (3-4)$$

in which T is the v_{IN} 's period, and k is an integer. Here, $d[l, b]$ at a particular l value, but different b values come from comparisons that are carried out at different k values—this has to be since the ADC only has 1 comparator. In general, k is a function of both l and b :

$$k = f(l, b) \quad (3-5)$$

For example, if the comparator in the ADC can make L comparisons in one v_{IN} period and the ADC is made to update its V_{TH} value once every T seconds as shown in Figure 3-5, k will be equal to $b - 1$. On the other hand, if the comparator can only make one comparison in one v_{IN} period, k can be made to be equal to, e.g., $(b - 1) \cdot L + l - 1$ using equivalent-time sampling while the ADC is made to update its V_{TH} value once every $L \cdot T$ seconds in performing the multi-pass digitization.

The result of the digitization of the v_{IN} by the ADC is an L -point waveform representation of the v_{IN} , $d_o[l] = \{d_o[1], d_o[2], \dots, d_o[L]\}$, that is formed by adding together the $d[l, b]$ at the corresponding l value for all the possible b values:

$$d_o[l] = \sum_{b=1}^{2^B-1} d[l, b] \quad (3-6)$$

That is, the points in the ADC's output waveform are each formed by accumulating the results of 1-bit v_{IN} versus V_{TH} comparisons at $t_l + k \cdot T$ across multiple v_{IN} periods until the v_{IN} has been compared to 2^B-1 threshold values.

3.1.3 The Proposed Equivalent-Time Sampling ADC Architecture

In the proposed ADC architecture (see Figure 3-6), a number of multi-pass ADCs, i.e., $ADC_i = \{ADC_1, ADC_2, \dots, ADC_{2^B-1}\}$, are operated together in which the outputs of these sub-ADCs, i.e., $d_{o,i}[l] = \{d_{o,1}[l], d_{o,2}[l], \dots, d_{o,2^B-1}[l]\}$, are added together. Following the analysis presented in section 3.1.3.1, the signal-to-noise ratio (SNR) at the output of a digitizer that is implemented based on the proposed ADC architecture can be up to $(2^B-1) \times$ better in linear scale as compared to if it is implemented as a lone multi-pass ADC when the input-referred noise of the comparators in the digitizer dominates over the noise in the digitizer's input signal. The overall L -point output waveform of the digitizer, $d_o[l]$, can be described as follows:

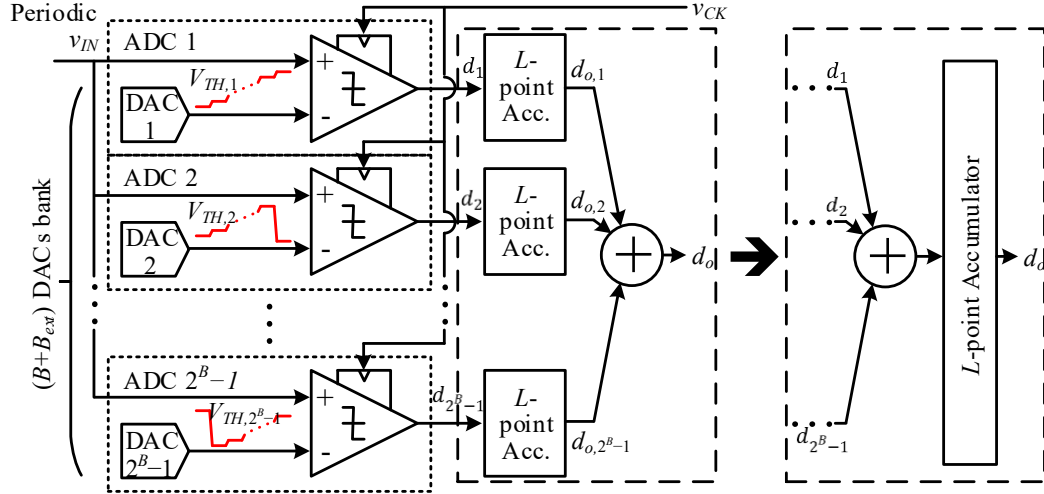


Figure 3-6 The block diagram of a digitizer that is implemented based on the proposed ADC architecture

$$d_o[l] = \sum_{i=1}^{2^B-1} d_{o,i}[l] = \sum_{i=1}^{2^B-1} \sum_{b_i=1}^{2^B-1} d_i[l, b_i] \quad (3-7)$$

In implementing the digitizer, the order of the summation in equation (3-7) can be swapped so that the required number of L -point accumulators in the digitizer's implementation can be reduced to 1, as shown in Figure 3-6: $d_i = \{d_1, d_2, \dots, d_{2^B-1}\}$ can first be added together before they are input into a shared L -point accumulator.

The advantages of the proposed ADC architecture are:

First, unlike in a flash-ADC, skews among the v_{IN} and clock signal (v_{CK}) paths to the comparators in a digitizer that is implemented based on the proposed architecture do not cause distortions (since the comparators belong to separate multi-pass sub-ADC units). The skews degrade only the overall digitizer's bandwidth by causing phase mismatches among the L -point output waveforms of the sub-ADCs in the digitizer.

Second, unlike in a flash-ADC, the offsets of the comparators in the digitizer, $V_{OFF,i} = \{V_{OFF,1}, V_{OFF,2}, \dots, V_{OFF,2^B-1}\}$, can be more than 1 LSB. If the offsets' values do not change with changing input common-mode level, the presence of the offsets will

only shift the DC levels of the respective $d_{o,i}[l]$ terms and, thus, the $d_o[l]$ term in equation (3-7). These shifts can be counteracted by shifting the sweep ranges of the respective $V_{TH,i}$ signals in the digitizer (see section 3.1.4). Note that $V_{OFF,i}$ may comprise some input-dependent components that are not insignificant [78]. The input dependence, however, is not expected to be a significant source of non-linearities for the digitizer: across 2^B-1 comparators, the average of the offsets at any given input common-mode level tends to be equal to 0 with a standard deviation (σ) that is equal to the σ of the offsets divided by $\sqrt{2^B-1}$ and, thus, is relatively small. This claim is supported by the digitizer's prototype's measurement results, whose INL is <0.5 LSB across most of its input range despite the large offsets of some of the comparators in the digitizer (see section 3.3).

The proposed ADC architecture has a loose skew and comparator offset design requirement, which helps lower the power consumption and the input capacitance of a digitizer that is implemented based on the architecture.

3.1.3.1 Analysis of the sub-ADCs' outputs correlation

The multi-pass sub-ADCs in the proposed ADC architecture, each, is assigned with its own V_{TH} signal: $V_{TH,i} = \{V_{TH,1}, V_{TH,2}, \dots, V_{TH,2^B-1}\}$, as illustrated in Figure 3-6, since the sub-ADCs must always have different threshold values from each other at any time. This arrangement minimizes the correlations among the B -bit outputs of the sub-ADCs, that is, among the $d_{o,i}[l]$ terms in equation (3-7). The correlations happen since the sub-ADCs digitize a common noisy v_{IN} . The correlations are unwanted since we want to average down v_{IN} 's noise component in $d_o[l]$ as much as possible as the v_{IN} is digitized. For the $V_{TH,i}$ to always have different values from each other, the b_i terms in equation (3-7) can be arranged according to the following equation:

$$b_i = g(b, i) = ((b - 1 + i - 1) \% (2^B - 1)) + 1 \quad (3-8)$$

in which $b = \{1, 2, \dots, 2^B - 1\}$ and $\%$ is the modulo operator. How $V_{TH,i}$ update over time under this arrangement is also illustrated in Figure 3-6.

In the following analysis, the term i that indicates the relative position in time within v_{IN}' 's period at which the v_{IN} is sampled is dropped for readability purposes.

Basically, the comparisons that are performed by each sub-ADC in the proposed ADC architecture are each a Bernoulli trial in which:

$$d_i[b_i] = \begin{cases} 1 & \text{if } v_{IN} + n_{in} + n_{adc,i} > V_{FS} \cdot b_i / 2^B \\ 0 & \text{if } v_{IN} + n_{in} + n_{adc,i} \leq V_{FS} \cdot b_i / 2^B \end{cases} \quad (3-9)$$

Here, $n_{adc,i}$ is the input-referred noise of the respective sub-ADC, and n_{in} is the v_{IN}' 's noise (that is, the v_{IN} term itself is noiseless here). The probability that $d_i[b_i]$ is equal to 1, $p[i, b_i]$, can be described by the following equation:

$$p[i, b_i] = \frac{1}{\sigma_{n,tot}} \cdot \int_{-\Delta v_{IN}[b_i]}^{\infty} \varphi\left(\frac{n_{tot}[i]}{\sigma_{n,tot}}\right) dn_{tot}[i] \quad (3-10)$$

in which $\Delta v_{IN}[b_i] = v_{IN} - V_{FS} \cdot b_i / 2^B$, $n_{tot}[i] = n_{in} + n_{adc,i}$, and $\varphi(x)$ is the probability density function of a standard normal random variable:

$$\varphi(x) = \frac{1}{\sqrt{2\pi}} \cdot e^{-x^2/2} \quad (3-11)$$

$n_{tot}[i]$ here is a normal random variable with 0 mean and a standard deviation $\sigma_{n,tot}$ that is equal to $\sqrt{\sigma_{n,in}^2 + \sigma_{n,adc}^2}$ if both the n_{in} and $n_{adc,i}$ are white gaussian noise with 0 mean and standard deviations of $\sigma_{n,in}$ and $\sigma_{n,adc} = \sigma_{n,adc}[i]$ for all i , respectively. $p[i, b_i]$ quickly tends to 1 or 0 as the ratio $\Delta v_{IN}[b_i] / \sigma_{n,tot}$ grows to a few times in value. The variance of $d_i[b_i]$, $\text{Var}(d_i[b_i])$, tends to 0 as $p[i, b_i]$ tends to 0 or 1 according to the following equation:

$$\text{Var}(d_i[b_i]) = p[i, b_i] \cdot (1 - p[i, b_i]) \quad (3-12)$$

As discussed in section 3.1.2, for a given i (that is, for each multi-pass sub-ADC), $d_i[b_i] = \{d_i[1], d_i[2], \dots, d_i[2^B-1]\}$ are comparison results that are obtained from different points in time. Henceforth, for a given i , $d_i[b_i]$ can be assumed to be independent of each other (that is, any noise that affects the comparisons are assumed to be sufficiently “white” here) and the $d_{o,i} = \{d_{o,1}, d_{o,2}, \dots, d_{o,2^B-1}\}$ terms in equation (3-7) are each a Poisson Binomial random variable with a variance of $\text{Var}(d_{o,i}) = \sum_{b_i=1}^{2^B-1} \text{Var}(d_i[b_i]) = \sum_{b_i=1}^{2^B-1} \text{Var}(d_i[g(b,i)])$ in which $g(b,i)$ may be set to follow equation (3-8). Now, the variance of the d_o in equation (3-7) can be described by the following equation:

$$\text{Var}(d_o) = \sum_{i=1}^{2^B-1} \text{Var}(d_{o,i}) + \sum_{b=1}^{2^B-1} \sum_{i=1}^{2^B-1} \sum_{j \neq i} \text{cov}(d_i[g(b,i)], d_j[g(b,j)]) \quad (3-13)$$

The 2nd summation term at the right-hand side of equation (3-13) is due to the correlations among the comparisons that are performed simultaneously (implied by them having the same b value). Each of the covariance terms in equation (3-13) can be elaborated as follows:

$$\begin{aligned} \text{cov}(d_i[b_i], d_j[b_j]) = & \int_{-\infty}^{\infty} \varphi\left(\frac{n_{in}}{\sigma_{n,in}}\right) \int_{\Delta v_{IN}[b_i] - n_{in}}^{\infty} \varphi\left(\frac{n_{adc,i}}{\sigma_{n,adc}}\right) dn_{adc,i} \int_{\Delta v_{IN}[b_j] - n_{in}}^{\infty} \varphi\left(\frac{n_{adc,j}}{\sigma_{n,adc}}\right) dn_{adc,j} dn_{in} \\ & \cdot \frac{1}{\sigma_{n,in} \cdot \sigma_{n,adc}^2} - p[i, b_i] \cdot p[j, b_j] \end{aligned} \quad (3-14)$$

The integration term at the right-hand side of equation (3-14) calculates for $\text{Pr}(p[i, b_i]=1, p[j, b_j]=1)$ which basically is the expected value of $(d_i[b_i] \cdot d_j[b_j])$. Meanwhile, $p[i, b_i]$ and $p[j, b_j]$, each, follows equation (3-10). As a note, n_{in} , $n_{adc,i}$, and $n_{adc,j}$ are all independent of each other. Equation (3-14) does not have a closed-form solution and must be computed using numerical means, but it can be shown that:

$$\lim_{\sigma_{n,in} \rightarrow 0} \text{cov}(d_i[b_i], d_j[b_j]) = 0 \quad (3-15)$$

$$\lim_{\sigma_{n,adc} \rightarrow 0} \text{cov}(d_i[b_i], d_j[b_j]) = \min(p[i, b_i], p[j, b_j]) - p[i, b_i] \cdot p[j, b_j] \quad (3-16)$$

For the in-between cases, $n_{adc,i}$ and $n_{adc,j}$ tend to reduce the sum of the covariance terms in equation (3-13) when $n_{adc,i}$ and $n_{adc,j}$ are strong enough.

Given $\sigma_{n,in}$ and $\sigma_{n,adc}$, equation (3-13) and (3-14) can be used to compute whether the *SNR* of a digitizer that is implemented based on the proposed ADC architecture reduces significantly when the digitizer is realized with a reduced number of sub-ADCs (for a reduced area usage and system power consumption). This optimization step is not performed here since the pulse radar receiver that the digitizer circuit is meant to be used in will only be implemented in one of our future works. Henceforth, we do not have a specific $\sigma_{n,in}$ value to use, which is a prerequisite for performing the optimization step.

3.1.3.2 Example Digitization Process

Table 3-1 illustrates, by example, how a digitizer that is implemented based on the proposed ADC architecture digitizes a periodic signal. The waveforms of the signals relevant to the example digitization are given in Figure 3-7.

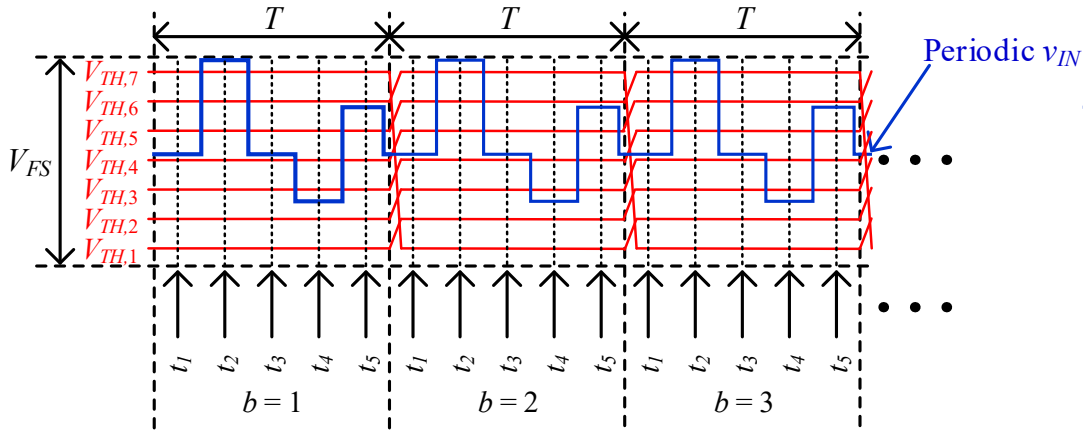


Figure 3-7 Waveforms illustrating the digitization process in a digitizer implemented based on the proposed ADC architecture (here, $B = 3$, $L = 5$, and 5 samples are taken in each v_{IN} 's period)

Table 3-1 An example digitization by a digitizer that is implemented based on the proposed ADC architecture for the v_{IN} waveform shown in Figure 3-7 (here, $B = 3$, $V_{FS} = 1$ V, $L = 5$, and 5 samples are taken in each v_{IN} 's period)

t_i	b	$i = 1$			$i = 2$			$i = 3$			$i = 4$			$i = 5$			$i = 6$			$i = 7$			
		b_1	$V_{TH,1}$	d_1	b_2	$V_{TH,2}$	d_2	b_3	$V_{TH,3}$	d_3	b_4	$V_{TH,4}$	d_4	b_5	$V_{TH,5}$	d_5	b_6	$V_{TH,6}$	d_6	b_7	$V_{TH,7}$	d_7	
t_1	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	d_o [1] = 7 × 4 = 28
	2	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	
	3	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	
	4	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	
	5	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	
	6	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	
	7	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	
		$d_{o,1}[1] = 4$			$d_{o,2}[1] = 4$			$d_{o,3}[1] = 4$			$d_{o,4}[1] = 4$			$d_{o,5}[1] = 4$			$d_{o,6}[1] = 4$			$d_{o,7}[1] = 4$			
t_2	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	1	7	7/8	1	d_o [2] = 7 × 7 = 49
	2	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	1	7	7/8	1	1	1/8	1	
	3	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	1	7	7/8	1	1	1/8	1	2	2/8	1	
	4	4	4/8	1	5	5/8	1	6	6/8	1	7	7/8	1	1	1/8	1	2	2/8	1	3	3/8	1	
	5	5	5/8	1	6	6/8	1	7	7/8	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	
	6	6	6/8	1	7	7/8	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	
	7	7	7/8	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	1	
		$d_{o,1}[2] = 7$			$d_{o,2}[2] = 7$			$d_{o,3}[2] = 7$			$d_{o,4}[2] = 7$			$d_{o,5}[2] = 7$			$d_{o,6}[2] = 7$			$d_{o,7}[2] = 7$			
t_3	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	d_o [3] = 7 × 4 = 28
	2	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	
	3	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	
	4	4	4/8	1	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	
	5	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	
	6	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	
	7	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	0	6	6/8	0	
		$d_{o,1}[3] = 4$			$d_{o,2}[3] = 4$			$d_{o,3}[3] = 4$			$d_{o,4}[3] = 4$			$d_{o,5}[3] = 4$			$d_{o,6}[3] = 4$			$d_{o,7}[3] = 4$			
t_4	1	1	1/8	1	2	2/8	1	3	3/8	0	4	4/8	0	5	5/8	0	6	6/8	0	7	7/8	0	d_o [4] = 7 × 2 = 14
	2	2	2/8	1	3	3/8	0	4	4/8	0	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	
	3	3	3/8	0	4	4/8	0	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	
	4	4	4/8	0	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	0	
	5	5	5/8	0	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	0	4	4/8	0	
	6	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	0	4	4/8	0	5	5/8	0	
	7	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	0	4	4/8	0	5	5/8	0	6	6/8	0	
		$d_{o,1}[4] = 2$			$d_{o,2}[4] = 2$			$d_{o,3}[4] = 2$			$d_{o,4}[4] = 2$			$d_{o,5}[4] = 2$			$d_{o,6}[4] = 2$			$d_{o,7}[4] = 2$			
t_5	1	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	0	7	7/8	0	d_o [5] = 7 × 5 = 35
	2	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	0	7	7/8	0	1	1/8	1	
	3	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	
	4	4	4/8	1	5	5/8	1	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	
	5	5	5/8	1	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	
	6	6	6/8	0	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	
	7	7	7/8	0	1	1/8	1	2	2/8	1	3	3/8	1	4	4/8	1	5	5/8	1	6	6/8	0	
		$d_{o,1}[5] = 5$			$d_{o,2}[5] = 5$			$d_{o,3}[5] = 5$			$d_{o,4}[5] = 5$			$d_{o,5}[5] = 5$			$d_{o,6}[5] = 5$			$d_{o,7}[5] = 5$			

In Figure 3-7, an arbitrary periodic signal, v_{IN} , is being digitized at 5 equivalent-time points, $t_i = \{t_1, t_2, \dots, t_5\}$, by a 3-bit digitizer that is implemented based on the proposed ADC architecture. The l , b , and i value of equation (3-7) thus range between 1 and 5, 1 and 7, and 1 and 7, respectively, here, as given in Table 3-1's first column, second column, and first row. Table 3-1 also lists the corresponding comparison thresholds, $V_{TH,i} = \{V_{TH,1}, V_{TH,2}, \dots, V_{TH,7}\}$, in the multi-pass A/D conversion of v_{IN} for each $b_i = \{b_1, b_2, \dots, b_7\}$ value in which $V_{TH,i} = V_{FS} \cdot b_i / 2^3$ and V_{FS} is 1. The b_i values are, in turn, computed from the corresponding b and i value combinations according to equation (3-8). The table then lists the comparison results between the v_{IN} and $V_{TH,i}$, d_i , at each t_i across the b_i values for all the sub-ADCs in the digitizer. The $d_{o,i}$ and d_o values at each t_i are finally computed from the corresponding d_i values according to equation (3-7), and the 5-point waveform representation of the v_{IN} is produced as given in Table 3-1's last column.

3.1.4 Calibration in the Proposed ADC Architecture

The offsets of the comparators in a digitizer that is implemented based on the proposed ADC architecture, $V_{OFF,i} = \{V_{OFF,1}, V_{OFF,2}, \dots, V_{OFF,2^b-1}\}$, degrade the digitizer's linearity performance, primarily, by reducing the digitizer's effective input range, thus constricting its usable dynamic range. $V_{OFF,i}$ reduce the range by introducing mismatched 1) offset errors and 2) gain errors to the sub-ADCs in the digitizer (i.e., to $ADC_i = \{ADC_1, ADC_2, \dots, ADC_{2^b-1}\}$ in Figure 3-6):

- 1) $V_{OFF,i}$ shift the input ranges of the sub-ADCs in the digitizer and cause them to mismatch, as illustrated in Figure 3-8a. Suppose the digitizer's input range is between 0 V and V_{FS} . In that case, $V_{OFF,i}$ will shift the corresponding sub-ADCs' input ranges to between $-V_{OFF,i}$ and $(V_{FS} - V_{OFF,i})$. With the digitizer's input signal biased at the midpoint of the digitizer's input range, the shifts will cause the sub-ADCs to saturate early as the signal's amplitude increases.

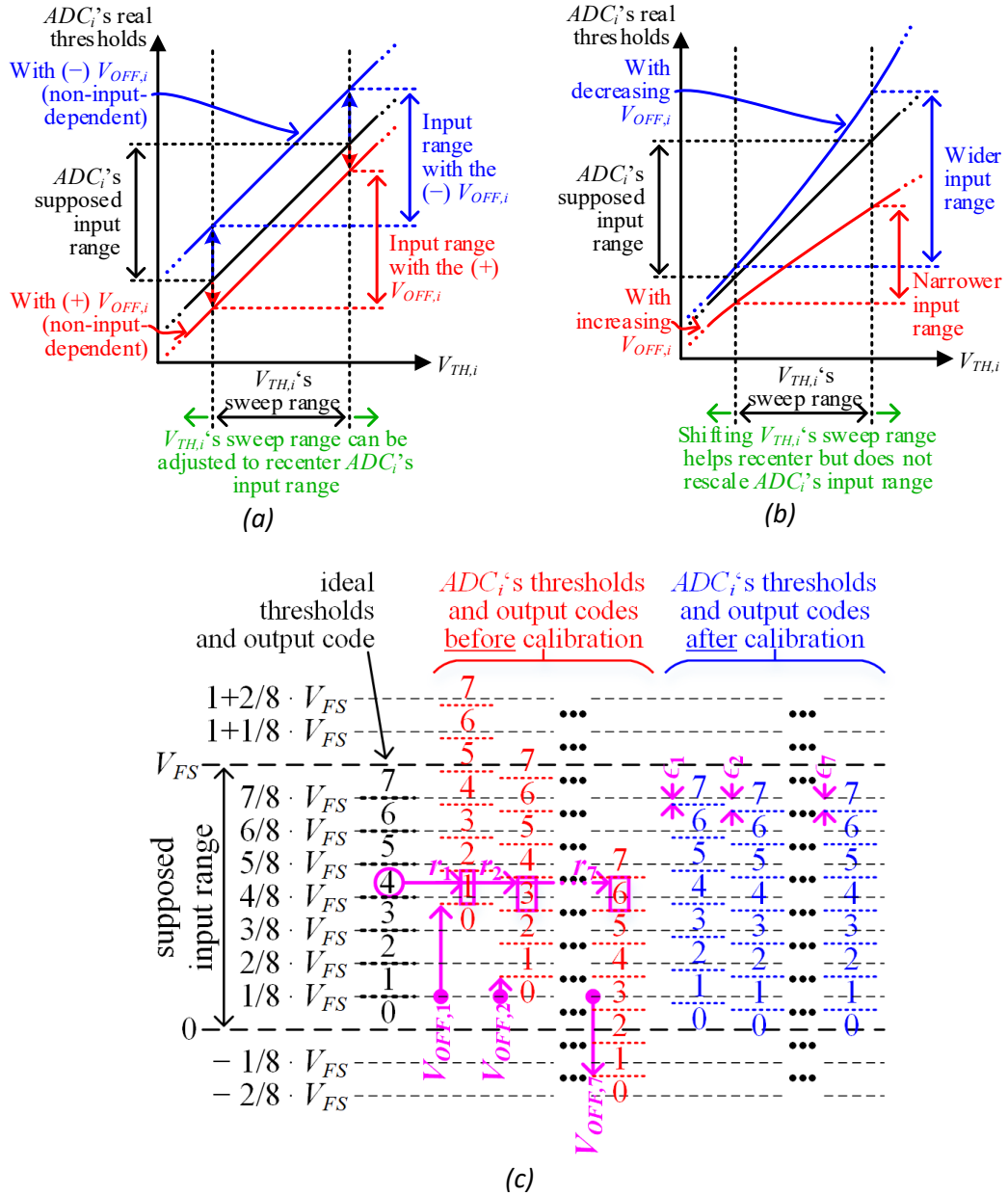


Figure 3-8 The thresholds and input ranges of the multi-pass sub-ADCs (ADC_i) of a digitizer that is implemented based on the proposed ADC architecture under the effect of comparator offsets ($V_{OFF,i}$) that are (a) non-input-dependent (b) input-dependent, and (c) an example illustrating the offset-errors-removing calibration proposed for the digitizer (here, $B = 3$ and the digitizer's input range is between 0 and V_{FS})

2) $V_{OFF,i}$'s input-dependent components scale the input ranges of the sub-ADCs in the digitizer, as illustrated in Figure 3-8b. If $V_{OFF,i}$ increase with increasing input common-mode level, the corresponding sub-ADCs' input ranges will decrease accordingly and vice versa. The presence of sub-ADCs with degraded input ranges degrades the digitizer's effective input range.

Note that $V_{OFF,i}$'s input dependence may follow a non-linear trend. However—as also noted in section 3.1.3— $V_{OFF,i}$'s average at any given input common-mode level tends to be equal to 0 across the many comparators in the digitizer (barring systematic mismatches). Therefore, the digitizer's overall DC transfer function will considerably be more linear (except near its endpoints) than the individual DC transfer functions of some of its sub-ADCs. Thus, $V_{OFF,i}$'s non-linear input dependence is not a significant source for non-linearities in the digitizer.

3.1.4.1 *The proposed calibration procedure*

In this work, we propose that the calibration employed by a digitizer implemented based on the proposed ADC architecture does not rescale but only recenters the input ranges of its sub-ADCs. The calibration does not need to correct the gain errors of the sub-ADCs since correcting their offset errors can already sufficiently mitigate the input range degradation suffered by the digitizer. Furthermore, correcting only the offset errors is beneficial for design simplicity (to save area and power usage).

To remove the offset errors, the sweep ranges of the $V_{TH,i}$ signals of the sub-ADCs in the digitizer can be adjusted according to the results of the A/D conversions of a reference DC voltage by the sub-ADCs. The calibration thus ends after every sub-ADCs in the digitizer each produces the correct output code given the reference DC input level, as illustrated in Figure 3-8c. Suppose the digitizer's input range is between 0 V and V_{FS} . In that case, with equation (3-7) as reference :

$$V_{TH,i} = V_{FS} \cdot b_i / 2^B \quad (3-17)$$

before the calibration and after the calibration:

$$V_{TH,i} = V_{FS} \cdot (b_i + r_i) / 2^B \quad (3-18)$$

in which $r_i = \{r_1, r_2, \dots, r_{2^B-1}\}$ are the differences between the respective sub-ADCs' actual $d_{o,i}$ values and the ideal $d_{o,i}$ value (that is, the $d_{o,i}$ value when $V_{OFF,i} = 0$) given the reference DC input voltage value. As a note, the reference DC voltage can be the digitizer's input signal bias voltage, whose value should normally lie at the center of the ideal input range of the digitizer. As a result, the calibration can be implemented without additional circuitries at the digitizer's input signal path.

For each sub-ADC (i.e., for each i), the calibration adjusts the sub-ADC's input range to between ϵ_i and $V_{FS} + \epsilon_i$ in which ϵ_i is an error due to the finite resolution of the sub-ADC. These residual errors affect only the digitizer's lowest and highest output codes since they cause the input ranges of the sub-ADCs in the digitizer to be slightly out of the intended input range, as illustrated in Figure 3-8c. If the overall noise level encountered during the calibration is very low:

$$|\epsilon_i| < V_{FS} \cdot 1/2^B \quad (3-19)$$

If the noise level is higher, $|\epsilon_i|$ can vary substantially from calibration to calibration and possibly get much larger than $V_{FS} \cdot 1/2^B$. Averaging can be employed if, due to noise, these residual errors can get too large. Lastly, if the DC offsets of the comparators in the sub-ADCs can change substantially with temperature, $|\epsilon_i|$ can be expected to grow over time if there is a gradual temperature change. The digitizer can be periodically recalibrated to cater to temperature change depending on the expected rate of temperature change.

3.1.4.2 Calibration-related design considerations

The comparator offsets calibration needed by a digitizer that employs the proposed ADC architecture described here has a loose accuracy requirement compared to the accuracy required by the comparator offsets calibration of a typical flash-ADC:

In a digitizer that is implemented based on the proposed ADC architecture, the offsets of the comparators in the digitizer do not need to be reduced to less than the digitizer's LSB size since they do not affect the digitizer's *DNL* except at the digitizer's lowest and highest output codes only. A slight input range degradation is less disruptive to a digitizer's operation than a degradation to its overall *DNL* performance. With its loose accuracy requirement, the digitizer's offsets calibration can cover a wider spread of comparator offsets without too huge an area cost, and the comparators in the digitizer can be designed with less concern for their random offsets. Therefore, the comparators in the digitizer can be designed using smaller transistors (for a lower power consumption figure and lower input capacitance).

Furthermore, since 1) the execution time of the comparator offsets calibration needed by the digitizer is relatively short since it requires only a few samples from each of the digitizer's sub-ADCs, and 2) the calibration's stimulus can be the input signal bias voltage, the calibration can be implemented to be executed in the background without much overhead. Figure 3-9 shows how this can be done in a UWB pulse radar receiver implementation. The extra *L*-point accumulator shown in Figure 3-9 (i.e., the "calibration" *L*-point accumulator) can be connected to any of the sub-ADCs in the digitizer, one at a time. When the digitizer's d_o value according to the digitizer's main *L*-point accumulator is equal to the d_o value when there is only the digitizer's input bias voltage at the digitizer's input, no radar pulse echoes are detected at the digitizer's input. The readouts from the calibration accumulator when no radar pulse echoes are detected at the digitizer's input can be used to compute the adjustments required to correct the offset errors of the sub-ADCs in the digitizer.

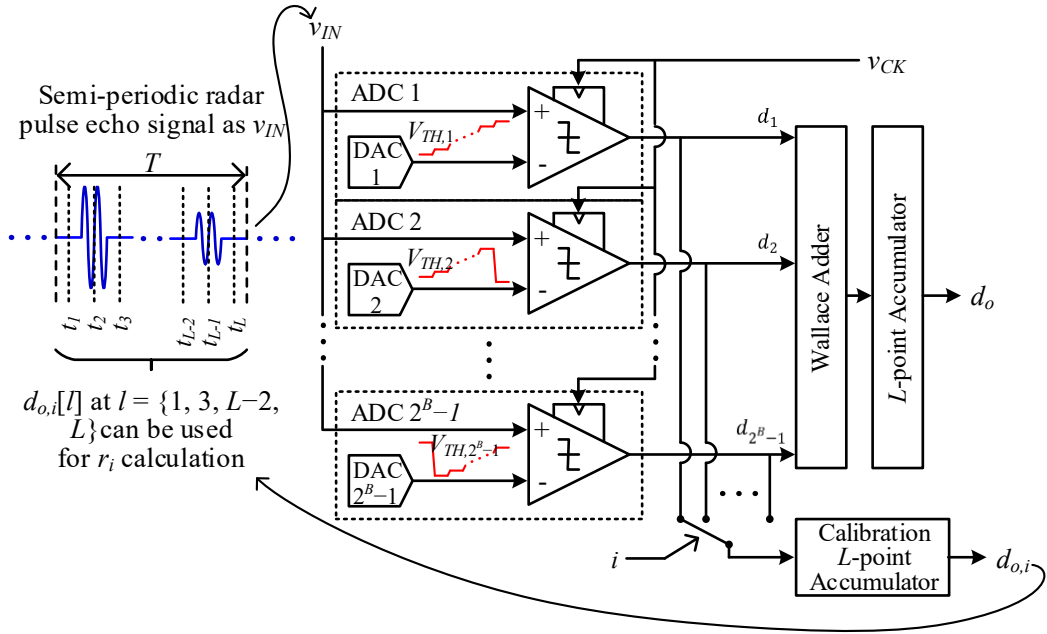


Figure 3-9 An example showing how a UWB radar pulse digitizer that is implemented based on the proposed ADC architecture can be calibrated in the background

Lastly, the offsets of the comparators in the digitizer may change the comparators' electrical performances critical to the digitizer's operation (e.g., sampling bandwidth) even after they are compensated. The changes can be minimized, but the ways to minimize them are specific to how the comparators are designed. Thus, these will only be discussed in section 3.2.1. Alternatively, following the analysis presented in section 3.1.3.1, the digitizer can also be operated with some of its sub-ADCs disabled without significantly degrading its noise performance, especially when its input signal is noisy. Therefore, the few comparators in the digitizer whose DC offsets are very large can be disabled. The SNR degradation due to the reduced number of active sub-ADCs can be deduced from equation (3-13) to be $< 10 \cdot \log(\frac{2^B-1}{l_{active}})$ in dB term (l_{active} here is the number of sub-ADCs still in operation). The "<" sign here is because the second term in equation (3-13) originating from the correlations among the sub-ADCs' outputs reduces faster than the reduction in the number of active sub-ADCs. Hence, if, for example, 3 sub-ADCs are deactivated, the SNR degradation will be $< \sim 0.22$ dB only in a 6-bit implementation of the digitizer.

3.1.4.3 Comparisons with prior-art flash ADC designs

Table 3-2 compares the overhead of the comparator offsets calibration required by a digitizer that is implemented based on the proposed ADC architecture and the overhead of the comparator offsets calibration required by some prior-art flash ADC designs. The table summarizes why a digitizer based on the proposed ADC architecture can be designed with lower input capacitance compared to if it is designed based on a traditional flash ADC architecture. However, it must be noted that the use of the proposed ADC architecture means that the digitizer's input signal must be periodic (or approximately so). Since the digitizer is meant to be used in a UWB pulse radar implementation, the digitizer's update rate must be very high compared to the rate of change in the time-of-flight and strength of the radar pulse echo signal received.

Table 3-2 Qualitative comparisons between the overhead of the comparator offsets calibration required in the proposed ADC architecture and that in some prior-art flash ADC designs

Calibration approach	Sizing for Low-Offset	Comparator Redundancy [70], [72]	Combinative Redundancy [71], [73]	Comparator's Load Tuning [74]	Reference Ladder Tuning [75]	Back-gate Bias Tuning [76], [77]	Proposed ADC Architecture
Calibration accuracy	N.A.	< 0.5 LSB					1 LSB or more (trades with input range)
Calibration execution time	N.A.	Short	Very long	Short			
Calibration stimulus	N.A.	Appropriate calibration stimulus required					Can be the ADC's input bias
Expected ADC's input capacitance	Very High	Medium	Low	Low to Medium			Low
Input signal	No requirement						Semi-periodic

3.2 Circuit Design

3.2.1 Comparator Design and Implementation

This work presents the design and implementation of a mm-wave UWB radar pulse digitizer based on the novel ADC architecture proposed in section 3.1. Figure 3-10 shows how the comparators of the sub-ADCs in the digitizer are implemented. The figure shows that the comparators are implemented using a bank of ‘bare’ StrongARM latches: the latches are implemented without the shared track-and-hold (T/H) circuit and the pre-drivers that usually precede them in a flash ADC. The T/H circuit is not necessary for the digitizer’s proper operation since the comparators in the digitizer belong to separate multi-pass sub-ADC units (see section 3.1). The comparators are implemented without pre-drivers since, without a T/H circuit, the pre-drivers will significantly limit the comparators’ sampling bandwidths, causing a significant amount of loss since the frequency of the signal of interest, i.e., the f_{in} in Figure 3-10, is in the mm-wave frequency range here.

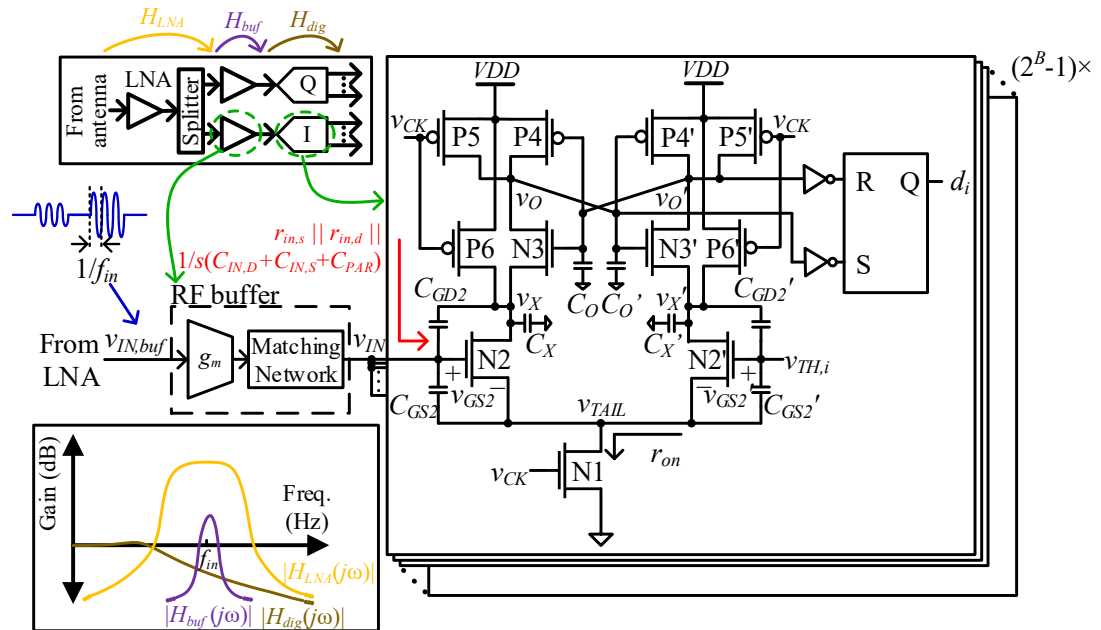


Figure 3-10 The comparator circuit of each sub-ADC in the mm-wave UWB radar pulse digitizer that is presented in this work; the diagram also shows how the digitizer is to be driven at the radar receiver system level

Figure 3-10 also illustrates how the digitizer is to be driven when it is used as part of a direct-RF mm-wave UWB pulse radar receiver implementation. In the receiver, the digitizer is to be driven by a mm-wave RF buffer with the buffer's output matching network tuned to resonate with the total parallel-equivalent capacitance at the input of the digitizer, $(2^B-1) \times (C_{IN,D}+C_{IN,S}+C_{PAR})$, at around the carrier frequency of the radar pulse echo signal the digitizer is digitizing.

In this section, the operation of the StrongARM latch circuit given in Figure 3-10 in its sampling phase is first reviewed. Afterward, the latch's design parameters that strongly influence its electrical performances that are important in the design of the digitizer are determined. The discussions adopt the standard signal naming convention: signal names written in all uppercase and lowercase letters denote the corresponding signals' biases and small-signal components, respectively. Note that, in the discussions, a signal's bias is almost always a time-varying quantity that gives rise to time-varying small-signal parameters. However, for the purpose of determining the trade-offs that are important in the latch's design for use in the digitizer, they may be represented by some non-time-varying quantities.

3.2.1.1 *The sampling phase of a StrongARM latch*

As the StrongARM latch circuit given in Figure 3-10 is triggered to perform a comparison (that is, as the signal v_{CK} in Figure 3-10 asserts), a process that works to determine which of the latch's two input signals (i.e., the v_{IN} and v_{TH} in Figure 3-10) has the higher average value within a certain aperture time starts in the latch. In each of these comparisons, the latch will go through several operation phases that start and end approximately when the respective conditions pointed out in Figure 3-11 are met [58, 79]. In each operation phase, a different set of transistors will have the central role in the ongoing operation. Note that the V_{TN} and V_{TP} in Figure 3-11 are the threshold voltages of the NMOSes and PMOSes in the latch, respectively.

Among the operation phases, the operation phase that is most important to the StrongARM latch circuit analysis presented here is the sampling phase. This phase is the only phase among the latch's operation phases in which the latch's input signals are capable of considerably influencing the latch's comparison results.

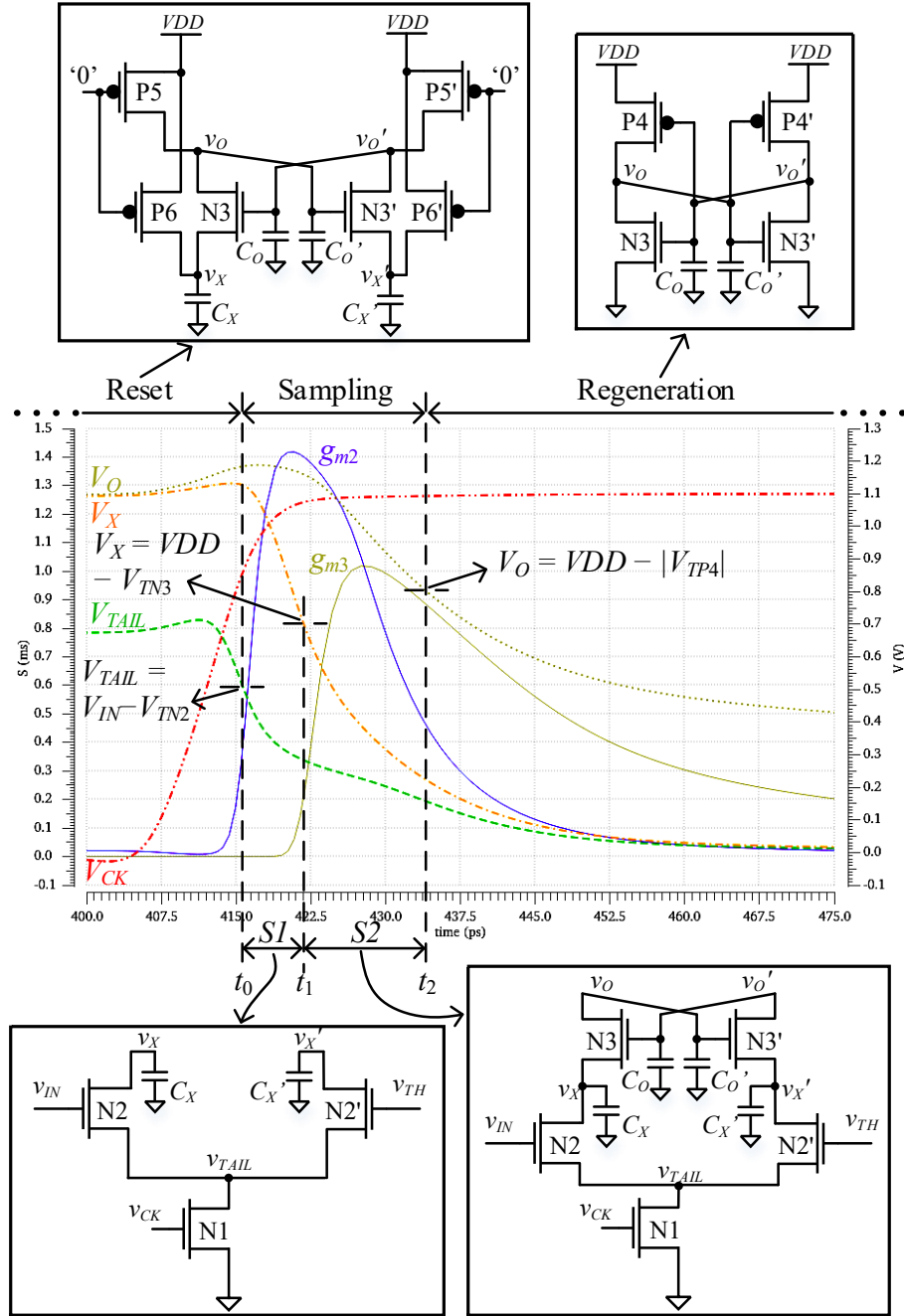


Figure 3-11 The phases of operation of the StrongARM latch circuit given in Figure 3-10

As shown in Figure 3-11, the transistors that have the central role in the sampling phase are N1, N2-N2', and N3-N3'. If the following condition is met, N1 will always operate in the linear region in the sampling phase:

$$V_{IN} < VDD + V_{TN2} - V_{TN1} \quad (3-20)$$

Whereas N2 and N2' will turn on to operate in the saturation region at the start of the sampling phase. Their transconductances (g_{m2} and g_{m2}') will initially grow as their gate to source voltages ($V_{IN}-V_{TAIL}$ and $V_{TH}-V_{TAIL}$) increase in the sampling phase. However, their drain to source voltages (V_X-V_{TAIL} and $V_{X'}-V_{TAIL}$) will decrease as time goes in the sampling phase since V_X and $V_{X'}$ decrease as time goes in the sampling phase. Therefore, N2 and N2' will transition to operate in the linear region after some time, causing g_{m2} and g_{m2}' to decay. As for N3 and N3', the transistors will always operate in the saturation region in the sampling phase after turning on at t_1 .

The sampling phase can be sub-divided into two distinct sub-phases, denoted as the S1 (t_0-t_1) and the S2 sampling phase (t_1-t_2) in Figure 3-11. The S1 sampling phase starts when the capacitors C_X and $C_{X'}$ in the latch are starting to discharge and ends when the voltages across the capacitors (V_X and $V_{X'}$ in Figure 3-11) have discharged to $VDD - V_{TN3}$ (the initial value of the voltages is equal to the latch's supply voltage value, VDD). When V_X and $V_{X'}$ have already been discharged to $VDD - V_{TN3}$, the transistors N3 and N3' in the latch will start to conduct, which marks the start of the latch's S2 sampling phase. The S2 sampling phase ends presumably when the transistors P4 and P4' in the latch are starting to conduct. When P4 and P4' are conducting, the back-to-back inverter pair formed by P4, P4', N3, and N3' are fully operational. With its output voltage difference being strongly regenerated, the latch's input signals can no longer contribute substantially to the latch's comparison results.

Note that Figure 3-11 only shows the transconductance and voltage waveforms from the left half of the StrongARM latch circuit being analyzed because the voltages at the circuit's right half nodes are assumed to be the same as those at their left half counterparts: V_{IN} is assumed to be equal to V_{TH} here. This treatment mimics the usual way the DC bias analysis of a non-time-varying circuit is done before it is analyzed for its AC behavior.

It must also be noted that the boundaries between the operation phases and sub-phases defined here are not 'hard' boundaries. A StrongARM latch circuit does not transition between its operation phases abruptly. Instead, the circuit's characteristics will gradually change as it transitions between the phases, as noted in [58]. Nevertheless, the approximation in which the transitions are abrupt helps in the circuit's analysis, making it easier to identify the circuit's key design trade-offs.

3.2.1.2 *Input path gain/loss*

This work presents the design of a digitizer that will be used in a direct-RF mm-wave UWB pulse-Doppler radar receiver implementation (see Figure 3-10). This section analyzes the gains/losses in the digitizer's input path when a mm-wave RF buffer is used to drive the digitizer. With Figure 3-10 as a reference, the path's transfer function can be decomposed as follows:

$$H(s) = H_{buf}(s) \cdot H_s(s) \quad (3-21)$$

in which $H_{buf}(s)$ is the transfer function of the mm-wave RF buffer that drives the digitizer and $H_s(s)$ is the component in the transfer function that comes from the finite sampling aperture of the StrongARM latches [58, 79] in the digitizer.

In designing the digitizer and its mm-wave RF buffer-driver, $|H_{buf}(j\omega_{in})|$'s value and $|H_s(j\omega_{in})|$'s value must be balanced, in which $\omega_{in} = 2\pi \cdot f_{in}$ where f_{in} is the digitizer's input signal frequency. Here, $|H_s(j\omega_{in})|$'s value is expected to be lower than one and $H_{buf}(s)$ must compensate for this loss. Hence, if $|H_s(j\omega_{in})|$'s value is very low, the digitizer's mm-wave RF buffer-driver must be designed with a very large gain, and the amplitude of the signal at the digitizer's input must be very large for it to span the digitizer's full-scale input range at f_{in} . This situation must be avoided since it is detrimental to the linearity of the digitizer and the mm-wave RF buffer.

3.2.1.2.1 StrongARM latch's sampling bandwidth and input attenuation

As with any other sampling circuit, a StrongARM latch does not sample its input signals instantaneously, i.e., a StrongARM latch circuit has a finite sampling aperture. In comparing its input signals (i.e., the v_{IN} and v_{TH} in Figure 3-11), the latch is sensitive to the signals' values during the whole of its sampling phase, and the result of the comparison will be based on the signals' averages across time after they are weighted accordingly by the latch's impulse sensitivity function (ISF), $\Gamma(t)$ [58].

With Figure 3-11 as a reference, the sampling phase's duration, also $\Gamma(t)$'s duration, of the StrongARM latch circuit whose schematic is given in Figure 3-10 lasts roughly between t_0 and t_2 . As discussed in section 3.2.1.1, the sampling phase can be divided into 2 sub-phases, denoted as the S1 sampling phase (t_0 to t_1) and the S2 sampling phase (t_1 to t_2) in Figure 3-11 whose durations can be approximated as:

$$S1: t_1 - t_0 = \frac{C_X \cdot V_{TN3}}{\overline{I_{D2}}} \quad (3-22)$$

$$S2: t_2 - t_1 = \frac{(C_X + C_O) \cdot |V_{TP4}|}{\overline{I_{D2}}} \quad (3-23)$$

in which I_{D2} is the drain current of the transistor N2/N2' in the latch.

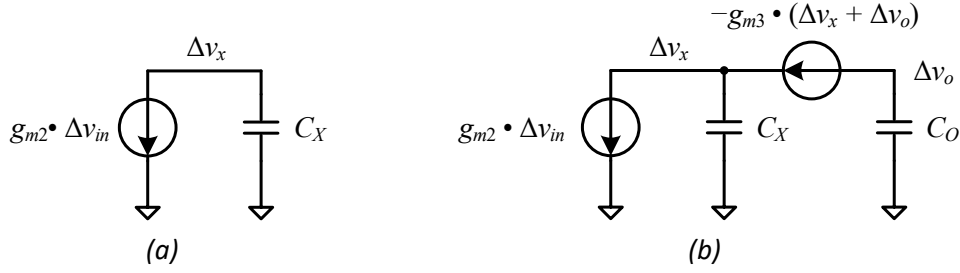


Figure 3-12 The small-signal model of the StrongARM latch circuit given in Figure 3-10 while it is operating in its (a) S1 sampling phase and (b) S2 sampling phase

Following the analysis presented in [58] and with the discussions presented in section 3.2.1.1 as a reference, the $\Delta v_x = v_x - v_x'$ in the S1 sampling phase and the $\Delta v_o = v_o - v_o'$ in the S2 sampling phase of the StrongARM latch circuit given in Figure 3-10 can be described in the s-domain based on the approximate small-signal models that are given in Figure 3-12 as follows:

$$\frac{\Delta v_x(s)}{\Delta v_{in}(s)} = \frac{g_{m2}}{s \cdot C_X} \quad (3-24)$$

$$\frac{\Delta v_o(s)}{\Delta v_{in}(s)} = \frac{g_{m2} \cdot g_{m3}}{s \cdot C_X \cdot C_O \left(s + \frac{g_{m3} \cdot (C_O - C_X)}{C_X \cdot C_O} \right)} \cong \frac{g_{m2} \cdot g_{m3}}{s^2 \cdot C_X \cdot C_O} \quad (3-25)$$

in which $\Delta v_{in} = v_{in} - v_{th}$, $C_X' = C_X$, $C_O' = C_O$, and g_{m2} and g_{m3} are the transconductances of the transistors N2/N2' and N3/N3' in the latch, respectively. As a note, the approximation in equation (3-25) is valid if the time constant of the non-zero pole in the equation is significantly longer than the S2 sampling phase's duration, i.e., if:

$$\left| \frac{C_X \cdot C_O}{g_{m3} \cdot (C_O - C_X)} \right| \gg t_2 - t_1 \quad (3-26)$$

From equation (3-24) and (3-25), it can be concluded that the StrongARM latch circuit given in Figure 3-10 performs an integration and double integration operation on Δv_{in} in its S1 and S2 sampling phase, respectively. If Δv_{in} is an impulse, Δv_{in} will produce a Δv_x step and a Δv_o ramp if it arrives at the latch's inputs while the latch is

operating in its S1 and S2 sampling phase, respectively. Any Δv_x step produced while the latch is operating in its S1 sampling phase will be converted to a Δv_o ramp after the latch enters its S2 sampling phase at t_1 . If g_{m2} is a constant, any impulses of the same amplitude that arrive while the latch is operating in its S1 sampling phase will produce the same Δv_o ramp. Meanwhile, if some (+) impulses of the same amplitude arrive while the latch is operating in its S2 sampling phase, the impulse that arrives earlier will produce a longer Δv_o ramp and causes Δv_o to reach a higher final value at the end of the S2 sampling phase. Thus, the StrongARM latch circuit's ISF can be described as follows:

$$\Gamma(t) \cong \frac{g_{m2}(t)}{C_X \cdot C_O} \cdot \int_{t_0}^{t_1} g_{m3}(\tau) d\tau \quad \text{for } t_0 < t < t_1 \quad (3-27)$$

$$\Gamma(t) \cong \frac{g_{m2}(t)}{C_X \cdot C_O} \cdot \int_t^{t_2} g_{m3}(\tau) d\tau \quad \text{for } t_1 < t < t_2 \quad (3-28)$$

Figure 3-13 shows how the ISF looks if g_{m2} and g_{m3} do not vary across time. However, it must always be noted that the shape of the ISF ultimately also depends on the shape of g_{m2} 's and g_{m3} 's trajectory across time. Nevertheless, in approximate hand analysis, it is helpful to assume that g_{m2} and g_{m3} do not vary across time. As a note, equation (3-27) and (3-28) improve on the expression for the ISF that [58] presents, which assumes constant g_{m2} and g_{m3} .

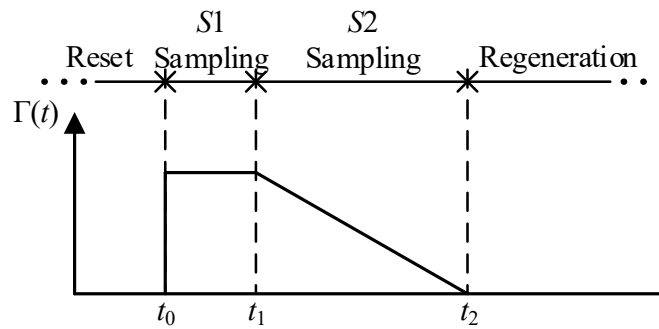


Figure 3-13 The ISF of the StrongARM latch circuit given in Figure 3-10 if the transconductances of N2, N2', N3, and N3' do not vary across time

Now, the I_{D2} in equation (3-22) and (3-23) are not some constants, and the exact t_0-t_1 and t_1-t_2 duration in equation (3-27) and (3-28) can practically be obtained only through simulations. Nonetheless, we are interested in some insights into how the durations change as the latch's design parameters are adjusted here.

With Figure 3-11 as a reference, we can find an approximation to I_{D2} 's peak value in the sampling phase, $I_{D2,peak}$, by solving the following equations:

$$I_{D1} = \mu_n \cdot C_{OX} \cdot \frac{W_1}{L_1} \cdot (V_{DD} - V_{TN1}) \cdot V_{TAIL} = \frac{V_{TAIL}}{r_{on}} \quad (3-29)$$

$$I_{D2} = \mu_n \cdot C_{OX} \cdot \frac{W_2}{L_2} \cdot (V_{IN} - V_{TAIL} - V_{TN2})^2 \cong \frac{I_{D1}}{2} \quad (3-30)$$

in which r_{on} here is the linear on-resistance of N1 looking into its drain terminal, μ_n is the electron's surface mobility, C_{OX} is the gate oxide capacitance of the MOSFETs in the latch per unit area, and W_1 and W_2 , L_1 and L_2 , V_{TN1} and V_{TN2} , and I_{D1} and I_{D2} are the widths, lengths, threshold voltages, and drain currents of N1 and N2/N2', respectively. Solving the equations yields the following expression:

$$I_{D2,peak} \cong \frac{1}{2 \cdot r_{on}} \cdot \left(V_{IN} - V_{TN2} + \frac{1}{2 \cdot k_2 \cdot r_{on}} \cdot \left(1 - \sqrt{1 + 4 \cdot (V_{IN} - V_{TN2}) \cdot k_2 \cdot r_{on}} \right) \right) \quad (3-31)$$

in which $k_2 = \mu_n \cdot C_{OX} \cdot W_2 / L_2$ here. From equation (3-31), it can be concluded that $I_{D2,peak}$ increases as r_{on} is reduced, V_{IN} is increased, or k_2 is increased. It must, however, be noted that the capacitances related to N2/N2' will increase as k_2 is increased, negating the effect of increasing k_2 . Moreover, $\lim_{k_2 \rightarrow \infty} I_{D2,peak} = \frac{V_{IN} - V_{TN2}}{2 \cdot r_{on}}$.

Conclusions:

In general, the bandwidth of the transfer function $H_s(s)$ in equation (3-21) will increase as the shape of its time-domain counterpart, i.e., the $\Gamma(t)$ given by equation (3-27) and (3-28), narrows. For a fixed C_O and C_X , $\Gamma(t)$'s shape will narrow as $I_{D2,peak}$ is increased since the durations t_0-t_1 and t_1-t_2 in equation (3-27) and (3-28) shorten and the shape of the $g_{m2}(t)$ waveform in equation (3-27) and (3-28) narrows as $I_{D2,peak}$ increases. $|H_s(j\omega_{in})|$ can thus be increased, primarily, by reducing r_{on} and increasing V_{IN} . Meanwhile, increasing k_2 increases $|H_s(j\omega_{in})|$ when the k_2 's value is smaller, after which increasing k_2 can decrease $|H_s(j\omega_{in})|$ instead. This conclusion generally holds although equation (3-30) is not strictly true (N2 and N2' may in some cases have operated in the linear region when I_{D2} peaks and I_{D1} does not all come from the drains of N2 and N2').

Figure 3-14 shows the pre-layout simulated values of the $|H_s(j\omega_{in})|$ of the StrongARM latch circuit given in Figure 3-10 at an f_{in} of 60 GHz under various W_1 and W_2 sizings across different V_{IN} values. Note that $r_{on} \propto 1/W_1$ and $k_2 \propto W_2$. As shown in Figure 3-14, $|H_s(j\omega_{in})|$ generally increases as V_{IN} is increased. $|H_s(j\omega_{in})|$ also generally increases as W_1 is increased and, thus, as r_{on} decreases. Meanwhile, $|H_s(j\omega_{in})|$ initially increases as W_2 is increased and, thus, as k_2 increases. However, further W_2 increments can cause $|H_s(j\omega_{in})|$ to decrease, instead. Therefore, we have confirmed that $|H_s(j\omega_{in})|$'s values across different V_{IN} levels, r_{on} values, and k_2 values behave as discussed in the analysis presented in this section.

As a note, in designing the radar pulse digitizer whose design is being presented here in this work, $|H_s(j\omega_{in})|$ should not be less than, give or take, -10 dB since it must be compensated by the signal amplification chain that precedes the digitizer

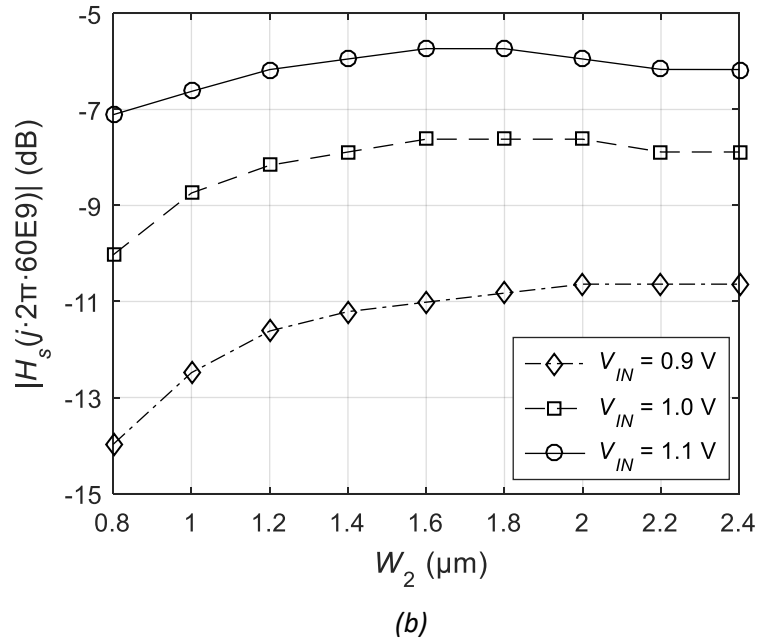
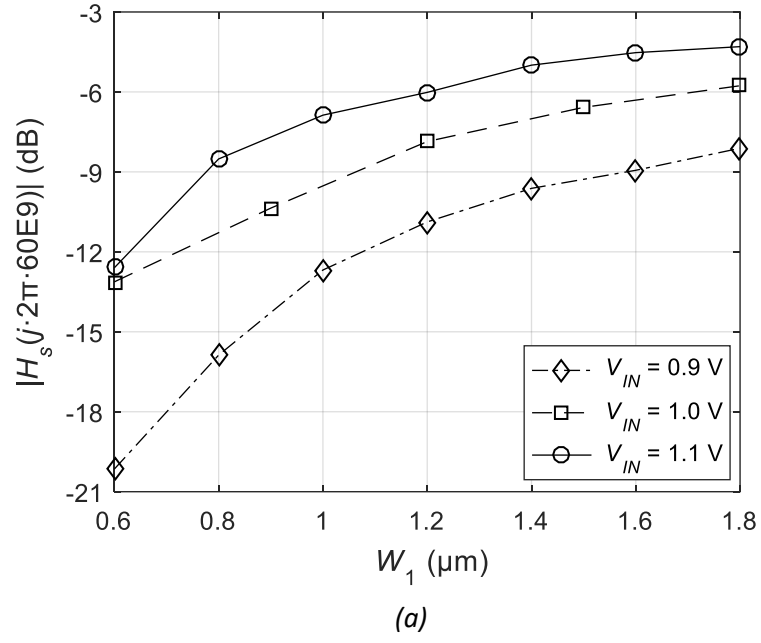


Figure 3-14 $|H_s(j\omega_{in})|$ of the StrongARM latch circuit given in Figure 3-10 at an f_{in} of 60 GHz with (a) its W_1 varied between $0.6\ \mu\text{m}$ – $1.8\ \mu\text{m}$ and its W_2 fixed at $1.6\ \mu\text{m}$ (b) its W_1 fixed at $1.2\ \mu\text{m}$ and its W_2 varied between $0.8\ \mu\text{m}$ – $2.4\ \mu\text{m}$; here, L_1 and L_2 are both at their minimum (40 nm)

3.2.1.2.2 StrongARM latch's parallel-equivalent input impedance

At f_{in} , the small-signal gain of the mm-wave RF buffer-driver of the direct-RF mm-wave radar pulse digitizer whose design is being presented here in this work with the buffer's output matching network designed to resonate with the total parallel-equivalent capacitance at the digitizer's input at f_{in} can be approximated as follows:

$$|H_{buf}(j\omega_{in})| \cong g_{m,buf} \cdot \frac{r_{in,d} \parallel r_{in,s}}{2^B - 1} \quad (3-32)$$

in which, with Figure 3-10 and Figure 3-15 as references:

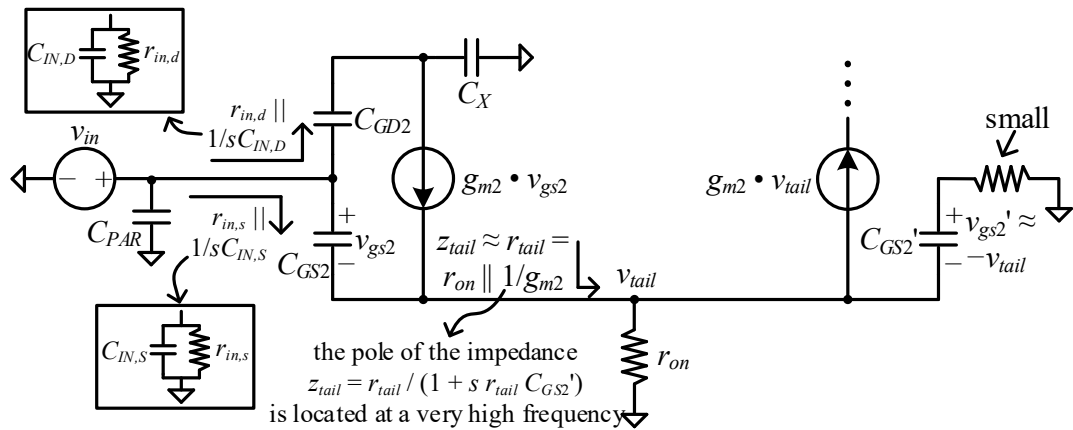
$$C_{IN,S} \cong \frac{C_{GS2}}{1 + g_{m2} \cdot r_{tail}} \cdot \frac{1}{1 + \left(\omega_{in} \cdot r_{tail} \cdot C_{GS2} / (1 + g_{m2} \cdot r_{tail}) \right)^2} \quad (3-33)$$

$$r_{in,s} \cong r_{tail} + \frac{r_{tail}}{\left(\omega_{in} \cdot r_{tail} \cdot C_{GS2} / (1 + g_{m2} \cdot r_{tail}) \right)^2}$$

$$C_{IN,D} \cong C_{GD2} \cdot C_X / (C_{GD2} + C_X) \quad (3-34)$$

$$r_{in,d} \cong (1/g_{m2} + r_{tail}) \cdot (1 + C_X/C_{GD2})$$

Here, $g_{m,buf}$ is the transconductance of the mm-wave RF buffer, B is the digitizer's resolution, $g_{m2} = g_{m2}'$, and r_{on} is the linear on-resistance of the transistor N1 in each StrongARM latch in the digitizer. Meanwhile, g_{m2}/g_{m2}' , C_{GS2}/C_{GS2}' , and C_{GD2}/C_{GD2}' are the transconductance, gate-to-source capacitance, and gate-to-drain capacitance of the transistor N2/N2' in the latches, respectively. The equations are derived based on the small-signal model given in Figure 3-15. The equations will be representative of $|H_{buf}(j\omega_{in})|$'s rough trend with changes in the latches' design parameters provided that: 1) the durations of the latches' S2 sampling phase are not significantly longer than those of their S1 sampling phase, 2) N2/N2' stays to operate in the saturation region for most of the latches' S1 sampling phase durations. The derivation also assumes that the quality-factor (Q -factor) of the buffer's output matching network, by itself, is high compared to the Q -factor of the digitizer's input impedance network.



In the particular StrongARM latch circuit that we designed to implement the direct-RF mm-wave radar pulse digitizer, $r_{in,d}$ and $r_{in,s}$ are both in a similar order of magnitude at 60 GHz, and $(r_{in,d} || r_{in,s})$ increases as the value of the term $r_{tail} = r_{on} || 1/g_{m2}$ in equation (3-33) and (3-34) is increased. Increasing r_{on} (which can be done by reducing N1's W/L ratio) will, in overall, also reduce the drain current values of N2/N2' in the latch's sampling phase. Hence, increasing r_{on} will also cause the effective value of the term $1/g_{m2}$ in equation (3-34) to increase.

Meanwhile, decreasing k_2 will increase $(r_{in,d} \parallel r_{in,s})$ primarily because decreasing W_2 will cause the C_{GS2} in equation (3-33) to decrease, increasing the second term in the right half side of the $r_{in,s}$ equation in equation (3-33).

Conclusions:

The StrongARM latches in the direct-RF mm-wave radar pulse digitizer whose design is presented in this work must be designed with smaller W/L ratios for their N1 and N2 so that the digitizer can present a higher total parallel-equivalent resistance to the mm-wave RF buffer circuit that drives the digitizer. A higher total parallel-equivalent resistance at the output of the mm-wave RF buffer means that, for a given $g_{m,buf}$ value, the buffer's gain will be higher.

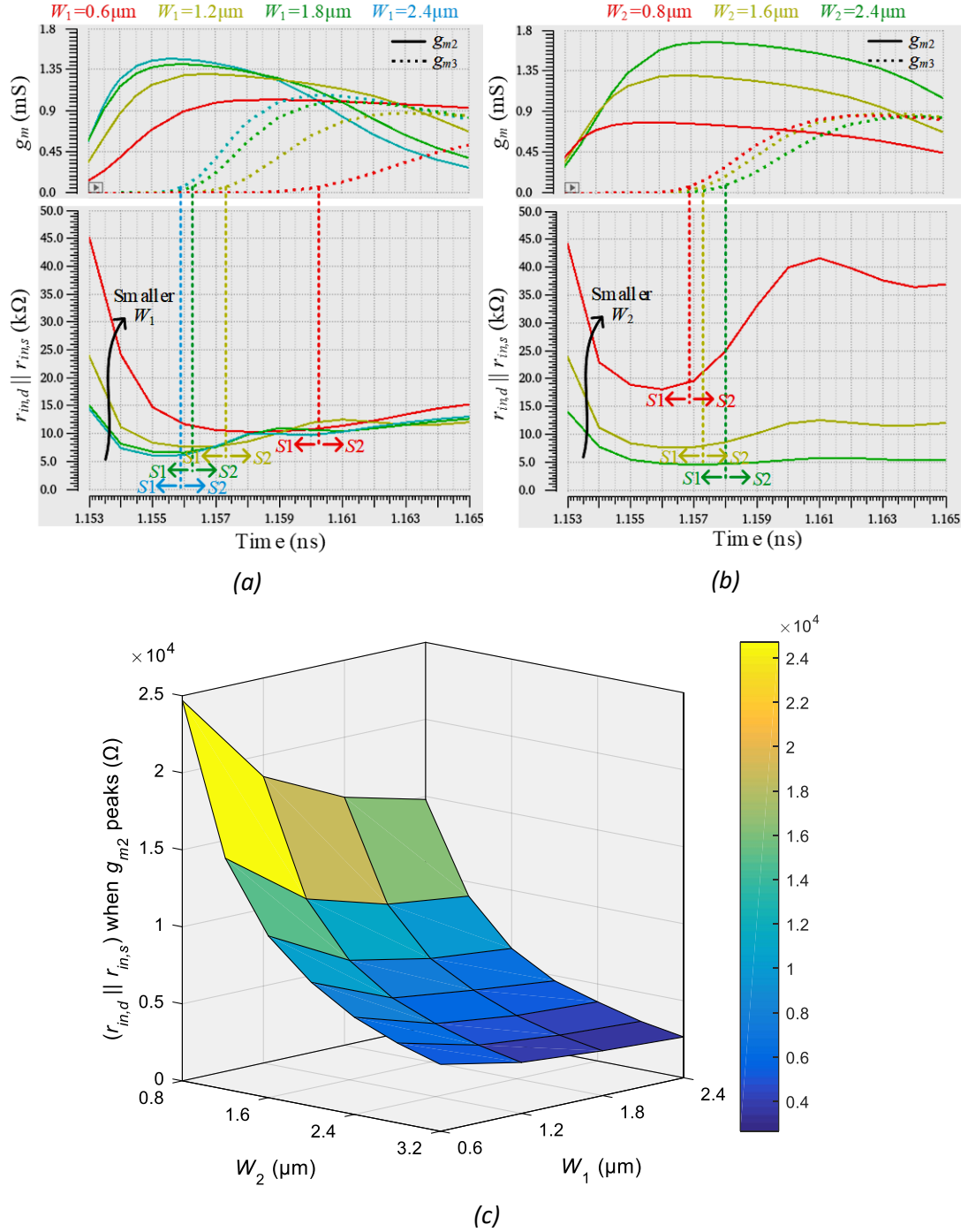


Figure 3-16 ($r_{in,d} \parallel r_{in,s}$) of the StrongARM latch circuit given in Figure 3-10 at an f_{in} of 60 GHz when the latch is operating in its sampling phase with (a) its W_1 varied between 0.6 μm – 2.4 μm and its W_2 fixed at 1.6 μm (b) its W_1 fixed at 1.2 μm and its W_2 varied between 0.8 μm – 2.4 μm , and (c) ($r_{in,d} \parallel r_{in,s}$)'s values when g_{m2} peaks in the latch's sampling phase across different W_1 (0.6 μm – 2.4 μm) and W_2 (0.8 μm – 3.2 μm) sizing combinations; here, L_1 and L_2 are both at their minimum (40 nm) and V_{IN} is 1V

Figure 3-16 shows the pre-layout simulated values of the $(r_{in,d} || r_{in,s})$ of the StrongARM latch circuit given in Figure 3-10 at an f_{in} of 60 GHz when the latch is operating in its sampling phase under various W_1 and W_2 sizing combinations. As shown in Figure 3-16a, a smaller W_1 and, thus, a higher r_{on} will notably increase the latch's parallel-equivalent input resistance in the latch's S1 sampling phase. Meanwhile, a smaller W_2 will increase the latch's parallel-equivalent input resistance throughout the latch's sampling phase, as shown in Figure 3-16b. This trend is further corroborated by Figure 3-16c in which we compare the latch's $(r_{in,d} || r_{in,s})$ values when the latch's g_{m2} peaks or, in other words, when its ISF peaks in its sampling phase across more W_1 and W_2 sizing combinations. As shown in Figure 3-16c, reducing W_1 or W_2 will always increase the latch's parallel-equivalent input resistance at the peak of the latch's ISF in the sampling phase. Thus, we have confirmed that the latch must be designed with smaller N1 and N2 transistors to increase its parallel-equivalent input resistance.

3.2.1.3 Linearity

This work presents a digitizer design that is meant to be used in a direct-RF mm-wave UWB pulse-Doppler radar receiver implementation. The digitizer is implemented based on the novel ADC architecture presented in section 3.1, and the schematic of the comparators in the digitizer is given in Figure 3-10. In designing the digitizer, the digitizer cannot, in a practical manner, be designed with a sampling bandwidth that is much higher than its input signal frequency since the digitizer's input signal frequency is very high here. This condition contrasts with the condition in which a typical ADC is operated. Thus, the modulation of the digitizer's sampling bandwidth by its input signal is a significant source of nonlinearity that must be addressed in the design of the digitizer.

From the analysis presented in section 3.2.1.2.1, it can be understood that the sampling bandwidth of the comparators in the digitizer, which is the bandwidth of the term $H_s(s)$ in equation (3-21), will vary when there is a large-signal change in the digitizer's input signal value, i.e., when there is a change in V_{IN} 's value. With a higher V_{IN} value, the waveforms of the bias current I_{D2} of the StrongARM latches in the digitizer in the latches' sampling phase will have narrower shapes and higher peaks, narrowing the latches' ISFs, and vice versa. Since the digitizer subjects its input signal to differing amounts of attenuation as the signal swings across the digitizer's input range, the signal will appear distorted at the digitizer's output. Therefore, the less sensitive the I_{D2} waveforms' shapes are to a change in V_{IN} 's value, the less distorted the digitizer's output waveform will be.

The following equation, which is derived from equation (3-31), can be used to deduce a trend in the sensitivity of the I_{D2} waveforms' shapes to a change in V_{IN} 's value:

$$\frac{V_{IN}}{I_{D2,peak}} \cdot \frac{dI_{D2,peak}}{dV_{IN}} = \frac{\frac{1}{\sqrt{1 + 4 \cdot V_{IT2} \cdot k_2 \cdot r_{on}} - 1}}{\sqrt{1 + 4 \cdot V_{IT2} \cdot k_2 \cdot r_{on}} - \frac{1 + 4 \cdot V_{IT2} \cdot k_2 \cdot r_{on}}{1 + 2 \cdot V_{IT2} \cdot k_2 \cdot r_{on}}} \cdot \frac{1}{1 + \frac{1}{2 \cdot V_{IT2} \cdot k_2 \cdot r_{on}}} \cdot \frac{1}{V_{IT2}} \cdot V_{IN} \quad (3-35)$$

in which $V_{IT2} = V_{IN} - V_{TN2}$ here. Equation (3-35) decreases monotonically as $k_2 \cdot r_{on}$ increases and:

$$\lim_{k_2 \cdot r_{on} \rightarrow 0} \frac{V_{IN}}{I_{D2,peak}} \cdot \frac{dI_{D2,peak}}{dV_{IN}} = \frac{2}{1 - V_{TN2}/V_{IN}} \quad (3-36)$$

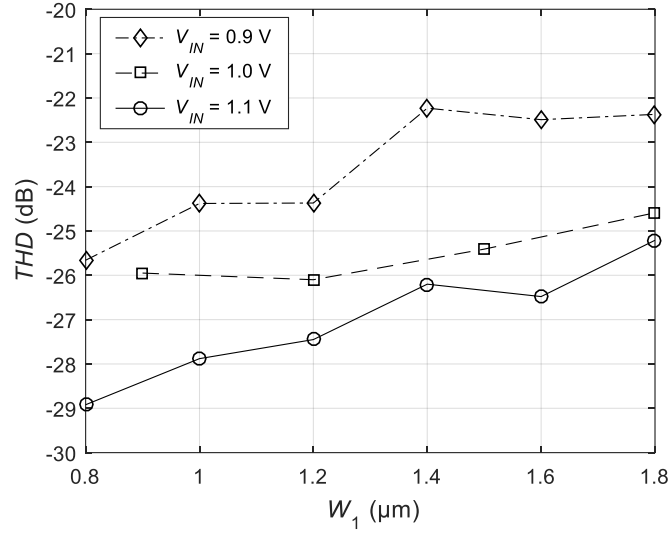
$$\lim_{k_2 \cdot r_{on} \rightarrow \infty} \frac{V_{IN}}{I_{D2,peak}} \cdot \frac{dI_{D2,peak}}{dV_{IN}} = \frac{1}{1 - V_{TN2}/V_{IN}} \quad (3-37)$$

Conclusions:

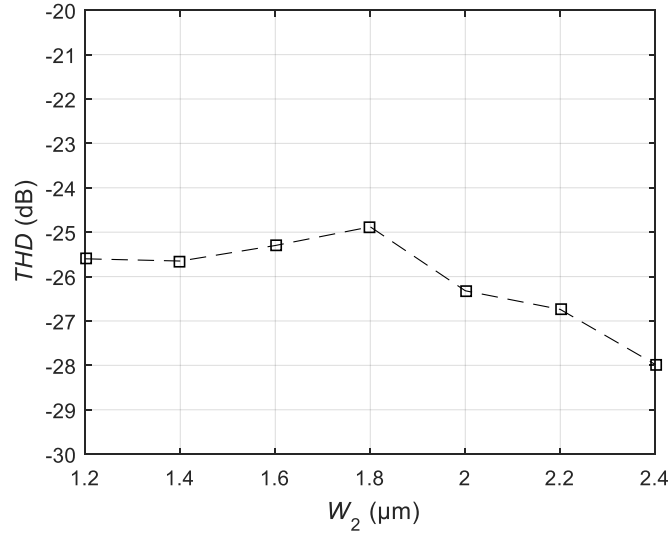
From equation (3-35), (3-36), and (3-37), it can be concluded that increasing r_{on} or V_{IN} will make the shapes of the I_{D2} waveforms of the StrongARM latches in the digitizer in the latches' sampling phase less sensitive to a change in V_{IN} 's value and, thus, improve the digitizer's linearity performance.

Note that we may also conclude from equation (3-35), (3-36), and (3-37) that increasing k_2 (i.e., increasing the W/L ratio of $N2/N2'$) will also improve the digitizer's linearity performance. However, it must be noted that the gate-to-source and gate-to-drain capacitance of $N2/N2'$ are not accounted for in equation (3-35). These capacitances will increase in value as k_2 is increased, increasing the coupling to and loading at the latches' internal nodes. The effect of increasing/decreasing k_2 on the digitizer's linearity performance is not very predictable.

Figure 3-17 shows the pre-layout simulated values of the -6-dBFS THD of the mm-wave UWB radar pulse digitizer design given in Figure 3-10 at an f_{in} of 60 GHz across different V_{IN} values with some variations in the W_1 and W_2 sizings of its latches. As shown in Figure 3-17a, the digitizer's linearity performance generally improves as the digitizer's V_{IN} level is increased. The digitizer's linearity performance also generally improves as the W_1 sizing of the latches in the digitizer is reduced (note that $r_{on} \propto 1/W_1$). Meanwhile, there is no consistent trend in the digitizer's linearity performance with the W_2 sizing of the latches in the digitizer varied. Therefore, we have confirmed that the digitizer's linearity performance across different V_{IN} level, W_1 sizing, and W_2 sizing behaves as discussed in the analysis presented in this section.



(a)



(b)

Figure 3-17 The pre-layout simulated values of the -6-dBFS THD of the mm-wave UWB radar pulse digitizer design given in Figure 3-10 at an f_{in} of 60 GHz with (a) its latches' W_1 and W_2 sizings varied between $0.8\text{ }\mu\text{m}$ – $1.8\text{ }\mu\text{m}$ and fixed at $1.6\text{ }\mu\text{m}$, respectively, and its V_{IN} bias level varied between 0.9 V – 1.1 V (b) its latches' W_1 and W_2 sizings fixed at $1.2\text{ }\mu\text{m}$ and varied between $1.2\text{ }\mu\text{m}$ – $2.4\text{ }\mu\text{m}$, respectively, at a V_{IN} bias level of 1 V ; here, L_1 and L_2 are both at their minimum (40 nm)

3.2.1.4 DC offset

According to [78], the random DC offset of a StrongARM latch circuit can be primarily contributed by the mismatches in the latch's differential input pair. This statement is especially true when the latch's input pair is designed using transistors with small gate lengths and operated with a large g_m/I_D ratio (i.e., when the gate width of the

transistors in the pair is relatively large), making the random threshold mismatch between transistors in the pair the latch's primary random DC offset contributor.

With Figure 3-10 as a reference, the variance of the random DC offsets, $\sigma^2(V_{OFF})$, of the comparators in the mm-wave UWB radar pulse digitizer circuit whose design is being presented here in this work can thus be approximated as follows:

$$\begin{aligned}
 \sigma^2(V_{OFF}) &\cong \sigma^2(\Delta V_{TN2}) + \frac{I_{D1}}{4 \cdot k' \cdot \frac{W_2}{L_2}} \cdot \left(\sigma^2\left(\frac{\Delta k'}{k'}\right) + \sigma^2\left(\frac{\Delta\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_2}{L_2}\right)}\right) \right) \\
 &= \sigma^2(\Delta V_{TN2}) + \frac{I_{D1}}{4 \cdot k' \cdot \frac{W_2}{L_2}} \cdot \left(\frac{A_{k'}^2}{W_2 \cdot L_2} + \frac{A_{WL}^2}{W_2^2} + \frac{A_{WL}^2}{L_2^2} \right) \quad (3-38) \\
 &= \sigma^2(\Delta V_{TN2}) + \frac{I_{D1}}{4 \cdot k'} \cdot \left(\frac{A_{k'}^2}{W_2^2} + \frac{A_{WL}^2}{W_2 \cdot L_2} \right) + \frac{I_{D1}}{4 \cdot k' \cdot \frac{W_2}{L_2}} \cdot \frac{A_{WL}^2}{W_2^2}
 \end{aligned}$$

in which ΔV_{TN2} is the random difference between the threshold voltages of N2 and N2', $k' = \mu_n \cdot C_{OX}$, $A_{k'}$ is a constant related to the random mismatch between the k' values of N2 and N2', and A_{WL} is a constant related to the random mismatches between the widths and lengths of N2 and N2'.

From equation (3-38), we can deduce how to reduce the random DC offsets of the StrongARM latches in the digitizer when the latches' transistor lengths must be kept at their minimum. First, the $\sigma^2(\Delta V_{TN2})$ term in equation (3-38) can be reduced by increasing the gate areas of the transistors N2 and N2' in the latches by increasing their widths. Meanwhile, assuming that, as the latches' r_{on} , V_{IN} , and k_2 parameters are varied, the general behavior of the I_{D1} terms in equation (3-38) follows that of the $I_{D2,peak}$ given in equation (3-31), the other terms at the right-hand side of equation (3-38) can be reduced by increasing r_{on} , reducing V_{IN} , or increasing W_2 .

Figure 3-18 shows the histograms of the Monte Carlo simulated post-layout offset of the StrongARM latch circuit that we designed for use in the proposed digitizer

under different V_{IN} bias levels at 4 GHz of clock frequency. The offset's standard deviation (σ) increases with increasing V_{IN} bias level. This behavior is expected considering equation (3-38), and since, as the V_{IN} bias level is increased, the latch's input pair will operate in the linear region for a longer portion of the latch's sampling phase, causing the transistors to operate with reduced transconductance values for a longer portion of the latch's sampling phase [78]. Nevertheless, as will be presented in section 3.3, the proposed digitizer's comparator offsets calibration function can be designed with the capability to compensate for these ranges of offsets. The measured *DNL/INL/THD* performance of a prototype of the digitizer presented in section 3.3.3 and 3.3.4 also shows that the digitizer can perform as expected, although some of its comparators have almost 100 mV of offsets.

Figure 3-18 also shows that the offset's σ increases with temperature, and the increase is more significant when the V_{IN} bias level is higher. Nevertheless, the increase in the σ can be small even when the V_{IN} bias level is equal to the latch's supply level, as in the case of our design. For our design, when the V_{IN} bias level is 1.1 V, the increase in the σ value is only from 26.2 mV at 27°C to 26.8 mV at 85°C.

Lastly, we note that the offset of a StrongARM latch may change discernibly with temperature change, and when it changes with temperature change, the change tends to be more significant when the latch's V_{IN} bias level is higher. The offset of the StrongARM latch circuit that we designed for use in the proposed digitizer may change by at most ~ 7.8 mV (i.e., 7.8 mV is a 6- σ value) between 27°C and 85°C/-20°C when its V_{IN} bias level is equal to 1.1 V. Therefore the latch's offset value may change by up to ~ 2 LSBs (the 6-bit proposed digitizer is implemented with an LSB size of ~ 3.9 mV) from its 27°C value. As described in section 3.1.4.2, comparator offsets cause a reduced input range for the proposed digitizer. If the range must be maintained, the digitizer can be calibrated during the pulse radar receiver's idle time before the radar

uses the digitizer to digitize a radar pulse-echo signal. Alternatively, an on-chip temperature sensor can be incorporated to detect a significant change in junction temperature and trigger a re-calibration when needed. Lastly, in the proposed digitizer, the few comparators whose offsets are known to change significantly across temperatures can be disabled without affecting the digitizer's operation while only causing a slight noise performance degradation to the digitizer, as described in section 3.1.4.2.

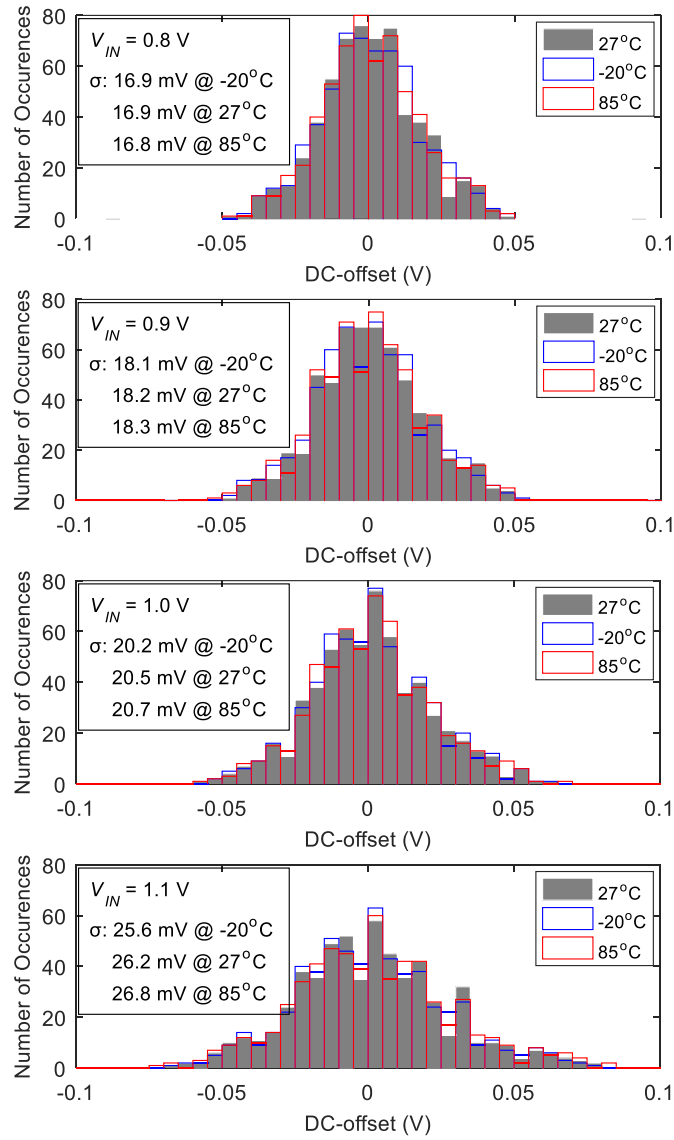


Figure 3-18 The histograms of the Monte Carlo simulated post-layout offset of the StrongARM latch circuit given in Figure 3-10 under different V_{IN} bias levels and temperatures while the latch is operated with a 4 GHz clock frequency (here, $W_1/L_1=1.2\mu\text{m}/0.04\mu\text{m}$, $W_2/L_2=1.6\mu\text{m}/0.04\mu\text{m}$, $W_3/L_3=1.6\mu\text{m}/0.04\mu\text{m}$, sample size=600)

3.2.1.5 Noise

Following the analysis presented in [58, 79], it can be deduced that the following can be done to reduce a StrongARM latch circuit's input-referred noise, that is, to reduce the input-referred noise of the StrongARM latches in the mm-wave UWB radar pulse digitizer circuit whose design is being discussed here in this work:

1. Increasing the W/L ratio of the transistors in the differential input pairs of the latches, that is, the W/L ratio of the transistors N2 and N2' in Figure 3-10.
2. Reducing the latches' input signal bias voltage, that is, the bias voltage of the signal v_{IN} in Figure 3-10.
3. Reducing the W/L ratio of the tail NMOS devices in the latches, that is, the W/L ratio of the transistor N1 in Figure 3-10.

3.2.1.6 Recap

This work presents the design of a digitizer that is meant to be used in a direct-RF mm-wave UWB pulse-Doppler radar receiver implementation. The digitizer's design is based on the novel ADC architecture presented in section 3.1, and each of the input signal comparators in the digitizer is implemented using a "bare" StrongARM latch circuit, as shown in Figure 3-10. Table 3-3 lists the electrical performances of the latch that are essential to the digitizer's operation. Table 3-3 also summarizes the relations between some of the latch's design parameters (i.e., the linear on-resistance of the tail NMOS device in the latch r_{on} , the input signal bias level of the latch V_{IN} , and the width of the transistors in the differential input pair of the latch W_2) and these electrical performances. Note that, in this work, the lengths of the transistors in the latch are fixed, that is, at their minimum because the shorter they are, the higher the latch's clock frequency and sampling bandwidth can be.

Table 3-3 The design parameters of the StrongARM latch circuit whose schematic is given in Figure 3-10 and how they affect the latch's electrical performances

<i>Desired Outcome</i>	r_{on}	V_{IN}	W_2	Note: ^ depends on the design point
<i>Increasing $H_{buf}(j\omega_{in})$</i>	increase^	minor contribution^	reduce^	
<i>Increasing $H_s(j\omega_{in})$</i>	reduce	increase	increase	
<i>Improving linearity</i>	increase	increase	not definite	
<i>Reducing random DC offset</i>	increase	reduce	increase	
<i>Reducing input-referred noise</i>	increase	reduce	increase	

In designing the StrongARM latches of the digitizer, judicious compromises must be made so that the goals of the digitizer's design efforts can be achieved, and Table 3-3 can be used to navigate the design efforts:

In this work, the primary goal of the digitizer's design efforts is to optimize the trade-off between the digitizer's noise and linearity performance, given some limitations concerning the digitizer's other electrical performances. Thus, the W_2 sizing of the StrongARM latches in the digitizer cannot be so large that the mm-wave RF buffer driving the digitizer must consume a large amount of power to drive the digitizer with a sufficient gain. Also, the latches' W_1 sizing cannot be so small that the digitizer's attenuation of its mm-wave input signal is very large since the large attenuation must be compensated by a large gain in the signal amplification chain that precedes the digitizer. Meanwhile, the digitizer's V_{IN} bias level choice will be discussed in section 3.2.1.6.1 since the trade-offs that ensued from an adjustment in the level are less straightforward. Lastly, comparator offsets reduction is not a priority in the latches' design optimization since the digitizer's architecture can tolerate large comparator offsets (see section 3.1.4). Nevertheless, comparator offsets cause some residual effects on the digitizer's linearity performances even after the digitizer has been calibrated to compensate for these offsets. Section 3.2.1.6.2 is dedicated to discussing how these residual effects can be managed.

3.2.1.6.1 Noise, linearity, and attenuation trade-offs through V_{IN} adjustment

The digitizer's noise performance, linearity performance, and attenuation of a very high-frequency input signal will trade-off with each other as the digitizer's V_{IN} bias level is adjusted. A higher V_{IN} will improve the digitizer's linearity and attenuation of a very high-frequency input signal and vice versa. However, a higher V_{IN} bias level will also increase the digitizer's input-referred noise level. Therefore, for a given full-scale input range at a certain input signal frequency higher than the digitizer's sampling bandwidth, there exists a V_{IN} level that will give the digitizer the best noise performance as the V_{IN} bias level is adjusted as illustrated in Figure 3-19. Furthermore, some of the digitizer's noise performance must be sacrificed if the design must achieve a better linearity performance. As a note, the gate voltages of the NMOS devices in the LP CMOS process used to fabricate the digitizer in this work can go above the maximum allowed supply level in a substantial manner ($\sim 1.4\times$) before they can cause the devices reliability issues. The digitizer's input voltage value can thus be higher than its supply voltage value.

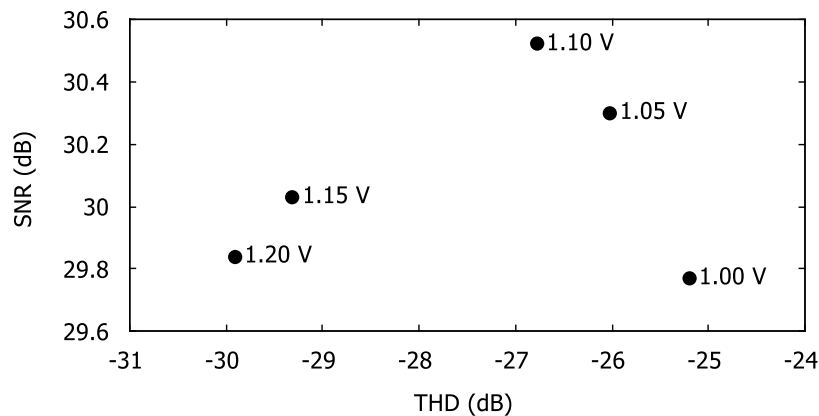


Figure 3-19 The post-layout simulated -1 -dBFS SNR and THD of the mm-wave UWB radar pulse digitizer design given in Figure 3-10 (without its RF buffer-driver) across different input signal bias levels (1.00 V to 1.2 V) for a 60 GHz input signal and a 60 GHz full-scale input range of 750 mV

3.2.1.6.2 Comparator offsets' residual effects

Considering the ADC architecture that the digitizer's design is based on (see section 3.1), the DC offsets of the comparators in the digitizer are not causes for concern by themselves.

The DC offsets are of concern when they can be large and cause some sub-ADCs in the digitizer to operate with a substantially lower input common-mode level due to how they are compensated in the digitizer (see section 3.1.4). The linearity performance of these sub-ADCs whose comparators have large negative DC offsets will not be as good as that of the other sub-ADCs in the digitizer.

The DC offsets are also of concern when they can be large and cause some sub-ADCs in the digitizer to operate with a substantially higher input common-mode level due to how they are compensated in the digitizer. These sub-ADCs whose comparators have large positive DC offsets do not attenuate their input signal as much as the other sub-ADCs in the digitizer. Consequently, if no sub-ADCs in the digitizer can be allowed to saturate, the digitizer's input signal amplitude must be constrained because of these few sub-ADCs.

Figure 3-20 shows that, for a 60 GHz sinusoidal input signal, the attenuation level of the StrongARM latch circuit used in the digitizer design (whose schematic is given in Figure 3-10) varies by about ± 1.5 dB as the latch's input common-mode level is adjusted by ± 0.1 V from a nominal value of 1.1 V.

Consequently, if the digitizer is to be operated with a V_{IN} bias level of 1.1 V and the DC offsets of the StrongARM latches in the digitizer are expected to be almost always less than, e.g., $(1.2 \text{ V} - 1.1 \text{ V}) = 0.1 \text{ V}$, around $(-7.5 \text{ dB}) - (-9 \text{ dB}) = 1.5 \text{ dB}$ of the digitizer's full-scale input range will be wasted if none of the sub-ADCs in the digitizer are allowed to saturate.

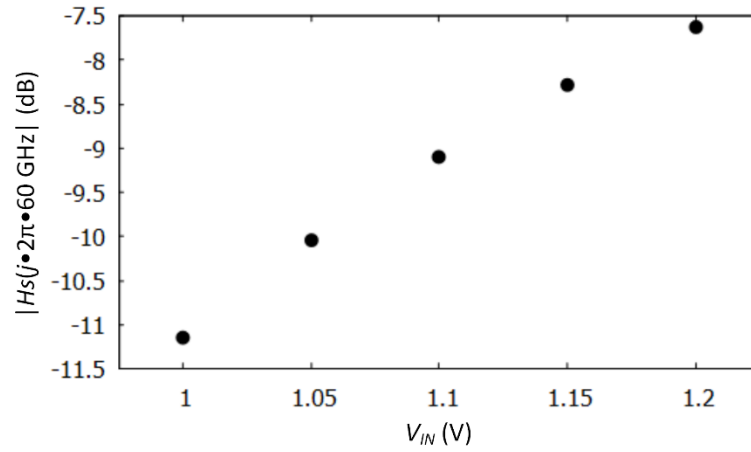


Figure 3-20 The post-layout simulated attenuation level of the StrongARM latch circuit given in Figure 3-10 across different input signal bias levels (1 V to 1.2 V) for a 675 mV_{pk-pk} 60 GHz sinusoidal input signal

One or a combination of the following can be done to manage the above-described problem:

- 1) The r_{on} and W_2 of the StrongARM latches in the digitizer can be increased to reduce the variance level of the random DC offsets of the latches. However, this adjustment will be limited since it must be made while paying careful attention to the changes in the latches' other electrical performances.
- 2) The digitizer's full-scale input range can be widened to cater to the few sub-ADCs whose comparator offsets are very large. However, this adjustment is limited by the increase in the digitizer's quantization noise level.
- 3) After the digitizer is calibrated and the DC offsets of the comparators in the digitizer are determined, the sub-ADCs whose comparator offsets are found to be large can be disabled. As discussed in section 3.1.4.2, doing so will only cause minor SNR degradation, especially if the digitizer's input signal is already noisy.
- 4) Lastly, we can also do nothing and let the sub-ADCs whose comparator offsets are large saturate. The distortions contributed by each of these sub-ADCs will be slight since the distortions that it contributes will be divided by the total number of sub-ADCs that the digitizer has.

3.2.2 Clock and Input Signal Distribution

3.2.2.1 Skew

This work discusses the design of a digitizer that is meant to be used in a direct-RF mm-wave UWB pulse-Doppler radar receiver implementation. Each of the digitizer's comparators belongs to a separate sub-ADC unit, and each of these sub-ADCs is operable as a complete digitizer by itself. Hence, the presence of skews among the clock (v_{CK}) and input signal (v_{IN}) paths to the comparators in the digitizer does not distort the digitizer's output waveform, unlike in a flash ADC. Nevertheless, the skews will degrade the digitizer's bandwidth by causing phase mismatches among the outputs of the sub-ADCs in the digitizer. In this work, the digitizer's clock distribution network and input signal distribution network are drawn as H-trees [80], as shown in Figure 3-21, to minimize this bandwidth degradation.

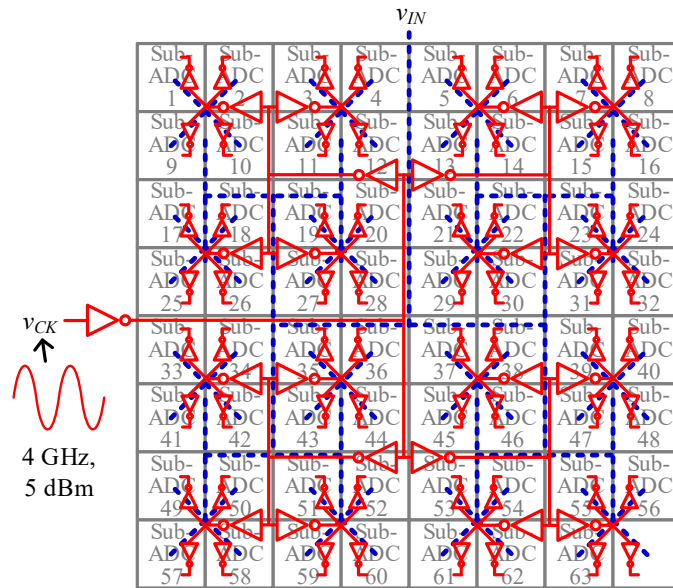


Figure 3-21 The clock (v_{CK}) and input signal (v_{IN}) distribution network of the 6-bit mm-wave UWB radar pulse digitizer circuit designed in this work

3.2.2.2 Jitter

The digitizer's input signal frequency, f_{in} , in its targeted end-use as the digitizer of a direct-RF mm-wave UWB pulse radar receiver will be very high. Thus, the digitizer's clock distribution network must be designed with a considerably low jitter level. Jitters in the clock signals of the sub-ADCs in the digitizer will limit the digitizer's noise performance as follows [81]:

$$SNR < -20 \cdot \log(2\pi \cdot f_{in} \cdot t_j) + 10 \cdot \log(2^B - 1) \quad (3-39)$$

in which t_j is the clock signals' jitter level in RMS seconds, and the $10 \cdot \log(2^B - 1)$ term in the equation accounts for the averaging inherent in the digitizer's digitization process (see section 3.1.3).

In this work, the digitizer's clock distribution network is designed with a simulated jitter level of ~35 fs RMS when the network is driven by a 5 dBm 4 GHz sine wave v_{CK} signal. The network's inverters are designed using transistors with large gate widths to achieve this level of jitter [82]. The effective jitter level in the network's v_{CK} signal input is expected to be <100 fs RMS with the self-coherence effect considered [51] (see section 4.3.4.1). Thus, the network's contribution to the total jitter level at the clock input pin of each comparator in the digitizer is small ($\sqrt{100^2 + 35^2} \approx 106$ fs RMS).

3.2.3 Staircase Threshold Voltages Generator Implementation

Figure 3-22 shows how the bank of digital-to-analog converters (DAC) that generates the staircase threshold voltages, $V_{TH,i} = \{V_{TH,1}, V_{TH,2}, \dots, V_{TH,2^B-1}\}$, for the sub-ADCs in the mm-wave UWB radar pulse digitizer whose design is being discussed here in this work is implemented. All the $(B+B_{ext})$ -bit DACs in the bank refer to the same reference resistor ladder. Here, B is the digitizer's resolution, and the DACs are implemented with extra input bits B_{ext} to support the implementation of the digitizer's offsets calibration (see section 3.1.4). Lastly, the ladder is decoupled at its taps to reduce the kickback-related crosstalks among the sub-ADCs in the digitizer.

As a note, in implementing the proposed digitizer, we designed the reference resistor ladder with low *DNL* values of much less than 0.1 LSB (based on our Monte Carlo simulation results). The *DNL* values do not have any noticeable increase/decrease with temperature (between -20°C and 85 °C), and the reference ladder's silicon area usage is still relatively small compared to the proposed digitizer's total silicon area usage (as shown in Figure 3-24 in section 3.3).

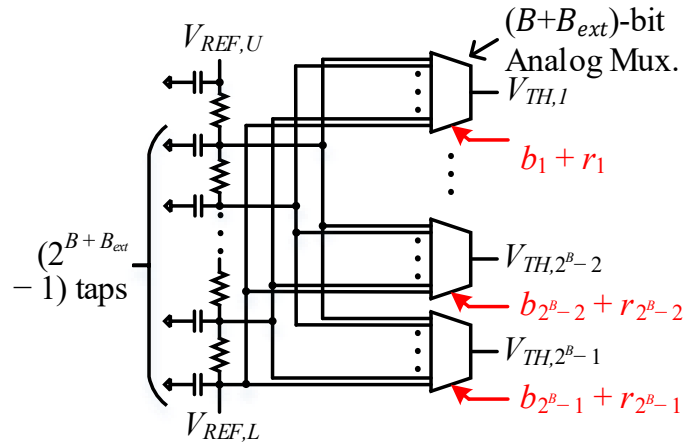


Figure 3-22 The bank of DACs generating the staircase threshold voltages for the sub-ADCs in the mm-wave UWB radar pulse digitizer circuit designed in this work

In generating the $V_{TH,i}$, the multiplexers in the bank, each, will select a tap on the ladder according to the sum of the output of a B -bit digital staircase counter (b_i) and the value kept in an offset calibration register (r_i). This arrangement implements equation (3-18) given in section 3.1.4. The counters, $b_i = \{b_1, b_2, \dots, b_{2^B-1}\}$, each will initialize to a unique value so that the counters' outputs are always different from each other, minimizing the extent of correlations among the B -bit outputs of the sub-ADCs in the digitizer, thus maximizing the digitizer's noise performance (see section 3.1.3). For an area-efficient design, the width of the calibration registers, $r_i = \{r_1, r_2, \dots, r_{2^B-1}\}$, should be chosen so that the resulting calibration range is just enough to cover the range of the offsets that the comparators in the digitizer can have.

3.2.4 Adder Design and Back-End Processing

The 1-bit outputs of the sub-ADCs in the mm-wave UWB radar pulse digitizer circuit whose design is being discussed here in this work, i.e., the $d_i = \{d_1, d_2, \dots, d_{2^B-1}\}$ as referred to in section 3.1.3, are added together using a pipelined Wallace tree adder circuit. The pipelines in the adder circuit are implemented using C²MOS flip-flops, whose schematic is given in Figure 3-23, with only up to two full adders in the paths between any two flip-flops in the adder. The adder circuit achieves a maximum operating clock frequency of more than 4 GHz.

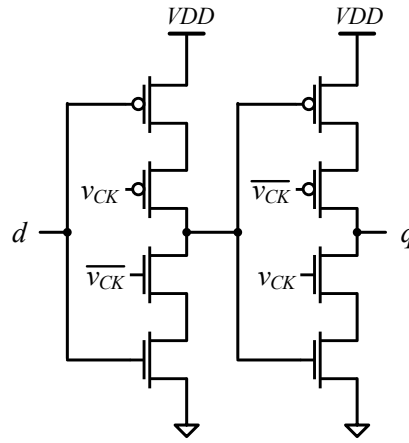


Figure 3-23 The schematic of the C²MOS flip-flop circuit used to implement the pipelines in the Wallace tree adder circuit in the mm-wave UWB radar pulse digitizer circuit designed in this work

In this work, the L -point accumulator of the digitizer is not implemented on-chip (see the discussions presented in section 3.1.3 for the role of the accumulator in the digitizer's operation). The accumulator is instead implemented using a logic analyzer off-chip. Before the outputs from the Wallace-tree adder circuit of the digitizer are sent off-chip, the data is first decimated on-chip so that they can be processed off-chip at a low enough rate.

3.3 Implementation and Measurement Results

A test chip containing a 6-bit prototype of the mm-wave UWB radar pulse digitizer proposed in this work is fabricated in a 40 nm LP CMOS technology. The prototype digitizer is implemented without its mm-wave RF buffer-driver in the test chip to allow for extensive characterizations of the digitizer circuit in itself. Figure 3-24 shows the die photograph and the layout of the test chip, and a schematic showing the circuitries included in the test chip is given in Figure 3-25.

Figure 3-25 also illustrates the setup used to characterize the test chip. The characterization was done on a probe station. In the characterization, Agilent E8361C and R&S SMF100A were used to generate the prototype digitizer's mm-wave sine wave input signal and 4 GHz sine wave clock signal, respectively. These signals were delivered into the test chip through 64-GHz-capable bias tees, coaxial cables, and probe heads. The test chip's control signals, which toggled at frequencies of a few MHz only, and power were delivered using multi-pin probe heads. The test chip has a ~ 0.5 nF on-chip bypassing to facilitate the through-probe power delivery.

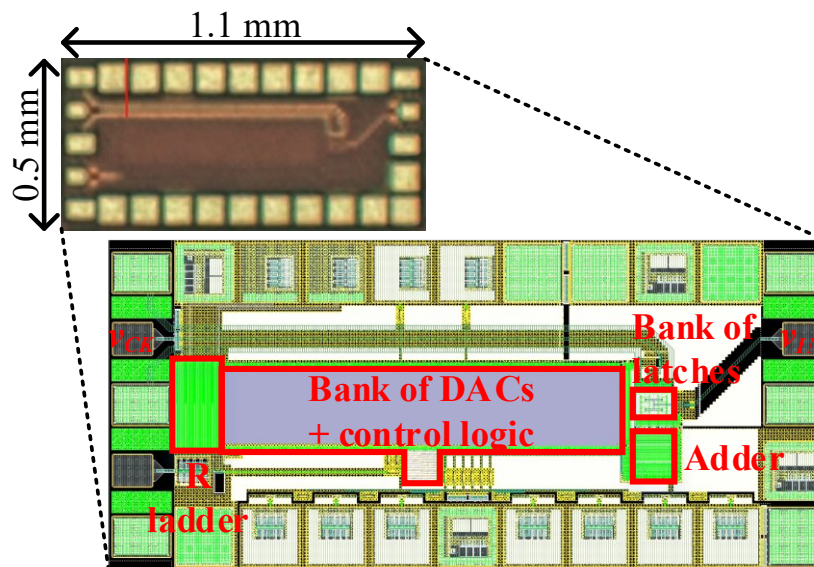


Figure 3-24 The die photograph and layout of a 6-bit prototype test chip of the mm-wave UWB radar pulse digitizer design proposed in this work that is fabricated in a 40 nm LP CMOS technology

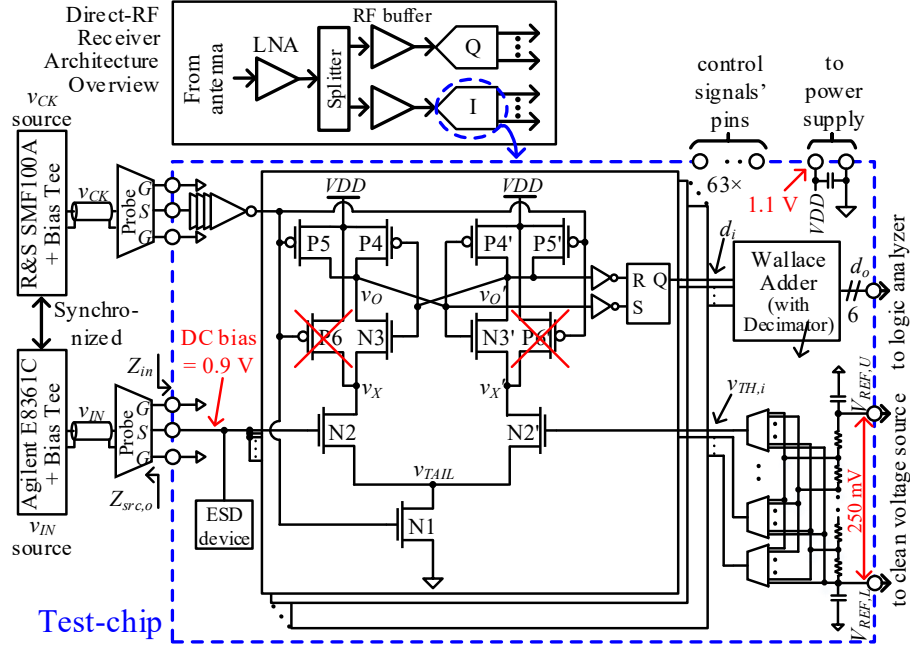


Figure 3-25 A schematic showing the circuitries included in the prototype test chip of the mm-wave UWB radar pulse digitizer design proposed in this work and the test chip's measurement setup

As a note, the StrongARM latches in the prototype digitizer are designed without the reset transistor P6/P6' as shown in Figure 3-25. Because of the electrostatic discharge (ESD) protection device that must be placed at the v_{IN} pin of the test chip, the prototype digitizer's V_{IN} bias level is constrained to a relatively low value. The constraint, which is not present when the digitizer is used as a part of a direct-RF mm-wave UWB pulse radar receiver implementation, is detrimental to the digitizer's sampling bandwidth and linearity (the optimum design point is when the bias level is higher, as discussed in section 3.2.1). Removing P6/P6' improves the latches' sampling bandwidth, allowing us to characterize the prototype digitizer without the need for input signals with too high of amplitude levels. Nonetheless, the prototype still serves the purpose of proving the concept and workings of the novel digitizer, and the prototype digitizer's degraded linearity performance can be anticipated. In section 3.3.4, the measured and simulated THD and SNR performance of the prototype digitizer under the constraint are shown to agree with each other generally.

3.3.1 Area Usage

The prototype digitizer is implemented with a total active area of less than ~ 0.11 mm² in the test chip. Most of this area is occupied by the control logic of the digitizer's bank of DACs, whose area usage will be optimized in our future work. As a note, the DACs bank's area usage is mostly (~ 75 %) due to logic gates implementing binary-to-1-hot decoders, adders, counters, and offset calibration registers.

3.3.2 DC Offsets Measurements

The standard deviation of the DC offset of the StrongARM latch circuit used to implement the input signal comparators in the prototype digitizer was measured to be ~ 32 mV, which is significantly more than that according to our Monte Carlo post-layout simulation results (see section 3.2.1.4). The measured standard deviation is higher, possibly, due to the random parasitic mismatches and layout effects (especially the well-proximity effect [83]) not considered in the simulation. Note that the prototype digitizer is designed with a comparator offset calibration capable of compensating for up to ± 125 mV of the offset. Additionally, the prototype digitizer's measured *DNL/INL/THD* performance presented in section 3.3.3 and 3.3.4 shows that the digitizer is resilient to the large variation in the offsets of its comparators.

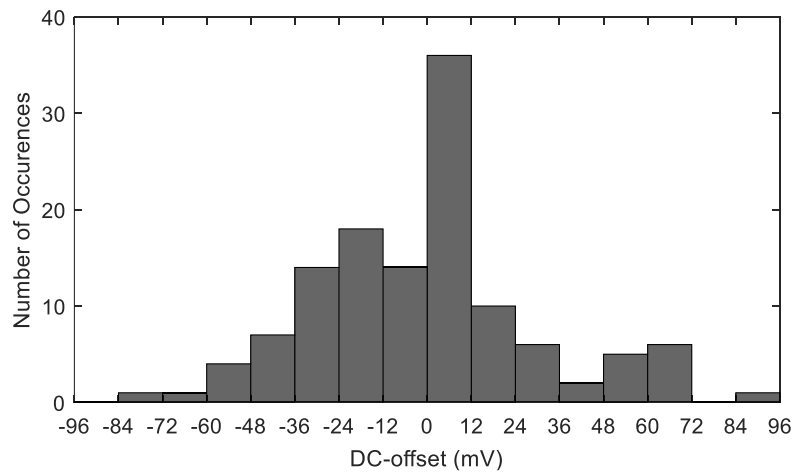


Figure 3-26 The histogram of the measured DC offset of the StrongARM latch circuit used as the input signal comparators in the prototype mm-wave UWB radar pulse digitizer (sample size=126, bin width=12)

3.3.3 DNL/INL Measurements

Figure 3-27 shows the measured *DNL/INL* of the prototype mm-wave UWB radar pulse digitizer. The *DNL/INL* curve is obtained using the histogram method after the sub-ADCs in the digitizer are calibrated to align their input ranges (the calibration procedure is discussed in section 3.1.4.1). In the characterization, the digitizer is clocked at its targeted operating clock frequency of 4 GHz with its DC full-scale input range set to be 250 mV (i.e., with the $V_{REF,U} - V_{REF,L}$ pointed out in Figure 3-25 set to be 250 mV). The stimulus used in the characterization is a low-frequency sinusoid whose frequency is unrelated to the digitizer's clock signal frequency.

The measured *DNL/INL* of the prototype digitizer stays within ± 0.5 LSB for an output code of between 2 and 61. The *DNL/INL* degrades at both the high and low end of the digitizer's output code range due to some input dependence in the offsets of the comparators in the digitizer and because the input ranges of the sub-ADCs in the digitizer cannot align perfectly, as discussed in section 3.1.4.

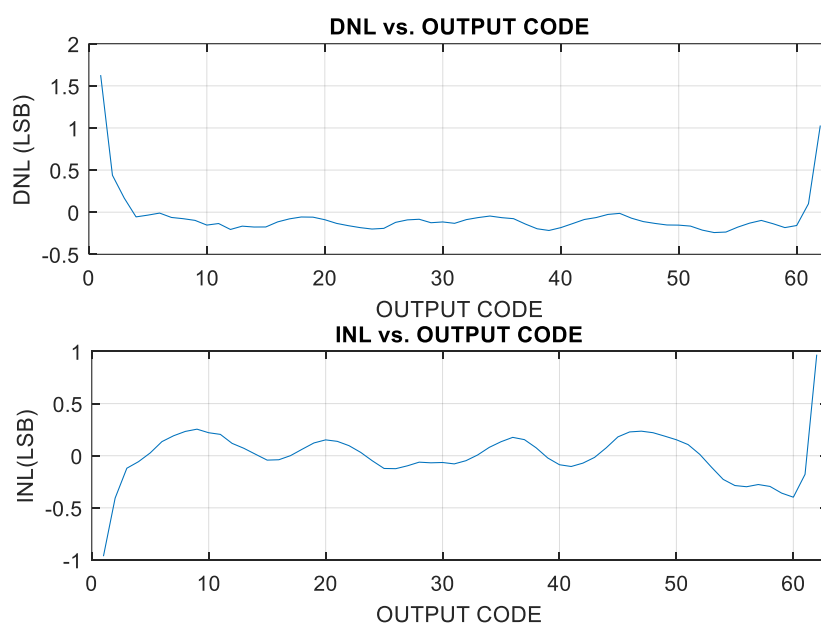


Figure 3-27 The DNL/INL of the prototype mm-wave UWB radar pulse digitizer measured after its sub-ADCs are calibrated to align their input ranges

3.3.4 THD and SNR Measurements

The digitizer design presented here in this work is a special-purpose design that works only with DC and periodic input signals (or signals that are approximately so). In digitizing a periodic signal, the digitizer must ultimately implement equation (3-7).

Here, in producing the spectrums needed to compute the prototype mm-wave UWB radar pulse digitizer's *THD/SNR* values, the digitizer is operated with the *L* value in equation (3-7) set to 512,000 points. However, because of equipment limitations, the data generated by the digitizer must first be decimated (by a factor of 500) before they are sent off-chip. The prototype digitizer, which has a resolution of 6 bits, will thus generate a total of 63 streams of 1,024 data samples for each complete digitization it performs here. In each digitization, the coherence between the digitizer's input and clock signal must be maintained so that the sine waves in the streams always start from the same phase and average together constructively. Here, the coherence does not cause increased output harmonics since the total noise encountered in the digitization is adequate to dither the digitizer's digitization results.

Figure 3-28 shows the spectrum of a ~60 GHz signal as digitized by the prototype mm-wave UWB radar pulse digitizer. Here, equivalent-time sampling causes the signal to appear as a 0.5 MHz waveform at the output of the digitizer. As shown, there are a phase noise skirt and some spurs present around the fundamental tone in the spectrum. They originate mainly from the Agilent E8361C used to generate the ~60 GHz signal. The phase noise and spurs must be de-embedded from the spectrum since it can significantly corrupt the digitizer's *SNR* characterization results. The de-embedding procedure will be discussed in detail in section 3.3.4.1.

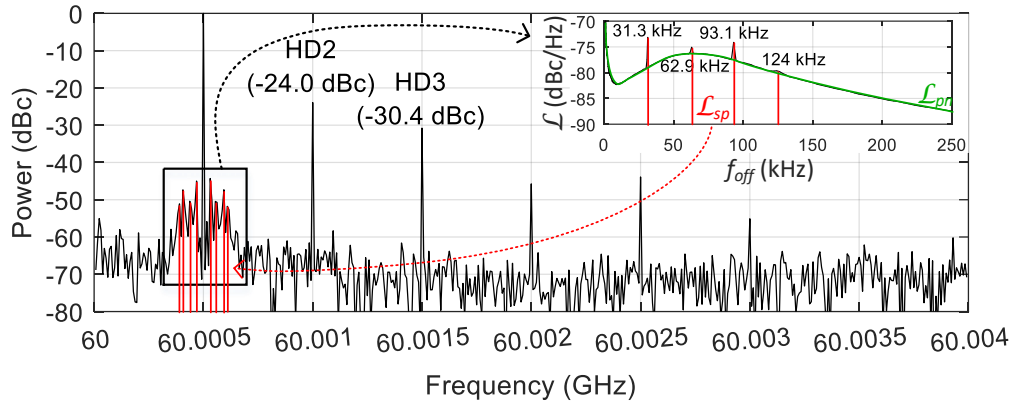


Figure 3-28 The spectrum of a -1.7 dBFS 60.0005 GHz signal as digitized by the prototype mm-wave UWB digitizer; the inset shows the spectral density of phase fluctuation of the signal as captured by a signal source analyzer, $\mathcal{L}(f_{\text{off}})$; the spurs in the signal, $\mathcal{L}_{\text{sp}}(f_{\text{off}})$, are more apparent in the digitizer's output spectrum due to the averaging done by the digitizer

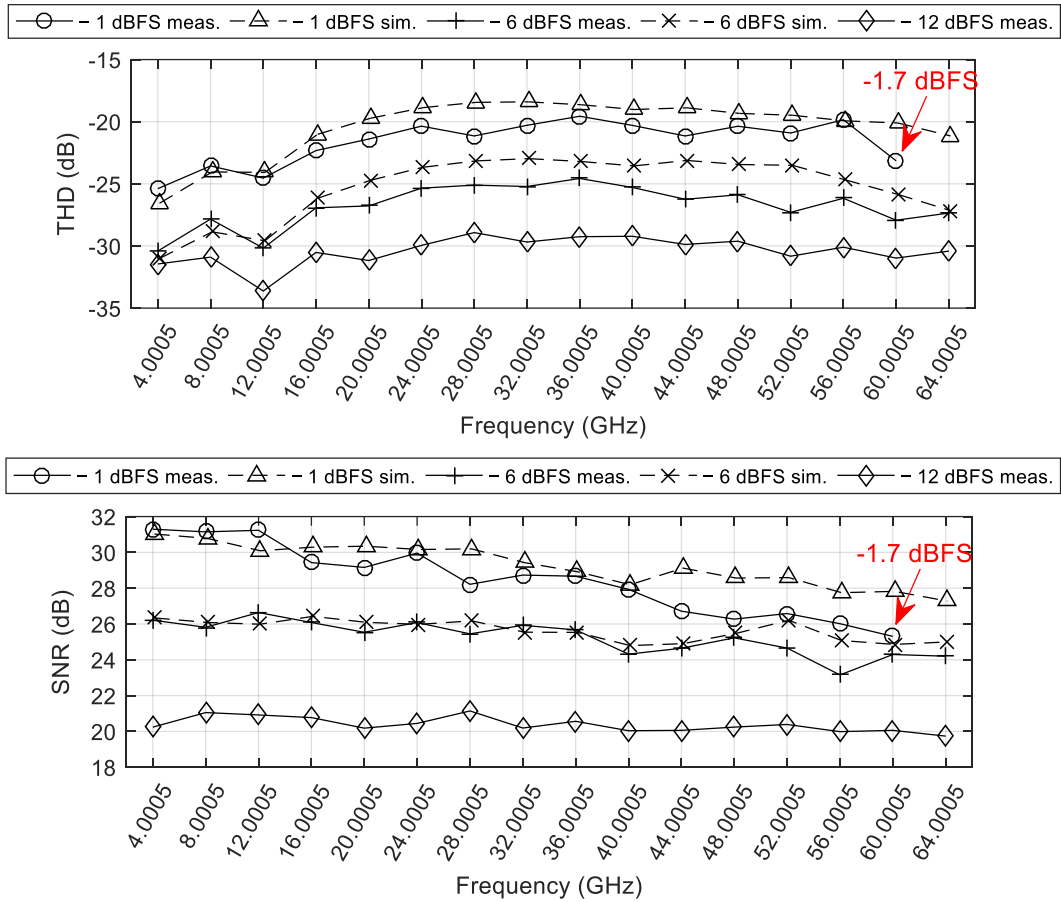


Figure 3-29 The prototype mm-wave UWB digitizer's measured (meas.) and simulated (sim.) THD and normalized SNR values (normalized to the case where there is no averaging) at output amplitudes (A_{out}) of -1 , -6 , and -12 dBFS between 4 GHz $- 64$ GHz; due to equipment limitations, the -1 dBFS 64.0005 GHz data is unavailable, and the 60.0005 GHz data is for an A_{out} of only up to -1.7 dBFS

Figure 3-29 shows the THD/SNR of the prototype mm-wave UWB radar pulse digitizer, measured at output amplitudes (A_{out}) of -1, -6, and -12 dBFS and input frequencies (f_{in}) of between 4 GHz and 64 GHz every 4 GHz with +0.5 MHz offset after the de-embedding. From the discussions presented in section 3.1.3, it can be understood that the 6-bit digitizer can only be operated with an averaging factor of 63× or its multiple. The SNR values given in Figure 3-29 are normalized to the case where there is no averaging so that they can be directly compared to those of conventional ADC designs.

Figure 3-29 also facilitates comparisons between the prototype digitizer's measured THD/SNR values and their simulated counterparts. From Figure 3-29, it can be observed that the digitizer's simulated THD values are generally worse (by ~1 to ~3 dB) than their measured counterparts. Nonetheless, the values follow the same general trend. It can also be observed from Figure 3-29 that the digitizer's measured SNR values also generally agree with their simulated counterparts. As a note, the digitizer's output data streams are not decimated, and the digitizer's comparators have no DC offsets in the simulations.

One interesting trend to note in Figure 3-29 is that the prototype digitizer's SNR degrades as f_{in} is raised, and the degradation becomes more evident when A_{out} is higher. We presume that this trend is due to the digitizer's sampling aperture jitter. Note that the simulated SNR values of the digitizer are generally better than their measured counterparts. The clock signal source used in the measurements has an RMS jitter of >80 fs, whereas the clock signal source used in the simulations is jitter-less. According to equation (3-39), the >80 fs jitter together with the jitter of the digitizer's v_{CK} distribution network limits the digitizer's normalized SNR (normalized to the case where there is no averaging) to below ~29.5 dB at 60 GHz.

As a note, two of the input signal comparators of the prototype digitizer in the test chip have very large positive DC offsets (almost +100 mV). As pointed out in section 3.2.1.6.2, the sampling bandwidths of the two corresponding sub-ADCs in the digitizer will thus be substantially wider than those of the other sub-ADCs in the digitizer. In our measurements, we let these sub-ADCs saturate when the amplitude of the prototype digitizer's input signal stimulus is large during the digitizer's -1 dBFS *THD/SNR* characterization. As also noted in section 3.2.1.6.2, doing so should not cause an appreciable degradation in the digitizer's linearity performance since the distortions contributed by these sub-ADCs are divided by the total number of sub-ADCs that the digitizer has. As shown in Figure 3-29, the prototype digitizer's measured -1 dBFS *THD* values are not worse than their simulated counterparts even though the comparators in the digitizer have no DC offsets in the simulations.

3.3.4.1 De-embedding v_{IN} 's phase noise and spur

The v_{IN} 's phase noise and spurs de-embedding process proceeds as follows:

- 1) First, a signal source analyzer is used to capture the spurs, $\mathcal{L}_{sp}(f_{off})$, and phase noise, $\mathcal{L}_{pn}(f_{off})$, of the prototype digitizer's input signal stimulus, v_{IN} . As a note, if $\mathcal{L}(f_{off})$ is the overall spectral density of phase fluctuations of v_{IN} as captured by the signal source analyzer (see Figure 3-28):

$$\mathcal{L}(f_{off}) = \mathcal{L}_{sp}(f_{off}) + \mathcal{L}_{pn}(f_{off}) \quad (3-40)$$

- 2) The offset frequencies of the spurs, $f_{off,x} = \{f_{off,1}, f_{off,2}, \dots, f_{off,X}\}$, are then noted, and v_{IN} 's *SNR* without its spurs, $SNR_{IN,no-sp}$, is then computed from the $\mathcal{L}_{pn}(f_{off})$ curve obtained in step 1 as follows:

$$SNR_{IN,no-sp} = 10 \cdot \log \left(\left(2 \cdot \int_{f_{off,a}}^{f_{off,b}} 10^{\frac{\mathcal{L}_{pn}(f_{off})}{10}} df_{off} \right)^{-1} \right) \quad (3-41)$$

in which X is the number of spurs in v_{IN} that can be identified from the $\mathcal{L}(f_{off})$ curve obtained in step 1 and the $\mathcal{L}_{pn}(f_{off})$ in equation (3-41) is in dBc/Hz. In evaluating equation (3-41), $f_{off,a}$ is chosen to be 3.90625 kHz here since the fundamental tone in the prototype digitizer's output waveform spectrum of the v_{IN} spans a 2×3.90625 kHz bin in the spectrum. $f_{off,b}$, meanwhile, is some arbitrarily chosen but practical f_{off} value ($f_{off,b}$ is chosen to be 500 kHz here—the lower this value is, the less the de-embedding strength will be).

- 3) If $S(f_l = l \cdot \Delta f)$ is the single-sided amplitude spectrum of v_{IN} as digitized by the prototype digitizer, f_{in} is the frequency of the fundamental tone of v_{IN} in $S(f_l)$, and $l = \{0, 1, \dots, L/2\}$ (L here is the same L defined in section 3.1.3), v_{IN} 's spurs in $S(f_l)$ should thus fall within the frequency bins, $f_{l_{\pm x}} = \{f_{l-x}, f_{l-x+1}, \dots, f_{l-1}, f_{l+1}, \dots, f_{l+x-1}, f_{l+x}\}$, whose frequency ranges, $[(l_{\pm x}-0.5) \cdot \Delta f, (l_{\pm x}+0.5) \cdot \Delta f]$, contain the frequencies $f_{in} \pm f_{off,x}$. For each of v_{IN} 's spurs that can be identified from $\mathcal{L}(f_{off})$, the spur is removed from $S(f_l)$ by replacing the amplitude value of the frequency bin that contains the spur, $S(f_{l_{\pm x}})$, with the root mean square amplitude value of the two frequency bins immediately adjacent to $f_{l_{\pm x}}$:

$$S(f_{l_{\pm x}}) = \sqrt{(S(f_{l_{\pm x}-1})^2 + S(f_{l_{\pm x}+1})^2)/2} \quad (3-42)$$

After v_{IN} 's spurs in $S(f_l)$ are removed, $S(f_l)$'s SNR without the spurs, $SNR_{OP,no-sp}$, can then be computed.

- 4) After completing step 3, the following formula can be used to compute the SNR of the digitizer's output waveform with v_{IN} 's spurs and phase noise de-embedded from the digitization result:

$$SNR_{dig} = SNR_{IN,no-sp} \cdot SNR_{OP,no-sp} / (SNR_{IN,no-sp} - SNR_{OP,no-sp}) \quad (3-43)$$

SNR_{dig} , $SNR_{IN,no-sp}$, and $SNR_{OP,no-sp}$ are in all linear scales here.

It can be noted from equation (3-41) that v_{IN} 's amplitude noise is not considered in the de-embedding procedure described here. This omission is not an issue since it, in fact, helps us prevent the de-embedding from being overdone.

Lastly, it can also be noted that the de-embedding will cause the uncertainties in the SNR values reported here to increase. Nonetheless, the increase in the uncertainties is acceptable since the prototype digitizer's reported SNR values after the de-embedding still show a clear trend across f_{in} instead of being highly random across f_{in} , as shown in Figure 3-29.

3.3.5 Input Attenuation, Input-Referred Noise, and Input Impedance

From our measurements, we deduce that the prototype mm-wave UWB radar pulse digitizer's input attenuation, $1/|H_s(j\omega_{in})|$, is less than ~ 13.5 dB at 60 GHz. Note that 13.5 dB is the upper bound of our estimate of the attenuation. In our measurements, part of the loss measured is due to a voltage division that occurs between the digitizer test chip's v_{IN} pin impedance, Z_{in} , and the output impedance of the input signal source used in the measurements as seen from the digitizer's side, $Z_{src,o}$, which ideally is equal to 50 Ω (see Figure 3-25). However, Z_{in} 's effective value at a mm-wave frequency cannot be measured using the available equipment since Z_{in} 's value is time-varying in nature. The prototype digitizer's input attenuation is approximated via simulations to be about 9 dB at 60 GHz.

With a 60 GHz input attenuation of about 9 dB and a DC full-scale input range of 250 mV, the prototype digitizer's full-scale input range at 60 GHz calculates to be about 700 mV. Since the prototype digitizer's 60 GHz SNR at an A_{out} of -12 dBFS is approximately equal to 20 dB (see Figure 3-29), the prototype digitizer's input-referred noise at 60 GHz thus calculates to be around -31.1 dBm. The above calculations are illustrated in Figure 3-30.

According to our simulations, the prototype digitizer's input impedance at 60 GHz is equivalent to a parallel R-C circuit whose capacitance and resistance values vary across the digitizer's sampling phase as shown in Figure 3-31. In designing the digitizer's mm-wave RF buffer-driver for 60 GHz operation, this impedance can, according to our simulations, effectively be replaced by a 120 fF capacitor in parallel with a 360 Ω resistor without altering the center frequency and the peak magnitude value of the digitizer and the buffer's combined transfer function. As a note, the capacitance and resistance values also vary across frequencies, and a more complicated model is needed to model the impedance across frequencies.

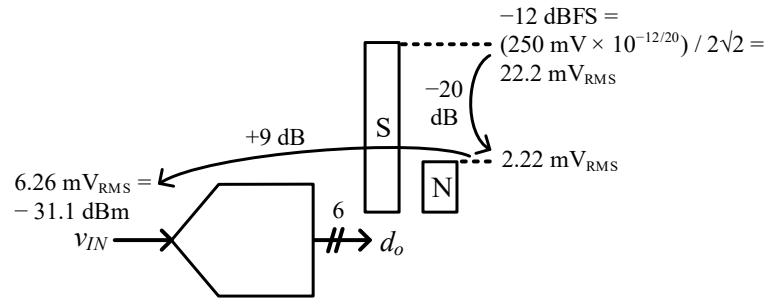


Figure 3-30 Input-referred noise calculation for the prototype mm-wave UWB digitizer

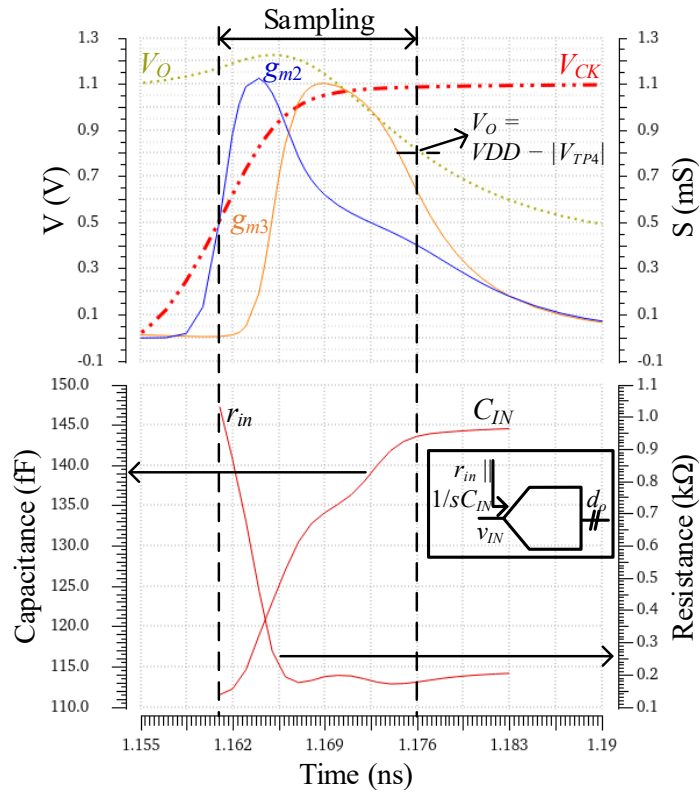


Figure 3-31 The simulated time-varying input impedance of the prototype digitizer

3.3.6 Power Consumption and Driving Requirement

The prototype mm-wave UWB radar pulse digitizer consumes a total of 19.7 mW of power when operated with a sampling rate of 4 GSa/s, 11.8 mW, 6.9 mW, and <1 mW of which is consumed in the digitizer's comparators (and its clock distribution network), adder, and staircase threshold voltages generator, respectively. Note that the staircase threshold voltages generator in the digitizer does not consume much power since the circuit operates at a low frequency (i.e., $4 \text{ GHz} / 1024 = \sim 3.9 \text{ MHz}$).

In its targeted end-use, the digitizer will be used with a mm-wave RF buffer as its driver (as discussed in section 3.2.1). To gain insight on how much power must the driver circuit consume so that it can be designed with a gain that exceeds the digitizer's attenuation at 60 GHz, we designed and simulated a simple cascode amplifier circuit with its output matching network tuned to resonate with the digitizer's effective input impedance at a frequency that is slightly above 60 GHz, as shown in Figure 3-32 below. The amplifier circuit is designed with a current consumption of $\sim 6 \text{ mA}$, and the total gate width of each transistor in the amplifier is $32 \mu\text{m}$. Note that the gate finger width of these transistors is relatively wide ($2 \mu\text{m}$) since the amplifier's noise performance does not need to be optimized.

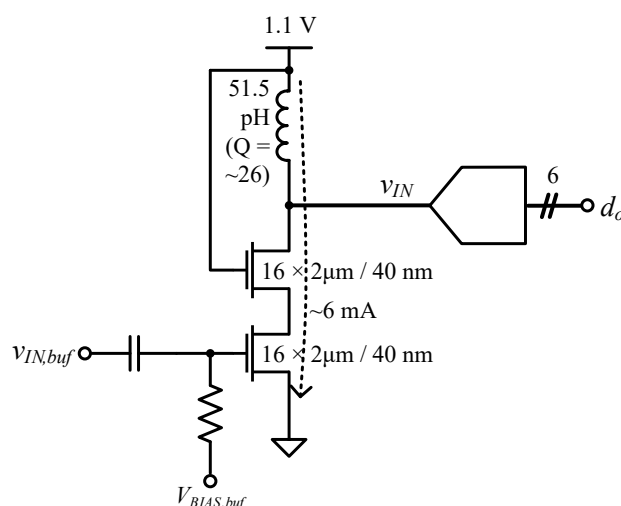


Figure 3-32 The schematic of a simple cascode amplifier circuit with a tuned output network driving the proposed mm-wave UWB radar pulse digitizer

According to our simulations, the combined -3 dB bandwidth of the amplifier/buffer and the digitizer circuit is ~ 7 GHz. The bandwidth is sufficient for a UWB pulse radar receiver implementation whose radar range resolution is in the cm level if the bandwidths of the other amplification stages in the receiver are much wider than 7 GHz, which is achievable if a gain-bandwidth enhancement technique is used in their designs [84]. In that case, the receiver's overall bandwidth will mainly be determined by the combined bandwidth of the digitizer and amplifier/buffer. As a note, if the center frequency of the combined transfer function of the digitizer and buffer can vary across process corners, the center frequency can be made tunable [85].

The simulated gain of the 6.6 mW amplifier circuit given in Figure 3-32 as it drives the digitizer is ~ 10 dB at ~ 61 GHz, which is enough to compensate for the digitizer's ~ 9 dB loss at 60 GHz. Note that the amplifier is designed with its output matching network tuned to resonate at slightly above 60 GHz here to compensate for the digitizer's transfer function's slope at around 60 GHz. Also, as pointed out at the beginning of section 3.3, the digitizer's V_{IN} bias level can be set higher when it is driven by an on-chip circuit. Thus, in the configuration shown in Figure 3-32, the digitizer's 60 GHz attenuation can be made lower than the ~ 9 dB quoted in section 3.3.5.

The simulated input-referred -1 dB compression point and input-referred 3rd order intercept point of the amplifier circuit given in Figure 3-32 at 60 GHz are around -1 dBm and 4 dBm, respectively. Also, according to our simulations, if the amplifier's output must swing across the digitizer's ~ 1 dBm full-scale input range at 60 GHz, the amplifier's 3rd order output distortion level will approximately be equal to -21 dBm. If a better linearity performance is required, a differential amplifier stage (followed by a balun) can instead be used to drive the digitizer [84].

Lastly, the output referred noise of the cascode amplifier circuit given in Figure 3-32 simulates to be less than 0.6 mV_{RMS}, which is significantly lower than the prototype digitizer's input-referred noise level (i.e., ~6 mV_{RMS}).

3.3.7 UWB Pulse Digitization Example

Figure 3-33 shows the waveform of a pulse signal as digitized by the prototype mm-wave UWB radar pulse digitizer. The pulse signal is a raised cosine pulse signal generated using Keysight M8196A. The pulse signal's full-width-at-half-maximum, pulse repetition frequency (*PRF*), and carrier frequency are equal to 100 ps, 88 GHz / (1152×4), and 25 GHz (<30 GHz due to equipment limitation), respectively. In digitizing the signal, the digitizer is configured to operate with an equivalent sampling timing resolution, $\Delta t_{s,eff}$, of ~45.45 ps using coherent ETS [56] with an *L* value (*L* is the number of points in a period of the periodic input signal the digitizer is digitizing as defined in section 3.1.3) that is equal to 1,152 points. As a note, the carrier frequency of the raised cosine pulse signal used as the digitizer's input signal here is offset from the exact integer multiple of the digitizer's clock frequency by +1 GHz since our setup can only operate one instance of the prototype digitizer at a time. The frequency offset prevents a repeated sampling at around the null points of the pulse signal's carrier from occurring. Figure 3-33 basically demonstrates that the prototype UWB radar pulse digitizer can faithfully digitize a high-frequency pulse signal.

3.3.8 Recap

Table 3-4 provides a summary of the prototype mm-wave UWB radar pulse digitizer's implementation results which have been presented in this section.

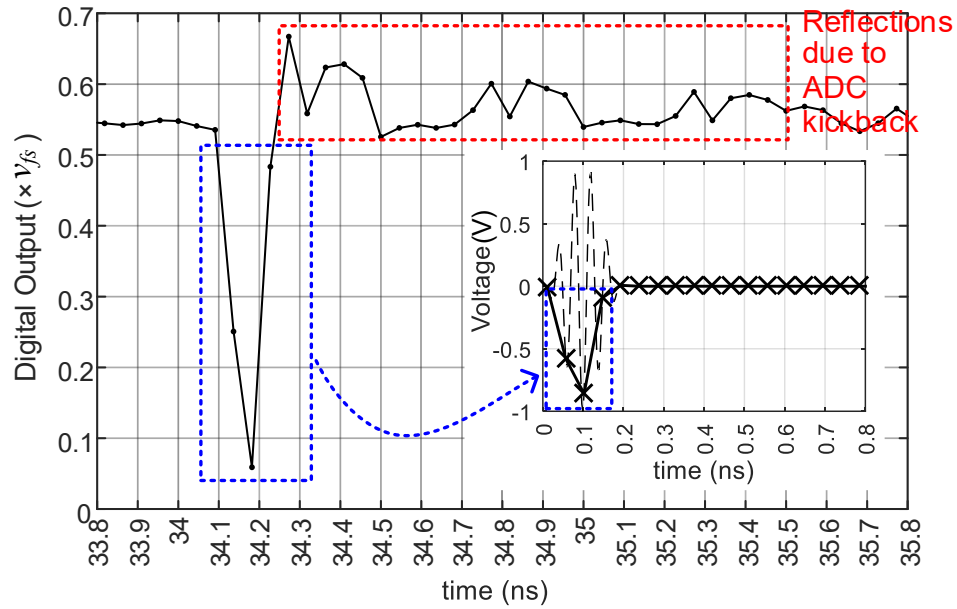


Figure 3-33 The waveform of a 100 ps 25 GHz raised cosine pulse signal as digitized by the prototype mm-wave UWB radar pulse digitizer with an inset showing the “ideal” digitization results

Table 3-4 Summary of the implementation results of the prototype mm-wave UWB radar pulse digitizer

Fabrication Technology	40 nm LP bulk CMOS
Supply	1.1 V
f_s	4 GSa/s
Resolution	6 bits
Area Usage	~0.11 mm ²
Full-Scale Input Range	250 mV @ DC ~700 mV @ 60 GHz
Comparator Offsets Calibration Range/Resolution	±125 mV/3.90625 mV (DC)
DNL/INL	within ±0.5 LSB (between output code 2 and 61)
THD	< around -20 dB @ -1dBFS, between 4 and 64 GHz < around -25 dB @ -6dBFS, between 4 and 64 GHz
SNR	around 20 dB @ -12 dBFS, between 4 and 64 GHz
Attenuation	~9 dB @ 60 GHz
Effective Input Impedance	can be approximated as 120 fF 360 Ω
Power Consumption	19.7 mW

3.4 Conclusions

In this work, a mm-wave UWB radar pulse digitizer is designed and implemented based on a novel flash-ADC-like equivalent-time sampling ADC architecture whose working principle is based on the multi-pass analog-to-digital conversion concept [53]. The novel ADC architecture allows the digitizer to be implemented in a bulk CMOS technology with an acceptable level of attenuation, low power consumption, and low driving requirement. These are due to the novel architecture's non-stringent comparator offsets calibration accuracy requirement.

Table 3-5 compares the proposed mm-wave UWB radar pulse digitizer to prior-art ADCs whose maximum input signal frequencies are ≥ 10 GHz. The proposed digitizer is the only design operating with an input signal frequency of up to 64 GHz. The digitizer achieves this while maintaining an effective number of bits (*ENOB*) of > 3.2 bits and a modest figure of merit without it needing to be fabricated in a much more advanced CMOS technology node. Additionally, the digitizer has also been shown to faithfully capture a 100 ps 25 GHz UWB pulse signal here (the signal's carrier frequency is not higher due to equipment limitations). Lastly, according to our simulations, the 60 GHz RF buffer that is to drive the digitizer in a 60 GHz direct-RF receiver implementation can be designed with less than 10 mW of power consumption. We conclude that the 4 GSa/s digitizer is suitable for use in the design of a direct-RF UWB pulse radar receiver, allowing for the implementation of a power-cycled mm-wave UWB pulse doppler radar IC with low power consumption.

Table 3-5 Comparisons with prior-art ADCs whose maximum f_{in} are ≥ 10 GHz

	This Work	JSSC '14 [62]	JSSC '14 [73]	ISSCC '17 [86]	VLSI '18 [50]	ISSCC '18 [49]	JSSC '19[64]	JSSC '20 [87]	TCAS-II '20 [88]	JSSC '20 [89]
CMOS Tech. LP	40 nm	65 nm	SOI 32 nm	20 nm	14 nm	14 nm	28 nm	7 nm	40 nm	16 nm
Supply (V)	1.1	1.2 / 1.1	0.9	-	0.8 / 0.95	0.8 / 0.9	-0.9 / 0.95	0.9 / 0.75	0.95	1.8 / 1
f_s (GS/s)	4	12.8	20	64	32	72	56	28	32	18
Max. f_{in} (GHz)	64	25	10	19	40	40	27.1	13.5	13	10
Resolution	6 bits	6 bits	6 bits	8 bits	10 bits	8 bits	8 bits	7 bits	7 bits	12 bits
$SNDR$ @ f_{in} (dB @ GHz)	-1.7dBFS: 21.1 @ 60 -6dBFS: 22.8 @ 60	26.4 @ 25	30.7 @ 10	32.5 @ 19	37.8 @ 39.8	30.4 @ 36.1	33 @ 27.1	32 @ 13.5	24 @ 13	47 @ 10
Power (mW)	19.7	162	69.5	950 [^]	199	235	702	77.9*	125	1300
FoM @ f_{in} (fJ/c-s @ GHz)	-1.7dBFS: 532 @ 60 -6dBFS: 434 @ 60	742 @ 25	124 @ 10	431 [^] @ 19	98 @ 39.8	121 @ 36.1	344 @ 27.1	85.4* @ 13.5	302 @ 13	395 @ 10
Input signal requirement	Periodic/ approxim- ately periodic	General Purpose								

[^] Includes the power consumption of an analog front-end circuitry and a reference generator

* Includes the power consumption of an analog front-end circuitry

Chapter 4

Future Work – A Proposed V-Band Pulse-Doppler Radar Transceiver Using Direct-RF Radar Pulse Digitizer

This chapter discusses the design of a 60 GHz UWB pulse-Doppler radar transceiver whose receiver is implemented using the direct-RF mm-wave UWB radar pulse digitizer circuit whose design is presented in chapter 3 in this work. It must be noted that, in this work, the full implementation of the radar transceiver is a future work. Nevertheless, the discussions presented in this chapter are instrumental for explaining how the mm-wave direct-RF digitizer proposed in this work is to be used in its targeted application and how the digitizer's design meets the specifications that are required of it when it is used to implement a direct-RF receiver in such an application.

4.1 Equivalent-Time Sampling and Power Cycling

Some radars are interested only in objects that move very slowly relative to the radars' pulse repetition frequency (*PRF*). These radars typically utilize equivalent-time sampling (ETS) to reduce the sampling rate (f_s) requirements of their digitizers [2, 4, 6, 7, 11, 29]. Figure 4-1 illustrates the waveform of the input signal of an ETS pulse radar in which a very slow-moving object reflects the radio pulses transmitted by the radar (TX pulses). Since the radar's target object is roughly stationary, the time-of-flight (*TOF*) of the pulses roughly stays the same. Consequently, the radar's input signal waveform is also roughly periodic.

In ETS, a period of a periodic signal is reconstructed from a digitization that spans a number of the signal's periods, as illustrated in Figure 4-1. In Figure 4-1, the

sampling positions (t_l) of an ETS radar system are arranged across a number of the radar's periodic input signal's periods in such a way that t_l correspond to the radar's range bins (R_l). Here, $l = \{1, 2, \dots, L\}$ and L is the number of range bins that the radar has. Without ETS, $1/f_s$ must be $\leq \tau$ so that the radar does not miss any pulses it must detect (i.e., the RX pulses in Figure 4-1) in which τ is the width of the said pulses [51]. With ETS, the radar's range bins width (R_o) is equal to the radar's effective sampling timing resolution ($\Delta t_{s,eff}$) instead of $1/f_s$, as illustrated in Figure 4-1.

Figure 4-1 illustrates the case in which an ETS pulse radar takes only 1 sample in each pulse repetition interval ($PRI=1/PRF$). However, this is not necessarily so in practice. The time required for an ETS pulse radar to complete an acquisition (T_{acq}) can be calculated as follows:

$$T_{acq} = N \times PRI \times L/M \quad (4-1)$$

in which M is the number of samples that the radar takes in each PRI and N is the radar's averaging factor (in pulse radar, RX pulses from successive TX pulses that fall on the same range bin are usually averaged together; the improvement in the radar's SNR is equal to N in linear scale if the averaging is coherent and ideal [51]). A larger M shortens T_{acq} and allows for a power-cycled radar [1, 10, 29] to be in its off-state longer, reducing its power consumption.

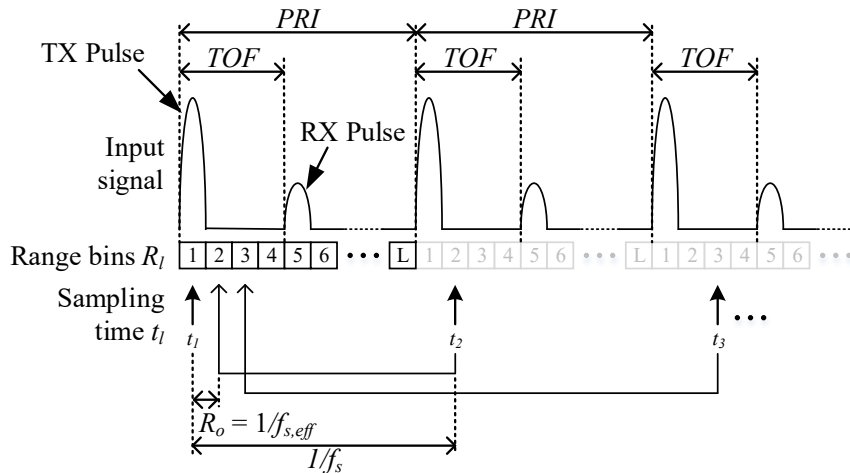


Figure 4-1 Equivalent-time sampling as utilized in a pulse radar system

4.2 Assumptions on the Radar Target Signal

The objects that are of interest to the radar system whose design is being discussed here (i.e., the target objects) are assumed to have the characteristics of either type I or type III Swerling targets [32]. That is, these objects are assumed to be capable of moving only slowly in such a way that their radar cross sections (RCS) do not fluctuate significantly across the duration of the radar system's acquisition time. A human is an example of such a target object. According to [90], for a radar system that operates with a radar signal whose frequency range is >2 GHz, a person's RCS conforms reasonably well to the type I Swerling model.

Given a pulse radar system whose PRI is equal to ~ 14 ns (which gives the radar a maximum unambiguous range of ~ 2.1 m), a human target, which can be expected to move with a speed of <2 m/s indoor, will have moved by only $<\sim 7$ μm across the duration of the radar's acquisition time if the number of radio pulses that the radar must transmit for it to complete an acquisition is equal to 252 pulses. The $<\sim 7$ μm movement translates to a difference of only <47 fs between the TOF of the first and last radio pulse that the radar transmits in an acquisition. As a note, the number 252 here corresponds to the case in which the radar system's N value and L/M value (as defined in section 4.1) are equal to 63 and 4, respectively. N here is equal to 63 since the radar pulse digitizer proposed in this work must operate with an averaging factor of $2^B - 1$ or its multiple (in which B is the resolution of the digitizer, which is equal to 6 bits in this work, see chapter 3 for more information). Whereas L/M is equal to 4 here is related to the choice of the sampling rate, PRI , and range resolution in the radar system's design (see section 4.3).

At 60 GHz, the <47 fs differences in the *TOFs* of the radio pulses transmitted by the radar system in an acquisition correspond to $<\sim 1^\circ$ differences in the carrier signal phases of the received radar echo pulses at the time of their sampling in the said acquisition. A coherent integration, hence, can be done without a significant integration loss here.

Lastly, considering the working principle of the radar pulse digitizer proposed in this work (which is based on the concept of multi-pass analog-to-digital conversion, see section 3.1.3), we believe that the afore-discussed progressive change in the received radar echo pulses' carrier signal phases relative to the pulses' sampling time will also not disrupt the digitizer's operation. This is especially true if a sufficient amount of noise has already dithered the echo pulses by the time the pulses reach the digitizer's input port. Basically, if a sinusoidal wave signal whose peak-to-peak amplitude spans the full-scale input range of the digitizer is input into the digitizer, a $\sim 1^\circ$ shift in the signal's phase corresponds to a ~ 1.1 LSB change in the digitizer's output waveform at the steepest portions of the waveform. Meanwhile, in the targeted end-use of the digitizer, the noise level present at the input of the digitizer is expected to be >1 LSB RMS, enough to dither the aforesaid gradual carrier signal phase shift.

An example of a prior-art pulse radar design that also has the issue described above is the pulse radar IC developed by Novelda AS [2]. The receiver in the pulse radar IC implements what [2] calls swept-threshold sampling. Like in the novel ADC architecture proposed in this work, in swept-threshold sampling, the input signal is compared to only one threshold value at a time.

4.3 Transceiver Architecture and Design Considerations

This section discusses how a mm-wave UWB pulse-Doppler radar transceiver can be designed with a direct-RF receiver using the direct-RF mm-wave UWB radar pulse digitizer circuit presented in chapter 3 of this work. Figure 4-2 shows an example of how such a pulse radar transceiver can be implemented. As shown in Figure 4-2, the receiver in the transceiver does not employ an explicit down-conversion block. Instead, down-conversion is carried out only at the end of the receive signal chain in the transceiver, together with a digitization using the principle of under-sampling.

The discussions presented in this section also aim to demonstrate how an ETS pulse-Doppler radar can be implemented so that it can be power-cycled with a low duty-cycle ratio. Pulse radar systems that achieve this operate with a large M value (M here is the M defined in section 4.1).

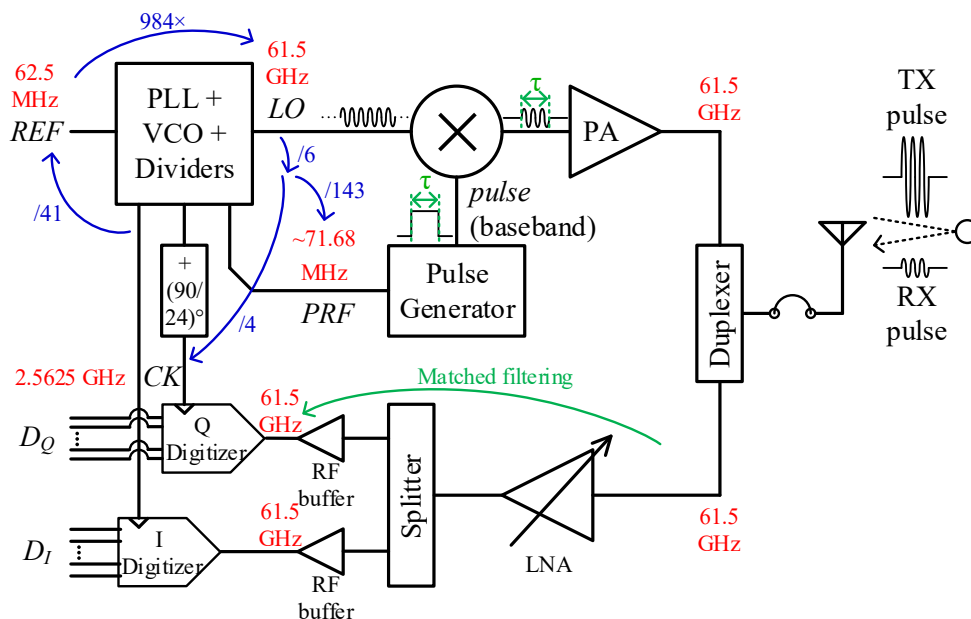


Figure 4-2 A possible mm-wave UWB pulse-Doppler radar transceiver implementation utilizing the proposed mm-wave UWB radar pulse digitizer

To show that such a pulse radar design can be implemented with a simple frequency arrangement, we deliberately avoid using a fractional-N phase-locked loop (PLL) circuit in the transceiver's design. As indicated in Figure 4-2, the transceiver requires only some integer frequency multiplications/divisions to generate the frequencies required for the transceiver's internal operations.

As a note, the carrier frequency of the radio pulses produced by the transceiver is chosen to be equal to 61.5 GHz here so that the spectrum of the pulse signal sits at the middle of the frequency range 57-66 GHz.

4.3.1 Link Budget Analysis

Table 4-1 presents a link budget analysis for the 61.5 GHz pulse-Doppler radar transceiver design whose block diagram is illustrated by Figure 4-2. The analysis assumes that the transceiver's end-use is for the implementation of a radar system whose uses are for monitoring human targets located at distances of less than 3 m from the radar system. The analysis also assumes that the width of the radio pulses that the transceiver produces, τ , is equal to 220 ps, giving the radar system a range resolution of <3.5 cm. Consequently, the spectrum of the radio pulse signal that the transceiver produces occupies the V-band between 57-66 GHz, and the signal paths in the transceiver need to be designed with a -3 dB bandwidth (BW_{-3dB}) of about $0.89/\tau = 4$ GHz or more. Lastly, the link budget analysis assumes that the antenna whose design is reported in [91] is employed as the antenna of the radar system. The antenna has an impedance bandwidth of >9 GHz and a compact dimension of <2 cm $\times$ 2 cm $\times$ 0.2 cm. Hence, the antenna is suitable for realizing the radar system as a compact portable radar for short-range ranging, detection, and monitoring applications with a cm-level accuracy requirement.

The link budget analysis expects some implementation losses (i.e., the L_M in Table 4-1) on top of the losses already present in the transceiver design. These are losses that are caused by the additional routings needed to fully implement a radar system using the transceiver (e.g., the routing between the transceiver and its antenna), the SNR degradation that may happen during the radar system's usage (e.g., due to the presence of in-band interferences), and unexpected losses that are not accounted for during the design of the transceiver. In the link budget analysis, we assign 6 dB as the total amount of these losses, 3 dB of which to account for the losses that may occur in the radar system's transmit (TX) signal path, and another 3 dB for the losses that may occur in the radar system's receive (RX) signal path. The larger these numbers are, the more conservative the radar transceiver design will be.

Table 4-1 Link budget analysis for the radar transceiver design given in Figure 4-2 assuming that design employs the digitizer circuit reported in chapter 3 of this work

Signal	
P_{TX} , peak TX output power	: 6 dBm
L_M , implementation loss	: -6 dB
G_{ANT} , antenna gain [91]	: 15.5 dBi
L_P , round trip path loss (at 3 meter)	: -98 dB
RCS , radar cross section (for a human as the target object) [34, 35, 92]	: -10 dBsm
$P_{RX} = P_{TX} + L_M + 2 \cdot G_{ANT} + L_P + RCS$, peak signal power at RX input	= -77 dBm
G_{LNA} , RX LNA gain	: 29 dB
L_{SPLIT} , attenuation due to RX power splitting to 2 digitizers	: -4 dB
G_{BUF} , digitizers' RF buffer-drivers gain (see section 4.3.3)	: 20 dB
$P_{DIG} = P_{RX} + G_{LNA} + L_{SPLIT} + G_{BUF}$, peak signal power at digitizers' inputs	= -32 dBm
Noise	
NF_{RX} , RX noise figure	: 6 dB
$BW_{-3dB, RX}$, RX -3dB bandwidth	: 4 GHz
$N_{RX} = -174 \text{ dBm/Hz} + NF_{RX} + 10 \times \log(\pi/2 \times BW_{-3dB, RX}) + G_{LNA} + L_{SPLIT} + G_{BUF}$, RX noise power at digitizers' inputs	= -25 dBm
N_{DIG} , digitizer's input-referred noise power (quoted from section 3.3.5)	: -31 dBm
N_{tot} , total noise power at digitizers' inputs	= -24 dBm
SNR	
$SNR_{pre-avg} = P_{DIG} - N_{tot}$, SNR before averaging	= -8 dB
G_{avg} , SNR gain due to averaging (63× averaging)	: 18 dB
$SNR_{post-avg} = SNR_{pre-avg} + G_{avg}$, SNR after averaging	= 10 dB

As a note, as indicated in Table 4-1, if the object reflecting the radio pulses transmitted by the transceiver is a person located 3 m away from the transceiver, the peak power of the echo pulses received by the transceiver calculates to -32 dBm at the inputs of the digitizers in the transceiver. With a full-scale range/resolution of 700 mV / 6 bits (see section 3.3), the peak-to-peak amplitude of the pulses is worth only ~ 1.45 LSB at the digitizers' inputs. 1.45 LSB is enough for the transceiver since the noise of the receiver circuitries in the transceiver will dither the pulses and since the receive signal processing in the transceiver employs averaging [93, 94]. As a note, with 6 bits, the digitizer allows the radar target's distance to vary by >2 range octaves without a gain adjustment in the receive signal path in the transceiver.

4.3.2 Transmit Signal Path

[19] presents the design of a radar transmitter capable of transmitting 60 GHz radio pulses with a very narrow pulse width (>25 ps). The design is done and fabricated in a 45 -nm silicon-on-insulator (SOI) CMOS process, and the width of the radio pulses produced by the transmitter is adjustable. The peak power of the radio pulses that the transmitter can transmit is >10 dBm when the pulses' width is >45 ps. The total power consumption of the transmitter circuit is equal to 0.46 W, excluding the power consumption of the frequency tripler circuit included in the design.

The width of the radio pulses considered for the pulse radar transceiver design being discussed here is not as narrow, i.e., at 220 ps. Therefore, a "scaled-down" version of the transmitter described above can be used in the design of the transceiver. Consequently, the transmitter subsystem in the transceiver does not need to consume as much as 0.46 W of power. Nevertheless, the transmit signal path in the transceiver still needs to be designed with a large enough bandwidth.

Examples of CMOS power amplifier (PA) designs suitable for the transceiver's implementation are the 40 and 65 nm CMOS PA design reported in [95] and [43] whose BW_{-3dB} / power gain is > 4 GHz / > 30 dB and power consumption / saturated output power (P_{sat}) is 99 mW / 10 dBm and 115 mW / 10.4 dBm, respectively.

4.3.3 Receive Signal Path

For the best SNR , the shape of the overall frequency response of the receive signal path of a pulse radar system must be matched to that of the pulse signal spectrum that the radar transmits [51]. As discussed in section 3.3.6, the combined -3 dB bandwidth of the 61 GHz tuned cascode amplifier circuit described in section 3.3.6 and the mm-wave direct-RF digitizer circuit used in the 61.5 GHz pulse radar transceiver design being discussed here is equal to ~ 7 GHz. Another output tuned stage can be added to the digitizer+buffer chain to reduce the chain's bandwidth to the 4 GHz required of the receive signal path in the transceiver design. In this way, the resulting digitizer buffer design should also achieve the 20 dB gain required of the circuit (see Table 4-1). The variable gain low noise amplifier (LNA) of the receive signal path in the transceiver (see Figure 4-2) can then be designed with a very wide bandwidth so that the path's overall bandwidth is still equal to 4 GHz. As a note, a 60 GHz LNA can be designed with a very wide bandwidth (>15 GHz) when the design employs a gain-bandwidth enhancement technique, as discussed in [84]. Lastly, if the center frequency of the transfer function across the receive signal path can vary significantly across process corners, the center frequency can be made tuneable to alleviate this concern [85].

One example of a prior-art design suitable for use as the design basis for the LNA of the receive signal path in the transceiver is the variable gain CMOS LNA design reported in [84]. [84] implements a gain-bandwidth enhancement technique using fourth-order magnetically coupled resonators in their LNA design to implement it with a -3 dB bandwidth of 28.3 GHz. As a note, the power gain/minimum noise figure/output-referred -1 dB compression point (OP_{1dB})/power consumption of the LNA is equal to 29.6 dB/6.4 dB/ ~ 1 dBm/31.3 mW.

As a note, the total gain required of the receive signal path in the transceiver is equal to 45 dB (see Table 4-1). Since this 45 dB gain is not spread across several frequency bands in the transceiver, care must be taken on how the amplifier stages in the receive signal path in the transceiver are laid out. A possible stability issue may occur due to some magnetic couplings between the stages in the path. According to [84], this can be anticipated during the design stage via electromagnetic simulations and can be managed using distancing, shielding, and cancelation techniques, whichever is appropriate for the design. An example of a prior-art design that contains a 60 GHz amplifier with a similar gain level is the 60 GHz transmitter design reported in [95]. The design contains a PA whose gain is equal to 38 dB and is unconditionally stable across its mm-wave signal path.

4.3.4 Frequency Generation

As shown in Figure 4-2, the frequency, f_{LO} , of the LO signal generated for the TX subsystem in the V-band pulse radar transceiver whose design is being discussed here is equal to 61.5 GHz. The TX pulses that the subsystem produces are generated in sync with this LO signal at a PRF that is equal to f_{LO} divided by an exact integer number (i.e., 858). Consequently, the carrier signal in the TX pulses always starts with the same phase in each pulse.

The I/Q CK signals clocking the I/Q digitizers in the transceiver are also generated in sync with the transceiver's TX LO signal with a frequency (f_{CK}) that divides f_{LO} into an integer number (i.e., 24). This arrangement allows for the TX pulses' echoes (i.e., the RX pulses) to be averaged coherently at the receiver end of the transceiver.

The chosen PRF and f_{CK} value implement a coherent ETS with a $\Delta t_{s,eff}$ of ~ 97.56 ps as calculated using the following equation:

$$\Delta t_{s,eff} = \frac{1/f_{CK} \cdot 1/PRF}{LCM(1/f_{CK} \cdot 1/PRF)} \quad (4-2)$$

in which LCM is the least common multiple operator [56]. In this arrangement, the transceiver implements a pulse radar system with 143 range bins ($L = PRI/\Delta t_{s,eff}$) and takes 35 and 3×36 samples for every 4 TX pulses that it transmits (i.e., $M = 35.75$ and $L/M = 4$). Under this arrangement, the maximum ambiguous range of the pulse radar system implemented using the transceiver is only ~ 2.1 m. The radar system can be made to occasionally scan at a lower PRF (by increasing the frequency division factor used to generate the PRF signal) to resolve range ambiguity when needed.

4.3.4.1 LO signal generation

In the presence of a strong clutter signal, the phase noise in the TX LO signal of the transceiver will affect the sensitivity of the Doppler measurements done by the transceiver. It will also degrade the overall SNR of the receive signal chain in the transceiver. Fortunately, since the same signal source (see Figure 4-2) is used to generate the TX LO signal and the CK signal used to clock the digitizers in the transceiver, self-coherence (also called range correlation) [51, 96] will reduce the effect of this phase noise. Self-coherence lowers the level of the phase noise at the output of the receiver in the transceiver since the phase noise in the transceiver's received echo signal and in the CK signal used to sample it are correlated [51, 96]:

$$\mathcal{L}_{coh}(f_{off}) = \mathcal{L}(f_{off}) + 10 \cdot \log \left(4 \cdot \sin^2(\pi \cdot TOF \cdot f_{off}) \right) \quad (4-3)$$

Here, TOF is the time-of-flight of the radar pulses transmitted by the transceiver, and $\mathcal{L}(f_{off})$ is the spectral density of phase fluctuations of the transceiver's TX LO signal in dBc/Hz.

One example of a PLL design suitable for use as the design basis for the PLL in the transceiver is the 60 GHz PLL design reported in [97]. The said PLL design is done and fabricated in a 65 nm bulk CMOS technology, and its power consumption is equal to ~25 mW. The PLL's integrated jitter (between 1 kHz and 40 MHz) computes to less than 250 fs RMS. If self-coherence is in effect, the jitter level at the receiver's output of the transceiver reduces to <80 fs RMS for a target located 3 m away from the transceiver. This jitter level is better than that encountered during the SNR characterization of the digitizer used in the transceiver design (see section 3.3.4).

4.3.4.2 I/Q CK generation

As shown in Figure 4-2, the transceiver employs a pair of I/Q digitizers in its design. I/Q digitization is required to avoid a repeated sampling at around the null points of the transceiver's received echo signal (i.e., at phase $0^\circ / 180^\circ$ of the pulse signal's sine wave carrier) from occurring [21]. To implement the I/Q digitization, one of the two digitizers is made to sample the signal at a phase offset of $(90/24)^\circ$ from the sampling position of the other digitizer. Under this arrangement, if one of the digitizers coincidentally samples the signal around the signal's null points, the other digitizer will sample the signal around its peak.

A circuit similar to the phase rotator circuit usually employed to shift the sampling position of a high-speed wireline receiver [98-100] can be used to implement the $(90/24)^\circ$ phase shift required in generating the quadrature (Q) CK signal in the transceiver. These phase rotators are usually designed with a resolution of 7-bit or

$2.8125^\circ/\text{LSB}$. Since what we are concerned with is the sampling position of the Q digitizer in relation to the phase of a 61.5 GHz carrier signal, a phase shift of $(90/24 \times 9)^\circ$ is equivalent to a phase shift of $(90/24)^\circ$. 2.8125° divides $(90/24 \times 9)^\circ$ exactly into 12.

As a note, the phase rotator circuit reported in [100] is designed and fabricated in a 65 nm bulk CMOS technology for operation with an input signal frequency of 7 GHz. The circuit's total power consumption is ~ 23 mW. The circuit's power consumption should reduce if it is designed for operation at ~ 2.5 GHz instead. The total integrated jitter (between 10 kHz and 1 GHz) of the phase rotator circuit is equal to around 106 fs RMS. This number should actually be lower since it should include the jitter of the signal source used in the circuit's characterization, as noted in [98].

4.3.5 Power Cycling

Based on the information provided in the previous section (section 4.3.4), the T_{acq} (i.e., the time required for an ETS pulse radar to complete an acquisition as defined in section 4.1) of a pulse radar system implemented using the proposed transceiver computes to ~ 3.5 μs . Consequently, if the targeted scan update rate of the radar system, f_{upd} , is equal to 1 kHz, the circuitries in the radar system can be switched off for $>99.5\%$ of the time. The settling times of the bias voltages of the circuitries reduce the percentage in which the circuitries can truly be in their off state. However, this overhead is expected to be <1 μs (the R-C time-constant of a 10 pF capacitor in series with a 10 k Ω resistor is equal to only 0.1 μs ; the capacitances present in each of the 60 GHz amplification stages in the transceiver should be <1 pF) except for that of the PLL in the transceiver. A PLL's loop response is expected to be slow since it is typically non-1st-order, and its bandwidth is typically <1 MHz.

The rate at which a person is breathing can be monitored using a radar device by measuring the Doppler shift in the frequency of the carrier signal of the radar echo signal reflected by him/her. Each Doppler shift measurement typically needs to run for as long as 10 seconds or more. The reason for this is so that the resulting radar echo signal spectrum can have a spectrum resolution bandwidth of <0.1 Hz [21, 22]. Fortunately, since a breathing-related movement phase modulates the radar signal with a modulation frequency of only ~ 1 Hz, a low f_{upd} of 50 Hz—for example—is sufficient for the measurement [21, 22]. With an f_{upd} of 50 Hz, the circuitries in the radar system can thus be power cycled with a duty cycle ratio that is 20× lower than that in the previous 1 kHz f_{upd} case. As a note, the PLL in the transceiver, however, cannot be power cycled if the transceiver's LO signal must be kept coherent across the duration of the Doppler shift measurement.

4.4 Estimated Performance and Comparisons

The proposed V-band UWB pulse-Doppler radar transceiver whose design is being discussed here and whose block diagram is illustrated in Figure 4-2 is estimated to consume <300 mW of power when the transceiver is not power cycled. This number is a guesstimate based on our literature survey of the building blocks required to construct the transceiver, as given in Table 4-2. The building block designs chosen to be referenced in the guesstimate are those that are close to what is required to implement the transceiver in a 40 nm CMOS technology. Their power consumption numbers are then adjusted based on the differences between their specifications and fabrication technologies and the proposed transceiver's implementation requirements. If there exists a reasonable possibility that a block's power consumption can be lowered, this will be indicated in Table 4-2 with the “<” symbol preceding the power consumption number. Lastly, our guesstimates will have some

inaccuracies. However, our evaluation of the proposed transceiver here will be from the perspective of its architecture choice, not block-level optimizations. Therefore, the inaccuracies in the block-level power consumption estimations should be relatively minor sources of inaccuracies in our evaluation of the transceiver.

Table 4-2 Estimating the power consumption of the V-band UWB pulse-Doppler radar transceiver design illustrated by Figure 4-2

		Power (mW)	Note
TX Path	PA	100	To be designed for a P_{sat} of ~ 10 dBm, an OP_{1dB} of ~ 5 dBm, a -3 dB bandwidth of >4 GHz, and a gain of >30 dB; the power consumption is estimated from [95], which reports a 40 nm CMOS PA design
	TX mixer + PA pre-amplifier	<30	We assume that the mixer and PA pre-amplifier chain does not attenuate the TX LO signal generated by the PLL; therefore, if the PLL's output power is >-20 dBm, the PA's 30 dB gain is enough to gain the TX LO signal to >6 dBm
	Baseband pulse generator	<10	The required pulse width and PRF are 220 ps and 71.68 MHz, respectively; the baseband pulse generator can be designed based on the propagation delay difference between two separate digital paths, as done in [101]; if process, voltage, and temperature spread is a concern, the delay can be controlled using a DLL feedback mechanism
RX Path	Variable gain LNA	45	To be designed for a maximum gain of 29 dB and a -3 dB bandwidth of >15 GHz; the power consumption is estimated from [84], which reports a 28 nm CMOS LNA design; [84]'s 31.3 mW power consumption is multiplied by $(40/28) \times$ to account for the technology node difference
	Digitizer's RF buffer	<30	• 2 copies with <15 mW of power consumption each • 2-stage mm-wave RF buffer circuit designed for a gain of 20 dB and -3 dB bandwidth of 4 GHz; each stage is expected to consume <7.5 mW of power (see section 3.3.6)
	Digitizer	<30	• 2 copies with <15 mW of power consumption each • The power consumption is estimated from the digitizer design presented in chapter 3; since the digitizer's design mainly consists of digital circuitries, the digitizer's power consumption should scale proportionally with its operation frequency
Fre- quency Gene- ration	PLL	25	• The power consumption is estimated from [97], which reports a 65 nm CMOS PLL design; the TX LO signal power generated by the PLL is assumed to be >-20 dBm, including routing loss • We assume that the frequency division ratios in the PLL's design can be tweaked to facilitate the generation of the $I\ CK$ and PRF signal in the transceiver (see Figure 4-2) without significantly affecting the design's performance and power consumption
	Q CK signal gene- ration	<20	The power consumption is estimated from [100], which reports a 65 nm CMOS phase rotator design operating at 7 GHz; [100]'s power consumption is ~ 23 mW; the power consumption should reduce if the circuit is designed for operation at ~ 2.5 GHz instead
	I/Q CK signal distribu- tion	<10	The capacitance of a 2 mm routing in the technology used to implement the transceiver is <1 pF, hence, the dynamic current consumed for distributing the two 2.5625 GHz CK signals can be expected to be $< \sim 6$ mA
Total Power		<300	

Table 4-3 Comparisons with prior-art CMOS UWB radar transceiver

	CMOS Tech.	Radar Type	Radar Signal Center Freq. Approx. BW_{-10dB} (GHz GHz)	Peak P_{TX} NF_{RX} (dBm dB)	G_{ANT} (dBi)	R_{max} for a 0.1 m ² target (m)	Range Bin's Width (cm)	T_{acq} L (μs bins)	Power Consumption Power-Cycling Duty Cycle Ratio (mW μs NIL)	T_{upd} $T_{upd,3m}$ $E_{3m} \cdot \frac{c}{2 \cdot BW_{-10dB}}$ (μs nJ • m)
This Work (estimate)	40 nm	Pulse Doppler (ETS, coherent)	61.5 6.6	6 6	15.5	3	1.46	3.5 143	<300 3.5 100% <26.5 1,000 0.35% (PLL is not power cycled) <1.75 1,000 0.35% (PLL is power cycled, needs 10 μs to lock)	3.5 <24 1,000 <600 1,000 <40
APMC '18 [4]	130 nm	Pulse (ETS, non-coherent)	8 1	- 6	7.1	6.3 ^{^^}	7.5	200 200 1 1	146 84 [#] 100%	2.06 45.1
JSSC '17 [2]	55 nm	Pulse Doppler (ETS, coherent)	7.25 1.5	5.6 6.3	6	11.2 [^]	0.64	4,681 1,536	92.9 excluding digital backend 4,681 100%	6.31 58.6
EuRAD '16 [6]	180 nm	Pulse (ETS, non-coherent)	4 0.5	- 5.2	9	7 ^{^^}	15	100 100 1 1	160 47 [#] 100%	0.68 32.6
JSSC '15 [8]	65 nm	Pulse Doppler (ETS, coherent)	4 0.7	-9 4.4	6 ⁺	3.9 [^]	0.023	2,500 25 ⁺ 100 1	88.2 2,500 ⁺ 100%	673 12,717
JSSC '14 [7]	130 nm	Pulse Doppler (ETS, coherent)	4 1.5	-3 3.7 - 4.3	3	8.7 ^{^^}	1.5	14,500 580 [#] 100 4	103 14,500 [#] 100%	71.5 738
JSSC '14 [29]	65 nm	Pulse Doppler (ETS, coherent)	161.4 15	10 22.5	8.8	0.3 [^]	0.375	0.8 80 [#] 0.16 16	>440 0.8 [#] 20%	80,000 > 351,756
TCASI '17 [1]	65 nm	Pulse (TDC-based, ΔΣ TDC)	3.2 - 4.64 0.62	1.48 6 - 10	-	0.6 ^{^^^}	0.568 (RMS)	6,250 1	17.2 6,250 mix of 20%, 40%, and 100%	Averaging to increase R_{max} is not applicable
ASSCC '15 [18]	65 nm	Pulse (TDC-based, 1TX, 4RX)	25.7 2.5	13.6 -	-	1.36	2.26	1 1	149 1 0.06% for the PA, 100% for the rest	
RFIC '14 [24]	65 nm	Pulse (TDC-based)	77.3 0.92	9.2 9	15.8 [*]	1.5 ^{^^^}	0.72	1.6 1	107 1.6 0.1% for the PA, 100% for the rest	

[#] Until R_{max} for a 0.1 m² target (target located at a distance of $>R_{max}$ from the transceiver is not scanned)

[^] Adjusted to lower the radar's average EIRP to -41.3 dBm/Hz; ^{^^} The radar's output SNR at R_{max} is not specified in the paper number of range bins = $2 \cdot (R_{max} \text{ for } 0.1 \text{ m}^2 \text{ target}) / (c \cdot \tau / 2)$

[^] Adjusted for an output SNR (post-averaging) of 10 dB for a 0.1 m² target located at a distance of R_{max} from the transceiver

^{^^} The radar's output SNR at R_{max} is not specified in the paper

^{^^^} No target RCS information

In Table 4-3, it is pointed out that the proposed radar transceiver can be power cycled either in part or its entirety, depending on its use case. I.e., if the PLL in the transceiver cannot be power cycled since the transceiver is carrying out a fully coherent Doppler shift measurement, the transceiver's average power consumption will be higher and will be dominated by the power consumption of its PLL. Here, the power cycling's duty cycle ratio is 0.35% when the transceiver is operated with a scan update rate of 1 kHz (as computed in section 4.3.5). With this duty cycle ratio, the difference in the transceiver's average power consumption when it is power cycled in part or its entirety will be between a few tens of mW and a few mW.

In Table 4-3, the estimated performance of the proposed radar transceiver is compared to that of some prior-art CMOS UWB pulse radar transceivers. Here, we introduce 2 performance metrics for comparing the transceivers' energy use efficiencies with the targeted end application of the proposed radar transceiver in mind: $T_{upd,3m}$ and $E_{3m} \cdot c / (2 \cdot BW_{-10dB})$. $T_{upd,3m}$ is the scan update period of a radar system with its averaging factor (N) adjusted so that its maximum range according to the radar range equation (R_{max}) [51] is equal to 3 m, and its number of range bins (L) scaled proportionally for operation with a maximum target range of 3 m:

$$T_{upd,3m} = T_{upd} \cdot (3 \text{ meter} / R_{max})^4 \cdot (3 \text{ meter} / R_{max}) \quad (4-4)$$

For simplicity, the $T_{upd,3m}$ values in Table 4-3 do not need to be achievable by the corresponding radar transceivers (due to some design constraints) or even practical. Meanwhile, E_{3m} is equal to $T_{upd,3m}$ multiplied by the power consumption of the corresponding radar transceiver. In other words, E_{3m} is the energy consumed by the corresponding radar transceiver to update its range scan results one time. Lastly, the $c / (2 \cdot BW_{-10dB})$ term is included in the metric so that the radar transceivers' performances for distinguishing closely spaced reflections are also considered. A radar whose -10 dB bandwidth (BW_{-10dB}) is higher has a finer range resolution but also a reduced R_{max} due to an increase in its receiver's noise floor level.

The $E_{3m} \cdot c / (2 \cdot BW_{-10dB})$ metric's value of the proposed radar transceiver can be among the lowest among the ETS pulse or pulse-Doppler radar transceiver designs listed in Table 4-3. The $E_{3m} \cdot c / (2 \cdot BW_{-10dB})$ metric's value of the proposed radar transceiver is among the lowest when the transceiver is not power cycled (i.e., <24 nJ•m) or when all the subsystems in the transceiver including its PLL are power cycled (i.e., <40 nJ•m). As a note, the prior-art radar transceiver designs whose $E_{3m} \cdot c / (2 \cdot BW_{-10dB})$ metric's values are low in Table 4-3 operate with radar signals whose center frequencies are below 10 GHz.

Table 4-3 also compares the proposed radar transceiver to some CMOS TDC-based pulse radar transceivers. The power consumption of a TDC-based pulse radar can be very low compared to its sampling-based counterpart, even without power cycling, since a TDC-based pulse radar requires a more straightforward receive signal processing. However, TDC-based pulse radars cannot incorporate averaging in their detection process. Consequently, their R_{max} are limited. As shown in Table 4-3, the power consumption of the proposed radar transceiver design, with power cycling, can be lower than that of a TDC-based pulse radar transceiver design.

4.5 Summary

This chapter discusses how a 60 GHz UWB pulse-Doppler radar transceiver can be designed with a direct-RF receiver using the direct-RF mm-wave UWB radar pulse digitizer circuit presented in chapter 3 of this work. The challenges to fully realize the transceiver are also anticipated and addressed. The performance of the proposed design is then estimated and compared with that of the prior-art CMOS UWB pulse radar transceiver designs. As discussed, the energy usage efficiency of the proposed 60 GHz UWB pulse-Doppler radar transceiver design is comparable to that of some prior-art UWB pulse radar transceiver designs operating at the sub-10 GHz UWB band.

Chapter 5

Conclusions and Future Works

5.1 *Conclusions*

This work aims to design a low-power digitizer capable of digitizing some mm-wave frequency signals (signals whose frequencies are >30 GHz) in bulk CMOS technology. The digitizer design is meant to be used to implement a CMOS mm-wave UWB pulse-Doppler radar transceiver with a direct-RF receiver. The receiver in such a radar transceiver must process narrow pulses and allow for adequately sensitive Doppler-shift measurements. Designing the radar transceiver with a direct-RF receiver allows for it to be designed with lower power consumption because a direct-RF receiver suffers less from flicker noise than its traditional super-heterodyne or homodyne counterparts. Additionally, without an explicit down-converter circuit, a direct-RF receiver does not need an LO signal, whose generation and distribution typically consume a lot of power at a mm-wave frequency.

The major hurdle in realizing a mm-wave UWB pulse radar transceiver with a direct-RF receiver is in designing a digitizer that can directly digitize a mm-wave UWB radar pulse signal. This work addresses this by proposing a novel ADC architecture which can be used to design such a digitizer with an acceptable level of attenuation, low power consumption, and reduced input capacitance. The DC offsets of the comparators in a digitizer that is designed based on the novel flash-ADC-like ADC architecture do not need to be calibrated down to less than a few LSBs. With this, the digitizer's calibration can cover a wide spread of DC offsets, and the comparators in the digitizer can be designed with less concern for their DC offsets variation.

On the downside, the proposed novel ADC architecture, whose working principle is based on the concept of multi-pass analog-to-digital conversion, requires the digitizer's input signal to be approximately periodic. Nevertheless, this downside is not an issue when the digitizer is used in the implementation of a pulse radar whose targets can be assumed to have the characteristics of either type I or type III Swerling targets whose *RCS* do not fluctuate significantly within the radar's integration time.

At the heart of the proposed digitizer is a comparator bank whose comparators must be designed with the capability to sample and compare a mm-wave frequency signal to some DC threshold values. In this work, each of these comparators is implemented as a 'bare' StrongARM latch. The comparator is implemented without a T/H circuit since a StrongARM latch can already perform the sampling function needed by each sub-ADC in the digitizer by itself. Meanwhile, the comparator is designed without a pre-driver stage since, without a T/H circuit, the stage will significantly limit the comparator's input bandwidth. The StrongARM latch circuit is then analyzed and designed considering its linearity, noise, input range, and input capacitance.

A 4 GSa/s prototype of the proposed digitizer design is designed and fabricated in a 40 nm LP CMOS technology. The prototype is measured to be capable of digitizing signals with frequencies of up to 64 GHz while maintaining an *ENOB* of >3.2 bits. This performance is achieved with a power consumption of <20 mW and a modest figure of merit without needing the digitizer to be fabricated in a much more advanced CMOS technology node. It is also shown that the 60 GHz tuned amplifier circuit that is to drive the digitizer circuit when the digitizer is used as part of a direct-RF receiver implementation can be designed with a gain that is more than enough to overcome the digitizer's 9 dB attenuation at 60 GHz while consuming <10 mW of power.

Lastly, the performance and power consumption of a 60 GHz UWB pulse-Doppler radar transceiver designed using the proposed digitizer is estimated. The prospective design then is compared with some prior-art CMOS UWB pulse radar transceiver designs reported in the literature. It is shown that the energy usage efficiency of the prospective 60 GHz design is comparable to that of the prior-art UWB pulse radar transceivers that operate at a much lower frequency band.

5.2 Future Works

As noted before, the power-cycled mm-wave UWB pulse-Doppler radar transceiver that the proposed digitizer circuit is meant to be used in has not been implemented yet. Therefore, the radar transceiver's full implementation, whose system-level design considerations are discussed in chapter 4 of this work, is one future work.

Additionally, as noted in section 4.4 of this work, the PLL in the power-cycled pulse-Doppler radar transceiver cannot be included in the transceiver's power cycling when the transceiver is used to carry out a Doppler shift measurement due to the transceiver's fully coherent design. Hence, the power-cycled radar transceiver is expected to consume a lot more power when the transceiver is used to carry out a Doppler shift measurement. Therefore, we propose the design of a pseudo-coherent version of the power-cycled pulse-Doppler radar transceiver as another future work. This type of pulse-Doppler radar is expected to come with a reduced Doppler shift measurement sensitivity, which may be tolerable in some applications.

Lastly, beamforming capability is desirable from a radar system's usage point of view. Therefore, a beamforming version of the radar transceiver is another future work suggested for the transceiver's design. Figure 5-1 illustrates a 4-channel phased-array receiver design that leverages the proposed digitizer circuit's direct-RF digitization capability.

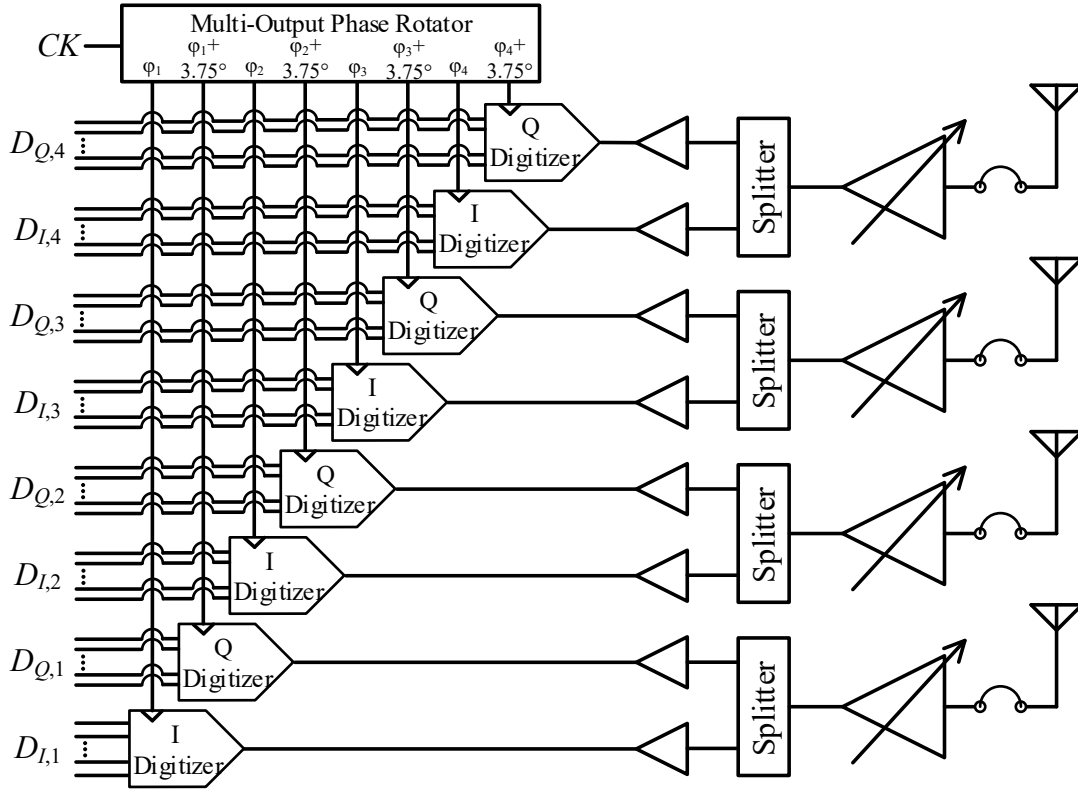


Figure 5-1 A 4-channel phased-array receiver design that does away with high-frequency LO or RF phase shifters; the Q-digitizers' clocks are phase-shifted by 3.75° from the I-digitizers' clocks here because, following the radar transceiver design proposed in chapter 4, the input signals' carrier frequency is $24\times$ the CK signal's frequency ($24 \times 3.75^\circ = 90^\circ$)

Regarding the proposed digitizer, the following design aspects can be further improved:

- The DACs' bank in the digitizer, which occupies most of the active area used in the prototype implementation of the digitizer, has not been optimized for its area usage. The DACs' bank mostly ($\sim 75\%$) consists of standard cell logic gates. Therefore, if a fully custom transistor-level logic design is pursued to compact the functionalities implemented by these standard cells, the resulting area usage of the digitizer can be reduced significantly.
- The prototype of the proposed digitizer, whose measurement results are reported in section 3.3 of this work, is designed for operation with a reduced input signal bias level because of the ESD protection device that needs to be placed at the input signal pin of the prototype's test chip. Consequently, the

prototype digitizer has a degraded sampling bandwidth and linearity performance. It will be interesting to know how much the digitizer's measured performance can be improved when this constraint is not present. Suppose the digitizer's attenuation level can be reduced while its *SNR* performance is maintained. In this case, we can proportionally reduce the gains of the amplifier stages that precede the digitizer when the digitizer is used as part of a direct-RF receiver implementation. With the gains of the amplifier stages reduced, the receiver's power consumption can be reduced.

Figure 5-2 below summarizes the improvements that can be made to the power-cycled mm-wave UWB pulse-Doppler radar transceiver design and the direct-RF mm-wave UWB radar pulse digitizer design proposed in this work.

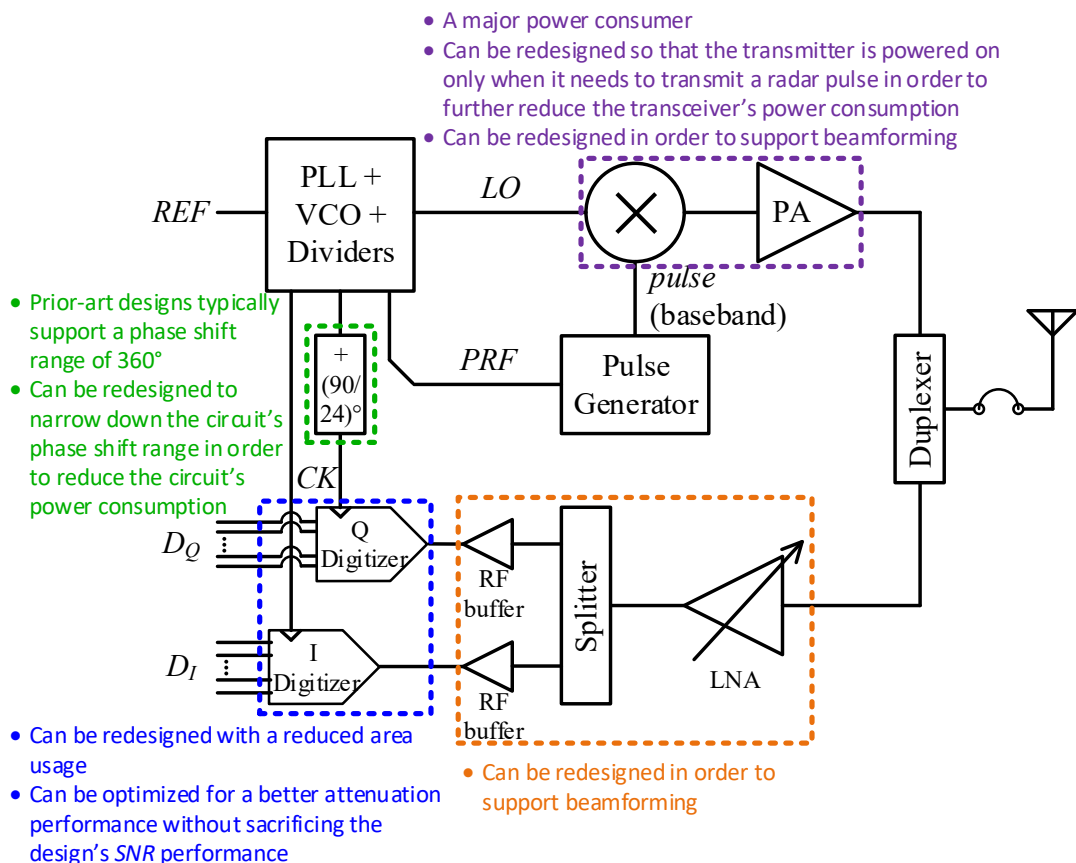


Figure 5-2 Improvements that can be made to the power-cycled mm-wave UWB pulse-Doppler radar transceiver design and the direct-RF mm-wave UWB radar pulse digitizer design proposed in this work

List of Author's Publications

- **G. L. Jaya**, C. C. Boon, S. Chen, and L. Siek, "An equivalent-time sampling millimeter-wave ultra-wideband radar pulse digitizer in CMOS," *IEEE Trans. Circuits Syst. I: Regular Papers*, submitted.
- **G. L. Jaya**, S. Chen, and L. Siek, "The design of clocked-comparator-based time-interval measurement circuit for pulse ToF measurement," *IEEE Sensors J.*, vol. 17, no. 20, pp. 6699 - 6706, Oct. 2017.
- **G. L. Jaya** and S. Chen, "A 40 nm CMOS T/H-less flash-like stroboscopic ADC with 23dB THD and >50 GHz effective resolution bandwidth," in *IEEE Int. Symp. Circuits Syst.*, Baltimore, MD, USA, May 28-31 2017, pp. 1 – 4.
- **G. L. Jaya**, S. Chen, and L. Siek, "A dual redundancy radiation-hardened Flip-Flop based C-element in 65 nm process," in *IEEE Int. Symp. Integr. Circuits*, Singapore, SG, Dec. 12-14 2016, pp. 1 – 4.
- **G. L. Jaya** and S. Chen, "Frequency-response-associated delay-dispersion issue in time-delay measuring sensors," in *IEEE Sensors*, Orlando, FL, USA, Oct. 30-Nov. 3 2016, pp. 1 – 3.
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- **G. L. Jaya**, S. Chen, and L. Siek, "A wideband memory-efficient analog to digital converter for periodic signals digitization," NTUitive, Nanyang Tech. Univ., Singapore, SG, Technol. Discl. Ref.: TD/077/15, 2015.

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