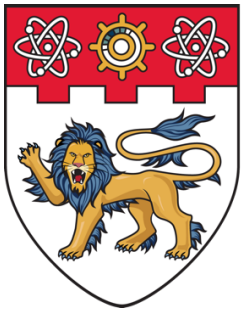


NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

Reliability Analysis and Improvement of Multilevel Converters

Tu Pengfei

School of Electrical and Electronic Engineering

2019

Reliability Analysis and Improvement of Multilevel Converters

Tu Pengfei

TU PENGFEI

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Reliability Analysis and Improvement of Multilevel Converters

Tu Pengfei

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

1 Apr. 2019 .....

Date

..... Tu Pengfei

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

1 Apr. 2019 .....

Date

..... Wang Peng

Authorship Attribution Statement

This thesis contains material from 2 papers published in the following peer-reviewed journals / from 2 papers accepted at conferences in which I am listed as an author.

Chapter 3 is published as P. Tu, S. Yang and P. Wang, "Reliability- and Cost-Based Redundancy Design for Modular Multilevel Converter," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2333-2342, March 2019. DOI: 10.1109/TIE.2018.2793263

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts, designed the case studies and analyzed the designs.
- Dr S. Yang revised the manuscript and verified the analytical results.
- Professor P. Wang revised and proofread the manuscript.

Chapter 4 is published as Q. Xu, P. Tu, C. Dong, C. Qi, S. Yang, S. Yao, P. Wang, "PoF based reliability prediction for cascaded H-bridge converter in drive application," *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 1759-1764. DOI: 10.1109/IFEEC.2017.7992314

The contributions of the co-authors are as follows:

- I prepared the manuscript drafts.
- Q. Xu edited the manuscript drafts and submitted it to the conference.
- C. Dong revised the manuscript and improved the figures.
- Dr C. Qi revised and proofread the manuscript.
- Dr S. Yang revised and proofread the manuscript.
- S. Yao revised the manuscript and improved the figures.
- Professor P. Wang reviewed the results and proofread the final manuscript.

Chapter 5 is published as P. Tu, P. Wang, X. Hu, C. Qi, S. Yin and M. A. Zagrodnik, "Analytical evaluation of IGBT turn-on loss with double pulse testing," *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, Hefei, 2016, pp. 963-968. DOI: 10.1109/ICIEA.2016.7603721

The contributions of the co-authors are as follows:

- I wrote the drafts of the manuscript. I performed data analyses and equation derivations.
- Professor P. Wang revised the manuscript and proofread the final conference paper.
- Dr X. Hu designed the hardware platform for experiments. He instructed me in experiments.

- Dr C. Qi designed and fabricated the hardware platform for experiments. He also instructed me in experiments.
- Dr S. Yin revised the manuscript and proofread the final conference paper.
- M. A. Zagrodnik helped us in the experiments and revised the manuscript.

Chapter 5 is also published as S. Yin, P. Tu, P. Wang, KJ Tseng, C. Qi, X. Hu, M. Zagrodnik, R. Simanjorang, "An Accurate Subcircuit Model of SiC Half-Bridge Module for Switching-Loss Optimization," in *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3840-3848, July-Aug. 2017. DOI: 10.1109/TIA.2017.2691734

The contributions of the co-authors are as follows:

- I developed the power semiconductor analytical model. I combine the analytical model with Dr S. Yin's circuit model to give accurate predictions on switching dynamics. I wrote the drafts of manuscript. I performed experiment data analyses.
- Dr S. Yin developed the circuit model and the hardware platform for experiments. The experiments validation were done by us together.
- Professor P. Wang reviewed the results and proofread the final manuscript.

- Professor KJ Tseng reviewed the results and proofread the final manuscript.
- Dr C. Qi instructed me in experiments. He revised the manuscript.
- Dr X. Hu instructed me in experiments. He revised the manuscript.
- M. Zagrodnik provided help on hardware platform development and experiments.
- R. Simanjorang provided help on hardware platform development and experiments.

1 Apr. 2019 Tu Pengfei

....

Date Tu Pengfei

Acknowledgements

I must express my sincere gratitude to those who have helped me in my Ph.D. journey. First of all, I must thank my supervisor professor Wang Peng for leading me to the exciting and challenging field, power electronics and its reliability. Thanks to the tolerant atmosphere created by him, I can try many interesting research problems in power electronics. I really appreciated his generous and invaluable advice during the course of my Ph.D. research.

I would also like to acknowledge financial support from the Rolls-Royce@NTU Corporate Lab. They provide world-class equipment and professional guidance for me to explore power electronics and its reliability. My special thanks go to my team members in medium voltage converter project under Rolls-Royce@NTU Corporate Lab. They are Mr. Michael Zagrodnik, Dr. Hu Xiaolei, Dr. Qi Chen and Dr. Yang Shunfeng, to whom I owe my early training in power electronics research. And thanks for their exciting problems and offering help when in need. Also thanks to the high power density converter team: Dr. Rejeki Simanjorang, Dr. Tong Chin Foong, Dr. Yin Shan, Dr. Arie Nawawi, Dr. Liu Yong for sharing knowledge and skills. Without their help, I can never imagine finishing the thesis smoothly.

I must express my gratitude to my colleagues and friends for their discussion, help, and encouragement. They are Ms. Chen Xuebing, Ms. Xu Qianwen, Mr. Fan Fei, Mr. Yu Yang, Mr. Zhai Jianyang, Mr. Lin Pengfeng, Mr. Li Ting, Mr. Wan Luoma, Mr. Li Benzhe, Dr. Ji Dongxu and Dr. Zhou Dehong. Also thanks to the technicians, Dr. Chen Jian, Mr. Tan Peng Chye and Mr. Lim Kim Peow for their patient assistance and help.

Finally, I would like to express my deep sense of gratitude to my family for their support and care all the time.

Abstract

Power converter based variable-frequency drive is much more energy efficient than traditional fixed-speed motor. It can reduce the operating cost of motor drive system significantly. However, the reliability of power converter is a salient concern for both manufacturers and end users as high failure rate will incur additional repairing cost. In high power drive applications, multilevel converters which utilize mature power semiconductors are superior to conventional two-level converters in efficiency and power quality. But the reliability problem of multilevel converters is more serious due to a large number of vulnerable power semiconductors used. Therefore, reliability analysis and improvement of multilevel converters are indispensable for popularization and application of variable-frequency drive.

Traditionally, there are two branches in reliability modeling: failure rate methods and Physics-of-Failure methods. The data-driven statistical failure rate methods are widely used in power system for their simplicity and effectiveness. There is a crucial assumption that the failure rate is constant during equipment useful lifetime. The assumption is reasonable in power system where equipment is operating in a relatively stable condition and under good maintenances. However, due to harsh environment and variable load in drive systems, the equipment stress change severely and rapidly leading to a questionable assumption of constant failure.

A load-dependent failure rate method is proposed to model the variable load. In the proposed method, the failure rate can be represented as an equivalent constant value or a time-varying function depends on the application. In traditional failure rate methods, the reliability index, Mean Time to Failure (MTTF), is widely used to give a life expectancy. MTTF is the reciprocal of system failure rate in the condition of constant failure rate. With time-varying failure rate, MTTF is almost impossible to calculate in practice. A new reliability index, MTTF consumption is proposed to describe the state of health of a power converter. Multilevel converters with modular design have inherent redundancy which gives them fault-tolerance capability. The network reliability modeling techniques, combinatorics and stochastic process,

are used to model the inherent redundancy in multilevel converters. With the aforementioned techniques, the complete and systematic load-dependent failure rate method can be applied to analyze multilevel converter reliability. The Monte Carlo simulation is used to verify the results of load-dependent failure rate method.

On the other hand, Physics-of-Failure methods which model failure mechanisms draw lots of attention in the power electronics community recently. These methods calculate components lifetime consumption under a mission profile with pre-established life-stress models. The converter system lifetime is determined by the weakest component. The Physics-of-Failure methods give a deterministic lifetime with clear physics-based models. However, multilevel converter redundancy and system-level reliability are hard to model as there is no component lifetime distribution. The randomness of failure and probabilistic property of reliability are lost.

A probabilistic Physics-of-Failure method is developed by including uncertainty of component parameters and life-stress model parameters. An assumption that parameters follow normal distributions is used in the proposed method to simulate the manufacturing process. Component lifetime distribution can be obtained by repetitive Physics-of-Failure analyses or a Monte Carlo simulation. The component reliability function can be extracted by probability distribution fitting. The multilevel converter redundancy and system-level reliability can be modeled by well-established statistical techniques.

This thesis provides reliability analysis methods for power converters and especially, multilevel converters and explores possible measures to improve reliability and reduce cost. The thesis has three parts. Part 1 has two chapters with chapter 1 introducing the multilevel converters and its reliability problems, and chapter 2 reviewing reliability modeling history and methods. The second part discusses the two proposed reliability modeling methods with case studies. Improving reliability in component level by switching loss optimization is also presented in this part. The last part draws the conclusions and proposes some future works.

Table of Contents

List of Figures

List of Tables

Nomenclature

Acronyms

3L-NPC	3-Level Neutral Point Clamped Converter
5L-ANPC	5-level Active Neutral Point Clamp converter
AGREE	Advisory Group on Reliability of Electronic Equipment
ASTM	American Society for Testing and Materials
CHB	Cascaded H-Bridge
CNPC	Cascade Neutral Point Clamp converter
CSI	Current Source Inverter
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DG	Distributing Generator
DUT	Device Under Test
EMI	Electromagnetic Interference
EPRI	Electric Power Research Institute
ESR	Equivalent Series Resistance
ETO	Emitter Turn Off thyristor

FIT	Failure In Time
FLC	Flying Capacitor
FOC	Field Oriented Control
FWD	Free-Wheeling Diode
GTO	Gate Turn Off thyristor
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
IRE	Institute of Radio Engineers
LV	Low Voltage
MH-217	Military Handbook-217
MH-217	Millitary Handbook 217
MMC	Modular Multilevel Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MTTF	Mean Time To Failure
MV	Medium Voltage
MW	Megawatt
NPC	Neutral-Point-Clamped
NPC-OWM	Neutral Point Clamp converter with Open end Winding Motor
PCB	Printed Circuit Board

PoF	Physics of Failure
PWM	Pulse Width Modulation
RADC	Rome Air Development Center
RBD	Reliability Block Diagram
RCA	Reliability Analysis Center
SOA	Safe Operation Area
THD	Total Harmonic Distortion
UTS	Ultimate Tensile Strength
VFD	Variable-Frequency Drive
VSI	Voltage Source Inverter
WBG	Wide Bandgap

Symbols

α_{Al}	CTE of aluminum
α_{Si}	CTE of silicon
β	transconductance coefficient
ΔT_j	junction temperature fluctuation amplitude
γ	crystalline material surface energy
λ	failure rate
μ	repair rate
π_j	j^{th} π factor
ψ_m	motor normal flux

$\sigma_{theoretical}$	theoretical strength of a crystalline material
ε	permittivity
B_α	percentiles of lifetime
C_{th}	thermal capacitance
E_a	activation energy
f	frequency
f_s	switching frequency
h	thickness of the bond heel
k_B	Boltzmann constant
l	length of the bond heel
L_C	life consumption
N_i	expected cycle to failure under repetative i^{th} stress
n_i	stress cycles of i^{th} stress
r_o	equilibrium distance between atomic centers
R_{th}	thermal resistance
T_0	core temperature of capacitor
T_c	core temperature of capacitor
Z_{th}	thermal impedance
ppm	parts-per-million

Chapter 1

Introduction

Power converter based variable-frequency drive (VFD) can save a lot of energy than the fixed-speed motor. Among a number of power converter topologies, multilevel converters have superior electrical performance but inferior reliability to 2-Level converter. Reliability problem of multilevel converters is a salient concern for manufacturers and consumers.

Improving reliability with limited cost is always a target of manufacturers and consumers. Accurate reliability analysis can provide guidance on reliability improvement cost-effectively. Traditional power converter reliability modeling methods are based on outdated standards using statistical models. Recent research efforts aim to develop accurate Physics-of-Failure (PoF) methods. As PoF methods usually ignore statistical properties of reliability, they fail to model redundancy which is a critical property of multilevel converters for reliability improvement.

In view of these issues, the thesis proposed two reliability modeling methods for multilevel converters, one is the load-dependent failure rate method and the other one is the probabilistic PoF method. With the failure rate method, a reliability and cost based redundancy design for module-design multilevel converters is provided. The Physics-of-Failure analysis concludes that high amplitude temperature cycling accounts for most of the fatigue damage on power semiconductors. Power semiconductor switching loss optimization is also investigated aiming to improve

reliability by reducing temperature cycling amplitude.

The rest of this chapter introduces the background, motivation, contribution, and organization of the thesis. This chapter gives a brief overview of multilevel converters in terms of merits, reliability problems, and reliability modeling challenges.

1.1 Background

1.1.1 Power Electronics for Energy Saving

Power electronics is an enabling technology for energy processing [1–3]. More than 70% of electrical energy produced is processed by power electronics converters before supplied to end-users [4]. Power converters are widely used for energy saving with its high conversion efficiency in Variable-Frequency Drive (VFD) systems, High-Voltage DC (HVDC) systems and Distributed Generators (DGs). Benefit from high efficiency, power converters could reduce system operation cost directly. Besides, power electronics would also mitigate global warming problem indirectly by allowing a higher renewable energy penetration.

The Electric Power Research Institute (EPRI) estimated that 60–65% of electrical energy is used for motor drive systems in the United States, 75% of which are variable-torque fan, pump and compressor loads [5]. For variable-torque fan, pump, and marine propulsion applications, the load torque and power vary with the square and cube of motor speed respectively. Compared to the fixed-speed motor drive, the VFD consumes much less power in light load. For example, VFD consumes only 12.5% of its full-speed power at 50% speed while fixed-speed pump may consume 50% to 100% full-speed power [6, 7]. For motors with VFD, energy can be saved up to 30% in light loading condition [5]. Only about 3% of the total motors are provided with VFD and about 30%-40% newly installed motors are equipped with VFD [8]. Note that most of AC motors are high-power equipment. There is a great potential to reduce energy consumption in high-power motor drives. Proper energy saving techniques for these motors are pressingly needed [9].

1.1.2 Multilevel Converter for High Power Drive

The high-power motor drives are widely applied in different industry sectors, such as pipeline pumps in petrochemical industry, fans in cement industry, traction applications in transportation industry, steel rolling mills in metals industry [10]. Although low-voltage (LV) drives have up to 5-6 megawatts (MW) power ratings, economic considerations usually favor medium-voltage (MV) drives. In high power MW-scale drive system, with the increase of voltage level, the ohmic loss reduces as load current decreases. Therefore MV drives from 2.3 kV to 13.8 kV are proposed to replace its low voltage counterparts in high power applications, such as ship propulsion and pipeline pumps.

Advances in power semiconductor devices lead the way in high power MV drive development. High power MV drive started in the mid-1980s with the commercialization of 4500V gate turn off thyristors (GTO), integrated gate commutated thyristor (IGCT) and emitter turn off thyristor (ETO) [10, 11]. With the advent of high-voltage insulated gate bipolar transistor (IGBT) in the late 1990s and commercialization of 6.5kV IGBT, the high-voltage IGBT has been accepted as the substitute to thyristor-based devices for high power applications [10, 11]. With the development of power semiconductor devices, different drive converter topologies are explored. Fig. 1.1 shows a classification of high power converter topologies in industry application [12].

The cycloconverter converts a constant frequency AC waveform to another AC waveform of a lower frequency by synthesizing the output waveform from segments of the AC supply without an intermediate DC link for AC motor drive systems [13]. The much lower output frequency and high content of harmonics limit the application of cycloconverter. A typical indirect power converter usually consists of three parts, a front-end rectifier, an energy buffer DC-link and an output inverter. Depending on whether inductor or capacitor is used as an energy buffer, power converter topologies are categorized into Current Source Inverter (CSI) and Voltage Source Inverter (VSI). For efficiency and power quality considerations, VSI is preferred in most motor drives.

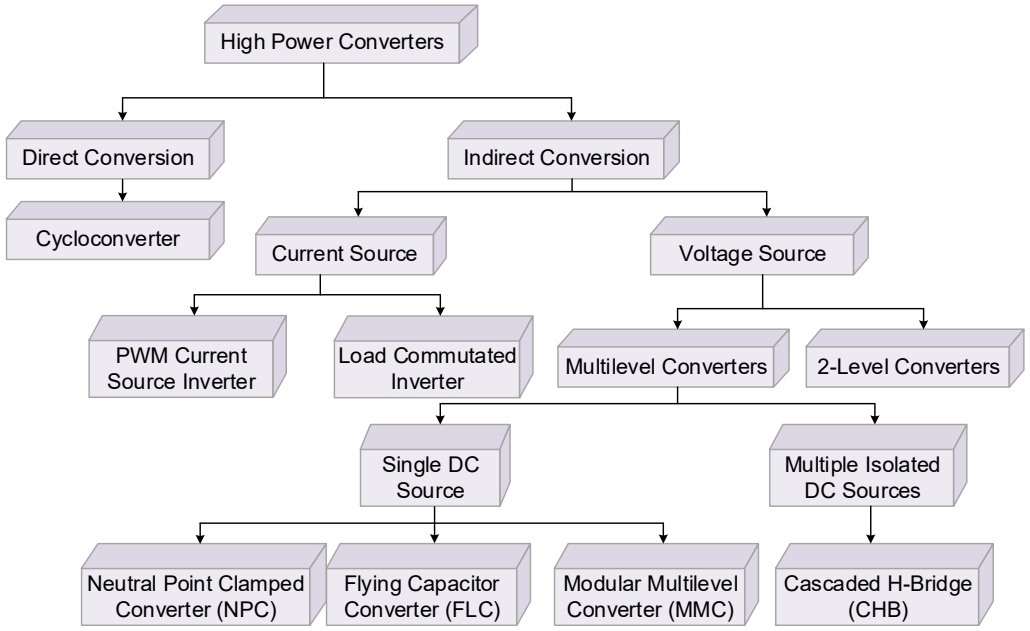


Figure 1.1. Tree diagram of different classifications of high power converters

Fig. 1.2 shows a 2-Level converter and four multilevel converters. Both 2-Level and multilevel converters can achieve high power conversions. For 2-Level converters, their voltage ratings are normally restricted by switching devices. The voltage blocking capability of the devices are limited by the inherent physical characteristics of semiconductor materials. There is always a need to develop high-voltage semiconductor switching devices [14]. Although switching devices with 6.5 kV voltage rating are available in market, it is much more expensive when compared to those mature low voltage semiconductors. Another way to overcome the voltage limit of 2-Level converters is to connect multiple low-voltage semiconductors in series to form a compound switching device. The series-connected switching device has voltage balancing and switching time synchronization problems [1]. Auxiliary circuitries are required to balance the voltage, resulting in power derating and additional losses [12].

The four multilevel converters in Fig. 1.2 are Flying Capacitor converter (FLC), Neutral-Point-Clamped (NPC) converter, Cascaded H-Bridge (CHB) converter, and

Modular Multilevel Converter (MMC). The NPC and CHB are the two commonly used converters in industrial MV drives. The MMC was proposed by Marquardt in 2003 for HVDC applications [15], and it is also a promising candidate for MV drive. Another well-known multilevel converter is the Flying Capacitor Converter (FLC) which uses capacitors for clamping. Due to the capacitors pre-charge and voltage balancing issues, the practical use of FLC in drive system seems to be limited [10].

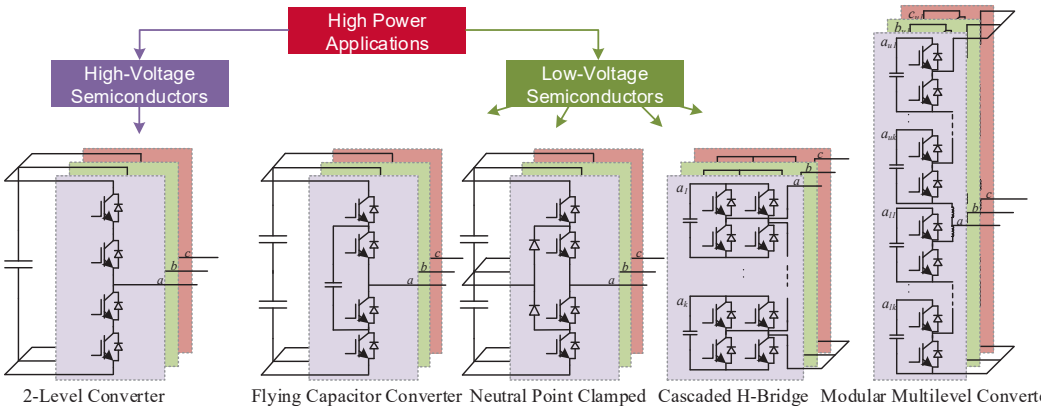


Figure 1.2. Topology competition for high-power applications

Multilevel converters were invented to overcome the limit of power semiconductor voltage blocking capability [12]. The converter could produce multi-step waveforms [16] and present elegant advantages over a 2-Level converter. The advantages mainly focuses on output power quality improvements including low total harmonic distortion (THD), low switching losses, low $\mathrm{d}v/\mathrm{d}t$, and redundant operation. These advantages together with the advancement in power semiconductor devices make the multilevel converters considerably attractive for high-power applications.

To show the advantages of multilevel converters, the output voltage of a 2-Level converter and several multilevel converters are shown in Fig. 1.3. The equivalent switching frequencies which equal the number of steps in 1 second are kept the same for fair comparisons.

It is apparent that power converters have better output voltage quality with

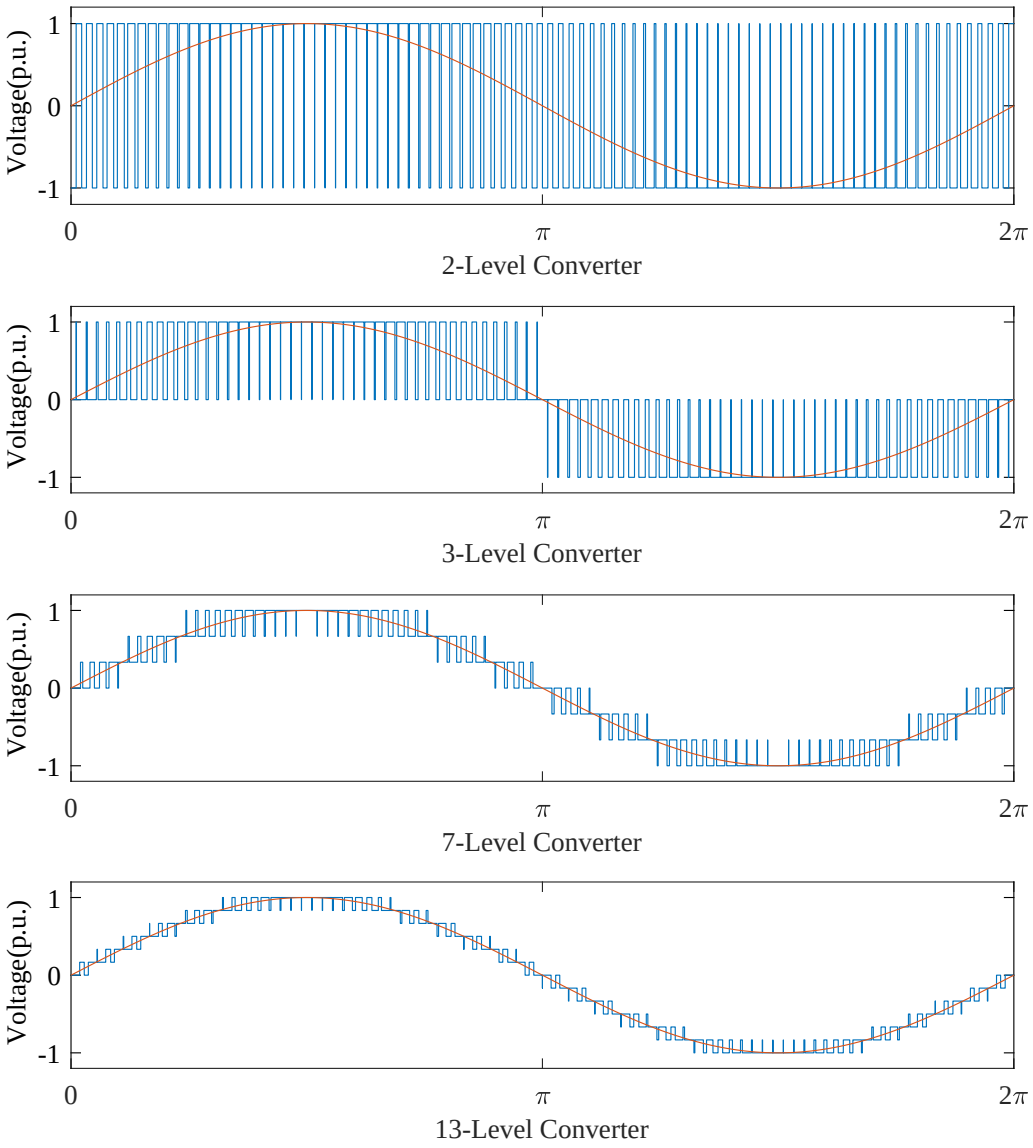


Figure 1.3. Comparison of output phase voltage waveforms among different converters

the increase of voltage levels. The multilevel converters resemble the sinusoidal reference more closely than the 2-Level converter.

Table 1.1 gives some key properties comparison for 2-Level, 3-Level, 7-Level, and 13-Level converters. With the same equivalent switching frequency, the required triangular carrier frequency decreases with the increase of voltage levels.

In high-power 2-Level converter, series-connected power semiconductors are used to withstand high voltages. All semiconductors would switch simultaneously at a high frequency, which gives a remarkable switching loss. For 2-Level converters, bulky inductors are needed to filter out the high frequency harmonics to attain high-quality currents. In contrast, multilevel converter output voltage THD is sufficiently low by nature. The bulky and costly inductor filters can be avoided in multilevel converters with enough output voltage levels. As the $\mathrm{d}v/\mathrm{d}t$ of multilevel converters are much lower than 2-Level converters, the common-mode choke inductance requirement is also reduced significantly. In conclusion, more voltage levels in a multilevel converters give better electrical performances. The THD indices in Table 1.1 is calculated under a unity modulation index. It should be noticed that, for MV applications, if high-voltage IGBTs are available, for example, 15 kV or even higher, there is no need to use series-connected compound IGBT.

Table 1.1. General electrical performance comparison of 2,3,7,13-Level converters

Topo. \ Prop.	$f_{carrier}$	THD	$\mathrm{d}v/\mathrm{d}t$
2 Level	4500Hz	100%	1.0 p.u
3 Level	2250Hz	52%	0.5 p.u
7 Level	750Hz	18%	0.17 p.u
13 Level	375Hz	9%	0.08 p.u

More IGBTs are needed in multilevel converters to produce more voltage levels. An intuitive perception is that more components involved lead to a lower reliability. Table 1.2 gives a brief summary of multilevel converters advantages and disadvantage over 2-Level converters.

Table 1.2. Properties summary of 2-Level and multilevel converters

Topo. \ Prop.	Efficiency	THD	EMI	Reliability
2 Level	> 95%	High	High	High
Multilevel	> 95%	Low	Low	Low

1.1.3 Reliability Problems of Multilevel Converters

It is unquestionable that multilevel converter would help to increase voltage levels. As explained previously, the increased voltage levels enabled by more power semiconductors (IGBT, MOSFET) and energy buffer elements (capacitors) certainly achieve better power qualities. However, the more components used, the lower reliability would be. Without redundant designs, multilevel converter is not as reliable as 2-Level converter.

However, the reliability performance of the 2-Level converter per se is not satisfactory in industrial applications. According to an industry-based survey on reliability [17], power converters are the most fragile devices in the motor drive system. The failure rate of the power converter in the motor drive system is much higher than those in the utility grid due to severe operating conditions such as frequently changing load and adverse environmental conditions. For an individual IGBT, its failure rate in multilevel converters is in the same order of magnitude as that in 2-Level converters. Nevertheless, multilevel converter has a higher failure rate than 2-Level converter due to that much more IGBTs are used. For example, IGBT quantity in a 13-Level converter is 12 times of that in a 2-Level converter, resulting in a much higher converter failure rate.

Besides the high failure rate, power converters failure/cost ratio in motor drives is also as high as 50%-80% compared to 10%-20% in utility grid. The failure/cost ratio is the ratio of failure cost to original system cost. As multilevel converters

make use of multiple IGBTs to withstand high voltage, one failed IGBT may shift its voltage stress to the other IGBTs, leading to cascading failures. Most power converters in motor drive system have no redundant design while utility industry always considers redundancy and backups [17,18]. The aforementioned three issues, high failure rate, high failure/cost ratio, and no redundancy, result in a large increase in motor drive life-cycle cost. These issues would be much more serious in multilevel converters than 2-Level converters. Reliability problem of multilevel converters is a prominent concern for both manufacturers and consumers, and they always target at improving reliability with limited cost. An accurate reliability modeling approach and related analyses are highly needed to provide guidance on reliability improvement cost-effectively.

1.1.4 Challenges of Multilevel Converters Reliability Modeling

Generally, there are two branches in reliability modeling: failure rate based statistical methods and root cause based Physics of Failure (PoF) methods.

The failure rate based statistical methods are widely used in power system for its simplicity and effectiveness. The constant failure rate assumption calculates directly the device expected lifetime as the reciprocal of device failure rate. This crucial assumption is reasonable for devices which are operating in stable condition and under good maintenances such as transformers and generators in the power system. The well-established statistical techniques also promote the prosperity of failure rate reliability modeling methods. Many reliability standards and handbooks are produced in the last 50 years. The most famous one is Military Handbook-217 (MH-217), which is the basis of many other standards. MH-217 starts its A version in 1965 and had stopped updating since 1995. Although the latest F version MH-217F has an outdated database, it is still widely used today. The statistical methods only use a constant failure rate under a typical or rated load to predict the expected lifetime. It is acceptable in topology comparison during the design stage for manufacturers.

However, the statistical methods are questioned and criticized recently due to large errors between predicted lifetime and field results [19]. The main cause of inaccuracy is the constant failure rate assumption. Motor drive systems are operating with harsh environment and fast-changing load. These versatile operations result in a time-varying failure rate. An oversimplified constant failure rate cannot reflect the fast-changing load in operation stage, thus giving a large error in lifetime prediction. To enhance accuracy, it is possible to incorporate a time-varying load-dependent failure rate model into reliability assessment in practice. But the expected lifetime calculation will be a problem with the time-varying failure rate as a full load profile is needed in advance.

On the other hand, the PoF methods which model failure mechanisms of components draw lots of attention in the power electronics community recently. The PoF methods are advocated by microelectronics industry for their clear physical meaning. The PoF methods calculate component lifetime by accumulating fatigue damage under a load profile. The fatigue damage is computed with component lifetime models obtained from accelerated testing. Once the fatigue damage accumulates to 100%, the component is regarded to be failed [20]. On these bases, an accurate lifetime can be identified for each component. The converter lifetime can be subsequently determined by the least component lifetime. The PoF methods improve the component lifetime prediction accuracy by using detailed lifetime models and complex load profile analysis. The PoF methods usually give lifetime consumption under a particular load profile. It is suitable to predict operating reliability for consumers.

However, PoF methods are deterministic. They do not consider the inherent probabilistic property of reliability as underlying uncertainty and randomness are not modeled. System-level reliability and redundancy are hard to model with PoF methods. Evolving PoF reliability analysis from component level to system level is still an open research topic in power electronics [4].

1.2 Motivation and Contribution

Power converter based VFD can save a lot of energy. Among a number of topologies, multilevel converters have superior electrical performance. Reliability problem of multilevel converters is a outstanding concern for manufacturers and consumers, who always target higher reliability with lower cost.

Accurate reliability analysis can provide guidance on reliability improvement in a cost-effective fashion. Traditional reliability modeling methods are either inaccurate or insufficient to model multilevel converters for which systematic reliability modeling methods are urgently needed.

Therefore, the thesis proposed two systematic reliability modeling methods for multilevel converters, one is the load-dependent failure rate method and the other one is the probabilistic PoF method. Based on statistical methods, a time-varying load-dependent failure rate method is proposed to model the variation of operating conditions. In traditional methods, the reliability index of an expected lifetime, Mean Time to Failure (MTTF), is not applicable to the newly proposed method. An alternative reliability index, MTTF consumption which takes time-varying load into consideration is proposed to model the state of health of a power converter. A reliability and cost based redundancy design guideline is also provided to improve multilevel converter reliability cost-effectively.

On the other hand, a probabilistic PoF method is developed based on the proposed component parameters normal distribution assumption. The proposed method bridges the gap between component level PoF reliability analysis and system level reliability modeling of multilevel converters. By means of the proposed PoF approach, it is found that the converter overall reability can be effectively improved by reducing thermal cycling stress in components. Moreover, further analyzing results indicate that thermal stress could be significantly lowered by optimizing switching loss when semiconductor gate driver is properly designed.

1.3 Thesis Organization

This thesis consists of six chapters which are organized as follows:

- Chapter 1 introduces the background, motivation, contribution, and organization of the thesis. It gives a brief overview of multilevel converters' merits, reliability problems, and their reliability modeling challenges. The motivation and contribution of the thesis are also summarized.

- Chapter 2 gives a detailed and in-depth literature review on reliability modeling of multilevel converters. Reliability history, fundamentals, and two widely used modeling methods, failure rate based methods and the Physics of Failure (PoF) methods, are first presented. Following that, reliability comparison of different multilevel converters is conducted with prevailing failure rate method.

- Chapter 3 presents the proposed load-dependent failure rate method for a systematic reliability modeling. A new reliability index, expected lifetime consumption, is introduced to replace the inapplicable MTTF index in the new method. A reliability and cost-based redundancy design guideline is provided to improve reliability cost-effectively for multilevel converters with a modular structure.

- Chapter 4 focuses on the development of the probabilistic Physics of Failure (PoF) method. The proposed method makes system level reliability analysis and redundancy modeling feasible. A case study is conducted to demonstrate the corresponding PoF methods. Sensitivity analysis identifies that the most critical stress lies in the temperature cycling of power semiconductors.

- Chapter 5 tries to improve multilevel converter reliability with the reliability analysis results from Chapter 4. Gate driver optimization is investigated in-depth to improve power semiconductors lifetime by reducing thermal cycling stress.

- Chapter 6 summarizes the key conclusions and recommends some future works on multilevel converter reliability improvement from design, modulation and control perspectives.

Chapter 2

Literature Review

2.1 Introduction

Multilevel converters are very attractive in high power applications in many industry sectors. They are suitable for diversified voltage applications without using high-voltage (HV) or series-connected compound power semiconductors, which is the main advantage of the multilevel structure. The low harmonic of multilevel converters avoids the usage of bulky filter inductors. Nevertheless, due to a high component count, the reliability performance of multilevel converters is always in question. But multilevel converters, especially those with modular structures, have redundant switching states which endow them with fault-tolerant operation capability. The capability could be utilized to improve their reliability significantly. Without quantitative reliability analyses, it is less possible for manufacturers and consumers to adopt multilevel converters. Systematic Reliability modeling methods considering redundancy are hence needed to mitigate their reliability concerns.

Reliability modeling received attention in World War II due to the high failure rates of electronics devices. Much pioneering research had been devoted to reliability modeling since the 1950s. Statistical techniques are well established to analyze the field data by mathematicians. Based on these techniques, one of the main streams of reliability modeling methods were prospering. Quantitative reliability modeling

methods along with previous empirical failure data are summarized to produce various reliability handbooks during last 50 years. These easy-to-use handbooks gained popularity very quickly although they gave inaccurate prediction sometimes.

Another stream of the reliability modeling focuses on identifying and modeling failure mechanisms by engineering principles. Failure causes are classified as different stresses such as thermal, electrical, vibration, etc. Lifetime models regarding different stresses were built to calculate the damage on components. When damage accumulates to 100%, the component would fail and should be replaced. This concept of reliability modeling is named as Physics of Failure (PoF) method. The PoF methods have started to gain attention in the 1990s with the fast development of microelectronics, especially in integrated circuit (IC) applications. The PoF methods can give an accurate lifetime prediction with complex multidisciplinary models. There is always a trade-off between accuracy and simplicity.

This chapter gives a detailed and scrupulous literature review on reliability history, reliability fundamentals, and two streams of reliability modeling methods (failure rate based statistical methods and Physics of Failure methods). Following that, a rough reliability comparison of multilevel converters for topology selection is conducted with a failure rate based method.

2.2 Reliability Modeling History

The last two centuries saw numerous engineered devices and systems contributed by technological revolutions. Since the first recorded usage of the word "Reliability", reliability has become a pervasive attribute. Before reliability developed into a scientific discipline, there were efforts to improve the reliability of engineered devices from design to manufacture. But the reliability improvement were not guided by the reliability research outcomes.

Since mass production is popularized for engineered devices in the early 20th century, the need for a methodology to assess large-scale products' reliability stimulates the growth of reliability engineering into a scientific discipline [21].

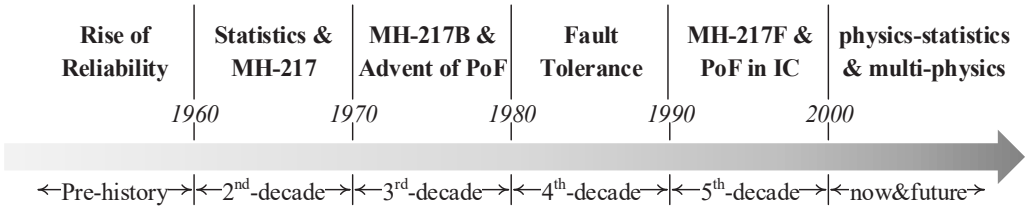


Figure 2.1. Reliability engineering development

Fig. 2.1 shows some key milestones in the development of the reliability engineering discipline. In the 1950s and 1960s, a variety of organized research efforts in reliability engineering were emerging due to lots of electronic equipment failures throughout the World War II. Electronic equipment played a critical role in World War II. For example, the US Navy was supplying a million replacement electronic parts a year to support 16000 pieces of equipment. The active electronic components, vacuum tubes, were the chief source of equipment failure. The tube was the most unreliable component with a five times replacement rate compared to all other components [22, 23]. The urgent reliability improvement requirements stimulated various studies to improve the reliability of electronic components, equipment, and systems. The research efforts in the 2nd decade resulted in five important conclusions [23]:

1. Better field reliability data need to be collected.
2. Component quality needs to be improved.
3. Quantitative reliability requirements need to be established.
4. Reliability needs to be verified by test before full-scale production.
5. A permanent committee needs to be established to guide the reliability discipline.

The last conclusion helped to establish the Advisory Group on Reliability of Electronic Equipment (AGREE). The AGREE committee aimed to improve electronic equipment reliability by providing consultancy to government and companies,

implementing reliability education programs, and developing reliability standards. This time period was the advent of reliability engineering discipline and the blossom of the reliability research in academia. Some pioneering and important work and events could be summarized below:

- The IRE transactions on reliability and quality control was published and evolved to *IEEE Transactions on Reliability*.
- The famous Weibull distribution was published in the Journal of Applied Mechanics resulting statistical techniques blossom.
- Reliability Analysis Center (RCA) released TR-1100, *Reliability Stress Analysis for Electronic Equipment*, which was the predecessor of the well-known US Military Handbook 217 (MH-217).

In 1965, US Military Handbook-217 version A was published by the US Navy. This formal first version, MH-217A quickly became the standard of reliability analysis as it was often cited in contractual documents [19].

In the early 1970s, the responsibility for preparing MH-217 was transferred to Rome Air Development Center (RADC), who published revision B in 1974. MH-217 was updated to reflect the technology at that time, but there were few efforts that changed the manner in which predictions were performed. In the mathematics community, redundancy modeling became a popular theoretical research topic, resulting in Bayes statistics and Markov Chain models. In the meantime, another branch of reliability discipline: Physics-of-Reliability (PoF), which focused on the discovery of failure mechanisms and processes, started the first symposium on "Physics of Failure In Electronics" sponsored by RADC. This symposium later became the "International Reliability Physics Symposium (IRPS)". The electromigration, corrosion, and electrostatic discharge are identified as the critical failure mechanisms in that day and they are still widely accepted in microelectronic reliability modeling.

In the 1980s, other agencies were also developing reliability models unique to their industries. For example, the Society of Automotive Engineers (SAE) Reliability

Standards Committee developed a set of models specific to automotive electronics. The Bellcore reliability-prediction standard is another example of a specific industry developed methodology. It was originally developed by modifying MH-217 to better reflect the interests in telecommunication industry. Fault tolerance at system-level which permits continued operation after failures was first proposed by military users. Another reliability initiative launched by US Department of Defense (DoD) is called STARS (software technology for adaptable reliable systems) which starts an individual path for software reliability development from that day.

In the 1990s, it soon became clear that the emerging discipline was using several different methods to achieve high reliability. One was the root cause identification of field failure and the determination of mitigation measures. Another was the quantitative reliability assessment. The debate on the direction of reliability research happened between the advocates of Physics of Failure methods and the supporter of failure rate methods. This debate is still ongoing today. A subsequent important event is that the US Army officially gave up maintenance on MH-217, and they ceased the document update. But the F version of MH-217 published in 1995 is still widely used today. On the other hand, PoF method has been extensively applied to microelectronics at that time. Many kinds of failure mechanisms, lifetime models were studied. However, there is no universal formula for all applications as the failure process is a comprehensive result of multidisciplinary mechanisms.

In 2010, there was an attempt to update MH-217F to a 'G' version [24]. Unfortunately, it was still hard to achieve agreement between the two branches of reliability modeling methods, resulting 'G' version update failed. The European FIDES method and the RIAC 217-PLUS method tried to enhance MIL-217F with PoF techniques. The related effort was quite welcome in academia. However, recent surveys show that MIL-217F is still preferable in industry. Another research direction proposed to shift reliability studies to a multi-physics simulation and test based discipline, in which advanced and more sophisticated PoF methods were used. The compromise between practicability and accuracy is always difficult in developing reliability modeling methods.

2.3 Reliability Modeling Methods

2.3.1 Reliability Fundamentals

A hypothetical example of 1000 identical equipment test is used to show the development of reliability and its key concepts. Table 2.1 shows the recorded equipment failures data with a 100 hours time interval. The failure data of the equipment are purely hypothetical for illustrative purpose.

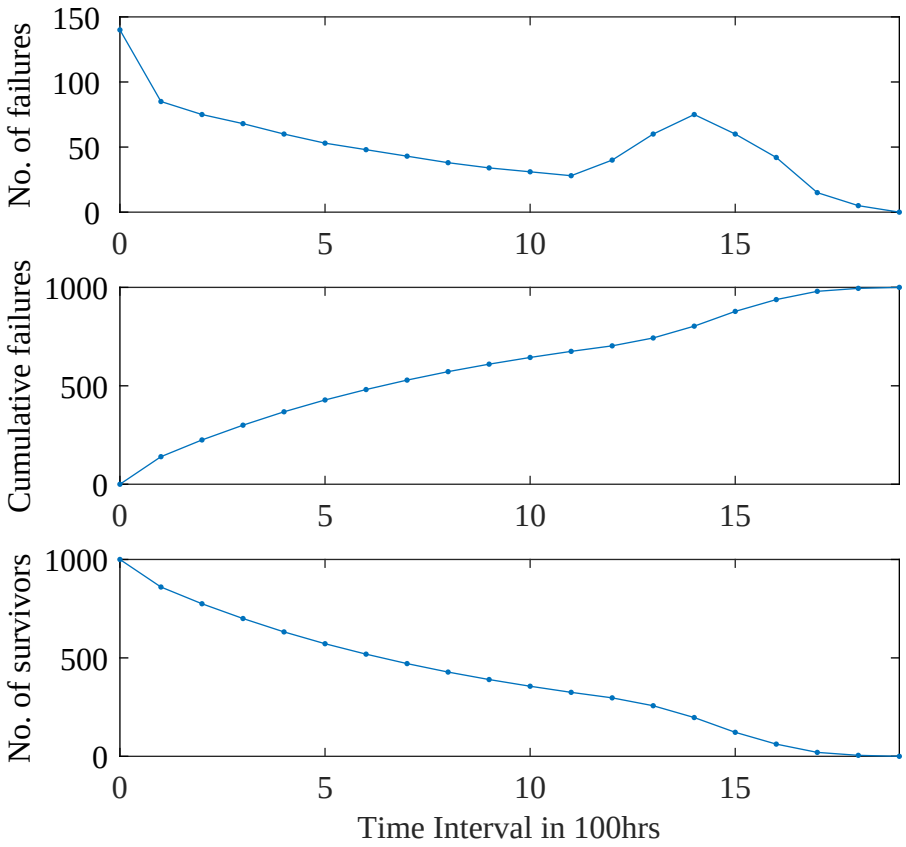


Figure 2.2. Recored reliability data of the hypothetical example

The full recorded failure and survivor data are plotted in Fig. 2.2. The last curve depicts the number of surviving equipment over time. The probability of a

Table 2.1. Recorded reliability data for a hypothetical example

Interval	No. of failures	Cumulative failures	No. of survivors
0	140	0	1000
1	85	140	860
2	75	225	775
3	68	300	700
4	60	368	632
5	53	428	572
6	48	481	519
7	43	529	471
8	38	572	428
9	34	610	390
10	31	644	356
11	28	675	325
12	40	703	297
13	60	743	257
14	75	803	197
15	60	878	122
16	42	938	62
17	15	980	20
18	5	995	5
19	0	1000	0

new equipment in good state during a specified time period can be estimated with the percentage of surviving equipment as:

$$Probability \approx \frac{Number\ of\ surviors}{Number\ of\ test\ equipment} \tag{2.1}$$

Reliability, $R(t)$, can be defined as the above probability and its value can be

estimated by the percentage of survivors over time.

Definition 2.1. Reliability is the probability of a device performing its purpose adequately for a period of time under specific operation conditions [25].

It is generally assumed that the equipment is in good state at the beginning and has a limited lifetime, i.e., at $t = 0$, $R(t) = 1$ and at $t \to \infty$, $R(t) = 0$.

With the full recorded failure and survivor data for the 1000 equipment test, three reliability related curves are shown in Fig. 2.2, and the corresponding concepts are defined as follows:

Definition 2.2. Unreliability is the failure probability of a device in a period of time under specific operation conditions.

Unreliability is a complementary probability to reliability. It can be directly calculated as: $F(t) = 1 - R(t)$, where $F(t)$ represents unreliability and $R(t)$ is reliability.

Definition 2.3. Failure density $f(t)$ is the derivative of unreliability $F(t)$.

Failure density, unreliability, and reliability functions for the 1000 equipment test are plotted with blue color in Fig. 2.3. And the test data can be curve-fitted with established mathematical functions in statistics. The Weibull distribution is widely used in reliability for lifetime data analysis for its versatility. Weibull function fitting results for the 1000 equipment test data are shown in Fig. 2.3 with red color.

Both the reliability function and failure density function are calculated with the initial number of test equipment. For manufactures screening test before mass production, the initial number of equipment is straightly available. But consumers or end-users may only have one equipment, or have a constant number of operating equipment with regular replacements. It is not always possible for them to maintain a complete database of the equipment. Additional issue is the complex mathematical functions are not easy to use in practice.

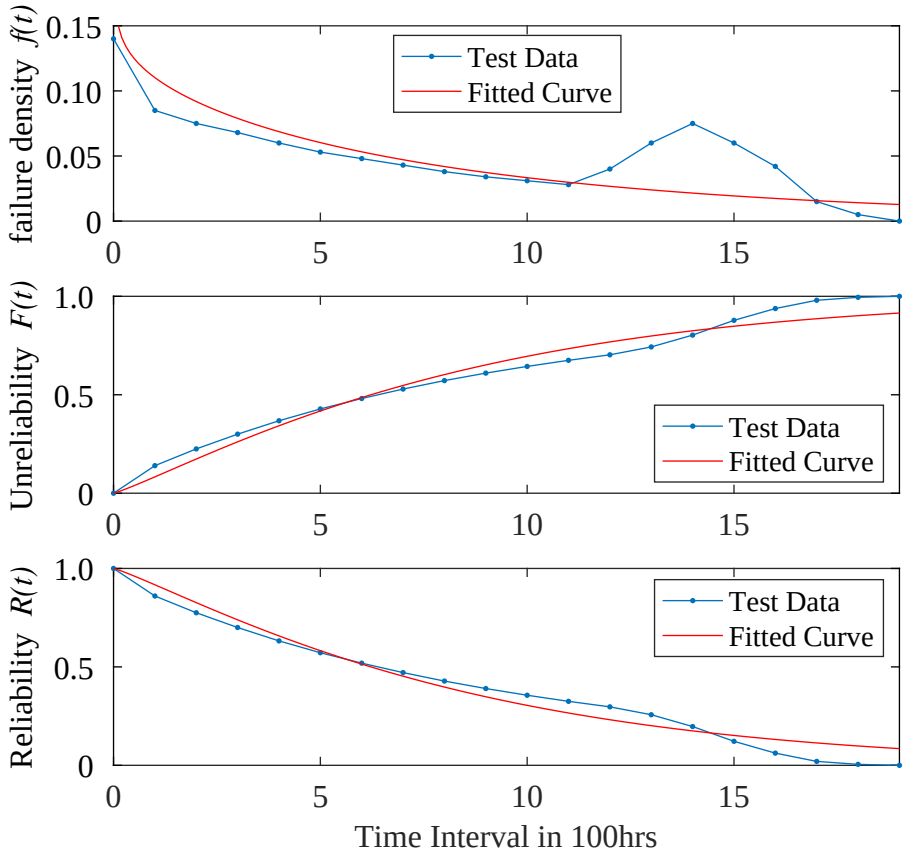


Figure 2.3. Reliability functions extracted from the hypothetical example

A simple characteristic value is needed to represent the reliability performance of an equipment. The failure rate, a.k.a, hazard rate, is usually used in reliability analysis. Failure rate λ is defined as the ratio of failures per time to the survivors at the beginning of time interval.

$$\lambda(t) = \frac{number\ of\ failures\ per\ unit\ time}{number\ of\ components\ exposed\ to\ failure} \tag{2.2}$$

Unlike failure density functions calculated with respect to initial number in the denominator, failure rate functions are calculated with respect to the number of survived equipment.

The formal definition of failure rate in IEC (International Electrotechnical

Commission) standard IEC-60050(191) is as below:

Definition 2.4. Failure rate is the limit, if it exists, of the quotient of the conditional probability that the instant of a failure of a non-repaired item falls within a given time interval $(t, t + \Delta t)$ and the duration of this time interval, Δt, when Δt tends to zero, given that the item has not failed up to the beginning of the time interval [26].

The mathematical expression of failure rate is as follows:

$$\lambda(t) = \lim_{\Delta t \to 0} \frac{1}{\Delta t} \frac{F(t + \Delta t) - F(t)}{R(t)} = \frac{f(t)}{R(t)} \tag{2.3}$$

where $F(t)$, $R(t)$ and $f(t)$ are respectively the unreliability function, reliability function, and the failure density function of the equipment [26]. It should be careful to distinguish failure density and failure rate: failure density is the ratio of failures per unit time over the initial number of equipment while failure rate λ is the ratio of failures per unit time over survivors. Failure density and failure rate have the same unit. In power system, failures/hour or failures/year are two most common units. For power electronics components, devices, and equipment, the Failures in Time (FIT) is the typical failure rate unit. 1 FIT is 1 failure/10^9hours.

Fig. 2.4 shows the failure rate function calculated from the 1000 equipment test failure data. There are three segments in the bathtub-shaped failure rate curve, an initial stage with a decreasing trend, an approximately constant middle part, and an exponentially increasing ending.

Although different equipment may have different failure rate functions, the shapes of the failure rate functions are similar to the bathtub curve. An idealized failure rate function is depicted in Fig. 2.5.

The failure rate bathtub curve can be divided into three periods. The infant mortality period in which the failure rate decreases over time. This failure rate stabilizes at time t_1 when the manufacture debugging process finished. In the useful life period, the failure rate is often characterized by a constant value. The failure rate increases dramatically over time as devices are going into the wear-out phase.

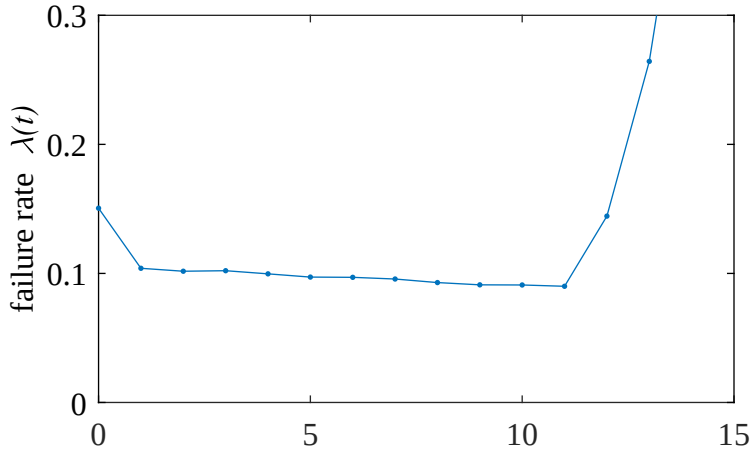


Figure 2.4. Failure rate extracted from the hypothetical example

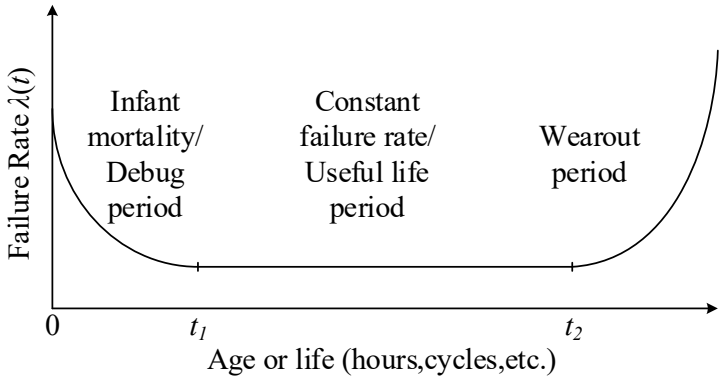


Figure 2.5. The bathtub curve of failure rate

In practice, the constant failure rate is usually used to represent the reliability performance by manufacturers and end-users. This is due to the debug period are usually prior to equipment shipment and replacement schedules are usually before equipment wear-out.

The constant failure rate describes the failure probability of an equipment in unit time, i.e., $\lambda \cdot \Delta t$ is the failure probability for an equipment in next time period of Δt. The failure rate is a failure probability related index for manufacturers and consumers. An expected service life is also a useful and intuitive way to show the

reliability performance. The widely used time-related reliability index is the Mean Time To Failure (MTTF).

Definition 2.5. Mean Time To Failure (MTTF) is the expected value of the equipment lifetime t.

In statistic theory, the equipment lifetime t is a random variable following a certain probability distribution, and the failure density function is the probability density function of the random variable t. Hence, MTTF can be calculated as:

$$MTTF = E(t) = \int_0^\infty t f(t)\, dt \tag{2.4}$$

In the case of an exponential distribution which implies a constant failure rate, the MTTF is the reciprocal of the failure rate λ. Therefore, with the assumption of constant failure rate, the reliability performance can be easily compared with either MTTF or λ. In practice, the failure rate function is easy to obtained and the other reliability functions and indexes can be calculated accordingly.

With a general failure rate function $\lambda(t)$, the reliability function can be derived as follows:

By definition of failure rate in equation (2.3),

$$\lambda(t) = \frac{f(t)}{R(t)} \tag{2.5}$$

By definition of failure density function, derivative of unreliability

$$f(t) = \frac{dF(t)}{dt} \tag{2.6}$$

With $R(t) = 1 - F(t)$, equation (2.6) can be rewritten as:

$$f(t) = -\frac{dR(t)}{dt} \tag{2.7}$$

Substituting equation (2.7) into equation (2.5) gives:

$$\lambda(t) = -\frac{dR(t)}{dt}\,\frac{1}{R(t)} \tag{2.8}$$

Solving the differential equation (2.8) gives

$$R(t) = e^{-\int_0^t \lambda(t)\,dt} \tag{2.9}$$

The equation (2.9) is the reliability function for a general failure rate function. With reliability function obtained, the unreliability and failure density function can be easily obtained. The MTTF can also be calculated as:

$$MTTF = \int_0^\infty R(t)\,dt \tag{2.10}$$

The equation (2.10) can be derived as follows:

By $MTTF$ definition in equation (2.4),

$$MTTF = \int_0^\infty tf(t)\,dt \tag{2.11}$$

Integration by parts, i.e., $\int_a^b uv'dt = [uv]_a^b - \int_a^b u'vdt$ and $[-R(t)]' = f(t)$:

$$\begin{aligned} \int_0^\infty tf(t)\,dt &= [-R(t)t]|_0^\infty - \int_0^\infty -R(t)\,dt \\ &= \int_0^\infty R(t)\,dt \end{aligned} \tag{2.12}$$

For a constant failure rate λ, reliability function and MTTF in equation (2.9) and equation (2.10) are simplified as follows:

$$R(t) = e^{-\lambda t} \tag{2.13}$$

$$MTTF = \frac{1}{\lambda} \tag{2.14}$$

Another lifetime related reliability index, percentiles of lifetime, B_α, is defined as the time at which α percent of equipment fail [27].

$$F(B_\alpha) = \frac{\alpha}{100} \tag{2.15}$$

$$B_\alpha = \frac{1}{\lambda}\ln\left(\frac{100}{100-\alpha}\right) \tag{2.16}$$

For a system contains a set of components, the system reliability function can be calculated based on probability theory and network techniques. There are two basic network structures in reliability: series systems and parallel systems.

Definition 2.6. Series systems in reliability point of view are systems in which all component are required to be in a good state for systems normal operation.

Definition 2.7. Parallel systems in reliability point of view are systems in which all component must fail for system failure.

By definition, the reliability function for a series system can be calculated as:

$$R_s(t) = \prod_{1}^{n} R_i(t) \tag{2.17}$$

And the unreliability function for a parallel system can be calculated as:

$$F_p(t) = \prod_{1}^{n} F_i(t) \tag{2.18}$$

where $R_s(t)$ is the series system reliability function

$R_i(t)$ is i^{th} component reliability function

λ_i is i^{th}component failure rate

$F_p(t)$ is the parallel system unreliability function

$F_i(t)$ is i^{th}component failure rate

For a series system, an equivalent system failure rate is defined as

$$\lambda_s = \sum_{1}^{n} \lambda_i \tag{2.19}$$

The series system reliability and MTTF can be calculated as:

$$R_s(t) = e^{-\lambda_s} \tag{2.20}$$

$$MTTF_s = \frac{1}{\lambda_s} \tag{2.21}$$

For parallel systems, the reliability function $R_p(t)$ is $R_p(t) = 1 - F_p(t) = 1 - [1 - R_1(t)][1 - R_2(t)] \cdots [1 - R_n(t)]$. It can not be expressed as a monomial, hence MTTF cannot be expressed in a simple monomial. Even all components reliability functions are the same, i.e., $R_1(t) = R_2(t) = \cdots = R_n(t)$, the equivalent system failure rate is still a time-varying function.

2.3.2 Failure Rate Methods

The most widely used reliability modeling method in the industry is the US Military Handbook-217 (MH-217) standard. The latest version "F" was released at 1991. After the minor revision in 1995, the MH-217F standard ceased to release a new version. Although there were efforts to revise the MH-217F [28], it was hard to make a trade-off between simplicity and accuracy [29]. There are also some other standards in the industry, such as Bellcore/Telcordia, IEC61709, and Handbook-217Plus [30, 31].

As most standards originated from MH-217F, only the methods in MH-217F are introduced in this thesis. There are two methods in the standard. One is 'parts count' which is suitable in the early design phase, the other is 'part stress' which is applicable when most of the design is complete and a detailed parts list including part stresses is available. The parts count method assumes typical operating conditions of part complexity, ambient temperature, various electrical stresses, operation mode and environment (i.e., reference conditions) [32].

The assumptions for the parts count and part stress methods are listed as follows:

- all components have constant failure rates
- all components are connected in series from reliability point of view

Parts Count:

$$\lambda_s = \sum_{1}^{n} \lambda_i \pi_{Qi} \tag{2.22}$$

where λ_s is the system equivalent failure rate

λ_i is the i^{th} component failure rate

π_{Qi} is the i^{th} component quality factor

n is the number of components

Part Stress:

$$\lambda_s = \sum_{1}^{n} \lambda_{pi} = \sum_{1}^{n} (\lambda_{bi} \prod_{1}^{m} \pi_j) \tag{2.23}$$

where λ_s is the system equivalent failure rate

λ_i is the i^{th} component failure rate

π_j is the j^{th} π factor

n is the number of components

m is the number of π factors The difference between the two methods is that the 'part stress' model takes more factors into consideration to modify each component's failure rate. This modification makes the model more accurate as the actual operating conditions are considered. The values of π factors are obtained from empirical formulas. The formulas of π factors are specified for different components. The quality factor is assumed to be unity.

It is obvious to find the problems of reliability modeling methods in the standards:

- redundancy is not modeled
- component failure rate may increase in the end of life
- failure root causes are unknown for users

Although the reliability modeling methods in MH-217F have some problems, they are still widely accepted in power electronics industry. The application of MH-217F in power converter reliability modeling will be introduced briefly.

There are mainly two critical categories of components in power converters, namely power semiconductors and capacitors. The wires, inductors, PCB, mechanical case, and so forth, can be ignored due to their much higher reliability and lower

failure rate compared to power semiconductors and capacitors. For power converter reliability modeling in design phase, only the main power circuit will be considered. The base failure rate data are cited from the datasheet and published literature available. Once the base failure rate data are obtained, the actual failure rate for power semiconductors, diode, IGBT, MOSFET, etc. and aluminum electrolytic capacitors can be determined based on empirical models and actual stresses in the design. Then the power converter equivalent failure rate is simply the summation of all critical components failure rate. The reliability functions can be calculated with techniques in subsection 2.3.1: Reliability Fundamentals. The π factors for the three critical components are listed below.

Diode:

$$\lambda_p = \lambda_b \pi_T \pi_S \pi_C \pi_E \tag{2.24}$$

where λ_p is the device equivalent failure rate

λ_b is the component base failure rate

π_T is the temperature factor

π_S is the electric stress factor

π_C is the contact construction factor

π_E is the environment factor

$$\pi_T = e^{-3091(\frac{1}{T_j+273}-\frac{1}{298})} \tag{2.25}$$

$$\pi_S = \begin{cases} 0.054 & V_S \leq 0.3 \\ V_S^{2.43} & 0.3 < x \leq 1 \end{cases} \tag{2.26}$$

where T_j is junction temperature

V_S is ratio of applied voltage to rated voltage

$$\pi_C = \begin{cases} 1.0 & \text{metallurgically bonded} \\ 2.0 & \text{non-metallurgically bonded} \end{cases} \tag{2.27}$$

$$\pi_E = \begin{cases} 1.0 & G_B : \text{Ground Benign} \\ 6.0 & G_F : \text{Ground Fixed} \\ 9.0 & G_M : \text{Ground Mobile} \\ 9.0 & N_S : \text{Naval Sheltered} \\ 19 & N_U : \text{Naval Unsheltered} \end{cases} \tag{2.28}$$

IGBT:

$$\lambda_p = \lambda_b \pi_T \pi_S \pi_A \pi_R \pi_E \tag{2.29}$$

where λ_p is the device equivalent failure rate

λ_b is the component base failure rate

π_T is the temperature factor

π_S is the electric stress factor

π_A is the application factor

π_R is the power rating factor

π_E is the environment factor

$$\pi_T = e^{-2114(\frac{1}{T_j+273} - \frac{1}{298})} \tag{2.30}$$

$$\pi_S = 0.045\, e^{3.1 V_S} \tag{2.31}$$

$$\pi_A = \begin{cases} 0.7 & \text{Switching} \\ 1.5 & \text{Linear Amplification} \end{cases} \tag{2.32}$$

$$\pi_R = P_r^{0.37} \tag{2.33}$$

where P_r is rated power and environment factor

π_E is the same as diode

Capacitor:

$$\lambda_p = \lambda_b \pi_T \pi_C \pi_V \pi_{SR} \pi_E \tag{2.34}$$

where λ_p is the device equivalent failure rate

λ_b is the component base failure rate

π_T is the temperature factor

π_C is the capacitance factor

π_V is the voltage stress factor

π_{SR} is the series resistance factor

π_E is the environment factor

$$\pi_T = e^{-4062(\frac{1}{T_j+273}-\frac{1}{298})} \tag{2.35}$$

$$\pi_C = C^{0.23} \tag{2.36}$$

$$\pi_V = (\frac{S}{0.6})^5 + 1 \tag{2.37}$$

$$\pi_{SR} = \begin{cases} 0.66 & 0.8 < CR \\ 1.0 & 0.6 < CR \leq 0.8 \\ 1.3 & 0.4 < CR \leq 0.6 \\ 2.0 & 0.2 < CR \leq 0.4 \\ 2.7 & 0.1 < CR \leq 0.2 \\ 3.3 & 0 < CR \leq 0.1 \end{cases} \tag{2.38}$$

$$\pi_E = \begin{cases} 1.0 & G_B : \text{Ground Benign} \\ 10 & G_F : \text{Ground Fixed} \\ 20 & G_M : \text{Ground Mobile} \\ 7.0 & N_S : \text{Naval Sheltered} \\ 15 & N_U : \text{Naval Unsheltered} \end{cases} \tag{2.39}$$

where S is the ratio of operating peak voltage to rated voltage

C is the capacitance in μF

CR is the ratio of effective resistance to peak voltage

Although failure rate methods are easy to use, there is no information on the cause of failure, and MTTF is a pure mathematical expectation. It is a probability-weighted average value without any engineering meaning. Sometimes, MTTF is misleading as it is higher than most equipment lifetime in operation. For example, the reliability at $t = MTTF$ can be calculated as follows:

With $\lambda = \frac{1}{MTTF}$

$$R_{MTTF} = e^{-\lambda \cdot MTTF} = e^{-1} = 36.78\% \tag{2.40}$$

Equation 2.40 indicates that, for a set of equipment under test, only 36.78% equipment are survived at time $t = MTTF$. MTTF gives an 'exaggerated' lifetime expectation to consumers, which may be condemned as an unconvincing reliability index. In contrast, the Physics of Failure methods allow engineers to estimate the remaining useful lifetime for consumers more accurately.

2.3.3 Physics of Failure Methods

Physics of Failure (PoF) method is a structural approach to root-cause wear-out failure analysis. It has a premise of 'cause and effect', which assumes any failure has some causes. To analyze failure causes, materials science, physics, chemistry and probabilistic mechanics should all be involved. PoF methods attempt to model failure mechanisms deterministically, as opposed to a traditional approach of using statistical models based on empirical data. PoF techniques can be very effective for estimating useful lifetime. This lifetime can be quantified as the end of useful lifetime or the beginning of wear-out periods shown in the failure rate bathtub curves at t_2 in Fig. 2.5.

An aluminum crank arm is used as an example to explain the PoF method for simplicity. There are two failure mechanisms of the crank arm: brittle fracture and fatigue fracture. Fig. 2.6 shows a zoomed-in cross-section view of a failed crank arm. In cross-section view, two distinct areas reflect tow failure mechanisms, where

Figure 2.6. Cross-section of a failed aluminum crank arm

the dark area is caused by fatigue fracture and bright area is the effect of brittle fracture [33]. The theoretical strength of a crystalline material can be estimated as [34]:

$$\sigma_{theoretical} = \sqrt{\frac{E\gamma}{r_o}} \tag{2.41}$$

where E is the Young's modulus of the material, γ is the surface energy, and r_o is the equilibrium distance between atomic centers.

The maximum strength can be calculated by theoretical equations or by a practical experiment test. In this crank arm example, the Ultimate Tensile Strength (UTS) of the aluminum is 320 Mpa, which is the maximum strength of aluminum crank arm. Once a load-induced stress excess the UTS, the crank arm will fail instantly. This acute failure is usually avoided by specifying a safe operating limit and employing overstress protection.

On the other hand, in crank arm daily operation, much lower normal loads only cause very tiny cracks. The tiny cracks accumulate day by day. After a long time

of fatigue accumulation, the crank arm will fail eventually. The lifetime model of the aluminum material can be obtained by accelerated experiments with different constant load stresses. The consumed lifetime and the remaining useful life can be calculated deterministically with the lifetime model and actual load stress profiles.

A stress-cycle curve for the aluminum can be obtained by repetitive accelerated tests. In each test, a regular periodic stress is applied to the aluminum bar. The number of cycles is recorded when the aluminum bar fails. The life expectancy is the product of number and period of the test stress cycles. In an accelerated test, the period of stress cycle is reduced significantly to shorten the test time. With a set of cyclic stress test data, the analytical lifetime model can be extracted by curve-fitting.

A typical aluminum cycle versus stress curve (N-S curve) is shown in Fig. 2.7. The dots in the blue line are test data points. A smooth connected blue line can be used to estimate expected cycle to failures under various load stresses by interpolation. The red line is a polynomial curve fitting result. The fitted function is easy for analytical reliability modeling. In this example, a third order polynomial is used to represent the lifetime model on stress.

$$\log_{10} N = -9.5147 \times 10^{-7} S^3 + 6.0447 \times 10^{-4} S^2 - 0.1427 S + 15.0024 \qquad (2.42)$$

where N is the expected cycle to failure and S is the stress amplitude. The lifetime model in equation (2.42) gives the relationship between expected cycle to failure and stress amplitude. The expected cycle to failure denotes the maximum cycles that the material can withstand. For a given constant amplitude stress, the corresponding expected cycle to failures can be calculated.

A case study is conducted to demonstrate the PoF method. A hypothetical load stress profile is exerted on the crank arm as shown in Fig. 2.8.

In the 10s irregular load stress profile, there are several different sinusoidal stresses with varying amplitude and period. To analyze the damage on the crank arm caused by the load stress, a cycle counting method is needed to quantify stresses with different amplitudes. In this hypothetical case study, the stress cycles

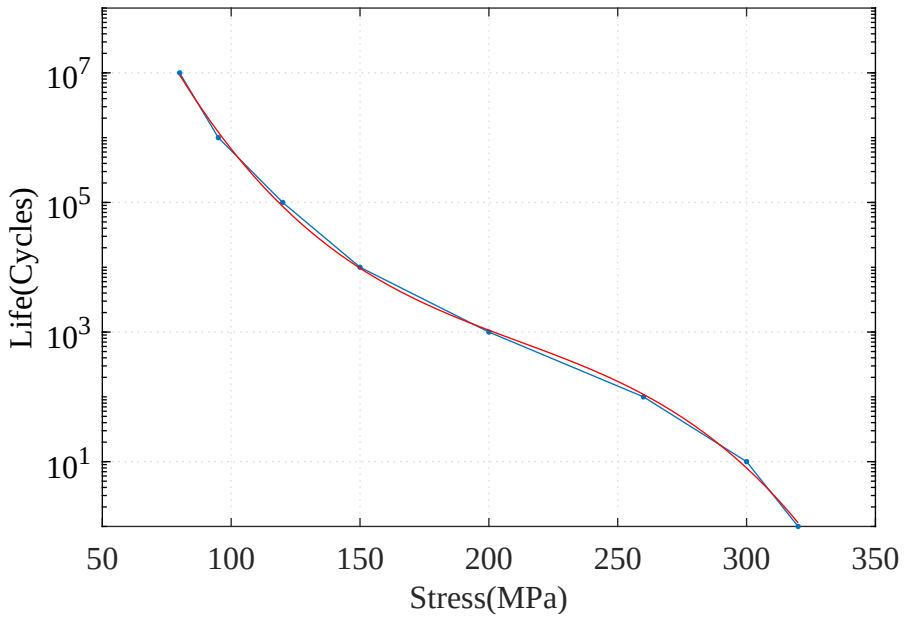


Figure 2.7. Stress-cycle curve for aluminum

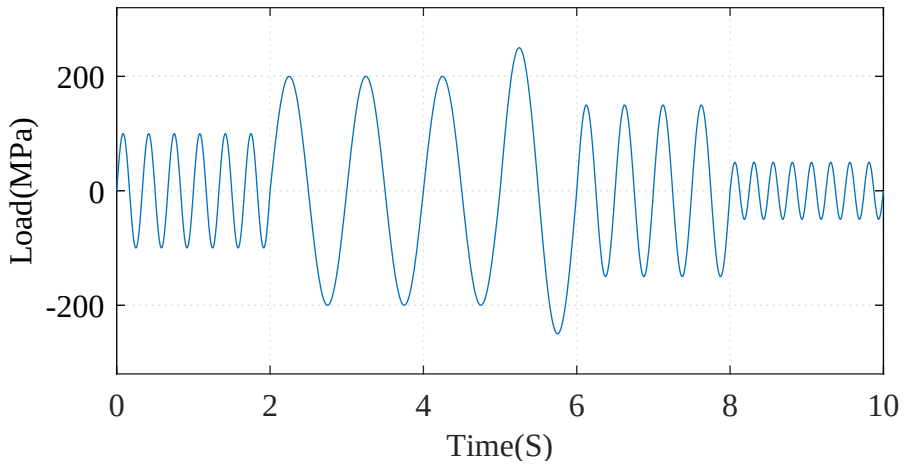


Figure 2.8. A hypothetical load stress profile

can be classified and counted by observation. The counting results are shown by the histogram in Fig. 2.9.

For i^{th} stress, the stress cycle shown in Fig. 2.9 is denoted as n_i. The expected cycle to failure calculated from lifetime model in equation (2.42) is denoted as

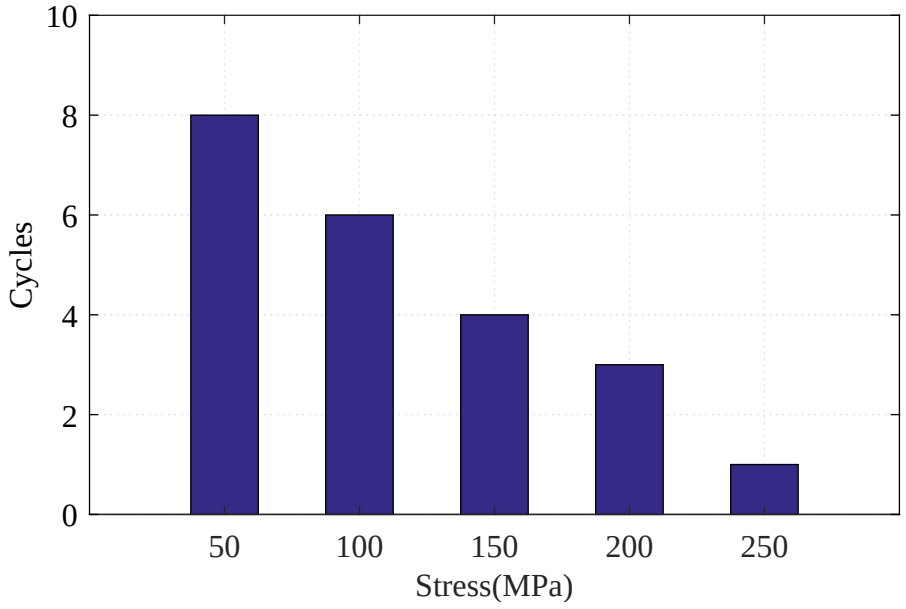


Figure 2.9. Stress cycles counting results

N_i. For example, the 3^{rd} stress in the histogram is 200Mpa. There are 3 cycles of 200Mpa in the hypothetical load stress profile. The expected cycle to failure calculated by equation (2.42) is 1070. It indicates that the 3 cycles only cause a 0.28% damage on expected cycle to failure. The damage caused by each stress is denoted as the life consumed. The life consumptions of all stresses are calculated and plotted in Fig. 2.10

With the life consumptions obtained in Fig. 2.10, the total life consumption under the assumed load stress profile can be calculated with a linear accumulation as,

$$L_C = \sum_{i=1}^{k} \frac{n_i}{N_i} \tag{2.43}$$

For the hypothetical load stress profile, the total life consumption is 0.9%, and the load period is $10s$. The expected useful lifetime will be $\frac{1}{0.9\%} \cdot 10 = 1111s$

With an actual load stress profile, the actual life consumptions can be calculated similarly. If the load stress profile is repeated within a given period, the life

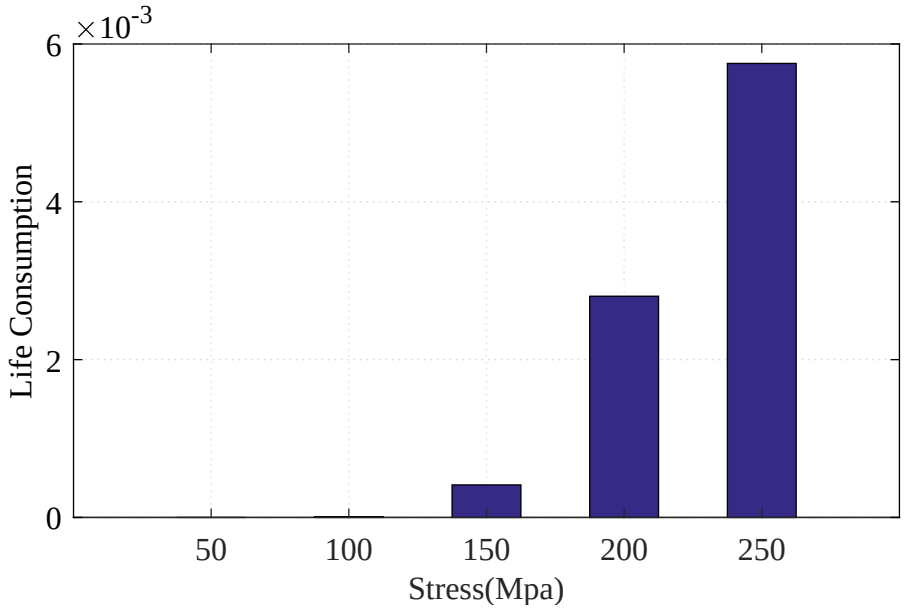


Figure 2.10. Life consumption of stress cycles

expectancy can be predicted accordingly.

In mechanical equipment, stresses are mainly mechanical and thermal cycling. For power electronic devices, voltage and current are the two apparent stresses. Voltage stresses act on insulation materials. Insulation breakdown failure is similar to the brittle fracture failure of crank arm, which are avoided by design with enough margin. For example, a 1200 V IGBT device usually operates at a 600 V DC link voltage. Short circuit and overloading are two main acute failures caused by current stresses. Devices usually explode in a short time due to the thermal runaway. These acute voltage and current over-stressing failures are avoided by proper design to ensure devices working in Safe Operation Area (SOA).

The PoF methods for power electronics mainly focus on fatigue failures induced by long-term normal load. In power converters PoF modeling, there are multiple failure mechanisms in component level, package level, and Printed Circuit Board (PCB) level. It is a challenge to include all failure mechanisms of the complex power converter system with limited failure mechanism models available [4].

In practice, the PoF method focuses on the failure mechanisms modeling and analysis of critical components. The critical components normally refer to power semiconductors and DC-link capacitors as they are the most vulnerable components in terms of failure rate [17, 18]. The main stresses of power semiconductors can be classified as electrical stresses and mechanical stresses. The electrical stress limits are specified by the SOA in datasheet. The mechanical stresses are caused by temperature cycling and mismatch of Coefficient of Thermal Expansion (CTE) between adjacent layers. The most common failure mechanisms of power semiconductors are Die-attach solder fatigue and bond wire lift-off, both of which are caused by thermo-mechanical stresses during operation [35].

Fig. 2.11 shows a power semiconductor module, bond wire crack failure, and solder fatigue failure.

Figure 2.11. Power semiconductor module, a cracked bond wire, and solder fatigue

Figure 2.12 is the cross section view of an IGBT power module. The CTE of materials for each layer are listed in Table 2.2.

The largest CTE mismatch are among the top three layers, bond wire (22ppm/ °C), Die (3ppm/ °C), and solder (28ppm/ °C). The temperature of the top three layers will fluctuates during the switching operation of a power module. Within a temperature cycle, the deformations of the three layers differ significantly. The different mechanical deformations yield shear strains on the materials of high CTE. Consequently, the two weak points are bond wire and solder as they have much higher CTE compared to their adjacent layer, i.e., the silicon die.

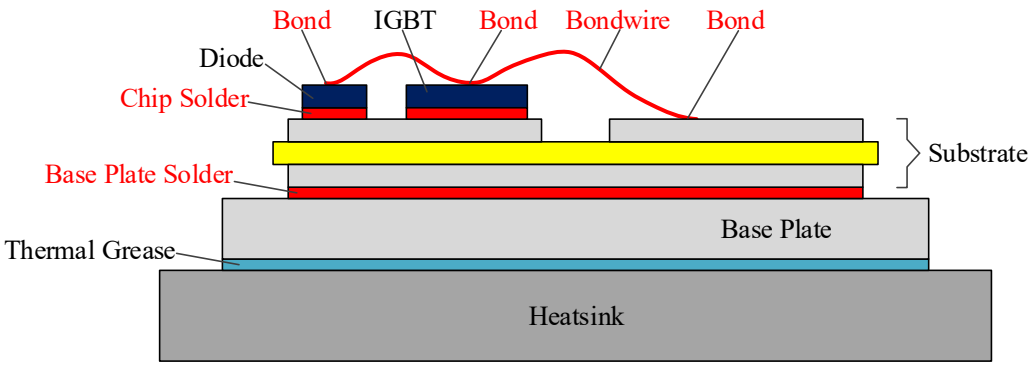


Figure 2.12. Inner structure layers diagram of a power semiconductor module

Table 2.2. Coefficient of thermal expansion for inner layers of a power semiconductor module

Layer	Material	CTE (ppm/ °C)
Bond wire	Aluminum	22
Die	Silicon	3
Die-attach solder	SnAg(3)	28
DCB-copper	Copper	17.5
DCB-ceramic	Al_2O_3 or AlN	7 or 4
DCB-copper	Copper	17.5
DCB-solder	SnAg(3)	28
Baseplate	Copper or AlSiC	17.5 or 8

The analytic lifetime model of the power module due to bond wire fatigue failure can be derived as follows:

The stress on the aluminum bond wire caused by temperature fluctuation can be calculated as [34]

$$S = \frac{L}{h}(\alpha_{Al} - \alpha_{Si})\Delta T_j \tag{2.44}$$

where l and h are the length and thickness of the bond heel respectively, α_{Al}

and α_{Si} are the CTE of aluminum and silicon respectively. All these parameters are constants. ΔT_j is the junction temperature fluctuation amplitude.

For the aluminum material, an analytical lifetime function with respect to stress is presented in equation (2.42). To simplify the model, high-order terms in equation (2.42) with tiny coefficients are ignored. A simplified lifetime equation can thus be expressed as,

$$N = a \times S^{-b} \tag{2.45}$$

Substituting equation (2.44) into equation (2.45) gives

$$N = a[\frac{l}{h}(\alpha_{Al} - \alpha_{Si})]^{-b} \times (\Delta T_j)^{-b} \tag{2.46}$$

Representing the first term with a new parameter $A = a[\frac{l}{h}(\alpha_{Al} - \alpha_{Si})]^{-b}$ to simplify the lifetime model form

$$N = A \times (\Delta T_j)^{-b} \tag{2.47}$$

Equation 2.47 is the well-know Coffin-Manson model which is usually used for lifetime estimation due to fatigue failure [36]. The Coffin-Manson model only consider temperature swings regardless of the mean operation temperature. A modified Coffin-Manson with an Arrhenius term which models the effect of mean temperature on device lifetime is expressed as [36],

$$N = A \times (\Delta T)^{-b} \times e^{E_a/(k_B \cdot T_m)} \tag{2.48}$$

where T_m is mean temperature of a temperature swing in Kelvin temperature scale with K as the unit, k_B is Boltzmann constant and E_a is activation energy. The Arrhenius term comes from the Arrhenius equation which gives the dependence of the chemical reaction rate on the absolute temperature. The Arrhenius term models the material strength deterioration on high temperature. The parameters and the coefficients in equation (2.48) can be obtained by numerical simulation or experiment test. There are also other modification terms added by researchers to improve the accuracy of the lifetime model. As many modifications are application

dependent, the specific lifetime model will be introduced in a case study in the following chapters.

Two widely used lifetime model for capacitors are also shown as follows [37]:

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times e^{\frac{E_a}{k} \cdot (\frac{1}{T_c} - \frac{1}{T_0})} \tag{2.49}$$

$$L = L_0 \times (\frac{V}{V_0})^{-n} \times 2^{\frac{T_0 - T_c}{10}} \tag{2.50}$$

where T_c is the core temperature of a capacitor. L_0 is the lifetime under test with core temperature T_0 and voltage V_0. The two models are known as Law of Arrhenius and Law of 10 °C 2 times lifetime.

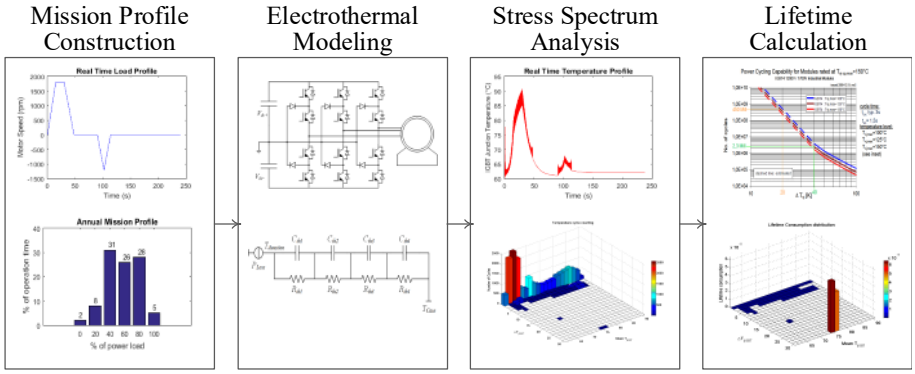


Figure 2.13. Flowchart of physics of failure analysis

Fig. 2.13 shows the flowchart of Physics-of-Failure reliability modeling of a converter. There are four steps of PoF reliability modeling method.

1. Mission Profile Construction

   The stresses are highly dependent on the mission profile. An actual mission profile is preferred to determine the load stresses. In some case, only the load distribution is available, a time domain mission profile needs to be reconstructed from limit data.

2. Electrothermal Modeling

   With a given mission profile, power components losses can be obtained from

the electrical simulation. The temperature profile can be calculated with the power converter losses and its thermal network model.

3. Stress Spectrum Analysis
   The temperature profile consists of lots of irregular cycles. Stress cycles counting should be conducted with a proper method. There are many cycle-counting methods, such as Level-crossing counting, Range-pair counting, and Rainflow counting. The Rainflow counting method is mostly used for its clear physical significance in stress impacts.

4. Lifetime calculation
   For each component, the lifetime consumption under the mission profile can be calculated with the stress cycles obtained. The reciprocal of the lifetime consumption is the expected number of same mission profile to be fulfilled in future. The expected component life can be calculated correspondingly. The converter lifetime is limited by the shortest component lifetime.

The failure rate methods focus on the power converter system level reliability prediction, while the Physics-of-Failure (PoF) methods aim to model the physical causes of component fatigue failure. Both methods are widely used in industry and academy to model and improve reliability. The PoF methods focus on improving reliability by stress reduction. The failure rate methods can improve reliability by redundant design and periodic preventative maintenance. Table 2.3 lists the pros and cons of the two methods.

There is always a trade-off between the usability and accuracy. The purpose of reliability modeling must be clearly understood before the selection of appropriate methods. In the design stage, a clear reliability index is needed for comparison purpose with limited operation data available, the failure rate methods are easy to use and the relative reliability index is also acceptable for comparison purpose. In the operation stage, the actual useful lifetime should be predict accurately. With abundant operation data, the PoF methods can estimate the state of health convincingly. The selection of reliability modeling methods also depends on different

Table 2.3. Comparison of reliability modeling methods

Methods \ Attributes	Pros	Cons
Failure Rate	actual failure data	unknown failure causes
	clear index	unknown useful lifetime
Physics of Failure	model failure mechanisms	hard to use
	accurate useful lifetime	hard to assess system

parties. For manufacturers, the failure rate methods are sufficient to calculate return rates and hence to determine warranty period. For consumers, the actual useful lifetime is the main concern, which could be addressed by PoF methods.

2.4 Reliability Based Multilevel Converter Topology Selection

The selection of the preferred converter topology is a complicated decision. Clearly, the topology must satisfy the basic performance requirements but a large number of converter topologies satisfy the basic requirements. For motor drive applications, the system reliability and life cycle costs are the key selection criteria.

Failure rate methods, used for decades in both industrial and military designs, have in recent years come under criticism [19]. Currently, PoF methods are advocated by researchers. However, it is difficult to apply such methods when only a circuit diagram is available, as is the case of topology selection [4]. In summary, methods to predict reliability, perhaps not surprisingly, continue to be of academic and industrial interest. The failure rate methods, despite its obvious limitations, is perhaps one of the only tools that are suitable for topology evaluation [38]. For this reason, the failure rate methods in the multilevel converter selection are discussed.

The objective of this section is to compare the reliability of six classical multilevel converter topologies. The Mean Time To Failure (MTTF) is selected as the reliability index to be compared. The 'part-counts' method in MH-217F are adopted in the initial design phase (topology evaluation). Once a preferred topology is selected, the detailed design specifications and operating conditions will be obtained. The 'part-stress' method is subsequently used for reliability improvement. The comparison will focus on a topology without considering the electronic controllers, gate drivers, and snubber circuits. The front-end diode-bridge rectifier will not be included in the evaluation as it is the shared part by the six topologies. A 6.7MW, 3.3kV/6.6kV motor drive application is used as the target design, on which components selection and topology comparison are based.

The six commonly used topologies in industry to be compared are:

- 3-Level Neutral Point Clamped Converter (3L-NPC)
- Neutral Point Clamped Converter-Open end Winding Motor (NPC-OWM)
- Cascaded Neutral Point Clamped Converter (CNPC)
- 5-Level Active Neutral Point Clamp Converter (5L-ANPC)
- Cascaded H-Bridge (CHB)
- Modular Multilevel Converter (MMC)

2.4.1 Neutral Point Clamped Converters

3-Level Neutral Point Clamped Converter

Fig. 2.14 is the topology of 3-Level Neutral Point Clamped Converter(3L-NPC). The 3L-NPC has been extensively studied since its invention in 1981 [39]. It is a mature topology with high efficiency and has been used in motor drive systems for over 20 years. The 3L-NPC is suitable for the DC-common bus distribution system

which is an emerging power distribution concept taking advantage of variable speed generation. The three phases in NPC share a common DC-link. In this structure, the DC-link capacitor can be smaller compared to that in a single phase topology. NPC also has several derivative version of topologies to increase their power ratings.

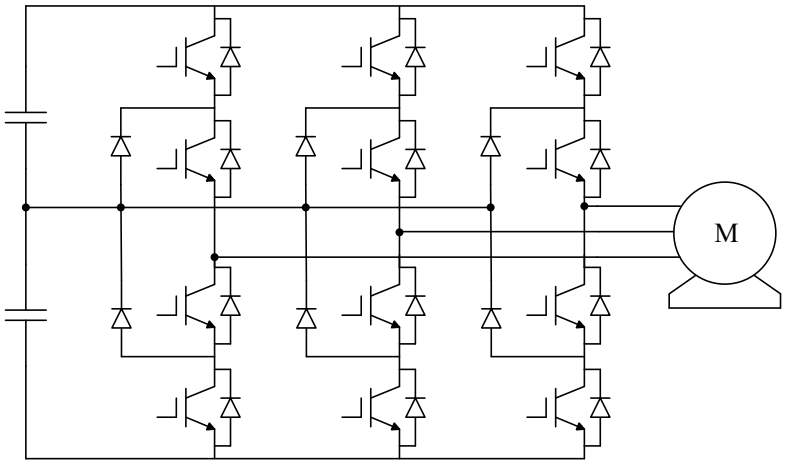


Figure 2.14. 3-Level Neutral Point Clamped Converter

For a 6.7MW, 3.3kV motor drive, to reserve a sufficient and proper margin, two IGBTs with current rating of 1000A could be connected in series at each phase to share load current of 1200A [40]. The film capacitors will be used as it is more reliable than aluminum electrolytic capacitors. A 5mF DC link capacitance is empirically selected to satisfy the DC voltage fluctuation requirement, and the result can be verified by simulation. To this end, a capacitor bank is constructed by five 2mF, 4kV capacitors connected in parallel. Two capacitor banks should be further connected in series to provide the voltage neutral point, achieving the 5mF DC link capacitance. The base failure rate of a 2mF, 4kV capacitor is 100 FIT [41], $1\,\text{FIT} = 1\,\text{failure}/10^9\text{hours}$. The IGBT module and clamping diode base failure rates 100 FIT are obtained from datasheet [40, 42]. The drawback of 3L-NPC is that it lacks redundancy. Failure of any component results in a system failure.

The parts counting result of NPC for the target 6.7MW, 3.3kV motor drive is

shown in table 2.4.

Table 2.4. Parts count of 3 Level Neutral Point Clamped Converter

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	24	100	2400
Diode	12	100	1200
Capacitor	10	100	1000

With the total failure rate summed as 4600 FIT, the MTTF index, which is the reciprocal of the total failure rate, is calculated: MTTF $= 1/(4600 \times 10^{-9}) =$ 217391 hours = 24.8 years.

Neutral Point Clamp Converter with Open-end Winding Motor

An open-end winding motor can be used in the 6.7MW, 3.3kV motor drive, which allows for two NPCs supplying power to the motor. There is no much difference between this design and the 3L-NPC. The high load current in the previous 3L-NPC are now deployed to the two half-rated converters. The two converters are connected to two ends of the open-end winding motor which is displayed in Fig. 2.15.

Although 5 mF DC link capacitance can satisfy the voltage fluctuation requirement, the capacitance values are discrete. Three 2mF, 4kV capacitors are needed to connect in parallel to provide a 6mF, 4kV capacitor bank. Four of this banks are used in this topology. Therefore there are totally 12 (4×3) capacitors in this topology, which is slightly higher than the previous design presented in table 2.4.

With the failure rate in table 2.5, the MTTF index of this topology is:
MTTF $= 1/(4800 \times 10^{-9}) = 208333$ hours = 23.8 years.

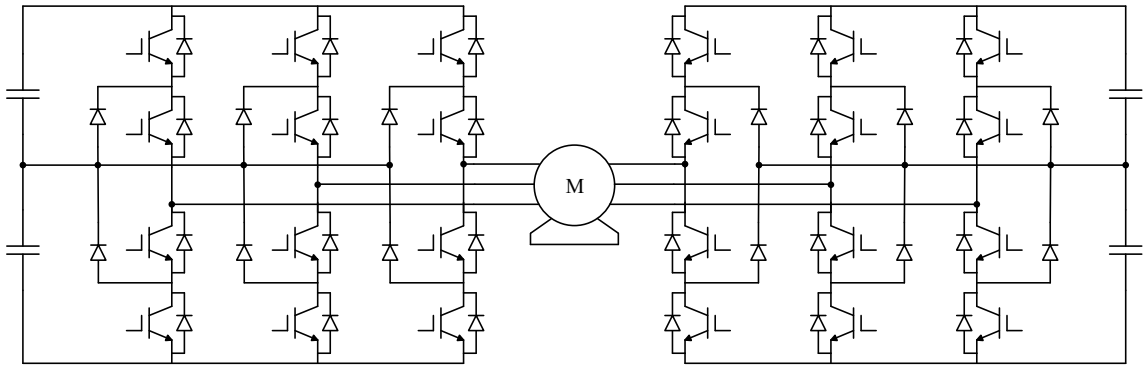


Figure 2.15. Neutral Point Clamp Converter with Open end Winding Motor

Table 2.5. Parts count of Neutral Point Clamp Converter with Open end Winding Motor

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	24	100	2400
Diode	12	100	1200
Capacitor	12	100	1200

Cascaded Neutral Point Clamp Converter

In the design of a cascaded NPC, the same IGBT is used for fair comparison. Hence there is only one submodule (SM) in each phase in Fig. 2.16.

As DC links of three phases in this design are independent of each other, there will be a double-line frequency power oscillation in each phase. Therefore much higher capacitance is needed for each DC link to accommodate the fluctuating power. 14mF capacitance is required for each phase to mitigate the voltage fluctuation to a desirable level.

With the failure rate in table 2.6, the MTTF index of this topology is:
MTTF $= 1/(7800 \times 10^{-9}) = 128205$ hours $= 14.6$ years.

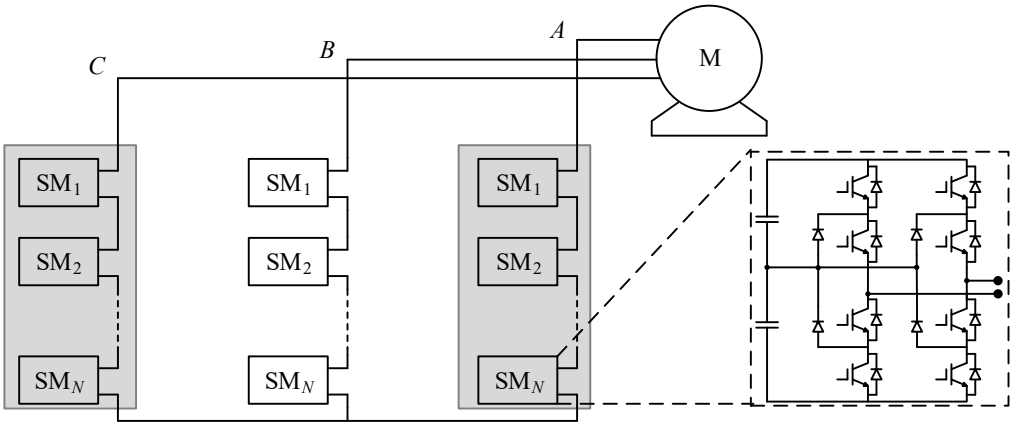


Figure 2.16. Cascaded Neutral Point Clamp Converter

Table 2.6. Parts count of Cascaded Neutral Point Clamp Converter

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	24	100	2400
Diode	12	100	1200
Capacitor	42	100	4200

5-level Active Neutral Point Clamp Converter

To avoid the IGBT parallel design in the original NPC, 6.6kV, 6.7MW voltage design is selected to replace the low 3.3kV design.The DC link bus voltage is twice of previous designs. Under the same voltage fluctuation percentage criteria, the capacitance of the DC-link can be reduced to a quarter of the NPC design while providing the same buffering energy ($\frac{1}{2}CV^2$). A capacitance of 1.25mF (5mF/4) is required in the main DC-Link. A capacitor bank with a structure of 2-series, 3-parallel 2mF, 4kV capacitors can be formed. Two banks are series-connected to provide a 1.5mF equivalent capacitance. There are additional 3 flying capacitors in clamping circuits that are also counted in table 2.7.

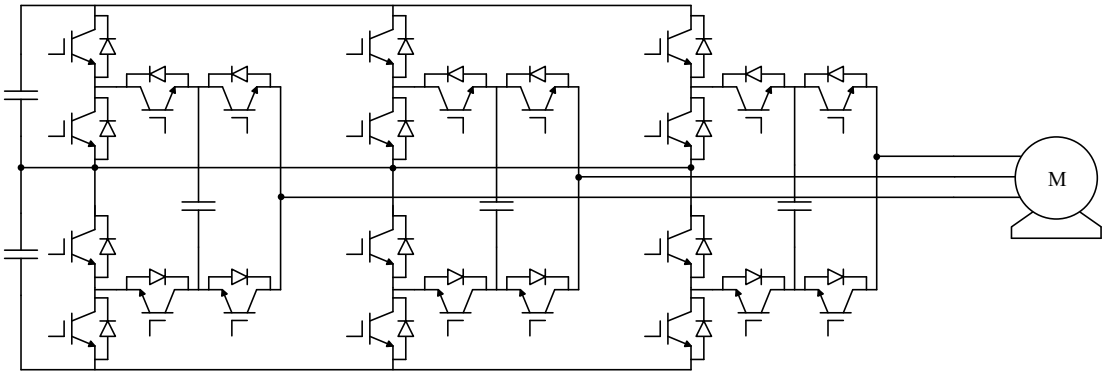


Figure 2.17. 5-level Active Neutral Point Clamp Converter

Table 2.7. Parts count of 5-level Active Neutral Point Clamp Converter

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	24	100	2400
Capacitor	15	100	1500

With the failure rate in table 2.7, the MTTF index of this topology is: MTTF $= 1/(3900 \times 10^{-9}) = 256410$ hours $= 29.3$ years.

2.4.2 Cascaded H-Bridge Converter

The cascaded H-bridge converter is first introduced in 1996 [43]. It synthesizes high voltage output based on cascaded power cells with low voltage devices. It is a cost-effective solution in high power drive. The CHB also features a high modularity which introduces redundancy and reduces maintenance time. Moreover, it has a fault tolerant capability which can increase the system MTTF [44]. For CHB, the reliability can be improved by a bypass contactor within each module [45]. The reliability of CHB with this basic fault-tolerant operation will be evaluated in

Chapter 3.

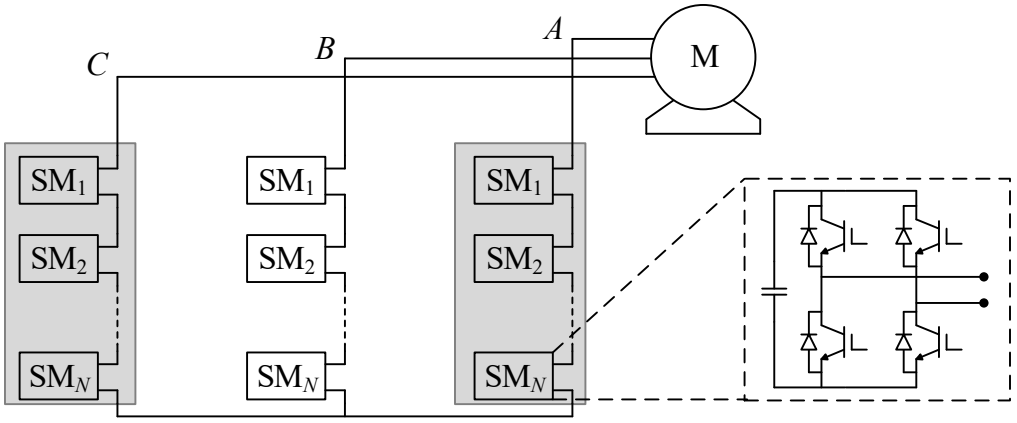


Figure 2.18. Topology of Cascaded H-Bridge Converter

The capacitors of rated voltage 1.85kV and 10.6mF is used in module design. There are 6 modules in each phase so there are 18 modules in total.

Table 2.8. Parts count of Cascaded H-Bridge Converter

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	72	100	7200
Capacitor	18	100	1800

Without Redundancy: MTTF $= 1/(9000 \times 10^{-9}) = 111111$ hours $= 12.7$ years

2.4.3 Modular Multilevel Converter

The modular multilevel converter (MMC) is first proposed in 2003 [15]. It is popular in HVDC power transmission system for its flexibility in power range and voltage range [15, 46–48]. The isolation transformer in CHB is replaced by a high voltage

common DC link. Despite the merits of MMC, reliability is a distinguished concern due to large numbers of components used [49, 50]. Recently, MMC is also advised to be used in MV drives [51–53].

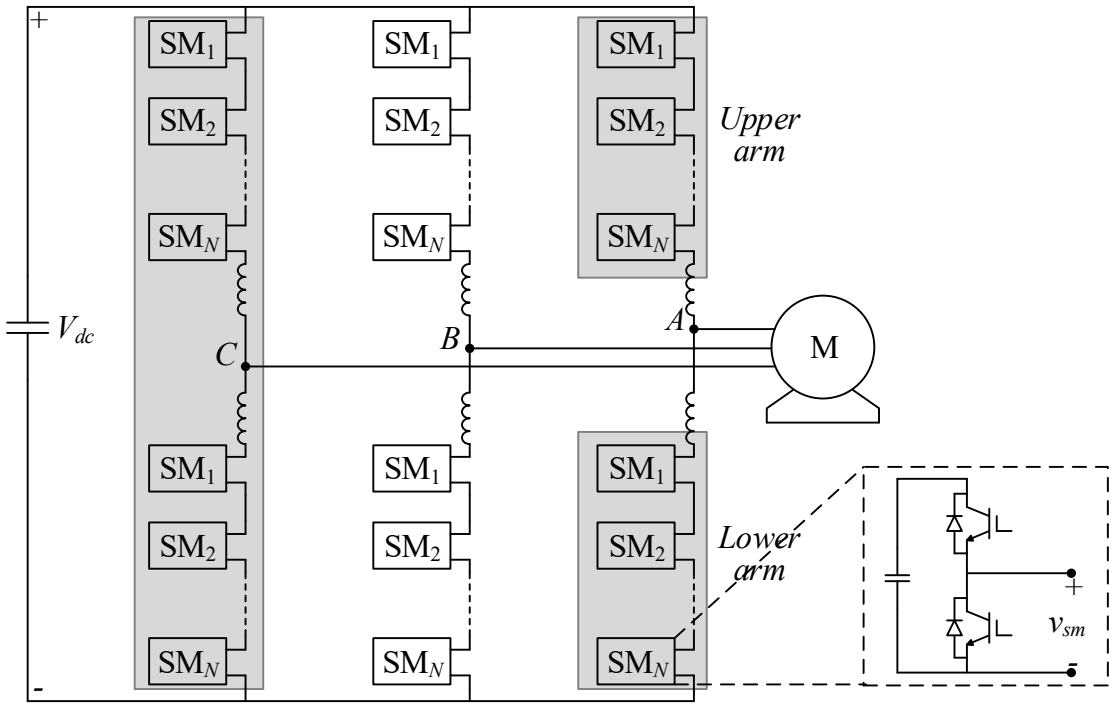


Figure 2.19. Topology of Modular Multilevel Converter with submodule

The topology of MMC is shown in Fig. 2.19. The MMC consists of a number of independent converter submodules (denoted as SM in Fig. 2.19). The number of series connected submodules can be scaled up/down depending on voltage level. A widely used half bridge submodule is shown in Fig. 2.19. It contains two semiconductor switches connected in series across a capacitor. Depending on which switch is turned on, the capacitor is either bypassed or inserted into the main circuit. Each submodule can generate a voltage of 0 or V_{dc}/N independently. Each phase leg can synthesize a stepped voltage waveform to approximate a sine-wave by inserting a suitable number of capacitors.

In 6.6 kV application, 10 submodules can be used in each arm. Half bridge module configuration is adopted in this design for less cost and higher reliability.

There are 60 submodules in total in Fig. 2.19. The parts count results are shown in table 2.9. If a complex submodule is used, the reliability index would be worsened. Without considering redundancy, the MTTF of the MMC is, MTTF = $1/(18000 \times 10^{-9}) = 55555$ hours = 6.3 years.

Table 2.9. Parts count of Modular Multilevel Converter

Components \ Attributes	Quantity	Base FIT	Total FIT
IGBT module	120	100	12000
Capacitor	60	100	6000

Table 2.10. Comparison of MTTF for different topologies

Topologies \ MTTF	λ	MTTF	B_{10}
3L-NPC	0.0403	24.8164	2.6147
NPC-OWM	0.0420	23.7823	2.5057
CNPC	0.0683	14.6353	1.5420
5L-ANPC	0.0342	29.2706	3.0840
CHB	0.0788	12.6839	1.3364
MMC	0.1577	6.3420	0.6682

The reliability index MTTF comparison of aforementioned topologies is concluded in table 2.10. Due to a large number of components in modular designs, their MTTFs are much less than the MTTFs for traditional designs. But modular designs have the ability to operate with one or more modular failures, their reliability can be improved with a simple redundant operation or redundant designs. Modular

designs are also convenient to maintain as replacing failed modules is easier than detecting the whole converter.

Chapter 3

Load-dependent Failure Rate Method

3.1 Introduction

The failure rate methods in standard MH-217F are widely used for its simplicity and effectiveness. Ideally, failure rate of a converter is the summation of critical components failure rates which are obtained from manufacturers or field records. The reliability index Mean Time To Failure (MTTF) is the reciprocal of the converter failure rate. Multilevel converter topologies reliability comparison can be conducted with failure rate methods. The topologies with modular designs have low reliability performance due to lots of components used. But the modular designed converters have the inherent redundancy for fault-tolerant operations. The fault-tolerant capability can increase the MTTF of converters by continuing operation after a failure. For multilevel converters with lots of submodules, their performances deteriorate insignificantly with the failure of one or two submodules. A redundantly designed converter can provide full power by replacing failure submodules with backup ones.

However, the reliability modeling methods in MH-217F are only applicable to a

series system in which there are only two states, normal and failed. Redundancy modeling techniques are needed to reassess the reliability of multilevel converters with fault-tolerant capability. The first part of this chapter will provide some redundancy modeling methods for multilevel converters. The reliability performance of multilevel converters with redundancy is calculated to give a complete comparison.

Oversizing components, additional submodules or backup converter are possible ways to improve motor drive system reliability but with different costs. Improving reliability with constrained costs is always a challenge for converter designer. Reliability- and cost- based redundancy design guideline is provided with a case study of Modular Multilevel Converter (MMC) redundancy design using load-dependent time-average failure rate method.

On the other hand, the crucial assumption of constant failure rate is reasonable for power system equipment which is operating in a relatively stable condition and under good maintenances. However, due to the harsh environment and variable load in drive systems, the operating conditions change severely and rapidly, making the crucial constant failure assumption under question. A load-dependent time-varying failure rate technique is proposed to model the varying operating condition and the changing failure rate in real time. However, the reliability index MTTF in traditional methods can only be calculated with equivalent constant operating conditions. To overcome this difficulty, a new reliability index, expected lifetime (i.e., MTTF) consumption taking real-time variable load into consideration, is proposed to model the state of health for power converters. Subsequently, a systematic reliability modeling method is developed based on the proposed load-dependent time-varying failure rate and expected lifetime consumption techniques.

3.2 Redundancy Modeling

Although the methods in 'MH-217F' are widely used. It cannot directly model a system with redundancy as it assumes all components are in series from a reliability point of view. Additional redundancy modeling techniques should be added to the

methods in 'MH-217F' for modeling multilevel converter reliability.

There are usually two operation modes of redundant submodules, active mode and standby mode. The two redundant modes are illustrated with series-connected submodules shown in Fig. 3.1. In the active redundant mode, all k basic submodules and additional m spare parts are sharing the voltage stresses and current load in normal operation. When a submodule fails, it will be bypassed from the converter by a normally-open contactor. In the standby redundant mode, the m spare parts are bypassed in normal operation by normally-closed contactors, and only k basic submodules share the stresses. When a basic submodule fails, one of the m standby submodules will be employed after the bypass of faulty submodule.

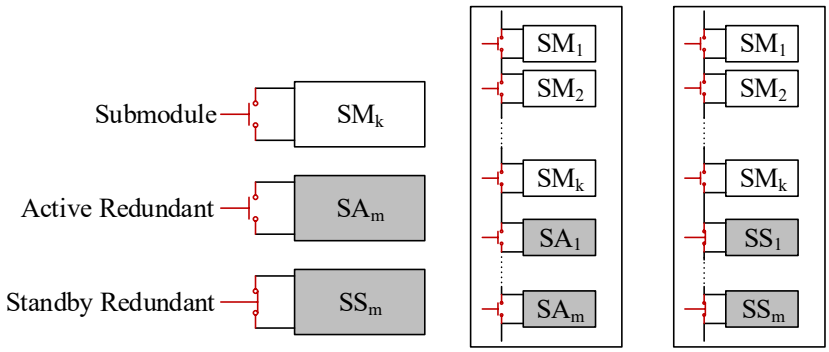


Figure 3.1. Two redundant operation strategies

The difference between active redundant mode and standby redundant mode is that, redundant submodules in active mode are sharing load during normal operation while they are not working during normal operation in standby mode. The reliability modeling of the two redundant modes is elaborated in detail as follows.

In the active redundant mode, k out of n submodules are required for multilevel converters normal operation and all n components are in operation initially, where $n = k + m$ as in Fig. 3.1. Submodule failure rate and reliability function in a system are assumed to be identical and denoted as λ, and $R(t)$ respectively.

The reliability of multilevel converter is the probability summation of states

with more than k submodules are in good state [27].

$$R_{active}(t) = \sum_{i=k}^{n} C_n^i R^i(t)[1 - R(t)]^{n-i} \tag{3.1}$$

C_n^i is the binomial coefficient,

$$C_n^i = \binom{n}{i} = \frac{n!}{(n-i)!i!} = \frac{n(n-1)\cdots(n-i+1)}{i(i-1)\cdots 1} \tag{3.2}$$

The MTTF for the multilevel converter is:

$$MTTF_a = \sum_{i=k}^{n} \frac{1}{i\lambda} \tag{3.3}$$

The equation (3.3) can be derived as follows:

Equation (2.10) states that MTTF is the integral of reliability function from 0 to infinity. Substituting equation (3.1) into equation (2.10) gives

$$MTTF_a = \int_0^\infty R_{active}(t) = \int_0^\infty \sum_{i=k}^{n} C_n^i R^i(t)[1 - R(t)]^{n-i} \mathrm{d}t \tag{3.4}$$

Exchanging calculation sequence of integral and summation:

$$MTTF_a = \sum_{i=k}^{n} C_n^i \int_0^\infty R^i(t)[1 - R(t)]^{n-i} \mathrm{d}t \tag{3.5}$$

Calculating $\int_0^\infty R^i(t)[1 - R(t)]^{n-i}\mathrm{d}t$ with 'integration by parts' method, and observing that

$$\frac{\mathrm{d}R^{(i)}(t)}{\mathrm{d}t} = iR^{(i-1)}(t)[-\lambda R(t)] = -\lambda i R^i(t) \tag{3.6}$$

$$\frac{\mathrm{d}[1 - R(t)]^{(n-i)}}{\mathrm{d}t} = (n-i)[1 - R(t)]^{(n-i-1)}[-\lambda R(t)] \tag{3.7}$$

Hence, the integrand in equation (3.5) can be calculated as follows:

$$\int_0^\infty R^i(t)[1-R(t)]^{n-i}\mathrm{d}t = \frac{R^i(t)}{-\lambda i}[1-R(t)]^{n-i}|_0^\infty + \frac{n-i}{i}\int_0^\infty R^{i+1}(t)[1-R(t)]^{n-i-1}\mathrm{d}t \tag{3.8}$$

As $[1 - R(0)] = 0$, and $R(\infty) = 0$, equation (3.8) can be simplified as,

$$\int_0^\infty R^i(t)[1 - R(t)]^{n-i}\mathrm{d}t = \frac{n-i}{i}\int_0^\infty R^{i+1}(t)[1 - R(t)]^{n-i-1}\mathrm{d}t \tag{3.9}$$

Calculating equation (3.9) recursively with 'integration by parts' method gives,

$$\int_0^\infty R^i(t)[1 - R(t)]^{n-i}\mathrm{d}t = \cdots = \frac{(n-i)(n-i-1)\cdots 1}{i(i+1)(i+2)\cdots(n-1)}\int_0^\infty R^n(t)[1 - R(t)]^0\mathrm{d}t \tag{3.10}$$

Simplifying equation (3.10) gives,

$$\int_0^\infty R^i(t)[1 - R(t)]^{n-i}\mathrm{d}t = \frac{(n-i)!(i-1)!}{(n-1)!}\frac{1}{n\lambda} \tag{3.11}$$

Substituting equation (3.2) and equation (3.11) into equation (3.5) gives,

$$MTTF_a = \sum_{i=k}^{n}\frac{n!}{(n-i)!i!}\frac{(n-i)!(i-1)!}{(n-1)!}\frac{1}{n\lambda} = \sum_{i=k}^{n}\frac{1}{i\lambda} \tag{3.12}$$

In standby redundant mode, k out of n submodules are required for multilevel converters normal operation, where $n = k + m$ as shown in Fig. 3.1. At any time, there are only k submodules in operation. Once a submodule fails and is bypassed, another submodule in the standby m submodules will be configured in operation. The standby replacement process can be modeled as a Poisson process with a constant rate $k\lambda$, where λ is the submodule failure rate. The homogeneous Poisson process fully characterizes a counting process $\{N(t), t \geq 0\}$ with a constant rate, where $N(t)$ denotes the total occurrences of the event up to and include time t [54]. The probability of submodule failure number equaling i follows a Poisson distribution, $i \sim Pois(k\lambda)$.

$$P[N(t) = i] = \frac{(k\lambda t)^i}{i!}R^k(t) \tag{3.13}$$

where λ and $R(t)$ are the submodule failure rate and reliability function respectively.

Therefore, the reliability of multilevel converter is the probability of the failed submodules no more than m, where $m = n - k$.

$$R_{standby}(t) = P[N(t) \leq (n-k)] = \sum_{i=0}^{n-k}\frac{(k\lambda t)^i}{i!}R^k(t) \tag{3.14}$$

The MTTF for multilevel converter is:

$$MTTF_s = \frac{n-k+1}{k\lambda} \tag{3.15}$$

The equation (3.15) can be derived as follows:

Equation (2.10) states that MTTF is the integral of reliability function from 0 to infinity. Substituting equation (3.14) into equation (2.10) gives

$$MTTF_s = \int_0^\infty R_{standby}(t)\mathrm{d}t = \int_0^\infty \sum_{i=0}^{n-k} \frac{(k\lambda t)^i}{i!} R^k(t)\mathrm{d}t \tag{3.16}$$

Exchanging calculation sequence of integral and summation:

$$MTTF_s = \sum_{i=0}^{n-k} \int_0^\infty \frac{(k\lambda t)^i}{i!} R^k(t)\mathrm{d}t \tag{3.17}$$

Considering the frequency-domain general derivative property of Laplace Transform,

$$\int_0^\infty t^i e^{-st}\mathrm{d}t = \frac{i!}{s^{i+1}} \tag{3.18}$$

Calculating $\int_0^\infty \frac{(k\lambda t)^i}{i!} R^i(t)\mathrm{d}t$ with equation (3.18)

$$\int_0^\infty \frac{(k\lambda t)^i}{i!} R^i(t)\mathrm{d}t = \frac{(k\lambda)^i}{i!}\frac{i!}{(k\lambda)^{i+1}} = \frac{1}{k\lambda} \tag{3.19}$$

Simplifying equation (3.19) gives,

$$\int_0^\infty \frac{(k\lambda t)^i}{i!} R^i(t)\mathrm{d}t = \frac{1}{k\lambda} \tag{3.20}$$

Substituting equation (3.20) into equation (3.17)

$$MTTF_s = \sum_{i=0}^{n-k} \frac{1}{k\lambda} = \frac{n-k+1}{k\lambda} \tag{3.21}$$

There is a '$N-1$' criterion which states that a system will not fail after a single component failure. It can be extended to a '$N-2$' criterion in the same definition [55]. Similar to the '$N-1$' and '$N-2$' criteria, two concepts are defined to describe the redundancy capability of a multilevel converter.

Definition 3.1. First order redundancy is the redundancy capability of a system which can withstand up to one submodule failure.

Definition 3.2. Second order redundancy is the redundancy capability of a system which can withstand up to two submodule failure.

MTTF for systems with redundancy capability can be calculated with equation (3.3) and equation (3.15) depending on which redundant strategy is adopted. MTTF with the first order redundancy

$$MTTF_{a1} = \frac{1}{(k+1)\lambda} + \frac{1}{k\lambda} \tag{3.22}$$

$$MTTF_{s1} = \frac{2}{k\lambda} \tag{3.23}$$

MTTF with the second order redundancy

$$MTTF_{a2} = \frac{1}{(k+2)\lambda} + \frac{1}{(k+1)\lambda} + \frac{1}{k\lambda} \tag{3.24}$$

$$MTTF_{s2} = \frac{3}{k\lambda} \tag{3.25}$$

These formulas are used for reliability comparison of systems with '$N-1$' and '$N-2$' design criteria, and it is assumed that all submodules are non-repairable and fault can be bypassed in a negligible time. Otherwise, the converter should be modeled as a repairable system. Then another reliability index, i.e., availability, can be used to describe the reliability performance.

Definition 3.3. Repair rate is the rate at which a repair action is performed. It describes the number of successful repairs per unit time.

Repair rate is a basic concept to describe system maintainability. The analogy between reliability and maintainability is shown in Table 3.1.

Definition 3.4. Availability is the ability of an item to be in a state to perform a required function under given conditions at a given instant of time or over a given time interval, assuming that the required external resources are provided.

Table 3.1. Analogy between reliability and maintainability

Reliability	Maintainability
failure density	repair density
$f(t)$	$g(t)$
reliability	maintainability
$R(t) = 1 - \int_0^t f(t)dt$	$M(t) = \int_0^t g(t)dt$
failure rate	repair rate
$\lambda(t) = \frac{f(t)}{R(t)}$	$\mu(t) = \frac{g(t)}{1-M(t)}$
Mean Time To Failure	Mean Time To Repair
$MTTF = \int_0^t tf(t)dt$	$MTTR = \int_0^t tg(t)dt$

The availability, A, can be expressed as,

$$A = \frac{E[uptime]}{E[uptime] + E[downtime]} = \frac{MTTF}{MTTF + MTTR} \tag{3.26}$$

From the above equation, it is clear that availability depends on the system reliability and maintainability.

Definition 3.5. A derated state is the state of an item, where that item is deliberately operated under limits that are lower than the rated values.

The Markov approach can be used for a wide range of reliability problems including systems that are either non-repairable or repairable, either series-connected or parallel-connected. Active mode redundancy can also be modeled by this method. The application condition for this method is that the system can be described as a Markov process which assumes failure and repairing characteristics follow exponential distributions. This method uses a state diagram approach to model the sequence of stochastic processes that govern the events occurring in a system. For example, a three-component system has 8 states as each component has two states, 1 denote 'good' and 0 denote 'failure'. The state diagram for the three-component

system is shown in Fig. 3.2, in which the underlined three-digit number represent the states of three components. For example, the second state '110' denotes the first and the second components in the system are in good state while the third one is failed. It should be noted that, some transitions are physically impossible. For example, the transition from state '111' to '100' is impossible as the probability of simultaneous occurrence of two independent failures at a time instant is zero. It is much more probable that the transition from state '111' to '100' will first go to '101' or '110' [25].

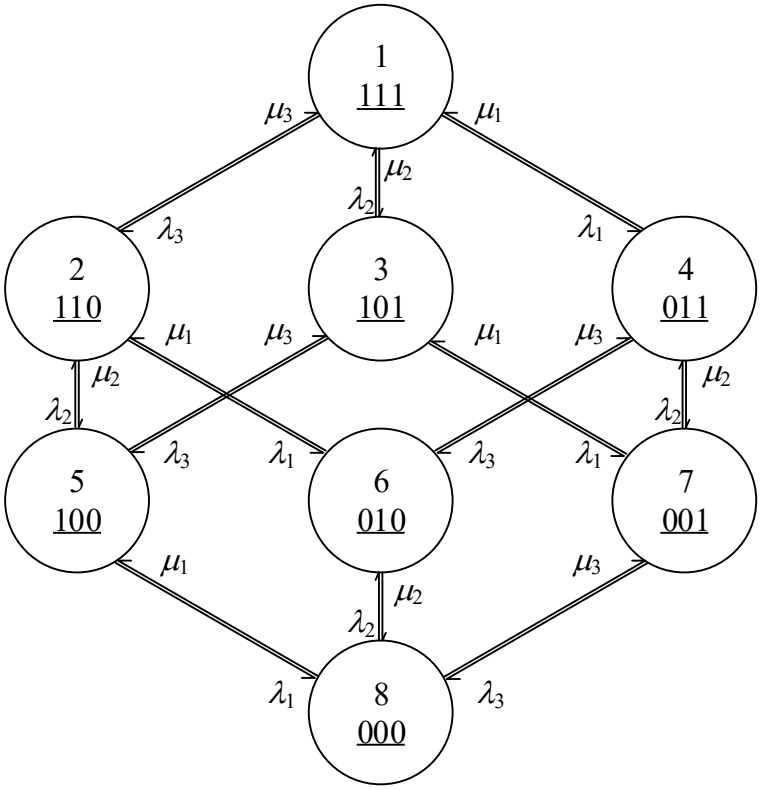


Figure 3.2. State diagram for a three-component system

Determining the state probabilities at any time requires solving the Chapman-Kolmogorov differential equation, which can be created directly from the state diagram.

$$P'(t) = P(t)\,Q \tag{3.27}$$

where $P(t) = [p_1\ p_2\ \cdots\ p_n]$ is the row vector of state probabilities at time t, and $P'(t) = [\frac{\mathrm{d}p_1}{\mathrm{d}t}\ \frac{\mathrm{d}p_2}{\mathrm{d}t}\ \cdots\ \frac{\mathrm{d}p_n}{\mathrm{d}t}]$ is the time derivatives of the state probabilities $P(t)$, and Q is the state transition matrix whose elements are defined by

$$q_{ij} = \lambda_{ij}, i \neq j \tag{3.28}$$

$$q_{ii} = -\sum_{j \neq i} \lambda_{ij}, i = j \tag{3.29}$$

where λ_{ij} is the transition rate from state i to j.

The previous system has only $n-1$ independent equations. To solve the steady state probabilities, an additional equation is needed:

$$\sum_{i=1}^{n} p_i = 1 \tag{3.30}$$

In addition to the probability of being in a given state, the mean frequency of encountering i^{th} state, f_i, and the mean duration of a stay in i^{th} state, T_i, are computed respectively as:

$$f_i = p_i \sum_{j \neq i} \lambda_{ij} \tag{3.31}$$

$$T_i = \frac{1}{\sum_{j \neq i} \lambda_{ij}} \tag{3.32}$$

Taking the redundancy into consideration, the reliability index MTTF is re-assessed for multilevel converter with modular design. Table 3.2 shows the MTTF results with active redundant operation.

Due to a large number of components used in multilevel converters with modular design, their reliability performances are incomparable to traditional 2-Level or 3-Level designs. But these multilevel converters have the ability to operate with one or two submodules failed. Hence, their MTTF with the first-order and the second-order redundancy can be improved significantly as seen from Table 3.2. Modular design converters are also easy to maintain by replacing only failed submodules.

Table 3.2. Comparison of MTTF for different topologies

Topologies \ MTTF	No redundancy	1^{st} order redundancy	2^{nd} order redundancy
3L-NPC	24.8164	–	–
NPC-OWM	23.7823	–	–
CNPC	14.6353	–	–
5L-ANPC	29.2706	–	–
CHB	12.6839	23.5558	33.0688
MMC	6.3420	11.7779	16.5344

After the comparison of electrical performance and reliability for the topologies aforementioned, CHB and MMC topologies are selected as the candidates for the high power motor drive system. To evaluate the cost-effectiveness of '$N-1$' and '$N-2$' design rules on the two selected topologies, quantitative reliability and qualitative cost comparison of different reliability enhancement methods are presented in table 3.3 and table 3.4 respectively.

Table 3.3. Comparison of reliability enhancement methods for CHB and MMC

MTTF \ $MTTF_N$	2 parallel active	2 parallel standby	$N-1$ design	$N-2$ design
12.6839	19.0259	25.3678	23.5558	33.0688
6.3420	9.5129	12.6839	11.7779	16.5344

The comparison results show that the '$N-1$' redundancy design is commensurable to the two parallel designs. But the cost of '$N-1$' redundancy design is much lower than standby system.

Table 3.4. Comparison of reliability enhancement costs for CHB and MMC

CHB/MMC cost \ Increment	active parallel	passive parallel	$N-1$
1 *pu*	Double	Double	Fractional

3.3 Reliability and Cost based Redundancy Design

'$N-1$' redundancy design and backup at converter-level are two possible ways to improve motor drive system reliability but with different costs. The previous section briefly discusses the reliability and cost of these redundant designs. Detailed design procedure and guideline are needed for accurate reliability and cost modeling for multilevel converters redundancy design. Of all the six topologies discussed, Cascaded H-Bridge (CHB) and Modular Multilevel Converter (MMC) are the two topologies with high modularity and scalability. CHB has been used in MV drive applications for many years while MMC based MV drive is still in development stage.

MMC employs as twice power devices as CHB to increase topology modularity, resulting in a lower reliability. The reliability of MMC can be improved by redundant designs. In practice, reliability improvement with constraint costs is a challenge. In view of these, a reliability and cost based redundancy design is developed for MMC. Reliability and cost are quantified for comparison purpose. A MV application is used to demonstrate the guideline. The reliability modeling is based on a load-dependent failure rate method and redundancy modeling techniques. The cost analysis focuses on capital cost and power loss cost.

Fig. 3.3 is the schematic of a three phase MMC MV drive with a modified submodule suitable for fault-tolerant operation. The faulty submodule can be isolated with the additional bypass switch and fuse.

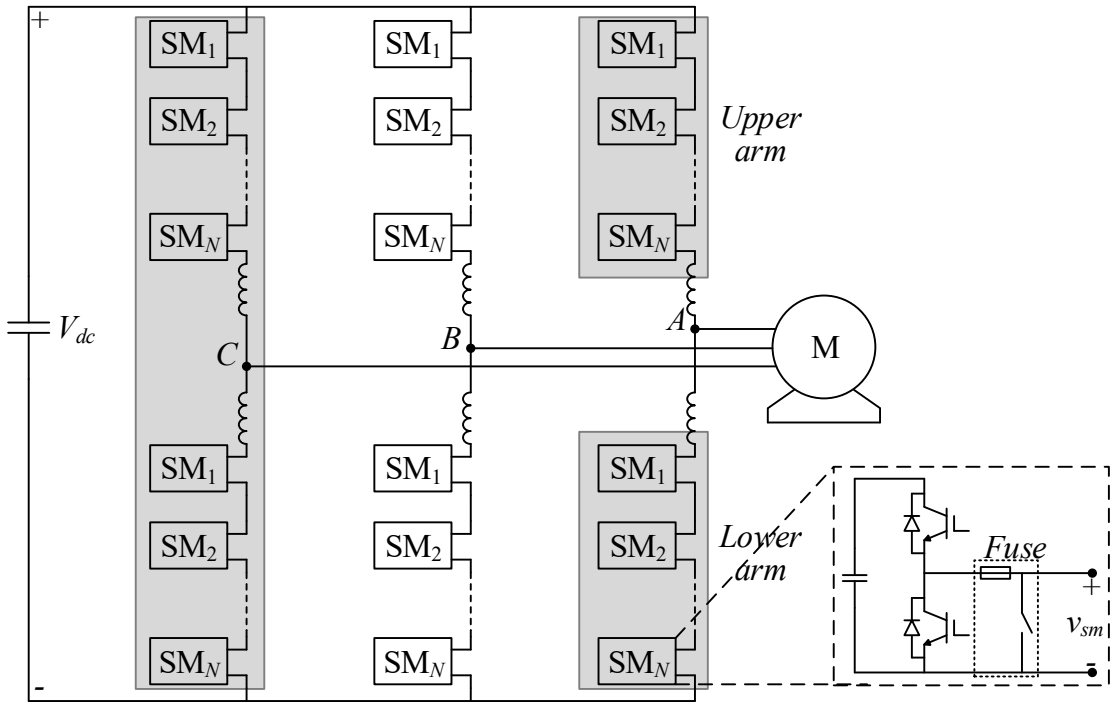


Figure 3.3. Schematic of a three phase MMC and a modified submodule

To make MMC more reliable in practical applications, many fault-tolerant methods are proposed to improve MMC reliability [50, 56–60]. These methods can be roughly classified as degraded operation and quasi-normal operation according to post-fault operation performance [18]. Fault-tolerant strategies relying on the inherent redundancy in MMC usually lead to a degraded performance of a post-fault operation. The degraded operation with modified modulation strategies has been studied in [61, 62]. The faulty converter cells are isolated from the system, and redundant switching states are used to generate a neutral voltage shift to maintain a balanced line-to-line AC output voltage. In comparison to normal operation, the magnitude of output voltage decreases and harmonic distortion increases. Due to the limitations of degraded operation, redundant designs are proposed to achieve normal post-fault operation [63–66].

Thanks to the high modularity of MMC, it is easy to implement redundant designs which include cell overrating [63] and backup cells [52, 57, 64–66]. In [64],

redundant designs are compared in terms of operation properties such as control complexity, capacitor voltage balancing, power losses and dynamical behavior. The effectiveness of reliability improvement regarding redundant designs and redundant strategies have not bee discussed yet. Additionally, to improve converter reliability with a constraint cost is a challenge. In view of these, a reliability and cost based redundancy design guideline for MMC is proposed. Quantitative reliability and cost assessment help to identify cost-effective redundant designs.

The flow chart of reliability and cost based redundancy design is shown in Fig. 3.4. The MMC function design and basic electrical simulations will be conducted first. Then for each basic design, reliability modeling is conducted. Several candidates which meet the basic requirements will be evaluated in terms of reliability and cost. If the design meets the specified reliability requirements, such as MTTF and B10 lifetime, the design is recorded after a cost analysis. For those designs which have lower reliability than requirements, redundant submodules will be added. Reliability of these designs will be reassessed. After several iterations, all redundant designs which satisfy the reliability requirements will be selected for cost analysis. The affordable design or the most cost-effective design will be selected at last.

With a basic concept and function design, the parameters of multilevel converters can be calculated. Converter components can be selected accordingly with appropriate margins. The component electrical stresses can be obtained from simulation. A steady-state power loss model and thermal model are used to calculate thermal stress for each component. The key steps for the reliability and cost modeling of modular designed multilevel converters are listed as below.

- Determine the load-dependent failure rate of critical components with real stresses.
  - The critical components in a submodule are power semiconductors and capacitors. The actual stresses of the device are calculated according to operating conditions.

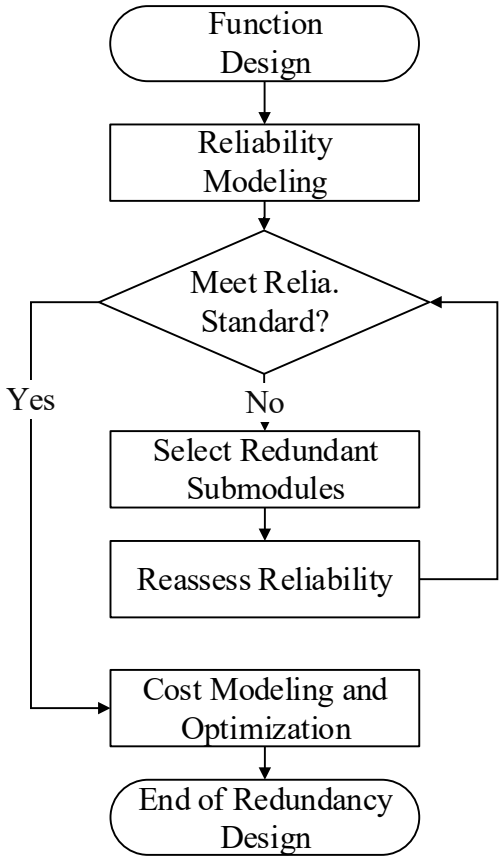


Figure 3.4. Flow chart of reliability and cost based redundancy design

- Formulate the submodule failure rate and reliability function.
  - The failure rate based methods are used to calculate the reliability function for the submodule.
- Calculate multilevel converter reliability with redundancy modeling techniques.
  - Submodules are series connected. The redundancy modeling techniques are needed to calculate the reliability of different designs.
- Establish component cost models.

  - The submodule cost model is derived based on IGBT and capacitor costs from manufacturers' viewpoint.

- Analyze cost for redundant designs which meet the reliability requirements.
  - In practice, manufacturers prefer a B10 lifetime to determine product warranty period. For end users, the MTTF is the only choice for failure rate based method.
- Identify an affordable redundant design or the most cost-effective design.
  - For different applications, the priorities of reliability are different. And special requirements from manufacturers and consumers are also needed to be taken care of.

These procedures will be discussed in detail in the following case study.

3.4 Modular Multilevel Converter Redundancy Design Case Study

A 3MW MMC is used in the case study to demonstrate the reliability and cost modeling method. Its parameter designs are listed in Table 3.5.

3.4.1 Reliability Modeling of Modular Multilevel Converter

In Fig. 3.5, the MMC is subdivided into three hierarchical levels such that the reliability function of each level is more easily obtained. In each hierarchal level, the reliability block diagram (RBD) is used to represent the reliability relationship of MMC components. In the first level, each arm is regarded as one lumped reliability block for MMC reliability evaluation. All six arms and auxiliary device are required in a good state for the MMC normal operation. Hence, they are connected in series from a reliability point of view.

Table 3.5. A 3MW MMC parameters

MMC		Submodule	
cell number per arm	10	Cap. Voltage	1000V
DC voltage	10kV	Voltage ripple	100Vpp
line voltage RMS	6kV	cell current (rms)	176A
active power	3MW	cell current (peak)	304A
arm inductance	1mH	cell capacitance	3.4mF
ac frequency	50Hz	switching frequency	2100Hz

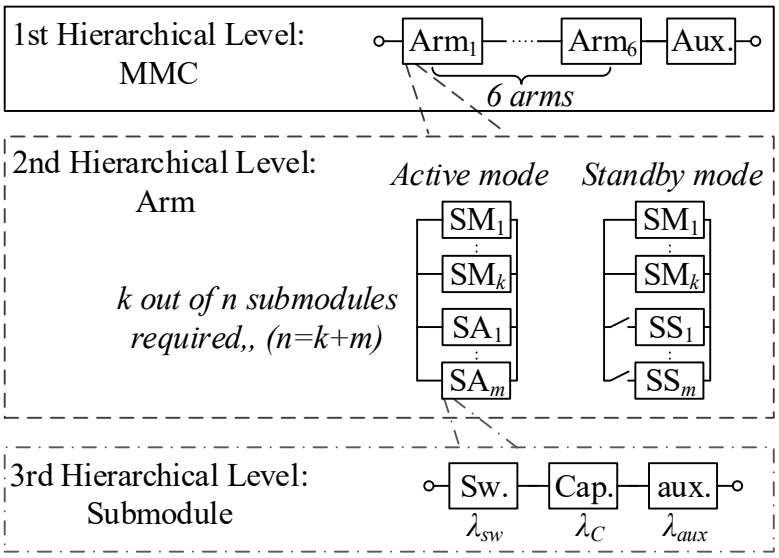


Figure 3.5. Hierarchical reliability modeling of MMC.

To calculate MMC reliability, each arm reliability in the first level are to be determined. The second hierarchical level shows the reliability modeling of one arm. For MMC designs with redundant submodules, the $k-out-of-n:G$ system can be used to represent each arm in reliability modeling. In Fig. 3.5, the

SM_1 to SM_k are the k basic submodules required for a conventional MMC design. There are n submodules in each arm with m spare parts as redundant cells, where $m = n - k$. There are two redundant operation modes, active redundant mode and standby redundant mode. Each arm can operate in either mode, in which arm reliability can be modeled correspondingly. The arm reliability can be calculated with the techniques introduced in Section 3.2: Redundancy Modeling.

Each submodule reliability evaluation is accomplished in the third hierarchical level in which basic electrical components are represented by reliability blocks. The failure rates of electrical components in one submodule are application dependent. The determination of failure rate is modeled with a load-dependent failure rate method. It should be noticed that the component failure rate is usually characterized by a constant value in their useful life period.

In a submodule, the most vulnerable components are semiconductor switches (IGBT/MOSFET) and capacitors. The Gate drivers, PCB board, auxiliary power supply and bypass switch and fuse can also be modeled for reliability analysis. Although these auxiliary devices are very important for reliability analysis, a lumped constant failure rate will be used to represent all these components' failure rates.

There are many IGBT candidates that satisfy the given specifications. The 1700V IGBT is selected for its low loss due to its mature technology. The IGBT chip and package are different although the voltage and current rating are the same. For 1700V voltage rating, candidates from different suppliers have similar performance, among which FF450R17IE4 is relatively superior to others due to its lower loss and better thermal dissipation [67]. The base failure rate for this IGBT module is 100 FIT [68]. 1 FIT is 1 failure in 10^9 hours.

The capacitor bank of 3.4 mF can be made by using either Aluminum Electrolytic capacitor or film capacitor. For an electrolytic capacitor, the capacitance can be very large while the voltage rating is usually less than 500V, leading to at least 3 capacitors connected in series to withstand 1000VDC (100V ripple) voltage in each submodule. Another drawback of electrolytic capacitor is its relatively short

lifetime when compared with film capacitor [37, 69, 70]. From a reliability point of view, the AVX film capacitor with 1850V, 3.56mF module is selected. Its base failure rate is 100FIT [71].

The failure rate first depends on the technology of devices and, obviously, on the voltage and thermal operating conditions. These operating conditions are included in the λ formulation through acceleration factors [32, 72].

$$\lambda_{submodule} = \sum_{1}^{n_c}(\lambda_i \prod_{1}^{n_p} \pi_j) \tag{3.33}$$

where $\lambda_{submodule}$ is the submodule failure rate, λ_i is the i^{th} component failure rate, π_j is the j^{th} stress factor, n_c is the number of components, and n_p is the number of π factors. For example, the impact of thermal stress and voltage stress on IGBT failure rate are given by,

$$\pi_T = e^{-2114(\frac{1}{T_j+273}-\frac{1}{298})} \tag{3.34}$$

$$\pi_S = 0.045\, e^{3.1V_S} \tag{3.35}$$

In MMC reliability evaluation, the basic component of the MMC is a submodule whose failure rate functions can be obtained in previous steps. The redundancy modeling techniques in Section 3.2 can be used for MMC arm reliability evaluation. The arm reliability can be calculated either by equation (3.1) or equation (3.14).

It should be noticed that, the voltage stress of each cell in active mode is less than those in standby mode. This effect is included in the submodule reliability formulations. Upon the symmetry of 3 phase 3MW MMC, one phase arm reliability can be calculated first. Then the other arms follow the same reliability calculating pattern. Each arm can be modeled as a redundant system with k equaling 10 while n is no less than 10. After the reliability function of each arm is obtained, the MMC reliability can be easily calculated with the RBD network modeling technique. For the MMC with 6 arms, without considering degraded operation, the system reliability model is a 6-arm series-connected RBD

3.4.2 Cost analysis of the Modular Multilevel Converter

The MMC cost includes initial cost and operating cost [73]. The initial cost mainly consists of the component cost. To assess the redundant submodules impact on operating cost, the power loss cost is selected as the main part of operating cost for comparison purpose.

The MMC initial cost can be represented by a summation of submodule cost and auxiliary system costs, such as cooling system cost. To simplify cost analyses, the auxiliary cost is assumed to be 10% of the submodules cost. There are some non-physical cost factors such as minimum ordering quantity (MOQ) and location. Generally, the cost structure of semiconductors derives from a complex mix of sophisticated manufacturing processes and high R&D investments, whereas the (unprocessed) raw materials take only a negligible share of the total cost [73]. To give a general and insightful model, only the physical cost factors are considered which directly relate to converter sizing process [68, 71]. From an engineering point of view, the two most important features of a semiconductor are its chip size and the package. Together they largely define the electrical and thermal behavior of the device. Therefore, the following IGBT cost model in [73] is used:

$$\Sigma_{SC} = \sum_{n} \sigma_{chip} A_{chip} + \Sigma_{pack} \tag{3.36}$$

where Σ_{SC} is the semiconductor cost, σ_{chip} is the specific price per chip area depending on chip technology, A_{chip} is the chip area, and Σ_{pack} is the package price. The Si IGBT chip price, diode chip price, and package price are $7.5\$/cm^2$, $5.1\$/cm^2$, and 17.2\$/unit respectively [68, 73]. The chip area is determined by the system current rating which is 450A in this case study. The chip current density of a Si IGBT is $75A/cm^2$ [74].

In general, there are two types of capacitors widely used in high power applications. One is the electrolytic capacitor (E-Cap) and the other is film capacitor. The E-cap has a low price due to its mature technology. Its prices are proportional to the energy stored,

$$\Sigma_{ECap} = b_e V_r + C_e C_r V_r^2 \tag{3.37}$$

where Σ_{Ecap} is the E-Cap cost, V_r and C_r are the rated capacitor voltage and capacitance. A typical value for b_e and c_e are 1.610^{-3}\$/V and 2.810^{-5}\$/mFV^2.

While the film capacitors have a much higher lifetime with a relatively high cost. Its prices are mainly dominated by its capacitance and insulation,

$$\Sigma_{film} = a_f + b_f V_r + c_f C_r \tag{3.38}$$

where Σ_{film} is the film capacitor cost. The coefficients a_f, b_f, c_f are -1.2\$, 0.06\$/V and 2.7\$/mF respectively.

The power loss is mainly determined by the semiconductor conduction loss. For the power loss cost calculation, the MMC steady-state loss models in [46, 75] are used,

$$V_F = V_{T0} + r_T \cdot i_T \tag{3.39}$$

$$P_F = i_T \cdot V_F(I_F) \tag{3.40}$$

$$P_{sw} = f_s E_{sw} \cdot S \tag{3.41}$$

where V_F, V_{T0}, r_T, and i_T are semiconductor forward voltage drop, threshold voltage, equivalent conduction resistance, and instantaneous conduction current respectively. I_F and $V_F(I_F)$ are average conduction current and equivalent conduction voltage function with respect to I_F. P_F and P_{sw} are power semiconductor forward conduction loss and switching loss respectively. f_s, E_{sw}, and S are switching frequency, switching energy loss, and scaling factor. The energy price can be selected according to different applications.

3.4.3 Reliability and Cost based Redundancy Selection

The reliability and cost are assessed for the 3MW MMC. For expression simplicity, the redundant designs of MMC are denoted by a 3-tuple with each number

representing basic cells, active reserve cells and standby cells respectively. For example, (10,0,1) represents a MMC design with 10 basic cells, 0 active redundant mode cell, and 1 standby redundant mode cell. The MMC designs require 10 basic cells in each arm. Referring to Fig. 3.5, the submodule reliabilty function can be calculated with equation (3.33) and denoted as $R_{sub}(t)$. Then each arm reliability $R_{arm}(t)$ can be accordingly derived with either equation (3.1) or equation (3.14) according to practical redundant modes. Subsequently, the MMC reliabilty can be calculated as follows,

$$R_{MMC} = R_{arm}(t)^6 \cdot R_{aux}(t) \tag{3.42}$$

where $R_{aux}(t)$ is the reliability function of auxiliary system.

To quantify thse effectiveness of redundant designs, reliability evaluation results of original design and two redundant designs are plotted in Fig. 3.6.

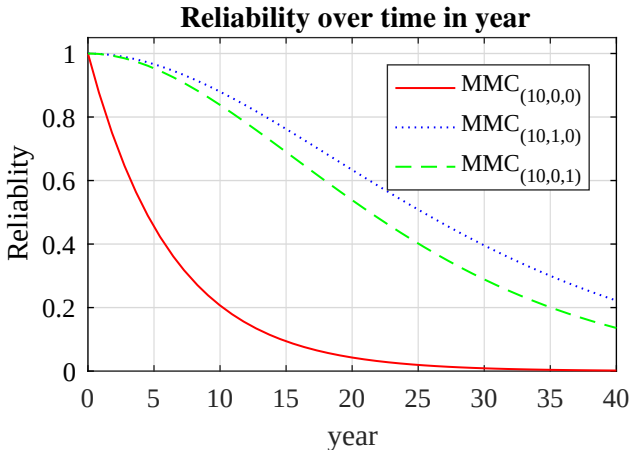


Figure 3.6. Reliability comparison of basic design and two redundant designs

With one redundant cell used, the reliability of MMC is improved significantly over a timespan of 40 years. With the reliability function obtained, the reliability indices, MTTF and B10 lifetime can be calculated correspondingly and are shown in table 3.6

To verify the theoretical reliability prediction results, the Monte Carlo simulation

Table 3.6. Reliability indices of MMC designs

Designs	MTTF (years)	B10 life (years)
(10,0,0)	6.3420	0.6682
(10,0,1)	23.9389	7.5835
(10,1,0)	28.4547	9.0115

which mimics the operations of complex systems by random sampling is used as a crosscheck. A 100 test Monte Carlo simulation reliability results and original calculated MMC reliability are shown and compared in Fig. 3.7.

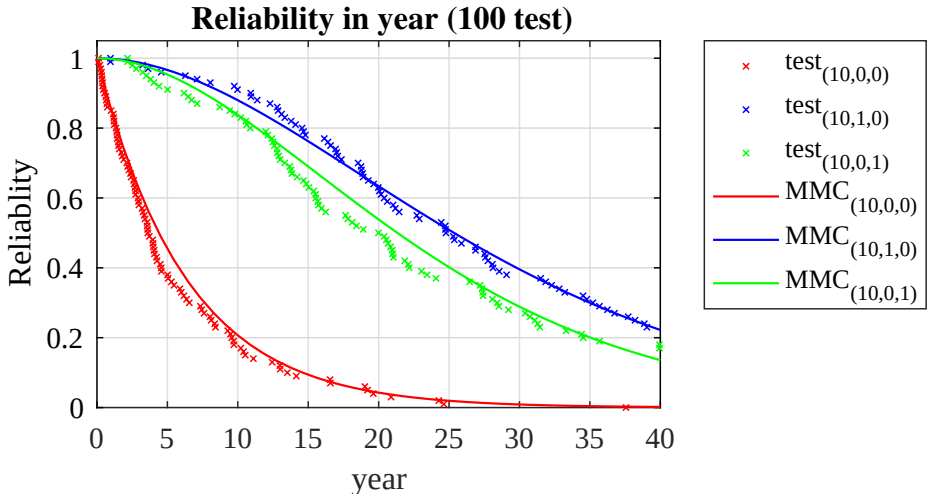


Figure 3.7. A 100 test Monte Carlo simulation reliability results

The scatter plots are a 100 test results of Monte Carlo simulation and the solid lines are obtained by the analytical model. Usually, 10000 tests are used for verification purpose . The comparison of analytical results with 1000 and 10000 test results are plotted in Fig. 3.8. The analytical reliability prediction results match well with the Monte Carlo analysis in the two tests.

The redundant designs with only one more cell in each arm improve the system reliability significantly while the cost is negligible. From the manufacturer point of

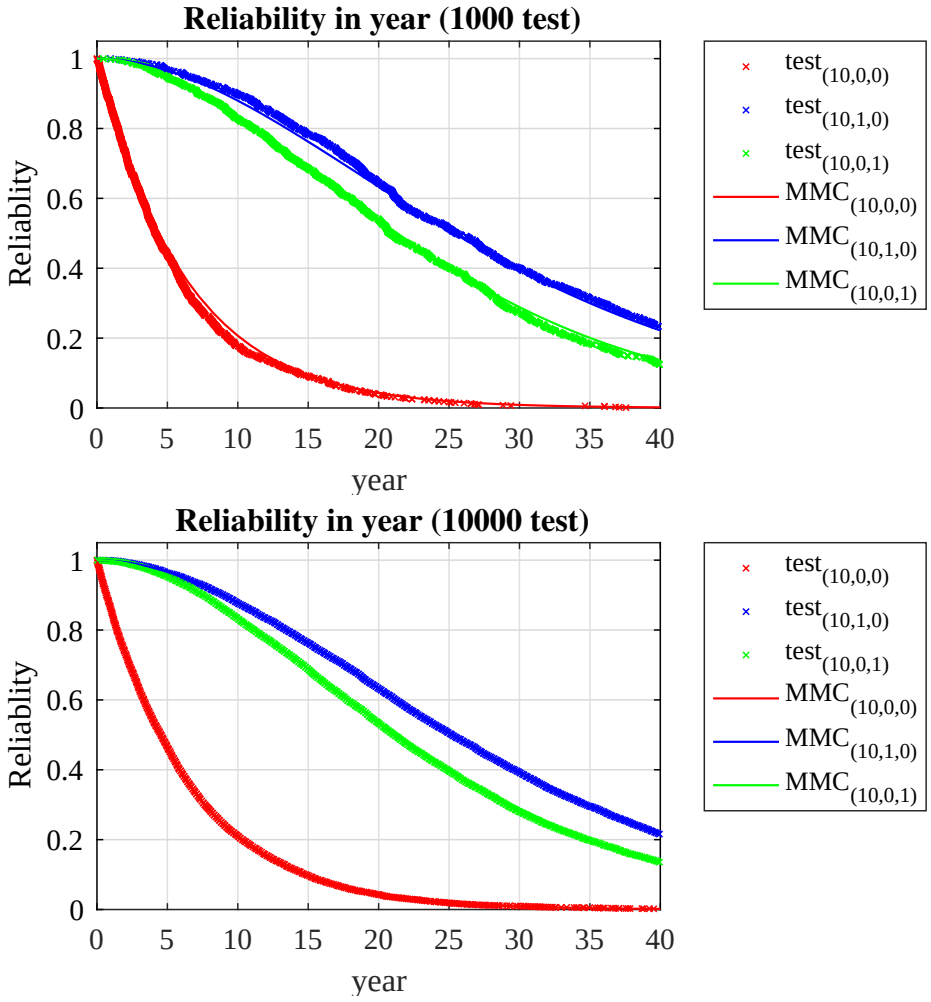


Figure 3.8. Monte Carlo simulation verification of MMC reliability modeling

view, the B10 lifetime should reach the 20/30 years requirement. This means at year 20 or 30, the MMC reliability should be higher than 0.9.

The one cell redundant designs improve the MMC reliability significantly. However, the reliability requirement is not met by the designs. To achieve reliability requirement, more redundant cells are needed. Reliability of different redundant designs with 1 to 10 redundant submodules is calculated. The reliability results of active redundant mode and standby redundant mode are shown in Fig. 3.9 and Fig. 3.10 respectively.

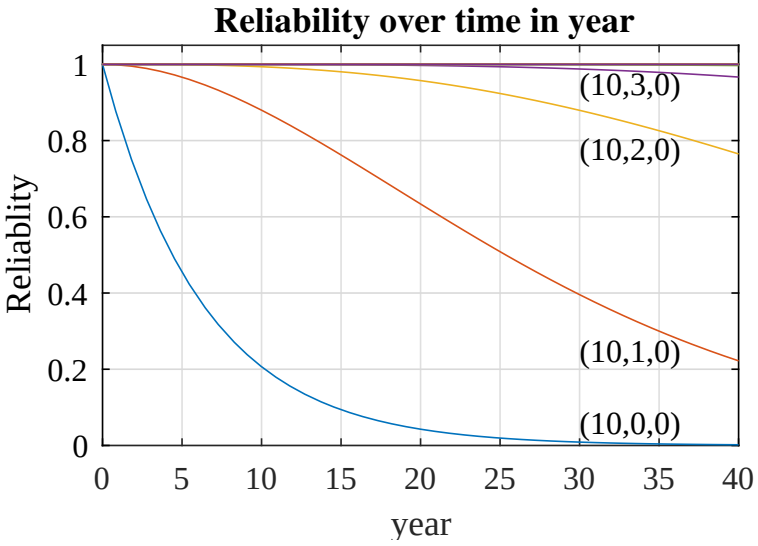


Figure 3.9. Reliability of different active redundant designs

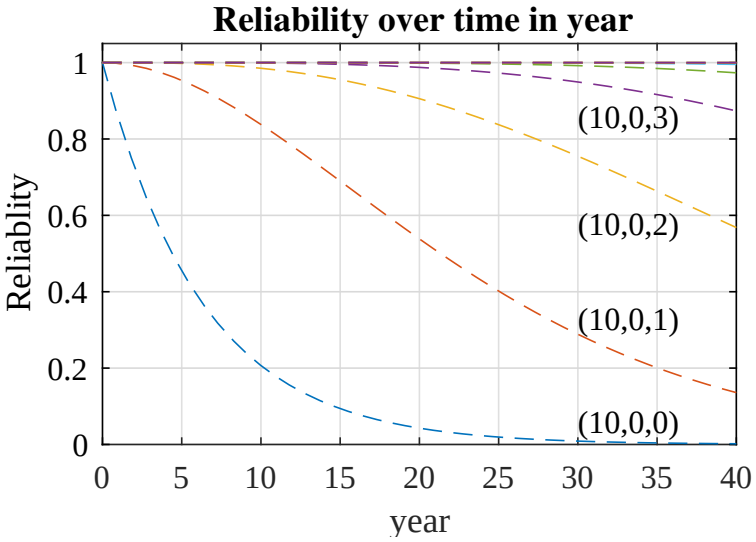


Figure 3.10. Reliability of different standby designs

A 10000 test Monte Carlo simulation for 2 and 3 redundant submodules designs are conducted. The Monte Carlo simulation results are compared with the analytical results in Fig. 3.11 and Fig. 3.12. The analytical reliability prediction results match well with the Monte Carlo analysis in the two tests.

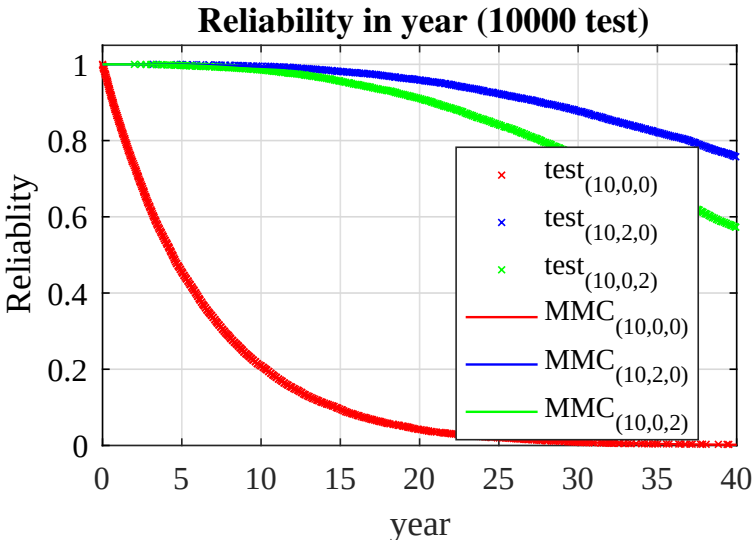


Figure 3.11. Monte Carlo verification of 2 redundant submodule MMC designs

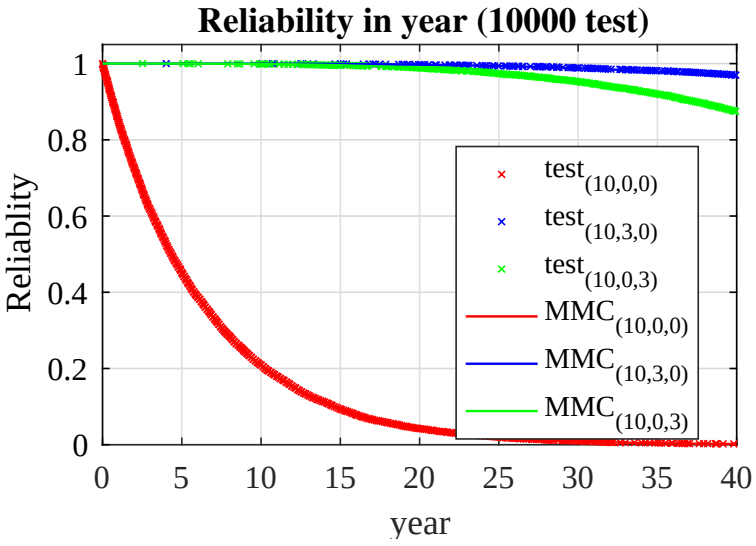


Figure 3.12. Monte Carlo verification of 3 redundant submodule MMC designs

When there are few redundant cells, with the increase of the redundant cells, the reliability of the MMC increase significantly. However, there is a saturation effect of the reliability improvement. The reliability improvement of the MMC is negligible when more than 4 redundant cells are added. But the cost still increases

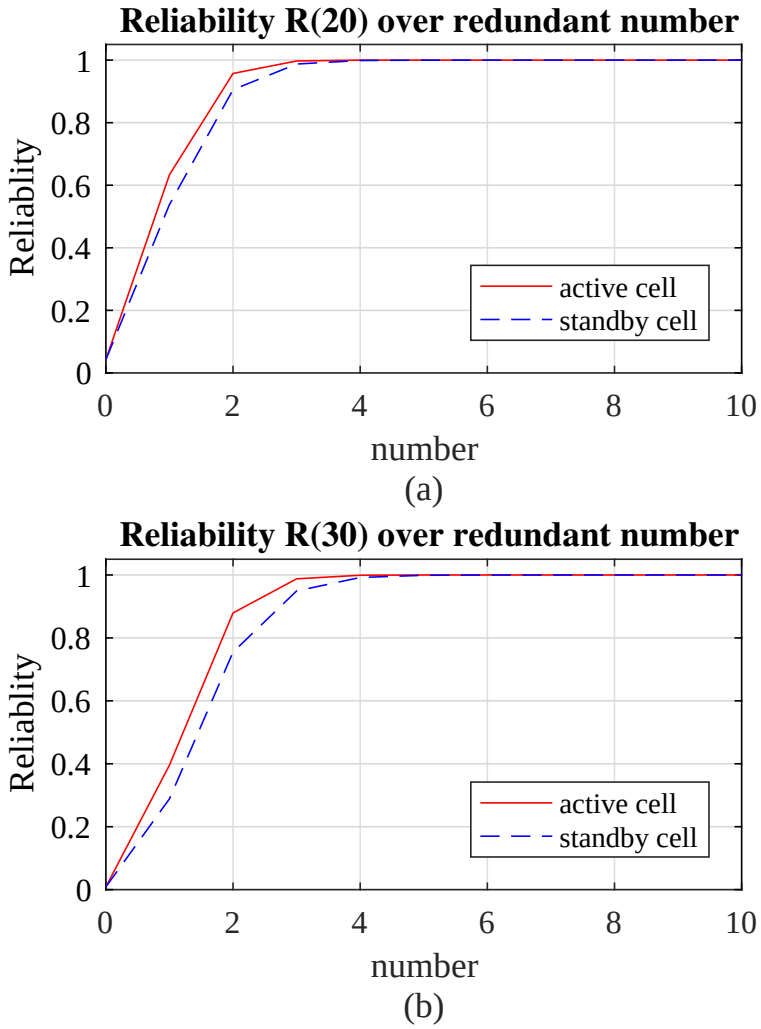


Figure 3.13. MMC reliability at year 20 and 30 with different redundant designs

if more redundant cell used.

To illustrate this saturation effect, the reliability of the MMC at year 20 and 30 with different redundant cell numbers are shown in Fig. 3.13. With redundant cells increase from 0 to 3, the MMC reliability starts increasing dramatically. But the reliability improvement is negligible with more cells added.

For the case study, to achieve a 20 year B10 lifetime requirement, 2 redundant

cells are needed for both active mode and standby mode. If a 30 year B10 lifetime is required, then at least 3 redundant cells are needed. Within the timespan of B10, a 10% return rate of product is expected. Therefore, manufacturers would select the warranty time based on this B10 lifetime index.

In summary, with this reliability analysis of redundancy, the minimum redundant cells for different reliability requirements can be identified. The more redundant cells, the higher the reliability but the cost will also increase. Another concern is the active redundant and standby redundant modes have different power losses. Therefore, a cost-effective redundancy design which ensures reliability requirements is yet to be identified. To show the influence of redundant cells cost on MMC cost, the MMC cost and its percentage change over redundancy are calculated.

Fig. 3.14 shows the estimated MMC initial cost and its percentage change over the redundant cell number. The initial cost change percentage is proportional to the redundant cell number. When redundant cell number equals to the original design, the MMC initial cost is almost double. It indicates that the redundant cells have a high impact on MMC capital cost. Since different redundancy modes utilize the same number of redundant cells, the operation modes have no impact on MMC capital cost.

Although the initial costs are the same in different redundant modes, the operating cost especially the power loss costs are different. A simplified power loss cost for 20 years 30% duty operation is shown in Fig. 3.15. The power loss cost is the product between the electricity cost and the energy dissipated by IGBT.

It can be seen that with the increasing number of redundant cells, the power loss cost increase with active mode while keeping unchanged with standby mode. In active mode, the redundant cells added are sharing the load in normal operation. Additional conduction loss of redundant cells is induced. While in standby mode, the number of submodules in normal operation is constant as redundant cells are isolated from the system. This strategy does not include any additional cell in normal operation, hence the additional power loss cost is zero. The unchanged power loss cost of standby mode is an attractive feature. The cost advantage of

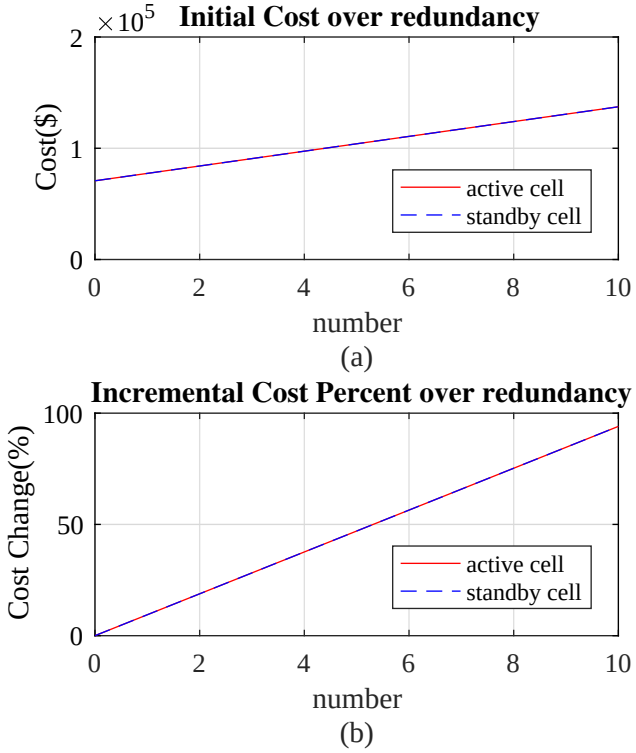


Figure 3.14. MMC initial cost over the redundant cell number

standby mode will be more significant with more redundant cells used.

The MMC system total cost and cost change percentage on redundancy are shown in Fig. 3.16. As the power loss cost is slightly higher than the component cost, the MMC system cost on redundancy tends to be affected mainly by the power loss cost. The initial cost change percentage on redundancy suggests that the additional cost of redundancy is less than 40% of original design when the redundant cell number equal to the basic cell number. If the standby mode of redundancy is adopted, the incremental cost is less than 10% to ensure the reliability requirement of a 30 year B10 lifetime.

As MMC users may have different concerns, the suitable redundant designs are application-dependent. Two applications are discussed for the case study to demonstrate the flexibility of redundant designs selection.

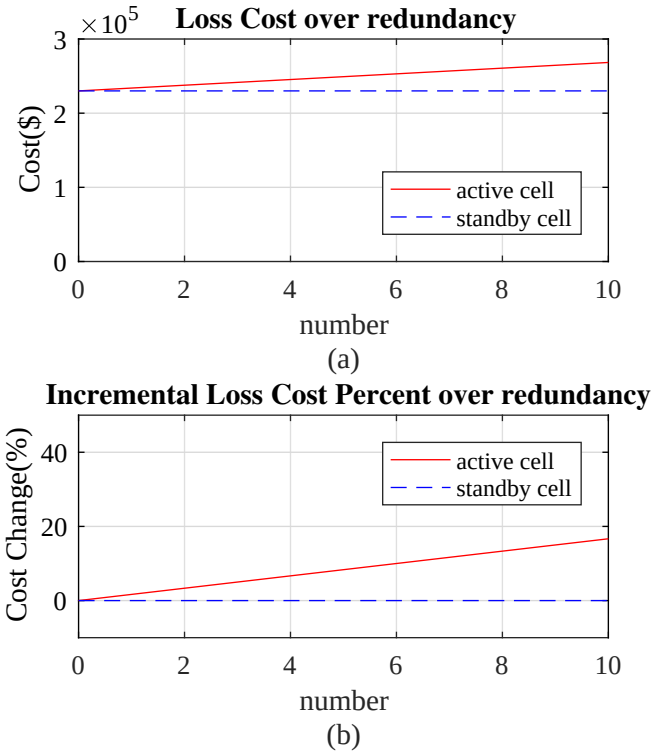


Figure 3.15. MMC operating cost over the redundant cell number

For a noncritical application such as marine propulsion, economy is the main concern. If less than 10% additional MMC system cost is the cost constraint, 2 redundant cell design is the only choice with active mode operation to meet the reliability (20 years B10 lifetime) and cost requirements, while up to 4 redundant cells can be used in standby mode. More redundant cells mean higher reliability and lower return rate. Therefore, the standby mode with 4 redundant cells is the best choice in such an application.

However, for those critical applications, standby mode operation has a underlying issue of power interruption during a fault. The seamless fault transition [76] may be required by users for some critical applications such as solid-state transform in power distribution system. In this critical application, the 2 redundant cells design with active mode operation is the best choice since the reliability requirement is

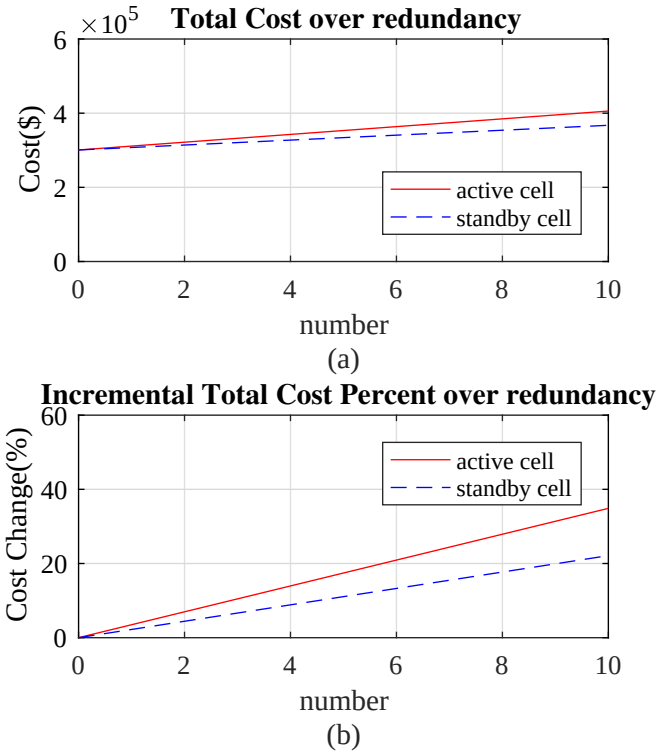


Figure 3.16. MMC total cost and cost change percentage on redundancy

met with the lowest cost.

For applications with no special requirement, the Cost of Reliability (CoR) index is proposed for cost effectiveness comparison. The CoR describes the additional cost per reliability percentage increment.

$$CoR(i) = \frac{Ct(i) - Ct}{(R_{20}(i) - R_{20})/R_{20}} \tag{3.43}$$

Where $Ct(i)$ is the total cost of a redundant design with i-th additional redundant cells, Ct is the total cost of original design, $R_{20}(i)$ is the reliability of i-th redundant design at year 20 and R_{20} is the original converter's reliability at year 20.

The CoRs for different designs are plotted in Fig. 3.17. For 2 redundant cells

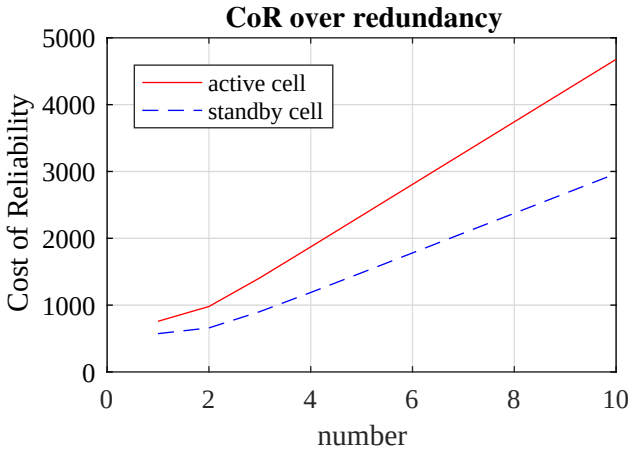


Figure 3.17. Cost of Reliability for redundant designs

operating in active mode or 3 redundant cells operating in standby mode, the cost for each reliability percentage increment is around 1000$. Hence, these two designs are comparable in cost-effectiveness. With this index, the two comparable redundant designs with different operation modes can be identified in Fig. 3.17 with a horizontal line. In this case study, as the reliability requirement is satisfied by 2 redundant cells in both operation modes according to Fig. 3.13, the standby operation mode is always preferable due to the low cost.

The reliability of MMC can be improved by redundant design and successive fault-tolerant operation. Lots of redundant designs and fault-tolerant control algorithms have been proposed while their reliability improvements are hardly quantified. In view of these, a 3MW MMC case study is conducted to demonstrate the proposed reliability and cost based redundancy design strategy. With the quantitative reliability analysis result, the redundant designs which meet the reliability requirement can be identified. In addition, the cost analysis assesses the redundancy cost impact on the MMC system cost to give the affordable choice for manufacturers. A cost of reliability concept is proposed to describe the cost-effectiveness of redundant designs and redundant strategies. With cost of reliability analysis, the cost-effectiveness can be compared for different redundancy designs.

3.5 MTTF Consumption for Time-Varying Failure Rate

Traditional failure rate methods assume a constant failure rate which can not model load variation. A Time-Varying failure rate method is proposed to take the load variation into account.

In practice, real-time load profile may not be available. A load distribution profile is usually given as shown in Fig. 3.18.

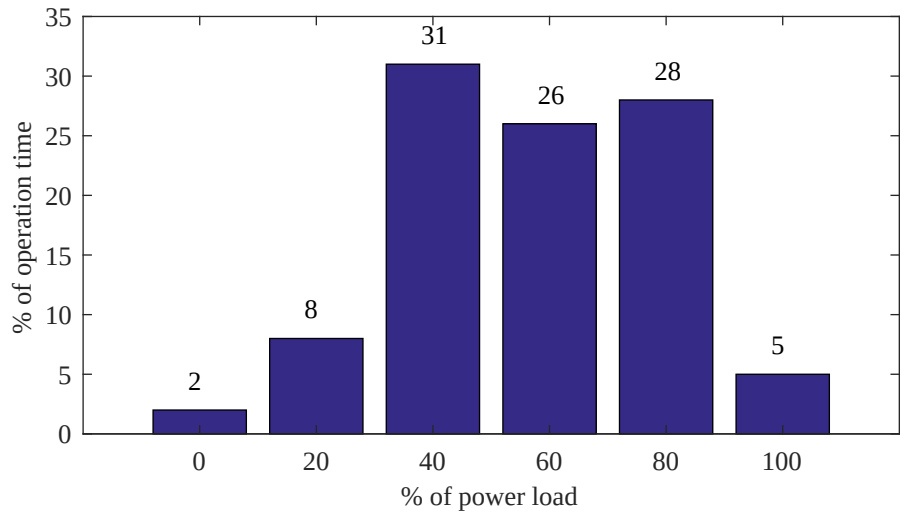


Figure 3.18. Converter load distribution profile

In Fig. 3.18, load information is collected with a 20% power interval and classified as six level from 0% to 100%. Each bar represents the duration of the load with a numeric label. For example, the third bar indicates that 31% of the operation time, the converter works at around 40% power level.

In the traditional failure rate based methods, the load factor is a duration weighted-average value of load. It is usually used as an equivalent load in reliability

analysis. For Fig. 3.18 , the equivalent load in one year can be calculated as:

$$\begin{aligned} Load_{equ} &= 8\% \cdot 0.2pu + 31\% \cdot 0.4pu + 26\% \cdot 0.6pu + 28\% \cdot 0.8p + 5\% \cdot 1.0pu \\ &= 0.57pu \end{aligned} \tag{3.44}$$

The equivalent load is $0.57pu$, the specific value can be used to adjust the load stress π factor to including the load variation into reliability modeling consideration. In this example, the per unit value of the equivalent load is the same as the load factor which is defined as the total load divided by the peak load in a specific time period. It is a measure of the utilization rate. The load factor is similar to the concept of the capacity factor of a power plant in power system, which is defined as the ratio of actual electrical energy output over a given period of time to the maximum possible energy output over the period.

With the equivalent load obtained, the equivalent failure rate can be adjusted as follows:

$$\lambda_{equ} = \frac{Load_{equ}}{Load_{base}} \cdot \lambda_{base} \tag{3.45}$$

The corresponding expected lifetime, MTTF, is the reciprocal of the equivalent failure rate. For this traditional reliability method, there are two issues. One is that the oversimplified weighted-average has an implicit assumption that the failure rate has a linear relation with the load stress. Another is that the method requires all load information to assess the reliability of the converter. These two problems make the method difficult to apply to power converters reliability analysis as failures in power converters are quite load dependent and the failure rate of components in power converters may not always have a linear relation with the load stress.

To cope with these issues, a load-dependent time-varying failure rate method is proposed. The idea is to adjust the failure rate in real-time to model the impact of load variation, and calculating the corresponding failure rate.

$$\lambda(t) = \frac{Load(t)}{Load_{base}} \cdot \lambda_{base} \tag{3.46}$$

With the real-time failure rate profile, the reliability function and MTTF can

be calculated directly.

$$R(t) = e^{-\int_0^t \lambda(t)\,dt} \tag{3.47}$$

$$MTTF = \int_0^\infty R(t)\,dt \tag{3.48}$$

The load profile in Fig. 3.18 is used to demonstrate the proposed load-dependent time-varying failure rate method. Load duration profile rearranges load level in a descending order reflecting cumulative duration information. Assume a real-time load profile is the load duration profile. The pseudo real-time load profile is plotted in Fig. 3.19. Whenever there is a real-time load profile available, the pseudo load profile can be replaced and the calculation of reliability remains the same.

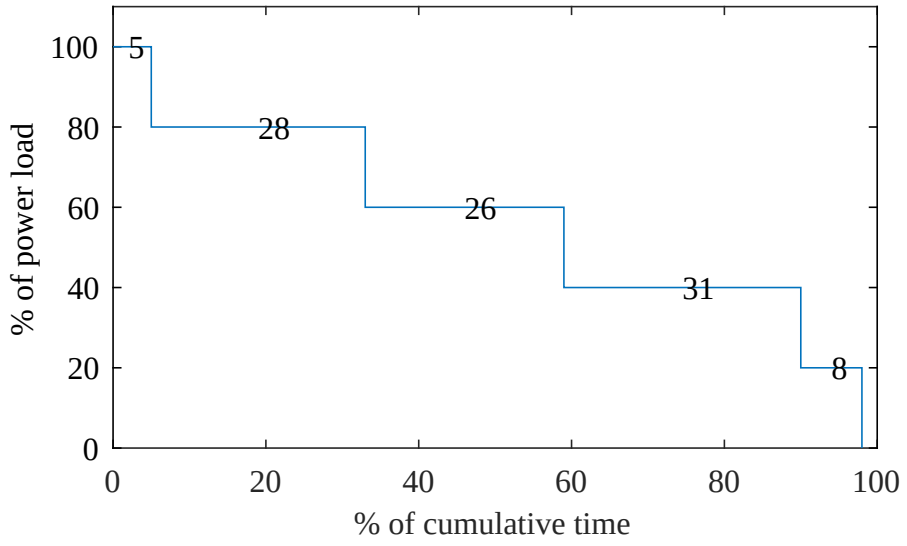


Figure 3.19. Pseudo real time load profile

Referring to equation (3.47), it is hardly to obtain the complete failure rate profile $\lambda(t)$ for reliability evaluation. Therefore, the concept of expected lifetime consumption, or MTTF consumption is proposed to tackle the incomplete failure rate profile problem.

The idea is that, for a very small time interval Δt, the load is constant denoted as $Load_i$. The corresponding failure rate can be calculated and denoted as λ_i. The

expected lifetime corresponding to this specific failure rate can be calculated and denoted as $MTTF_i$. Then in this time interval, the consumed expected lifetime caused by the $Load_i$ can be represented by the ratio between the actual time elapsed t_i and the expected lifetime $MTTF_i$ it can operate under this load condition.

There are 3 steps to apply the MTTF Consumption (MTTFC) to model converter reliability.

1. Calculating failure rate function:

$$\lambda(i) = \frac{Load(i)}{Load_{base}} \cdot \lambda_{base} \tag{3.49}$$

2. Calculating MTTF Consumption:

$$MTTFC(i) = \frac{t_i}{MTTF_i} = t_i \cdot \lambda_i \tag{3.50}$$

3. Accumulate Total Expected Lifetime Consumption:

$$MTTFC_{total} = \sum_{i=1}^{k} MTTFC(i) \tag{3.51}$$

The MTTF Consumption calculated for the example are shown in Fig. 3.20.

The distinguished advantage of this method is that, during the actual operation, only the past load information data is needed. This advantage is shown in Fig. 3.21.

The red line in Fig. 3.21 are past load profile recorded. The total MTTF consumption is 27.4% in the past.

3.6 Conclusions

This chapter reviews some redundancy modeling methods in probability theory and adapts them for multilevel converters. Detailed derivations of redundancy formulas are presented for better understanding. Multilevel converter redundancy

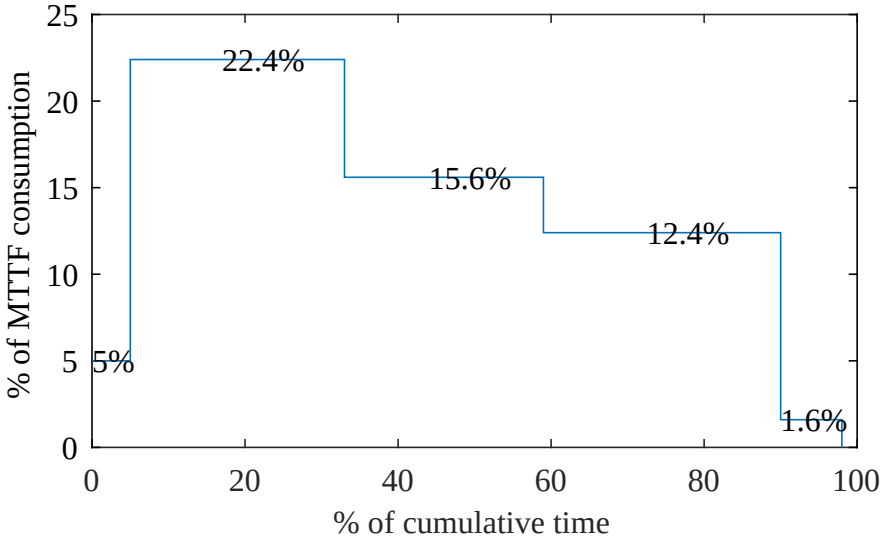


Figure 3.20. MTTF Consumption with known full load profile

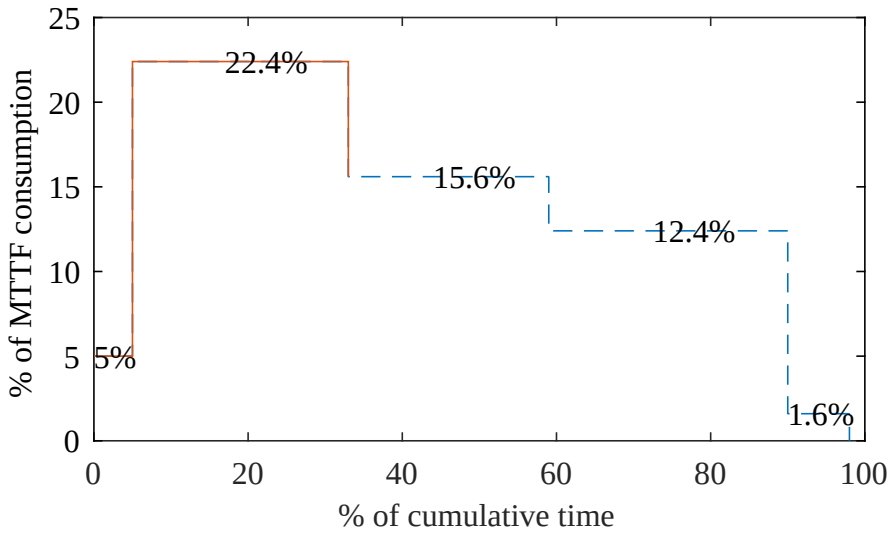


Figure 3.21. MTTF Consumption with only past load profile

capabilities are defined and quantified in reliability point of view. The reliability performance of multilevel converters with different redundancies are reassessed accordingly.

With redundancy modeling techniques, reliability- and cost- based redundancy design guideline is proposed and demonstrated with a case study of Modular Multilevel Converter (MMC) redundancy design. In this case study, load-dependent failure rates are used to model the MMC reliability. The case study results show that MMC reliability can be improved significantly with just a few backup submodules. However, the practical redundancy design depends on different applications and different users (manufactures or end-users), which are demonstrated with two cases in Section 3.3.

The load-dependent failure rate method in the MMC case study uses the equivalent load by averaging load profile over time, while the actual time-varying load is not modeled. To cope with this issue, a load-dependent time-varying failure rate technique is proposed to model the varying operating condition in real time.

To overcome the difficulty of calculating MTTF with time-varying failure rates, a new reliability index, expected lifetime (i.e., MTTF) consumption taking real-time variable load into consideration, is proposed to model the state of health for power converters. Subsequently, a systematic reliability modeling method is developed based on the proposed load-dependent time-varying failure rate and expected lifetime consumption techniques.

Chapter 4

Probabilistic Physics of Failure Method

4.1 Introduction

Physics of Failure (PoF) based reliability modeling methods which focus on failure mechanisms of electrical components draw lots of attention in the power electronics community recently. The PoF methods are advocated by integrated circuit (IC) industry for its clear physical meaning. The methods calculate the lifetimes of components by accumulating fatigue damage under a specific mission profile. An accurate lifetime can be obtained for each component, and the converter lifetime is determined by the component with the least lifetime.

However, the inherent probabilistic property of reliability is lost as uncertainty and randomness are not modeled by the deterministic physics of failure method. To cope with this issue, normal distributions of component parameters are used to simulate the manufacturing process. Tens of thousands virtual components are 'manufactured' by randomly sampling component parameters from normal distributions. Components lifetime can then be calculated by deterministic PoF methods. The reliability function of the component can subsequently be obtained

by the lifetime distribution. The reliability of the multilevel converter can be computed with the well-established statistical techniques in Chapter 2.

A probabilistic Physics-of-Failure method is proposed based on the normal distribution assumption of component parameters. The proposed hybrid physics and statistics method bridges the gaps between the component PoF methods and the system-level reliability and redundancy modeling.

In this chapter, the existing deterministic PoF methods are discussed in detail with a case study of Cascaded-H Bridge (CHB) multilevel converter. Key steps in PoF methods are presented. The drawbacks of PoF method are summarized. The proposed probabilistic PoF method is also presented with a case study of converter system level reliability and redundancy modeling.

4.2 Deterministic Physics of Failure Method

Fig. 4.1 shows the flowchart of the deterministic PoF method.

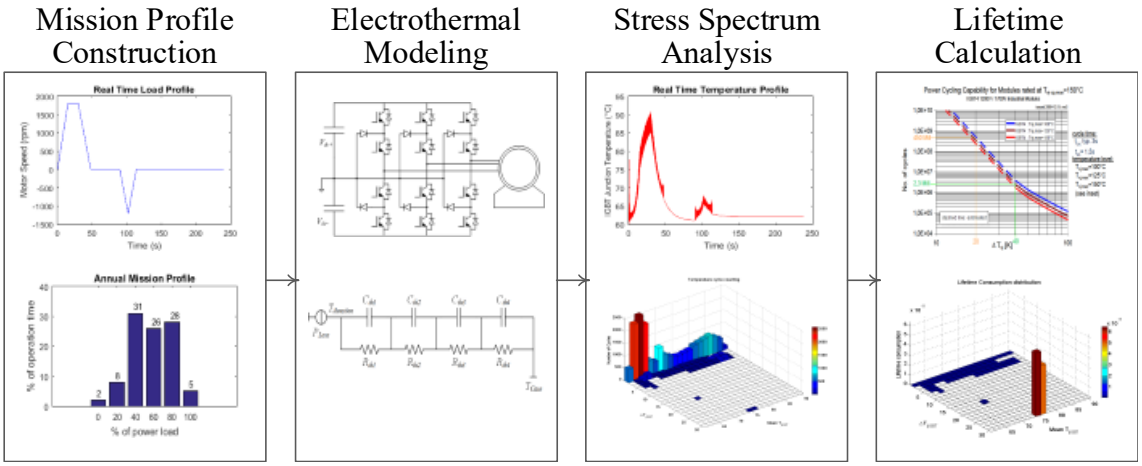


Figure 4.1. Flowchart of physics of failure analysis

The key steps are summarized and briefly explained below.

1. Mission Profile Construction

   (a) High resolution load profile is preferable

   (b) Mission Profile reconstruction from limited data

2. Electrothermal Modeling

   (a) component loss determination

   (b) thermal network modeling

3. Stress spectra analysis

   (a) thermal stress: temperature cycling is the main fatigue mechanism

   (b) cycling counting methods

4. Lifetime calculation

   (a) Lifetime models

   (b) Damage accumulation rules

The PoF methods mainly focus on the stress and damage analyses. With component damage obtained under a mission profile, the expected lifetime can be determined.

In PoF methods, the total damage on component closely relates to the actual mission profile. A high-resolution mission profile is preferable to include kinds of stresses. But in practice, the mission data may have a very low sampling rate. For example, a 30min/sample is much longer than converter time constant in milliseconds. Some interpolation techniques are needed to reconstruct the mission profile to match the converter dynamics.

For a given electrical system, system operators would generate load power command regularly to form a mission profile. Each command may have different stresses for components in power converters. A detailed converter electrothermal model is needed to map the each command to thermal stress. By doing so through analytical analysis or simulation, the thermal stress information in the time domain can be obtained.

In power converters, the thermal stress is the temperature cycling. The time domain temperature cycling data contain kinds of cycles with the different magnitude, period, and mean value. Time domain temperature cycles should be analyzed to extract the temperature spectrum. Proper cycle counting methods are needed. The cycle counting algorithm will be discussed in detail in the following section.

After the temperature cycle spectrum is obtained, the corresponding damage of each stress cycle can be calculated. If the damage is assumed to be accumulated linearly, the total damage can be attained by summation of each damage. Nonlinear damage accumulation algorithms can also be used to model an accelerated fatigue process.

The 4 key steps in deterministic PoF method will be explained in detail with a CHB converter demonstration. The problems of the deterministic PoF method will be discussed and followed by the proposed solution to the problem.

A Cascaded H-Bridge (CHB) converter is designed for a 6.7MW motor drive system. Its schematic diagram is shown in Fig. 2.18. The parameter of the converter is listed in Table 4.1.

Table 4.1. CHB converter key parameters

Parameter	Symbol	Value	Unit
Switching Frequency	f_s	600	Hz
Cell Number in each phase	N	6	–
DC Capacitance of each cell	C_{dc}	10	mF
Rated Cell Voltage	V_{dc}	990	V
Rated Motor Power	P_{mr}	6.7	MW
Motor Speed reference	r_m	1800	rpm
Rated Motor Torque	T_m	3500	Nm
Rated Motor Voltage	V_m	6.6	kV
Motor Normal Flux	ψ_m	14	Wb

1. Mission Profile Construction

   In this CHB converter based motor drive system demonstration, a self-defined real-time 240-second speed mission profile is used. The speed profile in Fig. 4.2 consists of motor four-quadrant operation, forward motoring, forward braking, reverse motoring, and reverse braking. The perfect match between the measured speed and the reference speed shows that the Field Oriented Control (FOC) gives a favorable speed tracking performance. For an actual motor drive system PoF reliability analysis, real speed mission profile can be used.

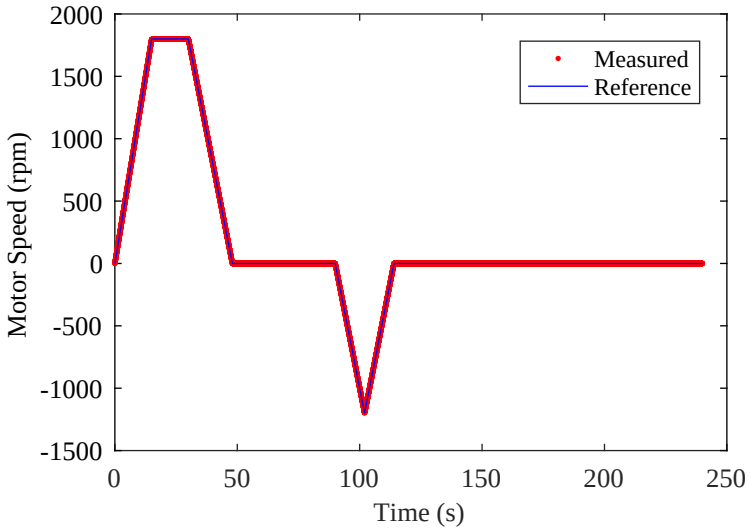


Figure 4.2. Mission profile of a motor drive

Fig. 4.3 shows the motor voltage and current waveforms in starting duration. The motor starting current inrush is well controlled.

Fig. 4.4 gives the filtered voltage and current waveforms during motor stable operation at full power.

2. Electrothermal Modeling

   (a) component loss determination

   To determine the thermal stress of components and converter, elec-

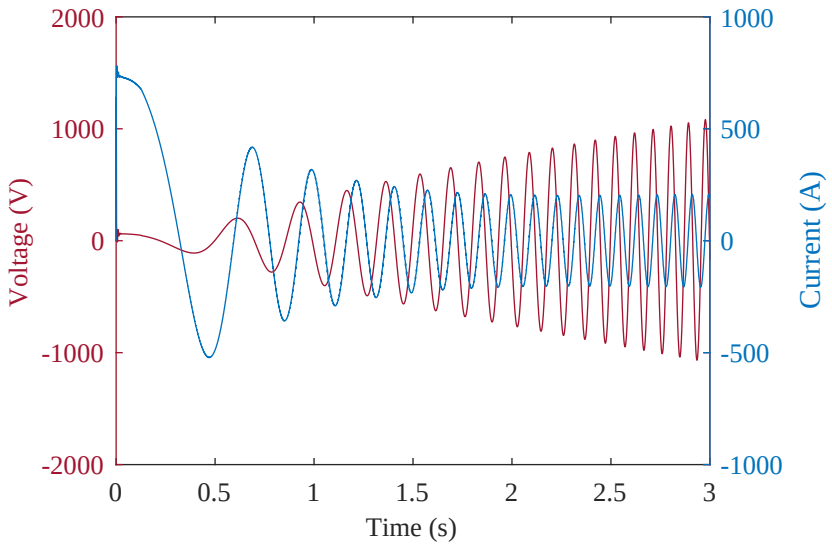


Figure 4.3. Motor starting voltage and current

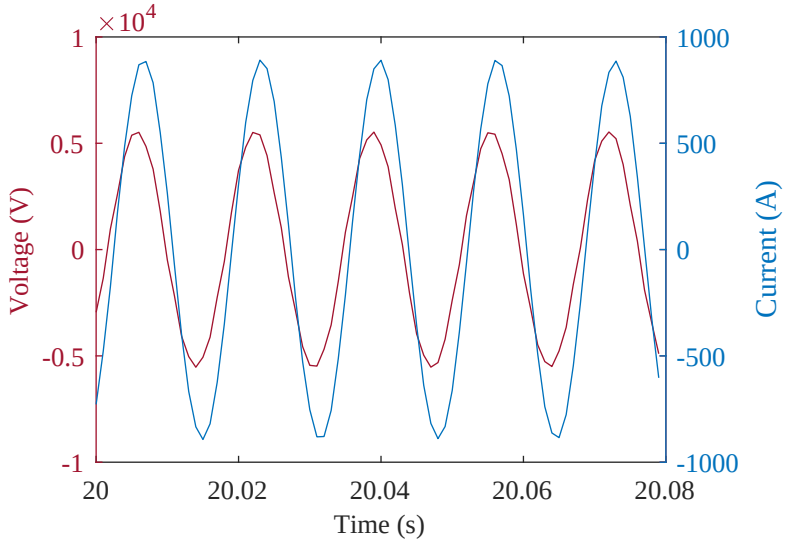


Figure 4.4. Motor stable operation voltage and current at full power

trothermal models are needed. Traditional simulations of converters only focus on system controller functionality and performance. Little attention had been paid to devices losses and thermal simulations. The converter loss and thermal modeling will be discussed in the following contexts.

Some simulation softwares/packages only use equivalent resistance to model the component loss. However, for power semiconductor components which are working in high-frequency switching states, the switching losses also contribute a lot to the system total loss. To model the switching loss, both analytical method and simulation method are acceptable.

To accelerate simulation of electro-thermal models, detailed IGBT physical models will not be used. A power loss lookup table which can be obtained in datasheet or by experiments will be used as the loss model for an IGBT [77]. A typical lookup table is shown in Fig. 4.5.

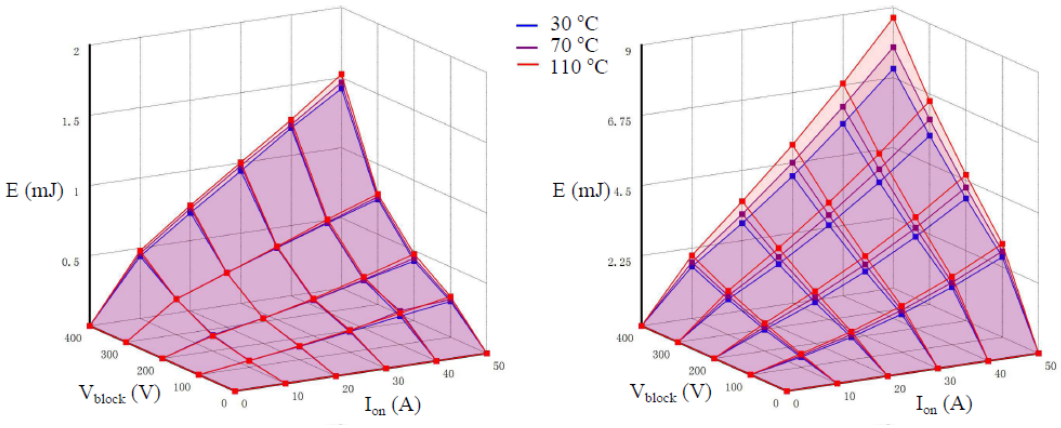


Figure 4.5. IGBT turn-on and turn-off loss lookup table

For capacitor thermal modeling, the dissipation factor, also known as the tangent of loss angle, will be used to model the power loss in a capacitor. The power loss can be obtained with this model by calculating power consumption in ESR (equivalent series resistance) and leakage resistance. In practice, the power loss in leakage resistor is negligible.

(b) thermal network modeling

Temperature affects the behavior of power semiconductor devices considerably, since many of their properties are strongly temperature dependent. Therefore thermal models for an IGBT module and heat sink are required to simulate the device junction temperature during operation. The propagation of heat in a system can take place in three different ways, convection, radiation or conduction. In solid materials, such as electronic devices, conduction is the dominant heat transfer mechanism. There are two interchangeable thermal networks for heat transfer modeling, Caucer network and Foster network which are shown in Fig. 4.6.

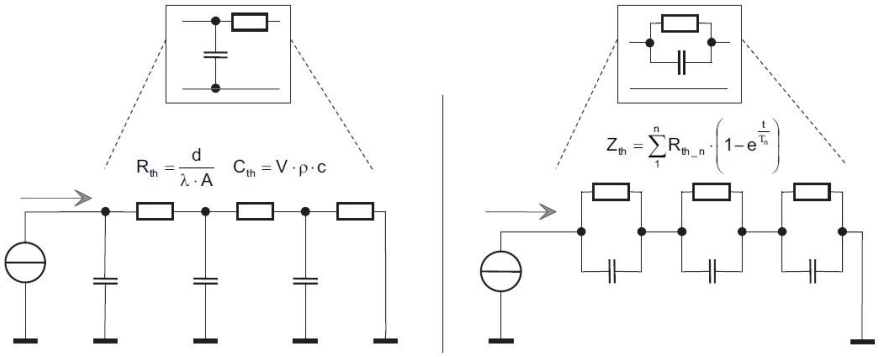
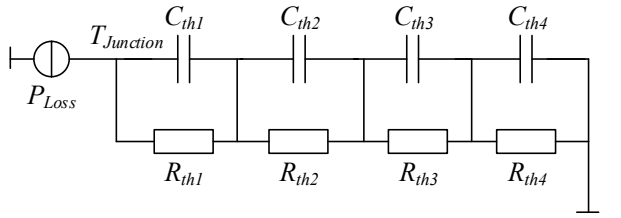


Figure 4.6. Cauer thermal network and Foster thermal network

The Cauer network, although it is mathematically complicated, refers to the physics of equivalent circuit diagram of heat conduction and is the only network that is able to describe the internal temperature distribution of the system correctly. In the PoF methods, only the IGBT and diode junction temperatures are of interest, hence another equivalent Foster network is used.

A lumped fourth order Foster thermal network which is shown in Fig. 4.7 is used to model the heat dissipation network from the junction to case. The IGBT and diode chip pair is normally optimized in layout without thermal coupling. The heat sink is assumed well designed that can

maintain its temperature at 60 °C at rated power. The Foster thermal network parameters can be obtained in the datasheet and verified by thermal test. The heat sink parameters obtained in the datasheet can also be verified by thermal test. The thermal network from capacitor core to the heat sink can also be modeled as Foster thermal network.



i:	1	2	3	4
$R_{thi\ [mK/W]}$:	0.8	3.7	17	2.5
$\tau_{i\ [s]}$:	0.0008	0.013	0.05	0.6

Figure 4.7. IGBT lumped fourth order Foster thermal network

3. Stress spectra analysis

   (a) thermal stress profile

   The temperature profile of one IGBT under a 240-second motor speed mission profile (see Fig. 4.2) is shown in Fig. 4.8.

   The large temperature swing is due to large variation of speed command. There are many small temperature swings due to the switching of IGBT. The capacitor core temperature is relatively more stable due to an over-sized design for voltage ripple consideration.

   (b) cycling counting methods

   There are several methods available to count cycles in irregular stress-versus-time profile, such as the level crossing counting method, peak counting method, simple range counting method, and rainflow counting method. For the level crossing method, the range between the maximum and minimum amplitudes of the stress profile is divided into discrete interval levels above and below the mean stress. A count is recorded

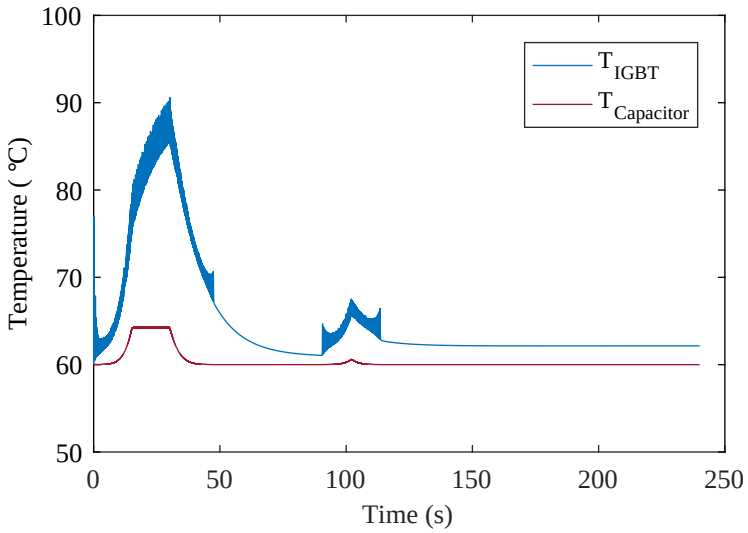


Figure 4.8. Temperature profile of IGBT and capacitor

whenever the stress profile crosses a preset level above or equal to the mean stress with a positive slope or a level below the mean stress with a negative slope [78].

Restrictions are needed to avoid small variations around the level to be counted which will lead to a large number of counts. This can be done by filtering the small noise prior to cycle counting or by ignoring the crossing until the adjacent next level is crossed. The counts are then combined to form completed cycles by first constructing the largest possible cycle within exist counts until all counts are used. Obviously, this method only gives the statistical summary of the stress amplitudes and consequently does not represent the actual stress profile.

The Rainflow algorithm in standard ASTM e1049-85 will be used [78]. Rainflow counting method is one of the most popular cycle counting techniques used in fatigue analysis [79]. Cycles counted by this technique correspond to the fully closed hysteresis loops in the temperature profile, which is the physical basis of this method. Fig. 4.9 shows a stress profile and the hysteresis loops of the stress.

As the material deforms from point A to D, it follows the path as shown

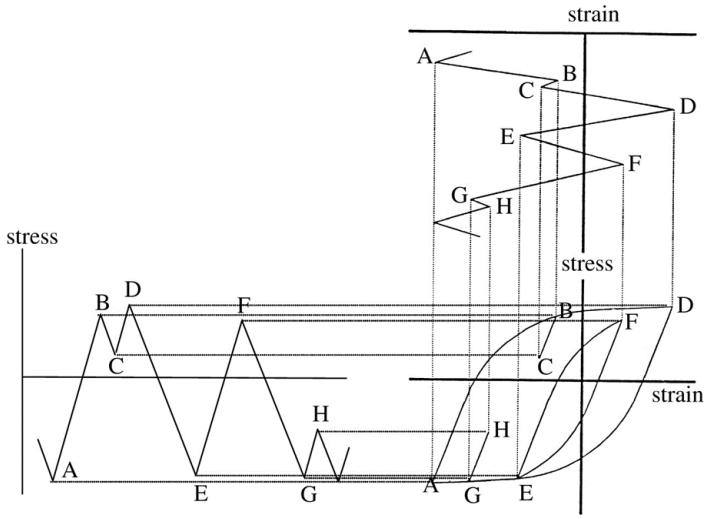


Figure 4.9. Rainflow counting method

in the hysteresis loop. For small stress cycles such as B to C, the stress is released slightly at point B and the material elastically shrinks to point C. When the stress increases from C to D, the material first remembers its prior history and elastically deforms to point B. After passing point B, the plastic deformation continues along path A to D as if the stress release from B to C never occurred. For large stress cycles such as E to G where the stress is reversed, plastic deformation occurs and appears as a small hysteresis loop within the large one. This indicates the fatigue damage appearing during the stress cycle E to G.

By using the Rainflow counting method, the temperature swings spectrum can be obtained. Figure 4.10 is the temperature cycle counting results of the 240 seconds operation.

4. Lifetime calculation

   (a) lifetime models

   The analytic IGBT lifetime model expresses the number of cycles to failure as a function of a stress. the modified Coffin-Manson model is

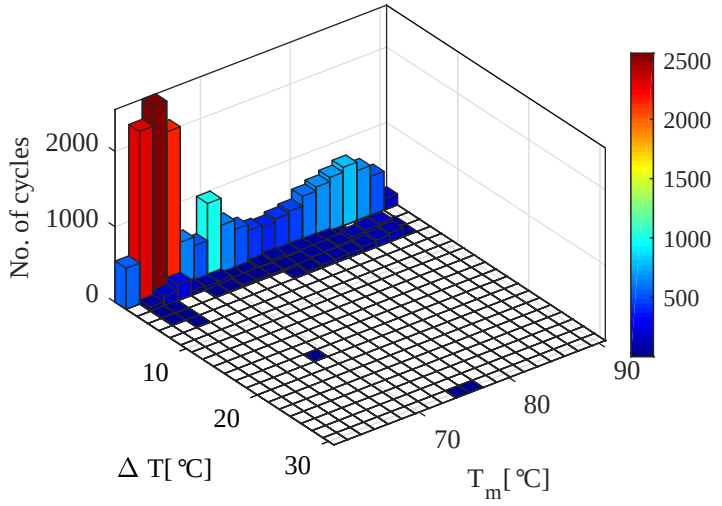


Figure 4.10. Temperature cycle counting results

usually used for estimate lifetime due to fatigue. The general Coffin-Manson lifetime models have been described in detail in chapter 2.

The general form of modified Coffin-Manson model in equation (2.48) is rewritten as:

$$N = A \times (\Delta T)^{-b} \times e^{E_a/(k_B \cdot T_m)} \tag{4.1}$$

where T_m is the mean temperature of a cycle, k_B is Boltzmann constant and E_a is activation energy. The parameters of this modified Coffin-Manson model can be extracted from datasheet by data fitting.

A typical power cycling capability curves of IGBT module is shown in Fig. 4.11.

The parameters of Coffin-Mansion model can be obtained by the least square curve fitting. The curve fitting results are shown in Fig. 4.12

The IGBT lifetime model from the curve-fitting result is:

$$N = \begin{cases} 1.2424 \times 10^{15} \times (\Delta T)^{-7.09} \times e^{2449.6/T_{max}} & \Delta T \leq 40\,^{\circ}\mathrm{C} \\ 5.8092 \times 10^{9} \times (\Delta T)^{-3.8} \times e^{2449.6/T_{max}} & \Delta T > 40\,^{\circ}\mathrm{C} \end{cases} \tag{4.2}$$

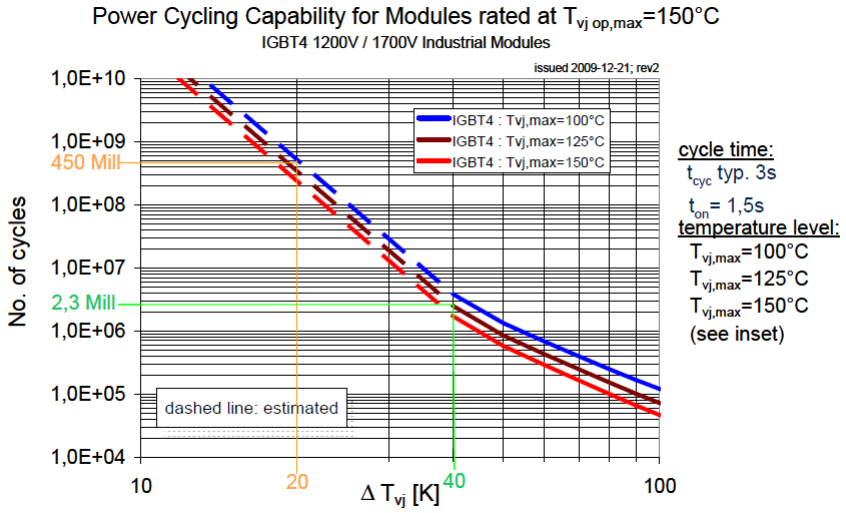


Figure 4.11. Power cycling capability for Infineon IGBT modules

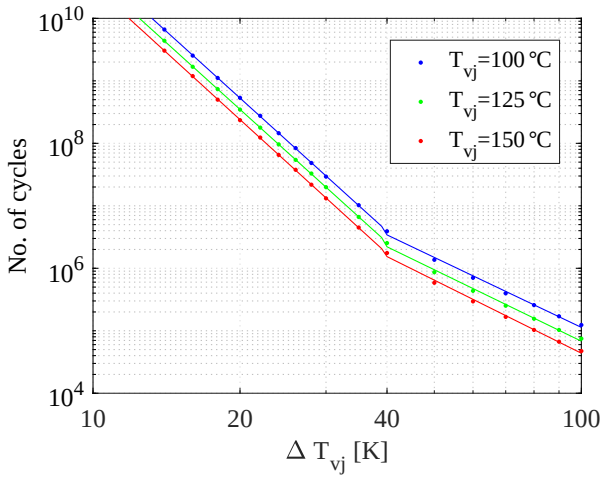


Figure 4.12. Curve-fitting for Infineon IGBT module lifetime model

where T_{max} is max temperature of a cycle. A scaling factor S_f related to temperature cycling period is suggested to adjust the life cycle.

$$S_f = (\frac{t_{on}}{1.5})^{-0.3}, 0.1s < t_{on} < 60s \tag{4.3}$$

(b) damage accumulation rules

Since the Coffin-Manson law gives the lifetime of a material under a

constant stress, some accumulation rule is needed to calculate total damage to the material under changing stress. One of the widely used cumulative damage calculation rule is Miner's rule as it is the simplest rule assuming a proportional effect of various stress. It states that if there are k different stress levels and the average number of cycles to failure at the i_{th} stress, S_i, is N_i, then the damage fraction, or lifetime consumption L_C, is:

$$L_C = \sum_{i=1}^{k} \frac{n_i}{N_i} \tag{4.4}$$

where n_i, is the number of cycles accumulated at stress S_i, L_C is the fraction of life consumed by exposure to the cycles at different stress levels. In general, when the damage fraction reaches 1, failure occurs.

The corresponding lifetime consumptions of each combination of temperature swing and mean temperature can be calculated with an established lifetime model, such as the modified Coffin-Mansion lifetime model. The lifetime consumption results are shown in Fig. 4.13.

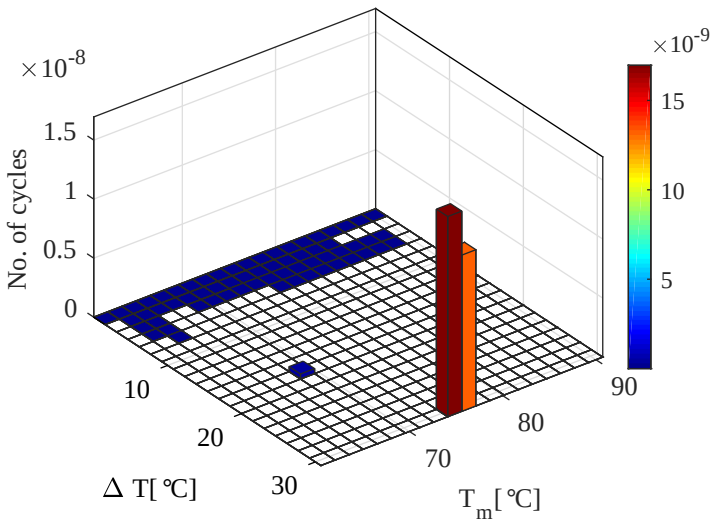


Figure 4.13. Lifetime consumption distribution

The lifetime consumption distribution shows that large temperature swings contribute to most of IGBT damages. To improve the lifetime of IGBT, a cost-effective way is to optimize the thermal design to reduce the junction temperature swings. Another way is to optimize IGBT switching loss by carefully designing the gate driver.

The total lifetime consumption of IGBT under the mission profile is $3.0672 \cdot 10^{-8}$. If the mission profile is repeated to form the future load profile, the expected life cycle is $1/(3.0672 \cdot 10^{-8}) = 3.2603 \cdot 10^{7}$. The expected lifetime is the product of mission profile period and expected life cycle, i.e., $3.2603 \cdot 10^{7} \times 240\text{s} = 2.1735 \cdot 10^{6}$ hours=248.1204 years.

Similarly, the capacitor lifetime can be calculated. The AVX TRAFIM high power film capacitor is used in the case study. The fitted lifetime model is given by,

$$L = 1.2002 \times 10^{6} \times (\frac{V}{V_0})^{-16.65} \times e^{317.6 \cdot (\frac{1}{T_c} - \frac{1}{T_0})} \tag{4.5}$$

The the datasheet specifies a 100,000 hours lifetime at 80 °C. Assuming a unity voltage ratio term, the calculated lifetime is 45.9709 years. In the deterministic PoF method, the expected converter lifetime is determined by the component with the least lifetime. Hence, the expected converter lifetime in this case equals the capacitor lifetime, 45.9709 years.

In practice, the temperature swing of IGBT junction may be much higher than the 30 °C in this simulation. The field lifetime may be less than the estimated. For example, if air-cooling is used in the case study to replace the water-cooling, the thermal resistance may increase by up to 20%, resulting a much higher mean temperature and a larger temperature variation. In this case, the total lifetime consumption of IGBT under the same mission profile is 1.6992×10^{-7}. The expected life cycle is 5.8853×10^{6}, and the expected lifetime is, 3.9235×10^{5} hours=44.7891 years. To improve the estimation accuracy, the real mission profile can be included and the thermal network parameters should be validated first.

The PoF method gives the deterministic lifetime of each component. The

lifetime of the converter is determined by its shortest comportment lifetime. The PoF method is suitable for end-user to analyze the specific converter with detailed converter parameters and mission profile.

However, for converter manufactures, a warranty period should be given to a batch of converters. Usually, the warranty period is given at which a 10% return rate occurs for economical and reputation considerations. The lifetime statistics of a batch of converter are necessary for manufactures. The probabilistic properties of reliability are not appearing in the deterministic PoF method, which thus fails to give a guideline to decide warranty period.

4.3 Probabilistic Physics of Failure Method

To overcome the shortcomings brought by PoF method, for multilevel converters, a probabilistic PoF method is proposed which also helps to model the converter redundancy in system level reliability assessments. The probabilistic PoF method constructs the lifetime distribution of components considering component parameter uncertainties. Hence, the reliability function of each component can be calculated for redundancy modeling and system level reliability evaluation.

One of the uncertainties is the IGBT turn-on voltage drop (V_{ce_sat}) which determines the conduction loss of IGBT. Table 4.2 shows the turn-on voltage drop variation of an IGBT under different junction temperature (T_{vj}) specified by manufacture technical datasheet.

It is easy to know from the table that, for the qualified IGBTs, their on-voltage variation can be as high as 30% while the typical value is usually used in reliability analyses. As most manufacture uncertainties follow the normal distribution, a normal distribution of on-voltage can be assumed to simulate the diversity of a batch of IGBT. For example, at $T_{vj} = 125\,°\mathrm{C}$, the on-voltage typical value is 2.15 and the maximum value is 2.75. A normal distribution with the typical value as the mean value can be used to describe the the IGBT on-voltage distribution. A three standard deviations, 3σ, which includes 99.73% of the sample population in

Table 4.2. IGBT turn-on voltage drop variations

Parameters \ T_{vj}	$T_{vj} = 25\,°C$	$T_{vj} = 125\,°C$	$T_{vj} = 175\,°C$
V_{ce_sat} typical	1.75	2.15	2.35
V_{ce_sat} max.	2.30	2.75	3.00
Variation %	31.42%	27.91%	27.66%

a normal distribution, is selected to cover the value range from 2.15 to 2.75. A simulated on-voltage drop V_{ce_sat} distribution histogram of 10000 IGBTs is shown in Fig. 4.14. A distribution curve fitting of the simulated results is shown in red line with mean and standard deviation highlighted.

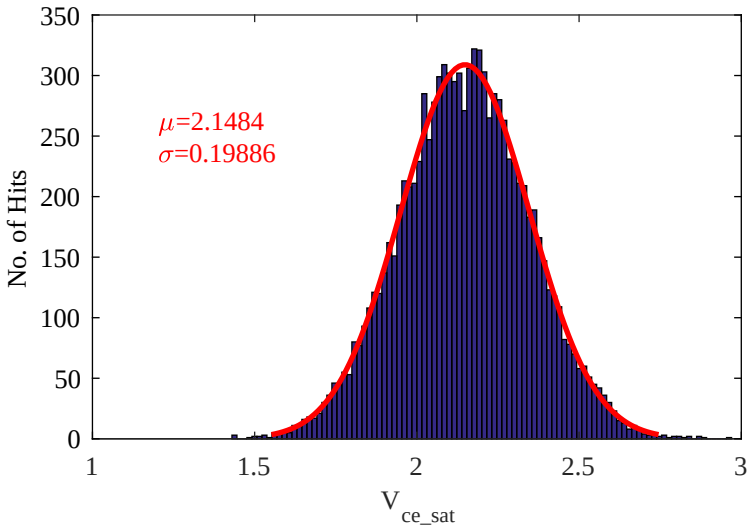


Figure 4.14. IGBT on-voltage drop V_{ce_sat} distribution

The switching loss and thermal impedance parameters which are shown in Fig. 4.15 with red color may also have some degree of uncertainties and also follow normal distributions. For actual components operating in multilevel converters with a given mission profile, all these intrinsic parameter variations result in different

component and submodule lifetimes.

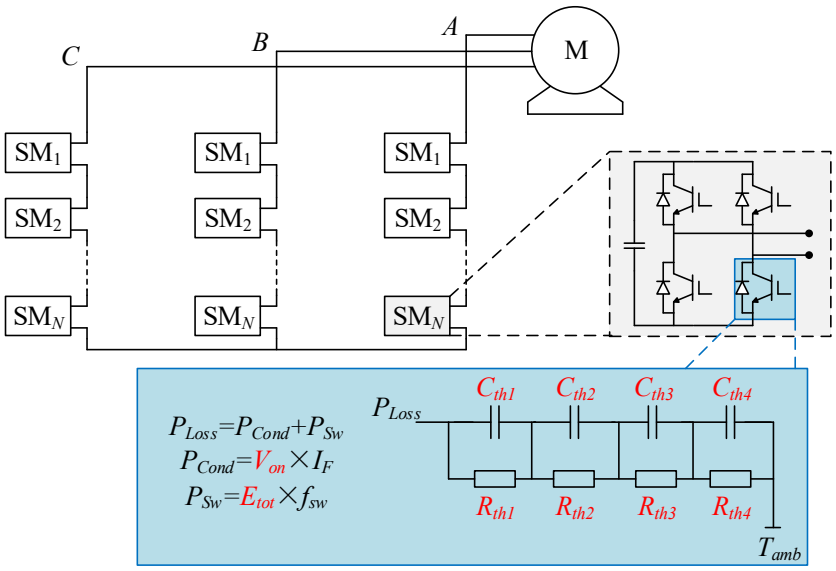


Figure 4.15. Power semiconductor parameters with uncertainties

Another source of uncertainty comes from the lifetime models which are extracted from limit samples. The highlighted parameters in lifetime model equation (4.6) are curve-fitted from the lifetime data of samples. The uncertainties of these parameters should also be modeled. A normal distribution can be used to model the uncertainties of these parameters. The actual distribution of these parameters can be accessed from manufactures if possible.

$$N = A \times (\Delta T)^{-b} \times e^{E_a/(k_B \cdot T_m)} \tag{4.6}$$

A Monte Carlo simulation which randomly select the power component parameters from normal probability distributions is used to simulate the actual manufacturing of power components. The lifetime of virtual components in a multilevel converter can be calculated by the PoF method. With a set of virtual components, the component lifetime distribution can be obtained by probability distribution curve fitting.

The proposed probability Physics-of-Failure method starts with the components variation distribution modeling, and then construct a set of virtual components to obtain the lifetime distribution and thus reliability function of components.

4.4 Cascaded-H Bridge Converter Reliability Analysis Case Study

The deterministic PoF method in Section 4.2 estimates that the CHB has a 44.7891-year life expectancy under air cooling condition.The CHB converter reliability is reassessed in this section with the proposed Physics-of-Failure method. The assessment includes the following steps.

1. Repetitive deterministic PoF analyses for virtual components.
   As explained in Section 4.2, the IGBT reliability function can be obtained by collecting the lifetime data of virtual IGBTs with randomly selected parameters. The lifetime of each virtual IGBT can be calculated with the deterministic PoF method. For easy implementations, it is not necessary to conduct the PoF analyses repetitively for all the randomly generated virtual components. There are two techniques which are recommended to simplify the analyses for engineering practitioner while maintaining the accuracies in an acceptable ranges. One technique is to select some representative virtual components. For example, there are 10000 randomly generated values of V_{ce_sat} in Fig. 4.14. The 10000 values are classified into around 100 groups which are the bars in the histogram. Hence only around 100 times of electrothermal simulations are conducted with the representative values. Another simplification technique is to identify the impacts of the component parameters on the lifetime and randomize the equivalent variables in the lifetime model. For example, the switching loss mainly affects the amplitude of temperature swings ΔT. The switching loss variations can be reflected by corresponding ΔT variations. Assuming mean temperature T_m, temperature

swing ΔT and lifetime model parameters have a 5% variation around their equivalent values. The corresponding IGBT annual damage probability distribution can be obtained as shown in Fig. 4.16.

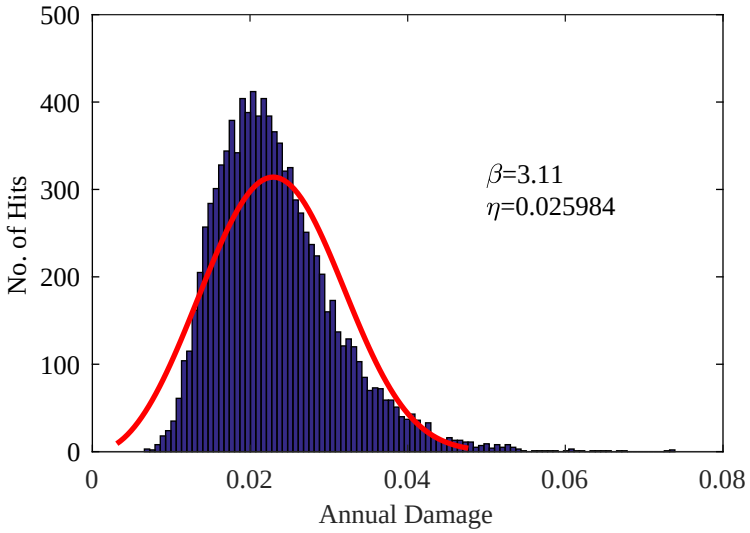


Figure 4.16. IGBT annual damage distribution

2. Formulating the reliability functions for critical components.
   The Weibull distribution is selected to fit the histogram for its flexibility and practicality. The failure density function and reliability function of Weibull distribution are listed below.

$$f(t) = \frac{\beta}{\eta}(\frac{\beta}{\eta})^{\beta-1}e^{-(t/\eta)^{\beta}} \tag{4.7}$$

$$R(t) = e^{[-(t/\eta)^{\beta}]} \tag{4.8}$$

   where β is the shape parameter, and η is the scale parameter. When $\beta = 1$, the Weibull distribution becomes an exponential distribution with a constant failure rate $1/\eta$.

   The IGBT lifetime distribution and its Weibull distribution fitting results are shown in Fig. 4.17.

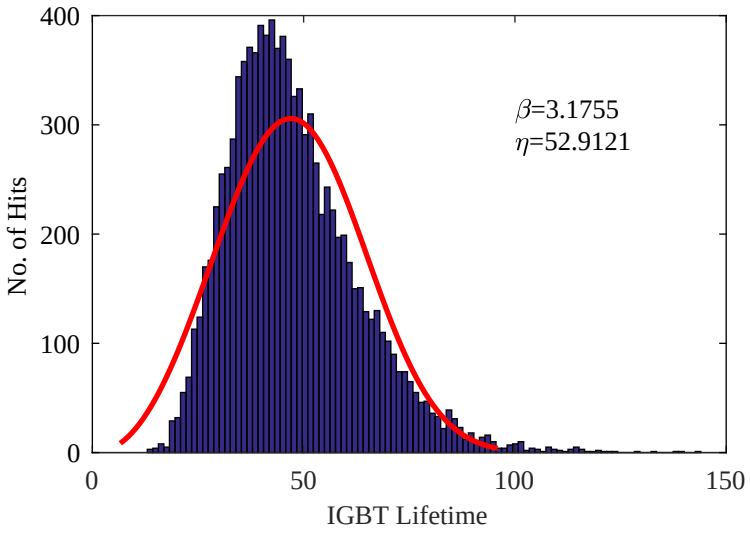


Figure 4.17. IGBT lifetime distribution

The reliability of the IGBT, $R(t) = e^{[-(t/52.9121)^{3.1755}]}$, is plotted in Fig. 4.18. The $\beta = 3.1755$ implies an increasing failure rate function of the IGBT.

3. Evaluating system level reliability.
   Base on the analytical reliability function of IGBT and capacitor. The CHB converter reliability can be calculated with the statistical reliability modeling techniques such as the proposed hierarchical modeling technique and redundancy modeling technique in Chapter 3.

The calculated CHB converter reliability function is shown in Fig. 4.19.

4. Calculating reliability indices.
   The MTTF of the CHB converter can be calculated by integrating the system-level reliability function with respect to time from zero to infinity. The MTTF of the CHB converter is 12.3209 years and the B10 lifetime is 6.7748 years.

For converter manufactures, a warranty lifetime can be given less than the B10 lifetime as the converter product return rate will be less than 10% during the given

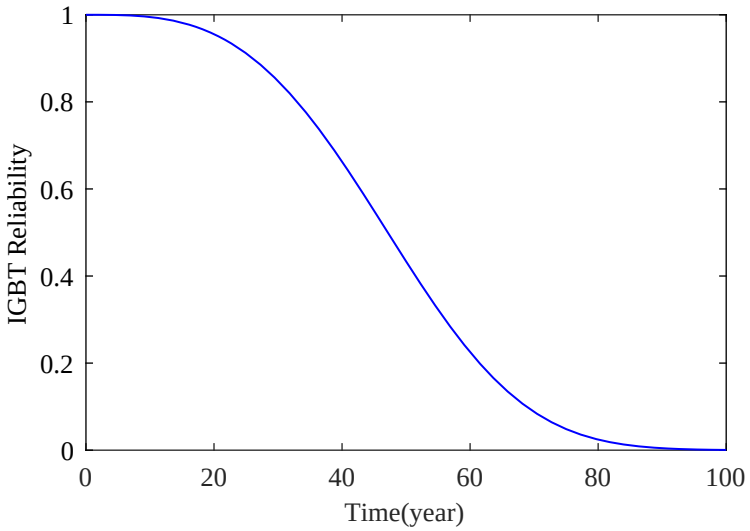


Figure 4.18. IGBT reliability

period. Compared to the deterministic Physics-of-Failure method, the proposed probabilistic Physics-of-Failure method gives more information on reliability and more realistic prediction results.

4.5 Sensitivity Analysis of Parameter Variation

In the Physics-of-Failure analysis, the parameters in the lifetime model have uncertainties. The stress parameters and lifetime model coefficients are highlighted in equation (4.9) with red and blue color respectively. The stress parameters are determined by the mission profile and the lifetime model coefficients are derived from test data.

$$N = A \times (\Delta T)^{-b} \times e^{E_a/(k_B \cdot T_m)} \tag{4.9}$$

These parameters variations may have different impacts on lifetime prediction. Sensitivity analyses should be conducted to identify the critical parameters which are most likely to affect lifetime model accuracy.

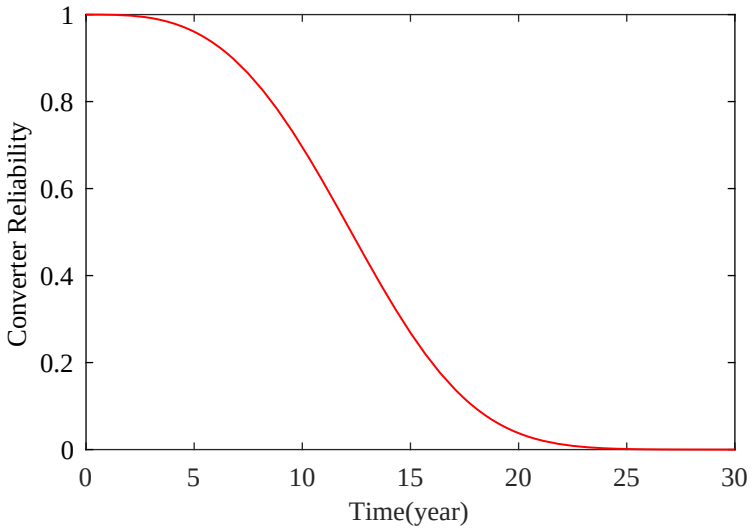


Figure 4.19. CHB converter calculated reliability function

It is assumed that there is a 10% variation of ΔT and other parameters have a 5% variations around their equivalent values. The IGBT annual damage and lifetime probability distributions are recalculated with the steps in Section 4.4 and shown in Fig. 4.20 and Fig. 4.21.

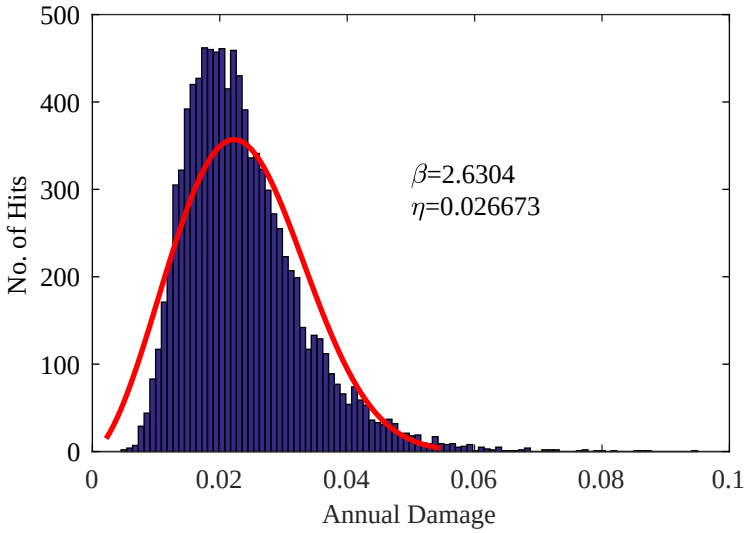


Figure 4.20. IGBT annual damage distribution with a larger ΔT variation

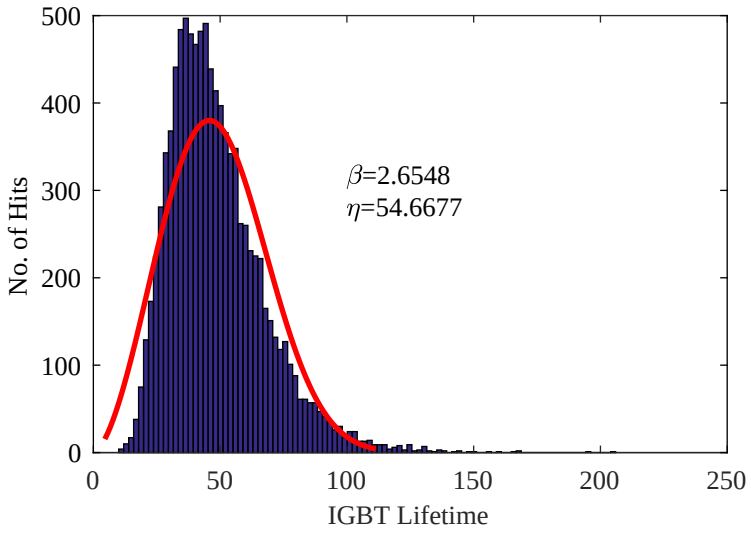


Figure 4.21. IGBT lifetime distribution with a larger ΔT variation

Then the reliability function of the IGBT can be obtained and depicted in Fig. 4.22

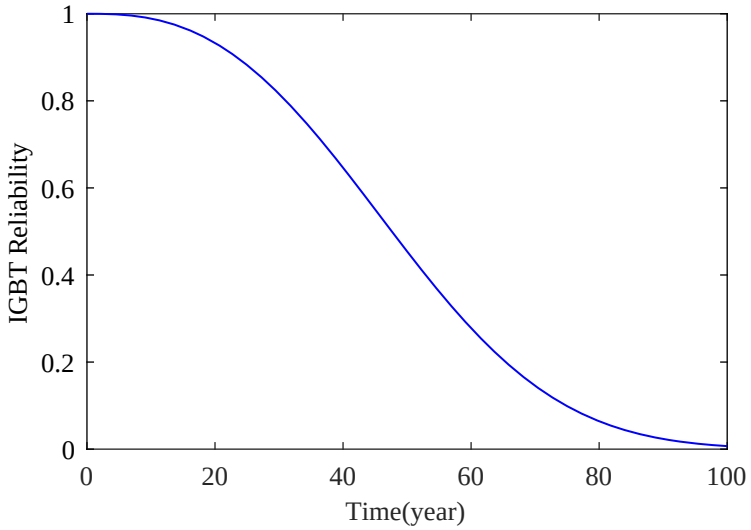


Figure 4.22. IGBT reliability with a larger ΔT variation

With the reliability function of each IGBT obtained, the converter reliability index can be calculated accordingly. The MTTF and B10 lifetime calculated in

this case are 9.7034 and 4.6774 years.

The impacts of other parameters on MTTF and B10 lifetime can be assessed in a similar way. The reliability indices, MTTF and B10 lifetime, are recalculated and shown in Table. 4.3.

Table 4.3. Sensitivity analysis results of lifetime model parameters

Para. \ Ind.	MTTF	B10
Original	12.3209	6.7748
A	12.2617	6.7263
$-b$	4.8157	1.5234
E_a	9.8923	4.8247
T_m	12.1901	6.6636
ΔT	9.7034	4.6774

Sensitivity analyses show that the temperature swings ΔT and its exponent $(-b)$ are the two critical parameters which have significant impacts on converter lifetime. Therefore, one should pay more attention to the accuracy of $(-b)$ in the lifetime model establishment stage. Another observation is that reducing the temperature swings ΔT is more effective in improving reliability during converter operating stage.

4.6 Conclusions

This chapter discuss the existing deterministic PoF methods in detail with a case study of Cascaded-H Bridge (CHB) multilevel converter. Key steps in PoF methods are presented and explained. The PoF analyses are conducted for IGBT and Capacitor. The system lifetime will be determined by the component with

least lifetime. Without actual load mission profile, the PoF analyses may give unrealistic lifetime predictions. The deterministic PoF method only consider the component level lifetime without modeling the converter system level redundancy and the probabilistic properties of components.

To cope with these issues, normal distributions of component parameters are used to simulate the manufacturing process. Tens of thousands virtual components are 'manufactured' by randomly sampling component parameters from normal distributions. A probabilistic Physics of Failure method is proposed based on the normal distribution assumption of component parameters. The proposed hybrid physics and statistics method bridges the gaps between the component PoF methods and the system-level reliability and redundancy modeling.

The proposed probabilistic PoF method is explained and demonstrated with a case study of CHB system level reliability and redundancy modeling. The temperature swings ΔT and its exponent $(-b)$ are identified as two critical parameters in lifetime prediction by sensitivity analyses. From converter operating perspective, restrictions and reductions on temperature stress cycle amplitude ΔT are recommended to improve converter reliability.

Chapter 5

Reliability Improvement by Switching Loss Optimization

5.1 Introduction

Conventional reliability improvement strategies are overcapacity design, redundant cell design, and redundant converter design. All of these traditional methods improve reliability while having an increased cost. The PoF methods identify that the larger temperature cycling contributes most of the damage to power semiconductors.

In the design for reliability (DfR) research, thermal control is a promising way of improving reliability cost-effectively. Cooling system optimization is one direction to reduce fatigue. Another solution is to reduce the power semiconductor switching loss by proper gate driver design. Although the switching loss reduction contributes a little improvement on system efficiency, it may have a significant impact on system reliability.

This chapter explores improving reliability in component level, optimizing gate driver design for reduced switching loss to achieve a reduced temperature cycling.

5.2 Power Semiconductor Switching Loss Modeling

One of the key processes in the PoF method is power semiconductor (IGBT, MOSFET) switching loss modeling. With the limited test data provided by the manufacturer, lookup table and interpolation are widely used to simplify the loss modeling process. However, the switching loss is dependent on applications and load conditions [80,81]. It can be fine tuned according to design requirements. This gives the opportunity to reduce switching loss for component reliability improvement.

There are two ways to model the switching loss accurately. One is lookup table method with enough test data. The lookup table method is simple, but a large amount of test data are needed, resulting in a tedious repetitive experimental tests. The other one is the power semiconductor sub-circuit level model based simulation method. Several tests are enough to extract the power semiconductor parameters. Besides switching loss, full switching transients can also be predicted by the simulation method. Other requirements, such as over-voltage and over-current, can also be tuned carefully. Both methods will be introduced in the following parts.

Switching Loss Measurement in Double Pulse Test

The double pulse test is usually used to obtain the power semiconductor switching loss. It can provide a benchmark loss data under different load conditions with actual converters. The schematic of double pulse test is depicted in Fig. 5.1.

In double pulse test, a first long gate pulse is used to charge the inductive load L to a desired current level I_L, and the freewheeling diode (FWD) is used to keep the current level when the device under test (DUT) is off. A second short pulse is used for IGBT switching transient characterization [82]. The IGBT parasitic parameters and switching loss can also be extracted from double pulse test [83].

As the second pulse is very short, typically less than 10 μs, the load current did not increase too much. Hence IGBT turns on and off at almost the same

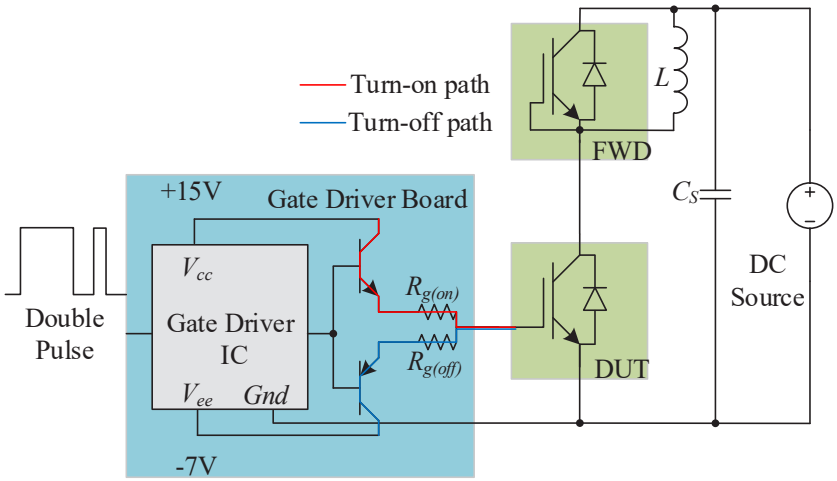


Figure 5.1. Schematic of Double Pulse Test

current level. The complementary transistors following gate driver IC output are used to separate turn-on and turn-off driver path. Therefore turn-on and turn-off processes can be tuned independently by adjusting turn-on resistor Rg(on) and turn-off resistor Rg(off).

Fig. 5.2 shows a typical qualitative IGBT switching transient waveforms under an inductive load. The switching process can be divided into turn-on and turn-off processes. The shadow areas are where switching losses occur as IGBT voltage and current are overlapped [84].

Fig. 5.3 shows the switching trajectory in IGBT output characteristics. The detailed switching process of an IGBT is explained in the following stages:

1. $[t_0, t_1]$, gate voltage V_{ge} is rising to threshold voltage V_{th}.
   Initially, IGBT is in Cut-off region which is between the forward blocking curve and x-axis in Fig. 5.3. When the positive gate driver voltage $V_{GG(on)}$ exerts between gate and emitter, V_{ge} starts to rise towards V_{th} as the C_{ge}, C_{gc} are charging. The IGBT input capacitance C_{ies} is defined as the summation of the two capacitance, $C_{ies} = C_{ge} + C_{gc}$. The inductance of wires and component leads is much smaller than the gate turn-on resistor and input

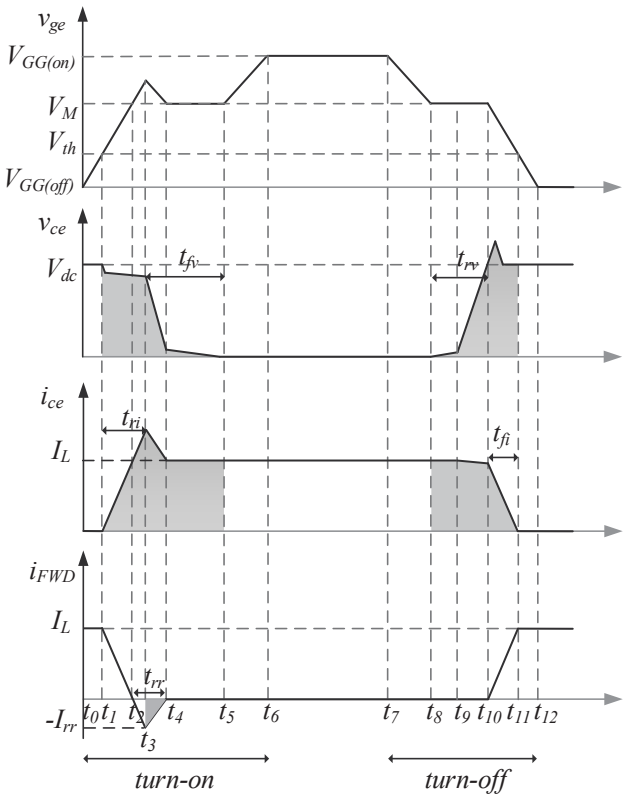


Figure 5.2. IGBT switching transient waveforms

capacitance. The inductance can be neglected to simplify the analysis. Then the increasing process of gate-emitter voltage V_{ge} can be well approximated by a first-order RC circuit. The time constant of this process is $R_g C_{ies}$, where R_g is the turn-on resistor.

2. $[t_1, t_3]$, collector-emitter current I_c are increasing.
   Once V_{ge} crosses over V_{th}, the conducting MOS channel is built by electrical field under gate oxide to conduct current. Since V_{ce} is much higher than V_{ge}, The MOS channel is saturated and the IGBT is operated in the active region where collector-emitter current I_c is mainly controlled by gate-emitter voltage V_{ge}.

3. $[t_3, t_4]$, freewheeling diode is recovering to be reverse biased.

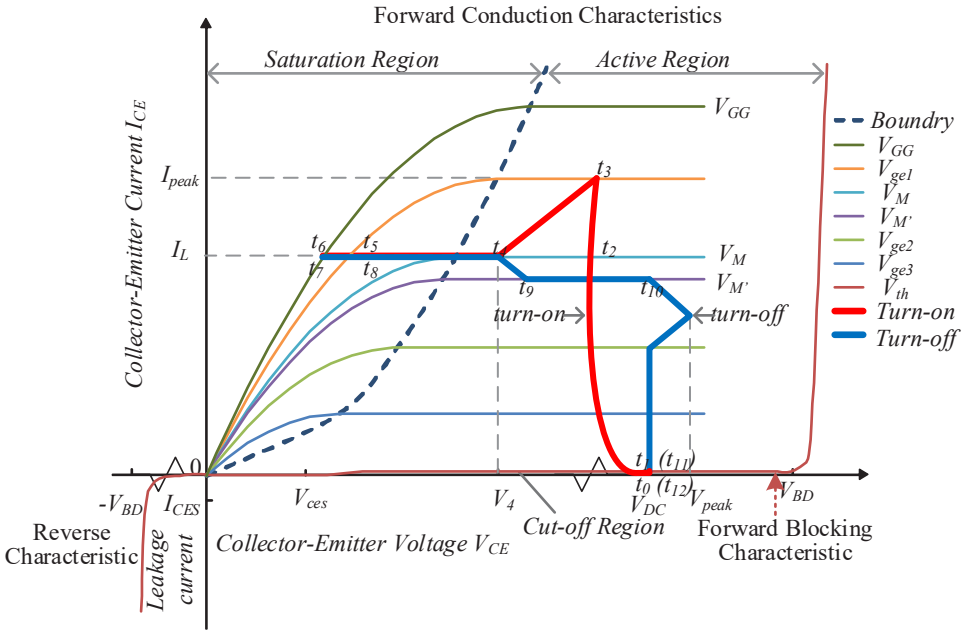


Figure 5.3. IGBT switching trajectory in its output characteristics

In this phase, IGBT still operates in the active region, and V_{ge} is therefore clamped by the load current. If the current spike is well controlled around load current, the gate-emitter voltage V_{ge} in this phase can be also approximated to the plateau voltage V_M. As V_{ce} is still higher than the gate voltage, the nonlinear capacitor C_{gc} is still constant. The positive gate current I_g flows into C_{gc} to reduce V_{gc}.

4. $[t_4, t_5]$ is the Miller Plateau.
   In this phase, I_c decreases to the constant load current I_L. V_{ce} is still high enough to maintain IGBT operating in the active region. Therefore V_{ge} is clamped to a constant value which is also called Miller Plateau V_M. The positive gate current I_g flows into C_{gc} to reduce V_{gc}. But in this phase, the nonlinear voltage dependent parasitic capacitance C_{gc} starts to increase as V_{ce} decrease.

5. $[t_5, t_6]$, V_{ge} is increasing to $V_{GG(on)}$.
   At the end of phase 4, V_{ce} reduces to a value that IGBT goes to the saturation

region. The input capacitance is much larger than that in phase 1, thus the time constant of the RC circuit is larger than that in phase 1. Therefore V_{ge} increases much slower than that in phase 1. At the end of this phase, V_{ge} will equal to $V_{GG(on)}$. In this phase, IGBT is fully on. The loss in this phase belongs to conduction loss according to definition.

The IGBT turn-off process is almost the inverse sequence of the turn-on process. The switching loss of IGBT is the integration of power loss on the device, i.e., the integration of product of V_{ce} and I_c over time.

The two issues during switching transition are current overshoot caused by the reverse recovery of the FWD at turn-on and voltage overshoot caused by the stray inductance at turnoff [85]. These two switching issues may also fail IGBT if it pushes IGBT out of the safe operating area (SOA) region [86].

Switching Loss Calculation by Sub-circuit Model Simulation

The optimization of switching loss is normally achieved by the repetitive double pulse test experiments. It is time-consuming to find an optimum gate resistance to achieve the trade-off between switching loss and issues of over-current and over-voltage. An accurate sub-circuit model is proposed to assist the optimization of switching loss.

The sub-circuit model of IGBT and circuit model of double pulse test is shown in Fig. 5.4. The gray areas in Fig. 5.4 are the IGBT and FWD models. The rest parts are circuit models of a gate driver, inductor load, and DC source. The inductor load is modeled as a constant current source during the second pulse as its inductance is large enough to maintain a constant current in the short second pulse. In the double pulse test, only the second pulse which characterizes IGBT switching transients need to be analyzed.

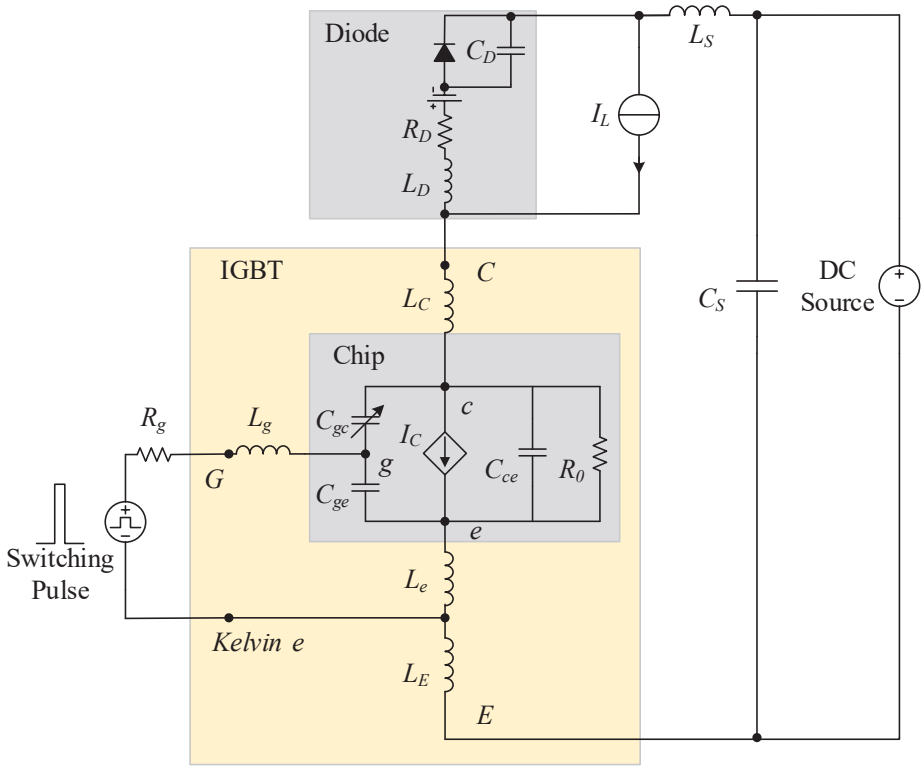


Figure 5.4. Double pulse test circuit with IGBT sub-circuit model

5.3 A MOSFET Switching Loss Optimization Case Study

Silicon carbide (SiC) MOSFET is regarded as the next-generation power semiconductor for high power density applications due to its superior switching speed and low switching losses [87–89].

The commercial 1.2 kV, 120 A SiC half-bridge module CAS120M12BM2 from Wolfspeed (former name: Cree) [90] is selected as the device under test (DUT) to verify the proposed sub-circuit model based switching loss optimization.

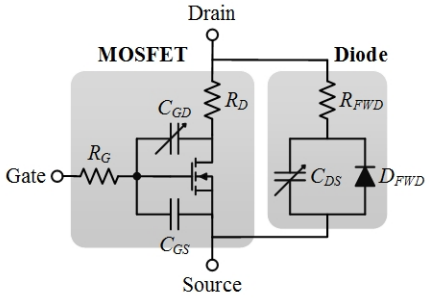


Figure 5.5. Equivalent circuit model of SiC power module.

5.3.1 Sub-circuit Model for MOSFET

The simplified equivalent sub-circuit model, with a SiC MOSFET and a SiC Schottky diode, is shown in Fig. 5.5. The external SiC Schottky diode serves as the freewheeling diode (FWD), which bypasses the internal body diode of SiC MOSFET as the body diode has a much higher knee voltage [91]. The body diode will not conduct during switching transients due to the presence of SiC Schottky diode. Therefore, there is no need to model the body diode. Additionally, the drain-source capacitance of SiC MOSFET is included in the junction capacitance model of SiC Schottky diode. The static and dynamic characteristics of the sub-circuit model are described in the following contexts.

When the gate-source voltage V_{GS} is lower than the threshold voltage V_{th}, the conduction channel has not been built. The MOSFET is in the cut-off region and no current flows through the channel. A leakage current may exist when V_{GS} is below V_{th}. As the subthreshold current is much smaller than the conduction current by orders of magnitude, it is normally neglected in the power MOSFET modeling.

Once V_{GS} is above V_{th}, the inversion channel is built between drain and source. The electrons now can move from source to drain via the conducting channel. The saturation voltage between drain and source is defined as $V_{DS,sat} = V_{GS} - V_{th}$. When V_{ch}, the voltage across the inversion channel, is lower than the saturation voltage $V_{DS,sat}$, the MOSFET is in the linear region (a.k.a Ohmic region). The

MOSFET behaves like a resistor, which is controlled by the gate voltage. The drain current is linearly proportional to V_{ch}:

$$I_D = \beta \left(V_{DS,sat} - \frac{V_{ch}}{2} \right) V_{ch} \left(1 + \lambda V_{ch} \right) \tag{5.1}$$

where β is the transconductance coefficient, λ is the channel modulation index. Due to the inversion layer charge, the channel electron mobility is proportional to the gate voltage bias [92]:

$$\beta = \left[\beta_0 + VC_1 \left(V_{GS} - V_{GS,nom} \right) \right] \tag{5.2}$$

where VC_1 is the voltage coefficient. As this coefficient cannot be fitted into the MOSFET level 1 model, a voltage-controlled current source (VCCS) is used to model the channel current. Once V_{ch} exceeds $V_{DS,sat}$, the MOSFET is in the saturation region. The inversion channel is pinched off near the drain area, and ideally, the drain current remains the same regardless of drain bias. However, when the shortened channel length is a significant fraction of the total length, the short-channel effect (SCE) needs to be taken into account in the device modeling. The drain current will increase slightly with the increase of drain bias. It has been found that SCE is an important consideration when modeling the SiC MOSFET [93]. The drain current in the saturation region is:

$$I_D = \beta \frac{{V_{DS,sat}}^2}{2} \left(1 + \lambda V_{ch} \right) \tag{5.3}$$

The on-state resistance of a MOSFET originates from metal contact, N+ source, accumulation layer, JFET region, drift and N+ substrate. For simplicity, only the drift resistance R_D is considered. The overall drain-source voltage drop V_{DS} can be expressed as:

$$V_{DS} = V_{ch} + I_D R_D \tag{5.4}$$

The current through the Schottky contact can be modeled by thermionic emission theory [94]:

$$I_F = I_S \left[\exp \left(\frac{qV_D}{kT} \right) - 1 \right] \tag{5.5}$$

where I_S is the reverse saturation current and V_D is the voltage drop across Schottky contact. The forward voltage across Schottky diode is contributed by the Schottky contact and the series resistance R_{FWD}, as given by

$$V_{SD} = V_D + I_F R_{FWD} \tag{5.6}$$

Here V_{SD} and I_F are used instead of V_{DS} and I_D in Eq.(5.4) since the Schottky diode is anti-parallel connected with the MOSFET.

The unipolar devices, MOSFET and Schottky diode, are inherently suitable for high-frequency operation as there is no carrier recombination at turn-off. Additionally, the lack of majority carrier also makes the dynamic characteristics temperature-independent. Hence, the dynamic characteristics at room temperature are investigated and modeled. For MOSFET, the dynamic characteristics are dominated by charging and discharging of the parasitic capacitors, which includes gate-source (C_{GS}), drain-source (C_{DS}) and gate-drain (C_{GD}) capacitors. C_{GS} is mainly due to an overlap of gate metalization over the source and P-well regions, and it can be modeled as a constant capacitor. C_{DS} is a bias-dependent depletion capacitor of P-well/N-drift junction, which can be modeled as the junction capacitance in the default diode model, as given by

$$C_{DS} = C_{DS0}\left(\frac{V_{bi}}{V_{DS} + V_{bi}}\right)^{M_{CDS}} \tag{5.7}$$

where V_{bi} is the built-in potential, and M_{CDS} is a fitting parameter.

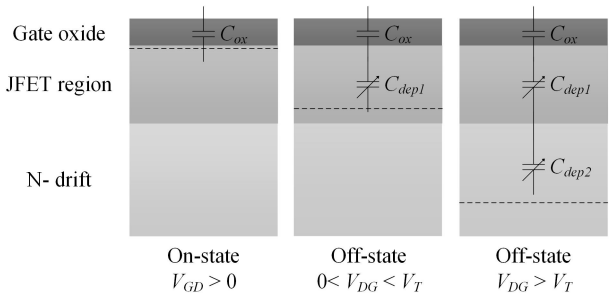


Figure 5.6. Miller capacitor model.

The Miller capacitor C_{GD} is the most important and complicated parasitic capacitor, as it provides the feedback loop between output and input. C_{GD} is

due to the overlap of gate metalization over drift region. It consists of a constant gate oxide capacitor C_{ox} in series with a bias-dependent depletion capacitor C_{dep} beneath the gate oxide, as Fig. 5.6 shows. With the decrease of V_{DG} at turn-on, the depletion region shrinks. At on-state, the depletion region disappears, the Miller capacitor equals to C_{ox}. With the increase of V_{DG} at turn-off, the depletion region gradually expands. As the depletion capacitors are in series with C_{ox}, the Miller capacitor decreases gradually. Since JFET region and drift region are doped differently, there are two different depletion capacitors C_{dep1} and C_{dep2}, which can be seen from from its C-V curve. A transition voltage V_T is defined based on the C-V curve. Therefore the Miller capacitor C_{GD} can be modeled as:

$$C_{GD} = \begin{cases} C_{ox}, \text{ when } V_{DG} < 0 \\ C_{ox} \parallel C_{dep1}, \text{ when } 0 < V_{DG} < V_T \\ C_{ox} \parallel C_{dep1}\left(V_T\right) \parallel C_{dep2}, \text{ when } V_{DG} > V_T \end{cases} \tag{5.8}$$

$$C_{dep1} = \left(\frac{\varepsilon q N_J}{2V_{DG}}\right)^{M_1} A = \frac{C_1}{{V_{DG}}^{M_1}} \tag{5.9}$$

$$C_{dep2} = \left[\frac{\varepsilon q N_D}{2\left(V_{DG} - V_T\right)}\right]^{M_2} A = \frac{C_2}{\left(V_{DG} - V_T\right)^{M_2}} \tag{5.10}$$

where N_J and N_D are the doping concentrations of JFET and drift region respectively, A is the active chip area, C_1 is the specific capacitance of JFET region at $V_{DG} = 1$ V, C_2 is the specific capacitance of drift region at $V_{DG} - V_T = 1$ V, and M_1, M_2 are the curve-fitting parameters. The procedure for parameter extraction from the datasheet are elaborated in the following section:

1. Threshold Voltage. V_{th} is defined as the gate-source voltage when the channel starts to conduct at a certain drain-source bias. However, there is no standard criterion for this current magnitude at V_{th}, such as 1 mA, 5 mA, 50 mA, et al. Hence, V_{th} needs to be extracted for the model even though it is provided by the the datasheet. In the saturation region, V_{ch} is the dominant factor of V_{DS} as the channel is pinched off. A simplification of Eq. (5.3) can be made with replacement of V_{ch} by $V_{DS} = 20$ V. From the transfer characteristics, a 2nd order polynomial fitting for I_D-V_{GS} is used to extract V_{th}.

2. Transconductance Coefficient. At low gate bias ($V_{GS} < 12\ V$), R_{ch} is the dominant factor of R_{on}. Hence, a similar simplification for Eq. (5.1) can be made with the replacement of V_{ch} by V_{DS} in the linear region. In addition, the SCE is also neglected. After considering the voltage-dependent property of β, the simplified I_D-V_{DS} relationship is given by

$$I_D = [\beta_0 + VC_1 (V_{GS} - 10)] \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \tag{5.11}$$

Two sets of I_D-V_{DS} data in the linear region at $V_{GS} = 10$ V (nominal voltage) and 12 V are used to extract β_0 and VC_1.

3. Drift Resistance and Channel Modulation Index. When the gate voltage reaches 20 V, R_{ch} is reduced significantly and becomes comparable with R_D. In order to extract R_{ch}, an assumption is made with $R_D = 0\ \Omega$ and $\lambda = 0$ in the simulation. Therefore, R_{ch} is the reciprocal of the slope of $I_D - V_{DS}$ curve. Then R_D can be derived as

$$R_D = R_{on} - R_{ch} = R_{on} - \frac{dV_{DS}}{dI_D} \tag{5.12}$$

where R_{on} is the typical on-resistance in the the datasheet. Finally, a channel modulation index of 0.01 is set after adjusting the simulated curves to fit the measurement.

4. Freewheeling Diode. As Fig. 5.7 shows, R_{FWD} is the reciprocal of the slope of I_F-V_{SD} curve, which can be derived by a linear fit. V_D is extracted by subtracting the voltage drop across R_S from V_{int} (intercept of linear fit curve at V axis):

$$V_D = V_{int} - I_{int} R_S \tag{5.13}$$

The knee voltage is defined at the forward current of 100 mA. Then I_S is calculated by the following equation. Finally, I_S is slightly adjusted in PSpice to make the simulated curve match the measurement:

$$I_S = 0.1 \times \exp\left(-\frac{V_D}{0.026} \right) \tag{5.14}$$

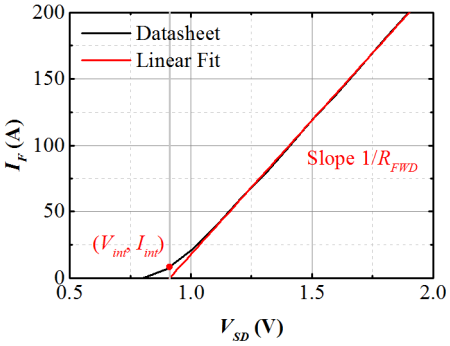


Figure 5.7. FWD characteristics of CAS120M12BM2.

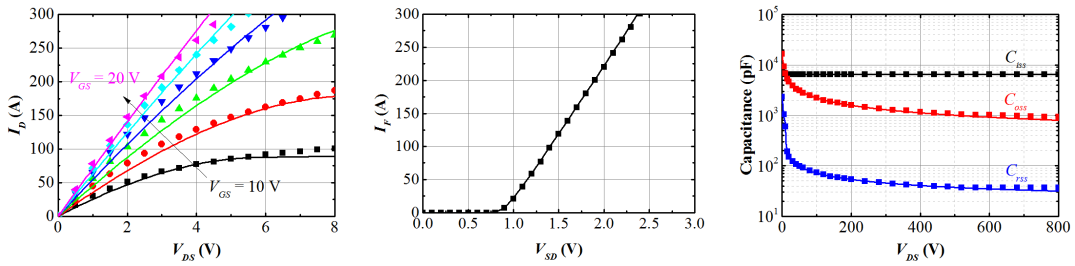
5. Parasitic Capacitance. Three equivalent capacitance are provided by the the datasheet: input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer (C_{rss}) capacitance. The parasitic capacitors can be calculated as:

$$C_{GS} = C_{iss} - C_{rss},\ C_{DS} = C_{oss} - C_{rss},\ C_{GD} = C_{rss} \tag{5.15}$$

Firstly, C_{GS} is extracted by subtracting C_{rss} from C_{iss}, and a constant value is obtained. The bias-dependent C_{DS} can be derived in a similar way. The fitting parameters for C_{DS} are extracted by curve fitting of C_{DS}-V relationship with Eq. (5.7). C_{ox} is extracted from C_{rss} at zero bias. V_T can be easily extracted from the C_{rss}-V curve due to the two remarkably different slopes. Then the fitting parameters for C_{dep1} and C_{dep2} are extracted by curve fitting of C_{rss}-V relationship in Eq. (5.9) and (5.10).

5.3.2 Model Evaluation

The comparison of static characteristics between the datasheet and PSpice simulation are shown in Fig. 5.8 (a) and (b), and the nonlinear C-V characteristics are plotted in Fig. 5.8(c). A good agreement between the datasheet and simulation is achieved. Especially, the transition region of C_{rss}-V is accurately modeled with the improved Miller capacitance model.



(a) (b) (c)

Figure 5.8. Comparison between the datasheet (dot) and PSpice simulation (line) for CAS120M12BM2: (a) *I-V* characteristics, (b) FWD characteristics, (c) *C-V* characteristics.

Experimental Setup of Double Pulse Test

A DPT experiment is set up to evaluate the accuracy of the circuit simulation model developed in this thesis, as Fig. 5.9 shows. The high side (HS) transistor is always off and the low side (LS) transistor is controlled by a double pulse gate signal generated by a digital signal processor (DSP) TMS320F28335 from Texas Instrument. A fully isolated half-bridge gate driver is designed and implemented by a four-layer printed circuit board (PCB). More details on the gate driver design were described in our previous work [95]. The gate driver board is directly mounted onto the module by solder to reduce the stray inductance of gate driver loop. As the coupling capacitances between the power devices, direct bond copper (DBC) and heat sink will lead to a low-frequency common-mode (CM) EMI, the power module is fixed onto a wood plate to make it float from the ground.

A 247-μH single-layer air-core inductor is used as the inductive load. The single-layer structure ensures low equivalent parallel capacitance (EPC), and the air-core avoids the potential saturation issue. The DC-link is charged by a high-voltage dc power supply. The stray inductance of DC-link should be minimized to reduce the ringings of voltage and current during the switching transition. The laminated structure is adopted for the DC-bus bar, in which the positive and negative plates are overlapped with each other to cancel the stray inductance [96]. The DC-bus bar

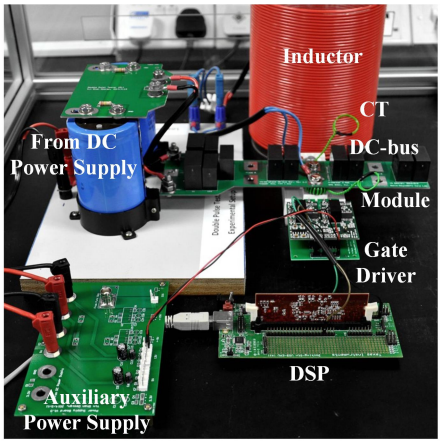


Figure 5.9. Double pulse test experimental setup.

is implemented by double-layer PCB with 2 oz thickness. The DC-link consists of 11 parallel 900-V film capacitors with a total capacitance of 41 μF, and thus to reduce the equivalent series capacitance (ESL). To measure the current commutation, a scaled-down current transformer (CT) is made, which comprises 10 turns of isolated wire wound on a ferrite toroid [97]. The output terminal of CT is connected to a current probe TCP0030 (30 A, 120 MHz) from Tektronix. The use of CT will add to the stray inductance of the power loop. The total stray inductance of DC-link and CT is measured by the Bode 100 vector network analyzer, and an average value of 16 ($\pm$1) nH is obtained.

The switching waveforms and other parameters regarding to the switching transition obtained from the PSpice simulation are compared with those from DPT experiment. Fig. 5.10 is the double pulse test circuit model built in PSpice simulation. The external gate resistance R_G and external stray inductance L_s needs to be extracted from the experiment to fit the two sets of curves. R_G is extracted based on the measured RC time constant of gate driver loop. L_s is extracted based on the resonant frequency of power loop [96]. Fig. 5.11(a) shows the LC resonant loop during the switching transient. Applying fast Fourier transform (FFT) to the switching waveforms, the spectra of switching waveforms can be obtained and a resonant frequency of 29 MHz is extracted, as Fig. 5.11(b) shows. Hence, the loop

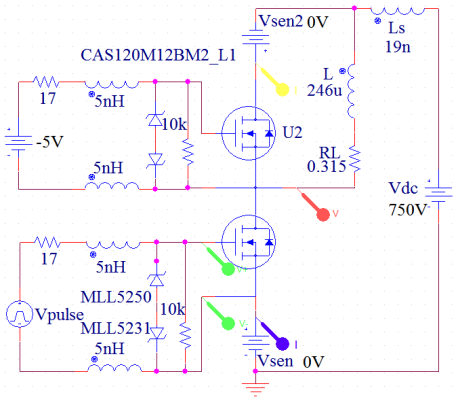


Figure 5.10. Circuit diagram of double pulse test in PSpice simulation.

stray inductance L_{loop} can be calculated with equation below:

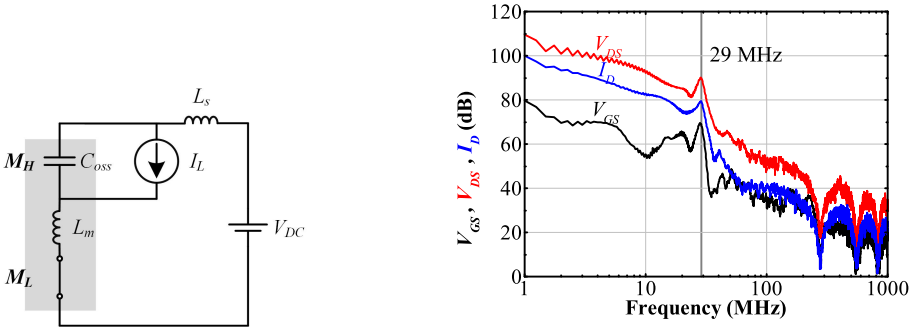
$$L_{loop} = \frac{1}{(2\pi f_r)^2 C_{oss}} \tag{5.16}$$

$$L_{loop} = L_s + L_m \tag{5.17}$$

Considering C_{oss} = 880 pF at 750 V DC-bus voltage and L_m = 15 nH from the the datasheet of CAS120M12BM2 [90], L_s is calculated to be 19 nH, which shows a good agreement with the measurement results.

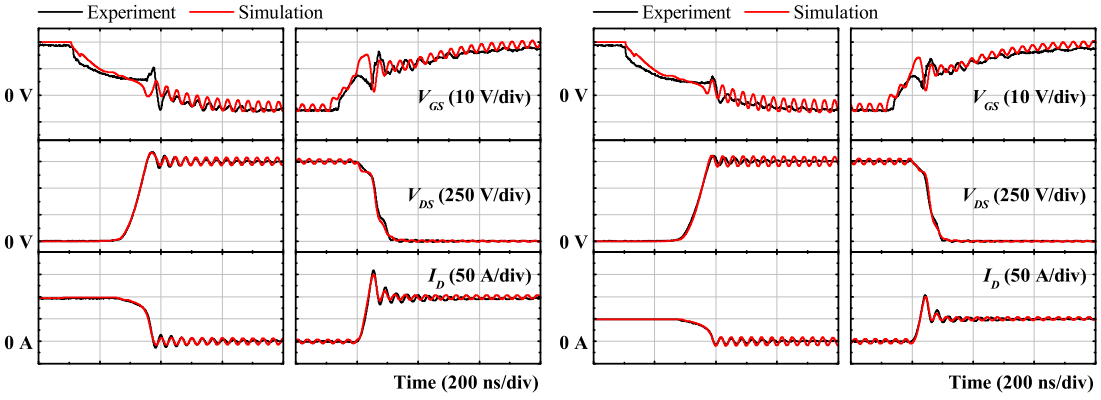
Comparison of Switching Waveforms

Firstly, the SiC MOSFET power module is tested at 750-V DC-bus voltage, 10-Ω gate resistance, and two different values of inductive load current (100 A and 50 A). Fig. 5.12 shows the comparison of switching waveforms including gate-source voltage (V_{GS}), drain-source voltage (V_{DS}) and drain current (I_D). A good agreement (especially the falling and rising edges) is achieved between experiment and simulation at both full- and half-load conditions. Due to the ignorance of ac resistance (skin effect) in simulation, the resonant amplitude of V_{GS} and V_{DS} shows a significant difference between experiment and simulation. However, it only has a remarkable impact on the prediction of EMI rather than switching loss.



(a) (b)

Figure 5.11. Switching ring analyses: (a) Equivalent circuit of LC resonant loop; (b) Spectra of switching waveforms.



(a) (b)

Figure 5.12. Comparison of switching waveforms at different inductive load currents: (a) full-load 100 A, (b) half-load 50 A.

This circuit simulation model is further validated at different gate resistances and DC-bus voltages. Fig. 5.13 shows the comparison of switching waveforms at 4.7-Ω gate resistance, 750-V DC-bus voltage and 100-A load current.

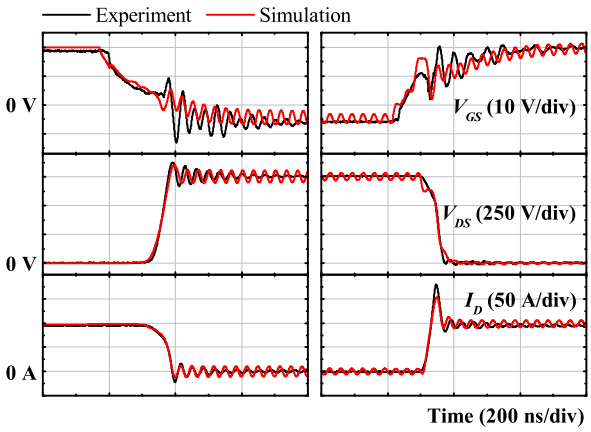


Figure 5.13. Comparison of switching waveforms at 4.7-Ω gate resistance.

Fig. 5.14 shows the comparison of switching waveforms at 4.7-Ω gate resistance, 100-A load current, and another two different values of DC-bus voltage (400 V and 600 V). It can be found that a good agreement is achieved between experiment and simulation under various testing conditions, although there is some mismatch at 4.7-Ω gate resistance.

5.3.3 Switching Loss Optimization

The foregoing discussion has shown that there is a significant current spike at turn-on. Although the SiC Schottky diode does not exhibit the reverse recovery process like the Si counterpart, its capacitive charge still leads to a similar current spike through the SiC MOSFET. Additionally, at turn-off, the current through L_s produces a voltage overshoot across it in the same direction. This overshoot at full-load can be as high as 50∼100% for Si device and 20% for SiC device with a well-designed DC-link in this thesis. Hence, the switching loss, current spike and voltage overshoot regarding the switching transition are discussed as follow.

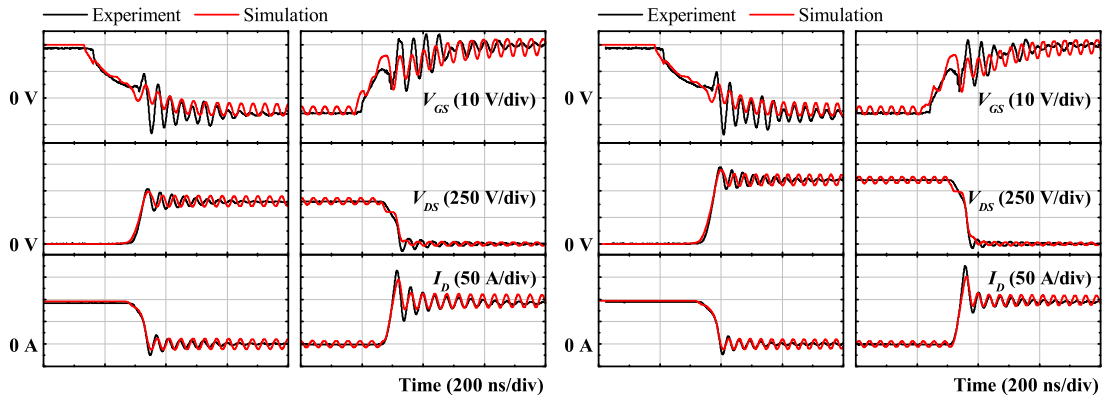


Figure 5.14. Comparison of switching waveforms at different DC-bus voltages: (a) 400 V, (b) 600 V.

Fig. 5.15 shows the comparison of total switching loss (E_{tot}), turn-on loss (E_{on}), turn-off loss (E_{off}) and diode reverse recovery loss (E_{rr}) between experiment and simulation at two different values of gate resistance (10 Ω and 4.7 Ω). Fig. 5.16 shows the comparison of peak voltage and peak current between experiment and simulation at two different values of gate resistance (10 Ω and 4.7 Ω). A good agreement is achieved between experiment and simulation, although there is some mismatch in the peak current at 4.7-Ω gate resistance.

The switching loss optimization problem can be expressed mathematically as follow:

$$\begin{aligned} &\underset{R_{on},R_{off}}{\text{minimize}} && E_{sw}(R_{on}, R_{off}, \cdots) \\ &\text{subject to} && v_{spike} < V_{rated} \\ &&& i_{spike} < I_{rated} \\ &&& \cdots \end{aligned}$$

The relationship between the switching transition and gate resistance is further investigated by PSpice simulation with a parameter sweep from 0 Ω to 40 Ω, as Fig. 5.17 shows. Based on the simulation results, the switching transition can be

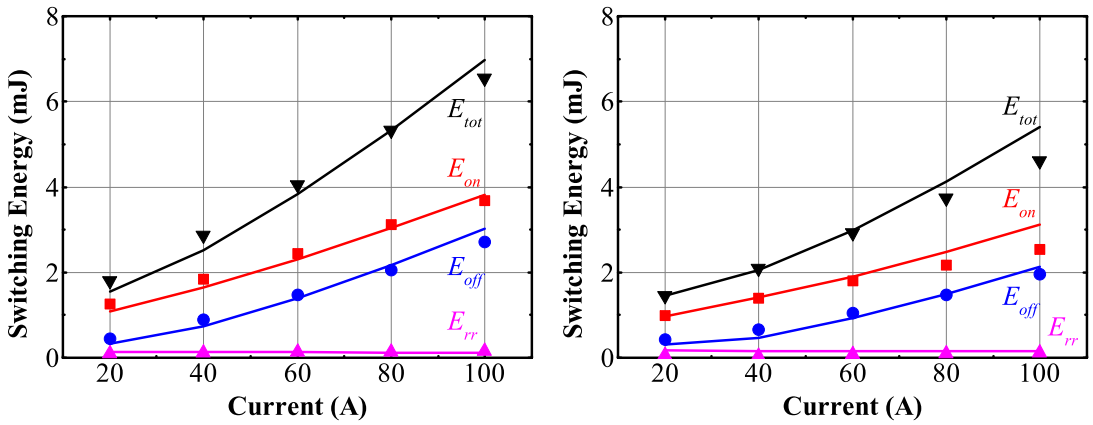


Figure 5.15. Comparison of switching losses at different gate resistances: (a) 10 Ω, (b) 4.7 Ω.

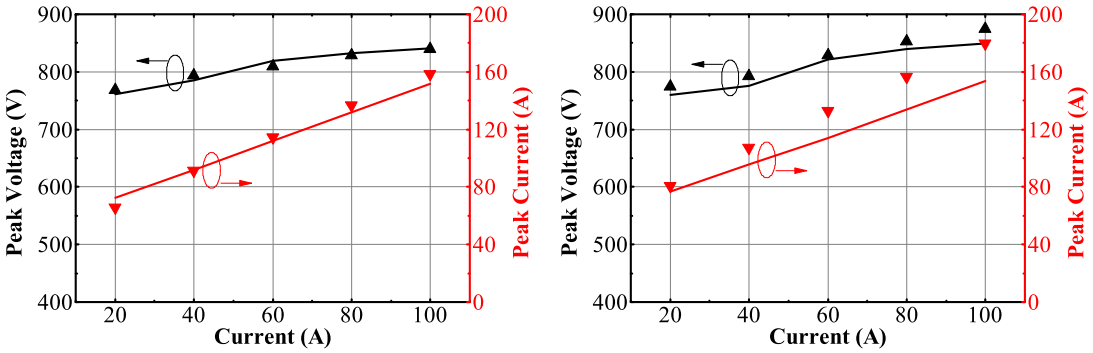
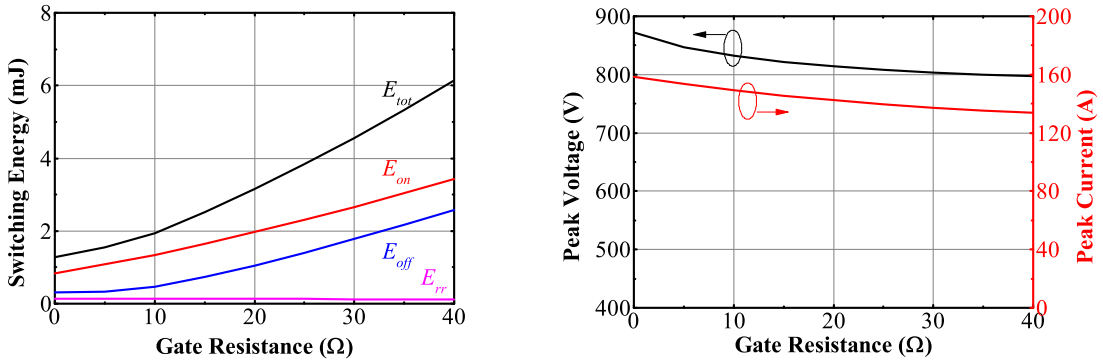


Figure 5.16. Comparison of peak voltages and peak currents at different gate resistances: (a) 10 Ω, (b) 4.7 Ω.

optimized by selecting a minimum gate resistance that meets the constraints of voltage overshoot and current spike. To summarize, the circuit simulation model developed in this work provides an accurate prediction of the switching loss, voltage overshoot as well as the current spike. It helps to optimize the switching loss by simulation.



(a) (b)

Figure 5.17. Simulation results of switching transition versus gate resistance at 750-V DC-bus voltage and 100-A load current: (a) switching loss, (b) peak voltage and peak current.

The conventional strategy to optimize the switching loss of power devices is usually achieved by the repetitive DPT experiments, which is time-consuming and has no physical insight into the device physics. In addition, the measurement setup is sensitive to the V-I misalignment as well as the bandwidth limitation of the current probe. Hence, an accurate circuit simulation model provides an alternative for the switching loss optimization.

In this case study, a sub-circuit model of SiC MOSFET half-bridge module is proposed. It is based on the datasheet and implemented in PSpice with consideration of device physics, especially the nonlinear Miller capacitance. The proposed model provides an accurate prediction on switching waveforms under various load currents, gate resistances, and DC-bus voltages. Besides, the switching loss, voltage overshoot, and current spike can also be predicted accurately. This model can be used to assist the optimization of switching loss in converter design.

It should be noticed that the proposed model shows some mismatch with the experiment at small gate resistance, especially in the current spike. This may be due to the inconstant output resistance of gate driver IC with the variation of gate current. The gate driver needs to be modeled accurately to evaluate the impact of

gate driver design on switching characteristics by simulation.

5.4 Conclusions

This chapter explores improving reliability in component level, i.e., optimizing gate driver design for reduced switching loss to achieve a reduced temperature cycling.

To achieve this target, sub-circuit models for IGBT and MOSFET are established with semiconductor physic characteristics and testing data. Detailed switching process of semiconductors are elaborated aiming to estimates the switching loss accurately. The proposed semiconductor sub-circuit models are validated by experiments.

With the proposed sub-circuit models, the switching loss can be predicted by simulation. Impact of different gate driver designs on switching loss and component lifetime can be analyzed by simulation. The gate driver development can be accelerated significantly. With a selected gate driver design, optimal gate resistance can be obtained with the sub-circuit model accordingly.

By reducing the switching loss in power semiconductors, the thermal stress can be reduced for a longer component lifetime and a higher converter reliability.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

Reliability modeling methods are investigated in this thesis aiming to provide systematic and practical reliability analysis and improvement for multilevel converters. The load-dependent failure rate method and probabilistic Physics-of-Failure method are developed to model the redundancy and system-level reliability of multilevel converters.

The data-driven failure rate methods are widely used in industry. Traditional failure rate methods pay little attention to multilevel converters' load variation modeling. A load-dependent failure rate method is hence proposed to model the fast-changing load in multilevel converters based motor drive systems. The load-dependent failure rate method can be used for the topology selection of multilevel converters in the design phase with an averaged characteristic failure rate.

Reliability of six typical multilevel converters is evaluated with the reliability index, mean time to failure (MTTF). Although the neutral point clamped converters have better reliability performances, they have no redundant component causing

difficulties in improving reliability cost-effectively.

With the proposed redundancy modeling techniques, the reliability of modular designed cascaded H-bridge (CHB) converter and modular multilevel converter (MMC) are reassessed assuming a smooth submodule fault bypass. With one additional submodule, the modular designed multilevel converters have an almost doubled MTTF. The cost of the additional submodule is a fraction of converter capital cost. The operating cost is increased slightly. The quantitative reliability and cost based redundancy design is provided with an MMC case study demonstration. With the proposed design guideline, the manufacturers are easy to select a redundant design which meets the reliability requirement while having an affordable cost.

The MTTF is a statistical mean value of converter life. The surviving percentage at t=MTTF is only 36.78%. The actual useful lifetime prediction is more concerned by end-users. The Physics of Failure method is usually used to predict the actual useful lifetime with a given mission profile. In practice, the PoF methods focus on modeling failure mechanisms of critical components and giving a system-level lifetime estimation with the weakest link effect in a deterministic way. However, multilevel converter redundancy and system-level reliability are hard to model as there is no component lifetime distribution. The randomness of failure and probabilistic property of reliability are lost.

A probabilistic Physics of Failure method is developed by including the uncertainties of component parameters and lifetime model parameters. An assumption that parameters follow normal distributions is made in the proposed method to simulate the manufacturing processes. Component lifetime distributions can be obtained by repetitive PoF analyses and Monte Carlo simulations. The component reliability function can be extracted by probability distribution curve fitting. The multilevel converter redundancy and system-level reliability can thus be modeled by well-established statistical techniques. A high power CHB converter is used to demonstrate the advantage of the proposed probabilistic PoF method over the conventional one. The proposed PoF method gives a much more realistic lifetime prediction.

With the proposed PoF reliability analysis, the high amplitude temperature swings are identified as the main contributor of power semiconductors fatigue failure. A cost-effectively way to improve the useful lifetime is to reduce the power semiconductor temperature swings by optimizing switching loss. Traditional switching loss optimization is a tedious and time-consuming repetitive experimental process. A sub-circuit power semiconductor model is proposed to analyze and simulate switching loss accurately. With the proposed sub-circuit model, a high power SiC MOSFET switching loss optimization is conducted with experimental verification. The simulation results match well with the experiments.

The two branches of reliability modeling methods should be selected depends on applications and users. The failure rate methods are good at comparing different topologies in the early design stage, and PoF methods can improve system reliability cost-effectively in the operational stage. The failure rate methods are suitable for manufacturers to determine the warranty time base on return rate. The end-users can use the PoF methods with condition monitoring to schedule maintenance and replacement with limit cost.

6.2 Recommendations for Future Research

Efforts have been made to update the failure rate methods standard "MH-217F" with consideration of Physics-of-Failure methods, such as a "G" version for "MH-217" in academia [29] and a "Fides" method proposed by a European industry consortium [98–100]. However, there is little progress on updating the failure rate methods in the last decade. On the other hand, the power electronics reliability research community prefer the scientific-based Physics-of-Failure methods than the data-driven empirical-based failure rate methods. It is still hard to harmonize the two branches of reliability modeling methods. Developing hybrid physics-statistic methods which can take both usability and accuracy is a possible solution in near future.

6.2.1 Challenges of Physics of Failure Methods

Although the pace of applying Physics of Failure methods to power converters is slow, there are vibrant research activities aimed at solving the challenges in PoF methods. There are three challenges for the popularization of PoF methods, accurate lifetime model establishment, reliability results validation, and method usability improvement.

Accurate Lifetime Model Establishment

The lifetime models are the basis of the PoF methods. Most of the power semiconductors lifetime models are extracted from power cycling test data. In the power cycling test, the device under test is heating up and cooling down repetitively either by an external heat source or self-generating power loss. The controllable variables in the cycling test are usually the mean temperature and the temperature swing amplitude [101]. The impact of other ambient conditions such as humidity and mechanical stress on lifetime are not well modeled. A comprehensive and solid lifetime model which gives an accurate device state of health can provide guidance on maintenance.

However, comprehensive power cycling test data are usually hard to obtain due to the high cost of a large number of devices needed and the time-consuming aging process of devices. Although there are several widely accepted general lifetime models, the actual parameters of these models differ from device ratings and manufacturers. A power cycling test standard and a test database for power converter components are important to academia and industry.

Reliability Results Validation

Reliability analysis is usually used for comparison purpose as the absolute reliability and lifetime are hard to be validated. The PoF methods aim to give actual useful lifetime. To make the PoF methods more convincing, the reliability analysis results

should be verified. The predicted lifetime can be verified directly by collecting actual field lifetime data or accelerated test data. It may take years to collect the lifetime data.

Indirect lifetime validation methods are to be developed for considerations of saving time and cost. For example, power components electrical and thermal parameters such as on-voltage drop and thermal resistance can be selected as the lifetime indicators. The detailed relationship between lifetime and the selected indicative parameters can be established in the power cycling test stage.

Method Usability Improvement

Compared to the widely used failure rate methods, the PoF methods are much more complex. There is no PoF methods standard and very few commercial software. Although the PoF methods have clear physics significance which makes them easy to understand, they are difficult to use in practice.

The standardization of PoF methods may help to reduce the difficulty in filed applications. It's also possible to simplify the PoF analysis procedures with open-source or commercial softwares.

6.2.2 Reliability Improvement Methods

The ultimate goal of reliability modeling and analysis is improving power converter reliability cost-effectively. There are many strategies for improving multilevel converter reliability. The cost-effectiveness of these strategies can be analyzed with the proposed reliability can cost analysis methods.

Active thermal control for even thermal stress distribution

With the observations from the PoF methods reliability analysis, large thermal cycling contributes most of the lifetime consumption and the power converter lifetime is determined by the least component lifetime. An effective way to improve

the power converter lifetime is to maintain a uniform thermal stress distribution among power converter components [102].

One of the active thermal control strategies is modifying existing modulation schemes for an even switching loss and conduction loss distribution in the multilevel converters. Active thermal control can also be achieved by adding power loss or temperature control loop into existing control schemes.

Power Converter Transients Overshoots Suppression

According to field experience, most of the failures occur in the transients such as short-circuit failure in switching transients and overloading failure in large load transients [81]. The transients in power converters differ in the magnitude and timescale. The switching transients may have 200% voltage and current spikes in around 10-100 ns. The switching waveforms oscillations caused by switching spikes are around 0.1-1 μs. Load transients are determined by controller and system dynamics which have much smaller overshoots but longer oscillations ranging from milliseconds to minutes. The transients in future power electronics will be much faster with wide bandgap (WBG) semiconductors such as SiC and GaN devices.

Although the failure mechanisms of these transients have not been investigated thoroughly, the suppression of transients overshoots is necessary for reliability improvement. Controller parameter design should pay more attention to the overshoots during load transients. The overshoots in switching transients can be tunned in gate drive design.

Author's Publications

Journal Publications

1. **P. Tu**, S. Yang, and P. Wang, "Reliability and cost based redundancy design for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, 2018.

2. S. Yin, **P. Tu***, P. Wang, K. J. Tseng, C. Qi, X. Hu, M. Zagrodnik, and R. Simanjorang, "An accurate subcircuit model of sic half-bridge module for switching-loss optimization," *IEEE Transactions on Industry Applications*, 2017.

3. C. Qi, X. Chen, **P. Tu**, and P. Wang, "Cell-by-cell-based finite-control-set model predictive control for a single-phase cascaded h-bridge rectifier," *IEEE Transactions on Power Electronics*, 2018.

4. D. Zhou, **P. Tu**, and Y. Tang, "Multivector model predictive power control of three-phase rectifiers with reduced power ripples under nonideal grid conditions," *IEEE Transactions on Industrial Electronics*, 2018.

5. C. Qi, C. Xiyou, **P. Tu**, and P.Wang, "Deadbeat control for a single-phase cascaded h-bridge rectifier with voltage balancing modulation," *IET Power Electronics*, 2017.

6. C. Qi, **P. Tu**, P. Wang, and M. Zagrodnik, "Predictive current control for multilevel cascaded h-bridge inverters based on a deadbeat solution," *Journal of Power Electronics*, 2017.

7. S. Yin, K. J. Tseng, R. Simanjorang, and **P. Tu**, "Experimental comparison of high-speed gate driver design for 1.2-kv/120-a si igbt and sic mosfet modules," *IET Power Electronics*, 2017.

8. Q. Xu, X. Hu, P. Wang, J. Xiao, **P. Tu**, C. Wen, and M. Y. Lee, "A decentralized dynamic power sharing strategy for hybrid energy storage system in autonomous dc microgrid," *IEEE Transactions on Industrial Electronics*, 2017.

9. C. Dong, H. Jia, Q. Xu, J. Xiao, Y. Xu, **P. Tu**, P. Lin, X. Li, and P. Wang, "Time-delay stability analysis for hybrid energy storage system with hierarchical control in dc microgrids," *IEEE Transactions on Smart Grid*, 2017.

10. C. Qi, **P. Tu**, P. Wang, and M. A. Zagrodnik, "Random nearest level modulation strategy of multilevel cascaded h-bridge inverters," *IET Power Electronics*, 2016.

Conference Publications

1. **P. Tu**, P. Wang, X. Hu, C. Qi, S. Yin, and M. A. Zagrodnik, "Analytical evaluation of igbt turn-on loss with double pulse testing," in Industrial Electronics and Applications (ICIEA), 2016

2. **P. Tu**, S. Yang, P. Wang, Q. Xu, and C. Qi, "Analytical averaged loss model of half-bridge modular multilevel converters," in Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017

3. **P. Tu**, S. Yin, P.Wang, K. Tseng, C. Qi, X. Hu, M. Zagrodnik, and R. Simanjorang, "An accurate subcircuit model of sic half bridge module for switching loss optimization," in Energy Conversion Congress and Exposition (ECCE), 2016

4. Q. Xu, **P. Tu***, C. Dong, C. Qi, S. Yang, S. Yao, and P. Wang, "Pof based reliability prediction for cascaded h-bridge converter in drive application," in

Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017

5. S. Yang, Y. Tang, **P. Tu**, and P. Wang, "A fault-tolerant operation scheme for a modular multilevel converter with a distributed control architecture," in Energy Conversion Congress and Exposition (ECCE), 2017

6. C. Qi, X. Chen, **P. Tu**, and P. Wang, "Low-complexity two-voltage-based model predictive control for a single-phase cascaded h-bridge inverter," in Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017

7. P. Lin, C. Zhang, P.Wang, X. Li, J. Xiao, **P. Tu**, and C. F. Hoong, "A global robust output regulation method for grid-connected inverter with lcl

   filter in weak grid condition," in Industrial Electronics and Applications (ICIEA), 2017

8. C. Qi, **P. Tu**, D. Shi, P. Wang, M. A. Zagrodnik, and G. Amit, "An efficient fpga-based implementation of predictive current control algorithms for an indirect matrix converter," in Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016,

9. S. Yin, K. Tseng, **P. Tu**, R. Simanjorang, and A. K. Gupta, "Design considerations and comparison of high-speed gate drivers for si igbt and sic mosfet modules," in Energy Conversion Congress and Exposition (ECCE), 2016

Bibliography

[1] L. G. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo *et al.*, "The age of multilevel converters arrives," *Industrial Electronics Magazine, IEEE*, vol. 2, no. 2, pp. 28–39, 2008.

[2] N. Mohan, *Power electronics: a first course*. Wiley, 2012.

[3] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 1, no. 2, pp. 59–72, 2013.

[4] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, no. 1, pp. 97–114, 2014.

[5] B. Bose, "The past, present, and future of power electronics [guest introduction]," *IEEE Industrial Electronics Magazine*, vol. 2, no. 3, pp. 7–11, 2009.

[6] M. Neufeld, O. Ramirez, and A. Ustinovich, "A comparative study of fixed speed vs. variable speed control of a series configured pipeline pumping application," in *Petroleum and Chemical Industry Technical Conference (PCIC), 2014 IEEE*. IEEE, 2014, pp. 491–500.

[7] M. Beck and P. U. Thamsen, "How to design a centrifugal pump with constant power consumption for all flow rates," in *16th International Symposium on*

Transport Phenomena and Dynamics of Rotating Machinery (ISROMAC 2016), 2016.

[8] Wikipedia, "Variable-frequency drive — Wikipedia, the free encyclopedia," http://en.wikipedia.org/w/index.php?title=Variable-frequency%20drive&oldid=849423792, 2018, [Online; accessed 13-July-2018].

[9] P. Waide and C. U. Brunner, "Energy-efficiency policy opportunities for electric motor-driven systems," 2011.

[10] B. Wu, *High-power converters and AC drives*. John Wiley & Sons, 2006.

[11] J.-S. Lai, L. Leslie, J. Ferrell, and T. Nergaard, "Characterization of hv-igbt for high-power inverter applications," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1. IEEE, 2005, pp. 377–382.

[12] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—state of the art, challenges, and requirements in industrial applications," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2581–2596, 2010.

[13] Wikipedia, "Cycloconverter — Wikipedia, the free encyclopedia," http://en.wikipedia.org/w/index.php?title=Cycloconverter&oldid=843915620, 2018, [Online; accessed 13-July-2018].

[14] S. A. Gonzalez, S. A. Verne, and M. I. Valla, *Multilevel converters for industrial applications*. CRC Press, 2013.

[15] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3. IEEE, 2003, pp. 6–pp.

[16] J. Rodriguez, L. G. Franquelo, S. Kouro, J. León, R. C. Portillo, M. A. M. Prats, M. Perez *et al.*, "Multilevel converters: An enabling technology for high-

power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009.

[17] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *Industry Applications, IEEE Transactions on*, vol. 47, no. 3, pp. 1441–1451, 2011.

[18] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *Power Electronics, IEEE Transactions on*, vol. 28, no. 1, pp. 591–604, 2013.

[19] C. Jais, B. Werner, and D. Das, "Reliability predictions-continued reliance on a misleading approach," in *Reliability and Maintainability Symposium (RAMS), 2013 Proceedings-Annual*. IEEE, 2013, pp. 1–6.

[20] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," *Power Electronics, IEEE Transactions on*, vol. 28, no. 8, pp. 4113–4119, 2013.

[21] E. Zio, "Reliability engineering: Old problems and new challenges," *Reliability Engineering & System Safety*, vol. 94, no. 2, pp. 125–141, 2009.

[22] A. Coppola, "Reliability engineering of electronic equipment a historical perspective," *IEEE Transactions on Reliability*, vol. 33, no. 1, pp. 29–35, 1984.

[23] W. Denson, "The history of reliability prediction," *Reliability, IEEE Transactions on*, vol. 47, no. 3, pp. SP321–SP328, 1998.

[24] J. G. McLeish, "Enhancing mil-hdbk-217 reliability predictions with physics of failure methods," in *Reliability and Maintainability Symposium (RAMS), 2010 Proceedings-Annual*. IEEE, 2010, pp. 1–6.

[25] R. Billinton and R. N. Allan, *Reliability evaluation of engineering systems*. Springer, 1992.

[26] IEC60050, "International electrotechnical vocabulary - chapter 191: Dependability and quality of service - edition 1.0," *IEC/TC 1 - IEC/TC 1 - TERMINOLOGY*, p. 13, Mar. 1993.

[27] K. C. Kapur and M. Pecht, *Reliability engineering*. John Wiley & Sons, 2014.

[28] L. Gullo, "The revitalization of mil-hdbk-217," *IEEE Reliability Newsletter, Sept*, 2008.

[29] J. W. Harms, "Revision of mil-hdbk-217, reliability prediction of electronic equipment," in *Reliability and Maintainability Symposium (RAMS), 2010 Proceedings-Annual*. IEEE, 2010, pp. 1–3.

[30] D. Nicholls, "What is 217plus/sup tm/and where did it come from?" in *Reliability and Maintainability Symposium, 2007. RAMS'07. Annual*. IEEE, 2007, pp. 22–27.

[31] A. Goel and R. J. Graves, "Electronic system reliability: collating prediction models," *Device and Materials Reliability, IEEE Transactions on*, vol. 6, no. 2, pp. 258–265, 2006.

[32] Handbook, Military Standardization, "MIL-HDBK-217F," *Reliability Prediction of Electronic Equipment, US Department of Defense*, 1995.

[33] Wikipedia, "Fracture — Wikipedia, the free encyclopedia," https://en.wikipedia.org/wiki/Fracture, 2018, [Online; accessed 23-July-2018].

[34] W. C. Young, R. G. Budynas, A. M. Sadegh *et al.*, *Roark's formulas for stress and strain*. McGraw-Hill New York, 2002, vol. 7.

[35] H. Huang, "Lifetime prediction for power converters," Ph.D. dissertation, University of Warwick, 2012.

[36] W. B. Nelson, *Accelerated testing: statistical models, test plans, and data analysis*. John Wiley & Sons, 2009, vol. 344.

[37] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—an overview," *Industry Applications, IEEE Transactions on*, vol. 50, no. 5, pp. 3569–3578, 2014.

[38] A. VanderMeulen and J. Maurin, "The reliability of neutral point clamped vs. cascaded h-bridge inverters," *Eaton White Paper TD02000001E, Arden, NC*, 2009.

[39] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *Industry Applications, IEEE Transactions on*, no. 5, pp. 518–523, 1981.

[40] Infineon, "FZ1200R45KL3-B5 datasheet."

[41] AVX, "DKTFMXXXI2197 datasheet."

[42] Infineon, "DD1200S45KL3-B5 datasheet."

[43] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *Industry Applications, IEEE Transactions on*, vol. 32, no. 3, pp. 509–517, 1996.

[44] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 7, pp. 2197–2206, 2010.

[45] L. Zhou and K. Smedley, "Reliability comparison of multi-level inverters for motor drive," in *Power & Energy Society General Meeting, 2009. PES'09. IEEE.* IEEE, 2009, pp. 1–7.

[46] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.* IEEE, 2008, pp. 174–179.

[47] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel

converters," *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 4–17, 2015.

[48] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *Power Electronics Conference (IPEC), 2010 International*. IEEE, 2010, pp. 502–507.

[49] R. Grinberg, G. Riedel, A. Korn, P. Steimer, and E. Bjornstad, "On reliability of medium voltage multilevel converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, 2013, pp. 4047–4052.

[50] K. Li, L. Yuan, Z. Zhao, S. Lu, and Y. Zhang, "Fault-tolerant control of mmc with hot reserved submodules based on carrier phase shift modulation," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6778–6791, 2017.

[51] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel pwm inverter," *Power Electronics, IEEE Transactions on*, vol. 25, no. 7, pp. 1786–1799, 2010.

[52] B. Li, S. Zhou, D. Xu, S. Finney, and B. Williams, "A hybrid modular multilevel converter for medium-voltage variable-speed motor drives," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4619–4630, 2017.

[53] B. Fan, Y. Li, K. Wang, Z. Zheng, and L. Xu, "Hierarchical system design and control of an mmc-based power-electronic transformer." *IEEE Trans. Industrial Informatics*, vol. 13, no. 1, pp. 238–247, 2017.

[54] C. G. Cassandras and S. Lafortune, *Introduction to discrete event systems*. Springer Science & Business Media, 2009.

[55] R. N. A. Roy Billinton, *Reliability evaluation of power systems*. Springer Science & Business Media, 1996.

[56] F. Deng, Y. Tian, R. Zhu, and Z. Chen, "Fault-tolerant approach for modular multilevel converters under submodule faults," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7253–7263, 2016.

[57] B. Li, Y. Zhang, R. Yang, R. Xu, D. Xu, and W. Wang, "Seamless transition control for modular multilevel converters when inserting a cold-reserve redundant submodule," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4052–4057, 2015.

[58] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single igbt open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron*, vol. 31, no. 4, pp. 3165–3176, 2016.

[59] T. Soong and P. W. Lehn, "Assessment of fault tolerance in modular multilevel converters with integrated energy storage," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4085–4095, 2016.

[60] A. Zapico, M. Lopez, A. Rodriguez, and F. Briz, "Fault tolerant cell design for mmc-based multiport power converters," in *Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*. IEEE, 2016, pp. 1–8.

[61] K. Shen, B. Xiao, J. Mei, L. M. Tolbert, J. Wang, X. Cai, and Y. Ji, "A modulation reconfiguration based fault-tolerant control scheme for modular multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*. IEEE, 2013, pp. 3251–3255.

[62] I. Mosgren, H. Nademi, and L. Norum, "Exploring a modulation strategy by experiments for modular multilevel converter in faulty operation," in *Industrial Technology (ICIT), 2017 IEEE International Conference on*. IEEE, 2017, pp. 101–106.

[63] M. Abdelsalam, M. I. Marei, and S. B. Tennakoon, "An integrated control strategy with fault detection and tolerant control capability based on capacitor voltage estimation for modular multilevel converters," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2840–2851, 2017.

[64] J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. S. Junior, and R. Teodorescu, "On the redundancy strategies of modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 851–860, 2018.

[65] Y. Chen, Z. Li, S. Zhao, X. Wei, and Y. Kang, "Design and implementation of a modular multilevel converter with hierarchical redundancy ability for electric ship mvdc system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 189–202, 2017.

[66] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters." *IEEE Trans. Industrial Electronics*, vol. 61, no. 10, pp. 5192–5202, 2014.

[67] J. Wang, V. Najmi, R. Burgos, and D. Boroyevich, "Reliability-oriented igbt selection for high power converters," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*. IEEE, 2015, pp. 2500–2503.

[68] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, 2013, pp. 2139–2146.

[69] H. Wang, D. Zhou, and F. Blaabjerg, "A reliability-oriented design method for power electronic converters," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*. IEEE, 2013, pp. 2921–2928.

[70] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, 2013.

[71] Y. Xue, B. Ge, and F. Z. Peng, "Reliability, efficiency, and cost comparisons of mw-scale photovoltaic inverters," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*. IEEE, 2012, pp. 1627–1634.

[72] I. . T. Committee *et al.*, "Reliability data handbook-universal model for reliability prediction of electronics components, pcbs and equipment," *IEC TR 62380*, 2004.

[73] X. Yu and A. M. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3881–3889, 2012.

[74] M. Rahimo, U. Schlapbach, A. Kopta, R. Schnell, and S. Linder, "Spt+, the next generation of low-loss hv-igbts," in *Proceedings PCIM*, vol. 5, 2005.

[75] S. Rodrigues, A. Papadopoulos, E. Kontos, T. Todorcevic, and P. Bauer, "Steady-state loss model of half-bridge modular multilevel converters," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2415–2425, 2016.

[76] S. Yang, Y. Tang, and P. Wang, "Seamless fault-tolerant operation of a modular multilevel converter with switch open-circuit fault diagnosis in a distributed control architecture," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7058–7070, 2018.

[77] N.-C. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, and P. de Place Rimmen, "Reliability oriented design tool for the new generation of grid connected pv-inverters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 5, pp. 2635–2644, 2015.

[78] ASTM-E1049-85, "Standard practices for cycle counting in fatigue analysis," *American society for testing and materials West Conshohocken, PA*, 2011.

[79] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *Power Electronics, IEEE Transactions on*, vol. 30, no. 2, pp. 590–602, 2015.

[80] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization for high frequency high power 3-level neutral point clamped phase leg," in *Energy*

Conversion Congress and Exposition (ECCE), 2013 IEEE. IEEE, 2013, pp. 3949–3956.

[81] H. Bai and C. Mi, *Transients of Modern Power Electronics.* John Wiley & Sons, 2011.

[82] Y. Shen, Y. Xiong, J. Jiang, Y. Deng, X. He, and Z. Zeng, "Switching loss analysis and modeling of power semiconductor devices base on an automatic measurement system," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2. IEEE, 2006, pp. 853–858.

[83] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the mosfet switching performance," *Power Electronics, IEEE Transactions on*, vol. 28, no. 1, pp. 573–590, 2013.

[84] V. K. Khanna, *Insulated gate bipolar transistor IGBT theory and design.* John Wiley & Sons, 2004.

[85] L. Chen and F. Z. Peng, "Closed-loop gate drive for high power igbts," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE.* IEEE, 2009, pp. 1331–1337.

[86] Y. Lobsiger and J. W. Kolar, "Closed-loop igbt gate drive featuring highly dynamic di/dt and dv/dt control," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE.* IEEE, 2012, pp. 4754–4761.

[87] T. E. Salem, D. P. Urciuoli, R. Green, and G. K. Ovrebo, "High-temperature high-power operation of a 100 A SiC DMOSFET module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 653–657.

[88] H. Sheng, Z. Chen, F. Wang, and A. Millner, "Investigation of 1.2 kV SiC MOSFET for high frequency high power applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2010, pp. 1572–1577.

[89] S. Hazra, S. Madhusoodhanan, S. Bhattacharya, G. K. Moghaddam, and K. Hatua, "Design considerations and performance evaluation of 1200 V, 100 A SiC MOSFET based converter for high power density application," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 4278–4285.

[90] "SiC half bridge module CAS120M12BM2, Wolfspeed Power," http://www.wolfspeed.com/Power/Products/SiC-Power-Modules/SiC-Modules/CAS120M12BM2, accessed: May 2016.

[91] "SiC MOSFET C2M0080120D, Wolfspeed Power," http://www.wolfspeed.com/c2m0080120d, accessed: May 2016.

[92] A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, "A field-effect electron mobility model for sic mosfets including high density of traps at the interface," *Microelectron. Eng.*, vol. 83, no. 3, pp. 440–445, 2006.

[93] B. Callanan, "Application considerations for silicon carbide MOSFETs," *Cree Inc. Application Note*, 2011.

[94] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John Wiley & Sons, 2006.

[95] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "A novel gate assisted circuit to reduce switching loss and eliminate shoot-through in SiC half bridge configuration," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 3058–3064.

[96] M. C. Caponet, F. Profumo, R. W. De Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 225–231, Mar. 2002.

[97] B. Callanan, "SiC MOSFET double pulse fixture," *Cree Inc. Application Note*, 2011.

[98] F. Guide *et al.*, "Reliability methodology for electronic systems," *FIDES group*, 2009.

[99] P. Charpenel, F. Davenel, R. Digout, M. Giraudeau, M. Glade, J. Guerveno, N. Guillet, A. Lauriac, S. Male, D. Manteigas *et al.*, "The right way to assess electronic system reliability: Fides," *Microelectronics reliability*, vol. 43, no. 9-11, pp. 1401–1404, 2003.

[100] M. Held and K. Fritz, "Comparison and evaluation of newest failure rate prediction models: Fides and riac 217plus," *Microelectronics Reliability*, vol. 49, no. 9, pp. 967–971, 2009.

[101] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules-various factors influencing lifetime," in *Proc. CIPS*, vol. 11, 2008, p. 13.

[102] J. Falck, M. Andresen, and M. Liserre, "Active thermal control of igbt power electronic converters," in *Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE*. IEEE, 2015, pp. 000 001–000 006.