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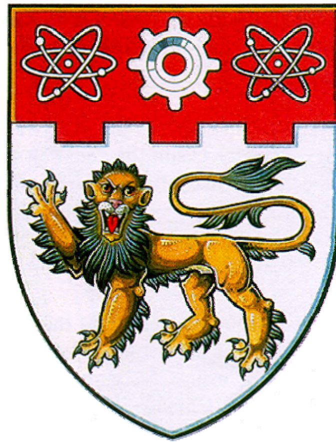
LOW TEMPERATURE POLYCRYSTALLINE SILICON THIN FILMS AND THIN FILM TRANSISTORS



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2006

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Low Temperature Polycrystalline Silicon Thin Films and Thin Film Transistors

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A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2006

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ABSTRACT

Low temperature polycrystalline silicon (LTPS) and LTPS thin film transistors (TFTs) have attracted great attention in recent years, with promising applications in flat panel displays as pixel addressing devices and circuit constructing components. High-quality LTPS films are necessary to achieve better device performance. Thermal crystallization techniques, including solid phase crystallization (SPC) and metal induced lateral crystallization (MILC) using nickel (Ni), are studied in this thesis. For SPC process, a low temperature limit is observed and process optimization is proposed. For MILC process, the lateral crystallization behavior is investigated and dendritic lateral growth behavior in micron scale is observed. Electric field effect on MILC process was also studied. Besides the field enhancement effect on the lateral diffusion of Ni, Joule heating was found to play a role as well to enhance the crystallization effects. Subsequently the detailed effects of grain boundary numbers along a TFT channel on the device performance are inspected by numerical simulation. Based on the simulation results and the studies on MILC process, an effort to obtain large, continuous grains is successfully made. LTPS TFTs by MILC are fabricated, with high level of uniformity and good performance capable of circuit construction. The device performance dependence on the device dimensions, Ni source pattern, and the gate dielectric process, is compared.

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TABLE OF CONTENTS

Page No.

ACKNOWLEDGEMENTS i

ABSTRACT ii

List of Figures vii

List of Tables xiii

Chapter 1 INTRODUCTION 1

1.1 Background 1

1.2 Motivation and objectives of the thesis 3

1.3 Contributions of the thesis 5

1.4 Thesis organization 7

Chapter 2 REVIEW OF LOW TEMPERATURE POLY-SI THIN FILMS AND THIN FILM TRANSISTORS 9

2.1 Requirement of thin film transistor for display applications 9

2.1.1 Pixel driving requirements for thin film transistor 9

2.1.2 Circuit integration requirements 15

2.2 Semiconductors for thin film transistors 16

2.3 Low temperature poly-Si Technology 19

2.3.1 Structure of polycrystalline silicon thin film transistor 19

2.3.2 Crystallization technologies of amorphous silicon films 20

Chapter 3 SOLID PHASE CRYSTALLIZATION OF AMORPHOUS SLILICON FOR THIN FILM TRANSISTORS 24

3.1 Solid phase crystallization of amorphous silicon 24

3.1.1 Amorphous silicon preparation 24

3.1.2 Mechanisms 27

ATTENTION: The Singapore Copyright Act applies to the use of this document. Nanyang Technological University Library

3.1.3 Uniformity and roughness 28

3.1.4 Temperature dependence..30

3.1.5 Time dependence...32

3.1.6 Process optimization considerations.....................................38

3.2 Thin film transistors using solid phase crystallized LTPS films 39

3.2.1 Fabrication of thin film transistors 40

3.2.2 Device characterization 42

3.2.2.1 Threshold voltage extraction.......................................42

3.2.2.2 Other device parameters..45

3.3 Summary 47

Chapter 4 NICKEL INDUCED LATERAL CRSYALLIZATION AND FIELD AIDED LATERAL CRYSTALLIZATION......................49

4.1 Introduction...49

4.2 Experiment details 51

4.3 Investigation on the crystallization behavior 52

4.3.1 Metal induced lateral crystallization 52

4.3.2 Field aided lateral crystallization..57

4.4 Application of *in situ* resistance measurement in crystallization process study 61

4.4.1 Experimental details 62

4.4.2 Measurement results and analysis 63

4.4.2.1 Exponential decay of resistance..................................63

4.4.2.2 Field enhancement factor 67

4.4.2.3 Chaotic fluctuation at FALC low resistance stage........68

4.4.2.4 Crystallization characteristics 70

ATTENTION: The Singapore Copyright Act applies to the use of this document. Nanyang Technological University Library

4.5 Summary 72

Chapter 5 FORMATION OF LARGE CONTINUOUS GRAINS BY FALC PROCESS 73

5.1 Numerical analysis of grain boundary effects on TFT performance 73

5.1.1 Introduction 73

5.1.2 Simulation method..74

5.1.3 Simulation Results and discussion 76

5.1.4 Conclusion on grain boundary number dependence 83

5.2 Large continuous grains by field aided lateral crystallization 84

5.2.1 Field aided lateral crystallization process..............................84

5.2.2 Results and analysis..85

5.2.2.1 Raman spectroscopy 85

5.2.2.2 Observation of the LTPS grains...................................86

5.2.2.3 Polarity dependence of the crystallization behavior 90

5.3 Summary 92

Chapter 6 THIN FILM TRANSISTORS BY NICKEL INDUCED LATERAL CRYSTALLIZATION 93

6.1 Fabrication of thin film transistors...93

6.2 Characterization of thin film transistors 97

6.2.1 Device performance..97

6.2.2 Scaling effects 102

6.2.3 The geometric effect of Ni patterning 106

6.2.4 Effects of SLTO and GLTO 112

6.3 Summary 115

ATTENTION: The Singapore Copyright Act applies to the use of this document. Nanyang Technological University Library

Chapter 7 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK 116

7.1 Conclusions 116

7.2 Recommendations for further studies 118

AUTHOR'S PUBLICATIONS 122

Bibliography 124

Appendix A SPC LTPS TFT PROCESS STEPS 142

Appendix B DESCRIPTION OF THE LAYOUT 145

ATTENTION: The Singapore Copyright Act applies to the use of this document. Nanyang Technological University Library

List of Figures

Page No.

Fig. 2-1 LCD pixel circuit structure (a) and the voltage waveform of pixel electrodes under frame inversion mode (b) 10

Fig. 2-2 An OLED pixel contains at least 2 TFTs (a). In practical designs, more than 2 TFTs are used (b) if a-Si TFTs are to be used, in order to compensate the V_{TH} shift. 14

Fig. 2-3 Schematic of a top-gate, self-aligned N-channel TFT structure 20

Fig. 3-1 3-D AFM image of deposited a-Si, showing a low degree of surface roughness 26

Fig. 3-2 Raman Spectroscopy of 90nm a-Si film, prepared by LPCVD at 550 ºC on SiO_2.. 27

Fig. 3-3 Surface morphology of 90nm poly-Si films SPC annealed at 600 °C for 24(a) and 72(b) hours 29

Fig. 3-4 Raman spectroscopy of 90 nm poly-Si SPC annealed for 6 hours at temperatures between 500 to 590 ºC. The Raman spectrum of crystalline Si (100) is also shown for comparison.............................. 31

Fig. 3-5 Cross-section TEM image of LTPS film, annealed by SPC at 600 ºC for 24 hours. (a) Bright field, (b) Dark field.................................. 32

Fig. 3-6 HRTEM of LTPS films by SPC annealing at 600 ºC. (a) 6 hours, (b) 24 hours... 34

Fig. 3-7 Sheet resistance of LTPS films vs. SPC annealing time at 570 °C and 590 °C 36

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Fig. 3-8 SPC annealed poly-Si grain sizes derived using Scherrer's equation 38

Fig. 3-9 Main process steps in SPC LTPS TFT fabrication 41

Fig. 3-10 Transfer characteristics of fabricated SPC LTPS TFTs 43

Fig. 3-11In linear region, field effect mobility is a function of V_G. The maximum value in the measured range is extracted as the device mobility.. 45

Fig. 3-12 Output characteristics of fabricated SPC LTPS TFTs. 46

Fig. 4-1 Definition of MILC regions 52

Fig. 4-2 SEM images of MILC LTPS film (90nm) after Secco etching. (a) Nickel covered region, (b) MILC region, near lateral crystallization front.. 53

Fig. 4-3 AFM image of Ni MILC front (Secco etched) showing the dendritic lateral crystallization behavior and mosaic structures of subgrains. The arrows indicate the boundaries between subgrains.. 55

Fig. 4-4 Schematic of Ni silicide mediated lateral crystallization of a-Si. The plane-filled precipitate illustrates one that initiates in-plan lateral growth... 55

Fig. 4-5 SEM images of LTPS films after Secco etching. (a) MILC front, (b) FALC front. The film is processed at 500 ºC for 5 hours, under no electric field (MILC sample) or 600 V/cm electric field (FALC sample). A clear FALC front can not be precisely defined due to the sparse distribution of the crystallites. 58

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Fig. 4-6 Optical micrograph of the nickel diffused region between two nickel pads, showing the electric field enhancement of nickel induced lateral crystallization with the FALC front indicated. The film is processed by FALC at 500 ºC for 5 hours, under 600 V/cm electric field. No Secco etching is applied................................60

Fig. 4-7 Schematic of the *in situ* resistance measurement set-up 63

Fig. 4-8 *In situ* resistance versus annealing time for MILC and FALC processed a-Si film at 500 °C. The electric field for FALC is 100 V/cm. 64

Fig. 4-9 Dependence of resistance fitting parameters, t_c, A, and R_0, on the annealing temperature for MILC processed a-Si film. 66

Fig. 4-10 AFM image of annealed a-Si at silicide diffusion front (a) Planer view; (b) 3D view...69

Fig. 4-11 Optical microscope images of Ni diffusion regions from (a) the positive and (b) negative electrodes. The Ni diffusion front in (b) has been darkened to present a high contrast for better visualization..70

Fig. 4-12 Raman spectra at various regions of MILC LTPS thin films. The curves have been shifted vertically for clarity.............................72

Fig. 5-1 TFT mesh structure used in numerical simulation 75

Fig. 5-2 Energy states distribution assigned to grain boundaries 75

Fig. 5-3 Transfer (a) and output characteristics (b) of TFTs with various number of grain boundaries in the channel 77

Fig. 5-4 Threshold voltage and field effective mobility dependence on grain boundary number in channel 79

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Fig. 5-5 Effects of grain boundary number on field distribution....................... 80

Fig. 5-6 Effects of grain boundary number on subthreshold swing and kink effects 81

Fig. 5-7 Effects of grain boundary number on I_{OFF} and I_{ON}/I_{OFF} ratio 82

Fig. 5-8 Schematic diagram of the FALC process set-up................................. 84

Fig. 5-9 Optical micrograph of the FALC sample (Secco etched) near the cathode with various zones marked.. 85

Fig. 5-10 Raman spectra for various FALC zones, as-deposited amorphous silicon thin film and crystalline silicon............................ 86

Fig. 5-11 SEM images of Secco etched poly-Si films. 87

Fig. 5-12 SIMS analysis for two-dimensional distribution of Ni concentration around the crystallization front. The sample under test was Secco etched. Ni concentration is proportional to the density of the white spots. 89

Fig. 5-13 Polarity dependence of Ni diffusion and crystallization effects 90

Fig. 6-1 Process steps of MILC TFTs.. 94

Fig. 6-2 MILC process sequence in LTPS TFTs with sacrificial LTO 95

Fig. 6-3 Optical microscopy image of a fabricated p-channel TFT, with W/L=8μm/4μm. MILC starts from both source and drain sides. No difference is observable between p- and n-channel TFTs under microscope.. 96

Fig. 6-4 Optical microscopy image of TFTs in display panels......................... 97

Fig. 6-5 I_D-V_G and I_D-V_D characteristics of a p-channel MILC TFT, with W/L=16μm/4μm. The extracted device parameters are as follows: (1) MILC TFT: V_{TH}= -4.95 V, μ_{FE}=71.38 cm^2/V*s, S_S= -0.51

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V/dec, I_{ON}/I_{OFF}=1.32x10^7; (2) Non-MILC TFT: V_{TH}= -9.56 V, μ_{FE} = 0.29 cm^2/V*s, S_S= -1 V/dec, I_{ON}/I_{OFF}=2.5×10^4. 98

Fig. 6-6 I_D-V_G and I_D-V_D characteristics of an n-channel MILC TFT, with W/L=16µm/4µm. The parameters extracted are as follows: V_T =3.89 V, μ_{FE}=70.29 cm^2/V·s, S_S=0.85 V/dec, and I_{ON}/I_{OFF} =2.27×10^6. The I_{OFF} at V_D = 10V is 7.99×10^{-11}. 100

Fig. 6-7 Comparison on characteristics of devices at different locations on the same substrate. The glass substrate is of the same dimension as a 4-inch Si wafer. 101

Fig. 6-8 Device parameters (a) and output characteristics (b) of p-channel TFTs with different dimensions but the same aspect ratio of W/L=0.5 103

Fig. 6-9 The ON and OFF current of MILC devices with various sizes 105

Fig. 6-10 Optical micrograph MILC processed active island, in a device with single side Ni source, and W/L= 4 µm / 64 µm........................105

Fig. 6-11 Schematic showing the Ni source pattern and its diffusion effects 107

Fig. 6-12 The effects of Ni source pattern on device performance: Line vs. oval pattern. (a) n-TFTs, (b) p-TFTs. 108

Fig. 6-13 The collection angle as a function of channel width. The inset shows the relative location of the Ni source to the channel. 110

Fig. 6-14 Leakage current dependence on device widths..............................111

Fig. 6-15 The effects of LTO process sequence in MILC on device performance. 113

Fig. 7-1 Schematic for guided laser-MILC...119

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Fig. B-1 Layout of one device matrix 145

Fig. B-2 A TFT (10μm/8μm) in a CM_D type matrix. 146

Fig. B-3 Alignment mark between ACTIVE and Ni Opening 147

Fig. B-4 (a) Etch cells and (b) a processed etching cell (layer ACTIVE). 147

Fig. B-5 Contact chain between GPoly and METAL1. 147

Fig. B-6 Sheet resistance measurement structure for layer GPoly. (a) Designed layout; (b) Fabricated pattern, after METAL1 and passivation. 148

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List of Tables

Page No.

Table 2-1 Comparison between a-Si and LTPS TFT technologies 18

Table 2-2 Comparison between MOSFET and LTPS TFT technologies 21

Table 2-3 Comparison of low temperature crystallization techniques of a-Si 23

Table 3-1 Process parameters for LPCVD 160 nm a-Si 25

Table 3-2 Characteristics of SPC LTPS TFTs 44

Table 6-1 Device performance of MILC TFTs with comparison with reported data. 101

Table 6-2 Ni pattern dependence of MILC n-channel TFTs 108

Table 6-3 Ni pattern dependence of MILC p-channel TFTs 109

Table 6-4 Comparison between device parameters of TFTs by GLTO and SLTO 114

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Chapter 1 INTRODUCTION

1.1 Background

Display comprises a great diversity of technologies. The most conventional one, cathode-ray tube (CRT) display is still the most common type of display today. CRT enjoys simple structure and matured fabrication process at trimmed cost. But it is heavy, bulky and radiation hazardous. Flat-panel display (FPD) avoids or alleviates these problems intrinsically with their slim structure. FPDs have been gaining popularity because they are lightweight, compact, and low power-consuming. The expansion of FPD can be observed in people's everyday life, as more FPD TVs and computer monitors go into families and offices.

Among the FPD technologies, liquid-crystal display (LCD) is currently dominating. The annual sale of active-matrix LCD (AMLCD) has been growing rapidly, reaching that of CRT by year 2002 [1]. AMLCDs have been applied in a comprehensive range of screen sizes from small (e.g. mobile phones and viewfinders for digital cameras), to medium (e.g. laptop or desktop monitors), and to large (e.g. large-screen LCD TVs) panels. LCD is not emissive display. It needs backlight, which prevents it from being as slim as organic light-emitting-diode display (OLED). The viewing angle and image quality under bright environment (e.g. sunlight) are inferior to that of emissive displays. OLED is an emissive display, which exhibits wide viewing angle, potentially very light weight, good luminance and contrast under bright environment. It is

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regarded as the most promising next-generation display technology and has attracted much research interest in recent years [2].

There are two main types of electronic driving schemes for LCDs and OLEDs, namely passive-matrix (PM) and active-matrix (AM) driving. PM is simple and suitable for small size, low information-content displays. In passive driving, the pixel matrix is defined by crossed rows and columns of electrode lines. A pixel is selected by applying a voltage on the corresponding row and column. This simplicity of PM driving comes at the cost of performance limitation. The passive-matrix addressing suffers from crosstalk, which degrades the contrast because the voltage is also applied on the adjacent, un-selected pixels through signal coupling. The display panel size is limited by the resistance of the electrode in passive driving. In OLED driving, a pixel is generally driven at a large peak current to obtain high luminance, which degrades the OLED device stability [2]. These issues are overcome in AM driving, in which each pixel is independently accessed, similarly to the addressing in a semiconductor memory array. Each pixel is turned on the desired brightness through an individual switch, which is commonly thin-film transistor (TFT). The crosstalk is minimized because each pixel is independently addressed. In OLED display pixels, only a small current is applied since the voltage signal can sustain during the whole frame time. And there is no inherent limitation in size or resolution with an active-matrix driving scheme, making it suitable for the fabrication of large sized, high-information-content displays.

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The most widely used TFTs for AM driving are amorphous silicon (a-Si) TFTs. However, since the introduction of low-temperature polycrystalline silicon (LTPS) TFTs [3], they have emerged in many products, replacing the role that a-Si TFTs play. The main advantage of LTPS TFT is its higher mobility, which enables its higher driving speed and larger current delivery capability.

1.2 Motivation and objectives of the thesis

Currently, there is a strong demand for faster switching speed and higher current delivering capability for driving devices, which requires higher carrier mobility of the semiconducting materials for TFTs. Firstly, the product development of handheld devices requires high resolution, high quality handheld displays, which need smaller switching devices to reach a higher resolution and high aperture ratio. Secondly, with its current driven nature, OLED needs higher current-delivering capability. Although larger width/length (W/L) ratio and higher driving voltage of a-Si enable its application in OLED, the aperture ratio is much lower than LTPS TFT pixels for bottom structure OLED [4]. Finally, high mobility of TFT is prerequisite for circuit integration, which has been an attractive target. Driver integrated circuit (IC) occupies more than 15 percent of TFT-LCD product cost [5], which can be lowered if the driver and controller ICs are integrated on the TFT backplane. In addition, integrating the driving electronics on the panel – which otherwise would be handled by external very large-scale integration (VLSI) – will enhance product yield (e.g. by elimination of the tab bond for driver ICs onto the TFT

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connection bus, where most failure occurs [6]). With higher integration enabling TFT performance, system-on-glass (SOG) is achievable. An 8-bit Z80 CPU has been successfully integrated on LCD glass, demonstrating the feasibility of SOG [6, 7].

LTPS TFT is the technology of choice for high mobility TFTs. To obtain LTPS films, there exist a few techniques, among which excimer laser annealing (ELA) has been most widely adopted. Nevertheless, the laser scanning over a large panel area introduces a uniformity problem, due to the laser energy fluctuation and beam overlapping. Additionally, ELA is an expensive process. Thermal annealing, on the other hand, is simple and isothermal over the substrate. While not as high as that of ELA LTPS films, the mobility of LTPS films by thermal annealing is still more than one order higher than that of a-Si. Since a-Si TFT has proven its applicability in AMLCDs and AMOLEDs [8-10], thermal annealing processed LTPS films have their applications. Moreover, the so-called metal induced crystallization (MIC), a catalyst assisted thermal annealing process, can achieve mobility two orders higher than a-Si, which is adequate for circuit integration [11]. Having the potential to offer both better large area uniformity and adequate mobility at lower process cost, thermal annealing deserves further study.

The motivation of this thesis is to further investigate the thermal annealing, including the mechanisms and process engineering for better performance, and figure out which one is most optimistic for application in manufacturing. Though many studies have been conducted on solid-phase crystallization (SPC), metal induced crystallization (MIC), and metal induced lateral crystallization

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(MILC) processes to obtain LTPS film and LTPS TFTs, thermal annealing has not found its application in mass production. SPC and MILC are expected to find their own specific applications but further improvement is needed.

The primary objective of this thesis is to investigate the thermal crystallization of a-Si films. A-Si is prepared by low pressure chemical vapor deposition (LPCVD) on amorphous substrate. LTPS films examined are obtained from a-Si films by thermal annealing process, including solid phase crystallization (SPC) and metal induced lateral crystallization (MILC). In the latter process, certain kind of metal is introduced to lower the activation energy and thus the process temperatures. The catalyst metals selected is nickel (Ni). Devices are subsequently fabricated after the SPC and Ni-MILC processes. The major purpose of the study is to get a better understanding of the behavior of the crystallization process of a-Si films. And thus to improve the thermal treatment processes in order to obtain high-quality LTPS films on amorphous substrates, which are suitable to be applied in LTPS TFTs and in fabricating high-performance LTPS TFTs.

1.3 Contributions of the thesis

Listed below describes the contribution of this thesis, among which there are original works as described.

(1) The SPC effects as a function of process temperatures and durations are studied. LTPS films are characterized in terms of the surface profile, microstructures, grain sizes and resistivity. Low temperature limit of 560 ºC is for the first time defined for SPC process. Annealing stages before

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and after the coalescence of most crystallites are for the first time defined as ‘primary crystallization’ and ‘secondary crystallization’ stages. The latter is proposed to be the stage where an annealing may stop at its early stage for practical SPC processes with reasonable cost and result. N-channel TFTs are fabricated on SPC LTPS films and good performance has been obtained.

(2) Ni induced MIC and MILC processes are studied. Dendritic grain growth behavior is observed at micron scale. The crystallization effects are examined in terms of surface profile, microstructure, grain sizes and integrity. For the first time, Joule heating is reported to diminish the polarity dependence. *In situ* resistance measurement is for the first time explored as a characterization method for crystallization processes.

(3) Electrical field effects on MILC are studied, using the field aided lateral crystallization (FALC). The crystalline growth behavior is studied. Strong electrical field is applied in MILC and better LTPS films are obtained. For the first time, totally different diffusion fronts are observed for MILC and FALC processes. Polarity dependence is investigated and Joule heating effect on polarity dependence is for the first time discussed.

(4) Numerical simulation is conducted to investigate the dependence of TFT performance on grain boundaries (GBs). The simulation results provide guidance for the subsequent study on LTPS film process. FALC is applied to obtain continuous grains as large as over 100 μm.

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(5) Device performance comparable to that of conventional ELA LTPS TFTs is obtained, proving the promising potential of MILC technique. Both p- and n-channel devices are fabricated using Ni MILC process. Threshold voltage and mobility values obtained are around -3 ~ -6V and 3 ~ 4V, 70~110 $cm^2/V{\cdot}s$ and 60~80 $cm^2/V{\cdot}s$, for p- and n-channel TFTs, respectively. ON/OFF current ratio achieved is as high as $1.4{\times}10^7$. Devices performance is dependent on device dimensions, the geometry of the Ni source pattern, and gate dielectric formation process, etc. For the first time, oval- and line-shaped Ni sources are compared and the former is found to render better device performance. The dependence between the device scaling effect and the variation of MILC LTPS quality along the channel length is for the first time investigated.

1.4 Thesis organization

The thesis is organized as follows. In Chapter 1, an introduction to the application background of the LTPS films and LTPS TFTs is presented. In Chapter 2, the TFT technology and LTPS film technologies are reviewed. In Chapter 3, SPC processes, including SPC temperature and time dependence, process optimization, are studied. SPC LTPS TFTs with good performance are successfully fabricated. In Chapter 4, Ni MILC processes, including MILC behavior, effects of electric field, *in situ* resistance measurement for process characterization, are discussed. In Chapter 5, an effort is made to achieve large, continuous grains by FALC process. The effects of grain boundaries on the TFT devices are studied by numerical simulation. And then suitable process

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parameters are selected to obtain larger, continuous grains. In Chapter 6, Fabrication and characterization of MILC LTPS TFTs are presented. Both n- and p-channel devices with high performance are successfully fabricated. Device performance depends on some structure and processes, including device dimensions, Ni source patterns, and the formation method of the gate dielectric. In Chapter 7, conclusion of the thesis is given and some suggestions for future work are proposed.

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Chapter 2 REVIEW OF LOW TEMPERATURE POLY-SI THIN FILMS AND THIN FILM TRANSISTORS

2.1 Requirement of thin film transistor for display applications

TFTs have been studied for several decades, with its original expected function for electrical circuits instead of driving displays. Since the first concept of field-effect device based on thin films [12], TFTs have undergone extensive evolution in almost every aspect, the most important being material advancement. For many years, TFTs had been overshadowed by the astonishing development of metal-oxide-semiconductor field-effect transistor (MOSFET) [13]. Things changed dramatically after AMLCDs were introduced by adding a non-linear circuit element – a TFT, at every x-y intersection of the LCD matrix [14]. The boom in LCD inspired intense research activity on TFT and the improvement of TFT performance, in turn, helps to boost the LCD industry.

The development of LTPS TFTs is driven by their applications or potential applications in FPDs, which can be distinguished by the purposes of TFTs: pixel driving and circuit integration. In both cases, the demands for main device properties are similar but there is varied emphasis.

2.1.1 Pixel driving requirements for thin film transistor

The equivalent circuit for one LCD pixel is shown in Fig. 2-1(a). It consists of a TFT, one storage capacitor (C_{ST}), and one liquid crystal capacitor (C_{LC}) constructed by the pixel electrode and the common electrode. This

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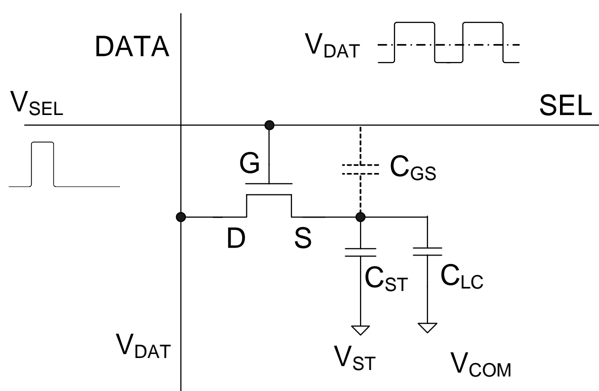
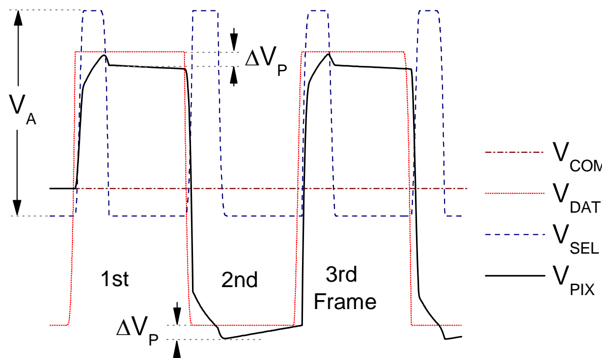
structure looks quite similar to a cell of dynamic random access memory, except for the excess capacitor which is designed for better retention capability of the signal charge. The pixel refreshing operation is also quite similar to the 'write' operation of a DRAM cell. When the pixel is addressed, the TFT is switched on. The voltage signal on the data line is transferred to the pixel electrode by charging the two capacitors. When other rows are addressed, the TFT is turned off and the capacitors hold the charge until the next refresh cycle.



(a)



(b)

Fig. 2-1 LCD pixel circuit structure (a) and the voltage waveform of pixel electrodes under frame inversion mode (b)

In conventional MOSFET definition, a drain electrode is the electrode biased at a higher voltage level for n-channel MOSFET or the electrode biased

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at lower voltage level for p-channel MOSFET, than the source electrode. However, as shown by V_{DAT} in Fig. 2-1(b), the polarity of data electrode is alternating because liquid crystal does not work properly under direct current (DC) bias. For simplification, the electrode on the data line side is defined as the drain electrode and the other terminal as the source.

Analysis on the pixel charging behavior reveals the demand for TFT parameters [15]. Since the frame refresh is accomplished by line-by-line scanning, each line of pixels are assigned limited addressing time, within which the data voltage must be transferred to the pixel electrode. This poses the requirement on TFT's ON-state conductance, which is proportional to the W/L ratio and μ_{FE} of the TFT. Assuming a charging behavior from the negative maximum to the positive maximum of V_{DAT}, the TFT must satisfy the following equation,

$$\left(\frac{W}{L}\right)\mu_{FE} > k_t \frac{m}{t_f - mt_d} \cdot \frac{C_{PIX}}{C_I} \cdot \left(V_{SEL} - V_{TH} - V_{DAT}\right) \qquad \textbf{(2-1)}$$

Where m is the number of scan lines, t_f is the frame time, C_{PIX} is the pixel capacitance, which equals the sum of C_{GS}, C_{LC} and C_{ST} shown in Fig. 2-1(a), C_I is the TFT gate insulator capacitance per unit area, μ_{FE} is the field-effect mobility, W and L are the width and length of the TFT, V_{TH} is the threshold voltage of the TFT and t_d is the signal delay on the inter-connection wires. The meaning of V_{SEL} and V_{DAT} is shown in Fig. 2-1. $t_f - mt_d$ is the sum of charging time within a frame (and $\frac{t_f - mt_d}{m}$ is the charging time for one pixel). k_t is a

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function of V_{SEL}, V_{TH}, V_{DAT}, and charging ratio r_c. which denotes the ratio between pixel voltage when charging is complete and V_{DAT}.

Mobility of a-Si TFTs is limited to around 1 $cm^2/V\cdot s$. For small or medium sized displays with a moderate value of m, a-Si:H TFTs with reasonable W/L ratio can be utilized for driving. However, with the increasing of display panel sizes and resolution, m will rapidly increase. From Eq. 2-1, if a-Si:H TFTs are used, their W/L ratios can become unreasonably large, say, a few tens to 1. In ref. [15], using numerical values of C_{PIX}=1 pF, μ_n=0.5 cm^2/vs, C_I=20 nF/cm^2, V_{SEL}=13V, V_{TH}=1V, V_{DAT}=8V, t_d=10 µs, m=480, refresh frequency f=60 Hz, W/L ratio needs to be no less than 4.3. If m changes to 768 or 1080, W/L ratio needs to change to 9.1 and 19.6, respectively. This huge ratio impairs the pixel aperture ratio because the width of the TFT is so large that it consumes a large area in the pixel, leading to lower aperture ratio. The field effect mobility, μ_{FE}, of LTPS TFT is one or two orders higher than a-Si TFT, so in terms of its driving capability, LTPS TFT is prefered as switching device in high difinition LCDs since LTPS TFTs occupies smaller area than a-Si TFTs for same driving capability.

It is worth mentioning that recently demonstrated large AMLCD panels (besides the 54" and 55" LCD TV in 2003 [9, 16], Samsung even demonstrated an 82" LCD TV [17].) are based on a-Si TFT backplane. It is understandable that a-Si TFT was used. Firstly, a-Si TFTs are cost effective compared with LTPS TFTs. Secondly, a-Si process is capable of deposition over very large area but current LTPS process has uniformity problem over such large area as generation 5 glass. Thirdly, the resolution of the display has not increased

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proportionally as the panel dimension. The 82" LCD TV still uses HDTV format: 1920 columns by 1080 rows of pixels. Some techniques are developed to help the application of a-Si for such large panel displays. These techniques include improving a-Si TFT performance to obtain mobility around 1 cm^2/Vs, careful design to minimize data line delay (t_d in eq. 2-1), and revised driving electronics that may include overdriving function [18], etc. Besides, the pixel area is much increased, as allows larger W/L ratio of a-Si TFT if necessary.

There is inevitablely leakage of the stored charge on C_{PIX} in an AMLCD pixel. For sufficient charge retention capability, the leakage time constant needs to be much larger than t_f. Assume this is the case, the ratio of the R_{OFF} and R_{ON} is obtained [15]

$$\frac{R_{OFF}}{R_{ON}} > \frac{k_t m\left(1+\frac{R_{OFF}}{R_{LC}}\right)}{(1-r)} \qquad \textbf{(2-2)}$$

where r is the charge retention ratio, i.e. the percent of charge left until next refresh cycle. Since the value of r is required to be very close to 1, m is a large number, and k_t is a number larger than 1 [15], the ratio requirement of R_{OFF}/R_{ON} is quite large. A high resistive off state, or a very small leakage current, is necessary.

It is also observable that there is a voltage shift at the negative margin of the TFT gate pulse, which results from the voltage coupling across the parasitic capacitance C_{GS} as shown in Fig. 2-1. The voltage shift ΔV_P can be written as:

$$\Delta V_P = V_A C_{GS} /(C_{GS} + C_{ST} + C_{LC}) \qquad \textbf{(2-3)}$$

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where, V_A is the gate voltage pulse amplitude. This voltage shift causes undesirable effects on the performance of the LCD such as flicker, image sticking and permanent brightness non-uniformities on the panel [15]. To minimize the voltage shift, lowering V_A and C_{GS} is a possible solution. The former requires a smaller V_{TH} because its value must ensure that the TFT is working in linear region. Otherwise there is a voltage loss (in the positive charging cycle for n-channel TFT and in the negative cycle for p-channel TFT) similar to the V_{TH} lost in NMOS pass-gate logic. To reduce C_{GS}, one needs to minimize the overlap between the gate electrode and the source. Self-aligned source/drain ion implantation process is such a method which uses the gate electrode to define the source and drain regions and the overlap is minimized.

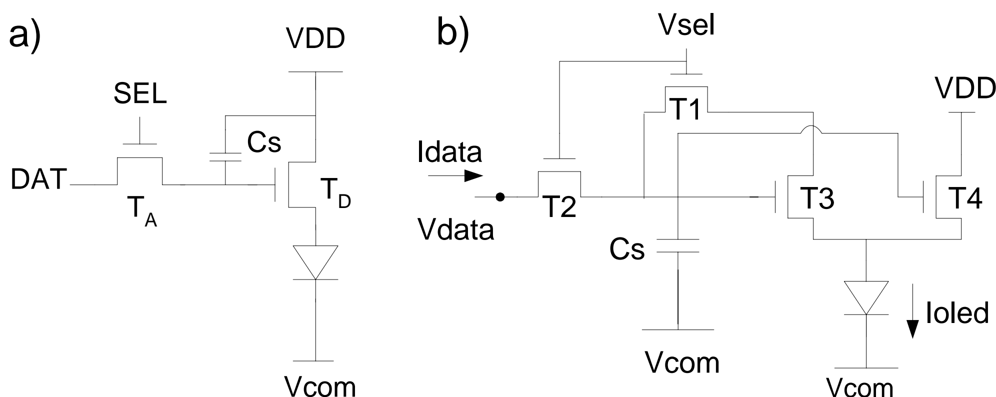

Fig. 2-2 An OLED pixel contains at least 2 TFTs (a). In practical designs, more than 2 TFTs are used (b) if a-Si TFTs are to be used, in order to compensate the V_{TH} shift.

As shown in Fig. 2-2, AMOLED pixel circuits consist of at least 2 TFTs: one addressing and one driving TFT [T_A and T_D in Fig. 2-2 (a)]. There needs more than 2 TFTs in V_{TH} shift compensated circuit scheme (e.g. Fig. 2-2 (b) [19]), if a-Si TFTs are to be used. V_{TH} compensated circuits further lower the

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aperture ratio of bottom emission OLED. P-type LTPS TFT can be used in the simple 2 TFT circuit scheme, while a-Si TFT is not capable in practical applications due to its V_{TH} shift. LTPS TFT is more reliable and thus is preferred [20].

2.1.2 Circuit integration requirements

TFT circuit is not widely applied currently because much improvement is still required. The requirements for LTPS TFT circuit integration lie in a few aspects of the TFT parameters.

Field-effect mobility μ_{FE} is the key factor for device speed. In digital circuits, the logic level change of a circuit node is generally charging or discharging processes of the corresponding capacitance load. The speed of these processes is determined by the device on-state current, which is proportional to the mobility.

Threshold voltage V_{TH} is another important factor of concern, especially in mobile applications, where power consumption is to be minimized to prolong the battery lifetime. Higher V_{TH} leads to higher driving voltages and higher power dissipation. However there exist challenges to lower the value of V_{TH}. One is that the threshold voltage of LTPS TFTs is determined by gate electrode, gate dielectric and channel LTPS film. All of them are to be processed at low temperatures, which limit the material quality. Another challenge is the threshold voltage scattering, which lowers circuit noise margin, degrades the circuit speed and brings more complexity to circuit design. Lower V_{TH} poses severer requirement on threshold voltage distribution around the designed value.

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Complementary MOS (CMOS) TFT circuit is more desirable than n-TFT circuit. CMOS TFT circuit typically consumes less power and less area for similar function compared with n-TFT circuit, and operates at higher speed. The expense is a bit of complexity in the manufacture processes.

In summary, the main requirements of an AMLCD pixel for LTPS TFTs are high ON current, low leakage current, high R_{ON}/R_{OFF} ratio, and small parasitic capacitance. LTPS TFTs are suitable for small to medium size AMLCDs with high resolution. LTPS TFTs are preferred in AMOLED pixel compared with a-Si. The desired properties are high mobility and good reliability. For circuit integration, the emphasis is on high field effect mobility, lower threshold voltage with high degree of uniformity.

2.2 Semiconductors for thin film transistors

There are several semiconducting materials which are explored for TFT applications, among which important ones are cadmium selenide (CdSe) [21], a-Si [22], polycrystalline silicon (poly-Si) [23, 24], organic materials [25] and recently, zinc oxide (ZnO) [26-28]. Cadmium selenide exhibits high mobility, but it is a polycrystalline compound and its properties depends on grain size, grain boundary interface states, stoichiometry, etc., and it can be sensitive to ambient gases such as H_2O and oxygen. A-Si:H has no grain boundaries and is more stable and predictable [13], which are determining factors for industry manufacturing. However, a-Si is disordered at the atomic scale and its semiconducting properties is much limited [29]. Typical a-Si TFT has a mobility around 0.5 $cm^2/V\cdot s$ and an ON/OFF current ratio about 10^6. Mobility

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as high as 1.15 $cm^2/V\cdot s$ has also been reported with the so called 'super a-Si TFTs' [10]. Polycrystalline silicon, though also disordered compared with single crystal silicon, is highly ordered compared with a-Si. Poly-Si has much higher mobility than a-Si and is a promising candidate for TFT circuit construction and the addressing for large-sized FPDs or novel display devices such as organic light emitting devices (OLEDs) due to the current driving nature. Mobility of organic active layer adopted for TFT fabrication is reported comparable to that of a-Si:H, of the order of 10^{-1} $cm^2/V\cdot s$. Mobility of 1.5 $cm^2/V\cdot s$ and ON/OFF current ratio of 10^8 has been reported [30]. Organic TFTs are envisioned as viable alternatives to a-Si:H TFTs with low-temperature processing on flexible, lost-cost substrate in applications such as flexible displays and low-end smart cards. They need further study before entering commercial market. Currently, they are mainly of academic interest. ZnO transistor stems from the possibility to fabricate "invisible electronics", which helps to increase the aperture ratio of display devices. Reported results vary significantly on the device processes and device performances [26-28]. Many material and manufacturing issues need to be identified and resolved before their application.

Among these materials for TFT fabrication mentioned above, in history, cadmium selenide has given way to a-Si:H because the latter is more independent on ambient gas, compatible with Si technology, and low-temperature processable. Currently a-Si TFTs are the most commonly used driving devices but their driving capability is very limited due to the low carrier mobility in a-Si. As a result, a-Si:H TFTs can do little on LCD driving electronics and discrete driver chips must be utilized for the display panel,

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which are becoming important portion of component cost in LCD system [6]. Moreover, bonding becomes a complex and expensive task because of the huge number of rows and columns and the necessity to bond every one of them. These two factors make the product cost high. And the FPD products demand for higher definition and better image quality also requires faster driving devices. High definition AMLCDs over 300 dot per inch (dpi), with integrated driver have been developed [31]. Beside the addressing and driving electronics for LCDs, the addressing of OLED needs higher current delivering devices. Polycrystalline silicon thin film transistors (poly-Si TFTs) attract much increasing interest, due to their better performance, mainly the higher driving capability and stability of their threshold voltage.

Table 2-1 Comparison between a-Si and LTPS TFT technologies

	LTPS TFT		a-Si TFT
☺	Higher carrier mobility, smaller TFTs and higher aperture ratio	☹	Lower carrier mobility, limited panel resolution and size
☺	Higher carrier mobility, driver circuit partially integrated with TFTs, more compact and cost saving for small resolution display	☹	Lower carrier mobility, separate LSI or VLSI drivers needed in display fabrication
☺	Better long-term stability	☹	Inferior long-term stability of device parameters
☹	Higher cost due to complexity added for the crystallization process of a-Si	☺	Lower cost
☹	Possible lower production yields due to difficulties of fabricating LTPS TFTs	☺	Well developed fabrication process with higher yield
☹	Inferior uniformity in fabrication	☺	Good uniformity over large area

☺ and ☹ denote advantage and disadvantage respectively.

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The differences between a-Si TFTs and LTPS TFTs are summarized in Table 2-1.

2.3 Low temperature poly-Si Technology

Poly-Si can be produced by high temperature or low temperature processes. For the concern of display applications, LTPS (processable at low temperatures not higher than 600 ^{o}C) is of interest as the typical display substrate, glass, softens and melts at high temperatures. Characteristics of a TFT depend on several factors of the device, including material microstructure, interface, and device structure.

2.3.1 Structure of polycrystalline silicon thin film transistor

Both bottom gate and top gate structures are adopted by LTPS TFT manufactures [32]. Bottom gate structure enjoys the easy conversion from a-Si line to LTPS line for manufacturers. Besides, continuous deposition of gate insulator and active layer is possible, leading to better interface between the two layers. On the other hand, top gate structure has better crystallization control because there is no gate metal under the LTPS film. With careful clean of the surface of the crystallized LTPS film interface problem can be alleviated. Top gate structure can thus yield better TFT performance. It is becoming the preferred structure [32]. In this thesis, top gate structure is studied.

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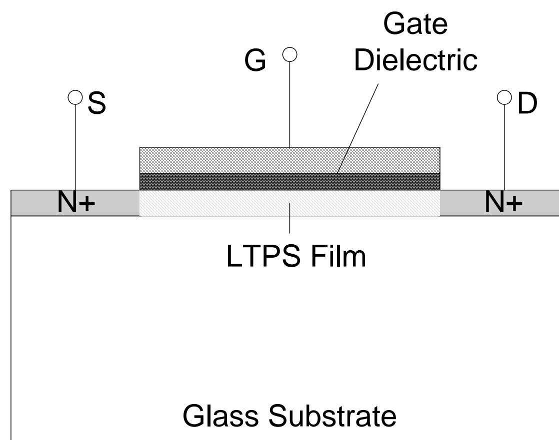

Fig. 2-3 Schematic of a top-gate, self-aligned N-channel TFT structure

A self-aligned top-gate n-channel TFT (n-TFT) is shown in Fig. 2-3. On the amorphous substrate is a thin layer of LTPS film formed by a-Si deposition and a consequent crystallization process. Gate electrode is separated from the LTPS film by a dielectric layer such as SiO_2 or Si_3N_4. Typically ion-implantation is applied to form source and drain regions, using the gate electrode as the implantation mask. The channel region directly under the gate electrode remains undoped.

2.3.2 Crystallization technologies of amorphous silicon films

LTPS TFT fabrication process includes many of the steps encountered in the fabrication of MOSFET for integrated circuits, such as thin film formation, photo lithography, etching, ion implantation, annealing and metallization, etc. However, despite these similarities, there are some critical differences, as illustrated in Table 2-2. Unlike MOSFETs, which are fabricated on monocrystalline Si wafer, TFTs are typically (not always) fabricated on amorphous glass substrates. Since glass is not as heat-resistant as Si wafers, the process temperatures must be constrained within the glass softening endurance.

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The most direct and critical impact from the amorphous substrate is that the semiconducting active layer is not available on the substrate. The layer has to be separately deposited on the host substrate, again with temperature limited processes.

Several techniques have been applied to form LTPS on amorphous substrate, namely, as deposited LTPS, SPC, rapid thermal annealing (RTA), MIC/MILC, and ELA, which are desired to come with low cost and high throughput.

Table 2-2 Comparison between MOSFET and LTPS TFT technologies

	MOSFET technology		LTPS TFT technology
☺	High temperature process acceptable	☹	Low temperature processes. Depend on the specific substrate material
☺	V_{TH}* adjustable by ion implantation	☹	V_{TH} affected by active layer quality
☺	Thin, high-quality gate SiO_2	☹	Low temperature deposited gate dielectric: inferior device performance
☺	Mono crystalline active material	☹	Impurities and defects in active layer
☹	Separate "WELL" regions required	☺	Simple isolation process.

* V_{TH} denotes the threshold voltage;

☺ and ☹ denote advantage and disadvantage respectively.

As-deposited poly-Si is most effective in terms of both productivity and cost, as no post process is needed. But it is inferior compared with after-deposition annealing in terms of poly-Si quality. The field-effect mobility is relatively low and the leakage current is too high [33]. SPC can be processed at low

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temperatures and good uniformity can be obtained by this method, as furnace annealing is isothermal and thus produces poly-Si films with uniform properties over the entire plate [34]. But SPC consumes a long time up to several dozens of hours [35, 36], which is undesirable in manufacturing. MIC/MILC was proposed to shorten the annealing duration and lower the annealing temperature by introducing catalyst (e.g. nickel, aluminum, etc.) into amorphous-Si [16, 37-44]. This process can be further accelerated by applying an electrical field in the crystallization direction [16, 42, 43]. But the metal introduced inevitably causes contamination problem. There are other annealing methods, which apply high temperature but somehow avoid thermal damage to the substrate. Rapid thermal annealing is actually high temperature based. But the time control on the temperature increase and decrease make the high temperature annealing very short to prevent the substrate and the devices fabricated on it from being damaged [45, 46]. Drawbacks of RTP are, (1) more expensive substrate must be used to avoid substrate deformation and breakage, and (2) the crystallized LTPS films contain high density of intra-grain defects, resulting in low carrier mobility and high leakage current in LTPS TFTs. Another low-temperature based process is ELA. ELA is a shallow melting and re-growing process. Relatively good poly-Si can be formed on glass and even plastic substrate [47, 48]. The most common problems that plague the ELA are, (1) the narrow beam size and small process window on laser fluence for large and uniform grain size, and (2) the large surface roughness inherent to this process [48]. Table 2-3 presents a comparison between the different LTPS techniques.

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Table 2-3 Comparison of low temperature crystallization techniques of a-Si

Property of poly-Si	Mobility	Large-area capability	Uniformity	Throughput
As-deposited	★☆☆	★★☆	★★☆	★★★
Furnace anneal (SPC)	★★☆	★★☆	★★☆	★☆☆
Metal Induced Lateral Crystallization	★★☆	★★☆	★★☆	★★☆
Excimer Laser Annealing	★★★	★☆☆	★☆☆	★★☆

Legend: ★—Better; ☆—Poorer

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Chapter 3 SOLID PHASE CRYSTALLIZATION OF AMORPHOUS SLILICON FOR THIN FILM TRANSISTORS

3.1 Solid phase crystallization of amorphous silicon

SPC became of interest for TFT work when it was determined that the field effect mobility was an order of magnitude larger than that for as-deposited poly-Si [29]. Disadvantage of SPC is that it needs high thermal budget, i.e. the product of annealing temperature and annealing time is large. In addition, the grain structure for thermally crystallized poly-Si by this method is inferior to that of laser crystallized films [47, 49]. SPC crystallized poly-Si has smaller grains with a variety of intra-granular defects, mainly threading dislocations and stacking faults. This has led to the decline in interest in SPC for poly-Si device fabrication and SPC is not currently adopted by LTPS AMLCD manufacturers. However, SPC annealed poly-Si can still be much better than a-Si and as-deposited LTPS. Comparing with other crystallization techniques, SPC process has its advantages such as simplicity, low cost, higher degree of uniformity and reproducibility. There exist applications suitable for SPC process, in terms of the trade-off between performance and cost. At this aspect, SPC deserves further study.

3.1.1 Amorphous silicon preparation

A-Si is ideally described as a covalently bonded, fourfold coordinated continuous random network of Si atoms. The atoms statistically distributed on

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the radius direction, which is represented by a radius distribution function [50]. However, the specific property of a-Si films strongly depend on their deposition conditions such as substrate temperature, reactor pressure, and flow rate of process gas. Among them, the deposition temperature is the key factor determining the structures and properties of the films.

Annealing in our experiment is based on a-Si thin films deposited on SiO_2 substrates. Before deposition of a-Si, n-channel <100>-oriented 6-inch diameter silicon wafers, with resistivity of 1-30 Ω·cm, are thermally oxidized to obtain an oxidation layer of 500 nm. This dioxide layer serves as the substitute for glass substrate, which is commonly used for a-Si deposition in the TFT fabrication. 90 or 160 nm thick undoped a-Si was then deposited on the thermally grown silicon oxide. Deposition was conducted using LPCVD reactor by thermal decomposition of undiluted silane gas. This process produced a-Si with relatively lower hydrogen content compared to that produced from plasma enhanced chemical vapor deposition (PECVD), another commonly used deposition technique [29]. The low hydrogen content favors the following crystallization process. Process parameters are tabulated in Table 3-1. The deposition rate is only about 23 Å/min and uniformity of the film is well assured, as shown below.

Table 3-1 Process parameters for LPCVD 160 nm a-Si

SiH_4 flow	Temperature	Pressure	Time	Rate
100 sccm	550 °C	250 mTorr	70 min	~23Å/min

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The atomic force microscopy (AFM) image in Fig. 3-1 shows the morphology of the deposited a-Si. The degree of the smoothness of the films, including a-Si and annealed poly-Si, are most commonly characterized by root mean square (RMS) roughness, which is defined as

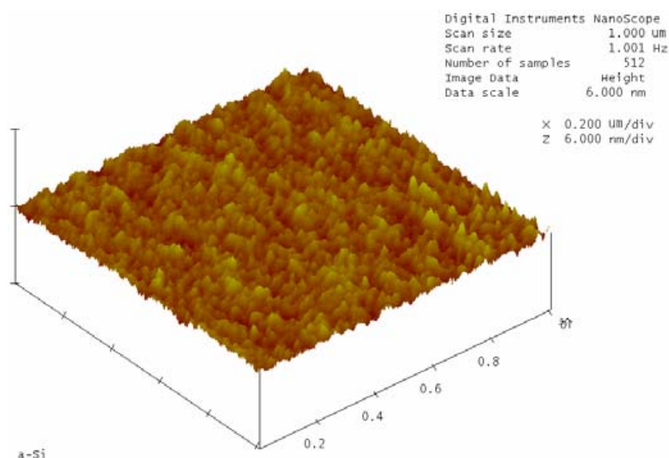

Fig. 3-1 3-D AFM image of deposited a-Si, showing a low degree of surface roughness

$$RMS = \sqrt{\frac{1}{n}\left[\sum_{1}^{n}\left(s(x) - \overline{s(x)}\right)^2\right]}$$

where *s(x)* is the surface height at point x in the surface profile, $\overline{s(x)}$ is the average height of the surface profile, and *n* is the points included in the calculation. RMS was obtained using the AFM attached digital image-processing package. The RMS of the deposited a-Si is 0.21 nm and the maximum roughness is about only 2.62 nm. This value is acceptable for a-Si TFT fabrication as the gate oxide thickness ranges from several tens to more than one hundred nanometer.

Raman spectroscopy (Fig. 3-2) shows the typical a-Si characteristic, with a broad and weak peak at 480 cm^{-1}, possibly due to the thin thickness of 90 nm.

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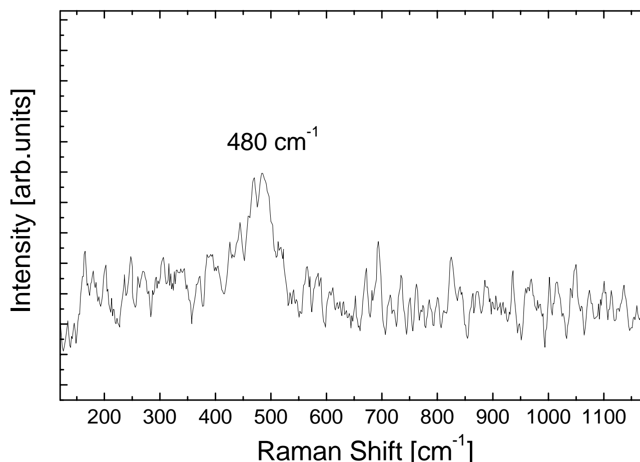

Fig. 3-2 Raman Spectroscopy of 90nm a-Si film, prepared by LPCVD at 550 °C on SiO_2

3.1.2 Mechanisms

A-Si is a metastable phase of Si as it has a higher free energy than crystalline silicon (c-Si). Crystallization is a process involves the rearrangement of the whole Si network to decrease its free energy [51]. The phase transition from a-Si to thermodynamically stable c-Si occurs provided the barrier energy (activation energy) is overcome. In most cases, the phase transition is achieved by thermal annealing methods, among which the initially studied one is SPC.

R. Bisaro has reported that the a-Si crystallization can be divided into two steps: "initialization" and "transition" [52], corresponding to nucleation and grain growth. Besides some crystalline clusters that exist in the prepared a-Si films [51], nucleation of new grains occurs in fine grain regions containing a high density of grain boundaries [53]. Grains grow from the nuclei that formed. And nucleation continues during the annealing process.

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Chemical vapor deposited a-Si generally contains a certain amounts of hydrogen from the reactive gas such as SiH_4 or Si_2H_6. The dehydrogenation proceeds during the crystallization, as complicates the annealing process, though it is not a serious barrier [29]. For fast crystallization process, a dehydrogenation process in advance will improve the following crystallization. In SPC process, the dehydrogenation and crystallization processes are combined. A-Si obtained by LPCVD contains less hydrogen (less than 1 atom percent) than that obtained by PECVD (typically 8 to 20 atom percent). And the former is chosen for our a-Si film deposition.

3.1.3 Uniformity and roughness

SPC is conducted under low vacuum furnace at 3 Torr with N_2 flow (10 sccm) to prevent the film from being oxidized. Temperatures are limited under 600 °C. Annealing time varies from 1 hour to a few tens of hours. Uniformity of the annealed poly-Si surface is well preserved by all the SPC process conditions. This verifies that SPC annealing is isothermal process and can obtain best uniformity because the process parameters are even over the whole sample and the annealing speed is relatively slow.

Surface roughness tends to grow with the annealing process. However, the nucleation occurs uniformly over the film and it progresses during the annealing process. A high density of nuclei constrains the size of the final grains but it favors a smooth surface, as explained in the following.

For SPC process in the experiment, the annealing temperature is relatively low as it is constrained within between 500 and 600 °C. The annealing time is

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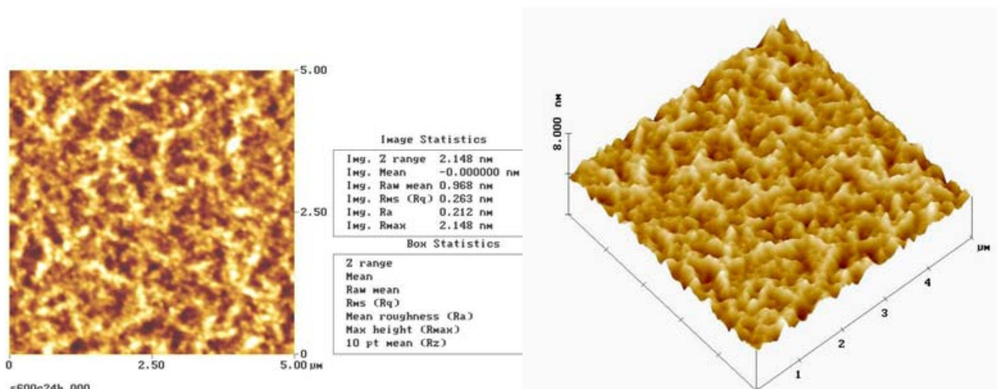
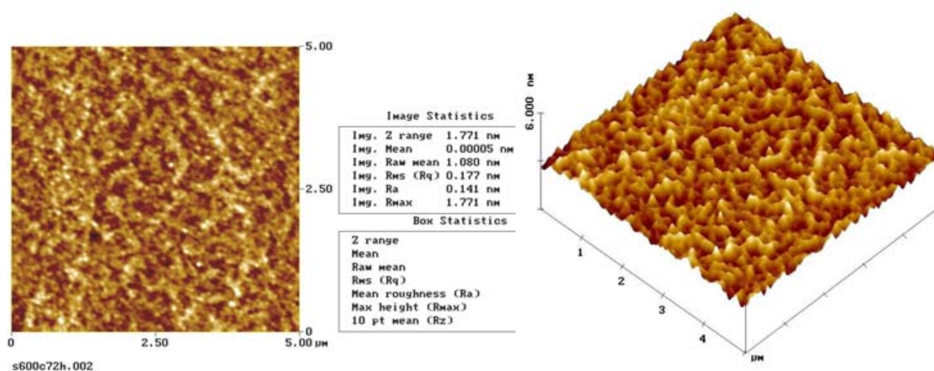
long compared with other annealing methods. In the initialization step, nuclei start to form. The early-formed nuclei grow at very low speed due to the low temperature, which leaves enough time and space for new nuclei to emerge where early-formed nuclei have not occupied. This step enables much more nuclei to be created. Initialization continues as



(a)



(b)

Fig. 3-3 Surface morphology of 90nm poly-Si films SPC annealed at 600 °C for 24(a) and 72(b) hours

the transition proceeds till the volume is mainly occupied with nuclei. In this case, many nuclei form and compete with each other during growth in gaining atoms. Large grains can hardly form and smooth surface is thus obtained, as shown in Fig. 3-3, which shows the results for long time annealing in our experiment at the highest temperature of 600 °C. The roughness of the SPC

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obtained LTPS films is not dramatically changed compared with a-Si. The RMS value is even a little smaller than that of a-Si (0.178 nm for poly-Si vs. 0.239 nm for a-Si). This is strongly desirable for TFT fabrication, because surface roughness degrades the ON current of the device. The scattering effects to carrier transport caused by the roughness of the Si/SiO2 interface dominates at low temperatures and high transverse electrical fields [54]. However, the smooth surface is formed at a cost of smaller grain sizes, which is the disadvantage of SPC.

3.1.4 Temperature dependence

SPC has been conducted with temperatures varying between 500 °C and 600 °C. Fig. 3-4 shows Raman spectroscopy of poly-Si annealed for 6 hours at different temperatures, including the spectroscopy for lightly n-doped single crystal silicon. It is shown that higher temperature steadily favors the crystallization. There exists one transition temperature at about 550 °C. Crystallization of a-Si cannot be achieved at temperatures below 550 °C due to the too slow nucleation and grain growth rate, as shown in Fig. 3-4(a). It has been reported that doping [52] and Si ion implantation [55, 56] of a-Si can improve the crystallization result. This means that the defects and crystalline distortion are critical for initiating crystallization. Some of these kinds of imperfections contribute to the initial nucleation. It was reported that the higher the degree of amorphization, the better the annealing effects [57]. This transition point at about 550 °C corresponds to the crystallization activation energy of the defects, vacancies and dangling bonds in a-Si. The thermal energy enables the atoms at these sites to reconstruct. A weak peak at 520 cm^{-1} emerges on Raman spectrum of SPC at

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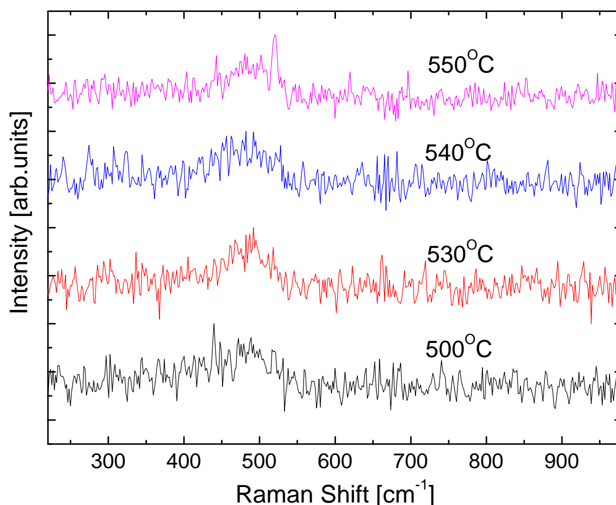
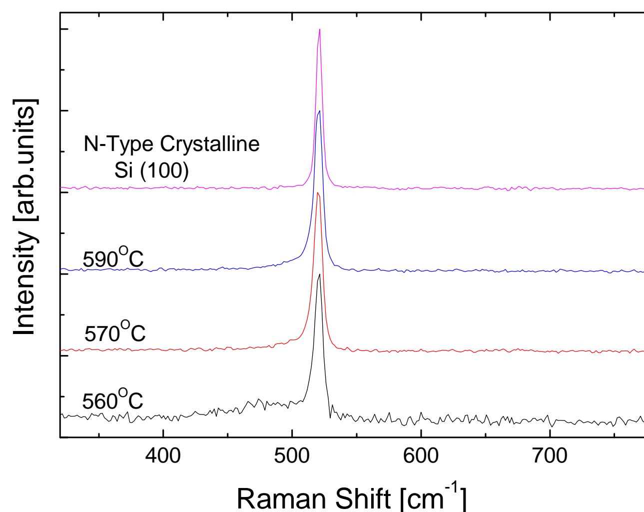
550 ºC. However, from Fig. 3-4(b), there is clearly a much stronger peak at 520 cm^{-1} on the Raman spectrum of SPC at 560 ºC, which is just above the transition point around 550 ºC.



(a)



(b)

Fig. 3-4 Raman spectroscopy of 90 nm poly-Si SPC annealed for 6 hours at temperatures between 500 to 590 ºC. The Raman spectrum of crystalline Si (100) is also shown for comparison.

The crystallization effect of SPC is further demonstrated by the tunneling electron microscopy (TEM) image shown in Fig. 3-5. Columnar grains are clearly visible, which sizes are in the range of a few to around 15 nm. It is also

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observed that the orientation gradually varies in a small range of a few hundred nanometers.

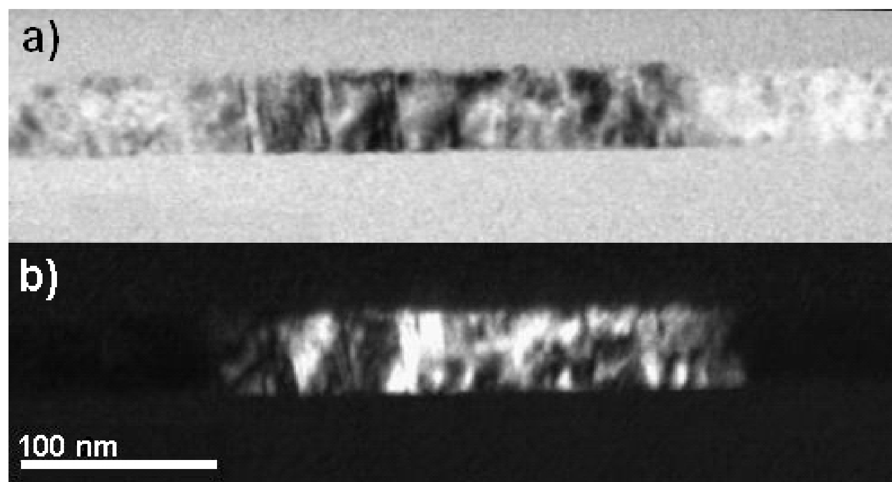

Fig. 3-5 Cross-section TEM image of LTPS film, annealed by SPC at 600 °C for 24 hours. (a) Bright field, (b) Dark field.

The above observation, combined with the limitation of glass softening temperature, defines a window for SPC process between 560 and 600 °C. This small window makes the SPC process less versatile and limits its application to a certain scope.

3.1.5 Time dependence

The grain growth rate is determined by the nature of the driving force that causes the grain growth. Three different phenomena have been reported to influence the grain growth: (1) strain, (2) grain-boundaries and interfaces, (3) impurities and defects. The grain sizes are proportional to the annealing duration, the square root, or the cubic root of the annealing duration, depending on crystallization mechanisms [53]. Here the annealing duration refer to the time during which the SPC process proceeds at a certain fixed temperature.

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However, the above description only applies to the early stage of the crystallization. Obviously, the grain growth rate will change after the grain is in contact with other grains, since the growth kinetics change. Coalescence occurs for many grains when most of a-Si has been converted to crystalline phase. For a better description, we further divide the "grain growth" stage into two steps: "primary crystallization", which represents the nuclei's growth before they touch each other; "secondary crystallization", which represents the grain's growth from their coalescence and thereafter. During crystallization process, when the grains touch each other, they all consume atoms of a-Si matrix at the grain interface and interact with each other. Some preferred orientations begin to grow slowly but steadily and finally become more prominent, at the cost of the consuming of the grains of other orientations, as proven by the high-resolution TEM (HRTEM) images that follow.

Fig. 3-6 shows the HRTEM images of SPC annealed LTPS films, which reveal the microstructure of the film at different annealing stages. Fig. 3-6(a) shows the cross-section HRTEM image of a LTPS film, obtained from 6 hours of annealing of a-Si, at 600 ^{o}C. The film consists of high density of columnar grains, whose longitudinal directions are perpendicular to the film surface. The microstructure suggests that the nucleation does not occur homogeneously throughout the film because otherwise the crystallites will be randomly distributed. It has been reported that nucleation occurs heterogeneously at the interface between a-Si film and the SiO_2 substrate [51, 58]. The formation of columnar grains perpendicular to film surface can be well explained if the thermal crystallization initiates from these nucleation sites at the a-Si/SiO_2 interface. The crystallite grows concurrently from the a-Si/SiO_2 interface

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towards the film surface. Small-sized columnar grains are finally resulted in the film. This type of microstructure introduces large amount of grain boundaries along the film, which are not desired for device application.

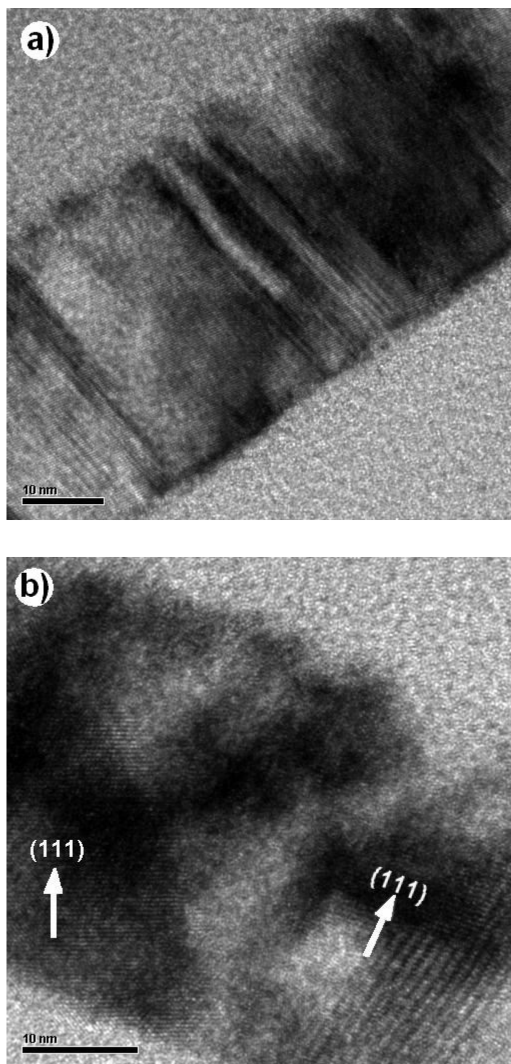

Fig. 3-6 HRTEM of LTPS films by SPC annealing at 600 °C. (a) 6 hours, (b) 24 hours

With a longer duration of SPC annealing, the grain sizes are enlarged. As shown in Fig. 3-6(b), no small-sized columnar grains exist. Instead, larger grains with sizes no less than 10 nm exist. Number of grain boundaries is

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diminished. Comparison between the two TEM images suggests that the larger grains are formed by the coalescent of the small columnar grains.

The electrical property of LTPS films is related to its microstructure. It is reasonable that the film resistivity varies with the crystallization progress. The sheet resistance in dark environment of LTPS films has been investigated. Fig. 3-7 shows the sheet resistance dependence on annealing time. The measurement was carried out using four point probe method, with a system combing Keithley 4200-SCS and Karl Suss PM8 probe station. In a general four point probe sheet resistance measurement, as long as distance from any of the four probes to the sample margin is larger than 4 times the spacing between the adjacent two probes, the sample can be considered as infinitely large and the following equation can be used to calculate the sheet resistance [59],

$$R_S = \left(\frac{\pi}{\ln 2}\right)\frac{V_M}{I_S}$$

where R_S is the sheet resistance, V_M is the voltage difference between the middle two probes, and I_S is the current through the outer two probes. In our measurement, this method is not very accurate due to the high resistivity of the undoped LTPS films. However, the measurement result gives an estimation of the resistance. From the resistance result, a transition stage is found on both annealing lines for 570 ºC and 590 ºC furnace temperature at 8-hour annealing position, as shown in Fig. 3-7.

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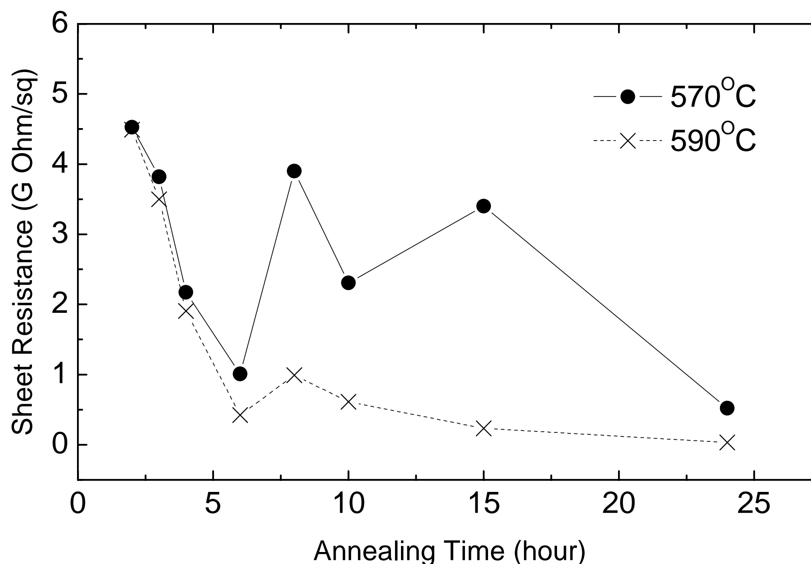

Fig. 3-7 Sheet resistance of LTPS films vs. SPC annealing time at 570 °C and 590 °C

In amorphous status, carriers move through a large quantity of potential barriers. But the barrier potentials are small in value. With the crystallite growth, the barriers inside grains are diminished greatly. The number of the overall barriers that carriers must pass in transportation is reduced and become less with the grain growth. The sheet resistance goes downwards as shown in Fig. 3-7. At the end of primary crystallization stage, most grains impinge each other. The texture at the grain boundaries is distorted and the interface will become more disordered. High potential barriers and carrier trapping centers occur at these interfaces, which impede the carrier transportation and lead to an increasing in resistivity. From the onset of secondary crystallization, some crystalline orientations with higher "priority" continuously increase in volume, consuming other less preferred orientations. Some grains with non-preferred orientations may diminish and even become distinguished, as leads to the decrease in quantity of the potential barriers. In addition, as described in last

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section, the interface regions become thinner and so are the potential barriers in terms of space distribution. The carrier tunneling possibilities also increase dramatically. These two factors favor the transportation of carriers and the sheet resistance goes downwards again.

This observation of resistivity variation is similar to that observed by R. Bisaro [52]. In his report, the phosphorus-doped a-Si experiences conductance variation during furnace annealing at temperatures between 510 and 650 °C. The conductance changes upward very slowly at first, then increases abruptly, and saturate at last. The first increase stage lasts for only 10 to 40 minutes, which is not visible in the experiment conducted in this report, as the shortest annealing time is 2 hours for the data shown in Fig. 3-7. The second conductance abrupt increase stage corresponds to the sharp decrease of the sheet resistance, indicating the ending of the primary crystallization progress. The following quasi-saturation stage of the conductance is in correspondence with gradually decreasing sheet resistance period, indicating the secondary crystallization process.

As the resistivity implies the poly-Si crystallization status, this method can be very valuable for monitoring the annealing process. There are several advantages using this method: (1) characterization can be conducted under air or vacuum condition, (2) no expensive and complex equipment needed, and (3) *in situ* measurement can be readily available by this method.

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3.1.6 Process optimization considerations

According to Scherrer's equation [60], X-ray diffraction (XRD) can be used to calculate grain sizes of polycrystalline materials. When the stress factor is omitted, the mean crystalline dimension, L_{hkl}, can be written as

$$L_{hkl} = \frac{0.89}{\beta_{hkl} \cos\theta}$$

where β_{hkl} is the full angular width at half maximum (FWHM) intensity of the reflection and θ is the Bragg diffraction angle. Fig. 3-8 shows the grain size calculated using Scherrer's equation, assuming the grain sizes of a-Si to be zero.

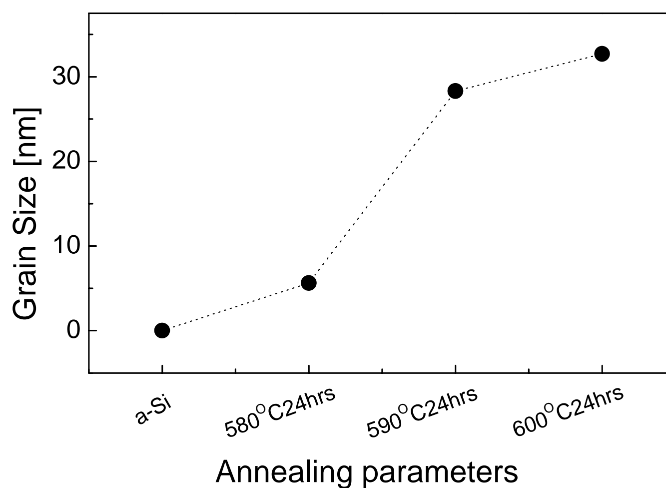

Fig. 3-8 SPC annealed poly-Si grain sizes derived using Scherrer's equation

It seems that higher temperature always favors the crystallization of poly-Si but a saturation-like behavior is observed. For the 24 hours annealing line, 590 °C exhibits much improvement than 580 °C. 600 °C sample also shows improvement than 590 °C but the change is much less. The conclusion is that

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the annealing temperature is limited in a small range limited by the glass softening temperature. Below the glassy temperature of the substrate, higher temperature is still favorable.

It has been widely accepted that longer annealing time is always favorable. But there are no decisive conclusions upon how long is the best, in terms of crystallinity and time consumed. As a conclusion, longer annealing time favors the LTPS film quality. Nevertheless, longer time means higher cost and lower prudctivity.

For 160 nm a-Si films on SiO_2 by LPCVD, 6 hours annealing reaches the transition states from primary crystallization stage to the secondary stage. To improve a-Si TFT properties with a reasonable cost, annealing time can be shortened to an optimized value. Crystallization can be optimized to conclude at the early period of the secondary crystallization. It takes a little more than 6 hours in the case discussed above. By around 6-hour annealing, crystalline structures are least distorted. Most of the film is occupied by grains except grain interfaces, which are very thin in term of space distribution. Carlos *et al* used 8 hours annealing in their device fabrication, and mobility up to 43 $cm^2/V\cdot s$ has been achieved [61]. However, to get even better quality of poly-Si film (larger grain sizes) the annealing time should be much longer because the secondary crystallization stage is slow process.

3.2 Thin film transistors using solid phase crystallized LTPS films

Though SPC needs high thermal budget and produce small grains in the film, it is still a promising technique in some applications where an order higher

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mobility than a-Si is required, due to its simplicity, low cost, higher degree of uniformity, and reproducibility as compared to other crystallization techniques. As has been reported, the active LTPS film thickness is found to affect the device performance to a limited extent [62].

3.2.1 Fabrication of thin film transistors

Fig. 3-9 shows the major fabrication steps with the corresponding cross-sections of a TFT. The devices were fabricated on Si wafers, considering the compatibility of Si wafers with the process facilities since the devices were fabricated in a CMOS line. The Si wafers were thermally oxidized to form 5000 Å SiO_2, which serves as the substrate for TFT fabrication, imitating the glass substrate. Then a-Si was deposited using LPCVD as described in section 3.1.1 with film thickness of 1600 and 900 Å, respectively (Fig. 3-9(a)). SPC was conducted using tube furnace at 600 °C for 72 hours, with N_2 passivation. After SPC process, the LTPS film formed was patterned by plasma etching (Fig. 3-9(b)). TEOS (Tetra-Ethyl-Ortho-Silicate) gate oxide of 700 Å was deposited at 600 °C, followed by the deposition of 2500 Å poly-Si at 600 °C, which served as the gate electrode (Fig. 3-9(c)). The gate poly-Si was densified by thermal annealing to minimize defects in the film and thus improve its electrical conductivity. Phosphorus doping was carried out in the mean time of densification with a target of 10~12 ohms/sq. of sheet resistance. The gate poly-Si was then patterned by plasma etching (Fig. 3-9(d)).

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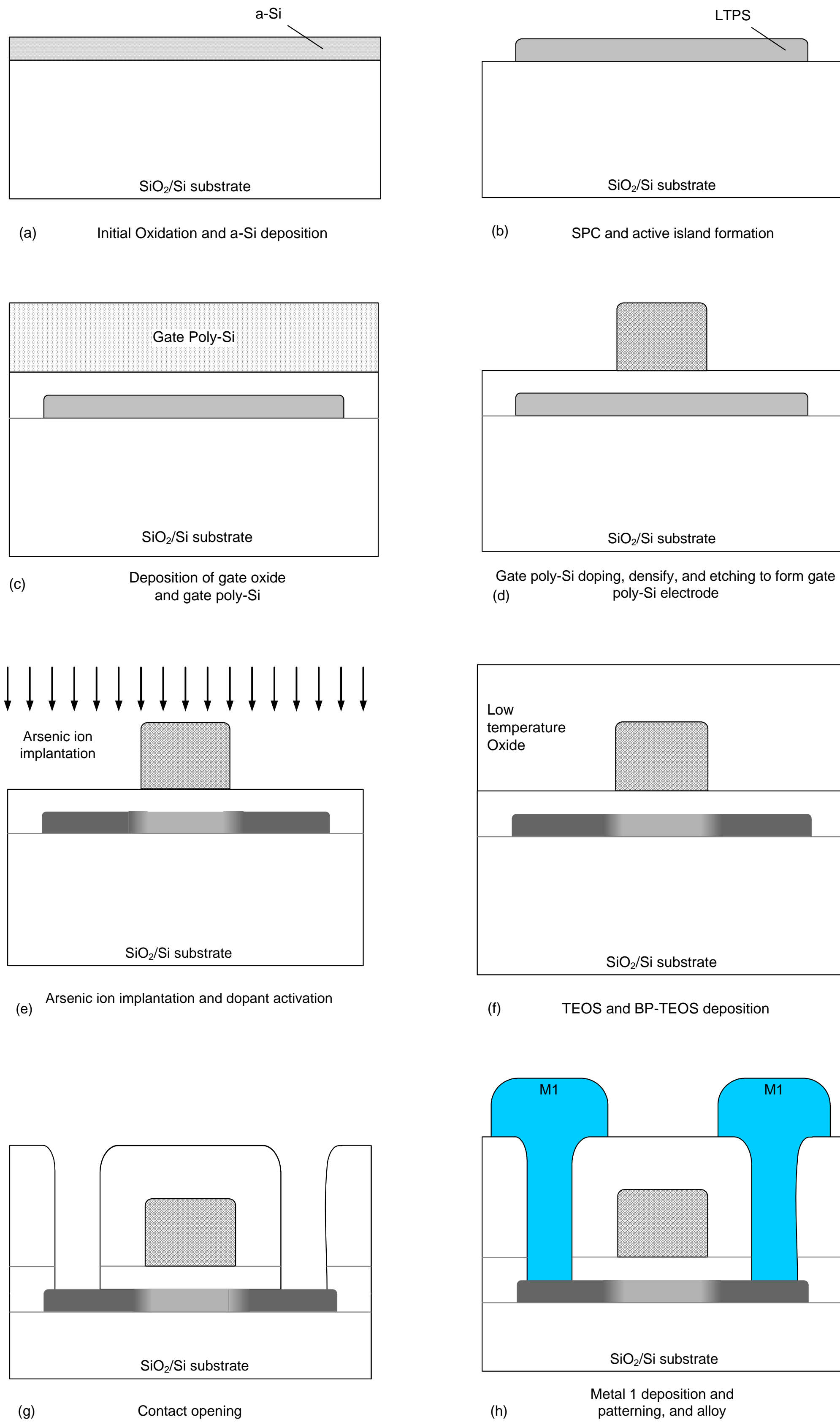

Fig. 3-9 Main process steps in SPC LTPS TFT fabrication

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Following the gate poly-Si etching was the self-aligned arsenic ion implantation to define the source/drain regions, with implantation dose of 5×10^{15} cm^{-2} (Fig. 3-9(e)). Dopant was activated by thermal annealing for 300 min, at 600 °C, with N_2 gas flow passivation. An insulating layer, boron phosphorus silicate glass (BPSG) was deposited at 600 °C (Fig. 3-9(f)). Contact hole was then opened using buffered oxide etch (BOE). For glass substrate, wet etching may affect the glass substrate (e.g. cause haze on the glass) and dry etching is thus preferred since it etches only one side of the substrate. Metal was deposited by sputtering and patterned to form connections (Fig. 3-9(g) and (h)). A more detailed process flow is shown in Appendix A.

3.2.2 Device characterization

3.2.2.1 Threshold voltage extraction

Devices fabricated are categorized into two groups with different LTPS film thickness: 160 nm and 90 nm. Fig. 3-10 shows their transfer characteristics, with V_D=0.1 V and 10 V respectively. Most device parameters, including threshold voltage V_{TH}, field-effect mobility μ_{FE}, ON/OFF current ratio I_{ON}/I_{OFF} are extracted from their transfer characteristics.

There exist a few methods to extract V_{TH} [63, 64], among which the most commonly used are linear extrapolation method and fixed current method. In extrapolation method, V_{TH} is defined as the V_G axis intercept (i.e. I_D=0) of the linear extrapolation of the I_D-V_G curve at its maximum slope, in the linear operating range of the device. However it is difficult to define the linear region of the I_D-V_G curve because it may deviate from ideal straight line due to the parasitic resistances [64]. The maximum slope in most cases can not be clearly

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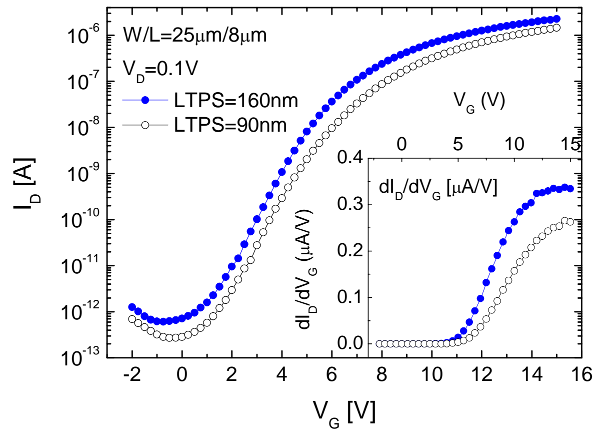
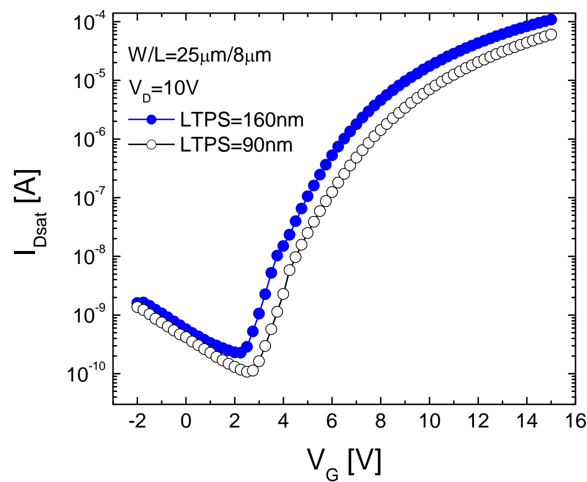


(a)



(b)

Fig. 3-10 Transfer characteristics of fabricated SPC LTPS TFTs

defined, as shown in the inset of Fig. 3-10(a). The extracted V_{TH} values may be different due to the arbitrary selection of the maximum slope point. Another extraction method is the constant-current method. In this method, a fixed drain current per unit W/L is chosen. V_{TH} is defined as the V_G value at which the chosen I_D value is reached, in the linear region (i.e. small V_D). Despite its simplicity, the V_{TH} value determined is totally dependent on the constant current which is arbitrarily chosen. However, reasonable values can be obtained if the value is chosen around the high bias end of the region where I_D ramps fastest. This region is constrained within a small gate voltage range, as can be seen

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clearly in the logarithmic scale of the transfer characteristic curve (e.g., the region is within 2 to 6 volts in Fig. 3-10(a)).

In this chapter, fixed current method is applied. The value 10^{-8} A per unit W/L with V_D biased at 0.1V is chosen, which is located at the high gate bias end of the region with highest current ramp rate (large sub-threshold swing region). The mobility is extracted by selecting the maximum when V_D=0.1V and V_G ranges between 10 to 15V.

Table 3-2 Characteristics of SPC LTPS TFTs

Device \ Parameter	V_T (V)	μ_{FE} (cm^2/v·s)	*Kink* (V/dec)	S_S (V/dec)	I_{ON}/I_{OFF}	
					V_{DS}=0.1V	V_{DS}=10V
LTPS thickness =160nm	4.48	21.86	31.9 (V_{GS}=15V)	0.86	4.76×10^5	3.7×10^6
LTPS thickness =90 nm	5.22	16.60	42.6 (V_{GS}=15V)	0.83	5.56×10^5	5.3×10^6
Ref. [55]*	20.5	17.5	-	3.0	1.1×10^6	1×10^6 **

* LTPS=100 nm

** Estimated from the plot in the reference.

It has been reported that high performance LTPS TFTs can be obtained using very thin active layer (<30nm) by SPC [65] or MILC method [62]. The active layer for SPC devices presented here is not ultra-thin film. The device performance with 90 nm active layer does not exhibit much improvement compared with that of devices with 160 nm thick active layer. However, there is still difference between the device parameters. As listed in Table 3-2, the V_T values extracted are 4.48 and 5.22V from Fig. 3-10(a), for LTPS film thickness of 160nm and 90nm respectively. The threshold values are much higher than

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crystalline MOSFETs and comparable to that of a-Si and microcrystalline Si TFTs [66].

3.2.2.2 Other device parameters

Field effect mobility is derived from the I_D-V_G curve in the linear region, with small drain bias (much smaller than V_G). The *I-V* relation is expressed as

$$I_D = \frac{W}{L}\mu_{eff} C_I (V_G - V_T) V_D \tag{3-1}$$

From this equation,

$$\mu_{FE} = \frac{I_D L}{W C_I V_D (V_G - V_T)}. \tag{3-2}$$

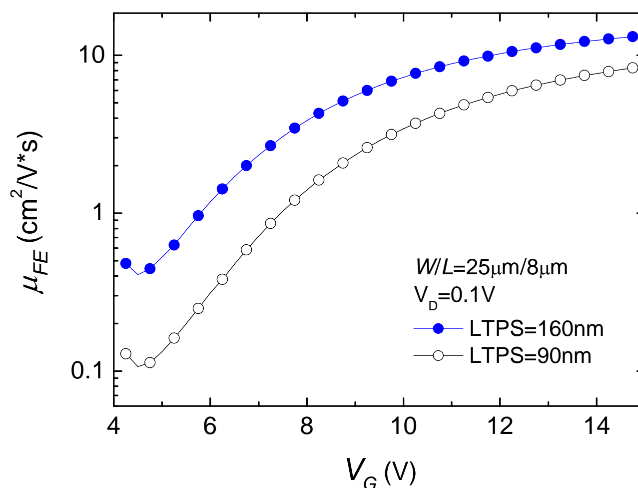

Fig. 3-11In linear region, field effect mobility is a function of V_G. The maximum value in the measured range is extracted as the device mobility.

As shown in Fig. 3-11, μ_{FE} is a function of V_G in linear region. In this thesis, the maximum value is extracted as the device mobility, corresponding to the bias of V_{GS}=14V.

μ_{FE} values extracted are 12.2 and 7.8 cm^2/V·s for TFTs with LTPS film thickness of 160 and 90 nm respectively. The mobility is about one order higher

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than that of a-Si TFTs, which is the key property by which SPC TFTs will find their applications.

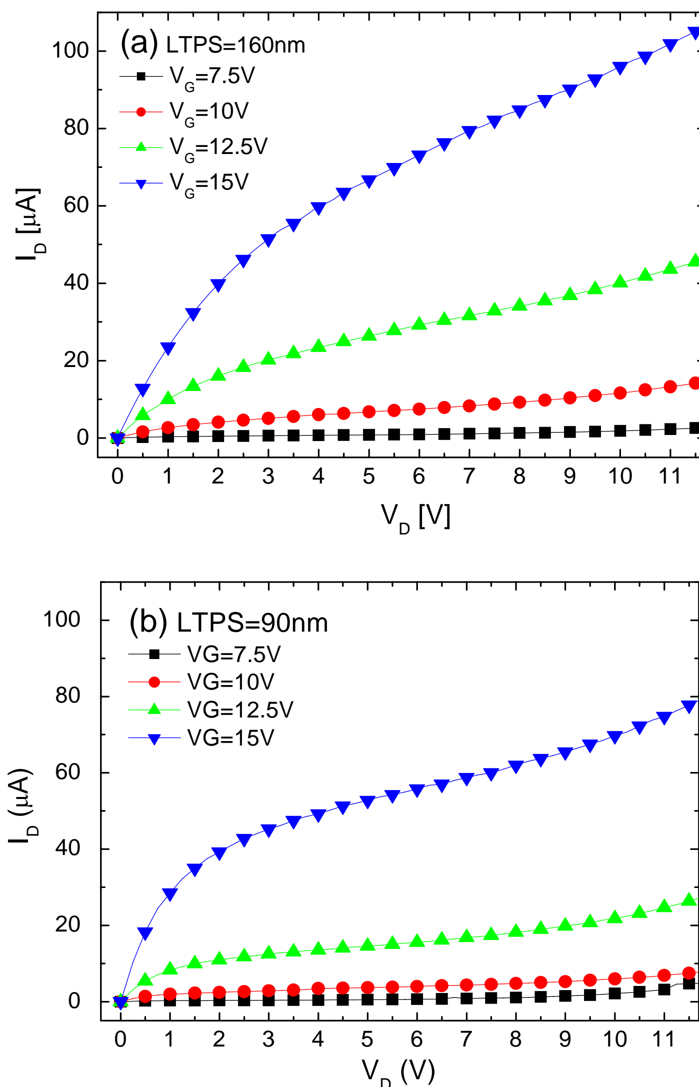

Fig. 3-12 Output characteristics of fabricated SPC LTPS TFTs.
(a) LTPS=160nm; (b) LPTS=90nm

Subthreshold swing S_S indicates the sharpness of the transition from off- to on-state. It is defined as the inversion of the slope of I_D-V_G curve before threshold voltage:

$$S_S = \left(\frac{d \log_{10} I_D}{dV_G} \right)^{-1} \tag{3-3}$$

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The S_S values of the SPC TFTs are around 0.8V/decade. This value is similar to that of the TFTs from ELA LTPS films (e.g. between 0.675~1.316 V/dec in [67]), proving that good turn-on characteristics are obtained from the SPC TFTs.

The ON/OFF current ratio is in the order of 10^5 to 10^6, similar to a common a-Si TFT. The ON/OFF ratio for device with 90 nm LTPS film is 5.56×10^5, which is a little higher than 4.74×10^5, the correspondence of the device with 160 nm active layer.

Kink effect is a parasitic effect caused by carrier generation and effective channel length modulation by the drain bias. Though it is not a severe issue in digital TFT circuits, it must be carefully taken into consideration if the device is used in analog modules [68, 69]. Kink effect is clearly observed in the output characteristics shown in Fig. 3-12. In this thesis, the kink effect can be quantitively represented by the slope of the linear approximation of the saturation region of the I_D-V_D curve. The kink effect of the SPC TFTs are 31.9 and 42.6 V/dec at V_G=15V, for LTPS film thickness of 160 and 90 nm respectively. Thinner active layer thickness is proved to have better kink effect immunity.

3.3 Summary

SPC annealing of a-Si is systemically studied. Temperature and time dependence is investigated using Raman spectroscopy, AFM, TEM, and poly-Si film sheet resistance measurement. Low temperature limit at 560 ºC was for the first time defined for practical SPC processes.

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Ex situ measurement is for the first time conducted to investigate film sheet resistance variation versus annealing duration. The result suggests a transition between annealing stages defined in this chapter as primary and secondary crystallization, which correspond to before and after the coalence of most crystallites. Process optimization of SPC process is also discussed. Crystallization time that proceeds to the early period of the secondary crystallization stage is suggested as the optimized value for practical SPC process, in terms of crystallization effect, cost and productivity.

TFTs by SPC LTPS films are fabricated and characterized. Reasonably good performance is obtained, especially the high μ_{FE} value and low S_S. Device characteristics have a weak dependence on the thickness of the active LTPS film.

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Chapter 4 NICKEL INDUCED LATERAL CRSYALLIZATION AND FIELD AIDED LATERAL CRYSTALLIZATION

4.1 Introduction

As a conventional thermal annealing method for a-Si crystallization, SPC has some disadvantages which have led to the decline of interest in it for LTPS device fabrication. The drawbacks are the inferior quality of the crystallized poly-Si films and the high thermal budget of SPC processes. SPC crystallized poly-Si has smaller grains with a variety of intra-granular defects, mainly dislocations and stacking faults. The high thermal budget means a large product of annealing temperature and annealing time. The annealing temperature of SPC LTPS process is found to be no lower than 560 °C, as illustrated in Fig. 3-4. And SPC process generally lasts ten to a few tens of hours.

MIC/MILC was later proposed for the crystallization of a-Si at low temperatures. MIC/MILC can produce poly-Si TFTs which have better electrical characteristics than poly-Si TFTs fabricated by SPC [70]. It was reported that the activation energy of the a-Si could be decreased by more than 50% with the presence of nickel (Ni) [71]. So effective MIC/MILC crystallization processes can be conducted at lower temperatures, with much shorter annealing duration than SPC [72].

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A few metals have been proposed to enhance the crystallization effects, including Ni, copper, cobalt, aluminum, and palladium, etc. [73], among which Ni has received special attention and become the metal of choice. Ni disilicide ($NiSi_2$) formation in annealing process is the key for crystallization [74]. The disilicide has the cubic structure and a very close lattice parameter to crystalline silicon (mismatch is less than 0.4%). The disilicide is actually the species that mediate the transformation of a-Si to c-Si [13].

Metal contamination is one problem that degrades device performance fabricated by metal mediated crystallization. In Ni induced MIC process, a thin film of Ni is directly formed on the a-Si film. In the consequent annealing, Ni silicide forms under Ni and crystallization occurs where the silicide is formed. In Ni mediated MILC process, Ni is deposited on a selected region and the crystallization proceeds along with the lateral diffusion of the formed Ni silicide. As a result, the MILC method leaves less metal in the active film. The contamination problem is alleviated. Besides, because the growth proceeds along with the silicide diffusion, the growth is somewhat in a continuous mode and larger grains can be formed [70, 101].

Electrical field has been found to favor a fast MILC process [75]. It has also been applied in MILC process. This electrical field enhanced MILC, or FALC, proceeds much faster than MILC process, which renders high productivity and cost reduction in manufacturing.

In this chapter, the crystallization process of MILC and FALC is studied. *In situ* resistance measurement method is applied in the study of MILC and FALC processes.

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4.2 Experiment details

Two types of crystallization processes, namely MILC and FALC, have been conducted, using the same substrate and a-Si films. Thermally grown SiO_2 of 500 nm on silicon was selected as the substrate, on which an a-Si film was deposited using LPCVD by pyrolysis of undiluted silane at 550 ºC. Then 10 nm Ni was electron-beam evaporated and patterned with a shadow mask into stripes with spacing of 1 mm. In MILC process, the samples were annealed at 500 °C, in 0.04 Torr argon gas environment for 5 hours. In the FALC experiment, the specimen was clamped on to an insulating boron nitride holder with two carbon electrodes, each in contact with the one of the two Ni strips. Besides the heat treatment as in MILC, a direct-current voltage was also applied between the carbon electrodes, which built up a strong electric field (up to a few hundreds voltages per centimeter) between the two nickel pads. The current in the circuit loop was monitored and recorded during the annealing process.

Annealed samples were investigated by optical microscopy, AFM, scanning electron microscopy (SEM), and Raman spectroscopy. Secco etching, a method to reveal grain boundaries of poly-Si films, was used to investigate the crystallization effect on the a-Si processed by MILC with and without electric field. Secco etchant ($K_2Cr_2O_7$:H_2O:HF = 2g:100ml:200ml) is a solution which reveals grain boundaries of poly-Si [76].

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4.3 Investigation on the crystallization behavior

4.3.1 Metal induced lateral crystallization

As shown in Fig. 4-1, the crystallized film can be divided into two parts: the MIC region (Ni covered region) and the MILC region (Ni laterally diffused region). In field aided lateral crystallization, the Ni diffused MILC region is called FALC region. Beyond the MILC region is the a-Si film, not crystallized due to lack of Ni catalyst. And in between the a-Si and the MILC region is the MILC front.

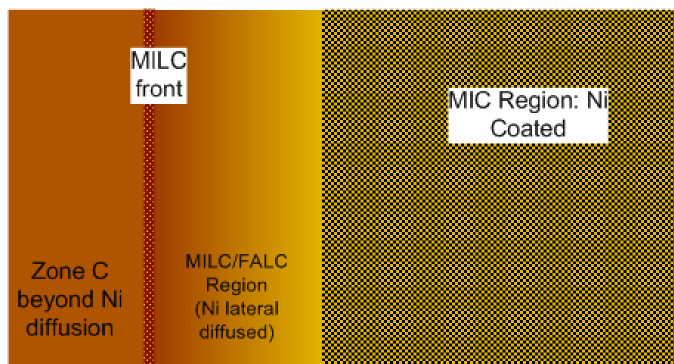

Fig. 4-1 Definition of MILC regions

The MIC region consists of small, randomly oriented grains and high density of grain boundaries, as shown in Fig. 4-2(a). The average grain sizes are estimated to be no more than 100 nm, which is comparable with the thickness of SPC LTPS films. For devices with same dimensions, smaller grains will introduce more grain boundaries in the device channel, which are well known to degrade the device performance in terms of both on-state current and off-state leakage current, by trapping free carriers, forming potential barriers, and

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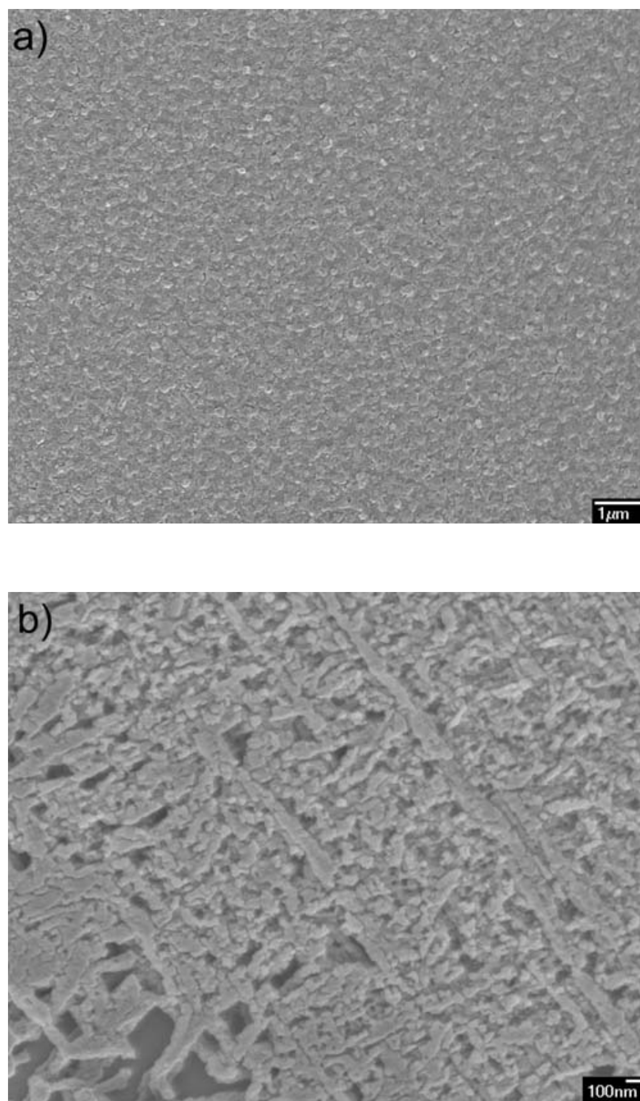

Fig. 4-2 SEM images of MILC LTPS film (90nm) after Secco etching. (a) Nickel covered region, (b) MILC region, near lateral crystallization front

assisting tunneling or emission of carriers [77 - 79]. It was also observed that there exists a large quantity of Ni silicide clusters in the film, as indicated by the etching pits among the small grains. The silicide clusters are detrimental to TFT performance, because the silicide conductivity is much higher than the LTPS film and its conductivity is not modulated by the gate voltage. This will increase the off-state leakage current and degrade the sub-threshold characteristics. Comparing to the randomly oriented small grains in MIC region,

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the MILC regions consist of larger and more ordered longitudinal grains up to a few microns in length, as shown in Fig. 4-2(b). There are still some etching pits (attacked by Secco etchant) distributed over the film, suggesting the aggregation of silicide and the existence of a-Si.

Fig. 4-3 shows the AFM image of a crystallization front in MILC region. Dendritic lateral growth behavior is observed. Ni diffusion front in MILC sample consists of a lot of needle-like crystallites, which are 80 to 300 nm in width and 100nm to a few microns in length. The observation about needle-like crystallites is similar to reported investigation, using TEM [75, 80, 81]. However, it can be seen from Fig. 4-3 that a large grain in MILC front is actually a mosaic of needle-like subgrains, whose orientations in some cases may deviate a bit from each other, as indicated by the arrows in the AFM image. Since the lattice orientation deviates, stacking faults and dislocations exist between the subgrains, which will degrade the field-effect property of LTPS films. This is probably one important reason why passivation techniques such as thermal treatment at higher temperature, or H_2/NH_3 plasma treatment, are useful to improve the film in terms of field effect characteristics.

The dendritic growth of crystallites has been reported previously [80, 82]. R. C. Cammarata suggested that $NiSi_2$ is the silicide phase that has the lowest surface energy with a-Si, and it is the only phase of Ni silicide formed by annealing if Ni is within, instead of at the surface of, the a-Si film [82]. $NiSi_2$ precipitate has octahedron structure, with minor lattice mismatch about 0.4% with crystalline silicon (c-Si) [80]. Illustrated in Fig. 4-4 are a few such randomly oriented octahedron $NiSi_2$ precipitates, which have the potential to

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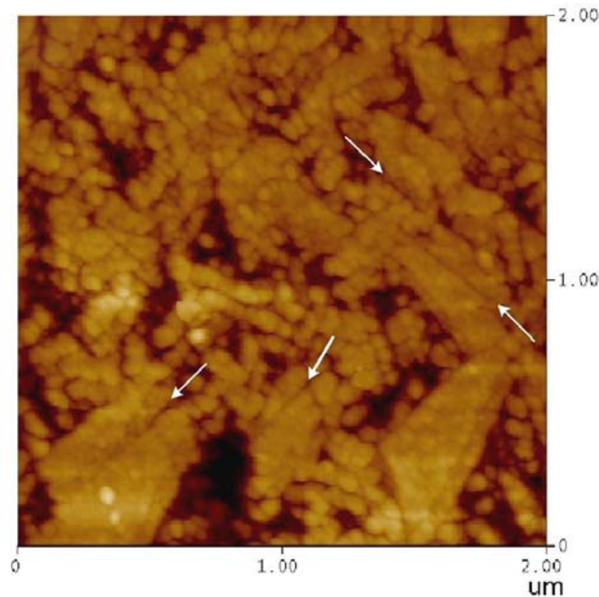

Fig. 4-3 AFM image of Ni MILC front (Secco etched) showing the dendritic lateral crystallization behavior and mosaic structures of subgrains. The arrows indicate the boundaries between subgrains.

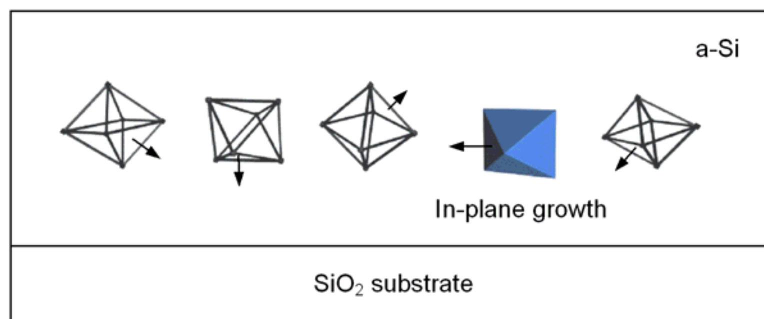

Fig. 4-4 Schematic of Ni silicide mediated lateral crystallization of a-Si. The plane-filled precipitate illustrates one that initiates in-plan lateral growth

initiate the polycrystalline silicon growth. The lateral crystallization originates from the epitaxial growth from one of the (111) facets of the $NiSi_2$ silicide precipitates. The chemical potential difference of Ni silicide between the $NiSi_2$/c-Si and $NiSi_2$/a-Si interface drives the silicide lateral diffusion and lateral crystallization of a-Si [74, 80]. So it is reasonable to conclude that the

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MILC process initiates from Ni diffusion into a-Si. This diffusion is a quick process because a-Si film is thin. Then $NiSi_2$ mediates the lateral crystallization. For the silicide precipitate with no (111) facets normal to film surface, the epitaxial growth still occurs but the process soon stops when the foregoing $NiSi_2$ reaches the film surface or film-substrate interface. So the crystallites formed from this kind of non-in-plane growth are small in size and they are not capable of producing large grains. Only the silicide precipitate with at least one of its (111) facets normal to the a-Si film (the darkened one in Fig. 4-4), can lead to in-plane growth with long crystallization path, because the film surface or the a-Si/SiO_2 interface does not confine their expansion. Based on the one-dimensional nature of the crystallite growth, we believe that the in-plane growth will scarcely stop until some stopping mechanism appears. The mechanisms could be: (1) the a-Si on the path of crystallization has been consumed by other nucleation processes; (2) The crystallite impinges other crystallites or nuclei ahead of its way. In the latter case, the crystallite growth does not necessarily terminate, since the diffusion mechanism still applies. It can deviate and initiate growth towards a different direction. The latter case can be regarded as a scattering event. The combination of growth and scattering of the crystallite results in zigzag way in-plane growth and leads to the dendritic structure.

Mitsutoshi's *in situ* TEM investigation explains the two-dimensional grain formation from this one-dimensional growth [83]. According to his observation, the growth direction of the needle-like crystallites frequently changes towards one of the possible <111> crystallographic directions, which is often opposite to the original advancing direction of the crystallite. It is this back-and-forth one-dimensional crystalline growth that result in large, two-dimensional grains.

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Since the $NiSi_2$ precipitates are randomly oriented, the probability of a precipitate's having (111) facet normal to a-Si film surface is small, only a small amount of crystallites which induce in-plane growth can laterally grow out of the Ni covered MIC area. As a result, the crystallite concentration in MILC region is much lower than that in MIC region. A lower probability of scattering to in-plane growth is expected. Grains much larger than those in MIC area can thus be created, which is in agreement with previous reports [80, 83, 84].

4.3.2 Field aided lateral crystallization

Electric field has been proved to be in a few ways beneficial to Ni mediated crystallization process of a-Si films. The crystallization rate was reported to be dramatically increased in both field aided MIC processes [35, 75, 80, 83] and MILC processes, at similar or even lower temperatures [42, 85]. The crystallization effects are also improved in terms of grain sizes and lateral crystallization lengths [35, 80].

In FALC region, dendritic crystallite growth is also observed, with better crystallinity, as is verified by the characterization of the film using Raman spectra and SEM (shown in next chapter, Fig. 5-10 and Fig. 5-11). The process parameters for the FALC samples are the same as the MILC samples except for the electric field, as described in section 4.2. The only difference in annealing process from MILC is the electric field employed in FALC, which should be responsible for better crystallinity. As discussed in the MILC part, in-plane growth results in larger grains. Whereas the not-in-plane growth soon reaches the film surface or a-Si/substrate interface and the progress terminates, leading

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to grain dimensions comparable to or less than the film thickness. Besides this in-plane growth mechanism, the crystallites grown in FALC region form even larger grains than those in MILC process, due to the additional effects from electric field, as discussed in the following.

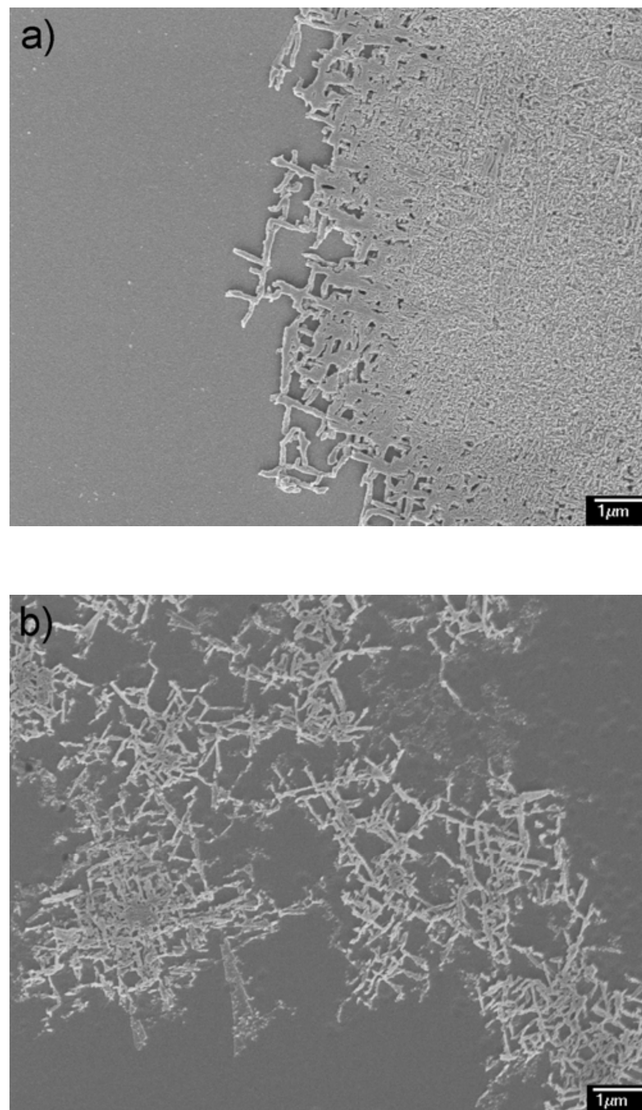

Fig. 4-5 SEM images of LTPS films after Secco etching. (a) MILC front, (b) FALC front. The film is processed at 500 ºC for 5 hours, under no electric field (MILC sample) or 600 V/cm electric field (FALC sample). A clear FALC front can not be precisely defined due to the sparse distribution of the crystallites.

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Firstly, the Ni lateral diffusion coefficient and the lateral crystallization rate, are accelerated by the electric field. J. Jang *et al.* ascribed the increased diffusion coefficient of Ni silicide under electric field to the negative Mulliken charge of Ni in a silicon network [78, 83]. Fig. 4-5 compares the crystallization fronts of MILC and FALC processes. Fig. 4-5(a) shows a clear boundary between a-Si and MILC LTPS region. While for the FALC sample, as shown in Fig. 4-5(b), the crystallites at the diffusion front are sparsely distributed. A clear FALC front can not be well defined in this case. According to above discussion on scattering mechanism, the sparse distribution of the crystallites further lowers the probability for a growing crystallite to be scattered, which favors the formation of grains larger than those in MILC. Secondly, besides increasing the Ni diffusion coefficient, electric field can also enhance the grain sizes by selecting the crystallization direction. The crystallite growth in direction parallel to the electric field is accelerated. The growth in direction not in parallel to electric field may be guided to be along the electric field, because of the force applied on the negatively charged Ni element. Due to this direction guiding mechanism, there are less scattering events along the lateral crystallization direction, which favors the large grain formation.

Based on the reported explanation that the enhancement effect of electric field is caused by the negative Mulliken charge of Ni [75], polarity dependence is expected, as was verified by our investigation as follows.

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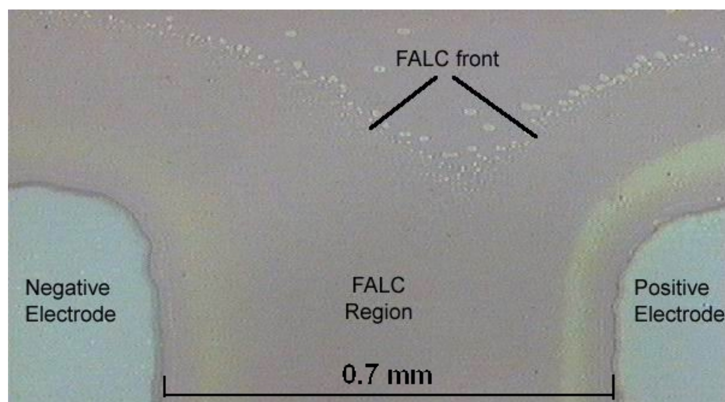

Fig. 4-6 Optical micrograph of the nickel diffused region between two nickel pads, showing the electric field enhancement of nickel induced lateral crystallization with the FALC front indicated. The film is processed by FALC at 500 ºC for 5 hours, under 600 V/cm electric field. No Secco etching is applied.

Fig. 4-6 shows the optical micrograph of FALC annealed sample (FALC, 500 ºC under 600 V/cm for 5 hours) with no Secco etching applied. Different FALC lengths are observed at the two electrodes. The width of FALC region at the negative electrode side is found to be 3 times larger than that at the positive side. However, the difference is much less than many other FALC reports (e.g., The lateral crystallization rate at 60 V/cm, 500 °C, has been reported to be 20 times higher than that at 0 V/cm [85].). We ascribe this to the Joule heating effect caused by the large current density in the film, which is up to 810 A/cm^2 during the annealing process. The Joule heating effects accelerate MILC rate of both polarities with no preference at either the positive electrode or the negative electrode. The difference of electric field enhancement effects between the two electrodes is thus diminished. We have also observed a comparable polarity difference of 6 times between the FALC lengths at the negative and positive

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electrodes, respectively. This larger difference was observed from FALC processed 160 nm thick LTPS sample at 500 ºC, 200 V/cm, for 5 hours. The difference (3 times versus 6 times) results from the current density difference. The maximum current density in the latter sample (in which 6 times polarity difference is observed) is 468 A/cm^2, which is close to a half of the value (810 A/cm^2) in the previous sample. The higher current density in the sample as shown in Fig. 4-6 results in stronger Joule heating effects and the polarity dependence is less prominent. This observation further proves the explanation.

4.4 Application of *in situ* resistance measurement in crystallization process study

During FALC or conventional MILC processes, a portion of the a-Si film outside the Ni source is gradually converted to poly-Si. And the portion of the converted LTPS film grows with time. As the resistivity of a-Si and poly-Si is much different, it is expected that the film resistance varies with the annealing time in the process of post-deposition annealing of a-Si. It is especially so in a MILC or FALC process, where the catalyst diffuses from the metal catalyst rich region to the pure a-Si and the crystalline front proceeds with the diffusion of the metal catalyst. The resistance in between two catalyst source regions in FALC will decrease gradually with the forward movement of the metal diffusion fronts as more and more a-Si is transformed into poly-Si. This phenomenon can be directly utilized for *in situ* monitoring of the annealing process. *in situ* resistance has previously been reported in studying the growth dynamics of indium tin oxide [86].

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In this section, we shall present the study on Ni induced lateral crystallization of a-Si where *in situ* resistance measurement is carried out for both MILC and FALC processes. The results show that this kind of *in situ* resistance measurement can be readily applied to study the annealing mechanism. *In situ* resistance measurement is less expensive and much easier to conduct to *in situ* monitor the crystallization process during the crystallization process, comparing to other characterization methods such as XRD, Raman spectroscopy, SEM and transmission electron microscopy (TEM).

4.4.1 Experimental details

160 nm thick a-Si film was deposited by LPCVD on SiO_2 formed by thermal oxidation on Si substrate. 60 Å Ni was then e-beam evaporated on the a-Si film and patterned to strips with a shadow mask. This thickness of Ni is different from that in section 4.2, which is 10 nm. However no special consideration has been given to the thickness of Ni. The length and spacing between two Ni strips were 10 mm and 0.7 mm, respectively. The annealing was carried out at temperatures between 500 °C and 600 °C in a tube furnace, which was kept at 50 mTorr by a mechanical pump and a constant flow of argon of 5 sccm. Resistance measurement was conducted between one pair of Ni strips during the annealing process. The Ni strips served as diffusion sources for MILC process as well as electrodes for resistance measurement.

Under room temperature, the undoped a-Si and poly-Si films are highly resistive and their resistance measurement needs specially prepared equipment. Fortunately, this poses no problem for the *in situ* measurement of MILC and FALC, as the resistivity of a-Si and poly-Si drops at the annealing temperatures

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to a level that can be precisely measured with common equipment. In our experiment, KEITHLY2000 multimeter, KEITHLEY220 programmable current source, and a common DC power supply were utilized.

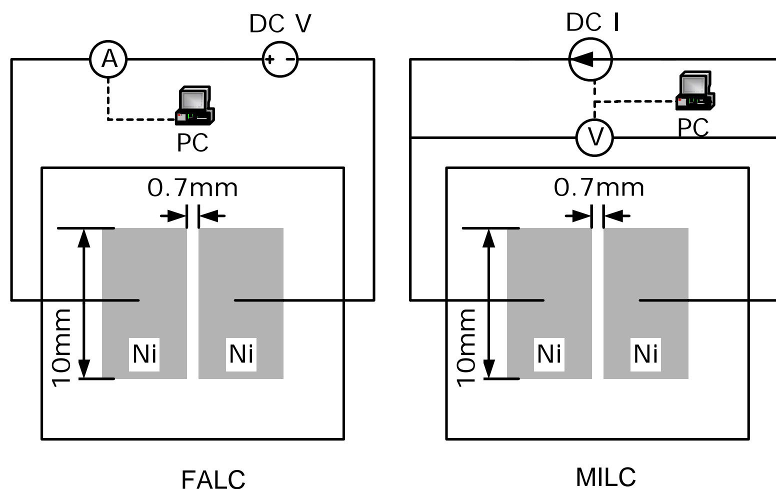

Fig. 4-7 Schematic of the *in situ* resistance measurement set-up

For FALC, a constant DC voltage of 7 V was applied between the electrodes, which built an electric field of 100 V/cm in between the Ni strips. For MILC, a small constant current (10 μA) was maintained in order to minimize the field enhancement effect. The maximum voltage applied in the MILC process was limited to less than 2 V to alleviate the field effect. Fig. 4-7 shows the schematic of measurement set-up.

4.4.2 Measurement results and analysis

4.4.2.1 Exponential decay of resistance

At the annealing temperatures, electron transportation is thermionic dominated [87]. Boltzmann distribution applies for the carriers that participate in the transportation. The grain boundary barrier is the main factor that impedes the carrier transport. Because Boltzmann distribution is exponentially

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dependent on the negative of carrier energy, the carrier density that can surpass the barrier, and the probability of an electron overcomes it, is exponentially dependent on the negative of the barrier height. Assuming a barrier height U, the probability of an electron surpassing n such barriers is proportional to $[\exp(-U/kT)]^n = \exp(-nU/kT)$, where k and T are Boltzmann constant and sample temperature in Kelvin, respectively. So the current density will be exponentially dependent on the negative of the product of average barrier height and the number of barriers. The product varies with the nucleation and grain growth during the crystallization process and thus the resistance variation is related to the crystallization process.

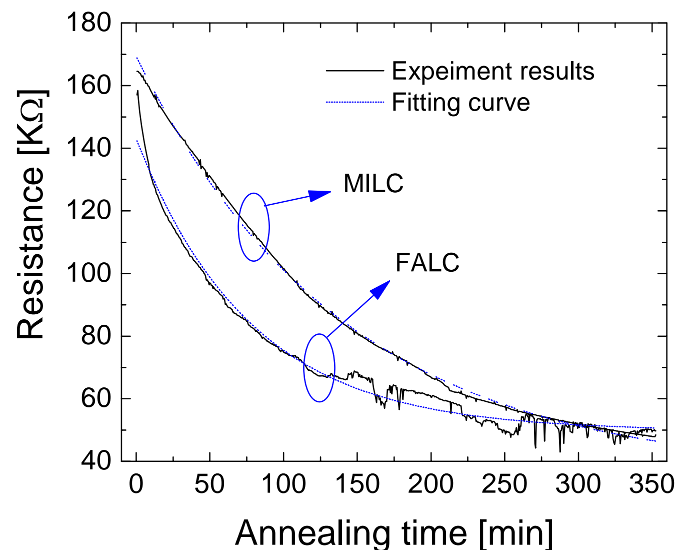

Fig. 4-8 *In situ* resistance versus annealing time for MILC and FALC processed a-Si film at 500 °C. The electric field for FALC is 100 V/cm.

Fig. 4-6 shows the in situ resistance measurement result for both MILC and FALC process at a fixed temperature of 500 °C. The dependence of the

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electrical resistance R, between two measuring electrodes, on annealing time, t, can be well fitted with an exponential decay approximation:

$$R = R_0 - A\left[1 - \exp\left(-\frac{t}{t_c}\right)\right] \quad \textbf{(4-1)}$$

where R_0 is a constant determined by the a-Si film property before annealing, A and t_c are process dependent constants. t_c denotes the decay time constant. In Fig. 4-8, the fitting parameters are: for MILC fitting, R_0=169.3KΩ, A=133.6KΩ, t_c=140min; for FALC, R_0=143.1KΩ, A=93.4KΩ, t_c=77.7min.

At the annealing temperature of 500 °C, silicide sites are necessary for crystallization to proceed. In the case of pure a-Si, i.e., in pure SPC process, this temperature is too low to observe obvious crystallization effects, as shown in Fig. 3-4. Ignoring the SPC effect of a-Si, the decay of resistance with time (Eq. 4-1) is related to the diffusion of Ni, i.e., related to how much a-Si has been converted to poly-Si. It has been reported that the MILC rate decreases with annealing time [88]. Thus, assume that the average lateral crystallization rate of Ni in MILC, regardless of the electrode polarity, is exponentially dependent on annealing time t, the resistance terms R_0 and A in eq. 4-1 can be precisely expressed by

$$R_0 = \rho_a L \quad \textbf{(4-2)}$$

$$A = (\rho_a - \rho_P)v_0 t_c \quad \textbf{(4-3)}$$

where v_0 is the initial lateral crystallization rate at the beginning of annealing, L is the spacing between two Ni electrodes, ρ_a and ρ_P are the resistance per unit

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length in the diffusion direction of the a-Si and poly-Si films, respectively. For the fitting in, v_o=0.16µm/min and 2.37µm/min are deduced. The physical meaning of Eqs. 4-2 and 4-3 is clear. R_0 represents the resistance before crystallization, A represents the change of resistance at $t=\infty$. Here an exponential relationship between lateral crystallization speed and annealing time is assumed, which fits the data well. There exists a maximum diffusion length based on this assumption, which equals to $v_0 t_c$. From the fitting in Fig. 4-8, the maximum diffusion lengths are 22.4 µm and 184 µm for MILC and FALC respectively. The assumption of diffusion speed on time may not be accurate. However, it can at least provide a first-order approximation of the experimental results. And in practice, a maximum diffusion length should exist for a Ni source limited process.

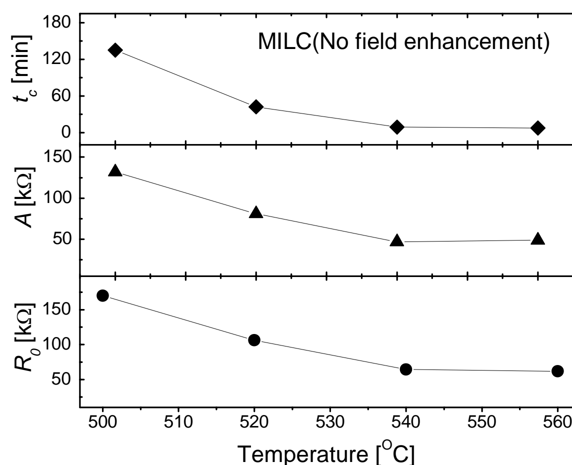

Fig. 4-9 Dependence of resistance fitting parameters, t_c, A, and R_0, on the annealing temperature for MILC processed a-Si film.

The MILC process is strongly temperature dependent. Fig. 4-9 shows the temperature dependence of three fitting parameters, A, t_c, and R_0 in Eq. 4-1 for MILC process. The strong temperature dependence of A and R_0 is

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understandable from eqs. 4-2 and 4-3: ρ_a and ρ_P and v_0 are all functions of temperatures. ρ_b decreases with higher temperatures. ρ_a also decreases as temperature increases, with the same trend as R_0 shown in Fig. 4-9, since R_0=L, where L is a constant. When annealing temperature is not high (so that SPC effect is weak) as in the case of MILC, v_0 is reported to be exponentially dependent on temperature [89]. t_c decrease with the increase of temperature, indicates a faster MILC process (Eq. 4-1).

4.4.2.2 Field enhancement factor

From the above discussion on $v_0 t_c$, it is reasonable to use the ratio of $v_0 t_c$ of FALC and MILC to examine the field enhancement effect. Thus we define the $v_0 t_c$ ratio of FALC to MILC as the field enhancement factor.

In our experiment, the factor is about 8.2 from the curve fitting results in Fig. 4-2. However, the electric field accelerates the MIC process by more than one hundred times [75]. The field enhancement factor in our FALC process is a bit smaller than that for MIC process reported. This disparity is probably due to the nature of *in situ* measurement itself. As long as resistance measurement is conducted, field is inevitably applied on the MILC film. Although the field was kept to be low (less than 24 V/cm) for MILC in our experiment, the field enhancement was clearly present.

In order to explain the field enhancement effect, silicide diffusion behavior needs to be investigated. There are two driving forces for silicide diffusion: (1) the chemical potential and (2) the electrical field. The chemical potential of Ni silicide at the a-Si/$NiSi_2$ interface is lower than that at the poly-Si/$NiSi_2$ interface [74]. This chemical potential difference was reported to be the primary

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driving force for the lateral diffusion of silicide [74]. Electrical field is another driving force. The crystallite growth rate has been reported to approximately increase with field strength linearly [90]. Between the two factors driving the lateral diffusion of Ni silicide, the latter one dominates when the electrical field is extremely strong. For an example, when a strong field of 1000 V/cm was applied with a similar configuration except that the a-Si thickness is 90 nm instead of 160 nm, the whole area (with 700 μm in width) between Ni electrodes was Ni diffused after 4 hours annealing at 500 ºC. In this case, the crystallization rate cannot catch up the Ni diffusion speed, leading to higher Ni concentration and more nucleation sites in un-crystallized a-Si films. This kind of annealing acceleration will induce the crystallized film containing more randomly oriented, smaller grains, which are not desired. Though exponential resistance decay behavior was also observed for this extreme case, eq. 4-3 is not applicable. The product $v_0 t_C$ will not be the limit of lateral crystallization because the Ni diffuses longer than this value.

4.4.2.3 Chaotic fluctuation at FALC low resistance stage

Chaotic fluctuation of the resistance for FALC at its later annealing stage is observed. This is probably caused by the diffusion of Ni silicide. During the annealing process, the $NiSi_2$ clusters that can form at 500 °C diffuse with a high concentration front, leaving behind crystalline silicon with low concentration of silicide [37]. Large grains can form along the silicide diffusion paths owing to less nucleation sites [81]. Some silicide nodules may diffuse forward much faster due to the influence of the electrical field. Impinging of a migrating silicide precipitate on an existing one in the a-Si will frequently lead to the growth of additional needles on variants of the <111> direction [74, 83]. The

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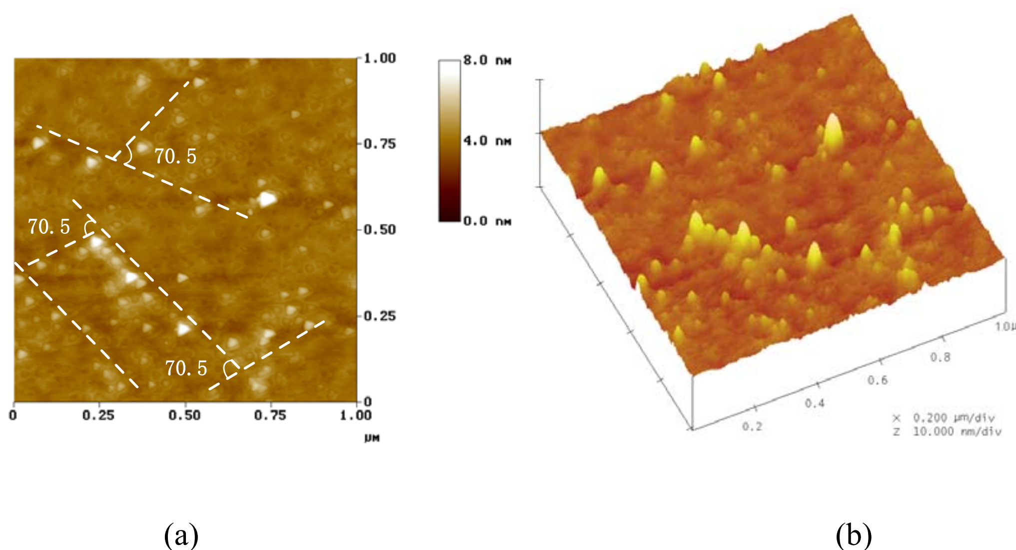
precipitate migrating direction may divert if this occurs, which can lead to the zigzag-way of diffusion, as shown in Fig. 4-10. It is consistent with the observation in reference [75]. The most forward diffused silicide clusters form some conducting paths with anisotropic conductivity [87]. The resistivity in the direction parallel to silicide nodule diffusion is much smaller than that perpendicular to the diffusion direction. Because of the large high-resistive a-Si region, these high conductive paths have little effect on the overall resistance between the electrodes when the distance between the silicide diffusion fronts is long. However, when the silicide fronts are close enough to each other, these high conductive regions are not negligible. The resistance variation can thus occur when the resistance is close to saturation, as can be observed in Fig. 4-10 (a). There are traces of fast-diffusing Ni silicide along the <111> directions in a zigzag way. The angle of around 70.5 º is the angle between two variants of



(a) (b)

Fig. 4-10 AFM image of annealed a-Si at silicide diffusion front (a) Planer view; (b) 3D view.

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crystallites of <111> direction. In comparison, the MILC sample showed no obvious resistance fluctuation, implying a lower but more uniform speed for the lateral crystallization in MILC process.

4.4.2.4 Crystallization characteristics

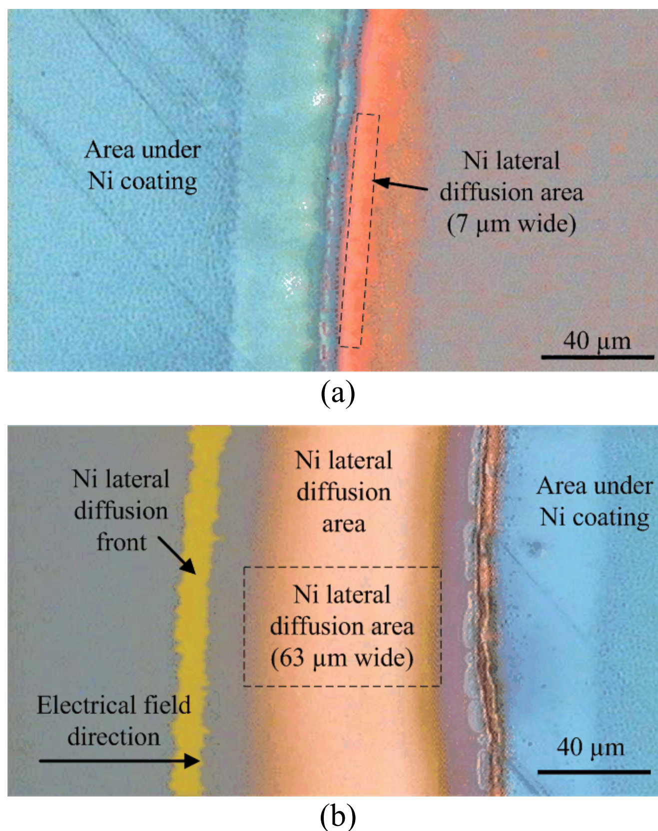

Fig. 4-11 Optical microscope images of Ni diffusion regions from (a) the positive and (b) negative electrodes. The Ni diffusion front in (b) has been darkened to present a high contrast for better visualization.

In accordance with the FALC results, it is noticed that the polarity of the applied electrical field influences the diffusion speed of the Ni silicide. The diffusion speed of Ni silicide from the low potential electrode is faster than that from the high potential electrode, as explained in section 5.2.2.3. Fig. 4-11 (a) and (b) show the optical microscope images of the Ni diffusion from the

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positive and negative electrodes respectively. The Ni diffusion length from the negative potential side is about nine times (63 μm vs 7 μm) longer than that from the positive counter electrode (Fig. 4-11).

Ni density on a-Si was reported critical to the quality of poly-Si by FALC or MILC. Too low a density may lead to incomplete crystallization and too higher a density would result in small grains [91]. The chemical potential difference of $NiSi_2$ at a-Si/$NiSi_2$ and poly-Si/$NiSi_2$ interfaces leads to the diffusion of Ni silicide out of the c-Si towards a-Si and Si atoms towards c-Si. In this way, while the silicide nodule mediates the crystallization of a-Si, the crystallization of a-Si in turn promotes the diffusion of Ni silicide towards a-Si, leaving c-Si with less silicide. So the MILC regions are expected to have the best crystal quality with large grains and less Ni contamination. Fig. 4-12 shows the Raman spectra of the Ni-coated region (MIC region), Ni-diffused (MILC) region, Ni diffusion front and amorphous region, together with that of crystalline silicon for comparison. Similar to crystalline silicon, the MIC and MILC regions are best fitted with a peak at 520 cm^{-1}, indicating a dominating crystalline phase. As shown in the inset of Fig. 4-12, the Ni diffusion front can be fitted by two peaks located at 480 cm^{-1} and 520 cm^{-1} respectively, indicating the coexistence of both crystalline and amorphous phases. The non-Ni area (a-Si region) can be well fitted with one weak and broad peak at 480 cm^{-1}, indicating an amorphous phase.

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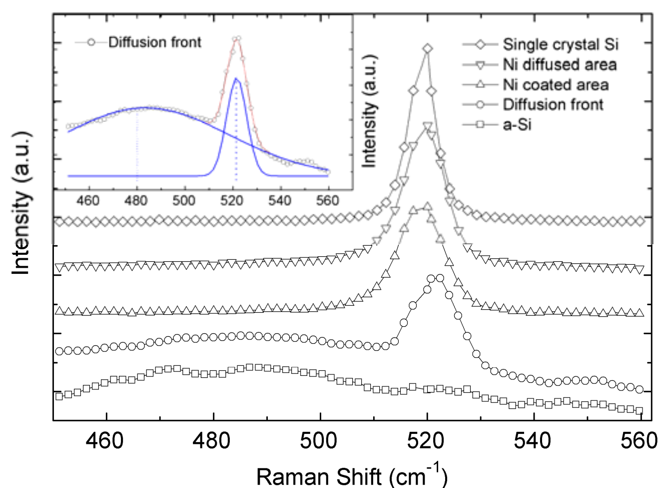

Fig. 4-12 Raman spectra at various regions of MILC LTPS thin films. The curves have been shifted vertically for clarity.

4.5 Summary

This chapter investigates the crystallization process of MILC and FALC. The crystallization behavior is studied. Dendritic lateral growth is observed in micrometer scale. A growth and scattering mechanism is utilized to describe the crystallization process. Clear different lateral crystallization fronts for MILC and FALC are for the first time observed. It was found that MILC has a well defined front but FALC does not, due to strong acceleration of electric field on Ni diffusion. Polarity and current heating effects are also presented. It is for the first time reported that the Joule heating effects diminish the polarity difference. *In situ* resistance measurement method is, for the first time, applied in the study of MILC and FALC process. Exponential resistance decay is observed for both MILC and FALC. The resistance at later FALC annealing stage is found to fluctuate.

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Chapter 5 FORMATION OF LARGE CONTINUOUS GRAINS BY FALC PROCESS

5.1 Numerical analysis of grain boundary effects on TFT performance

5.1.1 Introduction

Among the efforts to improve the performance of LTPS TFTs, an obvious emphasis is on the optimization of the active channel layer in two aspects: enlarge the grain sizes by engineering the crystallization processes [49, 92, 93] and reduce the inter- and intra-granular defects mostly by passivation [94- 98]. This is because that grain sizes and grain boundaries are the determining factors that affect the property of poly-Si films [38, 99]. In addition to the number of grain boundaries, their locations also affect the device characteristics [79]. Besides the successful efforts to enlarge grain sizes, another trend is the scaling down of TFTs in order to obtain better device performance and higher aperture ratio of a pixel. In view that crystallization techniques have enabled poly-Si films with grain sizes comparable to or even larger than device dimension [100, 101], it is necessary to control the number of grain boundaries and their positions along the channel of a TFT in order to minimize device-to-device variation. On this respect theoretical analysis and simulation play an important role in understanding the effects of grain boundaries on TFT performances.

Many works have been done on TFT simulation, aiming to study the devices or build analytical models for applications in TFT circuit simulation [102- 106]. As an important factor determining a TFT's characteristics, the

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grain boundary effect has always been included in the simulations, mainly in two approaches: effective medium method [102, 103] and potential barrier based method [99, 104, 105]. In the former, the channel is treated as a uniform layer with trap states evenly distributed in space. While in the latter, the grain boundary is treated as a thin and highly trap-concentrated layer perpendicular to channel length, which builds up a potential barrier for carrier transportation. This approach is more physically direct and more suitable than the former to study the grain boundary effect. Several reports have devoted to the grain size dependence of device property [93, 104]. However, little has been done using the physical 'grain boundary' method to study how the number of grain boundaries in the channel layer will affect the device characteristics. Varying grain boundary number is different from varying the grain size. With a fixed size of grain, the number of grain boundaries in the channel may vary depending on the location of the channel. Thus it is meaningful to study the TFT performance on the number of grain boundaries.

Besides the channel length, there will be averaging of the channel properties over the width of the channel. Hence the channel area will be a factor determining device property since it will determine the total grain population [107]. Regarding simplicity, only grain boundaries along channel length will be considered in discussing the uniformity problem.

5.1.2 Simulation method

Numerical simulation is conducted, using a 2-dimensional device simulator TMA-MEDICI. The mesh structure is shown in Fig. 5-1. The device is constructed as an n-channel LTPS TFT with 100 nm undoped LTPS active

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layer, 100 nm insulator SiO_2, and gate width/gate length=1 μm/1 μm. The channel LTPS film is treated as crystalline silicon grains with a certain density of trap states uniformly distributed in space, between which are grain boundaries. Source and drain regions are highly doped with phosphor (10^{21} cm^{-3}). No lightly-doped-drain (LDD) structure is included in the device structure, which is typically utilized to reduce leakage current.

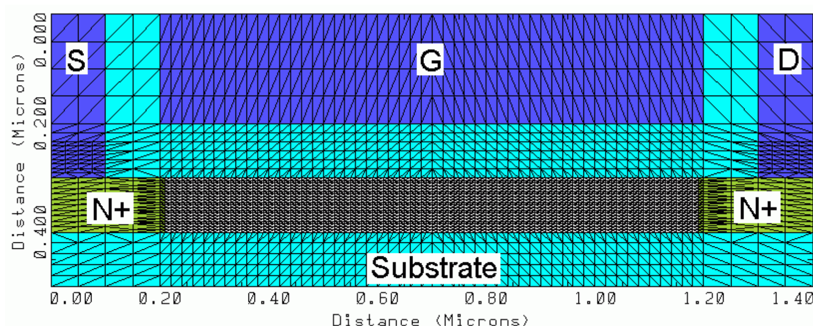

Fig. 5-1 TFT mesh structure used in numerical simulation

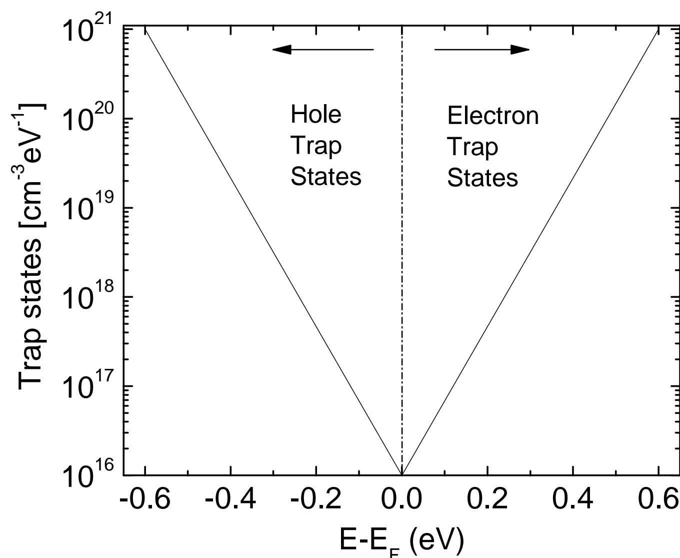

Fig. 5-2 Energy states distribution assigned to grain boundaries

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A grain is considered as crystalline silicon with a certain density of trap states uniformly distributed in space and a grain boundary is treated as a thin layer with high density of trap states distributed in the energy gap.

Based on the works by Migliorato and King, an exponential trap state distribution is chosen and assigned to grain boundaries, as shown in Fig. 5-2. The maximum density is 10^{21} cm^{-3} at band edges and the minimum is 10^{16} cm^{-3} at the mid-gap energy level [102,108]. The width of a grain boundary region is 20 nm, based on our investigation on the poly-Si films obtained by MILC of a-Si [109]. Besides the grain boundaries, the grains themselves are not perfect single crystalline silicon and intra-grain defects exist. A certain density of traps should also be assigned to them [94]. An energy distribution similar to that in grain boundaries but with a peak value of 10^{16} cm^{-3} ($\ll 10^{21}$ cm^{-3}) is assumed to distribute in the whole channel material. Poisson equation and current continuity equations are simultaneously solved. Carrier generation and recombination are included with fixed carrier life times of 10^{-5} and 10^{-6} s for electrons and holes respectively [110]. The effects of electric field, carrier concentration and temperature on carrier mobility are also included in the simulation.

5.1.3 Simulation Results and discussion

Simulated transfer and output characteristics are shown in Fig. 5-3. Corresponding to devices with grain boundaries ranging from 0 to 9, two groups of drain current I_D versus gate bias V_G curves for drain bias V_D equal to 0.1V and 10V respectively, are presented. Because the grain boundaries reduce the free carriers by trapping them and impede the movement of free carriers by

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forming potential barriers 79], a degradation of ON current is expected if more grain boundaries present in the channel. This is verified in Fig. 5-3. It can also be observed that the curves converge when the number of grain boundaries is larger than 5, implying a non-linear grain boundary dependence. This is also reflected in the device parameters discussed below, most of which are extracted from the transfer and output data.

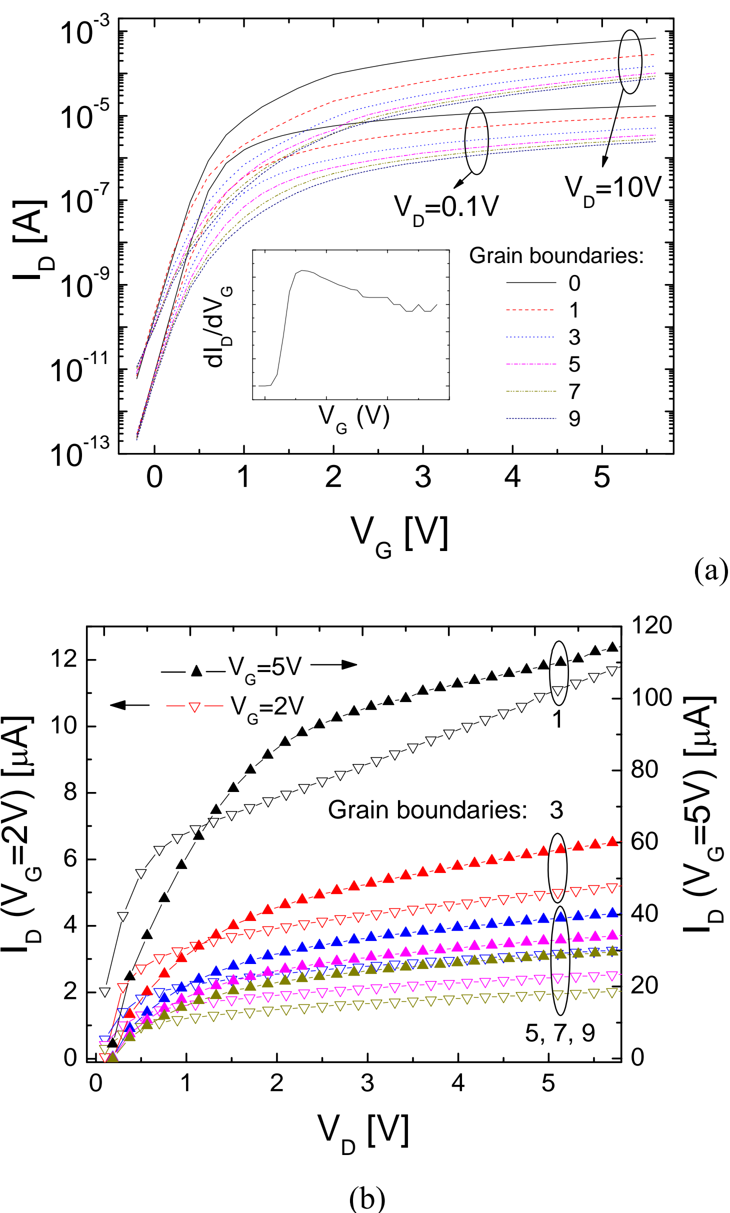

Fig. 5-3 Transfer (a) and output characteristics (b) of TFTs with various number of grain boundaries in the channel

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- Threshold voltage

Extrapolation method is applied for threshold voltage extraction, since the maximum first derivative clearly exists as shown in the inset of Fig. 5-3(a) and this method is readily applicable. V_{TH} is defined as the V_G axis intercept (i.e., I_D=0) of the linear extrapolation of the I_D-V_G curve in linear region. Fig. 5-4 shows V_{TH} dependence on grain boundary number. The V_{TH} value varies dramatically when there are few grain boundaries in the channel. If there are 3 or more boundaries along the channel, V_{TH} increases at a much slower pace and approximately in a linear mode.

In poly-Si TFT, the threshold voltage is affected by the trap states in the channel and the potential formed at grain boundary locations. An applied gate voltage first lowers the potential barriers formed at the grain boundaries and the induced carriers will first fill the trap states. Only after a certain voltage V_{TH} can the barriers be much lowered, the induced carriers be free carriers and mainly contribute to the current flow rather than filling traps.

At higher gate voltage, electrons accumulate and a small increase of the gate voltage will induce a large amount of carriers. Thus if an extra grain boundary emerges when there already exist a few, the additional trap states it introduced can be easily filled due to the availability of electrons or holes. The scattering effect of the additional grain boundary is less prominent compared to overall grain boundaries. This explains the behavior of the grain boundary effects on V_{TH}.

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Similar results have been reported about V_{TH} dependence on the grain sizes [104, 105]. However the result from grain size perspective does not reveal the device-to-device variation problem when grain size becomes large because it is applicable only when grains are much smaller than the channel dimension. With the increasing of grain dimensions, the statistical fluctuation of V_{TH} becomes prominently detrimental.

- Field effective mobility

The field effective mobility μ_{eff} is determined from the linear region of the I_D versus V_G curve at a small drain bias (V_D=0.1V), using Eq. 3-2 [111].

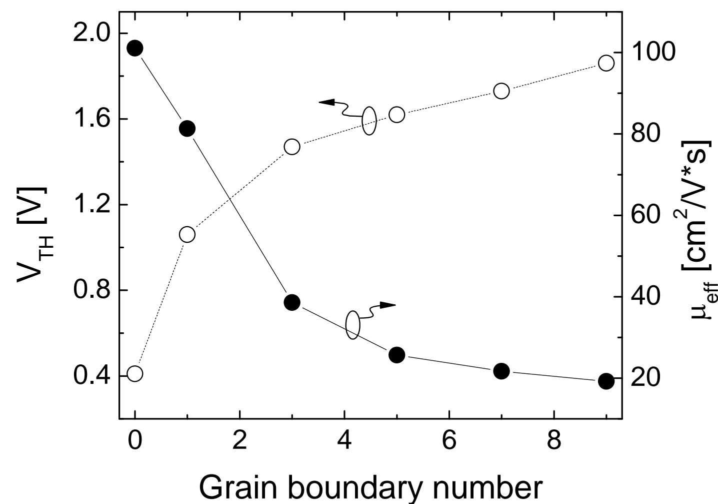

Fig. 5-4 Threshold voltage and field effective mobility dependence on grain boundary number in channel

As shown in Fig. 5-4, μ_{eff} degrades with more grain boundaries in the channel. This is expected since more grain boundaries introduce more trapping and scattering to moving carriers. Similar to the V_{TH} dependence, μ_{eff} varies remarkably when grain boundary number is small but it varies slowly in a near-linear mode when that number exceeds 5. This can be explained as follows.

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When there is no grain boundary in the channel, the intra-grain defects are the only factor impeding carrier transportation. The appearance of a grain boundary will greatly change the potential and trap distribution in the channel. With the increase of the grain boundary number, the boundaries play a more important role and become dominant. In this case, the addition of a grain boundary will cause less change to the overall potential and trap distribution in the channel, as shown in (Fig. 5-5). The trapping and scattering effects in the channel varies less with an additional grain boundary. So μ_{eff} is less dependent on the number of grain boundaries when this number is large (≥ 5).

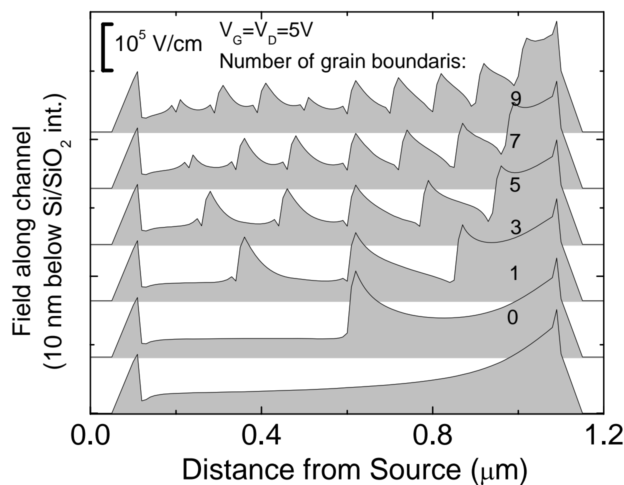

Fig. 5-5 Effects of grain boundary number on field distribution

- Subthreshold swing and kink effect

Fig. 5-6 shows the grain boundary effects on the subthreshold swing S_S and the kink effect of the device. It can be seen from the figure that S_S increases and the kink effects become weaker when grain boundary number increases. The S_S increases with grain boundary number because at a higher density of grain boundaries, a larger portion of gate bias increase will contribute to the trap

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filling rather than inducing more free carriers. So larger increase of gate voltage is necessary for a relatively small amount of increase in drain current, thus S_S value is larger. When there exist more grain boundaries, an additional one will contribute less to the overall trapping effects. So the effect of an additional grain boundary on S_S is less severe when there are more grain boundaries. This is the reason why the S_S variation rates decrease with the increasing of the grain boundary number.

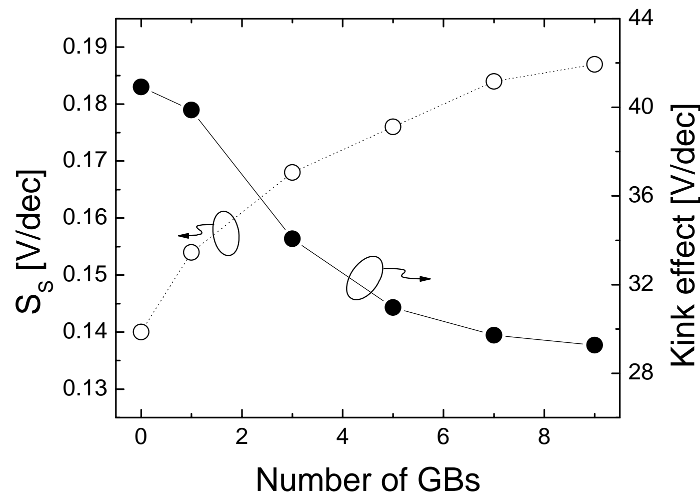

Fig. 5-6 Effects of grain boundary number on subthreshold swing and kink effects

To investigate the degree of impact by grain boundaries, the kink effect is defined in the same way as in the SPC TFT characterization (Section 3.2.2.2), using the I_D-V_D curve at V_G=5V. The field changes less with the introduction of an extra grain boundary when the grain boundary number exceeds 5 and the kink effect is less severe, as shown in Fig. 5-7. However, when there are only a few grain boundaries, one extra grain boundary will dramatically alter the electric field distribution in the channel, as illustrated in Fig. 5-5. This field change in turn affects the field-induced impact ionization and thus leads to

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greater kink effect. This observation is quite similar to the dependence of V_{TH}, μ_{eff} and S_S on the number of grain boundaries along channel length.

- Leakage current

Leakage current is defined as the drain current at V_G=0 V when the drain is specifically biased at certain fixed voltages (0.1V and 5V in the thesis). Fig. 5-7 shows the grain boundary effects on the off-state current I_{OFF} and ON/OFF current ratio of the device at V_D=0.1 and 5V respectively. When V_D=0.1V, leakage current is dominated by the thermal carrier generation via trap states. When V_D=5V, I_{OFF} is dominated by Frenkel-Poole emission [112]. Both occur mostly at grain boundaries due to high density of trap states. Thus more grain boundaries will lead to more carriers which contribute to the leakage current flow. On the other hand, grain boundaries impede the current flow by trapping and forming potential barriers. The overall effects result in a decrease in the OFF current but to a much-limited extent.

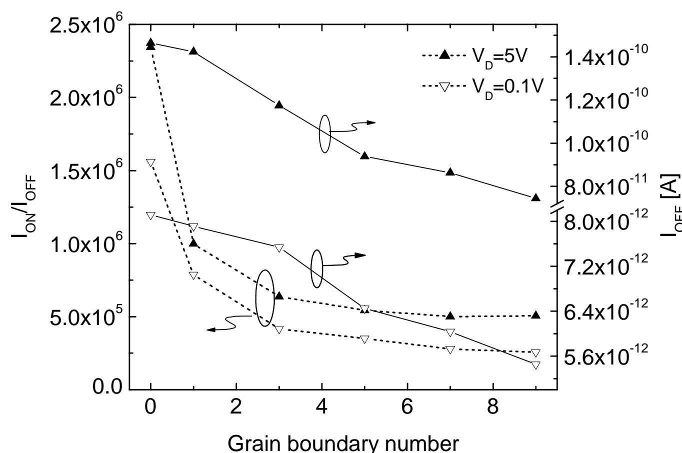

Fig. 5-7 Effects of grain boundary number on I_{OFF} and I_{ON}/I_{OFF} ratio

I_{OFF} decreases by no more than 2 times with 9 grain boundaries (Fig. 5-7), compared to about 10 times decrease for ON current I_{ON} (Fig. 5-3(b)). As a

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result, the I_{ON}/I_{OFF} ratio decreases as more grain boundaries exist in channel. The I_{ON}/I_{OFF} ratio is not very high for any grain boundary number (<2.2×10^6) because no LDD structure is included. The variation behavior of the ON/OFF current ratio with grain boundary is again similar to the parameters discussed above, in that the variation rate decrease with the increase of an additional grain boundary if there already exist 5 or above.

5.1.4 Conclusion on grain boundary number dependence

As the consequence from the increase of grain boundaries, I_{OFF} and kink effect are decreased. However other parameters including V_{TH}, μ_{eff}, I_{ON}, I_{ON}/I_{OFF} ratio and S_S are degraded.

In consistency with the statistical conception, when there are a small number (<5) of grain boundaries, any variation of boundary number will dramatically change the potential distribution in the channel and the device characteristics will be greatly affected. If the number of boundary reaches 5 or more, any additional grain boundary will cause much less device performance degradation. Besides, we can see that the effective medium approximation is valid only when there are more than 5 grain boundaries along the channel. Nowadays, annealing techniques are capable of obtaining poly-Si films with grain sizes comparable to or even larger than device dimension. In this case, it becomes important to consider the grain boundary effect and control the exact number of grain boundaries in the channel. This means that forming continuous large grains, controlling the dimension and location of crystalline grains with respect to the devices has become a crucial task. As an effort to obtain large

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continuous grains and controlled grain boundary distribution profiles, FALC was investigated.

5.2 Large continuous grains by field aided lateral crystallization

5.2.1 Field aided lateral crystallization process

A-Si films of 160 nm deposited on SiO_2/Si stack structure were annealed using FALC method. A DC voltage was applied between the carbon electrodes, which built up an electric field about 200V/cm between the two Ni pads. During annealing process, the current of the loop was also measured and recorded. The current in our experiment varies from 70 to 375μA, which correspond to a current density of 87 and 468 A/cm^2 respectively, calculated from dividing the current by the film cross section between the electrode strips.

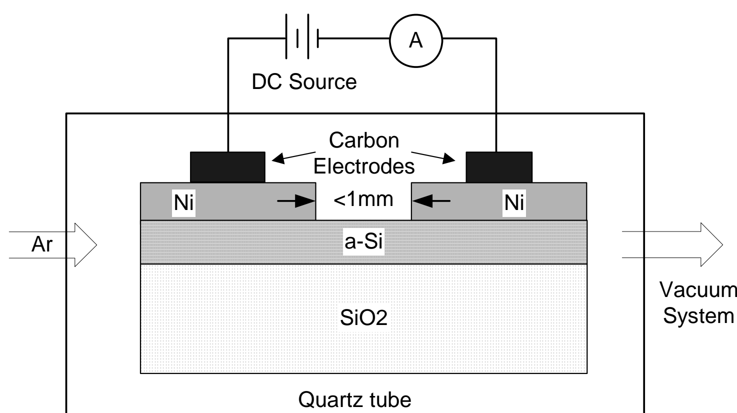

Fig. 5-8 Schematic diagram of the FALC process set-up

Various regions, including Ni-coated region, lateral crystallized region and amorphous region, of the annealed sample were characterized by optical microscopy and SEM after Secco etching. The crystallization effects of various regions of sample were also characterized by Raman spectroscopy.

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5.2.2 Results and analysis

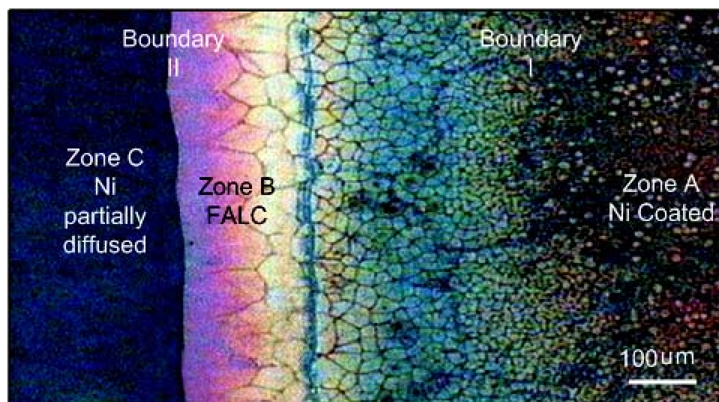

Fig. 5-9 Optical micrograph of the FALC sample (Secco etched) near the cathode with various zones marked.

The micrograph of the FALC sample is divided into three regions (Ni-coated region (Zone A), FALC region (Zone B) and region partially Ni diffused (Zone C)) beyond FALC. The regions are marked in Fig. 5-9. Significant difference in crystallization effects can be observed for various zones with diverse Ni concentrations [37, 40].

5.2.2.1 Raman spectroscopy

Fig. 5-10 shows the micro-Raman spectra of LTPS films at different regions defined above of the FALC sample, together with those of the as-deposited amorphous silicon and crystalline silicon wafer for comparison. The values for full width at half maximum (FWHM) of the corresponding films are also shown as the inset. The best crystallization effects are achieved in zones A and B but the former has high-density small grains and the latter has large grains, as will be demonstrated by SEM images of the annealed film. The peak for zone C is weaker comparing to zones A and B. But it still indicates the co-existence of a crystalline phase, which is quite different from the as-deposited

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amorphous silicon film. However, the left 'shoulder' of the peak is elevated a bit, indicating the presence of amorphous phase in Zone C. Obviously, the large grains in Zone B is favorable for device fabrications.

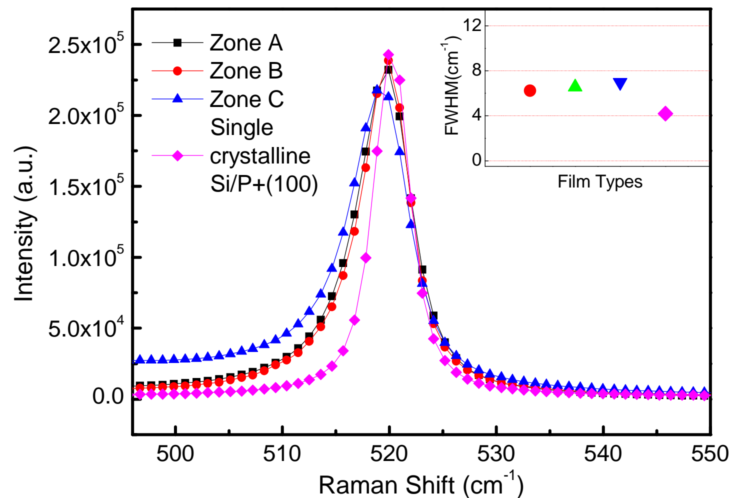

Fig. 5-10 Raman spectra for various FALC zones, as-deposited amorphous silicon thin film and crystalline silicon

5.2.2.2 Observation of the LTPS grains

Fig. 5-11 shows the SEM images of Ni-coated region (a), transition region (Boundary I) from Ni-coated region to FALC region (c), FALC region (d), boundary between FALC and amorphous region (Boundary II) (e), respectively. The Ni-coated region (Zone A in Fig. 5-9(a)) consists of a number of large grains and much smaller grains that spread all over the film (Fig. 5-11(a)). Some of the small grains fill up the inter-grain boundaries of large grains (Fig. 5-11(b)). The sizes of largest grains are up to about 20 μm and that for small ones varied extensively. The large grains are formed due to continuous grain growth and the small grain formation is due to the high Ni concentration that leads to numerous nucleation sites. Concurrent grain growth from all these nucleation sites results in small grains. However, for the large grains, there are

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still high density of intra-grain defects or silicide clusters, as shown by the etching pits (white points on grains) in Fig. 5-11(a) and (b).

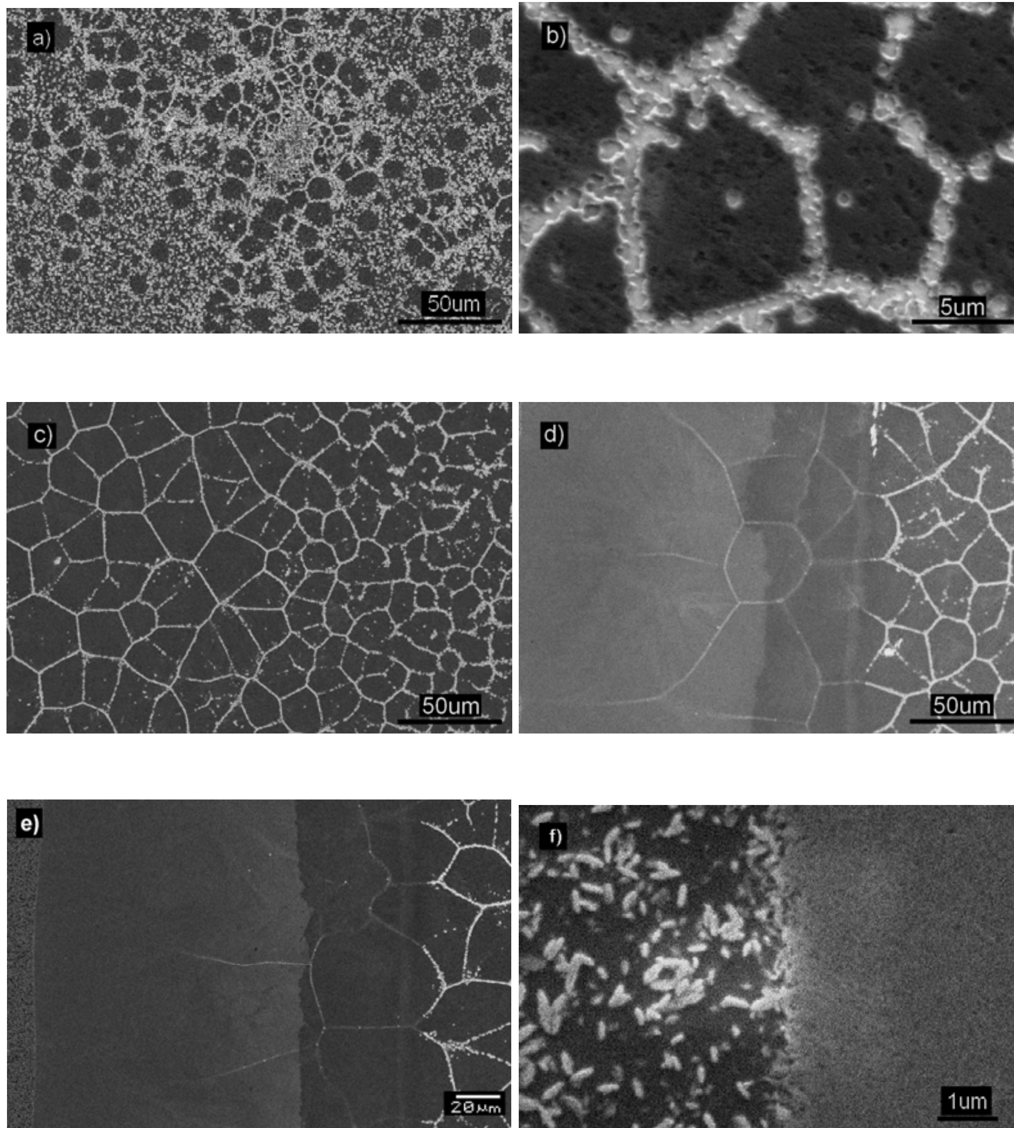

Fig. 5-11 SEM images of Secco etched poly-Si films.

(a) Center of zone A, (b) Zone A with magnification, (c) Boundary I, (d) Zone B, (e) Boundary II. The Zones and boundaries are defined in Fig. 5-9

Fig. 5-11(c) reveals the obvious transition from highly defective region with small grains to a less defective region with larger grains. Comparing to the grains in the right half of figure, the grains and their boundaries of the left half

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is much cleaner and clearer, indicating good crystallinity with less defects and silicide concentration. Two factors account for the improved crystal quality of the grains on the left over those on the right. One is that the Ni atoms are partially diffused forward. The electric field at the Ni coating edge (Boundary I in Fig. 5-9) is stronger than that of the area with Ni coating, due to the different conductivity of the Ni film and the silicide that would form subsequently. Thus, at the edge of Ni film, Ni is strongly depleted and smaller concentration is left which favors large grain formation. Another factor is the electric field applied during annealing process, which helps to speed up the metal induced crystallization significantly [37].

As has discussed, the chemical potential of Ni atoms is lower at the $NiSi_2$/a-Si interface, while that of the Si atoms is lower at the $NiSi_2$/c-Si interface [74]. Thus, while the Ni silicide induces the crystallization, the crystallization process also promotes the Ni diffusion towards a-Si. However, the Ni diffusion rate originated from this chemical potential driving force is quite limited. The MILC rate was reported to be no more than 2 µm/h (1~1.8 µm/h [40]; 1.6 µm/h [70]; 1.5~2 µm/h [73]) at 500 ºC annealing. And even worse, the MILC rate decreases as the process proceeds [113]. To shorten the annealing time and enhance the lateral crystallization length, FALC has been applied to improve the lateral crystallization rate drastically (9.5 µm/h for 3 hours annealing and a field of 2.1V/cm [73], ~21 µm/h for 80 minutes annealing at a field of 53.5V/cm [90], both at a temperature of 500 °C). From Fig. 5-11(d) and (e), by applying a strong electric field of 200V/cm, after 5 hours of annealing at 500 ºC, a FALC crystallization length of 170 µm and an average rate of 34 µm/h is achieved.

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Besides the field enhancement effect in MIC process [75,114], a current effect presents in the FALC [115]. The Joule heating caused by current crowding at the silicide locations accelerates the nucleation formation and grain growth from the sites. This is the reason why large grains, as large as 100 µm in sizes (Fig. 5-11(d)) have formed. After 20 seconds dip in Secco etchant, the grain surface remains featureless, indicating that they are monocrystalline grains [76]. In the area further away, there are sparsely distributed grains and most of the amorphous film has been etched away (Fig. 5-11(e)). The smaller grains are formed either by solid phase crystallization or Ni silicide facilitated nucleation more likely. The large grains formed by FALC are less Ni contaminated, as few etching pits can be observed in Fig. 5-11(d) and (e). This is because Ni is fast driven forward by the electric field and the chemical potential factors, leaving less contaminant in the polycrystalline silicon grains.

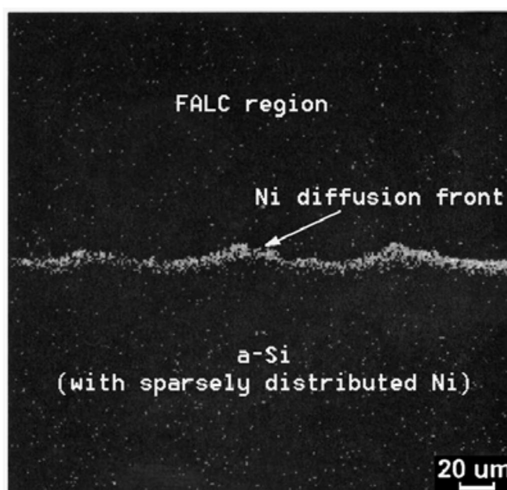

Fig. 5-12 SIMS analysis for two-dimensional distribution of Ni concentration around the crystallization front. The sample under test was Secco etched. Ni concentration is proportional to the density of the white spots.

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This is verified by two-dimensional scanning image of Ni distribution obtained with secondary ion mass spectrometry (SIMS) analysis, as shown in Fig. 5-12. A diffusion front with higher Ni concentration clearly presents, around which is less Ni contaminated. The sparsely distributed Ni in the amorphous region explains the existence of small grains beyond FALC area shown in Fig. 5-11(f).

5.2.2.3 Polarity dependence of the crystallization behavior

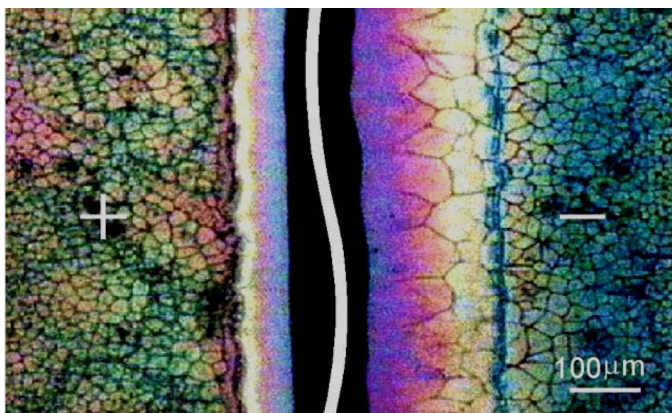

Fig. 5-13 Polarity dependence of Ni diffusion and crystallization effects

Since the Ni diffusion is strongly field-dependent, polarity-dependent diffusion behavior is expected naturally. Fig. 5-13 shows the optical microscopy image of the FALC sample showing the different lateral crystallization length from positive and negative electrodes. The diffusion length from the negative electrode is about 6 times longer than that from the positive one. It seems a sound explanation that Ni is negatively charged in $NiSi_2$ due to the negative Mulliken charge. What's more interesting is that the diffusion at the positive side is not suppressed. The Ni diffusion rate from the positive electrode in FALC is still a few times faster than that in MILC without electric field. For example, the diffusion rate is ~ 6 μm/h from positive electrode in FALC, comparing to < 2 μm/h in MILC [40, 73, 90]. The reason

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under the lateral diffusion enhancement at positive electrode is not clear yet and needs further investigation. A possible reason is the Joule heating by the current crowding at locations where higher conductive Ni silicide formed. Localized high temperature regions promote the diffusion process and crystallization at the site.

The FALC method reported in reference [42] applies electric field by constructing two electrodes, in between which patterned Ni is deposited and the devices are fabricated. In the FALC process proposed in this thesis, electric field is directly built between the Ni strips, which are also used for the metal sources in FALC process. Though more complicated in applying electric field, this method provides high electric field and great process flexibility without additional mask comparing to common MILC process. Also, for sparsely distributed devices as in display applications, it is not so difficult in applying electric field. Forming comb-like shaped electrodes can be a solution. As the Ni strips are close to each other (at most a few millimeters), the electric field can be more efficiently applied and higher electric fields can be easily realized. Besides, the electric field direction can be specifically defined locally, which provide more flexibility comparing to only one field direction reported in reference [42] and [116]. Device performance has been reported to be dependent on grain growth direction [101]. This field orientation will affect the device property by affecting the grain growth direction. Thus the devices can be fabricated in the large grain region (Zone B in Fig. 5-9) with an appropriate directionality for better performance. This FALC annealing is applicable for large-area electronics in terms of its capability of large grain formation.

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A-Si and Ni can be uniformly deposited over large area. Thermal annealing process is also uniform over large area. The uniformity of FALC process is thus obtainable. By setting the same relative location between Ni source and the device channel region, uniform device performance over large area can be achieved.

5.3 Summary

With the advancement of crystallization techniques, grains with sizes up to the device dimensions are obtainable. This leads to the statistical fluctuation of the distribution and location of grain boundaries in a device channel. Numerical simulation is conducted to analysis the detailed dependence of device performance on grain boundary numbers in the channel. The overall effect is that more grain boundaries will degrade a TFT's performance. It is a reasonable objective to obtain larger grains and a similar distribution behavior of grain boundaries in a device channel. FALC is conducted as such an effort. With FALC process at intermediate electrical field, continuous grains with sizes up to 100 μm are obtained. Since the grain distribution is strongly dependent on the Ni source and field polarity, similar grain boundary distribution can be achieved by the controlling configuration of Ni pad geometry and the same electric field intensity. The polarity dependence is investigated and Joul heating is for the first time interpreted as the reason for diminished polarity difference.

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Chapter 6 THIN FILM TRANSISTORS BY NICKEL INDUCED LATERAL CRYSTALLIZATION

6.1 Fabrication of thin film transistors

MILC TFTs are fabricated by MILC LTPS films. Fig. 6-1 shows key process steps with the corresponding cross-sections of the TFT. Corning 1737 glass was chosen as the substrate. A layer of 50 nm SiO_2 is formed by low temperature furnace deposition at 450 °C (low temperature oxide, LTO), which serves as a buffer layer to the contaminants from the glass substrate, such as aluminum, boron and sodium [117]. Then a layer of 50 nm a-Si was deposited using LPCVD as described in section 3.1.1. The a-Si layer was then patterned, forming active islands as shown in Fig. 6-1(a).

A layer of 50 nm LTO is deposited before the Ni for MILC process is evaporated (Fig. 6-1(b)). The purposes of this layer are: (1) to completely isolate the Ni from a-Si film where direct contact between Ni and a-Si should be avoided; (2) to serve as the gate dielectric. An a-Si layer of 300nm is then deposited and patterned (Fig. 6-1(c)), which serves as the gate electrode, combined with the following Ni MILC and ion implantation process. Opening holes on LTO for MILC are formed by lithography and wet etching. A thin layer of Ni (2 nm) is deposited by electron beam evaporation. MILC annealing is then conducted at 550 °C for 50 hours, after which the un-reacted Ni is removed with wet-etching (Fig. 6-1(d)). The annealing duration is determined

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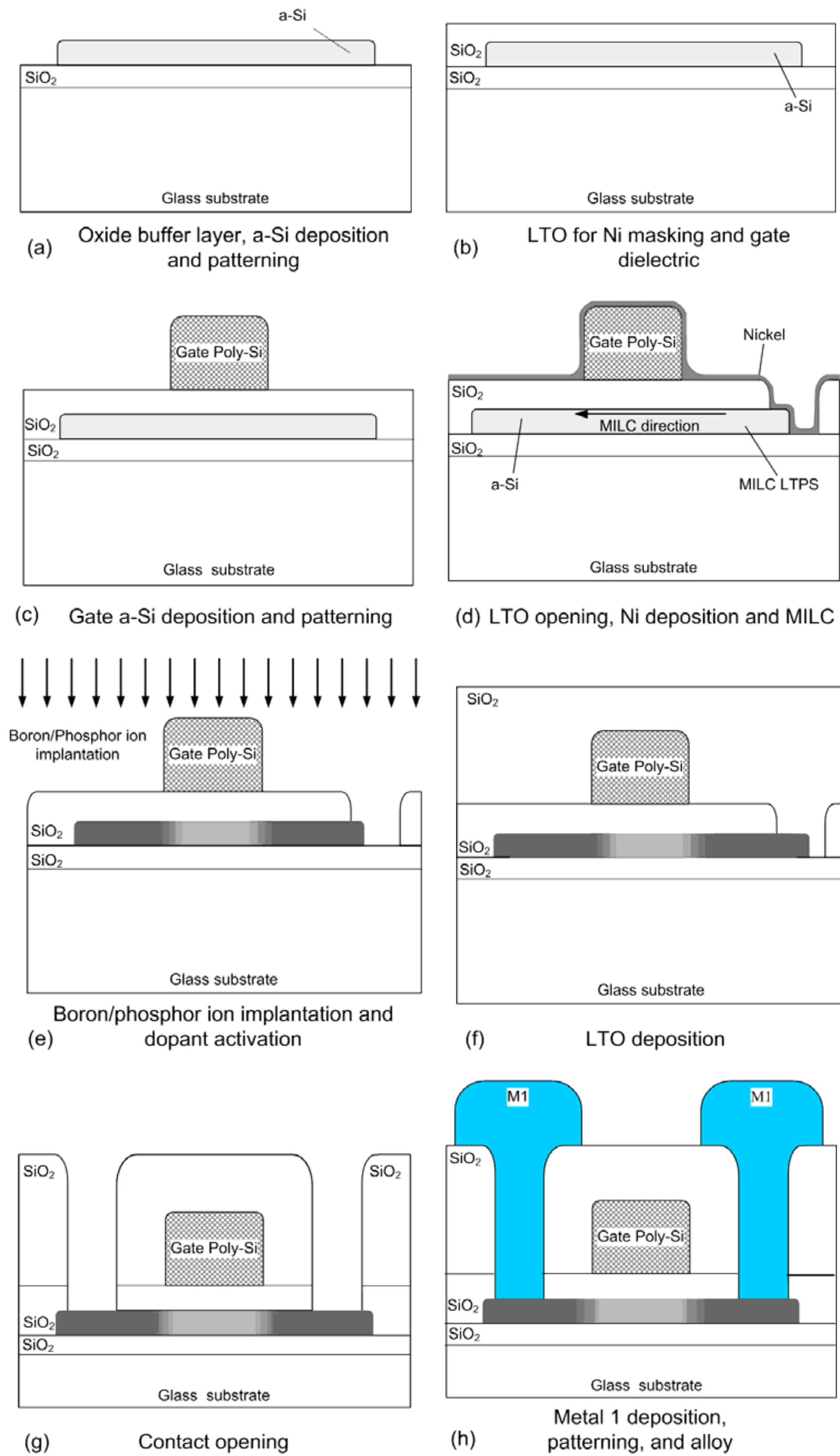

Fig. 6-1 Process steps of MILC TFTs

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such that the longest device (with channel length L = 64 μm) in the design will get fully crystallized (see section 6.2.2).

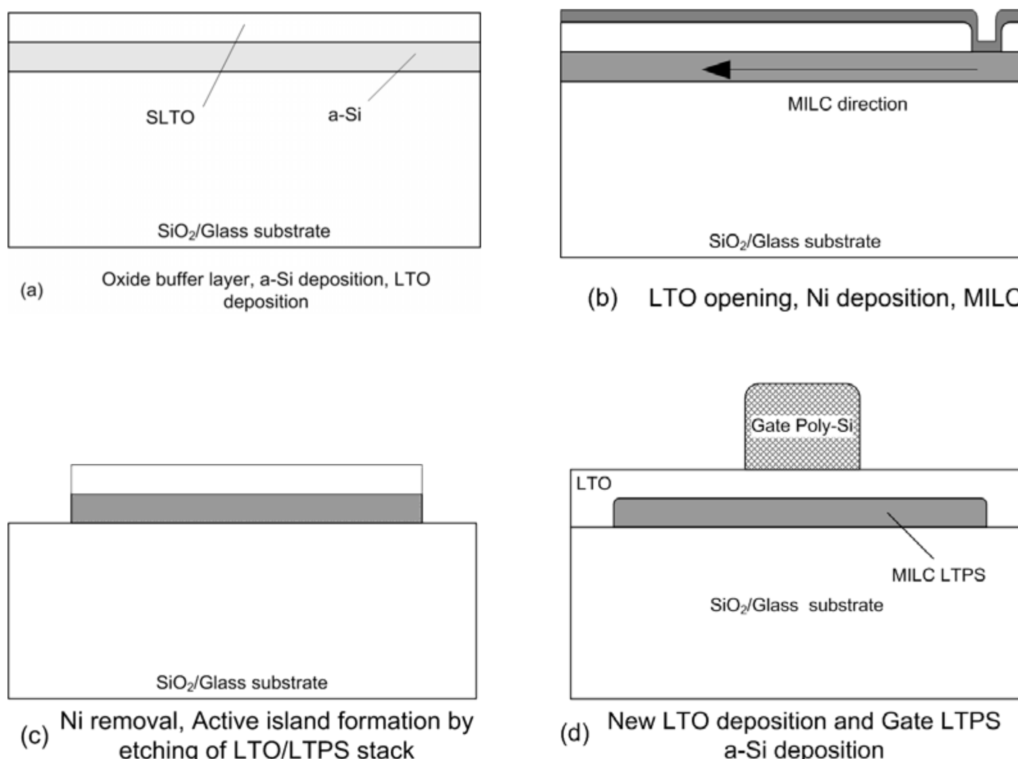

Fig. 6-2 MILC process sequence in LTPS TFTs with sacrificial LTO

For some substrates, the process sequence is different in the MILC process. In the processing of these substrates, the 50 nm LTO serves only as a sacrificial layer to completely isolate the Ni from a-Si film where direct contact between Ni and a-Si should be avoided. To differentiate, the LTO for this purpose only is called sacrificial LTO (SLTO), while the LTO that serves as gate dielectric as well is called gate LTO (GLTO). SLTO MILC process sequence is shown in Fig. 6-2. In SLTO process, the a-Si active layer is not patterned when the LTO sacrificial layer is deposited. After opening is formed by lithography and wet etching on the LTO, a thin layer of Ni (2 nm) is deposited. MILC annealing is then conducted at 550 °C for 50 hours. Wet etching is applied after the

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annealing process to remove the un-reacted Ni, completing the MILC process. Active region is defined by dry etching of the LTO/MILC LTPS film stack, after which the LTO is completely removed. A new LTO layer of 50 nm, which is free from Ni contamination, is deposited on to the LTPS films, which serves as the gate dielectric. After the gate oxide formation, LTPS of 300 nm is deposited as the gate electrode. The gate LTPS is then patterned by dry etching.

After the MILC process and the gate LTPS patterning, the following process steps are quite similar to those in SPC TFT fabrication. Main steps include boron and arsenic ion implantation and activation by thermal annealing (Fig. 6-1 (e)), LTO deposition (Fig. 6-1 (f)), contact hole opening (Fig. 6-1 (g)), metal deposition, patterning, and alloy formation (Fig. 6-1 (h)).

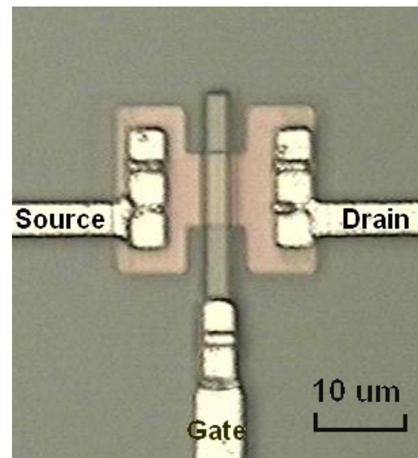

Fig. 6-3 Optical microscopy image of a fabricated p-channel TFT, with W/L=8μm/4μm. MILC starts from both source and drain sides. No difference is observable between p- and n-channel TFTs under microscope.

In the mask design, there are both standalone TFTs and TFT arrays. There are totally four TFT arrays, with one for a LCD panel and the rest three for

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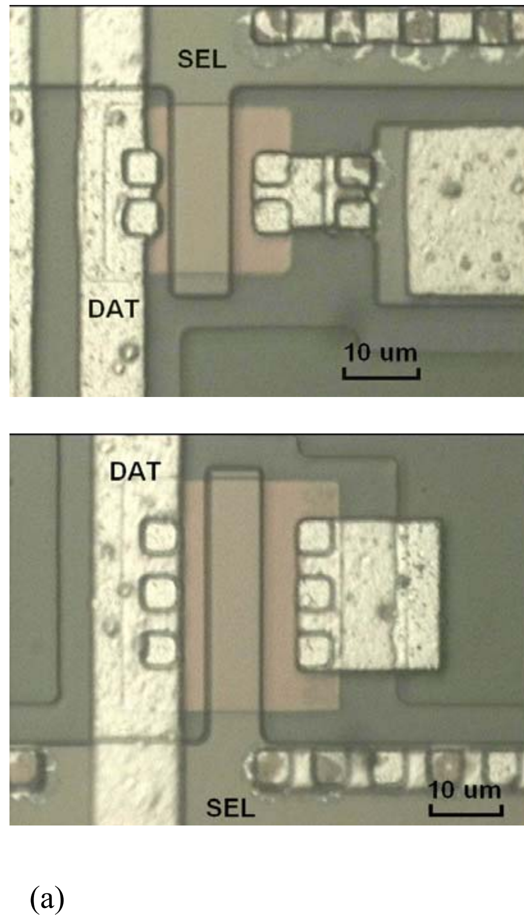
OLED panels. Fig. 6-3 shows the optical microscopy image of a standalone p-channel TFT. Fig. 6-4 illustrates two p-channel devices in an OLED panel (a) and in a LCD panel (b), respectively.



(a) (b)

Fig. 6-4 Optical microscopy image of TFTs in display panels.

(a) A TFT in an OLED panel, W/L=20μm/8μm.
(b) A TFT in a LCD panel, W/L=28μm/8μm

6.2 Characterization of thin film transistors

6.2.1 Device performance

It was found that TFTs exhibit the same *I-V* behavior, whether the side with Ni pattern is treated as the source or the drain in device measurement. The devices introduced below in this chapter will use the device measurement data

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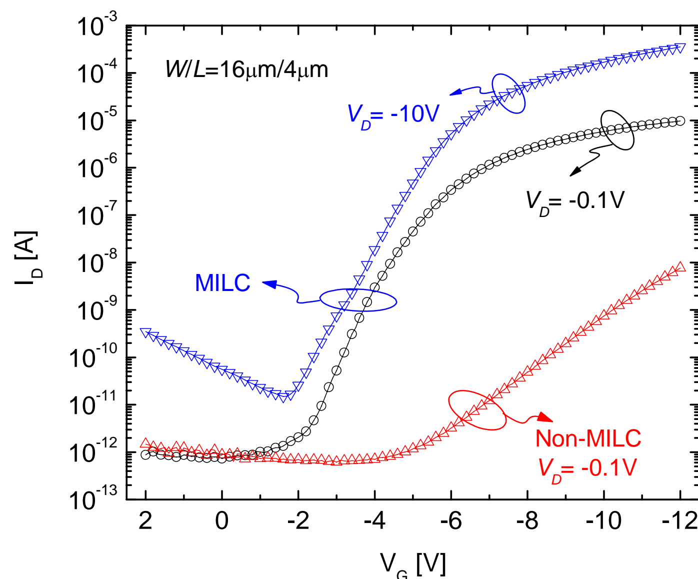
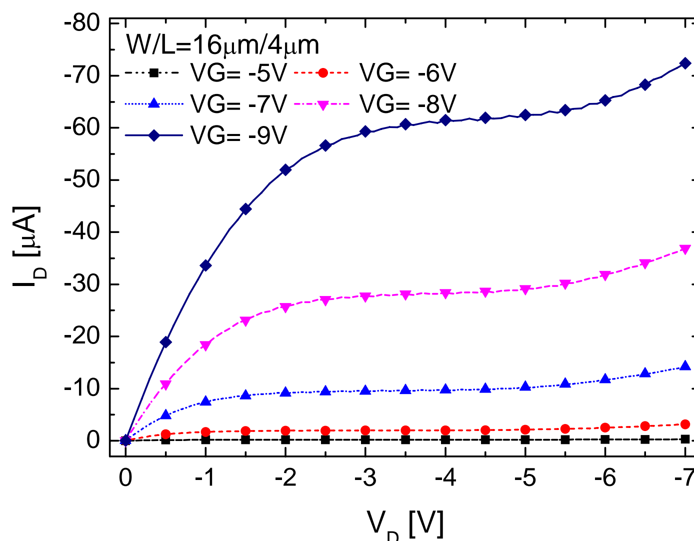


(a)



(b)

Fig. 6-5 I_D-V_G and I_D-V_D characteristics of a p-channel MILC TFT, with W/L=16μm/4μm. The extracted device parameters are as follows: (1) MILC TFT: V_{TH}= -4.95 V, μ_{FE}=71.38 cm^2/V*s, S_S= -0.51 V/dec, I_{ON}/I_{OFF}=1.32x10^7; (2) Non-MILC TFT: V_{TH}= -9.56 V, μ_{FE} = 0.29 cm^2/V*s, S_S= -1 V/dec, I_{ON}/I_{OFF}=2.5×10^4.

with the Ni pattern located at the drain side of the TFT. Fig. 6-5 shows the transfer and output characteristics of a p-channel MILC TFT, which W/L ratio

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is 16μm/4μm. Using the same parameter extraction methods as those applied for SPC TFTs (Chapter 3), device parameters are extracted as follows. Using I_D value of 10^{-8} A as the fixed drain current per unit W/L for V_{TH} extraction, the V_{TP} is extracted to be -4.95 V. Other parameters, such as carrier mobility, I_{ON}/I_{OFF} ratio, and the sub-threshold swing S_S are 71.38 $cm^2/V{\cdot}s$, 1.32×10^7, and 0.51 V/dec, respectively. The I_{OFF} at V_D = -10V is 1.5×10^{-11}A. For comparison, the I_D-V_G curve of a non-MILC-processed TFT with the same dimension is also shown in the figure, which is obviously inferior from the MILC-processed one. The non-MILC TFT parameters are extracted as follows: V_{TH}=-9.56V, μ_{FE}=0.29cm^2/V*s, S_S= -1V/dec, I_{ON}/I_{OFF}=2.5×10^4.

Fig. 6-6 shows the transfer and output characteristics of an n-channel MILC TFT, with W/L ratio of 16μm/4μm as well. The parameters extracted are as follows: V_T =3.89 V, μ_{FE}=70.29 $cm^2/V{\cdot}s$, S_S=0.85 V/dec, and I_{ON}/I_{OFF} =2.27×10^6. The I_{OFF} at V_D = 10V is 7.99×10^{-11}.

The mobility of the MILC TFTs falls into the range from 50 to 110 $cm^2/V{\cdot}s$. Table 6-1 compares the device performance with reported data. The overall device performance is comparable to the reported results. And the best devices obtained show even better performance than that the reported. The device performance is also comparable to that of TFTs by conventional ELA LTPS films, whose mobility ranges from 20 to above 200 $cm^2/V{\cdot}s$ [118]. Advanced ELA techniques render even higher mobility. The off-state current, especially when $|V_D|$=10V, ranges from 10^{-11} to about 10^9 A. The maximum value of 10^{-9} A is higher than expected values, which is typically in the order of

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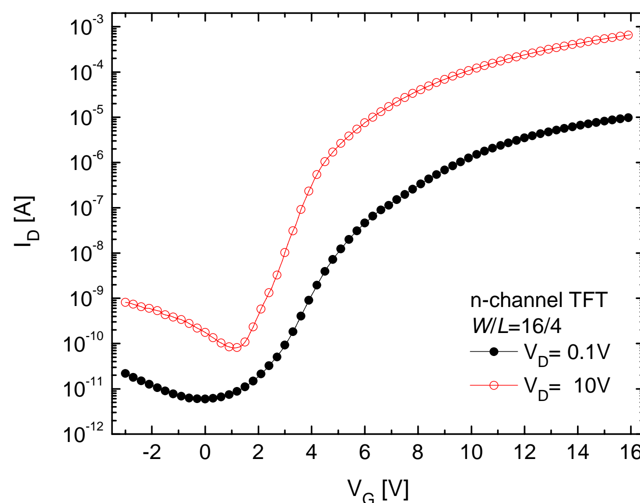
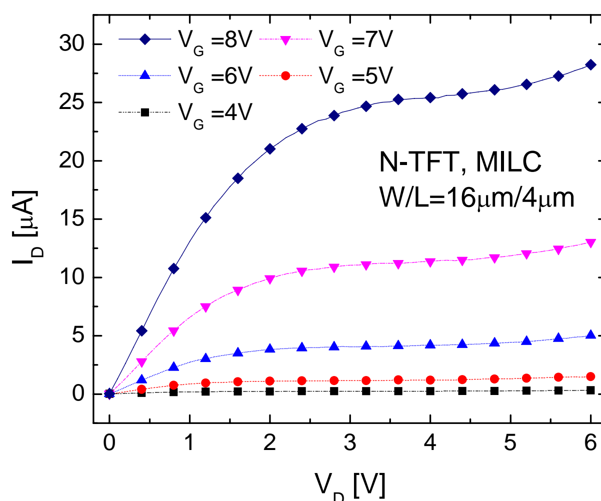
pA/μm. This issue can be addressed by process or device structure engineering, such as LDD structure, which is not applied in this thesis.



(a)



(b)

Fig. 6-6 I_D-V_G and I_D-V_D characteristics of an n-channel MILC TFT, with W/L=16μm/4μm. The parameters extracted are as follows: V_T =3.89 V, μ_{FE}=70.29 cm^2/V·s, S_S=0.85 V/dec, and I_{ON}/I_{OFF} =2.27×10^6. The I_{OFF} at V_D = 10V is 7.99×10^{-11}.

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Table 6-1 Device performance of MILC TFTs with comparison with reported data.

Parameter	P-TFT	Ref. 119	Ref. 120	N-TFT	Ref. 42	Ref. 121
V_{TH}	-4.5 - -6	-6	-1.7	3.6-3.98	3.7	7.5-7.7
μ_{FE}	45-86	35	90	50-110	21.74	70-86
S_S	0.4-0.7	1.1	0.71	0.85-1.2	N/A	2.21-2.24
I_{OFF}(pA/μm)	0.01-0.1	0.5	N/A	0.1-0.5	679	N/A
I_{ON}/I_{OFF}, 10^6) (VD=0.1V)	2.5-57	6	10	0.36-7	0.064	3.4-4.1

N/A = Not available.

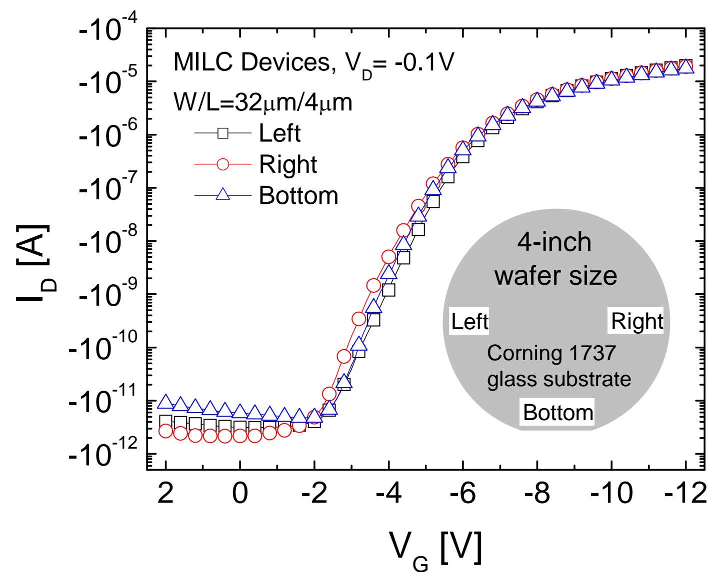

Fig. 6-7 Comparison on characteristics of devices at different locations on the same substrate. The glass substrate is of the same dimension as a 4-inch Si wafer.

Symmetric parameters are obtained for p- and n-channel TFTs. The symmetric values for V_T (-4.95V vs. 3.89V) and S_S (0.51 vs. 0.85 V/dec) simplify the voltage biasing scheme and the symmetric values for μ_{FE} (71.38 vs.

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70.29 $cm^2/V{\cdot}s$) enables similar device dimension in circuit design without lowering noise margin [122], in contrast to asymmetric device characteristics.

The MILC approach has high degree of uniformity over the whole substrate. As illustrated in Fig. 6-7, device performance over the whole substrate is uniform, which is important in order to construct circuit units using TFTs. The parameter variation extracted from the 3 regions in the figure is within 6 percent, proving the uniformity advantage of MILC process. The uniformity of MILC TFTs is resulted from the process uniformity: the thin film deposition and thermal treatment conditions in MILC processes are even over the whole substrate.

6.2.2 Scaling effects

Fig. 6-8 shows the extracted parameters (a) and output characteristics (b) of devices with different dimensions but the same W/L ratio of 0.5. Devices with large dimensions show similar behavior and their curves are close to each other. However, smaller devices are quite different.

Bulk MOSFETs and SOI transistors exhibit short channel effect (SCE) when the devices are scaled down to the sizes of submicron [63, 68]. However, for thin-film transistors, SCE occurs when the channel length downscales to a few microns [107, 123- 128].

Two factors favor the current conduction in TFTs with shorter channel. Firstly, there are fewer grains and grain boundaries in a smaller device, in favor of the carrier transportation because there are less carrier scattering events

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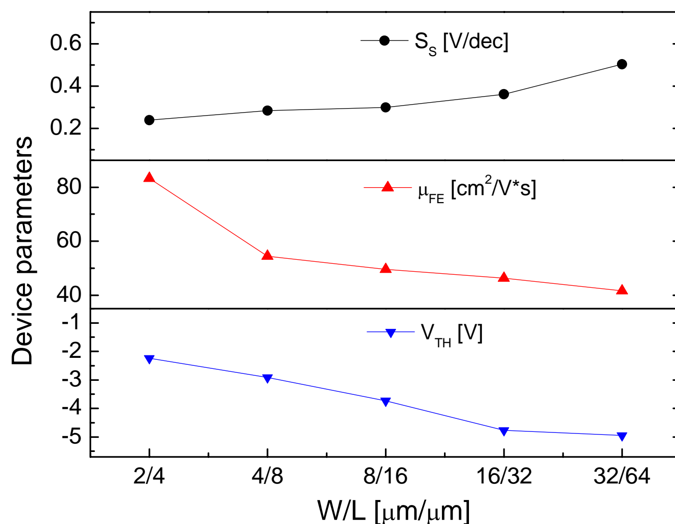
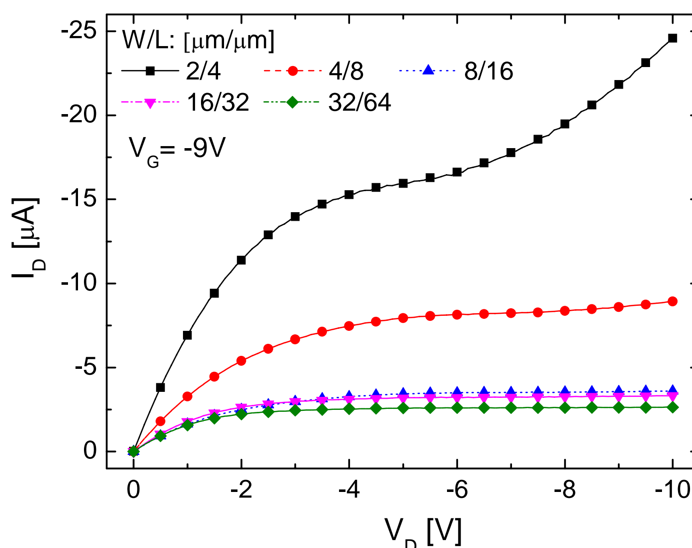
caused by GB barriers, which increases the device transconductance. Secondly, under a certain drain bias, the electrical field intensity is stronger in devices



(a)



(b)

Fig. 6-8 Device parameters (a) and output characteristics (b) of p-channel TFTs with different dimensions but the same aspect ratio of *W/L*=0.5

with shorter length. This stronger field increases the probability for impact ionization, which increases carrier density in the channel and the generated

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carriers redistribute the electric field along the channel, lowering the barriers at grain boundaries [124]. These two factors improve the device performance, by lowering the V_{TH}, S_S, and increase μ_{FE}, as shown in Fig. 6-8 (a).

However, there is an adverse effect by SCE, namely the kink effect, as shown in Fig. 6-8 (b). The peak electric field has been reported to be exponentially dependent on the reciprocal of the channel length [123]. So the peak electric field in the device with L=4μm is much stronger than those of the rest devices. At a certain field intensity, avalanche induced carrier multiplication occurs [127], and channel current will increase significantly. The I_D-V_D curve of TFT with W/L=2 μm / 4 μm illustrate this phenomena. This current increase is observed as indicated by the flexion of the I_D-V_D curve of the device with W/L=2 μm / 4 μm.

Based on the above discussion about SCE, higher leakage current is expected for TFTs with shorter channel lengths, as has been reported for SPC TFTs [125, 129]. However, this does not apply for our MILC TFTs fabricated. As shown in Fig. 6-9, the ON current of the devices increase as the channel length decreases. This is in agreement with the above discussions on SCE. However the leakage current decreases as the channel length scales down, in both high and low gate drain bias region. Devices with shorter channel lengths less than 4 μm exhibit improvement on both ON and OFF current compared with devices with large width. Obviously the suppression on I_{OFF} is not in agreement with and can not be explained by SCE. The MILC process should be responsible, as will be explained below.

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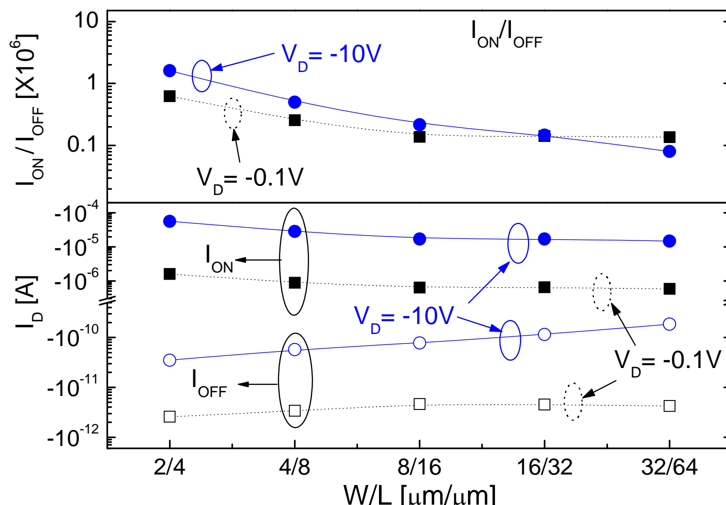

Fig. 6-9 The ON and OFF current of MILC devices with various sizes

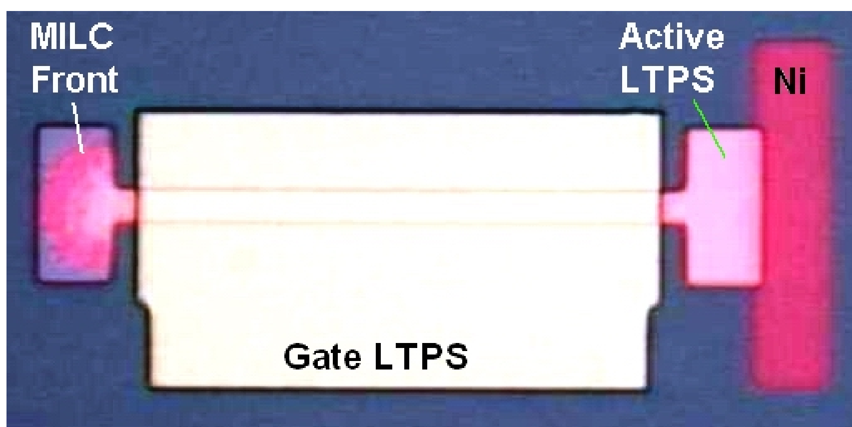

Fig. 6-10 Optical micrograph MILC processed active island, in a device with single side Ni source, and *W*/*L*= 4 μm / 64 μm

The MILC lengths have exceeded the length of the largest device and all device channels have been fully MILC crystallized, as is demonstrated by Fig. 6-10, which shows a TFT with the longest channel. The bright color in Fig. 6-10 indicates the MILC LTPS film and the MILC front can be clearly observed at the other end where no Ni is in contact with the initial a-Si film.

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However, difference in the crystallization quality of the LTPS film along the TFT channel is expected, since different locations have experienced different MILC annealing time (varying from a few to near 50 hours, for the left and right side of the channel). Since the distance from the Ni source to the channel is the same for every device, the active LTPS of shorter channels has experienced longest annealing time, which improves the LTPS quality. As a result, devices with smaller lengths are expected to exhibit better performance, including lower I_{OFF}, since TFT performance is strongly dependent on the LTPS film quality.

6.2.3 The geometric effect of Ni patterning

Yuen *et al.* have observed that the MILC grain growth directionality and uniformity are greatly dependent on the relative position and the shape of the Ni source origin [101]. In their experiment, a layer of LTO was deposited on the original a-Si film. Ni lines of different sizes were made in contact with a-Si through openings of the LTO. For a very long line of Ni, the grains in the middle part grow in a direction perpendicular to the Ni line. Grains at the ends of the line will divert from the direction of the grains grown from the middle part of the Ni origin. The grains at the Ni line ends are smaller than those in the centre position. For a shorter line of Ni, the grains will divert from the perpendicular direction. And unlike long Ni line patterns, the grain size at the end position of a short line is not necessarily smaller than that at the center position [101]. Based on this Ni pattern dependence of grain growth, it is expected that the pattern of the Ni source influences device behavior. In this

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chapter, two types of Ni source pattern, namely, line and oval shapes, are investigated.

Fig. 6-11 schematizes the shape and relative location of the Ni source and the devices. The line-shaped Ni overlaps the a-Si island (not necessarily the channel width) by 7 μm at both ends. The oval shape is 4 and 8 μm in its short and long axes respectively. The TFTs with line- and oval-shaped Ni sources are called L-TFT and O-TFT, respectively. The L-TFTs and O-TFTs are located adjacently on the same substrate to make sure that they experience the same thermal MILC process. The angle α in the figure is to be introduced below.

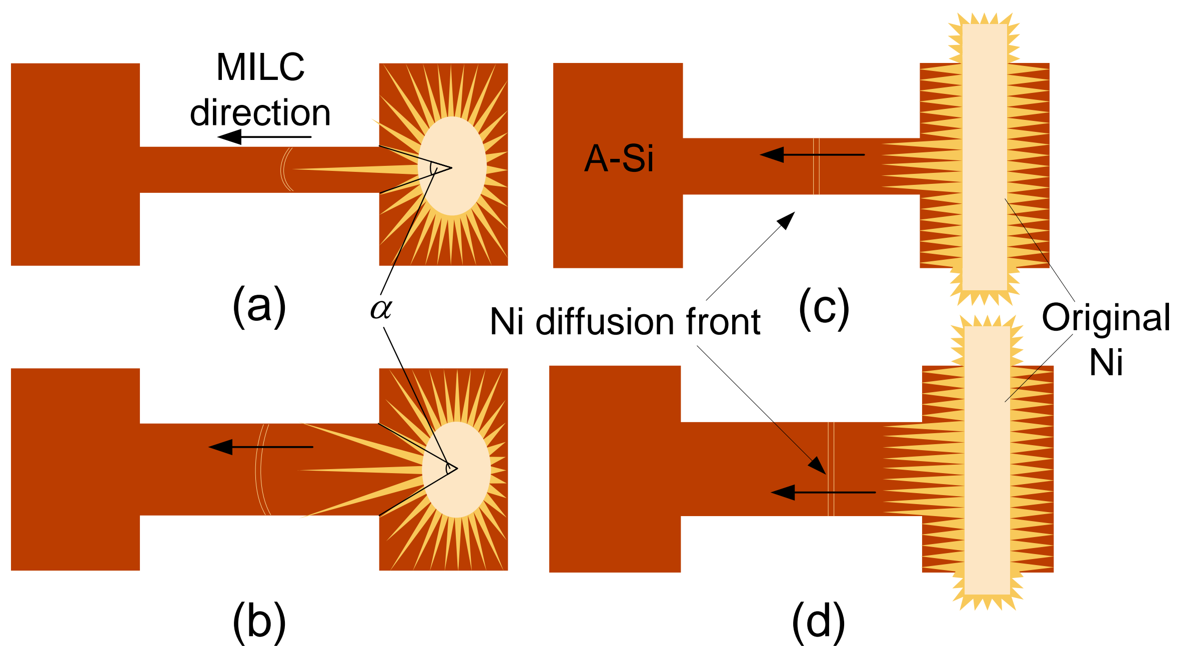

Fig. 6-11 Schematic showing the Ni source pattern and its diffusion effects

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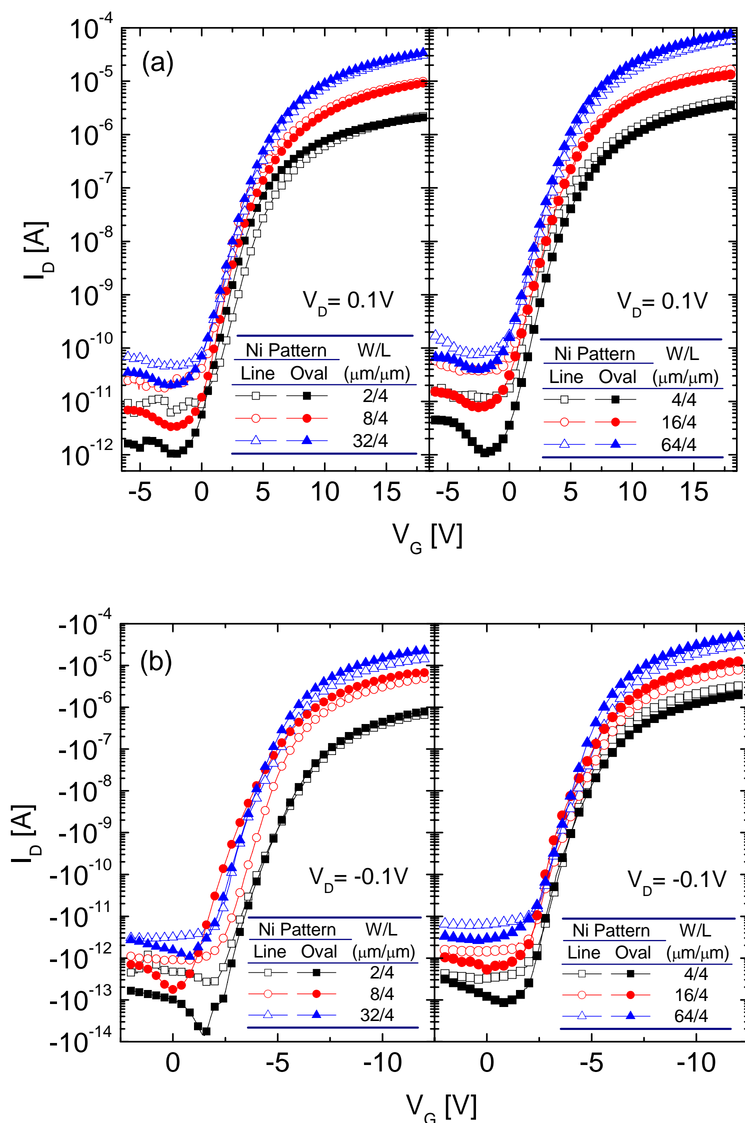

Fig. 6-12 The effects of Ni source pattern on device performance: Line vs. oval pattern. (a) n-TFTs, (b) p-TFTs.

Table 6-2 Ni pattern dependence of MILC n-channel TFTs

Parameters \ Devices	W/L=2μm/4μm		W/L=32/μm/4μm		W/L=64μm/4μm	
	Line-Ni	Oval-Ni	Line-Ni	Oval-Ni	Line-Ni	Oval-Ni
V_{TH} (V)	3.86	3.10	3.98	3.65	3.90	3.60
μ_{FE} (cm^2/V·s)	62.10	53.29	54.49	58.25	50.72	64.68
S_S (V)	1.17	0.97	1.13	1.05	1.17	1.08
I_{OFF} (×10^{-12}A)	6.07	1.02	43.8	20	74.5	39.5
I_{ON}/I_{OFF} (×10^5)	3.66	20.46	6.96	16.90	7.85	19.2

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Table 6-3 Ni pattern dependence of MILC p-channel TFTs

Parameters \ Devices	W/L=2μm/4μm		W/L=32/μm/4μm		W/L=64μm/4μm	
	Line-Ni	Oval-Ni	Line-Ni	Oval-Ni	Line-Ni	Oval-Ni
V_{TH} (V)	-5.67	-5.58	-5.03	-4.66	-5.27	-4.84
μ_{FE} (cm^2/V·s)	44.97	54.10	72.40	79.64	54.30	85.97
S_S (V/dec)	0.67	0.44	0.45	0.57	0.54	0.56
I_{OFF} ($\times 10^{-13}$A)	2.57	0.14	21.5	10.6	60.4	26.4
I_{ON}/I_{OFF} ($\times 10^6$)	2.58	56.7	8.88	21.42	5.02	18.48

Fig. 6-12 (a) and (b) show the transfer characteristics of the n-channel and p-channel TFTs respectively, for both L- and O-TFTs with varied channel widths of 2, 4, 8, 16, 32 and 64 μm, but fixed channel length of 4 μm. Table 6-2 and Table 6-3 tabulate the device paremeters extracted from Fig. 6-12. It can be seen from Fig. 6-12, Table 6-2, and Table 6-3 that, the O-TFTs exhibit better performance: (1) I_{OFF} is significantly reduced for O-TFT. (2) The on-state current (I_{ON}) of O-TFT is, on average, similar to or higher than that of the L-TFT. As a result, the I_{ON}/I_{OFF} ratio is improved by about half of an order. (3) The enhancement on the I_{ON} /I_{OFF} ratio of O-TFT is more prominent for small device widths. For wider devices, the improvement is still observable but less prominent. It is noted that, the I_{ON}/I_{OFF} ratio of p-channel O-TFT with W/L=2 μm/4 μm is distinctly larger than that of n-channel O-TFT, which is probably due to that, when the device dimension is comparable to the grain sizes, more obvious statistical distribution of TFT properties can be observed [130]. Other device parameters, including V_{TH}, S_S, and μ_{FE} were found comparable for L- and O-TFTs.

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The geometry effect of Ni source can be interpreted by the MILC behavior. As illustrated in Fig. 6-11 (c) and (d), for a line-shaped Ni source, the MILC direction (Ni diffusion direction) in the middle of the Ni source is perpendicular to the line source, although it bends near the ends of the line [101]. In the case of an oval-shaped Ni source, within a certain distance away from the Ni source, Ni diffuses approximately along the normal direction to the Ni boundary. This behavior affects the Ni concentration and the grain/grain boundary density of the LTPS in the channel.

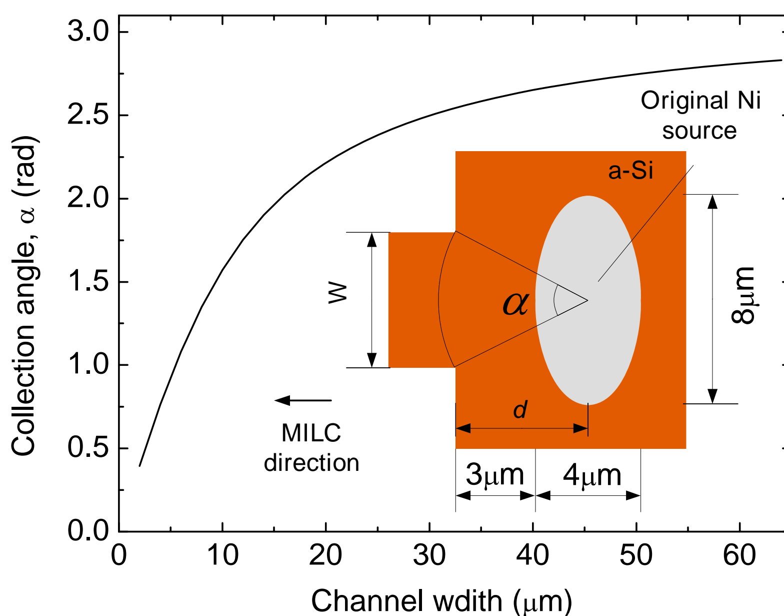

Fig. 6-13 The collection angle as a function of channel width. The inset shows the relative location of the Ni source to the channel.

For line-shaped Ni source, the Ni collected by the channel is proportional to the channel width [Fig. 6-11 (c) and (d)]. For oval-shaped Ni source, the amount of Ni capable of diffusing through the channel is reduced. As illustrated in Fig. 6-11 (a) and (b), some of the diffusing Ni will be blocked from diffusing into the channel region. As schematized in Fig. 6-11 and Fig. 6-13, the angle α,

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denoting the "collection angle", is introduced to represent the amount of Ni (contributing to the MILC process in the channel) collected by the channel. Approximately, for round or ellipse-shaped Ni source, the collection angle α can be written as

$$\alpha = 2\arctan(\frac{W}{2d})$$

where W is the TFT channel width, d is the distance between the center of the Ni source and the channel. Fig. 6-13 shows the collection angle as a function of the channel width using the experimental parameters of d = 5μm and W = 2 to 64μm. It can be seen from Fig. 6-13 that, the collection angle (Ni concentration in the channel) varies more significantly when the channel width is small, indicating the device performance as a function of channel width should vary more for smaller width devices, which is clearly reflected by the leakage current in Fig. 6-12 and Fig. 6-14.

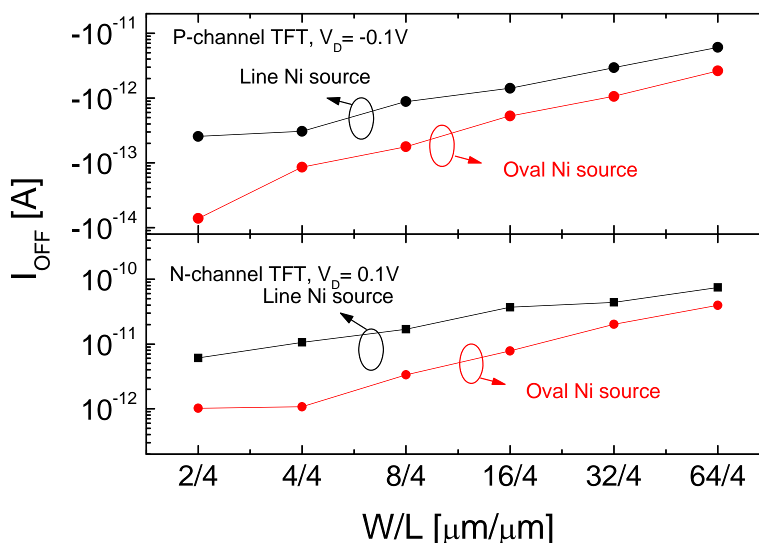

Fig. 6-14 Leakage current dependence on device widths

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The grain/grain boundary density in the channel differs for line- and oval-shaped Ni sources as well. For a line-shaped Ni source, the number of grains inside the channel is proportional to the channel width. For oval-shaped Ni source, the diffusion of Ni is along the radial directions of the oval. Compared to the line-shaped Ni source, the grain density in channel reduces faster with the reduction of channel width for oval-shaped Ni source, since less Ni diffusion leads to less nucleation sites. As has been discussed in our previous report, MILC is a diffusion and scattering process [131]. Less Ni diffusion introduces less scattering events for the crystallite growth, and thus larger grains can form. As a result, for devices with the same channel width, especially for smaller channel width, there are fewer grains and grain boundaries in the channel for O-TFTs than L-TFTs. It is worth mentioning that, although the grains are not perpendicular to the channel length direction, it is still meaningful that more grains/grain boundaries will render worse device performance. For narrower channels, with a smaller collection angle, the grain/grain boundary density is smaller, and hence, the leakage current is prohibited more, compared to wider channels.

Lastly, it is worth mentioning that, no obvious difference in the crystallization rate for L-TFTs and O-TFTs is observed.

6.2.4 Effects of SLTO and GLTO

As discussed in the fabrication of MILC TFTs, there are two types of LTO processes in MILC: SLTO and GLTO. Devices behave differently with different kinds of LTO.

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Fig. 6-15 shows the device transfer characteristics of p-channel devices with SLTO and GLTO, respectively. Device parameters extracted are listed in Table 6-4. Obvious differences can be observed, among which we notice: (1) The most significant is the difference in their device threshold voltages. The V_{TH} values of SLTO devices are 1 to 2 volts lower in absolute value than those of GLTO devices. (2) The sub-threshold swing S_S for SLTO is lower than that of GLTO by 0.1 to 0.36 V/dec. (3) The curves in the above threshold region are quite close to each other for the two kinds of devices, with the SLTO ones being a little higher. The leakage current is similar. The device performance disparity suggests different gate dielectric quality, since this layer is the main difference in the fabrication of the device in comparison, which should be responsible for the disparity in device performance.

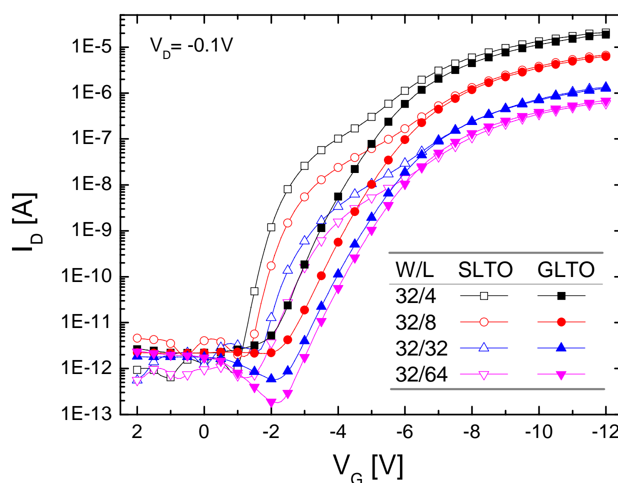

Fig. 6-15 The effects of LTO process sequence in MILC on device performance.

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Table 6-4 Comparison between device parameters of TFTs by GLTO and SLTO

W/L — Devices — Parameters	32μm/4μm		32/μm/8μm		32μm/32μm		32μm/64μm	
	GLTO	SLTO	GLTO	SLTO	GLTO	SLTO	GLTO	SLTO
V_{TH} (V)	-5.02	-3.77	-5.57	-4.52	-5.69	-4.95	-5.65	-4.95
μ_{FE} (cm^2/V·s)	71.93	74.92	52.85	58.17	43.54	48.91	46.22	41.59
S_S (V)	0.54	0.28	0.66	0.30	0.65	0.38	0.61	0.51
I_{ON}/I_{OFF} ($\times 10^6$)	8.65	33.42	2.93	3.64	2.18	2.40	3.74	1.06

In GLTO process, the Ni above the gate a-Si will quickly diffuse to the GLTO layer, since the Ni is a fast diffuser in Si and the gate a-Si layer is quite thin (300 nm). However, Ni diffusion does not reach the interface between gate dielectric and the channel LTPS film, because otherwise the active a-Si will be crystallized due to the Ni diffused through the LTO layer. This is confirmed by the characteristics of device for which no MILC opening is designed. As shown Fig. 6-5(a), the device without MILC opening on the LTO layer but fabricated by GLTO process exhibits a-Si TFT behavior, with a mobility as low as 0.29 cm^2/V·s. For SLTO, the gate dielectric layer is newly deposited after the MILC annealing. So less Ni contamination is expected in gate dielectric in a SLTO process. The difference in Ni contamination level is the main reason that results in the difference in V_{TH}.

In MILC process, difference of Ni chemical potential between the a-Si/$NiSi_2$ interface and c-Si/$NiSi_2$ interface is the main driving force for Ni diffusion and there is a higher density of Ni at the diffusion front (Section 5.2.2.2). The crystallite growth in most cases will terminate when it reaches the channel LTPS/GLTO interface. This means when Ni diffusion to the

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LPTS/GLTO interface, it stays there in most cases. The accumulation of Ni at the interface degrades the crystallization quality at the interface, increasing the density of trap states. In contrast, the Ni accumulated at the interface is removed along with the masking SLTO layer in SLTO process. So it can be concluded that GLTO process results in higher density of trap states, which are spatially distributed at the interface between LTO and LTPS film. The increased trap states reduce the sensitivity of free-carrier density to the gate bias, leading to poor turn-on performance and higher S_S value.

6.3 Summary

High performance devices have been successfully fabricated. The mobility is up to about 110 $cm^2/V \cdot s$; threshold voltages are -3 ~ -6V and 3 ~ 4V for p- and n-channel TFTs respectively; ON/OFF current is up to over 10^7. Scaling effects are investigated, which suggest different crystallization quality at different channel location. The geometry of Ni source is found to play a role in affecting LTPS films. For the first time, oval-shaped Ni source pattern is observed to achieve better device performance than conventionally line-shaped patterns, mainly by suppressing leakage current. For the first time, collection angle, a parameter to represent the amount of Ni diffusion in to the device channel region, is proposed to interpret the improvement. Different MILC process sequence, namely SLTO and GLTO processes are discussed. SLTO proves to be superior in achieving better device performance, mainly lower V_{TH} and S_S, indicating less contamination in the gate dielectric and better interface between the gate dielectric and the channel LTPS films.

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Chapter 7 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusions

LTPS TFT technology is the most promising technology for implementing large area microelectronics with moderate performance at reasonable costs. For circuit applications, a limited device parameter distribution is desirable, which means a high degree of uniformity over the substrate area. Since thermal treatment is capable to achieve large area uniformity, thermal crystallization techniques for LTPS films deserve further study to improve the device performance and minimize device parameter distribution. In this thesis, thermal crystallization processes, including SPC and Ni MILC process, are investigated. Devices are fabricated using these two annealing methods and high performance devices are obtained.

SPC annealing of a-Si is systemically studied. LTPS film sheet resistance variation versus annealing duration is for the first time investigated. The observation suggests the transition between annealing stages, defined in this chapter as primary and secondary crystallization. A little more than 6 hours of SPC annealing duration is suggested as the optimized value for practical SPC process, in terms of crystallization effect, cost and productivity. 560 °C is determined as the minimum temperature for practical SPC annealing. Secondary crystallization stage is proposed to be the stage where SPC process could conclude for effective crystallization in a reasonable duration. Devices

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are fabricated using SPC process. Good performance is obtained, proving the capability of SPC process for certain low demanding, low cost applications.

Investigation on MILC and FALC are presented. Dendritic lateral growth is observed and interpreted using a proposed growth and scattering mechanism. Different lateral crystallization behavior for MILC and FALC is observed. Polarity and current Joule heating effects are also presented. *In situ* resistance measurement method is for the first time applied in the study of MILC and FALC process. Resistance between Ni sources degrades exponentially during a MILC or FALC process.

Numerical analysis proves that grain boundaries are detrimental to device performance and the variation of grain boundary number along the TFT channel results in significant device fluctuation. FALC was utilized to obtain large grains. The largest grain achieved was over 100 μm, which is the largest grain size by MILC so far. In FALC, polarity dependence of lateral crystallization length is investigated and is, for the first time, interpreted by Joule heating.

MILC was used to successfully fabricate TFTs both in n- and p-channel. The performance is also comparable to reported high performance MILC TFTs, with ON/OFF current ratio over 10^7 is obtained without special structures such as LDD to minimize leakage current, V_{TH} in the range of -4.5~6V and 3.6~3.98V for p- and n-channel TFTs respectively, and mobility in the range of 45~86 and 50~110 $cm^2/V*s$ for p- and n-channel TFTs, respectively. Effects of process and device structure are discussed. The geometry of Ni source plays a role to affect the device property in MILC. Oval-shaped Ni source was found to render lower leakage current than conventional line-shaped sources. In MILC

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process, a sacrificial oxide layer to screen Ni from channel a-Si film is beneficial to device, with small S_S and V_{TH} values.

Among the studied thermal crystallization technologies, MILC is most promising. SPC takes too much time and is not practically feasible in mass manufacturing. Only when the trade-off between crystallization effects and productivity is optimized, can SPC find its applications in manufacturing. FALC has much higher lateral crystallization rate. However, it increases process complexity by applying the electric field, especially for large substrates. Special electrodes and conducting wires are needed to avoid contamination from the electrodes to the process chamber and the substrates. FLAC is premature to be adopted by industry. MILC combines the advantages of SPC and FALC. The crystallization rate (>1.6 μm/hour) is acceptable and the mobility of up to 110 $\mu m^2/V*s$ is capable of circuit integration. And, process engineering (e.g. forming oval- instead of line-shaped Ni source, adding LDD structure) can further improve the performance of MILC TFTs.

In short, this thesis explores the capability of thermal crystallization for LTPS films and proves the capability of thermal annealing to obtain reasonably good device performance, approaching the laser crystallization quality but with controlled uniformity.

7.2 Recommendations for further studies

To achieve high performance TFT circuits on glass substrates, much improvement in device is still desires. Based on the investigation of the thesis, some future work is suggested in the following.

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Based on the growth and scattering mechanism, a diffusion limit structure should be applicable to suppress the density of Ni silicide precipitates and the grain sizes may be further enlarged, due to lower probability of scattering. This can be achieved in two ways: (1) based on the investigation on Ni pattern effects (Section 6.2.3), it is worth engineering the Ni source geometry and it location with respect to the channel region, to achieve an optimized configuration for better MILC result and device performance; (2) a special device structure, such as a necking-down area may be applied to serve as a filter in order to suppress the density of Ni silicide precipitates and enlarge the grains.

In order to apply the large, continuous grains formed by FALC process, the fabrication of FALC LTPS TFTs, using suitable, directly applied electric field between Ni sources, can be conducted. Better device performance is expected. And the device performance should be dimension dependent, with respect to the crystallized grain sizes. Thus the scaling effects of the devices are worth to be investigated.

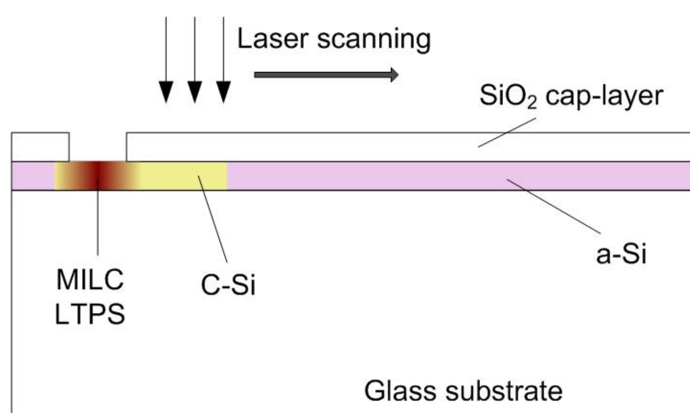

Fig. 7-1 Schematic for guided laser-MILC

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High quality LTPS film is possible by direct combining MIC/MILC with laser annealing [132, 133]. One more elaborate scheme is possible as shown in Fig. 7-1. A cap layer is coated onto the a-Si film. Ni is deposited on the cap layer/a-Si stack and contacts a-Si layer through openings on the cap layer. A quick MILC process is then conducted to form a region of LTPS films, which serves as seeds for the subsequent laser lateral crystallization. The LTPS region formed from MILC process will guide the lateral laser crystallization to generate a lateral epitaxial mode of crystalline growth, producing high quality LTPS films with large grains. The laser scanning will be in such a direction that the active region will be located in the guided lateral crystallized film.

Regarding the device fabrication, MILC process can be further engineered. Based on the discussion about the geometric effect of Ni patterning, the size of the oval Ni pattern is expected to have an effect on device property as well, since the ratio between size of oval pattern and the width of the device channel influence the Ni diffusion paths. Besides, as indicated by the discussion on the device scaling effect, different lateral crystallization quality is expected along the MILC length. Thus the distance from the Ni source to the channel, should also be further engineered. Besides, based on the discussion the MILC behavior for devices with a oval-shaped Ni source origin, it is reasonable to expect a much different MILC process if the channel width is downscaled to some extend (i.e. sub-micron dimensions). It is worth to study devices with narrow channel widths (say, sub-micron scale) and oval or round shaped Ni source.

There have been lots of reports on studies of TFT devices, such as the leakage current [134, 135] and hot-carrier effects [136, 137]. However, circuit

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blocks built from TFTs are much less reported. TFT devices and circuits are different from both bulk silicon MOS devices and silicon on insulator (SOI). So TFT circuits have their specific properties and are worth further study, which is crucial to realize TFT based SOG. Taking the scaling effects into consideration (Section 6.2.2), design and design rules specifically of MILC TFT circuits need to be created to approach the implementation of TFT based microelectronic systems on glass. The circuits may include: (1) device characterizing units such as inverters, ring oscillators; (2) basic circuit building cells such as simple logic gates, clock signal dividers; (3) building blocks for display driving circuitry, such as shift registers, level shifters and digital/analog converters, etc.

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Appendix A SPC LTPS TFT PROCESS STEPS

Step	Step Name	Description	Remark
0	Starting Wafer	N <100>, 1-30 Ω-cm	
1	INIT OX, 5000 Å	Wet oxidation at 1000 °C 95 min, Pyrogenic steam, 1000 °C 5 min. Dry Oxidation , 1000 °C 5 min. Anneal , 1000 °C	
2	LPCVD a-Si, 1600Å	250 mTorr, 70 min, 550 °C, SiH_4	Part of the wfrs
3	LPCVD a-Si, 900 Å	250 mTorr, 40 min, 550 °C, SiH_4	Part of the wfrs
4	SPC	72 hours at 600 °C, N_2	
5	Active island formation		
5a	PR Coat	AZ1813	
5b	Align/Expose	Island Mask	
5c	Develop/Hardbake		
6	Island Etch	RF plasma etching. Gases: Br, Cl_2, He.	
7	PR removal	O_2 Plasma etching and Piranha clean (Nano PR strip)	
8	Gate Oxide UD-TEOS 700Å	TEOS : 280 mG/min Press : 300 mTorr Dep. Time : 21 min	Part of the wafers

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9	Gate Oxide UD-TEOS 1000Å	TEOS : 280 mG/min Press : 300 mTorr Dep. Time : 30 min	Part of the wafers
10	Gate Poly-Si LPCVD Poly Si 2500Å	Gas : SiH_4 Pressure : 300 mTorr Temperature: 610 °C Dep Time : 60 mins	
11	Poly Si Densify and Doping Spec: Rs=10-12 ohm/sq	POCL3 Doping at 600°C Post doping clean (Remove phosphorous-rich oxide) 20:1 HF dip, dewet	
12	Gate Poly-Si patterning		
12a	PR Coat	AZ3100. Softbake : 110 °C, 90 sec	
12b	Algn/Expose	GPoly Mask	
12c	Develop/Hardbake	Hard-Bake : 120 °C, 120 sec	
13	Gate Poly Etching	Plasma PolySi Etch RF plasma etching. Gases: HBr, Cl_2, He	
14	PR Removal	O_2 Plasma etching and Piranha clean (Nano PR strip)	
15	N+ SD Implant	Arsenic, 120Kev, 7° tilt, +4 quarter implant, Dose = 5E15 cm^{-2}	
16	Dopant Activation	300 min, N_2=6 SLM, Temperature =600 °C	
17	BPSG Deposition	Target: UD-TEOS:1000 (+/-150) Å BP-TEOS:6500 (+/- 250) Å	

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17a	Layer 1: LPCVD UD-TEOS	TEOS=280 mG/min
17b	Layer 2: LPCVD BP-TEOS	Spc: 4% P and 4% B
18	Contact opening	
18a	PR coat	
18b	Align/Expose	CONT Mask
18c	Develop & hardbake	
19	Contact Etch	BOE : 2min. Rinse and Hardbake program to dry.
20	PR Removal	O_2 Plasma and Piranha Nano PR clean
21	Metal1 Deposition	Sputter Deposition Ti/TiN/AlSiCu = 300/300/8500Å
22	Metal1-Patterning	
22a	PR Coat	
22b	Align /Expose	M1 Mask
22c	Develop	Hard-Bake : 120 °C , 120 sec
23	Metal1 Etch	RF Plasma Etch (200W), Pressure=275mTorr BCl_3=75 sccm, Cl_2=32 sccm, N_2=25 sccm Over Etch 10 sec after endpoint
24	PR Removal	O_2 Ashing, End point + over etch, Cascade Rinse, QDR Dry
25	Metal1 Alloy	At 425 °C. N_2=6 SLM, N_2=100 sccm

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Appendix B DESCRIPTION OF THE LAYOUT

B.1 Devices

There are a few device matrices. In each complete device matrix, the devices are of the same type but their sizes vary. There are boarders (M1/M2 layer) between deferent matrices. The dimensions available in a matrix are 2, 4, 6, 8, 10, 12, 16, 32, 64 and 128 μm. shows one complete device matrix.

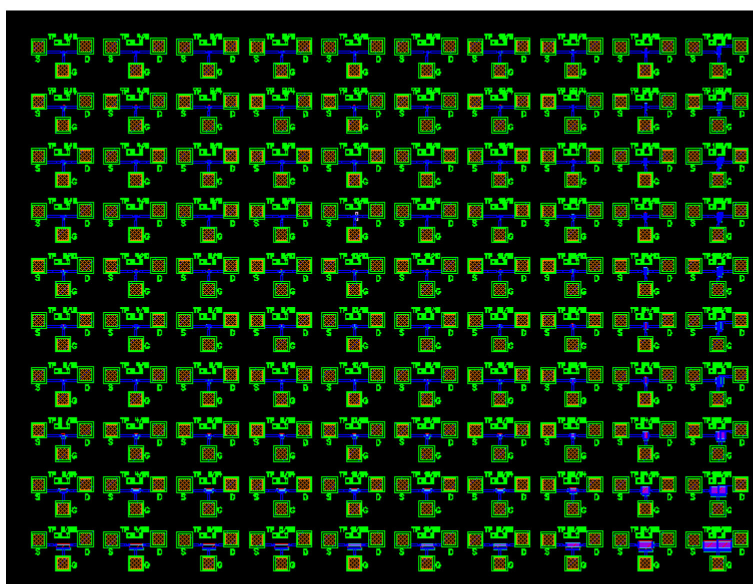

Fig. B-1 Layout of one device matrix

There are a few device types, differentiated by the locations of the Ni patterns for MILC with respect to the device structures.

- NBM: No Ni patterns for MILC. The device is not MILC crystallized.

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- CM_D: Ni patterns are located on drain side only. So the MILC process initiates from device's one of the drain/source side and proceeds to the the other end.

CMSD: Ni patterns are located at both device 'DRAIN' and 'SOURCE' side. The MILC process initiates from both sides and proceeds towards the center.

Fig. B-2 shows a device in CM_D type matrix with the layer legend.

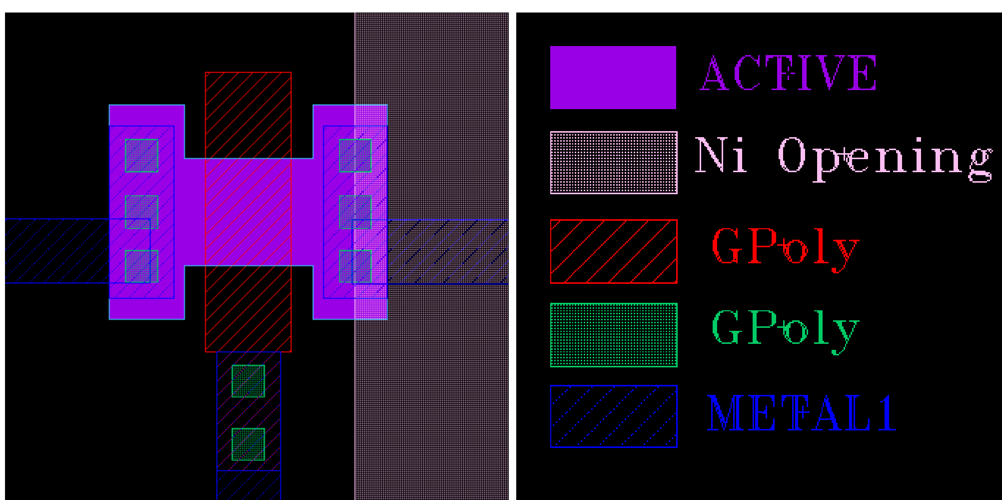

Fig. B-2 A TFT (10μm/8μm) in a CM_D type matrix.

B.2 Testing structures

Testing structures are mainly for process and process monitoring purposes, including alignment marks, etching monitoring cells, sheet resistance measurement structures, and contact chains.

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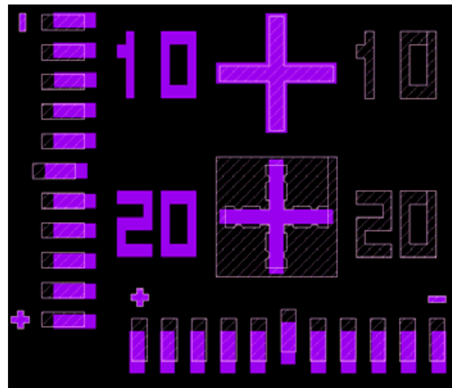

Fig. B-3 Alignment mark between ACTIVE and Ni Opening

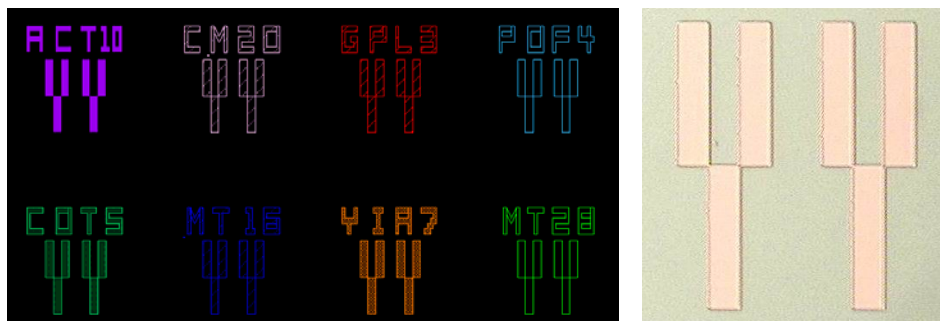

Fig. B-4 (a) Etch cells and (b) a processed etching cell (layer ACTIVE).

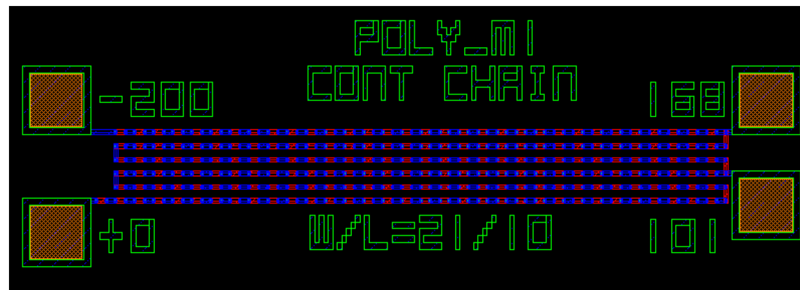

Fig. B-5 Contact chain between GPoly and METAL1.

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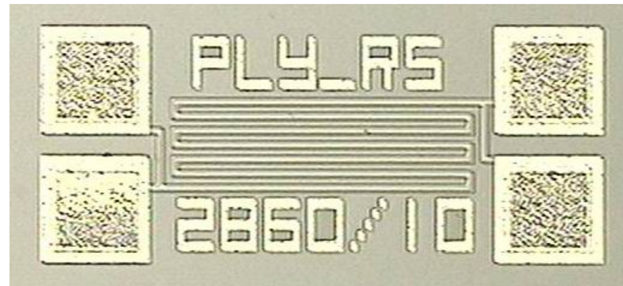
(a)



(b)

Fig. B-6 Sheet resistance measurement structure for layer GPoly. (a) Designed layout; (b) Fabricated pattern, after METAL1 and passivation.