Wideband Low Noise Amplifiers Employing Noise Cancelling Technique

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2018

Statement of Originality

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Chapter 3 is published as H. Yu, Y. Chen, C. C. Boon, C. Li, P.-I. Mak, and R. P. Martins, "A 0.044-mm2 0.5-to-7-GHz resistor-plus-source-follower-feedback noise-cancelling LNA achieving a flat NF of 3.3 ± 0.45 dB," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 66, no. 1, Jan. 2019.

The contributions of the co-authors are as follows:

- Prof Boon provided the tape-out support and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr Chen, Prof Mak, and Prof Martins.
- I co-designed the study with Dr Chen and performed all the laboratory work at the School of Electrical and Electronic Engineering. I also analyzed the data.
- All circuit simulation, including layout design and postlayout simulation, was conducted by me in IC Design Lab 1.
- Li Chenyang assisted in the collection of the measurement data.
- Dr Chen provided guidance in the interpretation of the measurement data.

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Acknowledgement

First of all, I need to thank my supervisor, Prof. Boon, for his help and full support over all these years. He always encourages his students to explore new ideas and to come up with novel designs. He is also a true gentleman and is patient with the mistakes that I made.

Next, I would like to express my appreciation and respect to Prof. Chen Yong, who is now with University of Macau. He has spent tremendous effort and time on guiding me through this journey of thorns. The experience of working with him is a priceless asset in my life.

I would thank my colleagues, Wang Peng, Kong Lingshan and Li Chenyang, who have been my support and companion. The discussions I had with them were very helpful for my research works.

Last but not least, I want to thank my mother for her financial support so that I can continue my pursuit for this doctoral degree. She is an amazing woman who is always my comforter.

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Summary

Currently, wideband receiver had become a highly popular research topic because of its capability to support both high-speed communication as well as multi-standard integration. Ultra-wideband (UWB) wireless transmission standard was established by Federal Communication Commission (FCC) to support high-speed transmission using bandwidth from 3.1 – 10.6 GHz. Software defined radios (SDRs) have enabled multistandard wideband receiver, which covers multiple wireless standards distributed over sub-6-GHz bands, such as WiFi, GSM and Bluetooth. The first building block in such wideband receivers, wideband low-noise amplifier (LNA), is critical to the performance of the entire receiver chain.

Noise cancelling (NC) is an interesting technique in wideband LNA design. It breaks the trade-off between input matching and noise performance of LNA. By adding two feedforward paths using two auxiliary amplifiers, the noise of input transistor is cancelled at output. The objective of this research is to explore this technique and propose novel NC LNA architectures that exploit improvements in gain, noise figure and linearity. These architectures are verified through simulation as well as silicon measurements.

A wideband resistive-feedback NC LNA with an additional source-follower-feedback (SFF), which improves both gain and NF, is presented. Fabricated in a 65nm CMOS process, the wideband LNA achieves a flat S_{21} of 16.8 dB, a flat NF of 2.87-3.77 dB and S_{11} below -10 dB over a 3-dB bandwidth of 0.5-7 GHz. It consumes a DC power

of 11.3mW from a 1.2-V supply and occupies an active area of only 0.044mm^2. Nevertheless, this LNA shows a mediocre IIP3 of -4.5 dBm, rendering the circuit vulnerable to intermodulation interference.

To address linearity issue in wideband application, a common-gate noise canceling LNA employing pMOS-nMOS complimentary pair as distortion cancellation is proposed. It is crucial for wideband LNAs to achieve high IIP3, preventing in-band intermodulation interference. Fabricated in a 65nm CMOS process, the wideband LNA achieves an S_{21} of 12.8 dB, a flat NF of 3.3-5.3 dB and S_{11} below -10 dB over a 3-dB bandwidth of 1-20 GHz. It shows an IIP3 larger than 2 dBm across the entire 19 GHz bandwidth and the highest measured IIP3 is 6.8 dBm.

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1. Introduction

1.1 Background and Motivation

The progress of semiconductor technologies has enabled the implementation of more complex systems on a single chip with cheaper price. The CMOS technology, initially exclusively used for digital application, is currently playing a significant role in analog and radio frequency (RF) circuit implementation due to its high transit frequency for high frequency application, area-efficiency for large-scale integration and capability for low-power design [1][2]. As a result, complicated system, i.e. a RF receiver, as shown in Fig. 1.1, including RF front-end, analog baseband, and digital baseband, can be realized on a single die through CMOS technology.

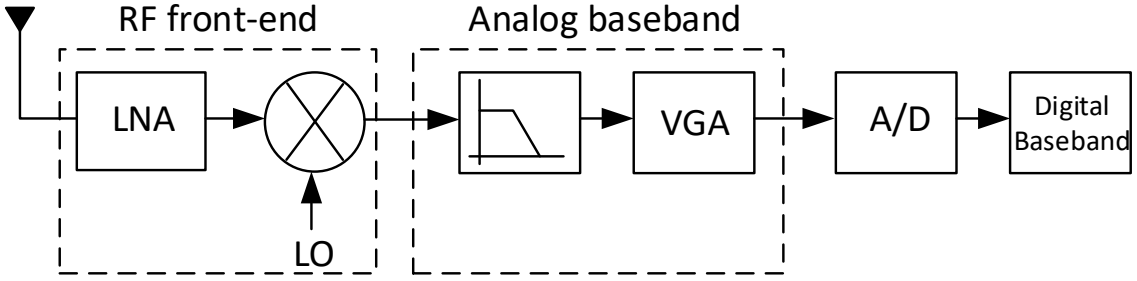


Fig. 1.1. A direct conversion RF receiver.

Nowadays, people are constantly looking for better connectivity, making the wireless communication market promising and profitable. In both industry and academy, tremendous work and effort is spent on RF receiver, a crucial component in wireless communication system. Among various kinds of receivers, wideband receiver has

attracted the attention of researchers and is considered for future radio [3]-[8]. There are two main reasons why wideband receiver becomes a popular RF application.

Firstly, wideband receiver can cover the multiple standards simultaneously [3]-[8]. Today's wireless devices like mobile phone communicate in various features like Global System for Mobile communication (GSM), Wireless Fidelity (Wi-Fi), Global Positioning System (GPS) and Bluetooth, all within a frequency range of 0.9-5.2 GHz. Conventionally, several individual receivers are required in the device to support all these features, causing the system to be power hungry, bulky and expensive to fabricate. Battery life, size and market competitiveness will thus be affected [9]. However, a wideband receiver caters all the features at the same time, since it operates across a wide frequency range. Therefore all the traditional RF receivers are replaced by a receiver, which saves power, area and cost, resulting in a low-power and low-cost system.

Table 1.1 Various standards used in a mobile phone [9]

Standards	GSM	Bluetooth	IEEE 802.11b	IEEE 802.11a	GPS
Freq (GHz)	0.9/1.8/1.9	2.4	2.4	5.2	1.2/1.6
Data rate (Mbps)	0.27	1	11	54	0.05
Access method	TDMA	TDMA	CSMA/CA	CSMA/CA	CDMA
Modulation	GMSK	GFSK	CCK, BPSK	BPSK, QPSK, 16/64 QAM	BPSK
TX power (mW)	2000	1/100	100	40	500,000
RX sensitivity (dBm)	-108	-70	-80	-82	-130

The second reason is that wideband receiver is capable of supporting higher transmission rate[3][4]. In 2002, Federal Communication Commission (FCC) set up the standard of ultra-wideband (UWB) for short-range and high-data-rate RF communication. The data

rate can be as high as 480 Mb/s and thus, large data like multimedia transmission can be completed within seconds. UWB is very suitable for wireless communication between computer and other electronic devices such as mobile phone, camera and projector as shown in Figure 1.2. The typical bandwidth for UWB system lies from 3.1 to 10.6 GHz, thus UWB receiver will need to have at least 7.5 GHz bandwidth to cover the entire bandwidth.

Fig. 1.2. UWB high-data-rate communication system.

Wideband low noise amplifier (LNA), which sits in the front position in a RF receiver chain, is a critical block. As the input of an LNA is usually connected to antenna or RF filter, an input matching of 50 Ω is required. However, tradition narrow band input matching techniques [10], which covers a range less than 1 GHz, is no longer valid in wideband LNA design. Proper bandwidth broaden technique is also required. The use of passive inductor is a convenient way to achieve wideband, however, over-dependence on inductors may occupy too much chip area, going against the initial intention of wideband

system, which is saving cost. Another method is to use a smaller size of transistor in design to reduce the gate capacitance, which is the major limitation to bandwidth. However, a smaller transistor results in smaller gain and higher noise. So careful consideration is required in designing the bandwidth. A flat noise figure across the bandwidth is also a challenge for wideband LNA design. Some wideband works achieves a low noise at certain frequency point, however, the noise figure increases fast with increasing frequency. Last but not least, the linearity of LNA is also important for wideband applications. As wideband system is more vulnerable to the intermodulation of nearby bands/frequencies, a good IIP3 is essential for wideband LNA design.

To sum up, wideband LNA is a critical block in CMOS RF wideband receiver for multi-standard or high-speed applications and it needs to meet stringent requirements such as sufficient bandwidth, flat and low noise figure and good input impedance matching across the bandwidth.

1.2 Objectives

The aim of this research is to develop new circuit structure and design techniques of wideband low noise amplifiers based-on Globalfoundries 65nm CMOS technology, which is a common and cost-effective process. The developed LNAs are to be designed with excellent input impedance matching, resulting in input return loss (S11) below -10dB across the entire wideband. The challenge of a flat noise figure across multiple gigahertz is also taken and studied in the process of developing these LNAs. A flat and sufficient gain, which is essential for a good design of wideband amplifier, is also to be achieved. Most importantly, proposed LNAs are to be able to break the trade-offs

existing in these key parameters in LNA design: input matching, gain and noise figure. Last but not least, linearity, which has more influence on wideband application than on traditional narrowband application, is to be improved compared to current arts.

1.3 Organization and Major Contribution of the Thesis

This thesis consists of five chapters and is organized as following:

In chapter 1, the background, motivation and objective of the research work are introduced.

In chapter 2, a detailed literature review on wideband low noise amplifier is presented. Different design approaches and circuit configurations are reviewed and their pros and cons are studied. The reason why noise-cancelling technique, which is a popular choice among current wideband design, is used in this work is emphasized. Possible improvement to the noise-cancelling technique is proposed.

Chapter 3 describes a noise-cancelling LNA utilizing a novel circuit structure by implementing a source follower feedback (SFF) in addition to traditional resistive feedback [11]. The introduction of SFF improves the gain and noise figure without compromising the input impedance matching. The design, analysis and measurement results of this work are discussed in detail. In this design, linearity performance, i.e. IIP3, is not optimized specifically, resulting in a mediocre IIP3 of -4.5 dBm. So the next work focuses to provide solution for IIP3 improvement.

In chapter 4, a 0.5 – 20 GHz noise cancelling LNA employing a novel triple path noise-cancelling technique [12] is presented. This work pushes the design limits and further

broadens the bandwidth of LNA up to 20GHz. A flat noise figure against frequency is also achieved. Moreover, due to the use of pMOS-nMOS complementary pair, this work shows an excellent linearity, i.e. IIP3. The design, analysis and measurement results of this work are discussed in detail.

Finally chapter 5 draws the conclusion for the thesis and proposes possibilities for future work.

Chapter 3 and chapter 4 are the major contributions of the thesis, where novel circuit designs are proposed to provide solution to meet the stringent requirements of wideband LNA, such as gain, noise figure and IIP3. Technical papers have been either published [11] or submitted for review [12] for these two works.

2. Literature Review

2.1 Fundamentals of Low Noise Amplifier

In a CMOS integrated RF receiver chain, the LNA is the first silicon circuit block since antenna is usually implemented as a discrete component on PCB board. In a commonly used direct conversion receiver, the output of LNA is often directly connected to a mixer, where signal is down converted to base band frequency. Due to its connection to the antenna, LNA need to have an input impedance matching with the output impedance of the antenna, which is usually 50 Ω. A good impedance matching ensures sufficient power is transferred from antenna to the amplifier. On the other hand, the input of following stage, i.e. mixer, conventionally is the gate of transistor, showing capacitive characteristics. Moreover, in wideband applications, it is preferable to design the metal connection between LNA and mixer as short as possible so that signal loss between the circuit blocks is minimized. This means that an output of LNA is almost directly connected to a capacitive load and an output impedance matching of 50 Ω for LNA is not always necessary. However, in the design of LNA as a circuit block, an output buffer is often added to achieve impedance matching for measurement purposes.

One key purpose of implementing LNA in a receiver is to amplify the desired signal while at the same time, to avoid the amplification of noise. In short LNA is crucial for the signal to noise ratio in a receiver chain. Therefore, LNA needs to boost the wanted RF signal with sufficient gain and suppress the noise with low noise figure. Intermodulation distortion handling ability of the LNA is also important. Two signal frequencies intermodulate with each other and may generate a frequency that interferences the desired

RF signal. The design consideration for the above mentioned LNA specifications are discussed in detail below.

2.1.1 S-parameters

It is known that a two-port network is popularly used in circuit design. To characterize a two-port network behavior, measured data of both transfer function and impedance function of the two-port network must be obtained. At low frequencies, Z, Y, H and ABCD parameters are used in the description of the two-port network. But at high frequency, these parameters cannot be measured accurately because the required short-circuit and open-circuit tests are difficult to achieve. Scattering parameters (S-Parameters), based on incident and reflected waves, are very useful in radio frequency range.

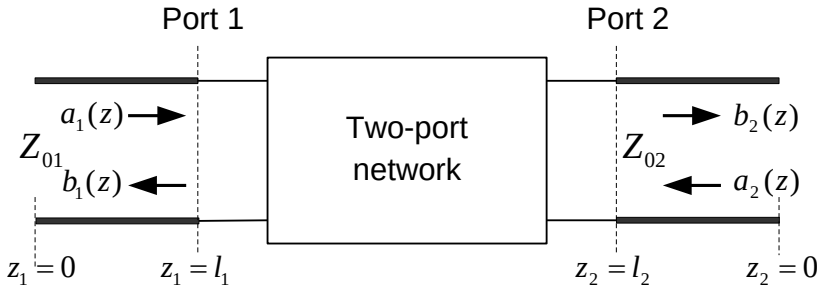


Fig. 2.1. A two-port network.

Figure 2.1 illustrates a two-port network, where a_1, a_2 are incident waves, b_1, b_2 are reflected waves. Their relation is expressed as:

$$\begin{bmatrix} b_1(l_1) \\ b_2(l_1) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1(l_1) \\ a_2(l_1) \end{bmatrix} = [S] \begin{bmatrix} a_1(l_1) \\ a_2(l_1) \end{bmatrix} \tag{2.1}$$

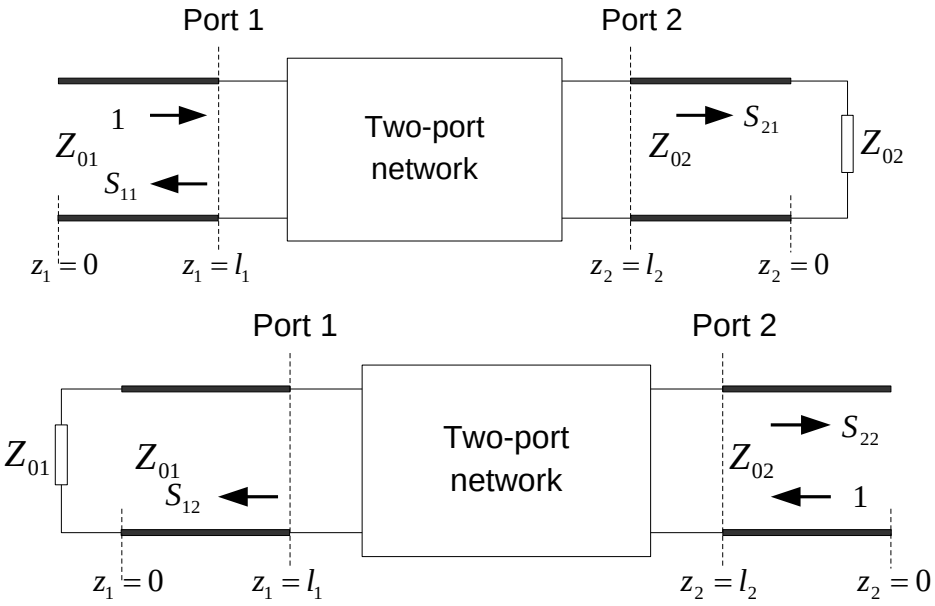


Fig. 2.2. Meaning of S-parameters.

The matrix $[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$ is called scattering matrix and the S-parameters can be calculated according to Figure 2.2 and Equations (2.2a) – (2.2d) [13][14]:

$$S_{11} = \frac{b_1(l_1)}{a_1(l_1)}\Big|_{a_2(l_2)=0}$$ = input reflection coefficient with matched output port; (2.2a)

$$S_{12} = \frac{b_1(l_1)}{a_2(l_2)}\Big|_{a_1(l_1)=0}$$ = reverse transmission coefficient with matched input port; (2.2b)

$$S_{21} = \frac{b_2(l_2)}{a_1(l_1)}\Big|_{a_2(l_2)=0}$$ = forward transmission coefficient with matched output port; (2.2c)

$$S_{22} = \frac{b_2(l_2)}{a_2(l_2)}\Big|_{a_1(l_1)=0}$$ = output reflection coefficient with matched input port. (2.2d)

2.1.2 Input Impedance Matching

From the view point of amplifier design, S_{11} denotes how well the input impedance is matched to the reference impedance. Ideally the input impedance of LNA should be 50 ohms, achieving a perfect matching, however, in the real implementation S_{11} is limited by other specifications and fabrication imperfections. S_{11} can be calculated as follows:

$$S_{11} = 10log_{10}\left(\left|\frac{Z_S - Z_0}{Z_S + Z_0}\right|\right) \tag{2.3}$$

where Z_S is the impedance looking into the input of LNA and Z_0 is the reference impedance 50 Ω. A commonly recognized good S_{11} is below -10 dB. Figure 2.3 shows the region in Smith chart where good input matching is achieved (S_{11}<-10dB).

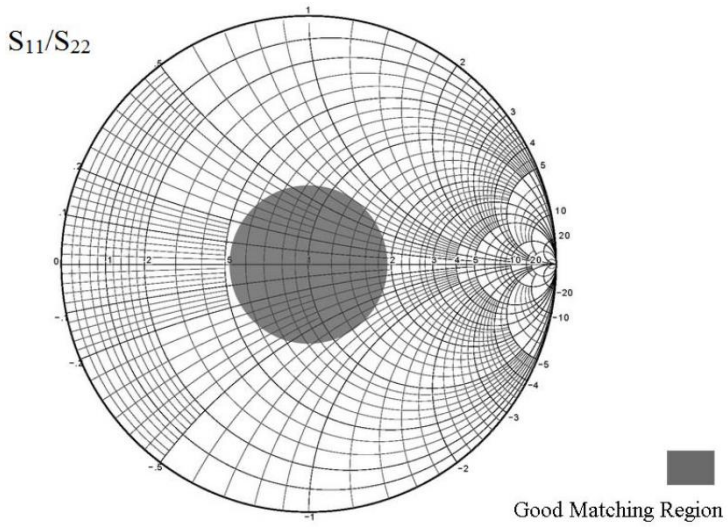


Fig. 2.3. Good matching region in Smith chart.

Similar to S_{11}, S_{22} represents how well the output impedance is matched to the reference one. As mentioned in the beginning of this chapter, in a fully integrated CMOS receiver, it is not necessary to match the output of LNA to 50 Ω. But as all RF measurement equipment has 50 Ω termination, an output buffer is often added to achieve output

matching for LNA measurement purpose. Similar to S_{11}, an S_{22} less than -10 dB is considered as good output matching.

2.1.3 Gain

S_{21} measures the insertion effect (power gain) of the amplifier. LNA gain is a critical specification and it mainly serves two functions. Firstly, a sufficient gain ensures a sufficient voltage swing of the RF signal so that the signal can be successfully processed by following circuits in a receiver chain. Secondly, a high gain of LNA will also suppress the noise of subsequent circuits, leading to a lower noise figure of the entire chain. However, in practice, a gain too high could deteriorate the linearity and lead to high power consumption. In the current literature, LNA usually designed with a gain of 10 – 20 dB. S_{21} also carries the information of bandwidth. Bandwidth is the range of frequency where the difference between the magnitude of S_{21} and the maximum magnitude is less than 3 dB. For the wideband LNA, the flatness of gain is important because if a fluctuation, which is more than 3 dB, occurs, the bandwidth will be seriously affected.

2.1.4 Noise Figure

Noise figure of a circuit is defined as the ratio of signal-to-noise ratio (SNR) at the input to the SNR at the output. It is given by:

$$NF = 10log_{10}(\frac{S_i/N_i}{S_o/N_o}) = 10log_{10}(\frac{N_o}{A \cdot N_i}) \quad (2.4)$$

where A is the gain of LNA and is defined by $A = S_o/S_i$. S_i and N_i are the signal power and noise power at input port respectively. S_o and N_o are the signal power and noise power at output port respectively. NF represents how much the SNR deteriorates after the

signal goes through the circuit. For the case of LNA, a low noise factor means the LNA amplifiers the signal while at the same time, it does not amplify the noise much. By (2.4), another interpretation of NF is the ratio of total noise power at output to the noise power caused by input port at output.

The reason why noise performance of LNA is critical to a receiver system is given by the Friis Equation [15]

$$F = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_n}{A_1 A_2 \ldots A_n} \tag{2.5}$$

F is the total noise factor a system consisting of n stages cascaded together. F_1, F_2 … F_n are the noise factors of 1st, 2nd … *n*th individual stages respectively. A_1, A_2 … A_n are the gain of 1st, 2nd … *n*th individual stages respectively. According to (2.5), noise of a later stage is buffered by the total gain from previous stages. Thus the first stage is critical to the overall noise of a system as F_1 contributes directly to the total F. A low noise factor of LNA is crucial to the overall noise factor of receiver and a high gain is also preferable since A_1 buffers all F_2, F_3 … F_n in the later stages. A high gain of LNA alleviates the noise design constrains in the subsequent stages.

To set the noise factor of an LNA, the parameters that determine the noise from a single transistor need to be identified. Thus noise model/sources [16] in a MOS transistor are to be studied. As shown in Fig 2.4, the two major noise sources are the channel thermal noise $\overline{i_{nd}^2}$ and the gate noise $\overline{i_{ng}^2}$. g_g, C_{gs}, and g_m are the gate conductance, gate-source capacitance and transconductance of the MOS transistor respectively. Although flicker noise is also one part of noise sources in a transistor, however, flicker noise density

decreases as frequency increases. Hence in the RF domain, thermal noise dominants flicker noise, which can often be neglected.

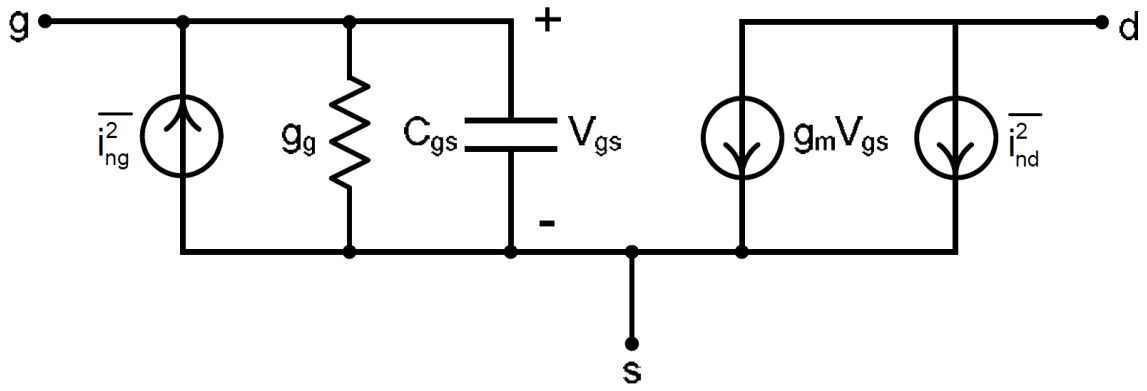


Fig. 2.4. Noise sources in a MOS transistor.

The channel thermal noise is given by:

$$\overline{i_{nd}^2} = 4KTg_m\frac{\gamma}{\alpha} \tag{2.6}$$

K is the Boltzmann constant, T is the absolute temperature, γ is the channel noise coefficient and $\alpha = g_m/g_{d0}$, where g_{d0} is the zero-bias drain conductance. For deep-submicron MOS transistor, α is usually less than unity and is approximated to be 0.85 [17][18]. γ is larger than unity and can become 2-3 for deep-submicron process [6][19].

The gate noise is given by:

$$i_{ng}^2 = 4KT\delta g_g \tag{2.7}$$

where $g_g = \omega^2 C_{gs}^2/5g_{d0}$. δ is the gate noise coefficient and can be larger than 2 for deep-submicron device. δ is taken as 2.21 in [6]. The gate noise is mainly caused by physical gate resistance, which can be reduced by implementing multi-finger gate in the design.

2.1.5 Third-order Intercept Point

The linearity of a system determines the maximum allowable signal level to its input. All real-life systems exhibit some degree of nonlinearity. Signal distortion is a direct consequence of the nonlinear behavior of solid-state devices in circuits. The 3rd order intercept point (IP_3) is another common measure of a circuit's nonlinearity. It is caused by the intermodulation (IMD) products of a signal and interferers.

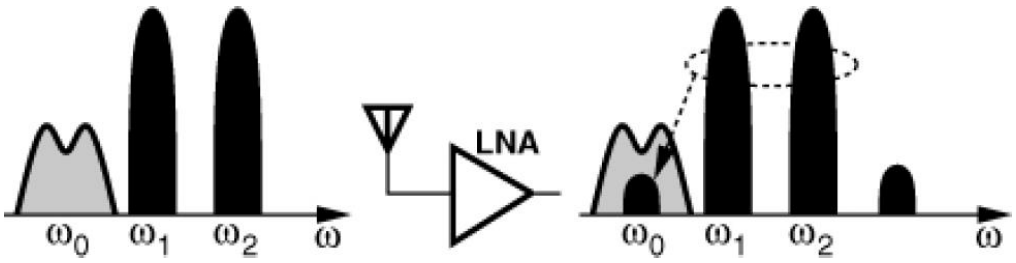


Fig. 2.5. Intermodulation-caused interference in LNA [21]

As shown in Fig. 2.5, two interferer signals ω_1 and ω_2, which are close the desired signal ω_0, will intermodulate with each other through LNA generating a new interferer signal located at frequency ω_0. The generated interferer appears at the output as signal distortion.

If the two-tone inputs have the same amplitude, the 3rd order IMD power will grow to a value that is equivalent to the cube of the input power as shown in Figure 2.6. In other words, the power of the third-order IMD increases three times faster than that of the fundamental. The input signal level, where the power of the third-order IMD equals to that of the fundamental is defined as "input-referred third-order intercept point" (IIP_3). And the corresponding output level is called the "output third-order intercept point" (OIP_3). The fundamental amplitude is a linear extrapolation of the small-signal fundamental output curve without the effect of gain compression.

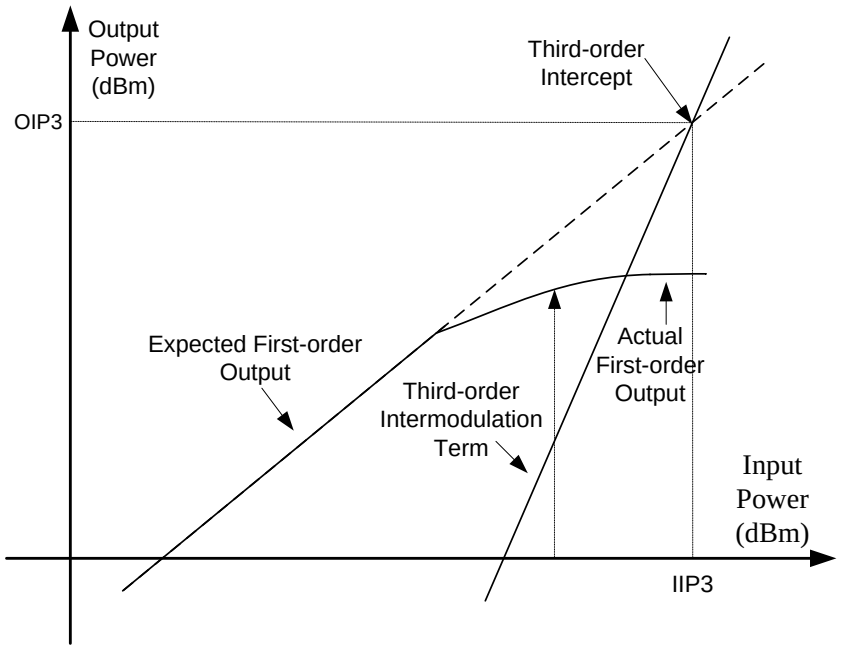


Fig. 2.6. Input-referred third-order intercept point

2.2 Review of Wideband LNA in Recent Literature

As discussed in section 2.1.1, one common requirement of LNA design is to match the input of LNA to 50ohm. Wideband LNA can be divided into two broad categories i.e. common source (CS) and common gate (CG), according to its input impedance matching architecture. Both architectures have a common limitation, i.e. trade-off between input matching and NF. Noise cancelling [5] is a popular technique, which is applicable to both common source and common gate architecture, in wideband LNA design. In section 2.2, firstly, CG and CS structure will be briefly discussed; secondly noise cancelling architectures in the literature will be studied. Lastly, research direction based on literature review will be given.

2.2.1 Common Source and Common Gate Wideband LNA

As the gate of LNA is a capacitive load and cannot match directly to 50 ohm, shunt resistive feedback is a common technique to design wideband common source LNA, as shown in Fig. 2.7.

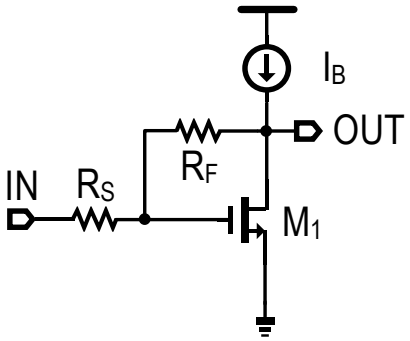


Fig. 2.7. Resistive feedback common source LNA

In this configuration, the input resistance can be approximated to be $1/g_m$. g_m is the transconductance of input transistor M_1. Noise figure is approximated as,

$$NF \approx 1 + \frac{4R_S}{R_F} + \frac{\gamma}{\alpha} g_m R_S \tag{2.8}$$

where R_F is feedback resistor and R_S is the 50Ω source resistor. According to (2.8), to achieve a lower NF, a larger g_m is preferred. However, since input resistance is directly related to g_m, a g_m too large deteriorates input matching. So this is the trade-off between matching and NF.

In a common gate case, the input impedance looking into the common-gate matching architecture is also $1/g_m$, as shown in Fig. 2.8.

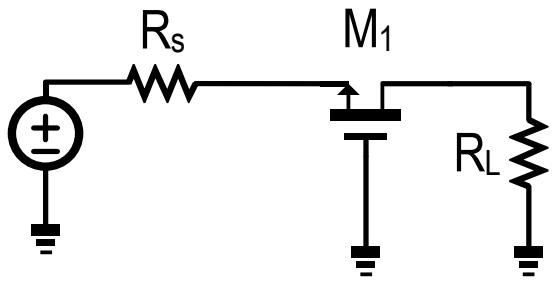


Fig. 2.8. Common-gate LNA

The noise factor in Fig. 2.8 considering only M_1 is approximated as,

$$F = 1 + \frac{\gamma}{\alpha g_m R_s} \tag{2.9}$$

By (2.9), an obvious trade-off between NF and input matching can also be observed. To show the trade-off in a quantitative way, some calculations are conducted as follows. When a perfect matching condition is fulfilled, i.e. $g_{m1} = 20mS$, and the process is deep sub-micron, i.e. α=0.85 and γ=2 [6], noise figure can be as high as 5dB. Even without considering other noise sources, the noise figure of a common-gate LNA is high for current state-of-art. In practice, a perfect input matching is not the in pursuit of designers, so g_{m1} can be designed larger to improve the noise performance. To make input matching less than -10 dB, g_{m1} can be increased to 38mS, however, under this condition, noise figure is still 4dB.

2.2.2 Noise-cancelling Wideband LNA

Noise cancelling technique aims to eliminate the noise from input transistor or the primary LNA shown in Fig. 2.9. The two nodes in primary LNA, X and Y, must fulfill one of the following conditions to enable noise cancelling technique to be applied:

1) Signals at X and Y are of the same phase, while noise caused by primary LNA at X and Y are out of phase.

2) Signals at X and Y are out of phase, while noise caused by primary LNA at X and Y are of the same phase.

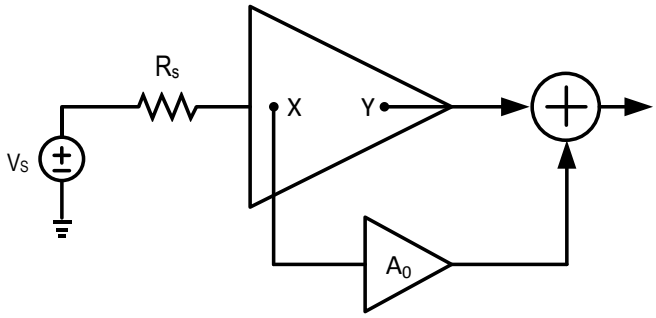


Fig. 2.9. Basic concept of noise cancelling LNA [20]

By setting the auxiliary amplifier non-reverse or reverse according to actual situation, signals will be added up at output, while noise caused by input matching transistor will subtract each other and be cancelled at output. Although the addition of the auxiliary amplifier will contribute some capacitive load to the input node, input impedance is still mainly determined by input transistor. Designers now can design the input transistor just for matching and amplification purpose without worrying about its noise contribution because the noise from input transistor will be cancelled or substantially reduced. Noise cancelling breaks the trade-off between input matching and noise figure. Noise cancelling technique can be used on the two wideband LNA architectures mentioned above, i.e. resistive feedback and common-gate.

The principle of resistive feedback LNA employing noise cancelling technique [5][6] is shown in Fig. 2.10. Similar to a conventional resistive feedback LNA, in Fig. 2.10, the

input impedance is approximated to be $1/g_{m1}$ without considering the loading effect at node Y, where g_{m1} is the transconductance of M_1. To see the effect of noise cancelling, noise voltage at node X and Y caused by thermal channel noise $I_{n,M1}$ is calculated as:

$$V_{n,X} = (R_S + R_F)I_{n,M1} \tag{2.10a}$$

$$V_{n,Y} = R_s I_{n,M1} \tag{2.10b}$$

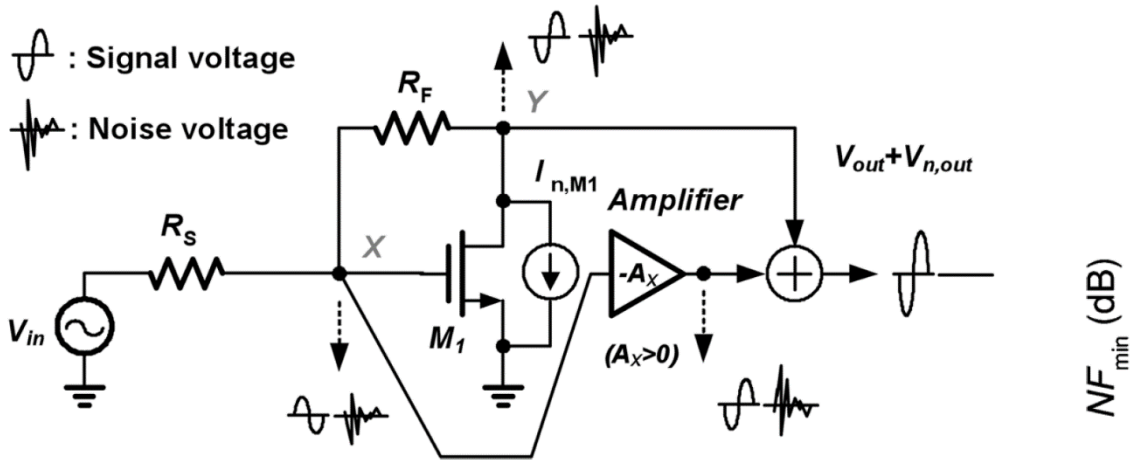


Fig. 2.10. Resistive feedback noise-cancelling configuration [6]

To have zero noise at output, the auxiliary amplifier A_x is designed so that $-A_x V_{n,X} + V_{n,Y} = 0$. So A_x is expressed as

$$A_x = 1 + \frac{R_F}{R_S} \tag{2.11}$$

With M1 noise cancelled, the major noise contributor are the feedback resistor R_F and auxiliary amplifier A_x. The overall noise figure is given by

$$NF = 1 + \frac{R_s}{R_F} + A_x^2 \overline{V_{n,Ax}^2} \frac{1}{4KTR_S A_v^2} \tag{2.12}$$

where A_v is gain of LNA and is expressed as,

$$A_v = \frac{V_{out}}{V_X} = (1 - g_{m1}R_F) - A_x = -R_F\left(g_{m1} + \frac{1}{R_S}\right) = -\frac{2R_F}{R_S} \tag{2.13}$$

(2.13) is based on the assumption of input matching condition, i.e. $R_S = 1/g_{m1}$. Based on (2.12), although noise from M_1 is cancelled, noise cancelling technique can not cancel the noise from feedback resistor R_F; moreover, it introduces a new noise source caused by auxiliary amplifier A_χ. The unsuppressed noise from R_F and the introduction of new noise source could beat the purpose of noise cancelling.

The principle of common-gate LNA employing noise cancelling technique [4] is shown in Fig. 2.11. Similar to a conventional common-gate LNA, in Fig. 2.11, the input impedance is approximated to be $1/g_{m1}$ without considering the loading effect at node Y, where g_{m1} is the transconductance of M_1. The thermal channel noise of input matching transistor M_1 is modeled as a noise current $I_{n,M1}$ across the drain and source. Two noise voltages, which have an opposite polarity to each other, are generated at node X and Y by $I_{n,M1}$. With a proper sizing of auxiliary amplifier M_2 and M_3, the noise current generated through M_2 and M_3 cancel each other at output node. On the other hand, signal voltages at X and Y are of the same polarity, generating signal currents that are combined and added at output. To see the effect of noise cancelling, noise current through M_2 and M_3 caused by thermal channel noise $I_{n,M1}$ is calculated as:

$$I_{n,M2} = -\frac{R_{L1} g_{m2}}{1 + g_{m1} R_S} I_{n,M1} \tag{2.14a}$$

$$I_{n,M3} = \frac{R_S g_{m3}}{1 + g_{m1} R_S} I_{n,M1} \tag{2.15b}$$

To have zero noise current at output, i.e. $I_{n,M2} + I_{n,M3} = 0$, the relationship between the transconductance of the two auxiliary transistors should fulfill:

$$\frac{g_{m2}}{g_{m3}} = \frac{R_S}{R_{L1}} \tag{2.16}$$

With M1 noise cancelled, the major noise contributor is the two auxiliary transistors M_2 and M_3 as well as the load resistor at node Y, R_{L1}. The overall noise factor is approximated to be:

$$\mathrm{F} = 1 + \frac{R_S}{R_{L1}} + \frac{R_S}{R_{L1}}\frac{\gamma}{\alpha}\frac{1}{g_{m2}R_{L1}} + \frac{\gamma}{\alpha}\frac{1}{g_{m3}R_S} \tag{2.17}$$

As this architecture can be interpreted as a current-mode circuit, the overall transconductance instead of voltage gain is given by:

$$G_m = \frac{I_{signal}}{V_{signal}} = \frac{1}{1 + g_{m1}R_S}(g_{m1}g_{m2}R_{L1} + g_{m3}) \tag{2.18}$$

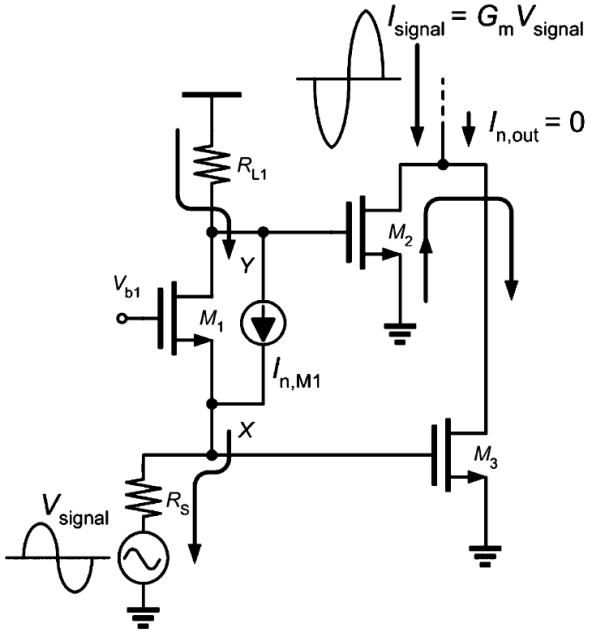


Fig. 2.11 Common-gate noise-cancelling configuration [4]

As mentioned in section 2.2.2, the noise figure of common-gate LNA can easily exceed 5dB, but with noise cancellation, noise figure can be reduced to 4.5dB [4]. Compared with resistive-feedback noise cancellation, noise figure of common-gate noise cancel LNA is independent of load impedance at the output. Moreover, the noise cancellation condition is directly determined by the sizing of M2 and M3, resulting in a more intuitive

design. However, circuit configuration shown in Fig. 2.11 shows an unsatisfying IIP3 performance of -6.2 dBm [4].

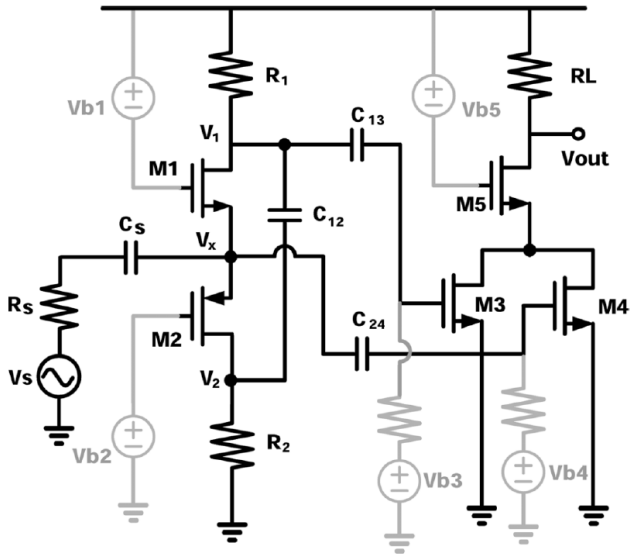


Fig. 2.12. Common-gate noise-cancelling LNA with pMOS-nMOS complementary pair as input [21]

The linearity performance can be further improved by adopting a pMOS-nMOS current reuse pair as the input matching stage [21], as shown in Fig. 2.12. The principle of distortion cancellation by pMOS-nMOS pair is explained as follows. For small signal operation, the nonlinearity transconductance of nMOS is represented by a power series:

$$i_{ds} = g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^2 + \frac{g_m''}{3!} v_{gs}^3 \tag{2.19}$$

The pMOS has the same characteristics but the subscript notation in (2.19) should be interchanged to reflect its opposite carrier type. Therefore the total current in a pMOS-nMOS pair is given by:

$$i_{total} = i_{ds,n} + i_{ds,p}$$

$$= \left(g_{m,n} v_{in} + \frac{g'_{m,n}}{2!} v_{in}^2 + \frac{g''_{m,n}}{3!} v_{in}^3 \right) - \left(g_{m,p}(-v_{in}) + \frac{g'_{m,p}}{2!}(-v_{in})^2 + \frac{g''_{m,p}}{3!}(-v_{in})^3 \right)$$

$$= (g_{m,n} + g_{m,p}) v_{in} + \frac{(g'_{m,n} - g'_{m,p})}{2} v_{in}^2 + \frac{(g''_{m,n} + g''_{m,p})}{6} v_{in}^3 \quad (2.20)$$

According to (2.20), a proper bias and sizing of the PNMOS pair can cancel the second-order distortion. In narrowband applications the second-order nonlinearity is usually not a concern because it results in distortion that is outside the frequency of interest. However, due to the cascade configuration in noise-cancelling LNAs, the second-order nonlinearity also contributes third-order distortion. Since the second order non-linear distortion of PMOS and NMOS have opposite sign, the pMOS-nMOS complementary pair can improve IIP3 dramatically. Work [21] achieves an excellent IIP3 of 16 dBm. However, it only achieves high linearity across a limited bandwidth of 1.4GHz.

2.2.3 Research Directions

By observing (2.12) and (2.13), it is found that increasing R_F can reduce the noise contribution from itself. Furthermore, a larger R_F leads to a high gain A_v, reducing the noise contribution from auxiliary amplifier. However, if R_F is increased too much, input impedance matching may be compromised. Therefore, a novel resistor-plus-source-follower noise cancelling LNA is proposed to increase R_F without compromising input matching. Details will be discussed in Chapter 3.

In the area of common-gate noise cancelling LNA, [4] managed to broaden the upper bond of bandwidth to 10.3 GHz with an inferior IIP3. On the other hand, [21] pushes IIP3 to 16dBm with a narrow bandwidth of 1.4GHz. To simultaneously achieve a bandwidth more than 10GHz and an IIP3 more than 0 dBm, a novel triple-path noise cancelling

LNA adopting pMOS-nMOS complementary pair is proposed. Details will be discussed in Chapter 4.

3. A resistive feedback LNA with enhanced noise figure and gain using noise-cancelation and source-follower-based feedback

3.1 Introduction

Compared with conventional wireless receiver, a wideband receiver is capable of higher data rate [3], [4]. Moreover, the wideband receiver can cover multiple standards such as GSM, Bluetooth, WiFi and GPS simultaneously [6], [22]. It is more power saving and area efficient to design one single wideband receiver than several individual receivers catering to the different standards. Wideband low noise amplifier (LNA) [4]-[6], [21]-[31] is a critical component in such wideband receivers for multi-standard or high-speed applications. The wideband LNA needs to meet stringent requirements such as flat and sufficient gain (S_{21}), flat and low noise figure (NF) and input return loss (S_{11}) below -10 dB across the bandwidth.

A common wideband input matching method is resistive feedback. However, in a typical resistive feedback configuration, the transconductance of input matching transistor is fixed around 20 mS to achieve good S_{11}, which limits noise performance [20]. Noise cancelling technique [4]-[6][8][21][22][26][27] has become the popular solution in breaking the trade-off between noise figure and input matching by cancelling the noise generated from input matching transistor. Several wideband resistive-feedback LNAs with noise cancelling [5], [6] have been reported. The concept was first proposed in [5], however, it only achieves a bandwidth of 1.6GHz, which is too low for high frequency

applications. In a later work, [6] broadens the bandwidth significantly to 5.2GHz. But it achieves a small gain of 10.7 dB even with an additional gain-enhanced signal path. Moreover it has a higher noise figure than [5]. To fulfill the input matching requirement, feedback resistor in [6] is designed relatively small, leading to low gain and higher noise contribution from feedback resistor. In noise cancelling situation, the noise from the resistor used in feedback network is not cancelled and this noise is not addressed specifically in above designs.

In this chapter, an additional local source-follower-based (SFB) feedback is introduced into a conventional resistive-feedback LNA by using a source follower that senses voltage from output node and injects a negative current into input. Effectively, this adds a shunt load at the gate of input matching transistor, allowing a larger value of feedback resistor for good input matching. Although addition of another transistor can bring excess noise, both gain and overall noise figure is improved due to a larger feedback resistor. A series inductor is used to broaden the input matching bandwidth and noise-cancelling is also adopted to provide extra gain and lower noise figure. The proposed LNA was implemented in a 65nm CMOS technology. It only occupies an active area of 0.044mm^2 and consumes 11.3 mW. Input return loss (S_{11}) is below -10 dB from 0.5 to 9.6 GHz. With low and flat noise figure and high gain, as shown in Table I, this work has a very competitive measured figure-of-merit (FOM) [6] of 3.57.

The rest of this chapter is organized as follows. Section 3.2 demonstrates the proposed LNA's frequency responses of the input return loss, gain and noise figure in detail. Section 3.3 evaluates and compares circuit performance of the LNA with and without

local SFB feedback. Section 3.4 presents measurement results. Finally conclusions are drawn in Section 3.5.

3.2 Principles of Circuit Design

3.2.1 Wideband Input Impedance Matching

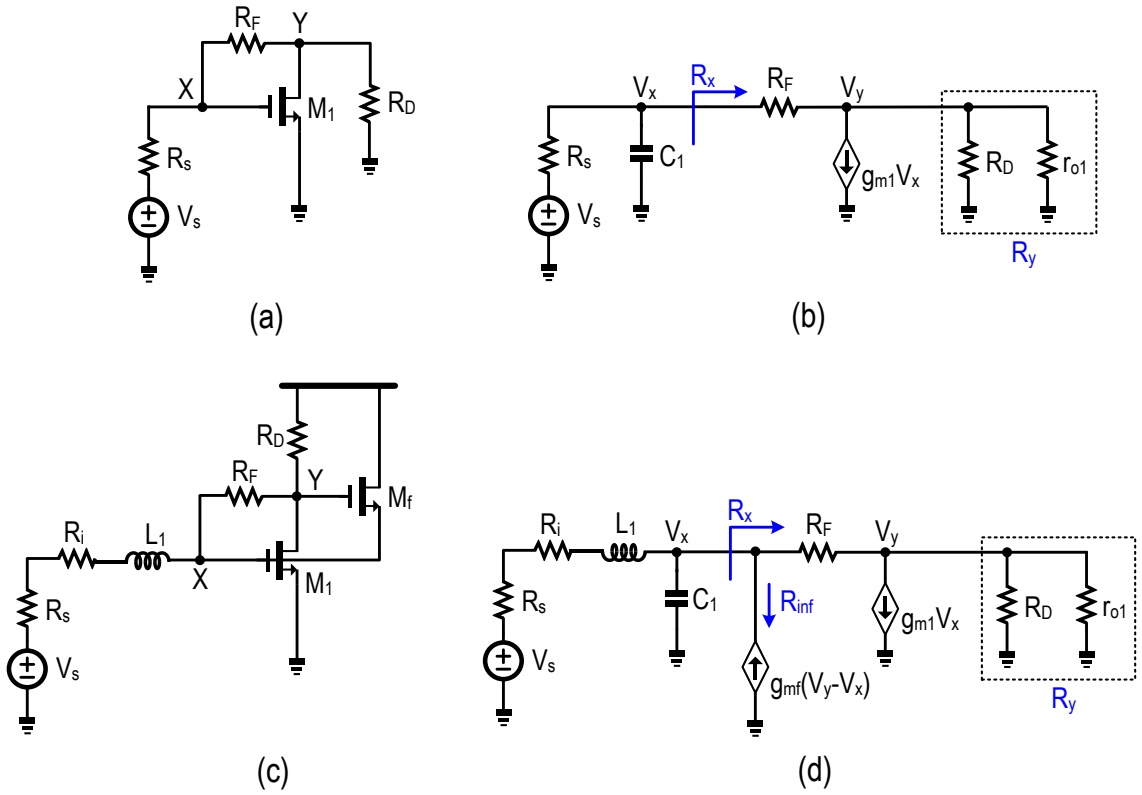


Fig. 3.1. (a) Schematic and (b) small-signal equivalent circuit of a typical resistive-feedback LNA. (c) Schematic and (d) small-signal equivalent circuit of the proposed resistive-feedback LNA with additional shunt-shunt feedback transistor.

Resistive feedback is one of most commonly used wideband input matching technique. Fig. 3.1(a) and 3.1(b) shows the schematic and equivalent small signal circuit of a typical resistive feedback configuration. The gate-drain capacitance is neglected. The input impedance of this typical configuration is derived as

$$Z_{in} = \frac{R_x}{C_1 R_x s + 1} \tag{3.1}$$

where $R_x = \frac{R_y + R_F}{g_{m1} R_y + 1}$ and $R_y = R_D || r_{01}$. R_y is the equivalent resistor of drain load resistor R_D parallel with the output resistance r_{01} of M_1. R_x is the resistance looking into the feedback resistor R_F. g_{m1} and C_1 are transconductance and gate-source parasitic capacitance of M_1 respectively. Voltage gain (A) of the typical configuration is given by

$$A = \frac{V_y}{V_x} = -\frac{R_y (R_F g_{m1} - 1)}{R_F + R_y} \tag{3.2}$$

By taking the first derivative of (3.2) with respect to R_F, it is found that gain increases with increasing R_F. Although it is desirable to have a larger R_F to obtain higher gain, the value of R_F is easily constrained by Z_{in}. According to (3.1), once R_F reaches certain value, it deviates Z_{in} too much away from 50 Ω and corrupts S_{11}. To overcome the trade-off between input matching and gain, a local SFB feedback loop is created between node X and Y by adding a source follower M_f, as shown in Fig. 3.1(c). In addition, a series inductor is connected to the gate of M_1 to provide matching for wider frequency range. Input impedance of this proposed structure is derived through small signal circuit Fig. 3.1(d) and shown as

$$Z_{in} = \frac{L_1 C_1 R_x s^2 + (L_1 + C_1 R_x R_i) s + R_i + R_x}{C_1 R_x s + 1} \tag{3.3}$$

where L_1 is the matching inductor and R_i is its parasitic resistance. The complete S_{11} is as follow:

$$|S_{11}| = \left|\frac{L_1C_1R_ss^2 + (L_1 + C_1R_xR_i - C_1R_xR_s)s + R_x + R_i - R_s}{L_1C_1R_ss^2 + (L_1 + C_1R_xR_i - C_1R_xR_s)s + R_x + R_i + R_s}\right| \tag{3.4}$$

Now with the addition of SFB feedback, the resistance looking into node X in Fig. 1(d) is expressed as

$$R_x = \frac{(R_y + R_F)R_{inf}}{(g_{m1}R_y + 1)R_{inf} + R_y + R_F} \tag{3.5a}$$

where

$$R_{inf} = \frac{1}{g_{mf}(1+A)} \tag{3.5b}$$

R_{inf} is the resistance looking into the source of M_f. Compared with original expression of $\frac{R_y+R_F}{g_{m1}R_y+1}$, R_x in (3.5) has a smaller value due to the term $R_y + R_F$ in denominator. Note that A is negative, leading to a negative $g_{mf}(V_y - V_x)$. Therefore, the small signal current in M_f is actually flowing from node X to ground, making M_f an effective resistor, R_{inf}, parallel connected to node X. R_{inf} brings down the input impedance of the proposed LNA. Compared with typical resistive-feedback configuration in Fig. 3.1(a), for the same DC input matching condition, i.e. same R_x, R_F can now be designed with larger value to improve gain. A larger R_F also produces a better noise performance, which will be discussed in detail in section 3.2.2.

3.2.2 Frequency Response of S_{21}

Noise cancelling technique is one of the most popular wideband LNA architecture as it reduces noise from input matching transistor. Moreover, it provides an additional feedforward path, improving gain. Fig. 3.2 (a) and (b) shows the schematic and small

signal circuit of resistive feedback LNA with transistor feedback (M_f) and noise cancelling paths (M_2 and M_3). C_1 and C_2 are total parasitic capacitance at node X and Y respectively. Voltage gain of this LNA is composed of two parts: $A_v = \frac{V_{out}}{V_x}$ and $A_0 = \frac{V_x}{V_s}$.

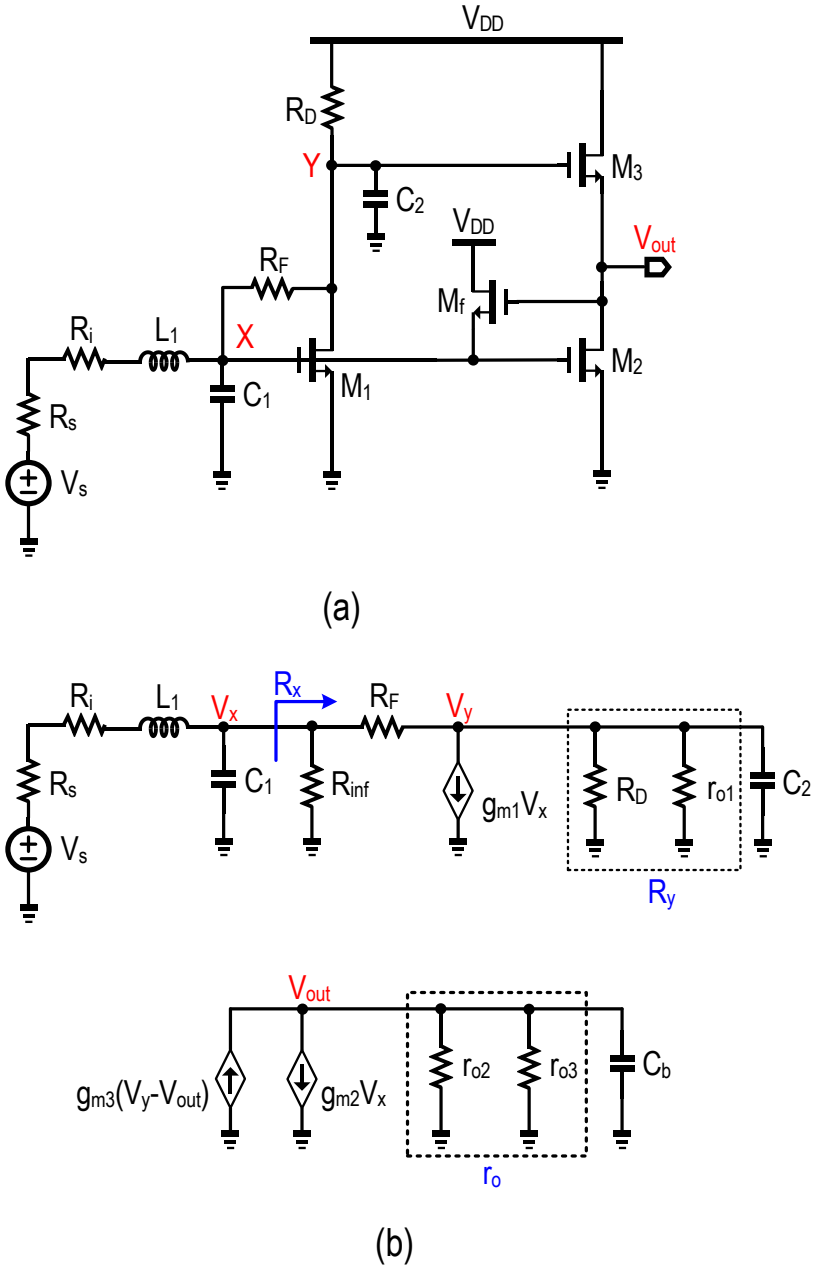


Fig. 3.2. (a) Schematic and (b) small-signal equivalent circuit of the proposed LNA combining local source-follower-based feedback with noise-cancelling technique.

A_v is the voltage gain from node X to output node and is given by:

$$A_v = \frac{V_{out}}{V_x} = -\frac{(-g_{m3}A_1 + g_{m2})(r_0||(1/sC_b))}{1 + g_{m3}(r_0||(1/sC_b))} \tag{3.6a}$$

where

$$r_0 = r_{02}||r_{03} \tag{3.6b}$$

$$A_1 = \frac{V_y}{V_x} = -\frac{R_F R_y g_{m1} - R_y}{C_2 R_F R_y s + R_y + R_F} \tag{3.6c}$$

A_1 is the voltage gain from node X to node Y. g_{m2}, g_{m3}, r_{02} and r_{03} are the transconductance of M_2 and M_3 and drain-source resistance of M_2 and M_3 respectively. C_b represents the gate capacitance of the buffer in next stage. If we assume $1 + g_{m3}r_0 \approx g_{m3}r_0$, which is usually the case, equation 3.6(a) can be further simplified as $A_v = A_1 - g_{m2}/g_{m3}$. Note that A_1 is a negative term and it is evident that noise cancelling architecture improves voltage gain. A complete expression of A_v is shown as:

$$A_v = \frac{C_2 R_F R_y g_{m2} r_0 s + (R_F + R_y) r_0 g_{m2} + R_y r_0 g_{m3}(R_F g_{m1} - 1)}{C_b C_2 R_F R_y r_0 s^2 + C_{b(} R_F + R_y) r_0 s + C_2 R_F R_y (1 + g_{m3} r_0) s + (R_F + R_y)(1 + g_{m3} r_0)} \tag{3.7}$$

Another part of the LNA gain A_0 is the voltage gain from source to node X, which is given by:

$$A_0 = \frac{V_x}{V_s} = \frac{R_x}{L_1 C_1 R_x s^2 + [L_1 + C_1 R_x (R_s + R_i)]s + R_s + R_x + R_i} \tag{3.8}$$

where R_x is given by (3.5a). However, the resistance looking into the source of M_f is slightly changed, $R_{inf} = \frac{1}{g_{mf}(1+|A_v|)}$. By (3.8), the reactive components that mainly determine the poles of A_0 are C_1 and L_1. C_2 is usually much smaller than C_1 because M_3 is designed smaller than M_1 and M_2 for noise cancelling purpose. Effect of C_2 on A_0 is neglected for simplicity. S_{21} is twice the voltage gain in a 50 Ω system with impedance matching and it is given by:

$$S_{21} = 2A_{core} = 2A_0A_v \tag{3.9}$$

where A_{core} is the total voltage gain from source to output in Fig. 2 and $A_{core} = A_0A_v$. Equation (3.6) and (3.8) show that addition of feedback transistor M_f only affects A_0 and has no influence on A_v. In fact, the DC expression of (3.6c) is shown by (3.2). Under impedance matching condition, i.e. $A_0 = 0.5$ at DC, S_{21} has same expression for both situations with and without M_f. However, as illustrated in part A, by adding M_f, R_F can be designed with a larger value compared with non-feedback situation. By (3.6), a larger R_F leads to a higher gain. In this way, S_{21} is improved by the feedback transistorM_f.

3.2.3 Frequency Response of NF

The major noise sources in the LNA are the channel resistance thermal noise from M_1, M_2, M_3 and M_f, as well as thermal noise from R_D and R_F. Noise contributed by input inductor parasitic resistance R_i is also taken into account. Fig. 3.3 shows the small signal equivalent circuit of Fig. 3.2(a) for noise calculation.

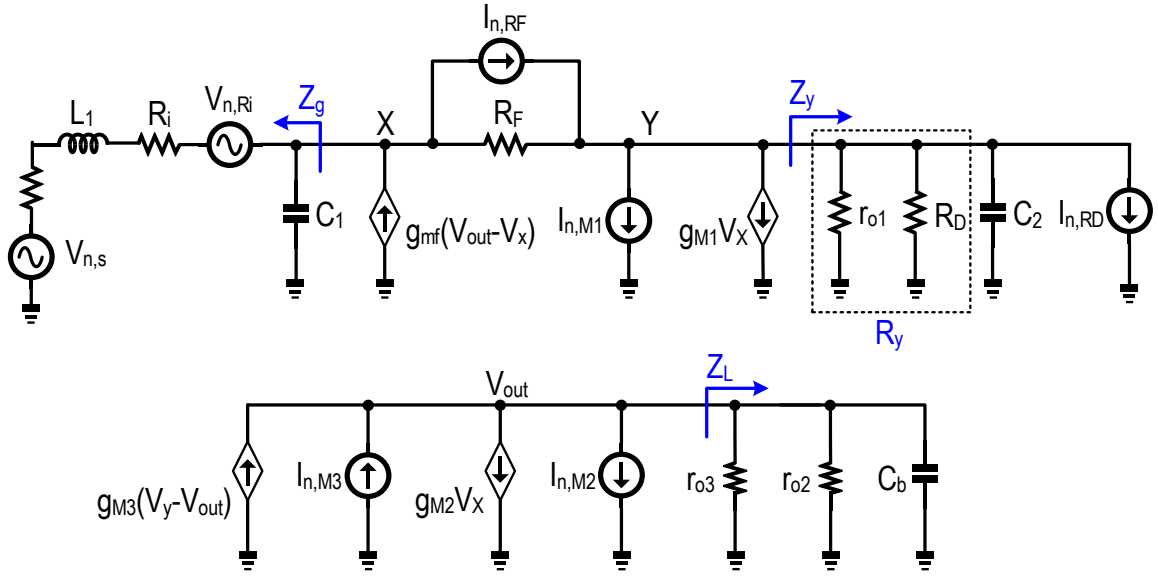


Fig. 3.3. Equivalent circuit of Fig. 3.2(a) for noise calculation

Noise factor contribution of M_1 is given by:

$$F_{M1} = \frac{g_{m1}}{R_s|A_{core}|^2}\frac{\gamma}{\alpha}\left|\frac{R_F}{\left(1+\frac{R_F}{Z_y}\right)A_{1,n1} + R_F g_{m1} - 1}A_{v,n1}\right|^2 \tag{3.10a}$$

where

$$A_{1,n1} = \frac{V_{y,n1}}{V_{x,n1}} = 1 + \frac{R_F}{Z_g} + g_{mf}R_F\frac{\frac{g_{m2}}{g_{m3}} + \frac{1}{g_{m3}Z_L} - \frac{R_F}{Z_g}}{1 + \frac{1}{g_{m3}Z_L} + R_F g_{mf}} \tag{3.10b}$$

$$A_{v,n1} = \frac{V_{out,n1}}{V_{x,n1}} = \frac{(g_{m3}A_{1,n1} - g_{m2})Z_L}{1 + g_{m3}Z_L} = \frac{g_{mf}R_F + \frac{R_F}{Z_g} + 1 - \frac{g_{m2}}{g_{m3}}}{g_{mf}R_F + \frac{1}{Z_L g_{m3}} + 1} \tag{3.10c}$$

As shown in Fig. 3.3, $Z_y = \frac{R_y}{C_2R_y s+1}$, $Z_g = \frac{L_1 s+R_s+R_i}{L_1C_1s^2+C_1(R_s+R_i)s+1}$ and $Z_L = \frac{r_o}{C_b r_o s+1}$. Z_y is the impedance of R_y parallel with C_2. Z_g is the impedance looking into matching network from node X. Z_L is the total impedance at V_{out}. $A_{1,n1}$ is the ratio of noise voltage caused

by M_1 at node Y to that at node X. $A_{v,n1}$ is the ratio of noise voltage at V_{out} to that at node X. γ is the coefficient of channel noise and $\alpha = g_{m1}/g_{d0}$, where g_{d0} is zero-bias drain conductance. Equation (3.10c) shows that perfect noise cancelling is achieved when $g_{mf}R_F + \frac{R_F}{Z_g} + 1 = \frac{g_{m2}}{g_{m3}}$, leading to $F_{M1} = 0$. However, since Z_g is complex and $\frac{g_{m2}}{g_{m3}}$ is real, a perfect noise cancelling cannot be achieved. A good approximation is $\Re(g_{mf}R_F + \frac{R_F}{Z_g} + 1) = \frac{g_{m2}}{g_{m3}}$. By looking at Fig. 3, the transfer functions from $I_{n,M1}$ and $I_{n,RD}$ to the output are the same. A similar case is true for $I_{n,M2}$ and $I_{n,M3}$. The noise factor contribution of R_D, M_2 and M_3 is given by:

$$F_{RD} = \frac{1}{R_D R_s |A_{core}|^2}\frac{\gamma}{\alpha}\left|\frac{R_F}{\left(1+\frac{R_F}{Z_y}\right)A_{1,n1} + R_F g_{m1} - 1}A_{v,n1}\right|^2 \tag{3.11}$$

$$F_{M3} = \frac{g_{m3}}{R_s |A_{core}|^2}\frac{\gamma}{\alpha}\left|\frac{Z_L}{g_{m3}Z_L(A_{v,n2} - A_{1,n2}) + g_{m2}Z_L + A_{v,n2}}A_{v,n2}\right|^2 \tag{3.12}$$

$$F_{M2} = \frac{g_{m2}}{R_s |A_{core}|^2}\frac{\gamma}{\alpha}\left|\frac{Z_L}{g_{m3}Z_L(A_{v,n2} - A_{1,n2}) + g_{m2}Z_L + A_{v,n2}}A_{v,n2}\right|^2 \tag{3.13a}$$

where

$$A_{1,n2} = \frac{V_{y,n2}}{V_{x,n2}} = \frac{Z_y - g_{m1}R_F Z_y}{Z_y + R_F} = -\frac{R_y(R_F g_{m1} - 1)}{C_2 R_F R_y s + R_F + R_y} \tag{3.13b}$$

$$A_{v,n2} = \frac{V_{out,n2}}{V_{x,n2}} = \frac{1}{g_{mf}}\left(\frac{1}{Z_g} + \frac{1}{R_F} - \frac{A_{1,n2}}{R_F}\right) + 1$$

$$= 1 + \frac{1}{g_{mf}}\frac{L_1 C_1 s^2 + C_1 R_s s + 1}{L_1 s + R_s} + \frac{1}{g_{mf}}\frac{C_2 R_y s + R_y g_{m1} + 1}{C_2 R_F R_y s + R_F + R_y} \tag{3.13c}$$

To analyze the effect of feedback on F_{M2}, noise factor contributed by M_2 under non-feedback condition is given by:

$$F_{M2,wofb} = \frac{g_{m2}}{R_s\left|A_{core,wofb}\right|^2}\frac{\gamma}{\alpha}|Z_L|^2 \tag{3.14}$$

For convenient comparison, (3.13a) is re-written as:

$$F_{M2} = \frac{g_{m2}}{R_s|A_{core}|^2}\frac{\gamma}{\alpha}\left|Z_L - \frac{g_{m3}Z_L\left(A_{v,n2} - A_{1,n2}\right) + g_{m2}Z_L}{g_{m3}Z_L\left(A_{v,n2} - A_{1,n2}\right) + g_{m2}Z_L + A_{v,n2}}\right|^2 \tag{3.15}$$

Since $A_{1,n2}$ is negative and $|A_{core}|$ is larger than $\left|A_{core,wofb}\right|$, F_{M2} and F_{M3} is reduced with the help of feedback M_f. Noise factor contributed by feedback resistor R_F is given by:

$$F_{RF} = \frac{1}{R_F R_s|A_{core}|^2}\left|\frac{A_{v,RF}}{\frac{1}{Z_g} + g_{mf}\left(1 - A_{v,RF}\right) + \frac{1 - A_{1,RF}}{R_F}}\right|^2 \tag{3.16a}$$

where

$$A_{1,RF} = \frac{V_{y,RF}}{V_{x,RF}} = -\frac{Z_y}{Z_g} - g_{m1}Z_y + g_{mf}\frac{g_{m3}Z_L\left(\frac{Z_y}{Z_g} + g_{m1}Z_y + 1\right) + g_{m2}Z_L + 1}{g_{m3}Z_L\left(g_{mf} - \frac{1}{Z_y}\right) - \frac{1}{Z_y}} \tag{3.16b}$$

$$A_{v,RF} = \frac{V_{out,RF}}{V_{x,RF}} = -\frac{Z_L\left(g_{m3}\frac{Z_y}{Z_g} + g_{m1}g_{m3}Z_y + g_{m2}\right)}{1 + g_{m3}Z_L}$$

$$+\frac{g_{mf}g_{m3}Z_L}{1 + g_{m3}Z_L}\frac{g_{m3}Z_L\left(\frac{Z_y}{Z_g} + g_{m1}Z_y + 1\right) + g_{m2}Z_L + 1}{g_{m3}Z_L\left(g_{mf} - \frac{1}{Z_y}\right) - \frac{1}{Z_y}} \tag{3.16c}$$

The term $g_{mf}(1 - A_{v,RF})$, which is introduced by M_f, in the denominator of (3.16a) reduces noise factor from R_F. Moreover, the term $\frac{1}{R_F}\left|\frac{A_{v,RF}}{\frac{1}{Z_g}+g_{mf}(1-A_{v,RF})+\frac{1-A_{1,RF}}{R_F}}\right|^2$ decreases with increasing R_F. Since addition of feedback allows a larger R_F and $|A_{core}|$, F_{RF} is also improved. One drawback of adding active feedback loop in LNA is the extra noise brought by active transistor. The noise factor contribution of M_f is given by:

$$F_{Mf} = \frac{g_{mf}}{R_s|A_{core}|^2}\frac{\gamma}{\alpha}\left|\frac{Z_g A_{v,nmf}}{\left(g_{mf}Z_g A_{v,nmf} - g_{mf}Z_g - 1\right) + \frac{Z_g\left(A_{1,nmf}-1\right)}{R_F}}\right|^2 \qquad (3.17a)$$

where

$$A_{1,nmf} = \frac{V_{y,Mf}}{V_{x,Mf}} = \frac{Z_y(1 - R_F g_{m1})}{R_F + Z_y} \qquad (3.17b)$$

$$A_{v,nmf} = \frac{V_{y,Mf}}{V_{x,Mf}} = \frac{Z_L}{1 + g_{m3}Z_L}\frac{g_{m3}Z_y - g_{m2}Z_y - g_{m2}R_F - g_{m1}g_{m3}R_F Z_y}{R_F + Z_y} \qquad (3.17c)$$

F_{Mf} is increasing with increased R_F due to the term $\frac{Z_g(A_{1,nmf}-1)}{R_F}$ in the denominator of (3.17a). This potentially limits the improvement of NF in a SFB feedback LNA. However, F_{Mf} is still buffered by an enhanced $|A_{core}|$. Moreover, it only contributes minimally to total noise factor, which is shown in the next section. The overall noise factor is given by:

$$F = 1 + \frac{R_i}{R_s} + F_{M1} + F_{RD} + F_{M2} + F_{M3} + F_{RF} + F_{Mf} \qquad (3.18)$$

By noise cancellation, noise from M_1 and R_D is reduced. Furthermore, all F_{RD}, F_{M2} and F_{M3} are decreased due to local SFB feedback.

3.3 Proposed Complete LNA

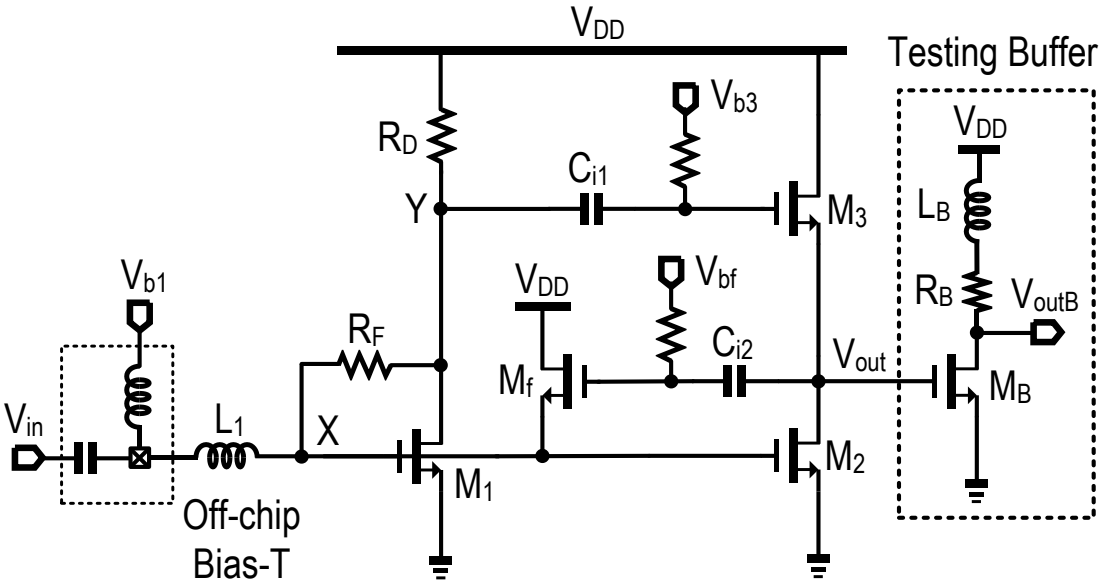


Fig. 3.4. Complete schematic of the proposed wideband LNA.

Fig. 3.4 shows the complete schematic of proposed wideband LNA. Two DC-decoupling capacitors (C_{i1}, C_{i2}) and two voltage biases (V_{b3}, V_{bf}) are introduced. Gate bias (V_{b1}) of M_1 is provided by off-chip bias-tee. A common-gate output buffer is added to provide output matching for measurement purpose. Inductor L_B is series connected to the drain of buffer transistor to counter the effect of load capacitance on core's bandwidth. Table 3.1 summarizes the dimension and value of devices presented in Fig. 3.4. Simulations are performed to verify the performance enhancement introduced by M_f. Fig. 3.5 shows at the same input matching of -12.5dB, the proposed LNA with feedback M_f has better S_{21} and NF performance than the LNA without feedback. Generally a S_{11} of -10 dB is considered sufficient for a good input matching, however, a design redundancy around

2.5dB is necessary in case of fabrication deviation. When both LNAs show a S_{11} of -12.5 dB, R_F in non-feedback LNA is 300Ω, while R_F in proposed LNA can be as high as 640 Ω. As discussed in section II, a higher R_F improves gain and NF. As shown in Fig. 5, S_{21} and NF are improved by 0.7 dB and 0.45 dB respectively.

Table 3.1
Dimension of Devices I

M_1	140μm/65nm	M_2	159μm/65nm
M_3	20μm/65nm	M_f	3μm/65nm
M_B	120μm/65nm	R_F	640Ω
R_D	135Ω	R_B	40Ω
L_1	0.54nH	L_B	1.5nH

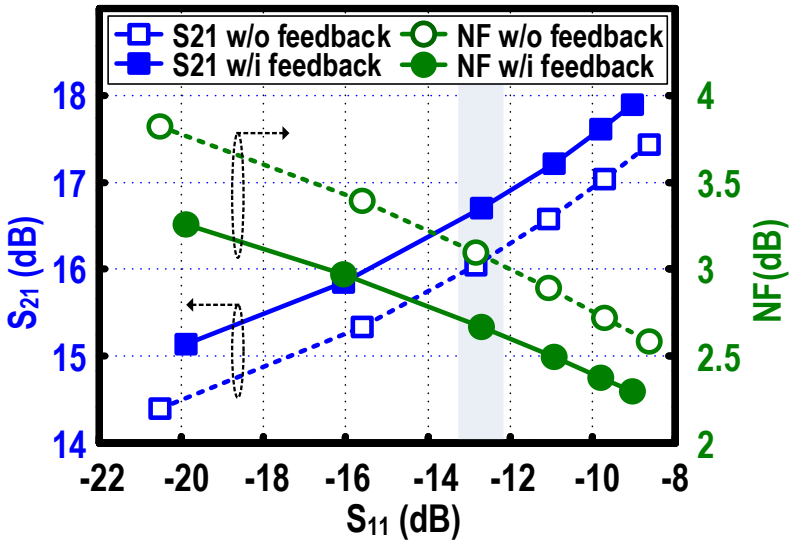


Fig. 3.5. Simulated NF and S_{21} versus S_{11} of the LNAs with and without the local SFB feedback.

Relative noise contributions by individual components in the LNA with and without transistor feedback are presented in Fig. 3.6. With feedback M_f, noise contribution

percentage of M_2, R_F, and M_3 drops from 17.4%, 11.9% and 6.7% to 12.0%, 6.6% and 4.6% respectively. The noise contribution reduction verifies the analysis in section II. Noise from M_f is 2.5%, which is relatively small compared with the total noise reduction in other components. Although, noise from M_1 is higher than the non-feedback situation, adding M_f into the LNA improves the overall NF, which is reflected by port noise contribution. Fig. 3.7 shows the circuit performance of LNA with and without feedback at various S_{11}. R_F is swept to obtain the various matching conditions. The maximum improvement of gain and NF are 2 dB and 0.57 dB respectively. Across a wide range of matching conditions, from -20dB to -8dB, the propose LNA with feedback always has a better S_{21} and NF than the LNA without feedback.

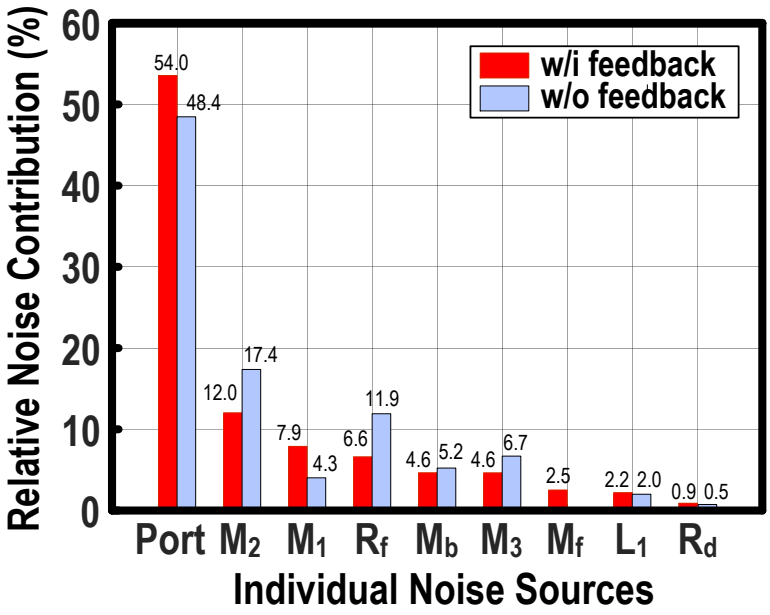


Fig. 3.6. Simulated relative noise contributions by individual components in the LNAs with and without local SFB feedback.

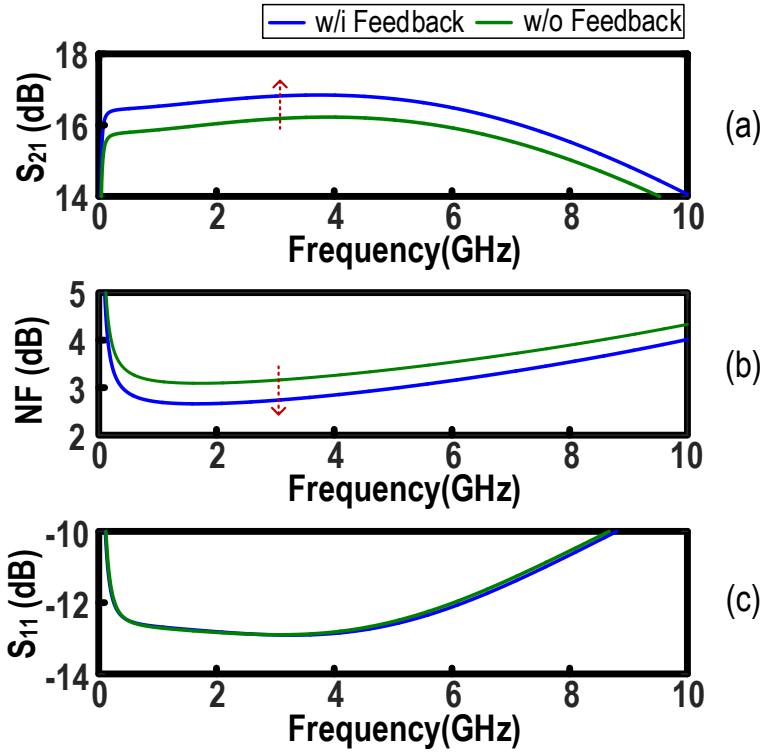


Fig. 3.7. Simulated (a) S_{21} and (b) NF versus frequency of the LNAs with and without local SFB feedback, under the same (c) input matching condition.

3.4 Measurement Results

The proposed LNA prototype has been implemented in a 65nm CMOS technology. Fig. 3.8 gives the die photo of the proposed LNA. It occupies a compact active area of 0.25 × 0.18 mm^2. The measurement was conducted using Agilent vector network analyzer (N5245A). The prototype draws 11.3 mW with a supply voltage of 1.2 V.

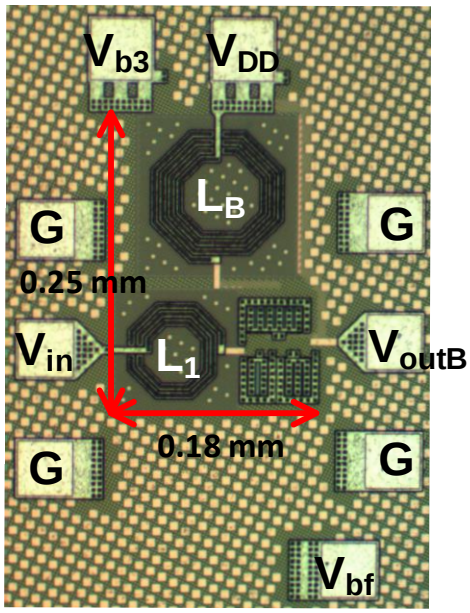


Fig. 3.8. Die photo of the proposed LNA.

Fig. 3.9 shows the measured S_{21}, NF and S_{11} versus gate bias (V_{b1}) of M_1. S_{21} and NF keeps improving as V_{b1} increases until $V_{b1} = 660mV$, after which S_{21} and NF begin to drop and increase respectively. At $V_{b1} = 660mV$, the peak S_{21} is 16.8 dB with a f_{-3dB} of 7 GHz. S_{21} has a maximum in-band ripple of 0.32 dB, shows excellent flatness in band. Measured NF_{min} and NF_{max} at $V_{b1} = 660mV$ is 2.87 dB at 2 GHz and 3.71 dB at 7 GHz. In-band variation of NF is only 0.84 dB from 0.5 to 7 GHz, which is very competitive to other results in literature. Fig. 3.9 also shows a clear trade-off between S_{11} and the other two parameters, i.e. S_{21} and NF. However, due to careful optimization, S_{11} is just barely above -10 dB for the entire band of interest at $V_{b1} = 660mV$, where S_{21} and NF are at their best. Fig. 3.10 shows the calculated, simulated and measured results of S_{21}, NF and S_{11} of the proposed LNA. Calculated result makes use of equations derived in Section 3.2.

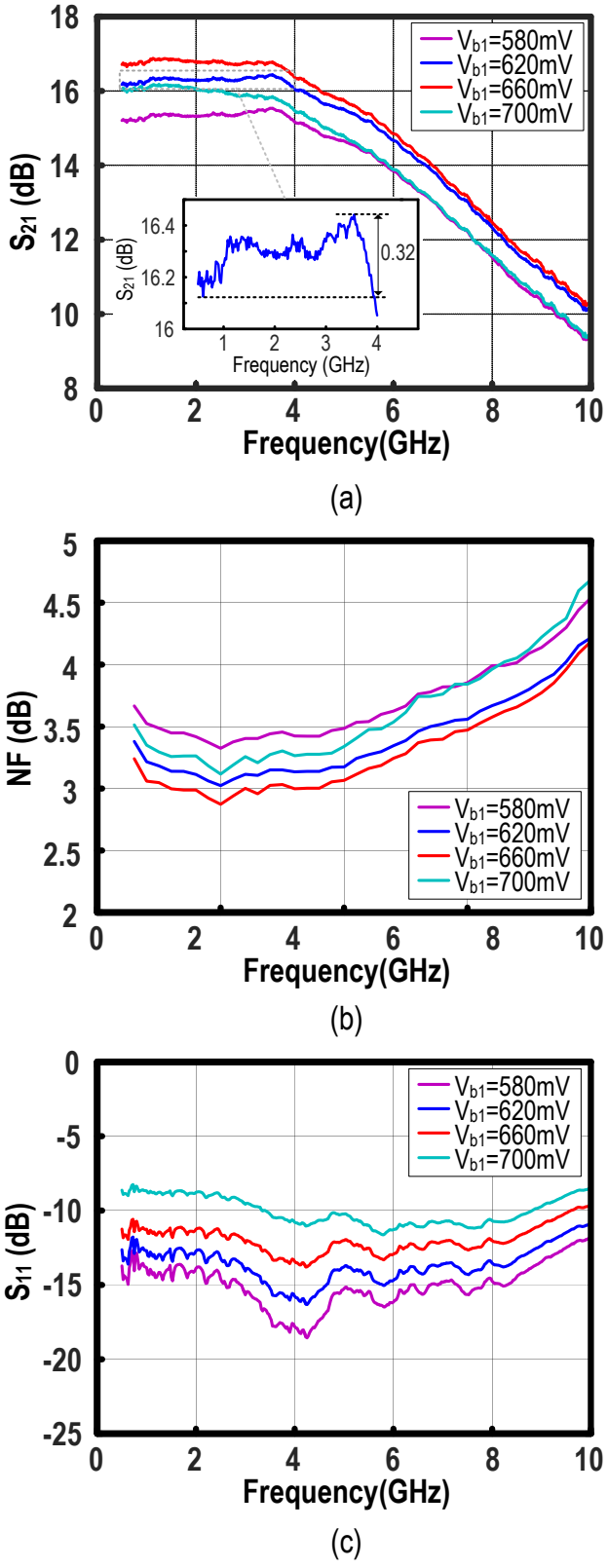


Fig. 3.9. Measured (a) S_{21}, (b) NF and (c) S_{11} versus frequency with different input bias voltage (V_{b1}) of the proposed LNA.

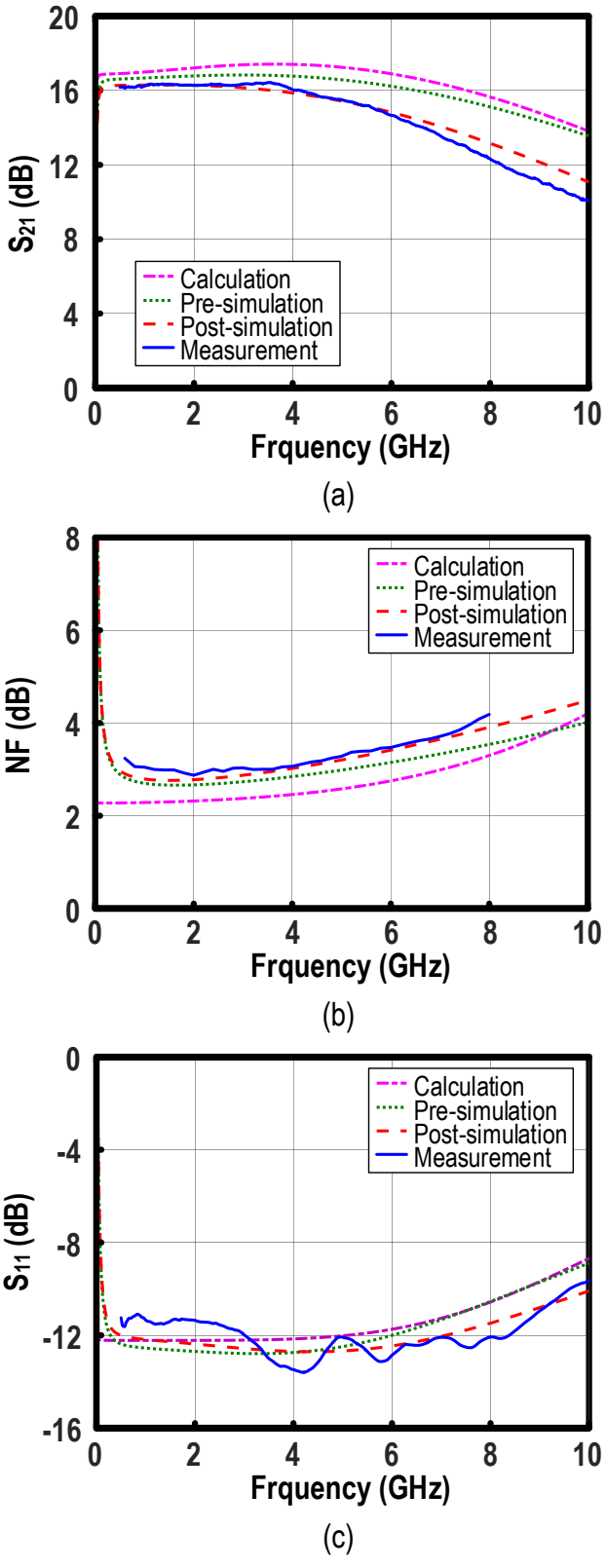


Fig. 3.10. Calculated, simulated and measured (a) S_{21}, (b) NF and (c) S_{11} versus frequency of the proposed LNA.

The calculated result is consistent with the simulated and measured results. Fig. 3.11 shows the measured IIP3 is -4.5 dBm when two-tone signals at 4 GHz and 4.1 GHz are applied. Space Δf between two-tone signals at 4 GHz is swept as shown in Fig. 3.12. The highest IIP3 is -4.5 dBm when the space is 10 MHz and lowest IIP3 is -5.8 dBm when the space is 80 MHz. IIIP3 is also measured across various center frequencies. IIP3 steadily increases with frequency due to lower gain at higher frequency. The highest IIP3 is -1.5 dBm at 7 GHz.

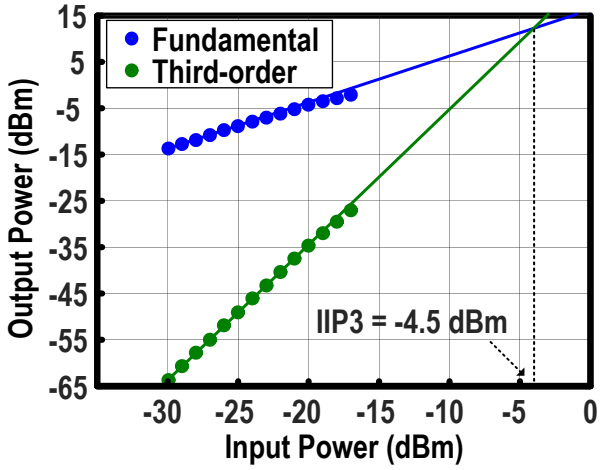


Fig. 3.11. Measured IIP3 of the proposed LNA for two-tone inputs of 4 and 4.01 GHz.

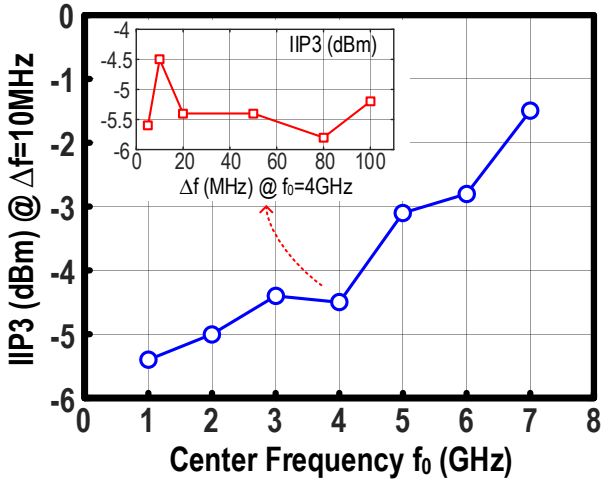


Fig. 3.12. Measured IIP3 versus center frequency (f_0) and two-tone separation (Δf) of the proposed LNA.

Table 3.2 summarizes performance benchmark. This work achieves good NF not only in terms of minimum NF but also in terms of NF flatness. Although inductor is used, the area of this work is still comparable to some of the works without passive inductors [6], [24], [27]. This work also has one of the highest gains. FOM of this work is the best among recent arts.

TABLE 3.2
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART I.

	CMOS Technology	Frequency (GHz)	Bandwidth (GHz)	Gain (dB)	Noise Figure (dB)	NF_{min} (dB)	IIP3 (dBm)	Supply Voltage (V)	Power (mW)	Area (mm^2)	FOM*
This Work	65nm	0.5 – 7	6.5	16.8	2.87 – 3.77	2.87	-4.5	1.2	11.3	0.044	3.57
[6] TCAS-I'12	65nm	0.1 – 5.3	5.2	10.7	2.9 – 5.4	2.9	-6	1	7	0.03	-3.43
[22] ESSCC'07	65nm	0.2 – 5.2	5	9.6	3 – 3.5	3	0	1.2	21	0.009	-2.82
[8]ESSCC'10	65nm	0.1 – 4.0	3.9	18	2 – 4.4	2	-5.5	1.2	12	0.001	1.9
[23] ASSCC'09	65nm	1 – 10	9	16.5	3.9 – 5.0	3.9	-5	1.2	36	0.021	-8.79
[24] MWCL'08	90nm	0.1 – 8	7.9	16	3.4 – 5.8	3.4	-9	1.2 & 1.4	16	0.034	-9.62
[25]TCAS-II'10	90nm	3.0 – 8.5	5.5	16	3.1 – 4.4	3.1	-5.4	1.2	16	0.022	-4.43
[27]JSSC'10	130nm	2.1 – 3.4	1.3	16.4	2.1 – 3.4	2.1	0	1.8	14.4	0.036	-1
[28] TMTT'10	180nm	1.7 – 5.9	4.2	11.2	3.6 – 4.7	3.6	-12	1.8	10.34	0.565	-22.84
[5] JSSC'04	250nm	0.02 – 1.6	1.6	13.7	1.9 – 2.2	1.9	-1	1.6	28.5	0.043	-7.89

$$^{*}FOM = 20log_{10}\left(\frac{IIP3[mW]\times Gain[lin]\times BW[GHz]}{P_{dc}[mW]\times(NF[lin]-1)}\right)$$ in [6]

3.5 Conclusion

This chapter has theoretically and experimental described a wide-band noise-cancelling LNA using source-follower-based feedback to enhance both gain and NF. Calculated,

simulated and measured results are highly consistent with each other. Measured results show a flat high gain and a flat low NF across the bandwidth compared with existing wideband LNAs. With excellent FOM, the proposed LNA is suitable for multi-standard receiver and high speed applications.

4. A 1-to-20-GHz Triple-Path Noise-Cancelling Common-Gate Common-Source LNA with Complementary nMOS-pMOS Configuration

4.1 Introduction

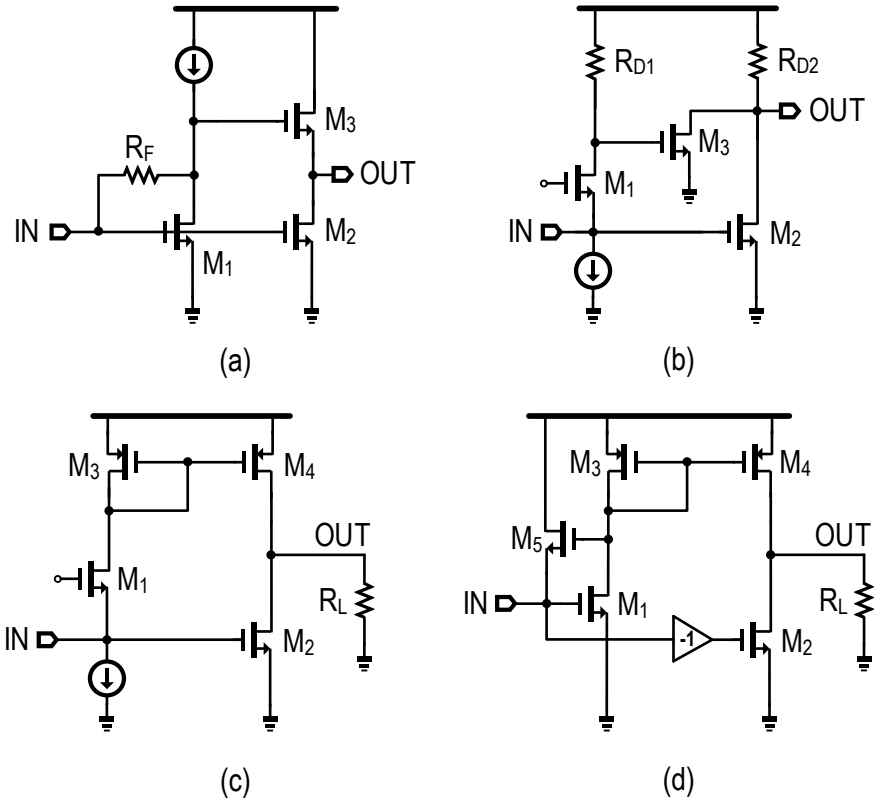


Fig. 4.1. NC LNAs. (a) Resistive feedback topology. (b) CG topology. (c) CG topology with current-mirror combination network. (d) Shunt- feedback topology with current-mirror combination network.

Wideband circuits are promising for multi-standard radios [32]-[33] and high-speed communications [34]. The wideband low-noise amplifier (LNA) is a key building block of wideband receivers dominating their power consumption and sensitivity performance. Many wideband LNAs have been reported, e.g. to cover the 3.1 to 10.6 GHz band ultra-

wideband (UWB) communication. Recently, [35]-[40] have aimed to push the LNA's bandwidth (BW) beyond 20 GHz. Yet, wideband input matching (S11) is challenging due to the parasitic capacitance of the CMOS devices; and the input impedance at high frequencies which can be heavily affected by its imaginary part, rendering the impedances at DC and high frequency very different from each other. In fact, S11 <-10 dB could not be achieved in a few works targeting 20 GHz [35]-[37]. The trade-off between S11 and the noise figure (NF) also imposes design challenges.

Noise cancelling (NC) is known for breaking the trade-off between S11 and NF. Without the concern of the noise contribution from the input matching transistor, S11 can be optimized with one additional degree of freedom. S11 can be easily designed below -10 dB with NC [4]-[6][11][21][41]-[49]. The NC LNA is categorized into two major types: resistive feedback and common gate (CG) based on input-matching method. Generally, the resistive-feedback NC LNA [Fig. 4.1(a)] provides higher and flatter gain than that in the CG configuration. The third-order distortion current of the input transistor can be cancelled in the same way as the noise current. Yet, the input third-order intercept point (IIP3) performance of the resistive-feedback NC LNA is less satisfactory [6], [11]. IIP3 is vital to LNAs whose BW is as wide as 20 GHz, because many other signals can intermodulate with each other and generate a third-order interference within the 20-GHz range of interest. Wideband LNAs in [6] and [11] report an IIP3 of ~-4 dBm. However, it is insufficient to suppress the inter-modulation due to the increased co-existence of adjacent blockers or transmitter on-chip leakage [21], [41]. The NC LNA adopting a CG configuration [Fig. 4.1(b)] can be employed for high linearity performance. In [21], a stacked pMOS and nMOS configuration as the input matching stage is combined with

noise cancellation based on a CG configuration to obtain an excellent IIP3. By properly biasing the transistors, the distortion components generated by pMOS and nMOS will cancel each other and improve IIP3 [50]. The NC LNA [42], [43] combines current mirror with CG, as shown in Fig. 1(c) and (d), to avoid distortions caused by voltage-to-current conversion and to improve IIP3. Fig. 1(c) shows a CG-based NC LNA using a current mirror, while Fig. 1(d) combines a common source (CS) feedback configuration with current mirror. Regrettably, due to the addition of a cascode transistor as a current mirror, the voltage headroom becomes constrained and a power supply as high as 2.2 V is necessary [43]. Moreover, [42] and [43] only accomplish a BW of 1.9 and 1.1 GHz, respectively. To obtain a good IIP3 across 20-GHz BW remains a challenge in the current state-of-the-art.

This chapter reports a wideband LNA which utilizes a π network reaching an input matching BW up to 20 GHz. We combine a resistive feedback structure with a CG-based NC configuration to improve S11, S21, and NF. The adoption of a stacked nMOS-pMOS configuration allows current-reuse and IIP3 improvement. Due to the pMOS and nMOS topology, the noise from the input transistors can be cancelled through three, instead of conventionally two, forward-feed paths. With an active area of 0.096 mm^2 and power of 20.3 mW, the proposed prototype realized in 65-nm CMOS shows an attractive FOM [6] of 22.7.

Section 4.2 introduces the proposed wideband LNA, followed its implementation details in Section 4.3. Section 4.4 analyzes the effect of the resistive feedback, triple-path NC mechanism and IIP3 improvement. Section 4.5 summarizes the measurement results. Finally, Section 4.6 draws the conclusions.

4.2 Proposed Wideband LNA

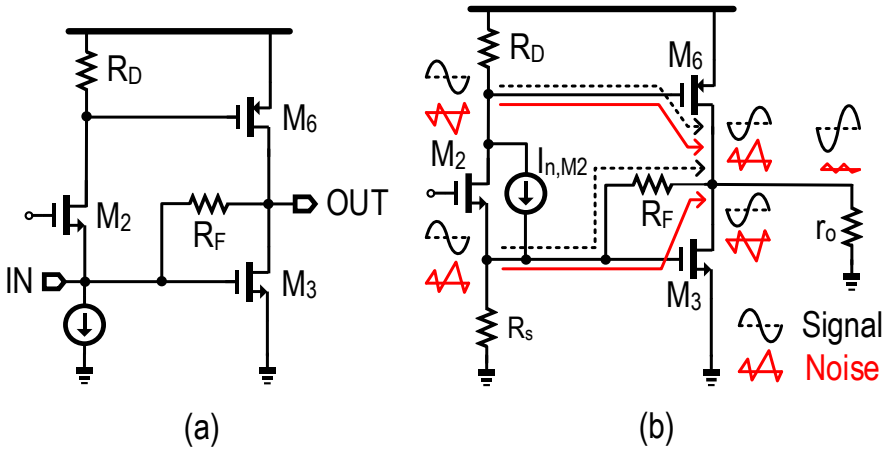


Fig. 4.2. (a) Proposed CG-based NC LNA with resistive feedback and push-pull output. (b) Its NC principle.

Fig. 4.2(a) shows the proposed CG-based NC LNA with a resistive-feedback auxiliary amplifier and a push-pull output. The feedback resistor (RF) improves input matching and in-band gain ripple, which will be detailed in Section IV. In our proposed topology, a single pMOS transistor (M6) is utilized to replace one nMOS transistor (M3) and one resistor (RD2) in a conventional CG-based NC LNA [Fig. 4.1(b)]. M6 together with M3 form a current-reused push-pull configuration at the output stage. When compared with current-mirror-based NC LNAs [Fig. 4.1(c) and 4.1(d)], which employ diode-connected transistor and consume large voltage headroom, the proposed LNA is more headroom-efficient.

Fig. 4.2(b) presents the NC principle of the propose wideband LNA. Herein, r_o is the equivalent resistance of the parallel-connected source-drain resistance of M3 and M6. The noise current of the input matching transistor (M2) generates opposite-polarity noise voltages at the source and drain of M2. The amplification by M3 and M6, respectively, inverts the polarity of both noise voltages. Thereafter, the noise voltages at the output

generated through the two paths have opposite polarities and cancel each other. Signal voltage as input located at the source of M2 travels to the output via two paths. The first path is through the M2 and then M6. The second path is through the resistive-feedback CS amplifier formed by M3. Both paths invert the signal voltages, adding them up at the output. Unlike the auxiliary amplifiers in the conventional CG-based NC LNA [Fig. 4.1(b)], which uses two nMOS transistors (M2 and M3), we employ the push-pull configuration (M6 and M3).

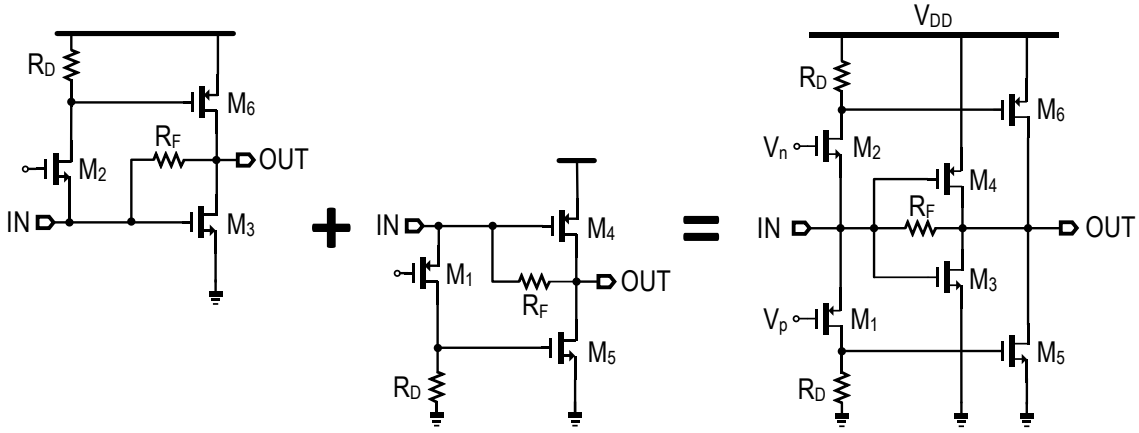


Fig. 4.3. Evolution from individual nMOS-pMOS configurations to stacked nMOS and pMOS architecture with the dual push-pull output.

Fig. 4.3 shows how the introduction of pMOS facilitates the evolution of the basic architecture to a pMOS and nMOS complimentary configuration. The CG-configured M1 and M2 form the input matching stage. M3, M4, and RF become an inverter forming the 1st auxiliary amplifier. M5 and M6 are CS-configured, creating the 2nd and 3rd auxiliary amplifiers, respectively. After evolution, push-pull and current reuse has been achieved at M3-and-M4 as well as at M5-and-M6 stage. Moreover, multiple works [21], [42], [50] have indicated that a complimentary pair will benefit the linearity performance of the

amplifier. The impact of the evolved pMOS and nMOS complimentary structure on IIP3 of the proposed LNA will be discussed in detail in Section IV.

4.3 Wideband LNA Design Details

Fig. 4.4 exhibits the implementation of the proposed wideband LNA. We obtain the input π network with the matching capacitor and inductor, C_m and L_m, respectively, as well as the parasitic capacitor C_x at node X. We add a testing buffer to drive the output capacitance and to provide output matching. To ensure good linearity, the testing buffer, which is the last stage, adopts resistive-degeneration configuration (R_{deg}). R_L is the 50-ohm load resistor and C_L is the pad capacitor. L_B is series connected to the drain of the buffer transistor to alleviate the effect of C_L on the BW of the LNA core. We insert L_o in the front of the testing buffer to broaden the BW of the signal at its gate. Further, C_y and C_b are parasitic capacitances at node Y and at the gate-source capacitance of M_b, respectively.

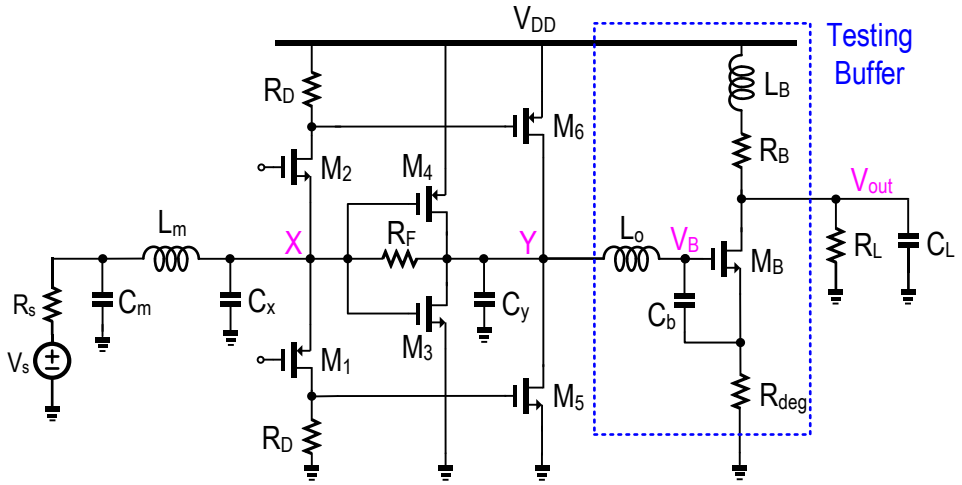


Fig. 4.4. Implementation of the proposed wideband LNA in Fig. 4.3.

4.3.1 Wideband Input Matching

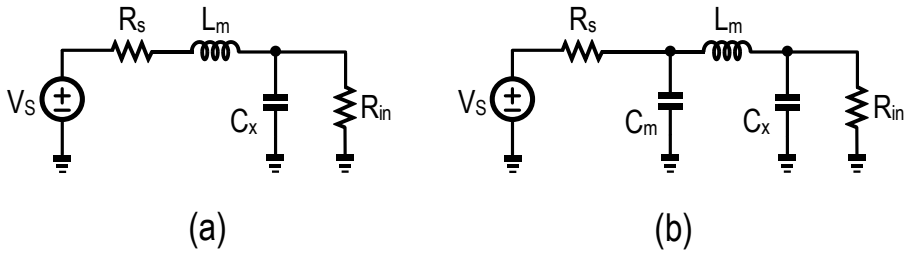


Fig. 4.5. Wideband input matching based on (a) L network and (b) π network.

The limiting factor in broadband input matching is the parasitic capacitor of the input transistor, which deteriorates matching at high frequency. Fig. 4.5(a) shows the common method to broaden the frequency of input matching which is the addition of a series inductor before the input transistor [4], [12]. C_x is the gate-source capacitance of the input transistor and R_{in} is the input resistance, approximated to $1/g_m$, generated by the CG amplifier. The resulting input impedance is,

$$Z_{in} = \frac{L_m C_x R_{in} s^2 + L_m s + R_{in}}{C_x R_{in} s + 1} = \frac{-L_m C_x R_{in} \omega^2 + j\omega L_m + R_{in}}{j\omega C_x R_{in} + 1} \tag{4.1}$$

By referring to (4.1), at a moderately high frequency, the second term $j\omega L_m$ in the numerator cancels the effect of $j\omega C_x R_{in}$ in the denominator to a certain extent. Yet, as the frequency increases to an even higher value the effect of the first term $L_m C_x R_{in} \omega^2$ in the numerator begins to merge and the condition of input matching degrades again. Thus, only introducing L_m limits the improvement of the matching range. A π network can be formed when C_m is considered before L_m as Fig. 4.5(b) illustrates. Then, the input impedance can be rewritten as,

$$Z_{in} = \frac{L_m C_x R_{in} s^2 + L_m s + R_{in}}{L_m C_m C_x R_{in} s^3 + L_m C_m s^2 + (C_m + C_x) R_{in} s + 1} \tag{4.2}$$

Assuming R_{in} designed as 50 ohm, i.e. $R_{in} = R_s$, and solving the frequencies corresponding to $Z_{in} = R_s$, will lead to,

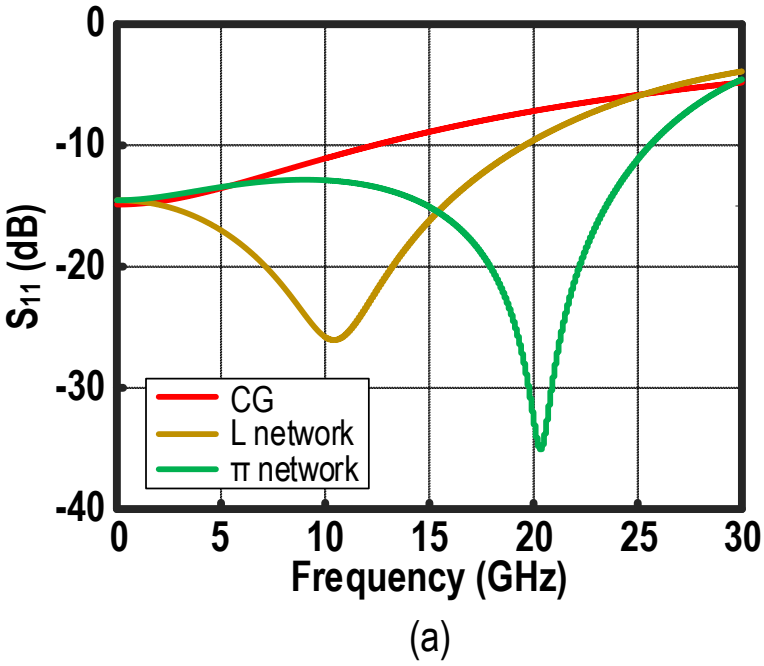
$$s[L_m C_m C_x R_{in}^2 s^2 + L_m R_{in}(C_m - C_x)s + (C_m + C_x)R_{in}^2 - L_m] = 0 \quad (4.3)$$

For simplicity, C_m is equal to C_x and the solution is,

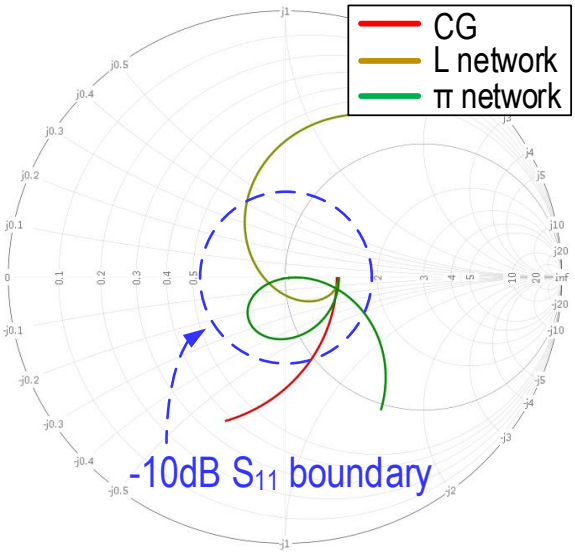
$$\omega_1 = 0 \quad (4.4a)$$

$$\omega_2 = \sqrt{\frac{2}{L_m C_x} - \frac{1}{R_{in}^2 C_x^2}} \quad (4.4b)$$

Based on (4.4b), apart from DC, there is another frequency where perfect matching can be obtained. By carefully optimizing the value of L_m, ω_2 can reach a very high frequency and allowing a 20-GHz matching feasible.



(a)



(b)

Fig. 4.6. S_{11} of a typical CG configuration with various matching networks in (a) dB format and (b) Smith Chart format.

Let us assume that the CG stage itself provides a reasonable S_{11} of -15 dB at DC. Fig. 4.6 plots the S_{11} under $C_m = C_x = 120fF$ and $L_m = 500pH$, by using simply the CG

configuration, S_{11} is less than -10 dB for only 12 GHz. While by adding L_m, the input matching frequency range approaches 19 GHz. With the π network, the input matching range is further extended to 26 GHz, ensuring S_{11}<-10 dB beyond 20 GHz.

In Fig. 4.4, the resistance R_{in_LNA} looking into the sources of matching stage transistors (M_1 and M_2) can be derived as,

$$R_{in\_LNA} = \frac{R_F + r_o}{2g_{m1}(R_F + r_o + g_{m5}R_D r_o) + 2g_{m3}r_o + 1} \tag{4.5}$$

where $r_0 = r_{03}||r_{04}||r_{05}||r_{06}$, r_{03}, r_{04}, r_{05} and r_{06} are the source-drain resistance of M_3, M_4, M_5 and M_6, respectively. g_{mx} is the transconductance of M_x (x=1 to 6), and we can assume that $g_{m1} \approx g_{m2}$, $g_{m3} \approx g_{m4}$ and $g_{m5} \approx g_{m6}$ to simplify the following analysis. R_D is the load resistor series connected to the drain of the CG stage. R_F is a feedback resistor between the gate and the source of the inverter formed by M_3 and M_4. Its effect on input matching, gain as well as NF will be discussed in detail in Section 4.4.1. In this case considering $R_{in\_LNA} = R_S$ and $C_m = C_x$, S_{11} becomes,

$$|S_{11}| = \left|\frac{-L_m C_m^2 R_S^2 s^3 + (L_m - 2C_m R_S^2)s}{L_m C_m^2 R_S^2 s^3 + 2L_m C_m R_S s^2 + (L_m + 2R_S^2 C_m)s + 2R_S}\right| \tag{4.6}$$

Further, C_x in Fig. 4 is the total parasitic capacitance, including the source-drain capacitance of M_1, M_2, M_3, and M_4 at node X. S_{11} calculation results based on (4.6) will be plotted later in Fig. 4.19(a) in Section 4.5.

4.3.2 Frequency Response of S_{21}

Referring to Fig. 4.4, the forward gain of the LNA can be divided into two parts: the first provided by the matching network A_0 (from V_s to V_X) and the second by the core of the

LNA A_v (gain from V_X to V_B). By referring to the small-signal equivalent circuit of Fig. 4.7, the voltage gain from node Y to the gate of the testing buffer transistor is given by,

$$\frac{V_B}{V_Y} = \frac{C_b R_{deg} s + g_{mb} R_{deg} + 1}{L_o C_b s^2 + C_b R_{deg} s + g_{mb} R_{deg} + 1} \tag{4.7}$$

where g_{mb} and C_b are the transconductance and gate-source capacitor of M_B, respectively. R_{deg} is the degeneration resistor. L_o, the inductor series connected to the gate of M_B, keeps the LNA's BW from being deteriorated by the parasitic capacitance at node Y. Equation (4.7) assumes that the source drain resistor of M_B, r_b, is large, such that Z_{out} has little impact on V_B/V_Y. Then, the voltage gain from node Y to X becomes,

$$\frac{V_Y}{V_X} = -\frac{2g_{m1}g_{m5}R_D R_F + 2g_{m3}R_F - 1}{Z_y + R_F} Z_y \tag{4.8a}$$

where

Z_y

$$= \frac{r_o\left(L_o C_b s^2 + R_{deg} C_b s + g_{mb} R_{deg} + 1\right)}{L_o C_b C_y r_o s^3 + \left(C_b C_y R_{deg} r_o + L_o C_b\right)s^2 + \left[C_b\left(R_{deg} + r_0\right) + C_y r_0\left(1 + g_{mb} R_{deg}\right)\right]s + g_{mb} R_{deg} + 1} \tag{4.8b}$$

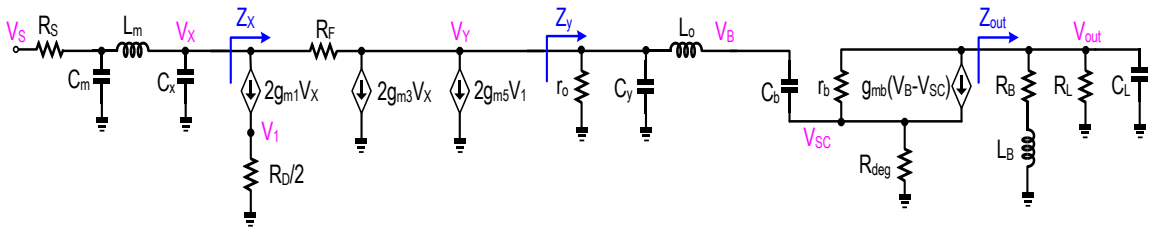


Fig.4.7. Small-signal equivalent circuit for S_{21} calculation.

Z_y is the total impedance at node Y and C_y is the total parasitic capacitance at node Y. Therefore the gain of the LNA's core, which is the gain from node X to the gate of the

testing buffer, becomes,

$$A_v = \frac{V_B}{V_Y}\frac{V_Y}{V_X} = -\frac{C_b R_{deg} s + g_{mb} R_{deg} + 1}{L_o C_b s^2 + C_b R_{deg} s + g_{mb} R_{deg} + 1}$$

$$\cdot \frac{2g_{m1} g_{m5} R_D R_F + 2g_{m3} R_F - 1}{Z_y + R_F} Z_y \tag{4.9}$$

On the other hand, the voltage gain matching network A_0 is given by,

$$A_0 = \frac{V_X}{V_S}$$

$$= \frac{1}{L_m C_m C_x R_s s^3 + L_m (C_m R_S Y_x + C_x) s^2 + (L_m Y_x + C_x R_s + C_m R_s) s + R_s Y_x + 1} \tag{4.10a}$$

where

$$Y_x = Z_x^{-1} = 2g_{m1} + \frac{2g_{m1} g_{m5} R_D Z_y + 2g_{m3} Z_y + 1}{R_F + Z_y} \tag{4.10b}$$

Herein, Y_x is the inverse of the impedance Z_x. S_{21} is twice the voltage gain in a 50 ohm system with impedance matching and given by,

$$S_{21} = 2A_0 A_v \tag{4.11}$$

S_{21} calculation results based on (4.11) will be plotted in Fig. 4.19(b) in Section 4.5.

4.3.3 Frequency Response of NF

The major noise sources in the LNA are the channel thermal noise from M_1, M_2, M_3, M_4, M_5 and M_6, as well as the thermal noise from R_D and R_F. Fig. 4.8 shows the small-signal equivalent circuit of Fig. 4.4 for noise calculation. Furthermore, the transfer function of the noise current source to the Y node are the same for M_3, M_4, M_5 and M_6, Thus, Fig. 4.8 only exhibits one of the four noise current sources. The same applies for M_1 and M_2.

The noise factor contribution of M_1 is given by,

$$F_{M1} = \frac{g_{m1}}{R_s|A_0A_v|^2}\frac{\gamma}{\alpha}\left|\frac{Z_y[g_{m5}R_D(Z_S+R_F)+Z_S-2g_{m3}R_FZ_S]}{R_F+Z_y+Z_S+2g_{m1}g_{m5}R_DZ_yZ_S+2g_{m1}R_FZ_S+2g_{m1}Z_SZ_y+2g_{m3}Z_yZ_S}\right|^2 \quad (4.12a)$$

where

$$Z_S = \frac{L_mC_mR_Ss^2+L_ms+R_S}{L_mC_mC_xR_Ss^3+L_mC_xs^2+R_SC_xs+1} \quad (4.12b)$$

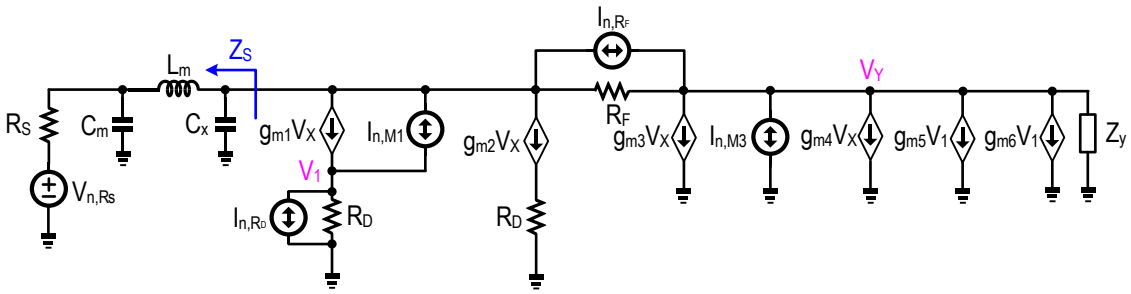


Fig. 4.8. Small-signal equivalent circuit for NF calculation.

Fig. 4.8 also shows that Z_S is the impedance looking towards the source from the parasitic capacitor C_x. γ is the coefficient of the channel noise and $\alpha = g_{m1}/g_{d0}$, where g_{d0} is the zero-bias drain conductance. Equation (4.12a) reveals that we can achieve a perfect NC $g_{m5}R_D\left(1+\frac{R_F}{Z_S}\right)+1 = 2g_{m3}R_F$, and it also shows that the left side is a complex number and the right side is a real number. Then, a perfect NC cannot be achieved, however, a good approximation will be $\Re[g_{m5}R_D\left(1+\frac{R_F}{Z_S}\right)+1] = 2g_{m3}R_F$. Plus, the transfer functions from $I_{n,M1}$ and $I_{n,M2}$ to the node Y are equal. A similar case is true for $I_{n,M2}$, $I_{n,M3}$, $I_{n,M4}$ and $I_{n,M5}$. The contribution of M_2, M_3, M_4, M_5 and M_6 for the noise factor is given by,

$$F_{M2} = \frac{g_{m2}}{g_{m1}} F_{M1} \tag{4.13}$$

$$F_{M3} = \frac{g_{m3}}{R_s |A_0 A_v|^2} \frac{\gamma}{\alpha} \left| \frac{Z_y (2 g_{m1} R_F Z_S + Z_S + R_F)}{2 g_{m1} g_{m5} R_D Z_y Z_S + 2 Z_y Z_S (g_{m1} + g_{m3}) + 2 g_{m1} R_F Z_S + R_F + Z_y + Z_S} \right|^2 \tag{4.14}$$

$$F_{M4} = \frac{g_{m4}}{g_{m3}} F_{M3} \tag{4.15}$$

$$F_{M5} = \frac{g_{m5}}{g_{m3}} F_{M3} \tag{4.16}$$

$$F_{M6} = \frac{g_{m6}}{g_{m3}} F_{M3} \tag{4.17}$$

Apart from the transistor channel thermal noise, the thermal noise from resistors R_D and R_F are also taken into consideration. The noise factor contribution from R_D and R_F can be obtained as follows,

$$F_{RD} = \frac{1}{R_D R_s |A_0 A_v|^2} \left| \frac{g_{m5} R_D Z_y (2 g_{m1} R_F Z_S + R_F + Z_S)}{2 g_{m1} g_{m5} R_D Z_y Z_S + 2 Z_y Z_S (g_{m1} + g_{m3}) + 2 g_{m1} R_F Z_S + R_F + Z_y + Z_S} \right|^2 \tag{4.18}$$

$$F_{RF} = \frac{1}{R_F R_s |A_0 A_v|^2} \left| \frac{R_F Z_y (2 g_{m1} g_{m5} R_D Z_S + 2 Z_S g_{m3} + 2 Z_S g_{m1} + 1)}{2 g_{m1} g_{m5} R_D Z_y Z_S + 2 Z_y Z_S (g_{m1} + g_{m3}) + 2 g_{m1} R_F Z_S + R_F + Z_y + Z_S} \right|^2 \tag{4.19}$$

Lastly, by taking the parasitic resistor (R_m) of L_m into account, the overall noise factor results in,

$$F = 1 + \frac{R_m}{R_S} + F_{M1} + F_{M2} + F_{M3} + F_{M4} + F_{M5} + F_{M6} + 2F_{RD} + F_{RF} \tag{4.20}$$

We will plot the NF calculation results based on (4.20) in Fig. 4.19(c) in Section 4.5.

4.4 Design Considerations and Simulation Results

Fig. 4.9 shows the complete schematic of the proposed wideband LNA, where we use capacitors C_{i1}, C_{i2} and C_{i3} for DC-decoupling in the forward path and voltages V_n, V_p, V_{n2}, V_{p2} and V_B to bias the transistors M_2, M_1, M_5, M_6 and M_B, respectively. We use an off-chip DC block at the input in order to maintain the internal bias condition of the LNA core protected from any external circuitry interference. Fig. 4.9 is the source for our analysis below.

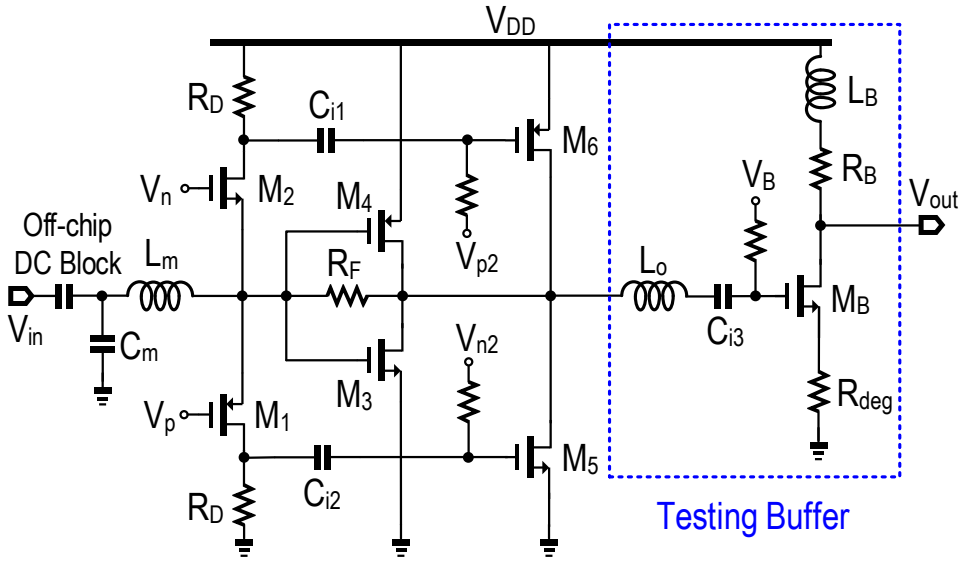


Fig. 4.9. Complete schematic of the proposed wideband LNA.

Table 4.1
Dimension of Devices II

M_1	10.5μm/65nm	M_2	5μm/65nm
M_3	48μm/65nm	M_4	88μm/65nm
M_5	16μm/65nm	M_6	27.2μm/65nm
M_B	45μm/65nm	R_F	1kΩ
R_D	293Ω	R_B	54Ω
L_m	0.5nH	L_o	0.9nH
L_B	1.5nH	C_m	120fF

4.4.1 Effects of R_F

Based on (4.5), the utilization of R_F increases the input transconductance by introducing the term $(2g_{m3}r_0 + 2g_{m1}g_{m5}R_Dr_0 + 1)/(R_F + r_0)$. Without R_F, i.e. R_F equal to infinity, a larger g_{m1} is required in order to reach the same input matching condition. In Fig. 4.10(a), we plot S_{11} under the situations where we only use CG and various values of R_F in addition to CG. Considering a CG-only situation, we adjust the size of M_1 and M_2 to obtain the same DC matching condition as when R_F is 1 kΩ. However, larger sizes of M_1 and M_2 produce larger parasitic capacitance, and further results in a degradation of S_{11} at higher frequency. By comparing S_{11} in 3 different situations with R_F equal to 500 Ω, 1 kΩ and infinity, we can observe that a smaller R_F will lead to a better S_{11}, but the effect of R_F on S_{21} and NF still needs to be studied to find an adequate value of R_F.

Plotted in Fig. 4.10(b), we compare S_{21} under different circumstances where we only use CG and various values of R_F in addition to CG. Under a CG-only situation, due to the increase of the size of the input transistors for matching purposes, the BW reduces significantly. Based on (4.9), the term $(2g_{m1}g_{m5}R_DR_F + 2g_{m3}R_F - 1)/(Z_y + R_F)$ indicates that the introduction of R_F will lower the gain of the proposed LNA. Such a gain becomes lower as R_F decreases in Fig. 4.10(b), but R_F can be used to facilitate a flatter in-band gain variation by reducing gain at lower frequency. This can be explained by the fact that R_F is a real impedance and it has higher influence on the gain in a lower frequency range than at higher frequency. Therefore, by choosing the value of R_F properly, we can broaden the LNA's BW, reducing the in-band gain variation, while maintaining a moderate gain around 13 dB simultaneously.

Considering a CG-only situation, due to the poor input matching at high frequency and

the large gain difference between low frequency and high frequency, NF [Fig. 4.10(c)] goes up rapidly with frequency. With the introduction of R_F, we obtain a better input matching and flatter gain, leading to a flatter NF across frequency. Yet, Fig. 4.10(b) and (c) show a trade-off between a low NF and a flat gain. To obtain a balance between a low NF and a flat gain, we need to increase the value of R_F until the in-band gain variation reaches 2 dB. We set a 1-dB margin to cater for process variations and choose R_F as 1 kΩ for the proposed LNA.

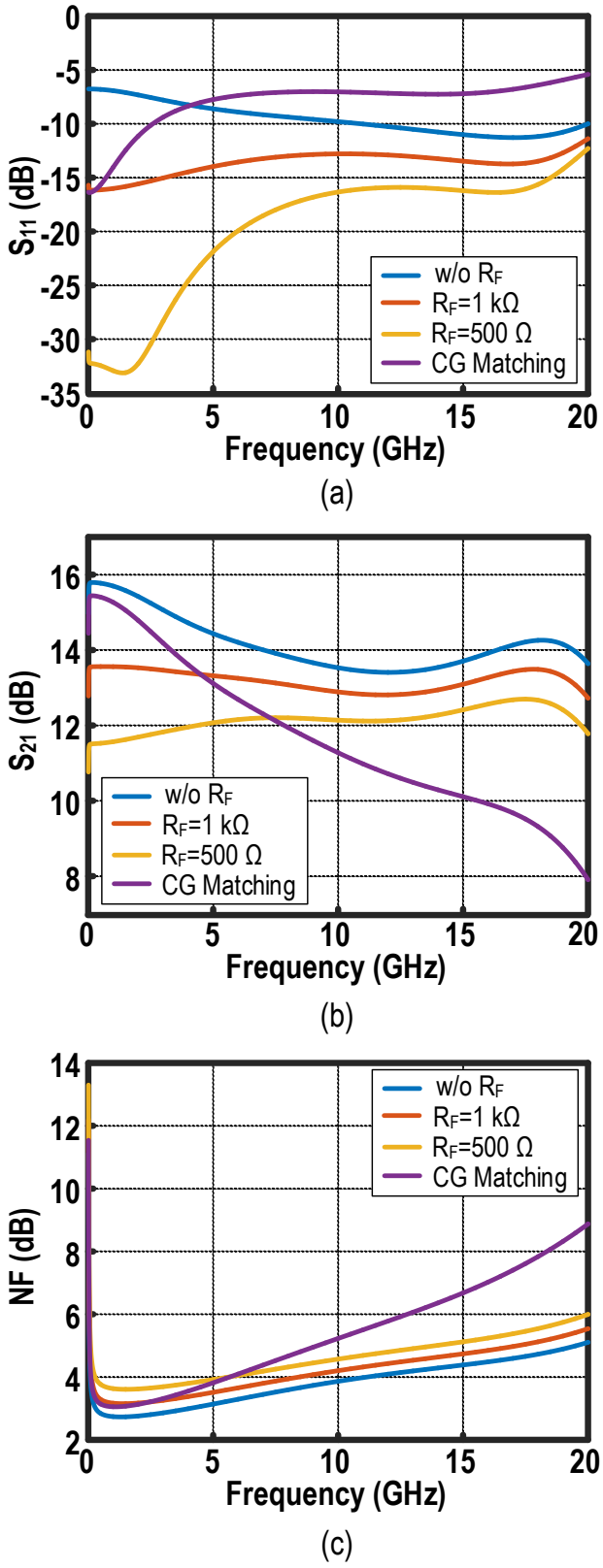


Fig. 4.10. Impact of R_F on (a) S_{11}, (b) S_{21} and (c) NF.

4.4.2 Triple-Path NC

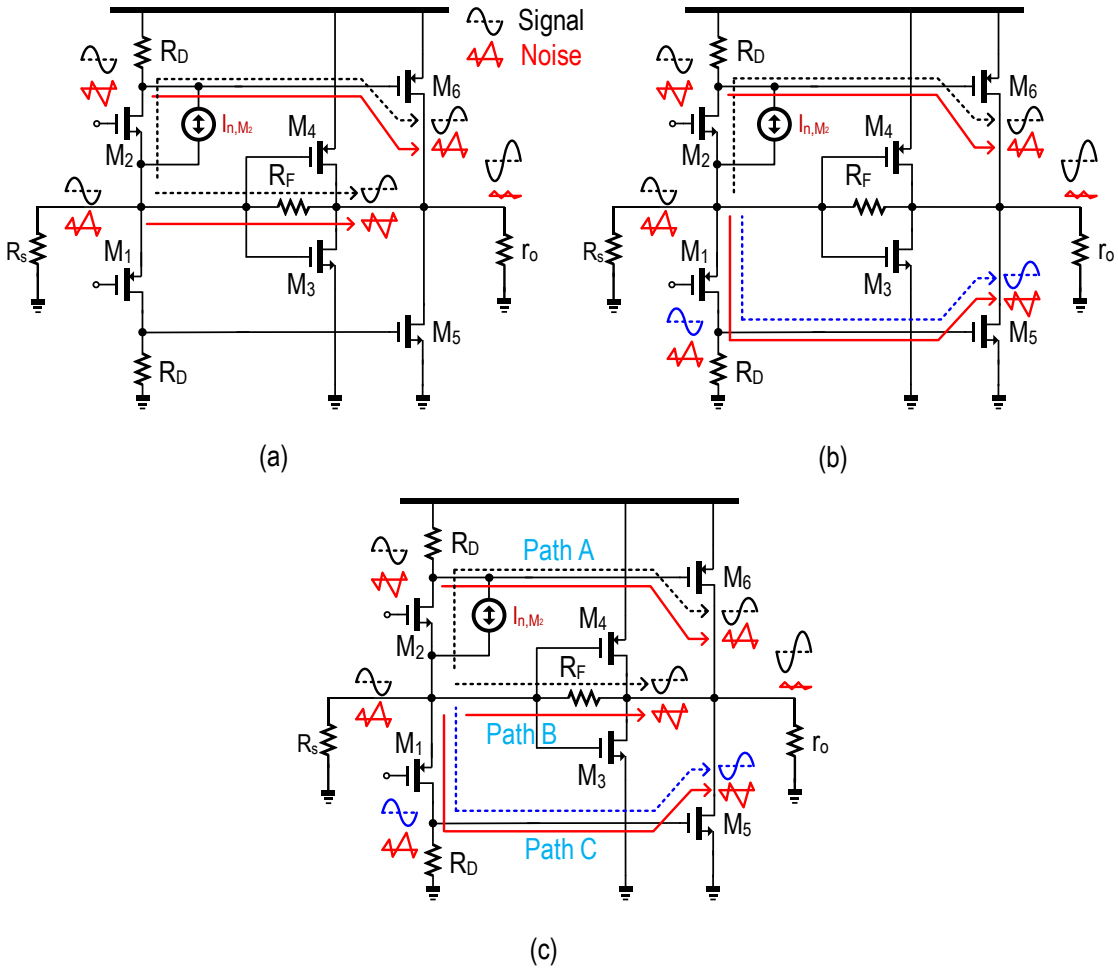


Fig. 4.11. (a) Conventional, (b) additional third-path and (c) overall NC mechanism in the proposed wideband LNA.

Fig. 4.11(a) shows how to realize conventional NC in CG-based NC LNA. The channel thermal noise of M_2 generates two off-phase noise voltages at the drain and source of M_2. The two noise voltages are both sources inverted and cancel each other due to their off-phase polarity. In the proposed LNA, we create an additional NC path with M_1 and M_5, as Fig. 4.11(b) illustrates. Parts of $I_{n,M2}$ flows through M_1 and R_D and it produces a noise voltage at the drain of M_1, which has an opposite phase to the noise voltage at the drain of M_2. These two noise voltages are both sources inverted by pMOS and cancel each

other at the output. Fig. 4.11(c) plots the overall NC scheme. The noise voltage generated by $I_{n,M2}$ through M_6 (path A) is cancelled by the noise through a conventional NC path, M_3 and M_4 (path B), as well as the noise through an extra NC path, M1 and M5 (path C) in the proposed design. On the other hand, signal voltages generated through all the three paths (A, B and C), have the same polarity and add up at the output. Fig. 4.12 shows the small-signal equivalent circuit used to study the NC mechanism in the proposed wideband LNA. We add an AC current source $I_{ac,M2}$ across the drain and source of M_2 to emulate its channel thermal noise. We studied the effect of the additional NC path across 0 to 20 GHz by comparing the noise current flowing through M_5 and M_6. Transfer functions $H_{n,A}$ and $H_{n,C}$ can be defined as,

$$I_{n,M6} = H_{n,A} I_{n,M2} \tag{4.21a}$$

where

$$H_{n,A} = -\frac{g_{m6}R_D\left(R_D Z_y Z_S g_{m2} g_{m6} + 2Z_y Z_S g_{m3} + Z_y Z_S g_{m2} + R_F Z_S g_{m2} + Z_S + Z_y + R_F\right)}{R_F + Z_y + Z_S + 2g_{m2}g_{m6}R_D Z_y Z_S + 2g_{m2}R_F Z_S + 2g_{m2}Z_S Z_y + 2g_{m3}Z_y Z_S} \tag{4.21b}$$

$$I_{n,M5} = H_{n,C} I_{n,M2} \tag{4.22a}$$

and

$$H_{n,C} = \frac{g_{m5}g_{m2}R_D Z_S(g_{m6}R_D Z_y + Z_y + R_F)}{R_F + Z_y + Z_S + 2g_{m2}g_{m6}R_D Z_y Z_S + 2g_{m2}R_F Z_S + 2g_{m2}Z_S Z_y + 2g_{m3}Z_y Z_S} \tag{4.22b}$$

Herein $I_{n,M5}$, and $I_{n,M6}$ are the noise current flowing through M_5 and M_6 respectively. Further, we define $H_{n,AC}$ as the sum of $H_{n,A}$ and $H_{n,C}$:

$$H_{n,AC} = H_{n,A} + H_{n,C} \tag{4.23}$$

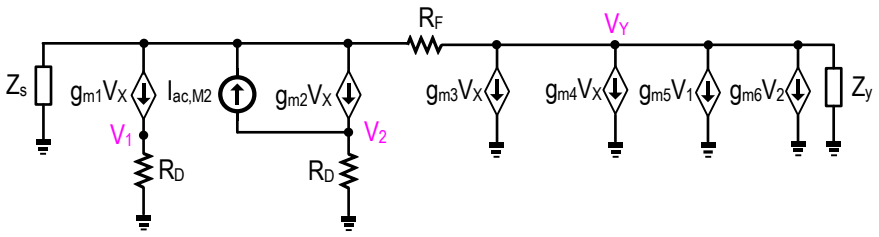


Fig. 4.12. Small-signal equivalent circuit for triple-path NC effect.

According to (4.21b) and (4.22b), $H_{n,A}$ and $H_{n,C}$ have opposite polarity, indicating that they can cancel each other. Fig. 4.13(a) displays the simulated and calculated $H_{n,A}$, $H_{n,C}$ and $H_{n,AC}$. We obtained the simulation results by setting $I_{ac,M2}$ to unity and plotting the drain current from M_5 and M_6. Noise current from the additional NC path (path C) cancels part of the noise current through M_6 (path A). This is supported by the fact that $H_{n,AC}$ is lower than $H_{n,A}$ across the entire BW in both the calculation and the simulation. Similarly, noise from pMOS M_1 is also cancelled by the additional NC path (path A in this case), and the cancellation effect is also supported by both calculation and simulation [Fig. 4.13(b)].

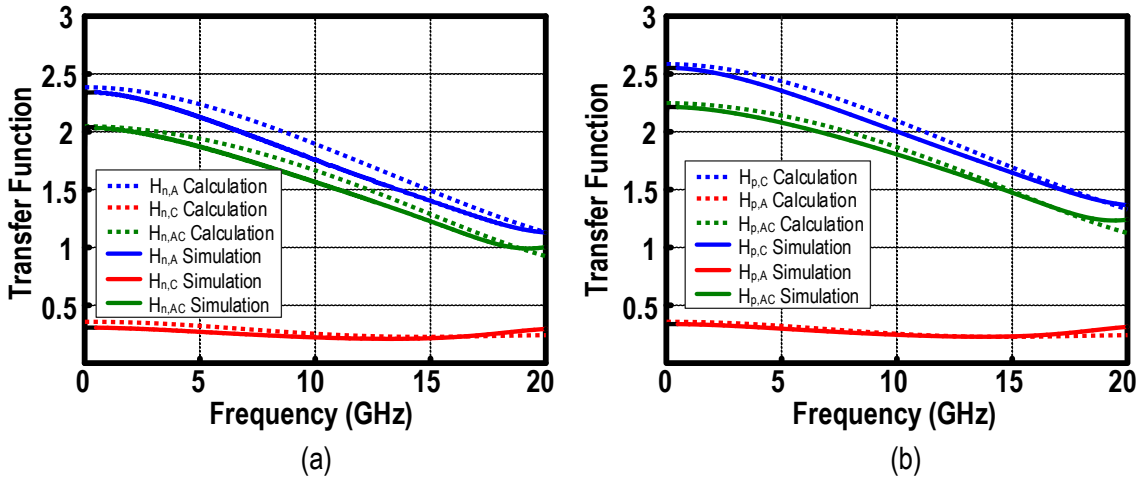


Fig. 4.13. Additional third-path NC effect on the channel thermal noise of (a) nMOS M_2 and (b) pMOS M_1.

After noises through M_5 and M_6 cancel each other, the remaining noise is then cancelled by the noise through M_3, M_4 and R_F (path B). Based on Fig. 4.12, the noise through path

B can be expressed by,

$$I_{n,M3} + I_{n,M4} + I_{n,RF} = H_{n,M34} I_{n,M2} \tag{4.24a}$$

where

$$H_{n,B} = \frac{g_{m5} R_D Z_y + 2 g_{m3} R_F Z_S + 2 g_{m3} g_{m5} R_D Z_S Z_y - Z_S}{R_F + Z_y + Z_S + 2 g_{m2} g_{m6} R_D Z_y Z_S + 2 g_{m2} R_F Z_S + 2 g_{m2} Z_S Z_y + 2 g_{m3} Z_y Z_S} \tag{4.24b}$$

$I_{n,M3}$, $I_{n,M4}$ and $I_{n,RF}$ are the noise current flowing through M_3, M_4, and R_F, respectively. Thereafter, the overall transfer function of $I_{n,M2}$ to the output becomes,

$$H_{M2,overall} = H_{n,AC} + H_{n,B}$$

$$= -\frac{g_{m5} R_D (Z_S + R_F) + Z_S - 2 g_{m3} R_F Z_S}{R_F + Z_y + Z_S + 2 g_{m1} g_{m5} R_D Z_y Z_S + 2 g_{m1} R_F Z_S + 2 g_{m1} Z_S Z_y + 2 g_{m3} Z_y Z_S} \tag{4.25}$$

Furthermore, (4.25) is consistent with (4.12a). Fig. 4.14 (a) and (b) show the overall NC effect of noise caused by M_2 and M_1, respectively. We can define the cancel ratio (CR) to evaluate the NC effect as,

$$CR = 1 - \frac{|H_{n,AC} + H_{n,B}|}{|H_{n,AC}|} \tag{4.26}$$

We obtain a good NC effect for both M_1 and M_2 at DC as CR is equal to 1. CR for M_1 and M_2 remains a minimum value of 0.5 and 0.43 over 20-GHz BW, respectively.

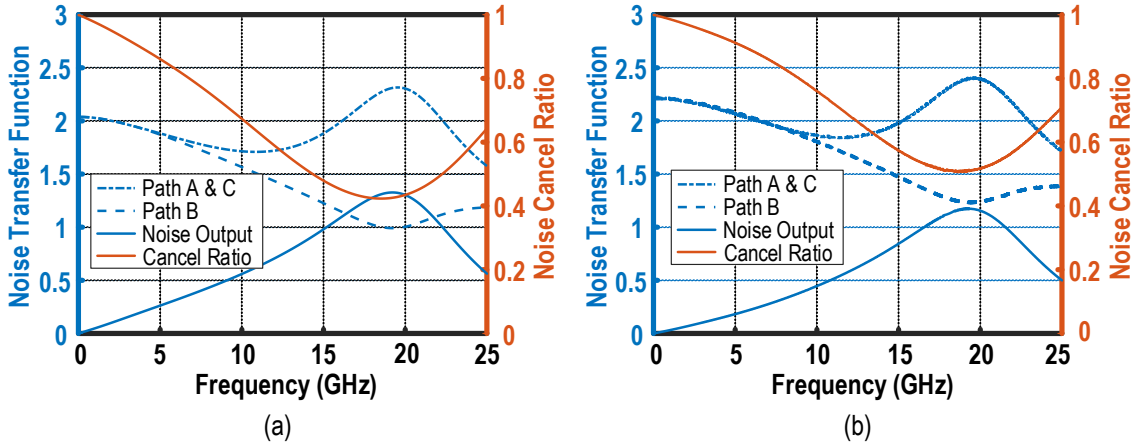


Fig. 4.14. Overall NC ratio of channel thermal noise of (a) nMOS M_2 and (b) pMOS M_1.

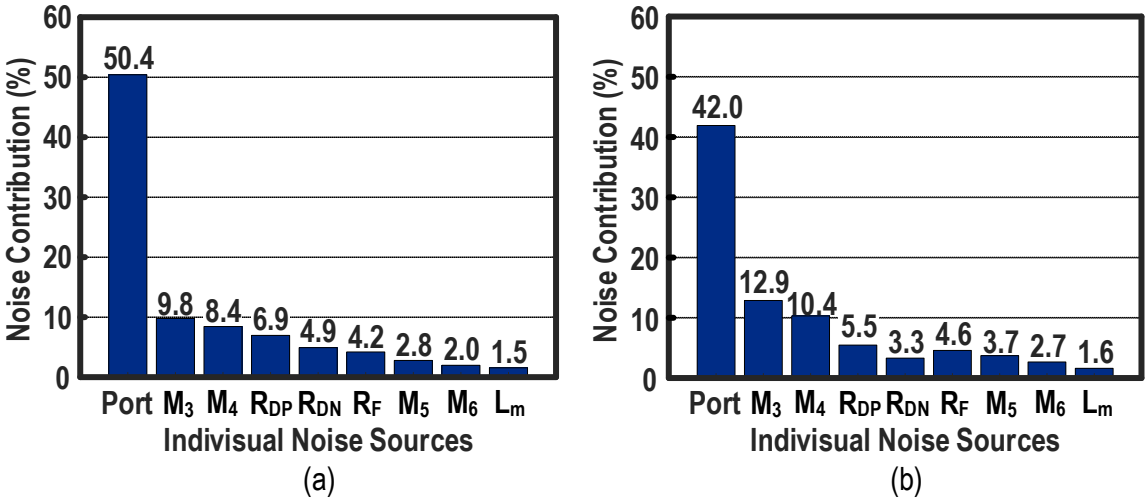


Fig. 4.15. Simulated relative noise contributions by individual components at (a) 2 GHz and (b) 10 GHz.

Fig. 4.15(a) and (b) show a summary of the major noise contribution sources at 2 and 10 GHz, respectively. R_{DN} and R_{DP} are the resistors connected to the drain of M_2 and M_1, respectively. Noise contributions from M_1 and M_2 are too low to be listed due to a good NC effect at both low and high frequency. By looking at the source resistor noise contributions, the simulated NF are 2.88 dB at 2 GHz and 3.58 dB at 10 GHz, respectively, showing an increase of 0.7 dB across the 8-GHz range.

4.4.3 Partially Distortion Cancelling

We apply a partial distortion cancellation which focus on the neutralization of the first and second derivative of the transconductance of M_5 and M_6. A complimentary pMOS and nMOS pair can have a low second-order and third-order distortion under specific bias conditions. Fig. 4.16 presents the small-signal equivalent circuit of Fig. 4.9 for IIP3 analysis. The study of the partial distortion cancellation focuses on the core of the LNA, which starts from V_X to V_Y. g_{m12} is the sum of g_{m1} and g_{m2}, g_{m34} is the sum of g_{m3} and g_{m4}, and g_{m56} is the sum of g_{m5} and g_{m6}. We use an analysis approach similar to [21] and [42].

Distortions of the transistors are considered up to the third-order. Applying Kirchoff's current law at node V_1 and node V_Y, we obtain,

$$\begin{cases} V_1 = \dfrac{R_D}{2}\left(g_{m12}V_X + \dfrac{g'_{m12}}{2}V_X^2 + \dfrac{g''_{m12}}{6}V_X^3\right) \\ \dfrac{V_X - V_Y}{R_F} = g_{m34}V_X + \dfrac{g'_{m34}}{2}V_X^2 + \dfrac{g''_{m34}}{6}V_X^3 + g_{m56}V_1 + \dfrac{g'_{m56}}{2}V_1^2 + \dfrac{g''_{m56}}{6}V_1^3 + \dfrac{V_Y}{Z_Y} \end{cases} \tag{4.27}$$

where g'_{mi} and g''_{mi} (i takes 12, 34 and 56) are the first and second derivatives of the transconductance of the complementary pair M_1&M_2, M_3&M_4, and M_5&M_6, respectively. By solving (27), the relationship between V_X and V_Y becomes,

$$V_Y = -\frac{Z_y}{8(Z_y + R_F)}\left(A_1V_X + A_2V_X^2 + A_3V_X^3\right) \tag{4.28a}$$

where

$$A_1 = 4R_DR_Fg_{m12}g_{m56} + 8R_Fg_{m34} - 8 \tag{4.28b}$$

$$A_2 = R_D^2R_Fg_{m12}^2g'_{m56} + 2R_DR_Fg'_{m12}g_{m56} + 4R_Fg'_{m34} \tag{4.28c}$$

$$A_3 = \frac{1}{6}R_D^3R_Fg_{m12}^3g''_{m56} + R_D^3R_Fg_{m12}g'_{m12}g'_{m56} + \frac{2}{3}R_DR_Fg''_{m12}g_{m56} + \frac{4}{3}R_Fg''_{m34} \tag{4.28d}$$

Therefore, IIP3 of the core of the LNA is

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|} \tag{4.29}$$

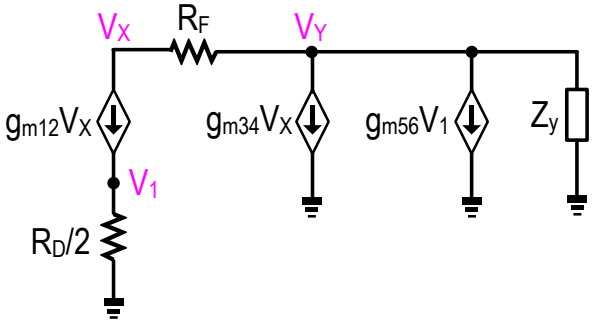


Fig. 4.16. Small-signal equivalent circuit for IIP3 analysis

According to (4.28d) and (4.29), g'_{m56} and g''_{m56} are directly related to IIP3. Small values of g'_{m56} and g''_{m56} under the proper bias voltage can improve the linearity performance.

Fig. 4.17 (a), (b) and (c) show the simulated g_{m56}, g'_{m56} and g''_{m56} versus the gate bias voltage (i.e. $V_{BP2} = V_{BN2} = V_{B2}$). At around $V_{B2} = 0.86V$, we obtain a good accumulation effect of g_{m5} and g_{m6}, leading to a maximum total transconductance for the M_5 and M_6 stage. Moreover, we achieve a good cancellation of g'_{m5} and g'_{m6}, resulting in a g'_{m56} close to zero. Although g''_{m56} is not exactly zero at this bias voltage, a clear cancellation of g''_{m5} and g''_{m6} can be observed at $V_{B2} = 0.86V$ in Fig. 4.17(c). In Fig. 4.17(d), simulated IIP3 of the proposed wideband LNA reaches a maximum value of 5 dBm at $V_{B2} = 0.88V$, which is consistent with the analysis above.

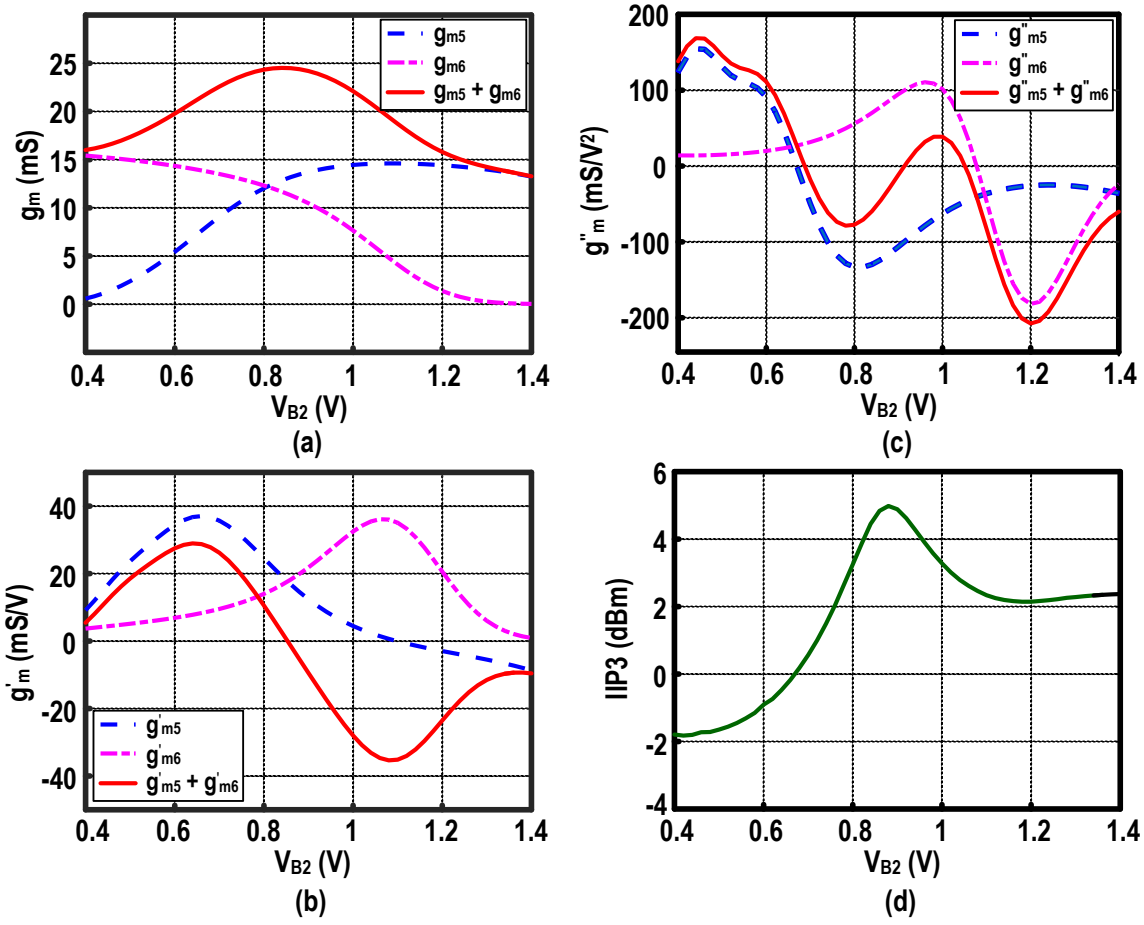


Fig. 4.17. (a) Transconductance, (b) First-order derivatives of the transconductance of the complementary forward stage. (c) Second-order derivatives of the transconductance of the complementary forward stage and (d) IIP3.

We will detail the simulation results of the proposed LNA later. The pre-simulation and post-simulation denote the schematic and post-layout simulation with the parasitics, respectively. We observe a good consistency between the calculated and simulated results, indicating the validity of our analysis and design approach

4.5 Measurement Results

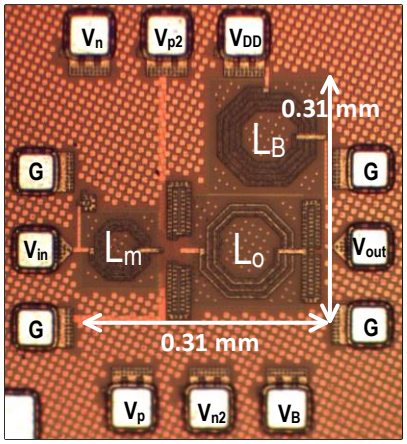
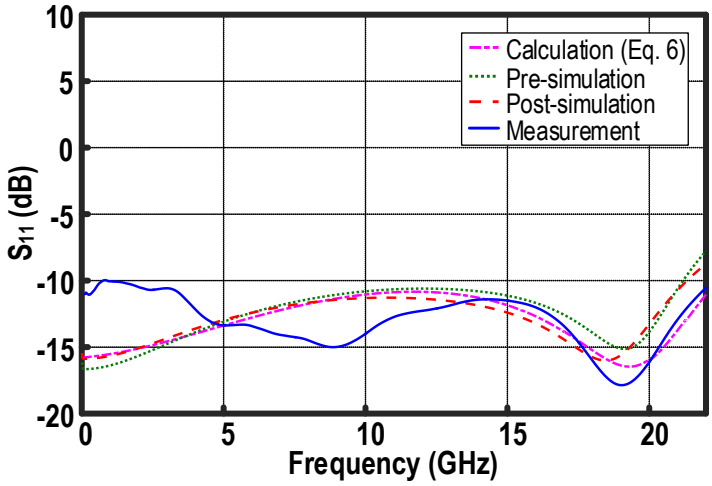


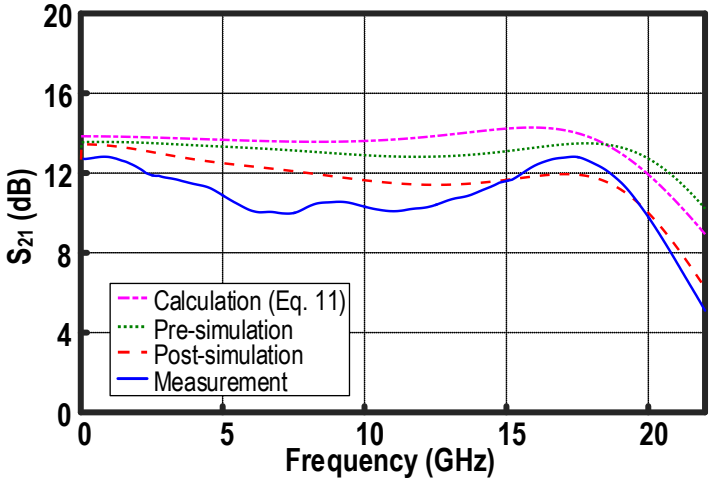
Fig. 4.18. Die photo of the fabricated wideband LNA.

Fig. 4.18 shows the die photo of the wideband LNA implemented in 65-nm CMOS occupying a compact die area of 0.31×0.31 mm^2. We conducted the measurement using an Agilent Vector Network Analyzer (N5245A). The prototype draws 12.6 mA from a supply voltage of 1.6 V, consuming a power of 20.1 mW. Fig. 4.19 compares the calculated, simulated and measured results of S_{11}, $S_{21,}$ and NF of the proposed wideband LNA. S_{11} is below -10 dB up to 23 GHz. S_{11} shows a dip at around 19 GHz, indicating the effect of the π network. In Fig. 4.19(b), the peak of S_{21} is 12.8 dB with a 3-dB BW of 19 GHz, from 1 to 20 GHz. Measured NF_{min} and NF_{max} are 3.3 dB at 3.5 GHz and 5.3 dB at 13.5 GHz, as Fig. 4.19(c), illustrates, respectively. In-band variation of NF is only 2 dB

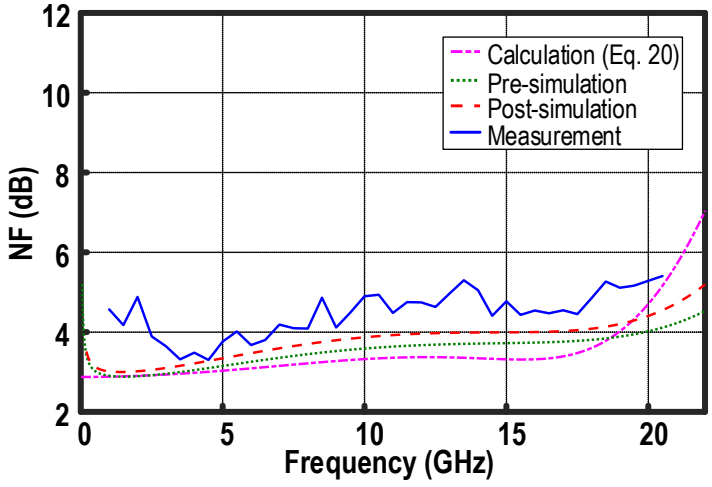
from 1 to 20 GHz, which is competitive with the state-of-the-art. The calculated results derived in Section III are consistent with the simulated and measured results. Fig. 4.20(a) shows that the measured IIP3 is 5.8 dBm, when we apply two-tone signals at 5 and 5.1 GHz. Fig. 4.20(b) shows that the measured IIP3 at different center frequencies (2, 5, 10, 15 and 20 GHz) with space Δf=100 MHz is always larger than 0 dBm. The results show also a good linearity performance across a wide range of frequencies.



(a)



(b)



(c)

Fig. 4.19. Calculated, simulated and measured (a) NF, (b) S_{11} and (c) S_{21} versus frequency.

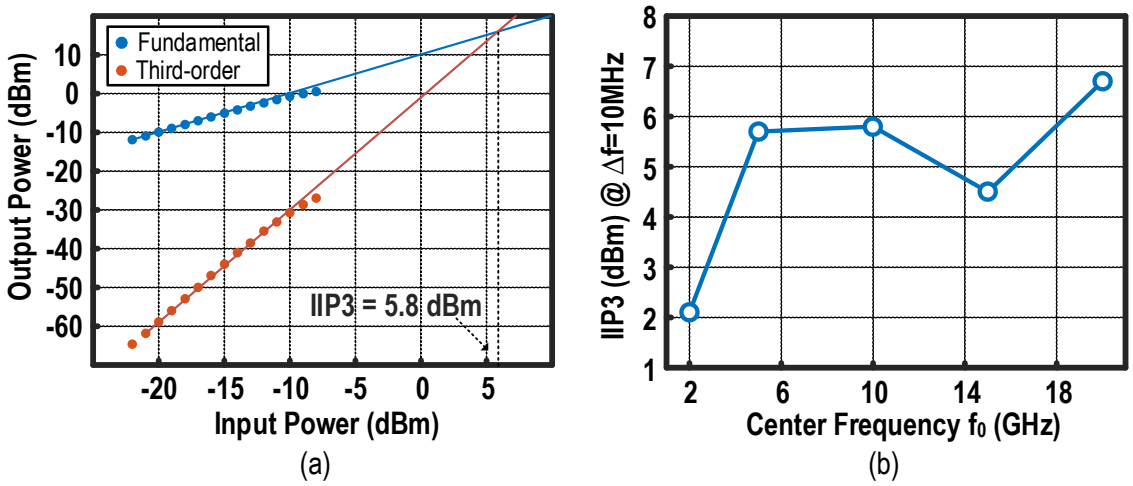


Fig. 4.20. (a) Measured IIP3 for two-tone inputs of 10 and 10.01 GHz. (b) Measured IIP3 versus center frequency (f_0).

Table 4.1 benchmarks the performance of the proposed wideband LNA with prior arts. The prototyped wideband LNA has an NF flatness of 0.1 dB/GHz, which is competitive with other wideband works in the table. NF flatness is characterized as $(NF_{max} - NF_{min})/BW$, which captures how fast NF increases over a certain range of frequency. Although [38] reports a superb NF flatness, it needs a larger area and an RF choke at the output, which is usually infeasible in a full receiver integration. This work also has a moderately low NF, better IIP3 and more compact area compared to other LNAs whose upper -3-dB frequency (f_{-3dB}) is higher than 10 GHz [37]-[40], [51]-[54]. Wideband LNAs based on GaAs and SiGe have either very high gain [55], [56], or very wide BW [57]. However, their FOM is inferior to our work due to their poor linearity or high power consumption. [42] and [58] also use linearity enhancement techniques and achieve better IIP3 than our work, however, the proposed wideband LNA achieves a very wide BW, which is more than ten times wider than the BW of [42] and [58]. To summarize Table 4.1, our proposed wideband LNA is a very promising topology due to very wide bandwidth, low-and-flat NF, high linearity and better overall FOM.

TABLE 4.2

PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART II.

	CMOS Technology	Freq. Range (GHz)	BW (GHz)	Gain (dB)	NF (dB)	NF Flatness (dB/GHz)	IIP3 (dBm)	Power (mW)	Area (mm^2)	FOM*
This Work	**65nm**	**1 – 20**	**19**	**12.8**	**3.3 – 5.3**	**0.10**	**5.8**	**20.3**	**0.096**	**22.7**
Upper f_{-3dB} larger than 10 GHz										
[37] TMTT'10	130nm	0.1 – 14	13.9	12.4	2.7 – 3.7	0.07	0	21	0.009	10.1
[38]TMTT'10	90nm	1.6 – 28	26.4	10.7	2.9 – 3.2	0.01	4	21.6	0.14	20.9
[39] RFIC'09	90nm	DC – 22.1	22.1	10.7	4.3 – 6.6	0.10	-2.67	8.4	0.131	9.1
[40] MWCL'09	90nm	0.1 – 20	19.9	12.7	3.3 – 5.5	0.11	-2.5	20.4	0.35	6.4
[51] ISSCC'09	130nm	DC – 12	12	15	2.3 – 4.5	0.18	1	26	0.38	13.4
[52] TMTT'11	90nm	3.0 – 10	7	12.5	3.0 – 7.0	0.57	-3^	7.2	0.64	6.3
[53] TMTT'13	180nm	2.2 – 12.2	10	13	1.9 – 2.6	0.07	-0.1	7.4	1.11	20.6
[54] CICC'08	130nm	0.8 – 10.6	9.8	16	3.4 – 5.6	0.22	1.6	14.4	0.84	14.4
Linearity enhancement used										
[42] JSSC'17	180nm	0.1 – 2	1.9	17.5	2.9 – 3.5	0.31	10.6	21.3	0.63	21.8
[58] TCASII'13	180nm	DC – 1.3	1.3	10	2.9 – 3.2	0.23	7.5	18	0.07	2.62
NC technique used										
[11] TCASII'18	65nm	0.5 – 7	6.5	16.8	2.9 – 3.8	0.14	-4.5	11.3	0.044	3.57
[48] TCASII'17	90nm	2.0 – 5.0	3	13	6.0 – 8.0	0.67	-9.5	1.8	0.72	-11.1
[49] TCASI'10	130nm	0.2 – 3.8	3.6	13	2.8 – 3.4	0.17	-4.2	5.7	0.025	1.47
[59] JSSC'16	130nm	0.6 – 4.2	3.6	14	4.0 – 9.0	1.39	-10	0.25	0.39	13.6
Non-CMOS										
[55] TCASI'18	GaAs 150nm	0.1 – 20	19.9	28.6	3.1 – 5.8	0.13	-11.6&	505	1.53	-23.0
[56] MWCL'17	SiGe 130nm	0.3 – 15	14.7	37.3	1.8 – 2.2	0.03	-27.3&	52	0.46	-22.5
[57] TMTT'11	GaAs 500nm	0.5 – 43.5	43	8.5	4.2 – 22	0.41	9.5&	225	2	8.9
Others										
[60] VLSI'15	90nm	0.1 – 7.0	6.9	12	5.5 – 6.5	0.14	-9	0.75	0.23	5.2
[61] TCASI'17	130nm	1.2 – 6.6	5.4	14	1.8 – 3.8	0.37	3.8	13.2	0.32	19.6

* $FOM = 20log_{10}(\frac{IIP3[mW]\times Gain[lin]\times BW[GHz]}{P_{dc}[mW]\times(NF[lin]-1)})$ in [11]; & Calculated from OIP3; ^ Calculated from P_{1dB}.

4.6 Conclusion

This chapter presented an attractive architecture for wideband LNAs which target high linearity and wide BW around 20 GHz. The effect of the feedback resistor, triple-path noise cancellation, and dual complementary topology has been detailed in depth. Realized in 65-nm CMOS, the prototype shows a BW of 19 GHz, an NF of 3.3 dB and an IIP3 of 5.8 dBm, while only occupying an active area of 0.096 mm^2. Measurement results agree well with the calculation and simulation, and the achieved FOM is favorable with respect to the state-of-the-art.

5. Conclusion and Recommendations

5.1 Conclusion

This thesis focuses on the design and implementation of the CMOS low-noise amplifiers for wideband applications. The noise cancelling technique, which releases the trade-off between input matching and noise figure, is employed in these designs. Two wideband input matching configurations, namely resistive feedback architecture and common-gate architecture are used together with noise cancellation. Both configurations are demonstrated to be eligible for wideband LNA design.

Firstly, a wideband resistive-feedback noise cancelling low noise amplifier with an additional source-follower-based (SFB) feedback is presented. SFB feedback can overcome the trade-off between input matching and gain. A larger feedback resistor can be realized in the resistive-feedback network, leading to a higher gain while maintaining good input matching. Noise contributions from feedback resistor and noise cancelling transistors are also significantly reduced, yielding a lower overall noise figure. Fabricated in a 65nm CMOS process, the wideband LNA achieves a flat S_{21} of 16.8 dB, a flat NF of 2.87-3.77 dB and S_{11} below -10 dB over a 3-dB bandwidth of 0.5-7 GHz. It consumes a DC power of 11.3mW from a 1.2-V supply and occupies an active area of only 0.044mm^2. Since the SFB feedback technique is not only limited to wideband applications, it can be commonly applied in a conventional resistive feedback design.

Secondly, a common-gate noise cancelling LNA employing PNMOS as distortion cancellation is proposed. By proper sizing and biasing the PNMOS pairs in input common-gate stage as well as in auxiliary amplifiers, the second-order distortion current

in NMOS and PMOS transistors cancel each other. Due to the cascade/feedback configuration in noise-cancelling LNAs, cancellation of second-order distortion also improves third-order linearity, yielding good IIP3 performance. Fabricated in a 65nm CMOS process, the wideband LNA achieves an S_{21} of 12.8 dB, a flat NF of 3.3-5.2 dB and S_{11} below -10 dB over a 3-dB bandwidth of 1-20 GHz. It shows an IIP3 larger than 5 dBm across the entire 19 GHz bandwidth and the highest measured IIP3 is 12.7 dBm. As shown in Table 4.1, works aiming for 20 GHz achieves IIP3 less than 0 dBm. However, it is crucial for wideband LNAs to achieve high IIP3, preventing in-band intermodulation interference. This works shows an excellent IIP3, enabling it for wideband applications.

Two wideband LNAs are presented in 65nm CMOS technology. These prototypes are very useful for wideband applications aiming for multi-standard and high-speed purposes. Simulation and measurement results are presented and compared with state-of-arts. Both works show better FOM than current literature.

5.2 Recommendations for further research

For these two designs, although post-layout simulation has been performed to ensure the simulation results match the measurement results, there are still some differences between the two, especially for the second design presented in chapter 4. It could be caused by the inaccuracy of the model of inductors provided in foundry's PDK. Future researchers are highly recommended to design their own inductors and extract their s-parameters using electro-magnetic simulations. This will improve the consistency between simulation and measurement results. Furthermore, the gate inductor L_1 in chapter 3 and L_m in chapter 4 contributes 0.5% and 1.6% to the total noise, respectively.

Noise contributed by inductors is usually caused by their parasitic resistors. Self-designing of inductor can be beneficial in controlling the parasitic resistor value and hence improves circuit's overall noise performance. More study on the design of inductors could be done in future works.

Although many wideband LNA works in literature do not report IIP2 performances, for LNA, whose BW is close to 20 GHz as presented in chapter 4, IIP2 could be important for evaluating the linearity performance of the circuit. In chapter 4, the pMOS-nMOS pair improves IIP3 by minimizing the second-order distortion generated by the transistor pair. So, in theory, this should also improve IIP2 performance. Future researchers could study more the second-order intermodulation of the wideband LNA in detail. Plus, the IIP2 performance could be verified through on-wafer measurement.

The second LNA design proposed in this thesis requires bias tuning to achieve a good IIP3. However, in industry and real product, this could be difficult. Future study can focus on designing a bias circuit that is robust to process and temperature variations. Another way to address the issue is to design a programmable bias circuit that can be used to calibrate the IIP3 performance of LNA.

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