

NANYANG
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**Analysis and Design of An
Adaptive-supply Class H Audio
Power Amplifier for Mobile Devices**

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

June 2017

Acknowledgement

First of all, I would like express sincere gratitude to my Ph.D. advisor Associate Professor Siek Liter for his kind guidance during my graduate study. I am grateful not only for his generosity in sharing with me his knowledge and insightful ideas, but also for the support he provided throughout the years. His wisdom in dealing with difficulties and challenges will benefit me for my future study and work.

Also, I would like to thank senior Ph.D. students from our lab: Sun Zhuochao, Howard Tang, Kok Chiang Liang, Wang Jiacheng, Zhu di, Xiao Zhekai and Kong Junjie, for their helps and discussions along the way, from computer setups at the very beginning to chip testing and paper writing. The path could not have been smooth without their support.

I would like to thank my Ph.D. cohorts: Wang Dong, Koay Kuan Chuang, Low Qiong Wei, Aaron Cai Qing Wei, Zhou Mi, Jia Meng, Teh Jian Sen, Jiang Jize, Liu Xu and Yu Chengyue, for the beneficial discussions on research and experiments. Particularly, I want to thank Wang Dong, Koay Kuan Chuang and Jiang Jize who generously helped me on the chip measurement setup with equipment from their own group.

I also want to thank the technicians in our labs: Mr Sia Liang Poo, Mr David Robert Neubronner, Ms Lim-Tan Gek Eng and Ms Quek-Gan Siew Kim, for their hardwork in maintaining VIRTUS IC design lab a nice place for us graduate students.

Last but not least, I am so grateful to have the support from my parents and my beloved wife. Your love and encouragement are the most precious things I have owned.

Abstract

In recent years, the market of consumer electronics has witnessed a growing demand for portable devices with high-fidelity audio playback functionality. For battery-powered devices like smart phones, smart watches and tablets, their form factor as well as weight keep on shrinking to enable the good portability required by the customers. As a result, the board space left for the battery is likely to be further reduced. On the other hand, more functional blocks are expected to be integrated into the system which will deplete the battery even more quickly. Therefore, low quiescent power and high power efficiency have become key performance metrics for audio amplifiers designed for portable applications.

Switched mode amplifiers such as class D amplifier have been quite popular in the market of audio amplifiers. Its switching nature minimizes the conduction loss of the output stage and hence high power efficiency is achieved. However, it is generally considered inferior in linearity as compared to its linear amplifier counterparts. More importantly, the switching noise generated at the output stage will cause electromagnetic interference (EMI) problems which may affect the performance of other Radio Frequency (RF) blocks. Besides, its output filter is comprised of huge inductor and capacitor which increases the implementation cost. Therefore, this research project focuses on the development of high linearity, high efficiency linear amplifiers for audio applications.

In order to enhance the power efficiency of a typical linear amplifier, e.g. class AB amplifier, emphasis should be drawn on the conduction losses at the output stage. The supply voltage is usually determined based on the requirement of the output voltage swing. However, when the output swing becomes small, there will be substantial amount of voltage drops across the power transistors which ultimately leads to conduction losses. As a straightforward solution, class G amplifier which uses two different supply rails for the output stage is proposed. However, the power efficiency is still low once the higher supply rail is selected. To further optimize the power efficiency, we proposed a novel class H architecture

which operates with only single-rail supply. The supply to the output stage is designed to be adaptive to the instant input signal level so that the voltage drop across the power transistor is kept constant. Therefore, compared with other linear amplifier architectures (class B/AB/G), the proposed design features much better overall power efficiency.

An existing issue with the above-mentioned adaptive-supply amplifiers is the additional distortions that occur during mode switching. For class G topology when the switching threshold is reached, the supply voltage sees step changes during the low to high transitions. These abrupt changes tend to add distortions to the outputs of the amplifier. Therefore, for conventional adaptive-supply amplifiers, there is a sudden burst in the Total Harmonic Distortion (THD) when the high supply starts operating. In this research, we proposed a common-mode modulation (CMM) scheme to resolve this problem. Instead of changing the system configuration upon the triggering of mode switching, the amplitude information of the input signal is extracted and embedded into the common-mode (CM) voltage of the output. As the CM voltage cancels out at the output stage, this scheme yields a much more smooth transition during mode switching, and no additional distortion is added to the output signal.

To validate the proposed amplifier architecture, a prototype of the design was fabricated in the 0.18- μm CMOS process. Measurement results show that the proposed amplifier achieves 80.4% peak power efficiency which is the highest among all linear amplifiers in the literature. In the intermediate output power range it demonstrates more than 25% higher power efficiency as compared to class AB and class G amplifiers. It also achieves a lowest THD+N value of -80.5 dB and no degradation on THD+N performance is observed during mode transition. Thus, the high linearity is preserved for the entire load range. Its quiescent power consumed by the whole system is 3.52 mW which is also significantly lower than the benchmark class H amplifier design due to the reduced circuit complexity.

Nomenclature

ADC Analog-to-Digital Converter

Audio CODEC Audio coder/decoders, which are a type of audio data converters that encode analog audio as digital signals and decode digital audio back into analog

BTL Bridge-Tied-Load

CCM Continuous Conduction Mode

CM Common Mode

CMC Current-Mode Control

CMFB Common Mode Feedback

COT Constant ON-Time

DCM Discontinuous Conduction Mode

DDA Differential Difference Amplifier

DR Dynamic Range

DSP Digital Signal Processing

EA Error Amplifier

EMI Electromagnetic Interference

EPP End-Point Prediction

ESR Equivalent Series Resistance

FCCM Forced Continuous Conduction Mode

FLL Frequency-Locked Loop

GBW Gain Bandwidth Product

GM Gain Margin

GSM Global System for Mobile communication

IAD Input Amplitude Detection

LDO Low Dropout Voltage Regulator

LHP Left-Half Plane

MC Miller Compensation

MIM Metal Insulator Metal

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NMC Nested Miller Compensation

NMCNR Nested Miller Compensation with Nulling Resistor

PAR Peak-to-Average Ratio

PFM Pulse-Frequency Modulation

PGA Programmable Gain Amplifier

PM Phase Margin

PSRR Power Supply Rejection Ratio

PWM Pulse-Width Modulation

RHP Right-Half Plane

RMS Root Mean Square

SMPS Switch Mode Power Supply

SMPS Switching Mode Power Supply

SNR Signal-to-Noise Ratio

SPL Sound Pressure Level

TDMA Time-division Multiple Access

THD+N Total Harmonic Distortion Plus Noise Ratio

VMC Voltage-Mode Control

ZCD Zero-Current Detection

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Chapter 1

Introduction

1.1 Background and Motivation

In recent years, there is a growing demand on the battery-powered electronic devices. These devices are ubiquitous in our daily life which cover people's needs for communication, data acquisition, entertainment, health monitoring and so forth. Audio processing unit, as one of those building blocks mounted on the battery-powered platform, is also going through evolutions from generation to generation. The requirements for audio unit has changed dramatically from basic requirements like two-way voice communication to more advanced functions like hi-fidelity music playback and stereo game sounds [1].

Audio power amplifier is an indispensable component in the audio processing unit. It amplifies the analog electronic signals within the audio frequency band (20 Hz to 20 kHz) and provides sufficient current to drive the external speaker or headphone. Although it seems that the design of audio amplifier has matured for several decades, new design challenges emerge for audio amplifier used in battery-powered systems [2, 3]. In a typical on-chip audio function unit, the audio signals are first processed in the digital domain. After going through filters and high precision digital-to-analog converters (DACs), they are eventually

fed into the audio amplifier as input signals. As the last stage from the digital audio input to the analog output, the linearity performance of the headphone amplifier determines the signal fidelity of this audio system. An important performance metric is the total harmonic distortion plus noise ratio (THD+N). It measures how much distortion and noise has been added to the amplified signal with respect to the original input. As mentioned previously, in order to alleviate the stringent power budget and achieve longer audio playback time, low quiescent power and high power efficiency are definitely desired for the audio amplifier. The power efficiency is defined as the ratio of useful power delivered to the headphone load compared to the power consumed from the battery. Another critical factor that the circuit designer has to consider is the amplifier's ability to suppress noise coming from the supply rail. Different from a stand-alone audio device like a MP3 player, a cellular phone is indeed a noisy environment for the audio amplifier. For instance, in a GSM system, the RF power amplifier switches periodically at a constant frequency of 217 Hz to transmit the TDMA bursts [4]. As different functional blocks are placed in close proximity for a compact board design, it is very likely that the power supply of the amplifier contains noise within the audio signal band. The third challenge is on the circuits' ability to reject supply noise, which is usually quantified by the power supply rejection ratio (PSRR). Last but not least, implementation cost is also a determining factor as eventually the design will be in production and the cost of it has to be competitive when compared to those already existed commercial products.

In summary, the above analysis generally delineates the requirements for the audio amplifier designed for a battery-powered system. An idealized solution should feature high linearity (very low THD+N ratio), low quiescent power, high power efficiency, high immunity to supply disturbances (high in-band PSRR) and low system complexity with less implementation cost at the same time.

The audio amplifiers available in the market can roughly be classified into two categories: the switched mode amplifier (class D-based) and the linear amplifier (class AB-based). This classification is based on the output stage topology. The power transistors in a class D amplifier are operated as switches connecting to either the supply or the ground. A train of square pulses are generated by modulation schemes which are similar to those used in the switch mode power supply (SMPS). The fundamental frequency component of the pulsating signal which is essentially the amplified signal can be recovered with the output filter. The most prominent advantage resulting from this switched nature is the high power efficiency. Ideally the energy is stored and transferred with passive components like inductor and capacitor, therefore the theoretical power efficiency can be 100%. Even with non-ideality like power transistor on-resistance and switching losses, its power efficiency can still exceed 85% easily. However, class D amplifiers are generally considered inferior to their linear amplifier counterparts in terms of linearity and power supply noise rejection, which is mainly due to the switching activities associated with the output stage. In some recent class D amplifier designs [5–7], with the help of high-order loop filters, very good THD+N ($\leq 0.02\%$) and PSRR performance (≥ 90 dB) are achieved.

However, to recover the original signal modulated with the high-frequency pulses, a bulky LC tank is needed at the output stage of a class D topology. The inductor used in a class D amplifier is usually large in value ($> 10\mu\text{H}$) and expensive [8]. As a result, the cost of class D amplifier is generally higher than linear amplifiers. Recently, some research works have been conducted on the filter-less class D topology where the LC filter is no longer needed [9–11]. However, such topology has many limitations on the speaker itself in the sense that the power amplifier must be in close proximity to the speaker. Secondly, the considerations on EMI (Electromagnetic Interference) issues further restrict the application of a class D amplifier. As the board space is premium, the designers are more motivated to eliminate the enclosure or shielding which are used to suppress adverse effect of EMI and switching noise [12]. As a consequence, a trade-off exists between the high fidelity

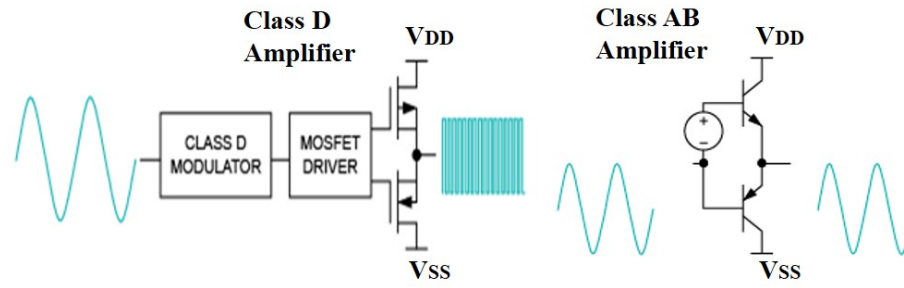


Figure 1.1: Comparison between a switched mode (class D) amplifier and a linear mode (class AB) amplifier

performance and low implementation cost for a class D amplifier. Thus, the linearity of class D amplifier is arguably comparable to its linear counterparts. Despite the high power efficiency of a class D amplifier, its intrinsic drawbacks make it generally not suitable for audio amplifier used in a battery-powered system. Therefore, the rest of this thesis will be focusing on the analysis and design of linear mode audio power amplifiers.

Fig 1.1 compares the different operation principle of a switched mode amplifier and a linear mode amplifier. Unlike switched mode amplifier where the gate control signals are pulsating, the gate of output stage transistors in a linear mode amplifier are controlled by analog signals from the preceding stages. Thus, the power transistors can still be viewed as voltage-controlled current sources instead of power switches. This ensures separation from the output terminal to the power supply. As a result, linear amplifier exhibits inherently better capability of supply noise rejection compared to switched amplifiers. As the name implies, linear amplifiers adopt continuous-time linear topology at the output stage, thus all transistors including the power transistors should be biased at the correct operation region. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which is the most widely-used semiconductor device in the present-day technology, requires a certain amount of voltage across its drain and source terminals in order to operate in the saturation region. These headroom voltages, however, contribute to conduction losses and reduce the power efficiency. As compared to the switched amplifier, it is evident that the overall power

efficiency of a linear power amplifier will become lower.

Class AB output stage is dominating in the selection of linear amplifier topology due to the minimization of crossover distortion as compared to class B topology and better efficiency as compared to class A topology. In view of the evolution of class AB amplifiers [4, 13–21], optimizations have been done in terms of frequency compensation, quiescent current control, reducing minimum operating voltage, enhancing PSRR and signal to noise ratio (SNR). Several designs have been dedicated for audio amplifiers in battery-powered system [4, 19–21]. The state-of-the-art design on class AB audio amplifier [4] has achieved THD+N of -95 dB, 120 dB PSRR and dynamic range (DR) of 111 dB. However, for all class AB audio amplifiers, one issue that cannot be circumvented is the low power efficiency. As much power is dissipated as heat at the output stage, the peak load power is limited otherwise heat sinks will be needed to alleviate the overheating problem. Among all those class AB candidates targeting for portable devices in the literature, the peak load power is capped up to 93.8 mW [20], which narrows its area of application as an audio power amplifier.

The basic concept for improving power efficiency of class AB amplifier is to minimize the conduction loss on power transistors. In other words, the culprit to low power efficiency is that the supply voltage to the output stage is unnecessarily high for amplifying an input signal with relatively small amplitude. Thus, if the supply voltage can be adjusted according to the input signal amplitude, the power efficiency can be much improved. This gives the motivation of designing an adaptive-supply power amplifier, in which the supply of the output stage is adjustable rather than fixed. Such kind of amplifiers are usually called the adaptive-supply power amplifiers, two examples of this concept are named as the class G and class H amplifiers. A class G amplifier senses the input signal amplitude and selects the proper supply voltages accordingly, the lower supply voltage reduces the conduction loss and improves the efficiency. However, once the triggering point is activated and the high supply voltage is selected, its advantage on efficiency over class AB topology diminishes. Therefore, the improvement on efficiency of class G amplifier is still marginal. In view

of the above analysis, it is highly desired to have a power amplifier that combines the advantages of a class AB and a class D amplifier. Reference [22] proposed a supply-tracking audio amplifier where a dc-dc converter is modulated to generate a variable supply voltage that keeps the power transistor headroom constant. The authors named their proposed amplifier as 'class I', however, the concept of their work is similar to the concept of a class H amplifier. Therefore, to avoid confusion on the naming, in the rest of this thesis the naming of such topologies will be unified as class H amplifiers. In the benchmark design, the circuit configuration is changed constantly depending on the instant signal amplitude. Therefore its linearity is jeopardized during large signal swing. As a result, the THD+N for supply-tracking mode is only 0.06%. This gives the research motivation of designing a novel architecture for such supply-tracking amplifier with better linearity performance.

1.2 Objectives

The main objective of this Ph.D. thesis focuses on the design and implementation of a class H adaptive-supply amplifier dedicated for audio applications in a battery-powered system. More specific objectives are listed as below:

- (i) To analyze the design considerations of a supply-tracking power amplifier targeted for audio applications. To have an investigation on the design tradeoffs among key performance metrics with emphasis on linearity performance and power efficiency, and hence to provide guidelines for design and implementation of a class H adaptive supply audio amplifier as in objective (ii).
- (ii) To propose a novel class H amplifier architecture operated with only single-rail power supply which should inherit the good linearity performance of a class AB amplifier and exhibit comparable power efficiency compared to a class D amplifier. This architecture should not introduce additional distortion during transitions between different operation modes which is the major drawback of the state-of-the-art design.

- (iii) To propose an improved control algorithm for the SMPS unit which should maximize the power conversion efficiency especially for light load condition.
- (iv) To implement a prototype of the proposed architecture as in (ii) which includes design and simulation with computer aided design (CAD) tools and silicon realization with a standard CMOS technology. On the basis of lab bench testing results, to compare the performance of the chip with benchmark design as well as other topologies in the literature, and hence validate the superiority of the proposed architecture.

1.3 Contributions

In the market for linear audio amplifier with adaptive supplies, based on the author's survey, the class G topology still dominates. This is mainly due to the lack of competence among the class H products. The major drawback is still the poor linearity issue, thus making them less qualified for audio amplification. This thesis aims to provide an optimal solution in terms of linearity, power efficiency and cost. The contributions that the author has made are listed below:

- (i) On the basis of audio signal characterization, an investigation was conducted on the performance comparison among different linear amplifier topologies, the power efficiency of class G and class H amplifiers were derived and compared to conventional class AB amplifier.
- (ii) More specifically, an investigation was conducted on the analysis of class H amplifier with single-rail power supply. The relationship between overall power efficiency and several design parameters including minimum operating supply voltage, power transistor headroom and supply noise rejection were studied.
- (iii) A novel class H topology with common-mode modulation (CMM) scheme was proposed and analyzed. The new architecture is able to work with only single-rail power

supply hence eliminates the need for generation of negative supply. More importantly, the proposed structure achieves a smoother transition between different modes without any increase in distortion.

- (iv) A buck dc-dc converter was developed with focus on the reference-tracking capability. The converter is able to track an audio band reference signal pertaining to the information of input signal amplitude. Multi-mode control scheme as well as zero current detection function were also implemented for an optimized conversion efficiency.
- (v) A prototype of the proposed design was fabricated with the AMS 0.18- μm CMOS process. The experimental results show that the chip achieves a peak power efficiency of 80.4% while is able to deliver a peak out power of 526 mW to a 16 Ω resistive load. The peak THD+N ratio measured is 0.01%(-80 dB) at input frequency of 20 kHz. The whole system consumes a quiescent power of 3.52 mW under a 3.3 V supply. The proposed design achieves the best efficiency performance among all linear power amplifiers and much better linearity performance compared to the state-of-the-art class H amplifier design to-date at the writing of this thesis.

1.4 Organization

The organization of subsequent chapters of the thesis are delineated as follows:

In Chapter 2, a comprehensive literature survey on linear audio amplifier is shown. It includes the basic characterization of audio electronic signals, evolution of class AB output stage and the developing trend towards linear amplifiers with adaptive supplies.

In Chapter 3, more specific analysis are provided for both the class G and H adaptive supply amplifiers. This includes the derivation of power efficiency, selection between single-rail operation or dual-rail operation and current design challenges.

In Chapter 4, the proposed class H amplifier architecture is illustrated and several

design considerations for performance optimization is discussed.

In Chapter 5, the circuit-level implementation of the class H amplifier is shown, which consists of three blocks, the input amplitude detection (IAD) block, the fully-differential class AB amplifier and the reference-tracking buck converter.

In Chapter 6, the experimental results based on the silicon chips are presented. The data are collected and compared with previous designs on linear power amplifier from both academic papers and commercial products

In Chapter 7, conclusions are drawn and suggestions for future works are proposed.

Chapter 2

Literature Review on Linear Audio Amplifiers

2.1 Introduction to Audio Systems on Portable Devices

The market for portable electronic devices has experienced a rapid development in the past decade. High quality audio playback is one of the functionalities that companies have been seeking to optimize user experience. As a result, the target applications for most of the audio amplifier designs have shifted toward portable devices recently. Fig 2.1 depicts the system-level block diagram of an audio codec together with a digital signal processing (DSP) core which is a typical integrated audio solution for handheld devices. As digital representations of audio signals are ubiquitous in modern consumer electronics, audio codec serves a very important role in the interface and communication between the digital core and the real analog world [23, 24]. The audio CODEC consists of two separate signal processing chains. The encoder path provides the interface between the recorded audio signal and the

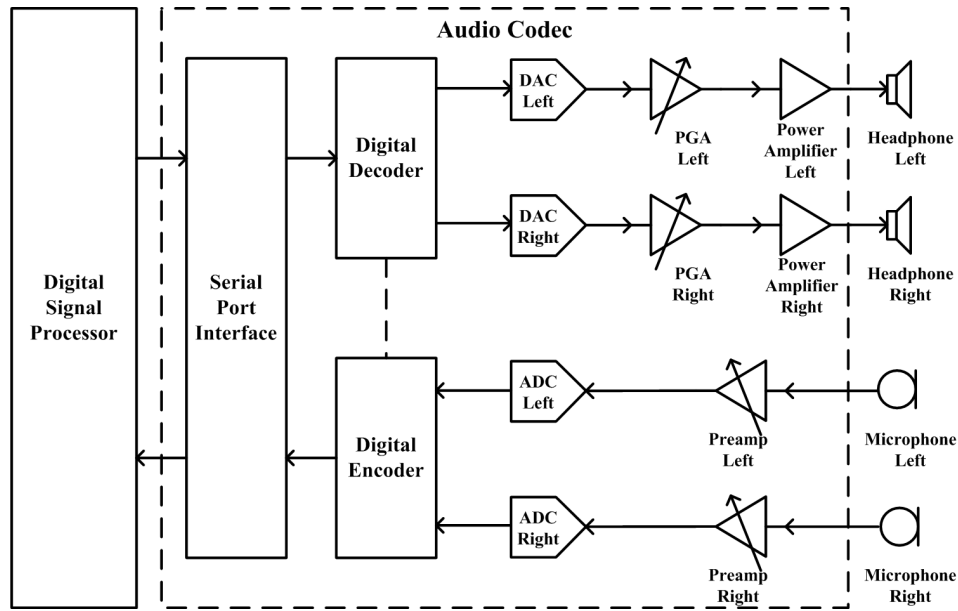


Figure 2.1: System-level block diagram of an audio CODEC

DSP core, since the sensed analog audio input signal is relatively small in amplitude (around the level of a few mV), a pre-amplifier stage is hence required to amplify the signal to the line level. In the opposite direction, the recorded or processed signals from the DSP core will be converted into analog domain by high-precision analog-to-digital converters (ADC). In the next stage, these converted analog signals will be amplified by the programmable gain amplifiers (PGAs) for volume control purposes. In real applications, the intermediate stage will be more complicated compared to the illustration in the figure, which may include other features such as equalization for adjusting the bass and treble, the tone controllers as well as fixer for additional electronic effects. Finally after going through all those functional blocks, the processed analog signals are to be amplified by the power amplifiers to drive the external headphones or loudspeakers.

As can be observed from the Fig 2.1, the power amplifier acts as the last stage in the signal processing chain for an audio CODEC. The voltage gain required at this stage is usually not large due to the preamplifier stages. However, in order to drive the small resistive load of the headphone substantial current gain is needed at the power amplifier stage. As a

result, the current driving capability of the power amplifier must be strong enough to meet the output swing specifications. Hence, not only linearity but also high power efficiency is definitely desired for a good power amplifier.

2.2 Audio Signal Characterization

Generally speaking, audio signal is the representation of the sound in the nature. When being processed in electronic circuits, it is represented typically as electrical voltage levels in a continuous manner. The properties of audio signals is widely studied, in the remaining sections, its property in terms of power level, frequency distribution and amplitude distribution will be introduced respectively.

2.2.1 Audio Signal Power Level

It is useful to introduce the terminology Dynamic Range (DR) [25] when dealing with the power level of audio systems. The DR of a system is defined as the ratio between the maximum power level the system can withstand and the power level of the system's noise floor. The power level of the sound can be quantified by a parameter called Sound Pressure Level (SPL). For example, the human hearing system has a threshold SPL of 2×10^{-5} Pascals (Pa) for middle band frequencies, and could bear a maximum pressure level of up to 200 Pa before any damage occurs, which yields a dynamic range of 140 dB [25]. For human hearing system, 0 dB SPL is defined as the hearing threshold 2×10^{-5} Pascals (Pa). Table 2.1 listed several situations of sound levels and the corresponding power rating requirements on the power amplifiers used.

Table 2.1: Amplifier power needed for different sound pressure levels

SPL [dB]	Sound Pressure Level (SPL) is equivalent to:	Power in LS that SPL @ distance from LS	Necessary amplifier power rating
50	Low level background music at 1m	100mW @ 1m	1.5mW
60	Normal speech at 1m	1mW @ 1m	15mW
80	Orchestra in concert hall	1W @ 3m	15W
110	Rock band	2kW @ 4.5m	30kW

2.2.2 Audio Signal Frequency Distribution

Frequency is an important characteristic of the audio signal, it is related to the vibration frequency of the audio signal source. From a human's perspective, the difference in frequency simply reflects the pitch of the tone. The hearing range defines the range of frequencies that can be heard by humans, which is normally given as 20 Hz to 20 kHz. Although 20 kHz is set as the upper bound of the hearing range, most people are not able to hear signals with such high pitches. Some high frequency harmonics around 10 kHz are mainly harmonics or overblows of some music instruments such as violin and piccolo. Such high frequency harmonics are harsh and unpleasant for a good hearing experience, this is to say that although the hearing range is quite wide, the focus for audio signals especially voice and music playbacks should be on the low and medium frequency range.

A previous report shows a study on the frequency distribution of audio signals [26]. In order to make the test more realistic, 80 music fragments were selected from various types of CDs which includes classical music, rock music, pop music, human speech signals and so forth. The frequency distribution of the selected music fragments are plotted as in Fig 2.2. The Fast Fourier Transform (FFT) was conducted to analyze the frequency distribution of those samples. The FFT analysis gives the power of different frequency harmonics in a certain fragment. The plotted data shows the integration of power normalized to total signal power

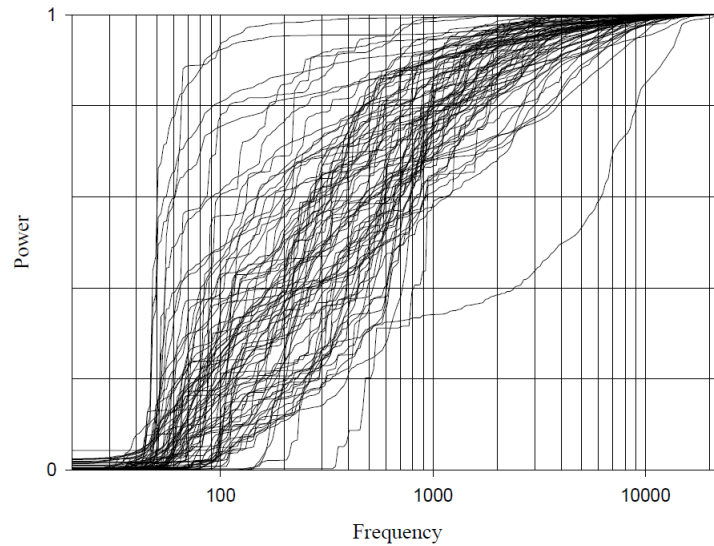


Figure 2.2: Accumulated power normalized to total signal power over frequency plot for various music fragments

across the frequency band. It can be inferred from the graph that for most of the samples, the accumulated normalized power ratio reaches 0.6 at 1 kHz and a substantial portion can even be higher than 0.8. Therefore, the averaged curve of frequency distribution is close to a S-shaped curve where the incremental power is large for low to medium frequency (50 Hz to 1 kHz) and gradually saturated for higher frequency (>1 kHz). The different emphasis on different fragments are due to the various music style. In summary, the investigation on audio signal frequency distribution reveals the fact that despite the wide range of audible frequency band, most of the signal power falls within a narrower range from 50 Hz to 3 kHz.

2.2.3 Audio Signal Amplitude Distribution

A sinusoidal wave is usually used for testing of the audio amplifier, however, the amplitude of real audio signals is constantly changing and has very large variations from time to time. To have a better view of the amplitude distribution of a signal, a parameter named Peak-to-Average Ratio (PAR) is introduced to see how fluctuating the signal is. As the

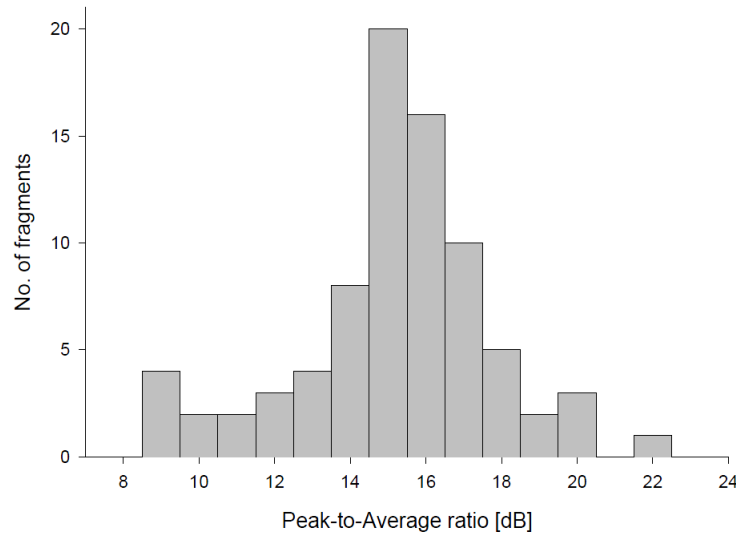


Figure 2.3: PAR distribution for all music fragments

name implies, it is defined as the ratio of the signal's peak amplitude over its Root Mean Square (RMS) value across time and it can be expressed in the equation below.

$$PAR = 20 \cdot \log_{10}\left(\frac{V_{\text{peak}}}{V_{\text{RMS}}}\right) \quad (2.1)$$

The PAR is also referred as the crest factor in audio engineering, for a sine wave input its PAR value can be calculated as 3 dB. However, things are much different for real audio signals like music. According to the audio signal characterization in previous works [26, 27], the PAR distribution for 80 music fragments is shown in the histogram in Fig 2.3. As can be seen from the figure, the value of PAR for most of the samples fall within the range of 12 dB to 18 dB, even the minimum value is still larger than 8 dB. The averaged PAR of all the fragments is 15 dB, this gives a totally different view on how the audio signal characterize the difference between its peak power level and its average power level can be very large. Therefore, it is more practical and meaningful to consider the effect of PAR when calculating the power efficiency of an audio amplifier. The results with purely sinusoidal wave may not be solid when subject to real audio applications.

2.3 Performance Metrics of Audio Power Amplifier

2.3.1 Total Harmonic Distortion Plus Noise Ratio

The Total Harmonic Distortion Plus Noise ratio (THD+N) is a commonly-used parameter that measures the linearity performance of a amplifier. It is defined as the ratio of the power of the fundamental frequency component to the power of all the in-band harmonics plus the noise power, which can be expressed as in the formula below.

$$THD + N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + Noise^2}}{V_1} \quad (2.2)$$

In the ideal case, the amplifier should not output any additional harmonics other than the amplified fundamental frequency component. With all the non-ideality, the THD+N is a straightforward measurement of the purity of the output sine wave with respect to the single-tone input signal. In audio applications, a smaller THD+N ratio is always desired to preserve high fidelity of the input signals. For linear audio amplifiers, it is easy to obtain a THD value of less than 0.1% (-60 dB). However, to further reduce the distortion and noise effects to the level of beyond 0.01% (-80 dB), extra attention has to be paid to every detail of the chip design process including component matching in layout and PCB routing. In the literature, the class AB-based linear audio amplifier designed by Mediatek [28] achieves a lowest THD+N ratio of 0.0017% (-95 dB) and hence sets the benchmark for ultra high-fidelity audio amplifier.

2.3.2 Signal-to-Noise Ratio and Dynamic Range

The Signal-to-Noise Ratio (SNR) and Dynamic Range (DR) are used to measure the level of desired signal compared to the background noise level. It is usually considered that these two terms are interchangeable for they are describing the same property of the system.

However, a closer look reveals that these two parameters still have some difference. DR by definition is the difference in level between the highest peak output signal where just before waveform clipping occurs and the highest spectral component of the noise floor. The highest peak output signal for a linear amplifier is usually defined as the point at which the THD value increases to 1%. While for SNR measurement, the signal level can be arbitrary and does not have to be at the maximum possible level. A high DR does not guarantee good SNR since it is also determined by how the amplifier is being operated. The A-weighted DR is a commonly-used parameter for comparison, it is quite normal to achieve a value of more than 80 dB for modern audio amplifiers.

2.3.3 Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is used to measure the circuit's immunity to disturbance from the power supply. It is defined as the ratio of the signal gain when the supply is ac grounded and the supply noise gain when the input is ac grounded. The expression is shown in the following formula.

$$PSRR = \frac{A_{id}(v_{sup} = 0)}{A_{sup}(v_{id} = 0)} \quad (2.3)$$

PSRR is becoming a critical specification in audio products for mobile devices. For conventional stand-alone audio amplifiers, the power supplies are normally pre-regulated and clean, thus the supply noise is no big issue. However, for audio amplifiers used on mobile devices, the cellular phone environment can no longer be considered as quite. The battery itself is not a clean power source, besides various Radio Frequency (RF) functional blocks which operate with high and periodical frequencies will make the supply to the amplifier even more noisy. For instance, the RF power amplifier switches on and off constantly at a frequency of 217 Hz to transmit TDMA bursts in a GSM system, which generates voltage droops and spikes at a low frequency rate. Therefore, requirement for high PSRR is prevalent

in today's audio amplifier design. A PSRR of at least (60 dB) is desired for the whole audio frequency band.

2.3.4 Power Efficiency and Maximum Output Power

The power efficiency of a audio amplifier is defined as the total power delivered to the load over the total power acquired from the power source. Generally it can be expressed as

$$\eta = \frac{P_{\text{load}}}{P_{\text{DC}}} \quad (2.4)$$

The numerator is the RMS power that is delivered to the headphone load, and the DC power in the denominator includes all kinds of losses dissipated within the system. For a linear type amplifier, the power efficiency increases when the output power becomes larger. However, there is a maximum output power for each circuits. As the output power increases, the output voltage swing increases correspondingly. As a result, the headroom voltages for the power transistors are gradually squeezed. The linearity of the amplifier will be jeopardized with the reduced headroom voltage and finally there will be a surge in the value of THD+N ratio. The maximum output power is defined as the maximum power the amplifier is capable to output to the load before the output signal THD+N ratio increases to above 1% (-40 dB). The 1% criterion is widely adopted among the commercial products. When THD+N exceeds 1% there will be significant amount of distortion which can be heard by human ear, therefore the amplifier is considered no longer capable for audio amplification.

2.4 Linear Amplifier Output Stage Topologies

2.4.1 Class A and Class B Output Stages

The simplified configuration of a class A output stage is depicted in Fig 2.4 on the left. The most distinct portion of the class A amplifier is the constant current source used to bias the output transistor. The output transistor will be conducting the entire cycle (360°) to amplify a periodical input signal. The good thing is that the signal is amplified by the same device at any time, there is no distortion due to the handover process between two devices. Therefore class A is generally considered to have the best linearity performance. Despite its excellent linearity performance, it also exhibits defects that limit its application. The circuit in the figure has a limited current sourcing capability and an unlimited current sinking capability (the power transistor). In order to match the current source and sink required by an audio power amplifier, the current source should be designed very large. Therefore a huge quiescent current will flow through the output stage even when it is producing zero output. This results in very low power efficiency and enormous amounts of wasted power, these power ultimately transfer to heat and hence bulky heat sinks are needed for reliability concern.

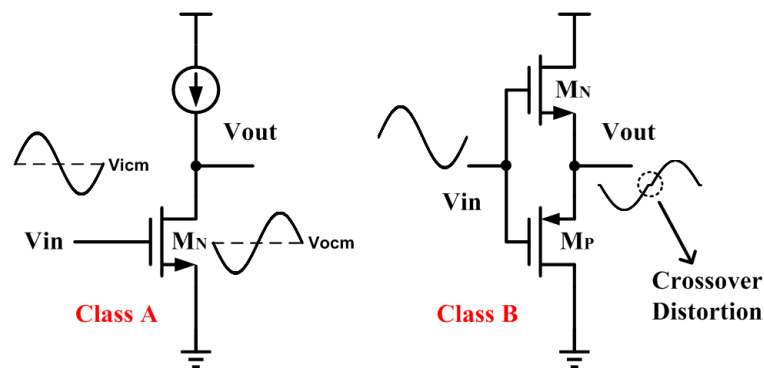


Figure 2.4: Simplified circuit configuration for class A (left) and class B (right) output stages

Class B amplifier make use of two complementary power transistors to deliver current to the load, the schematic of which is shown on the right of Fig 2.4. The common-drain structure used here is to increase the output stage driving capability. Instead of making one transistor conducting the whole cycle, power transistors in class B output stage are supposed to conduct for only half the cycle (180°). Each power transistor will only source/sink current when it is needed by the load. Hence, the quiescent current as well as wasted power is significantly reduced. Since the two power transistors are working towards the same direction as indicated by the input signal, the class B output stage is also referred as the push-pull structure. However, this complementary conducting scheme give rise to additional distortion which is called the crossover distortion. Ideally the two signal paths should have a seamless transition from one to the other as both of them are conducting for half a cycle. However, this is never the case as transistor behaves in an analog manner that it needs certain threshold voltage to turn on. Hence there be a blind region when both power transistors are considered not conducting and the input signal is missed. In summary, class A and B type output stages are the most basic topologies proposed in the early days for power amplifier. Due to their intrinsic defects in terms of efficiency and distortion, they are obsolete and replaced by the class AB topology.

2.4.2 Class AB Output Stage

Class AB output stage is proposed to combine the advantages of a class A and a class B output stages. As mentioned before, class B topology is more power efficient but suffering from the crossover distortion problem. Therefore, the concept of class AB mainly focuses on eliminating the distortion caused by the dead zone during transition. The topology of a class AB output stage is shown in Fig 2.5.

The operation principle of class AB output stage is simple, in order to eliminate the dead zone where both transistors are off, the conduction angle of each transistor can be extended a bit to more than half a cycle ($>180^\circ$). So that the operation region of the two

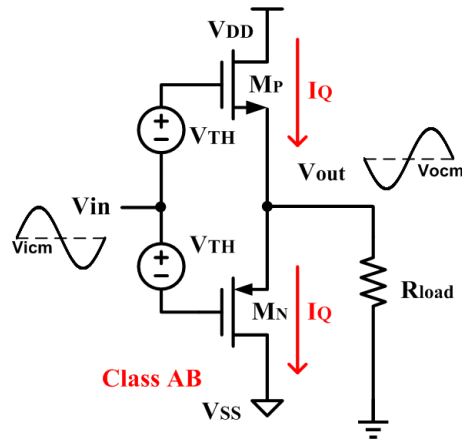


Figure 2.5: Simplified circuit configuration for class AB output stage

complementary transistors are overlapped and no dead zone is found during the handover process. To implement the overlapped conduction region, the gate control signals for the two output transistors are dc level-shifted as shown in Fig 2.5. The V_{TH} is to illustrate the bias voltages which some designers call them the "floating battery". It does not affect the ac signal gains seen from the two different paths, while for dc analysis it boosts the gate-to-source voltages of the power transistors by one threshold voltage, so that the output transistors are turned on in advance to avoid the dead zone. As compared with class A output stage, the class AB structure still make use of the push-pull concept and eliminates the enormous constant current source, hence the quiescent current consumption as well as wasted power is much reduced. While due to the handover process the linearity is slightly degraded as the price paid. Compared to class B structure, the class AB amplifier eliminates the dead zone of conduction. While as a penalty, a larger quiescent current I_Q flows in the output stage even though it is much smaller than in the case of class A. To sum up, class AB structure shows a good trade-off between linearity and efficiency concern.

As class AB is a dominant structure for the linear mode amplifier, details of its properties will be discussed in the remaining part of this section. The power efficiency of a class AB amplifier can be calculated as

$$\eta = \frac{P_{\text{load,RMS}}}{P_{\text{dc}}} = \frac{\pi \cdot V_{\text{OUT}}^2}{4V_{\text{DD}}(V_{\text{OUT}} + \pi \cdot R_{\text{load}}I_{\text{Q}})} \quad (2.5)$$

V_{OUT} , V_{DD} and I_{Q} are the output swing, supply voltage and the quiescent current respectively. It can be noticed from the equation that the ideal maximum efficiency of a class AB amplifier is the same as a class B which is 78.5%. However, this is under the condition that the output stage achieves full rail-to-rail swing and it does not consume any quiescent power. However, in real case the output stage is not supposed to swing rail-to-rail but leave certain headroom voltages to bias the conducting transistor in the correct operation region, otherwise the output transistors will be working in linear region and the forward gain of the amplifier is sacrificed. By denoting this headroom to be V_{DSAT} , the modified expression of class AB efficiency becomes

$$\eta = \frac{\pi \cdot (V_{\text{OUT}} - V_{\text{DSAT}})^2}{4V_{\text{DD}}(V_{\text{OUT}} - V_{\text{DSAT}} + \pi \cdot R_{\text{load}}I_{\text{Q}})} \quad (2.6)$$

From this expression we can see the trade-offs for different design parameters. To achieve a higher power efficiency, the headroom voltages V_{DSAT} as well as the quiescent current I_{Q} should be minimized. Consider the same resistive load, the smaller the headroom voltage, the higher the output swing and hence more current is demanded from the power MOSFET. It translates into a even smaller equivalent on-resistance of the power transistor. This can be obtained by either increasing the power transistor's geometric ratio (W/L) or its gate voltage swing. However, both methods are not free of charge, the former one directly increases the size of the chip while the latter one stresses the operation region of transistors in the prior stage. For the other parameter I_{Q} , a smaller value means the power transistors are closer to their off state during transition and hence makes it vulnerable to crossover distortion. To gain a better understanding of how the class AB stage is realized, the most widely used structure which is based on the translinear principle [13] will be analyzed.

Fig 2.6 depicts the transistor-level implementation of a typical class AB output stage

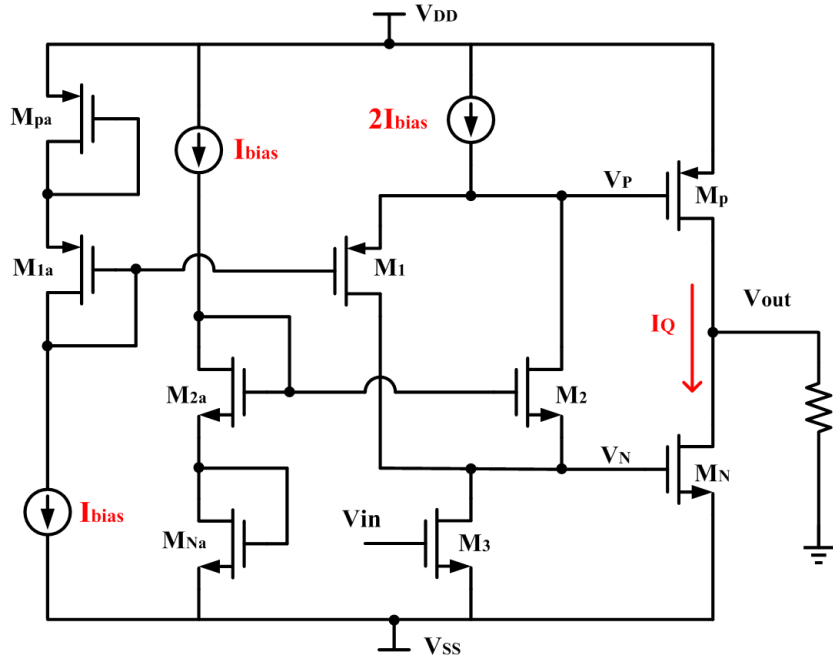


Figure 2.6: Transistor-level illustration of the class AB output stage based on the translinear loop principle

with translinear principle. V_{in} is the output signal from the prior stages of the amplifier, M_P and M_N are the complementary power MOSFETs at the output stage where V_P and V_N are the gate driving signals, respectively. In contrast to the schematic in Fig 2.5, for this rail-to-rail class AB configuration, M_P is the sourcing power transistor whereas M_N is the sinking power transistor. For a simple illustration, the biasing circuitry are replaced with ideal constant current sources. The analysis of the class AB amplifier can be done in two different perspectives, the dc I/V characteristics and the ac small-signal analysis.

For dc I/V characteristics, the output current is defined as the current flowing out from the output node which has an expression as:

$$I_O = I_{MP} - I_{MN} \quad (2.7)$$

which can be further extended with the MOSFET square law I/V characteristic equations

as below

$$\begin{aligned}
 I_O &= K_P(V_{OV,P} - V_{in})^2 - K_N(V_{OV,N} + V_{in})^2 \\
 &= K_{P/N}(V_{OV,P} + V_{OV,N})(V_{OV,P} - V_{OV,N} + 2V_{in}) \quad (2.8) \\
 \text{where } K_{P/N} &= \frac{1}{2} \cdot \mu C_{OX} \left(\frac{W}{L} \right)_{P/N}, V_{OV} = |V_{GS}| - |V_{TH}|
 \end{aligned}$$

For a symmetrical current driving capability, it is assumed that the parameter K_P is equalized to K_N . Then, by assuming the threshold voltages to be the same for both PMOS and NMOS output transistor, the effective gate overdrive voltages $V_{OV,P}$ and $V_{OV,N}$ under quiescent state are also the same. Therefore, under the condition that the amplified ac signal on gate control voltages V_P and V_N are smaller than the overdrive voltage V_{OV} , the expression in equation (2.8) reduces to:

$$I_O = 4K \cdot V_{OV}V_{in}, \text{ when } |V_{in}| < V_{OV} \quad (2.9)$$

For larger ac input $V_{in} > V_{OV}$ or $V_{in} < -V_{OV}$, the change in the gate control voltages V_P and V_N will cause either of the power transistor to be weakly conducting and the output current expression modifies to:

$$\begin{aligned}
 I_O &= K(V_{OV} - V_{in})^2, \text{ when } V_{in} < -V_{OV} \\
 I_O &= -K(V_{OV} + V_{in})^2, \text{ when } V_{in} > V_{OV}
 \end{aligned} \quad (2.10)$$

Based on the above analysis, the I/V characteristics is plotted in Fig 2.7. As shown in equation (2.8), (2.9), for input signal with small amplitude, both power transistors are fully on and the output current has a linear relationship with the input signal. As input increases further, one of the power transistor will be weakly on and kept a minimum current I_{min} unlike fully switched off as in the case of class B, while current in the other power transistor will yield a quadratic relationship with the input signal and hence the current driving capability

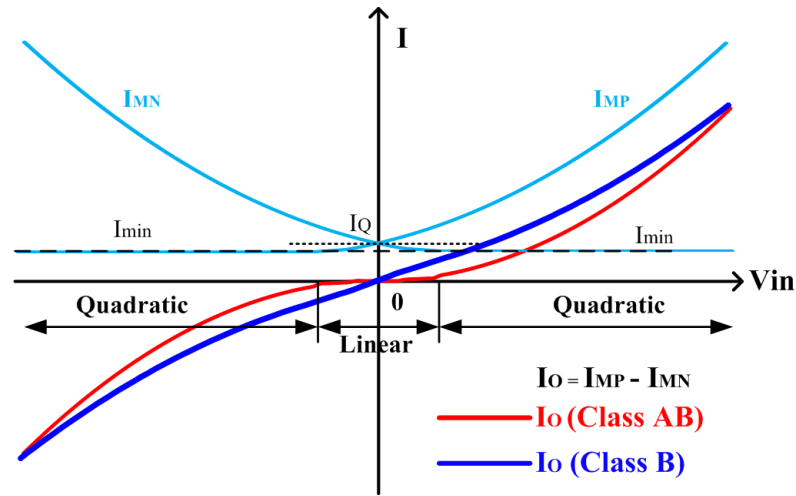


Figure 2.7: I/V characteristics of class AB and class B output stages

is ensured. Compared with the class B characteristics, the class AB output stage has a good definition of the current flowing in the transistor that is supposed to be off. Hence, there is never a moment when both transistors are off. When input signal increases further, the quadratic relationship between input signal and output current may no longer be valid. This is due to the shift of dc operation region of the power transistor. For instance, when V_{in} increases, the NMOS sinks current from the load and hence the output terminal is pulled down. For the power NMOS transistor, its gate-to-source voltage keeps increasing while its drain-to-source voltage keeps decreasing, finally it enters the linear region and the square law I/V relationship is no longer valid. As a result, the current will not increase quadratically but gradually saturates to the limit it can provide.

It is ideal that the class AB output stage works in the quadratic and near linear regions shown in Fig 2.7 as the power transistor are supposed to be working in the saturation region. However, this implies the output transistors need to be extremely wide, the large parasitics associated with the power transistors will in turn pose compensation problems. As a compromise, it is acceptable that the power transistors work in the triode region, and the penalty is, higher order harmonics will be present. With the high-gain feedback loop, the distortion can be linearized and sufficiently good THD performance can still be obtained.

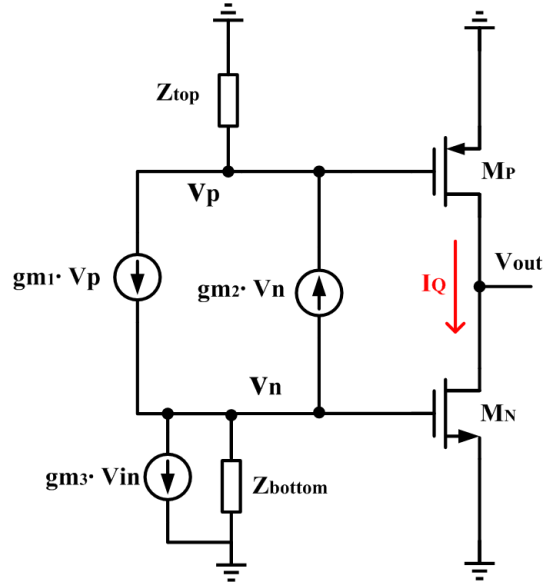


Figure 2.8: small-signal illustration of the class AB output stage

The ac analysis can be done with the help of the small-signal equivalent circuit which is plotted in Fig 2.8, where g_{mi} indicates the transconductance of transistor M_i in Fig 2.6. The input ac signal injected from transistor M_3 is denoted as a voltage controlled current source (vccs) in parallel with its impedance. The impedance notation Z_{top} and Z_{bottom} denote the impedances seen from V_p and V_n to ground, respectively. In order to analyze the small-signal properties of the output stage, it is necessary to know the impedance looking up from node V_n . I_n is defined as the small-signal current that flows upward through node V_n and is equal to the current that flows through the top current source Z_{top} . By using KCL equation, the voltage-current relationship can be derived as:

$$\begin{aligned} I_n &= g_{m2}V_n - g_{m1}V_p = I_{ztop} \\ &= g_{m2}V_n - g_{m1}I_n Z_{top} \end{aligned} \quad (2.11)$$

Rearranging equation (2.11), the small-signal impedance looking up from node V_n can be obtained as:

$$Z_n = \frac{V_n}{I_n} = \frac{1 + g_{m1}Z_{top}}{g_{m2}} \quad (2.12)$$

Therefore the small-signal gain from V_n to V_p can be calculated as.

$$\frac{V_p}{V_n} = \frac{Z_{top}}{Z_n} = \frac{g_{m3}Z_{top}}{1 + g_{m4}Z_{top}} \quad (2.13)$$

For balancing between the current sink and source capabilities of the output stage, the small-signal parameters of transistor M_1 and M_2 as well as the power transistors M_P and M_N are designed to match. Thus, it can be obtained from equation (2.13) that for small input signals, the gain from V_n to V_p approximately reduces to 1, which means the gate control signal of M_P will simply follows that of M_N and the push-pull effect is ensured to avoid distortion during the crossover region. However, the above analysis will no longer be valid as the amplitude of the input signal increases, this is due to the change of circuit configuration during large signal transient. The dc operating conditions of the output stage are reconfigured and the small-signal analysis has to be analyzed case by case.

The small-signal models under the two large signal transient conditions are depicted in Fig 2.9. The schematic on the left shows the circuit configuration when there is a large positive swing at the output. Under such circumstance, V_{in} increases to pull down both of the control signals V_p and V_n . As shown in Fig 2.6, the gate voltage of transistor M_1 is clamped by the biasing current I_{bias} as well as the sizing of the two diode-connected transistors M_{pa} and M_{1a} . Any further reduction of V_p will lower the source-to-gate voltage of M_1 and eventually switches it off. Thus, the effect of M_1 is cut off from the rest of the circuitry and is drawn with dashed lines in Fig 2.9. The small-signal analysis is conducted as follows. Since M_1 is cut off, M_2 now serves as a common-gate current buffer which simply pass the ac current variation caused by V_{in} to V_p . Thus, the small-signal gain from V_n to V_p can be derived as.

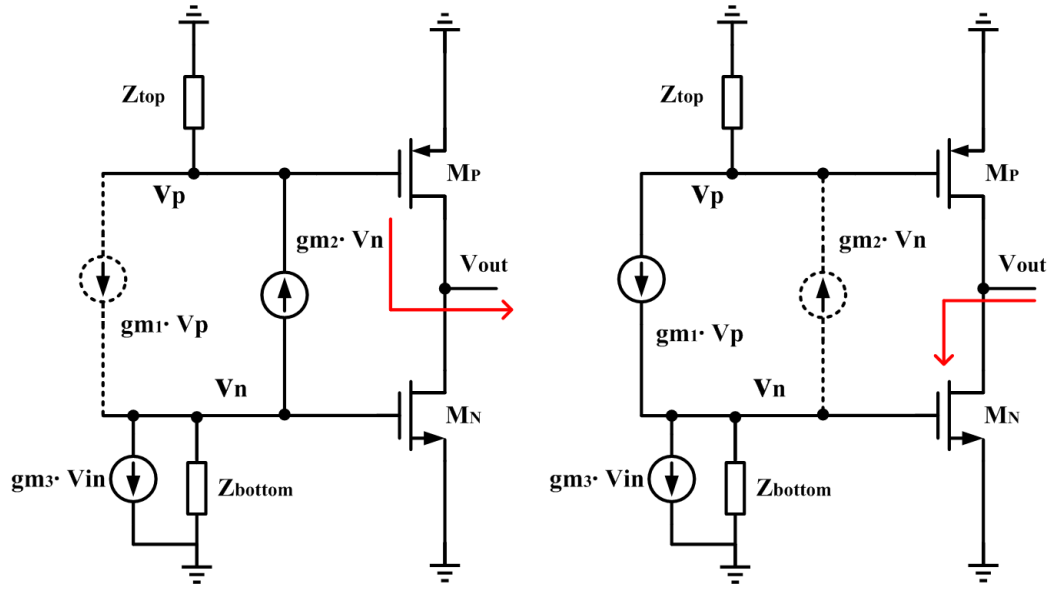


Figure 2.9: small-signal illustrations of the class AB output stage during positive and negative large signal transients

$$\frac{V_p}{V_n} = g_{m2} \cdot (Z_{top} \parallel g_{m2}r_{ds,2}Z_{bottom}) \approx g_{m2}Z_{top} \quad (2.14)$$

It can be seen that the gain of the class AB stage is still preserved which is part of the forward open-loop gain of the amplifier, thus higher voltage swing can be generated at V_p , and sufficiently large gate swing is ensured for better current source capability of the output stage. While for node V_n it becomes a low impedance node and the effect of V_{in} is minimal. Its biasing condition is now dependent on the translinear loop formed by M_N , M_2 , M_{2a} and M_{Na} . The translinear principle regulates the gate-to-source voltage of M_N as follows:

$$\begin{aligned} V_{GS,N} &= V_{GS,Na} + V_{GS,2a} - V_{GS,2} \\ &= \sqrt{\frac{2I_{bias}}{K'_{Na}}} + V_{TH,Na} + \sqrt{\frac{2I_{bias}}{K'_{2a}}} + V_{TH,2a} \\ &\quad - \sqrt{\frac{2 \cdot 2I_{bias}}{K'_2}} - V_{TH,2} \end{aligned} \quad (2.15)$$

If M_2 and M_{2a} are well matched, the above expression can be simplified to

$$V_{GS,N} = \sqrt{\frac{2I_{\text{bias}}}{K'_{Na}}} + V_{TH,Na} + (1 - \sqrt{2})\sqrt{\frac{2I_{\text{bias}}}{K'_2}} \quad (2.16)$$

It is interesting to notice that the V_{GS} expression is very similar to that of the quiescent state, the difference is that under this condition all the bias current flows through M_2 and hence the gate-to-source voltage of M_N is slightly smaller than in its quiescent state. This explains the difference between the quiescent state current I_Q and the minimum current $I_{\min}$ as shown in Fig 2.7. Using the same method, the analysis can be done for the condition where output has a large negative swing. The small-signal model for such condition is depicted on the right of Fig 2.9. As the bottom current sink is closed by the diminishing V_{in} , both V_n and V_p are charged up by the top current source, as a consequence, M_2 gradually enters the cut-off region and is denoted by the dashed lines. Now V_n becomes a high impedance node and the high gain is preserved for large gain swing, so that the current sink capability is ensured. As for node V_p , the small-signal gain can be derived as

$$\frac{V_p}{Z_{\text{top}}} = \frac{V_n}{Z_n} \text{ thus, } \frac{V_p}{V_n} = \frac{Z_{\text{top}}}{Z_n} = \frac{Z_{\text{top}}}{g_{m1}r_{ds,1}Z_{\text{top}}} = \frac{1}{g_{m1}r_{ds,1}} \quad (2.17)$$

In contrast to equation (2.14), we can see that for either case, whether the output is having a positive or negative swing, higher dc gain is always kept for the output stage which exhibits current source capability to the load. The minimum current flowing in the weakly conducting transistor is well defined by the translinear loop associated. Hereby, we can summarize the properties and design trade-offs of a class AB output stage as below.

- (i) For quiescent state, the output stage should have a well-defined static operating current, it should have minimum variation through different Process, Voltage and Temperature (PVT) corners. The amount of quiescent current trades with the suppression of crossover distortion. Although further increase in I_Q will only results in marginal

benefit in linearity, it is the worst case of the fabrication corner that matters. Therefore, it is highly desirable that the I_Q has a minimum deviation through all process corners.

- (ii) For signal transient, the class AB output stage is supposed to preserve high gain to the strongly conducting device and can also accurately limit the current in the weakly conducting device.
- (iii) A trade-off exists on the sizing of the power transistors over the required gate voltage swing for a specified load condition. The smaller the width of the transistor the larger gate swing needed to provide the same amount of current. And consequently larger supply voltage is required for the output stage.
- (iv) A trade-off exists on the maximum output swing and hence the peak power efficiency over the linearity performance for a given geometric ratio of the power transistors. The larger the output swing, the smaller voltage drop wasted on the power transistor and hence better efficiency can be obtained. However, as the headroom voltage of the power transistors shrinks, they are more prone to work in the triode region which introduce higher order harmonics and makes linearity worse. To discard the said trade-off and keep both the benefits at the same time, a wider transistor or larger gate swing voltage is required. The situation goes back to (iii), and either area or supply headroom is increased.

2.5 Analysis and Design of state-of-the-art class AB Amplifiers

In view of the properties and trade-offs of class AB amplifier design, many novel structures are proposed for improvement. Instead of tangling with the efficiency and headroom voltage trade-offs, previously reported works mainly focused on the method for reducing the

quiescent power consumption [13,17–19,28–30]. One way of doing it is through reducing the minimum operating voltage of the output stage [17,18,28], while the other way is to reduce the quiescent current variations through process corners [19,29,30]. In this section, a more in-depth review will be carried out on the state-of-the-art designs of class AB amplifiers.

2.5.1 Class AB Amplifier Using Output Buffers with Adaptive Load

As mention previously, one direction for improvement is towards a lower supply voltage at the output stage which directly translates into lower quiescent power. One method using this concept is the class AB amplifier using output buffers with adaptive load [17], the schematic of it is depicted in Fig 2.10.

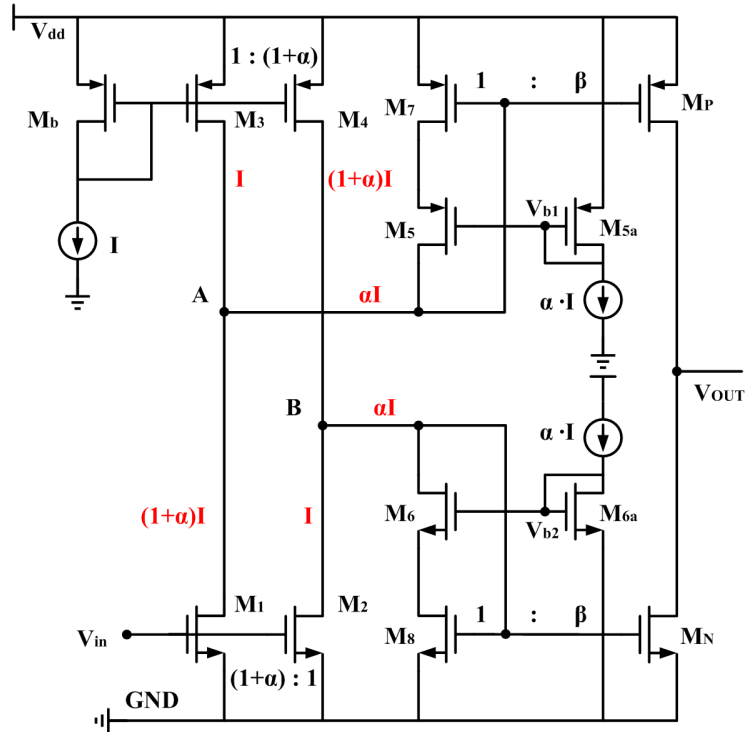


Figure 2.10: Schematic of a class AB amplifier design achieving lower minimum operating supply voltage

The schematic in Fig 2.10 depicts only the output stage of the design which contains the major novelty. Note that voltages at node A and B are actually the gate control signals driving the complementary power MOSFETs. Different from normal class AB amplifier, an additional adaptive load formed by $M_5(M_6)$ and $M_7(M_8)$ is added to either PMOS or NMOS, respectively. The idea behind this is that the adaptive load can reconfigure to change its impedance according to the load conditions. For quiescent state operation, take the NMOS side for instance, the biasing voltage V_{b2} is set to $V_{TH,N} + 2V_{DSAT}$. M_8 works in saturation region and the impedance seen at node B is small with a magnitude of $1/g_{m8}$. Therefore, the gain from V_{in} to $V_A(V_B)$ is small under quiescent state and the voltage variation at the power transistor's gate is reduced. Hence, the quiescent state current of the output stage is less sensitive to the process variations. For large signal transient, we still take NMOS as an example. When V_B increases and output is supposed to swing towards ground, due to the fixed biasing at V_{b2} the drain voltage of M_8 will drop and hence pushing M_8 into linear region. As a result M_8 now behaves like a voltage-controlled resistor instead of a diode-connected transistor, thus the impedance looking into the M_6 path is boosted drastically and the high gain from V_{in} to $V_A(V_B)$ is retrieved.

The benefit of adopting this adaptive load structure is that for quiescent state the reduced gain of the intermediate stage will desensitize the impact of process variation on quiescent current, while for large load transient the high gain enforces the voltage driving capability of the power transistor's gate. Most importantly, compared to the classic design [13] it achieves a minimum value of $V_{GS} + 2V_{DSAT}$. However, the drawbacks of this design are also easy to figure out. First, the diode structure will reduce the open-loop gain of the amplifier under quiescent state. If it is used as single-ended output driver, a larger dc error due to offsets can be found at the output. This again results in a quiescent state current if there is no dc decoupling capacitor. Secondly, the quiescent state current is not well defined although the gate voltage is not sensitive to the process variations. The fabricated chips may still yield large deviation on I_Q due to the large scaling factor β .

the current in the weakly conducting transistor M_{12} is regulated to $\beta \cdot I_Q$ while the strongly conducting transistor M_{10} is not affected by the internal feedback loop. Similar concept applies for the V_{in} reducing phase as now the drain of M_7 is pulled almost to V_{DD} and M_9 regulates the current in the weakly conducting M_{10} with the nested feedback loop.

As can be extrapolated from the schematic, the minimum supply voltage of this amplifier can be $V_{GS} + 2V_{DSAT}$ which is the same as in the previous design. However, both V_P and V_N are high impedance nodes which will not dilute the high open-loop gain as required. Meanwhile, the current for the quiescent state as well as the minimum on current are both well defined with respect to the reference current. Therefore, it is very promising for used as audio power amplifier. The only flaw is the slightly increased complexity.

2.5.3 Reducing I_Q Variation Due to Channel Length Modulation(CLM)

Another issue with the class AB amplifier is the quiescent current I_Q variation due to poor matching from reference to the output stage. Take a second view of the class AB amplifier with translinear loop as in Fig 2.6, it is desired that the I_Q in the output stage is precisely defined by the reference current. More specifically, it is assumed that the transistors M_N and M_{Na} are designed with same ratio but M_{Na} has a much larger number of fingers. This finger number is usually referred as the scaling factor. Ideally if the gate voltages of the two transistors are matched then the output stage current I_Q is well defined. However, due to the diode-connected structure of M_{Na} , the drain-to-source voltages of the two transistors are different and can result in large I_Q variations as large as $\pm 26\%$ over different process corners [29]. Therefore certain design techniques are needed to reduce the CLM-induced quiescent current variation.

One method for reducing the CLM-induced variation is shown in Fig 2.12. The proposed design [30] make use of the translinear loop concept similar to [13]. Instead of using two

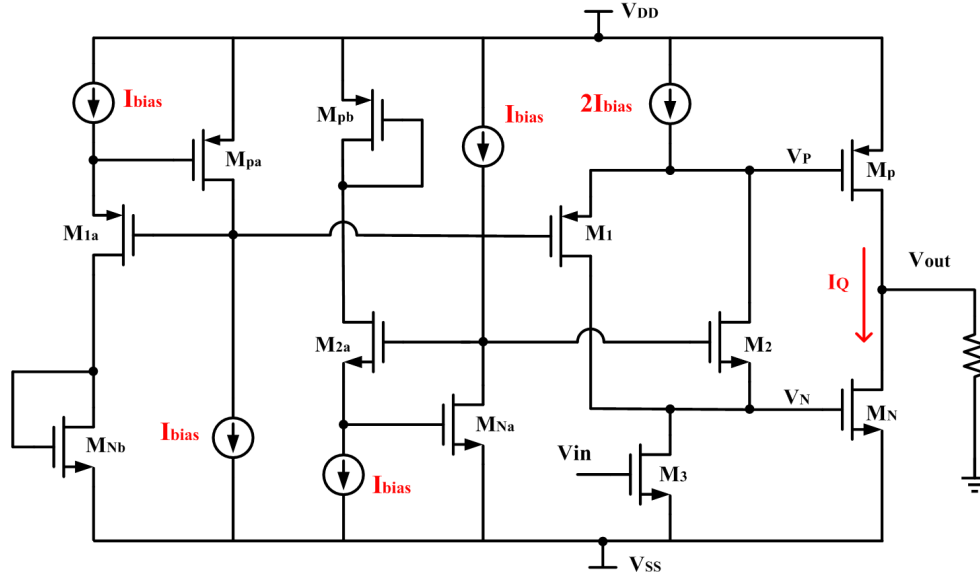


Figure 2.12: Schematic of a class AB amplifier design achieving lower CLM-induced I_Q variation

stacked diode-connected transistor, the drain of the scaled-down transistor M_{Pa} is connected to the gate of M_{1a} . In this case, the drain-to-source voltage of M_{Pa} is equal to $V_{GS,P_a} + V_{GS,1a}$ which is approximately equal to half of the supply voltage. Same concept applied for the NMOS part and better drain-to-source matching for the power transistor and the scaled-down transistor is thus achieved. However, despite the low accuracy on V_{DS} matching, the effectiveness of this technique is also dependent on the real values of the power supply and transistor threshold voltages, hence it is difficult to be mapped to other process.

Another design which embody the similar consideration is depicted in Fig 2.13 [29]. In this design, additional pair of OTAs are introduced to regulate the drain-to-source voltage of the scaled-down transistor. Take PMOS side for an example, if the drain voltage of transistor M_{Pa} is larger than the output common-mode voltage V_{CM} , the output of OTA A1 will go up and consequently the source voltage of M_{1a} will increase. This reduces the gate-to-source voltage of M_{Pa} and making its drain terminal drained by the current source. With the help of this negative feedback loop, the mismatch of the drain-to-source voltage

Chapter 3

Audio Amplifiers with Adaptive Power Supplies

3.1 Introduction to Power Amplifiers with Adaptive Supply Rails

As mentioned previously in Chapter 2, the theoretical maximum power efficiency of a class AB amplifier equates to $\pi/4$ which is around 78.5%. This is under the condition that a sine input is used, the maximum rail-to-rail output swing is achieved and quiescent current is neglected during the calculation. Things would be different if real audio signals with high PAR value are used as input. As the amplitude of typical audio signal has a Gaussian (normal) distribution, the probability density function (PDF) of audio signal amplitude information can be described as below [31]:

$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} \cdot \exp\left(\frac{-x^2}{2\sigma^2}\right), \text{ where } \sigma = V_{\text{RMS}} \quad (3.1)$$

Thus, the average value of the signal amplitude can be acquired from the mean value of equation (3.1) as:

$$\begin{aligned}
 V_{\text{AVG}} = \mu_x &= \int_{-\infty}^{\infty} \frac{x}{\sqrt{2\pi\sigma^2}} \cdot \exp\left(\frac{-x^2}{2\sigma^2}\right) dx \\
 &= 2 \cdot \int_0^{\infty} \frac{x}{\sqrt{2\pi\sigma^2}} \cdot \exp\left(\frac{-x^2}{2\sigma^2}\right) dx \\
 &= 2 \cdot \frac{-\sigma}{\sqrt{2\pi}} \cdot \exp\left(\frac{-x^2}{2\sigma^2}\right) \Big|_0^{\infty} \\
 &= \sqrt{\frac{2}{\pi}} \cdot \sigma
 \end{aligned} \tag{3.2}$$

By applying equation (2.4) the power efficiency of class AB amplifier with PAR value taken into account can be expressed as:

$$\begin{aligned}
 \eta &= \frac{P_{\text{RMS}}}{P_{\text{DC}}} \\
 &= \frac{V_{\text{RMS}}^2/2R_L}{V_{\text{Peak}}V_{\text{AVG}}/R_L} \\
 &= \frac{V_{\text{RMS}}^2/2}{V_{\text{RMS}} \cdot PAR \cdot \sqrt{\frac{2}{\pi}} V_{\text{RMS}}} \\
 &= \sqrt{\frac{\pi}{2}} \cdot \frac{1}{PAR}
 \end{aligned} \tag{3.3}$$

Note that the efficiency of class AB amplifier is now inverse proportional to the value of PAR. According to reference [26], the averaged PAR value of 80 samples of music fragments can be as high as 15 dB. Therefore, the actual power efficiency of a class AB amplifier is very low when amplifying real audio signals. Fig 3.1 plots the power efficiency of a class AB amplifier with a sine wave input and a 15 dB PAR input respectively. It can be seen that the maximum power efficiency when amplifying real audio signals can be as low as around 20%. This is due to the fixed high voltage supply used for class AB output stage where it defines the maximum output swing of the amplifier. However, for most of the time the signal level remains relative low and a large portion of the supply voltage is applied to the

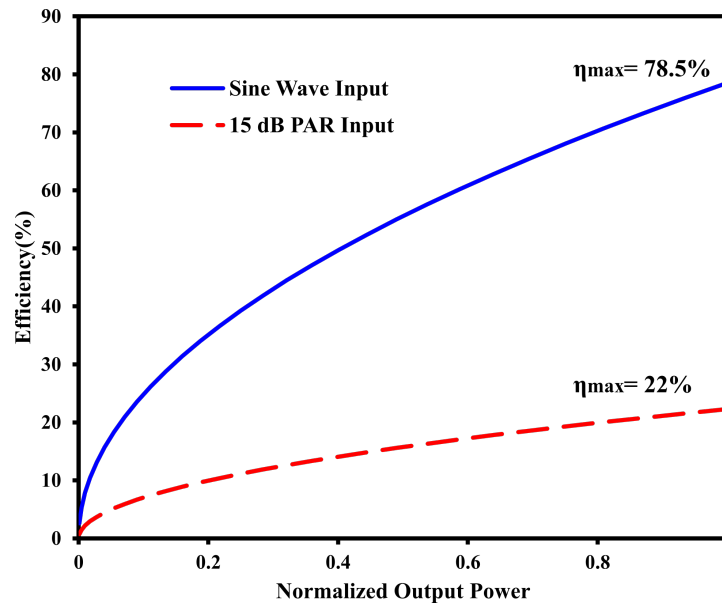


Figure 3.1: Comparison of class AB amplifier efficiency with different PAR input

power transistor. Thus, the conduction loss wasted on the power transistor is tremendous under this condition. A straightforward solution to this issue is to adaptively change the level of power supply voltage so that the instant supply voltage does not need to be as high as that required by the peak voltage swing. In ideal case, it can be at a precise level for which the output swing requirement of the current signal amplitude is just satisfied. This gives the definition of an adaptive supply power amplifier.

Comparing to the evolution from class A and class B amplifiers to class AB amplifier where the output stage of linear amplifier is modified to overcome the distortion issue, the change into adaptive supply focuses more on the output stage architecture where the adaptive supply is used. The concept of the adaptive supply power amplifier is illustrated in Fig 3.2. Briefly, an adaptive supply amplifier consists of three major building blocks, the input signal amplitude sensing block, the adaptive power supply unit and the linear power amplifier. The linear amplifier module used is usually a typical class AB power amplifier for its good linearity performance and mature structure. The other two blocks construct the

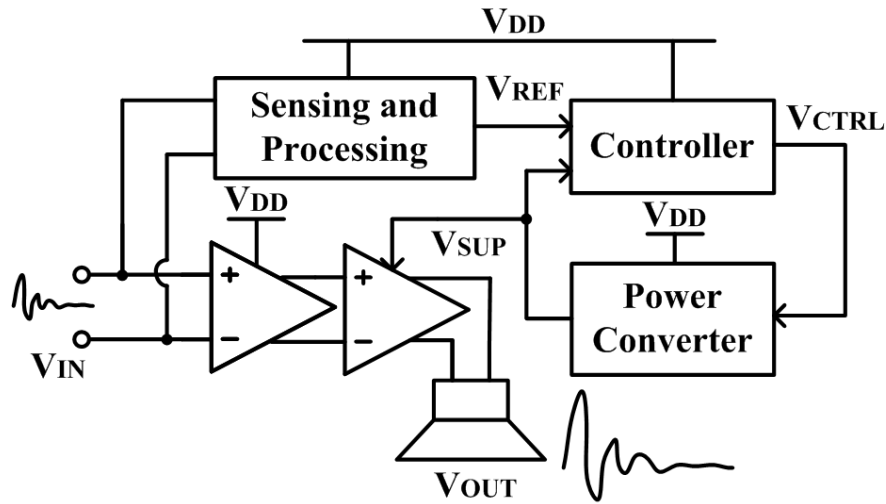


Figure 3.2: Conceptual block diagram of the adaptive supply power amplifier

adaptive supply generation module, the sensing block senses the instant input signal amplitude and generates the reference voltage for the power supply unit, then the power supply unit will adjust its output accordingly. The power conversion efficiency of this power converter is vital to the efficiency of the system as now it serves as the supply to the amplifier. Therefore, Switching Mode Power Supply (SMPS) becomes the only choice for this architecture. Generally there are two types of power converters, the switched capacitor-based and the switched-inductor based power converters. Both power converters when implemented as SMPS are also known as dc-dc converters. Although both converters transfer power to the load in a switched manner, there are still huge differences in terms of individual applications. The switched capacitor dc-dc converters can only obtain high conversion efficiency at the predefined conversion ratios. Thus, for highly efficient power conversion, the switched capacitor converter can only output at several discrete voltage levels. For switched inductor converter like buck converter, the conversion efficiency is high for a wide output range and is considered capable to output a continuously changing output which tracks the reference voltage.

Based on the discrete and continuous output voltage levels the power converter can

produce, the architectures of the adaptive supply amplifier are further classified into class G and class H amplifiers. In [26], the class H is referred as a special category of class G amplifier in which the higher supply voltage is realized by a bootstrapped capacitor and only temporary power from this higher supply voltage is available. In [22], an adaptive supply power amplifier which is able to continuously adjust the supply output is proposed but is referred to as class I amplifier. To the author's best knowledge, there is yet a naming convention for such architecture. However, the idea of this topology is actually one step further from the class G amplifier. To avoid any confusion resulting from the naming, such adaptive amplifier with a continuously changing supply is referred as class H amplifier in this thesis.

In the market for modern audio amplifiers, the adaptive supply amplifiers have become a popular topic for its good balance between linearity and power efficiency. For the rest of this chapter the two categories of the adaptive supply power amplifier will be analyzed and discussed. Their advantages and disadvantages are to be evaluated to appreciate the challenges of designing an optimal adaptive supply amplifier. Then the proposed class H amplifier architecture with output common-mode modulation will be delineated.

3.2 Class G Power Amplifiers

3.2.1 Power Efficiency of Class G Amplifiers

A class G amplifier is basically an analog linear amplifier which uses different supply voltage levels depending on the current amplitude of input signal level. Generally it has two sets of power supply rails, namely the high voltage supply V_{DDH} and the low voltage supply V_{DDL} . The supply of the output stage selects between the two discrete values and thus the class G topology is sometimes referred as the "supply switcher". Fig 3.3 depicts a typical dual-rail class G output stage and its output waveforms. In this case, the supplies of the

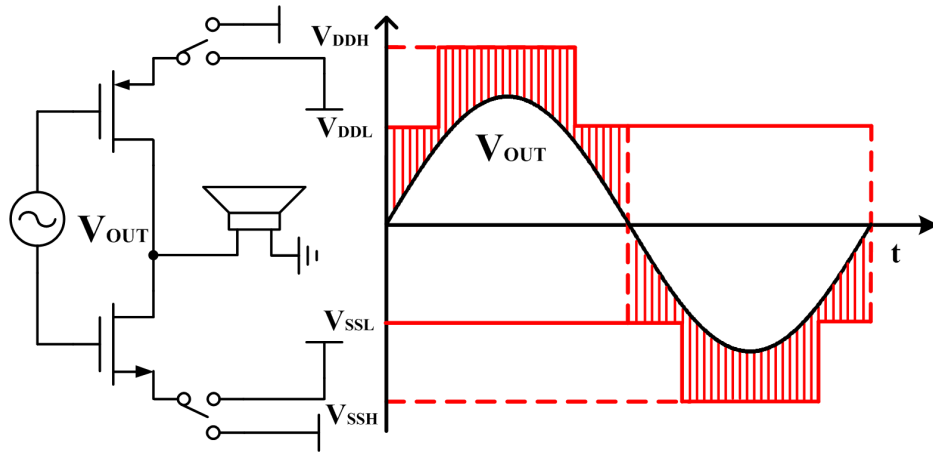


Figure 3.3: A typical class G output stage with dual-rail power supplies and its output waveform

output stages constantly switch among four different values including two sets of negative voltage levels so as to bias its output node to ground level.

As can be observed from the figure, the supplies of class G amplifier involves four switching activities for one sinusoidal cycle. The red solid lines indicate the amount of voltage drop across the power transistor that is strongly conducting, multiplied with the instant current it provides to the load it gives the conduction loss dissipated by the power transistor at that moment. As compared to class AB design where two fixed supplies V_{DDH} and V_{SSH} are adopted, the class G topology reduces such conduction loss by shrinking the supply voltage, better overall power efficiency can therefore be achieved.

To validate its efficiency superiority, the power efficiency of class G amplifier should be calculated. It is obvious that the power supply configuration of class G amplifier varies for different input signal levels. If the amplitude of the input signal keeps on being high above the switching threshold, then V_{DDH}/V_{SSH} will be selected throughout the cycle. As a result, the power efficiency of a class G amplifier makes no difference from a class AB amplifier. However, if the amplitude continues to be very small the V_{DDL}/V_{SSL} will be selected, and the voltage drop wasted on power transistor is cut drastically. Therefore it is evident that

the efficiency analysis of a class G amplifier needs to be calculated in a piecewise manner [27]. Meanwhile it is also dependent on the ratio of low supply to high supply as it shows directly to what extent the power is saved. Here the low-to-high supply ratio is denoted as $\alpha = V_{DDL}/V_{DDH}$, where α ranging from 0 to 1.

The efficiency of class G amplifier is analyzed with a sinusoidal input signal. The input amplitude is increased from 0 to the maximum level where the peak output swing is reached. When input signal level is small and the output swing is within the range that the V_{DDL} can handle, no switching to the V_{DDH} is triggered, thus the system operates as a normal class AB amplifier under the supply of V_{DDL} and its efficiency for such condition can be expressed as:

$$\eta_{G1} = \frac{\pi}{4\alpha} \cdot \frac{V_{OUT}}{V_{DDL}}, \text{ for } 0 < V_{OUT} \leq V_{DDL} \quad (3.4)$$

For larger input amplitude, V_{DDL} is insufficient to provide the output swing and the supply is going to switch to V_{DDH} . For this condition, the average power draw from the supply must be calculated by integration for different supply voltage respectively. The transition angle from where V_{DDH} is activated for a sine wave cycle can also be determined. The expression of the power efficiency for larger input signal level can be expressed as:

$$\eta_{G2} = \frac{\pi}{4} \cdot \frac{V_{OUT}}{V_{DDH}} \cdot \frac{1}{\alpha + (1 - \alpha)\cos\theta_t}, \text{ where } \theta_t = \sin^{-1}\left(\frac{V_{DDL}}{V_{OUT}}\right) \quad (3.5)$$

for $V_{DDL} < V_{OUT} \leq V_{DDH}$

By combining the expressions for the two input scenarios the power efficiency of the class G amplifier can be acquired. For a better illustration, the output power is normalized to the maximum output power to describe the instantaneous signal level with respect to the maximum power level of the amplifier. It is also important to take note that rail-to-rail output swing is assumed for the above calculation, thus we equalizes the peak output swing V_{PEAK} to the supply voltage V_{DDH} which is usually not the case for a real linear power

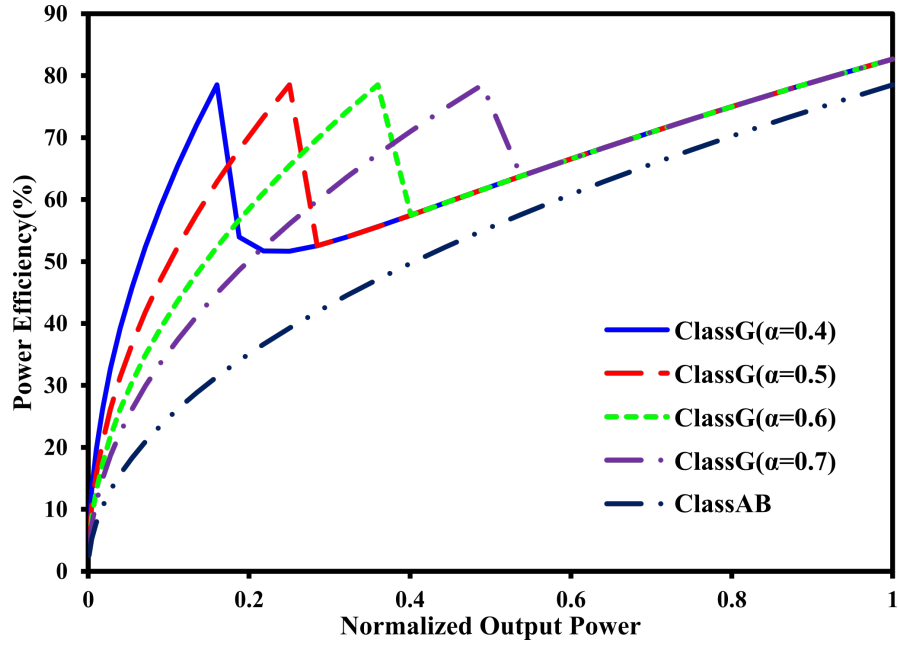


Figure 3.4: Efficiency comparison among class G amplifiers with different V_{DDL} and class AB amplifier with same V_{DDH}

amplifier. Therefore, the above efficiency obtained is the theoretical value and the values for real cases should be lower. As can be observed from the equations, besides the output swing which determines the transition angle from V_{DDL} to V_{DDH} , the low-to-high supply ratio α is also a variable that shapes the efficiency curve. Therefore, to have a better understanding of the class G amplifier efficiency, the efficiency is plotted over the normalized output power for different values of α as in Fig 3.4.

As shown in the figure, the efficiency of a class G amplifier incurs a sharp drop as V_{DDH} is selected as the supply voltage. Therefore for the region where the input signal exceeding the threshold voltage, the class G operates just as a conventional class AB and again substantial amount of voltage is wasted across the power transistor which makes the conduction loss surges. For the value of V_{DDL} , there does not exist a rule of thumb saying which value is better, as it be seen clearly from the chart that there is a trade-off between light load efficiency and medium load efficiency when the α ratio increases from 0.4 to 0.7. However, it is true that the power efficiency is closely related with the PAR value of the

input signal. For example, for audio signals with high PAR values, a smaller α ratio would be beneficial as most of the time V_{DDL} is sufficient to provide the output power. While the medium load range efficiency becomes important as the PAR ratio drops therefore rendering the optimization of α ratio input dependent.

3.2.2 Class G Amplifier with Dual-rail Power Supply

Class G amplifier with dual-rail power supplies has been a hot research topic in recent years [4, 28, 32–35]. It is convenient to use dual-rail supply as the output node can be biased to ground level and hence eliminate the use of a bulky dc decoupling capacitor which normally exists in the design of a single supply amplifier. The topology of class G amplifier with dual-rail power supply is relatively fixed as the output CM level is referenced to the ground at all times, it usually consists of a single-ended class AB amplifier, a switched capacitor dc-dc converter for generating V_{DDL} and a negative charge pump to produce the negative replica of the supply voltages. In recent designs, the research work mainly focuses on the performance optimization of the amplifier system. For instance, class AB quiescent current control [4], class AB PSRR enhancement [4, 28, 32], soft switching techniques to mitigate distortion during mode transition [34, 35] and control algorithms to improve overall power efficiency [4, 28].

Fig 3.5 depicts the schematic of one approach of dual-rail supply class G amplifier [34]. Two pairs of power transistors being supplied by two sets of dual-rail power supplies V_{DDL}/V_{SSL} and V_{DDH}/V_{SSH} serve as the class G output stage. The class G operation is enabled by steering the current that flowing in the class AB biasing circuitry and controlling the gate drive voltages of each power transistor. A dc voltage V_{OFFSET} is used as the threshold to trigger the transition at the output stage in advance, so that clipping can be avoided. The merit of using two pairs of power transistors is that the supply node will not endure a sharp step change from V_{DDL} to V_{DDH} or vice versa. Instead it goes through a handshake process between the two power transistors. Thus the disturbance from the

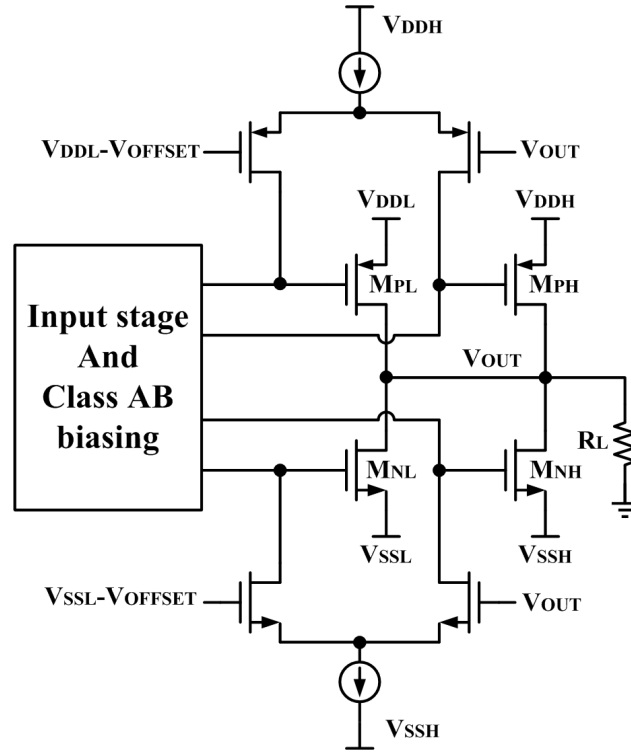


Figure 3.5: Schematic of one dual-rail supply class G amplifier embodying parallel output stages

supply node becomes much gentler. However, due to the handshake process the continuity of the current driving capability is affected, thus distortion can be expected during the transition of output stage. Moreover, the decision of shifting to higher supply is made by assessing the level of output voltage which has a latency from the real input. Therefore, the sensing of input signal level is kind of delayed as compared to the real-time input signal stream, which may cause waveform clipping as the frequency of input signal increases. The reported THD+N value is -80 dB for class AB mode when signal level is small, and it incurs a degradation of 6 dB as signal level increases and class G operation starts to take over.

Another method using the paralleled output stages is shown in Fig 3.6 [4]. Different from the previous one where the paralleled output stages are supplied by different supply voltages, the parallelism in this design is embodied with a combination of class AB and class B output stages. Being supplied with the same power rails, the class B output stage

is simply an auxiliary current provider which supports the current driving capability of the class AB output stage during large signal transient. Whereas the function of class AB is only as a quiescent current controller and amplifier for light load conditions. The voltage level shifter biases the gate of class B transistors and make sure they only become activated when the load is demanding. The benefit of doing so is that the size of class AB transistors can be designed relatively smaller (5 times smaller in this case) than its usual size as now it only takes care of the quiescent state and small-signal currents. As a result, the variation of quiescent current due to mismatch can be alleviated.

However, the reduction on the sizing of class AB transistors also bring in problems. With smaller transistors, the output stage transconductance g_m reduces, which results in smaller gain for the quiescent state as well as the light load conditions. Hence, the feedback loop gain of the amplifier is reduced which increases the distortion. To increase the loop gain of the system, an additional high-order loop filter is inserted before the class AB/B amplifier. The price paid here is the increased complexity and power consumption of the system. The measurement results exhibit a PSRR of 120 dB and a THD of -95 dB, but these performances are mainly ascribed to the high-order loop filter instead of the novelty of the output stage.

The schematic of the latest work on dual-rail class G amplifier is depicted in Fig 3.7 [28]. In this approach a single class AB output stage is used and it is supplied with the outputs of the positive and negative charge pumps. The quiescent current of the two power transistors are sensed, averaged and compared with a reference value and finally the gate drive voltages are adjusted to get a predefined quiescent current. The circuitry in the red box shows the negative feedback loop used for quiescent current control. Since the supply voltages for the output are from dc-dc converters and are usually quite noisy, a pair of supply noise correction circuits are added in this design. The noise from the supply is sensed and coupled to the gate drive voltage so that the supply noise cancels out in the expression of gate-to-source voltage, hence the bandwidth of PSRR is much extended. Another improvement of this design is

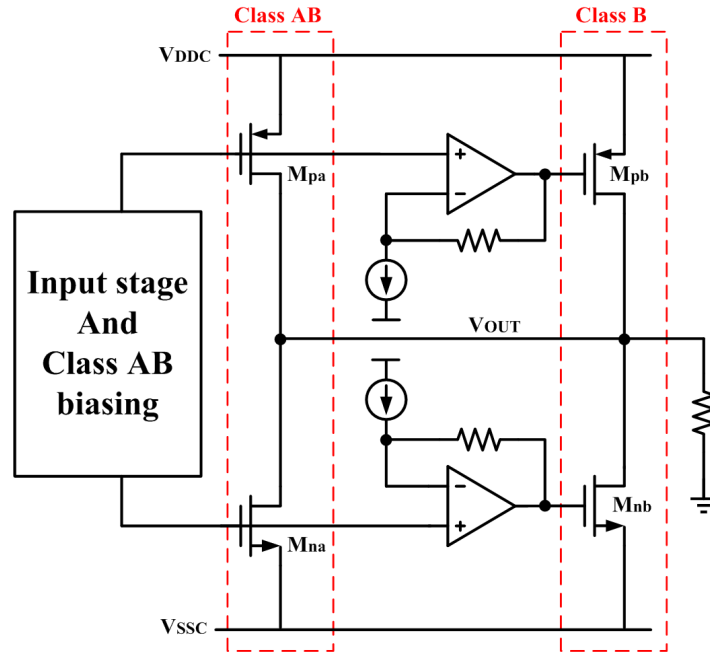


Figure 3.6: Schematic of one dual-rail supply class G amplifier embodying class B/AB output stages

on the algorithm of the charge pump controller. In normal class G systems, the output of charge pump toggles between V_{DDL} and V_{DDH} depending on the amplitude of the signal. In this design, to avoid the power losses resulting from the excessive switching activities and the charge pump, a minimum hold time is defined and implemented. Once the class G threshold is reached, the system will generate a minimum hold time of 100 ns, and the output of the charge pump will stay at V_{DDH} during this period. Therefore excessive switching between the two voltage levels is forbidden which results in better overall efficiency.

With the help of the supply noise correction circuits, the above mentioned class G amplifier achieves a remarkably high PSRR of 130 dB. However, its quiescent current variation from die to die is never mentioned. Due to the supply noise correction loop, the quiescent current sensing amplifier is actually separated from the output stage. Therefore, its quiescent current control capability would have been compromised.

In summary, class G amplifier with dual-rail supply have been optimized in terms of

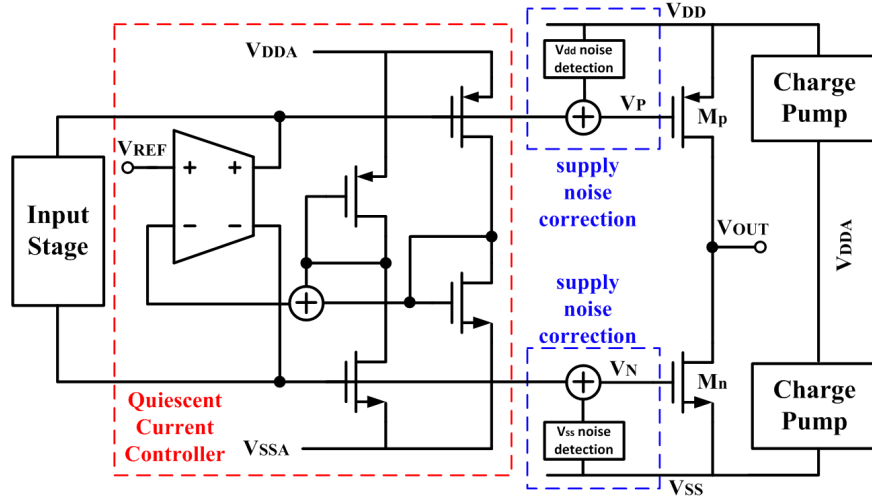


Figure 3.7: Schematic of one dual-rail supply class G amplifier with PSRR-enhanced class AB stage

linearity and supply noise rejection ratio. Some designs achieve even better performance than the pure class AB amplifiers. However, in order to generate the negative power supplies, additional charge pumps have to be added into the system. As switched capacitor dc-dc converter has already resides within the system for V_{DDL} generation, the added charge pump would become a hindrance to the precious chip area. For previously reported class G amplifiers operating with dual-rail supply, the maximum RMS output power is capped at 62 mW [28]. This may be enough for driving a headphone in a portable device like cell phone, while for other applications like driving the speaker in a tablet a few hundreds of mW output power is required. For a even larger output power requirement, the area for power switches as well as flying capacitors will become a big issue. Meanwhile, the existence of negative supply requires the use of deep n-well process technology which further increases the implementation cost. Applications for class G amplifier with dual-rail supply are limited by the output power rating as well as implementation cost.

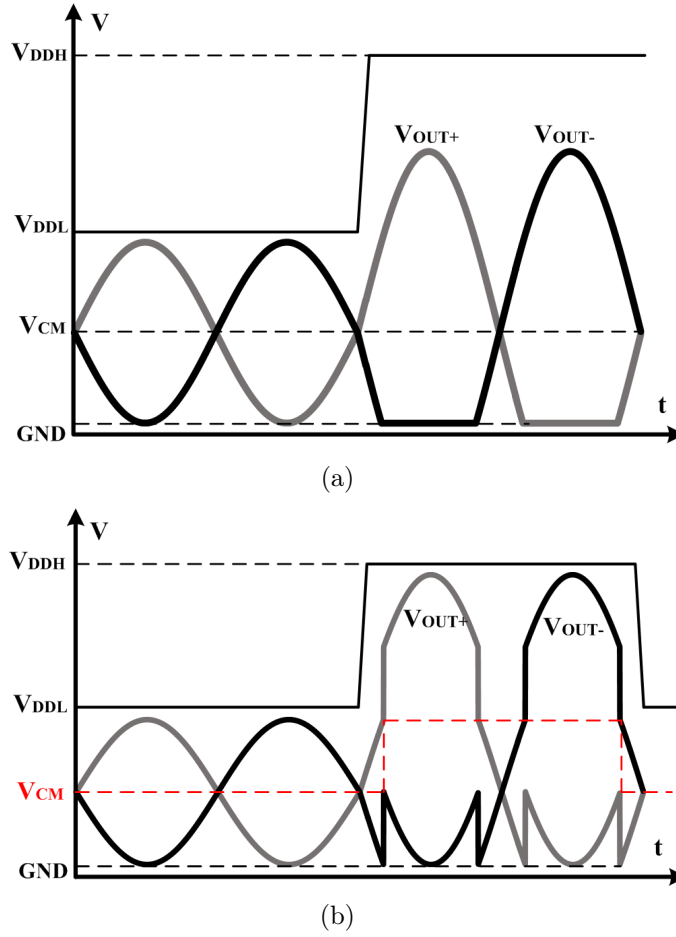


Figure 3.8: Single supply class G amplifier waveforms with (a) fixed output dc bias, (b) adaptive output dc bias

3.2.3 Class G Amplifier with Single-rail Power Supply

For class G amplifier with only single-rail supply, the output of the amplifier is dc biased at half the supply voltage to achieve maximum output swing. Unlike the amplifier with dual-mode supply, output of a single supply amplifier is not ground-referenced. Therefore a dc-decoupling capacitor is added to block the dc current under quiescent state. However, the size of this capacitor is normally in terms of hundreds of μF for the high-pass filter to have a cut-off frequency at the lower boundary of the audio signal band. The size of this capacitor is so huge that it has to be eliminated for a compact design. Thus differential output stage like the bridge-tied-load (BTL) structure seems to be the only solution for

single-rail supply amplifier, like in reference [36] two class AB amplifiers are connected tail-to-tail to implement the BTL structure. Another benefit differential output stage introduces is that the maximum output swing gets doubled hence makes the maximum output power four times larger.

A common problem encountered in single supply class G design is on the output dc biasing level. As mentioned above, output dc level should always be biased at half of the supply voltage. For class G amplifiers, since the supply voltage is switching between two levels, the output common mode voltage should also be changed accordingly. If output dc stays at half of the low supply, clipping will occur when the signal level becomes larger, which can be seen from Fig. 3.8(a). When the output dc bias is changing with the input signal level, clipping can be avoided as shown in Fig. 3.8(b). Although the waveforms of the two output nodes in Fig. 3.8(b) looks highly distorted as the common mode (CM) voltage is also switching, the differential output waveform can still be recovered as the CM voltage cancels out.

However, the switching nature of the output CM voltage brings additional concerns on the amplifier's linearity performance. Since the output CM level is now switching between half of V_{DDL} and V_{DDH} , it becomes pulsating as well. Therefore, the linearity performance of a single-rail supply class G amplifier is compromised as large step signals are applied not only to the power supply but also to the Common-mode Feedback circuit (CMFB). The THD performance of reference [36] is only 0.02% which is almost 20 dB larger than the state-of-the-art of dual-rail class G counterparts.

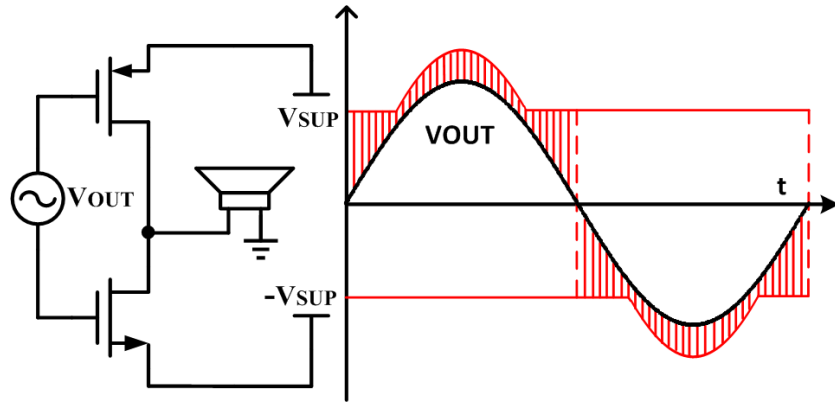


Figure 3.9: Typical class H amplifier and its output waveforms

3.3 Class H Power Amplifiers

3.3.1 Power Efficiency of Class H Amplifiers

Class H amplifier, as its naming implies, is actually one step further from the class G concept. The idea of class H operation is quite similar to that of a class G where the efficiency is improved by reducing the voltage drop wasted on power transistors. Different from the class G amplifier the supply of which connects directly to the high supply once the signal level reaches its switching threshold, the supply of a class H amplifier tracks the input signal level and keeps the voltage drop across the power transistors to a predefined value when the switching threshold is met. The output waveforms of a typical class H amplifier are plotted in Fig 3.9. Therefore, the efficiency of class H amplifier will not incur a drastic drop when the high supply kicks in and keeps increasing as the output power becomes larger. Therefore its efficiency plot is expected to have a similar shape as that of class D amplifiers.

Before deriving the efficiency expression for a class H amplifier, a set of terms should be defined as follows. V_{DDL} is the low voltage supply and V_{DDH} is the high voltage supply, V_{DSAT} is the headroom voltage defined for power transistor to ensure its correct operation region, R_L is the load resistance and I_Q is the quiescent current consumed by the whole

system. The maximum output swing under the low voltage V_{DDL} is equal to $V_{DDL} - 2V_{DSAT}$. The power efficiency is defined as the RMS output power delivered to the load over the average power draw from the battery. For a sine wave input, the output is also supposed to be a sine wave signal. It is easy to calculate the rms power of a sinusoidal signal once the amplitude and the load resistance is given. Thus the tricky part falls on the calculation of average power which is normally acquired through integration over one period. For small input levels, the dc power consumption is identical to the case of a class AB, while for larger signal levels, the expression becomes much more complicated as it has both the class AB and class H operation. Since the output waveform is quite symmetrical, the calculation can be done for one fourth of the whole cycle which eases the tedious derivation process. The average dc power obtained from the source for class H mode operation can be mathematically expressed as:

$$P_{DC} = \frac{1}{T/4} \left(\int_0^{t_{trans}} P_{AB} \cdot dt + \int_{t_{trans}}^{T/4} P_H \cdot dt \right) \quad (3.6)$$

where in this expression, P_{AB} and P_H stand for the power consumption for class AB mode and class H mode respectively, and t_{trans} represents the instant when the switching threshold is reached and the circuit architecture transform from class AB into class H. The reason for doing it in a piecewise way is because the supply voltage under class H mode is varying with signal amplitude, thus making the calculation widely different from the way for class AB. The transition instant for one quarter of the cycle can be found as:

$$t_{trans} = \frac{1}{\omega} \sin^{-1} \left(\frac{V_{DDL} - 2V_{DSAT}}{V_{OUT}} \right) \quad (3.7)$$

V_{OUT} in equation (3.7) stands for the output voltage swing, evidently if the desired output swing V_{OUT} is even smaller than V_{DDL} , it means the switching threshold will not be triggered and no transition into class H mode will happen. Thus V_{OUT} must be larger than

$V_{DDL}-2V_{DSAT}$ to satisfy the threshold of class H mode operation. With this condition, the power consumption expression for class AB mode and supply-tracking mode within $T/4$ can be expressed as:

$$\begin{aligned}
 P_{AB} &= V_{DDL} \cdot \left(\frac{V_{OUT} \sin \omega t}{R_L} + I_Q \right), \\
 &\text{for } 0 < \omega t \leq \sin^{-1} \left(\frac{V_{DDL} - 2V_{DSAT}}{V_{OUT}} \right) \\
 P_H &= (V_{OUT} \sin \omega t + 2V_{DSAT}) \cdot \left(\frac{V_{OUT} \sin \omega t}{R_L} + I_Q \right), \\
 &\text{for } \sin^{-1} \left(\frac{V_{DDL} - 2V_{DSAT}}{V_{OUT}} \right) < \omega t \leq \pi/2
 \end{aligned} \tag{3.8}$$

The average efficiency under for a class H cycle can be calculated by dividing the rms output power to the average input dc power. The final expression of efficiency can be derived as:

$$\eta_H = \frac{P_{OUT,rms}}{P_{DC}} = \frac{V_{OUT}^2/2R_L}{\frac{1}{T/4} \left(\int_0^{t_{trans}} P_{AB} \cdot dt + \int_{t_{trans}}^{T/4} P_H \cdot dt \right)} \tag{3.9}$$

substitute equation (3.8) into (3.6) we can obtain the expression for the averaged input power under class H mode operation. For a clearer illustration, the quiescent current I_Q can be neglected during the derivation as normally it is much smaller than the load current under class H mode. Therefore, equation (3.9) can be extended into:

$$\eta_H = \frac{V_{OUT}^2/2R_L}{\frac{1}{T/4} \left(\int_0^{t_{trans}} V_{DDL} \cdot V_{OUT} \sin \omega t \cdot dt + \int_{t_{trans}}^{T/4} (V_{OUT} \sin \omega t + 2V_{DSAT}) \cdot V_{OUT} \sin \omega t \cdot dt \right) / R_L} \tag{3.10}$$

with proper simplification, the final expression for power efficiency under class H mode is shown as below:

$$\begin{aligned}
 \eta_H &= \frac{V_{OUT}^2}{a \cdot \sin 2\theta + b \cdot \cos \theta + c \cdot \theta + d} \\
 \text{where } a &= \frac{V_{OUT}^2}{\pi}, b = \frac{4V_{OUT}}{\pi R_L}(2V_{DSAT} - V_{DDL}) \\
 c &= \frac{-2V_{OUT}^2}{\pi}, d = V_{OUT}^2 + \frac{4}{\pi}V_{OUT}V_{DDL} \\
 \theta &= \sin^{-1}\left(\frac{V_{DDL} - 2V_{DSAT}}{V_{OUT}}\right)
 \end{aligned} \tag{3.11}$$

From equation (3.11), it can be observed that three variables directly affect the efficiency performance of a class H amplifier, they are the output swing V_{OUT} , the power transistor headroom voltage V_{DSAT} and the low voltage supply V_{DDL} . Their effects on the efficiency performance will be analyzed individually. First the value of V_{DDL} is fixed and the impact on V_{DSAT} is analyzed. Fig 3.10 plots the power efficiency curves for class H amplifier with different values of V_{DSAT} , and to show the superiority of class H topology on power efficiency, the theoretical efficiency curves for class G and class AB amplifiers are also included. For a fair comparison, the values for high and low supplies are selected to be 3V and 1.2V respectively.

It is quite evident that the overall power efficiency of class H amplifier is much higher than its linear mode counterparts. This is mainly due to the input-tracking supply which fixes the voltage drops across those power transistors, unlike the case of class G, the efficiency curve of a class H amplifier increases in a monotonic manner all the way to its maximum power level. Before the input-tracking supply kicks in, the efficiency curve of class H topology grows in the same way as a class AB amplifier with a smaller supply V_{DDL} . After passing the switching point, although the voltage drop is clamped to V_{DSAT} , with the increment of output swing (output power), the portion of voltage wasted as V_{DSAT} gradually becomes relatively smaller as compared to the current supply voltage. This explains why the efficiency of class H amplifier increases with a smoother slope after the transition point. As for curves

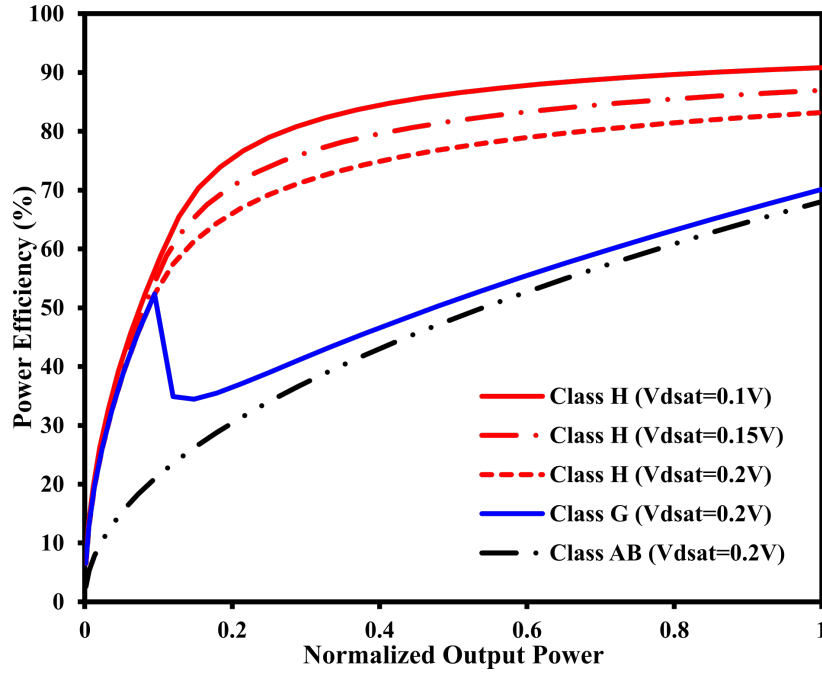


Figure 3.10: Efficiency comparison among class H amplifiers with different power transistor headroom voltage V_{DSAT} , class AB and class G amplifier

with different values of V_{DSAT} , it is also clear that a smaller V_{DSAT} gives better overall efficiency. Smaller V_{DSAT} simply means the power transistor works more like a power switch rather than a single-transistor amplifier, thus the efficiency looks more like that of a class D amplifier. However, the penalty associated with smaller V_{DSAT} is the degradation on amplifier's linearity, thus there exist a trade-off between higher efficiency and linearity.

The next step of the analysis is on the V_{DDL} 's effect on the efficiency. In Fig 3.11, the efficiency curves of class H amplifier with different V_{DDL} are plotted for comparison. This time V_{DSAT} is fixed to 0.2V, and the α denotes the ratio of V_{DDL} over V_{DDH} . The trend observed from this graph is very straightforward that a smaller V_{DDL} always gives better overall power efficiency. This unveils another advantage over the class G amplifier, unlike the design of class G amplifiers where the selection of V_{DDL} embodies the trade-off between light load and medium load efficiency, V_{DDL} should be as small as possible for the case of class H design. Again, the shrink on V_{DDL} does not come for free, it trades with the

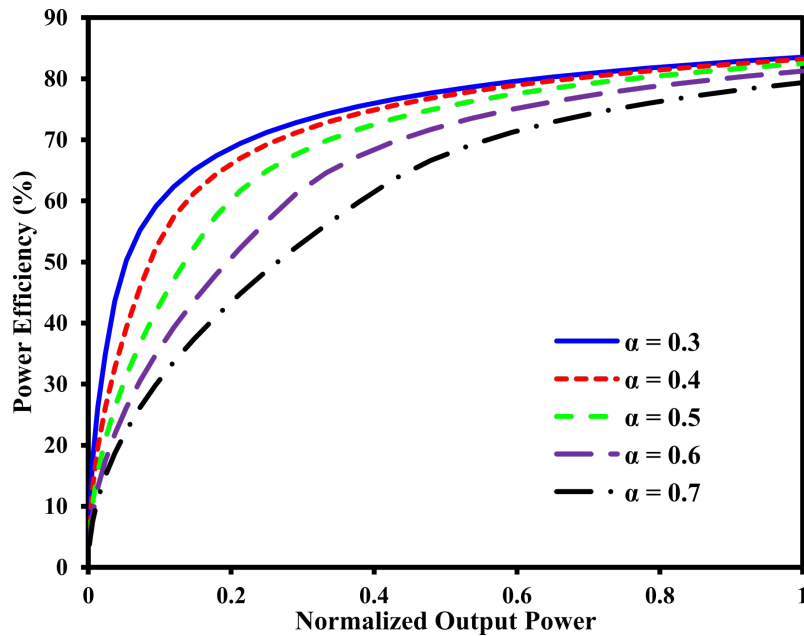


Figure 3.11: Efficiency comparison among class H amplifiers with different low voltage supply V_{DDL}

structure of the class AB output stage as well the sizing of the power transistors.

3.3.2 Design Considerations of Class H Amplifier with Input-tracking Power Supply

Similar to the class G amplifiers, the first and most difficulty problem of realizing the class H concept is on the implementation of the input-tracking power supply. To generate this input-tracking supply which can adjust its supplying voltage continuously with high conversion efficiency, the switched inductor dc-dc converter becomes the only feasible solution. For class G amplifiers, it is still applicable to generate a set of negative supply voltages V_{SSL}/V_{SSH} by using additional charge pumps, thus making the dual-rail class G topology rather popular among low power applications. However, for class H operation it is inappropriate to invert the phase of the supply voltage simply with charge pumps. First, for normal operation frequencies (around 1 MHz) an inductor in a dc-dc converter is area-consuming

and have to be implemented off the chip, thus it is not economical to design the output power rating small. Moreover, to invert the supply voltage with high power rating, the size of the charge pump will also increase drastically. Secondly, for the charge pump which is essentially a switched capacitor dc-dc converter, its higher conversion efficiency is only applicable for a fixed conversion ratio. Hence to convert a voltage that is continuously changing in an analog manner, the conversion efficiency will be largely compromised. Another way of generating the negative input-tracking supply is by using the inverting buck-boost topology or a transformer, but either way will have to make use of the external inductive component which render these options unpractical.

Since the only option to generate the input-tracking supply is via using one inductor-based dc-dc converter, the first design issue is on the topology of the converter. The buck and the boost converter are both very mature and widely-used topologies for dc power conversions. The only difference is on the input power source. For a typical battery-powered mobile device, a Lithium ion battery is normally used as the main power source which has a nominal cell voltage around 3.6 V and a end-of-discharge voltage around 2.8 V-3 V. To avoid the use of additional dc-dc conversion step, it is highly desirable to have a direct hook-up from the audio amplifier to the Lithium ion battery. In this case, the boosted voltage may easily exceed the junction tolerance voltage of transistors in deep sub-micro process and results in unnecessarily high output power for mobile devices. Therefore, a buck converter will be more appropriate.

As mentioned above, a buck converter providing single-rail supply voltage is most suitable for the class H amplifier design. Thus the second concern comes with the dc biasing points of the output nodes. To maximize the output swing, the output nodes are normally biased at half of the supply voltage. For amplifier with single-rail supply there will thus be a constant dc current flowing to the load at quiescent state. This problem gets exacerbated for audio power amplifiers with small resistive load. In the old days when the board area is not stringent, a dc decoupling capacitor will simply settle this issue. However, as the devices

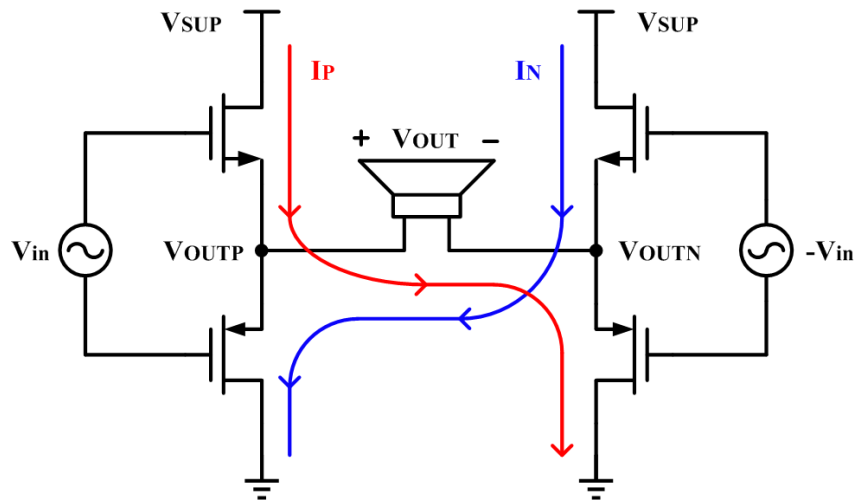


Figure 3.12: Transistor-level illustration of a BTL output stage

keep on shrinking in form factor, designers feel no longer affordable for such bulky passive components. Therefore, for class H architecture the differential output stage seems to be the only solution.

The differential output stage can be realized with a fully differential amplifier or a Bridge-Tied-Load (BTL) output stage. Fig 3.12 delineates the concept of a BTL output stage used as an audio driver. In this configuration, two pairs of power transistors are connected in a tail-to-tail manner, and input signals feeding into each single amplifier are 180° out of phase. During transient, the complementary MOSFETs in the diagonal direction will be conducting with respect to the phase of the input signal, thus generating either positive or negative current flowing through the audio load respectively. With such configuration, the output stage CM level can be biased at half of the supply voltage under quiescent state and eliminates the need for a dc decoupling capacitor. Moreover, the BTL output stage effectively doubles the maximum output swing with two output nodes swinging in the opposite direction. Thus the maximum output power that a BTL stage can deliver becomes quadruple as compared to a single-ended design whilst only gets the area and quiescent power consumption doubled. This gives differential output stage a prominent advantage to

be used for low power designs where the supply voltage is continually scaling down with the process technology. Last but not least, the fully differential structure can effectively suppress the even-order harmonics which will improve the amplifier's linearity performance.

The differential output stage does resolve the quiescent current issue with single-rail supplied amplifier. However, a distinction of the adaptive supply amplifiers (class G/H) from conventional linear amplifiers (class AB) is that the output stage supply voltage varies with input signal levels. This brings on the third design issue for single-rail supply class H amplifier that is the output CM biasing voltage. As previously touched in the section of single-rail supply class G amplifier, Fig 3.8(a) shows that a constant output CM biasing will lead to waveform clippings when the adaptive supply becomes enabled. This problem becomes even more tricky for class H mode operation as the adaptive supply is now tracking the input, thus the solution for class G case in which the output CM level switched between half of V_{DDL} and V_{DDH} will not work. Therefore, a new method for correct output CM level definition is required for a class H amplifier topology.

Last but not least, a key deficiency of the adaptive supply amplifier compared with normal class AB amplifier is the constant switching among different topologies. To make best use of the supply power, the system configuration morphs according to different load conditions. As a consequence, unwanted distortions are generated as the uniformity of the system is breached. Compared to the relatively matured class AB output stage design, it is usually the system-level uniformity that defines the performance limit of the adaptive supply amplifiers. Therefore on top of all those concerns on linearity, a desired class H architecture should not have its configuration vary too much for a wide load range.

stage supply V_{SUP} is fixed as V_{DDL} to save power, thus the output stage common-mode voltage (V_{OCM}) is clamped to half of V_{DDL} to maximize the output swing. The operation for the small signal level is the same as a class AB amplifier with low supply voltage of V_{DDL} . Hence these regions are denoted as "class AB mode" as shown in the figure. When the amplitude of the sine wave increases further and the switching threshold is reached, the class H mode operation kicks in and handles the operation for larger signal levels. It can be observed from the figure that when it is on the edge of transition from class AB into class H mode, one output node swings up to the value of $V_{DDL}-V_{DSAT}$ while the other swings down to V_{DSAT} . If the system stays in the class AB configuration then the node swinging downward will hit the ground level as input level keep increasing, which means clipping of output occurs. The proposed solution switches V_{OCM} directly to V_{DSAT} once the class H mode is triggered, and the node swinging downward will stay at the pre-defined value V_{DSAT} . On the other hand, the node that swings upward will have its gain doubled, hence the differential mode gain is intact and at the same time the output CM biasing issue is settled. The input amplitude during the class H mode is sensed and used as the reference voltage for the dc-dc converter, whereby the converter outputs a input-tracking power supply which is just one V_{DSAT} above the ascending output node. Through this approach, although the voltage waveforms at the two output nodes seem to be heavily distorted, the differential voltage can be recovered.

Implementation of the core circuits of the amplifier is depicted in Fig 3.14. AMP1 serves as a pre-amplifier stage which amplifies the audio input signals with predefined gains, the amplified signals are then compared with the window comparators to generate the control signals S_{1-4} for all the analog switches. The analog switches together with the resistive voltage divider which comprises of R_1 to R_4 are designed to perform the gain doubling or diminishing actions as mentioned previously. AMP2 and AMP3 are a pair of single-ended class AB power amplifiers connected in the BTL configuration. AMP4 is used to generate the reference voltage required by the dc-dc converter. As can be observed from the figure,

differential output voltage can be expressed as:

$$V_{OUT} = V_{OP} - V_{ON} = V_{id} \cdot A_{PRE} \left(\frac{R_3}{R_3 + R_4} + \frac{R_2}{R_1 + R_2} \right) \quad (3.12)$$

Where A_{PRE} is the gain of the pre-amplifier stage

- (ii) When input signal amplitude exceeds the switching threshold, either S_1 or S_2 will becomes high. For example, if S_1 controlled switches are closed, amplified signal through V_n will no longer see the potential divider and V_p will be connected to the ac ground V_{cm} . If R_1 and R_2 are designed to be of the same value, the gain from V_{in} to V_{on} is now doubled compared to the case in (i) while the gain from V_{ip} to V_{op} is killed. This action allows the V_{op} to stay at a predefined dc level instead of hitting the ground, at the same time the differential gain from $(V_{ip} - V_{in})$ to $(V_{op} - V_{on})$ is unaffected. Under this case, the output voltage will be either $V_{in} \cdot A_{PRE}$ or $V_{in} \cdot (-A_{PRE})$ depending on the polarity of the signals.

From the above analysis we can notice that there is inconformity for the gain expressions under different signal levels. When the signal amplitude is small at the beginning of each cycle, the gain for class AB mode is correlated to the resistor ratios, while for class H mode operation the resistive divider effect is bypassed and the resistor ratios are not present in the expression. Thus in order to keep the uniformity of the gain and hence the fidelity of the input signal, the following condition must be fulfilled:

$$\frac{R_3}{R_3 + R_4} + \frac{R_2}{R_1 + R_2} = 1 \text{ or } \frac{R_3}{R_4} = \frac{R_1}{R_2} \quad (3.13)$$

For smaller input level the system remain its configuration as in case (i). Even though the condition in (3.12) is not met the gain remains the same for each cycle. However, when input amplitude becomes larger, for one sinusoidal cycle, the configuration of the system will change constantly between case (i) and (ii), and all the three control signals will be ON

and OFF in sequence within one cycle as shown in Fig 3.13 (where H means high and L means low). The system sees three different circuit configurations within one cycle, thus the differential gain is distorted by the switching activities. In real implementation, there will be mismatch between the resistor ratios despite the efforts on careful layout. It is very hard to control the matching of all the resistors as well as linearity performance of those analog switches. Therefore the proposed topology compromises its linearity performance for the class H operation. As can be expected, the measured THD+N ratio of the benchmark design increases from 0.01% to 0.06% once the system operates in class H mode. In summary, the benchmark work proposed a rough idea of how the single-rail supply class H amplifier works, however, due to the constant change of the system configuration, linearity performance is still not comparable to the class AB counterparts. In other words, the benchmark work designed a good class AB amplifier but only a mediocre class H amplifier. The high linearity merit of the amplifier is only valid when input signal level is small, and the high signal fidelity is not preserved for all load conditions.

Chapter 4

Proposed Single-rail Supply Class H Amplifier

4.1 System Level Illustration of Proposed Architecture

In view of the design considerations for a class H amplifier, it is highly desired to have a new class H architecture that can operate with single-rail power supply and yet does not bring on additional distortion due to the innovation on the topology. Take a retrospection of the class H design in [22], we can find that the major cause of added distortion during the supply-tracking mode is due to the constant change of system configuration. However, it seems that such circuit reconfiguration is indispensable in order to achieve the class H mode operation. This is because the output CM level for low supply mode is fixed at half of V_{DDL} which is a improper value when the supply moves up with the increasing input amplitude. If no action is taken, there will be clipping due to the incorrect output dc bias. As for a single-rail supply class H amplifier, the fully-differential output stage must be applied to eliminate

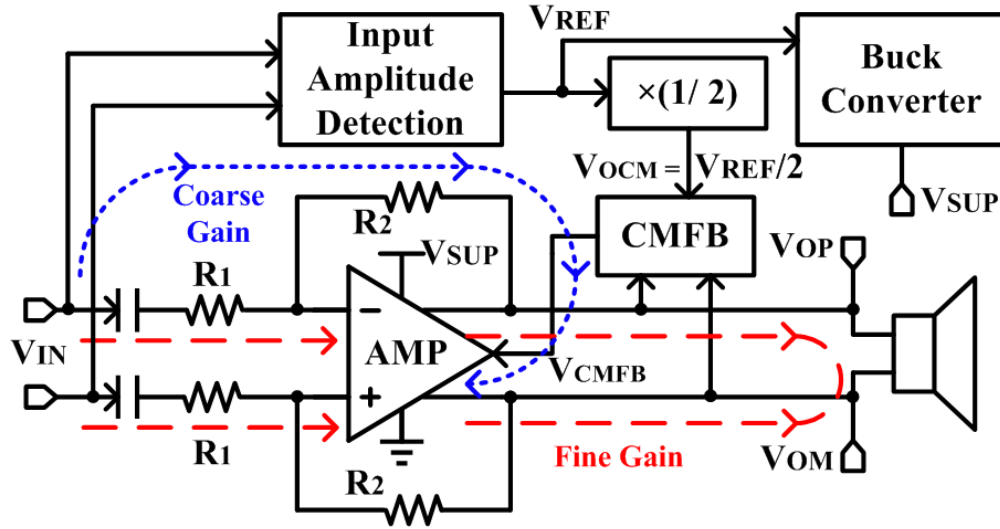


Figure 4.1: Proposed single-rail supply class H amplifier architecture

the dc decoupling capacitor. Therefore, an intuitive starting point to tackle this issue would be modulating the output common-mode voltage (V_{OCM}) of the differential amplifier.

In [22] the V_{OCM} is switched between half of V_{DDL} and one V_{DSAT} depending on the signal levels, thus the system configuration alters with V_{OCM} accordingly. To avoid such abrupt changes in system topology, a better idea would be making V_{OCM} adaptive to the input amplitude, whereby the output dc biasing point is correct all the time regardless of the instantaneous input amplitude. This gives the inspiration of the proposed class H amplifier architecture. Its detailed operation principle is to be delineated with the help of Fig 4.1 and Fig 4.2 in the rest of this section.

Fig 4.1 depicts the block diagram of the proposed class H architecture. It comprises three major building blocks, a fully-differential class AB power amplifier, an input amplitude detection (IAD) block and a buck dc-dc converter. The balanced input signals are fed into the IAD block and the class AB amplifier simultaneously. The IAD block will sense the input signal amplitude and outputs a reference voltage V_{REF} , which is to be used as the reference voltage of the buck converter. Thus the buck converter output will be tracking this reference level and is used as the supply voltage for the class AB amplifier output stage. The value

of this reference level is manipulated so that the output of the dc-dc converter V_{SUP} will be either V_{DDL} or input-tracking depending on the input signal levels. In order to maximize the output swing, V_{OCM} is defined as half the value of the instantaneous supply voltage V_{REF} . With the above definition, the common-mode feedback amplifier (CMFB) will sense and adjust the output dc bias level of the class AB amplifier to V_{OCM} . The key idea behind the proposed architecture is that we embedded the input signal amplitude information into the output CM level of the fully-differential amplifier. So that the gain seen from the two signal paths are modulated to avoid the waveform clipping issue in a single-ended power amplifier, at the same time the differential output voltage can still be recovered as the ac signal in output CM voltage cancels out.

As shown in Fig 4.1, there are actually two signal paths within the system. The one denoted with red line is the amplification path from input to the main amplifier output. It is named as the fine gain because the high-gain feedback loop will be applied to ensure the linearity, thus the closed-loop gain is well defined by the resistor ratios. The blue path indicates the gain from the input to the input-dependent V_{OCM} , to extract the input signal amplitude, several processing stages are added along the path including rectification, comparison, amplification and selection. Considering the distortion and latency along the path, the linearity of the ac portion in V_{OCM} is jeopardized as compared to the input. Thus it is labelled as the coarse gain path.

For a better understanding of the proposed architecture, the waveforms of the pertinent output nodes are plotted in Fig. 4.2. In this figure, a sinusoidal wave with sufficiently large amplitude to trigger the class H mode operation is used to illustrate the operation principle of the system. When input signal amplitude is small and the two output nodes swing within the range of V_{DSAT} to $V_{\text{DDL}} - V_{\text{DSAT}}$, the operation of the system is similar to the benchmark design, which is a fully-differential class AB driver with an output stage supply of V_{DDL} . Under this condition, the buck converter output is also fixed to V_{DDL} . When the input amplitude increases and output nodes swing beyond that range, same problem occurs as the

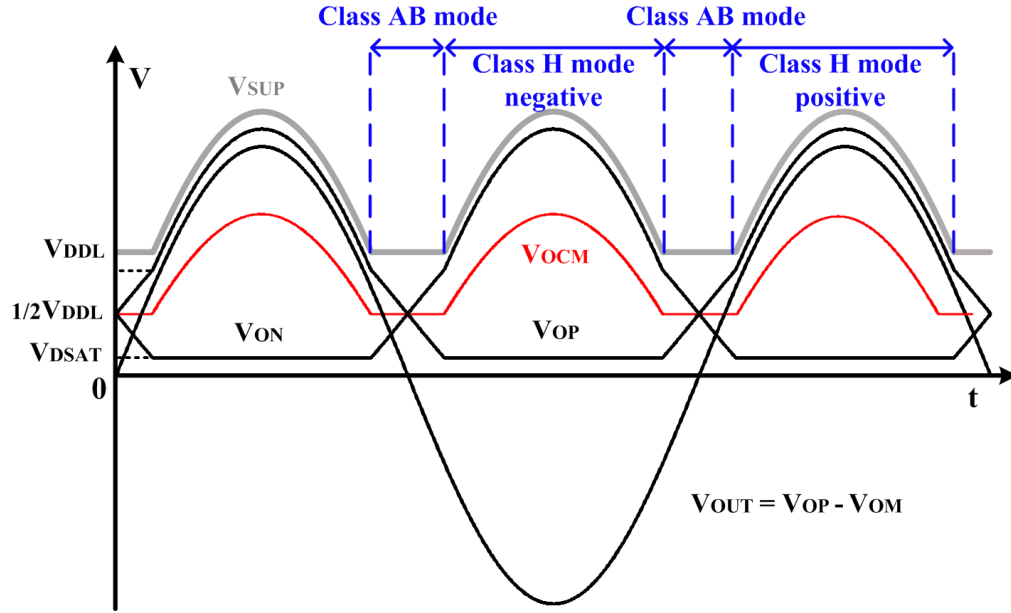


Figure 4.2: Waveforms of the pertinent output nodes of the proposed class H amplifier architecture

node swinging downward is going to hit the ground level. For this scenario, the input ac signal amplitude is extracted out and embedded into the output CM level V_{OCM} so that it becomes input-dependent. As shown in Fig 4.2, the ac gain in the V_{OCM} signal will be added to each output node. The values of the fine gain and the coarse gain are then equalized by using the same feedback resistor ratios. Therefore, the node which is supposed to swing up will see its ac gain almost doubled while the other output node will see its gain almost neutralized. The word "almost" used here indicates there is mismatch between the fine and coarse gain. However, critical matching between the two gain paths is not necessary as the purpose of an input-dependent V_{OCM} is only meant for avoiding waveform clipping. For instance, in Fig 4.2, when the system enters supply-tracking mode for the first time, V_{ON} is supposed to have its ac gain cancelled out and stays flat at the level of V_{DSAT} . Due to mismatch of the two gains, V_{ON} may stay at some levels close but not equal to V_{DSAT} . However, the value of V_{ON} under such circumstance only affects the headroom voltage of the NMOS power transistor, whose performance is insensitive to minuscule change on its

drain-to-source voltage. On the other hand, the differential output V_{OUT} is intact as the ac signal through the coarse gain path will be eventually cancelled as CM signals. As a result, the design requirement on the IAD block design is relaxed and its power consumption can be reduced.

Table 4.1: Nodal voltage expressions for the proposed class H architecture

Input Con- dition	$ V_{in} \leq V_{TH}$	$V_{in} > V_{TH}$	$V_{in} < -V_{TH}$
Operation Mode	Class AB	Class H(Positive)	Class H(Negative)
Buck Out- put (V_{SUP})	V_{DDL}	$2V_{DSAT} + A_{coarse} V_{in} $	$2V_{DSAT} + A_{coarse} V_{in} $
Output CM Level (V_{OCM})	$\frac{1}{2} \cdot V_{DDL}$	$V_{DSAT} + \frac{1}{2} \cdot A_{coarse} V_{in} $	$V_{DSAT} + \frac{1}{2} \cdot A_{coarse} V_{in} $
Negative Output (V_{ON})	$\frac{1}{2}(V_{DDL} - V_{in} \cdot A_{fine})$	$V_{DSAT} - \frac{1}{2}V_{in}(A_{fine} - A_{coarse})$	$V_{DSAT} - \frac{1}{2}V_{in}(A_{fine} + A_{coarse})$
Positive Output (V_{OP})	$\frac{1}{2}(V_{DDL} - V_{in} \cdot A_{fine})$	$V_{DSAT} - \frac{1}{2}V_{in}(A_{fine} - A_{coarse})$	$V_{DSAT} - \frac{1}{2}V_{in}(A_{fine} + A_{coarse})$
Differential Output (V_{OUT})	$A_{fine} \cdot V_{in}$	$A_{fine} \cdot V_{in}$	$A_{fine} \cdot V_{in}$

Table 4.1 summaries the nodal voltage expressions of the class H amplifier under different loading conditions. It can be observed that for output nodes V_{ON} and V_{OP} , due to the mismatch between the fine gain A_{fine} and the coarse gain V_{coarse} , the ac signal gain at the two nodes are not truly doubled or neutralized. However, the differential output V_{OUT} , the output CM voltage cancels out and the ac gain expression is kept uniform throughout different loading conditions. Therefore, there will be no additional distortion generated due

to different modes of operation and better THD+N performance can be expected for class H mode. Another benefit acquired from the design is that the output CM voltage is changing in a more smooth manner as compared to the benchmark design whose output CM voltages switches between two discrete values. Last but not least, the system complexity of the proposed class H architecture is much reduced, leading to much smaller quiescent power consumption of the system.

4.2 Design Considerations for Each Functional Block

As mentioned in the previous section, the system comprises two major building blocks, the main class AB fully-differential amplifier and the input-tracking dc-dc converter. Some design challenges associated with the proposed class H architectures are to be discussed in the rest of this chapter.

4.2.1 Enhancing Linearity of The Fully Differential Amplifier

For recent designs of both linear and switching amplifiers, a closed-loop structure with high in-band loop gain is widely employed to reject nonlinearity and retain high signal fidelity [4, 7]. According to the feedback theory, any nonlinearity injected along the signal path will be suppressed by the gain of the prior stages. Therefore high loop-gain is always of great help in feedback amplifier designs. This principle also applies for the proposed class H amplifier. There are three main sources of nonlinearity for the adaptive supply amplifier, the device mismatch, the disturbance injected from the varying output CM voltage level and the supply noise. The first one is seen in all types of amplifier design which can be mitigated by careful layout and application of feedback. The second type of disturbance is unique for single-rail adaptive supply power amplifiers. In methods [22, 36] the output CM level is switched constantly to enable the amplifier's operation with single-rail supply. These abrupt

changes on output CM level will lead to high frequency spikes at the output nodes and bring in more distortions. For the proposed design, the input signal is embedded into the output CM level which means there will be no sharp step changes in the output CM level. Thus less higher order harmonics can be coupled to the outputs. The last one is usually referred as the power supply rejection ratio (PSRR). For an adaptive supply amplifier, the supply at the output stage is from a dc-dc converter and can be very noisy due to the switching ripples. The supply of a class G amplifier sees steep and frequent switching between two supply rails which incorporates high frequency components with relatively large amplitude. These harmonics can be directly coupled to the output nodes through the large parasitic capacitances which are associated with the power transistors and hence result in spikes during mode switching. Unlike class G amplifiers, the supply of the class H amplifier moves in a smoother manner as its ac signal frequency is within the audio signal band. Therefore, the output of a class H amplifier should be cleaner than that of the class G. Besides the adoption of high-gain feedback loop, the symmetry of the fully-differential amplifier also have a critical impact on the PSRR performance.

Under the ideal condition where the perfect matching for all the devices including transistors, resistors and capacitors is achieved, the two signal paths in the fully-differential amplifier can be considered symmetrical. Therefore, the supply noise which is applied to the differential output stages simultaneously can be treated as a common-mode signal, and will get cancelled out for the differential output signal. Thus theoretically, the PSRR of a differential amplifier is infinity. However, such ideality is never the case in real implementation due to imperfect matching of the two signal paths. Here the effect of component matching on PSRR will be analyzed. The ac signal flow diagram of the proposed single-rail supply class H amplifier is shown in Fig 4.3.

The diagram briefly depicts how the supply noise is added to the fully differential amplifier by treating the amplifier as two balanced half circuits. Unlike a normal differential amplifier, the class H amplifier has its input stages supplied by a relatively clean power

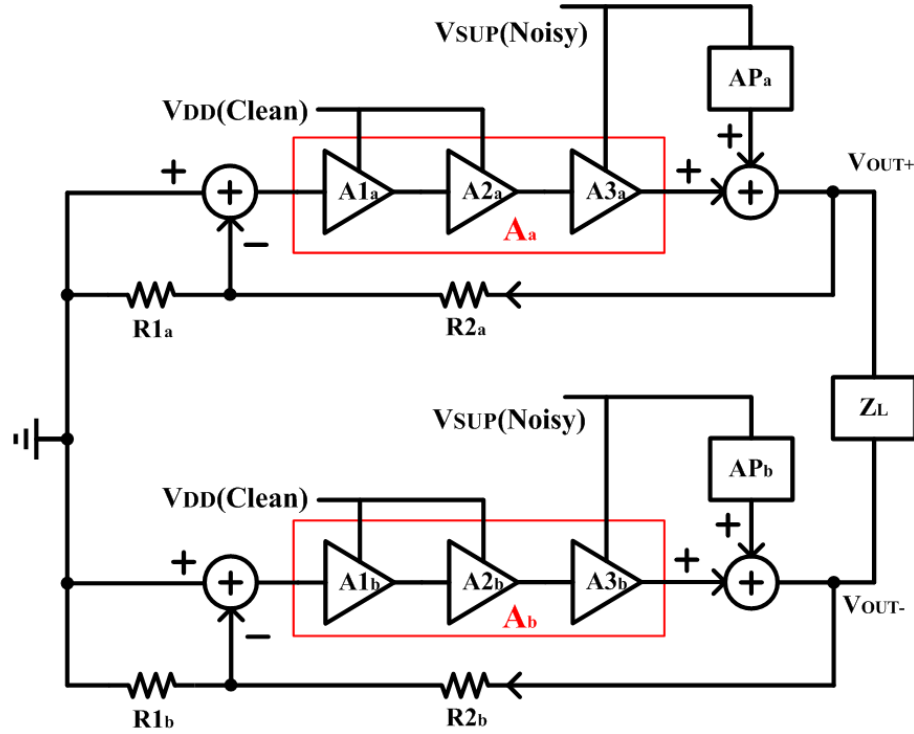


Figure 4.3: Signal flow chart of the proposed class H amplifier for PSRR analysis

source, while its output stages are supplied by the relatively noisy power converter. Therefore the main source of disturbance from the supply is coming from the output stages. Here the two different signal paths are labeled as a and b which also apply to the input and feedback resistors. The amplifier is connected in a closed-loop configuration with its gain defined as R_2/R_1 . The open-loop gain of the amplifier is denoted as $A_{a/b}$ as in the red box. $AP_{a/b}$ shows the supply noise gain from the output stage supply to the corresponding output node. For testing of PSRR, the input signals are grounded, and the output differential voltage across the load over supply noise can be expressed as:

$$\frac{V_{out+} - V_{out-}}{V_{sup}} = \frac{AP_a}{1 + A_a \cdot \frac{R_{1a}}{R_{1a} + R_{2a}}} - \frac{AP_b}{1 + A_b \cdot \frac{R_{1b}}{R_{1b} + R_{2b}}} \quad (4.1)$$

By assuming the loop gain of the amplifier is much greater than 1, the expression can be reduced to:

$$\frac{V_{\text{out}+} - V_{\text{out}-}}{V_{\text{sup}}} = \frac{A_{\text{Pa}}}{A_{\text{a}} \cdot \frac{R_{1\text{a}}}{R_{1\text{a}} + R_{2\text{a}}}} - \frac{A_{\text{Pb}}}{A_{\text{b}} \cdot \frac{R_{1\text{b}}}{R_{1\text{b}} + R_{2\text{b}}}} \quad (4.2)$$

In the above expression, $A_{\text{Pa}}/A_{\text{a}}$ is basically the open-loop supply rejection ratio of the half circuit. In real implementation, the signal paths of the two half circuits can not be perfectly matched hence there is definitely mismatch between this two ratios. For a simple derivation, the variation of the rejection ratio of path b with respect to path a is denoted as α , the above equation can be further extended to:

$$\begin{aligned} \frac{V_{\text{out}+} - V_{\text{out}-}}{V_{\text{sup}}} &= \frac{A_{\text{Pa}}}{A_{\text{a}}} \cdot \left(1 + \frac{R_{2\text{a}}}{R_{1\text{a}}}\right) - \frac{A_{\text{Pa}}}{A_{\text{a}}} \cdot (1 + \alpha) \left(1 + \frac{R_{2\text{a}}}{R_{1\text{a}}}\right) \\ &= \frac{A_{\text{Pa}}}{A_{\text{a}}} \cdot \left[\frac{R_{2\text{a}}}{R_{1\text{a}}} - (1 + \alpha) \frac{R_{2\text{b}}}{R_{1\text{b}}} - \alpha\right] \end{aligned} \quad (4.3)$$

It can be observed from the equation that both the symmetry of the feedback resistor network and the amplifier structure play a role in determining the PSRR of the differential amplifier. Due to the huge geometric ratio of the power transistors, the matching of the output stages can hardly be guaranteed or predicted. Therefore, to achieve better PSRR with the existing gain mismatch, the resistor ratios of the feedback networks should be better matched. As compared to single-ended amplifier, the expression inside the bracket is still much smaller than the resistor ratio value itself which shows the advantage of better PSRR for a differential amplifier. As inferred from the above analysis, to enhance the PSRR of the fully differential amplifier, the open-loop gain of the system should be maximized, the matching of the fully differential amplifier as well as the feedback resistor ratios should be accurately matched.

4.2.2 Latency Between the Coarse and Fine Signal Paths

One key challenge in design of adaptive supply amplifier is the latency issue of the power supply unit. As shown in Fig 4.1, there are two different signal paths the fine gain and coarse

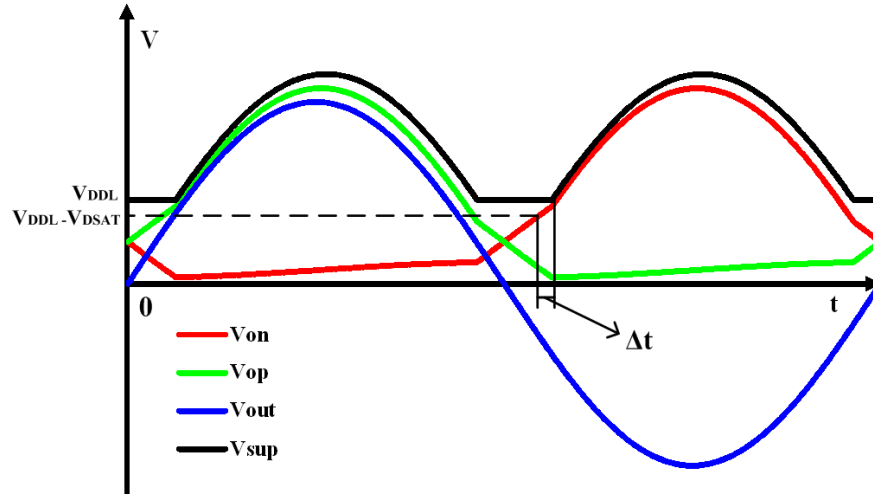


Figure 4.4: Simulated waveforms of the proposed class H amplifier with latency included

gain paths meant for signal amplification and adaptive supply generation respectively. The signal processing through these two paths are conducted at the same time, under the ideal condition when there is no delay through those analog building blocks, the event of input signal level exceeding class H threshold, output CM voltage becoming input-adaptive and buck converter output becoming input-adaptive should all happen simultaneously. However, under real cases, there is latency between the real-time input signal and the sensed reference voltage which indicates the amplitude of the signal level. Moreover, when the sensed reference voltage is used for the buck converter, it also needs response time for the buck converter to adjust its output voltage. Therefore, it is evident that there exists delay time between the main amplifier and the power supply module. During the increasing phase of the input signal, if the output swing of the amplifier keeps on increasing while the output stage supply voltage remains low as V_{DDL} due to this delay, the headroom voltages of the power transistors are going to be further reduced and possibly leads to clipping of waveform. Fig 4.4 depicts the simulated waveforms of the proposed architecture with this latency included.

The simulation uses a input signal of 2 kHz, and a delay time of $5\ \mu\text{s}$ from V_{in} to V_{OCM} and V_{SUP} . It can be noticed that when the threshold of mode switching is reached, that is when one output node exceeds the value of $V_{\text{DDL}} - V_{\text{DSAT}}$, V_{SUP} and V_{OCM} should have the input amplitude embedded and becomes input-adaptive. However, due to the added delay time, these two voltages stay at V_{DDL} and half of V_{DDL} respectively. As a consequence, the drain-to-source voltages left for both power transistor are squeezed which threatens the linearity performance of the amplifier output stage. In fact, apart from the gain mismatch between the fine and coarse gain paths, there is also a phase difference between them. As the latency is relatively fixed considering the physical circuit realization, this problem gets exacerbated as the frequency of the input signal increases. This is because as the frequency goes up, the relative phase difference between these two signal increase. Thus the worst case scenario for this issue should be tested with input signal of 20 kHz which is the upper boundary of the audio signal band.

To tackle this problem, various approaches had been implemented. One straightforward solution is to delay the audio input that is fed into the linear amplifier, therefore an additional delay time is added to the amplifier module [22]. The drawbacks of this solution is that it is still very hard to match this newly-added latency with the one of the power supply module, if it is over compensated similar issue will occur when the system is switching back from class H to class AB mode. Besides, the additional amplifier consume extra power and maybe more importantly, the distortion generated will jeopardize the linearity performance of the amplifier. A more popular and effective way used among those commercial products is to manage the delay in the digital domain as the audio signal is originally in the digital format before it is converted by the audio digital-to-analog converters (DAC). A good representation of such approach is illustrated in Fig 4.5 [4].

The magnitude of input signals is sensed and compared in the digital domain with a threshold voltage. A finite state machine (FSM) takes the comparator outputs to generate

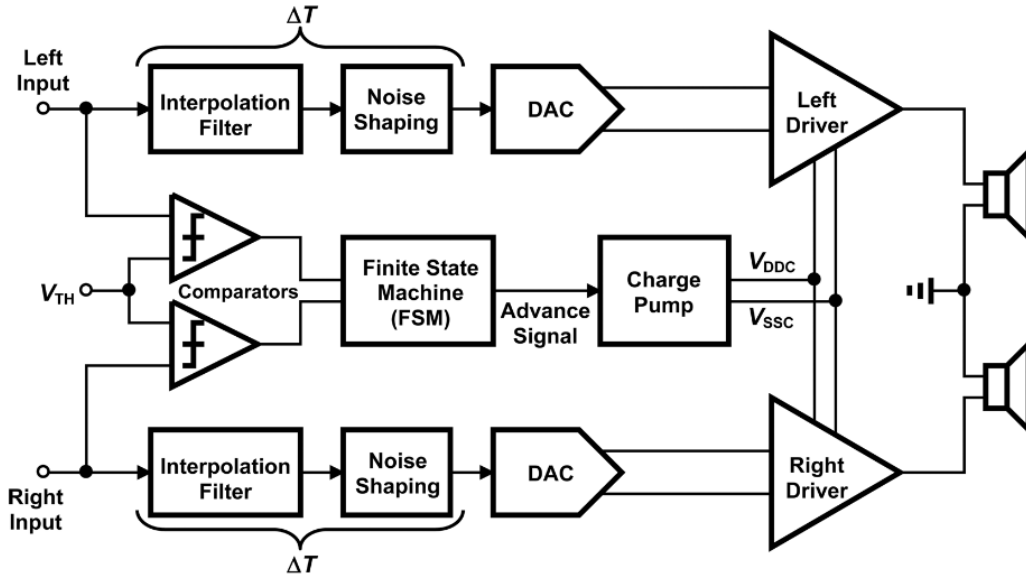


Figure 4.5: Control scheme of a class G audio amplifier with added latency

the signal that triggers the mode switching of the charge pumps. The latency is also generated in the digital domain which delays the input signal to the output driver and enables the predictive signal detection. This scheme achieves excellent prediction on the mode switching activities for an adaptive supply amplifier as it is more convenient to process and manipulate the data in the digital domain. However, the cost is that additional signal processing blocks are added which increases the system-level power consumption as well as design complexity. Moreover, the digital signal processing blocks are generally not easy to implement for an analog designer.

In order to mitigate this latency issue without the assistance of digital circuits, the design of headroom voltage V_{DSAT} has to be reconsidered. In chapter 3, the selection of V_{DSAT} is only subjected to the consideration of power efficiency. However, as can be seen from Fig 4.5, a larger headroom also gives better tolerance to the latency, thus sufficient value should be given to V_{DSAT} . On the other hand, increasing V_{DSAT} also decreases the overall power efficiency. To maintain a decent power efficiency plot that is comparable to class D amplifier, more effort should be put to reduce the latency of the power supply

unit. Therefore, as a key design requirement, the buck converter used in the proposed architecture should feature ultra-fast reference-tracking capability to allow the output stage supply voltage quickly settle to the desired level.

Chapter 5

Circuit Implementation

5.1 Architecture of Class H Power Amplifier

In the previous chapter we proposed a novel class H amplifier architecture with single-rail power supply, the concept of which is shown in Fig 4.1 in terms of block diagrams. In this chapter we will look into the details of the realization of each block of the system. The blocks in Fig 4.1 can be further crystalized as in Fig 5.1.

For the whole system, the single positive supply V_{BAT} will be used as the only power source, which mimics the Lithium-ion battery used for a typical mobile device. The nominal value of V_{BAT} is defined as 3.3 V, as the real voltage range for a Li-ion battery is from 2.8 V to 4.2 V, these two extreme conditions will also be used for testing. Input signals fed into the system first will be decoupled by the dc decoupling capacitors, this is to remove the dc bias level from the preceding processing unit which may be a DAC or a pre-amplifier. The Input Amplitude Detection (IAD) block senses and extracts the amplitude information of the current signal level. Based on its decision, it will output a reference voltage to both the CMFB amplifier as well as the buck converter. The buck converter will then adjust its output voltage to the desired level within its settling time, and together with the modulated

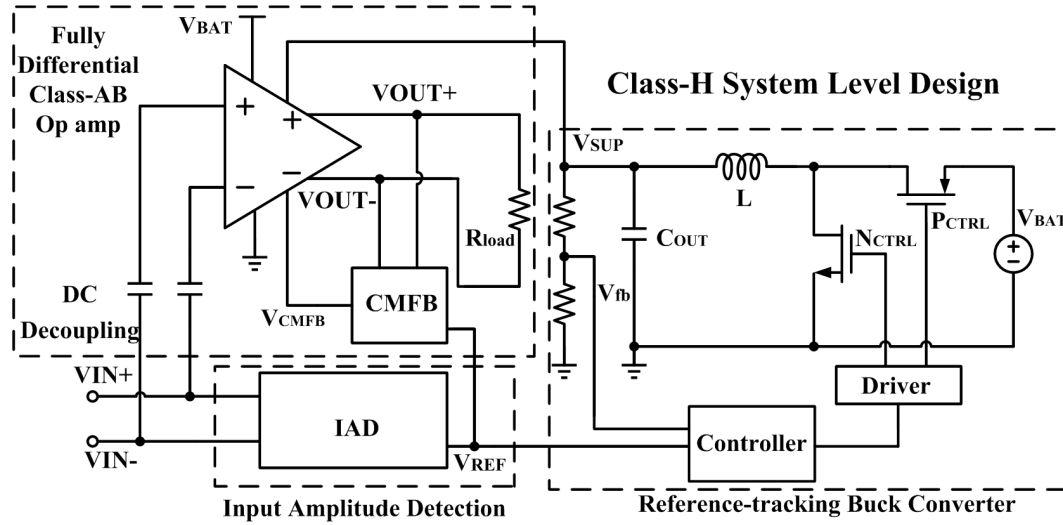


Figure 5.1: System-level architecture of the proposed class H amplifier

output CM voltage, the voltage drop across the strongly conducting power transistor in the class AB output stage will be optimized to the predefined level V_{DSAT} . Therefore the power efficiency is much improved compared to a conventional fixed-supply class AB amplifier. In the following sections of this chapter, the design details of each building blocks will be delineated.

5.2 Fully-differential Class AB Amplifier

5.2.1 Overview

The linearity performance of the class H amplifier is still embodied by the linear amplifier, thus the design of the class AB amplifier becomes paramount for the class H architecture to achieve high signal fidelity. As only single-rail power supply is used in this design, the fully-differential structure is required to eliminate the dc decoupling capacitors. Fig 5.2 depicts the block diagram of the desired three-stage fully-differential class AB amplifier.

For the concerns of signal gains, as discussed in the preceding chapters, a linear feedback

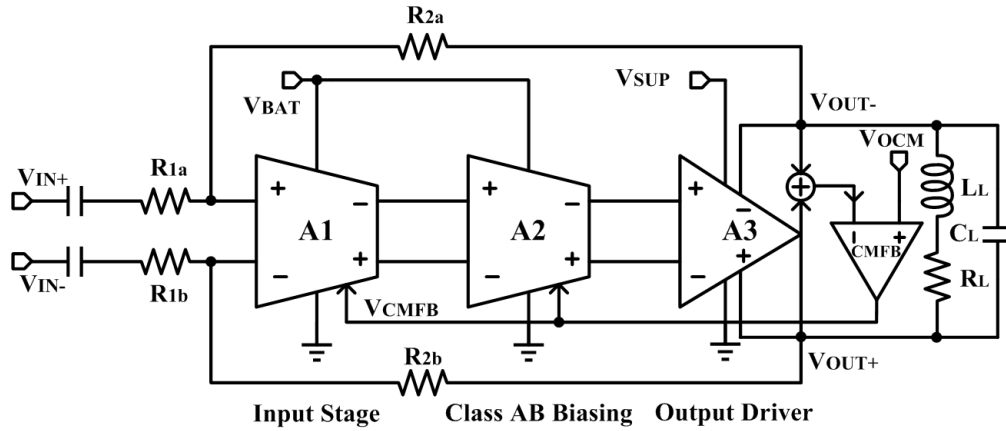


Figure 5.2: Block diagram of the fully-differential class AB amplifier

loop with high loop-gain is always preferred for better suppression to the nonlinearity and distortions that are injected into the system. For audio amplifiers, the loads of which are usually of small resistor values. For instance, a typical headphone load exhibits resistive load like $16/32\Omega$ together with inductive and capacitive loads. Under the dc condition, the gain contributed by the output stage is even less than 1. Therefore, to ensure large enough open-loop gain of the amplifier, the number of stages needs careful consideration. For deep sub-micro CMOS process, with the shrink of channel length the transistors are becoming faster but with a penalty of smaller dc gain. A folded cascode structure is normally used for the input stage as it can extend the input CM range, the gain for a typical folded cascode stage is around 70 dB [37]. A two-stage topology results in only around 50 to 60 dB open-loop gain with the output stage considered. To boost up the open-loop gain more stages can be cascaded, however, increasing of stages does not necessarily extend the Gain Bandwidth (GBW) of the amplifier due to the Miller compensation. Thus a three-stage is usually the upper limit as further increase in the stage will bring on more trouble in compensating the amplifier [16]. In our realization of the amplifier, a three-stage topology is adopted. It consists of a input stage, a class AB biasing stage and two output stages. The amplifier is connected in closed-loop configuration with its gain defined by the resistor ratios. Serving as the output stage driver, the closed-loop gain of the amplifier is usually small, some design

even adopts a unity-gain feedback configuration [30]. In this design, the closed loop gain is set to be 2.

Unlike the conventional class AB amplifier design, the output stage supply of this amplifier is from the output of the buck converter. While for the two preceding stages, the battery voltage is used. Therefore, the structure of the class AB stage must be carefully design to cater to the different voltage domains used for the different stages. Having the largest current driving capability among all the stages, the output stage also occupies most of the area and consumes most of the quiescent power as well. Therefore, it is always beneficial to have a lower V_{DDL} for the quiescent power will be reduced proportionally. However, the large geometric ratios of the output stage make it difficult for a good control of the quiescent current. This poses the design challenge and limitations on the class AB amplifier.

Last but not least, the bandwidth of the CMFB loop must be carefully designed. In this case, the CMFB not only defines the dc operating point of the differential output node, it also serves as an additional input signal injection point where the input amplitude information is embedded into the output CM level. Thus to cope well with a audio frequency band signal, the bandwidth of the CMFB loop must be much larger than the upper boundary of the signal band and stability of this loop must also be ensured.

5.2.2 Input Stage

The input stage of the amplifier is realized using the folded cascode structure as shown in Fig 5.3. The benefit for using this structure is the extended input CM range so that the gain of the class AB driver can be reduced. Transistor M_1 and M_2 form the input differential pair which are the most critical ones in the amplifier design. For better matching, these two transistors are broken into even number of fingers and laid out using the common centroid layout technique to minimize the offset voltage. The size of the input transistors are enlarged for better $1/f$ noise suppression. The highest thermal noise contribution is from the bottom

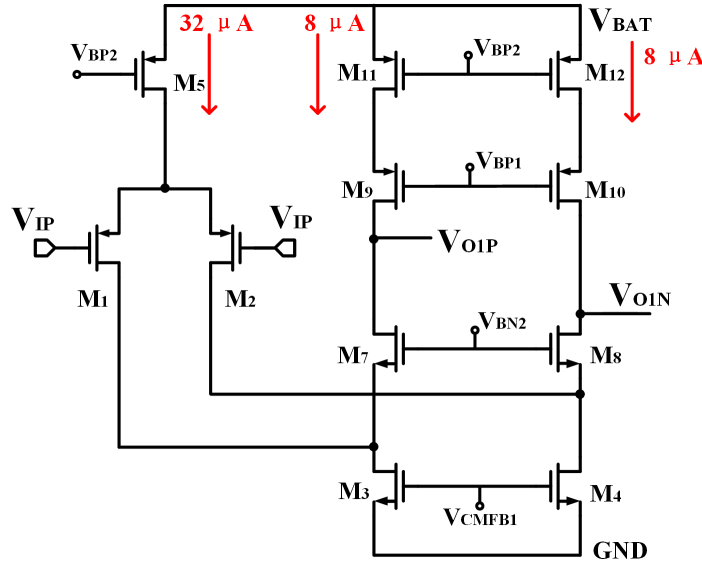


Figure 5.3: Transistor-level implementation of the input stage

NMOS current source pair M_3 and M_4 . Having the largest amount of current flowing which equals to the sum of the currents in the two upper branches, M_3 yields very large transconductance and hence outweighs the other transistors when calculating the input-referred noise. In order to minimize the ratio of g_{m3}/g_{m1} , the input transistor are designed wide to increase their transconductance for a fixed current consumption budget. For the same reason, M_3 and M_4 are designed very long to minimize the transconductance.

Additionally, the current distribution ratio are designed to be asymmetric in the M_5 and $M_{11/12}$ branch. For normal design, to ensure equal slew rate for different phases, it is usually a rule of thumb to design the current in M_1 and M_{11} to be the same. In our design, since the input audio signal does not exhibits fast changing rate like a step signal, the current ratio for M_1 to M_{11} is designed as 4:1. Thus the g_{m3}/g_{m1} ratio can be further reduced as now I_1 is now 80% of I_3 . The biasing voltages V_{BN1} , V_{BN2} , V_{BP1} and V_{BP2} are generated with a standard supply independent constant- g_m biasing circuit. Due to the fully differential structure, the CM voltage of the first stage output needs to be defined. This is done by a CMFB circuit which will be explained in detail later on. The sizing of each

Table 5.1: Transistor geometric ratios of the input stage (unit in μm)

Transistor Label	Finger count $\times$ (Width/Length)
$M_{1,2}$	$32 \times (7.5/0.6)$
M_5	$64 \times (1.5/1)$
$M_{11,12}$	$8 \times (1.5/1)$
$M_{9,10}$	$8 \times (1.5/1)$
$M_{1,2}$	$32 \times (7.5/0.6)$
$M_{7,8}$	$8 \times (2.4/1.4)$
$M_{3,4}$	$40 \times (0.6/3)$

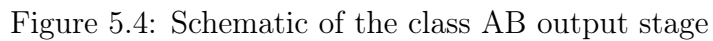
transistor of the first stage is shown in Table 5.1.

5.2.3 Class AB Output Stage

The second stage of the amplifier not only serve as an additional gain stage but also the biasing circuitry for the output power transistors. Thus although they are still two separated stages, they will be analyzed as a whole in this section. Based on the analysis of the class AB output stage in chapter 2 as well as the operation of class H topology in chapter 4, the desired properties of the class AB output stage can be summarized as below:

- (i) Low minimum operating supply voltage V_{DDL}
- (ii) Well controlled quiescent current I_Q
- (iii) High in-band (up to 20 kHz) gain

First, the minimum operating supply voltage is defined as the lowest value of V_{DDL} that is applicable without pushing all the pertinent transistors out of their correct operating region. For example, the minimum V_{DDL} for the topology in [13] equals to $2V_{GS} + V_{DSAT}$ due to the stacked diode-connected transistors. If this voltage is further reduced, the translinear loop which defines the quiescent current will be affected, at the same time the headroom voltage for the current source transistors will be reduced which jeopardize the gain of that



Based on the above analysis, the schematic of the class AB output stage is developed and depicted in Fig 5.4. The input signal is from the first stage output as in Fig 5.3. M_1 and M_2 forms an inverting stage with unity gain, thus with the subsequent inverting class AB biasing stage, the polarity of the second stage becomes non-inverting. Transistor M_{4-9} make up a differential pair which regulates the gate voltages of the power transistors M_P and M_N . Note that the input ac signal is actually injected as a CM voltage from the perspective of the differential pair, which satisfies the push-pull effect required by the class AB output stage. M_{10-14} form the circuitry that senses the minimum current flowing in the weakly conducting transistor, together with the differential pair a local feedback

Table 5.2: Transistor geometric ratios of the class AB output stage (unit in μm)

Transistor Label	Finger count $\times$ (Width/Length)
M_3	$4 \times (0.6/3)$
M_{10}	$4 \times (0.6/6)$
$M_{11,12,13}$	$4 \times (18/0.5)$
M_{14}	$2 \times (18/0.7)$
M_P	$600 \times (18/0.5)$
M_N	$300 \times (18/0.7)$

loop is constituted which compares and regulates the quiescent current with respect to the predefined reference current. With the feedback control mechanism [18], the quiescent current for different loading conditions is accurately defined. In this design, the scaling factor between the output power transistor $M_{P/N}$ to the sensing transistor $M_{11/14}$ is set to 150. The reference current is generated from the biasing circuitry and is designed to be $4 \mu\text{A}$, thus the expected quiescent current for each output stage is defined as $4 \mu\text{A} \cdot 150 = 600 \mu\text{A}$. The transistor geometric ratios for several key transistors are shown in Table 5.2.

The minimum operating voltage V_{DDL} of the output stage can be defined by the largest headroom voltage seen from each path from V_{SUP} to ground level. It is evident that this V_{DDL} is now constrained by the voltage swing at V_P instead of V_N due to the much higher supply voltage V_{BAT} applied to the second stage. The minimum V_{DDL} is hence defined by the path comprised of transistor M_P , M_5 and M_4 which equals to $V_{GS} + 2V_{DSAT}$. The V_{DSAT} here stands for the headroom voltages for $M_{4,5}$, further reduction of V_{DDL} will push these two transistors into triode region and the high-gain property of the second stage is ditched.

The adopted class AB biasing also demonstrate high gain for different loading conditions. For small ac input, the class AB biasing works as a cascode structure from the input to V_P and V_N , thus the gain of the second stage is in terms of $g_m r_o^2$. Thus the open-loop gain of the amplifier can easily reach more than 100 dB even with the gain of the output stage being much smaller than 1. Under large signal transient, the input signal is like CM voltage to both V_P and V_N . For the node which is supposed to drive the strongly conducting

power transistor, its connection to the local feedback loop will be cut off, resulting in high gain to provide large gain voltage swing. While for the node driving the weakly conducting transistor, the local feedback loop will fight against the input ac signal. thus the voltage at this node will not keep increasing/decreasing to completely switch off the power transistor. Instead it will be regulated to ensure that a certain amount of current is flowing in the weakly on power transistor. Besides, a second CMFB loop is adopted to boost up the response of the CMFB loop, the injection of this CM control signal is through the gate of M_9 which serves as the top current source. The trade-offs on selecting the current budget are also analyzed here. The quiescent current in the power transistor is mainly determined by the size of the device. If the device is too small, the overdrive voltage required during peak current sourcing or sinking will become large. On one hand, this will make the power transistor easily enters triode region when its headroom voltage is small. On the hand, the proceeding stage will also be stressed as the headroom for the bottom cascode structure shrinks. Both will jeopardize the linearity performance of the amplifier and results in a worse THD+N. Moreover, the ratio between the biasing branch to the power stage cannot be designed to small as large ratio will make the transistor matching to be more difficult. The biasing currents spent in each branch are highlighted in red as in Fig. 5.4.

5.2.4 Frequency Compensation and CMFB Circuitry

The class AB amplifier used in this design adopts a three-stage topology, thus the frequency compensation is to be discussed for a stable operation. Miller frequency compensation (MC) is a widely used compensation technique for two-stage operational amplifier and is also referred as the "pole splitting" technique [38]. It is also theoretically extendable to the application on multi-stage amplifier topologies. However, due to the gain and power trade-off, it is most extensively studied for the three-stage topology, and is usually referred as the Nested Miller Compensation (NMC) [39–41]. The NMC is usually criticized for its significant reduction on the GBW of the amplifier as well as the requirement for very large

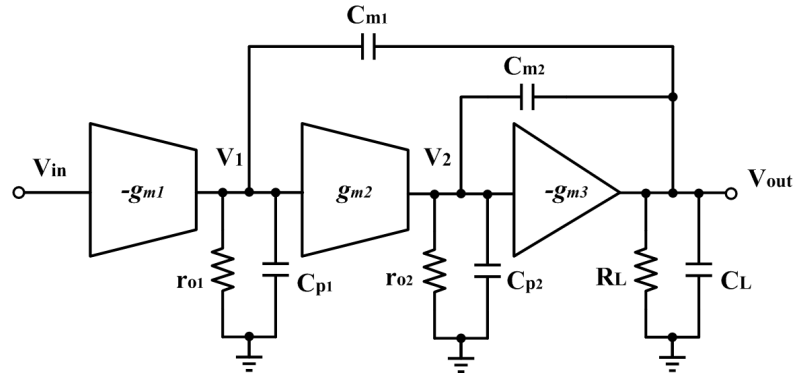


Figure 5.5: Topology of the three-stage NMC amplifier

transconductance g_m at the last stage [42]. It is also considered weak when driving large capacitive load up to few nF. Hence extensive research works have been done on the development of novel frequency compensation techniques for low power designs [43–46]. The design in [19] achieves driving a capacitive load up to 22 nF. However, in the author's point of view, the NMC is still competitive for audio amplifier design. First, the audio amplifier has an output stage with gigantic current driving capability, therefore the requirement of large output stage g_m can be easily met. Secondly, due to the large output stage g_m , the size of the frequency compensation capacitors as well as the maximum output capacitive load are both within the acceptable range. Hence it is arguable to apply complicated frequency compensation techniques to boost the capacitive load driving capability to a level that is impractical large. In this design, for less circuit complexity, the NMC technique is adopted for the three-stage class AB amplifier.

The topology of a typical three-stage NMC amplifier is depicted in Fig 5.5, where the r_{oi} and C_{pi} represent the output resistance and capacitance associated with the output of each stage. C_{m1} and C_{m2} are the two compensation capacitors. By applying KCL at different output nodes of the NMC small-signal circuit, the open-loop transfer function can be derived. For an audio power amplifier design, the following assumptions are valid. First, the output stage transconductance is much larger than its two preceding stages. Secondly,

the compensation capacitor as well as the load capacitor are much larger than the output capacitors in the intermediate stages. Thus the transfer function of a three-stage NMC amplifier can be expressed as follows:

$$A_{\text{NMC}}(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L(1 - s \cdot \frac{C_{m2}}{g_{m3}} - s^2 \cdot \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}})}{(1 + sC_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L)[1 + s \cdot \frac{C_{m2}(g_{m3}-g_{m2})}{g_{m2}g_{m3}} + s^2 \cdot \frac{C_{m2}C_L}{g_{m2}g_{m3}}]} \quad (5.1)$$

The transfer function can be divided into two parts, the first part is the dc gain times the dominant pole response which is the desired frequency response for a stable one-pole system. The second part is a biquadratic term having second order terms in both the numerator and denominator. The numerator describes the locations of the zeros. By noting that the negative coefficient of s^2 terms, we can conclude that there are one Left Half Plane (LHP) zero and one Right Half Plane (RHP) zero, and the RHP zero stays at lower frequency as the s term is also negative. In a two-stage MC amplifier, the existence of the RHP zero, which is due to the feedforward signal path through the Miller capacitor, degrades the Phase Margin (PM) and shall be eliminated by compensation techniques. However, this RHP zero effect is mitigated in a three-stage topology with a power output stage as the last stage. This is due to the large value of g_{mL} , as can be seen from the expression, the large g_{mL} leads to small coefficients of the second order term. Thus the feedforward effect of C_{m1} and C_{m2} only occurs at very high frequency. For the denominator side, both the s^2 and s term show positive coefficients. However, this is under the condition that $g_{mL} \gg g_{m1,2}$. If this condition is not met, the $(g_{mL} - g_{m2})$ of the s term in the denominator will reduce and hence reduces the damping factor of the second order function. Due to small damping ratio of the complex pole pairs, a drastic drop in phase plot and a peaking in gain plot can be observed which make the amplifier unstable. In summary, the large value of g_{mL} is required for a stable NMC three-stage amplifier. It is indeed a concern for normal low power amplifier designs, however, due to the power output stage this condition can be easily obtained for an audio

power amplifier. Therefore, the simple NMC scheme is adopted to avoid unnecessary circuit complexity. Based on the above assumptions, the transfer function of a NMC amplifier can be further rewritten as:

$$A_{\text{NMC}}(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L(1 - s \cdot \frac{C_{m2}}{g_{m3}} - s^2 \cdot \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}})}{(1 + sC_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L)(1 + s \cdot \frac{C_2}{g_{m2}g_{m3}R_L} + s^2 \cdot \frac{C_2C_L}{g_{m2}g_{m3}})} \quad (5.2)$$

C_2 in the above equation is a new definition from the conventional design. For conventional analysis [42], it is assumed that the Miller capacitors $C_{mi}(i = 1, 2, 3...)$ is much larger than the parasitic capacitance associated to the output node of each intermediate stage $C_{pi}(i = 1, 2, 3...)$. Plus the Miller effect, the equivalent capacitance due to C_{mi} seen at the input is much larger than these junction capacitances. Thus C_{pi} is usually neglected during the derivation. However, in the case of an audio power amplifier, the expression will be a little different. First, as mentioned before due to the small resistive load at the output stage, the gain of the last stage is much smaller than 1. The Miller effect which boost the equivalent capacitance is no longer valid under quiescent state. Secondly, the power transistors are designed with huge geometric ratios which results in large junction capacitance. For instance, the power PMOS used at the output stage shows a junction capacitance of around 40 pF under quiescent state. Combining these two factors we can find that the equivalent capacitance C_2 seen at the second stage output is no longer dominated by the value of C_{m2} which is usually in the term of few pF. Instead it is the sum of all sorts of capacitances seen at that node. In order to control the time constant of that node, the value of C_{m2} must be increased to a few 10s of pF to show significantly its effect. Thus the analysis of stability will slightly differ from the conventional analysis of a three-stage NMC amplifier.

Due to large value of g_{m3} , the effects of zeros in the numerator only occur in relatively high frequency and can be ignored. Hence the stability criteria simply relies on the second order term in the denominator of equation (5.2) which determines the locations of the two

non-dominant poles. The roots for the quadratic term can be found by equating it to 0:

$$1 + s \cdot \frac{C_{m2}}{g_{m2}g_{m3}R_L} + s^2 \cdot \frac{C_{m2}C_L}{g_{m2}g_{m3}} = 0$$

$$\text{Hence, } s = -\frac{1}{2C_L R_L} \pm \frac{1}{2C_L R_L} \sqrt{1 - \frac{4g_{m2}/C_2}{1/(g_{m3}R_L^2 C_L)}} \quad (5.3)$$

The condition that the load capacitor C_L is much greater than the parasitic capacitance C_2 is no longer valid as aforementioned. Thus its effect cannot be neglected any more. It is easy to find that the term under the square root function in equation (5.3) is always positive, thus the expression introduces two real poles on the LHP. The pole at higher frequency is very close to $1/(2\pi R_L C_L)$ which is indeed the pole at the output stage, while the lower frequency pole is dependent on the values of g_{m2} , g_{m3} and C_2 .

For this design the gains generated from the first two stages are approximately 82 dB, and 63 dB respectively. g_{m3} of the last stage is designed to be 8.35 mA/V, resulting in a gain of -17.5 dB under quiescent state. The three-stage topology exhibits a dc open-loop gain of 127 dB. Suppose the compensated gain plot of the amplifier behaves like a first-order system, and the GBW of the amplifier is selected to be one decade before the frequency of the output pole, the dominant pole frequency is determined as around 2.2 Hz. The compensation capacitor C_{m1} is calculated to be around 1 pF. Thus the expressions of the poles and zeros for the NMC compensated three-stage class AB amplifier is summarised in Table 5.3. By substituting the real numbers into the expressions, the frequencies for each pole and zero can be calculated as shown below:

It can be observed from the table that due to the large parasitic capacitance at the second stage output, a LHP pole p_2 exists well within the GBW. As a result, an additional 90° of phase drop is added and the PM of the amplifier is reduced. The output pole is not a big issue as it locates well beyond the GBW. The pair of zeros with one locate at RHP and one at LHP move around the value of $g_{m2}/2C_{m1}$ which is also not a big concern. To stabilize

Table 5.3: Pole and zero expressions and locations in frequency scale for the NMC compensated amplifier

Poles/Zeros	Frequency
$P_{-3dB} = -\frac{1}{g_{m2}g_{m3}r_{o2}R_L C_{m1}r_{o1}}$	-2.2 Hz
$P_2 = -\frac{1}{2C_L R_L} + \frac{1}{2C_L R_L} \sqrt{1 - \frac{4g_{m2}/C_2}{1/(g_{m3}R_L^2 C_L)}}$	-94.27 kHz
$P_3 = -\frac{1}{2C_L R_L} - \frac{1}{2C_L R_L} \sqrt{1 - \frac{4g_{m2}/C_2}{1/(g_{m3}R_L^2 C_L)}}$	-49.74 MHz
$Z_1 = -\frac{g_{m2}}{2C_{m1}} + \frac{g_{m2}}{2C_{m1}} \sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_2}}$	+19.6 MHz
$Z_2 = -\frac{g_{m2}}{2C_{m1}} - \frac{g_{m2}}{2C_{m1}} \sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_2}}$	-47.76 MHz

the amplifier the effect of the first non-dominant pole p_2 must be eliminated. This can be done by either pushing the pole to a higher frequency beyond the GBW or by introducing an LHP zero that realize a pole-zero cancellation. For the first method, we noticed that in the expression of p_2 , the closer the term inside the square root function is to 1, the smaller the pole frequency will be. Thus pushing this pole to a higher frequency by means of either increasing g_{m2} , g_{m3} , R_L and C_L or through reducing C_2 . R_L and C_L are fixed value external components, increasing g_{m3} will increase the quiescent power of the output stage as well as the size of the power transistors. C_2 is also dominated by the size of the power transistor. The only doable method is by increasing g_{m2} , however, its effect is still limited as in order to push this pole output GBW the value of g_{m2} has to be increased to be even larger than g_{m3} which is totally unreasonable. Thus the only feasible approach is by introducing a LHP zero to realize the pole-zero cancellation.

Recall the design of a two-stage amplifier, a nulling resistor is used to block the feed-forward path and push the RHP zero to the LHP. Similar concept can be applied to a three-stage topology to create a LHP zero. In a three-stage power amplifier, due to the gain from the second stage as well as the large transconductance at the output stage, this RHP

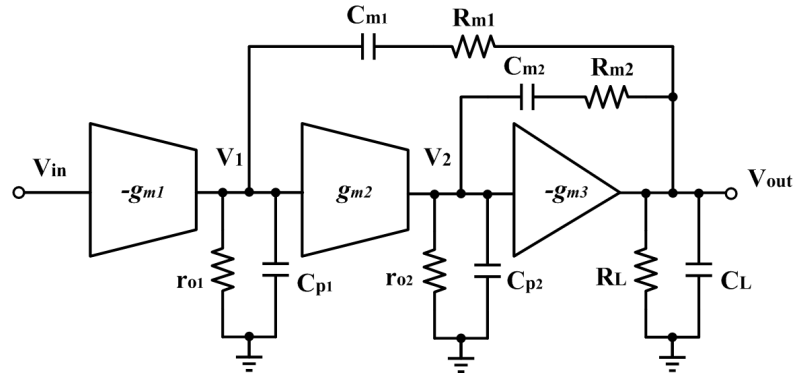


Figure 5.6: Schematic of the class AB output stage

zero due to feedforward from the compensation capacitor is pushed beyond the frequency of interest. However, this zero can still be controlled by the value of the nulling resistor and used to improve the phase margin. The block diagram of the Nested Miller Compensation with Nulling Resistor (NMCNR) is depicted in Fig. 5.6. The transfer function of the amplifier with NMCNR compensation scheme is derived as below:

$$A_{\text{NMCNR}}(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L[1 + s \cdot (R_{m1}C_{m1} + R_{m2}C_{m2}) + s^2 \cdot (R_{m1}C_{m1}R_{m2}C_{m2})]}{(1 + sC_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L)(1 + s \cdot \frac{C_2}{g_{m2}g_{m3}R_L} + s^2 \cdot \frac{C_2C_L}{g_{m2}g_{m3}})} \quad (5.4)$$

As shown in equation (5.4), a LHP zero at the frequency of $1/(C_{m1}R_{m1})$ is created. In order for a pole-zero cancellation the frequency of this z_1 should be designed to the proxy of p_2 which is around 100 kHz. The frequency of the pole and zero does not have to be exactly the same as they are meant for frequency compensation purpose, in fact it is advantageous to design the zero frequency slightly higher than the pole that it needs to match. By doing so, the gain plot of the amplifier will drop with a slope even steeper than 20 dB/decade after reaching the pole frequency. Thus the gain crossing point will be pushed to a lower frequency, it lowers the risk that the PM of the system to be jeopardized by higher frequency poles or RHP zeros and also increases the Gain Margin (GM). At the same time, the gain

for the frequency of interest (audio frequency band) is not affected and the introduced LHP zero will push the PM back to ensure stability of the system. For this reason, the introduced LHP zero is placed at 4 times the frequency of p_2 which is about 400 kHz. Thus the value of the nulling resistor can be acquired as around 400 k Ω . The realization of this resistor is by using the p-type poly resistors available in this process. According to the technology specification, the tolerance of the sheet resistance values for three resistor options are $\pm 8\%$, $\pm 15\%$ and $\pm 20\%$ respectively, while the value of the sheet resistance is too small for the $\pm 8\%$ high accuracy resistor. Thus considering both the resistor variation and occupied area, the resistor with moderate tolerance and sheet resistance value is selected. Since the value of the nulling resistor is critical to the effect of pole-zero cancellation and hence directly dictates the stability of the amplifier. Its variations to different process corners must be taken into account. Consider a tolerance of $\pm 20\%$ for the resistor value, stability simulations of the amplifier are carried out for nulling resistor ranging from 320 k Ω to 480 k Ω . The results are illustrated with Bode plots as in Fig 5.7.

It can be observed from the figure that for different values of nulling resistors, the locations of the introduced LHP zero moves accordingly. As the main purpose of this zero is to push back the PM, the exact pole-zero cancellation is not necessary. The mismatch causes a trench in the phase plot as in Fig 5.7, and it is soon recovered by the effect of LHP zero. PM of more than 75° can be achieved considering the worst corners of the passive component used. PM of the amplifier with different nulling resistors are shown in Fig 5.8. The GBW of the amplifier increases almost linearly as the increase of the nulling resistor, this is because the smaller the nulling resistor the higher the zero frequency will be and hence the gain will drop more quickly during the "trench region". Thus the gain crossing point occurs earlier which is indeed the GBW. As can be extrapolated from the Bode plots in Fig 5.7, the GBW value does not have a critical effect on the gain of the amplifier within the audio frequency range which is vastly determined by the dc gain and the dominant pole

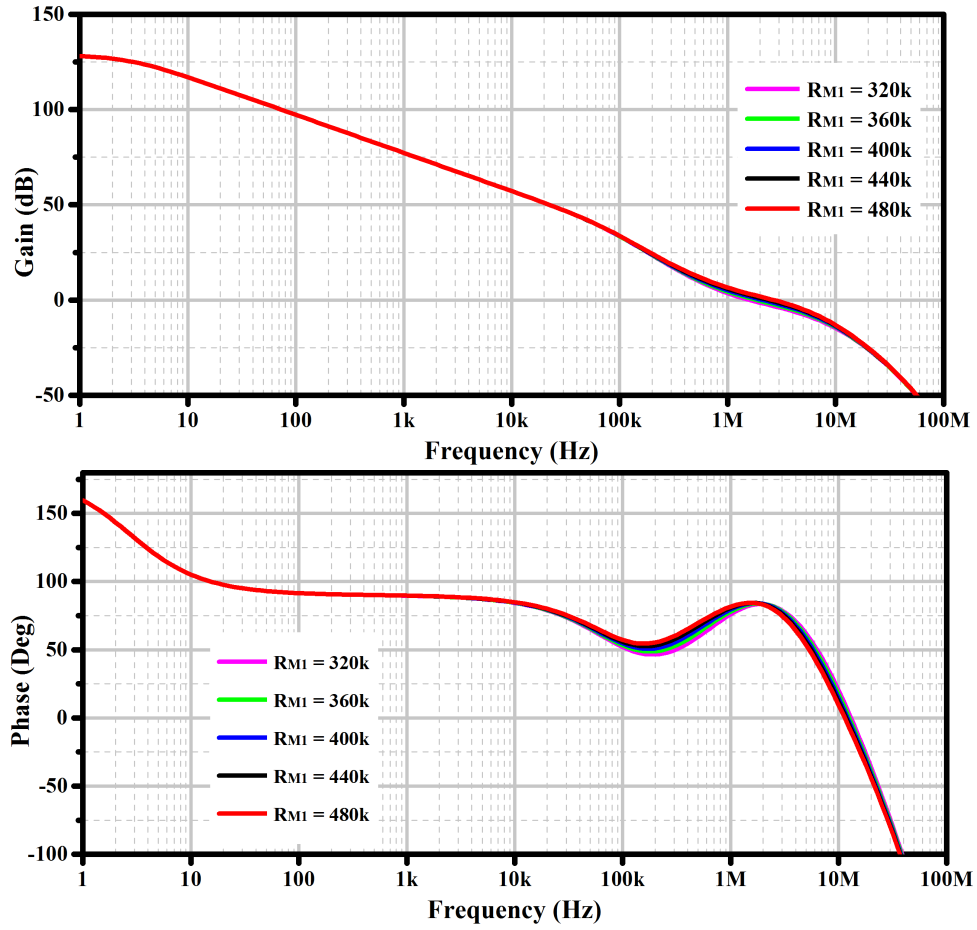


Figure 5.7: Simulated open-loop frequency response of the amplifier with different nulling resistors

frequency. Thus larger GBW does not necessarily mean a better design, on the contrary, it increases the risk that the amplifier's PM is degraded by the high frequency poles and zeros.

The effect of load capacitance variation on stability is also examined. As the load capacitor increases, the pole at the output stage gradually shifts towards lower frequency. Therefore, the PM of the amplifier will be degraded. Fig 5.9 plots the impact of load capacitor on PM and GBW. The designed three-stage amplifier is capable of driving a 2 nF load capacitor with a PM of greater than 60° . Values of the components used in the compensation network are listed in Table 5.4, label of each component can be referred as in Fig 5.2 and Fig 5.5.

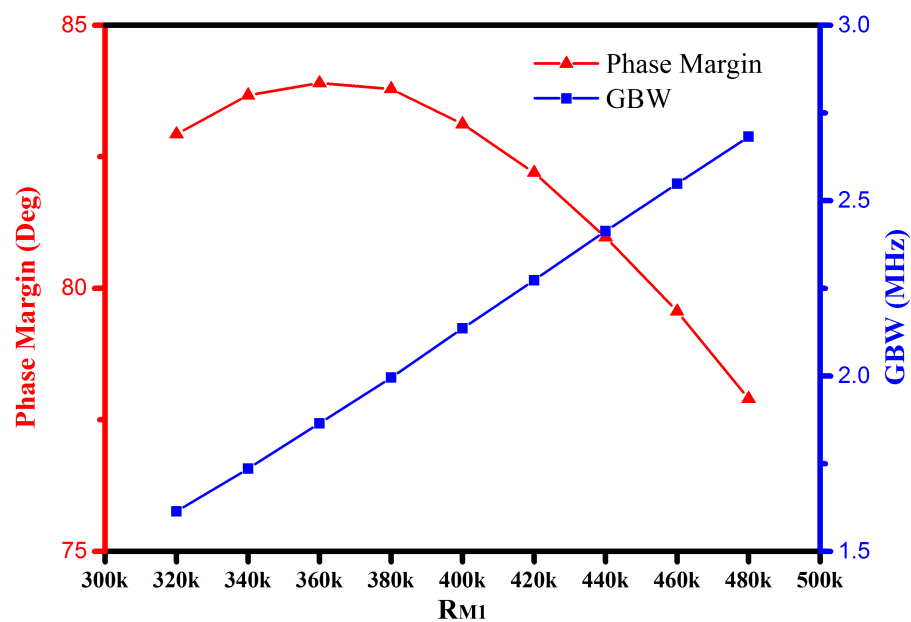


Figure 5.8: Phase margin and gain bandwidth product of the amplifier for different nulling resistors

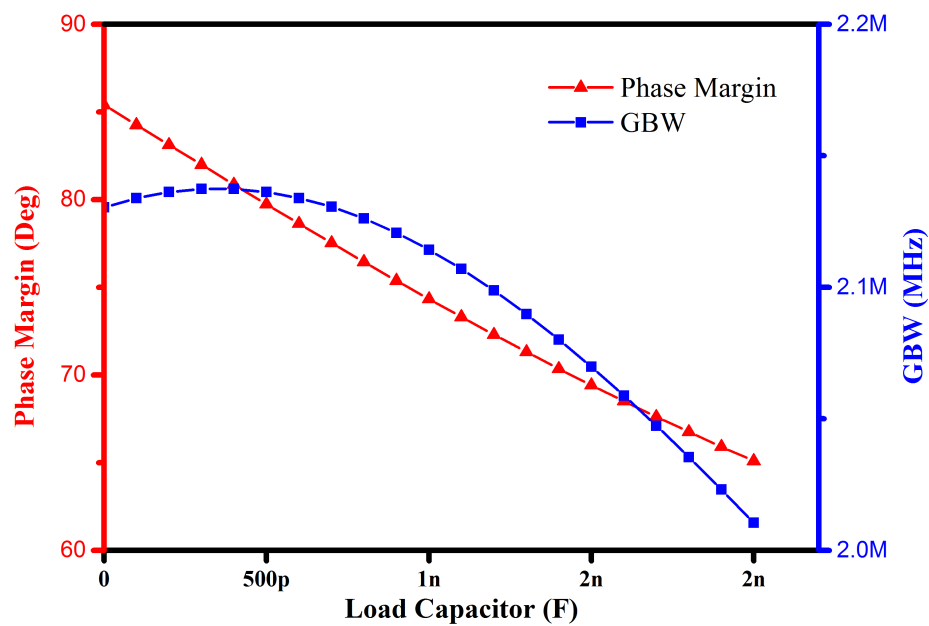


Figure 5.9: Phase margin and gain bandwidth product of the amplifier for different load capacitance

Table 5.4: Component values of the feedback network

Component Label	Value
C_{m1}	1 pF
C_{m2}	10 pF
R_{m1}	400 k Ω
R_{m2}	1.5 k Ω
R_1	32 k Ω
R_2	64 k Ω

In addition to the analysis of the amplifier's differential mode stability, the CMFB of this fully-differential amplifier also needs to be designed carefully. The operation of the proposed class H operation is achieved by modulating the output stage CM voltage level, hence a stable CMFB loop with fast transient response is required. As aforementioned, the class AB amplifier consists of three stages. If a global CMFB loop is applied across all the three stages, it would be difficult to obtain high bandwidth due to the cascaded stages. Moreover, the high frequency poles and zeros which reside along the signal path will make it hard for frequency compensation. Therefore, for this design in order to achieve a relatively simple structure of the CMFB loop, we break the long global CMFB loop into two short local CMFB loops. The first loop will sense the output voltages of the first stage and feed the control signal back as the gate voltage of the bottom current source transistors. The second CMFB loop will sense the output voltages of the power stage and regulate it with respect to the reference level generated from the IAD block. Thus the design considerations for these two CMFB loops are completely different.

Fig 5.10 depicts the schematics of the two CMFB amplifiers. The input CMFB amplifier senses the output CM level through two differential pairs [38], the four transistors in the differential pairs are well matched. The amplifier will output a voltage that is proportional to the difference of the output CM voltage and the reference voltage. The advantage of this structure is its high input impedance as the CM sensing process is done by the differential pair, thus its loading effect to the preceding output node is negligible. However, the CM sensing function is only effective when the CM differences ($V_{1P}-V_{REF}$ and $V_{1N}-V_{REF}$) are

small enough to apply the small-signal analysis. Therefore, the output nodes should not deviate from the expected CM voltage level too much even during large-signal transient. These properties of the structure make it perfectly applicable to be used as the input CMFB amplifier. First, the input stage is supposed to provide high gain to the three-stage topology. For normal approach where two resistors are used for CM voltage sensing, extremely large resistors must be used which increases the chip area. By using this structure high gain of the first stage is preserved. Secondly, due to the gain provided by the last two stages, the movements of the first stage output nodes are very small which satisfies the operation conditions required by this structure. The reference voltage is set to be 1.2 V which is the same as the lower supply voltage V_{DDL} . The Bode plot of the first CMFB loop is plotted as in Fig 5.11, due to the existence of the LHP zero at relatively high frequency, a compensation capacitor C_c of 5 pF is added along the CMFB path to stabilize the loop. The first stage CMFB achieves a GBW of 3.72 MHz and a PM of 75° .

The CMFB used for the power stage is a conventional structure based on a pair of resistors. The two output voltages are sensed and averaged to get the output CM level and is then compared with the desired V_{OCM} coming from the IAD block. Due to the small

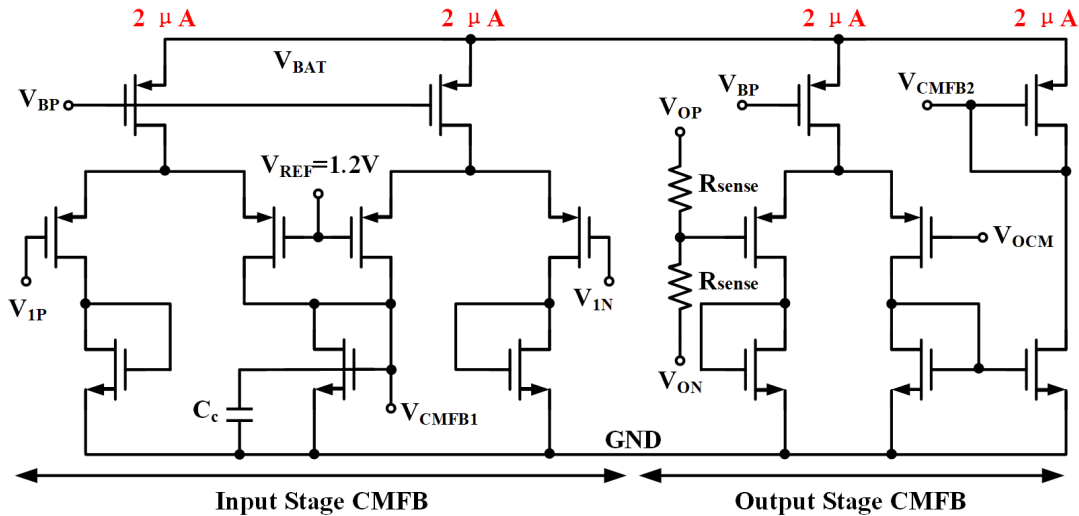


Figure 5.10: Schematics of the two local CMFB amplifiers

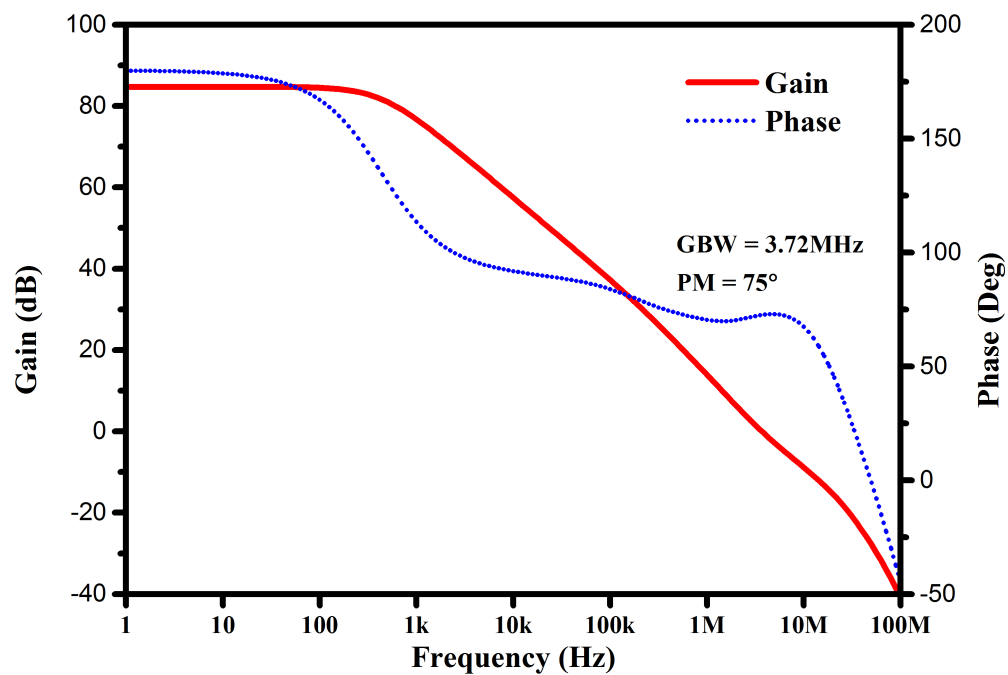


Figure 5.11: Frequency response of the first CMFB loop

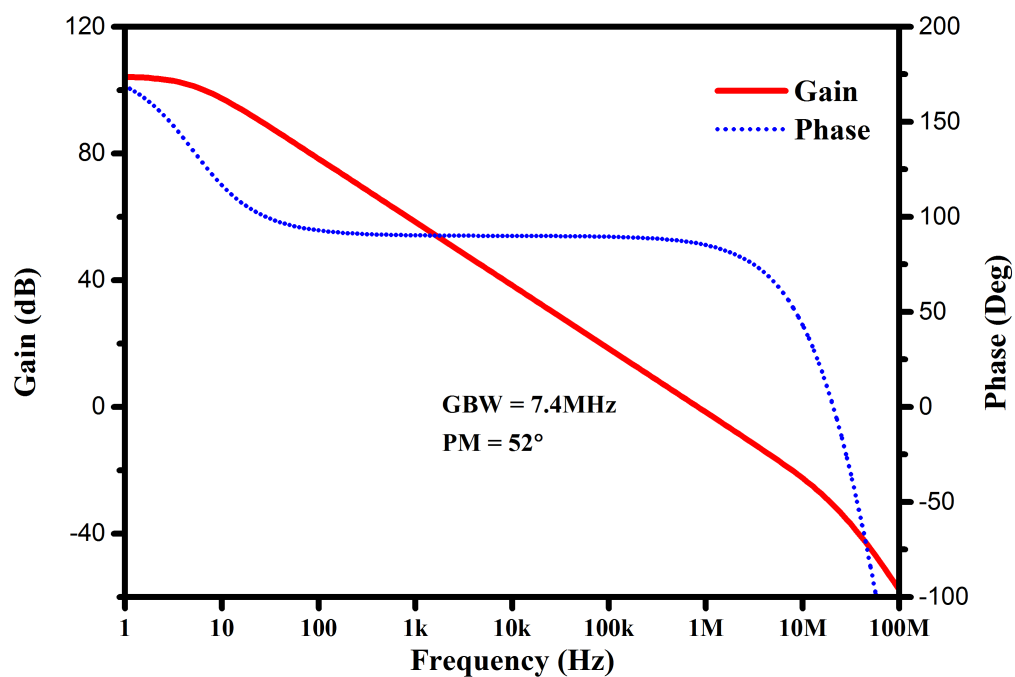


Figure 5.12: Frequency response of the second CMFB loop

resistive load at the output, the gain requirement of the output stage is relaxed thus the sensing resistors can be designed relatively small. However, the two output nodes have large output swings during signal transient which excludes the possibility of using differential pair based CM sensing structure. The frequency response of the second CMFB loop is plotted as in Fig 5.12. It achieves a GBW of 7.4 MHz which is much faster than the varying reference signal.

5.3 Input Amplitude Detection (IAD) Block

The Input Amplitude Detection (IAD) block senses the amplitude of the input signal and determines the operation mode accordingly. The processing of input signal is illustrated as shown in Fig 5.13. The balanced audio input signal denoted as V_{IN+} and V_{IN-} are fed into the IAD block. These two signals are 180° out of phase and is dc biased at the input CM voltage level V_{ICM} . This CM level may be different from the operating levels used for

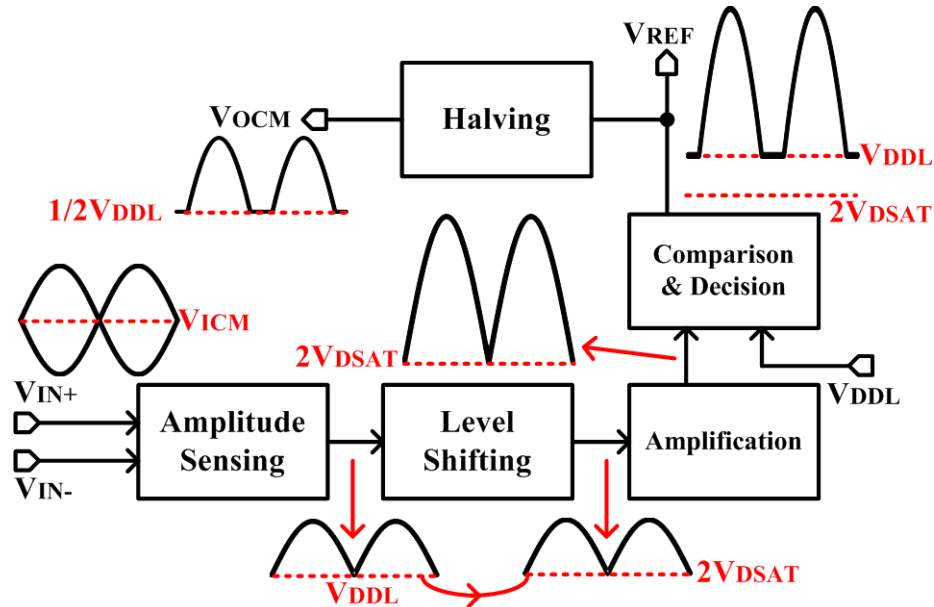


Figure 5.13: Signal flow diagram of the proposed IAD block

the following circuitry as the audio signals are normally coming from a preamplifier stage or an audio DAC. Thus a dc decoupling process must be included for the amplitude sensing stage. The amplitude of the balanced input signal can be obtained by passing them through a rectifier circuit which preserves only the positive half of the signals. For the following stages, the acquired ac amplitude is going to be compared with the reference voltage to determines the operation mode of the system. Recapitulate from Chapter 4, the transition from class AB mode to class H mode happens when one output node reaches within one V_{DSAT} from the low voltage supply V_{DDL} . Refer back to Table 4.1, this situation can be described as:

$$V_{\text{DDL}} = V_{\text{out}} + 2V_{\text{DSAT}} = A_{\text{coarse}} \cdot |V_{\text{in}}| + 2V_{\text{DSAT}} \quad (5.5)$$

Therefore the purpose of the following stages in the IAD block is to construct a voltage level that is equal to $A_{\text{coarse}} \cdot |V_{\text{in}}| + 2V_{\text{DSAT}}$, compares it with V_{DDL} and determines the mode of operation. By observing the above expression, it can be treated as it comprises of two parts, the ac and dc portion. We define the dc bias level as $V_{\text{OFFSET}} = 2V_{\text{DSAT}}$, thus the next stage will perform a dc level shift from V_{DDL} to V_{OFFSET} . In order to match the gain in IAD block with that of the fine gain path, an additional amplifier stage is cascaded to provide the coarse gain A_{coarse} . Then the constructed waveform will be compared with V_{DDL} and the one with higher value will be set as the reference voltage V_{REF} to the buck converter. So for class AB mode the supply stays at V_{DDL} , while for class H mode the instant supply equals to $A_{\text{coarse}} \cdot |V_{\text{in}}| + 2V_{\text{DSAT}}$ which is always one V_{DSAT} above the output voltage. For the last stage, V_{REF} is halved to get the corresponding output CM level for the class AB amplifier V_{OCM} .

The circuit-level realization of the IAD block is depicted in Fig 5.14. A differential amplifier OPAMP1 is deployed to serve as the input unity-gain buffer , together with the dc decoupling capacitor, the input ac signals are buffered and dc biased at $V_{\text{DDL}} = 1.2\text{V}$.

Selection of this CM level is based on the consideration of maximum input amplitude. The buck converter is supposed to output a maximum supply voltage of 3 V with 3.3 V input, with a predefined V_{DSAT} of 0.2 V, the maximum amplitude of output swing can reach 2.6 V. If the closed loop gain is set to 2, the maximum amplitude each single input node will be 650 mV. Therefore, using V_{DDL} as the output CM biasing for OPAMP1 satisfies the output swing requirement and avoid introducing another dc biasing level at the same time. Next the buffered ac signals are fed into the rectifier circuit which consists of a comparator COMP1 and a pair of transmission gates. The COMP1 compares the two signal values and passes the one whichever is higher. Due to the large swing of the input signals, transmission gates are used as switches for a relatively constant on resistance. At the output of this stage, the absolute value of input ac plus V_{DDL} will be sent to the level shifter. As the value of V_{OFFSET} is 0.4 V, it is not feasible to combine this level shifting function with the amplitude sensing stage. Thus a separate amplifier OPAMP2 as well as the resistor network are needed to perform the function of dc level shifting. The previous dc bias V_{DDL} is removed and the output is biased to V_{OFFSET} for the latter comparison.

The coarse gain is set by the amplification stage comprising of OPAMP2 and feedback resistors. The ratio of $R_4:R_3$ is set to 3 which gives a non-inverting gain of 4 at this stage. Due to the halving effect at the last stage, the gain from input all the way to V_{OCM} is 2 which is equalized to the fine gain path. The matching of the resistors are not critical as any slight gain mismatch between the fine gain path and the coarse gain path will have minuscule effect to the differential output. By far the desired voltage expression is obtained and the last stage is aimed to compare this input-dependent waveform with V_{DDL} . The concept of the comparison circuitry is similar to the rectifier, it compares and passes through the signal whichever is higher. At the same time, the comparison result is used as a digital signal *Mode_Select* which signifies the operation mode. At last, the reference voltage is buffered and halved to get the correct output CM level for the fully-differential class AB amplifier.

The IAD block is simulated with sine wave input signals, the transient results for input

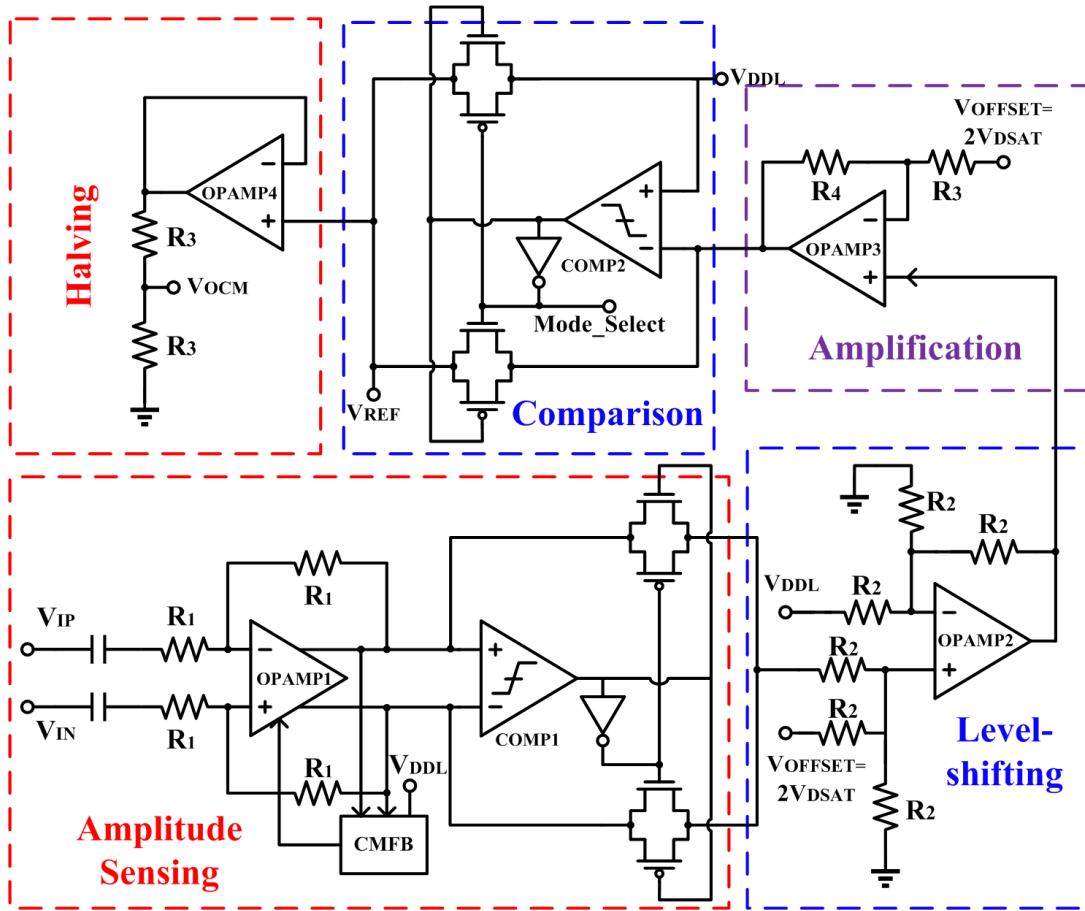


Figure 5.14: Realization of the IAD block

frequency of 1 kHz and 20 kHz are plotted in Fig 5.15. As expected the V_{REF} signal stays at 1.2 V for class AB mode operation and become load adaptive when the threshold is reached. For input signals with amplitude of 650 mV, V_{REF} achieves its maximum of 3 V. However, due to the different signal processing stages as in Fig 5.14, the ac signal within the final V_{OCM} shows some latency with respect to the original inputs. In the proposed system the input ac signals are simultaneously fed into the IAD block as well as the class AB amplifier. The delay seen from the class AB side is negligible which makes the latency in the IAD block an issue as analyzed in Chapter 4. For 1 kHz signal, the delay between input and V_{OCM} is around $1\mu s$, thus the sine wave portion of V_{OCM} waveform exhibits a phase delay of 0.36° . For 20 kHz signal, the delay reduces to 490 ns, whereas due to the increased frequency this

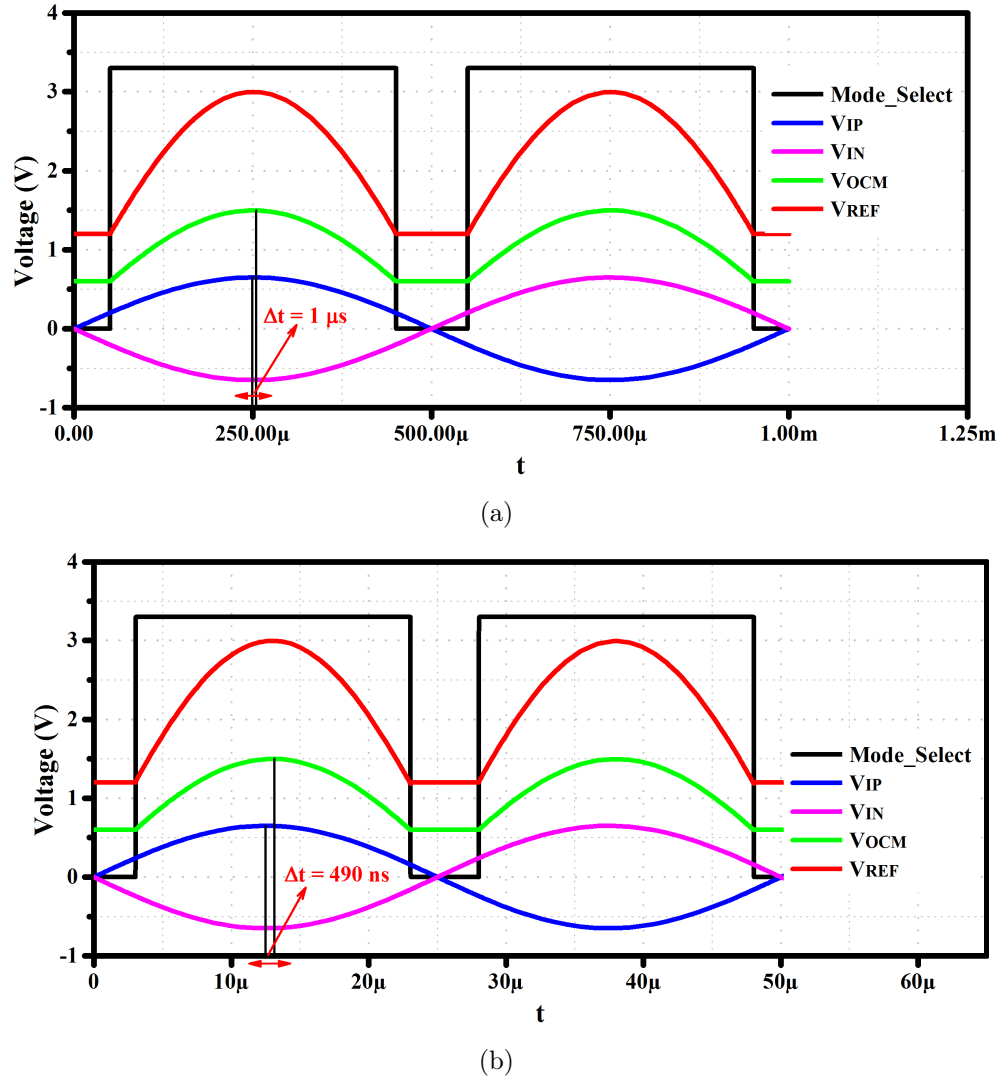


Figure 5.15: Transient simulation results of the IAD block with different input signal frequencies (a) 1 kHz, (b) 20 kHz

phase difference increases to 3.6° . In summary there exist both gain mismatch as well as phase mismatch between the fine gain path and the coarse gain path. The adverse effect caused by this phase mismatch is that the headroom voltage V_{DSAT} will be squeezed or enlarged a bit. However, slight mismatch between the two gain paths is still acceptable as the ac gain in the V_{OCM} will eventually cancel out at the differential output stage. Due to the high-gain linear feedback loop applied, the linearity is not sacrificed much.

5.4 Reference-Tracking DC-DC Buck Converter

5.4.1 Overview and Specifications of Buck Converter

The last and also the core part of the class H amplifier is the reference-tracking dc-dc converter. As mentioned in the previous section, the delay between the input signal and the input-dependent power supply play important roles in the transient operation. If the delay is too large, the class AB is at the risk of clipping the output waveform. Apart from this delay, a more crucial factor is the response time the dc-dc converter takes in order to track the reference signal. Since the reference signal is already lagging the realtime input signal, further delay at the converter output becomes unfavorable to the system. Thus the desired dc-dc converter should features very fast reference tracking capability. Secondly, the dc-dc converter serves as the power supply unit to the linear amplifier. Hence its efficiency will be directly linked to the efficiency of the system. Since the audio signal has a large PAR ratio, the current requested by the class AB amplifier varies continuously and stays a relatively low level for most of the time. This makes the design requirement of this buck converter different from the conventional designs. In this design, the power efficiency particularly at light load should be optimized. Last but not least, a more advanced control algorithm is required since the load condition of the class AB amplifier can be predicted and thus the converter's control scheme can be selected in advance.

The basic specifications of this buck converter is shown in Table 5.5. The proposed class H amplifier demonstrates directly battery hookup, thus the input voltage range of the

Table 5.5: Basic specifications of the buck converter

Input Voltage	3.3V - 4.2V
Output Voltage	1.2V - 3 V
Loop Bandwidth	$\geq 200\text{kHz}$
Switching Frequency	2 MHz
Peak Load Current	$>162.5\text{ mA}$

buck converter is indeed the operating range of the Li-ion battery. The output voltage range is from 1.2 V-3 V. The lower boundary is defined by the minimum operating voltage of the class AB output stage while the upper boundary is defined by the maximum duty cycle a PWM converter can achieve. The converter is supposed to adjust its output according to the reference voltage which is within the audio frequency range (up to 20 kHz), thus the bandwidth of the feedback loop should be much larger than the audio frequency. For this reason it is set to be at least 200 kHz. To ease the design of the compensator, the switching frequency of the converter is set to 10 times of the loop bandwidth. The maximum load current is defined by the class AB output swing. For a maximum differential output swing of 2.6V, the peak load current demanded by the amplifier is $2.6 \text{ V}/16 \Omega = 162.5 \text{ mA}$.

For the selection of the control schemes, hysteretic control has becoming very popular in recent years for its inherent fast loop response [47–52]. However, the switching frequency of the hysteretic converter is dependent on several design parameters such as the input and output voltages, load current, hysteresis window and so forth. The variable switching frequency results in difficulty in designing the input filter for Electromagnetic Interference (EMI) suppression, thus several reported works focused on the development of fixed frequency hysteretic controller assisted by a Frequency Locked Loop (FLL) [53–56]. However, the addition of the FLL greatly increases the design complexity of the converter and it is more appealing in the applications of fast load transient converters and high switching frequency converters. For our specific application, extreme fast load transient response is not required. Instead a robust design with fast reference-tracking capability is preferred, hence PWM-based fixed frequency converter becomes more suitable for this application.

For PWM-based control schemes, they can be classified into voltage-mode control (VM-C) and current-mode control (CMC). The difference between these two schemes is just that in VMC the output voltage is the only signal used for feedback while in CMC the inductor current is also sensed and used as control signal for the feedback network. As a result, the output LC filter reduces to a first order system in CMC while it remains as second order

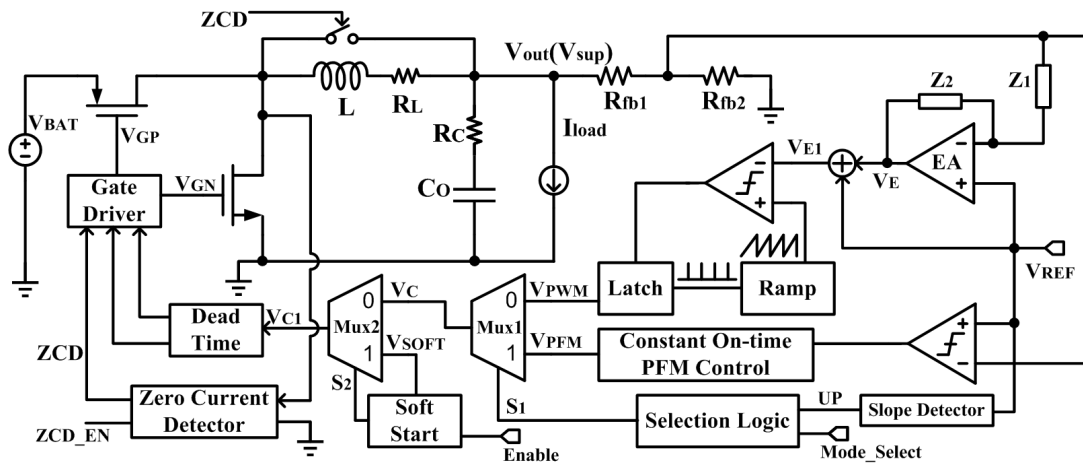


Figure 5.16: Architecture of the proposed voltage-mode control buck converter

system in VMC. Hence the compensator design in CMC becomes simpler and the loop bandwidth can be extended compared to VMC. However, the CMC design involves an accurate current sensor which senses the inductor current and use it as the ramp signal as in a VMC scheme. The realization of this current sensor poses design challenges on the robustness of the converter, which is quite sensitive to the transistor layout and PCB layout design. Thus its robustness as well as reliability is at risk. Based on the above consideration, the VMC PWM-based control is used for the design of the reference-tracking buck converter.

The architecture of the proposed dc-dc buck converter is depicted in Fig 5.16. The basic voltage-mode PWM feedback loop consists of a resistive divider, a error amplifier (EA) with compensation network, a comparator, a latch, a clock generator, a dead-time controller and gate drivers. The rest of the building blocks are meant for some specific functions which optimize the converter's performances, like zero current detection (ZCD), Dual-mode operation and so on. The details of these blocks will be delineated in the following sections.

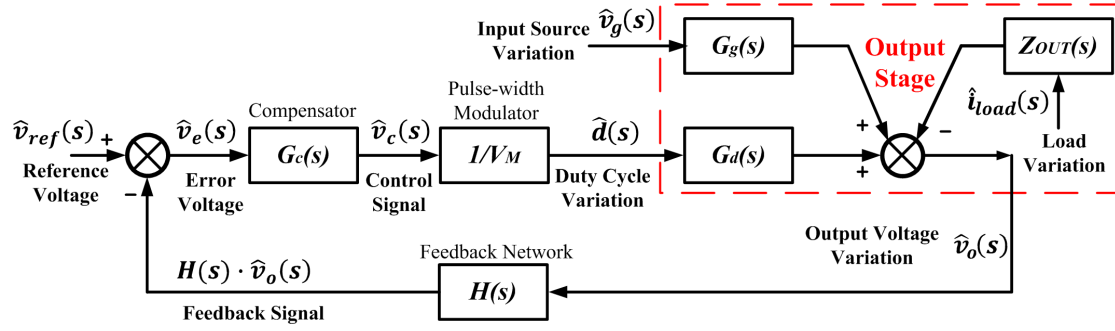


Figure 5.17: Small-signal flow diagram of a voltage-mode buck converter

5.4.2 Loop Stability Analysis of a Voltage-mode Reference-tracking Buck Converter

For most of the voltage regulators, feedback is applied to ensure the output voltage is at the desired level. Thus the stability condition of the feedback system must be analyzed. To study the stability conditions, an equivalent ac small-signal model is hence required. Different from a typical linear mode regulator like LDO, the switching mode regulators have its power output stages constantly switched on and off for power transferring purposes, resulting in a discontinuous nonlinear system. Thus certain modelling techniques are needed to average and linearize the switched system. A couple of converter ac modelling techniques have been reported in the literature [57–63]. The detailed derivation of two different approaches, the state-space averaging and linearization as well as the averaged switch modelling will be discussed in the Appendix A. Although they are expressed in different formats, the results achieved are similar. Refer back to Fig 5.16, the control-to-output transfer function can be expressed as:

$$G_d(s) = V_g \frac{1 + s/\omega_{esr}}{1 + s(R_C C_O) + s^2(1 + \frac{R_C}{R_{fb1} + R_{fb2}})LC} \quad (5.6)$$

The small signal model of a typical VMC buck converter is depicted in Fig 5.17. The feedback loop is constructed by the feedback network, the compensator, the pulse-width

modulator and the output stage. The loop gain is hence the multiplication of the transfer functions along the loop which can be expressed as:

$$T(s) = H(s) \cdot \frac{1}{V_M} G_c(s) G_d(s) \quad (5.7)$$

With proper approximation and linearization techniques, the small signal model of the buck converter now can be treated as a linear system. Thus the superposition principle can be applied to obtain the transfer function of the output with respect to all the small signal disturbances. The output voltage has the expression as follows:

$$\begin{aligned} \hat{v}_o(s) &= \frac{G_c(s)G_d(s)/V_M}{H(s) + H(s)G_c(s)G_d(s)/V_M} \hat{v}_{\text{ref}}(s) + \frac{G_g(s)}{H(s) + H(s)G_c(s)G_d(s)/V_M} \hat{v}_g(s) \\ &\quad - \frac{Z_{\text{out}}(s)}{H(s) + H(s)G_c(s)G_d(s)/V_M} \hat{i}_{\text{load}}(s) \\ &= \frac{1}{H(s)} \cdot \frac{T(s)}{1 + T(s)} \cdot \hat{v}_{\text{ref}}(s) + \frac{G_g(s)}{1 + T(s)} \cdot \hat{v}_g(s) - \frac{Z_{\text{out}}(s)}{1 + T(s)} \cdot \hat{i}_{\text{load}}(s) \end{aligned} \quad (5.8)$$

The three small signal disturbances injected into the system are coming from the load $\hat{i}_{\text{load}}(s)$, the source $\hat{v}_g(s)$ and the reference voltage $\hat{v}_{\text{ref}}(s)$ respectively. Unlike a normal buck converter where the reference voltage is simply a dc voltage, the reference voltage for a reference-tracking dc-dc converter also contains ac signal. Thus its effect to the system must also be analyzed. As can be observed from the above equation, for low frequency region where the loop gain $T(s)$ is very large in magnitude, the expression indicates that the high-gain feedback loop suppresses the variations from the load and the source substantially. For the relation with the reference voltage, the expression approximately reduces to $1/H(s)$ where $H(s)$ is the gain of the feedback network. For low frequency range, it simply equals to the ratio of the resistor divider. This means the desired output voltage is well defined by the reference voltage as well as the feedback network. Meanwhile, variations injected from either the input source or from the load are suppressed by the loop.

Therefore to design a buck converter which has its output voltage closely tracking the varying reference voltage, the foremost step is to design a stable feedback loop with high in-band gain and enough bandwidth. When the negative feedback is introduced, even though the open-loop response $T(s)$ is stable and contains no RHP poles, it is still possible that the closed loop characteristic $T(s)/(1+T(s))$ contains RHP poles. Thus the feedback system will fail to regulate the output voltage and is likely to induce oscillation. Even if the feedback system is stable, it is still possible for the converter output to have undesirable overshoot or undershoot effect. Therefore the stability of the feedback system must be carefully studied. The phase margin test can be adopted to evaluate the stability condition of the system. If there is only one gain crossover point and the loop gain $T(s)$ contains no RHP poles, the closed loop term $1/(1+T(s))$ will not have RHP poles if the phase margin is positive [57]. For better transient response where excessive ringing at the output node is avoided, a phase margin larger than 45° is usually preferred. For the VMC buck converter, by substituting equation (5.6) into (5.7), the transfer function from the duty cycle D to the output voltage can be expressed as follows:

$$T(s) = H(s) \cdot \frac{V_g}{V_M} \cdot \frac{1 + s/\omega_{\text{esr}}}{1 + s(R_C C_O) + s^2(1 + \frac{R_C}{R_{\text{fb1}} + R_{\text{fb2}}})LC} \quad (5.9)$$

The last term is the transfer function of the low-pass filter at the power stage which incorporates a pair of complex poles and one LHP zero. Although the system stability is evaluated by looking at the phase margin and gain margin, the damping factor associated with the output stage filter also has significant effect on the transient performance of the converter. For voltage mode buck converters, due to the complex pole pairs associated with the output filter, frequency compensation is required for a stable feedback loop. Dominant pole compensation is the most straightforward compensation scheme which creates a low frequency pole to keep the loop stable. However, the bandwidth of the loop is reduced to make the crossover frequency even lower than the output resonant frequency. The resonant frequency is determined by the L and C components and is usually at around a few 10s

of kHz, which means the bandwidth of the loop will be even smaller than the audio signal band. In order to meet the stability and larger bandwidth at the same time, additional phase boosting has to be introduced to compensate the phase drop caused by the complex pole pairs. Type II compensator provides a maximum phase boost of 90° which is normally used in CMC buck converter since the additional current loop reduces the complex pole pairs into one real pole. For voltage-mode buck converter, the pole pairs will have 180° phase drop to the loop response, thus using type III compensator becomes a typical solution for the VMC buck converter.

5.4.3 Compensator Design of The Voltage-mode Buck Converter

The schematic of a type-III compensation error amplifier (EA) is shown in Fig 5.18. The feedback network consists of three resistors and capacitors, the open-loop transfer function can be found as:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{(1 + s \cdot C_2 R_2)[1 + s \cdot C_3(R_1 + R_3)]}{s \cdot (C_1 + C_2)R_1(1 + s \cdot C_1 R_2)(1 + s \cdot C_3 R_3)} \quad (5.10)$$

As can be observed from expression, the type-III compensation introduces a pair of LHP

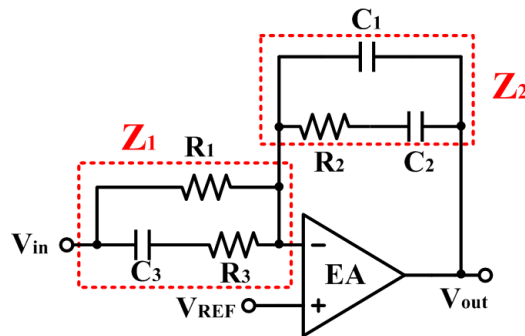


Figure 5.18: Topology of a typical type-III compensator

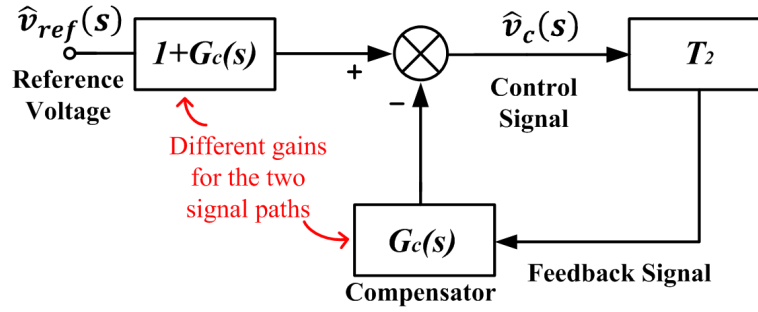


Figure 5.19: Small signal block diagram of the type-III compensated buck feedback system

poles and zeros. The two zeros can introduce 180° phase increase to compensate the phase drop at the complex pole frequency. The pair of poles are introduced to quickly diminish the gain at higher frequency. The locations of the LHP zeros are usually designed to be slightly lower than the resonant frequency so that higher in-band gain can be preserved. One pole is designed to cancel the effect of the LHP zero created by the equivalent series resistance (ESR) of the output capacitor.

For normal VMC buck converter, the above analysis holds for design of the compensator. However, for a reference-tracking buck converter, in Fig 5.18 the ac gains seen from V_{REF} to V_{out} and from V_{in} to V_{out} are not equalized. This is because the ac signal from the reference is fed into the system from the positive terminal of the EA. Thus the ac gain seen from the reference voltage and from the feedback signal are different. Referring back to Fig 5.17, the simple subtraction between reference voltage and feedback signal is no longer valid with typical type-III compensator as the gain seen from the two different signal paths are not exactly the same. Hence the reference to output transfer function needs some amendments. The simplified small signal block diagram of a type-III compensated feedback system without the disturbances from the source and load is depicted in Fig 5.19. The transfer function from the reference to the output can be derived as:

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{ref}(s)} = \frac{T_2 + T_2 G_c(s)}{1 + T_2 G_c(s)} \approx \frac{1 + G_c(s)}{G_c(s)} \quad (5.11)$$

Table 5.6: Component values used for the type-III compensator

R_1	220 k Ω
R_2	110 k Ω
R_3	5 k Ω
C_1	1 pF
C_2	30.5 pF
C_3	18 pF

$G_c(s)$ is actually the transfer function of the compensator, it can be expressed as Z_2/Z_1 as in Fig 5.18. The reference-tracking capability is only required for the audio band signal, thus the expressions of the two impedance can be further simplified. Since the purpose of C_1 is to create a LHP pole with R_2 at around half of the switching frequency, the value of C_1 is much smaller than C_2 , hence at low frequency range the expression of Z_2 can be approximated as $Z_2 = R_2 + 1/(s \cdot C_2)$. Similarly, the impedance of C_3 is much larger than R_1 at lower frequencies and Z_1 can be approximated as R_1 . Therefore, the reference to output transfer function at low frequency range (≤ 20 kHz) in equation (5.11) can be simplified into:

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{ref}(s)} = \frac{1 + \frac{Z_2}{Z_1}}{\frac{Z_2}{Z_1}} \approx \frac{R_2 + \frac{1}{s \cdot C_2} + R_1}{R_2 + \frac{1}{s \cdot C_2}} = \frac{1 + s \cdot (R_1 + R_2)C_2}{1 + s \cdot R_2 C_2} \quad (5.12)$$

One can infer from the above equation that the reference to output transfer function exhibit a pole-zero doublet the frequencies of which are not closely matched for R_1 and R_2 are in the same order of magnitude. This mismatch in frequency domain will translate to a phase delay in the time domain for the two signals. In other words, V_{out} may not closely track V_{REF} as expected which exacerbates the delay issue mentioned in the previous chapter. The solution to this problem is rather simple, we only need to equalize the gain seen from the two different signal paths. One solution would be cascading additional gain stage which equals to $G_c(s)/(1+G_c(s))$. However, the extra gain stage require additional resistors and capacitors which increases the active area.

Another solution would be subtract the difference between the reference and feedback

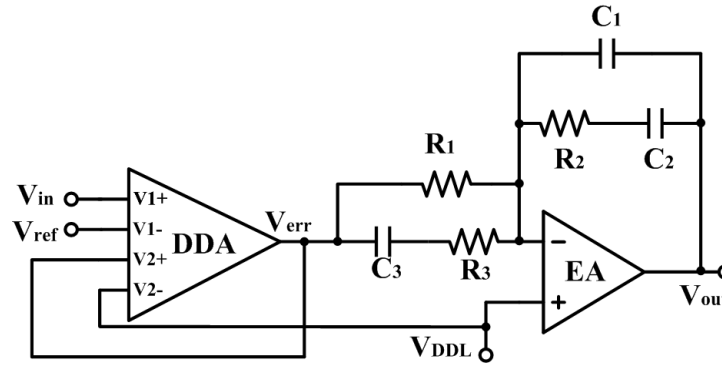


Figure 5.20: Proposed DDA-based type-III compensator

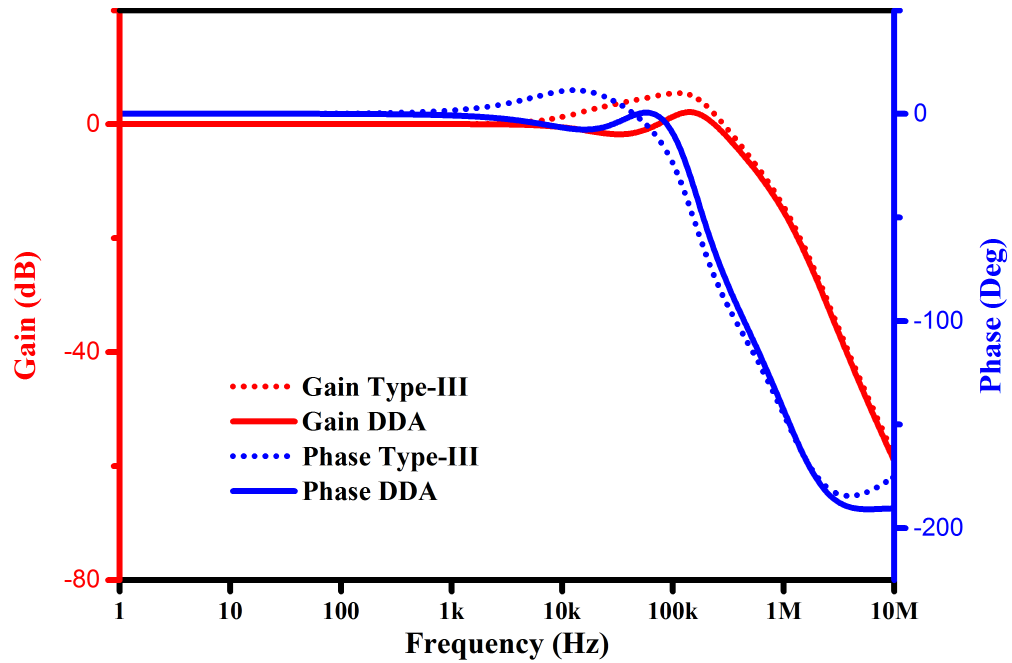


Figure 5.21: comparison between the closed-loop reference-to-output frequency response for type-III and DDA-based type-III compensators

signal first, and then feed only the error signal into the EA. To realize this idea, a differential difference amplifier (DDA) can be implemented right before the EA for the error voltage extraction. The realization of the proposed compensator for the reference-tracking buck converter is depicted in Fig 5.20. The feedback signal which is denoted as V_{in} to the compensator are fed into the first pair of input terminals of the DDA together with the

reference voltage. The DDA which is connected in a unity-gain configuration will sense the difference between these two signals and buffer the error signal to the type-III EA. The positive terminal of the EA as well as the positive terminal of the DDA will be dc biased to $V_{DDL} = 1.2$ V which ensures sufficient voltage swing of the compensator. Thus the ac error voltage V_{err} will swing around the dc biasing level and propagate through the EA. With the assistance of the DDA, the V_{ref} and V_{in} are no longer injected from different terminals of the EA, thus the gain of the two signal paths are equalized to ensure optimized tracking performance in the time domain. The closed-loop reference-to-output transfer function for the typical type-III and the DDA-based type-III compensators are plotted in Fig 5.21.

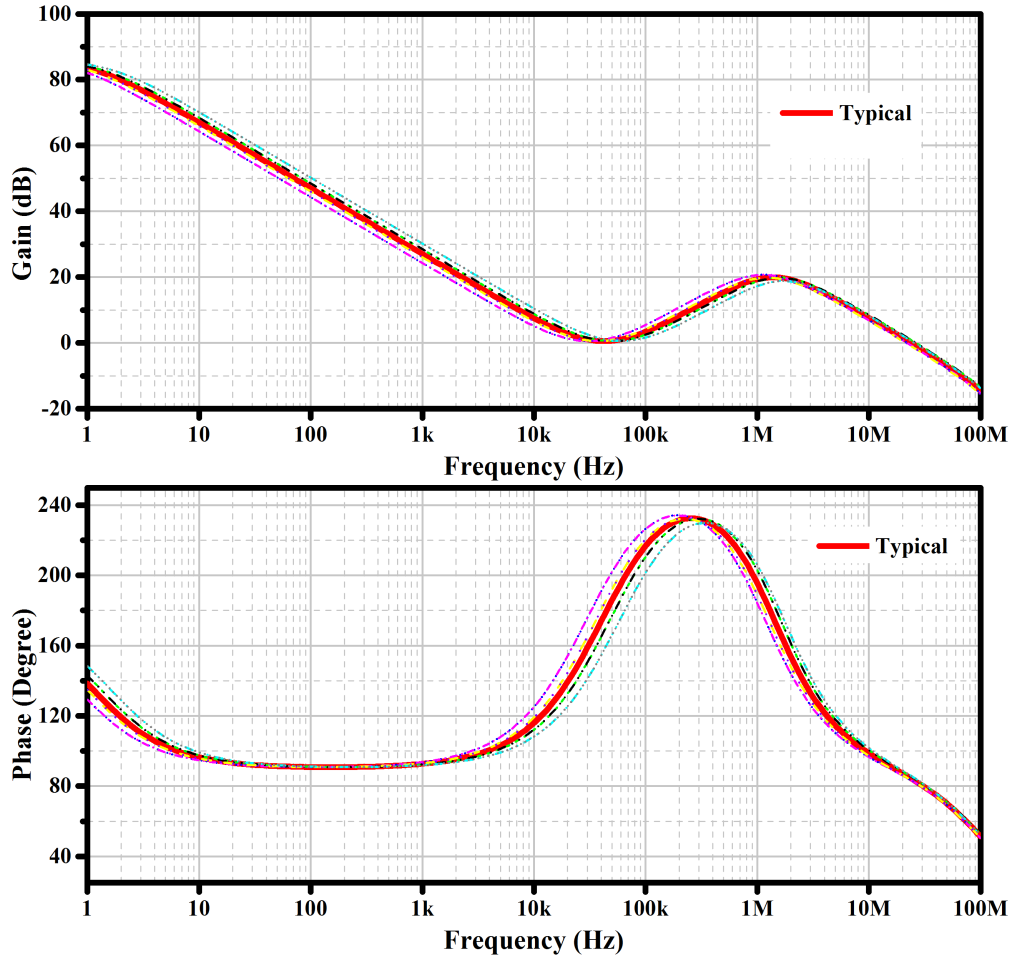


Figure 5.22: Simulated frequency response of the DDA-based type-III compensator

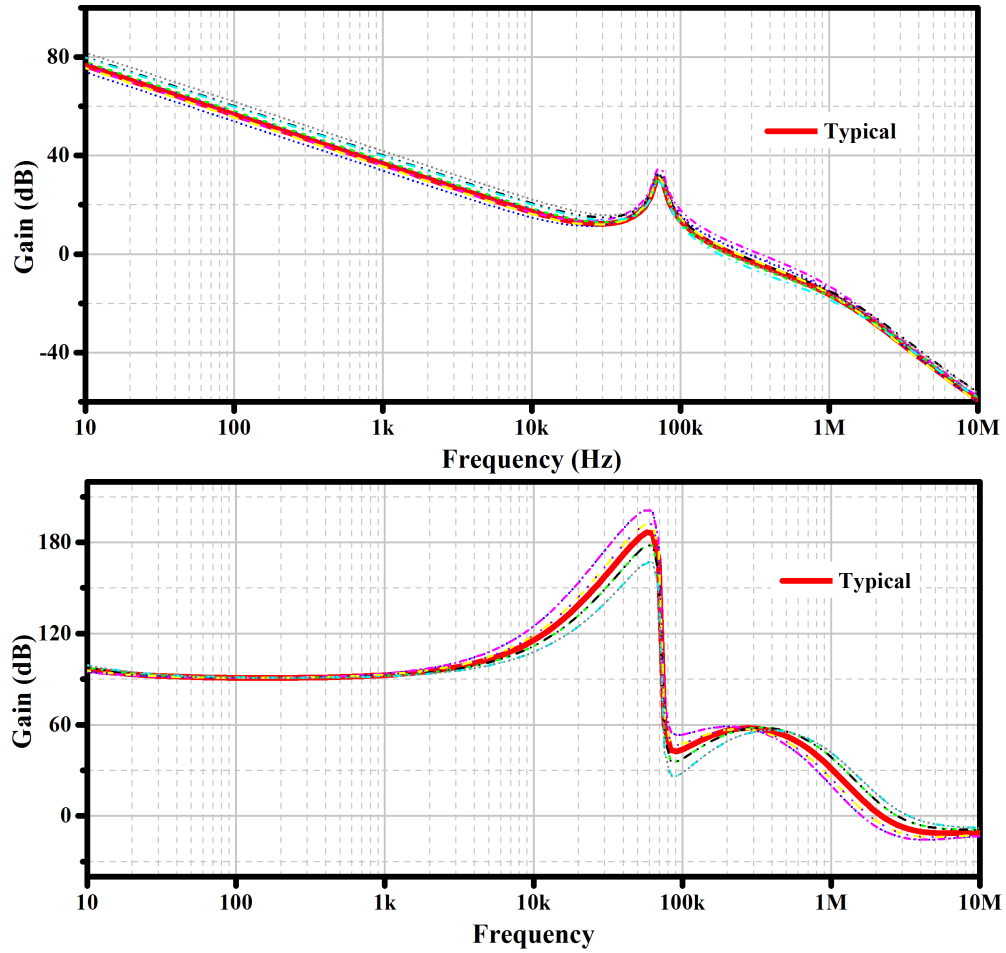


Figure 5.23: Simulated frequency response of the loop gain function of the buck converter

Results show that at lower frequency range the gain for both structures are close to unity. While as frequency increases beyond 10 kHz, the gain plot of the type-III only compensator yields a ramping up behavior due to the mismatch of the pole-zero doublet. For the DDA-based compensator, the gain plot remains flat with little deviation for the entire audio frequency band.

The component values of the passive components used in the compensator are listed in Table 5.6. Considering the deviation of the resistor values through extreme process and temperature conditions. The simulated frequency responses of the proposed type-III

compensator and the loop gain function across different process, voltage and temperature (PVT) variation corners are plotted in Fig 5.22 and Fig 5.23 respectively. The resistors are realized with p+ poly resistors which has a tolerance of $\pm 20\%$. For the temperature corners -40°C and 120°C are used as the two extreme conditions. The voltage variation for a buck converter mainly results from the change of the voltage rating at the battery source, therefore the operating voltage range of a Lithium-ion battery is used as the testing conditions with the typical value set to 3.3 V and the two extreme values set to be 2.8 V and 4.2 V. Considering all the three factors with each having two extreme conditions, it gives altogether eight corner cases which are shown in the two figures. For all the corner conditions, the buck loop achieves a minimum and maximum loop bandwidth of 182.1 kHz and 342.8 kHz respectively. For typical condition, the loop bandwidth is 225.4 kHz and the phase margin is 57° .

5.4.4 Transient Improvement for the Buck Converter

For conventional PWM-based buck converters where the reference voltage is a DC value, the load current step will cause overshoot or undershoot to the output voltage. This error voltage will be sensed and amplified to saturate the duty ratio and hence correct the output voltage. The loop response time is determined by the bandwidth of the control loop when the error voltage is small. For large transient, the response time is usually limited by the slew rate at the output of the error amplifier. For class H amplifier, The transient response requirement to the output load step is a bit different from the conventional buck converter. This is because for the class H amplifier system, the load seeing from the buck converter output is only the class AB amplifier cascading with the headphone load. As previously mentioned, the IAD block is used to sense and extract both the amplitude and frequency information of the input audio signals. Which means the reference signal can be predictive for the demanded load current. Therefore, the transient performance of the buck converter used in the class H system is largely dependent on its reference-tracking capability, which

will be the focus of the transient improvement of the buck converter.

The small signal analysis in the previous chapter analyzes the reference-to-output function of the converter. With the proposed DDA-based type-III compensator, the unity gain is kept for a wider frequency range which covers the audio signal band. However, the above ac analysis only applies for relatively small changes around its dc biasing point. When the circuit is facing large signal transient and the error voltage fed into the EA becomes much larger, it is usually the large signal analysis that is more effective in estimating the transient response time. For PWM control, its major drawback to be applied in a reference-tracking power converter is its slow response to the change of the error voltage. As shown in Fig. 5.20, when a sudden change appears at the reference voltage V_{ref} , the error voltage V_{err} will move counteractively to propagate this error to the EA. Consequently, the output of EA is supposed to be quickly pulled down or charged up in order to saturate the duty cycle, so that the output stage can react to adjust the output voltage. However, due to the type-III compensation network, large capacitors are associated with the EA output, for this case the value of C_2 can be as large as 30.5 pF. Hence the converter's response to V_{ref} change is limited by the slew rate of the EA. When frequency of the input signal increases, the frequency of V_{ref} goes up as well. If the converter output is unable to catch up with the fast changing V_{ref} , clipping will be observed at the amplifier output, resulting in severe distortion.

One straightforward solution would be enhancing the current driving capability of the EA, however this will lead to larger active area and quiescent power consumption of the EA. Another more effective approach is by applying the reference voltage feedforward technique as reported in [64, 65]. The concept of this technique is depicted in Fig 5.24. The varying V_{ref} is fed forward to add with the EA output V_E to get the final error voltage V_{E1} . This V_{E1} is the final error voltage which is compared with the ramp signal to generate the duty cycle for the power stage. Through this approach, the duty cycle of the PWM signal can almost instantly respond to the change in V_{ref} and does not have to wait for the slow charging behavior at node V_E . In order to crystalize this idea without affecting the behavior of the

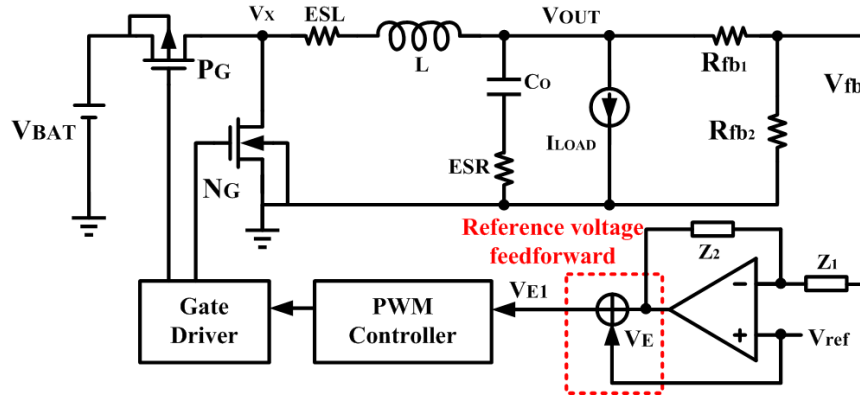


Figure 5.24: Concept of the reference feedforward technique for enhancement of reference-tracking capability

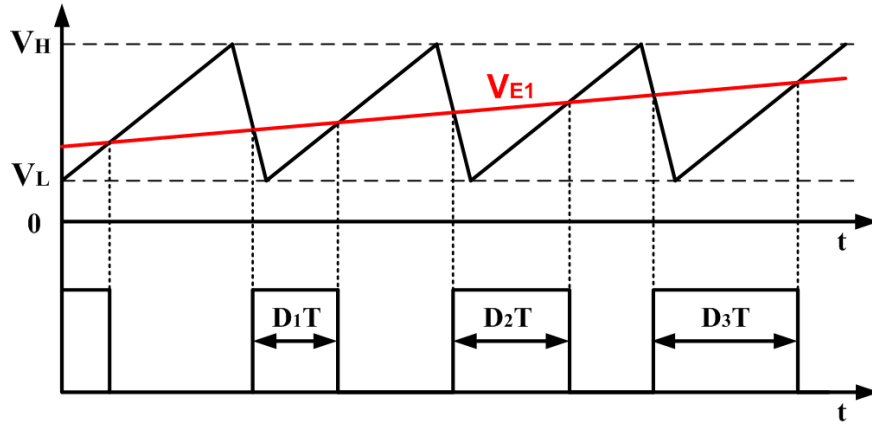


Figure 5.25: Duty cycle generation of a PWM-based buck converter

buck feedback loop, the steady state operations of the loop with the reference feedforward mechanism must be analyzed. At steady state, the output voltage is correlated with the reference voltage as:

$$V_{\text{ref}} = V_{\text{out}} \cdot \frac{R_{\text{fb2}}}{R_{\text{fb1}} + R_{\text{fb2}}} = b \cdot V_{\text{out}} \quad (5.13)$$

The duty cycle of the buck converter is determined by the ramp signal and the error voltage V_{E1} as shown in Fig 5.25. The instant voltage level of V_{E1} intersects with the

periodical sawtooth waveform and generates the fixed frequency pulse signals. Thus the relation between V_{E1} and the duty cycle can be expressed as:

$$D = \frac{V_{E1} - V_L}{V_H - V_L} = \frac{V_{E1} - V_L}{V_M} \quad (5.14)$$

where V_M stands for the magnitude of the ramp signal. By using the proper linearization method the output voltage at steady state can be expressed as the product of input voltage and the duty cycle. Thus equation (5.13) and (5.14) can be combined to obtain the relation between V_{E1} and V_{ref} .

$$\begin{aligned} V_{out} &= D \cdot V_{IN} = \frac{V_{E1} - V_L}{V_M} \cdot V_{IN} = V_{ref}/b \\ \text{thus, } V_{E1} &= \frac{V_M}{b \cdot V_{IN}} \cdot V_{ref} + V_L \end{aligned} \quad (5.15)$$

From Fig 5.24 it is obvious that:

$$V_{E1} = V_{ref} + V_E \quad (5.16)$$

By observing the terms in equation (5.15) and (5.16), it can be found that if we can equate the coefficient of V_{ref} , then V_E will simply be equal to V_L , which is a predefined dc level used as the low boundary for generating the sawtooth/ramp signal. In other words, the change of reference voltage will be directly coupled to the final error voltage V_{E1} and affect the value of duty ratio D almost immediately. At the same time, the EA output will be kept at a dc biasing level which means the charging effect at this node can be bypassed during large signal transient. To satisfy the above relation, the condition that $V_M = b V_{IN}$ must be met, which means the amplitude of the sawtooth signal must be designed proportional to the input battery voltage. In the literature, one embodiment of this idea is reported as the "End-point Prediction" technique (EPP) [64]. The schematic of the supply-dependent ramp signal generation circuit is depicted in Fig 5.26.

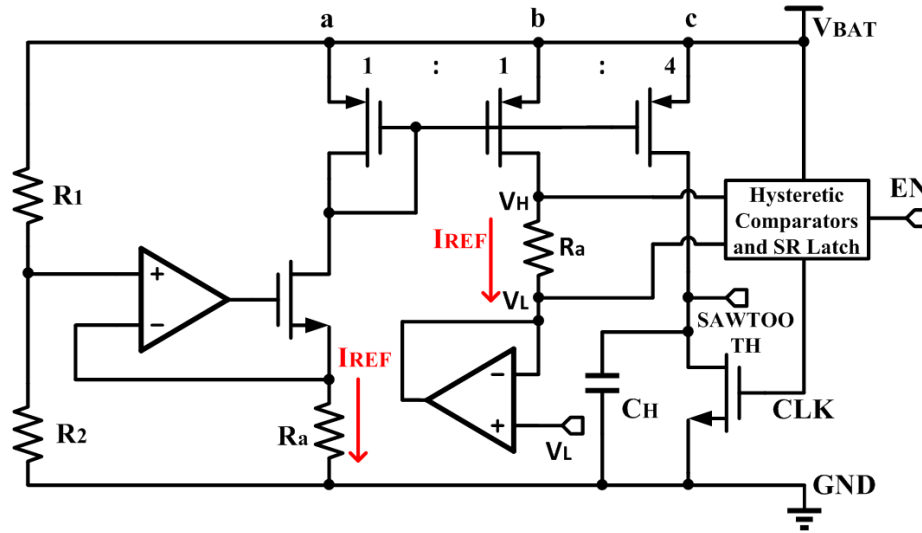


Figure 5.26: Supply-dependent ramp signal generator

With the resistor divider of R_1 and R_2 , the supply voltage is scaled down and the current I_{REF} which is proportional to V_{BAT} is generated. The 1:1 current mirror copies this current to branch b and hence the voltage difference between V_H and V_L also becomes supply dependent. The two voltage levels are used as the reference voltages for a typical ramp function generator which usually consists of a pair of hysteresis comparators and one SR latch. Therefore, the amplitude of the ramp signal V_M is related to the supply voltage V_{BAT} with a ratio dependent on the resistor values. In our design, similar topology was used. For our case, the ratio between V_{BAT} and V_M is set to be 3, thus V_M equals to 1.1 V under a supply of 3.3 V. V_L is selected to be 0.4 V, with a battery voltage ranges from 3.3V to 4.2V, the upper boundary V_H swings from 1.5V to 1.8V leaving enough headroom voltages for the transistors in this topology.

The clock frequency of this ramp generator is determined by the charging and discharging time of the hold capacitor C_H . In order to achieve a large maximum duty ratio for the PWM signal, the discharging current of C_H is designed to be much larger than the charging current so that the ramp down time of the sawtooth signal is very short. However, excessive large ratio of the discharging transistor will give undershoot below the value of V_L as the

feedback has delay time caused by the comparators as well as the SR latch. Thus the maximum duty ratio trades with the accuracy of V_M . As a compromise, we define the maximum duty ratio to be around 0.9 so that the maximum output of the buck converter can achieve 3 V. At the same time, the undershoot of the ramp signal is controlled within 100 mV so that the reference feedforward function is negligibly affected. For the realization, the values of R_a is 275 k Ω and the oscillation frequency is around 2 MHz. C_H is implemented with a metal-insulator-metal (MIM) capacitor of 1.04 pF.

The next step for implementing the EPP scheme is to realize the summing function of V_E and V_{ref} . It is realized by the current-mode summing circuit as shown in Fig 5.27. The reference voltage V_{ref} is from the IAD block which is exactly the same as the desired level of buck output. As in the EPP network, the reference voltage is scaled down for comparison with the sawtooth signal, thus the original V_{ref} must also be scaled with the same factor. The resistor divider formed by R_1 and R_2 are exactly the same as in Fig 5.26. Additional buffer is used to separate the IAD block from the current-mode adder. The current-mode adder circuit mainly consists of the current mirror as well as the buffer stage. The EA output V_E is buffered to generate a proportional current through resistor R_3 and this current is mirrored to the right side branch to perform the summing function of V_E and V_{ref} .

5.4.5 Light-load Efficiency Improvement with Dual-mode Operation and Modified Control Algorithm

Power losses during the operation of a dc-dc converter are mainly contributed by the conduction loss, the switching loss and the static power loss. The conduction loss scales quadratically with the load currents and is caused by the resistive components in series with the load due to non-ideality. These resistive components include the equivalent ON resistance of the power switches as well as the passive filter elements (L and C), the interconnections resulting from the chip packaging and PCB routing. The static power loss

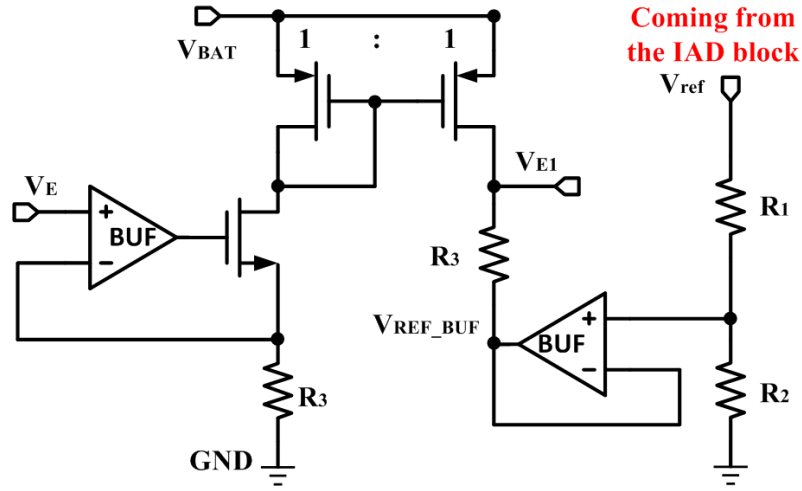


Figure 5.27: Schematic of the current-mode adder circuit

results from the quiescent power consumption of the controller circuitry, it can be optimized by switching off the blocks that are not being used. As load current increases, the weight the static loss contributes gradually becomes negligible. The switching power loss is associated with the switching activities of each clock cycle, which involves the charging and discharging of the gate of a power transistor, the charge loss on the capacitance at the switching node due to non-ideal dead time. These switching losses are independent of load current and will hence lower the converter efficiency under light load condition. For PWM-based control, the switching frequency is fixed despite the load current conditions, the switching losses which are load-independent will be more significant as the load current reduces. Thus the light-load power efficiency is degraded due to the excessive high operating frequency. The pulse-frequency modulation (PFM), on the other hand, does not rely on a high frequency clock. It switches on the power transistors for a constant period of time, and it determines the onset of next cycle base on the comparison between the output and the reference voltage levels. As a result, the idle time of the control pulse will increase with the decrease of load current, effectively reducing the switching frequency of the converter. Thus, the switching losses can also be scaled down with the load current. Therefore, a popular technique to achieve high power efficiency over a wide load range is the hybrid control scheme which

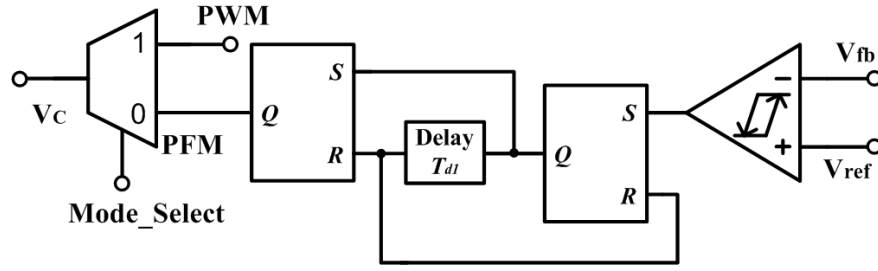


Figure 5.28: Schematic of constant on-time PFM control

incorporates both the PWM and PFM mode [66–70]. For light load conditions, the PFM mode is selected to reduce the operating frequency of the converter and hence boost the efficiency. For heavy load conditions, the PWM mode is activated so that the operating frequency is fixed and will not surge to an excessive high level.

In this design, the typical constant on-time (COT) control is adopted for the PFM control. The schematic of the COT blocks are depicted in Fig 5.28. Apart from the PWM path and additional control path is embodied with the COT concept. The scaled output voltage V_{fb} is fed back to compare with V_{ref} . Once V_{fb} drops below V_{ref} , the output of the hysteresis comparator will be flipped high and set the first SR latch. A constant delay time T_{d1} will generate a burst of signal with pulse-width of T_{d1} , then the second latch will be reset. At the same time, this reset signal will also reset the first latch so that the set signal of the second latch also stays low. After another delay time of T_{d1} , all nodes of the PFM block is reset to low and it will start another pulse base on the comparator output. At the last stage, a multiplexor (MUX) will select either the PWM or PFM control signal according to the mode selection signal which will be touched later on.

For the class H amplifier, the load current is relatively low when the lower supply V_{DDL} is being used. Therefore, the heavy load and light load conditions can roughly be distinguished by the *Mode_Select* signal from the IAD block as shown in Fig 5.14. When *Mode_Select*=1, the PWM signal is selected and the system is under class H supply-tracking mode. When *Mode_Select*=0, the PFM signal will take control and the system works

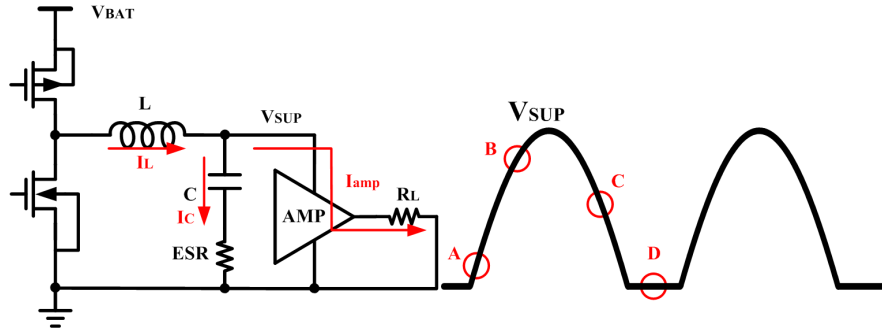


Figure 5.29: Illustrations of inductor current load condition under class H mode operation

under class AB mode. This is indeed the same control mechanism as in [22]. However, further investigation shows that determination of light/heavy load condition simply base on the mode of operation is not correct. This is because for class H mode, the output of buck converter is moving to track the input and hence substantial current is needed to charge/discharge the output capacitor. Thus, this portion of current must be taken into account when considering the inductor current condition. This can be exemplified with the illustration in Fig 5.28.

As shown in Fig 5.29, the inductor current is divided into two portions with one charging the output capacitor and the other one supplying the class AB amplifier. Consider the load points of A and B, although the amplifier's output swing at B is much greater than in A, it is not for sure that the inductor load current at B is larger than A. This is because the slope of increase for V_{SUP} is much greater at point A, thus the charging current required by the output capacitor make the inductor load current increases sharply although it is just at the onset of supply-tracking mode. Meanwhile, the direction of the capacitor current can be reversed, which means the charges stored on the output capacitor can be reused to supply the amplifier load when V_{SUP} is supposed to ramp downward. Now when considering the load conditions at point C and D, it can be noticed that although point C is still under class H mode while point D stays within the region of class AB operation, the load current demanded from the inductor for point C can be smaller as the output capacitor is strongly supporting

the amplifier. This phenomena will be even more obvious as the input frequency increases. In a word, the output capacitor charging behavior strongly affects the definition of light load condition from the inductor's perspective, hence a more advanced control algorithm is required for light load efficiency optimization.

To validate the analysis, the above-mentioned currents can be quantified with the specific parameters used for this design. For class H mode operation with balanced sinusoidal wave as input, the input signals, the output signals and the supply voltage have the following expressions:

$$\begin{aligned}
 V_{ip} &= V_{id} \cdot \sin(\omega t) \\
 V_{in} &= -V_{id} \cdot \sin(\omega t) \\
 V_{op} &= 4V_{id} \cdot \sin(\omega t) + V_{DSAT} \\
 V_{on} &= V_{DSAT} \\
 V_{out} &= 4V_{id} \cdot \sin(\omega t) \\
 V_{out} &= 4V_{id} \cdot \sin(\omega t) + 2V_{DSAT}
 \end{aligned} \tag{5.17}$$

the inductor load current can be expressed as:

$$\begin{aligned}
 I_L &= C_{out} \cdot \frac{dV_{sup}}{dt} + \frac{V_{out}}{R_L} \\
 &= 4V_{id}\omega C_{out} \cdot \cos(\omega t) + \frac{4V_{id} \cdot \sin(\omega t)}{R_L}
 \end{aligned} \tag{5.18}$$

Substitute the values of each parameter as $V_{id}=650$ mV, $V_{DSAT}=200$ mV, $C_{out}=2.2\mu\text{F}$ and $L=2.2\mu\text{H}$. The inductor load current for different input frequencies can be calculated. Results are shown in Fig 5.30. It can be observed from the figure that as input frequency increases, the portion of inductor current contributed by the output capacitor becomes more dominant. For a ramping up reference with high input frequency, the inductor current demanded by the output capacitor can be as high as a few hundreds of mA which overturns

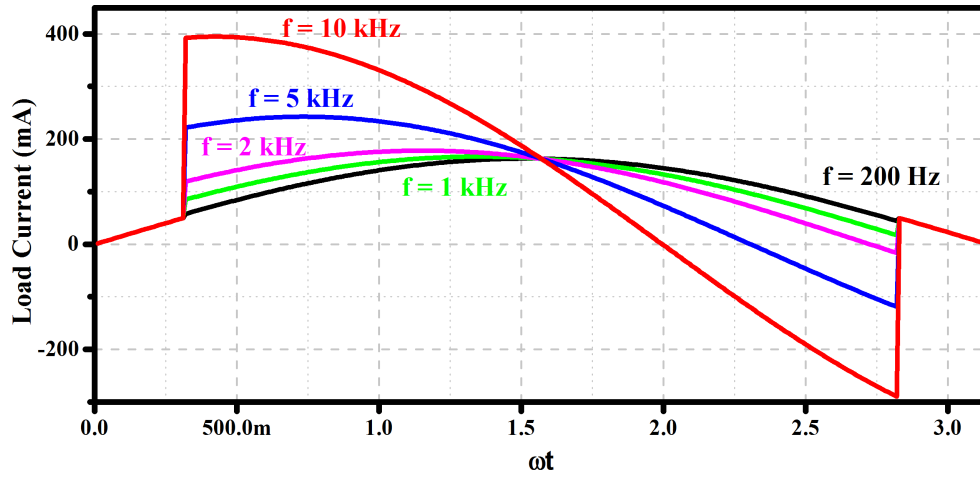


Figure 5.30: Inductor load current under supply-tracking mode with different input frequencies

the presumption of load current in Table 5.5 which only considers the load condition of the amplifier. Meanwhile, for the ramping down phase, the capacitor discharging current is so strong that it even needs the inductor currents to reverse direction to balance the charge delivered to the amplifier load. If PWM control is still selected based on the mode of operation, the excessive switching loss will degrade the efficiency. Hence the issue of determination of light load condition is validated. The strong discharging capacitor current may render the capacitor output voltage to be higher than the desired level as in equation (5.17) and fails to behave a close tracking relation. However, this is acceptable as the supplying voltage is higher than the amplifier output and the buck output shall just wait for the amplifier load current to discharge.

It can be inferred from Fig 5.30 that in order to optimize the control algorithm, first the ramping up transient of the reference voltage should be monitored and sufficiently large current driving capability of the converter should be designed. Secondly, for a correct judgement of the converter's load condition, the focus should be placed on the inductor current instead of the amplifier's load current. For this reason, the inductor waveform for different conditions should be analyzed. Fig 5.31 depicts the inductor waveforms for both

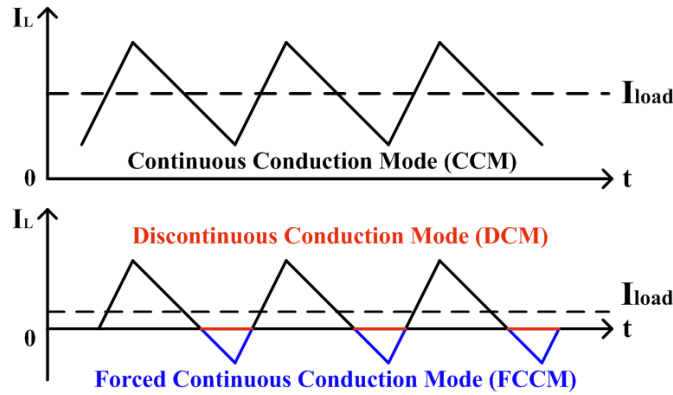


Figure 5.31: Inductor current waveforms under different mode of conduction

continuous conduction mode (CCM) as well as discontinuous conduction mode (DCM). The integration of inductor current over one switching cycle reveals how much charge is delivered to the output, which can be averaged within one period to get the averaged inductor current. Under steady state the averaged inductor current must be equal to the actual load current. When the inductor current reduces to be less than half of the peak-to-peak inductor current ripple, the DCM should take place otherwise the forced continuous conduction mode (FCCM) will make the inductor current flow in the reversed direction [71]. This negative inductor current must be prohibited as it is essentially draining the charge stored at the output capacitor to the ground. In this case, the average inductor current is not high enough to support the CCM operation, thus the triggering of DCM operation can be used as a signal when the inductor current enters light load condition regardless of the its output voltage level.

Therefore, in order to prevent the inductor current from reversing its direction and triggering the DCM operation at the same time, the zero crossing point of the inductor current must be monitored. This circuitry is usually referred as the zero current detection (ZCD) block. Instead of detecting the zero crossing of the inductor current, it is equivalent to detecting the zero voltage crossing of the switching node V_X . When the freewheeling NMOS switch is conducting, the voltage at V_X can be expressed as:

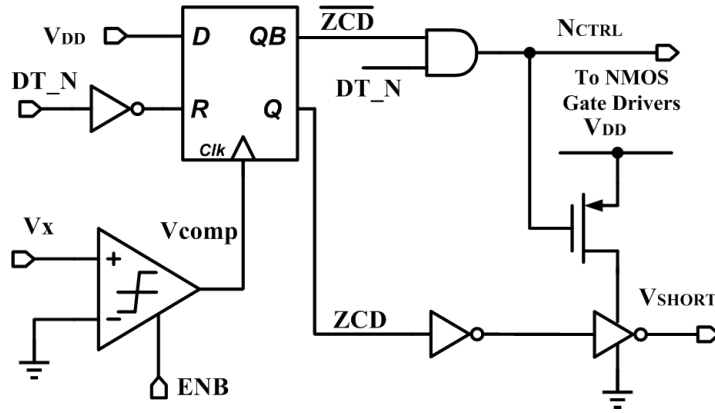


Figure 5.32: Schematic of the zero current detection block

$$V_X = -I_L \cdot r_{ds,n} \quad (5.19)$$

Thus, during the NMOS freewheeling phase, with the decrease of the inductor current, V_X will slowly ramps up from a negative value towards zero. In the ideal case, V_X will hit the zero level at exactly the same time when the inductor current diminishes to zero. Base on this concept, the ZCD block can be implemented as shown in the Fig 5.32. For real implementation, the comparator should react before the moment V_X increases to zero to compensate for the propagation delay of the comparator as well as all the digital logic circuits. Therefore, some offset should be added in order to make the comparator flip its output before the zero point. In our design, the input differential pairs of the comparator are designed to be unbalanced to create a input referred offset voltage. These two transistors are partitioned into 32 multiple finger elements and are laid out with the common-centroid layout pattern. For one transistor, one finger is connected as a dummy transistor, leaving only 31/32 of the equivalent geometric ratios. Hence the offset is created. Simulation results show that the comparator is pre-triggered and kept a minimum freewheeling current of 8.9 mA when both power switches are off.

The DT_N and DT_P are the NMOS and PMOS control signals generated from the

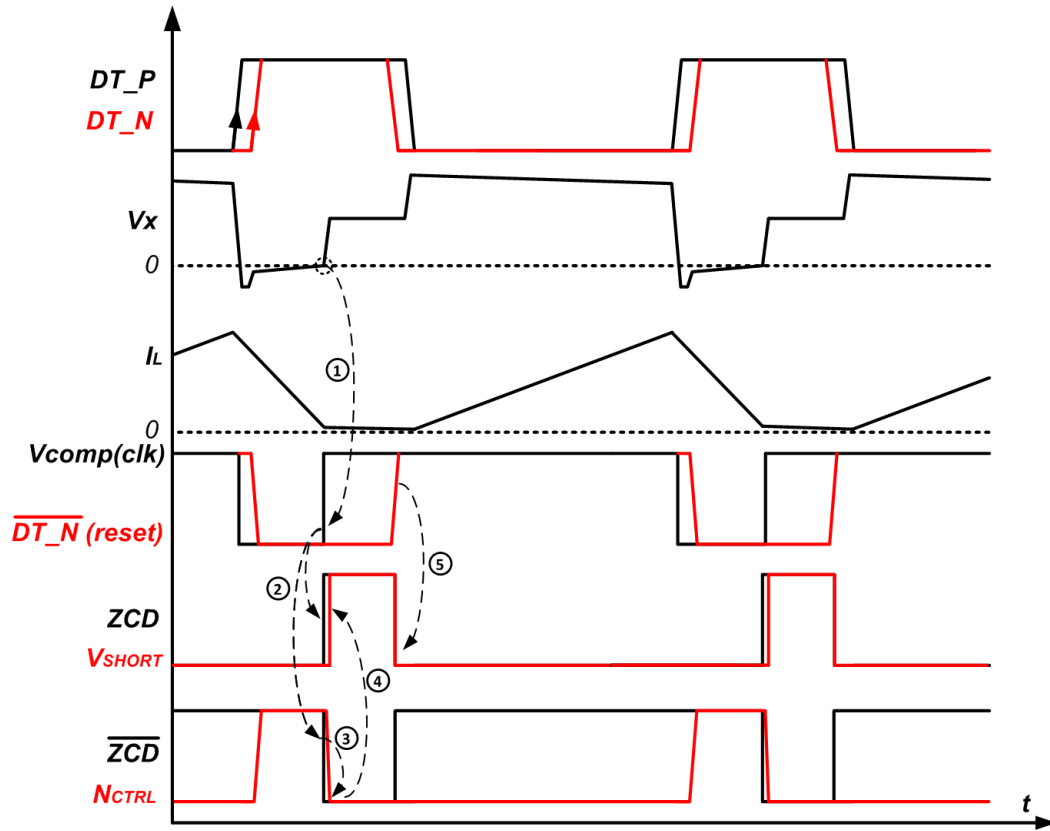


Figure 5.33: Waveforms of different control signals during the ZCD operation

preceding PWM/PFM stages with added dead time. ENB is the enable signal for the zero crossing comparator which is active low. N_{CTRL} is the final gate control signal for NMOS switch, before it is used to drive the power transistor it will go through a series of gate drivers to amplify its driving capability. V_{SHORT} is an additional gate control signal for a NMOS freewheeling switch, it is supposed to short the inductor L when both of the power transistors are switched off. In real implementation, due to the delay in each block, the NMOS switch cannot be switched off precisely at the moment when the inductor current reduces to zero, instead a small amount of current is allowed to flow in the inductor. Without the freewheeling path provided by this additional switch, oscillation will build up at the output filter which is now an LC tank. The ZCD signal is buffered to generate this V_{SHORT} signal, and only after N_{CTRL} becomes low will this V_{SHORT} be enabled. The operation of

this ZCD control logic is further delineated as waveforms of each control signals as in Fig 5.33.

As shown in the figure, the ZCD cycle starts with the PMOS being switched off, which also enables the zero crossing comparator. After a short dead time, NMOS is turned on to serves as the synchronous diode. As the inductor current keeps on decreasing and finally hits the zero level, the comparator output V_{comp} is flipped high, which is also the clock signal of the D flip flop. Thus the ZCD signal is activated at the rising edge of the clock, and consequently the NMOS control signal is turned low. After that, the freewheeling switch is turned on to short the inductor. The system remains in this state until the DT_N control signal is turned low which means the PMOS transistor is about to be switched *ON* for the next conduction cycle. Therefore, the D flip flop is reset and the comparator is disabled for the next cycle.

With the assistance of the ZCD block, the inductor current loading condition can be detected and used to trigger different modulation scheme respectively. At the same time, the heavy load condition where the reference voltage ramps up quickly should also be monitored. As shown in Fig 5.30, at the beginning of the supply-tracking operation, huge amount of current is required by the load due to the large slope of the reference voltage. Therefore a slope detector circuit should be designed and deployed to detect such drastic changes in the input transient. Normally, a differentiator circuit is able to sense the rate of change of an ac signal, however, its output swing with respect to the input rate of change is multiplied with the time constant of the R and C used in the differentiator. The variation of the resistor value across PVT corners will make the sensing of input rate of change inaccurate. Here we proposes a novel slope detection circuit which eliminate the effect of the inaccurate resistor. The schematic of the proposed slope detector is depicted in Fig 5.34.

AMP1 together with all the R and C components form the differentiator circuit, it senses the rate of change from the reference voltage V_{ref} of the IAD block. V_{DDL} is the 1.2 V bias voltage, it fixes the voltage at the positive input of AMP1 V_I , so that the AMP1

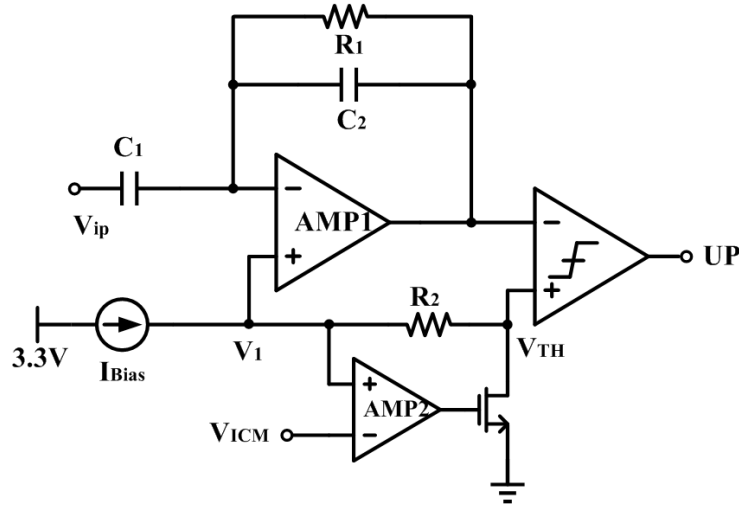


Figure 5.34: Schematic of the slope detection circuit

is dc-biased at 1.2V. V_{TH} is a dc level created for comparison purpose, in the schematic the difference between V_1 and V_{TH} is $I_{Bias}R_2$. When the reference voltage is having a high frequency spike, AMP1 will swing downward with the amplitude proportional to the time constant R_1C_1 . The condition for the comparator output to flip is described as below:

$$\begin{aligned}
 V_1 - R_1C_1 \cdot \frac{dV_{ref}}{dt} &= V_{TH} = V_1 - I_{Bias}R_2 \\
 \frac{dV_{ref}}{dt} &= \frac{R_2}{R_1} \cdot \frac{I_{Bias}}{C_1}
 \end{aligned} \tag{5.20}$$

By using the same type of resistance and matching the layout for R_1 and R_2 , the input rate of change to be detected is determined by the biasing current and C_1 only. The biasing current is generated from the constant- g_m biasing which serves as the biasing current for all the analog blocks in the class H system, the resistor used for the biasing circuit is an external high precision resistor. Therefore its deviation due to the variation of resistor value is much reduced. The *Mode_Select* signal is the same as in the IAD block which detects the mode of operation of the amplifier, thus the UP signal becomes high only when both of the following conditions are met:

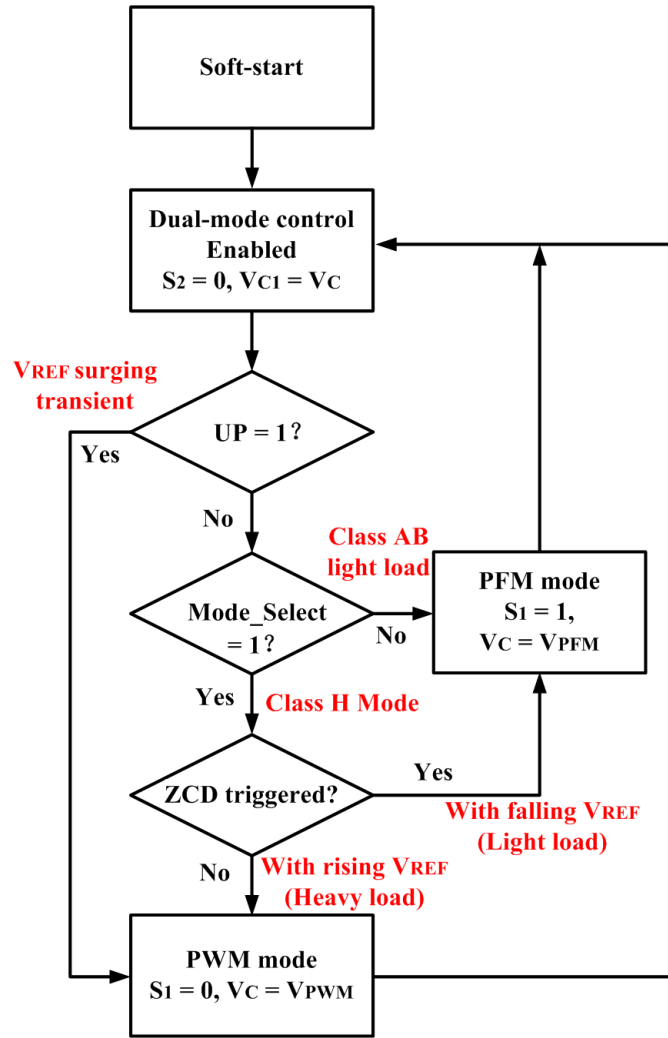


Figure 5.35: Flow chart of the modified control algorithm of the buck converter

- (i) High frequency signal is detected
- (ii) Input signal is large and the system will be working in class H mode.

With the ZCD and the slope detection circuit, both the light load and the fast reference rising transient can be detected. Thus the control algorithm can be modified to optimize the power efficiency of the buck converter for a wide load range.

The flow chart of the proposed algorithm for the buck converter is depicted in Fig 5.35. The system will first go through the soft-start process to have a smooth buildup of

the converter output voltage. The proposed soft-start logic will be touched in the successive section. After the buck output is settled, the dual-mode control scheme will be activated which means the MUX2 in Fig 5.16 will select V_C as the control signal, consequently comparators in the ZCD and the slope detection blocks will be activated. In the next step, the UP signal which is generated from the slope detection block will be checked. If it is high it means that due to the charging of the output capacitor the load current demanded from the inductor is tremendous. Therefore, it is deemed as the system is under heavy load condition and the control logic will select PWM regardless of the *Mode_Select* signal from the IAD block. As the slope detector directly senses the audio input voltage, the decision of control scheme is made immediately and does not need to wait for the delay in the IAD block. For input signals with moderate rate of change, the decision is made base on the operation mode of the amplifier unit. If the signal amplitude is small and the amplifier works in class AB mode, the PFM scheme will be selected. Otherwise, it is considered as the system enters the class H supply-tracking mode. For the next step, the zero current crossing will be used as the criteria to determine the buck converter's operation scheme. If the inductor current zero crossing is detected which means the DCM conduction occurs for PWM mode, it indicates that the inductor current level is small e.g. the reference voltage is ramping down. It is unnecessary to operate the controller at such a high frequency. Thus, the control scheme can be switched back to PFM. If the ZCD signal is never triggered, the inductor current is considered high and the controller will remain in the PWM scheme.

5.4.6 Soft-start Logic for In-rush Current Suppression

When the buck converter is first turned on, the converter's output is close to zero. Thus, the EA output V_E is close to the supply voltage V_{BAT} . If this V_E is still used to compare and intersect with the the sawtooth/ramp signal, the resultant duty cycle will be 100%. Therefore, the PMOS switch at the output stage will be fully turned on to charge the inductor and the value of the inductor current starts to soar. As the output voltage

increasing the rise time of the output voltage. Thus the inductor current will ramp up in a much "soft" manner and this protection scheme is called the "soft-start". The schematic of the proposed soft-start logic for the buck converter is depicted in Fig 5.36. The idea behind is to create a gradually increased pulsating signal in replace of the real PWM/PFM control signal which is 100% initially. So that, the rise time of the output voltage is effectively prolonged to reduce the peak inductor current value. The *Ramp* signal is the periodic sawtooth signal used for the PWM control. Before the system is enabled, the nodal voltage V_I is discharged to ground. Once the system is enabled, it will be gradually charged up to generate the soft-start pulsating signal V_{SOFT} . This V_{SOFT} has its duty ratio slowly increased from 0 to curb the in-rush inductor current. As shown in Fig 5.16, the V_{SOFT} signal is selected by the second 2-to-1 multiplexer MUX2 to serve as the gate control signals of the power switches. The MUX control signal S_2 is first reset to 0 when the system is disabled, which means the soft-start logic will be used whenever there is a low to high transition of the EN signal. After that, the termination of the soft-start process will be determined by the EA output. In this design, due to the adoption of the EPP scheme, the final EA output to be compared with the sawtooth signal is actually V_{EI} instead of V_E . With the buildup of the output voltage, this error voltage will gradually be pulled down. Once V_{EI} drops below V_H which is the predefined upper boundary of the sawtooth signal, the comparator output will be flipped and S_2 is going to be pulled low. This status means the error voltage has now reached the range of the sawtooth signal and the duty cycle generated from the PWM control block is valid to be used. Therefore, MUX2 will now select V_C as the control signal and the operation of the buck converter will be back on track.

For conventional soft-start logic, in order to effectively limit the inductor current, the rise time of the output voltage must be designed to be sufficiently long. This also requires the duty ratio ramp-up process of the pulsating signal V_{SOFT} to be slow, which further translate into a very slow charging behavior at V_I . Thus, the hold capacitor C_I is normally designed to be very large and needs to be implemented externally off the chip. This bulky

C_I however consumes an extra I/O pin and requires large board area. To circumvent this problem, another solution would be reducing the charging current at node V_I . However, for a normal constant- g_m biasing circuit, the transconductance is directly linked to the value of the resistor. Therefore, in order to reduce this charging current to the level of nA, the resistor value is drastically boosted to a few tens of Mega Ohms which will consume quite a lot of area. In stead of implementing the large resistance with real resistors, the transistor in triode region can be cascaded to realize the large resistance. The left portion of the circuit in Fig 5.36 is meant for generating a nA-level biasing current for the soft-start purpose. When the EN signal sees a low to high transition, V_I is reset to zero. If transistor M_2 and M_3 are designed with the same width but β times longer length as compared to transistor M_1 , they will be operating in the triode region, the current in this branch can be expressed as:

$$I_{\text{Charge}} = \frac{1}{2}\mu_p C_{\text{ox}}\left(\frac{W}{L}\right)_1 (V_{\text{OV}} - 2V_{\text{DS2}})^2 = \frac{1}{2}\mu_p C_{\text{ox}}\left(\frac{W}{L}\right)_2 [2V_{\text{OV}}V_{\text{DS2}} - V_{\text{DS2}}^2] \quad (5.21)$$

Here the bulk of all the three PMOS transistor are tied to their source respective terminal, so that their threshold voltage are close to have a valid assumption that their overdrive voltages V_{OV} , which equal to $V_{\text{BAT}} - V_{\text{TH}}$ are more or less the same. Thus, M_2 and M_3 can be considered as one transistor with doubled length, and the drain-to-source voltages V_{DS1} and V_{DS2} can be summed as V_{DS} . The equation can be further simplified into:

$$2\beta = \frac{2V_{\text{OV}}V_{\text{DS}} - V_{\text{DS}}^2}{(V_{\text{OV}} - 2V_{\text{DS}})^2} \quad (5.22)$$

Which leads to:

$$V_{DS} = V_{OV} \pm \frac{1}{\sqrt{1+2\beta}} V_{OV}$$

Since $V_{DS} < V_{OV}$

$$V_{DS} = V_{OV} - \frac{1}{\sqrt{1+2\beta}} V_{OV} \quad (5.23)$$

Thus the charging current in this branch becomes:

$$I_{\text{Charge}} = \frac{1}{2} \mu_p C_{\text{ox}} \left(\frac{W}{L} \right) \left(\frac{1}{\sqrt{1+2\beta}} V_{OV} \right)^2 = \frac{1}{1+2\beta} I_{\text{Bias}} \quad (5.24)$$

For this design, the β factor is selected to be 20, thus given the biasing current equals to $1\mu\text{A}$, the charging current can be scaled down to around 20 nA. The hold capacitor C_1 can be implemented with a MIM capacitor which has a value of 3 pF only while still achieving more than 100 μs of rise time for the soft-start process. The inductor current peak value during the start-up process is limited within 500 mA.

5.4.7 Output Stage Design and Layout Consideration

The output stage of the buck converter comprises mainly of the two power transistors as well as the gate drive circuits. Serving as the connection between the pulsating control signal and the switching node of the inductor, the power output stage contributes most of the losses of a buck converter and also consumes a vast portion of the area dedicated for the chip. Therefore, although the structure remains relatively simple for the output stage, it still calls for careful design considerations in order to achieve better overall performance of the converter.

The design of the size of the power FETs has to consider both the conduction loss and switching loss which are the major losses associated with the power transistors. The conduction loss can be generally expressed as:

$$P_C = I_{\text{rms}}^2 \cdot R \quad (5.25)$$

where the I_{rms} is the root mean square (rms) current flowing through the power FETs and R is the conduction resistance of the transistor. During the corresponding conduction phases, the power transistors operate in the deep triode region which gives the expression of R as below:

$$R_{\text{P/N}} = \frac{1}{\mu_{\text{P/N}} C_{\text{OX}} \left(\frac{W}{L}\right) (V_{\text{GS}} - V_{\text{TH}})} = R_0 \cdot \frac{1}{W} \quad (5.26)$$

As power transistors are normally realized with the minimum channel length of the process technology for a smaller form factor, the effect of transistor geometric ratio on the channel resistance is more reflected by its width. Therefore in the above equation, the resistance is shown inverse proportional to the width with a constant parameter R_0 . For heavy load condition, the converter operates under the PWM scheme and the output stage rms current can be found as:

$$\begin{aligned} I_{\text{rms}}^2 &= I_{\text{rms}(\text{dc})}^2 + I_{\text{rms}(\text{ac})}^2 \\ &= D I_o^2 + D \cdot \frac{1}{3} \cdot \left(\frac{\Delta I}{2}\right)^2 \end{aligned} \quad (5.27)$$

Here D stands for the fraction that the ON time occupies for one duty cycle. I_o is the dc load current, and ΔI is the peak-to-peak ripple of inductor current. The gate-drive loss is a main contributor of the switching-based losses which results from the periodically raising and lowering of the gate voltage of a power FET. Assuming the gate capacitance increases proportionally with the area and hence the width of the transistor, the gate-drive loss can be expressed in the form [72]:

$$P_G = E_{g0} \cdot W \cdot f_s \quad (5.28)$$

where E_{g0} represents the total energy required for a low-high and high-low transition on the gate of a power FET with unit width. It can be found that the conduction loss is inverse proportional to the width while the switching loss increases linearly with width. By using the algebraic minimization [73], the optimal width of the power FET can be obtained as:

$$\begin{aligned}
 W_{\text{opt}} &= \sqrt{\frac{I_{\text{rms}}^2 \cdot R_0}{E_{g0} \cdot f_s}} \\
 &= \sqrt{\left(I_{\text{LOAD}}^2 + \frac{1}{12} \left(\frac{V_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \cdot f_s \cdot L}\right)^2\right) \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}}^3 \cdot f_s \cdot \mu_{\text{N,P}} \cdot C_{\text{OX}}^2}}
 \end{aligned} \tag{5.29}$$

which yields a minimum total loss with equal value for the conduction and switching losses. As the switching frequency f_s remains fixed under the PWM scheme, the optimal transistor width is proportional to the rms rating of the load current.

For PFM scheme, the inductor current operates in DCM. The calculation of the optimal transistor width will be slightly different as the inductor current is discontinuous. The inductor current waveform under the DCM condition is illustrated in Fig 5.37. Where I_{PEAK} and I_{LOAD} are the peak inductor current and the load current respectively. a and b stand for the gradient of the inductor current waveform. t_{ON} , t_{OFF} and t_{idle} are the switch on time for the PMOS switch, NMOS switch and inductor freewheeling switch respectively. In the PFM scheme, t_{ON} is a predefined value. As can be inferred from the figure, for a fixed output voltage, t_{idle} is dependent on the value of I_{LOAD} . Thus the switching frequency of the converter also becomes dependent of the load current. The switching frequency under DCM can be derived as:

$$f_{\text{DCM}} = \frac{1}{T_{\text{DCM}}} = \frac{2V_{\text{OUT}} \cdot L \cdot I_{\text{LOAD}}}{V_{\text{IN}}(V_{\text{IN}} - V_{\text{OUT}}) \cdot t_{\text{ON}}^2} \tag{5.30}$$

Hence, the conduction loss for the PMOS and NMOS transistor under DCM can be derived as:

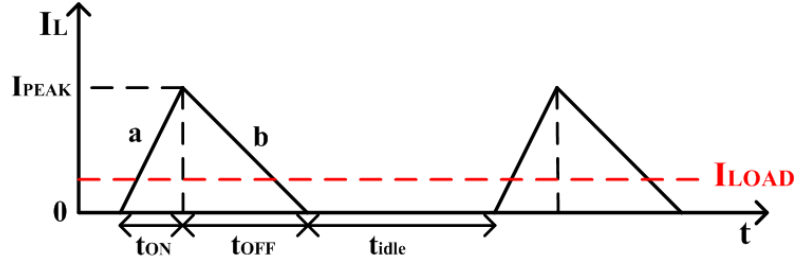


Figure 5.37: Inductor current waveform under the DCM for the PFM scheme

$$\begin{aligned}
 P_{C,P} &= \frac{1}{T_{DCM}} \int_0^{t_{ON}} (at)^2 \cdot (R_{0,P}/W) \cdot dt \\
 &= \frac{2}{3} \cdot \frac{V_{OUT}(V_{IN} - V_{OUT})(R_{0,P} \cdot W)I_{LOAD}t_{ON}}{V_{IN} \cdot L}
 \end{aligned} \tag{5.31}$$

$$\begin{aligned}
 P_{C,N} &= \frac{1}{T_{DCM}} \int_0^{t_{OFF}} (at_{ON} - bt)^2 \cdot (R_{0,N}/W) \cdot dt \\
 &= \frac{2}{3} \cdot \frac{(V_{IN} - V_{OUT})^2(R_{0,N} \cdot W)I_{LOAD}t_{ON}}{V_{IN} \cdot L}
 \end{aligned} \tag{5.32}$$

The gate-drive loss for DCM is frequency-dependent for both NMOS and PMOS transistor, and can be expressed as:

$$P_{G,DCM} = E_{g0} \cdot W \cdot f_{DCM} = V_{IN}^2 \cdot C_{OX}(W \cdot L)f_{DCM} \tag{5.33}$$

Again, by applying the algebraic minimization, the optimal width of the power transistor can be obtained by equating the gate-drive loss and the conduction loss for NMOS and PMOS separately:

$$W_{opt,P} = \sqrt{\frac{(V_{IN} - V_{OUT})^2}{3V_{IN}^2 \cdot (V_{IN} - V_{TH,P})} \cdot \frac{t_{ON}^3}{L^2 \cdot \mu \cdot C_{OX}^2}} \tag{5.34}$$

$$W_{\text{opt},N} = \sqrt{\frac{(V_{\text{IN}} - V_{\text{OUT}})^3}{3V_{\text{IN}}^2 \cdot V_{\text{OUT}} \cdot (V_{\text{IN}} - V_{\text{TH},N})} \cdot \frac{t_{\text{ON}}^3}{L^2 \cdot \mu \cdot C_{\text{OX}}^2}} \quad (5.35)$$

Since both the gate-drive loss and the conduction loss for DCM is dependent on load current, the optimal width expression has the load current term cancels out and is hence independent on the load condition. Which means for a given input and output voltage, the optimal width for DCM is fixed. Substitute in the process parameters into equations (5.34) and (5.35), the optimal width of the transistors for DCM can be calculated as: $(W/L)_P = 32982\mu\text{m}/0.5\mu\text{m}$, $(W/L)_N = 20364\mu\text{m}/0.7\mu\text{m}$.

The optimal width for CCM under PWM scheme is given in equation (5.29). For a load current of 50 mA, which is the load of class AB amplifier on the edge of mode transition, the resultant optimal width for PMOS transistor can be calculated as $39930\mu\text{m}$. However, this is the minimum load condition for the class AB amplifier working in the supply-tracking mode. With the output capacitor charging current included, the load current required from the buck converter will be much larger as depicted in Fig 5.30. Thus, if the transistor ratio is selected base on the optimal width in CCM, the size of the power transistor will be excessively large. For instance, when the load current is 200 mA and the buck output is 2V, the optimal width base on equation (5.29) will be as large as $150440\mu\text{m}$ which requires tremendous active area. Moreover, as mentioned in the introduction chapter, the audio signals are characterized with high PAR values which implies that for most of the time, the averaged amplitude of the signal is much smaller than its peak level. Therefore, it is not necessary to optimize the transistor size for the heavy load conditions which occurs infrequently. Instead, more effort should be added to improve the efficiency at DCM mode. Hence, the ratios for DCM optimization are used for the design of the power transistors. The on resistances of the two power transistors are also calculated as: $R_{\text{on},P} = 0.17\Omega$ and $R_{\text{on},N} = 0.103\Omega$. The average on resistance is around 0.135Ω which also meet the design rule of thumb that the conduction loss is below 1% of the load resistance.

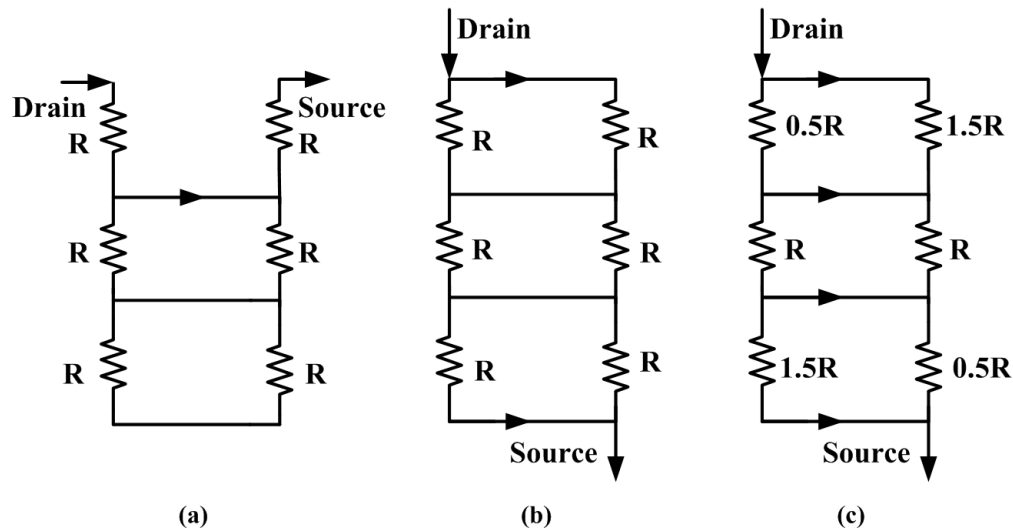


Figure 5.38: Equivalent circuit models of different power transistor layout

The size of the power transistors are so large that they have to be partitioned into an array of multiple parallel fingers for a compact layout design. Besides, as the power transistor carries large amount of current from one terminal to the other, the resistance as well as current distribution along the conduction path must be scrutinized. The on resistance of a power transistor includes not only the channel resistance but also the resistances of the interconnects like the equivalent resistance of the metal path and the vias across different metal layers. Fig 5.38 depicts the equivalent circuit model of several commonly-used layout structures for the power transistor. The illustration is simplified into several fingers, schematic (a) on the left shows the model of the multi-finger layout where the drain and source terminals are tapped from the same direction. The horizontal lines represents the channel resistances of each single transistor.

The problem for the first solution is the unbalanced current distribution among different finger transistors. As shown in the figure, the upper most channel sees the least of the interconnect resistances, thus this path is likely to carry most of the current flowing through the power transistor while the bottom paths are bypassed. Although the current driving capability is evenly distributed among the array of transistor fingers, the actual current does

not have a balanced distribution as expected. This give rise to reliability problem of the power transistor. As huge current is flowing in the upper path, hot spot can be detected close to the drain and source terminals. Hence the actual current driving capability of the power transistor is limited. The second solution as shown in schematic (b) alters the tap point of the source terminal, as a result the resistances seen from the top and bottom paths are equalized. Thus, the current instead of swarming into one path is split into two different paths. At the same time, the two hot spots at the drain and source terminals are separated which substantially cancels the thermal effects on the transistors. However, as the interconnection resistances are uniformly distributed, the current flowing in the transistors among the central area is still very small, which results in high current density in the outer paths. Compared to solution (a), the layout in (b) relaxes the situation a bit but the multi-finger structure is still not fully utilized. Solution (c) alters the interconnection resistances according to the current level. On the drain side, the interconnection resistance increases linearly as the current gradually branch out through different finger transistors. Whereas on the source side, the resistances decrease linearly as more current is to be collected from different paths. Therefore, the total current is distributed much more evenly among different branches, and thus the reliability of the power transistor is greatly improved in the sense that the current density of each individual component is much reduced. Compare the structure (b) and (c) we can observe that structure (c) is an improved method considering the interconnect resistance which are basically those resistors in the vertical direction. The idea behind structure (c) is that in order to have an evenly distributed current profile, the interconnect resistance along the current distribution path should be in linearly increased manner. Since the current at the beginning is the sum of all branches and is largest, it should see a gradually increasing resistance as the current branch out along the path.

In order to realize the linearly changed interconnection resistances along the current path, the width of the metal routing which carries the current must be changed adaptively. As the resistance of the metal routing is inverse proportional to its width, it results a

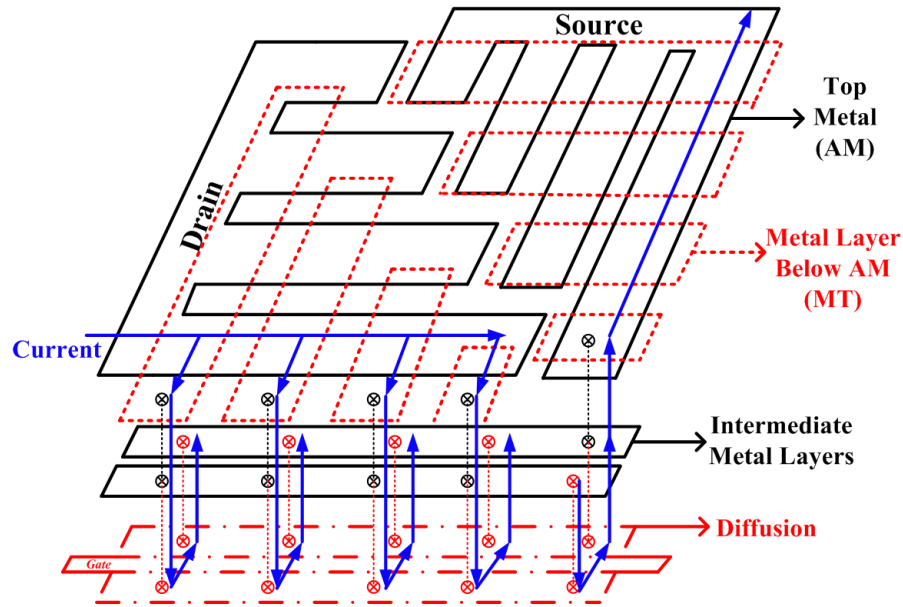


Figure 5.39: Proposed layout structure for the power transistors used in the buck converter

triangular shaped layout topology, which is also referred as the tapered layout structure. In real layout implementation, the triangular shaped layout is not allowed as there exist requirement on the maximum metal density for a certain area. In Fig 5.39, the layout for the power transistor used in this design is illustrated.

In this implementation, the tapered structure is realized with metal strips with decreasing length. The strips by the top metal (AM) and the layer just below AM (MT) are placed in a perpendicular manner so that the two metal layers form a mesh which minimizes the contact resistance. This results in a staircase-like layout pattern when looking from the top. For a compact layout design, the distance between each metal strip is set to be just larger than the minimum distance required by the layout design rules. The intermediate layers consist of several metal layers in this design. For a simple illustration, only one layer is shown in the figure. The circled cross symbol stands for the via between each two metal layers. For the vias between the intermediate layer and MT, the vias are build only for the area that is covered by the above AM layer. For example, the 4 vias in black are the vias

made between intermediate layer and MT for the longest AM strip on the drain side. The 4 vias are for illustration only, and in real implementation the number of vias are maximized for the area under AM strip to reduce the interconnect resistance. For vias and contacts from the intermediate layer all the way down to the diffusion region of the transistor, the vias are build for the full length of the power transistor to minimize the contact resistance. Take the current flowing in the longest AM strip as an example, the direction of the current is drawn in blue arrows. The current will split for different MT strips and flow downward through the vias, after passing through the channel, the current will be gathered at the source side. Due to the complementary staircase-like shape of the two meshes, the MT strip for the source side will be the shortest, hence the number of vias for the source side from the intermediate layer to MT will be minimal. This structure embodies the concept of a linearly shifted interconnect resistance from the drain to the source terminal. Thus, a more evenly distributed current profile can be acquired for the power transistor which greatly enhances the robustness of this power device.

Another benefit of the proposed layout structure is the 90° angle between the current flow-in and flow-out directions. Thus, the power transistor can be placed at the corner of a die, so that the I/O pads can be directly connected to the AM metal connecting to the drain and source without using additional metal routing. Therefore, the interconnect resistance is further reduced. For the PMOS finger transistors, a $18\text{ }\mu\text{m}$ wide transistor with 10 fingers are defined as a unit cell. The power transistor is built up with a 14×13 array of the unit cell and has an equivalent ratio of $32760\text{ }\mu\text{m}/0.5\text{ }\mu\text{m}$, which is close to the calculated optimal width. Similarly, the NMOS is realized with an array of 10×11 of $18.5\text{ }\mu\text{m}$ wide transistors with 10 fingers which has an equivalent ratio of $20350\text{ }\mu\text{m}/0.7\text{ }\mu\text{m}$. The array is defined in such a manner that the shape of the power transistor is close to a square, so that equal number of I/O pads can be assigned to the drain and source terminals respectively.

Since the power transistors are designed with extremely large form factors, large capacitances are associated with the gate terminal of the transistor. Hence, driver circuit is

required to ensure the expected rise and fall time of the gate control signals. For conventional designs, the power transistor is driven by a inverter chain which has a constant tapering factor u . The tapering factor u is designed such that [72]

$$u^N = \frac{C_g}{C_i} \quad (5.36)$$

where N is the number of stages for the inverter chain, C_g and C_i are the gate capacitance of the power transistor and the first buffer stage respectively. According to the literature [73], the minimum propagation delay can be obtain with the tapering factor equals to e , which is around 2.718. However, such small value of the scaling factor results in too many stages of the inverter, which not only increases the area consumption but also the switching loss resulting from the shoot-through current. Besides, the top concern of a power management unit usually lies on the power efficiency and reliability instead of the minimum propagation delay. Therefore, the number of inverter stages is capped to 4 and the ratio from the first buffer to the power transistor is set to be 1:6:60:900:30000. Due to the short period when both transistors are not completely off, there will be a large burst of short-circuit current flowing from the the supply to the ground. As the size of the buffer stage increases, this so-called shoot-through current cannot be ignored when considering the switching loss of the system. In this design, the inverter chain with built-in dead-time is used to suppress the switching loss due to shoot-through current [74]. The schematic as well as the timing diagram of the gate driver is depicted in Fig 5.40.

The main objective for introducing dead-time is to reduce the short-circuit current resulting from the overlapped conduction zone of the PMOS and NMOS transistors. Due to the tapering factor, the major contribution of the shoot-through current is by the last two stages of the inverter chain. Therefore, the purpose of the circuit in Fig 5.40 is trying to create a dead-time zone for the last stage buffer which consists of transistors M_1 and M_2 . Instead of connecting the output of the third inverter to gate terminal of both M_1 and M_2 .

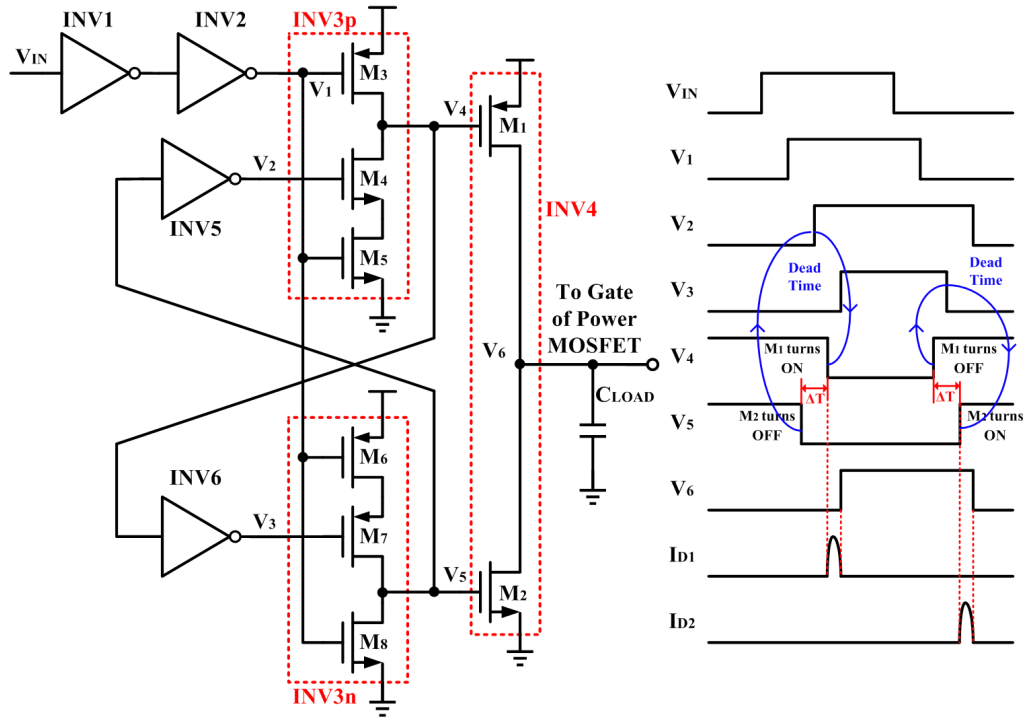


Figure 5.40: Gate driver circuit with build-in dead time buffer and its timing diagram

The gate control signal to the last stage is split into V_4 and V_5 respectively. Additional feedback loop is used to create a delay time for both the rising and falling edge of the control signal V_1 , so that the last stage transistors will not be conducting at the same time and hence eliminates the switching loss due to shoot-through current. The introduced dead-time can be controlled by properly adjusting the propagation delay time within the feedback loop, which can be done by limiting the charging or discharging current of inverter INV5 and INV6.

Chapter 6

Measurement Results and Discussions

6.1 Chip Fabrication and Testing Setup

A prototype of the proposed class H audio amplifier is realized and fabricated with the AMS 0.18- μm standard CMOS technology. The whole design including the power transistors and all the I/O pads occupies an area of 1.35 mm $\times$ 1.32 mm. The micrograph of the chip is depicted in Fig 6.1. The die is packaged in the 48-pin DIP package for measurements. The PCB board designed for testing is shown as in Fig 6.2.

The PCB is implemented with 4-layer structure with the second and third layers assign for the power and the ground plane, respectively. For the audio load, a 16- Ω resistor in parallel with 200-pF capacitive load is used. The passive components used for the buck converter are a 2.2- μH power inductor and a 2.2- μF ceramic capacitor. The basic testing setup follows the instruction as in the technical report for testing of a class AB audio amplifier [75]. The input signals are generated from the signal generator and the whole PCB is supplied by one dc power supply which has a nominal value of 3.3. The amplified signals are analyzed by the Stanford Research System SR1 Audio Analyzer, at the same time, they are also probed to be displayed by the oscilloscope. Therefore, the actual capacitive

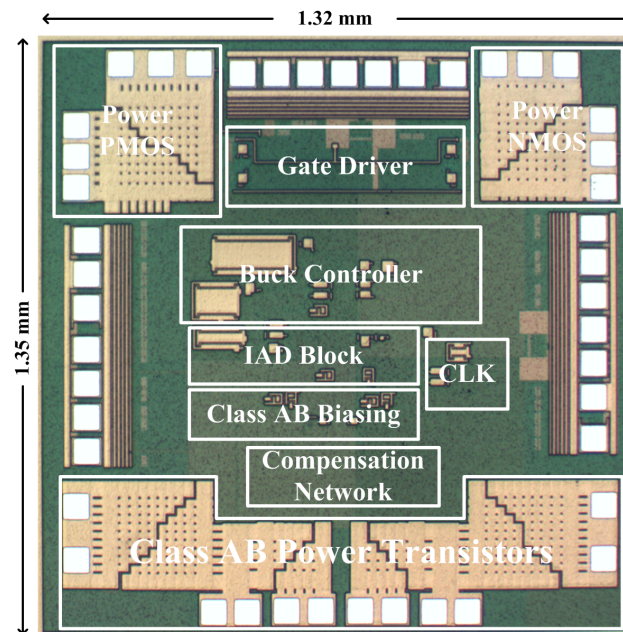


Figure 6.1: Chip micrograph of the proposed class H audio amplifier

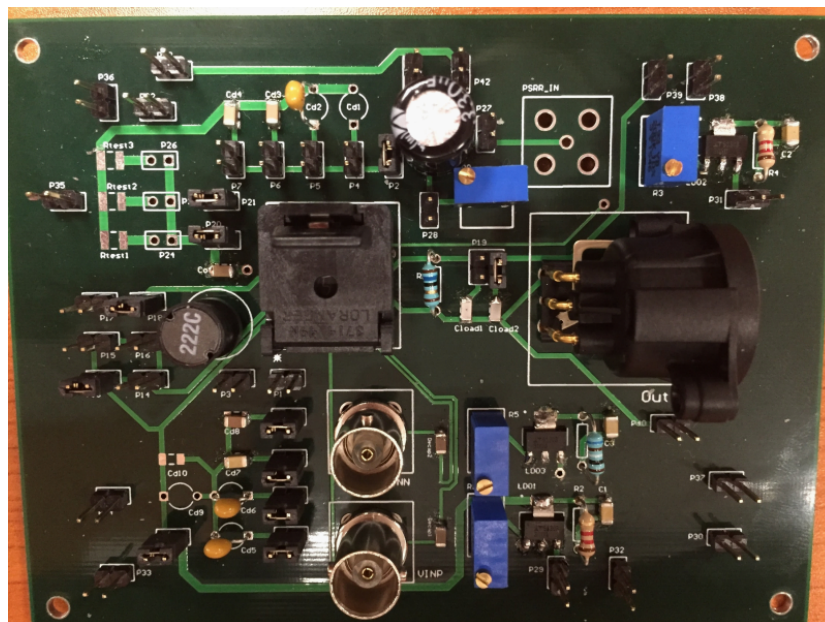


Figure 6.2: PCB designed for measurement of the chip

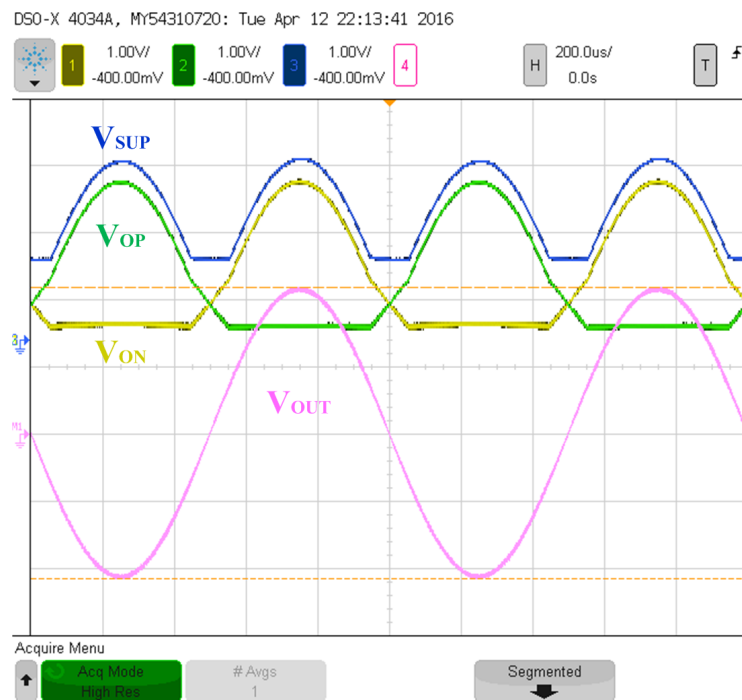
load driven by the audio amplifier should be larger than 200-pF which satisfies most of the headphone applications on the market.

For quiescent power testing, the input ac signal from the signal generator is grounded. The quiescent current will be monitored by the dc current rating of the dc power supply. For testing of the linearity performance, the amplitude and frequency of the input ac signal will be swept, the waveform will be captured by the oscilloscope and the distortion as well as noise will be analyzed by the Audio Analyzer. The efficiency can also be obtained the same time while testing the transient performance. The dc current rating of the power supply times the supply voltage will give the total power consumption of the system which includes all types of losses within the system. For testing of supply noise rejection, the input of the class AB amplifier will be grounded. The signal generator will generate an ac signal with relatively large amplitude, and this ac signal will be coupled to the dc supply to create a "noisy" power source. The differential output of the class H amplifier will be analyzed by the Audio Analyzer to obtain the value of PSRR.

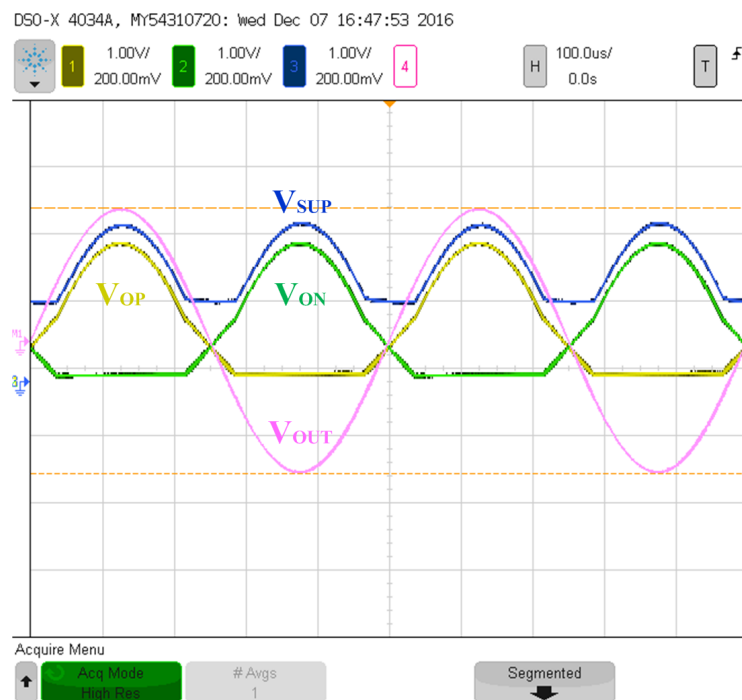
6.2 Measurement Results

The measurements were conducted on 15 chip samples. The averaged quiescent current consumption is 1.07 mA, which leads to a total quiescent power of 3.52 mW under a 3.3 V power supply. For transient testing, a pair of sinusoidal waves which are 180° out of phase generated from the signal generator are used as the input ac signals. To justify the amplifier's capability for driving audio signals, its supply-tracking performance is tested at different input frequencies. Fig 6.3 and Fig 6.4 plot the screen captures of the output waveforms at medium frequencies as well as higher frequencies. The output power delivered to the load is kept the same as 151 mW which is equivalent to a peak-to-peak output swing of 4.4 V across the 16-Ω load.

As can be observed from the figures, when the input frequency is low, the buck converter

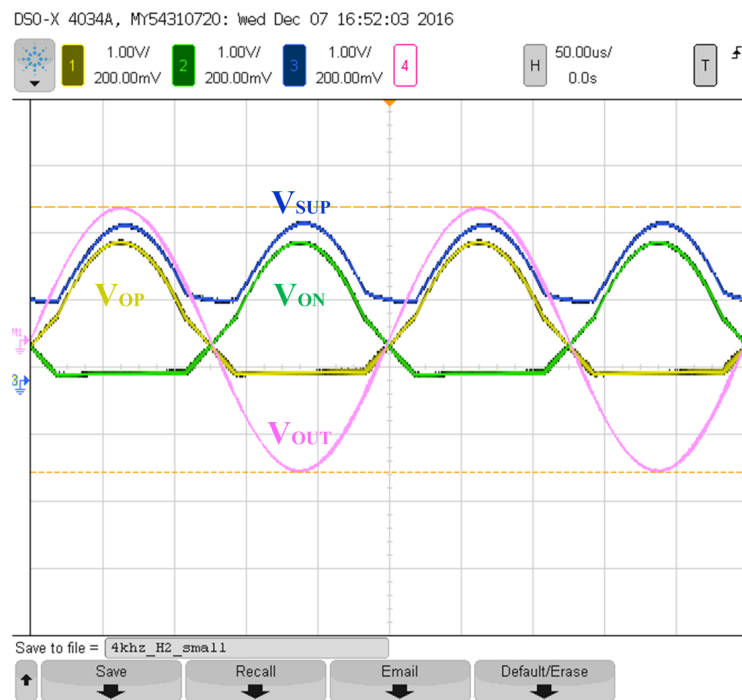


(a)

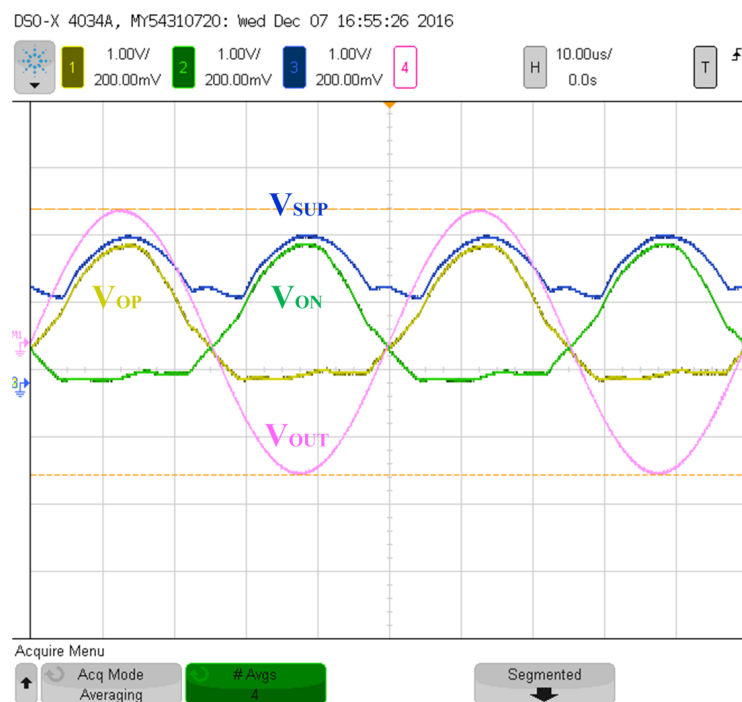


(b)

Figure 6.3: Measured output waveforms at 151 mW output power (4.4 V peak-to-peak output swing) with sine input at medium frequencies (a) 1 kHz, (b) 2 kHz



(a)

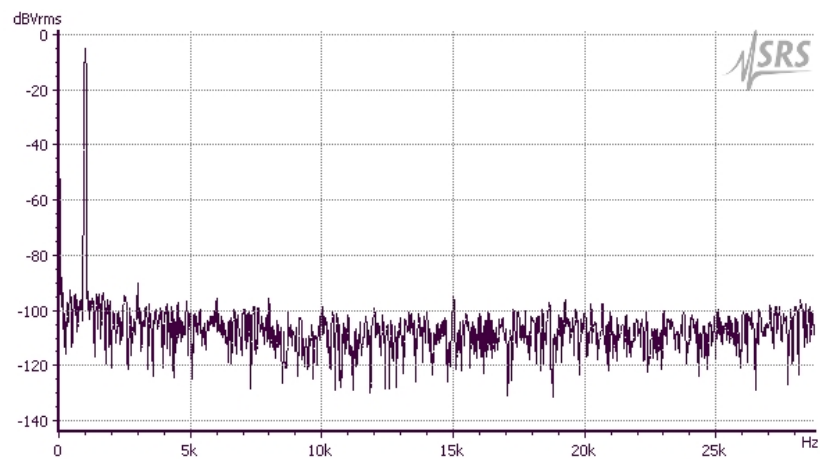


(b)

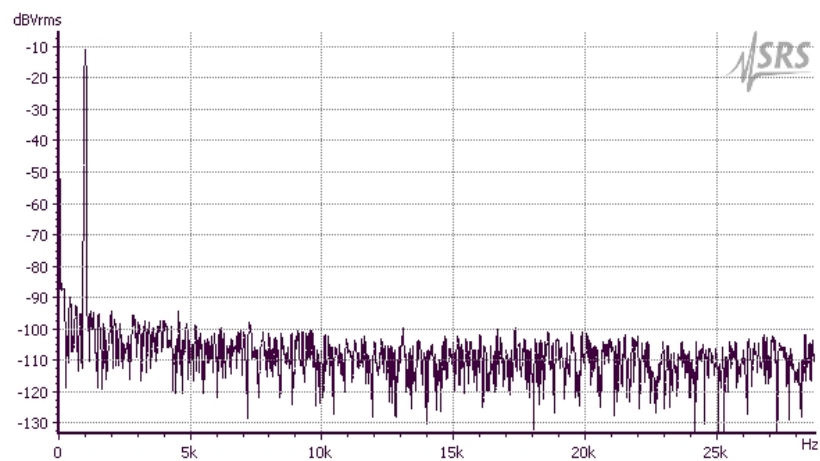
Figure 6.4: Measured output waveforms at 151 mW output power (4.4 V peak-to-peak output swing) with sine input at higher frequencies (a) 4 kHz, (b) 20 kHz

output V_{SUP} is able to closely track the amplitude of the input signal. As the input frequency increase, the phase shift between the reference signal generated from the IAD block and the class AB outputs also becomes larger. This leads to the buck converter output lags behind the realtime input signals. As a result, the headroom voltage left across the power transistor is further squeezed. When the input frequency increases further to 20 kHz, not only the phase difference between the two types of signals but also the response time of the buck converter become the limiting factors for the supply-tracking performance. The above issue due to the mismatch of latency between the fine gain and coarse gain paths justifies the analysis in Chapter 4. Although there exists mismatch between the coarse gain and the fine gain paths, the differential output which is the one driving the load is not affected. The reference feedforward technique speed up the converter's response to a reference voltage transient. With a predefined headroom voltage of 200 mV designed for the power transistor, no waveform clipping is observed throughout the audio frequency band. Therefore, the reference-tracking capability of the amplifier is validated for audio applications.

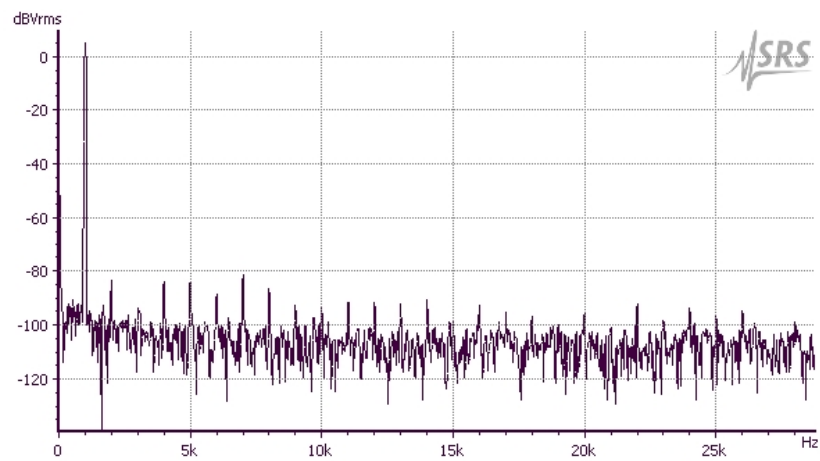
The linearity performance of the amplifier can be quantized by the THD+N ratio. Fig 6.5 (a) shows the spectrum of the amplifier working in class AB mode which delivers an output power of 5 mW to the load when the input frequency is 1 kHz. Under this condition, the converter output stays at a fixed value of 1.2 V as the V_{DDL} , and the measured THD+N ratio is -73 dB. Fig 6.5 (b) shows the spectrum when the output power is around 25 mW, under this load condition, the class H is just triggered and the measured THD+N is -78 dB. Fig 6.5 (c) shows the output spectrum when the output power is 180 mW, the lowest THD+N value is measured as -82 dB. The THD+N ratio over the output power plot of the proposed design is depicted and compared with the benchmark work on the single-rail supply class H amplifier [22]. It can be observed from the figure that for the benchmark design, the THD+N ratio incurs a sharp degradation from 0.01% to 0.05% when the class H supply-tracking mode is activated. The added distortion is mainly due to the switching scheme proposed in that work where the nonlinearity of the analog switches as well as the



(a)



(b)



(c)

Figure 6.5: Spectrum of the differential output at 1kHz for (a) class AB mode with 5 mW output power, (b) class H mode with 25 mW output power and (c) class H mode with 180 mW output power

resistor dividers substantially affect the linearity of the system. Therefore, for the whole class H operating region, as the output power increases the THD+N value hovers around 0.06% until waveform clips. In other words, the benchmark design demonstrated good linearity performance for a class AB amplifier design, while the high linearity is not preserved for class H mode operation. For our proposed design, the output common mode voltage is modulated to enable the supply-tracking operation. As its CM voltage is cancelled out in view of the differential output voltage, no additional distortion is generated during the transition between the two operation modes. Therefore, the THD+N ratio gradually ramps down as in a conventional class AB design. It remains below the value of 0.02% for the class H mode until the output power increases to the level where waveform clipping sets in. Hence, it is validated that the proposed class H amplifier design achieves better linearity performance for the entire load range.

Linearity performance of the class H amplifier at higher frequency range are also tested.

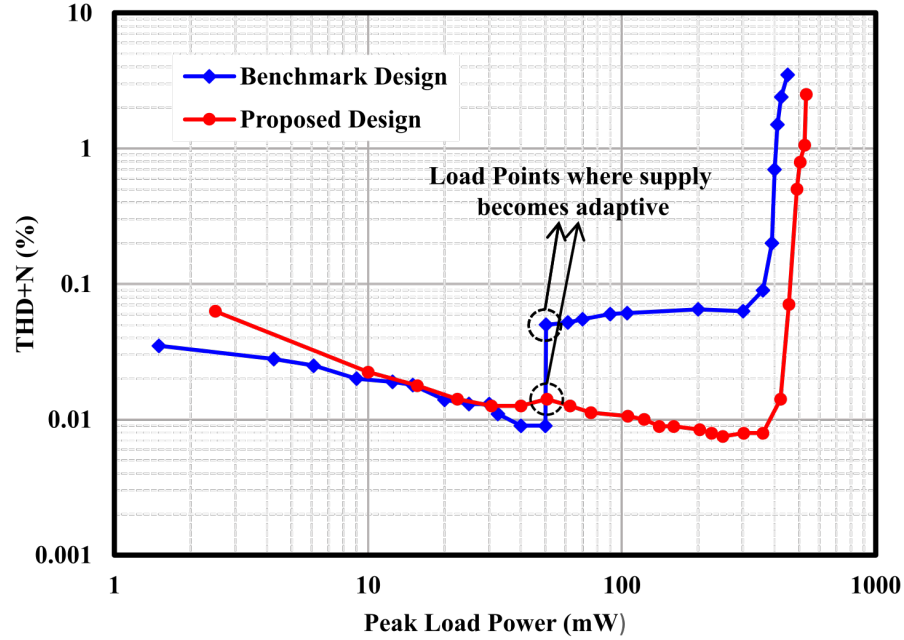


Figure 6.6: Comparison of the THD+N ratio at 1 kHz between the proposed design and the benchmark work

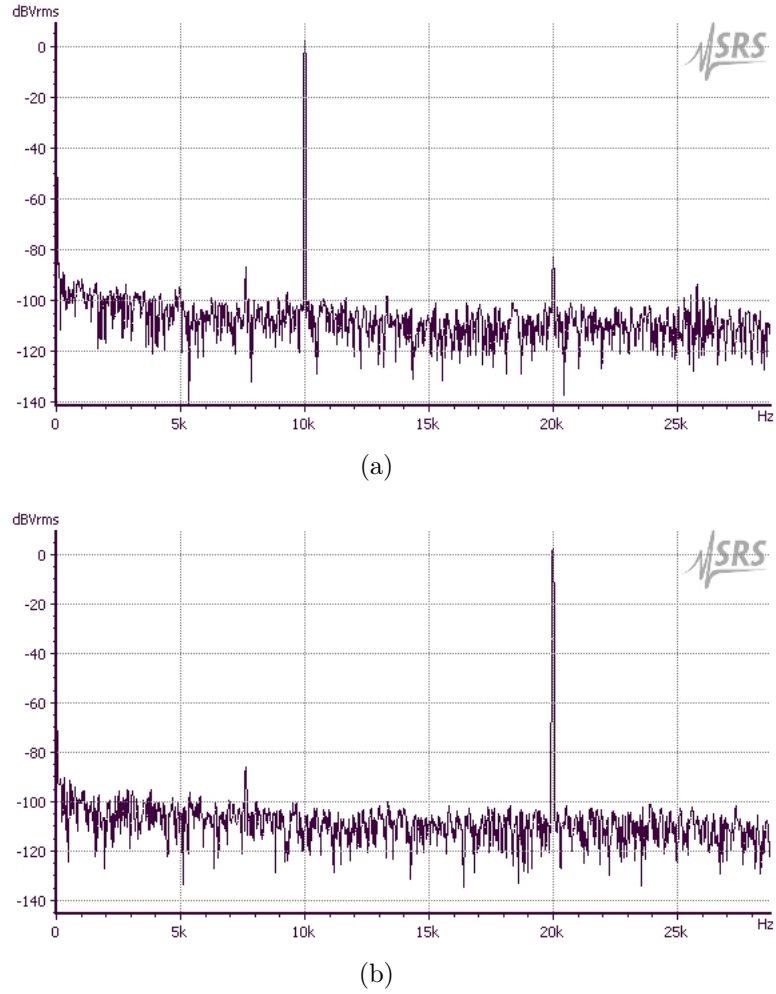


Figure 6.7: Output spectrum for class H mode operation with input frequency of (a) 10 kHz. (2) 20 kHz

Fig 6.7 (a) and (b) depict the output spectrum of the amplifier when amplifying single tone input signals with frequencies of 10 kHz and 20 kHz respectively. The output power is fixed to 151.25 mW which is equivalent to a peak load power of 302.5 mW. The differential output swing is 4.4 V_{pp}, and the system is operating under the class H mode. The measured THD+N ratio for with 10 kHz and 20 kHz input are -79 dB and -80.4 dB respectively.

The PSRR is tested for audio frequency range, the testing setup is shown in Fig 6.8. For PSRR testing, the ac input signals are connected to the ground. The amplifier output

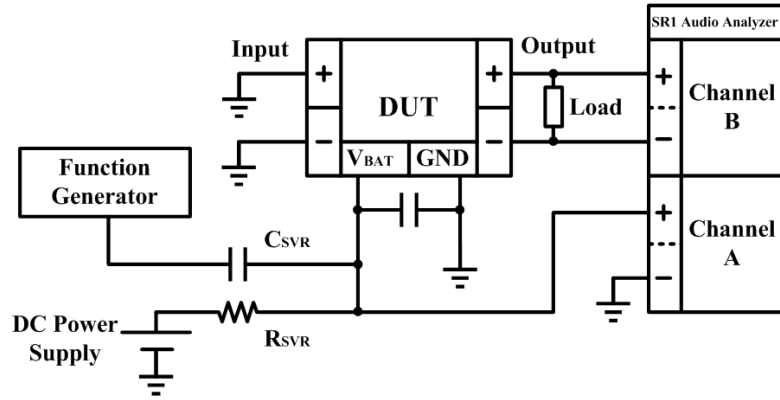
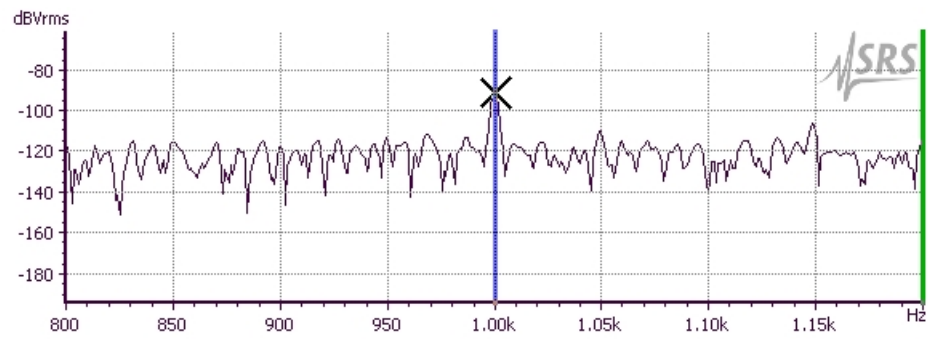
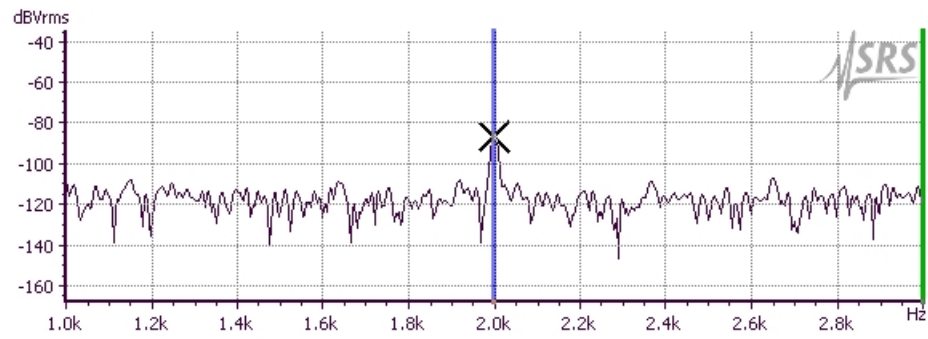


Figure 6.8: Testing setup for PSRR measurement

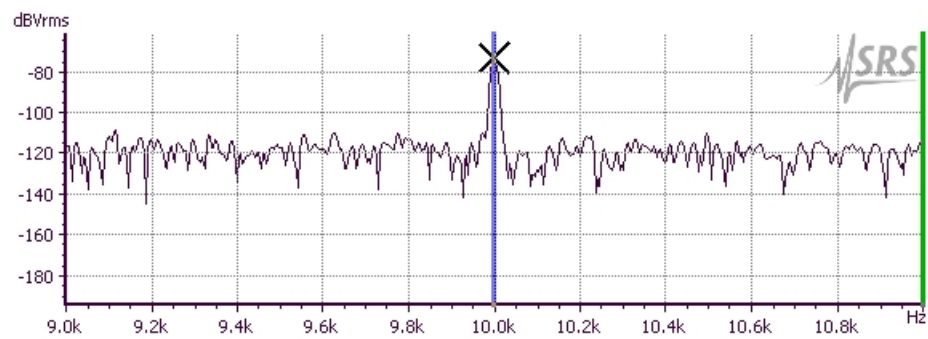
is connected to one channel of the audio analyzer. The noise is generated from the function generator and is directly coupled to the dc power supply. The dc power supply is usually designed with low output impedance, while the input impedance seen into the power pin of the audio amplifier is relatively large. Hence, when viewed from the supply node, it is the two resistors in parallel which is dominated by the much smaller power supply impedance in the milli-ohm range. At the same time, the function generator itself also has internal resistance in terms of few tens of ohms [75]. Therefore, the ac signal coming out of the function generator will almost see the supply node as an ac ground. In order to keep the ac signal amplitude at the supply node to a reasonable level, substantial value of resistance R_{SVR} must be added to create a voltage divider circuit from the function generator to the supply node. In this case, the value of the R_{SVR} is selected to be around the same value of the generator internal resistance which is 20 ohms. The R_{SVR} in series with the amplifier is only used for PSRR measurement, otherwise it incur voltage drop seen from the supply to the output. For quiescent state, the voltage drop across this resistor is still acceptable. While for transient testing, this compensator network will be bypassed to save power. The C_{SVR} is the ac coupling capacitor which serves as a high-pass filter to inject the ac signal into the amplifier's supply node. The corner frequency should be lower than the lower boundary of the audio signal band which is around 20 Hz. Based on this value, the value of the capacitor



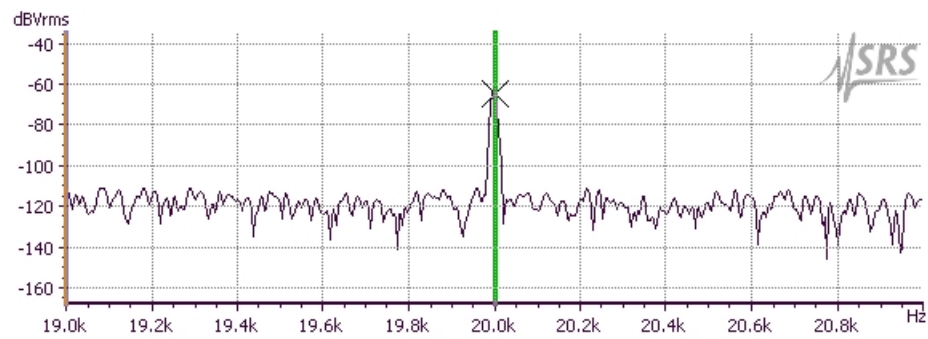
(a)



(b)



(c)



(d)

Figure 6.9: Output spectrum of PSRR testing at different frequencies (a) 1 kHz (b) 2 kHz (c) 10 kHz (d) 20 kHz

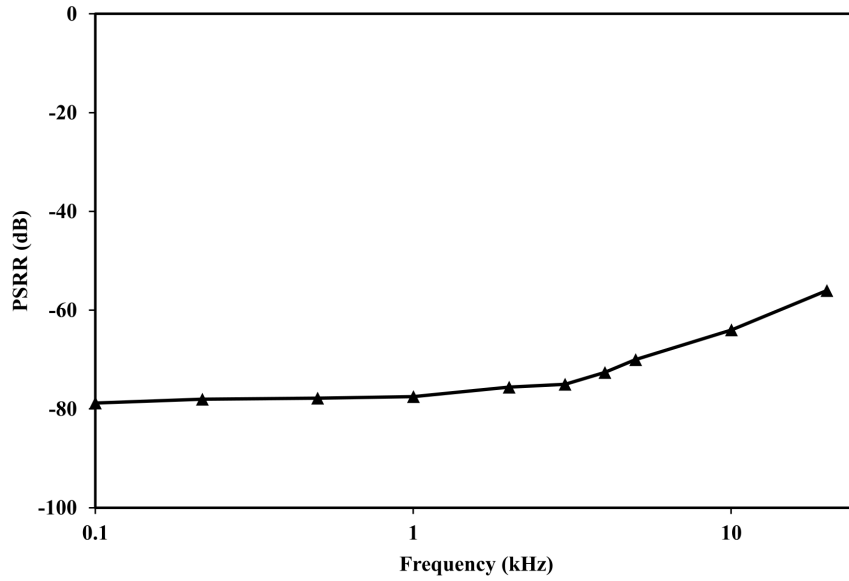


Figure 6.10: Measured PSRR of the amplifier for audio signal band

can be calculated subsequently as $201 \mu\text{F}$. This ac coupling capacitor is finally realized with an $220 \mu\text{F}$ electrolytic on the PCB. The ac signal level will be sensed by the audio analyzer using another channel. The difference in dB between the input (the supply node) and the output (the differential output of the amplifier) will be exactly the PSRR.

The amplitude of the ac signal is kept constant at 500 mV, with the voltage divider effect of the ac coupling filter, the amplitude captured at the supply node side is around 250 mV. The input ac signal frequency is swept from 20 Hz to 20 kHz for audio band. The spectrum of the amplifier differential output signal is shown in Fig 6.9 for different frequencies, and the PSRR plot is plotted in Fig 6.10 based on the collected data. It can be seen that the PSRR of the amplifier remains below -60 dB for the whole audio signal band.

Fig 6.11 plots the efficiency of the proposed design with sinusoidal input at different frequencies as well as analytical values for other types of linear amplifiers. The maximum output power is defined as the output condition where the THD+N ratio increases to 1%. The peak power efficiency is measured at the maximum output power of 263 mW which corresponds to a peak load power of 526 mW and 5.8 V_{pp} output swing. The efficiency

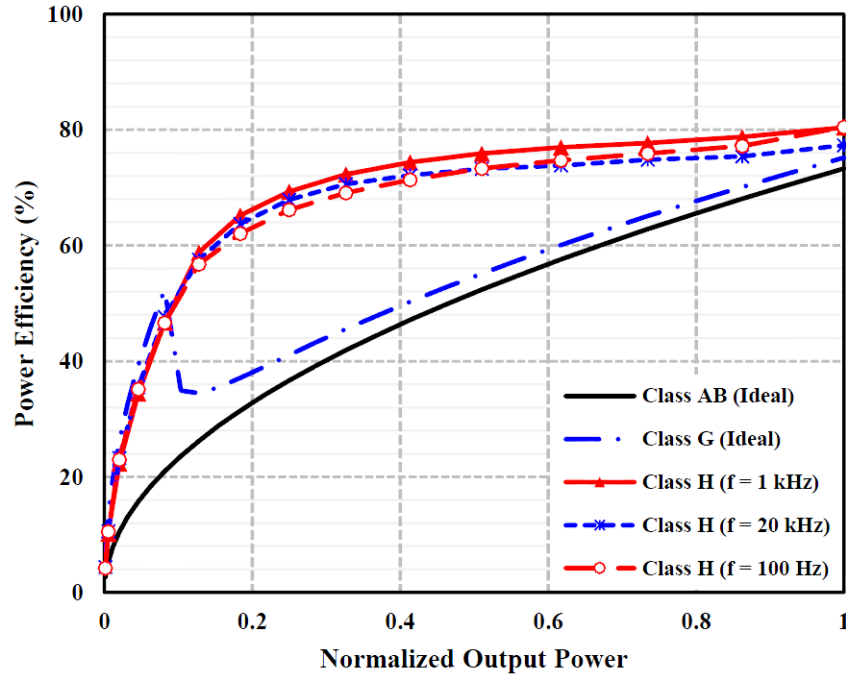


Figure 6.11: Measured power efficiency of the proposed class H amplifier at different input frequencies compared with analytical values of class AB and G amplifiers

measured is the system efficiency which has considered all kinds of losses in the system including the power conversion loss, static power consumption of all control circuits, and so on. Compared to class AB and G amplifiers, the proposed work achieves more than 25% improvement on efficiency during medium load range. This advantage will become even significant when the input signal exhibits high peak-to-average ratio like real audio signals.

The measured performance of the proposed class H amplifier is summarized and compared with both previously reported papers as well as commercial products in Tables II and III, respectively. From the tables, it can be seen that the proposed design features the highest peak power efficiency among all amplifiers. Compared with the benchmark class H amplifier in [22], the proposed design solves the nonlinearity injection problem encountered in class H mode operation. Meanwhile it attains a much lower quiescent power consumption and smaller area due to the reduced system complexity. For applications in mobile devices where single-rail supply is preferable, the proposed design demonstrates an optimal linear

amplifier solution with good balance among power efficiency, linearity, and cost.

Table 6.1: Performance comparison with recent works on linear amplifiers

References	[19]	[20]	[34]	[28]	[4]	[36]	[22]	This Work
Classification	AB	AB	G	G	G	G	H	H
Process(nm)	130	500	65	180	180	350	180	180
Single/Dual-rail Supply	Dual	Dual	Dual	Dual	Dual	Single	Single	Single
Supply Voltage(V)	± 1	± 1.5	$\pm 1.4/\pm 3.5$	± 1.5	N/A	1.8/3.6	1.4-3.1	1.2-3
Maximal Output Power $P_{out}(mW)$ @ THD+N = 1%	20	47	45	62	60	518	205	263
THD+N @ 1kHz A-weighted (dB)	-84	-77.9	-80	-95	-95	-73.5	-66	-82
Quiescent Power (mW)	1.2	1.43	0.41	1.65	3.05	18	9.9	3.52
Load (Ω)	16	16	32	16	16	8	8	16
Peak Power Efficiency (%)	62.8	N/A	70	N/A	N/A	67.2	80	80.4
Area (mm^2)	0.1	0.34	0.14	2.4	2.37	N/A	2.55	1.74
PQPR(Peak-to-quiescent Power Ratio) F.O.M	16.7	32.9	109.8	37.6	19.7	28.8	20.7	72.5

Table 6.2: Performance comparison with recent products on class G/H amplifiers

References	TS4621 Class-G [76]	TPA6140 Class-G [77]	LM48824 Class-G [78]	LM48580 Class-H with boost converter [79]	This Work
Supply Voltage(V)	2.3-4.8	2.5-5.5	2.4-5.5	2.5-5.5	3.3-4.2
Output Swing(V_{RMS}) THD+N $\leq 1\%$	0.77	0.91	0.8	7.8 (THD+N = 5%)	2.05
Quiescent Current(mA)	0.6	1.2	0.9	2.7	1.1
THD+N @ 1kHz (dB)	-84.4	-74	-66	-56	-82
THD+N @ 20kHz (dB)	-66	-81	-80	>-40	-80
PSRR @ 217Hz (dB)	100	100	94	75	77.5

Chapter 7

Conclusions

The focus of this thesis is on the analysis and design of a class H amplifier with the load-adaptive supply for audio applications. It provides an optimal linear amplifier solution incorporating both high linearity and high power efficiency. In this chapter, conclusions are drawn for the content presented in this thesis and recommendations for future work will be given.

7.1 Conclusions

The main objective of the Ph.D. research program is related to the analysis and design of a supply-tracking class H audio amplifier for mobile devices. In Chapter 1, the trade-offs between the linear amplifier and the switching amplifier are analyzed, and the motivations and objectives of this research project were described in detail.

In Chapter 2, a comprehensive literature survey on the linear mode audio power amplifier is unfolded. The literature review started with the audio signal characterization and is followed by the performance metrics of audio power amplifiers. Subsequently, the paramount

portion within a linear audio amplifier, the power output stage, is deeply reviewed for different topologies. More specifically, the class AB output stage being the most popular output topology in recent designs, is analyzed with the state-of-the-art design examples. Insights to their novelty as well as the limitations are provided.

In Chapter 3, The defect of class AB power amplifier in terms of power efficiency was analyzed and hence introduced the concept of linear power amplifiers with adaptive power supplies. The two embodiments of this concept, the class G and class H amplifier, are delineated with the design examples from the recently reported works. The derivation of class G amplifier power efficiency was offered to justify the feasibility of further improvements on efficiency with the class H topology. In the rest of this chapter, the previously reported class H amplifier architecture is illustrated which represents the state-of-the-art of the class H topology. However, this design is incapable to be used as a high fidelity audio driver in the sense that its linearity is severely degraded due to additional distortions introduced during switching of modes.

In Chapter 4, our proposed class H amplifier architecture was delineated. In the proposed design, the amplitude information of the input signals is embedded into the output CM voltage of the main amplifier. Thus, the single-rail supply class H operation is enabled without constant alterations of the system architecture. Better linearity performance is hence achieved compared to the previous design. The PSRR as well as the effect of the latency mismatch between the two different signal paths were also analyzed which gives design directions for the IC implementations.

In Chapter 5, the IC implementations of the proposed class H amplifier architecture were delineated. The system consists of three building blocks, the fully-differential class AB amplifier with modulated output CM level, the Input Amplitude Detection (IAD) block and the reference-tracking buck converter. The design analysis of each block is provided which includes the fundamental analysis like the dc and ac stability analysis, as well as specific concerns for it to be deployed within the class H system. A novel control algorithm was also

proposed for the buck converter to optimize its power efficiency under light load conditions.

In Chapter 6, the performance of the proposed work was validated with the measurement results based on the fabricated chips. The prototype of the class H amplifier was realized with a 0.18- μm CMOS technology. The collected data reveals that the proposed design achieves a quiescent power of 3.52 mW under a 3.3 V power supply and its peak power efficiency is acquired at its maximum load power of 263 mW as 80.4%. Compared with the benchmark class H amplifier [22], the proposed work does not incur a sharp degradation on THD+N ratio when the system operates under the supply-tracking mode, instead its high linearity is kept for the entire load range and achieves a minimum THD+N ratio of -80.5 dB. Hence, the superiority of the proposed architecture in terms of high linearity is justified.

In summary, this Ph.D. research project has contributed significantly upon the analysis and design of the class H supply-tracking audio amplifier. It improves the low linearity of the previous work to a level that is suitable for high-fidelity audio applications, meanwhile it provides an optimal linear amplifier solution with good balance among power efficiency, linearity and cost. However, we have also met some of the problems that limit the performance of this class H amplifier. This includes the limited PSRR, finite reference-tracking capability of the dc-dc buck converter, circuit reliability and so forth. In other words, there is still much space for the improvement work, and hence we list the shortcomings as well as possible areas for improvement in the next section of this chapter for readers to consider.

7.2 Recommendations for Future Work

The possible future working directions pertained specifically to this topic include:

First, further improvement on PSRR. On the basis of the literature review and the

experimental results it can be seen that the PSRR performance is not as good as the state-of-the-art designs in class AB or Class G amplifiers. As analyzed in Chapter 4, the fully-differential topology does not necessarily guarantee good PSRR performance. This is because the perfect matching of all the components including the transistors and resistors are not achievable in real circuit implementation. Thus, it is not possible to acquire excellent supply noise rejection through the differential topology. Therefore, the first recommendation for future work is on the improvement of PSRR with additional circuit techniques. As the supply noise for a class H amplifier is injected mainly from the last stage, it is intuitive to design the additional circuitry for supply noise cancelation. Besides, some external trimming networks can be added to correct the error due to mismatch of passive components like the feedback resistors.

Secondly, the realization with smaller input supply voltage and a boost converter. As described in this thesis, the adaptive power supply unit is realized with a buck converter with 3.3 V battery voltage as input. For modern low voltage designs, the supply voltage keeps on scaling with the process technology. In this case, a boost converter can be used instead of the buck converter for the supply unit, such that the output voltage range of the converter will not be constrained by the limited input supply voltage. As a result, the class H amplifier could have an even larger output power range which renders it suitable for a variety of applications.

Thirdly, the investigations into the control scheme of the power converter. PWM control scheme incorporating PFM scheme at light load condition was adopted in this design. The PWM scheme was selected for its constant switching frequency so that it is for sure that the spectrum of the switching regulator will not interfere with the audio signal band. However, for recent papers on hysteretic controlled dc-dc converters, it is also possible that the switching frequency of the converter is controllable or predictable to a reference frequency [80]. Thus, there exists the possibility for the hysteretic controlled buck converter to take the place of the PWM-controlled converters. The hysteretic controllers are inherently

stable and has very fast response to variations either from the load side or the reference voltage. With such modification, the complexity of the control circuitry can be further reduced and subsequently the quiescent power can be reduced. Meanwhile, the spectrum of the switching regulator can be predicted, even at the quiescent state when the load current is minimum, the switching frequency will be kept at a predefined minimum level instead of dropping below the audio signal band.

Bibliography

- [1] K. Boyce, “Cellular handset audio evolution—Part 1,” EE Times Design, Aug. 2005, [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1274727.
- [2] M. Hammes, C. Kranz, J. Kissing, D. Seippel, P. Bonnaud, and E. Pelos, “A GSM Baseband Radio in 0.13 μ m CMOS with Fully Integrated Power-Management,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2007.
- [3] P. Bonnaud, M. Hammes, A. Hanke, J. Kissing, R. Koch, E. Labarre, and C. Schwoerer, “A Fully Integrated SoC for GSM/GPRS in 0.13 μ m CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006.
- [4] S. Galal, H. Zheng, K. Abdelfattah, V. Chandrasekhar, I. Mehr, A. J. Chen, J. Platenak, N. Matalon, and T. L. Brooks, “A 60 mW Class-G Stereo Headphone Driver for Portable Battery-Powered Devices,” *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1921–1934, Aug 2012.
- [5] M. Wang, X. Jiang, J. Song, and T. L. Brooks, “A 120 dB Dynamic Range 400 mW Class-D Speaker Driver With Fourth-Order PWM Modulator,” *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1427–1435, Aug 2010.
- [6] Y. Choi, W. Tak, Y. Yoon, J. Roh, S. Kwon, and J. Koh, “A 0.018% THD+N, 88-dB PSRR PWM Class-D Amplifier for Direct Battery Hookup,” *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 454–463, Feb 2012.

- [7] L. Guo, T. Ge, and J. S. Chang, “A 101 dB PSRR, 0.0027% THD + N and 94% Power-Efficiency Filterless Class D Amplifier,” *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2608–2617, Nov 2014.
- [8] Y. Quek, “Class-D LC Filter Design,” Texas Instrumentation, Application Report S-LOA119B, Tech. Rep., April 2006.
- [9] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecch, and G. Nicollini, “A 1 W 104 dB SNR Filter-Less Fully-Digital Open-Loop Class D Audio Amplifier With EMI Reduction,” *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 686 – 698, Mar 2012.
- [10] M. A. Teplechuk, A. Gribben, and C. Amadi, “True filterless class-d audio amplifier,” *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2784 – 2793, Dec 2011.
- [11] H. Kim, S. Jung, H. Jung, J. Shin, and P. Choi, “Low cost implementation of filterless class D audio amplifier with constant switching frequency,” *IEEE Trans. Consum. Electron.*, vol. 52, no. 4, Nov 2006.
- [12] “Managing EMI in Class D Audio Applications,” Texas Instruments, Application Report SNAA050A, Tech. Rep., Nov 2007.
- [13] D. M. Monticelli, “A quad CMOS single-supply op amp with rail-to-rail output swing,” *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1026–1034, Dec 1986.
- [14] R. Hogervorst, J. Tero, R. Eschauzier, and J. Huijsing, “A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries,” *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505 – 1513, Dec 1994.
- [15] R. Eschauzier, R. Hogervorst, and J. Huijsing, “A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6 MHz UGF,” *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1497 – 1504, Dec 1994.

- [16] F. O. Eynde, P. Ampe, L. Verdeyen, and W. Sansen, “A CMOS large-swing low-distortion three-stage class AB power amplifier,” *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 265 – 273, Feb 1990.
- [17] F. You, S. Embabi, and E. Sanchez-Sinencio, “Low-voltage class AB buffers with quiescent current control,” *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 915 – 920, Jun 1998.
- [18] K. J. D. Langen and J. H. Huijsing, “Compact low-voltage power-efficient operational amplifier cells for VLSI,” *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct 1998.
- [19] V. Dhanasekaran, J. Silva-Martinez, and E. Sanchez-Sinencio, “Design of Three-Stage Class-AB 16 Ω Headphone Driver Capable of Handling Wide Range of Load Capacitance,” *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1734–1744, June 2009.
- [20] C. Mohan and P. M. Furth, “A 16- Ω Audio Amplifier With 93.8-mW Peak Load Power and 1.43-mW Quiescent Power Consumption,” *IEEE Trans. Circuits Syst. II*, vol. 59, no. 3, pp. 133–137, March 2012.
- [21] S. H. Wen and C. C. Yang, “A 5.2mW, 0.0016% THD up to 20kHz, ground-referenced audio decoder with PSRR-enhanced class-AB 16 Ω headphone amplifiers,” in *Proc. IEEE Symp. VLSI Circuits*, June 2012, pp. 20–21.
- [22] Z. Peng, S. Yang, Y. Feng, Z. Hong, and B. Liu, “An 80% peak efficiency, 410mW, single supply rail powered Class-I linear audio amplifier,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sept 2011, pp. 1–4.
- [23] C. Davis and V. Vergara, “How Audio Codecs Works,” EE Times, Oct. 2005, [Online].Available: http://www.eetimes.com/document.asp?doc_id=1274744.
- [24] “Automatic Hardware Implementation of Digital Filters for an Audio Codec,” Mathworks, Technical Articles and Newsletter, 2009, [Online].Available:

<https://se.mathworks.com/company/newsletters/articles/automatic-hardware-implementation-of-digital-filters-for-an-audio-codec.html>.

- [25] C. Davis, *Handbook for Sound Engineers, Fourth Edition*. Elsevier Inc, 2008.
- [26] R. van der Zee, “High efficiency audio power amplifiers design and practical use,” Ph.D. dissertation, University of Twente, May 1999.
- [27] F. H. Rabb, “Average Efficiency of Class-G Power Amplifiers,” *IEEE Trans. Consum. Electron.*, vol. CE-32, no. 2, pp. 145–150, May 1986.
- [28] S.-H. Wen, C.-M. Chen, C.-C. Yang, C.-H. Chen, J.-F. Jiang, K.-J. Hsiao, and C.-Y. Chien, “A Load-Adaptive Class-G Headphone Amplifier With Supply-Rejection Bandwidth Enhancement Technique,” *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2241–2251, July 2016.
- [29] X. Jiang, J. Song, J. Chen, V. Chandrasekhar, S. Galal, F. Cheung, D. Cheung, and T. Brooks, “A Low-Power, High-Fidelity Stereo Audio Codec in 0.13 μ m CMOS,” *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1221–1231, May 2012.
- [30] F. Xiao and P. K. Chan, “A Performance-Aware Low-Quiescent Headphone Amplifier in 65-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 505 – 516, Feb. 2017.
- [31] Y. Feng, “Research and design of high efficiency linear audio power amplifier with adaptive supply rails,” Ph.D. dissertation, Fudan University, Apr. 2011.
- [32] J. Chen, S. K. Arunachalam, T. L. Brooks, I. Mehr, F. Cheung, and H. Venkatram, “A 62mW stereo class-G headphone driver with 108dB dynamic range and 600 μ A/channel quiescent current,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb 2013, pp. 182–183.
- [33] M. Kim, D. Lu, T. Brooks, Y. Kim, V. Chandrasekhar, D. Stubbs, S. Maughan, and B. Mas, “A stereo 110 dB multi-rate audio $\Delta\Sigma$ DAC with Class-G headphone driver,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sept 2014.

- [34] A. Lollo, G. Bollati, and R. Castello, “A Class-G Headphone Amplifier in 65 nm CMOS Technology,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2530–2542, Dec 2010.
- [35] B. Bhamidipati, A. I. Colli-Menchi, and E. Sánchez-Sinencio, “Low power complementary metal-oxide semiconductor class-g audio amplifier with gradual power supply switching,” *IET Circuits, Devices & Systems*, vol. 9, no. 4, pp. 256–264, 2015.
- [36] H. Zhang, M. T. Tan, and P. K. Chan, “A single-supply inductorless CMOS class G speaker amplifier,” in *Proc. IEEE 54th Midwest Symp. Circuits Syst (MWSCAS)*, Aug 2011, pp. 1–4.
- [37] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, D. R. Holberg, Ed. Oxford University Press, 2002.
- [38] P. R. Gray, *Analysis and Design of Analog Integrated Circuits*, 5th ed. John Wiley & Sons, 2009.
- [39] R. Eschauzier, L. Kerklaan, and J. Huijsing, “A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure,” *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709 – 1717, Dec. 1992.
- [40] J. Huijsing, R. Hogervorst, and K. J. de Langen, “Low-power low-voltage VLSI operational amplifier cells,” *IEEE Trans. Circuits Syst. I*, vol. 42, no. 11, pp. 841 – 852, Nov. 1995.
- [41] R. Eschauzier and J. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Springer Science & Business Media, 1995.
- [42] K. N. Leung and P. Mok, “Analysis of multistage amplifier-frequency compensation,” *IEEE Trans. Circuits Syst. I*, vol. 48, no. 9, pp. 1041 – 1056, Sep. 2001.
- [43] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, “Multistage amplifier topologies with nested gm-C compensation,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 2000–2011, Dec. 1997.

- [44] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221 – 230, Feb. 2000.
- [45] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, p. 2074–2079, Nov. 2004.
- [46] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.
- [47] S. Kim, R. Nandwana, Q. Khan, R. Pilawa-Podgurski, and P. Hanumolu, "12.2 A1.8V 30-to-70MHz 87% peak-efficiency $0.32mm^2$ 4-phase time-based buck converter consuming $3\mu A$ /MHz quiescent current in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015.
- [48] M. S. J. Sankman and D. Ma, "A 6A 40MHz four-phase ZDS hysteretic DC-DC converter with 118mV droop and 230ns response time for a 5A/5ns load transient," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014.
- [49] B. Lee, M. Song, A. Maity, and D. Ma, "A 25MHz 4-phase SAW hysteretic DC-DC converter with 1-cycle APC achieving 190ns tsettle to 4A load transient and above 80Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Mar. 2017.
- [50] S. Lee, J. Bang, K. Yoon, S. Hong, C. Shin, M. Jung, and G. Cho, "A $0.518mm^2$ quasi-current-mode hysteretic buck DC-DC converter with $3\mu s$ load transient response in $0.35\mu m$ BCDMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015.
- [51] S. Huerta, A. Soto, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Advanced Control for Very Fast DC-DC Converters Based on Hysteresis of the Current," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 4, pp. 1052 – 1061, Apr. 2013.

- [52] P. Li, D. Bhatia, L. Xue, and R. Bashirullah, “A 90240 MHz Hysteretic Controlled DC-DC Buck Converter With Digital Phase Locked Loop Synchronization,” *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2108 – 2119, Sep. 2011.
- [53] Y. Zheng, H. Chen, and K. Leung, “A Fast-Response Pseudo-PWM Buck Converter With PLL-Based Hysteresis Control,” *IEEE Trans. VLSI Syst.*, vol. 20, no. 7, pp. 1167 – 1174, Jul. 2011.
- [54] F. Su, W. Ki, and C. Tsui, “Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 815 – 822, Apr. 2008.
- [55] Z. Sun, L. Siek, R. Singh, and M. Je, “A Fixed-frequency hysteretic controlled buck DC-DC converter with improved load regulation,” in *Proc. IEEE Int. Symp. Circuits Syst (ISCAS)*, Jun. 2015.
- [56] K. Hu, S. Lin, and C. Tsai, “A Fixed-Frequency Quasi- V^2 Hysteretic Buck Converter With PLL-Based Two-Stage Adaptive Window Control,” *IEEE Trans. Circuits Syst. I*, vol. 62, no. 10, pp. 2565 – 2573, Oct. 2015.
- [57] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Kluwer Academic Publishers, 2001.
- [58] D. M. Mitchell, *DC-DC Switching Regulator Analysis*. McGraw-Hill Book Company, 1988.
- [59] R. D. Middlebrook and S. Cuk, “A general unified approach to modeling switching-converter power stages,” *Int. Journal of Electron*, vol. 42, no. 6, pp. 521–550, Jun. 1977.
- [60] S. Cuk, “Modeling, analysis, and design of switching converters,” phdthesis, California Institute of Technology, Nov. 1976.

- [61] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch I: Continuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 490–496, 1990.
- [62] Vorperian, "Simplified analysis of PWM converters using model of PWM switch II: Discontinuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 497–505, 1990.
- [63] D. Maksimovic and S. Cuk, "A unified analysis of PWM converters in discontinuous modes," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 476–490, 1991.
- [64] M. Siu, P. K. T. Mok, K. N. Leung, Y. H. Lam, and W.-H. Ki, "A voltage-mode pwm buck regulator with end-point prediction," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 4, pp. 294–298, April 2006.
- [65] P. Y. Wu and P. K. T. Mok, "A monolithic buck converter with near-optimum reference tracking response using adaptive-output-feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2441–2450, Nov 2007.
- [66] W. R. Liou, M. L. Yeh, and Y. L. Kuo, "A high efficiency dual-mode buck converter ic for portable applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 667–677, March 2008.
- [67] J. M. Wang, S. T. Wu, and G. C. Jane, "A novel control scheme of synchronous buck converter for zvs in light-load condition," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3265–3273, Nov 2011.
- [68] B. Sahu and G. A. Rincon-Mora, "A high-efficiency, dual-mode, dynamic, buck-boost power supply IC for portable applications," in *Proc. IEEE VLSI Design*, 2005, pp. 858 – 861.

- [69] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, “A 4- μ A quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2342 – 2348, Dec. 2004.
- [70] H. Huang, K. Chen, and S. Kuo, “Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-On-Chip Applications,” *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2451 – 2465, Nov. 2007.
- [71] D. Meeks, “Loop Stability Analysis of Voltage Mode Buck Regulator With Different Output Capacitor Types – Continuous and Discontinuous Modes,” Texas Instruments, techreport, Apr. 2008.
- [72] A. Stratakos, S. Sanders, and R. Brodersen, “A low-voltage CMOS DC-DC converter for a portable battery-operated system,” in *Proc. IEEE Power Electronics Specialists Conf.*, Jun. 1994.
- [73] L. Casey, J. Ofori-Tenkorang, and M. Schlect, “CMOS drive and control circuitry for 1-10 MHz power conversion,” *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 749 – 758, Oct. 1991.
- [74] C. Yoo, “A CMOS buffer without short-circuit power consumption,” *IEEE Trans. Circuits Syst. II*, vol. 47, no. 9, pp. 935 – 937, Sep. 2000.
- [75] R. Palmer, “Guidelines for measuring audio power amplifier performance,” Texas Instruments, techreport, October 2001.
- [76] “High performance class G stereo headphone amplifier with I2C volume control,” STMicroelectronics, datasheet, Feb 2010.
- [77] “Class-G Directpath Stereo Headphone Amplifier with I2C Volume Control,” Texas Instruments, Inc, datasheet, 2009.
- [78] “LM48824 Class G Headphone Amplifier with I2C Volume Control,” Texas Instruments, Inc, datasheet, 2013.

- [79] “Boomer Audio Power Amplifier Series High Efficiency Class H, High Voltage, Haptic Piezo Actuator/Ceramic Speaker Driver,” Texas Instruments, Inc, datasheet, 2013.
- [80] X. Jing, P. K. T. Mok, and M. C. Lee, “A Wide-Load-Range Constant-Charge-Auto-Hopping Control Single-Inductor-Dual-Output Boost Regulator With Minimized Cross-Regulation,” *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2350 – 2362, Oct. 2011.

Publications

1. X. Zhang and L. Siek, "An 80.4% Peak Power Efficiency Adaptive Supply Class H Power Amplifier for Audio Applications," *IEEE Trans. VLSI Syst*, Volume 25, Issue 6, pp. 1954-1965, June 2017.
2. C. Yu, X. Zhang, and L. Siek, "A continuous switching mode step-down switched-capacitor regulator with inrush current control scheme," in *Proc. IEEE International Symp on Integrated Circuits (ISIC)*, 2016
3. X. Zhang and L. Siek, "A highly efficient, 420mW class-H headphone amplifier with single power supply rail," in *Proc. IEEE International Conf on Electron Devices and Solid-state Circuits (EDSSC)*, 2015