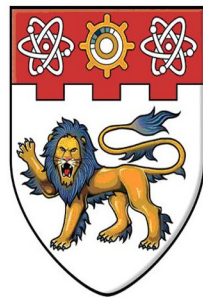


Advanced CMOS Technologies (High- k /Metal Gate Stacks) for Sub-22nm Node



**NANYANG
TECHNOLOGICAL
UNIVERSITY**

Wu Ling (G0802754A)

Supervisor: A/P Fan Weijun

Dr. Yu Hong Yu

**SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING
NANYANG TECHNOLOGICAL UNIVERSITY**

2013

Advanced CMOS Technologies (High-*k*/Metal Gate Stacks) for Sub-22nm Node

SUBMITTED

BY

Wu Ling

(G0802754A)

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

A thesis submitted to Nanyang Technological University
in fulfillment of the requirement for the
Degree of Doctor of Philosophy

2013

Statement of Originality

I hereby certify that the content of this dissertation is the result original research and has not been submitted for a higher degree to any other University or Institution.

Date

Wu Ling

ACKNOWLEDGEMENT

I would like to express my thanks and gratitude to my supervisor, Dr. Yu Hong Yu for his advice and guidance throughout the entire course of this project. His patience and understanding during the learning process is greatly appreciated, for he has imparted lots of knowledge and valuable experiences both in project-related area as well as in working life.

I would like to express my gratitude Assoc Prof Fan Wei Jun, Nanyang Technological University, Dr. Pan Ji Sheng, Institute of Materials Research and Engineering, for their guidance and valuable suggestions on my project and thesis work.

Special thanks go to Taiwan Semiconductor Manufacturing Company for their co-operation and sponsorship on the jointly developed project. I sincerely thank them for providing precious industry experience throughout this project.

I would also like to express his gratitude to Nanyang Technological University for providing research scholarships. Its education in Engineering equipped me with an analytical mind and strong fundamentals. Its dynamic environment and excellent facilities stimulate my interest in learning.

I am grateful to all the fellow students and staff for their invaluable suggestions and support during the project.

Last but not the least, I would like to thank my beloved family. My father, mother, brother provided their moral support during my study and stay in Singapore, without their love, I would not be able to reach this far. Most importantly, I thank my wife, Ms. Xu Mingjing, for her patience, care, love, and continuous encouragement.

ABSTRACT

A thermally grown silicon dioxide (SiO_2), which forms the insulating layer in the metal-oxide-semiconductor field effect transistor (MOSFET), is considered as the heart of a MOSFET. It has been essential for the microelectronics revolution due to the following outstanding properties: high resistivity ($\sim 10^{15} \Omega \text{ cm}$), excellent dielectric strength ($\sim 1 \times 10^7 \text{ V/cm}$), large band gap (9 eV), high melting point (1713 °C), native and low defect density interface with Si ($\sim 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$). However, high-K/metal gate technology is now replacing conventional SiO_2 (SiON)/Poly-Si gate in state-of-the-art transistors for both high performance and low-power applications to overcome the unacceptable large gate leakage current resulting from the extremely thin SiO_2 thickness ($< 1 \text{ nm}$), as well as Fermi level pinning, poly depletion and dopant penetration associated with Poly gate/ HfO_2 interface.

In this report, several advanced topics in high- k /metal gate stack are studied in order to address various issues, such as band-edge metal gate work function tuning, thermal stability of metal gate with different composition and deposition methods, and novel post deposition treatment and/or deposition technique to improve high- k quality. The topics studied including:

1. Electrical and Physical Properties of Er doped HfO₂ high-*k* dielectrics prepared by Atomic Layer Deposition

A metal gate/Hf-based high-*k* dielectric gate stack with an appropriate work function is considered as one of the critical technology solutions for sub-45 nm complementary metal oxide semiconductor technology. One of the major problems for HfO₂ is Fermi-level pinning between HfO₂ and the metal gate. Recently, HfO₂ incorporated with lanthanide (e.g., La, Dy, Er, etc.) received considerable attention due to its capability to tune the metal work function toward the Si conduction band-edge, enabling its n-FET application. In this work, Er-doped HfO₂ high-*k* dielectrics (with 4 and 7% Er) were prepared by atomic layer deposition (ALD), which is more compatible with the industrial needs due to excellent process controllability and is also more suitable for sub-1 nm equivalent oxide thickness scaling due to superb scalability. With 7% of Er incorporated into HfO₂, (1) the TiN metal gate work function can be modulated to a value of ~4.18 eV; (2) the thermal stability of the HfO₂ film is improved, as evidenced by X-ray photoelectron spectroscopy and X-ray diffraction studies; and (3) the *K*-value and leakage properties of HfO₂ are maintained after Er doping.

2. Thermal Stability of TiN Metal Gate Prepared by Atomic Layer Deposition or Physical Vapor Deposition on HfO₂ High-*k* Dielectric

The thermal stability of TiN metal gate with various composition prepared by either ALD or PVD on HfO₂ high-*k* dielectric is investigated and compared by electrical (Capacitance,

leakage current) and physical (X-ray Photoelectron Spectroscopy, High Resolution Transmission Electron Microscopy, and Electron Energy Loss Spectroscopy) analysis. After annealing of the TiN/HfO₂ stack at 1000 °C for 30 s, it is observed that: 1) Nitrogen tends to out-diffuse from TiN for all the samples; 2) Oxygen from the interfacial layer (IL) between HfO₂ and Si tends to diffuse towards TiN. PVD Ti-rich TiN shows a wider oxygen distribution in the gate stack and also a thinner IL than the N-rich sample. Besides, the oxygen out-diffusion can be significantly suppressed for ALD TiN compared to the PVD TiN samples. The work function of TiN metal gate is correlated with its thermal stability.

3. A Novel Multi Deposition Multi Room-Temperature Annealing Technique via Ultraviolet-Ozone to Improve High-*k*/Metal (HfZrO/TiN) Gate Stack Integrity for a Gate-Last Process

ALD HfZrO high-*k* fabricated by novel multi deposition multi annealing (MDMA) technique at room temperature in Ultraviolet-Ozone (UVO) ambient is systematically investigated for the first time via both physical and electrical characterization. As compared to the reference gate stack treated by conventional rapid thermal annealing (RTA) @ 600 °C for 30 s (with PVD TiN electrode), the devices receiving MDMA in UVO demonstrates: 1) more than one order of magnitude leakage reduction without EOT penalty at both room temperature and an elevated temperature of 125 °C; 2) much improved stress induced degradation in term of leakage increase and flat band voltage shift (both room temperature and 125 °C); 3) enhanced dielectrics break-down strength

and time-dependent-dielectric-breakdown (TDDB) life time. The improvement strongly correlates with the cycle number of deposition and annealing (D & A, while keeping the total annealing time and total dielectrics thickness as the same). Scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS) analysis suggest both oxygen vacancies (V_o) and grain boundaries suppression in the MDMA treated samples are likely responsible for the device improvement. Besides, the nMOSFETs with UVO MDMA show superior properties, in terms of enhanced channel electron mobility, improved immunity to biased temperature instability, and reduced gate dielectric relaxation current. This is explained by the reduction of bulk oxide trap and interface trap density because of healing of V_o after UVO MDMA annealing. The novel room temperature UVO annealing is promising for the gate stack technology in a gate last integration scheme.

Table of Contents

ACKNOWLEDGEMENT	i
ABSTRACT	iii
Table of Contents	vii
List of Figures	xiii
List of Tables	xxii
Chapter 1 Introduction	1
1.1 Background	1
1.2 Motivation	4
1.3 Objectives.....	4
1.4 Major Contributions of the Thesis	4
1.5 Organization of the Thesis	5
References.....	8

CHAPTER 2 Literature Review	10
2.1 Overview of MOSFET Scaling.....	10
2.2 Basic Requirements for High- <i>k</i> Gate Dielectrics.....	18
2.2.1 Dielectric constant, Barrier Height and Band Gap	18
2.2.2 Thermodynamic Stability on Si and Film Morphology.....	21
2.2.3 Channel Interface Quality.....	22
2.2.4 Carrier Mobility Issues	24
2.2.5 Threshold Voltage Instability	26
2.3 Metal Gate electrodes	27
2.3.1 Scaling Limits for Poly-Si Gate Electrode.....	27
2.3.2 Basic Requirements for Metal Gate Electrodes.....	31
2.4 Summary	36
References.....	37
CHAPTER 3 Experimental Procedure and Set-ups	47
3.1 Device Fabrication.....	47
3.2 Device Characterization.....	49
3.2.1 Electrical Characterization.....	49
3.2.2 Physical Characterization	58

3.3 Summary	62
References:.....	64

CHAPTER 4 Electrical and Physical Properties of Er Doped HfO₂

High-*k* Dielectrics Prepared by Atomic Layer Deposition 65

4.1 Introduction	65
4.2 Experimental	66
4.3 Results and Discussion	67
4.4 Summary	72
References.....	73

CHAPTER 5 Thermal Stability of TiN Metal Gate Prepared by Atomic

Layer Deposition or Physical Vapor Deposition on HfO₂ High-*k*

Dielectric..... 76

5.1 Introduction	76
5.2 Experimental	77
5.3 Results and Discussion	78
5.3.1 Ti-rich vs. N-rich.....	79
5.3.2 ALD vs. PVD	81
5.4 Summary	86

References.....	87
-----------------	----

**CHAPTER 6 A Novel Multi Deposition Multi Room-Temperature
Annealing Technique via Ultraviolet-Ozone to Improve High-*k*/Metal
(HfZrO/TiN) Gate Stack Integrity for a Gate-Last Process..... 89**

6.1 Introduction	89
6.2 Experimental	90
6.3 Results and Discussion	93
6.3.1 Electrical Characterization.....	93
6.3.2 Physical Characterization	101
6.3.3 Proposed Model.....	107
6.4 Summary	108
References.....	109

**CHAPTER 7 Device Performance and Reliability Improvement for
MOSFETs with HfO₂ Gate Dielectrics Fabricated using Multi
Deposition Multi Room-Temperature Annealing112**

7.1 Introduction	112
7.2 Experimental	113
7.3 Results and Discussion	114

7.4 Summary	119
References.....	120
CHAPTER 8 Conclusions and Recommendations.....	123
8.1 Conclusions	123
8.2 Recommendations	125
Author's Publication List	127

List of Figures

Fig. 2.1 Schematic of direct tunneling through a SiO₂ and alternative high-*k* dielectric. Physically thicker high-*k* material can reduce tunneling current. 17

Fig. 2.2 Dielectric constant versus band gap for various gate dielectrics.... 19

Fig. 2.3 Calculated conduction band and valence band offsets of various dielectrics on silicon. 20

Fig. 2.4 Carrier mobility increases with the interfacial oxide thickness..... 25

Fig. 2.5 (a) Schematics of high-*k*/poly-Si stacks and high-*k*/metal/poly-Si stacks. **(b)** TEM images and equivalent circuit of representative SiON/HfO₂/poly-Si and SiON/HfO₂/W stacks that illustrate the impact of poly depletion and the benefits of metal gates..... 29

Fig. 3.1 Illustration of MOSCAP fabrication process flow at NTU N2FC CR1. 48

Fig. 3.2 (a) Suss PM8 200mm manual probe station and (b) Keithley 4200 Semiconductor Characterization System.....	49
Fig. 3.3 Equivalent circuit of MOSFET in split <i>C-V</i> measurement.	51
Fig. 3.4 The experimental set-up of bulk capacitance measurement.....	53
Fig. 3.5 Equivalent circuits for conductance measurements: (a) MOS-C with interface trap time constant $\tau_{it} = R_{it} * C_{it}$, (b) simplified circuit of (a)	55
Fig. 3.6 Illustration of applied stressing voltage on gate electrode during dielectric relaxation current measurement.	57
Fig. 3.7 Illustration of basic components and working principle of an XPS system [5].	59
Fig. 3.8 Illustration of basic components and working principle of an STM system [6].	61

Fig. 4.1 The measured and simulated C-V curves for HfErO devices. Inset graph shows normalized C-V curves for HfErO with different Er concentration. The V_{fb} of HfO₂ control is about -0.1V. Capacitor area = $16 \times 10^{-5} \text{ cm}^2$ 67

Fig. 4.2 V_{fb} versus EOT of fabricated MOS capacitors with HfO₂ or HfErO gate dielectrics. 68

Fig. 4.3 Gate leakage current density versus EOT relationship for HfO₂ and HfErO with different Er concentration. 69

Fig. 4.4 Extracted dielectric constant K for HfO₂ and HfErO with Er of 7%. 70

Fig. 4.5 XPS shows that Hf 4f peak shifts to higher binding energy state after high-temperature annealing. 71

Fig. 4.6 XRD for HfO₂ and HfErO (7% Er) annealed at 800 °C and 1000 °C. 72

Fig. 5.1 HRTEM picture shows that the interfacial layer thickness of Ti-rich sample (1.3 nm) is thinner than N-rich sample (1.7 nm). 79

Fig. 5.2 EELS spectra show that Ti-rich (left) sample has wider O distribution than N-rich sample (right). A signal of Ti penetration into HfO gate dielectric is observed for Ti-rich sample than N-rich one. 80

Fig. 5.3 Gate leakage current comparison of Ti-rich and N-rich PVD TiN gated samples after 1000 °C annealing. Ti-rich sample shows initial hard breakdown behavior, while the N-rich sample I-V characteristic is “normal”. 81

Fig. 5.4 XPS Hf 4f spectra after 400 °C and 1000 °C anneal of ALD TiN (top) and PVD N-rich TiN (bottom). Hf signal were collected after Ar+ sputtering of the samples for 5mins, when top TiN film are all sputtered off. 83

Fig. 5.5 XPS Ti 2p spectra of TiN bulk after 1000 °C annealing for ALD and N-rich PVD TiN samples. PVD sample shows larger BE, indicating

more Ti-O bond formation than ALD. Ti signal were collected after Ar+ sputtering of the samples for 2mins, when TiN bulk is exposed for scan. .. 84

Fig. 5.6 Measured and fitted C-V for ALD and PVD N-rich sample. PVD sample shows more negative V_{fb} than ALD one..... 85

Fig. 5.7 The schematics of EWF change after high T annealing of ALD TiN (left) and PVD TiN (right). 86

Fig. 6.1(a) Device fabrication process flow; **(b)** Schematic shows the UVO annealing process..... 91

Fig. 6.2 TEM pictures confirm that all samples annealed at different condition have similar EOT, ~1.3 nm IL and ~2.0 nm HK. **(i)** RTP 600 °C 30 s; **(ii)** UVO 2min × 2; and **(iii)** UVO 1min × 4. Clear crystallization is observed in RTP samples..... 92

Fig. 6.3. (a) Measured CV for devices with only one-time UVO annealing after HK deposition; devices shows high leaky behaviour **(b)** measured (symbols) and fitted (lines) CV curves for devices with conventional RTP

(control) and MDMA (UVO annealing). Inset shows all samples are with similar EOT. 94

Fig. 6.4 Measured gate leakage current at room temperature. Leakage reduction more than one order is observed for UVO 1min × 4 sample compare with RTP control. 95

Fig. 6.6 Stress induced leakage current increase at (a) 25 °C; (b) 125 °C. At both temperatures, UVO annealed samples are less susceptible to current degradation at given bias condition ($V_{g, stress} = -2$ V), which is more prominent with increasing D & A cycles. 97

Fig. 6.7 Stress induced flat band voltage shift at 25 °C and 125 °C. UVO annealed samples are less prone to V_{fb} degradation after stress, which is probably due to less charge trapping inside the UVO annealed film. 98

Fig. 6.8 Cumulative probability of breakdown voltage for samples with different PDA. MDMA can significantly improve the breakdown voltage while increasing the number of D & A cycles can further improve V_{BD} 99

Fig. 6.9 TDDB characteristics at a given stress voltage ($V_g = -3.5$ V). The Breakdown time is significantly increased for samples annealed using MDMA (UVO annealing) compare with RTP control samples.100

Fig. 6.10 TDDB lifetime projections as a function of stressing voltage. 10 years life time is -1.36 V and -1.55 V for samples annealed at RTP and UVO 1min \times 4 conditions, respectively.....100

Fig. 6.11 Tunneling current collected by STM for different samples. UVO annealed samples shows much lower leakage than RTP control samples. Increasing number of D & A cycles gives additional tunneling reduction. 101

Fig. 6.12 High- k topography (upper) and the corresponding current map (lower) by STM of samples after (a) RTP 600 °C 30 s, (b) UVO 2min \times 2, and (c) UVO 1min \times 4. Clear grains are observed in RTP samples. Bright shades correspond to locally higher tunneling current.....102

Fig. 6.13 Normalized current distribution based on the analysis of the corresponding local *IV* spectroscopy. UVO 1min × 4 sample shows best electrical homogeneity.....103

Fig. 6.14 Comparison of I_t evolution by STM (@ $V_s = 1.5$ V) as a function of consecutive Ramp Voltage Stressing (RVS) cycles. Bottoms are the *IV* sweep of RTP (left) and UVO 1min × 4 (right) samples under 10 cycles of RVS.....104

Fig. 6.15 Si 2*p* XPS spectra of HfZrO/IL/Si stack . UVO 1min × 4 sample shows least sub-oxide intensity, indicating lowest V_o at HK/IL interface. Peak positions all aligned to C 1*s* peak binding energy.....106

Fig. 6.16 Hf 4*f* XPS spectra shows no obvious shift, excludes Hf-silicate influence. All peak positions are aligned to the C 1*s* peak binding energy at 285eV.106

Fig. 6.17 Schematic showing how MDMA (UVO annealing) can potentially improve HK film quality: 1) with UV light, oxygen can be cooperated into

to HK film to heal the V_o , especially along grain boundaries; 2) with multi deposition, the grain boundaries, which can serves as leakage path inside the film could be dis-connected due to the healing of V_o , thus leads to leakage reduction.....108

Fig. 7.1 Id-Vg characteristic of nMOSFETs with different D & A methods.115

Fig. 7.2 Effective electron mobility extracted by split C-V method and compared with universal electron mobility.115

Fig. 7.3 Interface trap density D_{it} extracted by conductance method. Inset shows the measured conductance over frequency (G/ω) as a function of frequency. D_{it} is lowest for UVO 1min \times 4 sample while highest for RTP control.....116

Fig. 7.4 Stress induced threshold voltage (V_t) shift and recovery at room temperature. UVO annealed samples are much less prone to V_t degradation after stress.....117

Fig. 7.5 Gate dielectric relaxation current measured after 100s stressing voltage $V_g = 2V$ is switch off. RTP control shows largest magnitude of relaxation current.118

List of Tables

Table 2.1 The scaling parameters for CES, CVS and generalized scaling rules.....11

Table 5.1 The atomic composition of TiN film after 400 °C and 1000°C annealing as measured by XPS77

Table 5.2 The amount of oxygen increased in the PVD and ALD TiN bulk. O signal were collected after Ar+ sputtering of the samples for 2mins, when TiN bulk is exposed for scan.....80

Table 6.1 The details of High K deposition and annealing conditions for all samples.....90

Chapter 1 Introduction

1.1 Background

The advent of the information technology boom has spurred enormous growth in Si microelectronics over the past two decades. Advanced microprocessors are tailored for high performance (e.g., CPUs, gaming chips, servers) and low power (e.g., handheld mobile phones), with metal oxide semiconductor field effect transistors (MOSFETs) as the key solid-state element within. MOSFETs can have either electrons (nFETs) or holes (pFETs) as the majority carriers, and these combine to form the basis for CMOS (complementary MOS) logic. At the core of the MOSFET is the gate oxide [conventionally Si dioxide or Si oxynitride compound, also denoted as SiO(N)], the thickness and quality of which play a critical role in device performance and scaling[1].

Rapid advances in CMOS technology have led to aggressive scaling of the MOSFET gate stack to achieve higher density and better performance. Conventional poly-Si/SiO₂ gate stack is approaching some practical limits, e.g. the gate oxide thickness has ceased scaling starting from 90nm node, because the gate leakage current due to tunneling and oxide breakdown is already quite high at its thickness of ~1.2 nm [1], discouraging its further reduction in physical thickness. Therefore, advanced gate stacks involving metal gate materials and high-*k* dielectrics may need to be introduced into IC

industry as well as some novel process integration technologies. However, immense challenges arise in material engineering and process integration of the advanced gate stack. Thus much attention has been drawn by both academic and industrial research and development (R & D) communities [2-3] over the past decade.

Owing to the higher permittivity, high- k dielectrics provide two primary advantages over conventional SiO(N) dielectrics. First, high- k dielectrics can be grown physically thicker while maintaining a similar Equivalent Oxide Thickness (EOT) as SiO₂, thus offering significant gate leakage reduction [2–3] and making these materials suitable for low-power applications. Second, high- k dielectrics have the potential to provide significantly lower EOT values than is possible with conventional SiON dielectrics, thereby re-enabling transistor scaling and the use of lower gate voltages. Starting in the late 1990s, there was a concerted worldwide effort to find an appropriate high- k dielectric for integration into CMOS technology. Although Hf-based high- k materials emerged as the dielectric of choice in 2001–2002 [4–9], many incompatibilities with conventional CMOS processes delayed their introduction. However, recent materials and process innovations paved the way for this technology to emerge as a product reality evidenced by the high-performance 45 nm [10, 11] and low-power 32 nm [12] high- k /metal gate technology results.

In view of the difficulties in planar CMOS transistor scaling to preserve an acceptable gate to channel control FET based multi-gate (MuGFET) devices have been proposed as a technology option for replacing the existing technology [13]. The

attractiveness of FINFET consists in the realization of self-aligned double-gate devices with a conventional CMOS process. This allows extending the gate scaling beyond the planar transistor limits, maintaining a steep subthreshold slope, better performance with bias voltage scaling and good matching due to low doping concentration in the channel. There are, however, several challenges and roadblocks that FINFET technology has to face to be competitive with other technology options: high access resistance related to the extremely thin body, V_{tau} setting, implementation of strain boosters and manufacturability related to the non planar process and very tight process control.

To further enhance the performance and with recent advancement of high k metal gate technology, the semiconductor industry is also showing interest in high-mobility substrates such as Ge and III-V materials for CMOS technologies. While Ge is being considered for high hole mobility, III-V materials such as GaAs, InP, InGaAs, InAs, and GaSb are being considered for their high electron mobility. Once these materials are integrated into the MOS device architecture, it will lead to a functional diversification with additional applications like high performance analog/RF devices. However, several critical issues need to be resolved before these channel materials are integrated into the CMOS device/process technologies [14]: First, well understood and acceptable interface states between high k and the new channel material. Second, formation of low-resistive source and drain with the allowed thermal budget is also required. Third, the channel structures may be different if the scaled device structures are modified to either FinFETs or nanowire structures.

1.2 Motivation

High- k gate dielectric, along with metal gate, has been under intensively research in both academic and industry to replace conventional Poly-Si gate/SiO(N) gate stack in order to meet aggressive EOT scaling requirement during the past decade. However, there are still many integration and reliability issues that both industrial and academic R & D teams are trying to resolve, such as: the Fermi level pinning induced metal gate work function instability, oxygen vacancy related performance degradation, etc. Thus material innovation in the high- k dielectric and novel deposition technique and/or post deposition treatment are required to improve the quality of the high- k /metal gate stack.

1.3 Objectives

The objective of this research work is to improve the high- k /metal gate stack performance for advanced CMOS technology either by doping new element into Hf-based high- k dielectric or by novel deposition technique and/or post deposition treatment of the high- k dielectric in either gate first or gate last integration scheme.

1.4 Major Contributions of the Thesis

The major contributions of this work are:

1. Successfully tune the TiN metal gate work function towards to Si conduction band-edge by incorporating Er into HfO₂ high- k dielectric, bringing HfErO a viable dielectric for nMOS application.

2. Systematic study on TiN metal gate composition and deposition method impact on material and device properties. The correlation between N concentration and TiN work function is revealed. ALD TiN metal gate is found to be more effective to suppress O out-diffusion than PVD one after 1000 °C annealing, which results the flat-band voltage difference between ALD and PVD TiN metal gated capacitors.

3. A novel multi deposition multi room-temperature annealing (MDMA) via ultraviolet-ozone (UVO) is proposed to be a promising technique for gate-last integration scheme. A physical model explaining the mechanism of device performance (both MOSCAP and MOSFET) improvement is provided based on the correlation of the electrical and physical characterized results.

The above work has been published in prestigious conferences, such as *IEEE International Electron Device Meeting (IEDM)*, as well as prestigious journals, such as *IEEE Electron Device Letters (EDL)* and *Transactions on Electron Devices (TED)*, *Applied Physics Letter (APL)*, etc.

1.5 Organization of the Thesis

This report consists of seven chapters. Chapter 1 introduces the background, motivation, objectives and organization of this thesis.

Chapter 2 provides a literature review on the recent development of high-*k*/metal gate technology.

Chapter 3 focuses on the experimental set-up. The chapter first explains the details of devices fabrication process and then describes the analysis technique used in this project, including both electrical and physical characterization methods.

Chapter 4 presents the electrical and physical properties of Er doped HfO₂ high-*k* dielectrics prepared by atomic layer deposition (ALD). This chapter describes that with 7% of Er incorporated into HfO₂, the TiN metal gate work function can be modulated towards to Si conduction band edge, at the value of ~4.18 eV, enabling its n-MOSFET application. The thermal stability of the HfO₂ film is improved, as evidenced by X-ray Photoelectron Spectroscopy (XPS) and X-Ray Diffraction (XRD) studies, while the *K* value and leakage properties of HfO₂ are maintained after Er doping.

Chapter 5 studies the thermal stability of TiN metal gate prepared by ALD or physical vapor deposition (PVD) on HfO₂ high-*k* dielectric. After annealing of the TiN/HfO₂ stack at 1000 °C for 30 s, which is normally required by source/drain activation, it is observed that 1) Nitrogen tends to out-diffuse from both PVD and ALD TiN; 2) Oxygen from the interfacial layer (IL) between HfO₂ and Si tends to diffuse towards TiN for all the samples. PVD Ti-rich TiN can scavenge more oxygen from IL, but also shows signal of Ti penetration into HfO₂, which poses a concern on its thermal stability; 3) The oxygen out-diffusion from HfO₂/IL stack can be significantly suppressed for ALD TiN compared to the PVD TiN, which is critical to maintain the HfO₂ integrity. The effective work function of TiN metal gate is correlated with its thermal stability.

A novel multi deposition multi room-temperature annealing (MDMA) technique via ultraviolet-ozone (UVO) to improve high- k /metal (HfZrO/TiN) gate stack integrity for a gate-last process is presented in Chapter 6. For the first time, novel MDMA technique for ALD HfZrO treatment using room temperature UVO annealing is investigated both physically and electrically. The grain boundaries suppression and the healing of oxygen vacancies (V_o) are believed to be responsible for its superior performance based on Scanning Tunneling Microscopy (STM) and XPS studies. MDMA in UVO is proposed to be a promising HK treatment technique that is highly suitable for gate last integration scheme due to its nature of low thermal budget.

Chapter 7 discusses device performance and reliability improvement for MOSFETs with HfO₂ gate dielectrics fabricated using multi deposition multi room-temperature annealing. Compared to the conventional rapid thermal annealing, the nMOSFETs with UVO MDMA show superior properties, in terms of enhanced channel electron mobility, improved immunity to biased temperature instability, and reduced gate dielectric relaxation current.

Chapter 8 concludes the major achievements on high- k /metal gate stack studies in this work, as well as suggestions and recommendations for future work can be done for better understanding the application of high- k /metal gate stack in the advanced CMOS technologies.

References

- [1]. D.A. Buchanan, "Scaling the gate dielectric: materials, integration and reliability". *IBM J. Res. Dev.* 43:245–64, 1999.
- [2]. G. D. Wilk, R. M. Wallace, J. M. Anthony, "High- κ gate dielectrics: current status and materials properties considerations", *J. Appl. Phys.* 89:5243–75, 2001.
- [3]. S. Guha, E. P. Gusev, M. Copel, L. A. Ragnarsson, D. A. Buchanan, "Compatibility challenges for high- κ materials integration into CMOS technology", *MRS Bull.* 27:226–29, 2002.
- [4]. A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, T. Zabel, "Physical and electrical characterization of hafnium oxide and hafnium silicate sputtered films", *J. Appl. Phys.* 90:6466–75, 2001.
- [5]. D. C. Gilmer, R. Hegde, R. Cotton, J. Smith, L. Dip, "Compatibility of silicon gates with hafnium based gate dielectrics", *Microelectron Eng.* 69:138–44, 2003.
- [6]. E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, "Ultrathin high- κ gate stacks for advanced CMOS devices", *IEDM Tech. Dig.*, pp. 451–54, 2001.
- [7]. B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing", *Appl. Phys. Lett.* 76:1926–28, 1999.
- [8]. M. R. Visokay, J. J. Chambers, A. L. Rotondaro, A. Shanware, L. Colombo, "Application of HfSiON as a gate dielectric material", *Appl. Phys. Lett.* 80:3183–85, 2002.
- [9]. S. B. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, E. Luckowski, "Dual-metal gate CMOS with HfO₂ gate dielectric", *IEDM Tech. Dig.*, pp. 433–36, 2002.

[10] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neiryneck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. T roeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", IEDM Tech. Dig. 2007, p.247.

[11]. M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, "High-performance high- κ /metal gates for 45 nm CMOS and beyond with gate-first processing", *Symp. VLSI Tech. Dig. Tech. Pap.*, pp. 194–95, 2007

[12]. X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, "A cost effective 32 nm high- k /metal gate CMOS technology for low power applications with single-metal/gate-first process", *Symp. VLSI Tech. Dig. Tech. Pap.*, pp. 88–89, 2008.

[13]. M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann, and S. Biesemans, "Review of FINFET technology", *IEEE International SOI Conference*, pp. 1-4, 2009.

[14]. D. Misra, "High k Dielectrics on High-Mobility Substrates: The Interface!", *The Electrochemical Society Interface*, pp. 47-51, 2011.

CHAPTER 2 Literature Review

2.1 Overview of MOSFET Scaling

During the past several decades, silicon-based microelectronics devices have infiltrated practically every aspect of our daily life. This has been accomplished by continuously achieving the characteristics of faster speed, higher density, and lower power for the individual devices, namely, the Metal Oxide Semiconductor Field Effect Transistors – MOSFETs. Therefore, “scaling”, which is the reduction in individual device size, became the focus of engineers over the past forty years. The scaling behavior has followed the well-known Moore’s law, which predicts that the number of devices on an integrated circuit increases exponentially, doubling over a 1.5–2 year period [1]. During the silicon industry’s history and for most of the time, line features of the MOS devices have decreased at the rate of ~ 30% every two or three years. In the meantime, cost per function has decreased at an average rate of ~ 25-30% per year per function [2]. Based on the predication of International Technology Roadmap for Semiconductors (ITRS), in the year of 2016, the MOSFETs with channel length (L_g) of ~ 10 nm would be required for the mass production [2].

There are several different scaling rules aimed to reduce the device size while keeping device function [3-5], such as Constant Electric-field Scaling (CES), Constant Voltage Scaling (CVS), and the generalized scaling rules. In CES, it was proposed to keep the electric field unchanged in a short-channel device in order to maintain comparable characteristics and reliability of a long channel device. The idea behind CES is to scale the device voltages and the device dimensions both horizontally and vertically by the same factor, so that the electric field remains unchanged. However, the requirement to reduce the supply voltage by the same factor as the physical dimension reduction in CES is difficult to meet since the threshold voltage and sub-threshold slope cannot be easily controlled for scaling [6]. If the threshold voltage scales slower than other factors, the drive current will be reduced. Thus, a constant voltage scaling rule (CVS) was proposed to address this issue, where the voltages remain unchanged while device dimensions are scaled. However, CVS will result in an extremely high electric field, which causes unacceptable high leakage current, power consumption, and dielectric breakdown as well as hot-carrier effects [6]. To avoid the extreme cases of CES and CVS, a generalized scaling approach has been developed, where the electric field is scaled by a factor of κ while the device dimensions are scaled by a factor of α [4]. In **Table 2.1**, the scaling parameters for CES, CVS and generalized scaling schemes are compared. In reality, the CMOS technology evolution has followed mixed steps of CES, CVS, and generalized scaling.

Table 2.1. The scaling parameters for CES, CVS and generalized scaling rules.

MOSFET Device and Circuit parameters	Multiplicative Factor for MOSFET's		
	Constant E	Constant V	Generalized
Device Dimensions (T_{ox}, L_g, W, X_j)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Voltage (V)	$1/\alpha$	1	κ/α
Electric Field (E)	1	α	κ
Capacitance ($C = \epsilon A/t$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Inversion Layer Charge Density (Q_i)	1	α	κ
Circuit Delay Time ($\tau \sim CV/I$)	$1/\alpha$	$1/\alpha^2$	$1/\kappa\alpha$
Power per Circuit ($P \sim VI$)	$1/\alpha^2$	α	κ^3/α^2
Power-Delay Product per Circuit ($P\tau$)	$1/\alpha^3$	$1/\alpha$	κ^2/α^3
Circuit Density ($\propto 1/A$)	α^2	α^2	α^2
Power Density (P/A)	1	α^3	κ^3

(α : Dimensional Scaling Factor; κ : Voltage Scaling Factor)

The outstanding properties of SiO₂ have been the key element enabling the scaling of Si-based MOSFETs. A thin SiO₂ layer with band gap of ~9 eV, which is amorphous, high resistive and both thermodynamically and electrically stable, acts as an excellent insulator between Si substrate and metallic gate electrode. Conventionally, defect charge density of $< 5 \times 10^{10} / \text{cm}^2$, mid-gap interface state densities of $< 5 \times 10^{10} / \text{cm}^2$ -eV, dielectric strength of ~ 15 MV/cm, minimal low-frequency CV hysteresis and frequency dispersion (< 10 mV), minimal dielectric charging and interface degradation, and the sufficiently high carrier mobility (both electrons and holes) can be usually obtained for the MOSFETs with Si/SiO₂ system [2]. With the rapid downscaling of SiO₂

gate insulators, several limits will become inevitable, such as gate leakage current, mobility degradation and gate electrode related issues, etc., which are briefly discussed below:

1) High leakage current: It is becoming the most serious issue in the ultra-deep-submicron CMOS technology due to the large power consumption of the devices. Therefore, these high leakages are very likely to be the show-stopper for the MOSFET scaling eventually. SiO₂, as a conventional gate oxide, has enabled the vertical scaling of Si-based MOSFET for several decades due to its outstanding dielectric properties. However, the gate oxide thickness of MOSFET has been scaled from 1000 Å of the first MOSFET to around 12 Å of 65 nm technology node. Moreover, it has been demonstrated that when the physical thickness of SiO₂ becomes thinner than ~30 Å, the gate leakage current will be dominated by direct tunneling through the dielectric, and the gate leakage current through the film increases exponentially with further decrease of SiO₂ thickness according to the fundamental quantum mechanical rules [7]. This will pose serious concerns regarding the operation of CMOS devices, especially with respect to power consumption.

2) Mobility degradation: Carrier mobility (μ) in a MOSFET channel, which is a critical parameter for determining a number of transistor characteristics, such as saturation current (I_{dsat}), speed ($1/\tau$), threshold voltage (V_{th}), transconductance (G_m), sub-threshold swing (SS) and the corresponding MOSFET performances, is significantly degraded with the continuous scaling down of gate oxide thickness and the increase of

poly-Si gate doping concentration [8]. Generally, there are three scattering mechanisms to determine the inversion carrier mobility. Namely, the Coulomb charge scattering, the phonon scattering, and the surface roughness scattering [9], where Coulomb scattering may originate from different scattering centers. Coulomb scattering centers was traditionally known to be due to the substrate impurities. However, remote Coulomb scattering (RCS) has been identified to play an important role for the mobility degradation phenomena in MOSFET with thin gate oxide layer [8]. Those remote scattering centers are away from the inversion layer, and may result from the presence of ionized charges in the gate dielectric and in the depleted poly-Si gate electrodes. In addition, it has been deduced that mobility degradation may be the main limitation in gate oxide scaling down to the 9 Å regime [8]. Therefore, the problem of carrier mobility degradation is necessary to be solved for maintaining the MOSFET performance in device scaling [10].

3) Gate electrode related issues: The aggressive scaling down of MOSFET device dimension will also aggravate several problems for conventional poly-Si gate electrode, such as poly-Si gate depletion, high sheet resistance and boron penetration from the p+ doped poly-Si gate into the channel region [11]. Poly-Si depletion occurs due to insufficient active dopant density in the gate [12]. It can compromise device performance because it donates an additional thickness of about 4 Å to the capacitance equivalent thickness (CET) of the gate stack [13, 14]. It reduces the gate capacitance in the inversion regime and hence the inversion charge density, or leads to a lower effective gate voltage to the substrate. This problem is especially serious when the gate oxide scales to sub-10

Å regime. Theoretically, the high sheet resistance can be reduced by increasing the active dopant density in the poly-Si gate. However, it has been demonstrated that the active poly-Si dopant density will saturate due to the limitation of solid solubility for both n+ doped and p+ doped poly-Si [12]. Moreover, for p+ doped poly-Si, the increasing doping concentration will aggravate boron penetration phenomenon. The penetration of boron into gate dielectrics is another critical issue for conventional MOSFET with poly-Si gate electrode [15, 16], and it becomes more serious as the thickness of gate oxide layer is below 20 Å. Hence, to suppress these issues for poly-Si induced by the scaling of gate length and gate oxide thickness, it is necessary to look for a new approach.

In order to address above mentioned concerns for ultra-thin SiO₂, silicon oxynitride (SiON) and nitride/oxide stack (Si_xN_y/SiO₂) structure as the near-term gate dielectric alternatives have been proposed [11]. However, the thickness scaling limits for SiON (Si_xN_y/SiO₂) would be around 13 Å [23]. Consequently, the aggressive shrinking of gate dielectric thickness is driving the conventional SiO₂ or SiON gate dielectrics to its physical limit so alternative gate dielectric candidates have to be found for future CMOS application to meet the ITRS specifications. It is reported that the electron and hole barrier height at the SiON/Si interface, the SiON band gap energy, as well as the dielectric constant varies linearly with the N concentration in the SiON film [24, 25].

The addition of N to SiO₂ could greatly reduce the impurity (especially for boron) diffusion through the dielectric, and was suggested to be due to the particular Si–O–N bonding lattice formed in SiN and SiON [26]. Small amounts of N (~ 0.1 at. %) at or near

the Si channel interface provide the ability of controlling channel hot-electron degradation effects [25]. However, larger amounts of N near this interface will degrade device performance. A work for depositing SiN directly on the Si channel by remote plasma chemical vapor deposition (RPCVD) claimed the poor pMOS performance, with significant degradation of channel mobility and drive current [27]. This degradation mechanism is mainly attributed to excess charge of pentavalent N atoms, and hence a high defect density arising from bonding constraints imposed at the interface, which causes increased channel carrier scattering. In addition, the defect levels in the SiN layer which reside near the valence band of Si also contribute to the degradation. Oxynitride/oxide stack structure with the oxide as interfacial buffer layer is thus proposed in order to obtain the improved electrical properties [28, 29]. Due to the ultimate limitation of the dielectric constant values of oxynitride (for Si₃N₄, the k value is ~ 7.8) and its smaller band gap energy compared to SiO₂, the scaling limits for thickness of oxynitride (oxynitride/oxide stack) would be around 1.2 nm [29]. Further scaling of gate dielectrics requires other materials with higher k values.

Therefore, the needs of high- k gate oxide become more and more practical. By using high- k gate dielectric as the replacement of the conventional SiO₂ dielectric, the physical thickness, T_{physical} of the gate dielectric could be increased with the decrease of the EOT, as described by equation-2.1 below:

$$\text{EOT} = \left(\frac{3.9}{K} \right) T_{\text{physical}} \quad (2.1)$$

where 3.9 and K are the dielectric constants of SiO₂ and high- k dielectric, respectively. Hence, with the replacement of physically thicker high- k gate oxide, the tunneling current

will be significantly reduced while maintaining same gate capacitance, ensuring comparable device performance with lower leakage current, as schematically illustrated in **Fig. 2.1**.

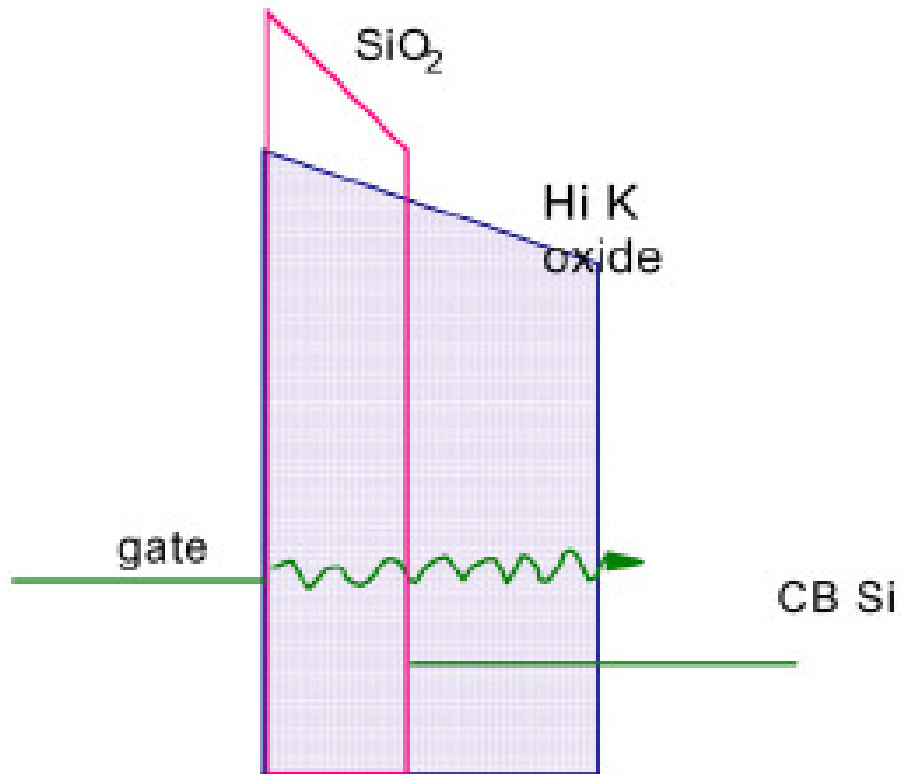


Fig. 2.1 Schematic of direct tunneling through a SiO₂ and alternative high-*k* dielectric. Physically thicker high-*k* material can reduce tunneling current [30].

2.2 Basic Requirements for High- k Gate Dielectrics

As an alternative to SiO₂ or SiON gate dielectric, high- k materials provide a substantial physically thicker dielectric layer for reduced leakage current and improved gate capacitance. Therefore, the timely implementation of high- k gate dielectric is an imperative task for maintaining the historical trend of device scaling in semiconductor industry. However, before that, all of the alternative high- k materials must meet a set of criteria, in addition to its k value, to serve as a successful gate dielectric. In this section, a systematic consideration of the selection guidelines for the appropriate high- k materials will be discussed.

2.2.1 Dielectric constant, Barrier Height and Band Gap

Theoretically, selection of a gate dielectric with a higher permittivity than that of SiO₂ is essential. However, in real fabrication processes, it cannot be assumed that the higher k value, the better the performance improvement. The required k value must be balanced with the barrier height for both electrons and holes (ΔE_C and ΔE_V) to Si, also known as conduction band offset, valence band offset, respectively, especially ΔE_C value, in the tunneling regime because the gate leakage current will increase exponentially with the decrease of barrier height for electron direct tunneling transport [15]. Since the ΔE_C and ΔE_V of many potential gate dielectrics have not been reported, the closest, most readily attainable indicator of band offset is the band gap

(E_G) of the dielectric. Generally, a large E_G corresponds to a large ΔE_C . Therefore, the E_G of the dielectric should be balanced against its k value. The k value generally increases with increasing atomic number for a given cation in a metal oxide. However, the E_G of the metal oxides tends to decrease with increasing atomic number [31]. **Fig 2.2** summarizes the relationships between k value and E_G for different gate dielectric materials. As shown, the E_G tends to decrease with increasing k value. This is the first reason that why k value for a gate dielectric candidate cannot be too high.

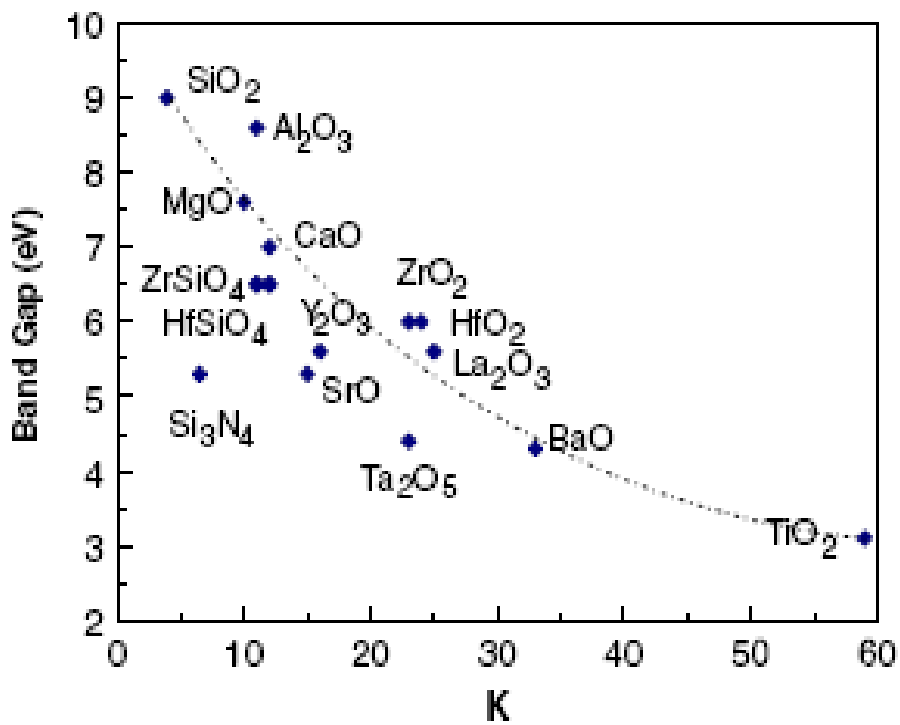


Fig. 2.2 Dielectric constant versus band gap for various gate dielectrics [32].

As discussed previously, a suitable gate dielectric oxide shall provide a reasonable conduction and valence band offset to Si, at least 1.5 eV or larger, to avoid large gate leakage. The calculated conduction and valence band offset with respect to Si for various dielectrics is shown in **Fig. 2.3**. For example, the dielectric TiO₂ has very high dielectric

constant, up to ~60, but pure TiO₂ cannot be used for gate dielectric application because of its small conduction band offset and high electron leakage currents [33]. In general, the alternate dielectric material should have a band gap of at least ~5 eV or higher to avoid unacceptable gate leakage issues.

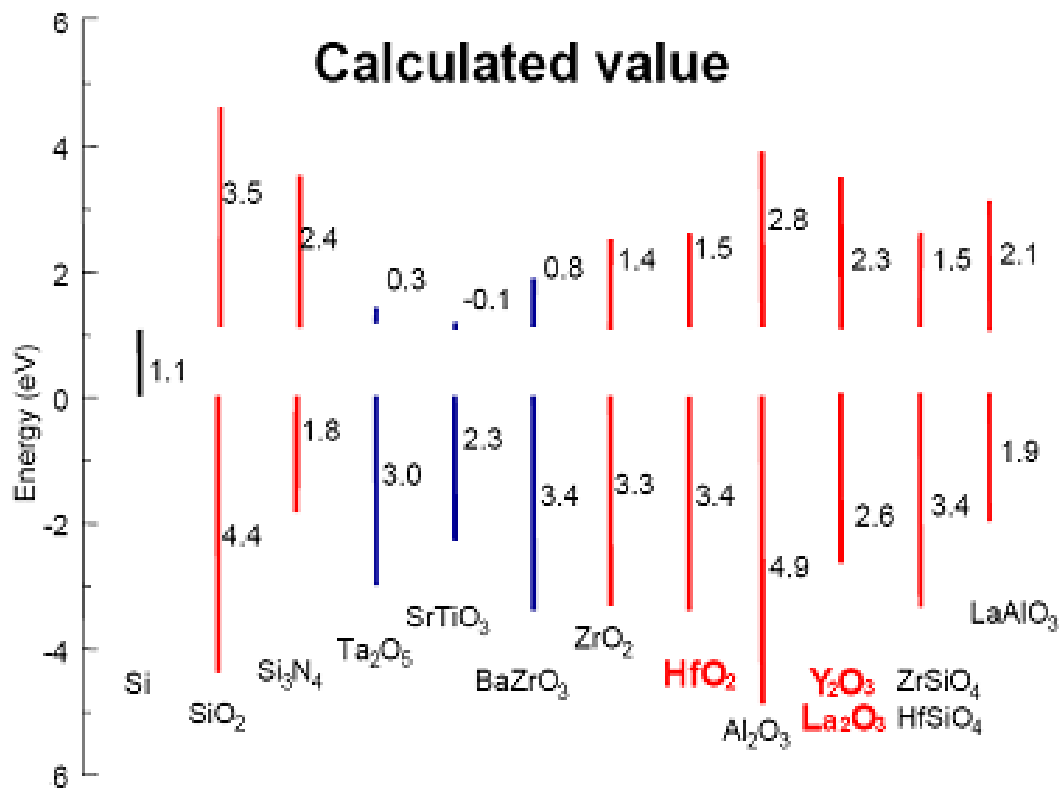


Fig. 2.3 Calculated conduction band and valence band offsets of various dielectrics on silicon [34].

In addition, it has also been reported that the dielectric materials with ultra-high *k* value may cause fringing-induced barrier lowering (FIBL) effect [35], which means that a significant fringing field at the edge of a high-*k* dielectric could lower the barrier for carriers transport into the drain, and hence seriously degrade the off-state

characteristics of the device. Therefore, it is more appropriate to find a dielectric with moderate K value for advanced CMOS gate dielectric application. With this in mind, a single high- k dielectric layer, even with k value ~ 12 – 25 , will allow a physical dielectric thickness of 35 – 50 Å, which is already thick enough to obtain the EOT required for 65 nm CMOS and beyond.

2.2.2 Thermodynamic Stability on Si and Film Morphology

As gate oxides must sit directly on the Si substrate, thus the second requirement arises from the condition that the oxides must not react with Si to form either SiO_2 or silicide during deposition or subsequent processing at elevated temperatures, such as source/drain activation annealing. This is because the resulting SiO_2 layer would increase the overall EOT and compromise the effect of using the high- k dielectric. In addition, any formed silicide would generally be metallic and would short out the field effect. However, most of the high- k materials investigated would react with the Si substrate during high thermal budget process due to their thermodynamic instability, forming an undesirable interfacial layer. Moreover, the thickness of this interfacial layer will normally increase with the temperature of the process, which results in increased EOT eventually.

In addition to good thermodynamic stability on Si, alternative high- k dielectrics should also have good kinetic stability for themselves, i.e., they must withstand the high thermal budget processing. Most of the advanced gate dielectrics are

either polycrystalline or single crystal films, but generally, those which can retain the amorphous structure throughout the subsequent processes are desirable because the polycrystalline structure for gate dielectrics would lead to undesirable interfacial growth, electrical instability and defect generation due to grain boundaries through the polycrystalline high- k layer, which may serve as high-diffusion paths for oxygen and dopant [36]. In addition, grain size and orientation changes throughout the polycrystalline dielectric layer could cause significant variations in dielectric constant, leading to inconsistent properties.

2.2.3 Channel Interface Quality

The interface with Si channel plays a key role for the realization of the high- k gate dielectrics in the advanced MOS application. Most of the high- k materials reported up to date show the interface states density (D_{it}) of $\sim 10^{11} - 10^{12}$ states/eV-cm², and a fixed charge density $\sim 10^{11} - 10^{12}$ /cm² at the interface. It is proposed that the Si-dielectric interface quality depends on the bonding constraints [37]. The interface defect density will increase proportionally if the average number of bonds per atom is higher/lower compared to that of Si, leading to an over-/under- constrained interface with Si. These metal oxide (either over- or under- constrained with respect to SiO₂) result in the formation of a high density of electrical defects near the Si-dielectric interface.

In addition, for most of the high- k materials, during their deposition on Si substrate under equilibrium conditions, there would be an undesirable and uncontrollable interfacial layer [38]. Therefore an interfacial reaction barrier should be required for better channel interface quality. The chemical stability of gate oxides on silicon in the subsequent process conditions also has a critical impact on the Si/dielectric interface quality. One step from typical CMOS process flow is the source/drain (S/D) activation annealing, which the gate stack must undergo. The typical S/D anneal is done by rapid thermal anneal technique (up to 1000 °C). If the cations from the gate dielectric diffuse into the channel region, the device electrical properties (especially the channel mobility induced by the impurity scattering) will be degraded. To control and improve the channel interface quality, the knowledge of the following for the gate dielectric is required during subsequent processing: reaction with silicon, oxygen diffusion kinetics, oxygen stoichiometry, film crystallization and component segregation.

For the high- k dielectrics with high oxygen diffusivities at high temperature, such as ZrO_2 and HfO_2 [39], rapid oxygen diffusion through the oxides could be expected when they are annealed with an excessive amount of oxygen present. And hence, the SiO_2 or SiO_2 -containing low- K interface layers would be formed, posing a serious concern regarding to EOT scalability of the high- k dielectric.

2.2.4 Carrier Mobility Issues

Mobility is a critical parameter to evaluate a high- k dielectric as the replacement to SiO₂. It is a key parameter determining a number of transistor metrics, such as saturation current, speed, threshold voltage, trans-conductance, and sub-threshold swing. It is desired to maintain the mobility of the high- k transistors close to that of the SiO₂ system.

Three scattering mechanisms determine the inversion carrier mobility: the Coulomb charge scattering, the phonon scattering, and the surface roughness scattering [40]. Surface roughness scattering dominates only when the effective field is high enough so that channel carriers are close to the Si substrate surface. It has been shown that at a high effective field (≥ 1 MV/cm), the mobility of high- k transistors becomes close to the universal mobility curve.

Coulomb scattering may originate from different scattering centers. Coulomb scattering centers was traditionally known to be due to the substrate impurities. However, remote Coulomb scattering (RCS) has been identified to play an important role for the mobility degradation phenomena in high- k transistors. These remote scattering centers are away from the inversion layer, and might be due to fixed charge, oxide trap, interface trap and micro-crystallization related to the high- k dielectric. It is reported that a thicker interfacial layer between high- k dielectric and Si substrate would lead to higher carrier mobility [41], as shown in **Fig. 2.4**, based on the results summarized from

various research groups. This suggests that the remote Coulomb scattering centers centroid is nearby the interfacial layer. A research group at International Sematech observes that the mobility increases with decreasing high- k physical thickness, which is attributed to the reduced total Coulomb scattering due to charges in the high- k [42].

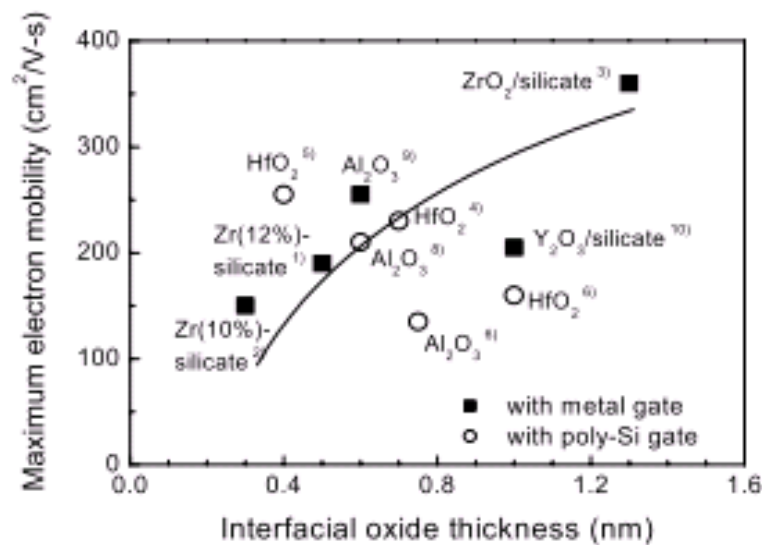


Fig. 2.4 Carrier mobility increases with the interfacial oxide thickness [41].

At low temperature, it is known that only Coulomb scattering and surface roughness scattering dominate for transistors with the SiO₂ dielectric [40], as the phonon scattering is suppressed. However, it is interesting to note that a recent study [53] suggests that soft phonons scattering in high- k dielectrics is a source of mobility degradation, by investigating the low temperature mobility of the HfO₂ transistor, and comparing it with the SiO₂ counterpart at the medium high effective electric field (when inversion charge $> 5 \times 10^{12}$ cm⁻²). On the other hand, another study on the low temperature mobility measurement [44] shows that electron mobility of HfO₂ transistor

is much lower than the SiO₂ control at the relatively low effective field, indicating the RCS is at least partly responsible for the mobility degradation in HfO₂ device.

2.2.5 Threshold Voltage Instability

Threshold voltage control is another key issue to be addressed in order to realize the high-*k* transistors in the advanced MOSFET. For the transistors with the poly-Si/HfO₂ gate stack and the poly-Si/Al₂O₃ gate stack, significant threshold voltage shift has been observed as compared to poly-Si/SiO₂ control devices [45]. It was found the respective positive and negative shifts in n- and p- MOSFETs with high-*k* gate dielectrics, and this has been interpreted as the Fermi level pinning occurring at the interface of poly-Si/HfO₂ and poly-Si/Al₂O₃ [45]. Recently, the high threshold voltage is also reported in the transistors with high-*k* gate dielectrics using metal gate electrode [46], and again the Fermi pinning was suggested to play a determining role for such an observation [46, 47].

The dopant penetration through dielectrics leads to the uncontrolled threshold voltage shift of the transistors. This issue might be more significant for high-*k* transistors compared to the device with SiO₂, as most of the high-*k* become crystalline during the S/D annealing process. N-incorporation in high-*k* dielectrics is expected to suppress the dopant penetration [48], similar as the current SiO_xN_y technology.

It was observed that charge trapping phenomena occurs in the HfO₂ gate dielectric for MOSFETs under DC uniform ($V_{ds} = 0$) static stress [49, 50], leading to severe bias temperature instability (BTI). BTI is important as it caused the device threshold voltage shift and saturation drive current decreases with electrical stressing. However, under AC ($V_{ds} \neq 0$) stressing, improvement of BTI degradation for MOSFETs with HfO₂ dielectric has been observed, and this improvement increases with increasing stress frequency [50]. It was thus concluded that the BTI should not be the “show-stopper” in realizing HfO₂ transistors for digital IC applications [50]. A model accounting for carrier trapping/de-trapping process and generation of new traps in HfO₂ dielectric under stress has been proposed to explain the frequency-dependant BTI degradation phenomena.

2.3 Metal Gate electrodes

2.3.1 Scaling Limits for Poly-Si Gate Electrode

Poly-Si was the most widely used gate electrode material for MOSFETs because it has an excellent compatibility with the self-aligned gate-first process and can be easily formed for dual gates. These merits make the poly-Si a superior gate electrode material for the gate-first CMOS process.

However, with MOSFETs scaling into the high performance 45nm technology node and beyond, some fundamental limits of poly-Si become more and more serious and tend to retard the further improvement of CMOS performance, such as poly-Si depletion, high sheet resistance and dopant penetration effect. In addition, high- k dielectrics would probably be finally required to break through the scaling limits of SiO₂ and SiON dielectrics in high performance 45nm technology and beyond. Therefore, besides the considerations from the high- k dielectrics themselves, the compatibility (or interface quality) between poly-Si and some promising high- k candidates is also a big challenge for the implementation of high- k dielectrics with the conventional poly-Si electrode.

2.3.1.1 Poly-Silicon Depletion Effect

The poly-Si depletion effect occurs when a MOS device with a poly-Si gate electrode is biased into depletion or inversion region. **Fig. 2.5** illustrates poly-Si depletion effect for a poly-Si/HfO₂ MOS device. When a positive bias is applied at the gate, a depletion layer with a finite thickness is formed at the poly-Si gate side at the poly-Si/oxide interface, associating with the non-negligible band bending in the poly-Si gate.

From an equivalent circuit diagram shown in **Fig. 2.5 (b)**, the poly-Si depletion capacitance C_{poly} is in series with the gate oxide capacitance, leading to a reduction of the gate oxide capacitance in inversion. This is equivalent to an increase of the EOT. As a result, a smaller inversion charge density is expected, and hence a reduction of the

drive current for the MOSFET device. With the aggressive scaling of the gate dielectric thickness, the poly-Si depletion effect becomes much more significant [2]. An increase of gate dielectric EOT of 5-6 Å due to poly-Si depletion effect is expected, as compared to EOT requirement (< 1 nm) in nanometer scale CMOS.

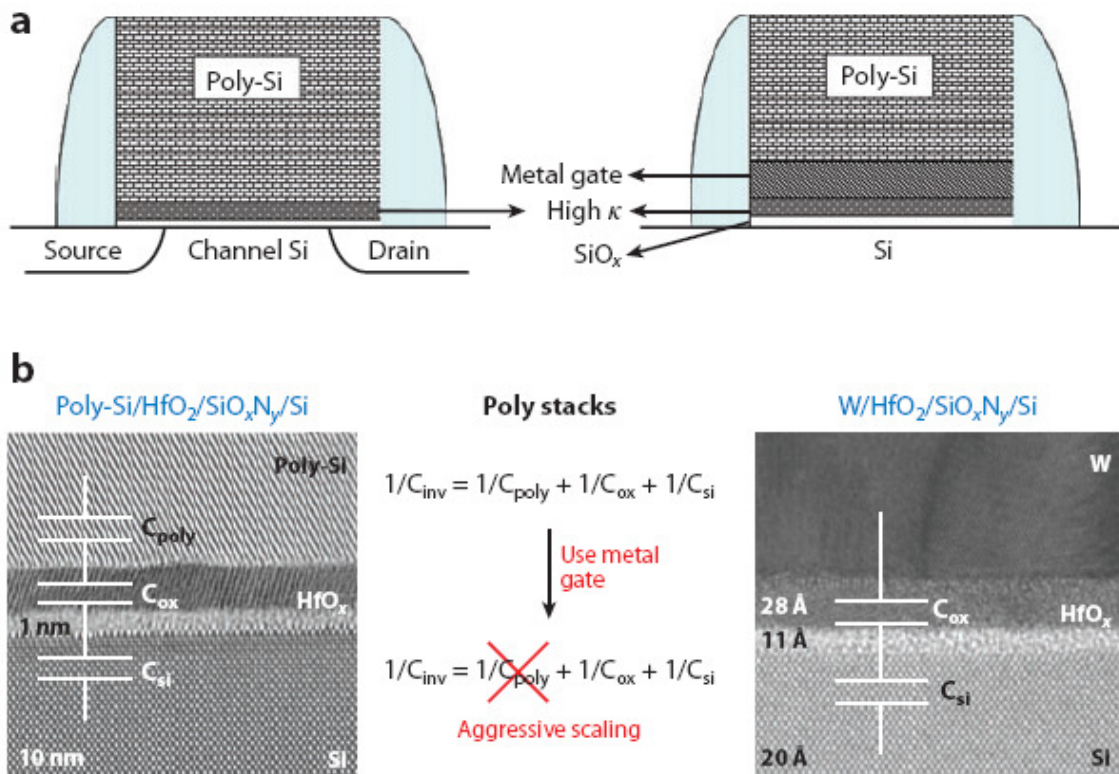


Fig. 2.5 (a) Schematics of high- k /poly-Si stacks and high- k /metal/poly-Si stacks. (b) TEM images and equivalent circuit of representative $\text{SiON}/\text{HfO}_2/\text{poly-Si}$ and $\text{SiON}/\text{HfO}_2/\text{W}$ stacks that illustrate the impact of poly depletion and the benefits of metal gates [75].

2.3.1.2 Gate Electrode Resistivity and Dopant Penetration Effect

The gate electrode resistivity is required to be scaled with the technology node. This is particularly important for MOS devices in RF application. One way to minimize the high gate resistance, as well as the poly depletion effect associated with poly-Si gate, is to increase the active dopant density in the poly-Si gate. However, it is difficult to get electrically active doping densities above 10^{20} cm^{-3} due to the limitation of the dopants solubility in the poly-Si films, especially for p+ poly-Si doped with boron [47]. Besides, for p-MOSFETs, the boron penetration through p+ poly-Si to the channel region induces threshold voltage shift and other reliability concerns for the transistors.

2.3.1.3 Fermi Level Pinning (FLP) induced V_{th} Instability

Work function of the conventional n+ poly-Si/p+ poly-Si is close to the conduction band/valence band edges of Si, and this is preferred for the optimal design of bulk n-/p-MOSFETs, respectively because of the requirements on the V_{th} and the need to use heavy dopants to control short-channel effects. However, The FLP phenomenon will occur when poly-Si gate is in contact with Hf-based high- k dielectrics, which leads to an undesirable V_{fb} shift, especially for p-MOSFETs [51]. This will lead to asymmetric high V_{th} for n- and p-MOSFETs, making these gate stacks difficult to be used for circuit design. C. Hobbs *et al.* proposed an Hf-Si bond induced dipole theory to explain the observed FLP phenomenon at the poly-Si/HfO₂ interface [52, 53], however, this theory cannot explain their own experiment that V_{fb} difference between p+ and n+ gates

decreases remarkably by a only very small amount of HfO₂ deposition. Recently, K. Shiraishi *et al.*, proposed another model in which the V_{fb} shift for p+ poly-Si on Hf-based dielectrics was attributed to the oxygen vacancy (V_o) which promoted charge transfer across the interface [54]. However, it is difficult to explain the opposite shift of V_{fb} for n+ and p+ poly-Si gates using this model. Apart from the disagreements in understanding the origin of the FLP effect, it is also a practical challenge to minimize this effect and to obtain reasonably low V_{th} for p-MOSFETs. M. Koyama *et al.* demonstrated a method to reduce the FLP effect by carefully engineering the gradient of Hf concentration in HfSiON film, where a low Hf concentration near the poly-Si/HfSiON interface is required to achieve large V_{fb} difference between n+ and p+ poly-Si [55]. But the disadvantage of this method is the overall dielectric constant of the high- k dielectric will be sacrificed. Another way to reduce the high V_{th} for p-MOSFETs is to cap the Hf-based high- k by a thin AlO_x layer in the p-MOSFET region [56, 57]. However, this will lead to a different EOT for n- and p-MOSFETs, as well as other challenges in process integration.

2.3.2 Basic Requirements for Metal Gate Electrodes

Metal gate technology has been extensively studied in recent years and it already replaced poly-Si gate in 45 nm technology node and beyond because a MG material not only eliminates the poly-Si depletion and dopant penetration problems, but also greatly reduces the gate sheet resistance. However, the insertion of MG electrodes may also bring about other new problems. Therefore, careful consideration of the choice of metals

for the gate electrode is needed. The following sections will review the basic requirements for MG candidates.

2.3.2.1 Thermal Stability Considerations

One of the most important parameters for MG candidates is their thermal stability. In conventional gate-first process, gate electrode is formed prior to the source/drain implantation and dopant activation annealing, which implies that the metal candidate and the metal-dielectric interface should be robust enough to stand up to a high thermal budget. However, the interface reaction or inter-diffusion between MG and the underlying gate dielectric always happen during the device fabrication process, wherein the interface reaction is thermodynamically driven, and likely to happen at the interface where the atoms have large differences in electronegativity and radius [58]. It has also been found that many metals with low work function (WF), like Ta, Hf, Ti and so on, tend to react with the gate dielectric at high temperature [59, 60]. On the other hand, some metals with high WF such as Pt, Ir, and Ni tend to diffuse or penetrate through the gate dielectric during the high temperature process.

In addition to the metal reaction/diffusion, some other thermal stability issues such as microstructure change, stress generation, and oxygen penetration at high-temperature should also be carefully avoided. Phase change or grain growth may affect the WF of MGs and roughen the gate-dielectric interface, leading to a change of V_{th} and

channel mobility upon annealing [61, 62]. Moreover, due to the extreme high temperature and the ultra-fast temperature ramp up/down rate used in conventional CMOS manufacturing process, the thermal induced stress would be a serious problem for MGs, especially for those who have very different expansion properties from Si and/or the underlying dielectric. The generated stress in the MOS stack will bring in some adherence problems, and even cause the metal film to crack or peel off after annealing. Besides these above-mentioned thermal stability issues, some metals also show poor barrier properties due to the diffusion of oxygen at high temperature [63]. This can lead to re-growth of the interfacial layer under the high- k dielectric due to the penetration of oxygen residues or moisture from the gas ambient during annealing, which makes it challenging to scale the EOT down to sub-1 nm.

2.3.2.2 Work Function Requirements

Another important parameter for MG candidates is their WF because it directly affects V_{th} of MOSFET, which has the most direct impact on the operation of a MOSFET. For sub-50 nm bulk-Si devices, it has been demonstrated that the optimal WF values required for NMOS and PMOS should be about 4.05 ~ 4.25 eV and 4.97 ~ 5.17 eV, respectively [64]. In other words, the WF of MGs should be within 0.2 eV from the band-edges of Si. In addition, for the fully-depleted and multi-gate devices, e.g. FDSOI or FinFET, the V_{th} will be determined only by the WF of MG since the channel region is almost intrinsic; accordingly the MGs with WF of ± 0.15 eV from the mid-gap position of Si will be best served for high-performance applications [65]. Recent study also shows

that when the body thickness of UTBSOI devices shrinks to less than 5 nm, band-edge WF will again be required due to the carrier quantization effect [66]. Therefore, metal materials with different WF values will be needed for various applications.

2.3.2.3 Process Challenges for Metal Gate Electrodes

Process integration issue is another tough challenge for the implementation of MG in CMOS fabrication. It includes metal deposition techniques, metal etching and post-etching cleaning issues, and the dual metal gate integration process.

The metal deposition techniques can affect the properties of metal gate electrode in many aspects, such as film morphology, resistivity, work function, thermal stability, and even the gate stack reliability [67-69]. The most commonly used method to deposit metal gate is physical vapor deposition (PVD) technique, including sputtering, evaporation and so on. For all the PVD deposition techniques, a fundamental limit is the step coverage issue in high aspect ratio structures [70], which may limit the applications of PVD techniques in 3-D device structures. However, this problem can be addressed by using CVD methods. The CVD methods not only have the advantages such as good step coverage and low damage to the dielectric, but they provide a number of variables, including temperature, pressure and gas flows which could be useful to control the film microstructure [70]. Among many kinds of CVD techniques, metal-organic chemical vapor deposition (MOCVD) and atomic-layer chemical vapor deposition (ALCVD) are two most important forms. Recently, ALCVD (or ALD) has drawn

considerable attention and has been utilized to deposit metal gate as well as high- k films. The major advantage of ALD technique is that it provides the ability to control the atoms layer by layer such that the film concentration and even the interface chemistry can be well engineered. However, one concern for ALD technique is its relative long lead time and hence low throughput due to the need to purge the ambient in every deposition cycle.

Metal etching and post-etching cleaning of metal gate electrodes is another practical issue for the integration of MG in CMOS process. To achieve high selectivity, vertical profile, and small feature size in the metal gate etching process, the selections of masks (photoresist or hard mask), etchant and the post-etching cleaning process need to be optimized systematically according to the properties of the specific MG materials. These practical issues can even affect the selection of metal gate candidates.

For the dual MG integration, a simple, reliable, and cost-effective scheme to integrate dual MGs on a same wafer would be desirable. The integration schemes generally fall into either metal gate first or metal gate last categories. For metal gate first integration, the gate electrode is typically patterned by dry etching at the same place in the flow as for conventional poly-Si and is therefore subjected to the source/drain anneal, which requires excellent thermal stability for both n- and p-type MG candidates, as well as refined metal etching and post-etching cleaning techniques [71, 72]. While for metal gate last integration, the gate electrode in its final state is formed much later in the flow, typically after the source/drain activation anneal, and is therefore exposed to a

much lower back-end thermal budget, which results in much less stringent requirements on the thermal stability for MG materials, but the process is relatively complex [73, 74]. There are pros and cons for both gate-first and gate-last integration. The advantages of the gate-first process over the gate-last process are the elimination of CMP steps, the retention of channel strain in both nFETs and pFETs, and the potential of obtaining conventional gate-length scaling for future technology nodes. The disadvantage of gate-first integration approach is that, owing to the requirements of high-temperature compatibility, there are restrictions on the choice of electrode and gate dielectric materials that can be used, whereas more materials flexibility is available for the gate-last scheme.

2.4 Summary

In summary, high- k /metal gate technology is a viable solution for advanced CMOS technology, especially in sub 32nm regime. However, many challenges, such as: oxygen vacancy in the high- k layer, V_t tuning of the gate stack, process integration of high- k /metal gate and reliability issues, etc, shall be addressed carefully in order to meet aggressive technology scaling requirements.

References

- [1]. G. E. Moore, "Progress in digital integrated circuit," IEDM Tech. Dig., pp. 11-13, 1975.
- [2]. International Technology Roadmap of Semiconductors (ITRS), Semiconductor Industry Association, SanJose, CA, 2001.
- [3]. R. H. Dennard, "Field-Effect Transistor Memory," U.S. Patent No. 3387286, 1968.
- [4]. G. Baccarani, M.R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to $\frac{1}{4}$ micrometer MOSFET design," IEEE Tran. Electron. Dev., vol. 31, pp. 452, 1984.
- [5]. Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, and H. S. Wong, "CMOS scaling into the nanometer regime," Proc. IEEE, vol. 85, pp. 486-504, 1997.
- [6]. Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge, U.K., Cambridge Univ. Press, 1998.
- [7]. S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra thin oxide nMOSFET's," IEEE Electron Device Lett., vol. 18, no. 5, pp. 209-211, 1997.
- [8]. M. S. Krishnan, L. Chang, T.-J. King, J. Bokor, and C. Hu, "MOSFETs with 9 to 13Å Thick Gate Oxides," in IEDM Tech. Dig., session 10, no. 1, 1999.
- [9]. S.-I. Takagi, A. Toriumi, M. Iwase and H. Tango, "On the universality of inversion layer mobility in Si MOSFETs: Part I – Effect of substrate impurity concentration," IEEE Trans. Electron Devices, vol. 41, no. 12, pp. 2357-2362, 1994.
- [10]. C. Hu, "Device Challenges and opportunities," in Symp. VLSI Tech. Dig., pp. 4-5,

2004.

[11]. International Technology Roadmap of Semiconductors (ITRS), Semiconductor Industry Association (SIA), San Jose, CA. (<http://www.itrs.net/reports.html>)

[12]. E. Josse, and T. Skotnicki, "Polysilicon gate with depletion – or – metallic gate with buried channel: what evil worse?" in IEDM Tech. Dig., pp. 661-664, 1999.

[13]. K. Roy, Hamid Mahmoodi-Meimand, and Saibal Mukhopadhyay, "Leakage control for deep-submicron circuits," Proceedings of the SPIE, vol. 5117, pp.135-146, 2003.

[14]. Ndubuisi Ekekwe, and Ralph Etienne-Cummings, "Power dissipation sources and possible control techniques in ultra deep submicron CMOS technologies," Microelectronics Journal, vol. 37, pp. 851-860, 2006.

[15]. J. R. Pfister, F. K. Baker, T. C. Mele, H. -H. Tseng, P. J. Tobin, J. D. Hayden, J. W. Miller, C. D. Gunderson, and L.C. Parrillo, "The effects of boron penetration on p+ polysilicon gated PMOS devices," IEEE Trans. Electron Devices, vol. 37, no. 8, pp. 1842-1851, 1990.

[22]. A. B. Joshi, J. Ahn and D. L. Kwong, "Oxynitride gate dielectrics for p+-polysilicon gate MOS devices," IEEE Electron Dev. Lett., vol. 14, no. 12, pp. 560-562, 1993.

[23].S. Song, W. S. Kim, J. S. Lee, T. H. Choe, J. K. Choi, M. S. Kang, U. I. Chung, N. I. Lee, K. Fujihara, H. K. Kang, S. I. Lee, and M. Y. Lee, "Design of sub-100 nm CMOSFETs: gate dielectrics and channel engineering," in Tech. Dig. VLSI Symp., pp. 190-191, 2000.

- [24]. X. Guo, and T. P. Ma, "Tunneling leakage current in oxynitride: dependence on oxygen/nitrogen content," IEEE Electron Device Lett., vol. 19, no. 6, pp. 207-209, 1998.
- [25]. M. L. Green, E. P. Gusev, R. Degraeve and E. L. Garfunkel, "Ultrathin SiO₂ and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits," J. Appl. Phys., vol. 90, no. 5, pp. 2057-2121, 2001.
- [26]. K. A. Ellis and R. A. Buhrman, "Time-dependent diffusivity of boron in silicon oxide and oxynitride," Appl. Phys. Lett. vol. 74, pp. 967-969, 1999.
- [27]. H. Yang and G. Lucovsky, "Integration of ultrathin (1.6~2.0 nm) RPECVD oxynitride gate dielectrics into dual poly-Si gate submicron CMOSFETs," in Tech. Dig. Int. Electron Devices Meet., pp. 245-248, 1999.
- [28]. S. C. Song, H. F. Luan, C. H. Lee, A. Y. Mao, S. J. Lee, J. Gelpey, S.- Marcus, and D. L. Kwong, "Ultra Thin high quality stack nitride/oxide gate dielectrics prepared by in-situ rapid thermal N₂O oxidation of NH₃-Nitrided Si," in Dig. 1999 Symp. VLSI., pp. 137-138, 1999.
- [29]. H. Y. Yu, Y. T. Hou, M. F. Li, and D.-L. Kwong, "Hole Tunneling Current through Oxynitride/Oxide Stack and the Stack Optimization for p-MOSFET's", IEEE Electron Dev. Lett., vol. 23, pp. 285-287, 2002.
- [30]. Lo S H, Buchanan D A, Taur Y and Wang W 1997 IEEE Electron Device Lett. 18, 209.
- [31]. J. Kwo, M. Hong, A. R. Kortan, K. T. Queeney, Y. J. Chabal, J. P. Mannaerts, T. Boone, J. J. Krajewski, A. M. Sergent, and J. M. Rosamilia, "High ϵ gate

dielectrics Gd_2O_3 and Y_2O_3 for silicon,” *Appl. Phys. Lett.*, vol. 77, no. 1, pp. 130-132, 2000.

[32]. Gusev EP, Narayanan V, Frank MM. 2006. Advanced high- κ dielectric stacks with poly-Si and metal gates: recent progress and current challenges. *IBM J. Res. Dev.* 50:387–410.

[33]. Campbell SA, Kim H-S, Gilmer DC, He B, Ma T, Gladfelter WL. 1999. Titanium dioxide (TiO_2)-based gate insulators. *IBM J. Res. Dev.* 43:383–92.

[34]. Robertson J 2000 *J. Vac. Sci. Technol. B* 18 1785.

[35]. B. Cheng, M. Cao, R. Rao, A. Inani, P. V. Voorde, W. M. Greene, J. M. C. Stork, Z. Yu, P. M. Zeitzoff, and J. C. S. Woo, “The impact of high- κ gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs,” *IEEE Tran. Electron. Dev.*, vol. 46, no. 7, pp.1537-1544, 1999.

[36]. S. H. Bae, C. H. Lee, R. Clark, and D. L. Kwong, “MOS Characteristics of Ultrathin CVD HfAlO Gate Dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 556-558, 2003.

[37]. G. Lucovsky, Y. Wu, H. Niimi, V. Misra, and J. C. Phillips, “Bonding constraints and defect formation at interfaces between crystalline silicon and advanced single layer and composite gate dielectrics,” *Appl. Phys. Lett.*, vol. 74, pp. 2005-2007, 1999.

[38]. G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-K gate dielectrics: Current status and materials properties considerations,” *J. Appl. Phys.* vol. 89, no. 10, pp. 5243-5275, 2001.

[39]. A. Kumar, D. Rajdev, and D. L. Douglass, *J. Am. Chem. Soc.* vol. 55, p.439, 1972.

- [40]. S.-I. Takagi, A. Toriumi, M. Iwase and H. Tango, "On the universality of inversion layer mobility in Si MOSFETs: Part I – Effect of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 47, pp.2357-2362, 1994.
- [41]. M. Hiratani, S. Saito, Y. Shimamoto, K. Torii, "Effective electron mobility reduced by remote charge scattering in high-kappa gate stacks" *Jpn. J. Appl. Phys.* Vol. 41, pp.4521-4522, 2002.
- [42]. R. W. Murto, M. I. Gardner, G.A. Brown, P.M. Zeitzoff, H.R. Huff, "Challenges in gate stack engineering," *Solid-State Technology*, pp. 43-47, Oct. 2003.
- [43]. Z. Ren, M.V. Fischetti, E.P. Gusev, E.A. Cartier, and M. Chudzik, "Inversion Channel Mobility in high-*k* high performance MOSFET's," in *IEDM Tech. Dig.*, 2003.
- [44]. F. Lime, K. Oshima, M. Casse, G. Ghibaudo, S. Cristoloveanu, B. Guillaumot, H. Iwai, "Carrier mobility in advanced CMOS devices with metal gate and HfO₂ gate dielectric," *Solid-State Electronics*, vol. 47, pp. 1617-1621, 2003.
- [45]. C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, G. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface", in *Symp. VLSI Tech. Dig.*, pp. 9-10, 2003.
- [46]. S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. Fonseca, A. Demkov, J. Scheaffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, G. Anderson, K. Moore, H. Tseng, C. Capasso, O. Adetutu, D. Gilmer, W. Taylor, R. Hedge, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates," in *Tech. Dig. IEDM*, 2003, pp. 307-310.

- [47]. Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology", *J. Appl. Phys.*, vol. 92, pp. 7266-7271, 2002.
- [48]. M. A. Quevedo-Lopez, M. El-Bouanani, M. J. Kim, B. E. Gnade, R. M. Wallace, M. R. Visokay, A. LiFatou, J. J. Chambers, and L. Colombo, "Effect of N incorporation on boron penetration from p+ polycrystalline-Si through HfSixOy films," *Appl. Phys. Lett.*, vol. 82, p. 4669, 2003 .
- [49]. S. Zafar, B.H. Lee, and J. Stathis, "Evaluation of NBTI in HfO₂ Gate-Dielectric Stacks with Tungsten Gates," *IEEE Electron Dev. Lett.*, vol. 25, pp. 153-155, 2004.
- [50]. C. Shen, H.Y. Yu, X.P. Wang, M.F. Li, Y.C. Yeo, DSH Chan, K.L. Bera, D.L. Kwong, "Frequency Dependent Dynamic Charge Trapping in HfO₂ and Treshold Voltage Instability in MOSFETs," 2004 International Reliability Physics Symposium (IRPS-2004), AZ, USA, Apr. 2004.
- [51]. C. W. Yang, Y. K. Fang, Ch. H. Chen, S. F. Chen, C. Y. Lin, C. S. Lin, M. F. Wang, Y. M. Lin, T. H. Hou, C. H. Chen, L. G. Yao, S. C. Chen, and M. S. Liang, "Effect of polycrystalline-silicon gate types on the opposite flatband voltage shift in n-type and p-type metal-oxide-semiconductor field-effect transistors for high-*k*-HfO₂ dielectric," *Appl. Phys. Lett.*, vol. 83, no. 2, pp. 308-310, 2003.
- [52]. C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, G. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface", in *Symp. VLSI Tech. Dig.*, pp. 9-10, 2003.

- [53]. C. Hobbs, L. Fonseca, A. Knizhnik, V. Dhandapani, S. Samavedam, W. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, M. Lovejoy, R. Rai, E. Hebert, H. Tseng, S. Anderson, B. White, and P. Tobin, "Fermi-level pinning at the polysilicon/metal oxide interface," IEEE Tran. Electron. Dev., vol. 51, pp. 971-984, 2004.
- [54]. K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikado, "Physics in Fermi level pinning at the polySi/Hf-based high- k oxide interface," in Symp. VLSI Tech. Dig., pp. 108-109, 2004.
- [55]. M. Koyama, Y. Kamimuta, T. Ino, A. Kaneko, S. Inumiya, K. Eguchi, M. Takayanagi, and A. Nishiyama, "Careful examination on the asymmetric V fb shift problem for poly-Si/HfSiON gate stack and its solution by the Hf concentration control in the dielectric near the poly-Si interface with small EOT expense," in IEDM Tech. Dig., pp. 499-502, 2004.
- [56]. H.-S. Jung, J.-H. Lee, S. K. Han, Y.-S. Kim, H. J. Lim, M. J. Kim, S. J. Doh, M. Y. Yu, N.-I. Lee, H.-L. Lee¹, T.-S. Jeon, H.-J. Cho, S. B. Kang, S. Y. Kim, I. S. Park, D. Kim, H. S. Baik, Y. S. Chung, "A highly manufacturable MIPS (metal inserted poly-Si stack) technology with novel threshold voltage control," in Symp. VLSI Tech. Dig., pp. 232-233, 2005.
- [57]. H.-J. Li and M. Gardner, "Dual high- k gate dielectric with poly gate electrode: HfSiON on nMOS and Al₂O₃ capping layer on pMOS," IEEE Electron Device Lett., vol. 26, no. 7, pp. 441-443, 2005.
- [58]. J. K. Schaeffer, S. B. Samavedam, D. C. Gilmer, V. Dhandapani, P. J. Tobin, J. Mogab, B.-Y. Nguyen, B. E. White, Jr., S. Dakshina-Murthy, R. S. Rai, Z.-X.

- Jiang, R. Martin, M. V. Raymond, M. Zavala, L. B. La, J. A. Smith, R. Garcia, D. Roan, M. Kottke, and R. B. Gregory, "Physical and electrical properties of metal gate electrodes on HfO₂ gate dielectrics," *J. Vac. Sci. Technol. B*, vol. 21, no. 1, pp. 11-17, 2003.
- [59]. V. Misra, G. P. Heuss, and H. Zhong, "Use of metal-oxide-semiconductor capacitors to detect interactions of Hf and Zr gate electrodes with SiO₂ and ZrO₂," *Appl. Phys. Lett.*, vol. 78, no. 26, pp. 4166-4168, 2001.
- [60]. T. Ushiki, K. Kawai, I. Ohshima, and T. Ohmi, "Chemical reaction concerns of gate metal with gate dielectric in Ta gate MOS devices: an effect of self-sealing barrier configuration interposed between Ta and SiO₂," *IEEE Trans. Electron Devices*, vol. 47, no.11, pp. 2201-2207, 2000.
- [61]. S. H. Bae, W. P. Bai, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D. L. Kwong, "Laminated metal gate electrode with tunable work function for advanced CMOS," in *Symp. VLSI Tech. Dig.*, pp. 188-189, 2004.
- [62]. M.-F. Wang, T.-Y. Huang, Y.-C. Kao, H.-C. Lin, and C.-Y. Chang, "Impact of thermal stability on the characteristics of complementary metal oxide semiconductor transistors with TiN metal gate," *Jpn. J. Appl. Phys.*, vol. 41, pp. 546-551, 2002.
- [63]. H. Y. Yu, J. F. Kang, J. D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M.-F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du, and D.-L. Kwong, "Thermally robust high quality HfN/HfO₂ gate stack for advanced CMOS devices," in *IEDM Tech. Dig.*, pp. 99-103, 2003.

- [64]. I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate workfunction on device performance at the 50 nm technology node," *Solid State Electronics*, vol. 44, no. 6, pp. 1077-1080, Jun. 2000.
- [65] B. Cheng, B. Maiti, S. Samavedam, J. Grant, B. Taylor, P. Tobin, and J. Mogab, "Metal gates for advanced sub-80-nm SOI CMOS technology," in *IEEE Intl. SOI Symp.Proc.*, pp. 91-92, 2001.
- [66] T. Low, M. F. Li, W. J. Fan, S. T. Ng, Y. Yeo, C. Zhu, A. Chin, L. Chan, and D. L. Kwong, "Impact of surface roughness on silicon and germanium ultra-thin-body MOSFETs," in *IEDM Tech. Dig.*, pp. 151-154, 2004.
- [67]. Y. H. Kim, C. H. Lee, T. S. Jeon, W. P. Bai, C. H. Choi, S. J. Lee, L. Xinjian, R. Clarks, D. Roberts, and D. L. Kwong, "High quality CVD TaN gate electrode for sub-100nm MOS devices," in *IEDM Tech. Dig.*, pp. 667-670, 2001.
- [68]. D.-G. Park, Z.J. Luo, N. Edleman, W. Zhu, P. Nguyen, K. Wong, C. Cabral1, P. Jamison1, B.H. Lee, A. Chou, M. Chudzik, J. Bruley, O. Gluschenkov, P. Ronsheim, A. Chakravarti, R. Mitchell, V. Ku, H. Kim1, E. Duch1, P. Kozlowski1, C.D'Emic1, V. Narayanan1, A. Steegen, R. Wise, R. Jammy1, R. Rengarajan, H. Ng, A. Sekiguchi, and C.H. Wann, "Thermally robust dual-work function ALD-MN x MOSFETs using conventional CMOS process flow," in *Symp. VLSI Tech. Dig.*, pp. 186-187, 2004.
- [69]. J. C. Hooker, R.J.P Lander, F.N. Cubaynes, T. Schram, F. Roozeboom, J. van Zijl, M. Maas, F.C. van den Heuvel, E.P. Naburgh, J.G.M. van Berkum, Y. Tamming, T. Dao, K. Henson, M. Schaekers, A. van Ammel, Z. Tokei, M. Demand, C. Dachs, "Tantalum-

based gate electrode metals for advanced CMOS applications,” Proc. 207th ECS meeting, 632, Quebec, Canada, 2005.

[70]. S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era, Volume 1*, 2nd Edition, California, Lattice Press, 2000, ch. 11 & ch. 6.

[71]. S. B. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, E. Luckowski, J. Schaeffer, M. Zavala, R. Martin, V. Dhandapani, D. Triyoso, H. H. Tseng, P. J. Tobin, D. C. Gilmer, C. Hobbs, W. J. Taylor, J. M. Grant, R. I. Hegde, J. Mogab, C. Thomas, P. Abramowitz, M. Moosa, J. Conner, J. Jiang, V. Arunachalam, M. Sadd, B.-Y. Nguyen, and B. White, “Dual-metal gate CMOS with HfO₂ gate dielectric,” in *IEDM Tech. Dig.*, pp. 433-436, 2002.

[72]. Z. B. Zhang, S. C. Song, C. Huffman, J. Barnett, N. Moumen, H. Alshareef, P. Majhi, M. Hussain, M.S. Akbar, J.H. Sim, S.H. Bae, B. Sassman, and B.H. Lee, “Integration of dual metal gate CMOS with TaSiN (NMOS) and Ru (PMOS) gate electrodes on HfO₂ gate dielectric,” in *VLSI Tech. Dig.*, pp. 50-51, 2005.

[73]. I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, “Dual work function metal gate CMOS technology using metal interdiffusion,” *IEEE Electron Device Lett.*, vol. 22, pp. 444-446, Sep. 2001.

[74]. C. Ren, H. Y. Yu, J. F. Kang, X. P. Wang, H. H. H. Ma, Yee-Chia Yeo, D. S. H. Chan, M.-F. Li, and D.-L. Kwong, “A dual-metal gate integration process for CMOS with sub-1 nm EOT HfO₂ by using HfN replacement gate,” *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 580-582, 2004.

[75]. S. Guha and V. Narayanan, “High-κ /Metal Gate Science and Technology”, *Annu. Rev. Mater. Res.* 2009.39:181-202.

CHAPTER 3 Experimental Procedure and Set-ups

3.1 Device Fabrication

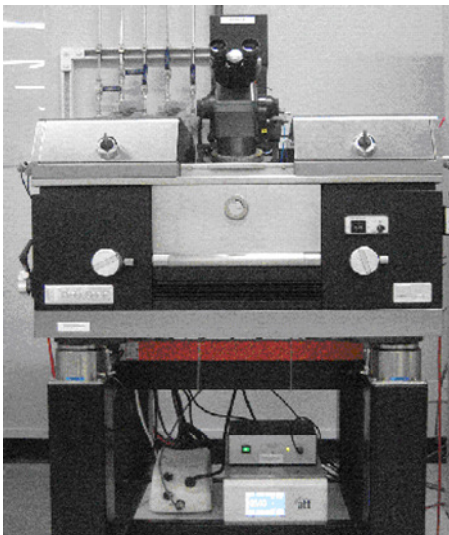
The devices studied in this project are mainly fabricated in NTU Nanyang Nano Fabrication Center (N2FC) Clean Room 1 (CR1) or sent from our collaborators, e.g. Taiwan Semiconductor Manufacturing Company (TSMC), ASM Microchemistry Ltd, Finland.

The process flow of high- k /metal gate MOSCAP fabricated in NTU N2FC CR1 is summarized in **Fig 3.1**. Capacitors were fabricated on p-type (100) Si substrate. After standard Radio Corporation of America (RCA) clean, ~ 5500 Å field oxide was thermally grown, followed by active area definition. high- k dielectric was then deposited by ALD. Post-deposition annealing is widely used to improve the electrical property of high- k film, notably hysteresis. After that, metal gate was deposited and patterned. Finally, forming gas annealing was performed for interface states passivation. For MOSFET devices, the source/drain ion implantation and dopant activation annealing steps were added accordingly. The detailed device fabrication process of each sample for different topics would be described in Experimental part of the following chapters.

3.2 Device Characterization

3.2.1 Electrical Characterization

After fabrication of the devices, the electrical and physical characterization would be performed. The equipment used for electrical characterization is an Suss PM8 200 mm manual probe station and a Keithley 4200 Semiconductor Characterization system, which are shown in **Fig. 3.2(a) & (b)**, respectively.



(a)



(b)

Fig. 3.2 (a) Suss PM8 200 mm manual probe station and (b) Keithley 4200 Semiconductor Characterization System.

The Suss PM8 200 mm manual probe station serves as a platform for all the related electrical measurements. Its main components are a probe chamber, a microscope, a gas distribution panel, a vibration isolation table and a chuck and platen controls. The Keithley 4200 Semiconductor Characterization System is mainly used to perform all the related electrical measurements. It consists of four highly accurate source-monitor units (SMUs) with a current resolution of 0.1 fA as shown in **Fig. 3.2(b)**. These SMUs are separately connected to four probe heads placed on the Suss 200 mm manual wafer probe station via Kelvin tri-axial cables with low leakage currents. These probe heads are primarily used to steadily hold the tungsten needles, which can separately connect device terminals or the ground.

Besides standard Capacitance-Voltage ($C-V$) and Current-Voltage ($I-V$) measurement, other electrical measurement techniques such as: split $C-V$, Conductance-Frequency ($G-\omega$), Gate dielectric relaxation current measurement, etc. were also frequently adopted to investigate the device performance thoroughly.

3.2.1.1 Split $C-V$ measurement

The split $C-V$ measurement is a widely accepted technique to extract the MOSFET effective channel carrier mobility. The basic MOSFET device equation tells that the drain current is proportional to the carrier mobility. However, the carrier mobility is dependent on the gate voltage or the transverse electric field applied. Accurate measurement of mobility at different effective electric field is important to device characterization.

The effective mobility is defined as:

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_d}{V_{ds}} \cdot \frac{1}{Q_{inv}} \Big|_{V_{ds} \rightarrow 0} \quad (3.1)$$

where I_d is the drain current, and Q_{inv} is the total inversion charge in the channel per unit area. Two quantities, I_d and Q_{inv} are to be measured to calculate the effective mobility as a function of gate voltage. The drain current is measured under a gate bias sweep, and a constant drain voltage bias. To measure the charge density, in the inversion layer, the split $C-V$ experiment is used.

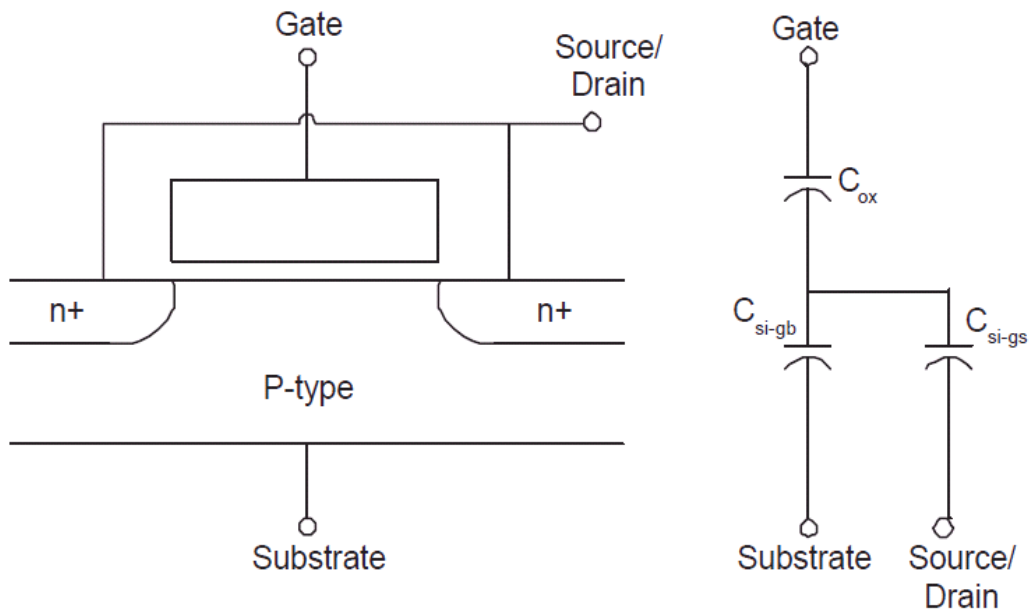


Fig. 3.3 Equivalent circuit of MOSFET in split $C-V$ measurement.

In the split C - V scheme, the MOSFET transistors are modeled by the equivalent circuit diagram as shown in **Fig. 3.3**. The charging and discharging of the minority carriers in the inversion layer gives rise to an inversion capacitance C_{Si-gs} , and is in parallel with the substrate capacitance C_{Si-gb} arising from the space charge of the depletion region. Both C_{Si-gs} and C_{Si-gb} are in series with the capacitance of the gate dielectric C_{ox} , and form the channel capacitance and the bulk capacitance:

$$C_{gs} = C_{ox} \cdot C_{Si-gs} / (C_{ox} + C_{Si-gs}) \quad (3.2)$$

$$C_{gb} = C_{ox} \cdot C_{Si-gb} / (C_{ox} + C_{Si-gb}) \quad (3.3)$$

By separately measuring the bulk capacitance density (C_{gb}) and the channel capacitance density (C_{gs}), the transistor C - V curve is split into two separate curve, reflecting capacitance arising from inversion charge and depletion charge, respectively. One can further evaluate the inversion and depletion charge density, as a function of V_g , by:

$$Q_{inv} = \frac{1}{W \cdot L} \int_{-\infty}^{V_g} C_{gs} dV \quad (3.4)$$

$$Q_{depl} = \frac{1}{W \cdot L} \int_{V_{fb}}^{V_g} C_{gb} dV \quad (3.5)$$

The extraction of effective mobility involves two independent measurements: the split C - V measurements for bulk and channel capacitance, and the I - V measurement for

channel conductance. The bulk capacitance measurement is performed with the set-up shown in Fig. 3.4. The Agilent 4284A LCR meter is controlled by a computer program through the GPIB interface, to perform the $C-V$ sweep. During the $C-V$ measurement, the 2 terminals of Agilent meter, namely, CV high and CV low are connected to the gate and substrate of the MOSFET, respectively, while source and drain remain grounded.

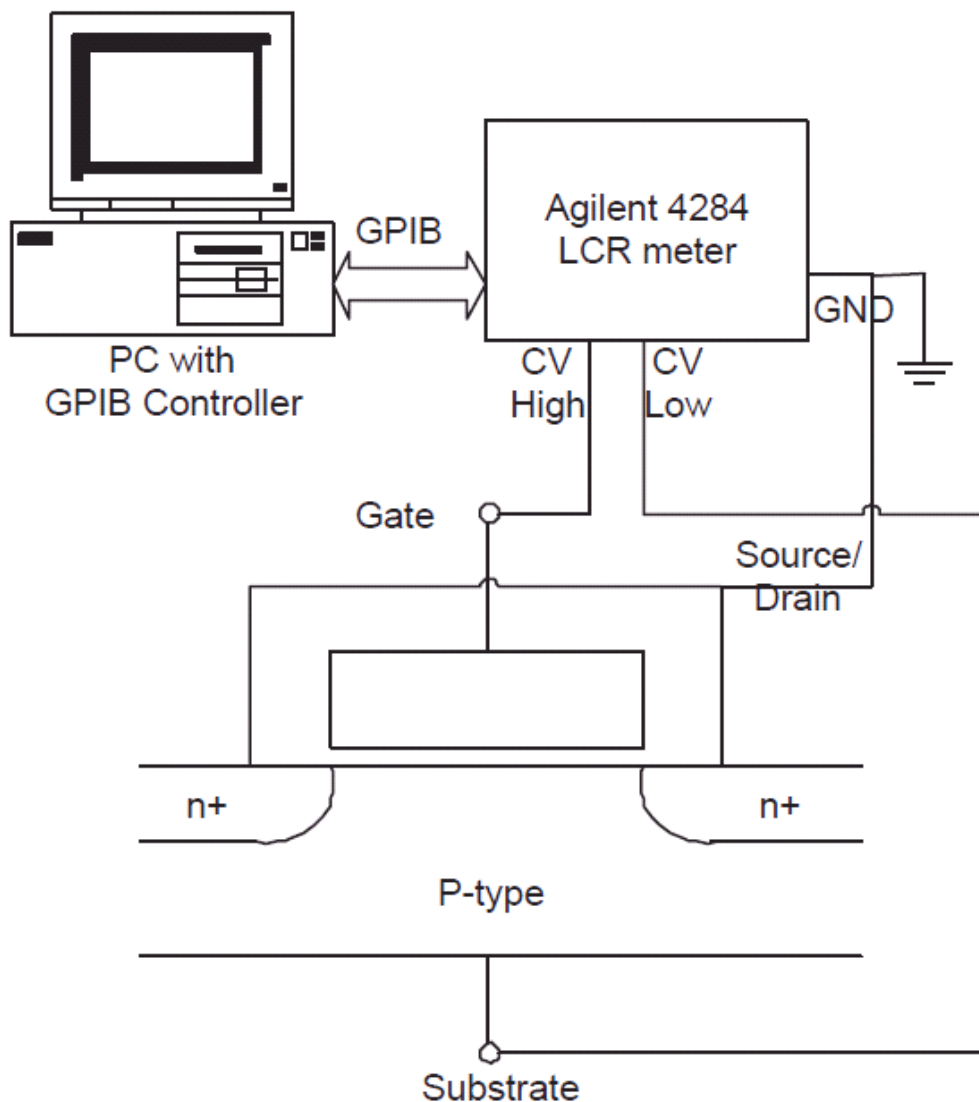


Fig. 3.4 The experimental set-up of bulk capacitance measurement.

The I - V measurement is performed by standard HP 4156A precision semiconductor parameter analyzer. Similarly, for channel capacitance measurement, the CV low terminal is connected to source and drain and the substrate is grounded, while other settings remain unchanged.

3.2.1.2 Conductance-Frequency (G - ω) measurement

Interface trapped charge, also known as interface traps or states (D_{it}) are attributed to the dangling bonds at the semiconductor/insulator interface. Their density is most commonly reduced by forming gas anneal. The conductance method is one of the most sensitive techniques to determine D_{it} [1]. It yields D_{it} in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuations. The technique is based on measuring the equivalent parallel conductance G_P of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in **Fig. 3.5 (a)**. It consists of the oxide capacitance C_{ox} , the semiconductor capacitance C_s , and the interface trap capacitance C_{it} . The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it} . It is convenient to replace the circuit of **Fig. 3.5 (a)** by that in **Fig. 3.5 (b)**, where C_P and G_P are given by:

$$C_P = C_S + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \quad (3.6)$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \quad (3.7)$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it} * C_{it}$, the interface trap time constant.

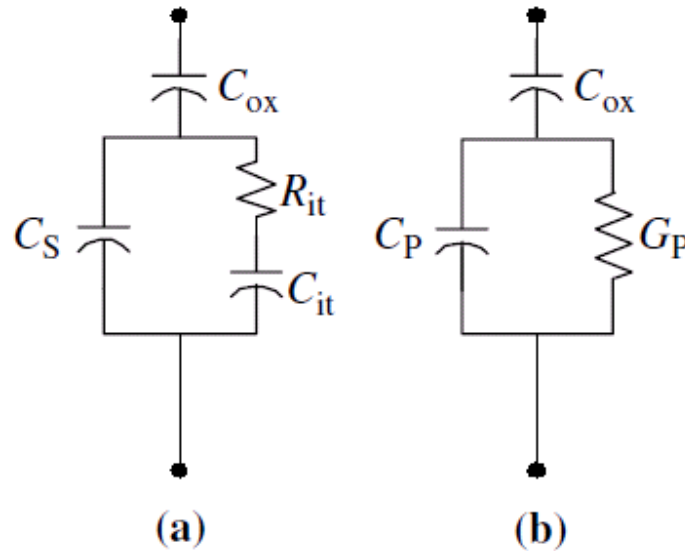


Fig. 3.5 Equivalent circuits for conductance measurements: (a) MOS-C with interface trap time constant $\tau_{it} = R_{it} * C_{it}$, (b) simplified circuit of (a).

The conductance is measured as a function of frequency and plotted as G_P / ω versus ω . G_P / ω has a maximum at $\omega = 1 / \tau_{it}$ and at that maximum $D_{it} = 2G_P / q \omega$. Hence D_{it} can be determined from the maximum G_P / ω and τ_{it} can be determined from ω at the

peak conductance location on the ω -axis. An approximate expression giving the interface trap density in terms of the measured maximum conductance is:

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_P}{\omega} \right)_{\max} \quad (3.8)$$

The conductance measurement must be carried out over a wide frequency range, the portion of the band gap probed by conductance measurements is typically from flatband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50 mV or less to prevent harmonics of the signal frequency giving rise to spurious conductances. The conductance depends only on the device area for a given D_{it} .

3.2.1.3 Gate dielectric relaxation current measurement

Gate dielectric relaxation current measurement is one of frequently used techniques that can indicate the integrity of the dielectric [2], namely, there is no measurable relaxation current after dielectric breakdown. The dielectric relaxation current has significant impact on the performance of MOS devices with high- k dielectric, such as the drive current variation, V_{th} instability and high frequency properties, etc. Traditionally, the origin of the observed dielectric relaxation current is attributed to dielectric material polarization relaxation induced by carrier hopping in double potential well [3].

For dielectric relaxation current measurement in this project, a constant voltage V_g stressing is applied to gate electrode initially, as shown in **Fig. 3.6**. V_g is switched off as preset after a fixed time of stressing, which is also the time “0” for measuring dielectric relaxation current.

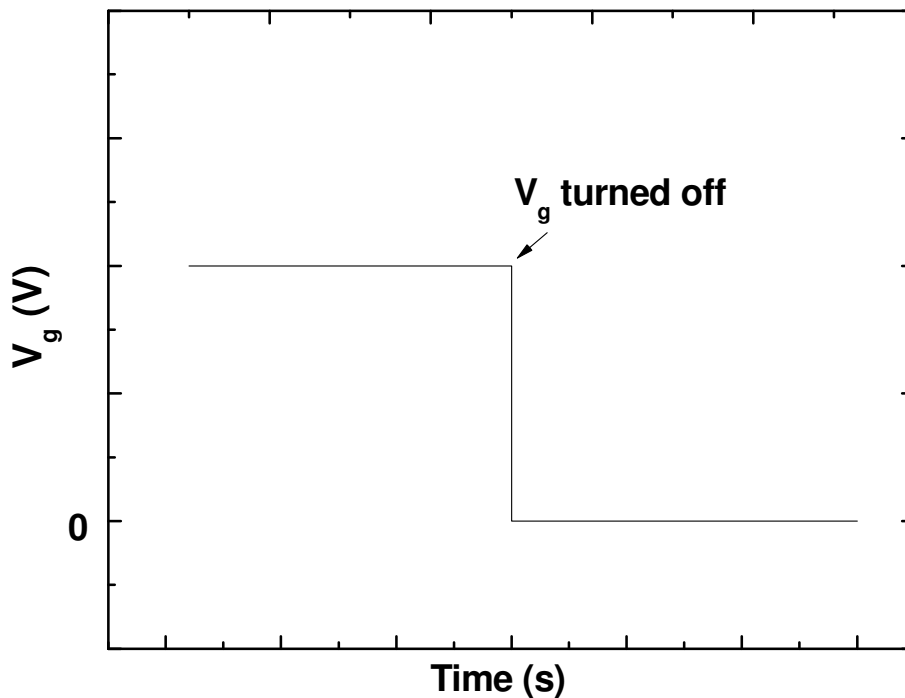


Fig. 3.6 Illustration of applied stressing voltage on gate electrode during dielectric relaxation current measurement.

Recently, after a series of systematic study on thickness dependence, gate voltage polarity dependence and temperature dependence of the relaxation current in high- k dielectric stacks, it is reported that the charge trapping and de-trapping at high- k /SiO₂ interface are mainly responsible for the dielectric relaxation current in high- k dielectric materials [4]. Thus, the interface trap information of the high- k /SiO₂ dielectric can be

obtained qualitatively by comparing the amplitude of the gate dielectric relaxation current of different gate stacks.

3.2.2 Physical Characterization

To gain in-depth understanding of the electrical behaviors of the devices and reveal mechanisms behind, physical characterization is usually applied to correlate with the results collected by electrical measurement, such as: X-ray Photoelectron Spectroscopy (XPS), Scanning Tunneling Microscopy (STM), High Resolution Transmission Electron Microscopy (HRTEM), Electron Energy Loss Spectroscopy (EELS), and X-Ray Diffraction (XRD), etc. Among all the techniques aforementioned, XPS and STM are the two important and powerful methods to characterize materials and to provide physical evidences to the hypothesis concluded from the electrical measurements in this project.

3.2.2.1 X-ray photoelectron spectroscopy

XPS is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a beam of X-rays on the materials to be analyzed while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material. XPS requires ultra-high vacuum (UHV) conditions. The basic components and working principle of an XPS system is shown in **Fig. 3.7**.

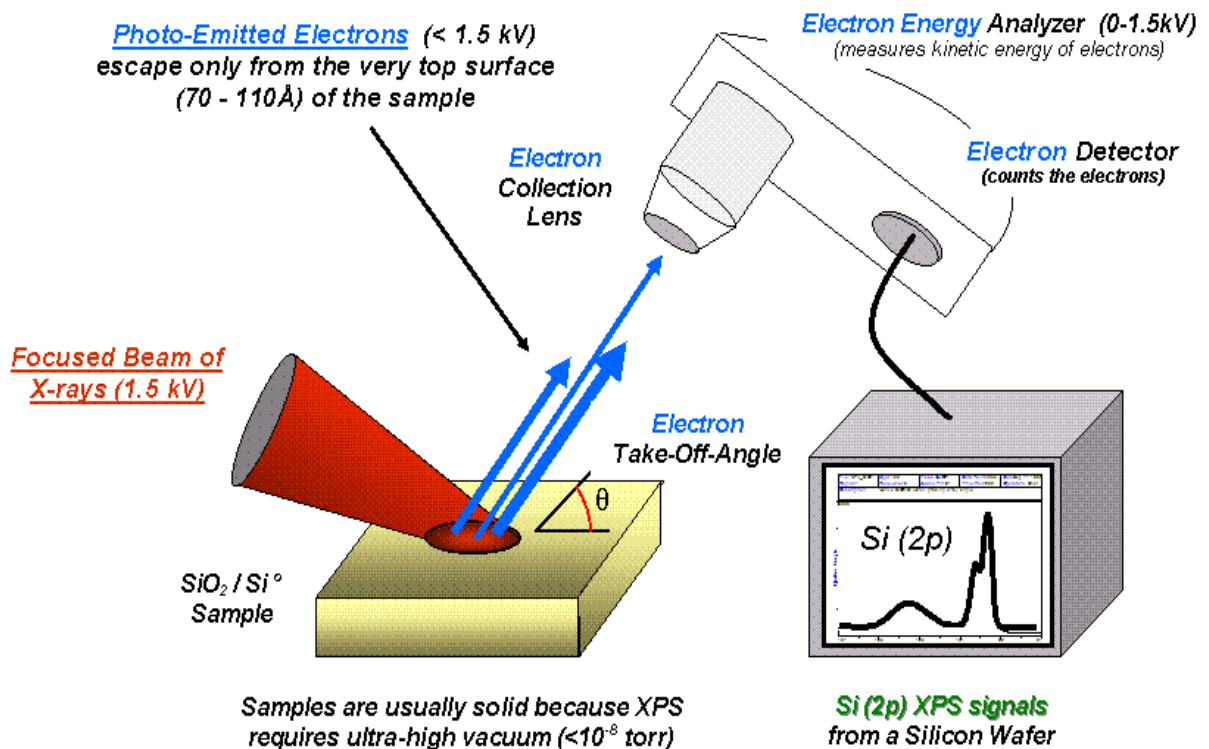


Fig. 3.7 Illustration of basic components and working principle of an XPS system [5].

During analysis, the chemical identification of the elements in the top atomic layers of a sample is done by recording the binding energies (BE) of the electrons associated with these atoms. Furthermore, because the binding energies differ not only from chemical species to species, but also vary with the bonding conditions in which the element is found, this technique also provides information on the actual compounds present on the surface. In essence, it probes the electronic structure of the surface. When used in combination with sputter depth profiling, in which Argon ions are used to remove surface layers from a sample, XPS provides elemental information about the depth profile of a sample. XPS can be used to analyze the surface chemistry of a material in its "as

received" state, or after some treatment, for example: fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some of the surface contamination, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light.

The Mg K α (1253.6 eV) or Al K α (1486.6 eV) are normally used as X-ray sources because their photons have limited penetrating capability in a solid. They interact with atoms in the sample surface region by the photoelectric effect, causing electrons to be emitted, whose kinetic energy (KE) can be calculated by:

$$KE = h\nu - BE - \Phi_s \quad (3.9)$$

where $h\nu$ is the energy of the photon, BE is the binding energy of the atomic orbital which the electron emitted, and Φ_s is the spectrometer work function. The binding energy may be regarded as ionization energy of the atom for the particular shell involved. There is a corresponding variety of kinetic energy of the emitted electrons since there are a variety of possible ions from each type of atom. The electrons leaving the sample are detected by an electron spectrometer according to their kinetic energy and therefore the chemical information of the sample can be identified.

3.2.2.2 Scanning tunneling microscope

STM provides a picture of the atomic arrangement of a surface by sensing corrugations in the electron density of the surface that arise from the positions of surface atoms. The components of an STM include scanning tip, which is usually made by tungsten, piezoelectric controlled height and x,y scanner, coarse sample-to-tip control, vibration isolation system, and computer, as shown in **Fig. 3.8**.

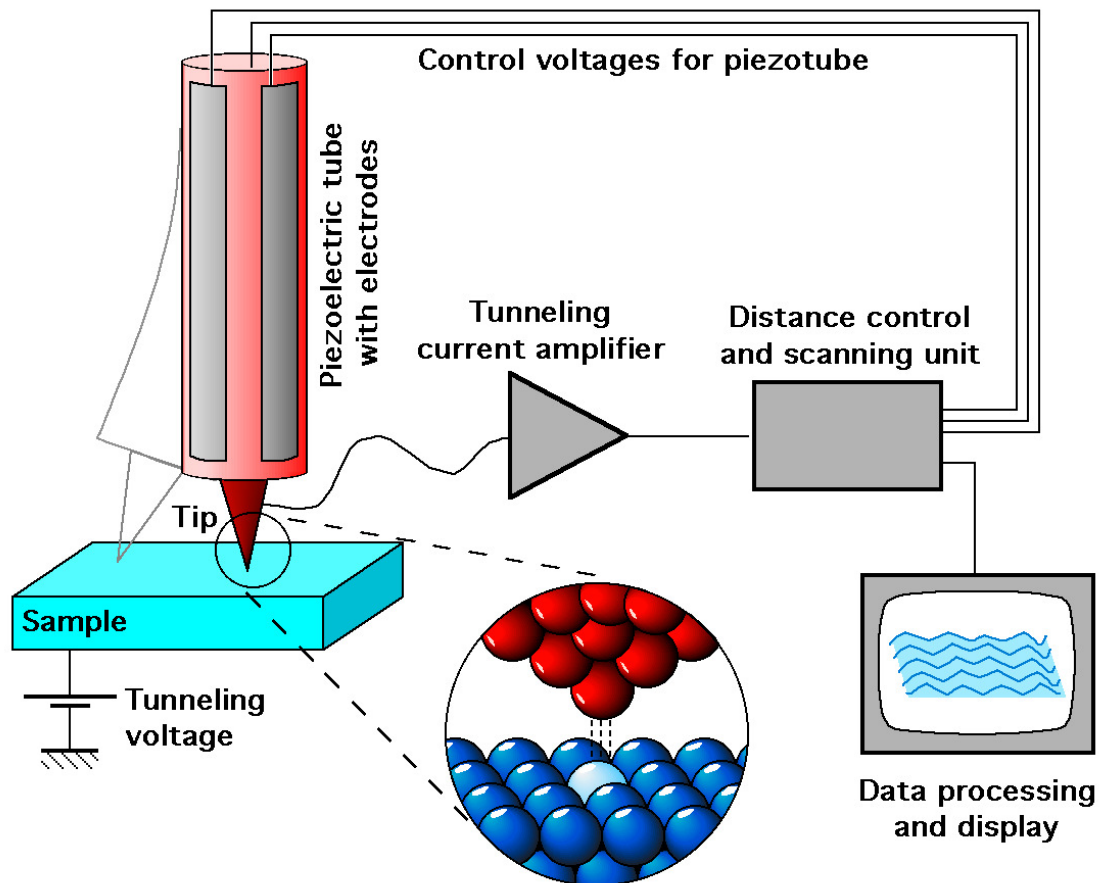


Fig. 3.8 Illustration of basic components and working principle of an STM system [6].

When a sample is scanned by STM, the voltage bias is applied and the tip is brought close to the sample (in nano- or sub-nanometer range), allowing electrons to tunnel through the vacuum between the sample under scanning and the tip. The resulting tunneling current is a function of tip position, applied voltage, and the local density of states (LDOS) of the sample. Once tunneling is established, the tip's bias and position with respect to the sample can be varied and data are obtained from the resulting changes in the tunneling current.

There are two operation modes for a standard STM system. One is constant height mode, i.e. the probe spacing is held constant as the probe is scanned, which means the voltage that controls the z-oriented piezoelectric element must be varied according to the sample contour, to provide the same probe current. Another one is constant current mode. In this operation mode, the probe is scanned across the sample and the spacing will now vary according to the sample contour to maintain a constant current reading, the height of the tip can be measured. This method is now used to determine the sample surface flatness.

3.3 Summary

In this chapter, MOSCAP/MOSFET process flow fabricated in NTU N2FC CR1 is briefly summarized. In addition, the standard experimental set-up and basic working principle of both electrical (Split $C-V$, $G-\omega$ and Gate dielectric relaxation current

measurement) and physical (XPS and STM) characterization methods that are frequently used in this research work are well introduced. The correlation between the electrical and physical characterized results provides clear and solid understanding of the devices' electrical performances.

References:

- [1]. E.H. Nicollian and A. Goetzberger, "The Si-SiO₂ Interface—Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique," *Bell Syst. Tech. J.* 46, 1055–1133, Jul, 1967.
- [2]. W. Luo, T. Yuan, Y. Kuo, J. Lu, J. Yan and W. Kuo, "Charge trapping and dielectric relaxation in connection with breakdown of high-*k* gate dielectric stacks", *Appl. Phys. Lett.* vol. 88, p. 202904, May, 2006.
- [3]. H. Reisinger, G. Steinlesberger, S. Jakschik, M. Gutsche, T. Hecht, M. Leonhard, U. Schroder, H. Seidl, and D. Schumann, "A comparative study of dielectric relaxation losses in alternative dielectrics," *IEDM Tech. Dig.*, pp. 12.2.1–12.2.4, 2001.
- [4]. Z. Xu, L. Pantisano, A. Kerber, R. Degraeve, E. Cartier, S. D. Gendt, M. Heyns, and G. Groeseneken, "A Study of Relaxation Current in High-*k* Dielectric Stacks", *IEEE Transaction on Electron Devices*, vol. 51, no. 3, pp 402-408, Mar. 2004.
- [5]. Wikipedia, the free encyclopedia, "X-ray photoelectron spectroscopy", available at: http://en.wikipedia.org/wiki/X-ray_photoelectron_spectroscopy.
- [6]. Wikipedia, the free encyclopedia, "Scanning tunneling microscope", available at: http://en.wikipedia.org/wiki/Scanning_tunneling_microscope.

CHAPTER 4 Electrical and Physical Properties of Er Doped HfO₂ High-*k* Dielectrics Prepared by Atomic Layer Deposition

4.1 Introduction

Metal gate/Hf-based high-*k* dielectrics gate stack with appropriate work function is considered as one of the critical technology solutions for sub 45nm CMOS technology [1]. One of the major problems for HfO₂ is Fermi-level pinning between HfO₂ and metal gate [2]. Recently, HfO₂ incorporated with lanthanide (e.g. La, Dy, Er etc) received considerable attention due to its capability to tune the metal work function towards Si conduction band edge [3-6], enabling the n-FETs application. In previous works, Er doped HfO₂ as high-*k* dielectrics has been reported, both of which are deposited by physical vapor deposition (PVD) [6, 7]. Further, HfErO (with 30% Er) prepared by PVD is found to tune the TaN metal gate work function of 4.1 eV [6]. In this work, Er doped HfO₂ high-*k* dielectrics (with Er ~ 4% and 7%) was prepared by Atomic Layer Deposition (ALD), which is more compatible to the industrial needs due to the excellent process controllability and is also more suitable for sub-1nm EOT scaling due to the superb scalability [8]. With 7% of Er incorporated into HfO₂, it is found that 1) the TiN metal gate work function can be modulated to a value of ~4.18 eV; 2) the thermal

stability of the HfO₂ film is improved, as evidenced by X-ray Photoelectron Spectroscopy (XPS) and X-Ray Diffraction (XRD) study; and 3) the k value and leakage properties of HfO₂ are maintained after Er doping.

4.2 Experimental

The high- k dielectric film was prepared on p-type (100) Si substrate in ASM Microchemistry Ltd, Finland. The Er doped HfO₂ was deposited using ALCVD(TM) reactor at a temperature of 315 °C. Before the film deposition, an IMEC clean [9] was used to create a chemical oxide interfacial layer with a thickness of ~ 1nm. The HfD-04 (Hf[C₅H₄(CH₃)₂(OCH₃)CH₃) /Er(thd)₃ / O₃ was used as the respective Hf / Er/ O precursors for the ALD deposition. The composition of Er doped HfO₂ was analyzed by RBS. Then the wafers were sent to NTU, Singapore for further fabrication. After receiving post deposition anneal in N₂ ambient at 800 °C for 60 s, TiN metal gate electrodes with ~50 nm thickness were then sputtered, followed by Cl₂ - based etchant patterning. Finally, all samples received a 425 °C forming gas anneal for 30 minutes. Electrical characteristics of the fabricated MOS capacitors were measured using Agilent Technologies E4156/5280 precision semiconductor parameter analyzer. The equivalent oxide thickness (EOT) and flatband voltage (V_{fb}) were extracted considering quantum mechanical effects [10].

4.3 Results and Discussion

As shown in **Fig. 4.1**, the measured CV from the HfErO capacitors (with a physical thickness of ~ 4 nm) can match well with the NCSU fitted curve [17], suggesting the good quality of the devices. Inset of **Fig. 4.1** demonstrate a strong V_{fb} tunability for the MOS devices due to the Er incorporation.

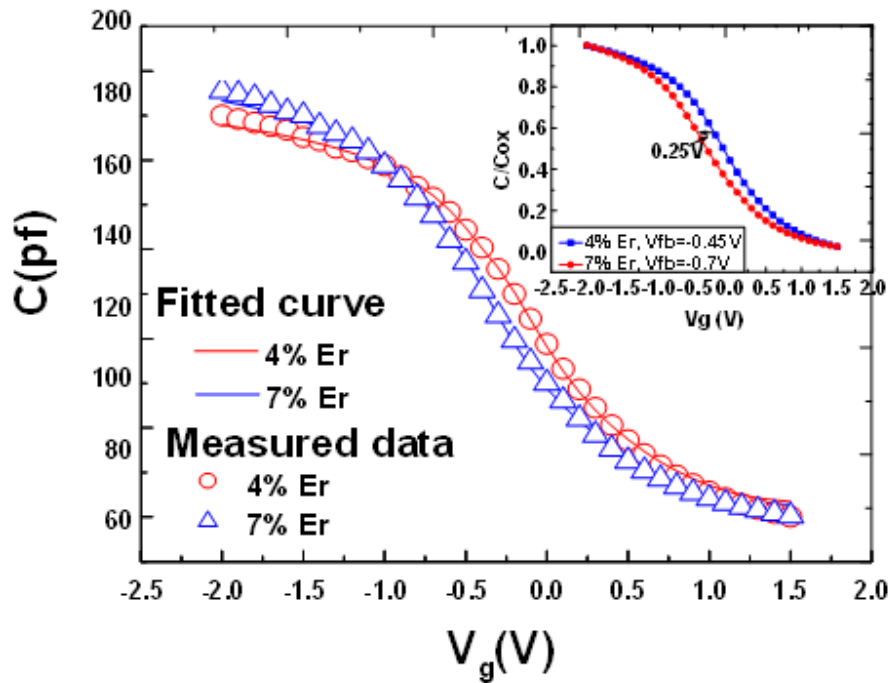


Fig. 4.1 The measured and simulated C - V curves for HfErO devices. Inset graph shows normalized C - V curves for HfErO with different Er concentration. The V_{fb} of HfO₂ control is about -0.1 V. Capacitor area = 16×10^{-5} cm².

V_{fb} was extracted from the $C-V$ curves and plotted as a function of EOT, as shown in **Fig. 4.2**. It is noted that adding Er into HfO_2 (with Er of $\sim 7\%$) can significantly reduce the TiN effective work function (EWF) to a value of ~ 4.18 eV, rendering HfErO a possible candidate for future nMOS gate dielectric. The possible mechanism for the work function modulation can be explained by the interfacial dipole contribution between TiN/HfErO [5], due to that Er has electronegativity of 1.24 on the Pauling scale, which is lower than those of both Hf (1.3) and Ti (1.54) [11]. Thus when Er is added into HfO_2 to replace the Hf atoms, electrons will be transferred from dielectric to metal gate, effectively reducing the TiN EWF.

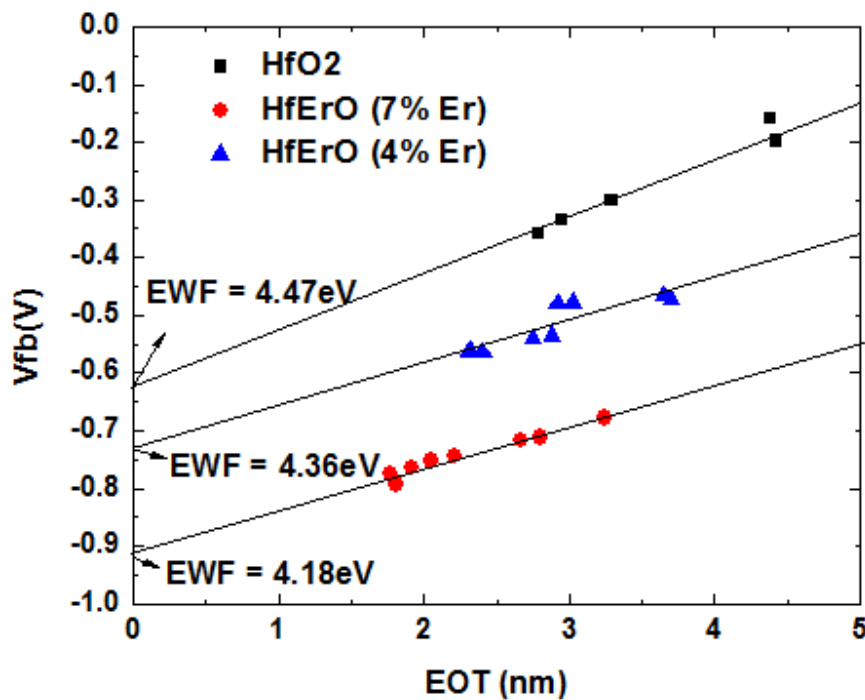


Fig. 4.2 V_{fb} versus EOT of fabricated MOS capacitors with HfO_2 or HfErO gate dielectrics.

Fig. 4.3 shows the gate leakage current densities of HfErO devices at different EOT. The leakage current densities are about four orders less than the reference Poly-Si/SiO₂ devices, similar to the HfO₂ control samples. It is noted that the conduction/valence band offset of ErO on Si is reported to be 3.1/3.5 eV respectively [12], which contributes to the good leakage property of HfErO. Despite the lower dielectric constant (*k*) of Er₂O₃ (~14) [13] as compared to that of HfO₂ (~22), as shown in Fig. 4.4, the extracted *k* value of HfErO in this work is equivalent with HfO₂, likely due to low Er concentrations in the dielectrics.

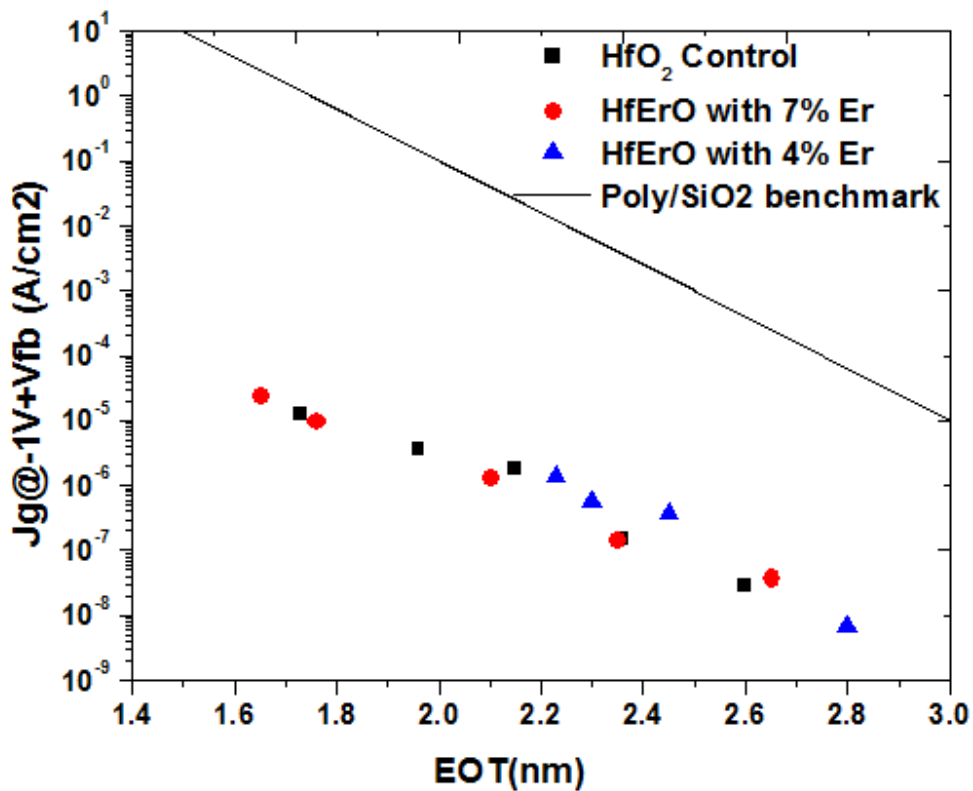


Fig. 4.3 Gate leakage current density versus EOT relationship for HfO₂ and HfErO with different Er concentration.

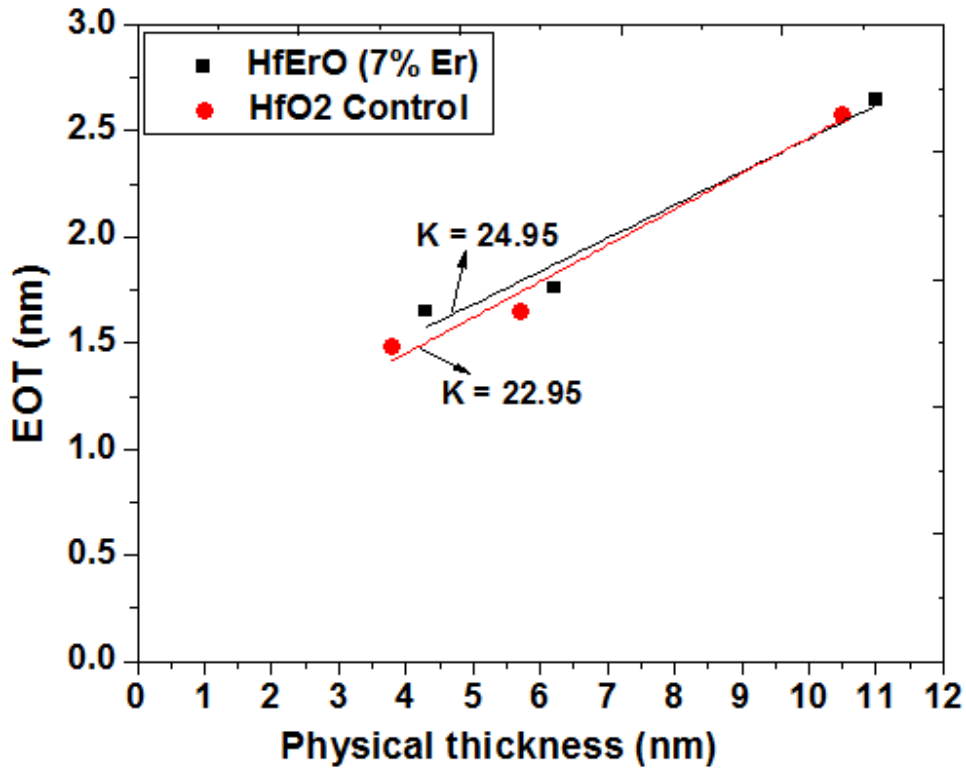


Fig.4.4 Extracted dielectric constant k for HfO₂ and HfErO with Er of 7%.

RTA were performed on samples with ALD blank deposited HfO₂ and HfErO dielectrics in N₂ ambient at temperature of 800 °C and 1000 °C for 30 s, and then characterized by both XPS and XRD. The films under examination are of similar physical thickness, ~11 nm. It should be noted all the XPS signals measured in this work are aligned with C 1s reference peak. As shown in **Fig. 4.5**, it is seen that Hf 4f_{7/2} XPS peak binding energy shifts to higher energy state, implying that Hf is more oxidized after the high temperature annealing [14]. It is reported that the oxygen concentration in HfO₂ tends to reduce after high-temperature annealing [15]. It is thus believed that Er can help at least retain O atoms in HfO₂ dielectric film after high temperature anneal, likely due to the lower electronegativity of Er, which is more prone to the oxygen bond. This is

important to suppress the oxygen vacancy (V_o) density inside the dielectric, which is a serious concern to the dielectrics reliability [16].

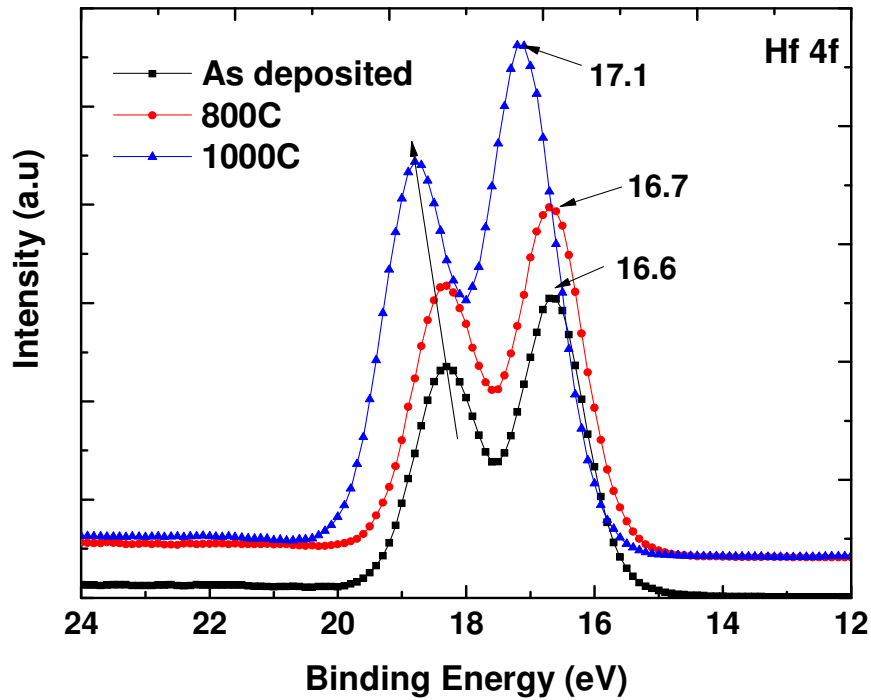


Fig. 4.5 XPS shows that Hf 4f peak shifts to higher binding energy state after high-temperature annealing.

Fig. 4.6 shows the XRD study on HfO_2 and HfErO samples annealed at 800 °C and 1000 °C, respectively. Due to adding of Er (with a concentration of 7%), the HfErO film crystallization temperature is increased to 800 °C, which may due to the suppression of the continuous crystal growth of the original film by Er incorporation into HfO_2 .

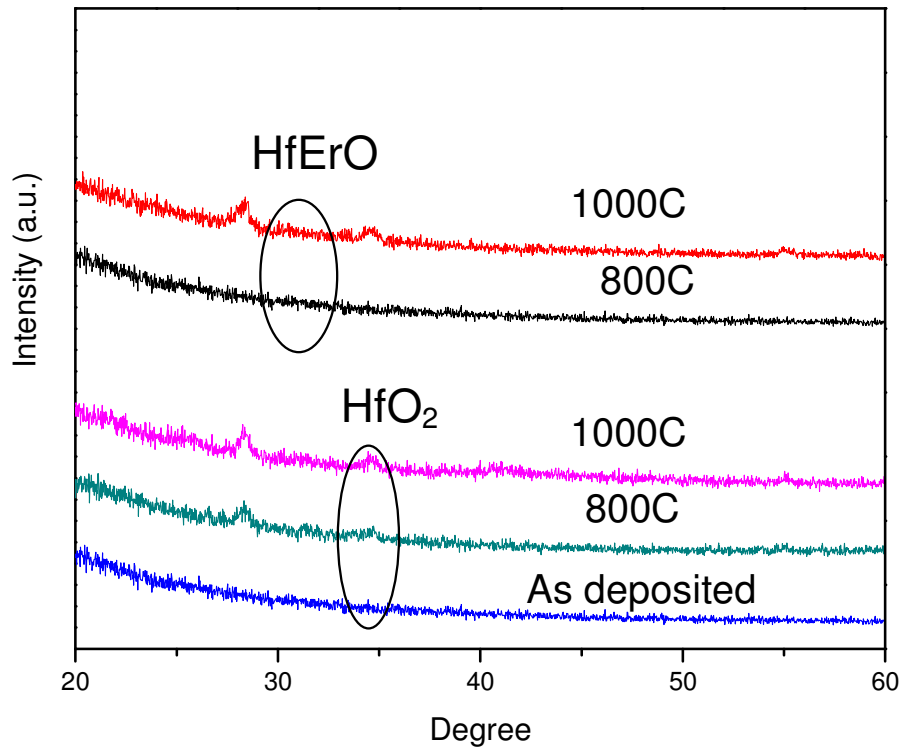


Fig. 4.6 XRD for HfO₂ and HfErO (7% Er) annealed at 800 °C and 1000 °C.

4.4 Summary

The TiN metal gate MOS capacitors with ALD deposited HfErO high-*k* gate dielectrics have been investigated both electrically and physically. By incorporating Er into HfO₂, the work function of TiN is tuned towards to Si conduction band edge, and the thermal stability of the high-*k* film is improved, without degrading the dielectric constant and leakage properties of HfO₂. This study suggests that ALD HfErO is a viable candidate for future n-FETs gate dielectric.

References

- [1]. International Technology Roadmap for Semiconductors (ITRS), San Jose, CA: Semiconductor Industry Assoc., 2007.
- [2]. S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, “Fermi level pinning with sub-monolayer MeOx and metal gates,” in *IEDM. Tech. Dig.*, 2003, pp. 307–310.
- [3]. H.N. Alshareef, H.R. Harris, H.C. Wen, C.S. Park, C. Huffman, K. Choi, H.F. Luan, P. Majhi, B.H. Lee, R. Jammy, D.J. Lichtenwalner, J.S. Jur, and A. I. Kingon, “Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric”, in *VLSI Symp. Tech. Dig.*, 2006, pp. 7-8.
- [4]. H.Y. Yu, S.Z. Chang, A. Veloso, A. Lauwers, C. Adelman, B. Onsia, S. Van Elshocht, R. Singanamalla, M. Demand, R. Vos, T. Kauerauf, S. Brus, X. Shi, S. Kubicek, C. Vrancken, R. Mitsuhashi, P. Lehnen, J. Kittl, M. Niwa, K.M. Yin, T. Hoffmann, S. Degendt, M. Jurczak, P. Absil, and S. Biesemans, “Low Vt Ni-FUSI CMOS Technology using a DyO cap layer with either single or dual Ni-phases”, in *VLSI Symp. Tech. Dig.*, 2007, pp. 18-19.
- [5]. X. P. Wang, H. Y. Yu, M.-F. Li, C. X. Zhu, S. Biesemans, A. Chin, Y. Y. Sun, Y. P. Feng, A. Lim, Y.-C. Yeo, W. Y. Loh, Q. Q. Lo, and D.-L. Kwong, “Wide Vfb and Vth tunability for metal-gated MOS devices with HfLaO gate dielectrics”, *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 258–260, Apr. 2007.

- [6]. J. D. Chen, X. P. Wang, M.-F. Li, S. J. Lee, M. B. Yu, C. Shen, and Y.-C. Yeo, “NMOS compatible work function of TaN metal gate with erbium-oxide-doped hafnium oxide gate dielectric”, *IEEE Electron Device Lett.*, vol. 28, no. 10, pp.862-864, Oct 2007.
- [7]. S. Govindarajan, T. S. Boscke, P. Sivasubramani, P. D. Kirsch, B. H. Lee, H. –H. Tseng, R. Jammy, U. Schroder, S. Ramanathan, and B. E. Gnade, “Higher permittivity rare earth doped HfO₂ for sub-45-nm metal-insulator-semiconductor devices”, *Appl. Phys. Lett.*, vol. 91, 062906, 2007.
- [8]. A. Delabie, M. Caymax, B. Brijs, D. P. Brunco, T. Conard, E. Smeets, S. V. Elshocht, L. Ragnarsson, S. D. Gendt, and M. M. Heyns, “Scaling to sub-1nm equivalent oxide thickness with hafnium oxide deposited by atomic layer deposition”, *J. Electrochem. Soc.*, 153 (8) F180-F187, 2006.
- [9]. M. Meuris, S. Amants, I. Comelissen, K. Kenis, M. Lux, S. Degen, P. Mertens, I. Teerlinck, R. Vos, L. Loewenstein, and M. M. Heyns, “Implementation of the IMEC-Clean in advanced CMOS manufacturing”, in *IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings.*, pp. 157-160, 1999.
- [10]. J. R. Hauser and K. Ahmed, “Characterization of ultra-thin oxides using electrical C-V and I-V measurements,” in *Characterization and Metrology for ULSI Technology*, Seiler *et al.*, Eds. Woodbury, NY: AIP, 1998, pp. 235–239.
- [11]. [Online]. Available: http://en.wikipedia.org/wiki/Pauling_scale.
- [12]. Y. Y. Zhu, S. Chen, R. Xu, Z. B. Fang, J. F. Zhao, Y. L. Fan, X. J. Yang, and Z. M. Jiang, “Band offsets of Er₂O₃ films epitaxially grown on Si substrates,” *Appl. Phys. Lett.*, vol. 88, 162909, 2006.

- [13]. H. R. Huff and D. C. Gilmer, *High Dielectric Constant Materials*. New York: Springer-Verlag, 2005, p. 246.
- [14]. J. Kim, and K. Yong, "Interfacial properties of Hf-silicate/Si and Hf-silicate/Al₂O₃/Si deposited by atomic layer chemical vapor deposition", *J. Electrochem. Soc.*, 152 (10) F153-F155, 2005.
- [15]. M. M. Hussain, M. A. Quevedo-Lopez, H. N. Alshareef, H.C. Wen, D. Larison, B. Gnade and M. El-Bouanani, "Thermal annealing effects on a representative high-*k*/metal film stack", *Semicond. Sci. Technol.* 21 pp. 1437–1440, Sep. 2006.
- [16]. E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, "Role of oxygen vacancies in VFB/V_t stability of pFET metals on HfO₂," in *VLSI Symp. Tech. Dig.*, 2005, pp. 230–231.
- [17]. J. R. Hauser and K. Ahmed, "Characterization of ultra-thin oxides using electrical C-V and I-V measurements," in *Characterization and Metrology for ULSI Technology*, Seiler et al., Eds. Woodbury, NY: AIP, 1998, pp. 235–239.

CHAPTER 5 Thermal Stability of TiN Metal Gate Prepared by Atomic Layer Deposition or Physical Vapor Deposition on HfO₂ High-*k* Dielectric

5.1 Introduction

In the advanced CMOS technology, metal gate along with high-*k* gate dielectric, is required to replace the conventional poly-Si/SiO₂ gate stack, in order to eliminate the poly depletion and achieve good equivalent oxide thickness (EOT) scalability without sacrificing the gate leakage. Among various metal and metal compounds, refractory metal nitrides have been intensively studied, such as: TiN, TaN, HfN, MoN [1-4], etc. It is especially worthy noting that the TiN, as the metal gate electrode for 45nm and beyond CMOS devices which are in mass production now [5], has received tremendous interests recently. On the other hand, a systematic study on the TiN thermal stability is lacking in literature, which is critical for the device integration. In this work, TiN metal gate with various composition (Ti-rich or N-rich) are prepared by either atomic layer deposition (ALD) or physical vapor deposition (PVD) on HfO₂ high-*k* dielectric. The electrical properties of TiN/HfO₂/Si after various thermal annealing are characterized by Capacitance-Voltage (*CV*) and Current-Voltage (*IV*) measurement and the physical properties are investigated and compared by X-ray Photoelectron Spectroscopy (XPS),

High Resolution Transmission Electron Microscopy (HRTEM), and Electron Energy Loss Spectroscopy (EELS).

After annealing of the TiN/HfO₂ stack at 1000 °C for 30 s, which is normally required by source/drain activation, it is observed that: 1) Nitrogen tends to out-diffuse from TiN for all the samples; 2) Oxygen from the interfacial layer (IL) between HfO₂ and Si substrate tends to diffuse towards TiN. It is interesting to note that PVD Ti-rich TiN shows a wider oxygen distribution in the gate stack and also a thinner IL than the N-rich sample after annealing. Ti penetration into HfO₂ is observed in the Ti-rich sample. It is found as well that ALD TiN help suppress oxygen out-diffusion as compared to the PVD TiN samples, which is potentially greatly beneficial for the high-*k* dielectrics integrity. The work function of TiN metal gate is thus correlated with its thermal stability.

5.2 Experimental

Three TiN/HfO₂ samples fabricated on p-type Si (100) substrate were investigated. After standard Radio Corporation of America (RCA) clean, ~25 Å HfO₂ were deposited by ALD, followed by ~200 Å TiN film deposition either by ALD or PVD, and PVD TiN composition was controlled by varying deposition parameters. Rapid thermal annealing in N₂ at 400 °C or 1000 °C for 30 s, respectively, was performed on all the TiN/HfO₂ samples. The physical properties of the fabricated TiN/HfO₂/Si stack were then studied by XPS depth profile, HRTEM and EELS. Ti/N ratio of as-deposited ALD, N-rich PVD, and Ti-rich PVD TiN samples are 0.937, 0.935, and 1.11 respectively, measured by XPS.

All the XPS binding energy (BE) peak energy was calibrated versus C 1s peak. MOS capacitors were defined by lithography and electrical measurements were performed using Agilent Technologies E4156/5280 precision semiconductor parameter analyzer.

5.3 Results and Discussion

Table 5.1 summarizes the Ti/N ratio in the various bulk TiN samples after 400 °C and 1000 °C annealing as measured by XPS. It is seen that Ti/N ratio increases after high temperature anneal for all three samples. Further no N signal can be detected in the HfO₂ layer in all the samples after high temperature annealing based on XPS, indicating the N out-diffusion from TiN bulky layer. On the other hand, the work function of TiN prepared by ALD (PVD) is reported to reduce from ~5.1 (5.0) eV to ~4.8 (4.7) eV when annealing temperature increased from 400 °C to 1000 °C [6, 7]. TiN work function is known to be closely related to N concentration, and the higher N concentration, the higher TiN work function [8]. It is thus believed that N out-diffusion is one of, if not the only one reason that cause TiN work function decrease to mid-gap when annealed at high temperature.

From **Table 5.1**, both ALD and N-rich PVD TiN films have similar as-deposited Ti/N ratio, ~0.94, hence these two samples are used for different deposition technique comparison, while PVD Ti-rich and N-rich samples are used for TiN composition comparison.

Table 5.1 The atomic composition of TiN film after 400 °C and 1000 °C annealing as measured by XPS.

Ti:N	400 °C	1000 °C
ALD TiN	0.937	1.03
PVD TiN (Ti-rich)	1.11	1.16
PVD TiN (N-rich)	0.935	1.03

5.3.1 Ti-rich vs. N-rich

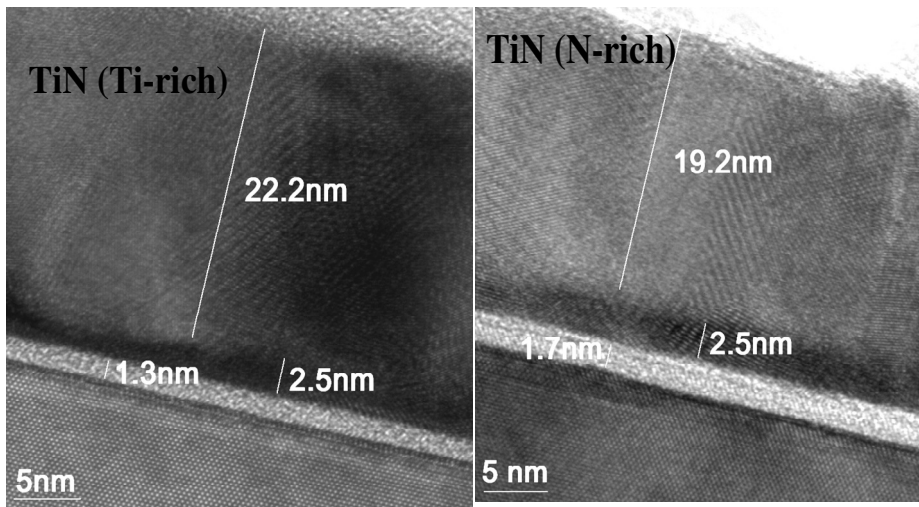


Fig. 5.1 HRTEM picture shows that the interfacial layer thickness of Ti-rich sample (1.3 nm) is thinner than N-rich sample (1.7 nm).

Fig. 5.1 compares high resolution XTEM of two PVD TiN samples after 1000°C annealing. It is seen IL thickness of Ti-rich sample (1.3 nm) is 0.4nm thinner than N-rich sample (1.7nm), which can be attributed to the fact that excess Ti in TiN can scavenge oxygen from the underlying dielectrics, more specifically from IL [9].

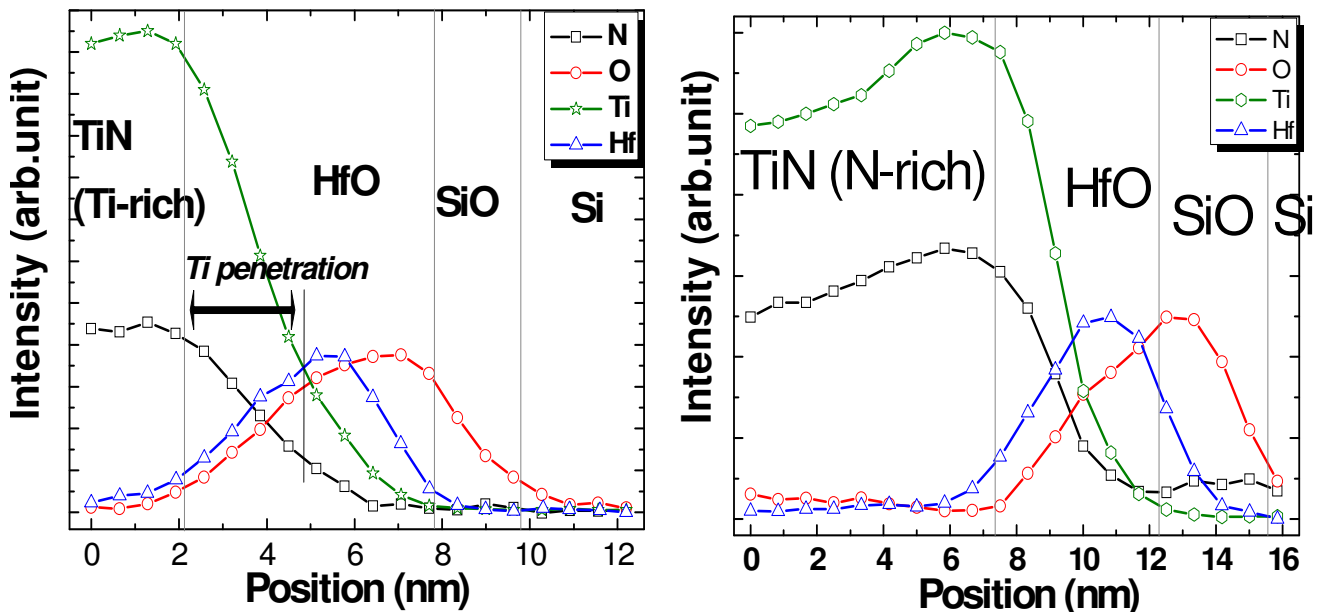


Fig. 5.2 EELS spectra show that Ti-rich (left) sample has wider O distribution than N-rich sample (right). A signal of Ti penetration into HfO gate dielectric is observed for Ti-rich sample than N-rich one.

Fig. 5.2 shows EELS of these two TiN samples after 1000°C annealing. It's noted that Ti-rich sample shows much wider oxygen distribution than N-rich one in the gate stack, which reinforces the fact that oxygen out-diffuse from IL more in the Ti-rich TiN (consistent with XTEM). Further when comparing Ti- and Hf- EELS profiles in Ti-rich sample with N-rich one, more intermixing between Ti & Hf is noted. This can be

explained by the Ti penetration into HfO_2 dielectric upon annealing due to the excess Ti in the Ti-rich sample. Ti penetration into HfO_2 poses a concern on Ti-rich TiN thermal stability, i.e. the initial dielectric breakdown, as shown in **Fig. 5.3**.

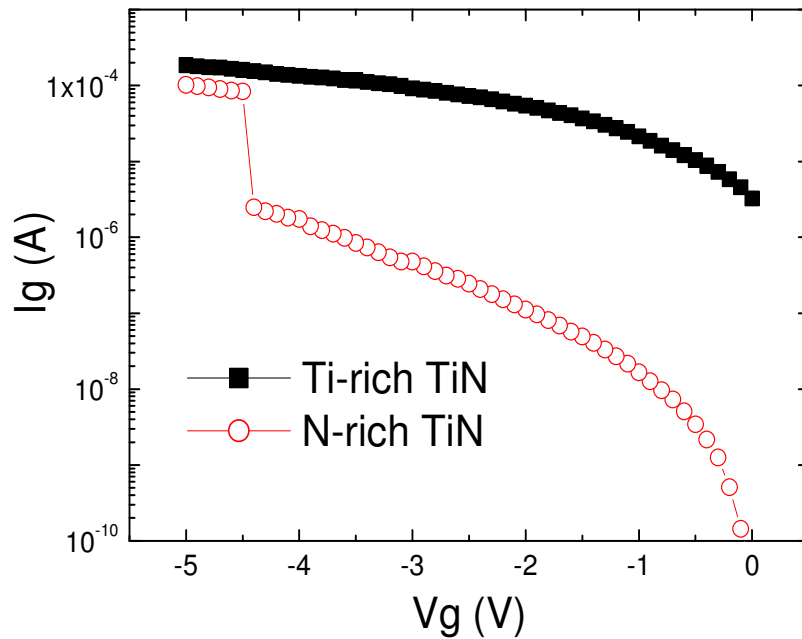


Fig. 5.3 Gate leakage current comparison of Ti-rich and N-rich PVD TiN gated samples after 1000 °C annealing. Ti-rich sample shows initial hard breakdown behavior, while the N-rich sample I - V characteristic is “normal”.

5.3.2 ALD vs. PVD

Both ALD and N-rich PVD TiN films have a similar as-deposited Ti/N ratio, ~ 0.94 . **Fig. 5.4** compares XPS Hf 4f spectra after 400 °C and 1000 °C annealing of the ALD and N-rich TiN samples. All the XPS peak binding energy (BE) reported in this work was

calibrated versus C 1s peak. Hf-silicide signal (Hf 4f BE ~ 14 eV) is observed in both samples, which might come from the IL [10]. After 1000 °C annealing, part of IL Hf-silicide is oxidized to HfO₂, as evidenced by the fact that Hf peak moves to higher BE. It is further seen that Hf-silicide reduction is more significant for the PVD TiN samples than the ALD TiN, which indicates that oxygen out-diffusion from the IL to TiN through Hf oxide is suppressed in ALD TiN sample.

This is also concluded from the comparison on oxygen concentration increase after high temperature annealing in the bulk TiN measured by XPS (**Table 5.2**). Comparing with the PVD TiN samples, the ratio of oxygen increase after 1000 °C annealing in ALD TiN bulk is significantly lower, which can be explained by the areal oxygen density difference [11]. ALD TiN has higher as-deposited oxygen concentration than PVD TiN owing to the oxygen-containing precursors used in ALD, hence the driving force of the oxygen out-diffusion from IL to TiN film - oxygen concentration gradient, is much smaller for ALD sample.

Table 5.2 The amount of oxygen increased in the PVD and ALD TiN bulk. O signal were collected after Ar⁺ sputtering of the samples for 2mins, when TiN bulk is exposed for scan.

	O% increased after 1000 °C anneal
ALD TiN	31%
PVD TiN (N-rich)	93%

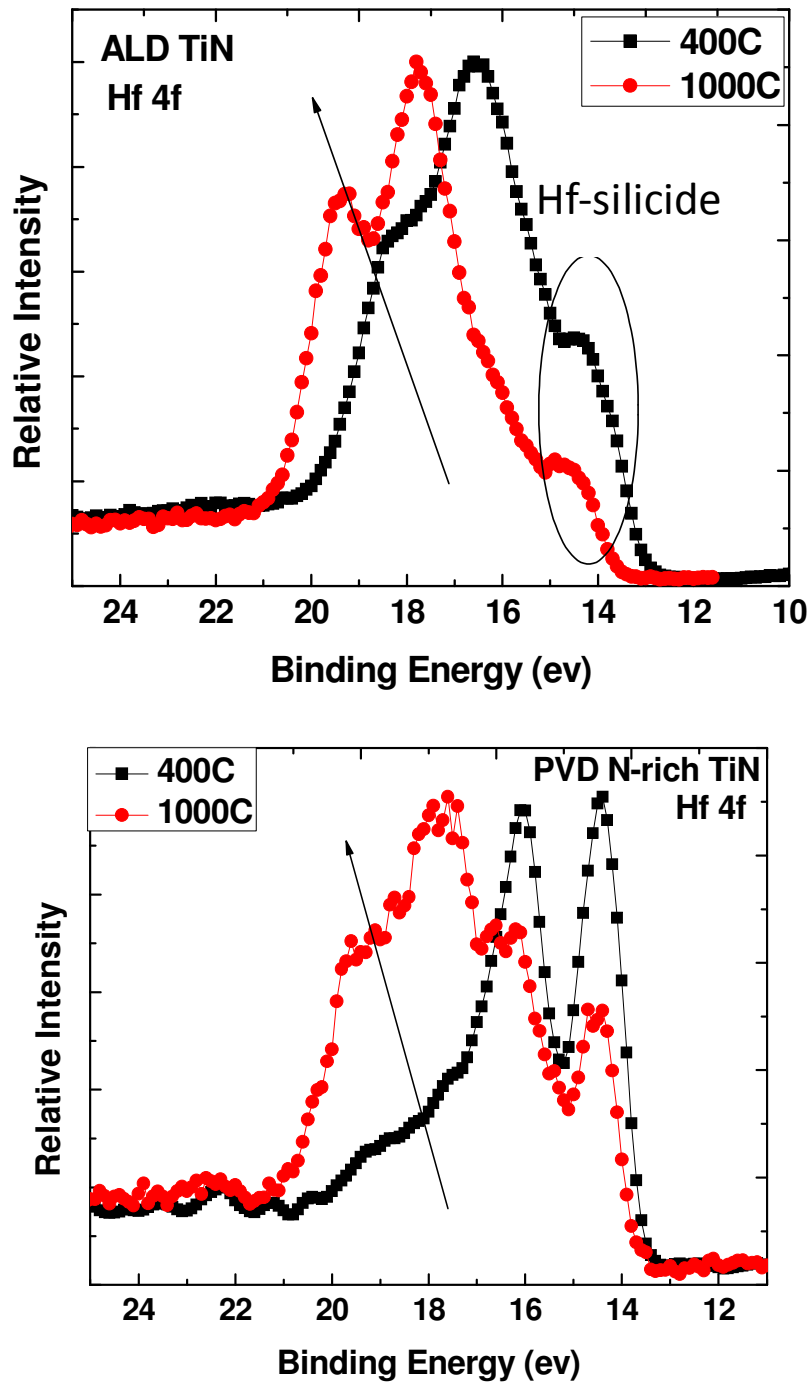


Fig. 5.4 XPS Hf 4f spectra after 400 °C and 1000 °C anneal of ALD TiN (top) and PVD N-rich TiN (bottom). Hf signal were collected after Ar⁺ sputtering of the samples for 5mins, when top TiN film are all sputtered off.

In Fig. 5.5, after 1000 °C annealing, Ti 2p peak BE of PVD TiN film is higher than ALD TiN, indicating more Ti-O bonds formed in the former sample [12], consistent with the oxygen concentration increase in the TiN film (Table 5.2) and the more Hf-silicide reduction for PVD TiN (Fig. 5.4).

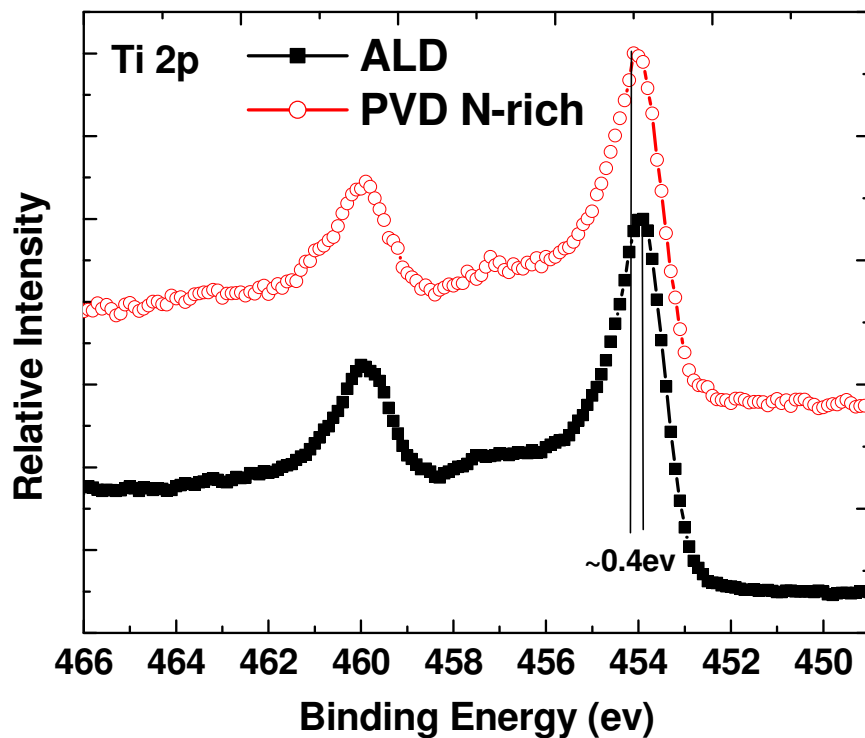


Fig. 5.5 XPS Ti 2p spectra of TiN bulk after 1000 °C annealing for ALD and N-rich PVD TiN samples. PVD sample shows larger BE, indicating more Ti-O bond formation than ALD. Ti signal were collected after Ar⁺ sputtering of the samples for 2 mins, when TiN bulk is exposed for scan.

The flat band voltages (V_{fb}) for these two samples were extracted from CV measurement, shown in **Fig. 5.6**. ALD samples show much smaller negative V_{fb} , indicating the higher WF of ALD TiN, consistent with literature [13]. This is correlated with that ALD TiN enables less oxygen out-diffusion from HfO_2/IL stack (evidenced by XPS in **Figs. 5.4& 5.5**), and hence less oxygen vacancy (V_o^+) in the dielectrics stack. Accordingly, the TiN Fermi level movement due to V_o^+ – related dipole will be less for ALD TiN than PVD TiN sample, leading to higher EWF of ALD TiN than PVD ones, as schematically shown in **Fig. 5.7**. Less V_o is also critical for HfO_2 dielectrics integrity.

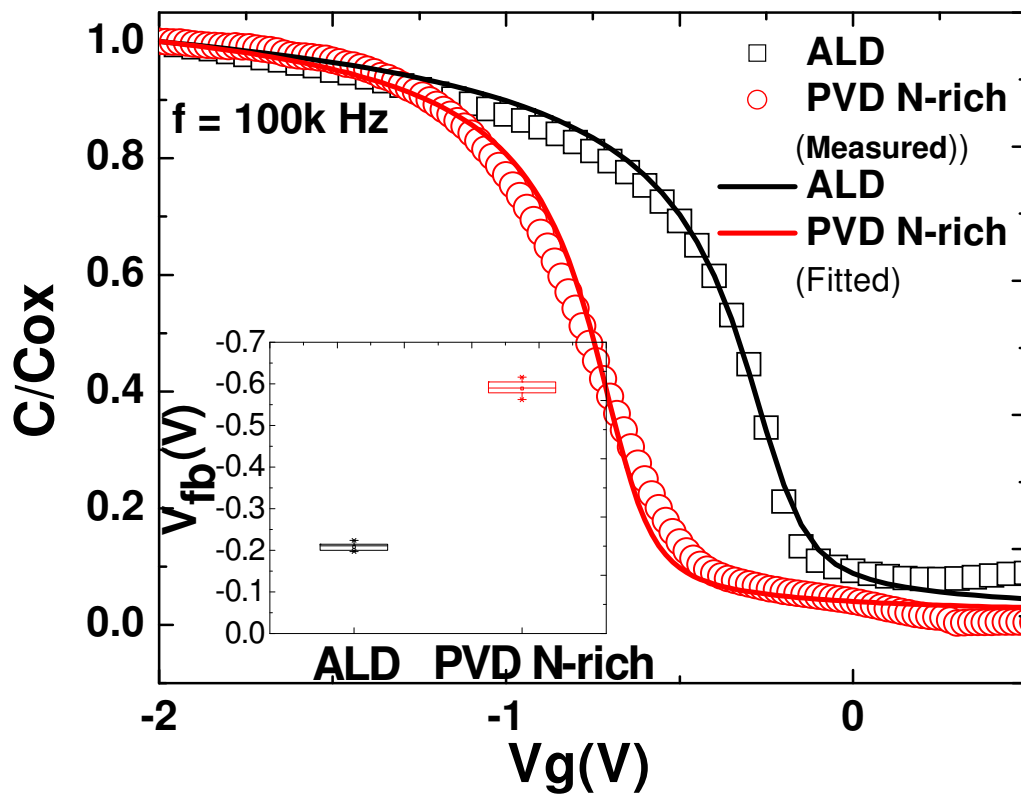


Fig. 5.6 Measured and fitted $C-V$ for ALD and PVD N-rich sample. PVD sample shows more negative V_{fb} than ALD one.

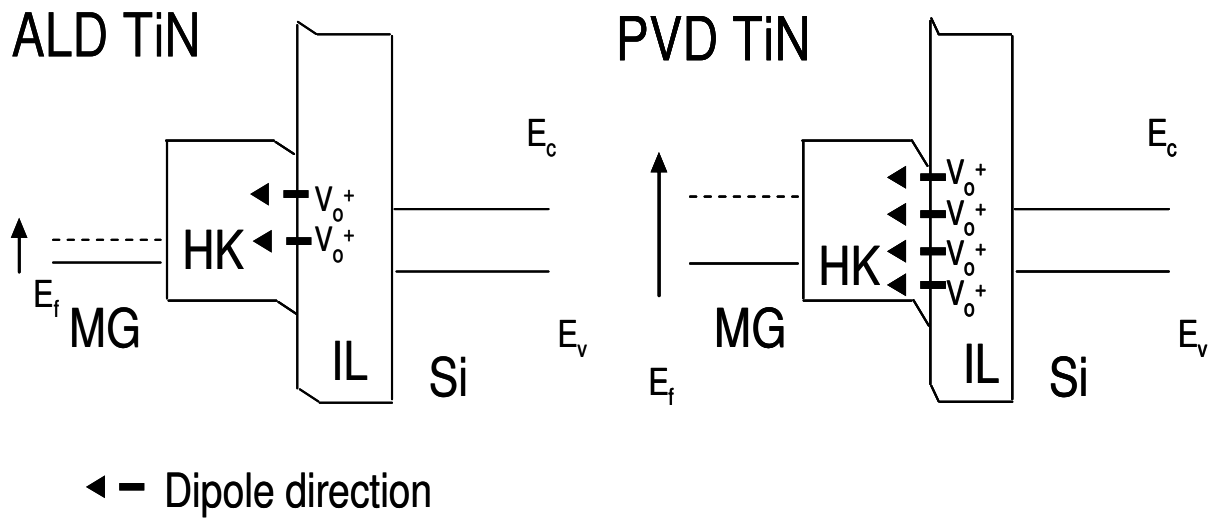


Fig. 5.7 The schematics of EWF change after high T annealing of ALD TiN (left) and PVD TiN (right).

5.4 Summary

The thermal stability of ALD and PVD TiN (both Ti-rich and N-rich) on HfO_2 stack has been systematically investigated. After 1000 °C annealing, Nitrogen tends to out-diffuse from TiN and Oxygen also diffuse from IL between HfO_2 and Si towards TiN. PVD Ti-rich sample shows wider oxygen distribution at dielectric layer and thinner interfacial layer thickness than PVD N-rich sample, owing to that Ti can help scavenge oxygen out from the underlying dielectrics. Finally, the oxygen out-diffusion into TiN film is significantly suppressed for ALD TiN compare with PVD TiN samples, which is correlated with the fact that ALD TiN has higher EWF than PVD TiN.

References

- [1]. J. Westlinder, T. Schram, L. Pantisano, E. Cartier, A. Kerber, G. S. Lujan, J. Olsson, and G. Groeseneken, "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices", *IEEE Electron Device Lett.* Vol. 24, no. 9, pp. 550-552, Sep. 2003.
- [2]. Y. Sugimoto, M. Kajiwara, K. Yamamoto, Y. Suehiro, D. Wang, and H. Nakashima, "Effective Work Function Modulation of TaN Metal Gate On HfO₂ after Postmetallization Annealing", *Appl. Phys. Lett.* 91, 112105, 2007.
- [3]. H. Y. Yu, H. F. Lim, J. H. Chen, M. F. Li, Chunxiang Zhu, C. H. Tung, A. Y. Du, W. D. Wang, D. Z. Chi, and D.-L. Kwong, "Physical and Electrical Characteristics of HfN Gate Electrode for Advanced MOS Devices", *IEEE Electron Device Lett.* Vol. 24, no. 4, pp.230-232, Apr. 2003.
- [4]. B. -Y. Tsui, C. -F. Huang, and C. -H. Lu, "Investigation of Molybdenum Nitride Gate on SiO₂ and HfO₂ for MOSFET Application", *J. Electrochem. Soc.* 153, G197-G202, 2006.
- [5]. L. Peters, Semiconductor International. http://www.semiconductor.net/article/200229-Physical_Analysis_Provides_Images_of_45_nm.php#id3260957-25-a.
- [6]. H. Y. Yu, Chi Ren, Yee-Chia Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, Ming-Fu Li, D. S. H. Chan, and D. -L. Kwong, "Fermi Pinning-Induced Thermal Instability of Metal-Gate Work Functions", *IEEE Electron Device Lett.* Vol. 25, no. 5, pp.337-339, May 2004.

- [7]. G. Sjoblom, J. Westlinder, and J. Olsson, "Investigation of the Thermal Stability of Reactively Sputter-Deposited TiN MOS Gate Electrodes", IEEE T. Electron Dev. Vol.52, no.10, pp.2349-2352, Oct. 2005.
- [8]. J. Westlinder, G. Sjoblom, and J. Oleeson, "Variable Work Function in MOS Capacitors Utilizing Nitrogen-Controlled TiN_x Gate Electrodes", Microelectron. Eng. 75, pp.389-396, 2004.
- [9]. H. Kim, P.C. McIntyre, C. O. Chui, K. C. Saraswat and S. Stemmer, "Engineering Chemically Abrupt High-*k* Metal Oxide/Silicon Interfaces using an Oxygen-Gettering Metal Overlayer", J. Appl. Phys. 96, 3467 2004.
- [10]. J. Kim, and K. Yong, "Interfacial Properties of Hf-silicate/Si and Hf-silicate/Al₂O₃/Si Deposited by Atomic Layer Chemical Vapor Deposition", J. Electrochem. Soc., 152, F153-F155, 2005.
- [11]. K. Kita, and A. Toriumi, "Origin of electric dipoles formed at high-*k*/SiO₂ interface", Appl. Phys. Lett. 94, 132902, 2009.
- [12]. Handbook of the elements and native oxides, 1999 XPS international, Inc.
- [13]. G.S. Lujan, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpela, H. Sprey, S. De Gendt, and K. De Meyer, "Impact of ALCVD and PVD Titanium Nitride Deposition on Metal Gate Capacitors", Proceedings of the 32nd Solid-State Device Research Conference, pp.583-586, 2002.

CHAPTER 6 A Novel Multi Deposition Multi Room-Temperature Annealing Technique via Ultraviolet-Ozone to Improve High- k /Metal (HfZrO/TiN) Gate Stack Integrity for a Gate-Last Process

6.1 Introduction

Gate last process has been introduced into mass production since 45nm technology node to implement high- k and metal gate stack [1], as it overcomes many technology hurdles faced by conventional gate first integration scheme, e.g. EOT and V_{th} thermal instability and V_o related reliability. In a gate last process, due to the low thermal budget restrict (normally <600 °C concerning NiSi source/drain), appropriate post-deposition treatment of the gate stack is thus critical to cure the possible defects in the deposited high- k and enhance the gate dielectrics integrity. MDMA using RTA as annealing means was reported to improve device performance in a gate-first process [2], however, undesirable EOT growth is a concern. In this work, for the first time, a novel MDMA at room temperature in UVO is demonstrated to treat the ALD HfZrO (a promising high- k for sub-45 nm CMOS), which greatly enhances the gate dielectrics integrity without EOT penalty as compared to the conventionally used RTA annealed sample, highly suitable for

the gate last integration scheme. The mechanism responsible for the high- k performance improvement is proposed based on scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS) studies.

6.2 Experimental

The device fabrication process flow is shown in Fig. **6.1(a)**. After ~ 5500 Å field oxide thermally grown on the p-type (100) Si substrate and active area definition, ~ 1 nm interfacial layer (IL) was intentionally prepared to improve the interface between HK and substrate. ~ 2 nm HfZrO is deposited by ALD using MDMA technique (deposition at 300 °C and annealing at room temperature ex-situ in a UVO chamber). The UV light was generated by low pressure Mercury vapor grid, and interacts with oxygen to produce ozone (**Fig. 6.1(b)**).

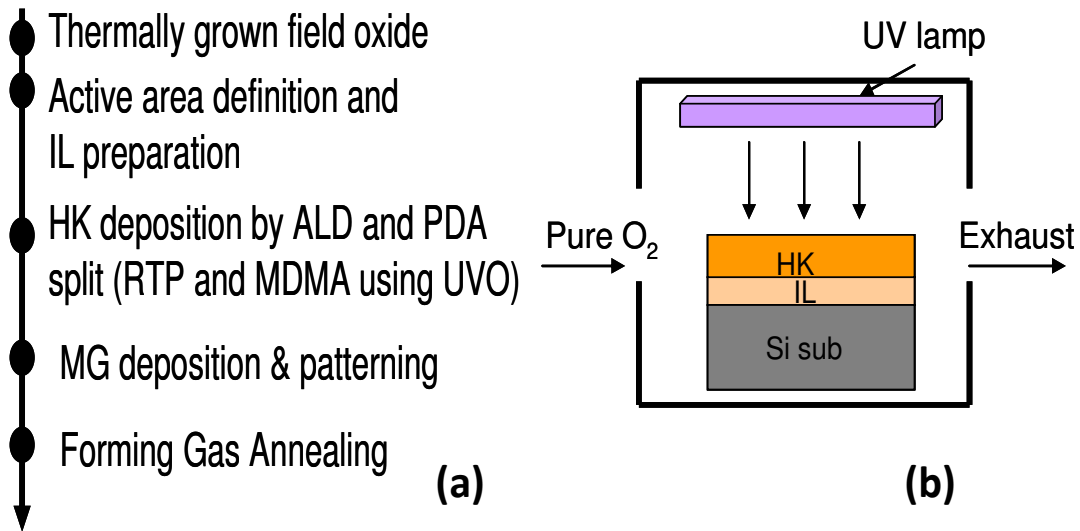


Fig. 6.1(a) Device fabrication process flow; **(b)** Schematic shows the UVO annealing process.

Two different samples were prepared: 2min × 2 (1min × 4) refers to 2 (4) D & A cycles. Reference ALD HfZrO was annealed by RTA at 600 °C for 30 s in N₂ (**Table 6.1**). The total ALD deposition cycles are kept as constant among all samples. 50nm TiN electrode were deposited by PVD and patterned. Finally, all samples received forming gas annealing at 425 °C for 30 mins without other thermal budget to mimic the gate last process. From the XTEM micrographs (**Fig. 6.2**), all samples are with ~1.3 nm IL and ~2 nm HK, regardless of annealing condition. Further from TEM, clear crystallization is seen in the RTA control sample, while less visible in the MDMA samples.

Table 6.1 The details of High k deposition and annealing conditions for all samples.

Sample	D & A Cycles	HK thickness/cycle	Annealing after each cycle	Total HK Thickness	Total Annealing Time
RTP (control)	1	2nm	RTP 600 °C 30s N ₂	2nm	30s (RTP)
UVO 2minX2	2	1nm	UVO 2min	2nm	4min (UVO)
UVO 1minX4	4	0.5nm	UVO 1min	2nm	4min (UVO)

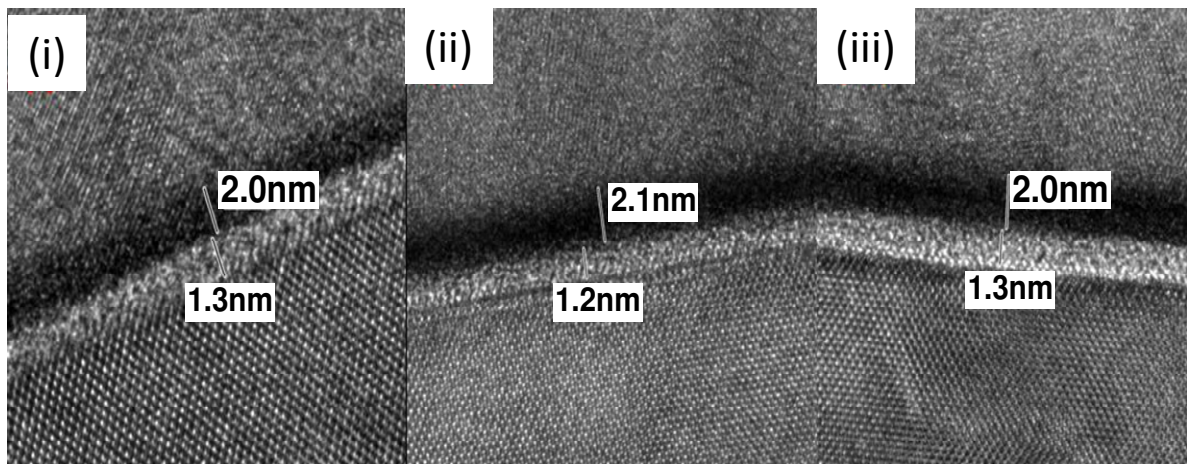


Fig. 6.2 TEM pictures confirm that all samples annealed at different condition have similar EOT, ~1.3 nm IL and ~2.0 nm HK. (i) RTP 600 °C 30 s; (ii) UVO 2min × 2; and (iii) UVO 1min × 4. Clear crystallization is observed in RTP samples.

6.3 Results and Discussion

6.3.1 Electrical Characterization

The HfZrO with one-time only UVO anneal was initially studied, and high leaky behavior from CV measurement is revealed in **Fig. 6.3 (a)**. This is probably due to that UVO treatment can only modify very top surface quality [3], which means the bottom HfZrO may still act like the as-deposited one with low quality. The modification is likely constrained within 1nm region, as the 2min \times 2 UVO annealed device displays well-behaved CV curve, as shown in **Fig. 6.3 (b)**. Further in this figure, the measured CV from the devices receiving MDMA can perfectly match with the CVC simulation with quantum mechanical correction [4], suggesting excellent device quality. The extracted EOT (\sim 1.2 nm) of MDMA devices are similar with the RTP control (inset of **Fig. 6.3 (b)**), in consistent with TEM observation.

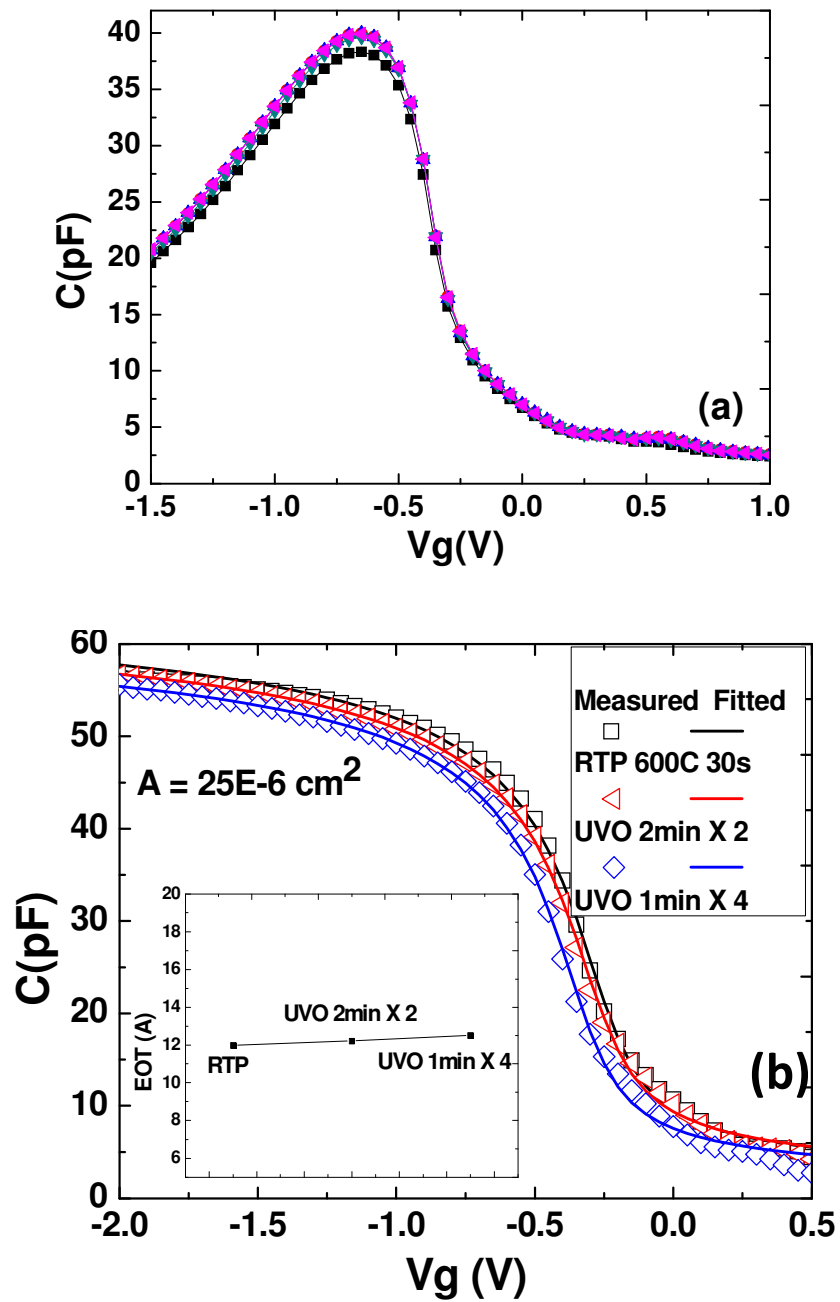


Fig. 6.3 (a) Measured CV for devices with only one-time UVO annealing after HK deposition; devices shows high leaky behaviour (b) measured (symbols) and fitted (lines) CV curves for devices with conventional RTP (control) and MDMA (UVO annealing). Inset shows all samples are with similar EOT.

Gate leakage current (J_g) measurement of all devices is shown in **Figs. 6.4 & 6.5**. It is observed the J_g reduction becomes greater with the increase the number of D & A cycles. It shall be noted that current density of RTP control still has 3-4 order of reduction compared to Poly-Si/SiO₂ benchmark, which is similar as literatures [5-7], suggesting reasonable quality of control devices. It is also observed that MDMA can significantly reduce leakage current by more than one order of magnitude and it is worth noting that J_g reduction is more prominent with the increasing number of D & A cycles. More than two order of leakage reduction was achieved for the UVO 1min × 4 sample as compared to the RTP control at both 25 °C and 125 °C.

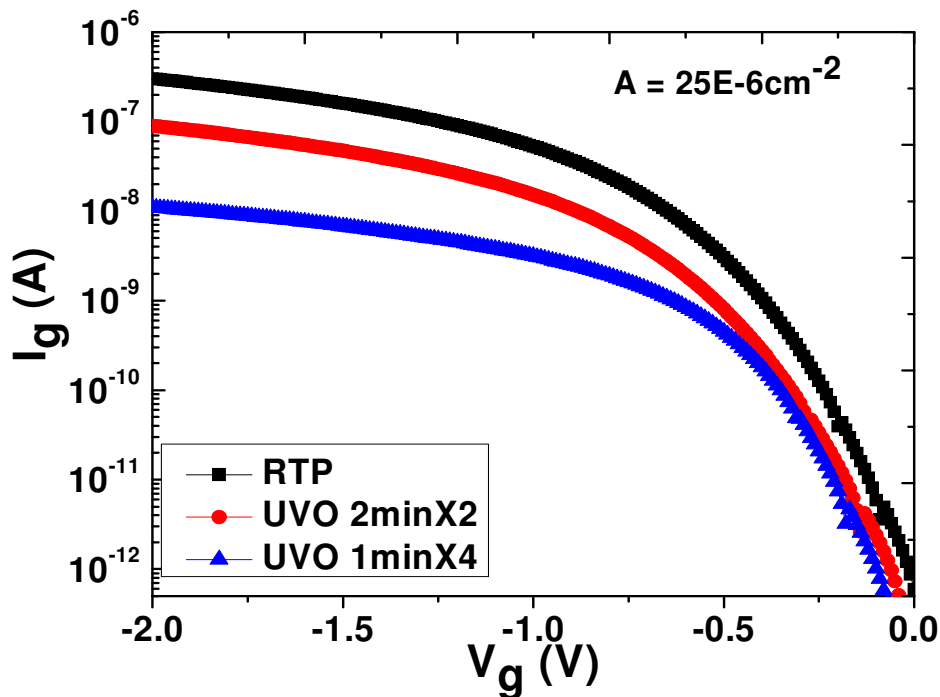


Fig. 6.4 Measured gate leakage current at room temperature. Leakage reduction more than one order is observed for UVO 1min × 4 sample compare with RTP control.

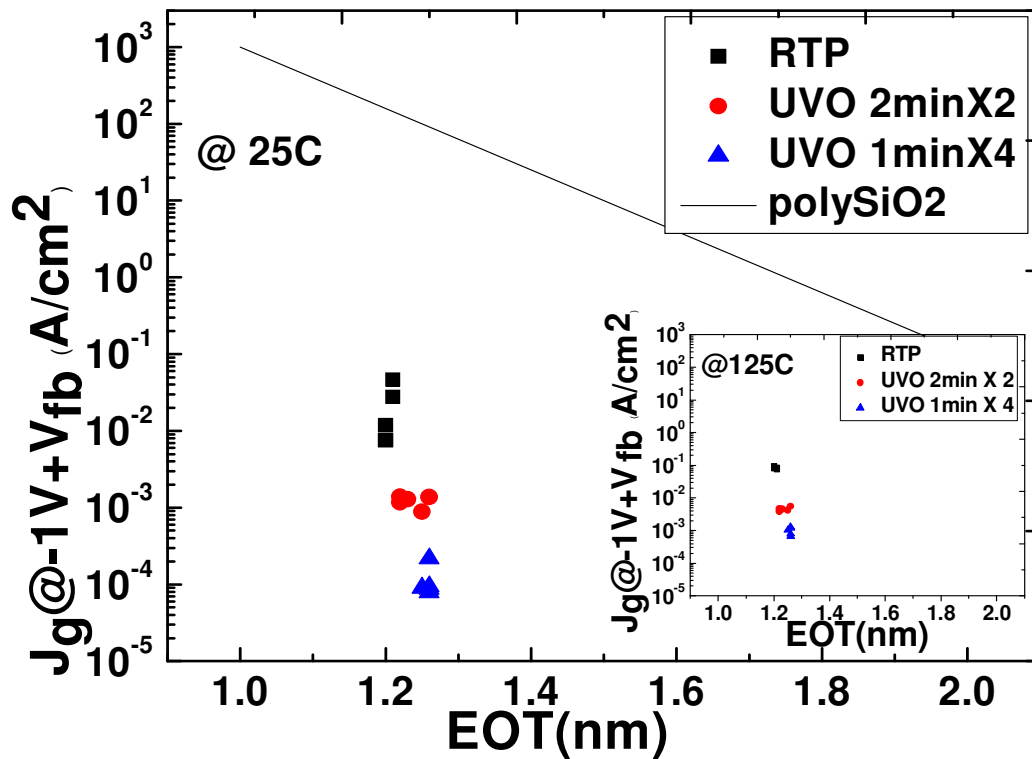


Fig. 6.5 Current density versus EOT at room temperature in comparison with Poly/SiO₂ benchmark for devices with different annealing conditions. More than 1 order leakage reduction at similar EOT regime is observed for UVO 1min × 4 sample compare with RTP control. High T leakage is shown in the inset. Similar leakage reduction trend is observed.

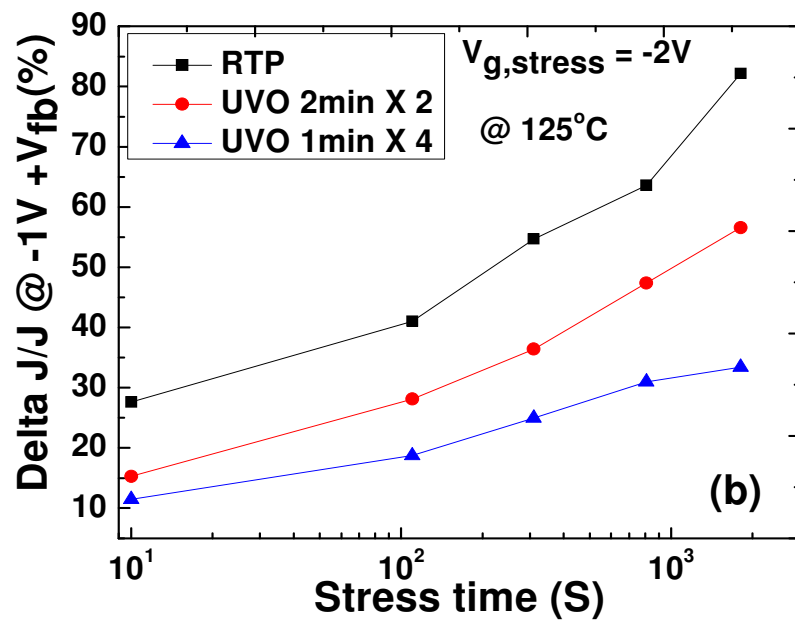
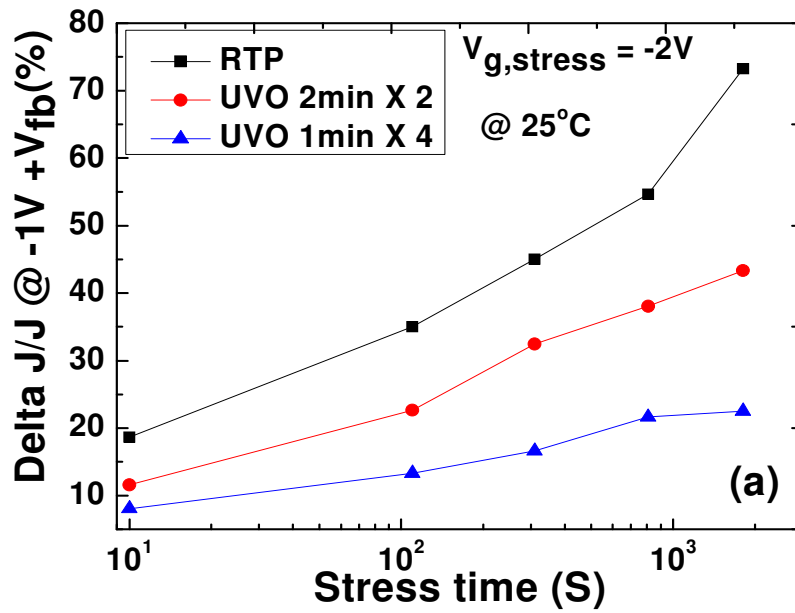


Fig. 6.6 Stress induced leakage current increase at (a) 25 °C; (b) 125 °C. At both temperatures, UVO annealed samples are less susceptible to current degradation at given bias condition ($V_{g, stress} = -2 V$), which is more prominent with increasing D & A cycles.

The stress induced J_g increase and flat band voltage (V_{fb} , extracted from CV simulation) shift are shown in **Figs. 6.6 & 6.7**, respectively. UVO 1min \times 4 sample shows best immunity to stress induced degradation, followed by UVO 2min \times 2 and then the RTP control one. In **Fig. 6.8**, it is seen that MDMA can significantly improve the breakdown voltage (V_{BD}).

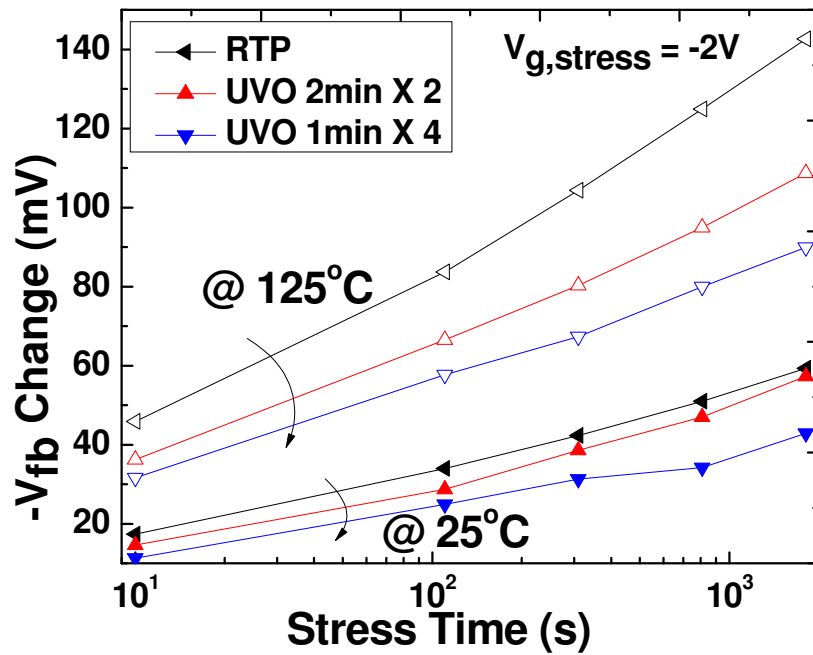


Fig. 6.7 Stress induced flat band voltage shift at 25 °C and 125 °C. UVO annealed samples are less prone to V_{fb} degradation after stress, which is probably due to less charge trapping inside the UVO annealed film.

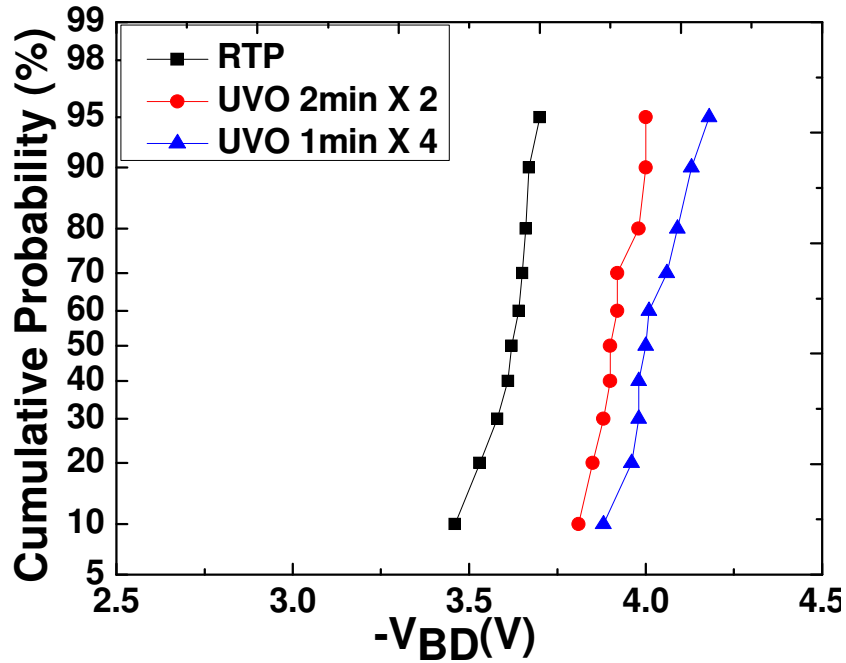


Fig. 6.8 Cumulative probability of breakdown voltage for samples with different PDA. MDMA can significantly improve the breakdown voltage while increasing the number of D & A cycles can further improve V_{BD} .

TDDB characteristics and projected life time comparison among all the samples are shown in **Fig. 6.9** and **Fig. 6.10**, respectively. The projected TDDB lifetime is predicted from a series of TDDB measurements under different stressing voltages (-3.3 V, -3.5 V and -3.7 V). The extracted 10-year lifetime for the UVO 1min \times 4 sample (-1.55 V) is improved compared to that of the RTP control (-1.36 V). The TDDB lifetime prediction of devices with MDMA is significantly prolonged. Again for both TDDB and V_{BD} , the improvement is closely correlated with the number of D & A cycles.

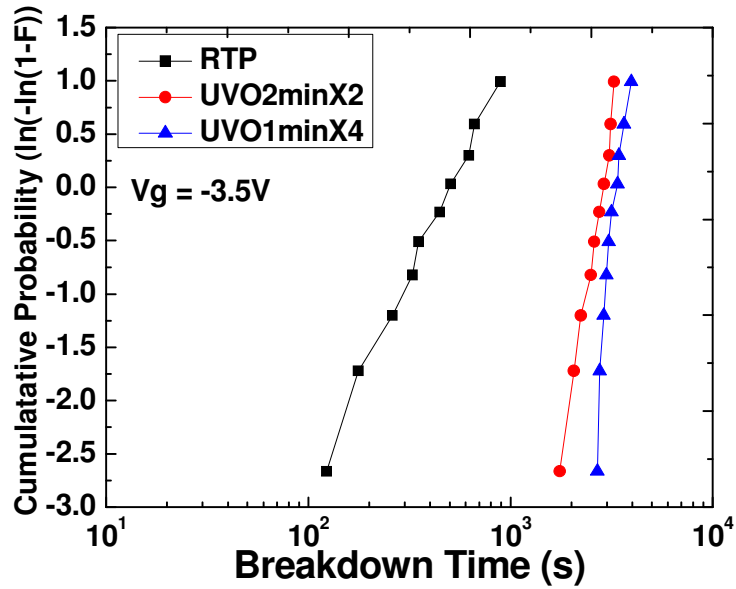


Fig. 6.9 TDDDB characteristics at a given stress voltage ($V_g = -3.5$ V). The Breakdown time is significantly increased for samples annealed using MDMA (UVO annealing) compare with RTP control samples.

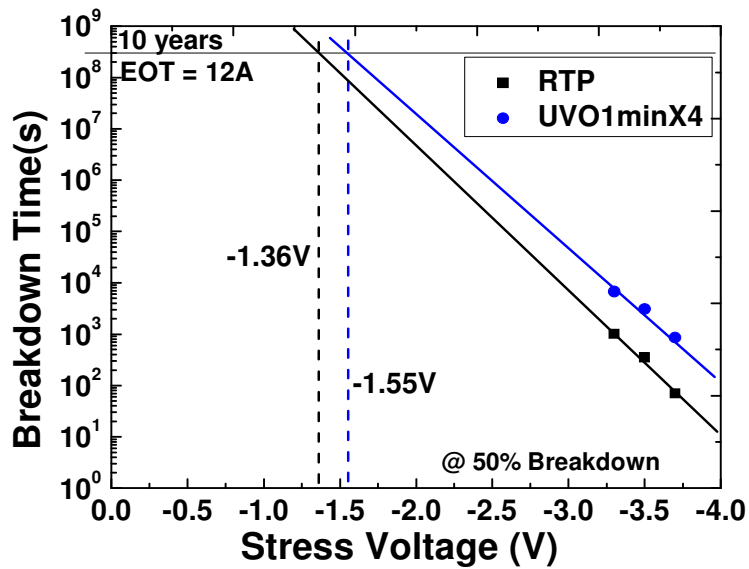


Fig. 6.10 TDDDB lifetime projections as a function of stressing voltage. 10 years life time is -1.36 V and -1.55 V for samples annealed at RTP and UVO 1min \times 4 conditions, respectively.

The observed improvement mentioned above is probably due to less charge trapping inside the high- k film annealed by the MDMA technique, as a result of the healing of oxygen vacancies, which can serve as charge trapping centers [8].

6.3.2 Physical Characterization

6.3.2.1 Scanning Tunneling Microscopy (STM) analysis

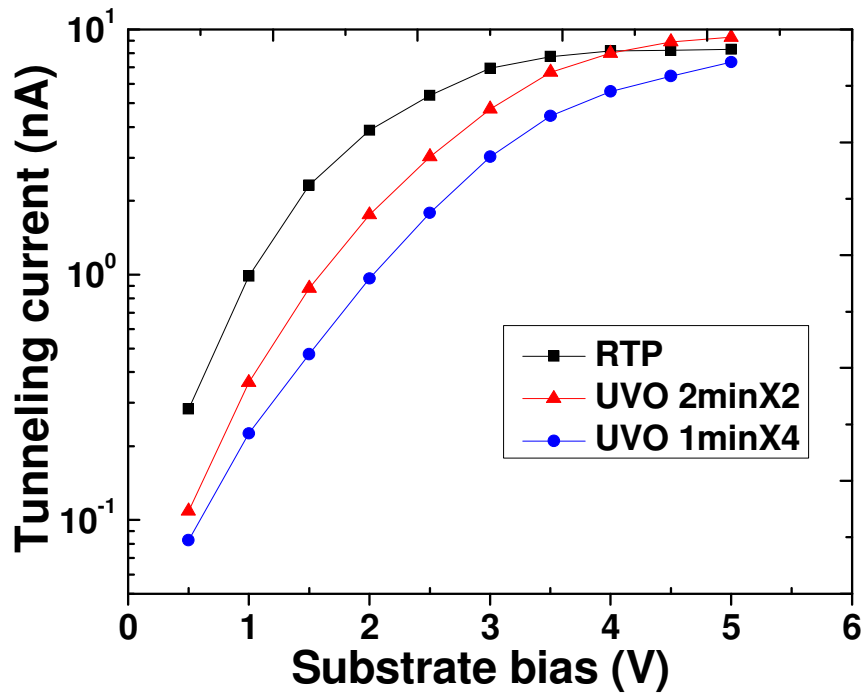


Fig. 6.11 Tunneling current collected by STM for different samples. UVO annealed samples shows much lower leakage than RTP control samples. Increasing number of D & A cycles gives additional tunneling reduction.

The exactly same HK/IL stacks were prepared for STM and XPS studies. STM measurement in ultra-high vacuum was used to study HfZrO/IL/Si stack at the atomic level. As shown in **Fig. 6.11**, the tunneling current collected by STM from MDMA UVO samples is much lower than RTP control and interestingly, the tunneling leakage is reduced with increasing the number of D & A cycles, in excellent agreement with the J_g measurement as presented in **Figs. 6.4 & 6.5**.

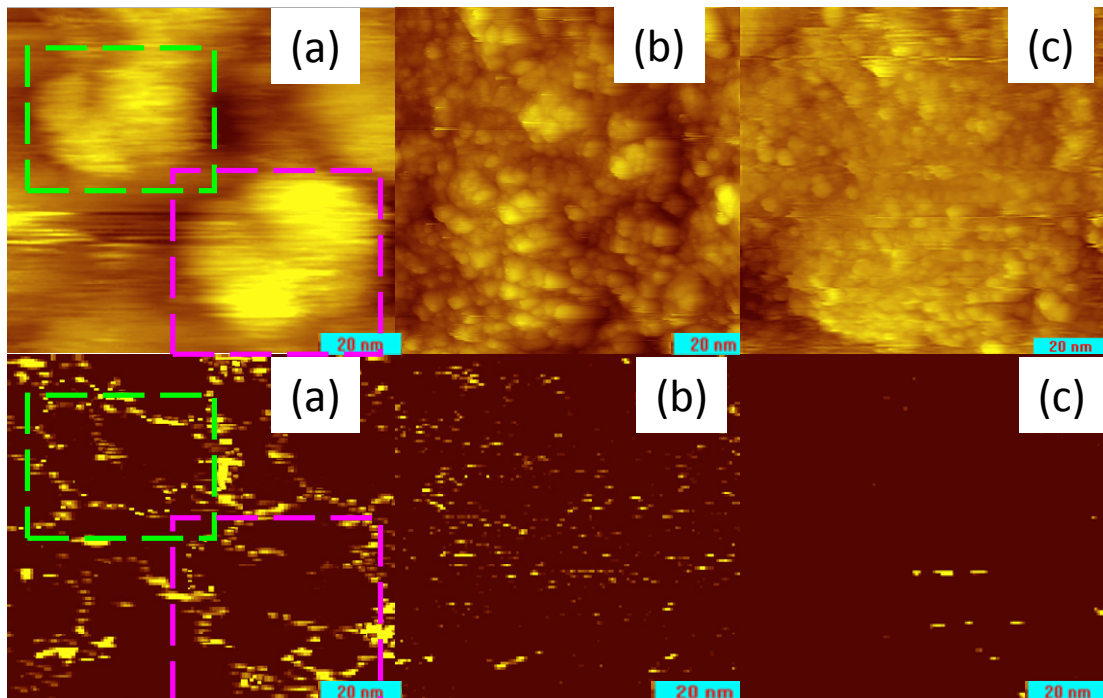


Fig. 6.12 High- k topography (upper) and the corresponding current map (lower) by STM of samples after (a) RTP 600 °C 30 s, (b) UVO 2min \times 2, and (c) UVO 1min \times 4. Clear grains are observed in RTP samples. Bright shades correspond to locally higher tunneling current.

The HK topography scanned by STM and corresponding current maps are shown in **Fig. 6.12**. Bright shades in the current map correspond to locally higher tunneling current. Clear grains are observed in RTP sample (in consistent with TEM of **Fig. 6.2**) and the tunneling current is much higher along the grain boundaries than inside the grains (**Fig. 6.12(a)**). On the other hand, MDMA samples do not show noticeable granular features, suggesting HK remains amorphous, also match with TEM. It is worth noting that MDMA 1min \times 4 sample has the lowest tunneling leakage as can be seen from the current map (**Fig. 6.12(c)**), followed by MDMA 2min \times 2 sample (**Fig. 6.12(b)**) and then the RTA control one (**Fig. 6.12(a)**). From The current distribution based on the analysis of the corresponding local *IV* spectroscopy, UVO 1min \times 4 sample shows best electrical homogeneity (**Fig. 6.13**).

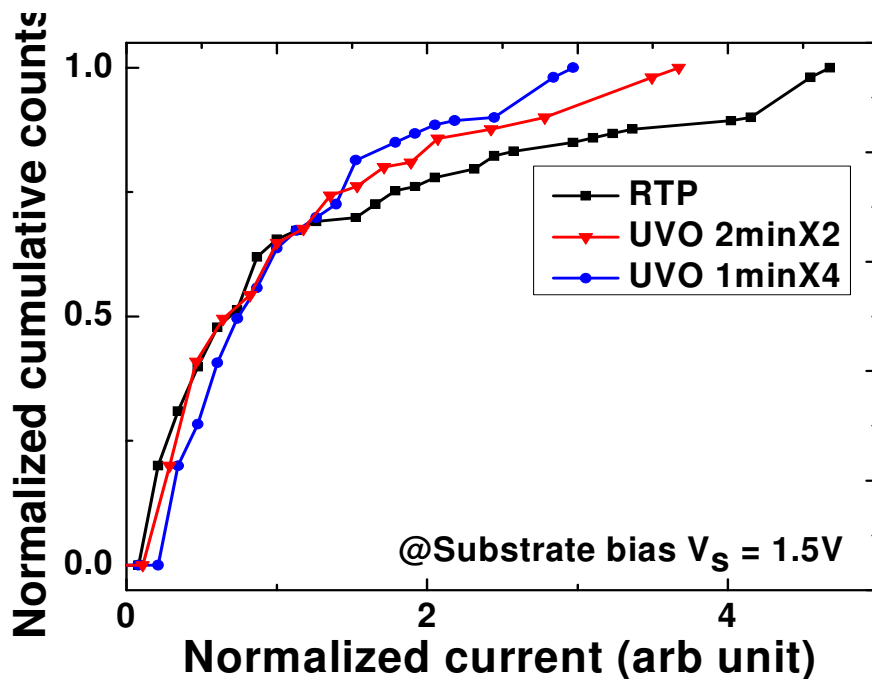


Fig. 6.13 Normalized current distribution based on the analysis of the corresponding local *IV* spectroscopy. UVO 1min \times 4 sample shows best electrical homogeneity.

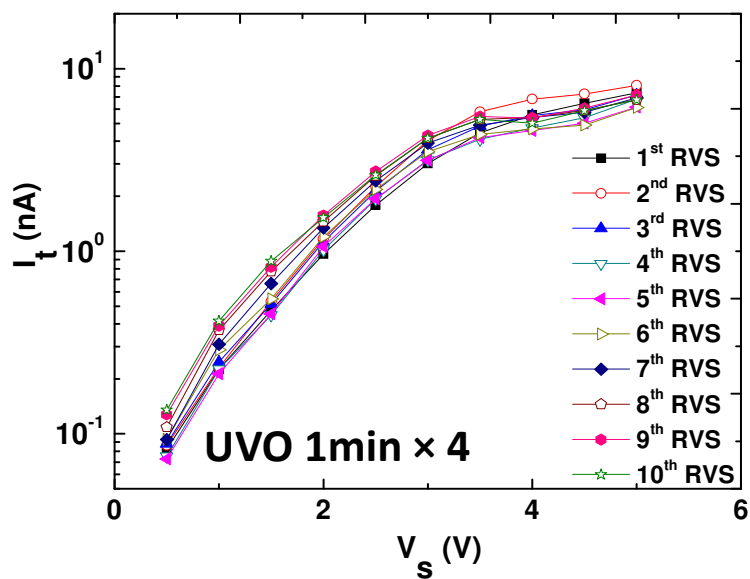
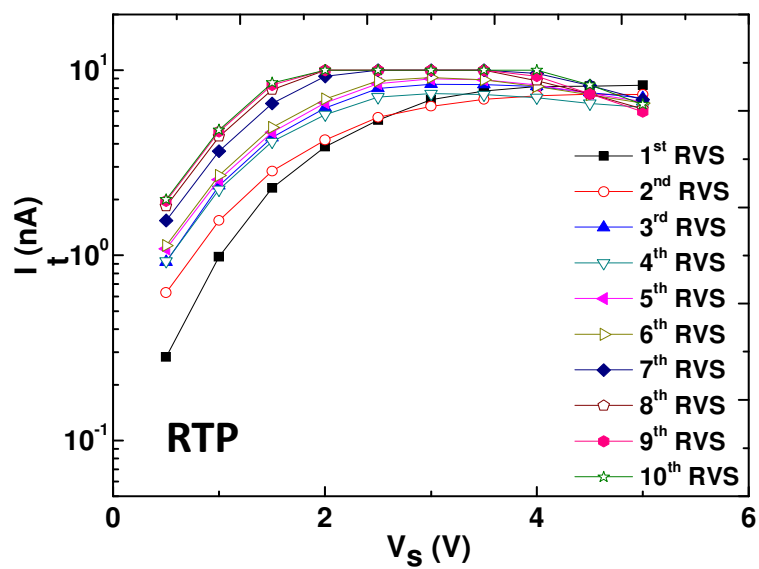
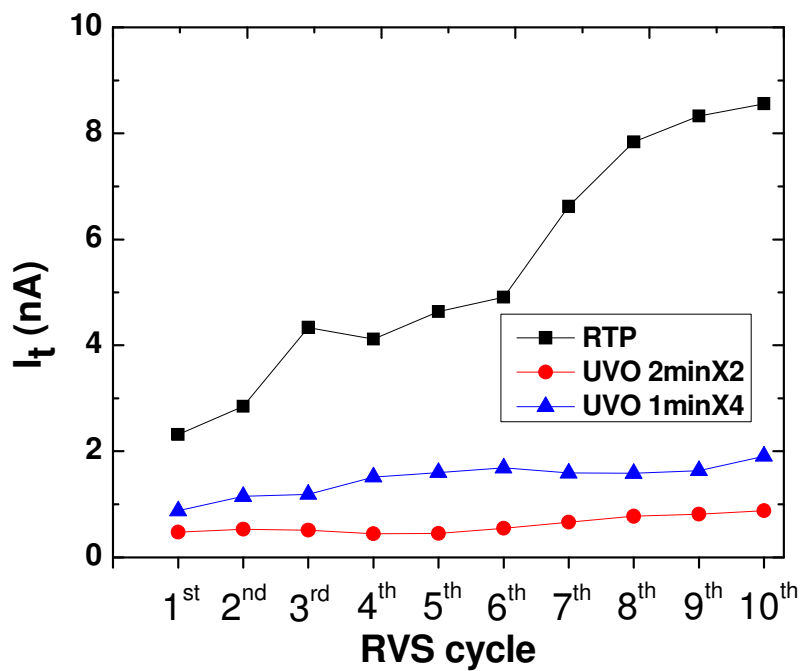


Fig. 6.14 Comparison of I_t evolution by STM (@ $V_s = 1.5$ V) as a function of consecutive Ramp Voltage Stressing (RVS) cycles. Bottoms are the IV sweep of RTP (left) and UVO 1min \times 4 (right) samples under 10 cycles of RVS.

Fig. 6.14 compares the tunneling current evolution under consecutive Ramp Voltage Stressing (RVS). Bottom figures show the IV sweep of RTP and UVO 1min × 4 samples under 10 cycles of RVS. It is clearly noted that the current are much more wide-spread for RTP control after 10 cycles of stressing, suggesting that UVO 1min × 4 has the lowest susceptibility to degradation against RVS, which is also consistent with the stress induced degradation as presented in the electrical characterization part.

6.3.2.2 X-ray photoelectron spectroscopy (XPS) analysis

The XPS of Si 2p spectra are shown in **Fig. 6.15**. The peak intensity located at ~102eV is highest in RTP control and lowest in UVO 1min × 4 one, which is probably due to more Si sub-oxide (SiO_x , $x < 2$) [9] or more Hf-silicate formation [10] at HK/IL interface in RTP control than UVO annealed samples.

It is reported that Hf 4f peak binding energy in Hf-silicate is higher than that in HfO_2 [11]. However, there is no obvious shift in Hf 4f peak binding energy across all three samples, as shown in **Fig. 6.16**, which excludes the Hf-silicate influence that leads to the change of Si 2p spectra. Therefore, the difference of Si 2p spectra, as shown in **Fig. 6.15**, can only be caused by more Si sub-oxide formation at HK/IL interface in RTP control sample.

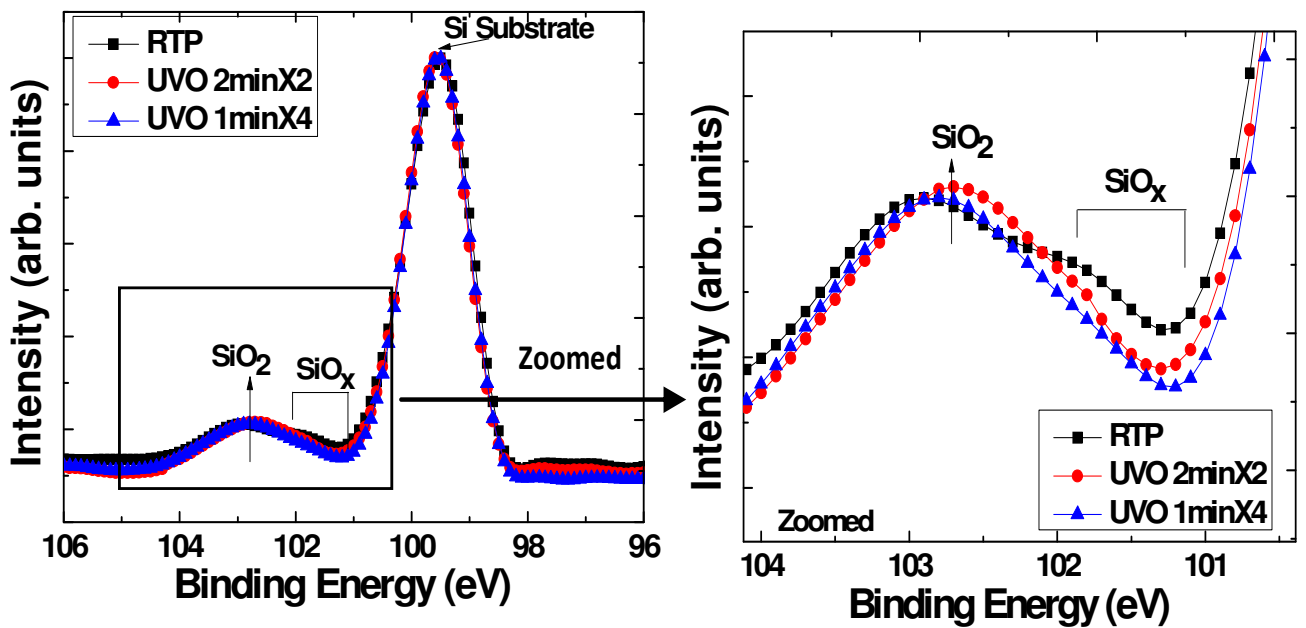


Fig. 6.15 Si 2p XPS spectra of HfZrO/IL/Si stack . UVO 1min × 4 sample shows least sub-oxide intensity, indicating lowest V_o at HK/IL interface. Peak positions all aligned to C 1s peak binding energy.

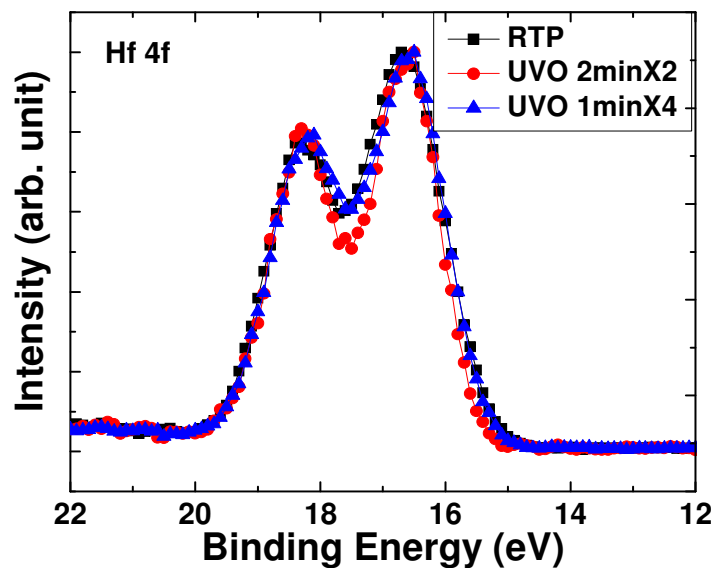


Fig. 6.16 Hf 4f XPS spectra shows no obvious shift, excludes Hf-silicate influence. All peak positions are aligned to the C 1s peak binding energy at 285eV.

This observation implies that the V_o concentration within the HfZrO/IL gate stack is the highest in the RTP control sample, while it is lowest in the UVO 1min \times 4 sample. It is thus believed that fewer V_o would be created inside the HK film prepared using the MDMA technique, owing to oxygen incorporation during the UVO annealing process. Thus fewer V_o would be transferred to HK/IL interface, as the V_o formation energy at the HK/IL interface is lower than that in the bulk HK layer [12]. Thus the detected Si-sub oxide intensity is higher for RTP control than UVO annealed samples.

6.3.3 Proposed Model

Based on STM & XPS, the possible mechanisms explaining why devices with MDMA (UVO annealing) have superior electrical performance are schematically illustrated in **Fig. 6.17**. For RTA control sample, HfZrO films usually become poly-crystallized after high temperature annealing, thus V_o can be easily aggregated along the grain boundaries [13], serving as leakage path. With MDMA using UVO annealing, this phenomenon is suppressed mainly due to 1) the healing of V_o due to oxygen incorporation during UVO annealing: the more D & A cycles, the more healing of V_o , and thus the less V_o -related defects inside the HK film; 2) suppression of grain boundaries, and thus the leakage path is dis-connected.

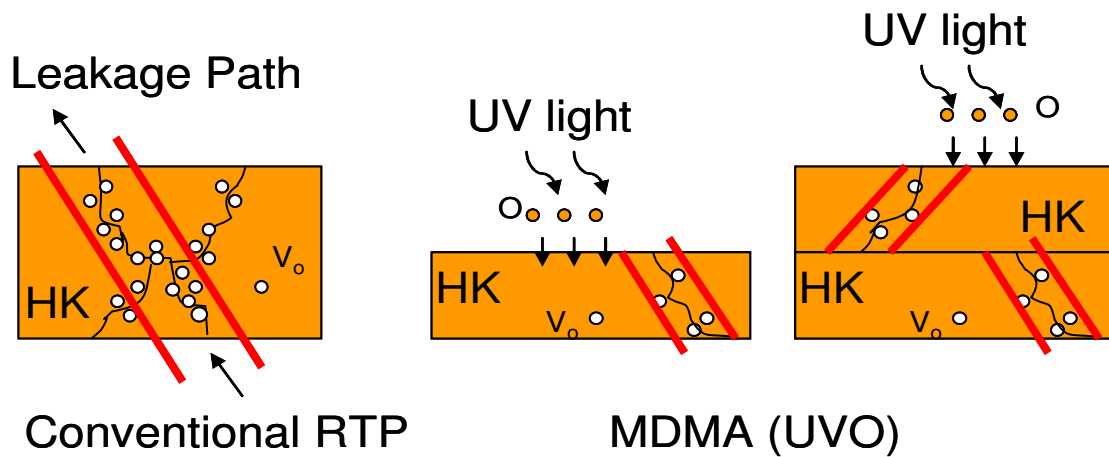


Fig. 6.17 Schematic showing how MDMA (UVO annealing) can potentially improve HK film quality: 1) with UV light, oxygen can be cooperated into to HK film to heal the V_o , especially along grain boundaries; 2) with multi deposition, the grain boundaries, which can serves as leakage path inside the film could be dis-connected due to the healing of V_o , thus leads to leakage reduction.

6.4 Summary

In summary, a novel MDMA technique for ALD HfZrO treatment using room temperature UVO annealing is investigated both physically and electrically. Grain boundary suppression and annealing of V_o are believed to be responsible for its superior electrical performance based on STM and XPS studies. MDMA in UVO is thus a promising HK treatment technique suitable for gate-last integration scheme due to its inherently low thermal budget.

References

- [1]. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neiryneck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. T roeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with high- k +Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", IEDM Tech. Dig. 2007, p.247.
- [2]. T. Nabatame, K. Iwamoto, H. Ota, K. Tominaga, H. Hisamatsu, T. Yasuda, K. Yamamoto, W. Mizubayashi, Y. Morita, N. Yasuda, M. Ohno, T. Horikawa, and A. Toriumi, "Design and Proof of High Quality HfAlOX Film Formation for MOSCAPs and nMOSFETs", VLSI Symp., 2003, p.35.
- [3]. W. J. Song, S. K. So, D. Y. Wang, Y. Qiu, and L. Cao, "Angle Dependent X-ray Photoemission Study on UV-Ozone treatments of Indium Tin Oxide", Appl. Surf. Sci. 177, p.158, 2001.
- [4]. J. R. Hauser and K. Ahmed, in Characterization and Metrology for ULSI Technology, D. G. Seiler, A. C. Diebold, W. M. Bullis, T. J. Shaffner, R. McDonald, and E. J. Walters, Editors, "Characterization of Ultra-Thin Oxides Using Electrical C-V and I-V Measurements", AIP, Woodbury, NY, 1999, pp. 235–239.

- [5]. J. Chen, X. P. Wang, M. -F. Li, S. J. Lee, M. B. Yu, C. Shen and Y. C. Yeo, "NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric", IEEE Electron Device Lett., vol. 28, no. 10, pp. 862-864, Oct. 2007
- [6]. P. D. Kirsch, M. A. Quevedo-Lopez, S. A. Krishnan, C. Krug, H. AlShareef, C. S. Park, R. Harris, N. Moumen, A. Neugroschel, G. Bersuker, B .H. Lee, J.G. Wang, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, J. S. Jur, D. J. Lichtenwalner, A. I. Kingon, and R. Jammy, "Band Edge n-MOSFETs with High- k /Metal Gate Stacks Scaled to EOT=0.9nm with Excellent Carrier Mobility and High Temperature Stability", IEDM Tech. Dig. 2006.
- [7]. L. Wu, H. Y. Yu, K. L. Pey, J. S. Pan, M. Tuominen, Eva Tois, D. Y. Lee, K. Y. Hsu, K. T. Huang, H. J. Tao, and Y. J. Mii, "Electrical and Physical Properties of Er-doped HfO₂ High- k Dielectrics Prepared by Atomic Layer Deposition", Electrochem. Solid-State Lett., 13, G21 2010.
- [8]. C. Shen, M. F. Li, X. P. Wang, H. Y. Yu, Y. P. Feng, A. T.-L. Lim, Y.-C. Yeo, D. S. H. Chan, and D.-L. Kwong, "Negative U traps in HfO₂ Gate Dielectrics and Frequency Dependency of Dynamic BTI in MOSFETs", IEDM Tech. Dig., 2004, p.733.
- [9]. H. Takahashi, H. Minakata, Y. Morisaki, S. Xiao, M. Nakabayashi, K. Nishigaya, T. Sakoda, K. Ikeda, H. Morioka, N. Tamura, M. Kase and Y. Nara, "Ti-capping Technique as a Breakthrough for Achieving Low Threshold Voltage, High Mobility, and High Reliability of pMOSFET with Metal Gate and High- k Dielectrics Technologies", IEDM Tech. Dig. 2009, p427.

- [10]. M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame and A. Toriumi, "Gate-First Processed FUSI/HfO₂/HfSiO_x/Si MOSFETs with EOT=0.5 nm-Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing-", IEDM Tech. Dig. 2007, p523.
- [11]. G. D. Wilk, R. M. Wallace and J. M. Anthony, "Hafnium and Zirconium Silicates for Advanced Gate Dielectrics", J. Appl. Phys. Vol. 87,p. 484, Jan. 2000.
- [12]. J. L. Gavartin, L. Fonseca, G. Bersuker, and A.L Shluger, "Ab Initio Modeling of Structure and Defects at the HfO₂/Si Interface", Microelectron. Eng. vol. 80, p. 412, Jun. 2005.
- [13]. K. McKenna and A. shluger, "the Interaction of Oxygen Vacancies with Grain Boundaries in Monoclinic HfO₂", Appl. Phys. Lett. 95, 222111, 2009.

CHAPTER 7 Device Performance and Reliability

Improvement for MOSFETs with HfO₂ Gate Dielectrics Fabricated using Multi Deposition

Multi Room-Temperature Annealing

7.1 Introduction

High-*k*/metal gate (HK/MG) stack technology has been under intensive investigation to replace conventional SiO₂/ Poly-Si gate stack over the past decades. Starting from 45 nm technology node, HK/MG stack has been successfully introduced into mass production via the implementation of gate-last or replacement gate integration scheme [1-2]. As device size continuously scaled down, gate-last process has been more widely accepted [3], because of its low thermal budget experienced by the gate stack and its ease of threshold voltage (V_t) tuning.

In previous chapter, chapter 6, gate last processed capacitors with HK/MG stack are investigated and show superior performance after room-temperature multi deposition multi annealing (MDMA) in ultraviolet ozone (UVO) ambient, which is mainly due to the healing of oxygen vacancies (V_o) and suppression of grain boundaries based on the

Scanning Tunneling Microscopy and X-ray Photoelectron Spectroscopy analysis [4]. In this chapter, with the application of the newly developed UVO MDMA method on the HK/Metal (HfO₂/TiN) gated nMOSFETs, enhanced channel electron mobility, improved immunity to biased temperature instability and reduced gate dielectric relaxation current are successfully demonstrated. It is believed that the reduction of interface trap density thanks to the healing of V_o plays an critical role for the improvement. The novel room temperature UVO annealing is believed to be a promising technique to enhance the gate stack integrity in a gate last integration scheme.

7.2 Experimental

The nMOSFETs devices were fabricated using p-type (100) Si substrates with 6×10^{15} cm⁻³ boron doping. After active area definition, source/drain implantation of arsenic (20k eV, 1×10^{15} cm⁻²) was performed, followed by dopant activation. ~4nm HfO₂ was then deposited by ALD using MDMA technique (deposition at 300 °C during ALD and annealing at room temperature ex-situ in an UVO chamber with 254 nm wavelength). The Tetrakis (dimethylamino) hafnium/H₂O was used as the Hf/O precursors, respectively for the ALD deposition. The UV light was generated by a low pressure mercury vapor grid, and its interaction with oxygen produced the ozone. Two different samples were prepared: 2min × 2 (1min × 4) means 2 (4) D & A cycles, i.e. after 2 nm (1 nm) HfO₂ deposition, the sample was annealed in UVO chamber for 2 mins (1 min). The total HK thickness and UVO annealing time for these two samples are the same. A control ALD HfO₂ was annealed by RTP at 600 °C for 30 s in N₂ with traceable amount of oxygen [5].

The total ALD deposition cycles are kept as constant to ensure all samples are with a similar EOT [4]. TiN electrode of ~50 nm thickness was then deposited by sputtering and patterned. Finally, all samples received a forming gas annealing at 425 °C for 30 mins without other thermal budget to imitate the gate-last process. The capacitors were also fabricated using exactly the same method except that the source/drain implantation step was skipped.

7.3 Results and Discussion

Fig. 7.1 shows the I_d - V_g characteristics of nMOSFETs with different D & A methods. Subthreshold slope of ~76 mV/dec was obtained for all samples, suggesting good device quality. It is noted that I_d is higher for samples with UVO MDMA and increases with the greater number of D & A cycles. This improvement may be interpreted by the enhancement of the channel electron mobility after UVO MDMA treatment, as shown in **Fig. 7.2**.

It is reported that V_o can serve as charge trapping centers [6], and thus the increase in the V_o density will degrade the channel carrier mobility and threshold voltage (V_t) stability [7]. Therefore, with UVO MDMA treatment, the channel electron mobility is increased mainly due to the healing of V_o by oxygen incorporation into the HK film during UVO annealing process. And the more cycles of D & A, the more healing of V_o can be expected, and thus the fewer V_o -related defects inside the HK film.

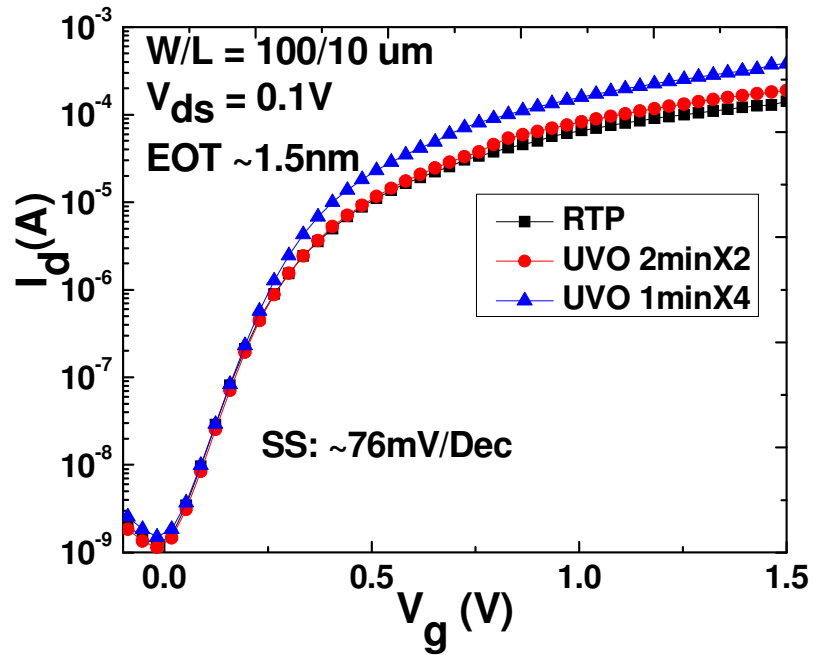


Fig. 7.1 I_d - V_g characteristic of nMOSFETs with different D & A methods.

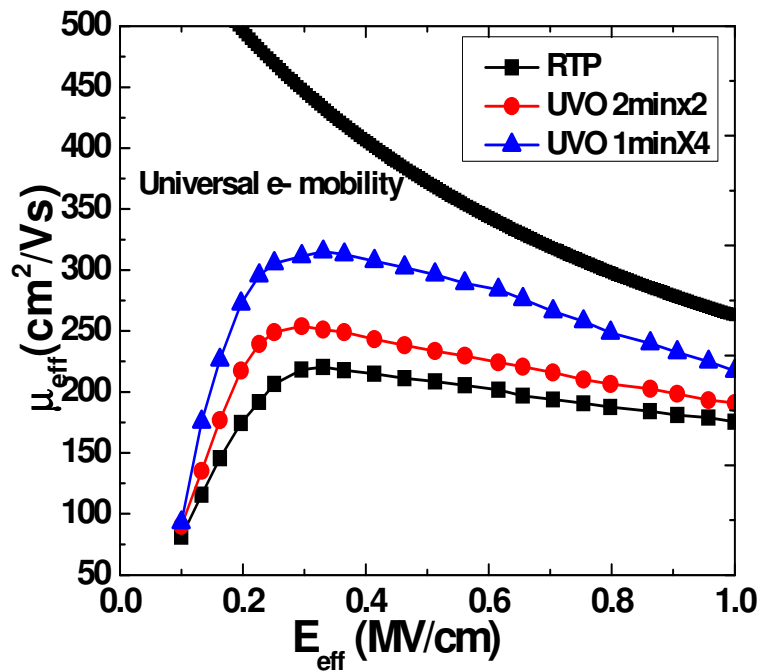


Fig. 7.2 Effective electron mobility extracted by split C - V method and compared with universal electron mobility.

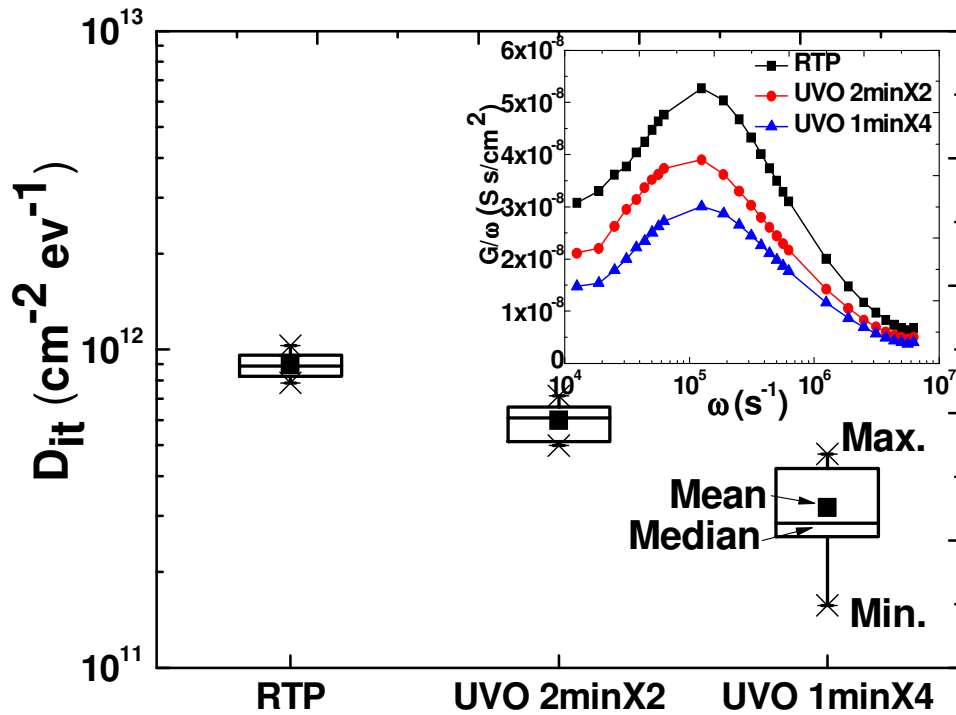


Fig. 7.3 Interface trap density D_{it} extracted by conductance method. Inset shows the measured conductance over frequency (G/ω) as a function of frequency. D_{it} is lowest for UVO 1min \times 4 sample while highest for RTP control.

Conductance-frequency ($G-\omega$) measurement was performed on capacitors to extract interface trap density (D_{it}) at room temperature. The conductance method is based on measuring the equivalent parallel conductance G as a function of bias voltage and frequency [8]. The measured conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density. From **Fig. 7.3**, it is clearly noted that D_{it} is lowest for UVO 1min \times 4 samples, while highest for RTP control ones. This can be explained by the following: with UVO MDMA annealing, fewer V_o would be created inside the HK film, and thus fewer V_o could be

transferred to the HK/IL interface, as the V_o formation energy at HK/IL interface is lower than that in bulk HK layer [9], thus leaving less defected Hf dangling bonds or metallic Hf-Si bonds at the interface [10], contributing to the reduced interface trap density, which is consistent with the enhanced channel electron mobility as shown in **Fig. 7.2**.

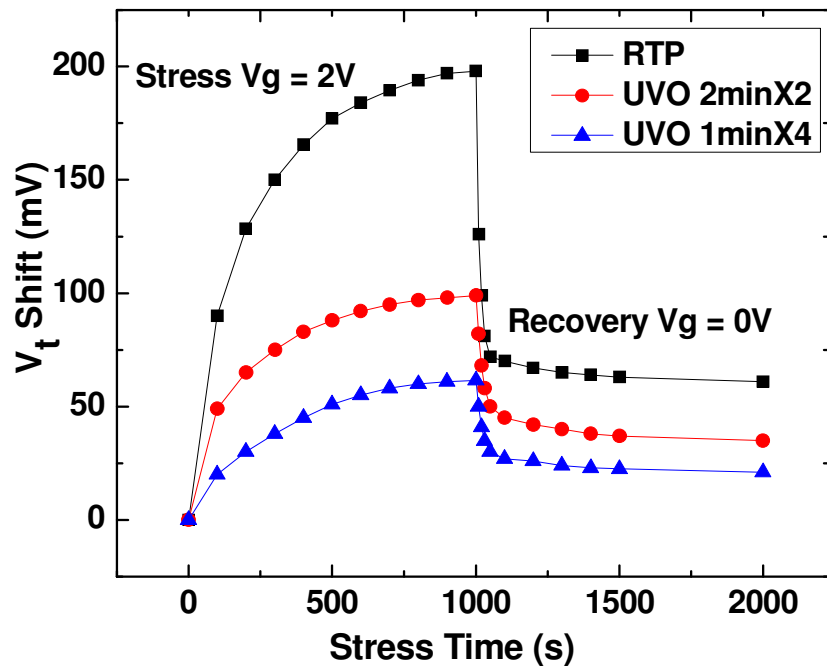


Fig. 7.4 Stress induced threshold voltage (V_t) shift and recovery at room temperature. UVO annealed samples are much less prone to V_t degradation after stress.

Stress induced V_t shifts and recovery at room temperature are shown in **Fig. 7.4**. UVO 1min \times 4 sample shows best immunity to V_t degradation, followed by UVO 2min \times 2 and then the RTP control one. The observed improvement is probably due to less charge trapping inside the HK film annealed by the UVO MDMA technique, as a result

of reduced charge trapping center, i.e. V_o , after UVO MDMA treatment. Again, it shall be noted that the improvement is closely related to the number of D & A cycles.

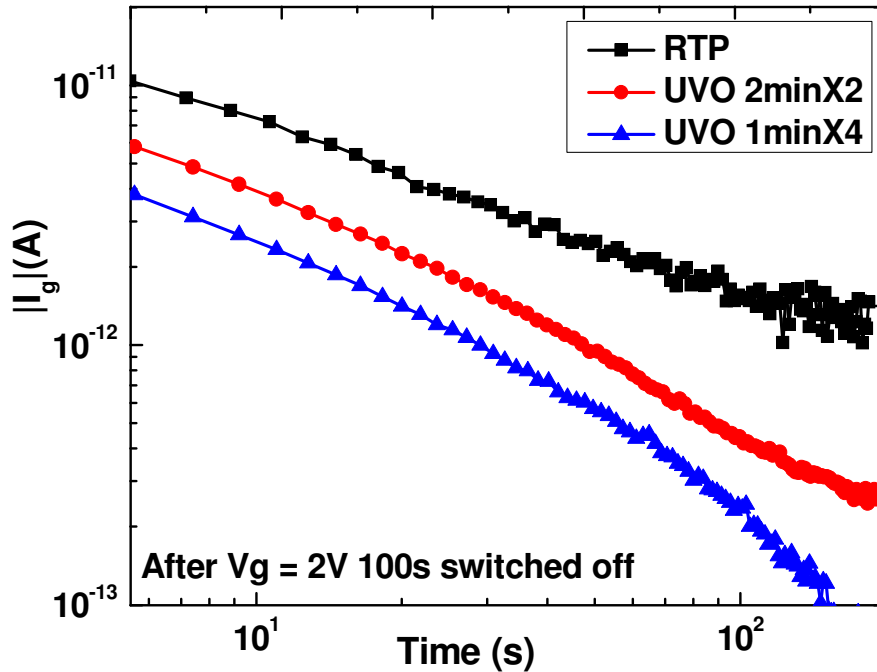


Fig. 7.5 Gate dielectric relaxation current measured after 100 s stressing voltage $V_g = 2$ V is switched off. RTP control shows largest magnitude of relaxation current.

Gate dielectric relaxation current measured after 100 s stressing ($V_g = 2$ V) is switched off is shown in **Fig. 7.5**. The existence of dielectric relaxation current indicates dielectric's integrity, and the disappearance of relaxation current always accompanies with the dielectric breakdown [11]. It is also reported that dielectric relaxation in SiO_2/HK stack is mainly due to the traps near the SiO_2/HK interface [12]. From **Fig. 7.5**, the relaxation current is significantly reduced for samples went through UVO MDMA treatment compared to RTP control, implying that there are fewer interface traps for UVO annealed samples, and thus after gate stressing voltage is suddenly switched off,

less charge de-trapping would occur, resulting smaller magnitude of dielectric relaxation current, which is also in excellent agreement with the extracted D_{it} as shown in **Fig. 7.3**.

7.4 Summary

In summary, a newly-developed MDMA technique for ALD HfO_2 treatment using room temperature UVO annealing is investigated in nMOSFETs. The devices with UVO MDMA treatment show increased channel electron mobility, improved V_t stability after stressing and reduced dielectric relaxation current compared to RTP control, resulting from the reduced bulk oxide traps and interface traps via effectively passivation of V_o during UVO annealing process. MDMA in UVO is thus believed to be a promising HK treatment technique suitable for the gate-last integration scheme due to its inherent low thermal budget.

References

[1]. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neiryneck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High- k +Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", IEDM Tech. Dig. 2007, p.247.

[2]. P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neiryneck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, and S. Natarajan, "High Performance 32nm Logic Technology Featuring 2nd Generation High- k + Metal Gate Transistors", IEDM Tech. Dig. 2009, p.659.

[3]. Solid State Technology, "Common Platform Goes Gate-Last – at Last!", available online:

http://www.electroiq.com/index/Semiconductors/sst-blogs/sst-blog-display/blogs/sst-blogs/chipworks/post987_2728535383529004751.html.

- [4]. L. Wu, H.Y. Yu, K.S. Yew, J.S. Pan, W.J. Liu, and T.L. Duan, "Multi Deposition Multi Room-Temperature Annealing via Ultraviolet-Ozone for HfZrO High- k and Integration with TiN Metal Gate in a Gate-Last Process", IEEE Transaction on Electron Devices, vol. 58, pp. 2177-2181, July, 2011.
- [5]. H. Y. Yu, N. Wu, M. F. Li, Chunxiang Zhu, B. J. Cho, D.-L. Kwong, C. H. Tung, J. S. Pan, J. W. Chai, W. D. Wang, D. Z. Chi, C. H. Ang, J. Z. Zheng and S. Ramanathan, "Thermal Stability of $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ on Si", Appl. Phys. Lett. vol. 81, p. 3618, Nov. 2002.
- [6]. C. Shen, M. F. Li, X. P. Wang, H. Y. Yu, Y. P. Feng, A. T.-L. Lim, Y.-C. Yeo, D. S. H. Chan, and D.-L. Kwong, "Negative U traps in HfO₂ Gate Dielectrics and Frequency Dependency of Dynamic BTI in MOSFETs", IEDM Tech. Dig., p.733, 2004.
- [7]. X. P. Wang, H. Y. Yu, M.-F. Li, C. X. Zhu, S. Biesemans, A. Chin, Y. Y. Sun, Y. P. Feng, A. Lim, Y.-C. Yeo, W. Y. Loh, Q. Q. Lo, and D.-L. Kwong, "Wide V_{fb} and V_{th} tunability for metal-gated MOS devices with HfLaO gate dielectrics", IEEE Electron Device Lett., vol. 28, no. 4, pp. 258–260, Apr. 2007.
- [8]. D. K. Schroder, "Semiconductor Material and Device Characterization". John Wiley & Sons, 3rd ed., 2006.
- [9]. J. L. Gavartin, L. Fonseca, G. Bersuker, and A.L Shluger, "Ab Initio Modeling of Structure and Defects at the HfO₂/Si Interface", Microelectron. Eng. vol. 80, p. 412, Jun. 2005.
- [10]. M. H. Hakala, A. S. Foster, J. L. Gavartin, P. Havu, M. J. Puska, and R. M. Nieminen, "Interfacial oxide growth at silicon/high- k oxide interfaces: First principles modeling of the Si-HfO₂ interface", J. of Appl. Phys., vol. 100, p. 043708, Aug. 2006.

- [11]. W. Luo, T. Yuan, Y. Kuo, J. Lu, J. Yan and W. Kuo, "Charge trapping and dielectric relaxation in connection with breakdown of high- k gate dielectric stacks", Appl. Phys. Lett. vol. 88, p. 202904, May. 2006.
- [12]. Z. Xu, L. Pantisano, A. Kerber, R. Degraeve, E. Cartier, S. D. Gendt, M. Heyns, and G. Groeseneken, "A Study of Relaxation Current in High- k Dielectric Stacks", IEEE Transaction on Electron Devices, vol. 51, no. 3, pp 402-408, Mar. 2004.

CHAPTER 8 Conclusions and Recommendations

8.1 Conclusions

Several advanced topics for high- k /metal gate stacks are systematically investigated to address various concerns under both gate-first and gate-last integration schemes. For gate-first integration, the following two topics are intensively studied: electrical and physical properties of Er doped HfO₂ dielectric deposited by ALD and thermal stabilities of TiN metal gate prepared by different deposition methods.

With the incorporation of Er into HfO₂ high- k dielectric, the work function of TiN metal gate, which is intrinsically p-type like (~4.9-5.1 eV), can be tuned towards to Si conduction band-edge, mainly due to the difference of the electronegativity between the host (Hf) and dopant (Er) atoms. With 7% of Er doped into HfO₂, the TiN metal gate work function can be modulated to a value of ~4.18 eV. XPS and XRD studies prove that the thermal stability of the HfO₂ film is improved after Er is incorporated, while the K -value and leakage properties of HfO₂ are almost maintained. These superb properties make HfErO capable as a candidate for nMOSFET application.

The thermal stabilities of TiN metal gate with various composition prepared by either ALD or PVD on HfO₂ high- k dielectric are investigated and compared by electrical

(*C-V*, *I-V*) and physical (XPS, HRTEM, and EELS) analysis. After annealing at 1000 °C, which is normally required for source/drain activation, nitrogen tends to out-diffuse from TiN regardless of the composition and deposition condition, which is probably the root cause for the work function reduction of TiN metal gate after high temperature annealing as found in other research works. On top of that, oxygen from the interfacial layer between HfO₂ and Si tends to diffuse towards TiN metal gate. PVD Ti-rich TiN shows a wider oxygen distribution in the gate stack and also a thinner IL than the N-rich sample. The oxygen out-diffusion can be significantly suppressed for ALD TiN compared to the PVD TiN samples. These results obtained from comprehensive studies provide insightful guidance for the application of the TiN metal gate in gate-first integration.

For gate-last integration, because of the restriction of the thermal budget on the gate stack, a novel high-*k* deposition and/or post deposition annealing technique is necessary. ALD HfZrO high-*k* fabricated by MDMA technique at room temperature in UVO ambient is systematically investigated for the first time under this background. As compared to the reference gate stack treated by conventional RTA @ 600 °C for 30 s, the capacitors receiving MDMA in UVO demonstrates:

- more than one order of magnitude leakage reduction without EOT penalty at both room temperature and an elevated temperature of 125 °C,
- much improved stress induced degradation in term of leakage increase and flat band voltage shift,
- and enhanced dielectrics break-down strength and TDDB life time.

The improvement strongly correlates with the cycle number of D & A, i.e. the more cycles of D & A, the more improved performance is achieved. STM and XPS analysis suggest both V_o and grain boundaries suppression in the MDMA treated samples are likely responsible for the device improvement.

Besides, the nMOSFETs with UVO MDMA also show superior properties, in terms of enhanced channel electron mobility, improved immunity to biased temperature instability, and reduced gate dielectric relaxation current. This is explained by the reduction of bulk oxide trap and interface trap density because of healing of V_o after UVO MDMA annealing. The novel room temperature UVO annealing is thus promising for the gate stack technology in a gate last integration scheme.

8.2 Recommendations

The following research works could be done in the future by successors to gain more in-depth and complete understanding of the high- k /metal gate stack in advanced CMOS technologies:

1. Higher- k dielectric (k value $> k_{\text{HfO}_2}$) application in gate-last integration. Higher- k material in gate-first integration has been studied by many research groups before. With the incorporation of certain element, for example: Ti. The k value of Hf-based ternary or quaternary dielectric can be increased up to ~50. However, the gate leakage is a concern since the conduction band offset of the dielectric with respect to Si substrate will be significantly lowered after

adding Ti. As gate-last integration scheme is more and more widely accepted in industry since its first introduction in 2007. Thus a creative idea to integrate higher- k dielectric using gate-last approach would be an interesting and practical research topic to work on.

2. Detailed study on MOSFET with MDMA UVO annealing. More characterization can be performed, such as: TDDB, charge pumping, $1/f$ noise, etc. Its impact on pMOSFET can also be investigated.
3. Research on the influence of MDMA UVO annealing temperature on device performance. In this research work, only room temperature UVO annealing is studied in using MDMA method due to the limitation of the equipment capability. Device performance is sensitive to the temperature used in traditional RTP annealing, especially in gate-last integration approach. The O atom become more active and diffuse faster under higher temperature, therefore it can more effectively passivate V_o , thus reducing V_o related defect in high- k dielectric. On the other hand, with higher temperature, O can easily react with Si substrate to form low k SiO interfacial layer, which will degrade the device performance. Thus, the temperature dependent analysis for MDMA UVO annealing is crucial — how the two contradicting mechanisms affect each other and hence impact on the devices' final electrical behavior are pending for future systematic investigation.

Author's Publication List

High-*k*/Metal Gate papers

1. **L. Wu**, H.Y. Yu, K.L. Pey, D.Y. Lee, K.Y. Hsu, K.T. Huang, H.J. Tao, Y.J. Mii, J.S. Pan, M. Tuominen, and Eva Tois, "Electrical and Physical Properties of Er doped HfO₂ high-*k* dielectrics prepared by Atomic Layer Deposition," *Electrochemical and Solid-State Letters*, pp. G21-23, vol. 13 (2), 2010.
2. **L. Wu**, H.Y. Yu, X. Li, K.L. Pey, J.S. Pan, J.W. Chai, Y.S. Chiu, C.T. Lin, J.H. Xu, H.J. Wann, X.F. Yu, D.Y. Lee, K.Y. Hsu, H.J. Tao, "Thermal Stability of TiN Metal Gate Prepared by Atomic Layer Deposition or Physical Vapor Deposition on HfO₂ High-*k* Dielectric", *Applied Physics Letter*, vol. 96, pp.113510, March, 2010
3. **L. Wu**, H.Y. Yu, X. Li, K.L. Pey, K.Y. Hsu, H.J. Tao, Y.S. Chiu, C.T. Lin, J.H. Xu, H.J. Wan "Investigation of ALD or PVD (Ti-rich vs. N-rich) TiN Metal Gate Thermal Stability on HfO₂ High-*k*", *International Symposium on VLSI Technology, Systems and Applications (2010 VLSI-TSA)*, pp.90, Apr. 2010, Hsinchu, Taiwan, ROC
4. **L. Wu**, H.Y. Yu, "Device Performance and Reliability Improvement for MOSFETs with HfO₂ Gate Dielectrics Fabricated using Multi Deposition Multi Room-Temperature Annealing", *IEEE Electron Device Letter*, vol.32, no. 9, pp. 1173, September, 2011.
5. **L. Wu**, K.S. Yew, D.S. Ang, W.J. Liu, T.T. Le, T.L. Duan, C.H. Hou, X.F. Yu, D.Y. Lee, K.Y. Hsu, J. Xu, H.J. Tao, M. Cao, and H.Y. Yu, "A Novel Multi

- Deposition Multi Room-Temperature Annealing Technique via Ultraviolet-Ozone to Improve High-*k*/Metal (HfZrO/TiN) Gate Stack Integrity for a Gate-Last Process,” *IEEE International Electron Device Meeting 2010 (IEDM-2010)*, pp.11.6-1, Dec., 2010, SF, USA
6. **L. Wu**, H.Y. Yu, K.S. Yew, J.S. Pan, W.J. Liu, and T.L. Duan, “Multi Deposition Multi Room-Temperature Annealing via Ultraviolet-Ozone for HfZrO High-*k* and Integration with TiN Metal Gate in a Gate-Last Process”, *IEEE Transaction on Electron Devices*, vol. 58, pp. 2177-2181, July, 2011.
 7. T.L. Duan, H.Y. Yu, **L. Wu**, Z.R. Wang, and J.S. Pan, “Investigate HfO₂ High-*k* Dielectrics Electronic Structure on SiO₂/Si substrate by X-ray Photoelectron Spectroscopy”, *Applied Physics Letter*, vol. 99, pp.012902, July, 2011.

Resistive RAM (RRAM) paper

8. X.A. Tran, H.Y. Yu, Y.C. Yeo, **L. Wu**, W.J. Liu, Z.R. Wang, Z. Fang, K.L. Pey, X.W. Sun, A.Y. Du, B.Y. Nguyen, and M.F. Li, “A High Yield HfOx Based Unipolar Resistive RAM Employing Ni Electrode Compatible with Si-Diode Selector for Cross-Bar Integration”, *IEEE Electron Device Letter*, vol.32, no. 3, pp. 396, March, 2011
9. X.A. Tran, B. Gao, J.F. Kang, **L. Wu**, Z.R. Wang, Z. Fang, K.L. Pey, Y.C. Yeo, A.Y. Du, B.Y. Nguyen, M.F. Li and H.Y. Yu, “High Performance Unipolar AlO_y/HfO_x/Ni based RRAM Compatible with Si Diodes for 3D Application”, *IEEE Sym. VLSI Tech. 2011 (VLSI-2011)*, pp. 44, Jun., 2011, Kyoto, Japan.

10. X.A. Tran, B. Gao, J.F. Kang, X. Wu , **L. Wu**, Z. Fang, Z.R. Wang, K.L. Pey, Y.C. Yeo, A.Y. Du, B.Y. Nguyen, M.F. Li, H.Y. Yu, “Self-Rectifying and Forming-Free Unipolar HfO_x based-High Performance RRAM Built by Fab-Availbe Materials”, *IEEE International Electron Device Meeting 2011 (IEDM-2011)*,), pp.31.2.1, Dec., 2011, Washington DC, USA.
11. Z. Fang, H.Y. Yu, W. J. Liu, K.L. Pey, X. Li, **L. Wu**, Z.R. Wang, Patrick G.Q. Lo, B.Gao, J. F. Kang, “Bias Temperature Instability of Binary Oxide Based (HfO_x) ReRAM” *2010 International Reliability Physics Symposium (IRPS-2010)*, pp. MY.4.1, May, 2010 Anaheim, USA
12. Y S Chen, J F Kang, B Chen, B Gao, L F Liu, X Y Liu, Y Y Wang, **L. Wu**, H Y Yu, J Y Wang, Q Chen and E G Wang, “Microscopic mechanism for unipolar resistive switching behaviour of nickel oxides”, *J. Phys. D: Appl. Phys.* **45** (2012) 065303.

Graphene Papers

13. Zhongrui Wang, V. Tjoa, **L. Wu**, W.J. Liu, Z. Fang, X.A. Tran, J. Wei, and H.Y. Yu, “Mechanism of Different Switching Directions in Graphene Oxide based RRAM”, *Journal of Electrochemical Society*, pp. K177-182, vol. 159 (6), 2012.
14. Zhongrui Wang, W. G. Zhu, A. Y. Du, **L. Wu**, Z. Fang, X.A. Tran, W. J. Liu, K. L. Zhang and H.Y. Yu, “Highly uniform, self-compliance and forming free ALD HfO₂ based RRAM with Ge Doping”, *IEEE Transaction on Electron Devices*, vol.59, no.4, pp. 1203, April, 2012.

15. W. J. Liu, X. W. Sun, Z. Fang, Z. R. Wang, X. A. Tran, F. Wang, **L. Wu**, G. I. Ng, J. F. Zhang, J. Wei, H. L. Zhu and H. Y. Yu, “Positive Bias Temperature Instability in Single and Multilayer Graphene Field Effect Transistors”, *IEEE Electron Device Letter*, vol.33, no. 3, pp. 396, March, 2012.
16. W. J. Liu, X. W. Sun, X. A. Tran, Z. Fang, Z. R. Wang, F. Wang, **L. Wu**, J. F. Zhang, J. Wei, H. L. Zhu and H. Y. Yu, “ V_{th} Shift in Single Layer Graphene Field Effect Transistors and Its Correlation with Raman Inspection,” *IEEE Transaction on Devices and Materials Reliability*, **accepted**, 2012.
17. W. J. Liu, H. Y. Yu, Z. Fang, X. A. Tran, Z. R. Wang, F. Wang, **L. Wu**, J. F. Zhang, R. Murali, James D. Meindl, J. Wei, H. L. Zhu, “Ambient Doping Effect in NBTI and PBTI for Single Layer Graphene Field Effect Transistors”, *IEEE Electron Device Letter*, **under revision**.