

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**FABRICATION AND CHARACTERIZATION OF
ALGAN/GAN HIGH ELECTRON MOBILITY
TRANSISTORS ON SILICON**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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ABSTRACT

“Moore’s Law” states that the number of transistors in an integrated circuit will double approximately every two years. True to this observation, the number of transistors per Si IC indeed has doubled every 18 months since the 1970s. In accordance with the scaling trend predicted in Moore’s Law, not only is the packing density of transistors increased but devices’ performance are significantly improved as well. However as the size of transistors continuously shrinks, several issues such as the fundamental limitation of Si, quantum physics of carrier transport, severity of short channel effects and lithography challenges need to be taken into consideration. Examples of these limitations can be seen in the power density and clock speed of silicon CMOS processors, where it hits saturation at about 100 W/cm^2 and 4 GHz respectively. Owing to such limitations, the margin of improvement achieved by transistor scaling is no longer substantial. Thus, the global semiconductor industry has looked towards the direction of More than Moore (MtM) where both analog and digital functionalities are incorporated into a System-on-chip (SoC) platform for higher system values. For this to materialize, alternative materials with superior properties are explored in the manufacturing of semiconductor devices. Semiconductors with wide band gap properties such as the III-V compound, SiC and diamond have been successfully used in high power electronic applications. Among the III-V compounds, Gallium Nitride (GaN) is a promising alternative due to its superior inherent material properties. With its large band gap, high breakdown field, coupled with high 2DEG carrier density and superior saturation velocity, the properties of GaN offer excellent device

performance, thus attracting significant attention from the next generation of optoelectronics, RF communications and high power applications.

In the fabrication of high electron mobility transistors (HEMTs), it is essential to have device grade AlGaN/GaN heterostructure layers. Generally, the AlGaN/GaN epitaxy layers are mostly grown on foreign substrates such as sapphire and silicon carbide (SiC) due to the current unavailability of large high quality single crystal bulk GaN substrates. Both sapphire and SiC substrates exhibit impressive device performance, but neither offers a clear commercialization pathway due to high growth cost and limited wafer size. Therefore, strong GaN epitaxy research and development efforts which focus on silicon substrates are being pursued, which are primarily motivated by the low cost and scalability of silicon, as well as the well-established Si CMOS process. Unfortunately, the large lattice and thermal mismatch between Si and GaN introduce high threading dislocations, cracking and bowing issues in the substrates. Thus, substantial development have been carried out to grow high quality and crack-free GaN on Si wafers, including thick bulk Si and thin Silicon-on-insulator (SOI) substrates.

In this dissertation, one of the main objectives is to focus on the study and comparison of AlGaN/GaN HEMTs performances on both bulk Si and thin SOI substrates using the standard gold base contact. This paper also aims to discuss the AlGaN/GaN heterostructures growth properties on both substrates, where its properties have been studied and documented. GaN on SOI wafers are found to exhibit lower wafer bowing (~50%) and lower defect density as per High Resolution X-ray Diffraction (HRXRD) analysis. Owing to the reduced bowing and lower epilayer defects, an improvement in the 2DEG mobility and sheet-

resistivity uniformity across the SOI wafers is observed. The HEMT test structures fabricated on SOI substrates exhibit ~20.5% higher drain saturation current and ~19.5% higher peak transconductance as compared to bulk Si. The channel temperature profiles for both substrates have also been investigated using the micro Raman method. Results showed that HEMTs on SOI have a higher channel temperature which is ascribed to the lower thermal conduction of the buried oxide (BOX) layer. Nevertheless with the mitigation of self-heating, GaN-on-SOI substrates is deemed to be an excellent alternative in the Si integration technology.

AlGaN/GaN HEMT is normally-on (depletion mode) in nature due to the existing 2DEG channel which is induced by the strong polarization charges from the AlGaN/GaN heterostructure. A normally-off (enhancement mode) device is desirable as it is able to eliminate negative power supply which reduces the overall design cost, size and complexity of the system. Several approaches in achieving Enhancement mode HEMT have been reported; such as gate recess etching, fluorine plasma treatment, and AlGaN barrier thinning. However, a standard processing method with good controllability, uniformity and reproducibility is still lacking. Therefore, another important objective of this report is to investigate the effect of Germanium diffusion on shifting the threshold voltage of AlGaN/GaN HEMT at the gate region. Si and Ge are generally used as n-type dopants in AlGaN/GaN epilayers. Similarly in Si technology, where dopants are used for threshold voltage adjustment, Ge is believed to be able to compensate the positive sheet charges on the AlGaN surface which reduces the polarization effect and hence depletes the 2DEG carrier concentration. A single RTP annealing (825 °C 60 s) is used to form the

Ohmic contacts as well as to diffuse Ge into the AlGaN barrier concurrently. The fabricated Ge-diffused AlGaN/GaN HEMTs exhibit a threshold voltage shift of +1.15 V, compared to the control sample which has a threshold voltage of -3.52 V. However, there are limitations to this approach as it is constrained by the optimum temperature used in Ohmic contact processing. With higher temperature annealing, a larger positive threshold voltage shift is observed but this is at the expense of Ohmic contact and transconductance degradation coupled with a higher gate leakage. Therefore, the current experimental studies suggest that the Ge doping approach is more suitable as a V_{TH} tuning method.

Although the fabrication cost of GaN-based devices can be reduced significantly through the incorporation with Si technology, there are several challenges which impede the incorporation of GaN-based devices with Si technology. One of them is the prerequisite of Au-free low resistance CMOS compatible metal contacts. AlGaN/GaN HEMTs are typically Au-based devices where Ti/Al/Ni/Au and Ni/Au metal stacks are used as the source/drain and Gate electrodes. However, the use of highly diffusive Au is prohibited in the Si industry due to contamination risks. Moreover, Au-based contacts exhibit an overall rough surface morphology which is unfavorable for high frequency and microwave applications. Several Au-free metal schemes with good contact resistance have been reported but at the expense of high temperature annealing (>800 °C). This increases the thermal budget and limits the self-aligned gate-first process which is a mainstream approach in the Si CMOS technology. Hence in this report, a lower temperature (500 °C) process for Au-free metal scheme using (Ti/Al/NiV) contacts with a contact resistance of 0.8 Ω .mm has been demonstrated on AlGaN/GaN HEMT fabricated on Si (111) bulk

substrates. The Au-free HEMT devices exhibit a smoother surface morphology and overall lower off-state current. Furthermore, excellent I_{ON}/I_{OFF} ratio $\sim 10^9$ with a Subthreshold Swing of 71.42 mV/dec which are desirable for fast switching power applications, were observed in the fabricated devices. Therefore, we believe that the Au-free low temperature metal scheme has great prospects and potential in the fabrication of AlGaN/GaN HEMTs on Si platform.

Last but not least, the performance of AlGaN/GaN HEMT is usually restricted by the severe gate leakage and high access resistance between the source and gate. In order to overcome the gate leakage issue, a MIS structure is introduced, where a high-k material is used as a gate insulator. On the other hand, access resistance can be reduced by decreasing the spacing between source/drain and gate. Nonetheless, the minimum source-to-gate access distance is constrained by the lithography tool's capability and gate alignment issues. Hence, a self-aligned gate first process is usually preferred. Unfortunately, such gate-first process is hard to implement in GaN HEMT fabrication due to the high temperature annealing (>800 °C) needed for source/drain Ohmic contacts formation. Gate degradation and the likelihood of gate-to-drain/source shorts caused by the high thermal-budget Ohmic contact formation preclude the direct implementation of the gate-first approach in GaN HEMT fabrication. Therefore a self-aligned low temperature CMOS compatible processing is preferred. Hence in this report, an innovative self-aligned AlGaN/GaN MISHEMT fabricated using common gold-free metal and single mask for source/drain/Gate is demonstrated. Using Al_2O_3 as the gate dielectric, and the aforementioned low temperature gold-free metal scheme (Ti/Al/NiV), MISHEMT devices with low

interface state density ($\sim 5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) coupled with good gate leakage current characteristics (sub-nA off-state leakage current at $V_G = -15 \text{ V}$) are successfully demonstrated. In addition, the fabricated MISHEMTs exhibit excellent I_{ON}/I_{OFF} ratio and good sub threshold swing characteristics, which reflects on the good quality of our gate stack approach. Such fabrication method reduces the parasitic inhomogeneities associated with the numerous front-end processing steps and offers more flexibility in device design with limited form factor. Hence, the demonstrated novel approach is a promising alternative in gold-free GaN-on-Si integration.

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CHAPTER 1: INTRODUCTION

1.1 Background

1.1.1 More than Moore vs Moore

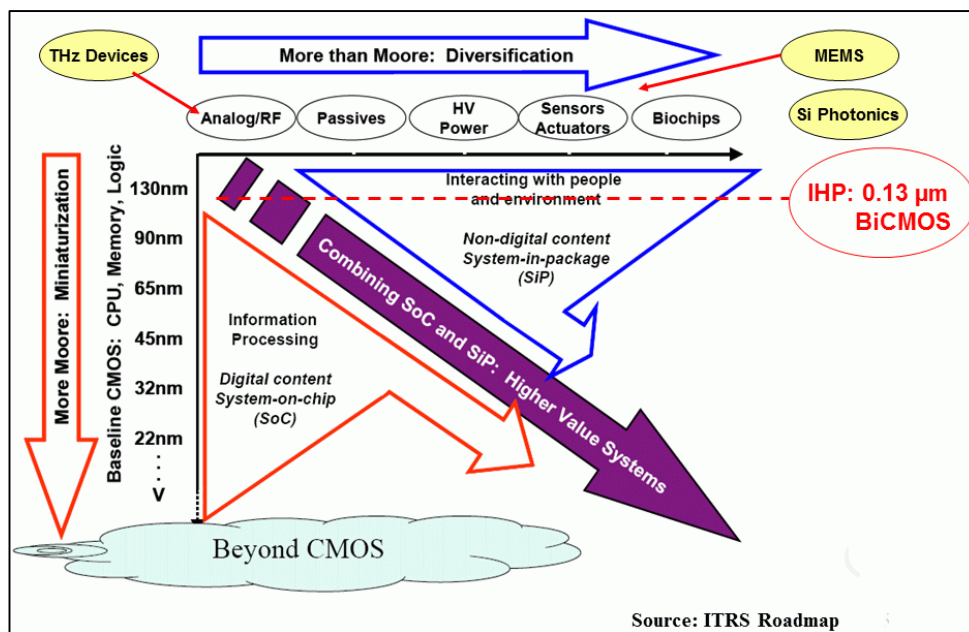


Fig 1.1: Schematic illustration of the miniaturization of digital functions “More Moore” and functional diversification “More than Moore” highlighting the importance of both towards higher value systems (Ref: ITRS 2007) [1, 2].

As early as the 1970s, Moore’s Law has been a dominant force in steering the silicon semiconductor industry towards transistors scaling (Logic, Memory & Microprocessors). Gordon E. Moore, the co-founder of Intel claimed that the number of transistors inside an integrated circuit will double approximately every 2 years (18 months). With rapid advancements in processing technologies such as in the lithography process (double patterning, immersion and extreme

ultra-violet), the critical dimensions of transistors can be shrunk to as small as 14 nm, as claimed by Intel in 2014 [3]. Compared to the number of transistors inside a microprocessor in the year 2000 which used 90 nm technology, a staggering increase in the number of transistors has been observed, going from thousands in the previous decade, to billions of transistors per IC to date [4]. Furthermore, the increase in silicon wafer size from 51 mm (2 inch) in 1969 to 450 mm today (18 inch-*in development*), allows for higher transistor packing density [5]. Therefore with Moore's scaling, the mass production of higher density transistors with significantly lower cost per die can be achieved.

Larger dimension Si wafers which are cheap, abundant and readily available have dominated the semiconductor industry over the past 40 years. In addition, the electrically and thermally stable performance of the native silicon dioxide (SiO₂) insulator has greatly contributed to the development of metal oxide semiconductor field effect transistors (MOSFET) in the CMOS industry. However, as transistors continue to be scaled further, Silicon approaches its fundamental limits, where short channel effects and limitations in quantum physics start to become more dominant. Reliability issues will begin to emerge and silicon will no longer be able to meet market demands for devices with higher operating temperature, power and frequency requirements. The performance of silicon CMOS processors gradually saturate at a power density and clock speed of around 100 W/cm² and 4 GHz, respectively [6]. Moreover, Si-based power devices will start to degrade at temperatures above 200 °C as the maximum operating temperature of a Si junction is around 150 °C [7]. Furthermore, the lithography process is also faced with new challenges as the industry tries to go beyond the 20 nm node [8]. As newer generations of

automotive and RF communication industries demand much higher speed, power and operating temperature, silicon is no longer able to meet the requirements of these applications. The overall improvement margin provided by the higher packing density of transistors alone is no longer substantial. Hence, the global semiconductor industry is looking into a new trend called “More than Moore” (MtM) where both digital and analog functionalities are integrated into a single platform for higher value systems [1]. In order to realize the MtM concept, alternative compound semiconductors with higher performance material properties such as GaAs, SiC and GaN are required.

1.1.2 Gallium Nitride Compound as Alternative

Due to the excellent thermal stability of silicon as well as the well-established CMOS processing line, silicon laterally diffused metal oxide semiconductor (Si-LDMOS) devices, with operating frequencies ranging from 2.5 to 3 GHz, is the state-of-the-art material used in power amplifier industries. However, the major setbacks of these silicon devices are its low breakdown capabilities, lower bandwidth range and small range of operating temperatures [9].

Therefore, III-V semiconductor compounds have been researched intensively by the semiconductor industry as an alternative candidate in fulfilling the demands of applications which require higher performance. Among these materials, Gallium Nitride (GaN) from group III-nitride has attracted significant interest in the industry due to its superior material properties compared to silicon and other competitor materials. Gallium Nitride has direct and wide energy band gap which are suitable for LED and

optoelectronic applications. Furthermore, GaN, in addition to having a high breakdown field, also has high electron saturation velocity and good thermal conductivity which are useful for high power and temperature applications as well as applications in RF telecommunications. The material properties and the applications of GaN devices will be discussed in detail in Chapter 2: Literature Review.

GaN is able to form heterostructure layers with AlGaN, AlN and InN for the development of various devices such as LEDs, laser diodes, high frequency-voltage amplifiers and High Electron Mobility Transistors (HEMTs). In this thesis, the AlGaN/GaN High Electron Mobility Transistors (HEMT) will be the main focus. The advancement of GaN technology has eventually paved its way towards the integration with Si CMOS technology. By integrating GaN on the Si platform, it enables the industry to enhance the performance and functionalities of GaN-based devices while maintaining low manufacturing costs by exploiting the existing and well-established Silicon foundries. This will provide a wider range of operation in terms of power, temperature, and frequency for the next generation of devices.

1.1.3 Development of Gallium Nitride

In 1938, R. Juza and H. Hahn have already reported their findings on the synthesis of Gallium Nitride substrates by supplying liquid gallium with ammonia at a high temperature [10]. Ideally, good GaN-based devices should be fabricated on large single crystal GaN substrates for better lattice matching, lower defect density and smoother morphology properties. However, it is very expensive and difficult to grow single crystalline bulk GaN substrates with such

good qualities. The classical melt approach to grow bulk GaN crystals is not feasible mainly due to the high vapor pressure and low solubility of nitrogen on GaN [11]. The vapor pressure of nitrogen which reaches approximately 1000 atm at 1200 °C, prevents the incorporation of nitrogen into GaN due to the evaporation of nitrogen at high temperatures [12]. Nevertheless, a high temperature is needed in order to dissolve nitrogen into GaN. Therefore it is still a challenge to grow high quality and uniform GaN bulk crystal in large dimensions. As of 2009, GaN costs about \$2000 per cm² for a 2-inch wafer [13]. Due to such high costs, industries tend to grow GaN on foreign substrates such as silicon carbide (SiC) and sapphire instead.

In 1968, the very first growth of single crystalline GaN on sapphire substrate was successfully demonstrated by the H.P. Maruska group using the hybrid vapor phase epitaxy (HVPE) method [14]. Later in 1971, Pankove *et al.* reported the first GaN-based light emitting diode (LED) [15]. However, commercialized LED is still not available back then due to low efficiency. A lot of work has been done with regards to trying to overcome the main challenges of growing high quality GaN films as well as searching for alternative inexpensive substrates to grow n-type and p-type GaN.

Finally there was a major breakthrough in 1986, where Amano *et al.* proposed the metal organic chemical vapor deposition (MOCVD) technique which is capable of growing high quality GaN films on sapphire substrates with the help of an Aluminum Nitride (AlN) nucleation buffer layer at low temperatures [16]. Subsequently in 1991, Khan *et al.* achieved a major breakthrough with the discovery of two-dimensional electron gas (2DEG) which is one of the most important material properties of AlGaIn/GaN

heterostructures in providing high channel velocity applications [17]. Khan reported findings on strong polarization effects which led to the formation of high density 2DEG channels inside AlGa_N/Ga_N heterostructures [18]. This led to the development of the first Ga_N-based Metal-Semiconductor Field Effect Transistors (MESFET) and Heterostructure Field Effect Transistor (HFET) in 1993 and 1994 respectively [19, 20]. Later, Nakamura *et al.* also successfully demonstrated the very first high efficiency (0.22%), double heterostructure blue light LED with an output power of 125 μW [21]. Finally after years of development, in June 2009, the Efficient Power Conversion Corporation (EPC) presented the first commercially available enhancement mode/normally-off AlGa_N/Ga_N HEMTs [22].

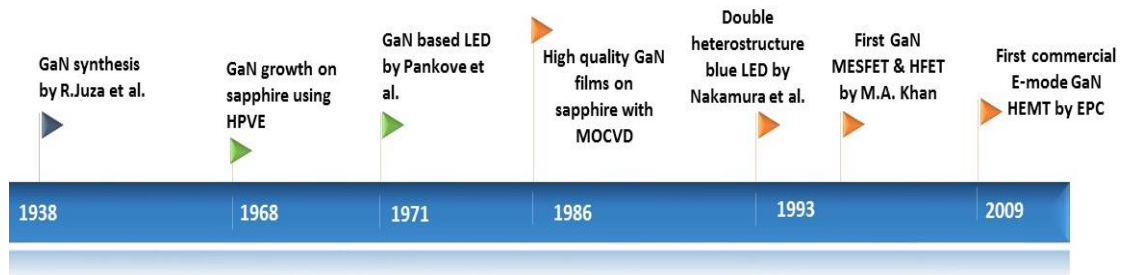


Fig 1.2: A brief timeline of the evolution of Gallium Nitride.

1.1.4 Applications of GaN Devices

Research breakthroughs and advancement in Ga_N technology have given rise to Ga_N devices being used extensively in both optoelectronics and microelectronics industries. When Ga_N was first introduced, it was mainly used in light emitting diodes (LED) in optoelectronics, but due to its unique properties, Ga_N devices were subsequently developed for radio frequency (RF) wireless applications as well. In recent years, Ga_N applications have extended

to the power electronics industry, and today, GaN technology has successfully paved its way into military and aerospace applications.

Since the 1990s, due to its direct and wide energy band gap, GaN devices were commonly used in optoelectronics applications, such as light emitting diodes (LED), photo detectors and lasers [23], where most of these GaN lighting devices were fabricated on sapphire substrates. At a temperature of 300 K, GaN has a band gap energy of about 3.44 eV which corresponds to wavelengths near the ultra violet (UV) region. Unlike GaN, SiC which was initially used to fabricate blue light LEDs for flat panel LED-based television, is not efficient due to its indirect band gap property. With the development of GaN technology, blue and white LEDs were successfully fabricated with a brightness which is reported to be about 100 times better compared to SiC-based LEDs. Common applications of GaN LEDs include backlighting in mobile phones and tablets, white flash lights, chemical pollution sensors, medical sensors, and even in plume detection in military applications. GaN-based blue violet laser diodes, which are used to read Blue Ray data discs, have already become a significant contribution towards the future of this data storage industry. Additionally, blue laser diodes can also be used for laser TV display.

With the development of AlGaIn/GaN HEMT devices, GaN applications started making headway into the microelectronics market, and gained popularity in the telecommunications, power, as well as space and military sectors. In telecommunications, GaN HEMT is used extensively in radio frequency (RF) and wireless telecommunication applications. The high saturation velocity of GaN allows the devices to have high cut-off frequencies, making them suitable for high frequency applications.

As mentioned earlier, the power electronics has been dominated by silicon-based lateral diffused metal oxide semiconductor (Si LDMOS) transistors. Apart from commercially available competitors, such as GaAs Heterojunction Field Effect Transistor (HFET) and Si Bipolar Junction Transistors (BJT), Si LDMOS is considered as the pioneer in power amplifier stations. However, newer generations of devices demand higher power and temperature, as well as a higher frequency range. Correspondingly, silicon based transistors are unable to meet these demands as their performance approaches a saturation point. GaN-based devices, with superior material properties, have provided the industry a promising alternative for applications which require larger frequency bandwidths and higher power densities. As shown in Fig 1.3 below, GaN-based devices are capable of delivering both higher frequency bandwidth and power range for enhanced performance.

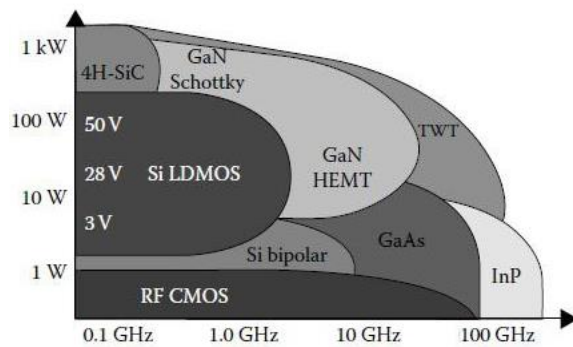


Fig 1.3: Power Frequency Diagram comparing several high power semiconductor electronics materials [24].

The power industry is mainly divided into two sectors; the power management and the power switching industries. The power management sector consists mainly of IT consumer products which operates in a lower voltage range (30 V – 600 V) such as mobile phones, laptop computers, and camera recorders. As for the power switching sector, the high power capability of GaN

devices allow higher voltage applications of up to 1.2 kV. Examples of these applications are automotive vehicles, motors, power generators, DC/AC inverters, and amplifier stations.

As of today, AlGaIn/GaN HEMT is being used in military defense systems as well as in the field of aerospace. AlGaIn/GaN HEMTs can be found in satellite transceivers, weather sensors, navigation as well as wireless networking systems. Several European countries, such as Germany, France, Italy and United Kingdom have launched a joint program with the GaN Research Organization to develop advanced GaN-based components such as broadband high power amplifiers (HPA), radio communicators used in battlefields, satellite link systems, radars as well as receiver/transmitter systems. Applications which require higher frequencies, ranging from 2 GHz to 40 GHz, can be easily achieved using GaN. Figure 1.4 below illustrates the various applications of GaN devices.



Fig 1.4: State-of-the-art GaN based devices for high power, high temperature, high frequency, optoelectronics and military/space applications.

1.2 Motivation

In order to realize in the implementation of GaN-based devices on the Si platform and to enhance the overall performance of the AlGaN/GaN HEMTs, there are several main challenges which need to be addressed as follows:

i. Availability of Good Quality and Cost-Effective Non-native Substrates

Due to the current unavailability of good quality single crystal bulk GaN substrates, AlGaN/GaN heterostructures are grown on non-native substrates such as sapphire and silicon carbide (SiC). However owing to the expensive cost of fabrication, the semiconductor industry is looking into the possibility of integrating GaN with the Si technology, which is primarily motivated by the low cost of Si and the mature back end Si CMOS processing line. Although the approach of implementing GaN-based devices on Si technology is able to offer a much lower manufacturing cost, GaN on Si substrates suffer from high threading dislocations, cracking and bowing issues which are attributed to the large lattice and thermal expansion mismatch between Si and GaN. Intensive R&D has been done with a focus on growing high quality crack-free GaN on the bulk Si [25] and thin silicon-on-insulator (SOI) substrates [26-28]. Both types of substrates have their advantages and disadvantages which prevail over one another. Therefore, it is essential to compare and study the properties of both bulk Si and SOI substrates. Both composite substrates will be evaluated in terms of their respective bowing and electrical properties, the structural and crystalline growth quality, and finally, the HEMT devices' performance and channel temperature profile.

ii. Development of Enhancement mode AlGaN/GaN HEMTs

AlGaN/GaN HEMT is normally-on (depletion mode) in nature due to the existing 2DEG channel which is induced by the strong polarization effect of GaN. A typical -4 V threshold voltage is needed to turn off the device. A normally-off (enhancement mode) device is desirable as it allows the elimination of negative power supply usage. This reduces the overall circuit design and system architecture complexity in terms of size and cost. In addition, an enhancement mode type of AlGaN/GaN HEMT inherently has better fail-safe operation coupled with lower power consumption. Several approaches of fabricating enhancement mode AlGaN/GaN HEMTs, such as gate recess etching, fluorine plasma treatment, and thinning of AlGaN barrier, are reported [29-32]. Nonetheless, a standard processing method with good uniformity and repeatability is still lacking. Therefore, it is of our interest to study the effect of Germanium doping at the gate region of the AlGaN/GaN HEMT in order to shift the threshold voltage. Germanium, which acts as an n-type donor in the AlGaN barrier layer, is proposed to be able to compensate the effects of positive sheet charges at the heterointerface, which eventually depletes the 2DEG channel leading to a positive shift in the threshold voltage. The efficiency and feasibility of this approach in achieving an enhancement mode of operation are studied.

iii. Development of Au-free Metallization Scheme for AlGaN/GaN HEMT

Conventional AlGaN/GaN HEMTs are fabricated using Au-based contacts; Ti/Al/Ni/Au (source/drain) and Ni/Au (Gate). However, Au is

prohibited in the CMOS foundry due to the contamination risks of Au which introduce deep level traps in Si [33]. In addition, Au-based contacts require very high annealing temperature (>800 °C) to form Ohmic contacts. At such high temperatures, these contacts exhibit rough surface morphology due to the formation of the AlAu_4 alloy phase and Ni-Al agglomeration [34, 35]. Rough surface contacts are not desirable for high frequency microwave applications due to the non-uniform current distribution and poor line edge definition. Furthermore, contacts annealed at high temperatures are likely to have lateral overflow problems, which can result in gate to source/drain shorts. Therefore, it is essential to develop a process with lower temperature for the gold-free metallization scheme, with smooth surface morphology for AlGaN/GaN HEMT fabrication. We believe that this metal scheme will provide an interesting alternative towards a lower thermal budget in HEMT fabrication, and as a result, will encourage the implementation of the gate first process.

iv. Development of Self-aligned AlGaN/GaN MISHEMT Fabrication Process using Au-free Contacts

AlGaN/GaN HEMT with the Schottky metal gate structure typically suffers from high gate leakage current due to the lower barrier height and high metal-induced interfacial trap density [36]. High gate leakage limits the gate voltage swing, which reduces the maximum channel current [37]. Moreover, this reduces the gate-to-drain breakdown voltage, and this can result in further reliability concerns [38]. In order to overcome this issue, a metal-insulator-semiconductor (MIS) structure is used to fabricate the AlGaN/GaN MISHEMT. With the addition of an insulation layer, the gate leakage can be suppressed,

coupled by the passivation of surface-induced traps. Several gate insulators have been explored such as HfO_2 , Al_2O_3 , ZrO_2 , SiO_2 , Si_3N_4 and Ga_2O_3 . Due to the excellent material properties of Al_2O_3 , with its large band gap ($E_g \sim 7.0$ eV), high dielectric constant ($\epsilon \sim 9.0$) and high breakdown field (10 MV/cm) [39], it is used as a gate insulator in this study.

Another performance limiting factor of AlGaN/GaN HEMT devices is the access resistance caused by the gate to source/drain spacing. High access resistance affects the transconductance as well as the gain cutoff frequency performance [40]. The minimum spacing between the source/drain and gate is restricted by the photolithography tool's capability. Controllability of the source-access resistance would then become a major challenge for highly-scaled devices due to alignment issues. Therefore, a self-aligned gate first method is preferred in order to minimize the source/drain-to-gate distance with improved design flexibility. However, the implementation of the gate-first approach is hindered by the high thermal budget Ohmic contact formation in conventional HEMT fabrication. Therefore in this study, we integrated a low temperature process for the Au-free metal stack and demonstrated an innovative approach in fabricating AlGaN/GaN MISHEMTs using common metal stack and single mask for source/drain/gate patterning.

1.3 Objectives

The overall aim of this dissertation is to fabricate and study the characterization of AlGaN/GaN Heterostructure devices on silicon-based substrates. This report will be focusing on 4 major objectives; (i) to study and compare the performance of AlGaN/GaN HEMTs on both Si and thin SOI

substrates using standard gold base contacts, (ii) to investigate the effects of n-type Ge dopant diffusion for enhancement mode device operation, (iii) development of a gold-free low temperature Ohmic contact on the AlGa_N/Ga_N HEMT and (iv) integration of a common metal stack and single mask for Source/Drain/Gate patterning to fabricate AlGa_N/Ga_N MISHEMTs.

The detailed scopes and objectives of this dissertation are as follows:

1. To fabricate conventional Au-based AlGa_N/Ga_N HEMT heterostructures grown on both Ga_N on Si and Ga_N on SOI substrates.
2. To study and compare the structural quality and electrical properties of the AlGa_N/Ga_N epilayers grown on both bulk Si and thin SOI substrates using scanning transmission electron microscope (STEM), high resolution x-ray diffraction (HRXRD), and micro-photoluminescence (PL) spectroscopy.
3. To study the DC electrical performance of AlGa_N/Ga_N HEMT devices grown on both bulk Si and SOI substrates.
4. To study the channel thermal behavior of the HEMT devices in on-state operation on both bulk Si and SOI substrates using the micro-Raman analysis.
5. To investigate the effects of Germanium diffusion in the gate, and on the threshold voltage shift in AlGa_N/Ga_N HEMT fabricated on SOI substrates.
6. To study the effects of annealing temperature on Germanium diffusion and its impact on the threshold voltage and gate current of the AlGa_N/Ga_N HEMTs.

7. To develop and characterize a low temperature Au-free Ohmic metal stack using Ti/Al/NiV contacts.
8. To fabricate and characterize the AlGaN/GaN HEMTs using the developed Ti/Al/NiV contacts.
9. To develop, fabricate and characterize a self-aligned AlGaN/GaN MISHEMT using a novel single mask approach with a common metal stack of Ti/Al/NiV for Source/Drain/Gate patterning.
10. To study the interface trap characteristics of the self-aligned single mask AlGaN/GaN MISHEMT using AC conductance C-V analysis

1.4 Organization of the Report

This thesis is divided into **eight** chapters, organized as follows:

- **Chapter 1** introduces the background of Gallium Nitride and highlights the motivation and objectives of this research.
- **Chapter 2** provides a literature review on the material properties of Gallium Nitride, the fundamentals and operating principles of AlGaN/GaN HEMT, including the origins of the 2DEG channel.
- **Chapter 3** describes the process flow of fabricating AlGaN/GaN HEMT using Au-based contacts as well as several characterization methods used to study and investigate the performance of the fabricated devices.
- **Chapter 4** presents a study and comparison of AlGaN/GaN epilayers grown on both silicon-on-insulator (SOI) and bulk-Si substrates. The electrical properties and film quality of both substrates are investigated. The DC characterization as well as the channel temperature profile of the

AlGa_N/Ga_N HEMTs fabricated on both composite substrates are also analyzed.

- **Chapter 5** presents a study on the effect of Germanium diffusion at the gate region of AlGa_N/Ga_N HEMT with regards to the threshold voltage control. C-V, AFM, SIMS and electrical analysis are used to study the effect of Germanium doping. The impact of annealing temperature on Germanium diffusion and the threshold voltage shift is highlighted.
- **Chapter 6** presents an innovative approach in developing and optimizing a low temperature Au-free AlGa_N/Ga_N HEMT using Ti/Al/NiV as Ohmic contacts. The metal distribution and structural changes of the Ti/Al/NiV contacts after annealing are investigated using STEM-EDX and AFM analyses. The electrical performance and C-V analysis of the Au-free AlGa_N/Ga_N HEMTs are evaluated.
- **Chapter 7** presents an innovative method in fabricating a self-aligned AlGa_N/Ga_N MISHEMT using single mask for Source/Drain/Gate with a common metal stack (Ti/Al/NiV). The DC electrical characteristics of the MISHEMTs are studied. In addition, the interface traps attributed to the AlGa_N/Ga_N and oxide/AlGa_N interfaces are analyzed using the AC conductance C-V method.
- **Chapter 8** finally presents the main contributions of this thesis as well as recommendations for future research work.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

In chapter 1, the history and development of Gallium Nitride based materials together with their potential applications are discussed. Several main challenges of the current AlGa_N/Ga_N HEMT development are also addressed which led to the motivation and objectives of this thesis. In this chapter, the material properties of Gallium Nitride as compared to other semiconductor materials will be reviewed. In addition, the device structure and operating principle of the AlGa_N/Ga_N High Electron Mobility Transistor (HEMT) will be discussed. Finally, the origins of the two-dimensional-electron-gas (2DEG) channel in the AlGa_N/Ga_N heterostructure will be reviewed.

2.2 Gallium Nitride Material System

2.2.1 Crystal Structure of Gallium Nitride

The lattice structure of Ga_N has led to the unique polarization effect of the III-nitride compound system. This hugely contributes to the formation of the 2DEG channel which has high carrier mobility and high charge sheet density as different lattice structure affects the band gap of the material. The 2DEG channel can be formed by growing two different band gap materials epitaxially on top of each other. The physics behind the 2DEG formation will be discussed at the latter part in Section 2.3.2.

Generally, Group III-nitrides such as AlN, InN, and GaN have three different crystal structures namely; wurtzite, zinc-blende and rock-salt. At ambient environment, the wurtzite structure is the more thermodynamically favorable phase. Zinc-blended structure of GaN and InN is formed by growing epitaxial thin films on [011] crystal plane substrate such as GaAs, Si and MgO. The rock-salt structure is formed only under very high pressure conditions. Thus, GaN can be generally categorized into the two more common structures; the wurtzite and the zinc-blende, as shown in Fig 2.1.

Wurtzite, Fig 2.1(b) is of hexagonal unit cell with two lattice constants, c and a . The lattice c/a ratio is $5.188/3.189 = 1.627$. It is formed by two interpenetrating hexagonal closed packed lattices offset along the c axis by $5/8$ of the cell height. It is closely related to the hexagonal diamond structure with a band gap of 3.4 eV. Each GaN atom is bonded to four nitrogen atoms. As for zinc-blende structure, as shown in Fig 2.1(a), it consists of four Group III elements and four nitrogen elements. It can be seen as two interpenetrating face-centered cubic (FCC) lattices offset by $1/4$ of the distance along a body diagonal. The c/a lattice constants ratio is $5.188/4.52 = 1.148$. The atoms position is similar to the diamond structure with band gap energy of 3.2 eV.

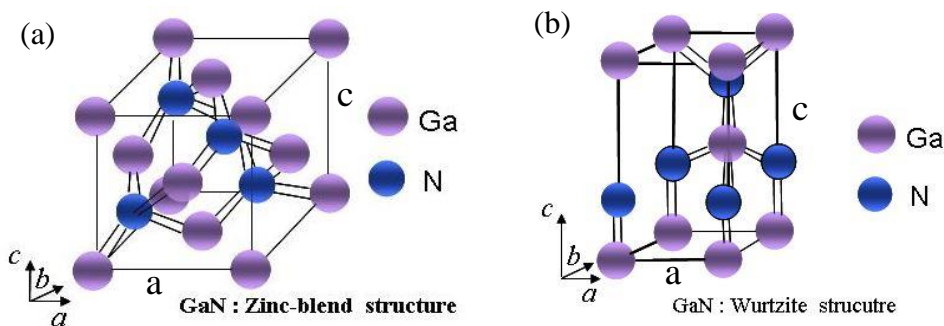


Fig 2.1: GaN Crystal Structure: (a) Zinc Blende (b) Wurtzite [41].

GaN are of tetrahedral bonds with sp^3 hybridization which each atom is tetrahedrally bonded to four atoms of different types. The bonding angle is 109.47° with bond length of 19.5 nm. GaN exhibits a mixture of ionic and covalent bonding. However, GaN is predominantly covalent with a significant contribution of ionic bonding to the structure due to the large difference in electronegativity between Gallium and Nitrogen. Generally, wurtzite and zinc-blende crystal structures will exhibit different types of material properties. One of the most important property exhibited by the wurtzite structure is the polarization effect which will be discussed later. This polarization effect is responsible towards the formation of the 2DEG channel of the AlGaIn/GaN heterostructure device.

2.2.2 Band gap of Gallium Nitride

Different crystal lattice and bonding properties constitute to different band gap energy. Compared to Silicon which has indirect band gap, GaN has direct and wide band gap making them suitable for light emitting devices applications. Direct band gap allows the recombination of holes and electrons at the forbidden band gap, emitting light as photon. Silicon doesn't has such optical emission properties because its band gap is indirect and the recombination takes place through non-radiative transition. Fig 2.2 shows the band structure of zinc-blende and wurtzite GaN as compared to Silicon. Fig 2.3 shows the energy band gap comparison of GaN with several other important semiconductor materials (including Si and GaAs) with respect to their lattice

constant. It can be seen that GaN has a direct band gap of 3.4 eV larger than Si (1.12 eV) and GaAs (3.26 eV).

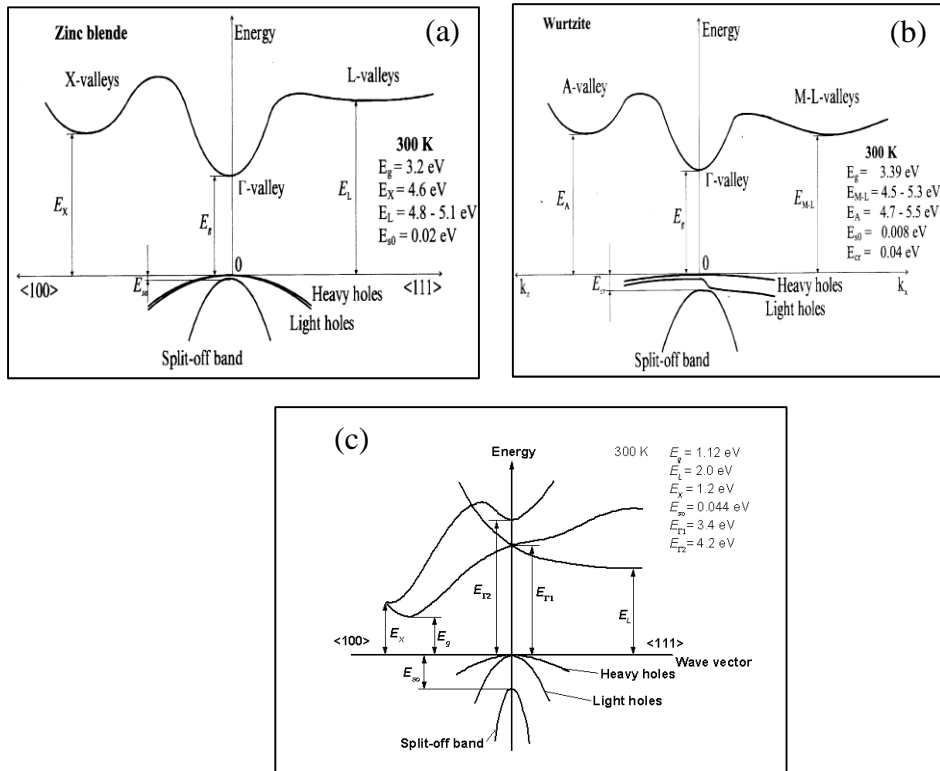


Fig 2.2: (a) Zinc Blende GaN Band structure (b) Wurtzite GaN Band Structure and (c) Silicon Band structure [42, 43].

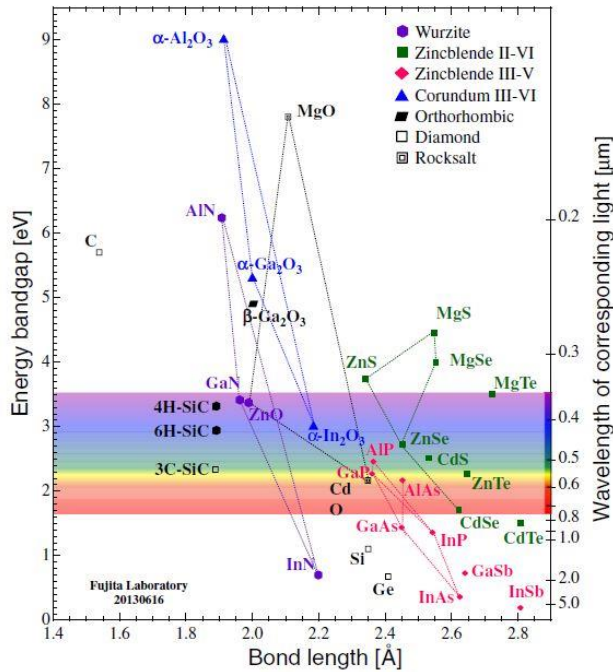


Fig 2.3: Bandgap energy of wurzite (α -GaN) with several important elemental semiconductor while the right-side scale indicates the wavelength corresponding to the band gap energy [44].

2.2.3 Material Properties of Gallium Nitride

As time progresses, the newer generation of devices demand higher performance material to meet the higher power, temperature, and operating frequency applications which Silicon is unable to fulfill. Therefore, industries have start to explore the possibilities of using wide band gap semiconductor such III-Nitride and SiC. In this section, the superior electrical and physical properties of Gallium Nitride as compared to other materials will be discussed. The material properties of GaN in comparison with Si and other wide band gap materials are shown in Table 2.1 below.

Material Property	Si	SiC	Diamond	GaN AlGaN/GaN	GaAs AlGaAs/ InGaAs	InP InAlAs/ InGaAs
Bandgap energy, E_g (eV)	1.12	3.26	5.45	3.44	1.43	1.35
Electron mobility, μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	1500	700	4800	1500-2000**	8500-10000**	5400-10000**
Saturated velocity electrons, v_{sat} ($\times 10^7$ cm/s)	1.0	2.0	2.7	2.5	1.0	1.0
Electric breakdown field, E_c (MV/cm)	0.3	3	10	3	0.4	0.5
2DEG density, n_s ($\times 10^{13}$ cm^{-2})	N.A.	N.A.	N.A.	1.0	< 0.2	< 0.2
Thermal conductivity, κ (W/cm·K)	1.5	3.7-4.5	22	2.1-2.3	0.5	0.7

N.A. refers to not available

** refers to the 2DEG channel velocity of the heterostructure

Table 2.1: Material Properties of GaN in comparison to Si and other wide bandgap semiconductors [45, 46].

A wide band gap is essential for applications which require a high voltage supply as it contributes to a higher electric field breakdown. From the Table 2.1, it is clear that GaN has a larger band gap of 3.4 eV compared to that of Silicon. A high electric field breakdown of the electronic devices is desirable to sustain a high power supply in applications such as automotive and power generators. GaN has an electric breakdown field ~10 times higher compared to that of Si. Additionally, the direct wide band gap property of GaN is suitable for optoelectronic applications (Blue and White Light Emitting Diodes (LEDs)) as well as data storage applications (Blue ray discs).

For high frequency and high drain current applications, carriers with high mobility, density, and saturation velocity are essential. The 2DEG channel formed due to the AlGaIn/GaN hetero-junction structure exhibits a channel mobility of 1500-2000 cm²/V·s and saturation velocity of 2.5×10^7 cm/s which further supports the superiority of GaN as compared to Si [46].

The thermal conductivity of a material defines its capability to dissipate heat. Effective heat dissipation is important to prevent performance degradation of a device at elevated operating temperatures. From Table 2.1, GaN has an average thermal conductivity of 2.3 W/cmK which is higher than Si with 1.5 W/cmK. Conversely, GaAs has the poorest thermal conductivity with only 0.5 W/cmK.

The excellent electron mobility of the GaAs/AlGaAs material system has opened up possibilities for it to explore applications with higher power and frequency. However, GaAs-based devices have drawbacks which include low thermal conductivity and high substrate cost. Similarly, although silicon carbide (SiC) is another promising material for high power and temperature

applications due to its good thermal conductivity and large band gap characteristics, it is inferior to GaN in terms of its lower carrier mobility and higher manufacturing costs. Furthermore, the mass production of GaN-based devices can be achieved at a substantially lower cost, as industries start to incorporate GaN into mature silicon platforms, as discussed earlier. Among other materials, diamond, with a much larger band gap energy (5.45 eV) and a thermal conductivity which is ~4 times higher compared to SiC, might seem like a compound with the best material properties. Unfortunately, in addition to the extremely high cost of diamond, the overall material quality of diamond is poor and its superior carrier performance is subject to dopant activation at high temperatures (500 K) [47]. Thus, diamond is not expected to be a serious competitor to GaN and SiC devices in the near future. Therefore, GaN-based devices are the most favorable and cost-effective candidate to fulfill the demands of applications which require higher power, temperature and frequency.

2.3 Fundamentals of AlGaN/GaN High Electron Mobility Transistors (HEMT)

Among all the applications mentioned earlier, High Electron Mobility Transistors (HEMT) is one of the most important GaN-based devices of particular interest in the high voltage and high frequency industries. HEMT is also known as Modulation Doped Field Effect Transistors (MODFET), Two Dimensional Electron Gas Field Effect Transistors (TEGFET) and Heterostructure Insulated Gate Field Effect Transistors (HIGFET). The first generation of HEMT devices was published in 1980 which is based on the

AlGaAs/GaAs heterostructure [48]. Other semiconductor alloys which are being researched as well are InGaAs/GaAs and InP-based InAlAs/InGaAs heterostructures.

However, since 1990s AlGaN/GaN based HEMT devices have attracted a lot of interest due to the overall better performance of GaN compared to GaAs and other semiconductor materials. In 1991, M.A. Khan successfully demonstrated the first AlGaN/GaN HEMT device using low pressure metal organic chemical vapor deposition (MOCVD) method [17]. Based on the excellent material properties discussed earlier, AlGaN/GaN HEMT has become a promising candidate for next generation of high power, temperature and frequency applications.

2.3.1 AlGaN/GaN HEMT device structure and operating principles

Below is the schematic of the typical Au-based AlGaN/GaN HEMT device structure. Similar to MOSFET, HEMT is basically a three terminal device comprises of a source, drain and gate. The Source/Drain Ohmic contacts are formed by Ti/Al/Ni/Au metal stack while Ni/Au is used as the Schottky gate electrode. The 2DEG channel is formed at the AlGaN/GaN interface layer. Typically, an AlN buffer layer grown on top of the Si substrate is essential to ensure good quality growth of the subsequent GaN buffer layers due to the lower lattice mismatch between AlN and Silicon.

The AlGaN/GaN HEMT structures make use of the two different band gap materials of AlGaN and GaN to form the active layers where the 2DEG channel is formed. The AlGaN layer has higher conduction band energy level

than the conduction band of the GaN layer. Due to the discontinuity and conduction band offset between the AlGaN and GaN layer, a triangular quantum well is formed at the hetero-interface between AlGaN and GaN layer as shown in Fig 2.5. Due to the large conduction band offset and high polarization effect, high density 2DEG is confined within this quantum well forming the channel. This 2DEG channel is modulated by the gate bias to control the turn-on and turn-off of the HEMT device.

Due to this triangular quantum well, the electrons are confined and separated from the positively charged donors by the potential barrier. Therefore, the electrons are free from impurity scattering and thus have very high mobility. In addition, the trapped electrons transport in a 2-dimensional (x and y-direction) manner which contributes to the high channel mobility of the HEMT devices. This 2DEG channel offers high electron mobility about $1500\text{-}2000\text{ cm}^2/\text{V}\cdot\text{s}$ and high electron density of $1\times 10^{13}\text{ cm}^{-2}$ even without modulation doping making GaN far more capable than Silicon in terms of speed and performance.

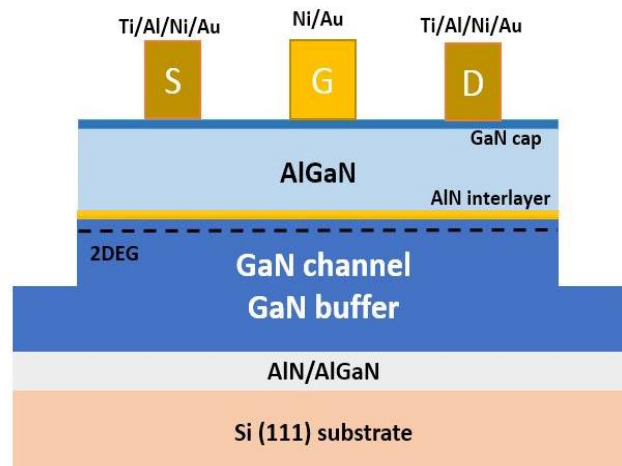


Fig 2.4: AlGaN/GaN HEMT (Gold-based) device structure cross-section overview.

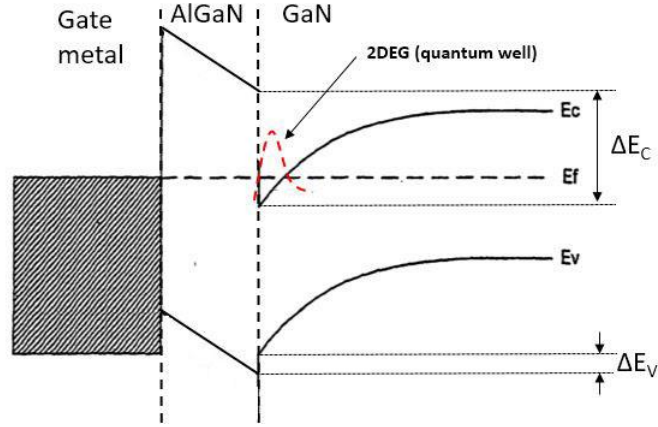


Fig 2.5: Band Diagram of the AlGaN/GaN heterostructure [49]; ΔE_C denotes the conduction band offset between AlGaN and GaN, ΔE_V denotes the valence band offset between AlGaN and GaN.

Due to existence of the 2DEG channel, AlGaN/GaN HEMT is typically a normally on or depletion mode device by nature with a negative threshold voltage, V_{TH} . Negative voltage supply requires a more complicated circuit and hence increases the circuit design cost. Therefore, there is a need of developing normally off or enhancement mode AlGaN/GaN HEMT which is also one of the motivation in this report. Typically V_{TH} of GaN HEMT is about -4 V [30] and a negative bias is needed to put the device into OFF-state.

At thermal equilibrium state and gate bias $V_G = 0$ V (on-state), the current is free to flow across the channel without any external bias due to the 2DEG accumulation at the hetero-interface as shown in Fig 2.6 (a). As the gate bias increases, more carriers are accumulated at the 2DEG channel heterointerface leading to higher sheet carrier density. When a negative bias is applied at the gate, the depletion region starts to shift the conduction band of the AlGaN/GaN interface above the Fermi level (Fig 2.6 (b)). Hence, the electrons in the 2DEG channel starts to deplete reducing the channel electron concentration. Eventually when $V_G < V_{TH}$, the electrons are all depleted and the channel is pinched-off (off-state).

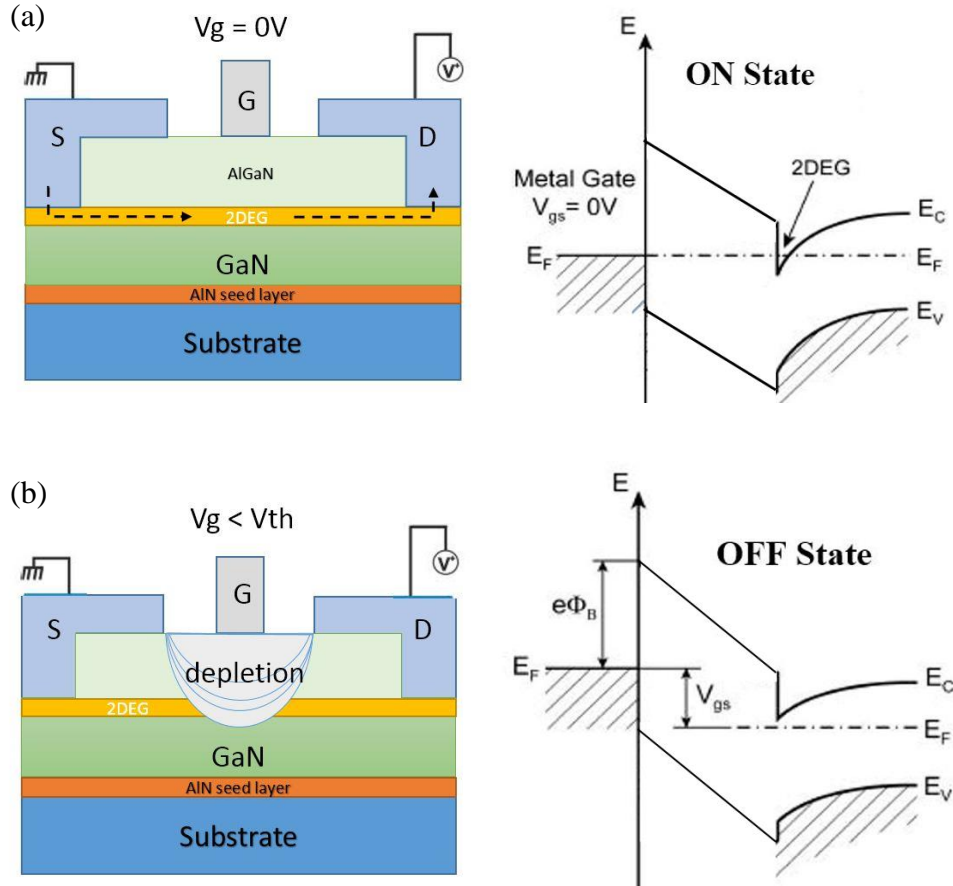


Fig 2.6: Thermal Equilibrium Band diagram and Schematic illustration of AlGaIn/GaN HEMT under the influence of gate bias (a) on state ($V_G = 0 \text{ V}$) and (b) off state ($V_g < V_{th}$) [50].

2.3.2 Formation of the 2DEG Channel due to Polarization Effect

In this section, formation of the 2DEG channel due to the lattice crystal structure of wurzite GaN is reviewed. Regardless of many debates, researchers believed that the formation of the 2DEG channel in the AlGaIn/GaN structure is due to the strong polarization effect [51]. For conventional AlGaAs/GaAs HEMT structures, the 2DEG channel originated from the modulation doping of the AlGaAs layer with donor ions which are separated from the electrons in the quantum well by the AlGaAs spacer. However for AlGaIn/GaN system, a significant $\sim 10^{13} \text{ cm}^{-2}$ sheet charge density is observed even without any doping

in the AlGaN layer. Ambacher *et al.*, suggested that the 2DEG formation is due to the strong polarization effect contributed by both spontaneous and piezoelectric polarizations [52].

I. Spontaneous Polarization (P_{SP})

Spontaneous Polarization is defined as the built-in polarization field in an unstrained crystal or zero strain. Spontaneous polarization is dominant in wurtzite structure of group III-nitrides. Group III-nitride compounds are indifferent in term of properties mainly due to the presence of the nitrogen element; the smallest and most electronegative element in Group V. Due to the lack of electrons in the outer orbit of nitrogen, electrons will be strongly attracted by the Coulomb potential of nitrogen atom resulting in a very strong ionicity metal-nitrogen covalent bond. Such ionicity which is now microscopic polarization will enhanced into macroscopic polarization if there is lack of symmetry in the crystal. Therefore, as the wurtzite III-nitride structures doesn't have inversion symmetry in the [0001] direction as shown in Fig 2.7, the crystal is distorted in nature resulting in a macroscopic polarization field along with the strong ionicity of the nitrogen atom. Since the polarization takes place in the lattice at zero strain, it is therefore called as spontaneous polarization (P_{SP}). P_{SP} is dependent on the Al mole fraction, x by the following expression:

$$P_{SP} = (-0.052x - 0.029) C/m^2 \quad (2-1)$$

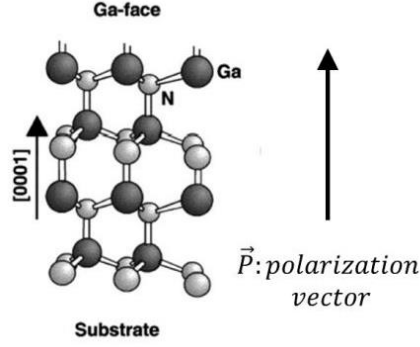


Fig 2.7: Atomic arrangement of Ga-faced GaN crystals [51].

II. Piezoelectric Polarization (P_{PE})

Polarization of a crystal will be affected when the ideality of the lattice is changed. One way to distort the crystal lattice is through the application of strain. Therefore, such strain-induced polarization effect is called the piezoelectric polarization (P_{PE}). The piezoelectric polarization is expressed as follow:

$$P_{PE} = e_{33} \cdot \varepsilon_z + e_{31} \cdot (\varepsilon_x + \varepsilon_y) \quad (2-2)$$

where $\varepsilon_z = \frac{c - c_0}{c_0}$ is the strain along the c axis, the in plane strain

$\varepsilon_x = \varepsilon_y = \frac{a - a_0}{a_0}$ is assumed to be isotropic, where a and c are the lattice

constants of the strained layer, e_{31} and e_{31} are piezoelectric coefficients respectively. The strains in the lattice are related by:

$$\varepsilon_z = -2 \cdot \frac{C_{13}}{C_{33}} \cdot \varepsilon_x \quad (2-3)$$

Where C_{13} and C_{33} are elastic deformation constants. Therefore, combining both equation (2) and (3) will get the final expression for P_{PE} as follows:

$$P_{PE} = 2 \cdot \frac{a - a_0}{a_0} \cdot \left(e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right) \quad (2-4)$$

Wurtzite	AlN	GaN	InN
P_{SP} (C/m ²)	-0.081	-0.029	-0.032
e_{33} (C/m ²)	1.46	0.73	0.97
e_{31} (C/m ²)	-0.60	-0.49	-0.57
C_{13} (GPa)	108	103	92
C_{33} (GPa)	373	405	224
a_0 (Å)	3.112	3.189	3.54
c_0 (Å)	4.982	5.185	5.705

Table 2.2: Lattice constant parameters for polarization calculation for different wurtzite III-nitrides at 300 K [51].

Due the smaller lattice constant as compared to GaN, without any strain relaxation, AlGa_xN will be under tensile when grown on top of GaN creating an additional piezoelectric polarization field as shown in Fig 2.8 (b). GaN is generally assumed to be in relaxation state due to the nature of thick GaN layer (few micrometers). Therefore, apart from the spontaneous polarization, an additional piezoelectric polarization is formed due to the strain developed in AlGa_xN layers. When AlGa_xN is epi-grown on the GaN substrates, a net polarization charge, σ is developed at the interface due to the difference in polarization as shown in Fig 2.9.

The amount of polarization charge density at the AlGa_xN/GaN heterointerface due to the polarization difference between AlGa_xN and GaN can thus expressed as:

$$|\sigma(x)| = |P_{SP}(AlGaN) + P_{PE}(AlGaN) - P_{SP}(GaN)| \quad (2-5)$$

Due to the positive polarization at the AlGa_xN/GaN interface, free electrons form the 2DEG channel at the interface in order to compensate those positive charges. The 2DEG electron density, n_s at the channel can be estimated with the following equation [51]:

$$n_s(x) = \frac{+\sigma(x)}{q} - \left[\frac{\epsilon_0 \epsilon_r(x)}{t_0 q^2} \right] (q\phi_b(x) + E_F(x) - \Delta E_C(x)) \quad (2-6)$$

where t_0 is the AlGa_xN layer thickness, ϵ_r is the dielectric constant for the AlGa_xN barrier layer, q is the electric charge, ϕ_b representing the Schottky barrier height and E_F is the GaN Fermi energy level with respect to the conduction band, E_C is the conduction band offset at the AlGa_xN/GaN interface. Generally, the 2DEG channel give rise to high electron density about of 1×10^{13} cm⁻² with mobility up to 1500-2000 cm²/V·s as shown in the Table 2.1.

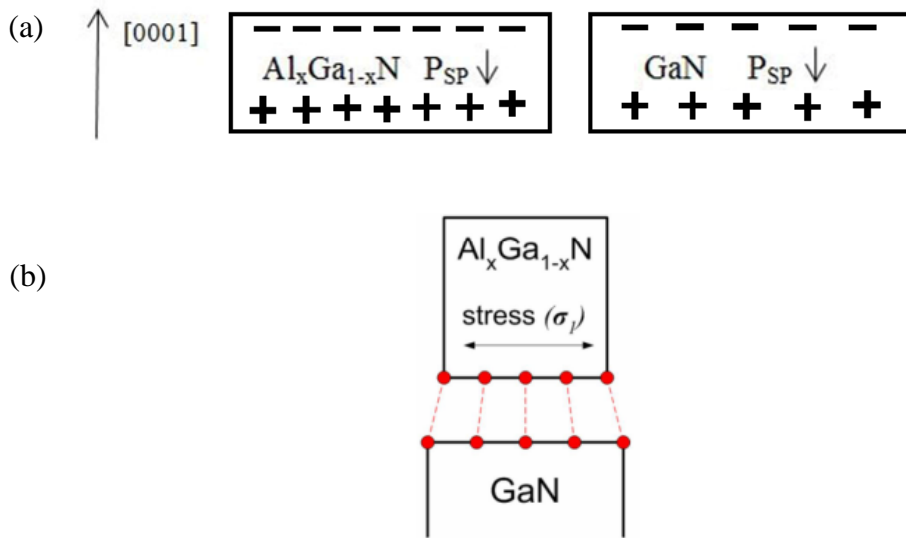


Fig 2.8: (a) Electric field and sheet charge due to spontaneous polarization in AlGa_xN and GaN crystals respectively on the c-plane (b) AlGa_xN layer is under tensile stress when grown on top of comparatively thicker GaN substrate.

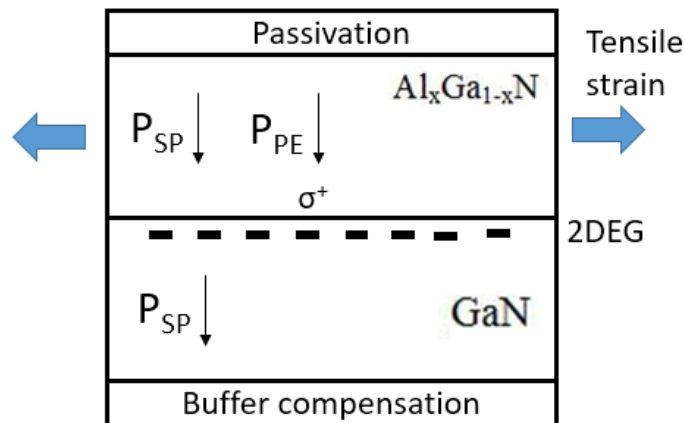


Fig 2.9: Net charges induced taking account of both Spontaneous and Piezoelectric Polarization [53].

CHAPTER 3: FABRICATION PROCESS & CHARACTERIZATION METHODS FOR ALGAN/GAN HEMTS

3.1 Introduction

In Chapter 3, the process flow of the AlGaN/GaN HEMT fabrication using Au-based contacts is reviewed. All the process steps are developed and optimized using the cleanroom facilities at both the Institute of Material Research and Engineering (IMRE) and Nanyang Technological University (NTU). The HEMT devices are fabricated using a planar process on diced-samples from growth-ready GaN on Bulk-Si and silicon-on-insulator (SOI) wafers (6 to 8" in diameter). Apart from the process flow, several important characterization methods used to evaluate the electrical performance of the fabricated device are reviewed. All the electrical and capacitance-voltage measurements are conducted in the Semiconductor Characterization 2 (SC2) Lab at NTU using a Keithley 4200-SCS Parameter Analyzer.

3.2 Key Process Flow for AlGaN/GaN HEMT Fabrication

Fig 3.1 illustrates the main process flow of fabricating the normally off/depletion mode AlGaN/GaN HEMTs using Au-based contacts. In general, the main process flow consists of sample cleaning and preparation, mesa isolation etching, Source/Drain Ohmic contact formation and a final Schottky gate formation.

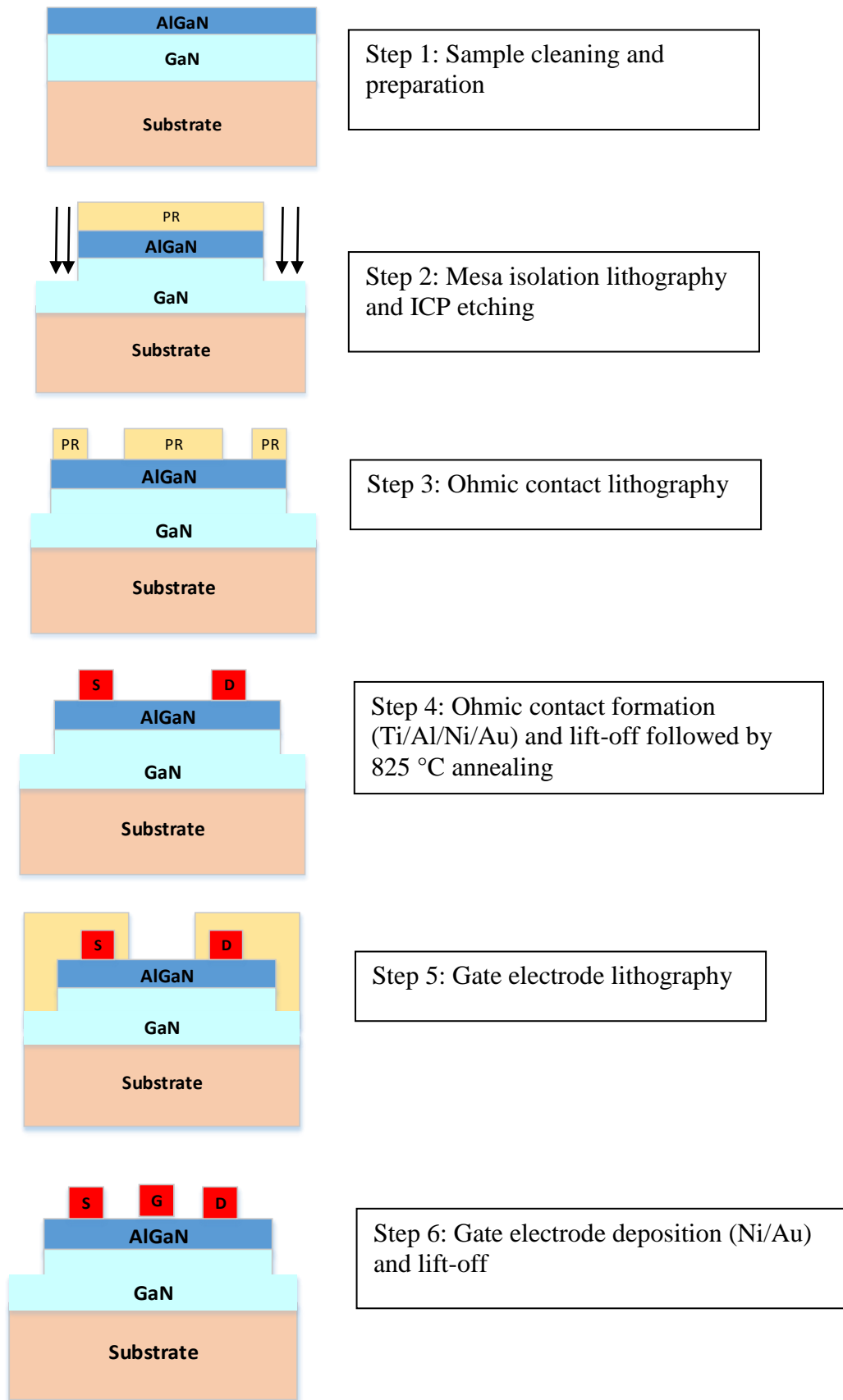


Fig 3.1: Schematic illustration of AlGaN/GaN HEMT fabrication main process steps using Au-based contacts.

3.2.1 Sample Preparation (AMI Cleaning & Spin coating)

From the epi-grown wafers, samples are diced into 1 cm x 1 cm size before being processed. The diced samples firstly go through a standard AMI (abbreviation for Acetone, Methanol and Iso-propanol (IPA)) cleaning process. This step generally removes any photoresists, particles and organic contaminants on the substrate's surface. The samples are immersed inside each solvent for 5-10 mins in an ultra-sonic cleaner. Next, the samples are rinsed with de-ionized water (DIW) before being dipped inside a pure 97% hydrochloric (HCl) acid solution for 1 minute to remove any residual native oxide. A final DIW rinse step is carried out to remove any remaining organic and acid solvents on the samples. The cleaned samples then undergo a dehydration bake using a hot plate set at a temperature of 120 °C for 5 mins to remove any moisture residue. A spin coating process is then carried out prior to the photolithography step. The samples are coated with AZ7217 positive photoresist. A positive resist denotes that any portion of the resist which is exposed to UV light during the photolithography step will become soluble and will be removed by the photoresist developer. An optimized spin-coating recipe of 5000 rpm for 30 s (1500 rpm ramping up) achieved a photoresist thickness of approximately 1.6 μm . After spin-coating, the samples are post-baked at 95 °C or 1 min to improve the resist adhesion and remove any solvent content on the samples' surface.



Fig 3.2: CEE 200x Precision Spin Coater [54].

3.2.2 Mesa Isolation Etching

Mesa isolation is essential to prevent any unwanted leakage from spreading between the adjacent devices. After the samples are spin coated, the active area pattern is defined using the Mask & Bond Aligner, MA8/BA6 (SUSS MicroTec) lithography tool. Using CH1 light source (*i-line 365 nm*) with an intensity of 13 mW/cm^2 , samples are exposed for a duration of 15 seconds. Next, the exposed photoresist-coated samples are developed using the AZ developer diluted with DI water with a 1:1 ratio for 60 s. This is followed by a hard bake at $110 \text{ }^\circ\text{C}$ for 5 minutes to remove any remaining moisture and to increase the etch resistance/thermal stability of the resist mask.

After the active area is defined by photolithography, the mesa isolation etching is carried out using the Inductive Coupled Plasma and Reactive Ion Etching (ICP-RIE) Oxford PlasmaPro100 System. The plasma dry etching using the ICP-RIE system has an advantage of mitigating the plasma damage while maintaining a good etching profile with high etch rates. The ICP-RIE system is also equipped with a chiller which is capable of maintaining the chamber temperature to as low as $6 \text{ }^\circ\text{C}$ during the etching process. Low temperature etching is essential in III-V systems in order to prevent the photoresist from burning. The ICP plasma will generate heat during the etching process which will increase the reaction between the GaN and the photoresist. Such reactions will introduce after-etch polymers, as shown in Fig 3.3 (c). These polymers are very hard to be removed using typical chemical cleaning. The existence of these polymers might lead to future processing issues such as high contact resistance, high leakage current and even device failure. Therefore,

a high temperature post bake coupled with an efficient wafer-cooling system are required to prevent photoresist burning.

The etching recipe is optimized based on a BCl_3/Cl_2 (10/20 sccm) chemistry. The etch chamber is maintained at a pressure of 10 mTorr and a low temperature of 6 °C. The etching process is carried out at an ICP and RF power of 100 W and 200 W respectively. An etch rate of 45 nm/min is achieved. With an etch duration of 8 minutes, a step height of 350-400 nm is achieved. To achieve sufficient isolation characteristics, the devices are etched until the GaN buffer layer. This isolation scheme is important in order to achieve good current leakage and low I_{OFF} performance. After plasma etching, the resist mask is removed using the acetone and IPA solvent followed by DI water rinsing before proceeding to the next process step.

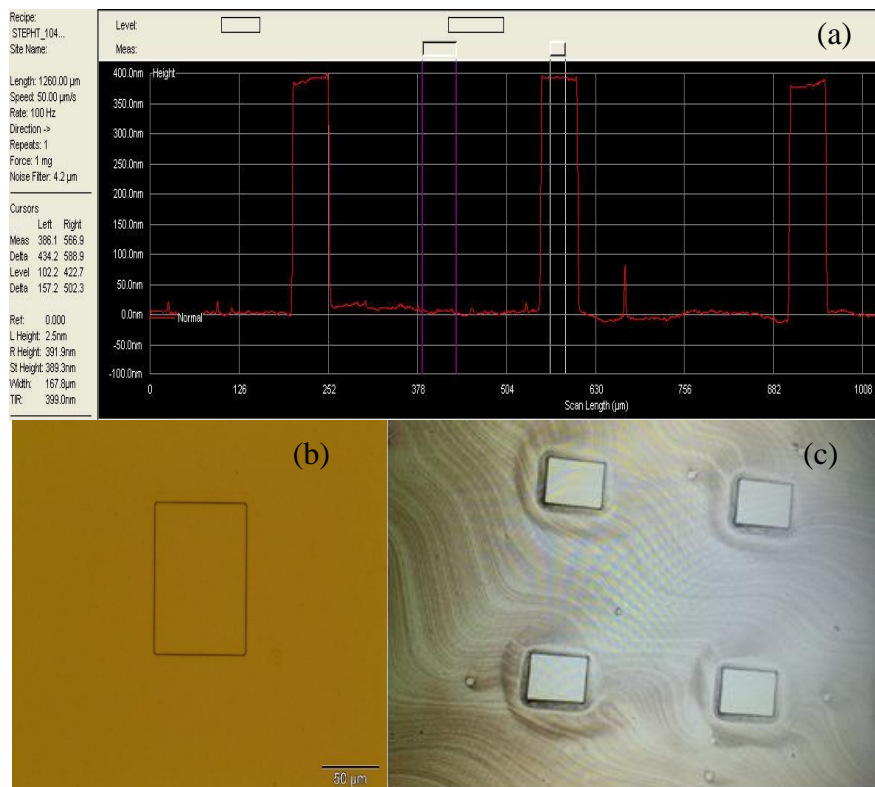


Fig 3.3: (a) Step profiler measurement of the mesa etched island with a step height of 389.3 nm, (b) microscopic image of the Mesa island structure etched using the ICP-RIE dry plasma system and (c) photoresist burning due to elevated temperature after several runs of ICP plasma etching.

3.2.3 Source/Drain Ohmic Contact (Gold-based)

Source/Drain Ohmic contacts with low resistance are very important for AlGaIn/GaN HEMT to obtain fast switching and high drive current performance. The good quality of Ohmic contacts is influenced by the surface morphology, the type of metal, the relative thickness of the metal stack, the pre-metal deposition surface treatment as well as the post metallization annealing treatment.

The source/drain area is patterned using a photolithography recipe similar to the mesa isolation scheme as reviewed earlier. Using the AZ 7217 photoresist, samples are spin-coated at 5000 rpm for 30 s to achieve a resist thickness of approximately 1.6 μm . A short 1 min soft-bake is carried out at 95 °C to harden the resist and to remove any remaining moistures. Using the CH1 light source (*i-line 365 nm*) with an intensity of 13 mW/cm², the resist is exposed for 10-15 seconds. The exposed resist is developed using the AZ developer: H₂O solution with a ratio of 1: 1 for 90 s. Prior to metal deposition, a surface treatment using diluted HCl with H₂O (1:1) for 60 s is recommended to remove any contaminants and native oxide at the source/drain opening. The presence of thin resist or interfacial oxide will lead to subsequent lift-off problem and increase in contact resistance during the post metallization annealing step.

Each metal layer is deposited in a certain order at the patterned areas using the Denton Explorer E-Beam Evaporator System. During deposition, an electrical current is applied to the tungsten filament inside the main chamber which emits an electron beam. The electron beam is bent and directed via a magnetic force onto the crucible which contains the desired deposition metal.

The metal in the crucible is melted and evaporated by the electron beam. The vaporized metal travels in all directions (line of sight) and condenses on the substrate surface mounted on top of the chamber. The quality and uniformity of the deposited layer is ensured by maintaining a high vacuum in the chamber, at a pressure of 5×10^{-7} Torr. After metal deposition, the lift-off process is carried out via sonication in acetone and IPA solvent to remove any unwanted metal. A resist stripper is used to remove any remaining sidewall resists which could not be removed using acetone. Finally, the samples are annealed at 825 °C (30 to 60 s) using the Jet First Rapid Thermal Processing (RTP) System to form the Ohmic contacts.

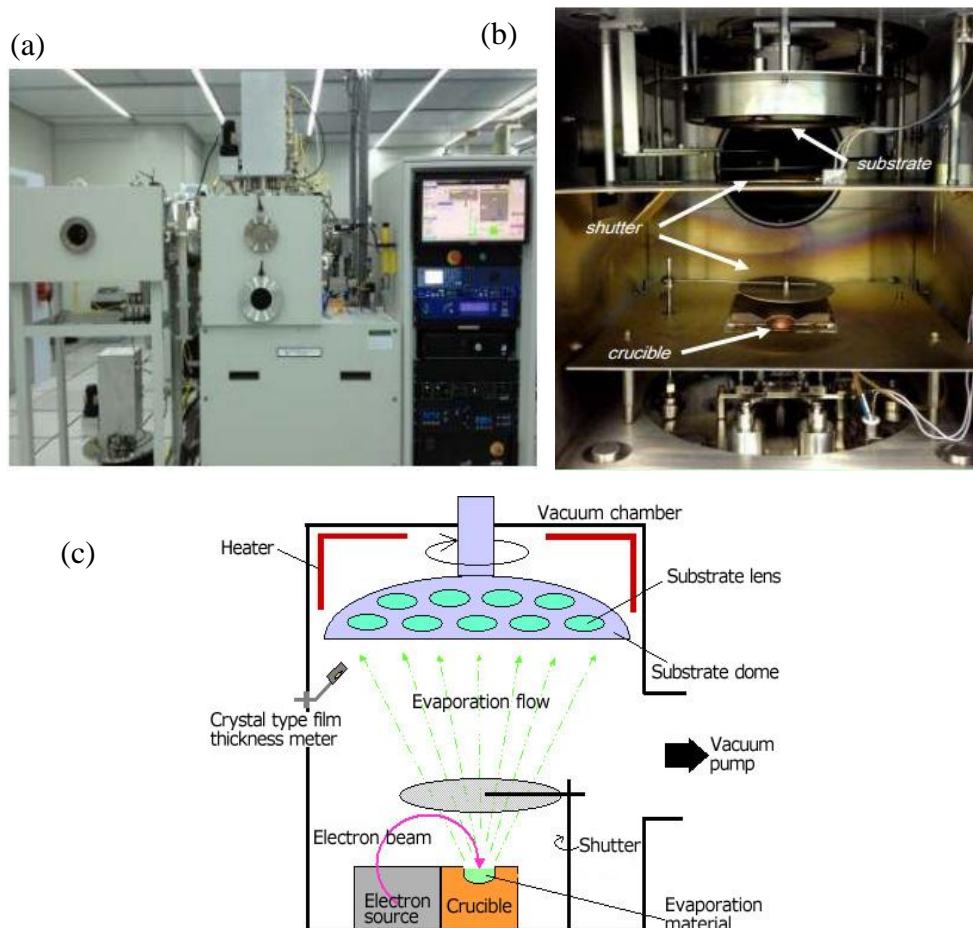


Fig 3.4: (a) Denton Explorer E-Beam Evaporator System (b) the interior of the main chamber of the system and (c) schematic overview of the film deposition process using E-beam evaporation [55].

Mechanism of Ohmic Contact Formation

There are several types of metal which are commonly used in semiconductor processing to form Ohmic contacts. Generally for AlGaIn/GaN HEMT, metals with low work function, low resistivity and comparable thermal expansion coefficient with GaN are used. Equally important, the first metal layer in contact with the AlGaIn layer must have good adhesion in order to prevent the metal from lifting off during the lift-off process. Ti/Al/Ni/Au is the conventional state-of-the-art Au-based multilayer metal scheme used as source/drain contacts for AlGaIn/GaN HEMT. The properties of the Ti/Al/Ni/Au metals are listed below in Table 3.1.

Metal	Work Function (eV)	Resistivity ($10^{-6} \Omega \cdot \text{cm}$)	Thermal Expansion Coefficient (10^{-6} K^{-1})
Ti	4.33	39.00	8.60
Al	4.28	2.42	23.10
Ni	5.15	6.16	13.40
Au	5.10	2.05	14.20

Table 3.1: Work function, resistivity and thermal expansion coefficient properties of the commonly used Ti/Al/Ni/Au metal schemes for the AlGaIn/GaN HEMT system [56].

Ti/Al with an Au-based multilayer metal scheme is a widely adopted choice for source/drain contacts in the fabrication of AlGaIn/GaN HEMTs due to its low contact resistance, with an average value of $1.5 \Omega \cdot \text{mm}$ and below [35, 57]. These metal layers can be easily deposited using the conventional electron beam evaporation system and patterned using a simple acetone lift-off process.

Generally, the low contact resistance of the Ti/Al/Ni/Au metal scheme is attributed to two main current transport mechanisms; (i) carrier tunneling mechanism due to effective barrier height reduction caused by the formation of intermediate TiN layer and (ii) direct conduction path between the metal contact and 2DEG channel due to the inclusion of Ti(Al)N alloy which penetrates through the AlGaN barrier.

The first current transport mechanism is the direct tunneling of carriers due to the reduced effective barrier height. During the high temperature annealing step (800 to 900 °C) via RTP, both Ti and Al from the Al/Ti/GaN contact layers will react with the nitrides in the GaN surface; forming TiN, AlN and AlTi₂N interfacial nitride layers on the surface [58]. Ti will react with GaN at the Ti/GaN interface to form a thin layer of TiN while creating N vacancies at the GaN surface during annealing. These depleted N will form a heavily n-doped GaN surface region underneath the metallization layers. As the thin layer of TiN has a low work function of 3.7 eV, it causes bending in the GaN conduction band which eventually reduces the effective barrier height. As a result, the electrons are able to travel between the Ohmic contacts and the 2DEG channel through tunneling mechanism [59].

The second proposed mechanism is a direct conduction path via metal protrusion which penetrates into the AlGaN/GaN interface. During high temperature annealing, inclusions of Ti(Al)N alloy take place whereby the metal penetrates through the AlGaN barrier layer. M.W. Fay *et al.* proposed that Au plays a vital role in assisting the metal spiking phenomenon [60]. Owing to such contact inclusions, a localized conduction path is formed, allowing electrons to flow freely between the metal contact and 2DEG channel

[61]. Due to the direct linking between the metal contacts and the channel, this mechanism is believed to be the more efficient and dominant transport mechanism which is responsible for the Ohmic contact formation at high temperatures. Fig 3.5 shows the cross-sectional TEM image of the annealed source/drain Ohmic contact using the Ti/Al/Ni/Au metal stack. A clear diffusion of metal into the AlGaN barrier layer is observed. This provides a direct conduction path between the metal and the 2DEG channel which contributes to low contact resistance.

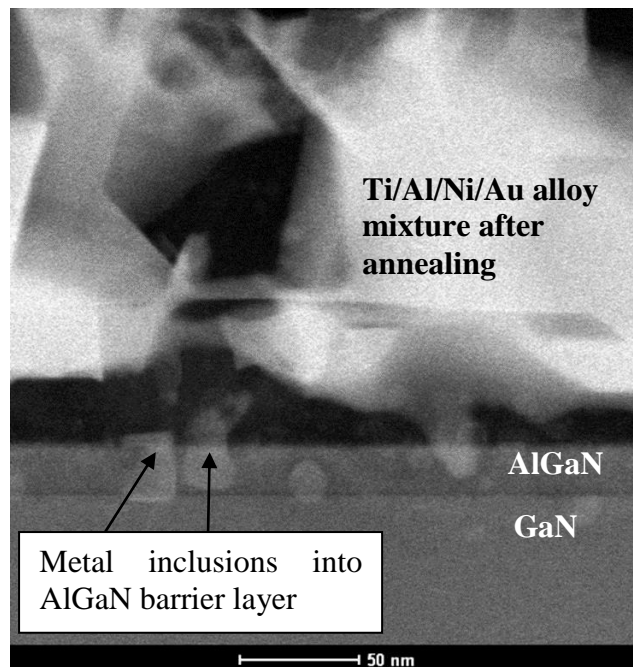


Fig 3.5: Cross-section TEM image of the source/drain contacts using Ti/Al/Ni/Au metal stack after annealing at 825 °C for 60 s. Metal inclusions into the AlGaN/GaN interface are observed.

Besides being involved in the reaction with Al and GaN in the formation of Ohmic contacts, Ti also acts as a wetting agent which promotes Al adhesion onto the GaN/AlGaN layers. Nevertheless in the fabrication process, the Ti/Al layers are prone to oxidation which can degrade the durability and resistivity of the contacts. Hence, an anti-oxidant coating material such as gold (Au) is used as a capping layer to prevent the oxidation of the Ti/Al layers [60]. In addition

to improved oxidation resistance, Au provides better electrical contact due to its lower metal sheet resistance. However, research later found that the highly diffusive Au can penetrate through the Ti/Al layers and react with the Al; forming a highly resistive purple plague alloy which degrades the contact performance [62, 63]. Thus a transition layer, Ni acting as a diffusion barrier between the Ti/Al bilayers and the Au cap is needed. This diffusion barrier serves to prevent the inward diffusion of Au, as well as the outward diffusion of Ti/Al [64]. The schematic below briefly illustrates the possible metal inter-diffusion of the Ti/Al/Ni/Au contacts during alloy formation at high temperature annealing.

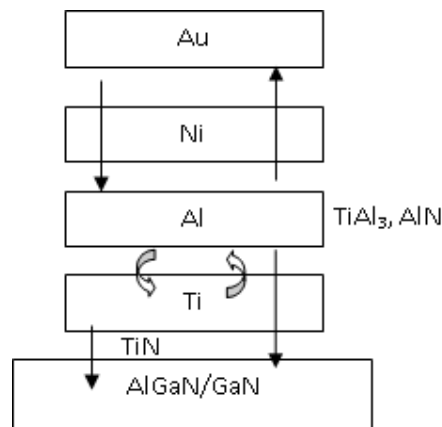


Fig 3.6: Schematic illustration of Ti/Al/Ni/Au Ohmic contact alloy mechanism during the high temperature annealing step.

Studies showed that the relative thickness between the Ti and Al layers is an important factor as both layers are equally responsible for achieving optimum Ohmic contact properties. Higher annealing temperature is required for Ti-rich samples to achieve comparable contact resistivity with respect to Al-rich contacts [65]. Having said that, a sufficient amount of Ti is needed to form the TiN layer at the interface, which is responsible for the carrier tunneling mechanism. However, too much Ti will result in an aggressive reaction with

GaN, leading to the formation of large voids underneath the TiN layer [66]. The presence of large voids will reduce the effective contact area and increase the contact resistance. Therefore, a relative amount of Al should be present as Al is able to mitigate the aggressive Ti-GaN reaction as reported by Van Daele *et.al* [67]. There are several reported optimum Ti/Al ratios (0.10 to 0.167) [66, 67] which are material and process dependent. It is therefore essential to conduct experiments to investigate the optimum Ti/Al relative thickness of the fabricated contacts to achieve the lowest possible contact resistance.

Generally, the conventional Ti/Al/Ni/Au metal contact scheme has good contact resistance but poor uneven surface morphology as shown in Fig 3.7. The reported average root mean square (RMS) value of surface of Ti/Al/Ni/Au contacts after annealing is about 40 nm for a 10 μm x 10 μm sampling size [68]. The bumpy bulgy surface is attributed to the Ni-Al agglomeration as well as the formation of AlAu₄ alloy phase caused by high temperatures during annealing [34, 35]. A rough surface is not desirable for high frequency microwave applications due to non-uniformity current distribution and inconsistent signal attenuation. Furthermore, there is also a significant lateral overflow issue which leads to poor edge line definition. This could be a problem for short channel devices which have very small gate to source/drain critical dimensions, leading to further reliability (gate-to-source/drain shorts) and down scaling issues.

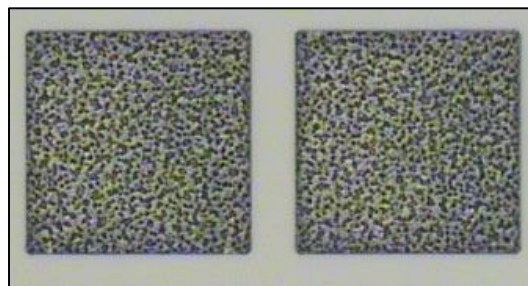


Fig 3.7: Optical micrographs of the rough surface morphology of the Ti/Al/Ni/Au metal stack on TLM test structures after annealing at 825 °C for 60 s.

3.2.4 Schottky Gate Formation

After the source/drain Ohmic contacts optimization, Schottky gate contact formation is the next crucial step in the AlGaIn/GaN HEMT process flow. The gate patterning is defined using optical lithography with a similar photoresist spin coat recipe as that for the mesa isolation and source/drain patterning schemes. However, the exposure time is slightly longer as the dimensions of the gate opening are significantly smaller. This is to ensure that the gate openings are exposed and defined properly in between the source and drain. Optimizing the developing duration is needed in order to define the gate structures perfectly. The gate electrode requires good rectifying behavior in order to achieve good gate control as well as low leakage current performance. Thus, metals such as Ni, Au, Pt, and Pd with high work function, high Schottky barrier height and good adhesion property to the AlGaIn/GaN semiconductor are preferred [64, 69, 70]. In this report, Ni/Au (20/100 nm) is deposited using an e-beam evaporator as the gate contact. Ni is reported to have good adhesion on the AlGaIn and GaN epilayers while Au is crucial in preventing oxidation of Ni as well as providing low gate contact resistance [66]. Typically, a Ni/Au Schottky gate has a reported ideality factor and barrier height of 1.04 and 0.95 eV respectively [71]. However, the ideality factor is usually larger than unity due to the high dislocation density of the GaN layers, as reported by Q.Z. Liu [72]. HEMT device with various gate lengths ranging from 2 to 10 μm are fabricated in this research for multi measurement purposes.

3.3 Electrical Characterization Methods

3.3.1 Introduction: Prober System

In this research, most of the current-voltage (I-V) and capacitance voltage (C-V) measurements used to characterize the electrical properties of the fabricated AlGaIn/GaN HEMTs are done using the 200 mm Cascade Microtech wafer probe station and the 4200-SCS Keithley Semiconductor Characterization System as shown in Fig 3.8.

The Keithley Semiconductor Characterization System is preinstalled with the Keithley Interactive Test Environment (KITE) software which offers a user friendly interface for parametric extraction and analysis with graphical support. The source-monitor-units (SMU) of the Keithley system are connected to the probe heads of the wafer probe station via tri-axial cables which are 1.5 m in length. To provide contact for the measurements of the samples, a total of four probe heads with tungsten pins mounted are available. The wafer probe station also includes a thermal chuck holder which acts as a stage; which is capable of holding sample wafers with sizes ranging from 1 cm x 1 cm size to 8 inches. The chuck is also connected to an ATT System Heater which enables temperature variations ranging from room temperature to temperatures as high as 300 °C. Air leg stabilizers are also installed at each of the probe station's legs in order to minimize external contacts and vibrations. Lastly, the system is capable of measuring very low currents with a resolution as low as 0.1 fA with two pre-installed remote preamps.

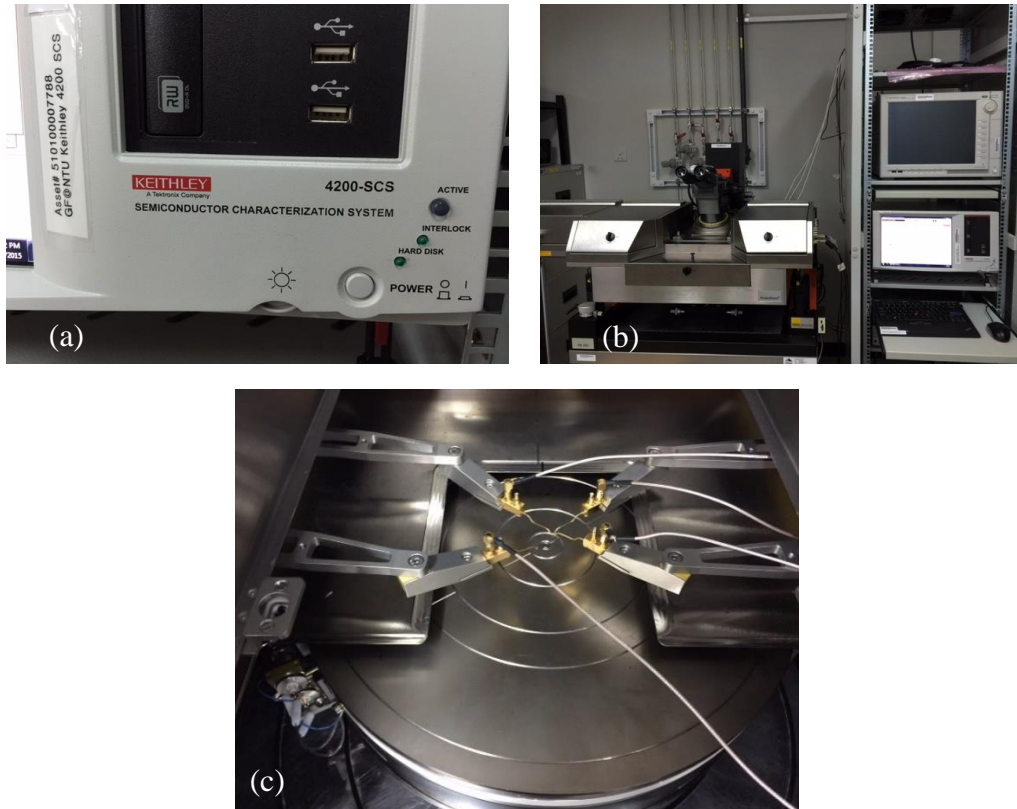


Fig 3.8: Overall electrical testing and measuring environment (a) Keithley 4200-SCS Semiconductor Characterization System, (b) 200 mm Cascade Microtech wafer probe station for device under test (DUT) and (c) 200 mm wafer chuck holder with 4 prober heads connected to the SMU of the Keithley.

3.3.2 Transmission Line Method (TLM)

Low Ohmic contact resistance is essential for AlGaIn/GaN HEMT in order to achieve high drain current performance especially when Au is not compatible for the Si CMOS technology. Hence, it is important to extract parameters such as contact resistance, R_C and specific contact resistivity, ρ_c in order to study the quality of the Ohmic contact formation.

In this report, the Transmission Line Method (TLM) developed by Shockley [73] is used to evaluate the contact resistance properties of the AlGaIn/GaN HEMT devices. Generally, two types of test structures are used; the Linear TLM (LTLM) and the Circular TLM (CTLM) structures. In this

thesis, the LTLM structure is used with an additional mesa isolation etching as compared to CTLM structure. The mesa isolation is essential to avoid any unwanted current spreading and to ensure the current only flows between the adjacent contact pads in the x-direction as shown in Figure 3.9 below.

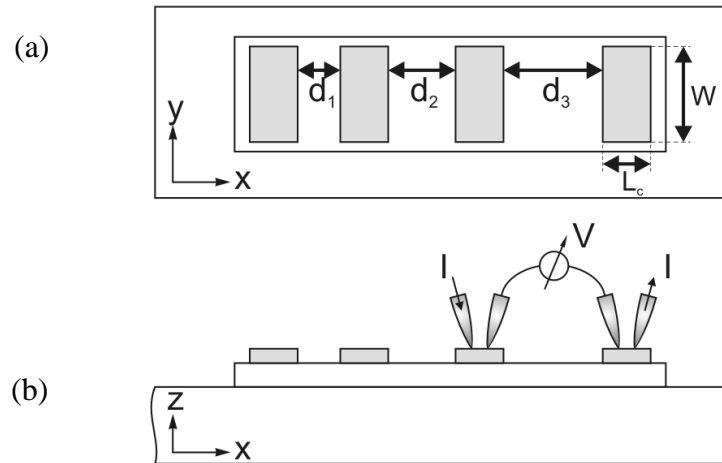


Fig 3.9: (a) Schematic representation of the LTLM test structures to extract the contact resistance parameters. W and L represents the width and length of the contact pad, d is the gap distance between the contact pads (b) Measurement configurations using the 4 point-probe or Van der Pauw method (2 for current and 2 for voltage) to measure the resistance.

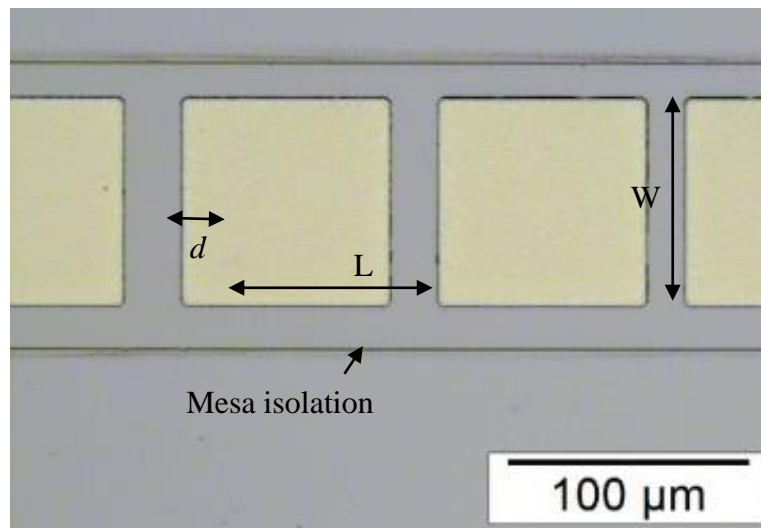


Fig 3.10: Optical micrographs of the fabricated Linear Transfer Length Method (LTLM) test structure. L and W represent the length and width of the square contact pads while d represents the gap between each pads. ($L=W = 85 \mu\text{m}$ while the gap distance, $d = 13, 17, 21, 25, 29,$ and $37 \mu\text{m}$ respectively).

In this report, the contact pads are square with $L=W=85 \mu\text{m}$. The gap distance between the contact pads are 13, 17, 21, 25, 29, and 37 μm respectively. Mesa isolation is done using dry ICP plasma etching with an average step height of 350-400nm. The measured total resistance is basically contributed by several components as shown in the expression below:

$$R_T = 2R_C + 2R_M + R_{semi} \quad (3-1)$$

Where R_T is total resistance measured, R_C is the contact resistance between the metal and semiconductor interface, R_M is the metal resistance and R_{semi} is the semiconductor resistance. Generally, the R_M is very low ($R_C \gg R_M$) and can be neglected. Therefore, equation (3-1) can be further expressed as follow:

$$R_T = 2R_C + R_{semi} \quad (3-2)$$

$$R_{semi} = R_S \frac{L}{W} \quad (3-3)$$

Where R_S is the sheet resistance in terms of Ω/sq and R_C is the contact resistance in terms of $\Omega.\text{mm}$. The effective contact length or transfer length, L_T is defined as the average distance for a carrier (electron or hole) to transport in the semiconductor under the contact before it flows up into the contact.

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \quad (3-4)$$

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_S L_T}{W} \quad (3-5)$$

$$\rho_C = \frac{R_C^2}{R_S} \quad (3-6)$$

Where ρ_C is the specific contact resistivity in terms of $\Omega.\text{cm}^2$ and the effective area of contact is assumed to be $L_T W$. Equation (3-2) can be further expressed as follows [74]:

$$R_T = 2\frac{R_S L_T}{W} + R_S \frac{L}{W} \quad (3-7)$$

$$R_T = \frac{R_S}{W} (L + 2L_T) \quad (3-8)$$

Hence, when the measured resistance, R_T is plotted as function of gap distance between the contact pads, the contact resistance and specific contact resistivity can be extracted accordingly as shown in Fig 3.11 below.

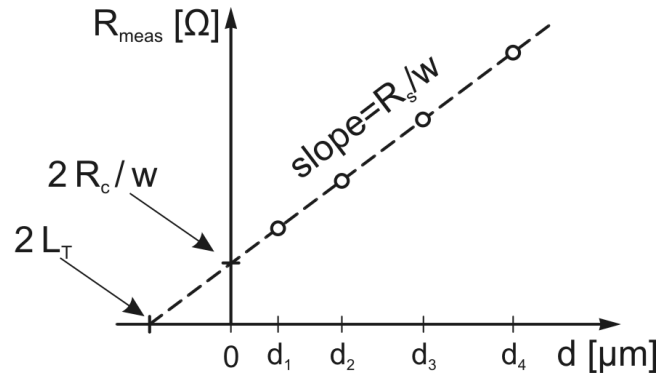


Fig 3.11: Total resistance measured as a function of contact pad spacing, d .

3.3.3 Schottky Contact Parameters Extraction (Current-Voltage Method)

A good quality and thermally stable Schottky contact is very important for the AlGaIn/GaN HEMT device. Schottky contacts with good gate control, low reverse gate leakage current while maintaining high breakdown voltage are essential. Two important parameters in characterizing Schottky contacts are the Schottky barrier height, ϕ_B and the ideality factor, n . In an ideal case, the forward current-voltage characteristics should be linear with a unity ideality factor; indicating that the barrier height is independent of the gate bias and the current transport mechanism is governed by thermionic emission (TE). However, most of the practical devices usually deviate from the ideal scenario due to several factors such as the presence of interface states, gate bias

dependent barrier height as well as the existence of other transport mechanisms other than thermionic emission [75].

There are several methods in extracting Schottky contact parameters, namely; (i) current-voltage (I-V) method, (ii) capacitance-voltage (C-V) method, (iii) activation energy method and (iv) photo-emission method. In this report, the current-voltage (I-V) method is used to extract the Schottky barrier height and the ideality factor of the fabricated devices. Generally, the thermionic emission current-voltage relationship of a Schottky barrier diode is expressed as the equation (3-9) below [76]:

$$I = I_S \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (3-9)$$

where I_S is the saturation current, n is the ideality factor, q is the electric elementary charge, k is the Boltzman constant, T is the absolute temperature (300K) and V is the bias voltage applied.

The saturation current can be further expressed as:

$$I_S = AA^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \quad (3-10)$$

where A is the effective diode area, ϕ_B is the Schottky Barrier height at zero bias, and A^* is the effective Richardson constant for n-type AlGaIn/GaN ($26.64 \text{ Acm}^{-2}\text{K}^{-2}$) [77]

For $V \geq \frac{3kT}{q}$, equation (3-9) can be simplified as:

$$I = I_S \exp\left(\frac{qV}{nkT}\right) \quad (3-11)$$

$$\ln I = \ln I_S + \frac{qV}{nkT} \quad (3-12)$$

From equation (3-12), it can be observed that by plotting the forward current-voltage curve in the semi-log scale, the ϕ_B and n can be determined from the y-intercept and the slope of the plot respectively. Hence, the Schottky Barrier

height and ideality factor can be calculated respectively from equation (3-13) and (3-14):

$$\phi_B = \frac{kT}{q} \ln \left(\frac{AA^*T^2}{I_S} \right) \quad (3-13)$$

$$n = \frac{q}{kT} \left(\frac{dV}{d \ln I} \right) = \frac{q}{kT} \left(\frac{1}{\text{slope}} \right) \quad (3-14)$$

3.3.4 Hall Measurements

In this report, the Bio-Rad HL5500 setup is used to conduct the Hall measurements in order to study and characterize the AlGaIn/GaN heterostructures grown on the SOI and bulk Si substrates. Hall measurement is a well-known semiconductor characterization technique as it provides information about the carrier mobility, the carrier concentration as well as the sheet resistivity of the given substrates [78].



Fig 3.12: Bio-Rad HL5500 Hall Measurement Setup.

Hall effect was discovered by Edwin Hall in 1879 [79] which basically is a process of measuring the potential difference or Hall Voltage between two non-adjacent contact points when a current is flowing between them under magnetic field. The induced voltage is under the influence of a magnetic field perpendicular to the substrate which generates a force called the Lorentz force

[79]. A typical method of measuring the Hall Effect is by using the Van Der Pauw test method [80]. The working principle of the Van Der Pauw method is shown in Figure 3.13 where the current is flown between contacts 1 and 3 while a magnetic field, B is applied perpendicular to the sample. The potential difference between contact 2 and 4 is measured as the Hall Voltage, V_H . The contacts 1, 2, 3 and 4 are made of indium.

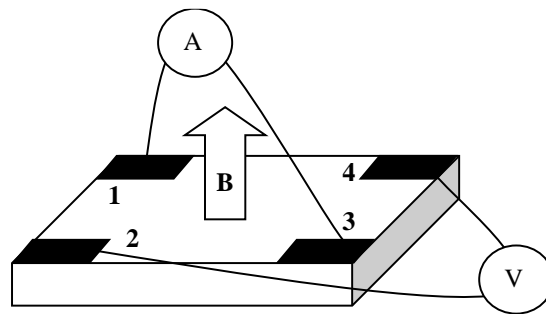


Fig 3.13: Operating Principle of Van Der Pauw Method in Hall Effect measurement.

The measured potential difference can be related to the Lorentz Force by the following expression:

$$\mathbf{F} = q (\mathbf{E} + \mathbf{v} \times \mathbf{B}) \quad (3-15)$$

where F is the Lorentz Force, B is the induced Magnetic field, q is the elementary charge and v is the drift velocity. The Lorentz Force must be compensated by the established electric field called the Hall field, E and hence equation (3-15) can be expressed as following:

$$F = qvB = qE = q \frac{V_H}{d} \quad (3-16)$$

Where V_H is the hall voltage measured and d is the distance between 2 contacts.

The current can also be expressed in terms of drift velocity as follows:

$$I = nqdtv \quad (3-17)$$

Where n is the carrier charge density, and t is the sample thickness ($d \times t$ represents the effective cross section area, A). Combining equation (3-16) and (3-17), the Hall field can be derived as below:

$$E = \frac{V_H}{d} = \frac{I}{nqdt}B = \frac{1}{nq} \left(\frac{IB}{dt} \right) = R_H \left(\frac{IB}{dt} \right) \quad (3-18)$$

Where R_H is the Hall coefficient which is determined through measurement.

From the determined R_H , the respective carrier concentration, n can be calculated using equation (3-19):

$$n = \frac{1}{qR_H} \quad (3-19)$$

Finally, the mobility can be calculated with the following expression:

$$\mu_n = \frac{1}{qnR_{sheet}} \quad (3-20)$$

$$R_{sheet} = \frac{\pi}{\ln 2} \left(\frac{R_{12,34} + R_{41,23}}{2} \right) F \quad (3-21)$$

Where R_{sheet} is the sheet resistivity, and F is the Van Der Pauw shape dependent parameter ($F=1$ for symmetrical shapes).

3.3.5 Interface Traps Analysis using Frequency-dependent Conductance Method

Due to the lattice mismatch and strain induced between AlGa_N and GaN, the heterostructures are prone to the presence of high trap density. These traps locate at the surface of AlGa_N, the hetero-interface of AlGa_N/GaN as well as in the deep buffer layers. These traps can be dislocations, dangling bonds, crystal imperfections, rough interface and defects which are commonly known to exist in III-V materials. Presence of traps can lead to further device degradation. Surface traps acting as trapping centers is similar to a virtual gate which partially depletes the 2DEG channel leading to current collapse

phenomenon [81]. Hetero-interface traps induces scattering at the 2DEG channel which affects the carrier mobility while deep level bulk traps may lead to gate leakage and further reliability issues [82]. R. Stoklas *et al.* reported two types of traps were found in the AlGaIn/GaN heterostructure-based transistors, which are the fast traps (time constant, τ in μs) and slow traps (time constant, τ in ms) [83, 84]. It is claimed that the slow transient traps are attributed by the surface states and buffer layer trapping which can be mitigated by passivation methods [85, 86]. Conversely, AlGaIn/GaN interface induced traps have faster trapping and de-trapping time constant of $\sim 0.1\text{-}1.0 \mu\text{s}$.

Capacitance-voltage measurement is widely used in profiling the interface state density, D_{it} at the AlGaIn/GaN interface. The conductance method proposed by E.H. Nicollian and A. Goetzberge [87] is one of the most sensitive method capable of measuring defect density as low as $10^9 \text{ cm}^{-2} \text{ eV}^{-1}$. This method was first developed to study the interface states of a metal-oxide-silicon (MOS) structure which were later adopted into the AlGaIn/GaN heterostructure system [88] assuming that the AlGaIn barrier acts as a lossy insulator. This frequency-dependent capacitance and conductance technique is effective in providing information of the interface state density at the depletion and weak inversion regions of the AlGaIn/GaN heterostructure [89, 90]. Generally, the reported interface traps density of the AlGaIn/GaN heterointerface are of the value from 10^{12} to $10^{14} \text{ cm}^{-2} \text{ eV}^{-1}$ with an average time constant of $\sim 0.1\text{-}1.0 \mu\text{s}$ for trapping and de-trapping [84, 88, 91]. It is essential to evaluate the quality of the AlGaIn/GaN heterointerface as high interface trap density can cause threshold voltage instability and high leakage current which is ascribed to trap assisted tunneling.

Frequency-Dependent Conductance Method

This AC conductance method is based on the principle of equivalent parallel conductance and capacitance, G_p and C_p measurement as a function of gate bias and frequency. Assuming the conductance as a representation of the loss mechanism due to the interface trap and carriers emission, it is hence a good indication of the interface trap density [92].

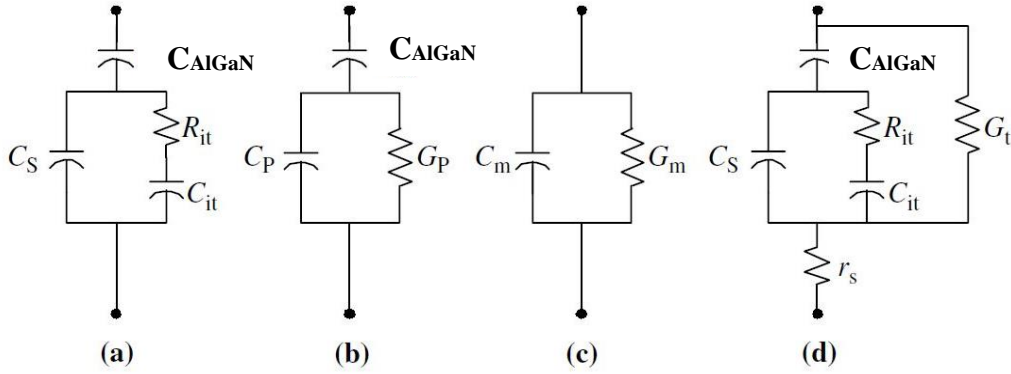


Fig 3.14: Equivalent circuit model of (a) Schottky diode AlGaIn/GaN structure considering AlGaIn/GaN interface states with interface trap time constant, $\tau_{it}=R_{it}C_{it}$ (b) simplified circuit (c) measurement circuit model and (d) the interface trap circuit model considering the series resistance due to gate leakage [92].

Figure 3.14 (a) represents the equivalent circuit model of a Schottky diode AlGaIn/GaN structure with the consideration of AlGaIn/GaN interface states. R_{it} and C_{it} represent the recombination/generation of traps through the interface states, C_{AlGaIn} is the fully depleted AlGaIn barrier capacitance and C_S is the GaN depletion layer capacitance. Circuit in Figure 3.14 (a) can be represented by the simplified circuit (b) where the parallel capacitance and conductance, C_P and G_P are given by the following expressions:

$$C_P = C_S + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \quad (3-21)$$

For single energy level traps, equation (3-21) can be divided by ω leading to equation (3-22) below which is symmetrical in $\omega\tau_{it}$:

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \quad (3-22)$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ and $\tau_{it} = R_{it}C_{it}$.

As for a continuum of trap energy levels, $\frac{G_p}{\omega}$ can be expressed as follows:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad (3-23)$$

Circuit in Fig 3.14 (b) can be further converted into a measurement circuit model in terms of measured capacitance and conductance, C_m and G_m as represented by Fig 3.14 (c). Conductance is measured as a function of different frequencies at varying gate bias. G_p/ω can be plotted against ω and D_{it} can be estimated with the following equation:

$$D_{it} \approx \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{max} \quad (3-24)$$

where A is the effective capacitance area, q is the elementary charge, and $\left(\frac{G_p}{\omega} \right)_{max}$ is the maximum $\frac{G_p}{\omega}$ value at $\omega \approx \frac{2}{\tau_{it}}$. The value of $\frac{G_p}{\omega}$ can be determined with the following equation in terms of measured capacitance and conductance, C_m and G_m assuming negligible series resistance:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{AlGaN}^2}{G_m^2 + \omega^2 (C_{AlGaN} - C_m)^2} \quad (3-25)$$

The discussion so far has been assuming that the series resistance, r_s is negligible. For thin oxides, the amount of gate leakage current is non-negligible. Hence, equation (3-25) is now expressed as below accounting for the series resistance, r_s and tunnel conductance, G_t effect as represented by the circuit model in Fig 3.14 (d) [93]:

$$\frac{G_p}{\omega} = \frac{\omega(G_c - G_t)C_{AlGaIn}^2}{G_c^2 + \omega^2(C_{AlGaIn} - C_c)^2} \quad (3-26)$$

Where $C_c = \frac{C_m}{(1-r_s G_m)^2 + (\omega r_s C_m)^2}$ and $G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1}$

The series resistance, r_s can be calculated at the accumulation bias with the following equation [94]:

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad (3-27)$$

where G_{ma} and C_{ma} are the measured conductance and capacitance at accumulation region. The tunnel conductance, G_t can be estimated from G_c as $\omega \rightarrow 0$.

The distribution of interface state density with respect to energy levels can also be determined with the following equation [95]:

$$E_T = E - E_C = -kT \ln(\tau_{it} \sigma_T N_c v_t) \quad (3-28)$$

where $\tau_{it} = \frac{2}{\omega}$, capture cross section of trap states $\sigma_T = 3.4 \times 10^{15} \text{ cm}^2$, the density of state of conductance band $N_c = 2.2 \times 10^{18} \text{ cm}^{-3}$, and average carrier thermal velocities $v_t = 2.6 \times 10^7 \text{ cm/s}$ [96].

CHAPTER 4: FABRICATION AND CHARACTERIZATION OF ALGAN/GAN HETEROSTRUCTURES GROWN ON SILICON-ON-INSULATOR (SOI) AND BULK-SILICON SUBSTRATES

4.1 Introduction

In the previous chapter, the conventional fabrication process for Au-based AlGaN/GaN HEMT is reviewed along with several electrical characterization methods which were used to analyse the performance of our fabricated devices. In this chapter, the growth of GaN-based devices on available state-of-the-art native and non-native substrates are discussed. The challenges of growing high quality single crystal bulk GaN are reviewed. The challenges faced eventually led to commercially available GaN-based-devices being grown on non-native substrates such as sapphire and silicon carbide (SiC). The sapphire and SiC substrates both have their own advantages and disadvantages. Therefore in recent years, significant attention has been put into the development of the integration of GaN-on-Si. Leveraging on the low cost of Si, its availability in large dimensions, coupled with well-established back-end Si CMOS foundry, silicon appears to be an effective solution for the large-scale production of low cost GaN. However, problems can arise due to GaN and Si having very different in-plane thermal expansion coefficients ($5.6 \times 10^{-6} \text{ K}^{-1}$ for GaN and $2.6 \times 10^{-6} \text{ K}^{-1}$ for Si) and also, a large lattice mismatch of ~17%. Such big differences would induce a large tensile stress, resulting in a high

density of threading dislocations in the AlGaN/GaN heterostructure as well as severe wafer bowing and even cracking. Hence, large scale (150 and 200 mm diameter) GaN-on-Si substrate growth remains a major challenge.

Several growth techniques have been explored to improve the crystalline quality and optical properties of III-V nitrides on Si [26, 28, 97-101]. Among them includes growing AlGaN/GaN heterostructures on thick (1.2 mm) bulk Silicon substrates as well as Silicon-on-insulator (SOI) substrates with a thin 30 nm Si over layer. The GaN on SOI option can potentially result in better device performance which is attributed to reduced bowing and defects. Based on the objective of this report, the properties of AlGaN/GaN heterostructures grown on both bulk Si and SOI substrates will be studied. For further investigation, the electrical performance of HEMT test structures on SOI substrates will be evaluated with respect to those of the bulk-Si counterpart.

4.2 State-of-the-art Gallium Nitride Substrates

4.2.1 Bulk Single Crystal GaN Substrates

Despite the superior material properties of GaN-based-devices in high frequency and high power applications, the device lifetime and performance are constrained by high defect densities and strain-related issues which are caused by growth on foreign substrates [102]. In order to maximize the potential of GaN material properties, GaN devices are ideally grown on large bulk GaN single crystal substrates which have a low dislocation density, with matching lattice properties as well as smooth morphology. However, large dimension single crystal GaN bulk substrates which are of high quality are not

commercially available due to high growth cost and limitations in scalability. As of 2009, GaN costs about \$2000 per cm² for a 2-inch wafer [103].

Typically, crystal materials are grown from liquid or gas phase using the classical growth method which is applicable to thermodynamically stable materials. Unfortunately, these “melt and grow” techniques are not feasible with GaN due to the high vapor pressure and low solubility of nitrogen on GaN [11]. The vapor pressure of nitrogen reaches about 1000 atm at 1200 °C which prevents the incorporation of nitrogen into GaN due to the evaporation of nitrogen at high temperatures [104]. However, at the same time, high temperatures are needed to dissolve nitrogen into GaN. Consequently, in order to suppress the decomposition of GaN at high temperatures near its melting point, extremely high pressures are required. Therefore, due to these constraints, growing uniform and high quality GaN bulk crystals in large dimensions remains a significant challenge.

Another solution that can overcome the challenges brought forth by the classical growth method is to use the hydride vapor phase epitaxy (HVPE) method, where a thick GaN crystal layer is grown epitaxially on a foreign substrate such as sapphire [105]. Free standing bulk GaN is later separated from the sapphire substrate. However the separation process is very difficult due to the hardness and etch-resistance property of sapphire. In addition, large defect densities might be generated at the interface after separation [106]. Therefore, it remains a huge challenge to grow cost effective and high quality single crystalline GaN in a large scale.

4.2.2 GaN on Foreign Substrates: Sapphire (Al_2O_3) and Silicon Carbide (SiC)

Due to the difficulty arising from growing high quality single crystalline bulk GaN substrates, most of the commercialized GaN-based optoelectronics and power devices are grown on foreign substrates. However to date, there is no perfect all-in-one foreign substrate material which can overcome all the challenges posed by the lattice mismatch, thermal expansion coefficient and other compatibility issues with GaN. Two substrates which are being used extensively for commercialized GaN-based-devices are sapphire (α - Al_2O_3) and silicon carbide (SiC). Sapphire is the most commonly used conventional substrate to grow GaN for optoelectronic applications such as UV detectors and LEDs [107]. As for high power microwave and high temperature operations, SiC is the more favorable substrate platform [108].

In order to better understand the advantages and disadvantages of conventionally used substrates for AlGaIn/GaN heteroepitaxy growth, table 4.1 illustrating the comparison of material properties for sapphire, SiC and silicon with respect to GaN is prepared below. The properties of the silicon substrates will be reviewed in the subsequent section of this chapter.

Due to its semi-insulating property, high temperature growth stability and relatively low wafer cost (\$100 for a 2-inch wafer) [109], sapphire has become a promising platform for GaN in optoelectronics devices. However, sapphire has poor thermal conductivity ($0.47 \text{ Wcm}^{-1}\text{K}^{-1}$ at 298 K), a large thermal expansion mismatch (-34%) and also, a significant lattice mismatch (-13%) which make them unfavorable for high power applications. On the other hand, from Table 4.1, SiC has a low lattice mismatch (3.4%), better thermal

conductivity ($4.5 \text{ Wcm}^{-1}\text{K}^{-1}$ at 298 K), and relatively lower thermal expansion coefficient ($4.5 \times 10^{-6} \text{ K}^{-1}$). These properties of SiC have a positive impact on the growth of better quality SiC substrates. Hence, its 2DEG properties are superior and with better heat dissipating capabilities, SiC appears to be the best choice for high power microwave applications. However, the cost of SiC is high, and compared to Si and even sapphire, the cost of SiC is considerably higher. Therefore, researchers in this industry started to look for a more cost effective alternative and eventually found silicon to be a promising candidate.

Substrate Properties	Sapphire (Al ₂ O ₃)	Silicon Carbide (SiC)	Si (111)	GaN
Lattice constant (Å)	4.758	3.081	3.846	3.189
Lattice mismatch (%)	-13	3.4	-17	-
Thermal expansion coefficient (TEC) (10^{-6} K^{-1})	7.3	4.5	2.6	5.6
Thermal expansion mismatch (%)	-34	25	56	-
Thermal Conductivity ($\text{Wcm}^{-1}\text{K}^{-1}$)	0.47	4.5	1.5	1.3
Energy Gap (eV)	9.9	4H-SiC: 3.26 6H-SiC: 3.03	1.12	3.4
Wafer size availability (inch)	2-8	2-6	2-12	2
Relative Cost	Expensive	Expensive	Cheap	Very Expensive
Feasibility of Integration	Hard	Moderate	Easy	-

Table 4.1: Comparison of key GaN substrate material properties [110].

4.2.3 Integration of GaN on Silicon Substrates Technology with Bulk Silicon and Silicon-on-Insulator (SOI) Substrates

Due to the substantially lower cost and well-established Si-microelectronics processing line, silicon substrates have provided a tremendous opportunity in the integration of GaN-based-devices on silicon platforms. Despite having very large lattice and thermal expansion mismatches (17% and 56% respectively), due to the benefits of Si, which includes its abundance and low cost, average thermal conductivity comparable to GaN and most importantly, the availability of large scale Si wafers up to 12 inches, Si is considered to be a more promising candidate compared to SiC and sapphire. Interestingly, the performance of state-of-the-art GaN transistors fabricated on Si substrates are comparable to those grown on sapphire as well as SiC [111, 112].

Why does the incorporation of GaN with Si technology attract significant attention from the industry? As mentioned earlier, Si substrate is able to offer larger wafer diameters which leads to the reduction of cost per die. Moreover, the successful integration of GaN devices on Si platforms provides an enormous opportunity for the industry to go towards the system-on-chip (SoC) concept. The idea that SoC is able to increase the overall performance and functionality of a system chip by integrating GaN devices with Si CMOS devices, has led to a whole new level of circuit design flexibility [113]. A good example of this is the normally-on GaN HEMT and the normally-off Si MOSFET based configuration for a power switching circuit [114].

The two major challenges of integrating GaN on silicon are achieving good quality epitaxial growth of GaN on Si, and developing a fully CMOS-

compatible process. As reviewed earlier, conventional AlGaN/GaN HEMT devices are Au-based. However, Au cannot be used in the CMOS line due to contamination risks. Hence, an Au-free metal scheme has to be developed for successful integration of GaN devices on a Si platform. The development of Au-free AlGaN/GaN HEMTs will be discussed in Chapter 6.

The efforts to achieve good quality and crack-free GaN epitaxy growth on Si have not been very successful mainly due to the large lattice and thermal mismatch between GaN and Si. The in-plane thermal expansion coefficient mismatch ($5.59 \times 10^{-6} \text{ K}^{-1}$ for GaN and $2.6 \times 10^{-6} \text{ K}^{-1}$ for Si) is ~56% and the lattice mismatch between GaN and Si is about 17% [114]. This induces an in-plane tensile stress and mechanical strain on the grown GaN structures, leading to high threading dislocation density and cracking in the GaN layers when the sample is cooled from growth temperature to room temperature [115]. Moreover, a severe bowing effect which leads to non-uniform electrical properties across the wafer is noticed. To address these issues, several works have been done to reduce the tensile stress to achieve crack-free GaN heterostructures, such as AlN seed interlayers [116], multi-step graded AlGaN buffer layers [98] and the insertion of AlN/GaN superlattices [117]. Among them, the AlN buffer layer is essential for high quality epitaxial GaN growth as well as preventing the diffusion of Si into the GaN layers [97]. Typically, the low temperature of the AlN buffer is reported to be an efficient solution to significantly reduce the thermally induced tensile stress, as well as the crack density, ensuring the quality of the GaN epitaxy growth [116].

As mentioned, the high strain induced in-plane triggers severe bowing issues on the 150 mm to 200 mm Si substrates, leading to non-uniform

electrical properties and it also impedes large-scale GaN wafer processing. Hence, to minimize wafer bowing, very thick Si substrates (~1.2 mm) are used to compensate the in-plane generated stress [25]. Reports have shown that increasing Si thickness leads to lower defect dislocations density [118]. Additionally, a thicker GaN buffer layer also helps to reduce buffer leakage as well as improve the crystalline quality [119]. Unfortunately, thick Si substrates are not compatible with existing Si CMOS foundry and processing equipment (lithography and etc.).

An alternative approach, called silicon-on-insulator (SOI), is to grow GaN on a SiO₂ substrate with a thin Si top layer which is 30-35 nm thick. Several works describing the fabrication of GaN-based-light emitting diodes (LED) on SOI substrates have been reported [120-122]. Results showed that by incorporating thin layers of silicon on top of the BOX structure, bowing effects are significantly reduced, compared to growing the GaN directly on the thick bulk Si substrates [123]. A SOI epiwafer with less bowing effects will result in fewer defects, a more uniform distribution of strain and an improvement in two-dimensional electron gas (2DEG) properties which leads to enhanced electrical performance of HEMTs compared to bulk-Si substrates. Furthermore, large dimension SOI substrate wafers are commercially and readily available compared to thick bulk Si substrates.

However, only minimal attention has been paid to the growth of AlGaN/GaN heterostructure on a SOI substrate for HEMT applications. In view of possible tensile stress reduction using the thin Si overlayer and also with the impending maturity of the SOI-based FinFET technology, it is important to explore the potential of a GaN-on-SOI HEMT technology in detail. Moreover,

the growth of GaN-on-SOI looks promising from the viewpoint of integration with SOI-based optoelectromechanical systems and sensors [27, 124, 125].

4.3 Growth & Characterization of AlGaN/GaN Heterostructures on SOI & Bulk Si Substrates

4.3.1 Experimental Details

In this thesis, the growth of AlGaN/GaN heterostructures on a 150 mm diameter silicon-on-insulator (SOI) substrate is studied with an ultra-thin (35 nm) Si overlayer. For comparison, similar AlGaN/GaN heterostructures are simultaneously grown on 150 mm bulk Si (111) substrate. Detailed characterizations are performed to evaluate the wafer and film quality of the grown heterostructures. The wafer bowing, sheet resistivity, and mobility of the AlGaN/GaN layers on both types of substrates are measured. The structural and crystalline quality grown AlN seed buffer layer, GaN and AlGaN layers are studied using several techniques such as scanning transmission electron microscope (STEM), high resolution x-ray diffraction (HRXRD), and micro-photoluminescence.

4.3.2 Growth of AlGaN/GaN Heterostructures

The $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ -based ($x = 0.24 \sim 0.26$) heterostructures are grown on 150 mm diameter SOI (111) as well as bulk Si (111) substrates by metal organic chemical vapor deposition (MOCVD) for comparison purposes. The starting Si handle substrate thickness for SOI (111) growth is $650 \pm 25 \mu\text{m}$

while for bulk Si (111), the substrate thickness is about $675 \pm 25 \mu\text{m}$. The top active Si (111) over layer is realized using separation by implantation of oxygen (SIMOX) process. The buried oxide thickness (BOX) is about 70 – 75 nm. The top Si over layer formed by SIMOX process is ~35 nm thick, with a starting resistivity of $> 2500 \Omega\cdot\text{cm}$. The crystalline quality of the subsequent AlN nucleation seed layer is influenced by high growth temperature (~1100 °C) in which threading dislocations propagate at the heterointerface attributed to the viscous and softening nature of the buried oxide layer [123]. This buried oxide layer serves as an amorphous gliding plane which relaxes the induced strain and mitigates the cracking and bowing issue [126]. As the BOX layer is amorphous in nature, a thin Si over layer is necessary as a compliant substrate to grow the AlN nucleation layer. Reports also found that apart from absorbing the generated dislocations, this thin Si over layer is also effective in reducing the strain generated by the mismatch [127], thus improving the quality of GaN growth [26]. Due to this ability to minimize the strain, as the diameter increases, the SOI substrates exhibit less wafer bowing compared to growing GaN directly on highly resistive bulk Si substrates.

Next, an AlN seed buffer layer with a thickness of ~ 100 nm, which is used for AlGaIn/GaN nucleation, is grown on top of the thin Si over layer. The AlN acts as a nucleation layer for better quality GaN growth due to the smaller lattice mismatch between AlN and GaN (2.5%), compared to Si and GaN (17%) [128]. Thus, such an AlN starting layer followed by AlGaIn/GaN multiple intermediate layers are critical in reducing the stress generated by the large lattice and thermal mismatch between GaN and Si in order to facilitate the growth of crack-free and high quality GaN layers [129]. Studies showed that

this intermediate defect layer generates compressive strain at the growth temperature which counterbalances the thermal induced tensile stress [130].

Subsequently, an intermediate $\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{Al}_z\text{Ga}_{1-z}\text{N}$ ($y = 0.20$; $z = 0.60$) superlattice layers with a total stack thickness of $\sim 2.0 \mu\text{m}$, are grown on top of the AlN seed layer. Primarily, the purpose of these buffer layers is to mitigate stress and reduce threading dislocations [131, 132]. Next, a device grade carbon-doped semi insulating GaN layer with a thickness of approximately $1.0 \mu\text{m}$ is grown on top of the AlGaN/GaN superlattice buffer layer.

For the formation of 2DEG, a 1.0 nm thick AlN spacer followed by a 20 to 25 nm $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer were grown on top of the GaN layer. Reports showed that the additional thin AlN exclusion layer between the AlGaN/GaN heterostructures is able to improve the 2DEG channel charge density and mobility by reducing remote Coulombic scattering. The larger band offset of the AlN with respect to GaN contributes to higher channel charge [133]. With the inclusion of the AlN spacer layer, an increase of 10% and 50% in the density and mobility of 2DEG respectively is reported [134].

Finally a thin GaN cap layer which is $\sim 2.0 \text{ nm}$ thick is grown to protect the top active layer from oxidation and other contaminants. The GaN cap layer also has several other functions which contribute to the surface morphology. The alloy composition with GaN cap is more uniform which results in a more planarized growth. Hence the very thin GaN cap layer is able to improve the inhomogeneties of the AlGaN surface by providing a smoother contact surface with the metal, and this will ultimately result in better electrical properties and improved uniformity across the wafer [135, 136]. Furthermore, the thin GaN cap layer increases the effective Schottky barrier height due to piezoelectric

polarization which successfully reduces the gate leakage [137] and current collapse [138]. Moreover, GaN cap layers can be doped accordingly to improve the Ohmic contact resistance [139]. However, the GaN cap layer cannot be too thick as increasing the thickness can lead to the reduction of 2DEG channel density as reported by A. Asgari [140]. Detailed schematic representations of the AlGaN/GaN heterostructure layers grown on both SOI (111) and bulk Si (111) are shown in Fig 4.1.

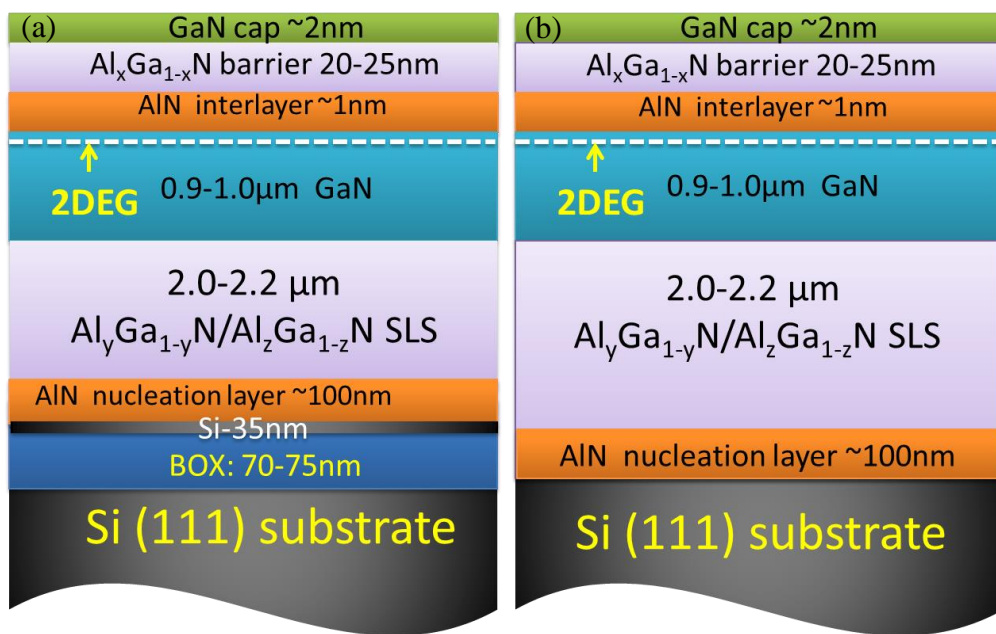


Fig 4.1: Schematic diagrams (not drawn to scale) of AlGaN/GaN heterostructure layers grown on (a) 150 mm SOI (111) and (b) 150 mm bulk-Si (111).

4.3.3 Results & Discussion

The epilayered structures are analyzed using a FEI Titan 80/300 transmission electron microscope (TEM). Fig 4.2 (a) and (b) show the cross-sectional bright field TEM images of the GaN/Al_xGa_{1-x}N/AlN heterostructure grown on the bulk-Si and SOI substrates, respectively. Highly uniform epilayers with sharp transition (i.e. interface) between layers can be observed.

The target thicknesses of individual layers are kept similar during the MOCVD growth for both substrates.

Crystalline quality of the grown layers is analyzed using the high resolution X-ray diffraction (HRXRD) technique. The HRXRD is equipped with a PANalytical X'Pert PRO diffractometer using a four-bounce hybrid mirror monochromatized Cu $K\alpha_1$ radiation ($\lambda = 1.5406 \text{ \AA}$) and an open detector for ω and ω - 2θ scans for symmetry and asymmetry analysis.

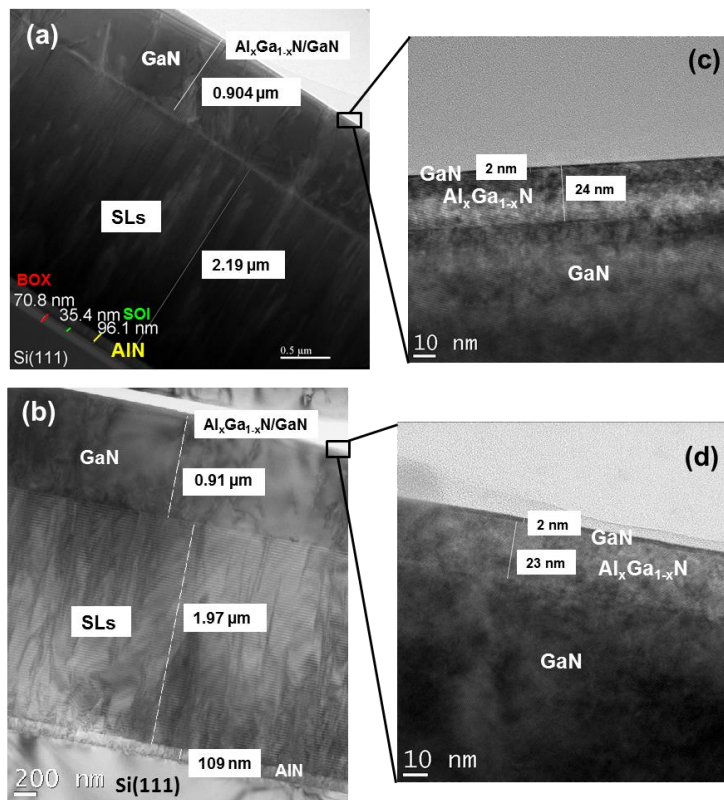


Fig 4.2: High resolution bright-field TEM images of AlGaIn/GaN grown on (a) SOI (111) and (b) bulk Si (111) substrates. Images (c) and (d) on the right illustrate the higher magnification TEM of top 2DEG interfaces with GaN cap/AlGaIn barrier layers.

High resolution x-ray diffraction (HRXRD) scans are generally used to study defects such as misfit and threading dislocations in the GaN epilayer films. The FWHM value of the rocking curves gives an indication of the density and types of defects. To evaluate strain induced defects, where the tilt in GaN

with respect to Si is very high, the (105) reflection FWHM are also studied in GaN heteroepitaxial layers. The line width of these scans addresses the amount of line broadening with respect to (002). If the FWHM for (105) is very high compared to (002) the sample is considered to have a large amount of defects originating from the crystal tilt.

The typical rocking curves for the GaN (002) and (105) diffraction planes are shown in Fig 4.3 (a) and (b) respectively, for the SOI substrates. For each diffraction plane, the full-width at half maximum (FWHM) is extracted and compared to that for the bulk-Si substrate in Table 4.2. For the SOI substrate, the FWHM value for the GaN (002) plane is 680-690 arc sec, which is lower than the 710-720 arc sec for the case of bulk-Si substrate.

The superior crystal quality of the AlGaIn/GaN heterostructures grown on a thin SOI (111) substrate is also proved from the FWHM of the x-ray rocking curves of (105) asymmetric planes. The GaN buffer layer on bulk Si (111) shows the FWHM of 920-930 arc sec for the (105) scan, while similar buffer layer grown on thin SOI (111) shows FWHM of 880-890 arc sec. The higher values of FWHM values from (002) and (105) diffraction planes for GaN buffer on bulk-Si (111) indicates a higher dislocation density in the epilayer.

The wafer bowing and electrical properties of the AlGaIn/GaN epilayers grown on both 150 mm diameter SOI (111) and bulk Si (111) substrates are measured and summarized in Table 4.3. The 2DEG sheet carrier density and mobility of the as-grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure on both substrates are extracted using the Hall Effect measurement via a Bio-Rad HL5500 setup while the wafer bowing properties are measured ex-situ.

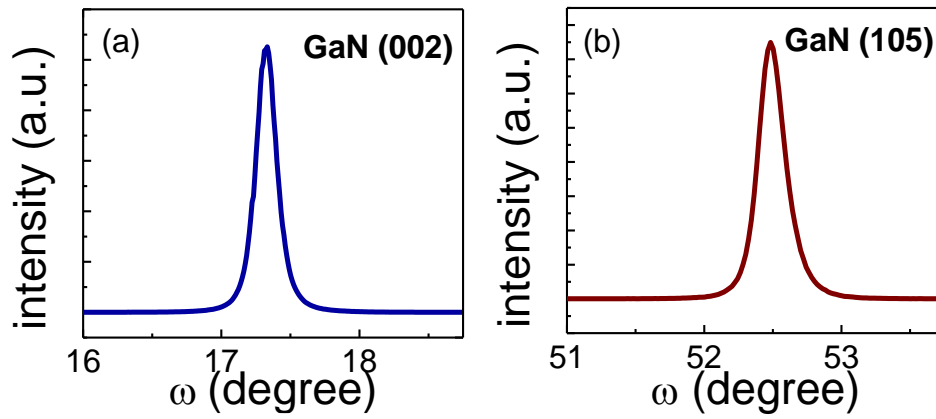


Fig 4.3: Rocking curve of the GaN (002) and (105) diffraction planes, obtained by HRXRD omega scan of the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure grown on SOI (111) substrate.

Sample	Rocking Curve	FWHM (arcsec)
AlGa _x N/GaN on SOI(111)	002	680-690
	105	880-890
AlGa _x N/GaN on Si(111)	002	717-720
	105	920-930

Table 4.2: HRXRD omega scan of (002) and (105) diffraction planes of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ Epitaxial layers on thin SOI (111) and bulk-Si (111).

Properties	AlGa _x N/GaN on Si(111)	AlGa _x N/GaN on SOI(111)
Bow (μm)	-81.74	-39.77
SORI (μm)	103.16	82.29
Resistivity (Ohm/sq)	433.7	356
Mobility ($\text{cm}^2/\text{V.s}$)	1490	1930
Sheet carrier Conc. (cm^{-2})	9.66×10^{12}	9.10×10^{12}

Table 4.3: Wafer bowing and electrical properties of AlGa_xN/GaN epilayers on 150 mm diameter Si (111) and SOI (111) substrates.

From Table 4.3 above, the wafer bowing values for the HEMT stack grown on bulk-Si (111) and SOI are about 81 μm and 40 μm , respectively. Due to the usage of thin SOI (111), similar thickness of AlGaIn/GaN epilayer stacks resulted in a lower wafer bowing property and hence better uniformity of electrical characteristics is expected. In the CMOS processing foundries, the equipment's maximum tolerance level for wafer bowing is 50 μm . Since the obtained wafer bowing value on bulk-Si (111) does not fall within the foundries' specifications, it cannot be fabricated in a conventional Si fab. To prevent this problem, one option is to reduce the GaN buffer thickness since the amount of bowing is proportional to the buffer thickness. However, simply reducing the GaN buffer thickness is not a practical solution as it affects and deteriorates the electrical performances of subsequent grown HEMT structures. On the other hand, the bowing of SOI (111) is flat and falls within the specifications (<50 μm), which is compatible with device fabrication in a standard CMOS line.

Apart from the bowing parameter, the average sheet resistivity estimated from the Hall Effect on bulk Si (111) and SOI (111) are 433.7 Ohm/sq and 356 Ohm/sq respectively. The sheet resistivity is defined by the equation below [20]:

$$R_s = \frac{1}{\int_0^j \mu_n(x) q N(x) dx} = \frac{1}{n_s q \mu_n} \quad (4-1)$$

where n_s is the sheet carrier concentration, μ_n is the electron mobility, and q is the electron charge. In the case of a HEMT structure, the sheet resistance is referred to as the resistance of 2DEG parallel to the surface. The higher the n_s and μ_n , the lower the sheet resistance. The experimental data show that the value of μ_n is ~22% higher for AlGaIn/GaN on SOI (111) compared to that on bulk-Si (111). It is believed that reduced bowing in the epitaxy layer on SOI wafer leads to fewer defects, a more uniform distribution of strain and superior

two-dimensional electron gas (2DEG), which result in improved electrical performance compared to bulk-Si [141].

The bowing effect is higher in Bulk-Si (111) which indicates the presence of higher tensile strain in the layer and thus higher piezoelectric fields. The presence of high tensile strain leads to higher occurrences of point defects as shown in the full-width at half maximum (FWHM) of the XRD peak and the shift in PL peak positions. The point defects in the GaN layer may increase the scattering of 2DEG electron and thus reduce the carrier mobility in the case of the HEMT layers on bulk Si substrates. In the case of GaN grown on a very thin silicon-on-insulator (SOI) substrate (top Si thickness <100 nm), the crystalline quality of initial AlN nucleation is influenced by the high growth temperatures (surface temperature ~1100 °C). The softening and viscous nature of the buried oxide contributes to dislocation movements at AlN/SOI interface, leading to a change in the structural quality of overgrown nitride layers. For larger diameter SOI substrates, the strain balance mechanism thus leads to a reduce wafer bowing as compared to the case of GaN directly grown on bulk Si substrates.

Fig 4.4 shows the full wafer maps of non-destructive sheet resistance measurement of the HEMT stacks on both SOI and Si substrates. Despite similar growth conditions of the epilayers, the heterostructures on SOI substrates show a more uniform sheet resistivity profile with a variation of less than 20%, with an average sheet resistance of about 299 Ω/sq , whereas a variation of approximately 27%, with an average value of 334 Ω/sq , is observed in bulk Si. The non-destructive sheet resistance mapping matches well with the contact-based Hall measurements data.

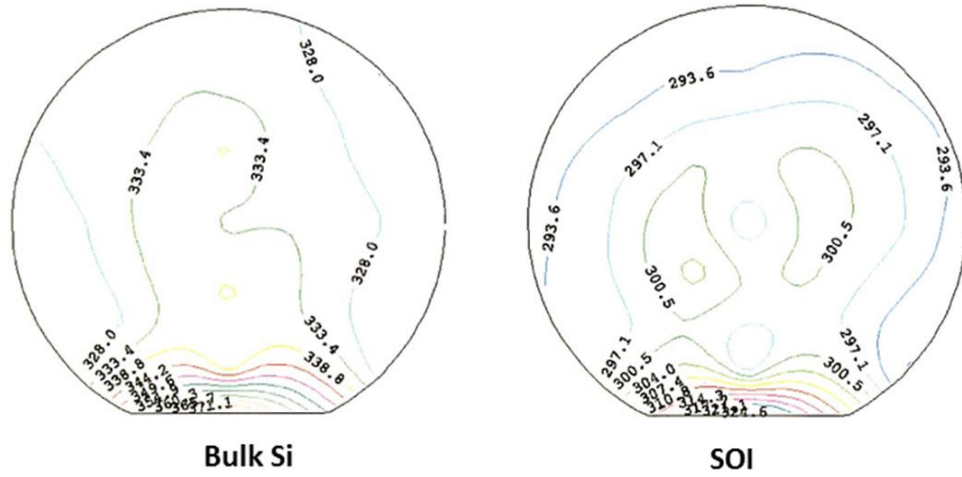


Fig 4.4: The full wafer map of sheet resistance of AlGaIn/GaN epilayer grown on bulk Si (111) and SOI (111) substrates.

Apart from alloy composition, the amount of mechanical stress in the AlGaIn/GaN heterostructure also affects the formation of 2DEG. The ultraviolet (UV) PL measurement is carried out using a 266 nm laser excitation source and Fig 4.5 shows the room temperature micro-PL spectra of AlGaIn/GaN layer grown on both bulk-Si and SOI substrate. The PL spectra show strong band-edge PL peaks near the 362 nm wavelength from the 2DEG GaN channel. The PL peak energies are observed near 3.439 and 3.427 eV for GaN band-edge grown on SOI and bulk Si (111) substrates, respectively. A higher residual interfacial tensile stress in the case of bulk Si slightly increased the sheet carrier density due to band bending.

The Al composition in the thin $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer can also be estimated using the ultraviolet (UV) micro-PL measurements and related PL peaks from the AlGaIn barrier around 3.49 - 4.02 eV. The band gap of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layers as a function of Al composition, x can be expressed as following [142]:

$$E_g^{\text{AlGaIn}}(x) = (1 - x)E_g^{\text{GaN}} + xE_g^{\text{AlN}} - bx(1 - x) \quad (4-2)$$

where $E_g^{AlGaN}(x)$ is the bandgap of $Al_xGa_{1-x}N$, x is the Al fraction, $E_g(GaN)$ is the bandgap of GaN = 3.42 eV, $E_g(AlN)$ is the bandgap of AlN = 6.20 eV [143], and b is the bowing parameter = 1.0 eV. The UV-PL measurements revealed an average Al content of ~ 26% on SOI and ~ 24% in the case of bulk Si (111). This variation is caused by the surface temperature modulation during the growth by MOCVD when SOI induced a much uniform wafer bowing compared to bulk Si. This thus resulted in a lower sheet resistance in the case of SOI whereas improved crystal quality of the GaN buffer, led to the increase in electron mobility as shown in Table 4.3 earlier.

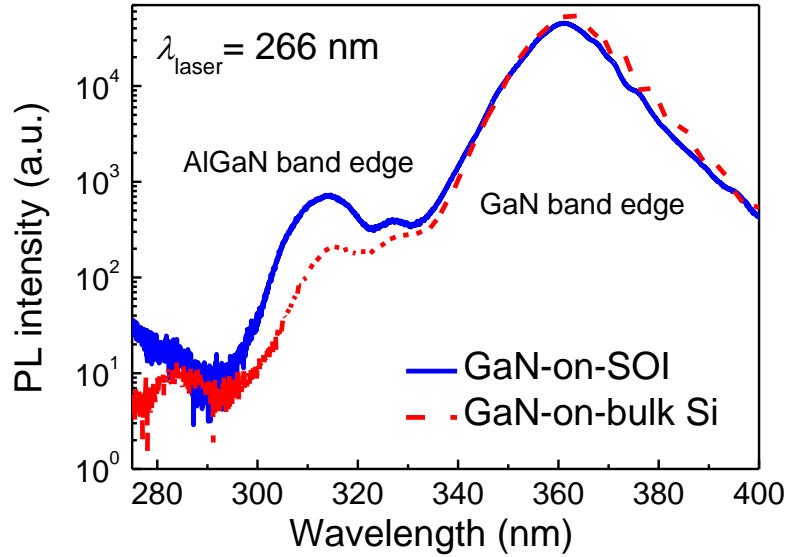


Fig 4.5: Ultraviolet (UV) PL spectra excited using a 266 nm laser from the AlGa_N/Ga_N layer grown on both Bulk-Si and SOI.

The surface roughness of the as-grown epilayers is measured using the Digital Instruments Nanoscope III atomic force microscope (AFM) and the respective AFM images are shown in Fig 4.6 (a) and (b). The extracted root mean square (RMS) surface roughness is almost the same for the nitride structures on both substrates (~0.4 nm for 5.0 $\mu\text{m} \times 5.0 \mu\text{m}$ sampling size). The Etch Pitch Density (EPD) is a measurement method used to determine the

quality of wafers where an etching solution is applied to the surface of the substrate wafers. This is based on the notion that the etch rate will increase at dislocation points in the crystal, which will result in pit formation [144]. Hence, the etch pits counts gives an indication of the threading dislocation density across the 150 mm diameter HEMT epiwafers, where the more pits formed, the higher the number of threading dislocations in the wafer. Using hot phosphoric acid as an etchant, the etch pit density (EPD) of the order of 1.0×10^9 to $2.0 \times 10^9 \text{ cm}^{-2}$ was estimated from the AFM imaging for both type of substrates. With a similar surface roughness observed in the case of both SOI and Si, HEMT test structures fabrication is then carried out using identical device processing schemes.

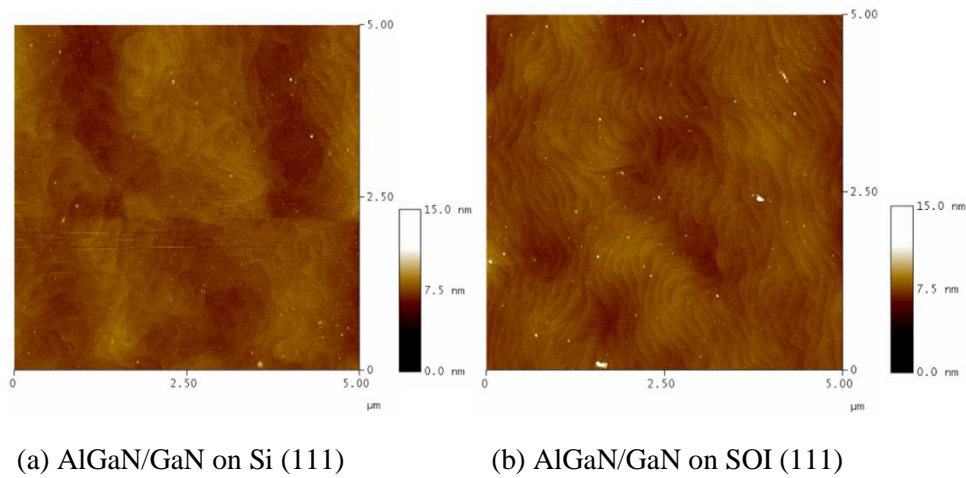


Fig 4.6: AFM images of top GaN/AlGaIn layer grown on (a) bulk-Si and (b) SOI.

4.4 Fabrication & Characterization of HEMTs on Bulk Si and SOI Substrates

4.4.1 Experimental Details

In order to demonstrate and study the comparison of actual device properties fabricated on both bulk Si (111) and SOI (111) substrates, Au-based AlGaIn/GaN HEMT test structures are fabricated on both type of composite substrate simultaneously. The HEMT device fabrication process flow is as described earlier in Chapter 3. This section will be divided into two major parts. Firstly, the device performance of the HEMT devices fabricated on both bulk Si and SOI substrates are evaluated using electrical characterization (DC and C-V measurements). Next, the channel temperature profile of the HEMT devices on both composite substrates is investigated. The micro Raman technique is employed in order to evaluate the self-heating effect of the HEMT devices on both substrates at real-time ON-state operation.

4.4.2 AlGaIn/GaN HEMT Electrical Characterizations

First, the contact resistance of the Ohmic S/D metal stack is characterized using the transmission line method (TLM). Fig 4.7 (a) shows the average total resistance plotted as a function of varied gap spacing of mesa-isolated metal pad TLM structures. From linear fit using the least-squares method, the contact resistance ' R_c ' and specific contact resistivity ' ρ_c ' are extracted with values of 0.52 Ω .mm and 3.0×10^{-6} Ω .cm², respectively, at RTA condition 825 °C for 60 s.

Fig 4.7 (b) shows the high frequency (1 MHz) capacitance-voltage plot of the fabricated HEMTs structure measured in dark environment. Both C-V curves of bulk Si and SOI samples look similar to that of a typical Schottky Gate transistor. The plateau region of constant capacitance in both samples indicates the manifestation of 2DEG. The plateau is longer and the capacitance reduction occurs at higher reverse voltages for GaN on SOI sample as compared to GaN on Si, which is generally observed for higher sheet carrier concentration as reported by J. Osvald [145]. However, Hall measurements show that the carrier concentration is almost similar for both GaN on bulk-Si and GaN on SOI. The defect density level is higher for bulk-Si compared to SOI as observed from the XRD data. We believe that the defects are positively charged which causes the C-V plot shifting towards the positive bias as compared to SOI. As a result, the C-V curve plateau of GaN on SOI looks longer than GaN on bulk-Si. The maximum of the CV curve capacitance value is lower for GaN on SOI, which is due to the slightly higher thickness of AlGaN layer as seen from the TEM images in Fig 4.2.

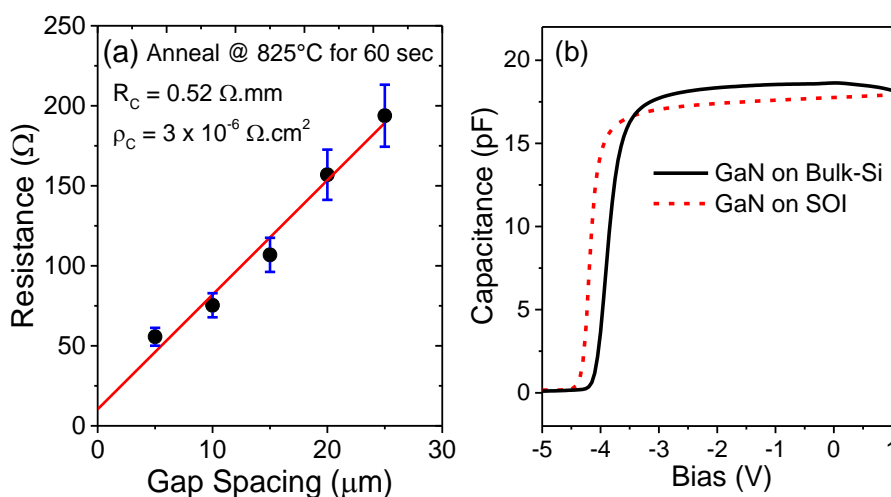


Fig 4.7: (a) Total resistance as a function of contact spacing for Ti/Al/Ni/Au (15/120/40/150 nm) metal stack TLM structure annealed at 825 °C for 60 s. (b) High frequency (1 MHz) capacitance voltage characteristics in dark environment of Ni/Au Schottky gate diode fabricated on 150 nm GaN on SOI and GaN on bulk-Si.

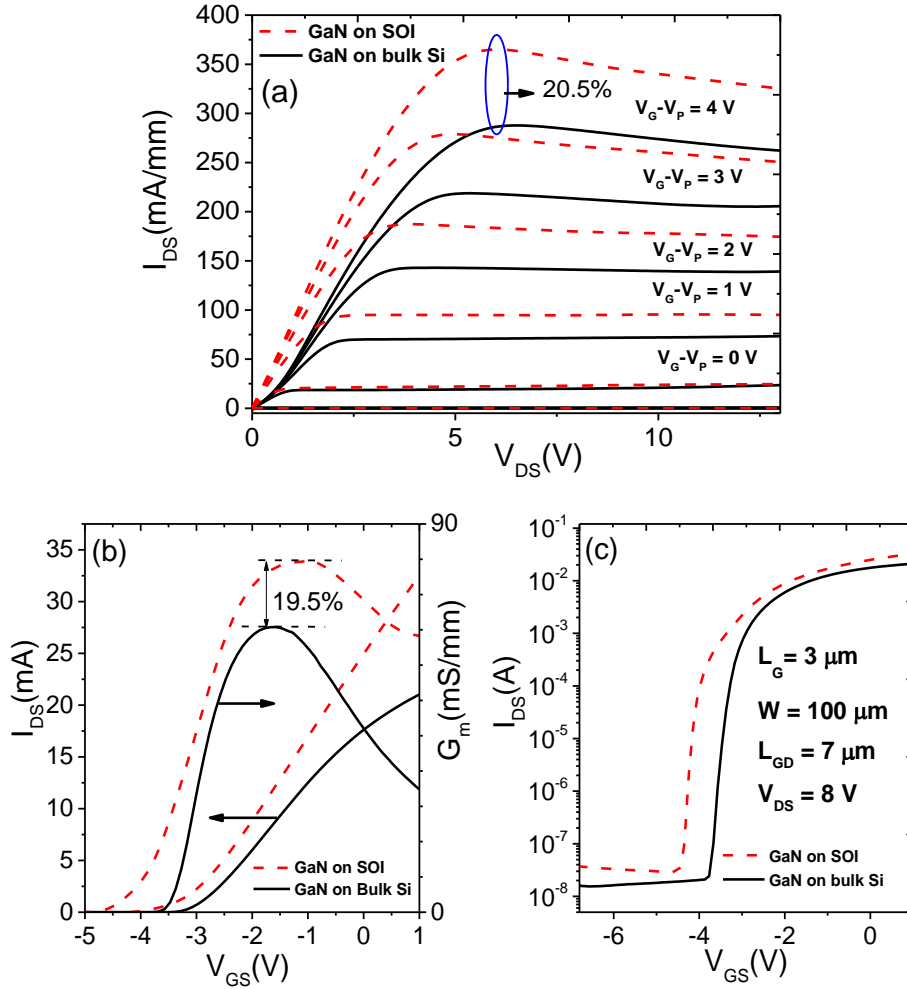


Fig 4.8: (a) Output I_{DS} - V_{DS} characteristics with different V_{GS} - V_P , where V_P is the pinch-off voltage. (b) Transfer characteristics linear I_{GS} - V_{GS} and transconductance G_m plots at $V_{DS} = 8$ V (c) Transfer characteristics logarithmic I_{DS} - V_{GS} plot. Dashed line represents AlGaIn/GaN HEMTs on SOI, while solid line denotes the AlGaIn/GaN HEMTs on bulk Si.

Fig 4.8 (a) shows the I_{DS} - V_{DS} characteristics with different V_{GS} - V_P , where V_P is the pinch-off voltage, for drain current comparison of HEMTs fabricated on both the substrate with $L_G = 3 \mu\text{m}$, $W = 100 \mu\text{m}$ and $L_{GD} = 7 \mu\text{m}$. The gate voltage V_{GS} - V_P steps were maintained same for both the devices during I_{DS} - V_{DS} measurement. The linear and logarithmic plots of I_{DS} - V_{GS} characteristics of AlGaIn/GaN HEMTs are shown in Fig 4.8 (b) and (c) respectively. From the linear extrapolation of I_{DS} - V_{GS} plots, the pinch-off voltage extracted for GaN on SOI is -3.25 V, while for GaN on bulk-Si, it is -

2.8 V. The GaN HEMTs fabricated on SOI substrates exhibit ~20.5% higher I_{DSAT} as compared to bulk-Si counterparts which is attributed to the higher electron mobility and related improvement in the structural quality of the SOI substrates. The slope of the $I_{DS}-V_{DS}$ curves from the HEMTs on GaN-on-SOI is larger than that of device on GaN-on-bulk-Si. Qualitatively it implies that the self-heating effect is higher in these devices compared to the HEMTs on GaN-on-bulk-Si. A higher trans-conductance, G_m of 82.15 mS/mm is observed for the HEMTs on SOI as compared to 66 mS/mm of that on bulk Si. The improvement of the G_m is approximately 19.5% which is in agreement with the carrier mobility improvement as extracted from the Hall Effect measurements, shown in Table 4.3. In addition, both devices show good pinch-off behavior and an I_{ON}/I_{OFF} ratio of 6 decades. It is noteworthy that the device performances (I_{DSAT} , G_m) of a much longer gate length, $L_G = 3 \mu\text{m}$ in our case, is comparable to other reported GaN on SOI and Si device data with shorter channel lengths. A comparative benchmarking is shown in Fig 4.9 with available literature [146-150].

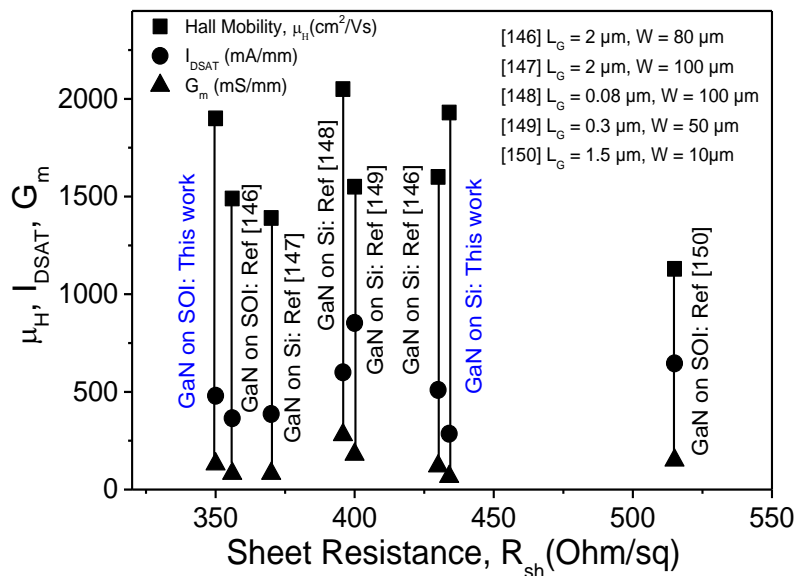


Fig 4.9: Bench mark of Hall mobility μ_H , I_{DSAT} , G_m values against sheet resistance R_{sh} of our results on GaN-on-SOI and GaN-on-bulk-Si with reported results.

4.4.3 AlGaN/GaN HEMT Channel Temperature Probing using Micro Raman Analysis

As shown in the electrical characterization results, reduced wafer bowing in the epitaxy layer on SOI leads to fewer defects, a more uniform distribution of strain and superior two-dimensional electron gas (2DEG) properties, which result in the improved electrical performance of the HEMTs compared to that on bulk-Si. High performance HEMTs yields a high saturation drain current. The high drive current dissipates high power during “on” state operation at large biases, which causes heat generation in the HEMT’s channel. Consequently, this increases the phonon scattering, leading to the reduction of channel carrier mobility and saturation velocity. Therefore, the saturation drain current (I_{DSAT}) characteristics of a HEMT will deteriorate significantly at high drain bias (V_{DS}). This phenomenon is known as localized Joule self-heating effect [151]. The self-heating effect in high-power and high-frequency operation degrades the device performance and introduces long term reliability issues, for example the current collapse phenomenon [152]. In the case of HEMTs on SOI substrate, the self- heating effect may be slightly worse than that of HEMT on bulk Si. Thus, it is important to understand the channel temperature of the HEMTs on SOI during device operation. The extraction of the channel temperature profile can provide useful insights and information for thermal management optimization and device lifetime estimation for reliability testing [151].

Some of the common techniques such as infrared image method, micro-Raman method and electrical temperature sensitive parameter (TSP) method are used to estimate the device channel temperature [151]. The lower spatial

resolution (5-15 μm) of the infrared image method may provide an underestimation of the channel temperature especially for the devices with narrow gate-to-drain architecture. Similarly, the electrical TSP method might not be able to provide an accurate spatial temperature distribution as the method depend on several temperature dependent electrical parameters and assumptions [153]. Amongst the methods, micro Raman technique is well recognized and can be used to extract thermal properties and lattice stress strain in the semiconductor devices with the advantages of high space resolution. Therefore, the thermal effect of substrate on the HEMTs channel temperature during device operation is studied using the Raman method.

4.4.3.1 The Theory of Raman Spectroscopy

Raman scattering is an inelastic process of additional photon scattered from a molecule at different frequencies compared to the incident light. The molecules can be in the forms of gas, liquid or solid state. Generally in solid state, the excitations studied are called quantized lattice vibrations which are known as phonons. In a Raman spectroscopy experiment, photons of a single wavelength from a monochromatic laser source are focused onto a sample and the scattered photons are studied, as illustrated in Fig 4.10.

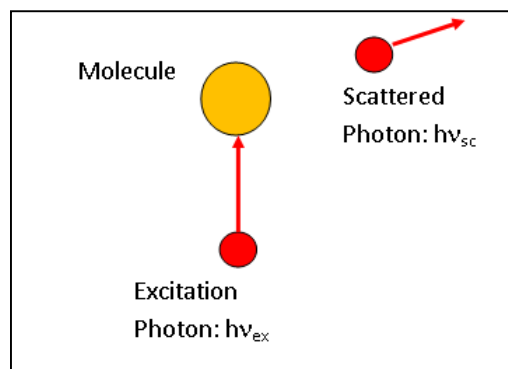


Fig 4.10: Schematic illustration of the Raman scattering event.

Raman scattering is an inelastic interaction where transfer of energy is involved between molecules and photons ($\nu_{sc} \neq \nu_{ex}$). The Raman spectrum is an intensity plot of the Raman scattered radiation as a function of its frequency difference from the incident radiation (usually in units of wave numbers, cm^{-1}) [154]. The differential in frequencies is called the Raman shift. The shift in the in-elastically scattered radiation provides the chemical and structural information of a semiconductor device. The vibrational states of the molecule will determine whether the Raman shift have higher or lower energy levels than the incoming photons (excited) as shown in a simplified energy diagram illustrated in Fig 4.11.

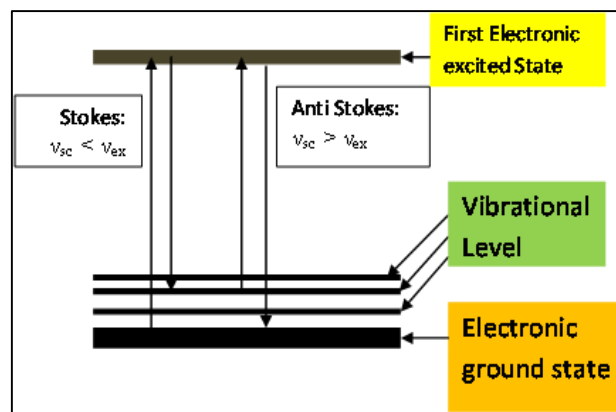


Fig 4.11: Simplified energy diagram illustrating the Raman scattering mechanism.

The energy of the scattered radiation is lower than the incident radiation ($\nu_{sc} < \nu_{ex}$) for the Stokes line while the reverse ($\nu_{sc} > \nu_{ex}$) is known as the anti-Stokes line. The scattering phenomenon varies with molecular arrangement. In the case of GaN, the lattice structure is wurtzite and the analysis of the phonon modes is complicated due to the larger number of atoms in the basis. The various modes of atomic vibration in the GaN crystal are illustrated in Fig 4.12. Among the optical phonons above, the A_1 and E_1 modes are both Raman and infrared active, the E_2 modes are only Raman active while the B_1 modes are

optically silent regardless of Raman or infrared excitation [155, 156]. Fig 4.13 shows the phonon dispersion curves for bulk GaN taken from reference [156]. Typically, the E_2 (high) and A_1 (LO) are the dominant scattering phonons for the AlGaN/GaN material as indicated by the arrow in Fig 4.13.

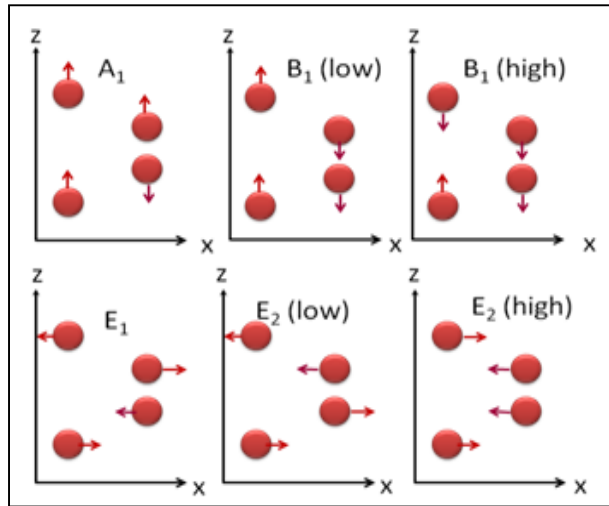


Fig 4.12: Optical phonon modes in the GaN wurtzite structure.

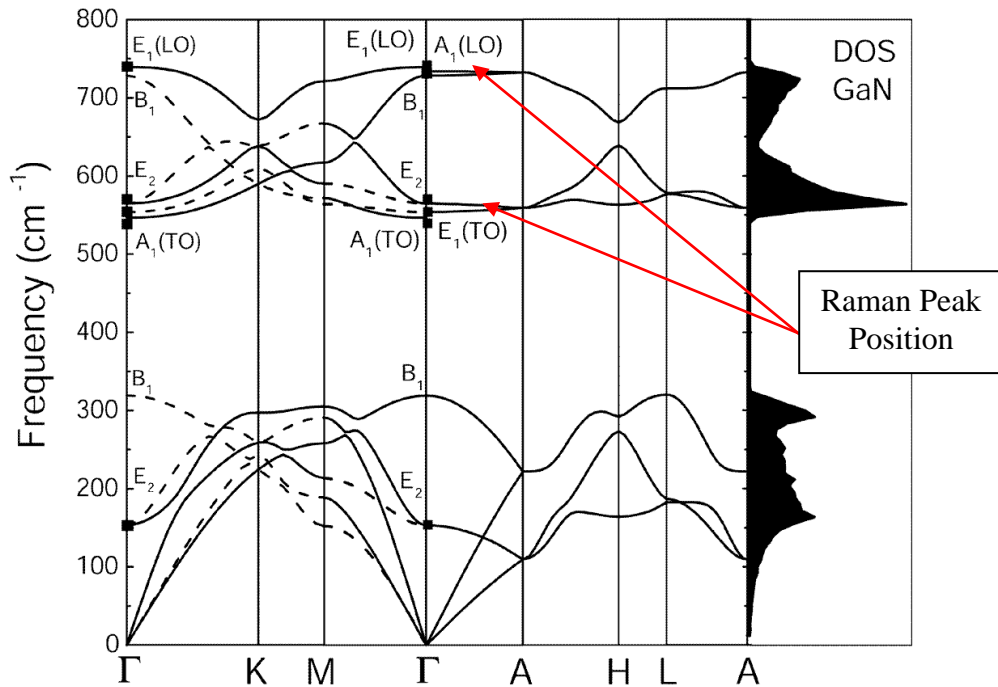


Fig 4.13: Phonon dispersion curves for bulk GaN structure [156].

4.4.3.2 Channel Temperature Measurement Setup

A portable micro-positioner with probe pins and Agilent's Semiconductor Parameter Analyzer have been used in a JY T64000 micro-Raman system. As per experimental protocol, prior to optical probing using the Raman laser, the DC characteristics were monitored using the parameter analyzer. Once the device under tests is marked, the Raman scan is first performed without any biasing, followed by subsequent scans performed under several biasing states. Actual temperature calibration on similar layer structures are required to understand the behavior of several Raman phonon modes in different temperatures prior to starting the device wafer scan. Table 4.4 shows the measurement conditions for temperature profiling using both the calibration wafer and device wafer. The calibration wafer/device wafer was placed in a vacuum chamber with a heater and temperature controller to set up the wafer temperature. After collecting the data and performing the analysis on the bare wafer and a piece of the device wafer, the device wafer was probed for both electrical and Raman scans. The subsequent tests are conducted using line scans.

Temperature	Scan data range (515.45 nm) cm^{-1}
300	400-900
320	400-900
340	400-900
360	400-900
380	400-900
400	400-900
420	400-900
440	400-900
460	400-900
480	400-900

Table 4.4: Measurement conditions for temperature profiling using both calibration and device wafer.

4.4.3.3 Results & Discussion

The Raman spectra are captured using a backscattering geometry with the 515.45 nm Ar-ion laser line excitation. GaN has a hexagonal wurtzite-type crystal structure by nature. According to the Group Theory and experimental findings [157, 158], one A_1 , one E_1 and two E_2 phonon modes are Raman active in a single crystal GaN structure. In this study, the temperature sensitive Raman active peaks of both E_{2H} and Si degenerate O (Γ) phonons are used to study the temperature dependence in the single crystal AlGaN/GaN films.

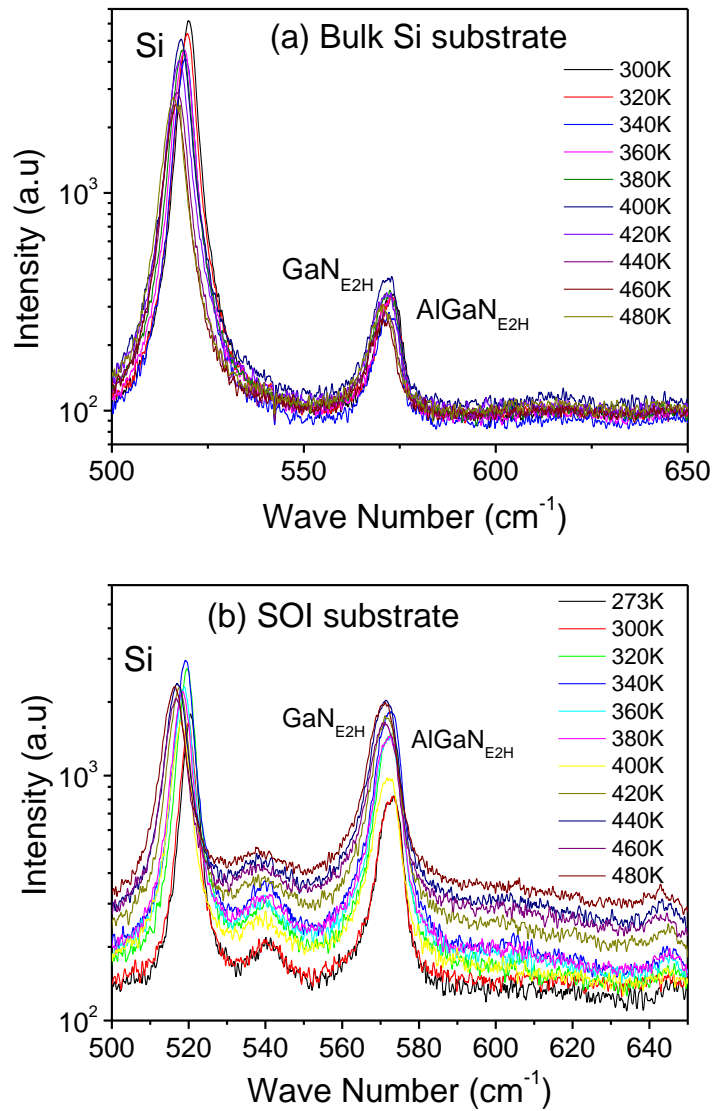


Fig 4.14: Visible Micro-Raman spectra of AlGaN/GaN HEMT on (a) bulk Si and (b) SOI substrates at different temperature using 515.45 nm Ar-ion laser line excitation.

Fig 4.14 (a) and (b) show the visible Micro-Raman Spectra of AlGaIn/GaN HEMT on SOI and bulk Si substrates respectively using 515.45 nm Ar-ion laser line excitation at different temperatures. Attribute to the reflective nature of the SOI substrate (backside mirror at Si/SiO₂/Si interface, the E_{2H} high-phonon peak of GaN is stronger as shown in Fig 4.14 (b) compared to bulk Si substrate. The strong reflective laser light due to the bottom Fabry-Perot cavity allows higher amount of scattered Raman photons to be collected.

The energy peak positions of GaN E_{2H} from buffer and AlGaIn E_{2H} from intermediate superlattices appear to be very close to each other. Thus it is essential to differentiate and extract the precise energy location corresponding to GaN and AlGaIn respectively. The E_{2H} peaks for both GaN and AlGaIn are separated using the de-convolution approach with the Lorentzian fitting as shown in Fig 4.15. Next, the Raman peak shift of GaN E_{2H} with temperature is fitted with the theoretical data for temperature calibration in the later section. Using the temperature calibrated curves, the channel temperature profiles of the HEMTs at ON-state operation can be extracted.

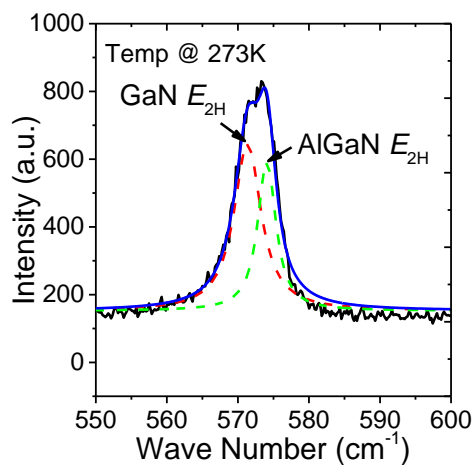


Fig 4.15: De-convolution of Raman spectra to E₂-high peak of GaN and AlGaIn at temperature 273K. Dashed lines denote the Lorentz de-convolution components.

Generally, the temperature dependent phonon frequency and line width are attributed to anharmonic terms of the vibrational Hamiltonian of the crystal lattice [159]. These anharmonic terms contribute to the lattice thermal expansion and interaction between phonons. The phonon frequency shifts with temperature captured by the Raman experiments are the resultant value of the thermal expansion of the lattice, the decay of zone-center optical phonons into phonons of lower energy and strain energy originating from the lattice mismatch during epitaxial growth [160].

Hence, the total phonon frequency with respect to temperature is defined as [161]:

$$\omega(T) = \omega_o + \Delta\omega_e(T) + \Delta\omega_d(T) + \Delta\omega_s(T) \quad (4-3)$$

where ω_o is the phonon frequency in the perfect harmonic lattice, $\Delta\omega_e(T)$ denotes the shift in frequency due to thermal expansion, $\Delta\omega_d(T)$ denotes the frequency shift contributed by the decay of optical phonons to lower energy phonons, and $\Delta\omega_s(T)$ is the frequency shift due to the strain induced by the lattice mismatch.

The phonon frequency shift due to the thermal expansion of the lattice $\Delta\omega_e(T)$, can be further expressed as an isotropic approximation as [162]:

$$\Delta\omega_e(T) = -\omega_o\gamma \int_0^T [\alpha_c(T) + 2\alpha_a(T)]dT \quad (4-4)$$

where α_c and α_a are the thermal expansion coefficients parallel and perpendicular to the wurtzite c axis, respectively, and γ is the Grüneisen parameter. The value of γ is taken as 1.47 for GaN on both bulk Si and SOI [161].

The phonon frequency shift due to the decay of zone-center optical phonons into phonons of lower energy $\Delta\omega_d(T)$ is defined as [163]:

$$\Delta\omega_a(T) = G[1 + 2\eta(T, \omega_o/2)] + H[1 + 3\eta(T, \omega_o/3) + 3\eta^2(T, \omega_o/3)] \quad (4-5)$$

where $\eta(T, \omega) = \left[\exp\left(\frac{\hbar\omega}{k_B T}\right) - 1 \right]$ is the Bose-Einstein distribution function, G and H are anharmonic constants responsible for the symmetrical decay of one phonon into two or three identical phonons.

The phonon frequency shift due to strain component induced $\Delta\omega_s(T)$ is defined in the following equation [164]:

$$\Delta\omega_s^{\frac{GaN}{AlN}}(T) = 2a_{GaN}\epsilon_{xx}^{\frac{AlN}{GaN}} + b_{GaN}\epsilon_{zz}^{\frac{AlN}{GaN}}(T) \quad (4-6)$$

where $\epsilon_{xx}^{\frac{AlN}{GaN}} = (1 + \epsilon_g) \frac{1 + \int_{T_g}^T \alpha_a^{AlN}(T)DT}{1 + \int_{T_g}^T \alpha_a^{GaN}(T)DT} - 1$ and $\epsilon_{zz}^{\frac{AlN}{GaN}} = -\frac{2C_{13}(GaN)}{C_{33}(GaN)} \epsilon_{xx}^{\frac{AlN}{GaN}}$,

α_a^{AlN} and α_a^{GaN} are the temperature dependent in-plane linear expansion coefficients of the AlN and GaN, respectively. The phonon deformation potentials are a_{GaN} and b_{GaN} and the elastic constants are C_{13} and C_{33} of the GaN layer. All the constant parameters used to fit the experimental data using equations (4-3) to (4-6) are shown in the Table 4.5 below.

Properties	AlGaN/GaN on Si(111)	AlGaN/GaN on SOI(111)
γ	1.47	1.47
G (cm ⁻¹)	-0.01	-0.01
H (cm ⁻¹)	-0.12	-0.11
a_{GaN} (cm ⁻¹)	-830	-830
b_{GaN} (cm ⁻¹)	-860	-860
C_{13} (GPa)	106	106
C_{33} (GPa)	398	398
ω_o (cm ⁻¹)	571	571.8

Table 4.5: Parameters used to fit the E_{2H} Raman mode dependence on temperature from HEMTs fabricated on GaN on SOI and GaN on Bulk-Si in Fig 4.16 (a) and (b) using equation (4-3) to (4-6); Ref [161].

The temperature dependent experimental and theoretical values obtained from the fitting using equations (4-3), (4-3), (4-5) and (4-6) of the GaN E_{2H} phonon shifts for GaN on SOI and GaN on bulk-Si HEMTs are shown in Fig 4.16 (a) and (b), respectively. The overall downwards shift of the E_{2H} phonon with respect to temperature is mainly contributed by the thermal expansion of the intrinsic lattice $\Delta\omega_e(T)$.

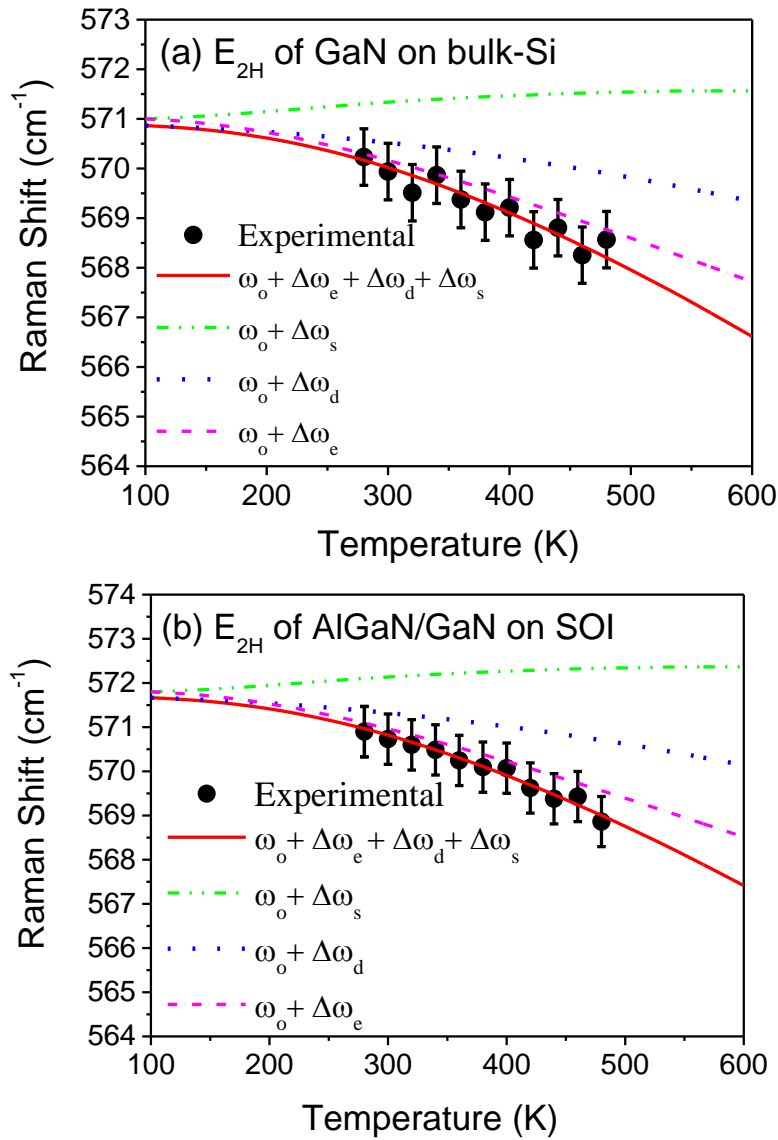


Fig 4.16: Shift in E_{2H} Raman mode of the GaN as a function of temperature: (a) AlGaIn/GaN HEMTs on Bulk-Si and (b) AlGaIn/GaN HEMTs on SOI. The black dots are measured data. The solid red full line is a fit using Eq. 4-3. Different contributions of the phonon decay, thermal expansion as well as strain induced towards the phonon frequency shift are calculated using Eq. 4-4, 4-5 and 4-6 with the fitting parameters in Table 4.5.

The relative E_{2H} phonon decay influence is estimated from the G/H value. The ratio value of G/H is ~ 0.1 , which indicates that the decay into two phonons is negligible [161]. The energy gap of GaN is nearly equal to one half of the E2-phonon energy and is located at the lower edge of the optical phonon branch. Therefore the probability of the phonon to decay into two phonons is low and instead, the likelihood of three phonon decay is higher. The three phonon decay contribution is represented by the blue dotted line in Fig. 4.16 (a) and (b). The contribution of strain is almost flat. However, when all the components are put together, the resultant effect is a downwards shift in the phonon frequency with increasing temperature (solid red line in Fig. 4.16 (a) and (b)). These two curves have been used as temperature calibration curves to estimate the channel temperature of AlGaIn/GaN HEMTs on SOI and bulk-Si during “on” state operations. The protocol of channel temperature estimation is schematically shown in Fig 4.17 below.

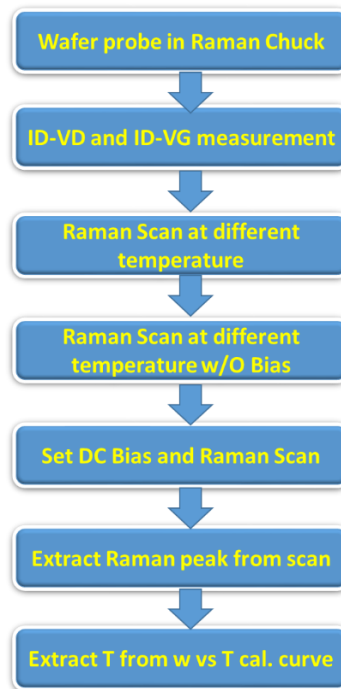


Fig 4.17: Standard Protocol of extracting channel temperature using bare calibration wafer.

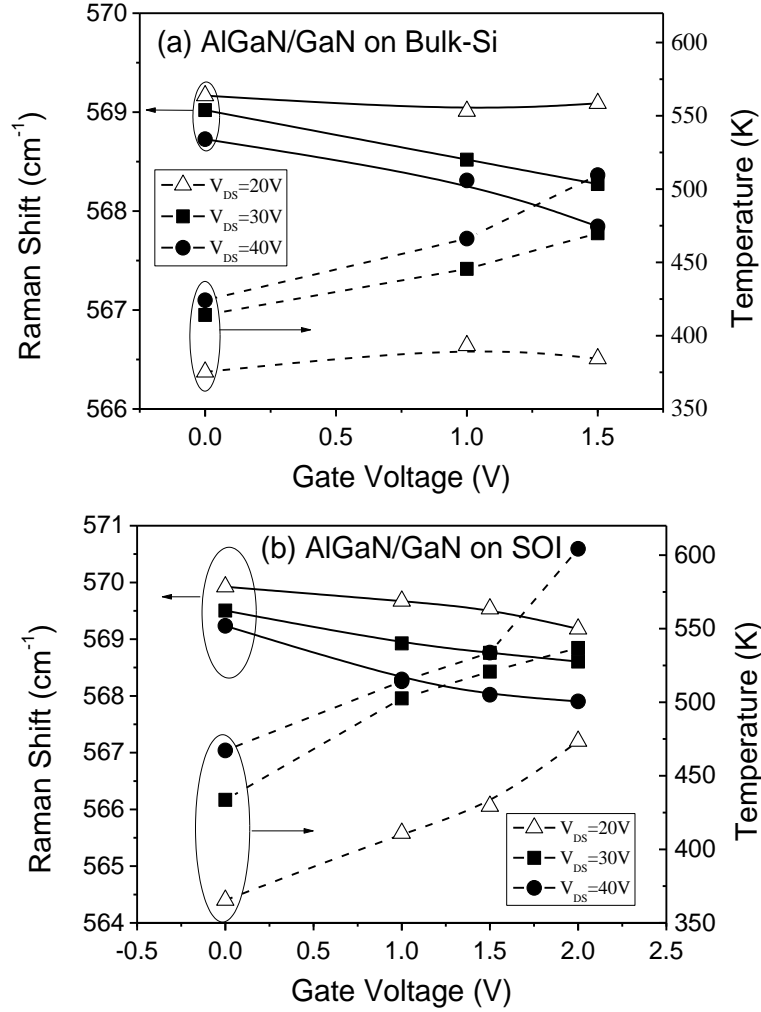


Fig 4.18: Shift in E_{2H} Raman mode and channel temperature of the GaN as a function of gate and drain bias: (a) AlGaIn/GaN HEMTs on Bulk-Si and (b) AlGaIn/GaN HEMTs on SOI.

Fig 4.18 (a) and (b) show the gate and drain bias dependence of the E_{2H} Raman frequency shift and channel temperature. The channel temperature increases with the increase of gate bias (V_{GS}). As the gate bias increases, the opening of the channel widens and thus allows more carriers in the channel. The presence of more carriers in the channel escalates the phonon scattering events and eventually increase the lattice temperature, resulting in higher channel temperature. The channel temperature also increases with the increase of drain bias (V_{DS}) for a fixed gate voltage. The larger drain bias will increase the channel electric-field which accelerates the 2DEG traveling from source to

drain. Once the carrier electrons gain sufficient kinetic energy, they become hot electrons, resulting in increased electron temperature. Consequently, a higher electron temperature will transfer heat to the lattice and thus increase the channel temperature. The transfer of heat from hot electrons also depends on the number of electrons. Fig 4.18 (a) and (b) show that the rate of increase of channel temperature from $V_{DS} = 20$ V to $V_{DS} = 40$ V is not uniform. The initial rate from 20 V to 30 V is significantly higher than 30 V to 40 V for a fixed V_{GS} . This phenomenon is due to the saturation effect of the number of hot electrons in the channel at high V_{DS} .

The channel temperatures have been compared for both GaN on SOI and bulk-Si HEMTs at on-state operation with different level of DC power dissipation as shown in Fig 4.19. The DC power is approximated via $I_{DS} \times V_{DS}$ as dissipated power. The higher temperature of AlGaN/GaN on SOI at fixed power dissipation indicates that its heat dissipation is lower compared to the case of bulk-Si. This is because the thermal conductivity of SiO_2 is lower than Si and thus the generated heat is confined in the layer on top of the BOX, which results in higher temperatures in the GaN on SOI.

Besides self-heating, the presence of defects at the channel layer also influences the current collapse [165]. From the AFM imaging of the samples subjected to hot phosphoric acid etching, we did not observe any significant change in density of surface pits in the two samples. Majority of defects reside at the buffer interfaces in such epitaxial layers. Based on our Raman analyses of Si peak shifts at the AlN/substrate interface, when devices are under ON-state operation, we conclude that the self-heating contributes significantly to the DC characteristics.

The effect of the substrate on the temperature distribution from drain to gate at the AlGaIn/GaN channel region and AlN/Si substrate interface is also investigated using GaN- E_{2H} and optical phonon peak shifts of Si at ON-state operation. The DC biasing conditions are $V_{DS}=20$ V and $V_{GS}=1.5$ V. The line scans of the Raman experiment from drain to gate have been carried out with a step size of $0.2 \mu\text{m}$. Fig. 4.20 shows the channel and substrate temperature profiles obtained from the Raman scattering method. As seen, the temperature distribution from drain to gate is quite uniform for both cases of GaN on SOI and GaN on bulk Si. It is also observed that the AlGaIn/GaN channel and Si substrate temperature is ~ 50 K higher for the case of SOI compared to bulk-Si. This is attributed to the lower thermal conductivity of SiO_2 which has a value of $0.014 \text{ Wcm}^{-1}\text{K}^{-1}$ compared to Si, at $1.5 \text{ Wcm}^{-1}\text{K}^{-1}$ [166]. The generated heat in the ON-state operation is not dissipated due to the presence of BOX and thus the temperature at the channel region and the Si on top of BOX rises higher than the HEMTs on bulk-Si. These observations clearly address the nature of self-heating induced in HEMTs fabricated on SOI as compared to bulk Si with similar Si handle thickness of $650\text{-}675 \mu\text{m}$.

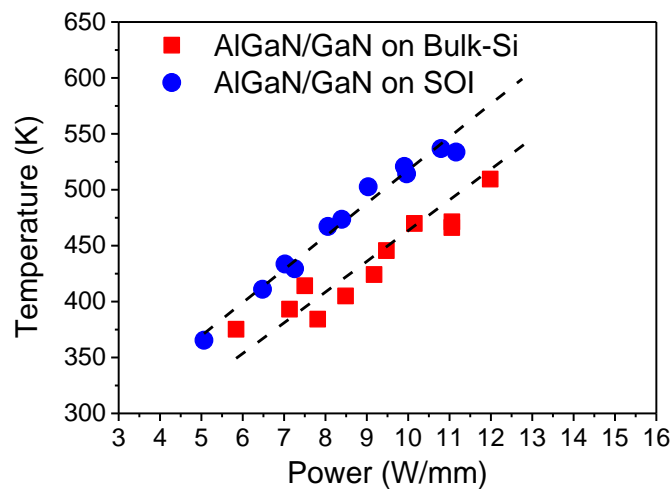


Fig 4.19: The channel temperature measured by micro-Raman thermography techniques on HEMTs device with $L_G=3 \mu\text{m}$, $W=100 \mu\text{m}$ and $L_{GD}=7 \mu\text{m}$ fabricated on both GaN on Bulk-Si and SOI substrate at on state operation with power dissipation.

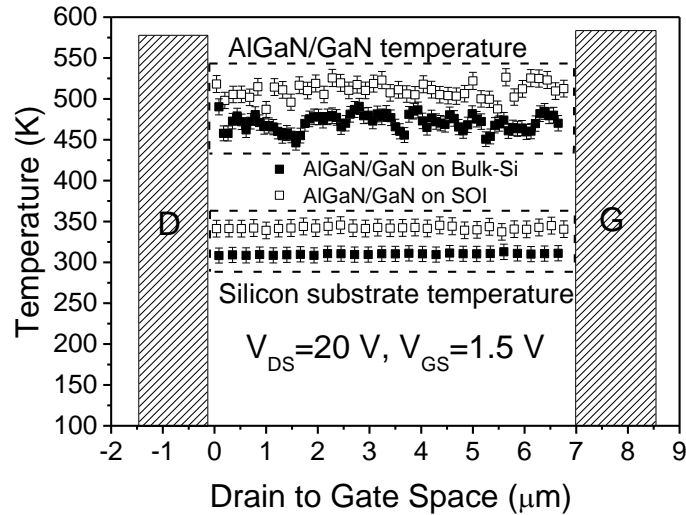


Fig 4.20: The channel temperature in the drain-gate gap of HEMTs device with $L_G=3 \mu\text{m}$, $W=100 \mu\text{m}$ and $L_{GD}=7 \mu\text{m}$ fabricated on both GaN on Bulk-Si and SOI substrate measured by micro-Raman thermography technique.

4.5 Chapter Summary

The growth and characterization of 2DEG in AlGaIn/GaN HEMTs heterostructures epitaxial layer on 150 mm diameter thin SOI (111) substrate (thin Si overlayer $\sim 35 \text{ nm}$) and bulk Si (111) have been discussed in this chapter. An improvement in 2DEG mobility and sheet resistivity uniformity in GaN on SOI substrates is attributed to the reduced wafer bowing. Due to the viscous and softening nature of the buried oxide in SOI substrates, it acts as an amorphous gliding platform to reduce the induced strain during high temperature growth. Due to such a strain balancing mechanism, SOI substrates demonstrate overall lower wafer bowing. The crystalline quality of the AlGaIn/GaN heterostructures grown on both substrates is studied using the high resolution X-ray diffraction (HRXRD) analysis. Both rocking curves of the GaN (002) and (105) diffraction planes show a lower FWHM value in GaN on SOI which implies a lower dislocation density in the epilayers hence confirms

the superior crystal quality of the AlGaIn/GaN heterostructure grown on SOI as compared to bulk Si.

In order to study the actual device performance, AlGaIn/GaN HEMT test structures are fabricated and characterized on both SOI and bulk Si substrates. From the DC characterizations, an improvement of 20.5% and 19.5% in I_{DSAT} and g_m respectively for HEMTs on SOI is observed compared to bulk Si counterparts. Such electrical improvements are attributed by the higher electron mobility and related structural quality improvement of the SOI substrates.

The effect of substrate heating on the HEMTs channel temperature during on-state operation is studied using the micro Raman method. The channel temperature increases with the increase in gate bias (V_{GS}) and drain bias (V_{DS}) due to the combined effects of channel carrier enhancement and increased hot electron temperature caused by the higher drain bias field. For on-state fixed power dissipation, AlGaIn/GaN HEMT on SOI suffers a greater self-heating, with ~50 K higher channel temperature compared to the case of bulk-Si. This is attributed to the lower thermal conduction of SiO_2 of the buried oxide layer. Nevertheless, with mitigation of self-heating, the AlGaIn/GaN-on-SOI, in view of its more superior structural, thermal stability and improved 2DEG performance, should offer an attractive alternative for integration of GaN-based technology with the CMOS platform. Additional thermal management solution may also be needed to explore the applicability of GaN-SOI for high speed electronic devices.

CHAPTER 5: EFFECT OF GERMANIUM DIFFUSION ON $Al_xGa_{1-x}N/GaN$ HEMT FOR ENHANCEMENT MODE OF OPERATION

5.1 Introduction

AlGaN/GaN HEMT exists as a normally-on or depletion mode (D-mode) device due to the presence of the 2DEG channel formed by the polarization effect of the nitride natures. The typical threshold voltage for a conventional AlGaN/GaN HEMT is about -4 V [51, 52]. With regards to RF and microwave applications, enhancement mode (E-mode) HEMT devices are favorable because a single polarity RF supply which reduces the overall complexity, cost and size of the circuit design and system architecture, can be used [167]. As for power switching applications, E-mode HEMTs are inherently better in terms of fail-safe operation in addition to overall power consumption reduction. Moreover, a large positive threshold voltage is desirable to avoid unintentional faulty power-on due to electrical or magnetic interference. Furthermore, for digital logic applications, E-mode is needed for integration with D-mode HEMT to form the Direct Coupled FET Logic (inverter or ring oscillator) which offers a much simpler circuit design configuration [168]. Therefore, E-mode HEMT devices are able to deliver an overall improved performance in both circuit and system levels for RF, power and digital logic applications.

In this study, a novel approach in diffusing germanium at the gate region of AlGaN/GaN HEMT through annealing for threshold voltage shifting is demonstrated. Germanium, being an n-type dopant with respect to the AlGaN

layer, is proposed to be able to compensate the positive sheet charges at the AlGa_N surface, which leads to the 2DEG channel depletion and thus threshold voltage shift. There are reported works on Ge-doping on GaN whereby these results are primarily focused on relieving the induced stress when growing crack-free MOCVD-based GaN on Si substrates [169], as well as for n-type dopant conductivity purposes [170, 171]. In this work, the investigation of Ge diffusion at the gate and its impact on threshold voltage shift for possible E-mode type behavior for AlGa_N/GaN HEMT fabrication have been presented.

5.2 Literature Review of Enhancement mode AlGa_N/GaN HEMT Development

There are several approaches reported by different groups with regards to tuning the threshold voltage to achieve enhancement mode behavior. However, developing a standard processing method with good uniformity and repeatability still remains a challenge, mainly due to the strong polarization charges in the AlGa_N/GaN heterostructure layers. Generally, the threshold voltage of the AlGa_N/GaN heterostructures is dependent on several factors, such as the design of the epitaxy layers, the quality of the substrate growth, the doping concentration, the Al composition %, and the thickness of the AlGa_N epilayer.

Typically, one method to achieve E-mode type behavior is by reducing the gate to channel distance using the gate-recess etching technique [31] or by reducing the thickness of the AlGa_N barrier layer growth [172]. The standard thickness of the AlGa_N layer is approximately 20 to 25 nm. As the AlGa_N thickness reduces, the overall induced polarization effect is decreased.

Subsequently, the 2DEG channel density beneath the gate region is reduced and the threshold voltage is shifted positively [32]. However, using a thinner barrier increases the access resistance which eventually degrades the trans-conductance [168]. As for the gate-recess approach, a well-controlled etching method is lacking. The conventional gate-recess etching which uses ICP-RIE plasma dry etching, suffers from depth profile control as well as plasma damage which degrades the device performance. Lanford *et al.* proposed a post annealing treatment method [32] to recover the induced plasma damage attributed to the gate-recess approach. The proposed treatment requires an additional high temperature (>700 °C) pre-gate annealing using RTP which has to be done prior to gate metal deposition to avoid the degradation of the Schottky gate. Besides, an extra gate-level lithography step is needed to deposit the subsequent gate metal contacts. As a result, the gate recess etching and gate patterning steps are separated, leading to subsequent lithography and self-aligning issues. Moreover, the recess etching depth has to be precisely controlled in order to prevent the 2DEG channel from being over-etched at the AlGaIn/GaN interface. Owing to the issues mentioned above, high uniformity, controllability and reproducibility are still difficult to achieve.

E-mode HEMT can also be realized using fluorine-based plasma treatment. A fluorine plasma ion implantation technique coupled with post annealing recovery treatment at 400 °C is demonstrated by Y.Cai in 2005 [173]. This method has effectively shifted the threshold voltage from -4.0 V to +0.9 V. The overall mechanism is to implant negatively charged fluorine ions into the AlGaIn layer to shift the threshold voltage positively. Fluorine ions, which have strong electronegativity by nature, contribute immobile fixed negative charges

to the AlGaN barrier layer which result in the depletion of electrons in the 2DEG channel as well as in the conduction band modulation. Owing to these combined effects, the threshold voltage is being shifted to the positive region. The fluorine is incorporated into the AlGaN barrier through CF₄ plasma treatment using the RIE, but with different timing. Similarly, Hongwei Chen reported a threshold shift from -1.9 V to +0.6 V by implanting Fluorine ions into the gate region using the Varian CF3000 implanter at a high energy of 25 keV and a F⁺ ions dose of 5.0 x 10¹² cm⁻² [29].

However these fluorine implantation methods have several drawbacks. Firstly; (i) Fluorine dosage is hard to control, leading to difficulty in repeatability as high energy fluorine can penetrate deep into GaN and buffer layers; (ii) Implantation is being done using a non-uniform low power plasma which leads to device-to-device variation across the wafer, and finally; (iii) The thermal stability and plasma induced damage which degrades the channel mobility [174]. The plasma power is limited to 250 W to prevent the Fluorine from penetrating into the 2DEG channel and degrading the channel mobility [175]. In addition, post annealing treatment is required to recover the induced plasma damage and the performance of such fabricated E-mode device is moderate [176].

More recent works reported the usage of the metal insulator semiconductor (MIS) gate structure to shift the threshold towards the positive region [176, 177]. As conventional Schottky gate GaN HEMT devices suffer from high gate leakage current due to lower turn-on voltage, researchers have looked into incorporating dielectrics layers such as Al₂O₃, LaLuO₃ (LLO), and HfO as gate insulators. These gate insulator layers, treated with Fluorine ions,

have successfully suppressed the gate leakage, in addition to shifting the threshold voltage positively. Other reported techniques are p-type AlGa_xN cap [178] and InGa_xN cap [179]. As each method has its own benefits and drawbacks, a consistent and standardized method of fabricating enhancement mode device is still lacking.

5.3 Experimental Details

In this section, all the AlGa_xN/GaN HEMTs are fabricated on 150 mm diameter thin silicon-on-insulator (111) substrates. The Al_xGa_{1-x}N/GaN-based heterostructures are grown on 150 mm diameter float zone SOI (111) substrates using the metal organic chemical vapour deposition (MOCVD) method. The SOI (111) substrates, with a thin top Si over layer of about 30 - 35 nm and buried oxide thickness of about 70 - 75 nm, are prepared on handle Si substrates of thickness 650 - 675 μm (the starting Si resistivity is ~2500 Ω.cm) using the separation by implantation of oxygen (SIMOX) process. About 100 nm of AlN buffer is first grown on top of the thin SOI over layer, followed by ~2.1 μm of intermediate AlGa_xN/GaN superlattice layers. Next, ~1.0 μm carbon-doped semi-insulating GaN is overgrown followed by the heterostructure active layers which consist of a thin 1.0 nm AlN spacer, ~20 - 25 nm Al_xGa_{1-x}N barrier layer and a thin ~1.5 nm GaN cap layer.

All the HEMTs are fabricated using the Au-based process as reviewed earlier in Chapter 3. In order to study the effect of Germanium diffusion, Ge-doped HEMT samples and control samples are fabricated concurrently. The control samples HEMTs are fabricated using the Au-based process without any Ge doping at the gate area which denotes the typical depletion-mode

AlGaIn/GaN HEMT behavior. As for Ge-doped HEMTs, a thin 10 nm of Germanium layer is deposited at the gate area after source/drain metal contact (Ti/Al/Ni/Au) formation via e-beam evaporation followed by a RTP annealing step to diffuse Ge into the AlGaIn barrier layer.

The carrier confinement and the impact of Ge diffusion are investigated using high frequency gate-to-channel capacitance voltage (C-V) analysis. Secondary Ion Mass Spectrometry (SIMS) analysis is used to confirm the diffusion of Ge towards the AlGaIn barrier layer. DC characterizations are done on both control and Ge-doped samples to study the impact of Ge diffusion on the devices' electrical performance. The threshold voltages for both samples are extracted using the linear transconductance method. Next, a design of experiment is carried out by annealing the Ge-doped HEMTs at different temperatures to study the effect of temperature on the threshold voltage shift.

5.4 Device Fabrication

As mentioned earlier, the control samples are fabricated using the Au-based AlGaIn/GaN HEMT process flow as reviewed in Chapter 3. As for the Ge-doped samples, the fabrication flow is similar but with an additional gate-level lithography to deposit a thin 10 nm Ge layer. Fig 5.1 shows the optical micrograph of the fabricated AlGaIn/GaN HEMT after Ge (gate-region) and source/drain metal annealing process while Fig 5.2 illustrates the Ge-diffused HEMT fabrication process flow.

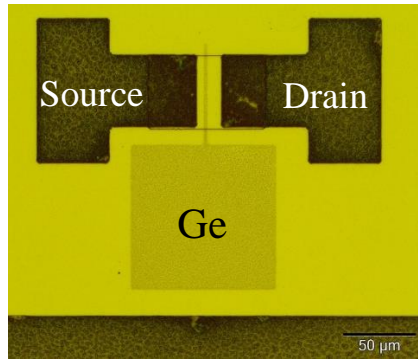


Fig 5.1: Optical micrograph of Germanium Diffused AlGaIn/GaN HEMT after Source/Drain annealing at 825 °C prior to Gate metal deposition step.

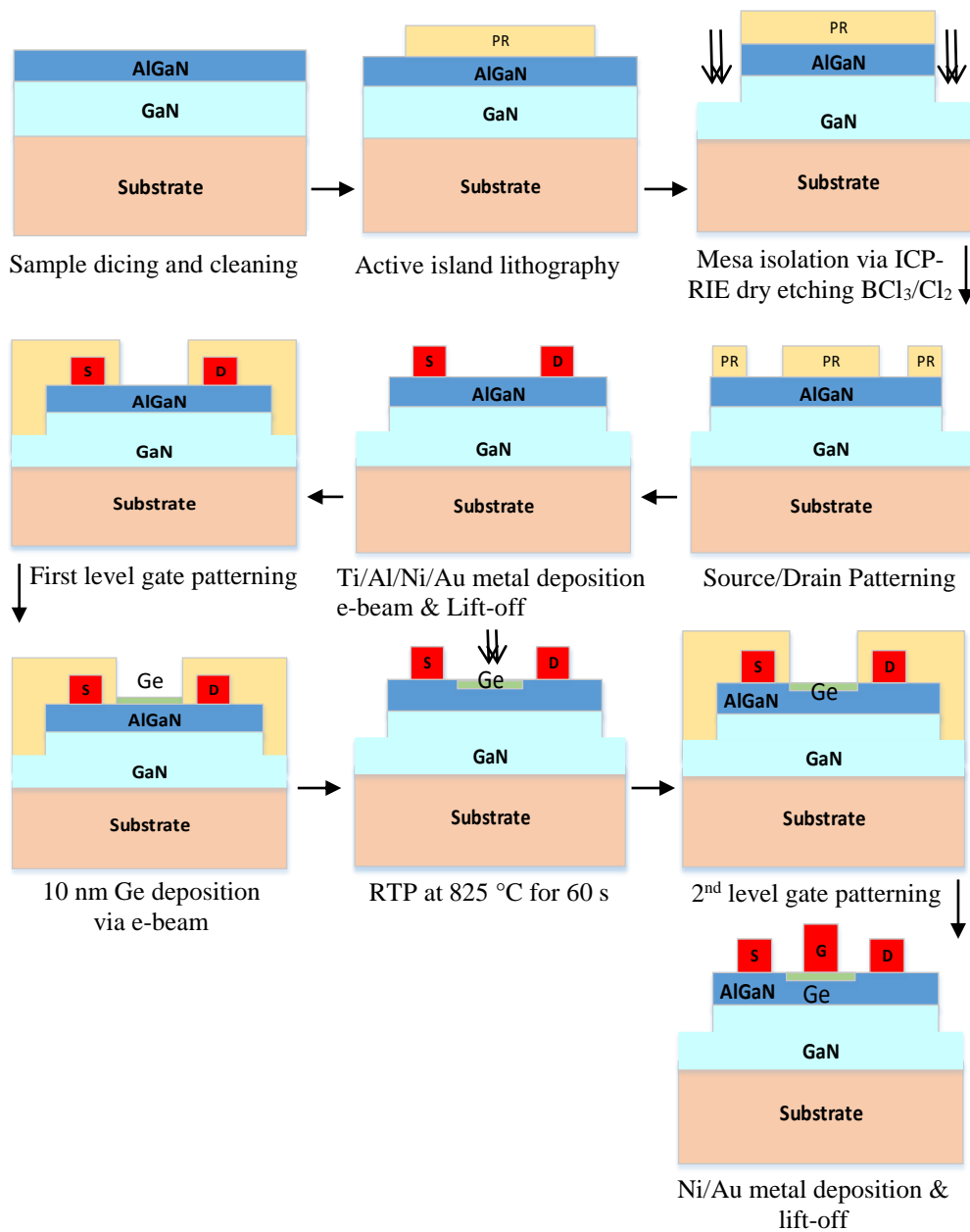


Fig 5.2: Schematic illustration of the main process flow of Ge-diffused (gate-region) AlGaIn/GaN Heterostructure High Electron Mobility Transistors (HEMT).

5.5 Mechanism Overview of Germanium Diffused AlGaN/GaN HEMT

In this report, the effect of using Germanium doping at the gate region in order to shift the threshold voltage positively is being investigated. The group IV element, germanium, is predominantly a n-type donor impurity with respect to the AlGaN semiconductor barrier layer. During the source/drain high temperature annealing step, germanium will be diffused into the AlGaN barrier at the gate region as illustrated in Fig 5.3. We proposed that the diffused Ge will compensate a certain degree of positive sheet charges induced by the Al on the AlGaN surface, which reduces the polarization effect. The reduced polarization at the AlGaN/GaN heterointerface leads to a lower 2DEG carrier concentration. In addition, the effective AlGaN barrier thickness is also reduced slightly due to the Ge diffusion into the gate region. Hence, due the combined effect of both lower 2DEG carrier concentration and effectively thinner AlGaN barrier layer, the threshold voltage is shifted positively.

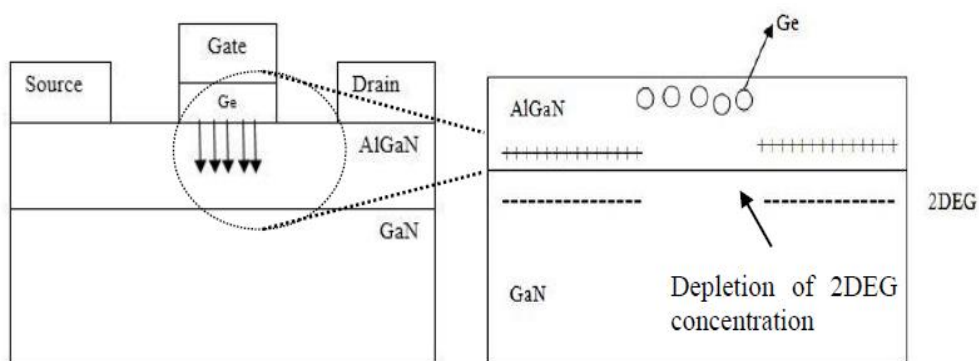


Fig 5.3: Schematic representation of Germanium diffusion at the gate region of AlGaN/GaN heterointerface after source/drain annealing step. Diffused Ge compensate the positive sheet charges at the AlGaN surface leading to the depletion of the 2DEG channel at the AlGaN/GaN interface and thus lowering the 2DEG electron concentration.

5.6 Results & Discussion

5.6.1 C-V Analysis of Germanium Diffusion

The capacitance-voltage (C-V) measurement is a good gauge to study the effect of Ge diffusion as well as the quality of the 2DEG structure at the AlGaIn/GaN interface. With the usage of Keithley 4200 SCS parameter analyzer, two terminals C_{LF} and C_{HF} are probed to the source/drain and gate contacts to measure the C-V at a high frequency of 1 MHz. The amplitude of the AC signal is kept at 30 mV to fulfill the small signal conditions. The typical C-V profile is influenced by the slow electron traps or interface states which responds to the small AC signal. C-V measurements are thus performed at 1 MHz to eliminate the traps effect as they are unable to follow the AC signal at high frequencies [180].

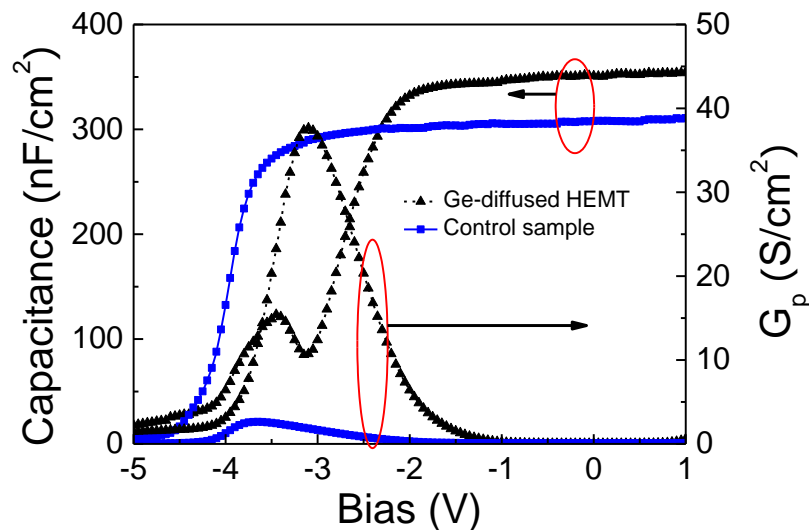


Fig 5.4: High Frequency 1 MHz Capacitance-voltage (C-V) and Conductance-voltage (G-V) measurements of both Ge-diffused HEMT and control HEMT (without Ge) samples.

From Fig 5.4 above, it is observed that the C-V curve profiles for the Schottky gate on AlGaIn/GaN heterostructures for both the Ge-diffused and the

control (without Ge) samples, are similar to that of a typical metal insulator semiconductor structure with a significant long plateau region at the end. The plateau's existence clearly reflects on the presence of the 2DEG channel at the AlGa_N/Ga_N interface. The large band gap property of AlGa_N acts as an insulator where the 2DEG is formed in the Ga_N region at the AlGa_N/Al_N/Ga_N interface. At positive bias, the electrons are accumulating at the AlGa_N/Ga_N interface and therefore the capacitance voltage behaves like a parallel plate capacitor. This carrier confinement beneath the AlGa_N/Al_N interlayers which has high electron concentration is responsible for the constant flat capacitance region over a large range of bias, as shown in Fig 5.4. It is observed that the plateau region for the Ge-diffused HEMTs is shorter as compared to that of the control sample due to the lower sheet carrier concentration after Ge diffusion. This correlates with the findings by Osvald [145] who reported that a higher sheet carrier concentration leads to a longer plateau region. As proposed earlier in the mechanism overview, during the source/drain annealing at 825 °C, Ge diffuses into the AlGa_N barrier region beneath the gate area. Ge tends to compensate the positive sheet charge induced in the AlGa_N barrier and hence reduces the polarization effect. This leads to a lower 2DEG carrier concentration at the AlGa_N/Ga_N interface. Hence, lower 2DEG carrier concentration coupled with thinner effective AlGa_N barrier layer due to Ge diffusion, shorten the flat capacitance region of the Ge-diffused HEMTs, as shown in Fig 5.4. As a result, the pinch-off voltage is shifted to the right, towards the positive region for Ge-diffused HEMTs.

The maximum capacitance, C_{\max} of the Ge-diffused HEMTs is higher due to the lower effective AlGa_N barrier thickness after Ge diffusion, compared

to the control samples without any Ge doping. The C-V slope for both samples are similar, indicating that the doping level at the GaN layer is not affected. A minimum capacitance at a voltage bias of -4.65 V for the control sample is observed at the onset of depletion and inversion region. As for the Ge-diffused devices, an anomalous hump is observed at the C-V characteristics. The capacitance decreases from the constant plateau region with the increase of negative gate bias due to the depletion of the AlGaIn/GaN layer. The negative applied bias eventually drifts the electrons away from the AlGaIn/GaN interface until a minimum capacitance is observed. The first minimum is first observed at a bias of -3.15 V followed by a hump at -3.45 V before reaching the final minimum capacitance. We proposed that this hump phenomenon might be attributed to the combination effect of interface state density and charge buildup at the band offset regions for these voltages. More analysis will be performed and discussed in another section to study the validity of the hump existence in the Ge-diffused HEMTs.

The deposited Ge at the gate using the e-beam evaporator is of 10 nm thick. The distribution of Ge inside the AlGaIn barrier layer is determined using the secondary ion mass spectrometry (SIMS) in a time-of-flight spectrometer (ToF SIMS IV from ION-ToF GmbH) through the detection of negative ions. The sputtering beam used is Cs 1 keV of 10 nA current whilst the pulsed analysis beam is Bi 25 keV of 0.5 pA current. During the spectral measurement, the sputtering rate was approximately 3.6 nm/min. The first 3 nm depth of the SIMS data is influenced by the experimental limitations. The ToF-SIMS analysis of the Ge and oxygen profiles for both samples are shown in Fig 5.5 (a) and (b) below. From the SIMS analysis of the Ge profile, a noticeable higher

intensity count of Ge is observed for Ge-diffused HEMTs for the first 20-30 nm of depth, which represents the GaN cap layer and the AlGa_N barrier region. Ge diffused into the GaN/AlGa_N interface and a thin Ge cap layer remained. It is suggested that the remaining Ge at the top of the GaN/AlGa_N layer modifies the band structure as illustrated in Fig 5.6.

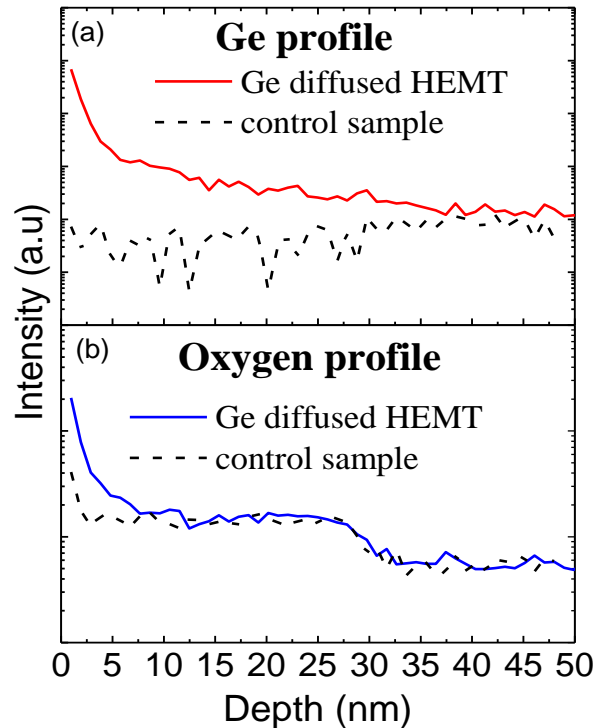


Fig 5.5: Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) analysis of (a) Germanium and (b) Oxygen diffusion profile at the AlGa_N/GaN interface layer after annealing at a temperature of 825 °C for 60 s for both Ge-diffused and without Ge (control sample) HEMTs. Solid line represents the Ge deposited sample while dashed line is the control sample without any Ge doping. Sputtering rate was 3.6 nm/min hence the depth of 50 nm corresponds to the scan time of 14 min.

The diffused Ge introduces n⁺ doping at the GaN cap/AlGa_N layer which causes a threshold voltage shift towards the enhancement region. The presence of a lower band gap Ge layer on the GaN cap induced a large conduction band offset at the Ge/GaN interface as illustrated in Fig 5.6. As the bias is swept from positive to negative, electrons start to get depleted at the metal/semiconductor interface. However the large conduction band offset (~1.6

eV) created a barrier which piles up the electron up to a certain bias range at the Ge and GaN cap interface. Attributed to the charge build up, there is an increase in capacitance, thus forming the anomalous hump at a bias of -3.45 V, as shown earlier in the C-V curve in Fig. 5.4. As the negative bias is increased further, the electrons eventually obtain sufficient energy to overcome this barrier offset and the depletion width increases, hence the capacitance value is reduced to a minimum.

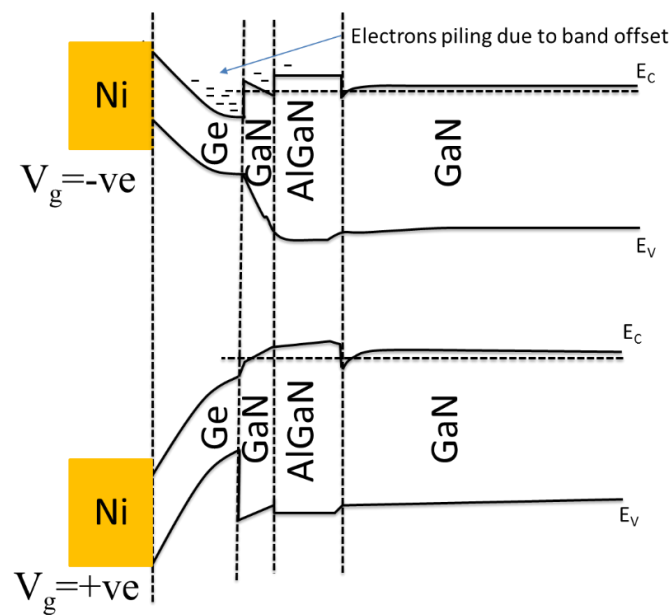


Fig 5.6: Band bending illustration of the AlGaIn/GaN heterostructure due to the presence of Ge layer at positive and negative gate bias. Electrons piling can happen due to the large conduction band offset region at the Ge/GaN/AlGaIn interface.

As proposed earlier, the hump formation might be due to the charge buildup effect due the large conduction band offset at the Ge/GaN cap interface and the influence of interface state density. It is important to study the defect levels in the AlGaIn barrier to understand possible barrier degradation after Ge diffusion. Hence further capacitance-voltage (C-V) and conductance-voltage (G-V) frequency dispersion analysis are used to study the interface state density, D_{it} . The C-V and G-V measurements of both samples for frequencies

ranging from 10 kHz to 1 MHz are shown in Fig 5.7 and Fig 5.8. From Fig. 5.7 (b) a strong frequency dispersion is observed for the Ge-diffused HEMTs which might indicate a high interface state density (D_{it}). However, the G-V frequency dispersion analysis is a more sensitive method in determining the trap density, compared to C-V frequency dispersion. Fig 5.8 (a) and (b) shows the G-V characteristics of the control sample and Ge-diffused HEMTs at the depletion region respectively.

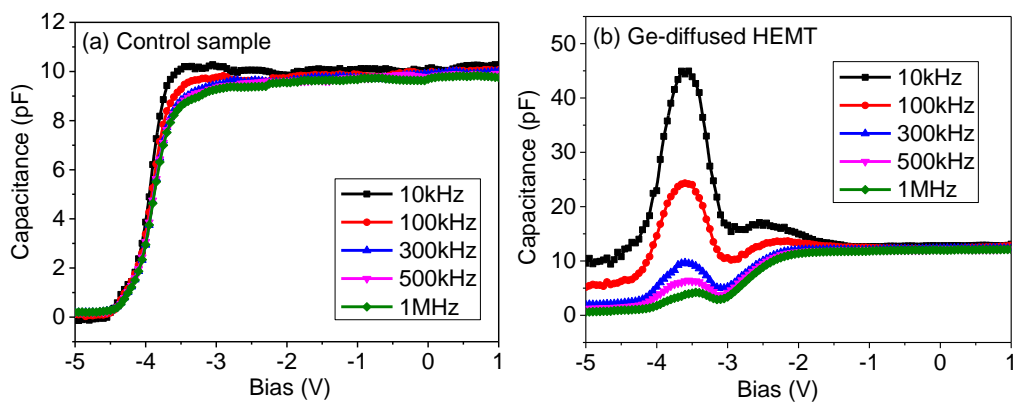


Fig 5.7: C-V frequency dispersion characteristics of (a) control sample (b) Ge-diffused HEMT sample for frequencies ranging from 10 kHz to 1 MHz.

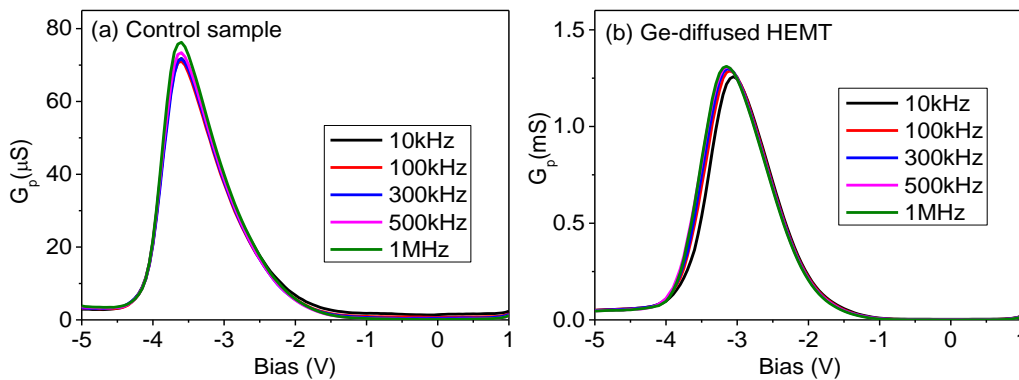


Fig 5.8: G-V frequency dispersion characteristics of (a) control sample (b) Ge-diffused HEMT sample for frequencies ranging from 10 kHz to 1 MHz.

Depletion charges are the interfacial 2DEG at the AlGa_N/Ga_N and Ge/Ga_N cap interface. The electron confinement observed in Ge-diffused HEMT sample is due to the Ge/Ga_N cap conduction band offset, which is

inclined to contain higher interfacial carrier concentration than the control sample. The higher density gives rise to a stronger G-V peak intensity (~2 order higher than control sample) at the depletion region of Ge-diffused HEMT as shown in Fig 5.8 (b). The high interface state density (D_{it}) might be responsible for the frequency dispersions of the CV-GV characteristics, hump formation in C-V and higher G-V peak. However, the conductance method is a more sensitive method and the interface state density is extracted using the technique recommended by E. H. Nicollian and Goetzberger which is capable of detecting interface state densities as low as $10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ [87]. Both G-V characteristics revealed a very weak dispersion which indicates the presence of moderate level D_{it} .

The density of interface states (D_{it}) and the interface trap time constant (τ) are extracted from the G_p/ω against ω plot using the AC conductance technique reported by E. H. Nicollian [87]. D_{it} and τ are extracted using equation (5-1) and (5-2) as follows:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau} \ln[1 + (\omega\tau)^2] \quad (5-1)$$

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{max} \quad (5-2)$$

Several interfaces such as Metal/GaN, AlGaN/GaN are present in Schottky diodes for both the Ge-diffused HEMT and the control HEMT samples. The peak in the G_p/ω versus ω plot is caused by the presence of interface traps attributed to these interfaces. The D_{it} value achieved for the control sample is $\sim 2.7 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and a higher value of $4.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ is obtained for the Ge-diffused HEMT samples which are similar to the reported values by Freedman et al. [181]. The extracted interface trap time constant (τ) obtained

for both samples are about $\sim 3.5 \times 10^{-5}$ s. However, both D_{it} values are lower than the commonly reported value of AlGaIn/GaN HEMTs without a gate insulating layer, which is in the order of $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ [182]. Therefore, instead of the high interface state density, D_{it} , we believe that the piling of electrons at the Ge/GaN interface is responsible for the hump formation and related C-V dispersion.

Apart from Ge diffusion, several other factors which may cause V_{TH} shifting as well as high D_{it} , such as O_2 diffusion into AlGaIn and surface roughness, are studied. To determine the presence of O_2 diffusion, ToF SIMS analysis was done, as shown earlier in Fig 5.5 (b) along with the Ge profile. The SIMS O_2 depth profile shows that negligible O_2 diffusion is observed during annealing for both control and Ge-diffused HEMT samples.

Atomic force microscopy (AFM) is used to investigate the surface morphology after Ge deposition, annealing and pre gate cleaning. The AFM results of the surface topology after Ge deposition and pre gate cleaning are shown below in Fig 5.9 (a) and (b). AFM is done using a scan area of $1.0 \mu\text{m} \times 1.0 \mu\text{m}$. Study shows that the surface roughness increases significantly after the annealing step due to the agglomeration of Ge on top of the GaN/AlGaIn layer. However, the roughness reduces after pre gate cleaning (acetone, IPA and HCL chemistry) as shown in Fig 5.9 (b). The slight reduction of surface roughness after pre-gate cleaning is probably contributed by the chemical etching of Ge. Such surface morphology change observed for Ge-diffused HEMT sample might be responsible for the higher D_{it} value as reported earlier.

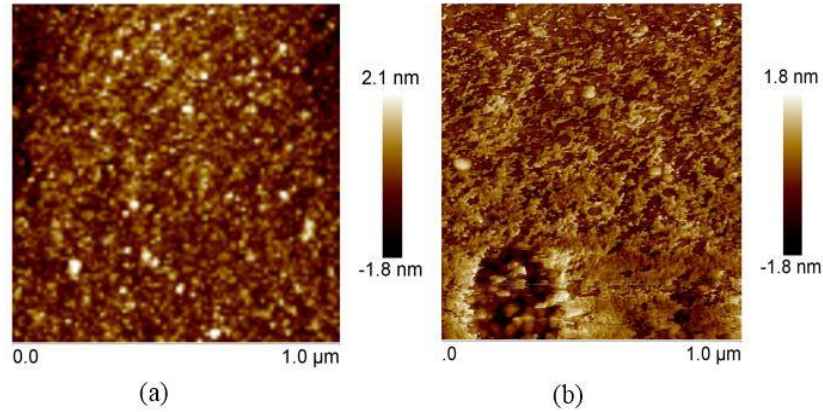


Fig 5.9: AFM study on surface morphology (a) after Ge deposition and (b) pre gate cleaning on the sample surface

5.6.2 DC Electrical Characterization

DC characteristics of the Ge-diffused HEMT samples, compared to the control sample, are studied to investigate the impact of the Ge diffusion on the device's electrical performance. The DC output I_{DS} - V_{DS} characteristics of both Ge-diffused and control samples are shown in Fig 5.10 (a). A noticeable lower drive current is observed for the Ge-diffused HEMTs compared to the control samples. This is due to the diffusion of Ge into the AlGaN barrier, compensating the positive dipoles, which reduces the 2DEG concentration and hence, resulting in a lower drive current. The transfer characteristics I_{DS} - V_{GS} and transconductance (g_m) are shown in Fig 5.10 (b). The threshold voltage for both Ge-diffused HEMTs and control samples are extracted using the transconductance linear extrapolation method. The values are similar to the pinch-off values obtained from the high frequency C-V plots. The drain current and transconductance values are observed to be lower for the Ge doped HEMT compared to the control sample. The channel mobility in the Ge/AlGaN interface are expected to be lower than the conventional 2DEG AlGaN/GaN

channel, which reduces the I_{DS} and g_m . As Ge acts as a donor in GaN-based material, it might increase the gate leakage after diffusion due to defects in the AlGaN/GaN barrier. The presence of the lower band gap Ge cap at the top coupled with Ge diffusion into GaN/AlGaN layers are expected to yield higher gate leakage characteristics. The gate to drain leakage characteristics for both samples are shown in Fig 5.10 (c). The reverse gate leakage current for the Ge diffused samples are slightly higher compared to the control sample without any Ge doping at the gate. On the other hand, the forward current for both types of samples is comparable.

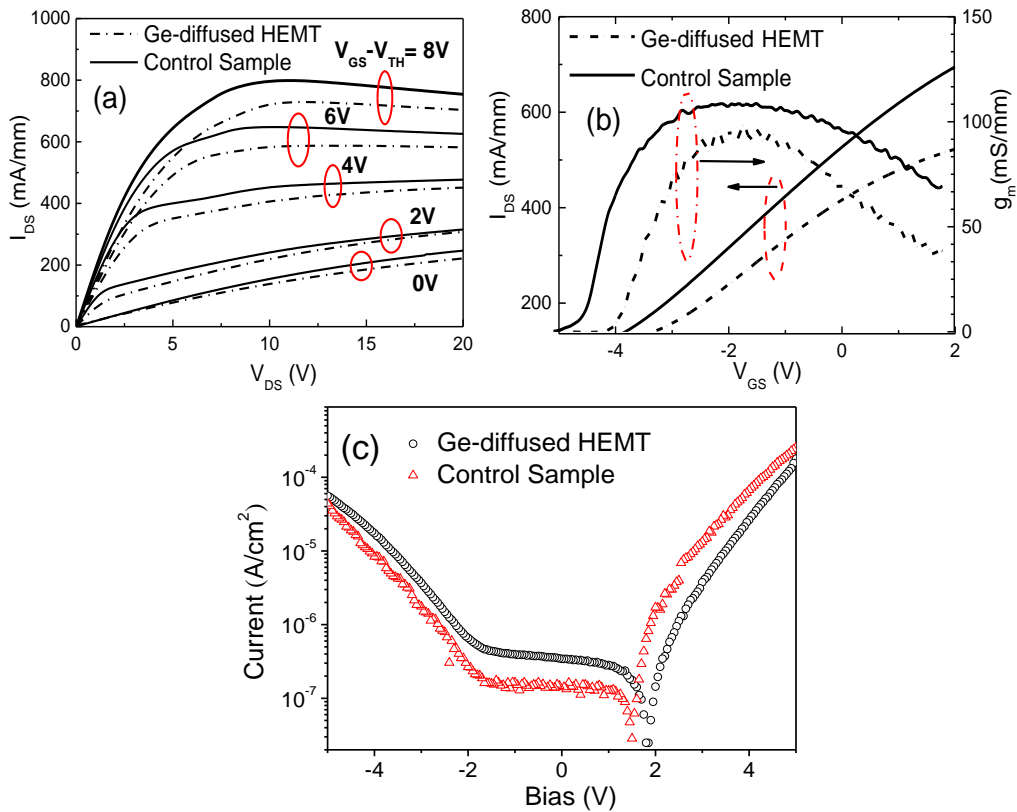


Fig 5.10: (a) I_{DS} - V_{DS} characteristics, (b) I_{DS} - V_{GS} and Transconductance g_m ($V_{DS} = 8V$) characteristics and (c) Gate-to-Drain leakage characteristics of Ge-diffused HEMTs and control HEMTs.

5.6.3 Effect of Annealing Temperature on the Ge Diffusion

The impact of Ge diffusion in the GaN/AlGaN epilayers and the corresponding V_{TH} shift have been investigated in the previous section. In this section, the main focus is to study the V_{TH} shift and the gate leakage of the Ge-diffused AlGaN/GaN HEMTs as a function of annealing temperature. The HEMT devices with Ge-deposited at the gate region are annealed at different temperatures ranging from 800 °C to 900 °C with the annealing duration fixed at 60 s. The temperature range is constrained by the optimum Ohmic contact annealing process to maintain the device's performance.

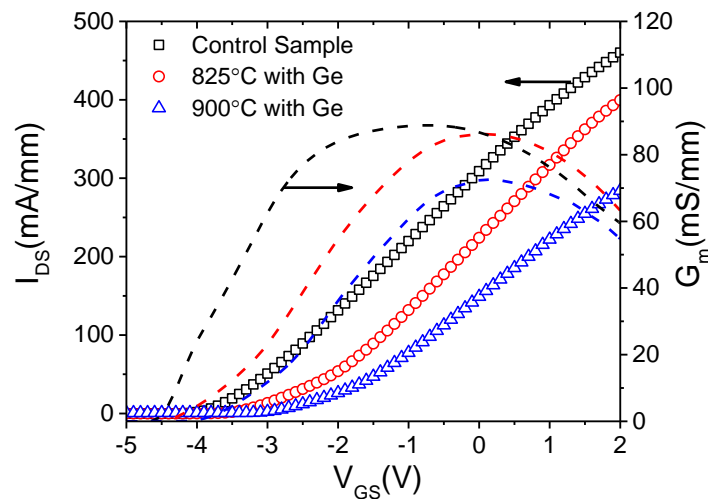


Fig 5.11: I_{DS} - V_{GS} and g_m characteristics of Ge-diffused HEMTs annealing at different temperatures compared to control samples. Respective threshold voltage is extracted using the transconductance linear extrapolation method; Control Sample HEMT $V_{TH} = -3.52$ V, Ge-diffused HEMT (825 °C) $V_{TH} = -2.37$ V, Ge-diffused HEMT (900 °C) $V_{TH} = -2.0$ V.

Fig 5.11 shows the transfer and transconductance characteristics of the Ge-diffused HEMT annealed at 825 °C and a higher 900 °C, compared to the control sample. In comparison to the control sample which is annealed at the same temperature at 825 °C, the additional Ge diffusion shifted the threshold voltage from -3.52 V to -2.37 V. A larger threshold voltage shift to -2 V is

observed for the Ge-diffused HEMT samples annealed at a higher temperature of 900 °C. Therefore at a higher annealing temperature, the threshold voltage shifts further towards the positive region at the expense of lower g_m and I_{DS} . The degradation in peak transconductance and maximum drain current might be attributed to the higher level of Ge diffusion into the AlGaIn barrier layer. At higher annealing temperatures, a higher level of Ge might diffuse further into the AlGaIn barrier layer. This will deplete more 2DEG carrier and thus cause a larger threshold voltage shift towards the enhancement mode direction. This is in agreement with the earlier observation in Fig 5.10 (b) which is due to the depletion of 2DEG concentration.

Fig 5.12 shows the linearity of the threshold voltage shift (ΔV_{TH}) as a function of annealing temperature. At 800 °C, an average voltage shift of 0.915 V towards the positive region is obtained for Ge-diffused HEMT, compared to the control sample without any Germanium doping. As temperature is increased to 825 °C and 900 °C, an average voltage shift of 1.138 V and 1.50 V are obtained respectively.

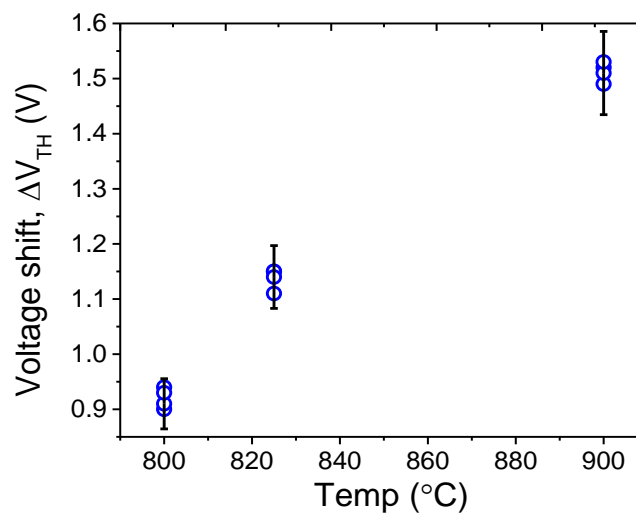


Fig 5.12: Average threshold voltage shift ΔV_{TH} due to the diffusion of Germanium after annealing at temperatures 800 °C, 825 °C and 900 °C respectively. Threshold voltage shift increases with annealing temperature.

It was mentioned earlier that Ge-diffused HEMT will exhibit higher gate leakage characteristics compared to normal AlGaIn/GaN HEMT. As shown in Fig 5.13, the reverse gate leakage current at $V_{GS} = -15$ V has increased by more than 3 orders for annealing at 900 °C compared to 800 °C and 825 °C. Hence, there are tradeoffs in increasing the annealing temperature to shift the threshold voltage further towards the enhancement region. The annealing temperature range is constrained by the optimum source/drain Ohmic formation as the Ge is diffused concurrently during the source/drain annealing treatment. Temperatures which are too low or too high will degrade the contact resistance of the devices. Higher annealing temperature reduces the drain current and transconductance of the device, in addition to degrading the gate's Schottky leakage current.

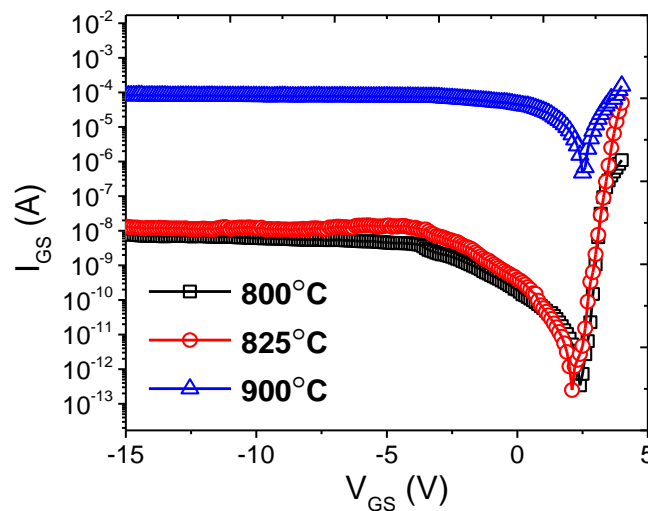


Fig 5.13: Reverse gate leakage current characteristics of Germanium diffused AlGaIn/GaN HEMT at different annealing temperatures. Device annealed at 900 °C showed reverse gate leakage current which is almost 3 orders higher.

In order to overcome these limitations, we proposed a double annealing step where Ge is first deposited and annealed at high temperatures to allow it to diffuse into the AlGaIn barrier layer. This is then followed by the deposition of

source/drain contact with a second annealing step for optimum Ohmic contact formation. Finally, the gate metal stack is deposited. Hence, the source/drain contact is not degraded by the high temperature annealing process of diffusing Ge into the gate region. In order to overcome the gate leakage, a metal-insulator-semiconductor (MIS) structure is proposed before the gate metal deposition. However, such fabrication process is more complex and involves additional reticle masks. The effect of double annealing on the incorporation of Ge at the gate region is also unknown. Future works have to be done to optimize the concept of Ge diffusion in order to shift the threshold voltage without degrading the gate, as well as the source/drain Ohmic contact.

5.7 Chapter Summary

In summary, the effect of germanium doping at the gate electrode area on the electrical properties of AlGa_N/Ga_N HEMT on Ga_N SOI (111) substrates is demonstrated and studied. A positive threshold voltage shift of 1.15 V after annealing at 825 °C is observed which is ascribed to the Ge diffusion. The formation of hump is observed from the capacitance-voltage characteristics, which is explained by the confinement of electrons at the Ge/AlGa_N interface which causes n-type doping at the Ga_N/AlGa_N layer. Germanium diffused AlGa_N/Ga_N HEMT also shows a reduction in drain current and transconductance due to the reduction of the 2DEG carrier concentration. The impact of annealing temperature on the Ge diffusion on AlGa_N/Ga_N HEMT is also being studied. Results showed that higher temperatures can lead to a larger positive threshold voltage shift. However the threshold voltage tuning is limited to the degradation of leakage current characteristics of the gate electrode as well

as the optimum contact resistance of the Ohmic contacts. Hence with the current process design of AlGaIn/GaN HEMT, higher temperature annealing is not an effective way to realize a fully enhancement mode HEMT. To date, the Ge-diffused HEMT samples are not fully enhancement mode HEMT, even though a positive shift in threshold voltage is observed. It is worth emphasizing that this is the first study performed on the feasibility of Ge dopants towards the aim of developing a fully enhancement mode AlGaIn/GaN HEMT. Current experimental studies suggested that the Germanium doping method is more suitable for threshold voltage tuning, rather than achieving a fully enhancement mode HEMT. More detailed studies are needed to fully understand the diffusion mechanism, defect rate reduction, and the proper placement of Ge dopant (similar to V_{th} implant, pocket implant in Si technology) in order to develop a fully enhancement mode AlGaIn/GaN HEMT.

CHAPTER 6: FABRICATION & CHARACTERIZATION OF GOLD-FREE ALGAN/GAN HEMTS USING TI/AL/NIV OHMIC CONTACTS

6.1 Introduction

As discussed earlier in Chapter 3, the typical metallization scheme for Ohmic formation on AlGaN/GaN HEMTs is Ti/Al/X/Au-based. X denotes the transition metals such as Ni, Pt, Cr, Ti, and Mo which serve as a diffusion barrier between Al and Au [183]. Source/Drain is formed via Ti/Al/Ni/Au while gate Schottky is formed using Ni/Au. Au is important as it provides low contact resistance while preventing the oxidation of the Ti/Al-based metal stacks [60]. In general, AlGaN/GaN HEMTs fabricated with Au-based contacts yield an average contact resistance, R_C of $< 1.0 \Omega \cdot \text{mm}$ [35, 58, 60]. However, such metallization schemes require very high annealing temperature ($>800 \text{ }^\circ\text{C}$) for Ohmic alloy formation. Apparently, this increases the thermal budget as well as induces rough surface morphology due to the formation of AuAl₄ alloy at high temperature which has been discussed earlier [34]. Rough surface morphology leads to further reliability and scalability issues which are not favorable for high frequency microwave operations. In addition, high temperature processing restricts the implementation of gate first process. Hence, a stable Ohmic contact of low processed temperature is desirable as it gives more flexibility in the

device processing where gate Schottky and Ohmic contacts can be annealed together.

To integrate GaN-based HEMTs into the Si CMOS technology, Au-based contacts are prohibited due to the cross-contamination [184]. Au which is highly diffusive, introduces deep level traps in silicon which leads to the device performance degradation [33]. Hence, it is desirable to showcase an Au-free CMOS compatible metallization scheme for AlGaN/GaN HEMT coupled with low processing temperature, good surface morphology and low contact resistance.

Scheme	Metal Stack	R_c (Ω.mm)	Process Condition	Ref.
Au-based	Ti/Al/Ni/Au	0.17	900 °C, 30 s	[185]
	Ti/Al/Ni/Au	0.12	825 °C, 30 s	[57]
	Ti/Al/Ni/Au	0.45	825 °C, 60 s	[186]
	Ti/Al/Ni/Au	1.8	825 °C, 30 s	[149]
Au-free	Ta/Si/Ti/Al/Ni/Ta	0.24	800 °C, 30 s	[187]
	Ti/Al/Ni/Pt	0.60	975 °C, 30 s	[188]
	Ta/Al/Ta	1.40	575 °C, 30 s	[150]
	Ti/Al/W	0.49	870 °C, 30 s	[189]
	Ti/Al/TiN	0.62	550 °C, 90 s	[190]
	Ti/Al/Ti/TiN	1.25	550 °C, 90 s	[191]
	Ti/Al/W	0.93	875 °C, 90 s	[192]
	Ti/Al	0.76	550 °C, 60 s	[193]
	Ti/Al/NiV	0.80	500 °C, 30 s	This work

Table 6.1: Benchmarking summary of the contact resistance values (with processing conditions) of our Ti/Al/NiV metal scheme as compared to both Au-based and Au-free metal schemes on AlGaN/GaN HEMTs.

Recently, several Au-free metallization schemes have been reported; utilizing metals such as W [189, 194], TiN [190], Cu [195], Ta [187] and Pt [33, 188] to replace the top Au layer. Table 6.1 shows the comparison between several reference works using both Au-based and Au-free metal contact schemes including the Ti/Al/NiV Ohmic contacts developed in this study. Liu *et al.* demonstrated a Ti/Al/Ni/Pt Ohmic metal scheme annealed at 975 °C for 30 s in N₂ atmosphere resulting in a contact resistance (R_C) of ~0.6 Ω.mm [185]. Similarly, Ta/Si/Ti/Al/Ni/Ta Ohmic metal stack annealed at 800 °C for 30 s in a N₂ environment with a $R_C \sim 0.24$ Ω.mm was demonstrated by S. Arulkumaran *et al.* [187]. However, it is noteworthy to emphasize that the low contact resistance are usually achieved at the expense of high temperature (≥ 800 °C) annealing process. As discussed earlier, high temperature processing increases the thermal budget, introduces rough surface morphology and induces metal spiking which degrades the device breakdown [196]. In addition, it also limits the implementation of gate-first Si CMOS process. Recently, Z. Liu *et al.* demonstrated a low R_C of 0.3 Ω.mm using Ti/Al metal stack with annealing temperature between 450-550 °C [197]. However, the major drawback of the method is it requires a highly doped n+ GaN cap layer which introduces high gate leakage current. In addition, a very good vacuum RTP system is required as Ti/Al is susceptible to oxidation without the top metal cap layer. A low-temperature (550 °C) Au-free Ti/Al/TiN metal scheme is also reported recently [190] with a low R_C of 0.6 Ω.mm. Nevertheless, the low contact resistance performance is achieved by partially-recessed source/drain patterns which increase the process complexity. Thus, in order to avoid process complexity for the fabrication of Al_xGa_{1-x}N/GaN HEMTs on 200-mm Si(111), it is desirable to

showcase low-temperature non-recess Au-free source/drain contacts with an $R_C < 1.0 \Omega \cdot \text{mm}$.

Among various metal alloys, nickel-vanadium (NiV) alloy is typically used in the electroplating industry due to its high corrosion resistance and slow oxidation rate. NiV is proposed to promote intermetallic reaction at low temperature while providing a smooth surface morphology [198]. To our best knowledge, there has been limited work in studying the NiV alloy as cap layer for Ohmic metal stack formation in the AlGaN/GaN HEMT structures.

Thus in this section, an Au-free HEMTs fabrication method using Ti/Al/NiV as Ohmic contacts on AlGaN/GaN 2DEG heterostructures grown on 200 mm Si (111) substrates is demonstrated. A comparable contact resistance, R_C of $0.8 \Omega \cdot \text{mm}$ with specific contact resistivity, ρ_c of $6.33 \times 10^{-6} \Omega \cdot \text{cm}^2$ are achieved by a low temperature RTA process at 500°C without any recess etching. We believe that the development of such low-temperature non-recessed Au-free Ohmic metallization scheme may find its applications in GaN-on-Si processing with the possibility of integration with a self-aligned process.

6.2 Experimental Details

In this study, The $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMT structures are grown on a 200 mm diameter p-type Si (111) substrate. The epitaxial growth of HEMT layers is carried using an AIXTRON CCS metal organic chemical vapor deposition (MOCVD) system. The $3.8 \mu\text{m}$ thick HEMT structure comprised of a $\sim 380 \text{ nm}$ thick AlN nucleation layer, three step-graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ intermediate layers, and a GaN buffer of $\sim 1.6 \mu\text{m}$ thick. The top layers consist of a $\sim 300 \text{ nm}$ undoped GaN channel, a thin AlN spacer ($\sim 1.0 \text{ nm}$), an $\text{Al}_{0.23}\text{Ga}_{0.76}\text{N}$ barrier

layer (~20 nm), and a top undoped GaN (~3.0 nm) thin GaN cap layer. The Al composition of ~23-24% in the barrier across the wafer is determined by the reciprocal space mapping in a high-resolution x-ray diffraction setup. Hall measurements on the samples show an average sheet resistance of ~430 ohm/sq with a sheet carrier density of about $1.1 \times 10^{13} \text{ cm}^{-2}$.

The overall Au-free HEMTs fabrication in this study is similar to the process flow previously reviewed in Chapter 3. The main difference would be the Source/Drain (Ti/Al/NiV) and Gate (Ni/Al) contacts which are formed using Au-free contacts. The schematic illustration and top view optical micrograph of the Au-free AlGaN/GaN HEMT device structure are as shown in Fig. 6.1 (a) and (b), respectively.

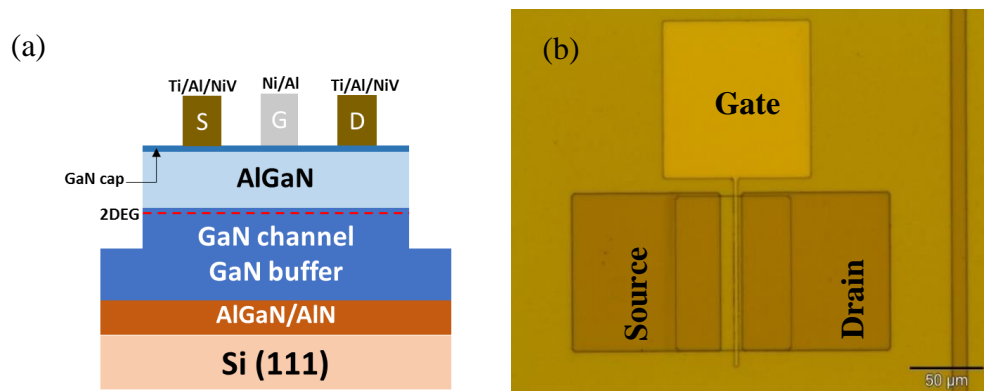


Fig 6.1 (a) Schematic cross-section and (b) Optical micrograph of fabricated AlGaN/GaN HEMTs using Ti/Al/NiV as Ohmic contacts and Ni/Al as Schottky gate.

In order to achieve the optimum Ohmic performance, the Ti/Al/NiV metal stack has been optimized in terms of Ti/Al relative thickness ratio, annealing temperature and RTP duration. Earlier in Chapter 3, studies show that the relative Ti/Al thickness has a huge impact towards the Ohmic contact formation at the top surface. Both Ti and Al will react with GaN during the RTP process to form a thin interfacial layer of TiN, AlN or AlTi₂N while generating N vacancies which acts as n-type dopants [58, 66]. In this study, the

Ti/Al ratio is varied between 0.05, 0.10, 0.15, and 0.167 while fixing the top NiV cap layer thickness at 70 nm to investigate the optimum Ti/Al relative thickness which exhibits the lowest contact resistance. Next, the thickness-optimized Ti/Al/NiV metal stack undergo annealing at different temperature between 400 °C to 700 °C for 30 s in 1500 sccm flow of N₂ ambient. Finally, the optimum annealing duration window (30-60 s) is investigated. Table 6.2 summarizes the overall design of experiment (DOE) in optimizing the Ti/Al/NiV metal stack in terms of different metal thicknesses and processing conditions (RTP annealing temperature and duration).

Experiment	Metal Thickness (nm)			Temp (°C)	Time (s)
	Ti	Al	NiV		
Ti/Al Relative Thickness	15	300	70	500	30
	20	200	70	500	30
	30	200	70	500	30
	20	120	70	500	30
Annealing Time	20	200	70	500	30
	20	200	70	500	45
	20	200	70	500	60
Annealing Temp	20	200	70	400	30
	20	200	70	450	30
	20	200	70	475	30
	20	200	70	500	30
	20	200	70	600	30
	20	200	70	700	30
	20	200	70	750	30

Table 6.2: Design of experiment in optimizing various parameters for optimum contact resistance for Ti/Al/NiV metal stack (Ti/Al ratio, annealing temperature, annealing time).

The DC characteristics of the fabricated AlGaIn/GaN HEMTs are studied using the optimized Ti/Al/NiV metal scheme which gives the lowest contact resistance. The contact surface morphology, interfacial metal distribution and microstructural changes of the Ti/Al/NiV contacts after annealing are investigated using atomic force microscopy (AFM) and STEM-EDX (Scanning transmission electron microscope - energy dispersive X-ray spectroscopy) analyses.

6.3 Results and Discussion

6.3.1 Optimization of Ti/Al/NiV Ohmic contact

As mentioned earlier, the Ti/Al/NiV ohmic contacts are optimized in terms of Ti/Al relative thickness, annealing temperature and duration in order to achieve the optimum contact resistance. The linear Transmission Line Method (TLM) has been employed for extracting the Ti/Al/NiV contact resistance and specific contact resistivity. Fig 6.7 (a) shows the TLM test structure fabricated using (Ti/Al/NiV) with square pads ($W=L=100\ \mu\text{m}$) and varying gap spacing ($d=13\ \mu\text{m}, 17\ \mu\text{m}, 21\ \mu\text{m}, 25\ \mu\text{m}, 29\ \mu\text{m}$ and $37\ \mu\text{m}$). Mesa isolation etching is essential to prevent unwanted current spreading confining the current flow within the mesa height of conductive epitaxial layer. In this section, I-V characteristics at different gap spacing of the TLM structures are measured using 4200-SCS Keithley Parameter Analyzer. Based on the current-voltage (I-V) characteristics and extracted R_C , the optimum processing conditions are determined.

Fig 6.2 (a) and (b) shows the I-V characteristics of TLM contact pads

fabricated using different Ti/Al thickness (15/300 nm, 20/200 nm, 25/200 nm, and 20/120 nm) while fixing NiV cap layer thickness (70 nm), and the annealing condition at 500 °C and 30s. Non-linear I-V characteristics are observed for Ti/Al thickness (15/300 nm-ratio 0.05) and (20/120 nm-ratio 0.167) as shown in Fig 6.2 (b) with very low current. Linear Ohmic characteristics are observed for both Ti/Al thicknesses (20/200 nm-ratio 0.10) and (25/200 nm-ratio 0.15), with 0.10 ratio giving the steepest slope indicating the lowest resistance among both. At this ratio, the top Al layer is consumed by reacting with Ti to form Al_3Ti at low temperature ~250 °C, along with an excess remaining Ti layer in contact with the GaN cap/AlGaN layer [199]. It is proposed that Ti will react with the thin GaN cap and AlGaN barrier layer at 500 °C by catalyzing effect due to the presence of NiV alloy layer. The lower Ti/Al thickness ratio of 0.05 (15/300 nm) sample is Al rich and attributed to the fixed annealing temperature and time, the whole Ti layer is consumed first with some Al remained unreacted resulting in a non-Ohmic behavior. In contrast, for the higher Ti/Al thickness ratio of 0.167 (20/120 nm), the stack is Ti-rich and the Al layer require a higher thermal budget (temperature and duration) to achieve complete reaction.

In subsequent studies, the Ti/Al thickness ratio is thus fixed at 0.10 (20/200 nm) for further annealing temperature optimization to achieve the lowest contact resistance. Fig 6.3 (a) shows the I-V characteristics after annealing at different temperature from 400 °C to 700 °C while (b) shows the extracted contact resistance for respective temperatures. Non-linear behavior is observed for annealing temperature of 400 °C and 700 °C respectively. As discussed, at temperature below 450 °C, the total thermal budget is not

sufficient for the formation of TiN layer which generates nitrogen vacancies at the interface acting as n-type dopants. Linear Ohmic I-V characteristics are obtained at temperatures between 450 °C to 600 °C annealing for 30 s, with highest slope attained at 500 °C indicating the lowest contact resistance. Table 6.3 shows the summary of contact resistance extracted for samples annealed cumulatively at different temperatures.

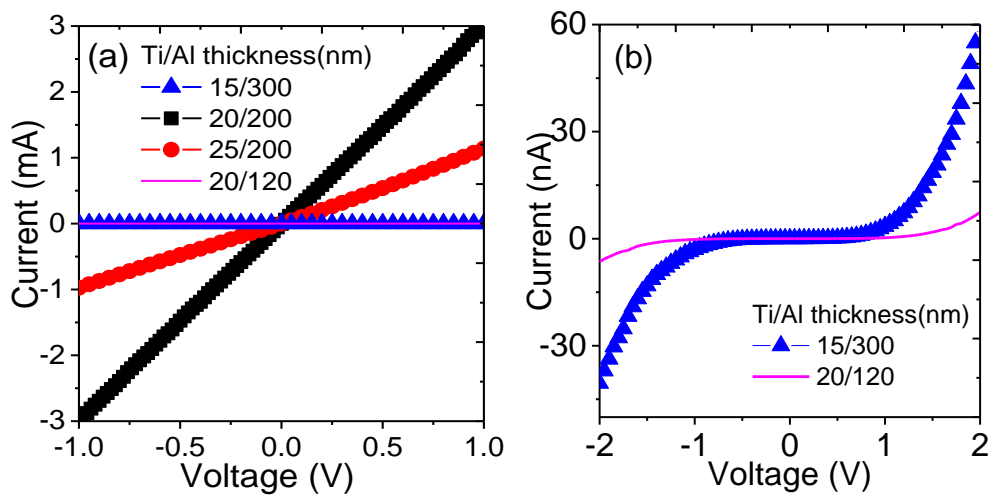


Fig 6.2: (a) I-V characteristics measured between two consecutive TLM contact pads (Gap spacing = 13 μm) with different Ti/Al relative thickness (b) Higher resolution I-V characteristics of Ti/Al thickness of 15/300 nm and 20/120 nm.

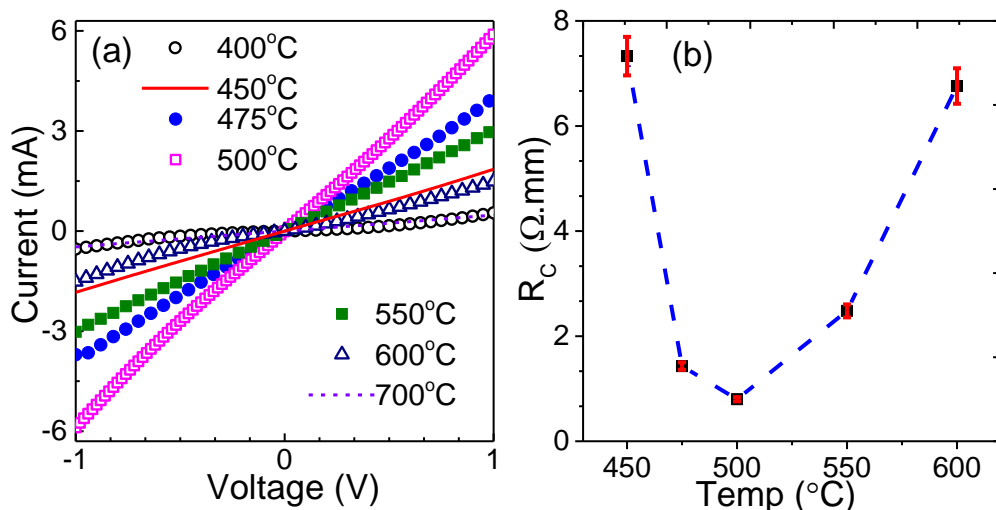


Fig 6.3: (a) I-V characteristics of Ti/Al/NiV contacts at different annealing temperatures and (b) contact resistance, R_C as a function of annealing temperature.

Metal Thickness (nm)			Temp (°C)	Time (s)	Contact resistance (Ω.mm)	Specific contact resistivity (Ω.cm ²)
Ti	Al	NiV				
20	200	70	400	30	-	Non-linear
20	200	70	450	30	7.33	1.466 x 10 ⁻³
20	200	70	475	30	1.43	2.41 x 10 ⁻⁵
20	200	70	500	30	0.80	6.33 x 10 ⁻⁶
20	200	70	550	30	2.48	7.73 x 10 ⁻⁵
20	200	70	600	30	6.76	1.285 x 10 ⁻⁴
20	200	70	700	30	-	Non-linear

Table 6.3: Summarized accumulated results of Ti/Al/NiV contacts annealed at different temperatures between 400 °C to 700 °C with fixed duration of 30 s.

At higher temperature (>600 °C), the non-linear behavior of the *I-V* characteristics with higher contact resistance are probably due to the micro-structural changes at the metal-semiconductor junction. Atomic Force Microscopy (AFM) is employed to study the micro-structural changes and the surface topographies of the Ti/Al/NiV contacts after annealing. AFM scans of the contacts annealed at 500 °C and 700 °C are shown in Fig 6.4 (a) and (b) respectively. With 10 μm × 10 μm sampling size, the root-mean-square (RMS) surface roughness increases from 5.8 nm at 500 °C to 12.4 nm at 700 °C annealing for 30 sec. Such substantial surface roughness evolution is caused by the microstructural changes of the epitaxial semiconductor film underneath the metal layer which affects the 2DEG channel resulting in a non-linear *I-V* characteristics leading to an increase in resistance at higher processing temperatures.

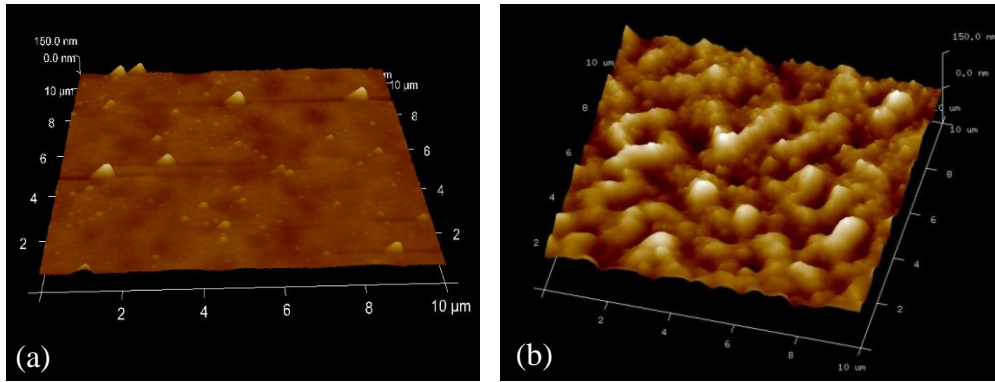


Fig 6.4: 3D-AFM images of Ti/Al/NiV contacts annealed at (a) 500 °C and (b) 700 °C for 30 s respectively. The sampling size is 10 μm × 10 μm.

Fixing the temperature at 500 °C, the TLM structures undergo different annealing duration from 30-60 s to study the best processing time window. Annealing duration of 30 s gives the optimum contact resistance with good surface morphology. The decrease in slope with increasing annealing duration in Fig 6.5 (a) indicates the increase in resistance. Prolonged annealing might lead to the out diffusion of Al while Ti/Al layers are more susceptible to oxidation at higher RTP duration [200]. Fig 6.5 (b) shows the extracted contact resistance as function of RTP duration.

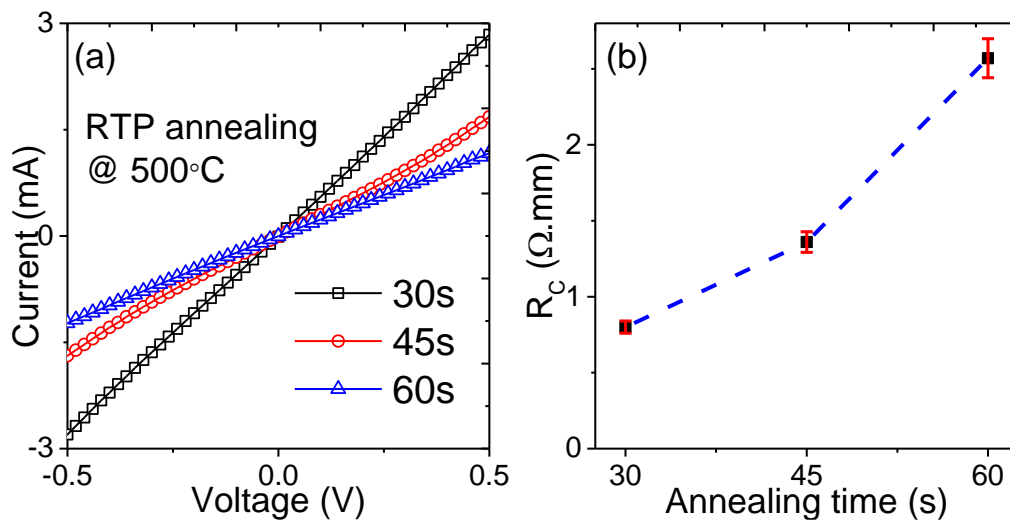


Fig 6.5: (a) I-V Characteristics and (b) R_C as function of annealing time of Ti/Al/NiV TLM structures annealed at 500°C.

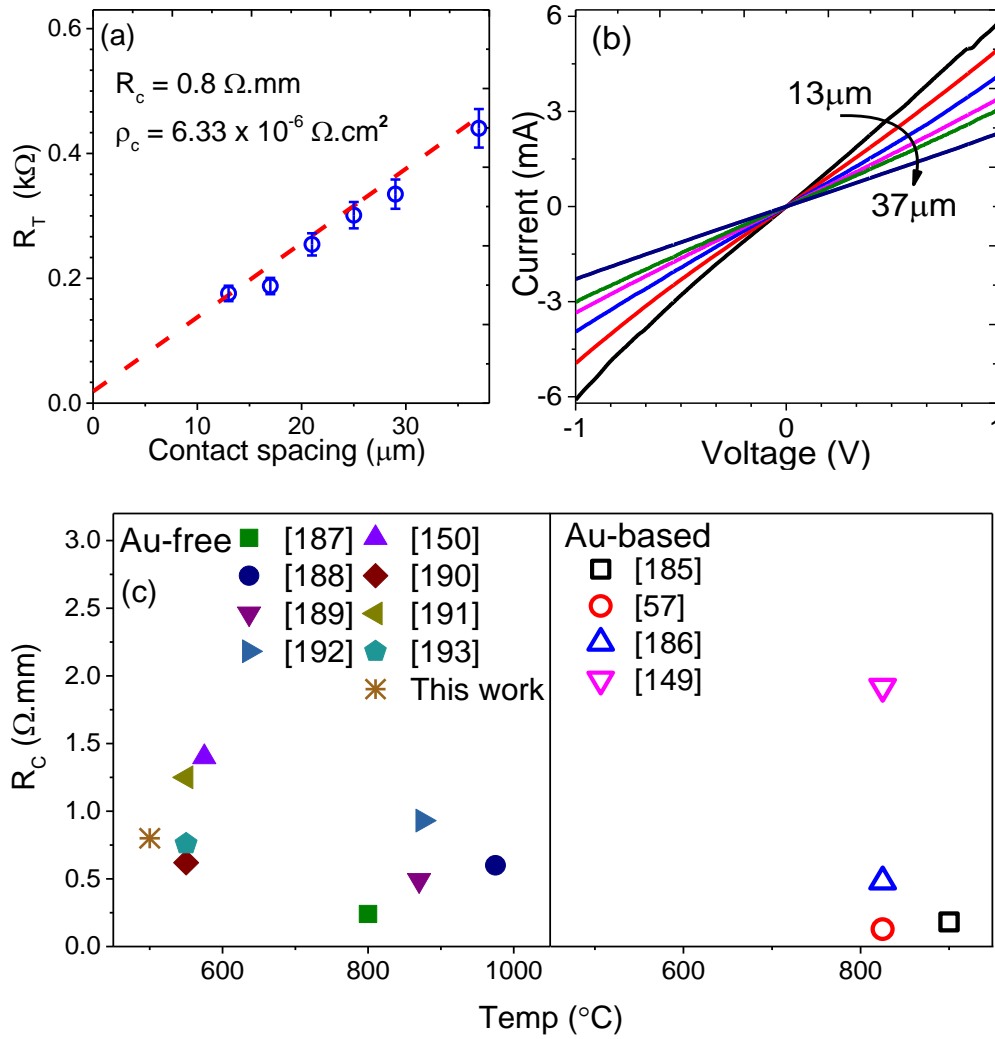


Fig 6.6: (a) Total resistance as function of contact spacing (b) I-V characteristics of each contact spacing of the optimized Ti/Al/NiV TLM structures annealed at $500^{\circ}C$ and 30 s (c) Bench mark of contact resistance R_C against annealing temperature of our optimized Ti/Al/NiV contacts with reported Au-free and Au-based metal schemes.

Based on the conducted experiments, the Ti/Al/NiV metal stack with the lowest contact resistance are found to be optimized with a Ti/Al relative thickness ratio of 0.10 (20/200 nm), with RTP annealing at $500^{\circ}C$ for 30 s. The contact resistance R_C and specific contact resistivity, ρ_C are extracted with value of $0.8 \Omega \cdot mm$ and $6.33 \times 10^{-6} \Omega \cdot cm^2$ respectively as shown in Fig 6.6 (a). I-V characteristics of each contact gap spacing of the optimized Ti/Al/NiV TLM structures are shown in Fig. 6.6 (b). We believed that a well-controlled precise

recess etching at the Source/Drain area will further improve our contact resistance. By etching the GaN cap layer and reducing the AlGaN barrier thickness, a better conduction path between the metal and 2DEG channel can be provided [201]. However, it is noteworthy that even without source/drain recess-etch, the contact resistance value achieved by the optimized Ti/Al/NiV metal scheme is comparable to other reported Au-free and Au-based schemes as shown in Table 6.1. A benchmarking of contact resistance values against annealing temperature of our optimized Ti/Al/NiV contacts with reported Au-free and Au-based metallization schemes is shown in Fig 6.6 (c).

6.3.2 Physical Characterization of Ti/Al/NiV Metal Scheme using AFM, STEM & EDX Analysis

In this section, the optimized Ti/Al/NiV contacts are studied using several physical characterizations which include AFM, STEM and EDX analyses. A rough comparison between the optical micrographs of the TLM test structures in Fig 6.7 show that (a) Ti/Al/NiV contact exhibits much smoother surface morphology than (b) Ti/Al/Ni/Au contact. It is well-known that Ti/Al/Ni/Au-based contacts are prone to rough surfaces due to the high temperature processing and the formation of AlAu₄ alloy [34]. Rough surface contacts are unfavorable for high frequency microwave applications due to non-uniform current distribution, along with poor line edge definition leading to scalability and reliability issues (gate-to-source/drain shorts) in GaN RF applications [61].

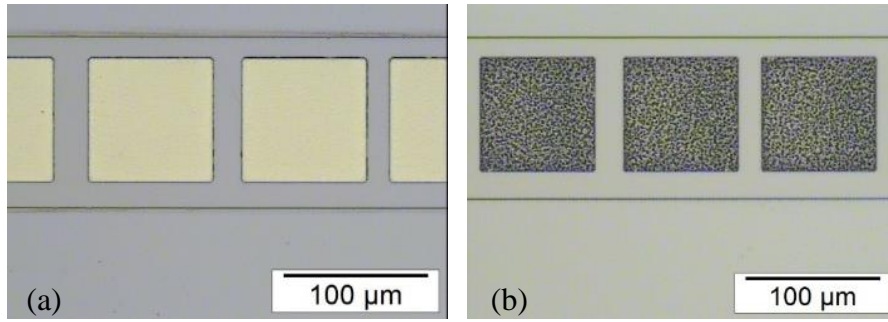


Fig 6.7: Optical micrographs of TLM test structures with (a) Ti/Al/NiV contact annealed at 500 °C 30 s and (b) Ti/Al/Ni/Au contact after annealing at 825 °C 60 s.

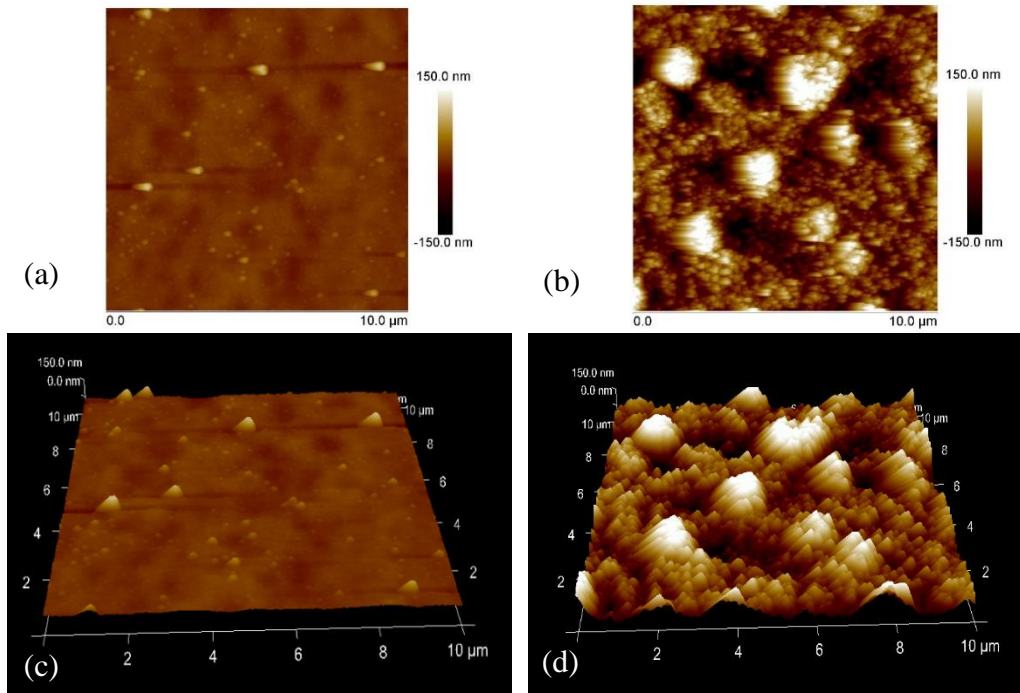


Fig 6.8: (a) 2D and (c) 3D-AFM images of Ti/Al/NiV (500 °C 30 s); (b) 2D and (d) 3D-AFM images of Ti/Al/Ni/Au (825 °C 60 s). Extracted RMS roughness of Ti/Al/NiV and Ti/Al/Ni/Au are 5.8 nm and 44.2 nm respectively (sampling size: 10 μm × 10 μm).

AFM scan is employed to extract the RMS surface roughness for both contacts studied above. Fig 6.8 shows the 2D and 3D-AFM scans of the optimized Ti/Al/NiV contacts and the standard Ti/Al/Ni/Au contacts after annealing process. With a sampling size of 10 × 10 μm, the extracted root-mean-square (RMS) surface roughness for Ti/Al/NiV and Ti/Al/Ni/Au contacts are 5.8 nm and 44.2 nm respectively. The low temperature processed Ti/Al/NiV

metal scheme shows a much lower RMS value in contrast to the Ti/Al/Ni/Au contacts. This can be attributed to the lower thermal processing and the absence of AlAu₄ alloy along with the catalyst effect of vanadium alloy [198].

Next, the interfacial elemental distribution and structural changes of optimized Ti/Al/NiV contacts (Annealing at 500 °C for 30 s) are investigated using high resolution transmission electron microscopy (HR-TEM) and Energy Dispersive X-Ray (EDX) Spectroscopy via a Titan 80-200kV Monochromated-Scanning TEM. The TEM lamella is prepared using a dual-beam Helios Nanolab 600 focus ion beam (FIB) system. The FIB cut location is taken across the source/drain contacts in order to study the Ti/Al/NiV metal stack structure.

Fig 6.9 (a) and (c) show the cross-sectional TEM images of the Ti/Al/NiV metal stack as deposited on top of the AlGaIn/GaN heterostructure after annealing. Smooth transition of metal semiconductor interface is observed from the TEM images. Intermixing of metal layers occurs during RTA and the distribution of each element is then investigated using the EDX probe. A 350 nm EDX line scan is performed along the solid orange line as indicated on Fig 6.9 (a) to study the elemental profile along the Ti/Al/NiV metal stack after RTA. One EDX spot is taken at every 5-nm step. The respective EDX elemental profile is shown in Fig 6.9 (b) where Ni and Al are distributed within the entire metal stack due to strong intermixing during annealing. The results show that Al diffuses toward the top of the metal stack while the stable V remained only at the top of the metal stack, acting as an oxygen diffusion barrier layer. As depicted in Fig 6.9 (b), a very low oxygen profile intensity is observed across the metal stack. This implies the effectiveness of the top NiV

cap in preventing oxygen diffusion during annealing, which mitigates the oxidation of the Ti/Al-based metal stack.

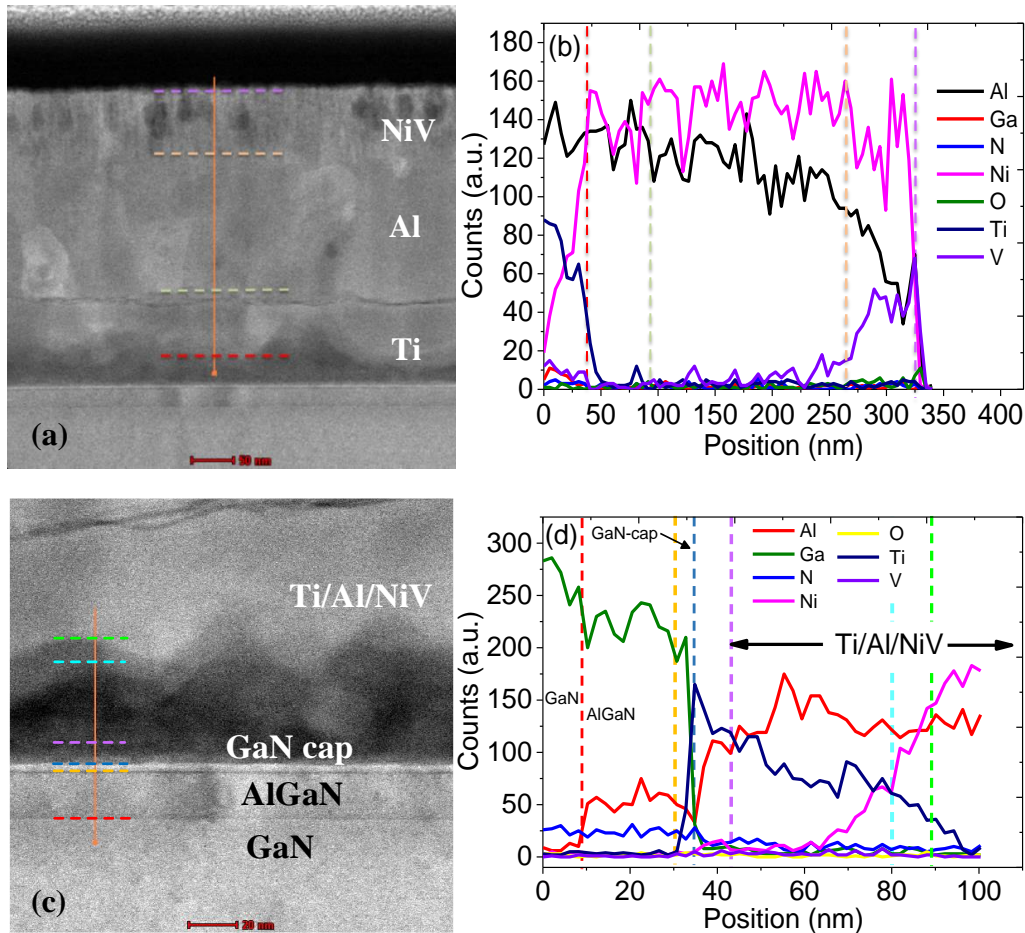


Fig 6.9: (a) The cross-sectional STEM image across the Ti/Al/NiV metal stack with EDX scan line of 350 nm and (b) EDX elemental profile corresponding to the 350 nm line scan (c) Cross-sectional STEM image across the Ti/GaN-cap/AlGaN/GaN interface with EDX scan line of 100 nm and (d) EDX elemental profile corresponding to the 100 nm line scan; The scan positions of the EDX profile with respective to the TEM images are as indicated with the dashed color lines.

A subsequent 100-nm interfacial EDX line scan across the Ti/Al/GaN-cap/AlGaN/GaN interfaces is performed along the vertical solid line as shown in Fig 6.9 (c). This analysis is performed to study the diffusion of metal into the GaN-cap/AlGaN barrier. The EDX spot is taken at a step size of 2 nm. From the EDX profile in Fig 6.9 (d), both Ti and Al diffuse into the top thin GaN cap layer with intermixing between GaN, Al and Ti. The presence of such complex

ternary or quaternary compounds of GaN, Ti and Al nitrides at the AlGaN/GaN/metal interface reduces the barrier height to GaN, which consequently led to the formation of low resistance Ohmic contact at source/drain as reported by L.S. Tan *et al.* [202].

6.3.3 Electrical Characterization of AlGaN/GaN HEMTs fabricated using Ti/Al/NiV Contact Scheme

Based on the optimized Source/Drain Ohmic contacts, the Schottky gate is formed using Ni/Al (20/200 nm) metal layers. Figure 6.10 (a) shows the I-V characteristics of the Ni/Al gate Schottky diode. Using the I-V method as reviewed in Chapter 3, the Schottky barrier height, ϕ_B and ideality factor, n are extracted to be 0.73 eV and 1.48 respectively which are comparable to several reported Ni contacts on n-type AlGaN/GaN structure [77, 203]. A higher ideality factor, $n > 1$ implies that the current transport mechanism is not purely dominated by thermionic emission instead a trap-assisted tunneling mechanism might be present at the metal/semiconductor interface [204]. Higher ideality factor might also be attributed to the presence of interfacial native oxide layer and barrier inhomogeneities [205]. The barrier height value (0.73 eV) is lower compared to the value reported by Z.H Liu *et al.* using a similar (Ni/Al) gate metal stack [188]. Such barrier height reduction might be attributed to the interface states at AlGaN/GaN barrier [206]. Compared to other conventional non-native substrates like SiC or sapphire, a higher density of vacancy-impurity complexes at the top AlGaN/GaN interfaces is common for such GaN-on-Si epitaxy.

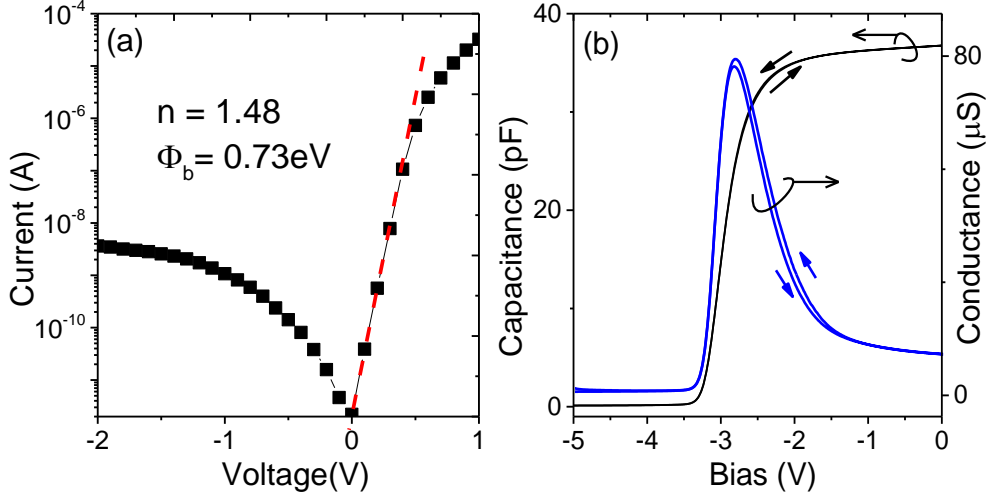


Fig 6.10: (a) I-V characteristics of Ni/Al Gate Schottky Diode on AlGaN/GaN HEMT and (b) Capacitance and Conductance-Voltage characteristics of AlGaN/GaN HEMT at high frequency 1 MHz.

Fig 6.10 (b) shows the capacitance-voltage and conductance-voltage characteristics of the fabricated AlGaN/GaN HEMT using the Ti/Al/NiV Ohmic contact scheme with Ni/Al Schottky gate. Minor hysteresis effect is observed when sweeping the gate bias from -5 V to 0 V and back to -5 V. The maximum accumulation capacitance of 36.7 pF at zero bias corresponds to the AlGaN barrier layer capacitance. At a deep reverse bias, the capacitance steeply decreases to nearly zero, indicating the 2DEG depletion at the AlGaN/GaN interface. At $V_G < -3.5$ V, a capacitance minimum is observed indicating that the 2DEG channel is fully depleted.

The interface traps density of the AlGaN/GaN interface is analysed using the frequency-dependent conductance method [92] with the following equations:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{\text{AlGaN}}}{G_m^2 + \omega^2 (C_{\text{AlGaN}} - C_m)^2} \quad (1)$$

$$D_{\text{it}} \approx \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{\text{max}} \quad (2)$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad (3)$$

where G_m and C_m are the measured conductance and capacitance using the equivalent parallel model; C_{AlGaN} is zero bias accumulation $\text{Al}_x\text{Ga}_{1-x}\text{N}$ capacitances; ω is frequency; A is gate area and q is electronic charge. The conductance, G_p/ω versus frequency ω plot at different gate biases and trap energy distribution of the as-measured interface state density, D_{it} and trap-time constant, τ_{it} are as shown in Fig 6.11 (a) and (b) respectively. As the gate bias increases from depletion to near accumulation, the peak intensity of the G_p/ω becomes larger and the corresponding D_{it} value increases. The increase of gate bias induces the 2DEG channel electron to transfer from the AlGaN/GaN interface to the Schottky gate. These electrons can trap at AlGaN defect sites. Such acceptor-type trap states are responsible for the higher G_p/ω intensity and D_{it} value. The extracted interface trap density of values $5 \times 10^{12} - 1.8 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ with corresponding time constant of 0.35 - 1.0 μs are not only comparable but also an order of magnitude lower than reported results with similar AlGaN/GaN HEMTs structure [88, 91]. The trap time constant reduces exponentially with increase of energy implying that the trap states are continuum in nature at the interface. This is in agreement with the reported findings where traps with higher energy levels usually take shorter time for trapping/de-trapping process [91].

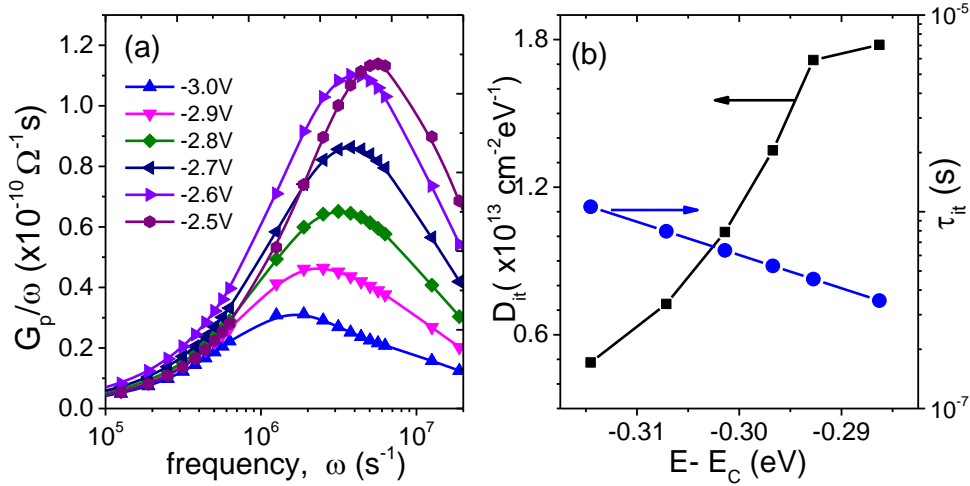


Fig 6.11: (a) Normalized Conductance G_p/ω versus frequency ω characteristics for different gate biases (b) Energy distribution of as-measured interface-trap density D_{it} and trap time-constant τ_{it} .

Next, the DC characteristics of the gold-free AlGaN/GaN HEMTs fabricated using the optimized Ti/Al/NiV contacts are studied. Fig 6.12 (a) and (b) show the DC output and transfer characteristics of the devices with gate width, $W = 100 \mu m$, $L_G = 2 \mu m$ and $L_{GD} = 3 \mu m$. Device shows good pinch-off performance at around -3 V with a maximum drain current, $I_{D_{MAX}} \sim 320$ mA/mm at $V_G = 2$ V. The maximum transconductance, $g_m \sim 88$ mS/mm at $V_{DS} = 6$ V. It is notable that the HEMTs demonstrate excellent I_{ON}/I_{OFF} ratio $\sim 3 \times 10^9$ with a subthreshold swing, SS of 71.42 mV/decade, which are comparable or even higher than the reported HEMTs [207, 208]. High I_{ON}/I_{OFF} ratio and low SS are favorable for high-speed power switching applications.

The fabricated HEMTs exhibit low gate leakage current performance at ON-state ($V_{DS} = 8$ V) with $I_G = 3.2 \times 10^{-6}$ mA/mm at $V_G = -20$ V as shown in Fig 6.12 (c). Such low leakage might be attributed to the lower thermal processing which is applied throughout the fabrication process of the AlGaN/GaN HEMTs. The gate leakage is expected to reduce further if a metal-insulator-semiconductor (MIS) type HEMT configuration is adopted. Such a

low-temperature Ohmic metal stack scheme would be a promising solution for CMOS type gate-first approach towards the development of low-cost $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ MISHEMTs.

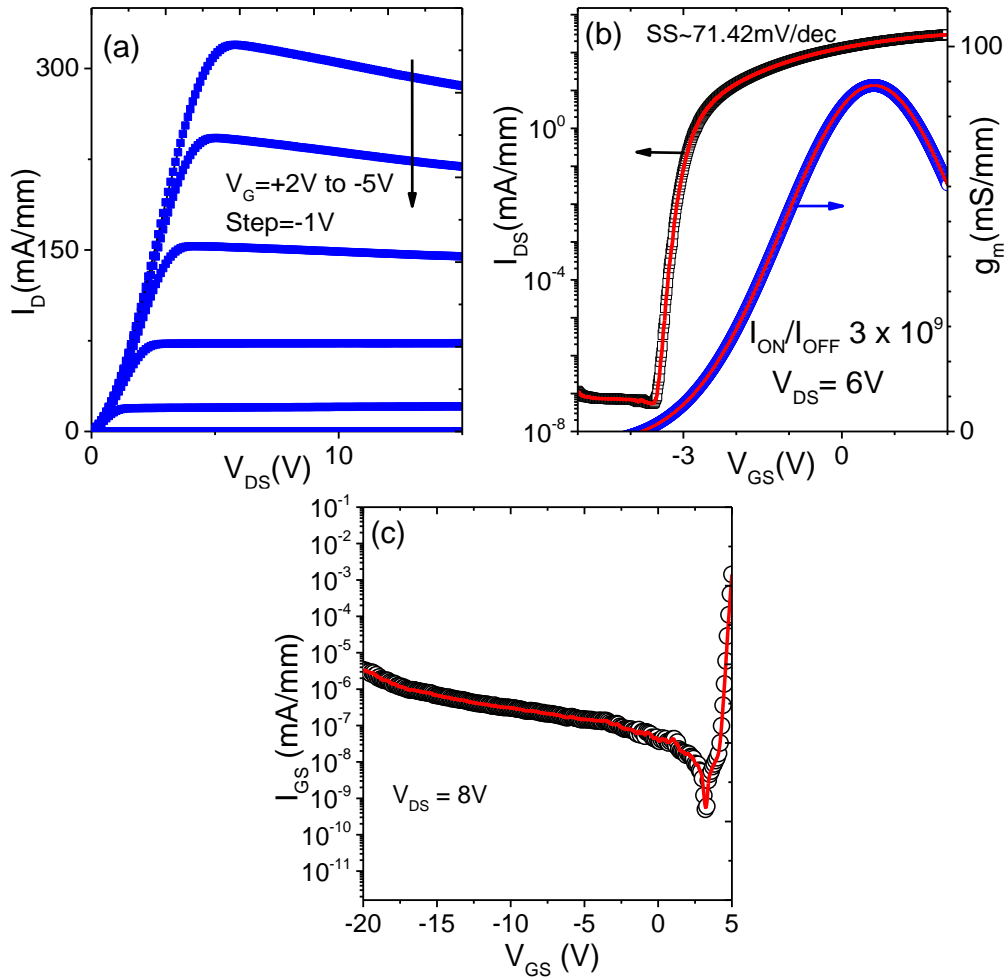


Fig 6.12: (a) DC output and (b) transfer characteristics of AlGa_xN/GaN HEMT fabricated using the Au-free Ti/Al/NiV metal contacts; (c) ON-state gate leakage current characteristics of AlGa_xN/GaN HEMT at $V_{DS} = 8V$.

6.4 Chapter Summary

In this chapter, a gold-free AlGaN/GaN HEMT using a novel Ti/Al/NiV Ohmic S/D contact and Ni/Al Schottky gate fabricated on a 200-mm Si (111) substrate is demonstrated. The Ohmic contact is optimized through variation of Ti/Al thickness ratio, annealing temperature and RTA time. An optimum contact resistance, R_C of $0.8 \Omega \cdot \text{mm}$ with specific contact resistivity, ρ_c of $6.33 \times 10^{-6} \Omega \cdot \text{cm}^2$ are achieved with Ti/Al/NiV (20/200/70 nm) metal stack annealed at 500°C for 30 s. The fabricated HEMTs exhibit excellent $I_{\text{ON}}/I_{\text{OFF}}$ ratio $\sim 3 \times 10^9$ and subthreshold swing, $SS \sim 71 \text{ mV/dec}$ with is desirable for fast switching power applications. Owned to the low thermal processing window, the HEMT devices demonstrate a very smooth Ohmic contacts surface with a lower OFF-state drain current. The metal interdiffusion and structural changes of the Ti/Al/NiV metal stack at the AlGaN interface after annealing are studied using the STEM and EDX analyses. From the EDX elemental profile, a very low oxygen intensity is observed across the metal layers indicating the NiV cap layer effectively prevents the oxidation of the Ti/Al metal stack during RTP annealing. We proposed that the formation of complex ternary or quaternary compounds of GaN, Ti and Al nitrides which reduces the barrier height to n-GaN is responsible for the Ohmic property behavior at low temperature. We believe that the development of such a low temperature Au-free metallization scheme will find its applications in GaN-on-Si integration with the possibility of a self-aligned gate approach where Gate and Source/Drain can be annealed together.

CHAPTER 7: $Al_xGa_{1-x}N/GaN$ MISHEMTS USING COMMON GOLD-FREE METAL STACKS & SINGLE MASK FOR SOURCE/DRAIN/GATE

7.1 Introduction

Numerous works highlighting the superior performance of AlGaN/GaN HEMT especially in high power, high frequency and low noise regimes have been published [209-211]. These are attributed to the material properties of GaN, such as high breakdown field, high carrier density and high mobility of the 2DEG channel. The performance of the AlGaN/GaN HEMT can be further improved through the scaling of gate length dimensions [212-214]. However, the performance of high frequency AlGaN/GaN HEMT is limited by the source-to-gate access resistance which degrades the transconductance and current gain cutoff frequency [215]. Several approaches have been reported in order to reduce these parasitic access resistance. Examples of these are Si ion implantation [216, 217], self-aligned gate [218], and multi-channel devices [219]. The ion implantation technique is effective in reducing the access resistance, however it is a complicated process and devices suffer from implantation damages.

From the fabrication point of view, access resistance can be reduced by scaling the source/drain to gate spacing which eventually improves the unity gain cutoff frequency, f_T . To restrict thermal-induced degradation, the Schottky gate is traditionally formed after the high-temperature source/drain (S/D)

Ohmic-contact annealing. However, controllability of the source-access resistance would become a major challenge for highly-scaled devices due to alignment issues. The minimum source-to-gate access distance is limited by the lithography tool's capability. Therefore, the most effective method for obtaining the minimum allowable spacing between the source/drain and gate is using the self-aligned gate first method [218, 220]. The self-aligned gate-first integration would be the most desirable since it is already a mainstream approach in Si CMOS technology. However, realization of such implementation into GaN HEMTs is difficult due to the high temperature Ohmic contact annealing ($> 800^{\circ}\text{C}$). Gate degradation and the likelihood of gate-to-drain/source shorts caused by the high thermal-budget Ohmic contact formation impede direct implementation of the gate-first approach in GaN HEMT fabrication [218]. Therefore, to reduce the parasitic inhomogeneities associated with numerous front-end process steps in addition to achieving higher device performance, a CMOS compatible low temperature self-aligned fabrication with gold-free metal stack is preferred.

Apart from access resistance, another performance limiting factor of typical Schottky gate AlGaIn/GaN HEMTs is the severe gate leakage current [36]. Device degradations attributed to high gate leakage are low $I_{\text{ON}}/I_{\text{OFF}}$ ratio, current dispersion and large Sub threshold Swing (SS) [221]. High gate leakage current limits the gate voltage swing and hence the maximum channel current [37]. Moreover, this reduces the gate-to-drain breakdown voltage, leading to further reliability concerns [38]. In order to reduce the gate leakage, AlGaIn/GaN MISHEMT structures are used. "MIS" denotes metal-insulator-semiconductor where a thin dielectric layer is inserted as a gate insulator

between the gate metal and the AlGaN barrier layer. MISHEMTs have higher RF output power attributed to improved voltage swing, leading to higher maximum drain current [222]. Apart from suppressing gate leakage, MISHEMT devices reportedly have improved noise performance too [38]. Taking into consideration the following properties of large band gap, high dielectric constant ϵ , and low interface state density, several dielectric materials have been investigated and reported as a gate insulator for AlGaN/GaN MISHEMT. Examples include HfO₂ [223], Al₂O₃ [37, 224, 225], ZrO₂ [95], SiO₂ [226], Si₃N₄ [227, 228] and Ga₂O₃ [229]. Among the dielectric materials, Al₂O₃ has attracted huge interest especially for high voltage applications due to its material properties; large band gap ($E_g = 7.0$ eV), high dielectric constant ($\epsilon = 9.0$) and high breakdown field (10 MV/cm) [39]. Hence for this thesis, Al₂O₃ is used as the gate insulator in the fabrication of AlGaN/GaN MISHEMT.

Using the low temperature Ti/Al/NiV metal scheme which was developed in Chapter 6, an innovative approach employing a CMOS compatible AlGaN/GaN MISHEMT (Al₂O₃) using common metal stacks and single masks for source/drain/gate is demonstrated and characterized. This novel approach extends the device's design and processing flexibility, which improves the limitation imposed by critical dimensions alignment in addition to having a lower thermal budget requirement.

7.2 Experimental Details

In this section, the HEMT structure is epitaxially grown on a 200-mm diameter Si (111) substrates of 1-mm thick using an AIXTRON CCS MOCVD system. The complete structure with total thickness ~ 3.8 μm , comprises of a

~380 nm AlN nucleation layer, three step-graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ intermediate layers, and a $\sim 1.5 \mu\text{m}$ GaN buffer layer, is achieved via uninterrupted growth. The 2DEG quantum well is formed by the overgrowth of ~ 300 nm undoped GaN channel, a thin AlN spacer (~ 1.0 nm), an $\text{Al}_{0.23}\text{Ga}_{0.76}\text{N}$ barrier layer (~ 20 nm), and a top un-doped GaN cap layer (~ 3.0 nm). The Al composition of the AlGaN barrier was determined by reciprocal space mapping in a high-resolution x-ray diffraction set up. The average full width at half maximum of the (002) and (102) rocking curves of the GaN buffer are ~ 510 and ~ 1275 arcsecs respectively. Hall measurements revealed an average sheet resistance of $\sim 430 \Omega/\text{sq}$ with a 2DEG sheet carrier density of $\sim 1.1 \times 10^{13} \text{ cm}^{-2}$.

The fabrication steps of the MISHEMT device structure using common metal stack for concurrent Source/Drain/Gate will be discussed. A poor quality interface can lead to degradation issues such as threshold voltage fluctuations and trap-assisted leakage current. Hence, it is important to study the gate stack integrity with its interface traps density. The gate oxide/AlGaN and AlGaN/GaN interface traps are studied using the capacitance–conductance frequency dependent analysis. Finally, the DC electrical characterizations are performed on the fabricated MISHEMTs to evaluate their electrical performance.

7.3 Device Fabrication

The HEMT devices were fabricated using the standard, non-planar mesa etch and metal lift-off process. Fig 7.1 shows the process flow of the MISHEMT device fabrication. The HEMT epiwafers are first treated with standard cleaning method via immersion of acetone, methanol and isopropyl

alcohol. It is then followed by active island lithography and mesa isolation etching by inductively coupled plasma (ICP) with BCl_3/Cl_2 chemistry. The gate insulator layer Al_2O_3 of ~ 12 nm is then formed via atomic layer deposition (ALD). A subsequent lithography and dry etching were done to remove unwanted Al_2O_3 at the S/D regions. No recess etching was performed. After wet chemistry cleaning, a single mask containing structures with different gate lengths and width variations is being used for photolithography process to pattern S/D/G. A blanket deposition of Ti/Al/NiV metal stack followed by lift-off process is executed to construct the S/D contact and metal gate structure concurrently. Finally, the metal stacks undergo rapid thermal annealing (RTA) process at 500°C for 30 s in N_2 ambient to form the S/D Ohmic contacts. Fig 7.2 shows the schematic cross-section of the fabricated MISHEMT device structure.

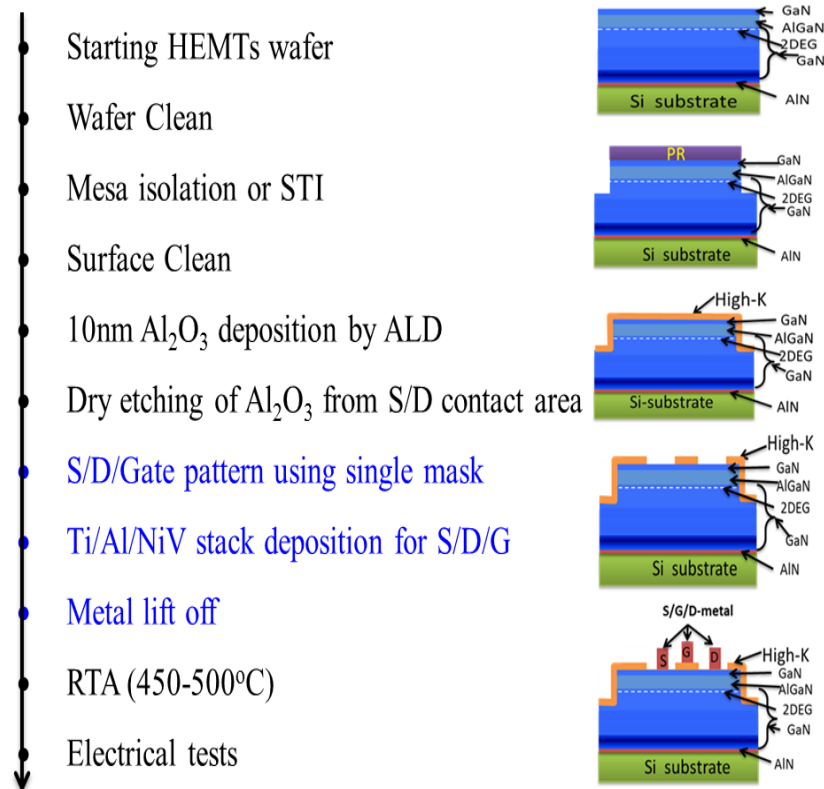


Fig 7.1: Schematic of MISHEMT fabrication process flow using the common metal stack and single mask for concurrent Source/Drain/Gate formation.

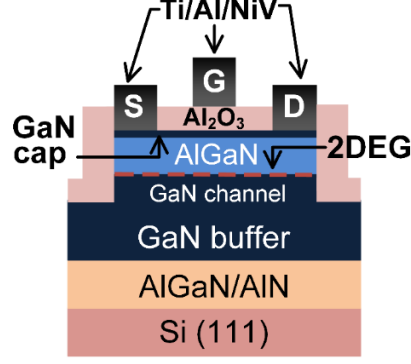


Fig 7.2: Schematic cross-section of fabricated AlGaN/GaN MISHEMT device structure using a common Ti/Al/NiV metal stack for Source/Drain/Gate formation.

7.4 Results & Discussions

7.4.1 Impact of Ti/Al/NiV Contact on the Gate Stack Integrity

The impact of the Ti/Al/NiV stack on the integrity of the Al₂O₃/AlGaN/GaN structure was examined using capacitance versus gate-voltage (C_p - V_g) and conductance versus frequency (G_p - ω) measurements of a MIS-HEMT sample annealed at 500 °C. Fig 7.3 (a) shows the C_p - V_g curves measured between the gate and S/D terminals for different small-signal frequencies. The maximum C_p (270 nF/cm²) corresponds to the strong 2DEG accumulation at the AlGaN/GaN interface, and is in good agreement with the calculated series equivalent of the Al₂O₃ and AlGaN capacitances (273 nF/cm²), based on a dielectric constant of 9 and 10.5, respectively. The Al₂O₃ thickness can be further estimated using the following equations:

$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{AlGaN}} + \frac{1}{C_{Al2O3}} \quad (7-1)$$

$$C_{Al2O3} = \frac{\epsilon_{Al2O3}\epsilon_0 A}{d} \quad (7-2)$$

where C_{TOTAL} is the as measured series equivalent capacitance of AlGaN and Al₂O₃, C_{AlGaN} is the capacitance of AlGaN barrier and C_{Al2O3} is the oxide

capacitance, $\epsilon_{Al_2O_3} = 9.0$ is the dielectric constant of Al_2O_3 [225], ϵ_0 is the vacuum permittivity, A is the effective area, and d is the thickness of Al_2O_3 . The calculated Al_2O_3 thickness is 12.4 nm which is in agreement with the thickness obtained from the cross-section TEM in Fig 7.4 (b). For $V_g < -4$ V, C_p decreases towards zero due to the depletion of 2DEG. In order to evaluate the hysteresis effect, the gate bias is firstly swept from -6 V to 0 V. Then the direction of bias voltage is changed from 0 V back to -6 V as shown in Fig 7.3 (b). The minor frequency dispersion and hysteresis effects indicate that the Ti/Al/NiV stack has no adverse impact on the underlying $Al_2O_3/AlGaN/GaN$ structure.

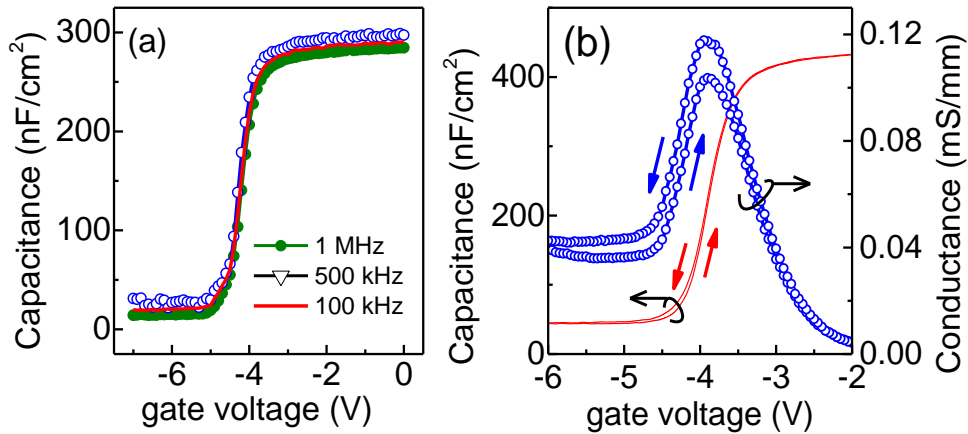


Fig 7.3: (a) Capacitance-voltage characteristics of the AlGaN/GaN MISHEMT for different small-signal frequencies. (b) Minor hysteresis in the capacitance and conductance characteristics arising from a dual-direction voltage-sweep. Arrows denote the directions of voltage sweep.

The diffusion of metal through the gate dielectric is also investigated by HRTEM and EDX analyses after S/D/G annealing. Smooth interface of the gate metal/ Al_2O_3 /GaN-cap/AlGaN/GaN layers is observed as depicted from the cross-sectional TEM images in Fig 7.4 (a) and (b). The EDX line scan profile as indicated in Fig. 7.4 (c) has been analyzed with a 2-nm resolution. The

termination of Ti profile at the Al_2O_3 surface indicates that metal is not diffusing into the dielectric layer after annealing. Similar intermixing of Al and Ti is observed as discussed earlier on ohmic contact formation at S/D in Chapter 6.

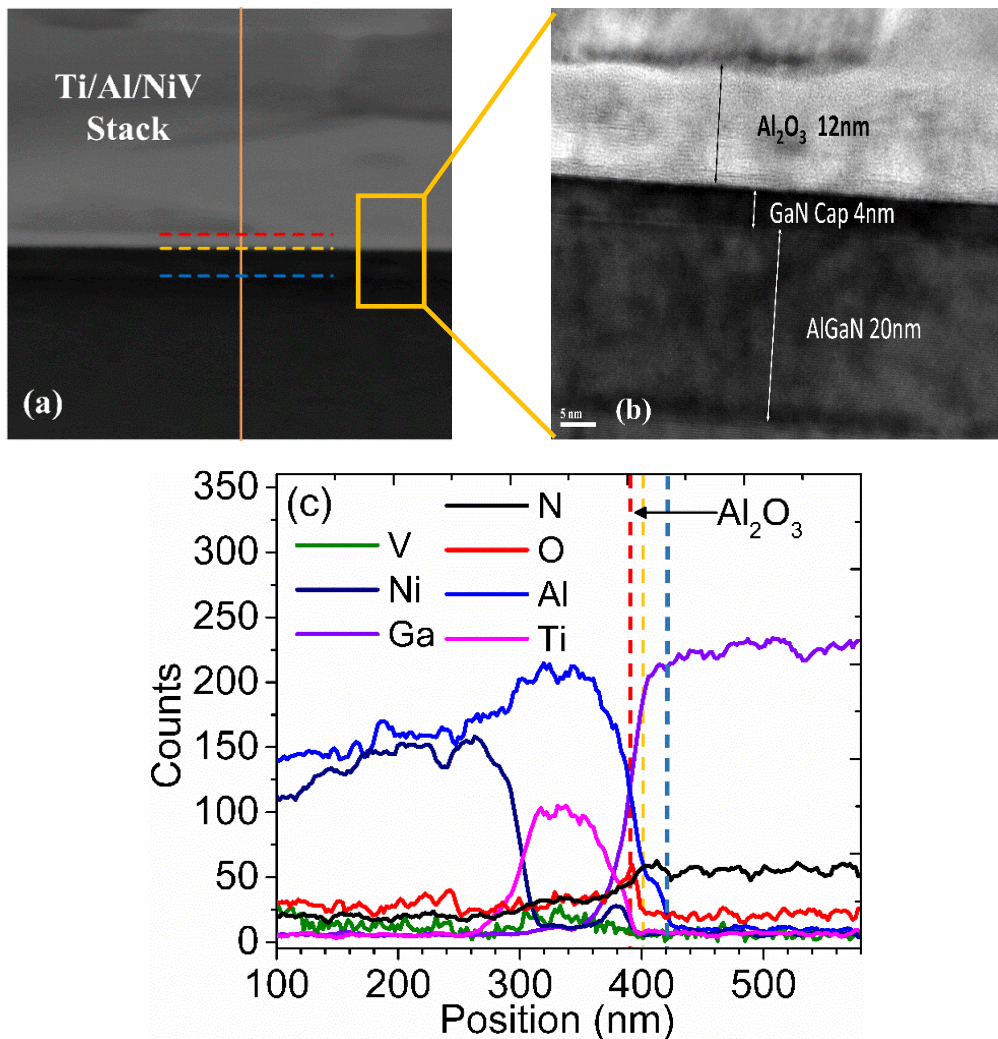


Fig 7.4: The cross-sectional HRTEM images across the (a) Ti/Al/NiV Gate metal stack, (b) Magnified image of the gate dielectric (Al_2O_3)/GaN-Cap/AlGaIn interface and (c) EDX elemental profiles corresponding to the 550-nm line scan.

Fig 7.5 shows the gate current characteristics of our AlGaIn/GaN MISHEMT with sub-nA reverse leakage current (up to $V_{\text{GS}} = -15$ V) and a nominal breakdown field of 8.7 MV/cm for thick (> 5 nm) Al_2O_3 which is in

agreement with the reported value by H.C. Lin et al. [230]. The large turn-on voltage of 3 V, defined as the forward gate current at 1 $\mu\text{A}/\text{mm}$ is due to the large band gap of Al_2O_3 [36]. The forward gate current leakage shows two parts (i) a monotonic increase of current with gate bias up to 3 V, whereby the conduction mechanism in this range is probably due to the Poole-Frenkel emission (PFE), and (ii) after 3 V, the gate leakage increases linearly in a log scale with the gate bias in a linear scale, indicating Fowler-Nordheim tunneling (FNT). This is similar to the observation of the gate leakage of Al_2O_3 MISHEMT on GaN/AlGaIn reported by Z.H. Liu [231]. The kink noticed at a gate bias of 3 V signifies the change in conduction mechanism, from PFE to the dominant FNT mechanism. Below 3 V, the forward current is determined by the total barrier, comprising Al_2O_3 and AlGaIn layer. As the gate bias increases, the 2DEG might transfer to the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface, therefore thinning the effective AlGaIn barrier layer, which eventually results in only the thin Al_2O_3 layer limiting the current flow

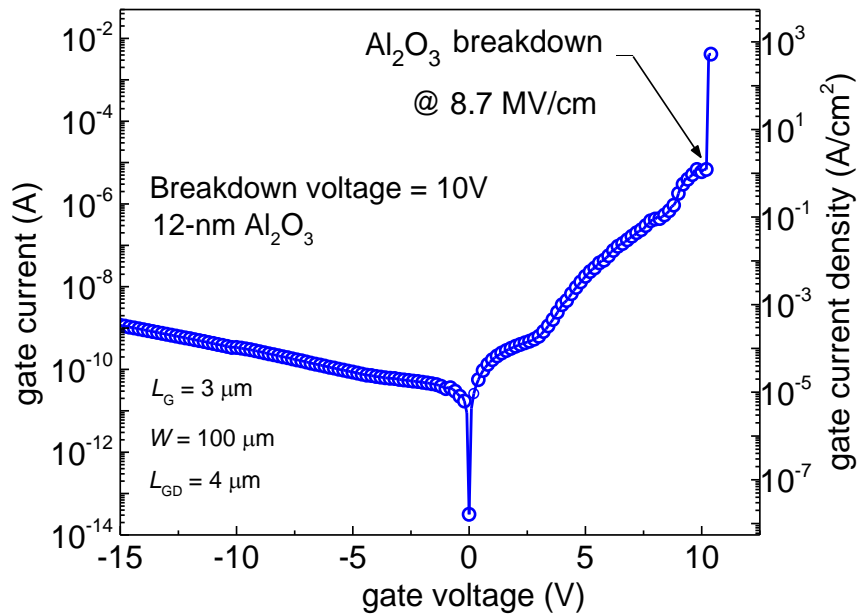


Fig 7.5: Typical gate current characteristic of single mask AlGaIn/GaN MISHEMT measured at 300 K. A nominal breakdown field of 8.7 MV/cm is extracted from the sudden step increase in gate current at forward bias.

7.4.2 Analysis of the AlGaN/GaN Interface State Density

A high level of D_{it} may lead to several degradation phenomena such as threshold voltage fluctuations, trap-assisted tunneling leakage, current collapse and C-V stretch out behavior [232]. Therefore, the characterization of interface trap density is essential for the development and optimization of high quality insulators for the AlGaN/GaN MISHEMT device. Unlike typical MOS structures where the channel is formed at the dielectric/semiconductor interface, MISHEMT structures have two interfaces due to the additional insulating layer which consist of the oxide/AlGaN and AlGaN/GaN. Due to the existence of this additional interface layer, together with the buried channel at the AlGaN/GaN heterointerface, the potential modulation and extraction of the interface traps become more complicated.

Several methods of determining the interface trap density for GaN-based HEMTs have been reported; CV hysteresis sweeping [233], frequency dispersion characterization [234], gate-to-drain conductance analysis [88], deep-level-transient-spectroscopy (DLTS) [235] and capacitance-frequency-temperature mapping [236]. It is worth mentioning that the standard C-V measurements used are only capable of detecting interface state densities with energy levels near the conduction band. This is ascribed to the large band gap of GaN where deep interface traps have a very long emission time constant, hence it is hardly detectable at room temperature. Chihoko Mizue from Hokkaido University reported as an example for the AlGaN layer (Al composition of 30%), the estimated thermal electrons emission time constant is 10^{10} - 10^{20} s at room temperature conditions [233]. Hence, a temperature dependent method coupled with a photo-assisted C-V measurement technique are needed in order

to evaluate the mid gap and deeper interface traps across the whole band gap energy which is not in the scope of this study. In this study, we will first focus on the interface traps analysis at the AlGaN/GaN heterointerface and the Al₂O₃/AlGaN interface at the subsequent section.

In order to study the interface state density of the AlGaN/GaN heterointerface, frequency-dependent conductance measurements are carried out at frequencies ranged from 1 kHz to 5 MHz with the Keithley 4200-SCS Parameter Analyzer at room temperature. The AC signal amplitude is maintained at below 50mV to meet the small signal requirement. The AlGaN/GaN interface-trap density D_{it} and interface-trap time constant, τ_{it} were extracted using the AC conductance method [237] based on the following expressions:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{eq}}{G_m^2 + \omega^2 (C_{eq} - C_m)^2} \quad (7-3)$$

$$D_{it} \approx \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{\max} \quad (7-4)$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln \left[1 + (\omega\tau_{it})^2 \right] \quad (7-5)$$

where G_m and C_m , are, respectively, as-measured conductance and capacitance; C_{eq} is series equivalent of Al₂O₃ and AlGaN capacitances; ω is frequency; A is gate area and q is electronic charge.

Fig 7.6 (a) shows the G_p/ω versus ω curves for different gate biases. For $V_G > -4.2$ V, the G_p/ω peak is shifted to frequencies beyond the maximum (5 MHz) allowed by the measurement system. We do not expect this limitation to result in the underestimation of D_{it} . This is because the G_p peaks at $V_G = -4$ V (Fig 7.3 (b)) and decreases with further increase of V_G , indicating that the

sensitivity of the ac conductance method is decreased due to the “shunting” of the interface-trap impedance by the 2DEG impedance which is shown by the equivalent circuit model in inset of Fig 7.6 (b). The very large value of 2DEG capacitance at accumulation region will screen the dispersion attributed by the interfacial traps, C_{it} and R_{it} limiting the energy level available to be extracted by the conduction method.

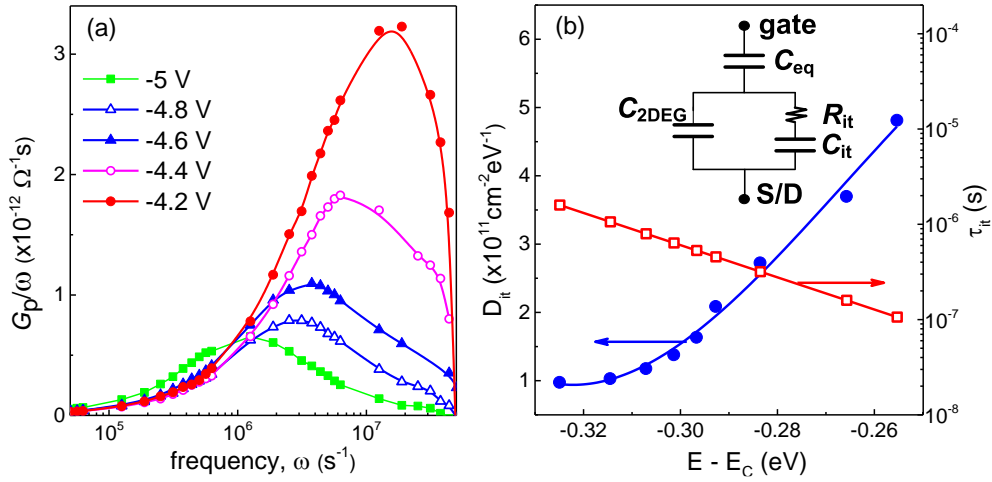


Fig 7.6: (a) Normalized conductance G_p/ω versus frequency ω characteristics for different gate biases. (b) Energy distribution of as-measured interface-trap density D_{it} and trap time-constant τ_{it} . Inset shows the equivalent impedance circuit.

The trap energy distribution of the extracted D_{it} and τ_{it} are depicted in Fig 7.6 (b). The respective trap state energy levels, E_T can be estimated using the expression (3-28) as described in Chapter 3 earlier. As the negative gate bias increases, a reduction in D_{it} and increase in τ_{it} are observed which is attributed to the lowering of Fermi level with respect to the conduction band of GaN. This is in agreement with R.M. Chu’s findings, where traps with higher energy levels usually take shorter time for trapping/de-trapping process [91]. At $V_G = -4.2$ V, D_{it} of $5 \times 10^{11} cm^{-2} eV^{-1}$ is extracted. It is noteworthy that this D_{it} value is similar to the reported values [96, 238-240], confirming that the

Ti/Al/NiV metal stack has no adverse impact on the Al₂O₃/AlGa_N/Ga_N structure.

7.4.3 Analysis of the Al₂O₃/AlGa_N Interface State Density

As mentioned earlier, the AlGa_N/Ga_N MISHEMT structures have two different interfacial layers due to the gate insulator and the AlGa_N barrier layer. Recently, studies showed that a typical high quality Ga_N MISHEMT structure will exhibit two rising slopes in their AC capacitance-voltage behavior [233, 241, 242]. The second C-V rising slope at the positive bias regime which represents the Al₂O₃ oxide capacitance, is attributed to the transfer of electrons from the 2DEG AlGa_N/Ga_N to the Al₂O₃/AlGa_N interface.

Nevertheless, several groups reported C-V curves of the MISHEMTs without the second step characteristics at the positive bias regimes [89, 243]. This unique second C-V rising slope feature is non-observable if the dielectric/III-V interface consists of high density states [244]. In addition, the observation of the second capacitance plateau is limited by the high gate leakage current at high forward biases which results in a sharp increase of the conductance measured. Owned to such limitations, the oxide capacitance which corresponds to the thin Al₂O₃ layer can not be observed [233].

In order to study the oxide/AlGa_N interface state traps, the capacitance-voltage measurements are conducted by sweeping the gate bias from -5 V to +3 V and back to -5 V as shown in Fig 7.7. A second rising slope is observed at Step 2 which confirms the transferring of electrons from the 2DEG channel to the oxide/AlGa_N interface. The frequency-dependent AC conductance method is used to analyze the interface traps at the second rise slope (Step 2). The

conductance G_p/ω as function of frequency ω at different gate bias and the energy distribution of the extracted D_{it} and τ_{it} are depicted in Fig 7.8 (a) and (b).

The $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces exhibit an average interface trap density value of $9.8 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ with corresponding time constant of $0.4 - 1.6 \mu\text{s}$ for positive gate bias of 2.0 V to 2.6 V. The extracted D_{it} is slightly lower than the reported values of similar MISHEMT structures which uses a thinner (5 nm) Al_2O_3 insulator as per reference [245]. We proposed that the origins of the high trap density might be due to the formation of thin native GaO_x layer during the ALD process of depositing Al_2O_3 [246]. However, it is noteworthy to acknowledge that the extracted trap density at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface might be under/over-estimated due to the AlGaIn barrier dynamic resistance at the positive bias regime. Given that the interface state density is very low, the ac-response of the AlGaIn barrier and the interface traps could be comparable at the second rising slope (Step 2) [247]. Therefore, the stretch-out phenomenon at the second C-V slope might be contributed by both interface traps and the AlGaIn barrier impedance.

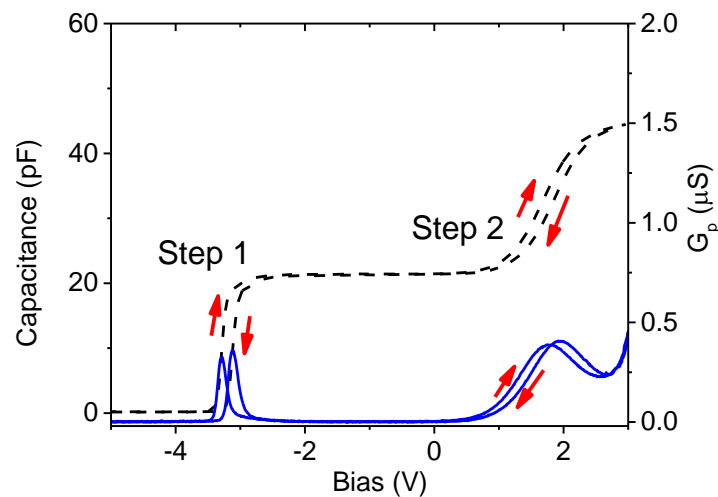


Fig 7.7: Capacitance and Conductance-Voltage characteristics of the AlGaIn/GaN MISHEMT at 10 kHz.

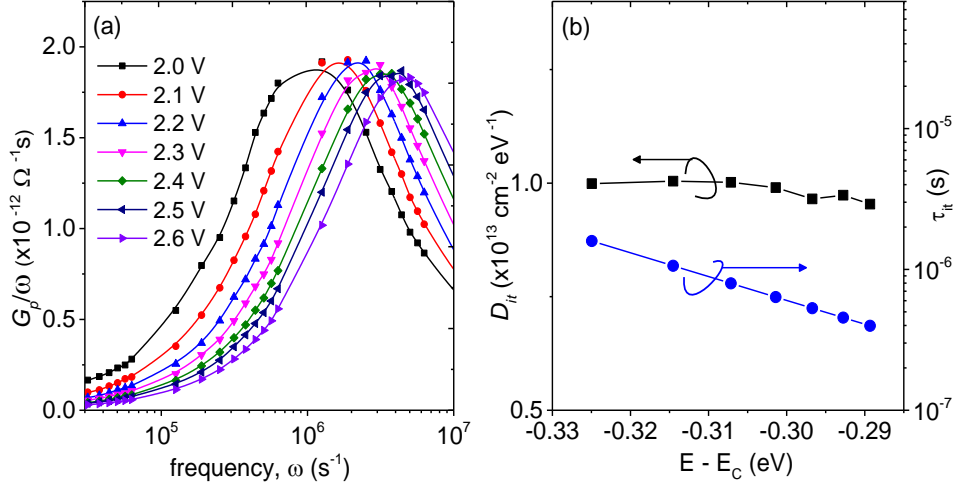


Fig 7.8: (a) Conductance ‘ G_p/ω ’ versus frequency ‘ ω ’ characteristics for different gate bias (at the positive bias regime) and (b) Energy distribution of as-extracted interface-trap density D_{it} and trap time-constant τ_{it} of the MISHEMT structure.

Fig 7.9 (a) and (b) show the capacitance and conductance-voltage measurements with varying frequencies from 10 kHz to 200 kHz. A stretch-out effect is observed at the second rising slope denoted by “Step-2”. The large frequency dispersion at Step-2 might be attributed to either high interface traps or the impedance effect of the AlGa_N barrier layer or even both. Capriotti *et al.* recently reported that the strong frequency dispersion at the second C-V slope and a peak occurrence in the G_p/ω are possible even without the presence of trap states ($D_{it} = 0$), due to the intrinsic response of the gate stack [248]. This is in agreement with our results in Fig 7.9 where a drop in capacitance, C_p is observed at the second rising regime as the frequency increases. We believe that this phenomenon is attributed to the intrinsic gate response and the decrease in resistance of the AlGa_N barrier, R_{br} at forward applied bias [248]. The onset of the second capacitance rise is reported to be strongly frequency dependent [242, 249]. Thus at higher frequencies, the 2DEG electrons might not have sufficient time to travel through the AlGa_N barrier to achieve a uniform distribution at the Al₂O₃/AlGa_N interface.

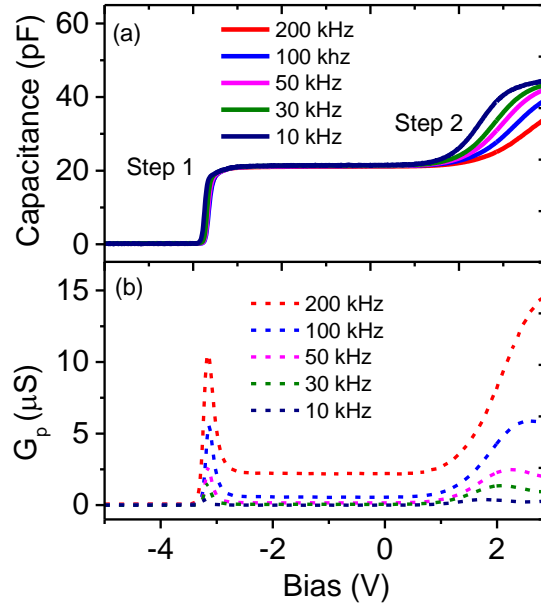


Fig 7.9: (a) Capacitance-voltage frequency dispersion and (b) Conductance-voltage frequency dispersion characteristics of AlGaIn/GaN MISHEMT ranging from 10 kHz to 200 kHz.

In addition, it is reported that when the leakage through the AlGaIn barrier is negligible, the dielectric interface and the 2DEG channel at the AlGaIn/GaN interface are not effectively shorted out [247]. Thus, an additional component of barrier impedance need to be considered as modelled by the equivalent circuit in Fig 7.10. Owned to this additional “low-pass filter” component (C_{br} and R_{br}), the extraction of interface traps becomes more complicated.

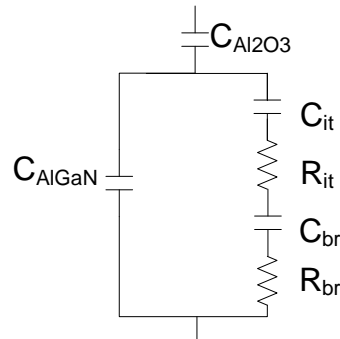


Fig 7.10: Small Signal equivalent circuit of AlGaIn/GaN MISHEMT, taking into consideration the series impedance of the AlGaIn barrier (C_{br} and R_{br}) to the trapping/detrapping of interface traps (C_{it} and R_{it}) [247].

Therefore, due to such limitations, it is difficult to distinguish the dispersion at the second rising slope which is contributed solely by the oxide/AlGa_N interface traps. An equivalent model which can effectively decouple the series impedance caused by the AlGa_N barrier layer is needed in order to capture the oxide interface traps accurately. Another possible solution is to compare the experimental results with a simulated ideal curve (without any traps consideration). However, it remains a challenge as the simulation might not capture the actual device's behavior accurately.

Therefore, the accuracy of the AC conductance method in extracting the oxide/AlGa_N interface traps density is limited due to the complicated interdependence of the interface traps and the gate stack intrinsic response which result in comparable effect towards the measured capacitance and conductance [248]. At this point of study, it stills remain a challenge to determine precisely the trap emission contributed by the oxide/AlGa_N interface which is beyond the scope of this thesis. Future work is recommended to analyse the oxide/AlGa_N interface trap in greater detail.

7.4.4 DC Characterization of the AlGa_N/Ga_N MISHEMT using the Common Metal Stack Scheme

Finally, the DC performance of the fabricated devices are evaluated. Typical DC characteristics of a MISHEMT, of equal gate length and gate-drain access region of 3 μm , fabricated using the single-metal scheme are depicted in Fig. 7.11 (a) and (b). From the output curves (Fig. 7.11 (a)), the specific on-state resistivity at $V_{\text{GS}} = 2 \text{ V}$ is $2.3 \text{ m}\Omega\text{-cm}^2$, comparable to values reported by Van Hove *et al.* [39]. A maximum saturation drain current of 210 mA/mm is

achieved at $V_{GS} = 2 \text{ V}$ with marginal current collapse. The AlGaN/GaN MISHEMTs device operating at $V_{DS}=20 \text{ V}$ exhibit a pinch-off voltage of -3 V . The transfer curves (Fig. 7.11 (b)) reveal a sub threshold swing of 80 mV/dec and an I_{ON}/I_{OFF} ratio of 10^9 . It is noteworthy to highlight the exhibited I_{ON}/I_{OFF} ratio is similar or even better than the reported AlGaN/GaN MISHEMTs [33, 207, 208]. A large I_{ON}/I_{OFF} ratio and low SS are essential for fast switching power applications. These good transfer characteristics are consistent with the quality of the gate stack. The lower transconductance peak of 60 mS/mm , as compared to the value (88 mS/mm) of a conventional HEMT realized on the same type of substrate, may be ascribed to the reduced gate capacitance arising from the Al_2O_3 incorporation. Fig 7.12 shows the three terminal off-state breakdown measurement for the AlGaN/GaN MISHEMT devices. I_{DS} is measured as a function of increasing V_{DS} with fixed $V_{GS} = -8 \text{ V}$ (off-state). Measurements are done in Flourinert ambience to avoid early breakdown/burn-off in air due to the high electric field induced. A high off-state breakdown voltage (BV_{off}) of 510 V is extracted from the sharp increase of drain current for the device with $L_{GD} = 3 \mu\text{m}$.

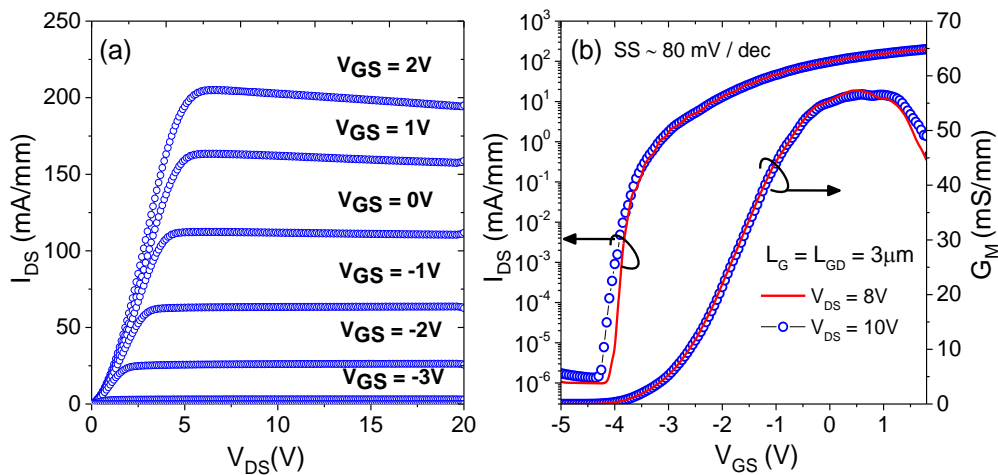


Fig 7.11: (a) DC output I_{DS} - V_{DS} and (b) transfer characteristics semilog I_{DS} - V_{GS} of AlGaN/GaN MISHEMT using the single mask approach. Device dimensions are $W=40 \mu\text{m}$, $L_G=3 \mu\text{m}$, and $L_{GD}=3 \mu\text{m}$.

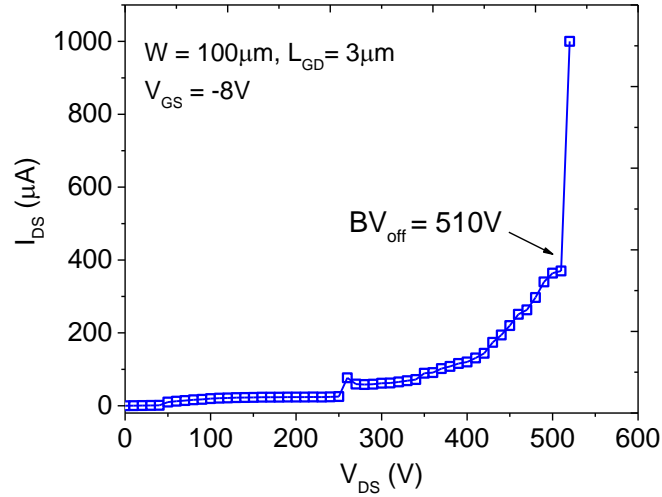


Fig 7.12: Three terminal off state breakdown measurement I_{DS} - V_{DS} of AlGaIn/GaN MISHEMT at $V_{GS} = -8V$. $BV_{off} = 510V$ is extracted for device with dimension $L_{GD} = 3 \mu m$.

7.7 Chapter Summary

In this chapter, a novel approach in fabricating an AlGaIn/GaN MISHEMT using common metal stacks and single masks for the source/drain/gate is demonstrated. The fabrication flow of the MISHEMT is discussed. The MISHEMT demonstrated excellent electrical characteristics: an I_{ON}/I_{OFF} ratio of 9 decades (due to sub-nA off-state leakage current up to a -15 V gate bias), and a sub threshold swing of 80 mV/dec. The interface traps at the AlGaIn/GaN heterointerface are evaluated using the frequency-dependent conductance method. A low $D_{it} = 5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ is extracted at $V_G = -4$ V which might be attributed to the low temperature process, surface states and metal-induced traps reduction by the incorporation of the dielectric layer.

A brief analysis is also conducted in order to study the extraction of trap density at the critical oxide/AlGaIn layer. The analysis process becomes more complicated due to the buried channel property of AlGaIn/GaN HEMT and the presence of two interfacial layers, oxide/AlGaIn and AlGaIn/GaN. Some

limitations and challenges faced in the estimation of traps due to the oxide/AlGaN interface are discussed. The conventional conductance method may lead to under/over-estimation of the D_{it} due to the complex interdependence between the interface traps and the intrinsic gate response. An equivalent circuit model or correction method is required in order to decouple effectively the series impedance response of the AlGaN barrier layer from the oxide interface traps.

As demonstrated, our approach offers a low thermal budget gold-free process for AlGaN/GaN MISHEMTs fabrication. The novel approach utilizes a self-aligned single mask and common metal scheme (Ti/Al/NiV) for concurrent source/drain/gate formation. This overcomes the issues of misalignment in devices with tight design rules which are restricted by the lithography tool capability. In addition, the demonstrated approach offers a low thermal budget process which mitigates the defects and the incorporation of during high processing temperature. This reduces the thermal budget while maintaining the gate stack quality which is essential for a gate-first implementation. Owned to the design flexibility which our approach offers, structures such as symmetric and asymmetric MISHEMTs, capacitor split C-V structures, vertical and lateral breakdown test structures, Source/Drain and gate field plates, and dual gate RF transistors can be implemented.

In conclusion, we believe that our proposed single-metal scheme for the concurrent formation of gate, source and drain thus offers a bright prospect for GaN-on-Si integration with reduced complexity. Such fabrication scheme may find its applications in the CMOS compatible high voltage and RF electronics.

CHAPTER 8: CONCLUSION & RECOMMENDATION

8.1 Conclusion

In this dissertation, investigations have been primarily focused on the fabrication and characterization of the AlGa_N/Ga_N heterostructure and devices grown on silicon based substrates, namely, the thin Silicon-on-Insulator (SOI) and bulk Si. As discussed earlier in the motivation Section 1.2, there are several main challenges in the integration of Ga_N on Si technology for cost effective mass production of Ga_N devices. These challenges have thus led to the development of the objectives and scope of this dissertation.

All the HEMT devices in this report are fabricated using a planar process. Each processing step recipe which includes sample cleaning/spin coating, optical lithography, e-beam evaporator, RF sputtering, ICP-RIE plasma etching and Rapid Thermal Annealing is developed and optimized at the cleanroom facilities at IMRE and NTU. Apart from device level planar fabrication development, electrical characterizations (DC and C-V analysis) and physical analysis (STEM, AFM, EDX, micro-PL and Raman) have been employed to provide useful information and insights of the fabricated devices. The key findings and achievements of this research are summarized as follows:

1. AlGa_N/Ga_N heterostructures grown on SOI substrates exhibit a 50% lower wafer bowing and a comparatively lower level of induced stress. As a result, the 2DEG mobility and sheet-resistivity uniformity are improved

due to lower dislocation defect density. In terms of device performance, HEMT structures fabricated on the AlGaIn/GaN-on-SOI exhibit ~20.5 % higher saturation drain current and ~19.5% higher peak trans-conductance as compared to the bulk-Si counterparts. From the Raman spectroscopy, the AlGaIn/GaN HEMTs on SOI suffer greater channel self-heating (~50 K) ascribed to the lower thermal conductivity of the buried oxide (BOX) layer.

2. A novel investigation on the effect of germanium diffusion at the gate region of AlGaIn/GaN HEMT and its impact on threshold voltage shift is presented. A positive threshold voltage shift of ~1.15 V is demonstrated by annealing the Ge-deposited HEMT at a temperature of 825°C. Ge-diffused HEMTs exhibit a lower transconductance and lower drive current due to the 2DEG carrier compensation caused by the Ge diffusion. Studies showed that a higher annealing temperature contributes to a larger positive threshold voltage shift. This is attributed to the higher and deeper level of Ge diffusion into the AlGaIn barrier which depletes more 2DEG carriers.
3. The fabrication of AlGaIn/GaN HEMT using low thermal budget Au-free Ohmic contacts of Ti/Al/NiV is demonstrated. The Ti/Al/NiV metal stack is optimized in terms of Ti/Al relative thickness, thermal processing temperature and annealing duration. An optimized Ti/Al/NiV (20/200/70 nm) metal stack annealed at 500 °C for 30 s exhibit smooth surface morphology with a R_c of ~0.8 Ω .mm and ρ_c of ~ 6.33×10^{-6} Ω .cm². The Au-free HEMTs demonstrate excellent switching performance with an

I_{ON}/I_{OFF} ratio $\sim 3 \times 10^9$ and a subthreshold swing 'SS' of ~ 71 mV/decade which is attributed to the low thermal budget processing.

4. By integrating the developed Ti/Al/NiV metal stack, a self-aligned AlGaIn/GaN MISHEMT fabrication using an innovative approach of single mask and common metal stack for concurrent source/drain/gate patterning is demonstrated. The fabricated MISHEMTs have excellent electrical characteristics; an I_{ON}/I_{OFF} ratio of 9 decades and a subthreshold swing of 80 mV/dec. The good integrity of the demonstrated gate stack is confirmed by the low gate leakage characteristics (sub-nA up to $V_G = -15$ V) and low interface state density of $\sim 5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

8.2 Recommendations

Based on the achieved results in this report, several future work are proposed as follows:

1. To extract temperature depth profiling of the AlGaIn/GaN HEMTs on SOI and bulk Si substrates at different on-state bias conditions using micro Raman and PL analyses.
2. To study the role of Ge thickness and its impact towards the threshold voltage shift during the annealing process.
3. To optimize the placement of Ge in the AlGaIn barrier for effective threshold voltage control
4. To study the defects generation and behavior due to the Ge doping in the gate region of the AlGaIn/GaN HEMTs.

5. To incorporate a double annealing method in order to overcome the limitation of Ohmic contact degradation when Ge is diffused using higher temperature annealing.
6. To improve the electrical contact resistance of the developed Ti/Al/NiV metallization scheme using Ohmic contact recess etching method.
7. To explore other potential dielectric materials such as Ga_2O_3 , HfO_2 , ZrO_2 , and SiO_2 to be incorporated into the AlGaN/GaN MISHEMTs fabrication scheme using common metal stack and single mask for source/drain/gate formation.
8. To study the surface passivation and performance enhancement through the incorporation of the SiN layer with the Al_2O_3 insulator in fabricating Au-free AlGaN/GaN MISHEMTs. Reports showed that the bilayer design of the SiN/ Al_2O_3 structure is able to improve the current collapse performance and reducing the traps density.
9. To develop an equivalent circuit model for an in-depth study of the critical oxide/AlGaN interface trap behavior. An improved model is required in order to decouple the effect of the AlGaN barrier layer impedance which is able to result in comparable small signal response with the interface traps.

PUBLICATIONS

1. L. K. Bera, **W. H. Tham**, R. S. Kajen, S. B. Dolmanan, M. K. Kumar, V. K. X. Lin, *et al.*, “Effect of Ge diffusion on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistors on a thin silicon-on-insulator”, ECS Solid State Letters, vol. 2, pp. Q105-Q108, 2013. DOI: [10.1149/2.002312ssl](https://doi.org/10.1149/2.002312ssl)
2. **W. H. Tham**, L. K. Bera, D. S. Ang, S. B. Dolmanan, T. N. Bhat, and S. Tripathy, “ $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ MISHEMTs with a Common Gold-Free Metal-Stack for Source/Drain/Gate”, IEEE Electronic Device Letters, vol. 36, pp. 1291-1294, 2015. DOI: [10.1109/LED.2015.2491362](https://doi.org/10.1109/LED.2015.2491362)
3. **W. H. Tham**, D. S. Ang, L. K. Bera, S. B. Dolmanan, T. N. Bhatt, V. K. X. Lin, and S. Tripathy, “Comparison of the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ Heterostructures Grown on Silicon-on-Insulator and Bulk-Silicon Substrates”, IEEE Trans. Electronic Device, vol. 63, pp. 345-352, 2016. DOI: [10.1109/TED.2015.2501410](https://doi.org/10.1109/TED.2015.2501410)
4. **W. H. Tham**, D. S. Ang, L. K. Bera, S. B. Dolmanan, T. N. Bhatt, R. S. Kajen, H. R. Tan, S. L. Teo and S. Tripathy, “Gold-free Ohmic contacts on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ high electron mobility transistor structures grown on 200-mm diameter Si”, J. Vac. Sci. Technol. B, *submitted (2015)*.

PATENT

1. L. K. Bera, Y. C. Loke, S. B. Dolmanan, S. Tripathy, **W.H. Tham**, “Common metal stack and single mask self-align source, drain and gate process for III-V nitride MISHEMTs”, A* STAR IMRE, PCT Application No: PCT/SG2016/050111, ETPL ref: IMR/P/08873/01/PCT, IMRE ref: 201471

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