Coupled-Inductor-Based Bidirectional Z-Source Breaker for DC System Protection

Mridul Marwaha[1], Kuntal Satpathi[2], Josep Pou[3], Devinda A. Molligoda[4], Chandana Gajanayake[5], Amit Kumar Gupta[6]
[1,2,3,4] Rolls-Royce@NTU Corporate Lab, Nanyang Technological University, Singapore
[1,3,4] School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
[5,6] Rolls-Royce Electrical, Singapore
[1]mridul004@e.ntu.edu.sg, [2]ksatpathi@ieee.org, [3]josep.pou@ieee.org, [4]liyanage001@e.ntu.edu.sg,
[5]chandana.gajanayake@rolls-royce.com, [6]Amit.Gupta@Rolls-Royce.com

***Abstract*—A coupled-inductor-based bidirectional Z-source breaker topology is introduced in this paper, which has the ability to detect and isolate the faulty section of the dc power system. Compared to existing topologies, the proposed topology utilizes a lower number of components and the coupled inductors reduce the footprint of the breaker. Analytical design equations are derived for the sizing of inductors and capacitor. Fault condition is analyzed to compute the essential criteria for the breaker to operate. Operation under step load and fault conditions are validated by simulation in both SPICE and MATLAB/Simulink environment.**

***Index Terms*—DC circuit breaker, dc system protection, fault isolation devices, microgrids, Z-source breaker.**

I. Introduction

In recent years, dc power distribution networks are becoming increasingly popular in many applications including marine vessels, more/all-electric aircrafts, microgrids and high voltage dc system [1]–[5]. DC grids offers many advantages such as absence of reactive power flow, easier integration of the renewable energy sources, reduced number of power conversion processes, integration of asynchronous ac power networks, and so on.

Despite the abovementioned advantages, the lack of current zero-crossing makes the fault isolation a major challenge in such systems [6]. When a circuit breaker (CB) is operated in conventional ac power systems, the arc formed during the separation of metal contacts of the CB is extinguished automatically due to the zero crossing of current every half cycle. Absence of current zero-crossing in dc system results in a sustained arc, thereby requiring special consideration in the fault isolation circuit. To mitigate the problem of arcing, it is envisioned that the mechanical CBs alone are not sufficient, and it should be complemented with semiconductor-based fault isolation devices in most of the dc applications. In this regard, the Z-source breaker (ZSB) is one of the emerging and promising topologies to realize such fault isolation devices [7]. ZSB is inspired by the Z-source inverters, which can operate in buck as well as boost mode using a crossed *L-C* connection [8], [9].

ZSB is a passive protection module, which automatically trips during a fault condition. Silicon controlled rectifier (SCR) is the main conducting device, which is unidirectional in nature and the gate signal can be removed once the device starts conducting. In ZSB, SCRs are supplemented by inductors and capacitors to force the current to zero and stop the device from conduction during a fault condition. One of the prime advantages of ZSB is that it has inherent fault limiting capability, resulting in the dc system protection to be more tolerant to faults. Due to fast isolation, these breakers provide many advantages such as reduced fault current magnitude and component stress, and simplicity of the interfaced control circuit.

Unidirectional ZSB topologies and their applications in various dc networks were proposed in [10]–[20]. Incorporation of distributed generation sources and energy storage systems implies the need for bidirectional power flow in many subsystems of the power networks/architecture. One of the main disadvantages of ZSB is that it requires a very large fault current or extreme/severe conditions to operate the breaker [7]. It is thus needed to design a bidirectional ZSB which is capable of interrupting a wide range of fault currents.

This paper proposes a novel coupled-inductor-based bidirectional ZSB (CI-BZSB) topology which can operate in a wide range of transient fault current. Additionally, the low number of components and integrated coupled inductors reduce the weight and volume of the breaker compared to already existing topologies. The proposed topology can also provide step load change flexibility greater than the steady-state load current, alongside maintaining the bidirectional symmetricity. Losses are also reduced since only one semiconductor device conducts at a time.

This paper is organized as follows. A review of bidirectional ZSB topologies is presented in Section II. The proposed ZSB topology and various operation modes are discussed in Section III. Design criteria for the proposed ZSB inductors and capacitor, followed by analysis under fault condition and step load change are presented in Section IV. Finally, Section V summarizes the main conclusions of the paper.

II. Review of Bidirectional ZSB Topologies

Classical bidirectional ZSBs were proposed in [21], [22]. Classical topologies lack of common grounding because inductors are present in the return path. ZSB-based fault current

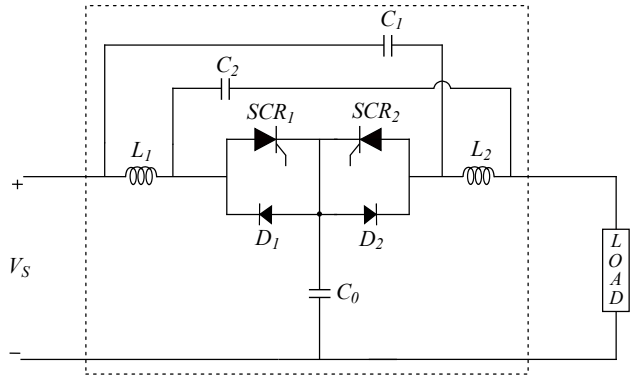


Fig. 1. Z-source breaker-based fault current limiter and interrupter (FCLI).

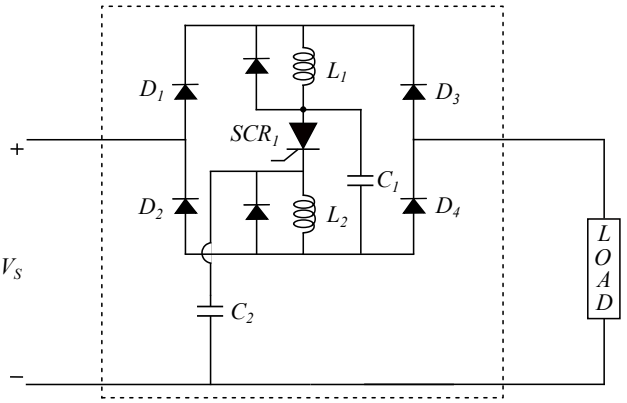
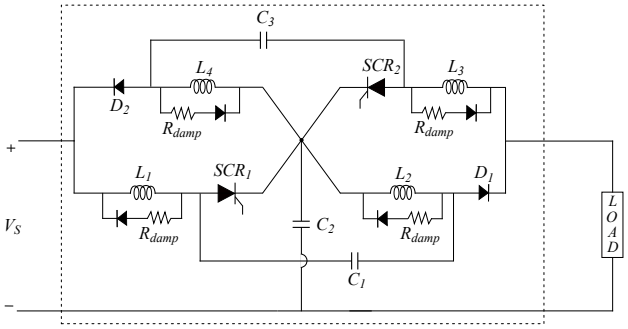
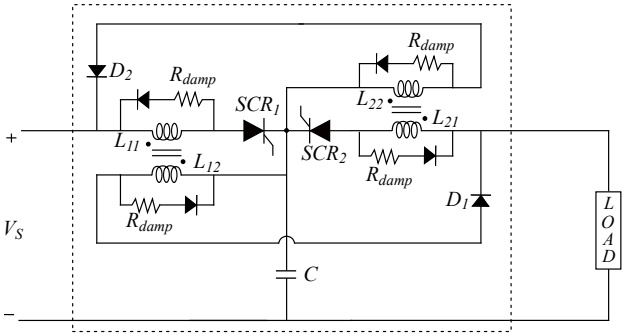


Fig. 2. Bidirectional series Z-source breaker.



(a)



(b)

Fig. 3. (a) Bidirectional Z-source breaker and (b) bidirectional Z-source breaker with coupled inductor.

limiter and interrupter (FCLI) was proposed in [23], as shown in Fig. 1. This topology provides common grounding with reduced number of controlled semiconductor devices. During steady-state operation, depending on the current flow direction, one of the SCRs (SCR_1 or SCR_2) and diodes (D_2 or D_1) conduct to supply the load current, while inductors (L_1 and L_2) and capacitors (C_0, C_1 and C_2) behave as short circuit and open circuit elements, respectively. To facilitate the analysis, the current is assumed to flow through the path $V_s - L_1 - SCR_1 - D_2 - L_2$. During a fault condition, source and capacitors supply the fault current through the high-frequency low-impedance path ($C_0 - SCR_1 - C_2$ and $V_s - C_1 - D_2 - SCR_1 - C_2$), opposing the original steady-state current flow through SCR_1. Immediately after the current through SCR_1 reaches zero, it commutates naturally. During the next interval, source (V_s), capacitors (C_0, C_1 and C_2), inductors (L_1 and L_2), and fault conductance resonate. Post resonance, the fault is isolated with the capacitors C_1 and C_2 charged to the source voltage.

A bidirectional series ZSB topology was proposed in [24], as illustrated in Fig. 2. This topology employs only one SCR and two capacitors compared to two SCRs and three capacitors required in the previous topology. During the steady-state operation, depending on the direction of current flow, two of the four diodes (D_1, D_4 or D_3, D_2) and SCR (SCR_1) conduct to supply the load. The intervals of operation are similar to FCLI.

Bidirectional ZSB and bidirectional ZSB with coupled inductor topologies were proposed in [25], as shown in Fig. 3. Bidirectional ZSB with coupled inductor has the advantage of reduced number of capacitors and, additionally, reduced weight and size of inductors compared to conventional inductor-based topologies. In Fig. 3(b), during steady-state operation depending on the current flow direction, one of the SCRs (SCR_1 or SCR_2) and diodes (D_1 or D_2) conduct to supply the load current. Inductors L_{11} and L_{12} and capacitor C behave as short-circuit and open-circuit elements, respectively. To facilitate the analysis, the current is assumed to flow through the path $V_s - L_{11} - SCR_1 - L_{12} - D_1$. During fault condition, the capacitor C supplies the fault current through the high-frequency low-impedance path ($C - L_{12} - D_1$). This transient current in L_{12} induces current in L_{11} opposing the original steady-state current flow through SCR_1. Immediately after the current through the SCR_1 reaches zero, it commutates naturally. During the next interval, capacitor C, L_{12} and fault conductance resonate. The diode across the inductor starts conducting once the voltage across it changes polarity, dissipating the remaining inductor stored energy.

In [26], a ZSB topology based on the similar working

principle was proposed to achieve a reduction in the number of components by combining the redundant magnetic structure in Fig. 3(b). A further reduction was achieved in [27], but the topology is constrained to have equal value of inductors to maintain bidirectional symmetricity.

III. Proposed CI-BZSB Topology

The proposed CI-BZSB topology is shown in Fig. 4. SCR_1 and SCR_2 are the main SCRs used for steady-state bidirectional power flow operation. SCR_3 and SCR_4 are auxiliary SCRs, which conduct only during fault condition. L_{11}, L_{12}, and C are two coupled inductors and a capacitor, respectively.

- During steady state condition, one of the two pairs of SCRs (SCR_1, SCR_3 or SCR_2, SCR_4) is gated depending on the direction of current flow. The gating signal to the main SCR (SCR_1 or SCR_2) is withdrawn once the current through the SCR exceeds the latching current, while the auxiliary SCR (SCR_3 or SCR_4) is continuously gated. In the example shown in Fig. 5(a), the current flows through the path $V_S - SCR_1 - L_{12} - L_{11} - R_L$.
- During fault condition, represented by a conductance of value G_{fault}, the source (V_s) supplies the transient current through the high-frequency low-impedance current path ($V_s - C - L_{11}$) shown in Fig. 5(b). This transient current through the inductor L_{11} induces current in inductor L_{12}, such that the induced current opposes the original steady-state current flow through the SCR_1. SCR_1 commutates naturally as soon as its current reaches zero.
- During the post-commutation stage, source (V_s), C, L_{11} and fault resonate, as shown in Fig. 5(c). Resonance continues until the voltage across the inductor L_{11} becomes negative, which starts dissipating the stored energy in the damping resistor R_{damp} and SCR_3. Finally, the current in the circuit decays to zero with the capacitor charged to the source voltage. Hence, CI-BZSB successfully isolates the source and the load in case of a fault condition, preventing any potential damage to the system.

During reverse power flow condition, SCR_2 and SCR_4 are gated similar to the previous case. During fault condition,

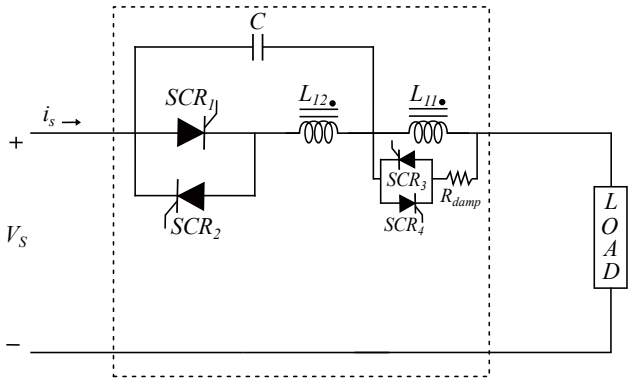


Fig. 4. Coupled inductor based bidirectional Z-source breaker (CI-BZSB).

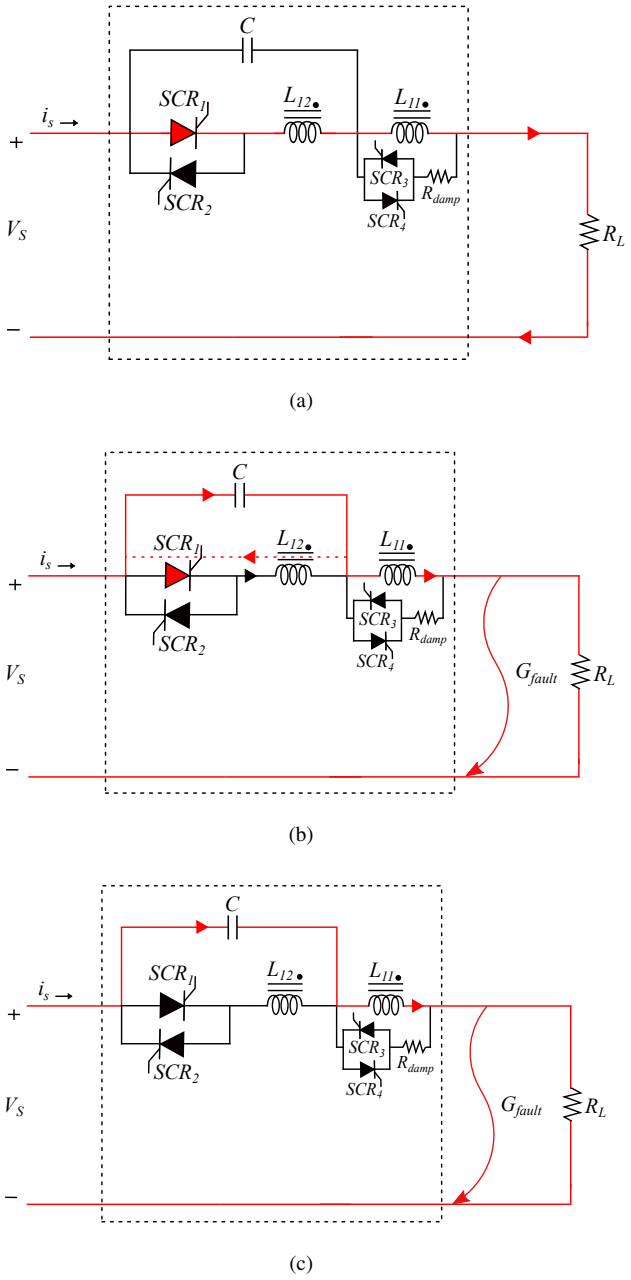


Fig. 5. Various operation modes of the proposed CI-BZSB. (a) Steady-state interval, (b) fault condition and (c) post-commutation stage.

source (V_S) supplies the transient current through the high-frequency low-impedance current path ($V_s - L_{11} - C$), shown in Fig. 6. The induced current in L_{12} opposes the steady-state current through SCR_2, thereby SCR_2 commutates naturally. Post-commutation stage is similar to the previous case.

IV. Design and Analysis of Proposed CI-BZSB

In this section, design criteria for the coupled inductors and capacitors used in the proposed CI-BZSB are derived. Expressions for the maximum step load change and SCR reverse recovery time are analysed. Without loss of generality,

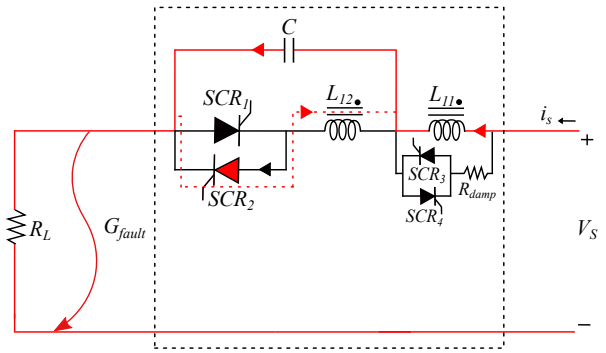


Fig. 6. Fault condition during reverse power flow operation.

the expressions are valid for the time interval before the conduction of damping resistor (R_{damp}) with time origined at the fault instant. Simulation parameters for this analysis are described in Table I.

A. Maximum Allowable Step Load Change / Minimum Fault Current Magnitude

The equivalent circuit of the CI-BZSB for the analysis, assuming negligible voltage drop across the SCR, is shown in Fig. 7. In this section, the limiting value of G_{fault} is calculated for the breaker to operate, which signifies the maximum allowable step load change or minimum fault current magnitude. The inductor windings are assumed to be strongly coupled implying that the coupling coefficient is $K = 1$. Using Kirchoff's Voltage Law, loop equations can be derived. Applying the Laplace transform to these equations and using initial conditions specified as,

$$V_c(0) = 0 \tag{1}$$

$$I_1(0) = I_2(0) = I_{load} = \frac{V_S}{R_L} \tag{2}$$

Then, $I_2(s)$ can be expressed as a function of circuit components in $s-$domain:

$$I_2(s) = \frac{(as^2 + bs + c)}{s(ds^2 + es + f)} \tag{3}$$

where,

$$a = C(L_{12} + M)I_{load}(R_f \parallel R_L) - CMV_s \tag{4}$$

$$b = (L_{11} + L_{12} + 2M)I_{load} \tag{5}$$

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Source Voltage, V_s	270 V
Inductance, L_{11}	100 μH
Inductance, L_{12}	100 μH
Capacitance, C	220 μF
Load Current, I_L	90 A

$$c = V_s \tag{6}$$

$$d = CL_{12}(R_f \parallel R_L) \tag{7}$$

$$e = L_{11} + L_{12} + 2M \tag{8}$$

$$f = R_f \parallel R_L \tag{9}$$

$$M = \sqrt{L_{11}L_{12}} \tag{10}$$

$$R_f = (G_{fault})^{-1} \tag{11}$$

During the fault instant, the SCR experiences a dip in current, shown in Fig. 8. This phenomena can also be verified by taking the inverse Laplace transform of the above equation. Criteria for the circuit breaker to trip can be calculated using the initial value theorem on $I_2(s)$ and imposing it to be less than zero, which is given by:

$$G_{fault} \geq \frac{L_{12}}{MR_L}\ \Omega^{-1} \tag{12}$$

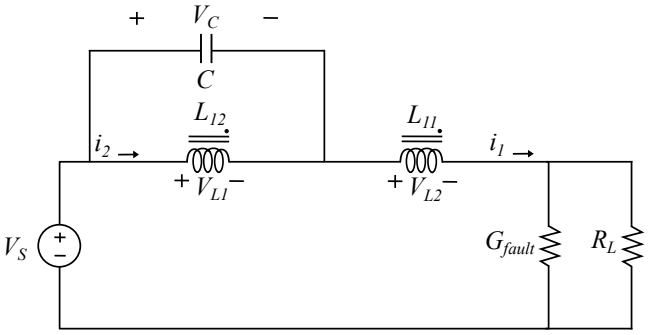


Fig. 7. Equivalent circuit of CI-BZSB.

Expression (12) can be used for designing the CI-BZSB inductors to satisfy the step load change requirement depending on application. Substituting the values of the parameters specified in Table I into (12), the limiting value of G_{fault} is calculated as 0.33 Ω^{-1}. Simulation results for different values of fault conductance are shown in Fig. 8, where the fault conductance is connected to the system at time $t = 2$ ms.

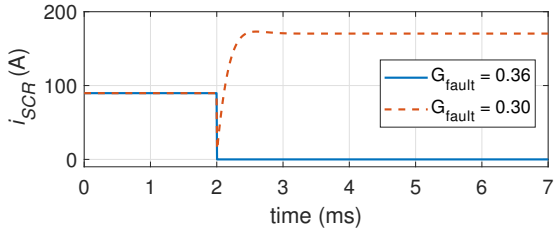


Fig. 8. SCR current during a step change in the load.

B. SCR Reverse Recovery Time

Once the SCR is commutated, a reverse voltage has to be applied across the device for a certain time interval to prevent false turning on of the device. During this interval, the device undergoes a reverse recovery of the charge carriers. Similar analysis can be done to calculate $V_{scr}(s)$ across the device. Taking the inverse laplace transform of $V_{scr}(s)$, the variation of voltage with time can be calculated as,

$$v_{scr}(t) = \alpha + \frac{\beta\cos(\omega t)e^{-\delta t}}{L_{11}C} + \frac{(\gamma - \beta\delta)\sin(\omega t)e^{-\delta t}}{\omega L_{11}C} \quad (13)$$

where,

$$\alpha = V_s \quad (14)$$

$$\beta = (R_f \parallel R_L)I_{load}MC - V_sC(M + L_{11}) \quad (15)$$

$$\gamma = I_{load}(M + L_{11}) - V_sC(R_f \parallel R_L) \quad (16)$$

$$\delta = \frac{R_f \parallel R_L}{2L_{11}} \quad (17)$$

$$\omega = \sqrt{\frac{1}{L_{11}C} - \left(\frac{R_f \parallel R_L}{2L_{11}}\right)^2} \quad (18)$$

Equation (13) can be solved numerically using Newton-Raphson method to calculate the instant t_{off} at which $v_{scr}(t) = 0$. t_{off} represents the time interval during which voltage across the SCR is negative. The value of t_{off} is calculated for different values of inductors and capacitor, shown in Fig. 9. Inductors L_{11} and L_{12} are assumed to be equal in this analysis. Inductors and capacitor should be designed such that t_{off} is greater than the turn off time value specified in the datasheet of the SCR. Inverter grade SCRs with turn off times in the range of few μs are preferred as it reduces the size of inductors and capacitor in the circuit.

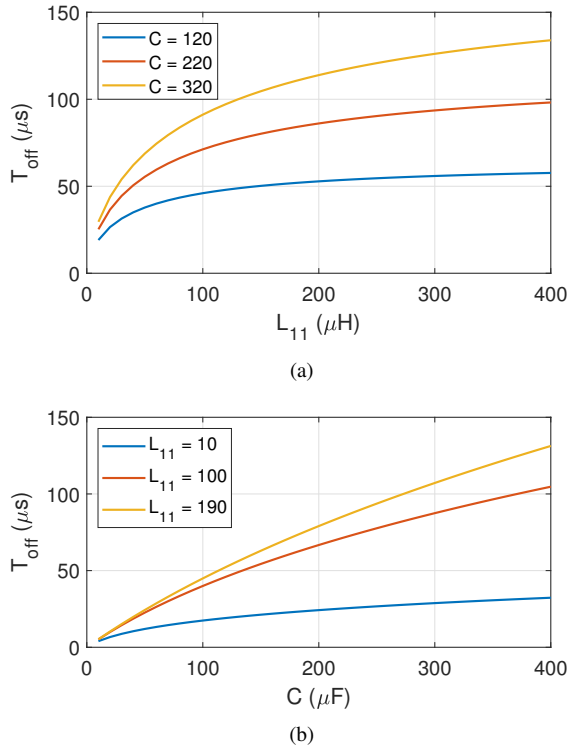


Fig. 9. Variation in t_{off} versus variation in inductance and capacitance.

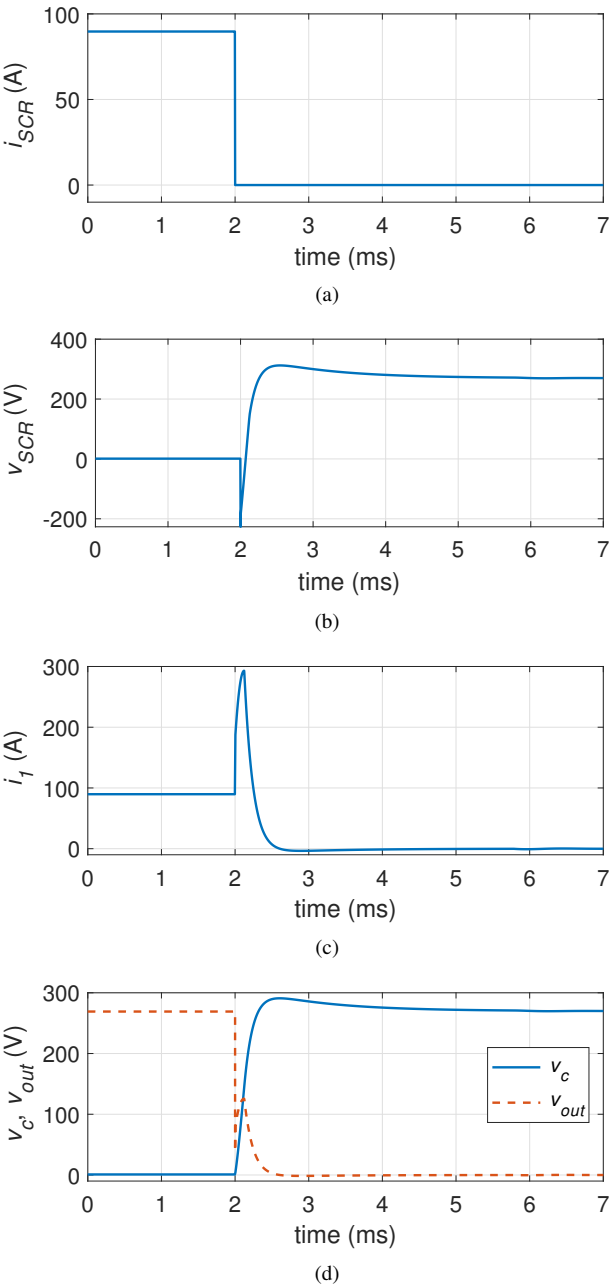


Fig. 10. Simulation results for a fault condition.

Simulation results for a fault initiated at $t = 2$ ms is shown in Fig. 10. The fault is initiated with G_{fault} of value 2 Ω^{-1}, which is capable of generating a very high current across the circuit. The CI-BZSB isolates the source and the fault

by forcing the current through the SCR to zero, as shown in Fig. 10(a), and thereby limiting the fault current. Once the SCR commutates, negative voltage developed across the device helps in the reverse recovery of charge carriers, as shown in Fig. 10(b). In the next interval, current resonates in the circuit until the voltage across the inductor L_{11} becomes negative, dissipating the stored energy in the damping resistor R_{damp} and SCR_3, shown in Figs. 10(c) and (d). Manual tripping for overload condition can be introduced by adding additional circuitry as suggested in [17], [28]. A comparison of the number of power devices and components in the proposed topology with already existing bidirectionally symmetric topologies is shown in Table II.

TABLE II
TOPOLOGIES COMPARISON BASED ON NUMBER OF COMPONENTS

Topology	Power Semiconductor Devices	Inductors	Capacitors	Ref.
Fig. 1	4	2	3	[23]
Fig. 2	5	2	2	[24]
Fig. 3(b)	4	4	1	[25]
–	4	3	1	[26]
Fig. 4	2	2	1	–

V. CONCLUSION

In this paper, a coupled-inductor-based bidirectional ZSB topology has been presented, which achieves a reduction in the number of components and losses. The use of coupled inductors reduces the weight and size of the breaker. Expressions for maximum allowable step load change and SCR reverse recovery time are derived and analysed for proper sizing of inductors and capacitor. Additionally, the ZSB can distinguish between step load change and fault condition, enabling self-directed protection of a dc system. Performance of the topology is verified for both the conditions using SPICE and MATLAB/Simulink simulation.

ACKNOWLEDGMENT

This work is jointly funded by the National Research Foundation (NRF) of Singapore, Rolls-Royce Singapore Pte. Ltd, and Nanyang Technological University, Singapore.

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