Heterogeneous Integration of GaN and BCD Technologies and Its Applications to High Conversion-ratio DC-DC Boost Converter IC

Fanyi Meng, *Member*, *IEEE*, Don Disney, *Fellow*, *IEEE*, Bei Liu, Yildirim Baris Volkan, Ao Zhou, Zhipeng Liang, Xiang Yi, Susai Lawrence Selvaraj, Lulu Peng, Kaixue Ma, *Senior Member*, *IEEE*, and Chirn Chye Boon, *Senior Member*, *IEEE*

***Abstract*—This paper presents a novel technology for the integration of GaN power devices with silicon control circuits. It comprises stacked gallium nitride (GaN) power transistors and Bipolar-CMOS-DMOS (BCD) circuits. It leverages on both advantages of the high-voltage low-loss GaN devices and the high-integration BCD circuits. Using conventional manufacturing, packaging, and assembly techniques and equipment, the proposed technology is technology transferrable and applicable for commercial power electronic applications. To validate the concept, a 3.3V-to-70V DC-DC boost converter is designed, implemented, and verified experimentally. It features conversion efficiency of 70.3%, output power of 1.68 W, and compact size of 0.32×0.18 cm².**

***Index Terms*—Boost Converter, CMOS DC-DC converter, Complementary-metal-oxide-semiconductor (CMOS), Gallium nitride (GaN), Heterogeneous integration, High Conversion-ratio, Integrated Circuits (ICs)**

I. INTRODUCTION

DRIVEN by advancement of semiconductor technologies and *Moore's Law*, the 3D integrated ICs especially heterogeneous integration of III-V semiconductors and silicon process becomes a hot research area in the past years. Among them, the integration of high-voltage gallium nitride (GaN) semiconductor and silicon (Si) complementary-metal-oxide-semiconductor (CMOS) becomes a promising platform for the advanced microsystem developments [1-5].

In power electronics, the heterogeneous integrated circuits (ICs) were explored in the area of power converters recently [1, 2]. Advantages of circuit compactness and function complexity over conventional monolithic designs [6, 7] were demonstrated.

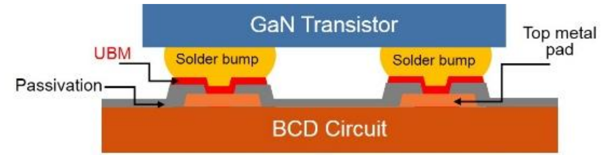

Fig. 1 Cross-section sketch view of the GaN2BCD™ technology.

Fig. 2 Design flow of the GaN2BCD™ technology.

In this paper, a new GaN and Si heterogeneous integration technology is proposed. The detailed design flow and utilized devices/process are illustrated in Section II. Based on the technology, a high conversion-ratio DC-DC boost converter is designed and implemented in Section III [8]. Measured results show superiorities in terms of integration level, output power level, efficiency, and form factors.

II. THE GAN2BCD™ TECHNOLOGY

This work is enabled by the GLOBALFOUNDRIES GaN2BCD™ Technology, by which the GaN power transistors are mounted directly on top of a Bipolar-CMOS-DMOS (BCD) circuit via solder bumps, as shown in Fig. 1. It is noteworthy that the GaN2BCD™ technology is transferable to the generic combinations of high-performance GaN/GaAs/InP devices and high-integration CMOS/BiCMOS/ BCD chips.

A. *GaN2BCD™ Design Flow*

Fig. 2 gives the design procedures. First, it is important to co-design the BCD circuits and GaN devices with circuit models, and carefully considering the parasitic effects of the

TABLE I
TYPICAL CHARACTERISTICS OF THE EPC2036 GAN FET

Parameter	Test Condition	Typical Value
$R_{DS(ON)}$ (Drain-source on resistance)	V_{GS} = 5 V, I_D = 1 A	50 mΩ
$V_{GS(TH)}$ (Gate threshold voltage)	V_{DS} = V_{GS}, I_D = 0.6 mA	1.4 V
V_{DS_MAX} (Maximum drain-source voltage)	Continuous	100 V

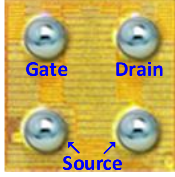

Fig. 3 Micrograph of EPC2036 eGaN® FET in passivated die form with solder bumps [9]. (Die Size: 0.9×0.9mm^2)

solder bumps and the thermal dissipation of the GaN transistors to the BCD circuits. After the BCD wafer is processed, an under-bump metallization (UBM) layer is formed on the top metal of BCD wafer. Then the GaN transistors are flip-chip soldered directly on top of the BCD top metallization using the die-to-wafer transfer (D2W) assembly, followed by associated packaging and system-level testing. The integrated design environment and entire fabrication process are provided within the GaN2BCD™ Technology.

B. GaN Power Transistor

In this prototype, the enhancement-mode (normally-off) EPC2036 GaN FET [9] is selected as the power transistor to validate the proposed technology and design flow practically. With the enhancement-mode nature, the associated driver circuit can be designed with nominal positive PMW signals without additional negative voltage generation circuitry [1, 2].

Table I summarizes the typical device characteristics. The small drain-source on resistance $R_{DS(ON)}$ of only 50 mΩ is the main advantage to reduce the conduction loss and hence improve the system efficiency. The gate threshold voltage $V_{GS(TH)}$ of 1.4 V provides the circuit design guide for the BCD driver. It is also noted that the device is capable to support converting operation up to 100 V.

Fig. 3 shows the die micrograph of the EPC2036 GaN FET with solder bumps. It has a size of 0.9×0.9 mm^2. It is noted that multiple dies can be parallel connected for larger conduction current to meet the design requirements.

C. BCD Process

The GLOBALFOUNDRIES 0.18-μm BCDLite™ process is used as the driver implementation platform. It features bipolar transistors, 1.8/5 V CMOS MOSFEFs, and high voltage (up to 65V) LDMOS. To cope with the EPC2036 control voltage (nominal V_{GS} = 5 V), the 5-V MOSFETs are utilized in implementing the pulse-width modulation (PMW) driver. On-chip metal-insulator-mental (MIM) capacitors and ESD

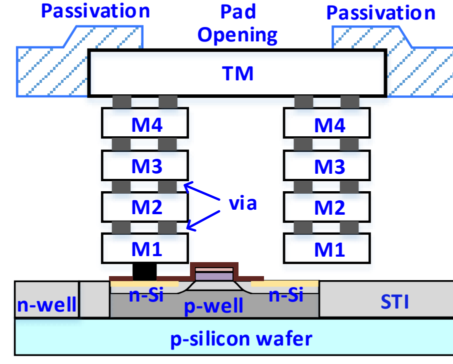

Fig. 4 Cross-sectional back-end-of-line (BEOL) metal stack of the GF's 0.18-μm BCDLite™ process. (STI: Shallow trench isolation)

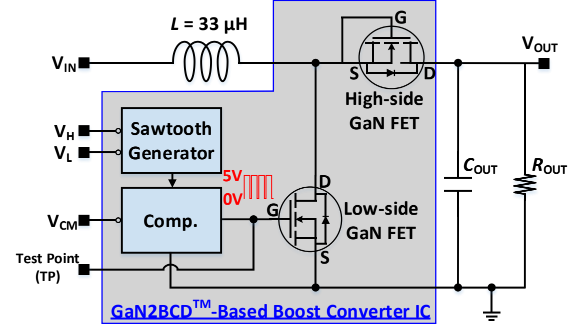

Fig. 5 Schematic of the 3.3-to-70 V boost converter prototype.

circuits are designed and used in the driver implementation. As shown in the cross-sectional metal stack (Fig. 4), the top metal (TM) are designed with two pad opening types, i.e. the octagonal opening structure used as the flip-chip pads soldered to the GaN devices and the square opening structure used as the wire-bonding pads to the printed evaluation board. The shallow trench isolation (STI) layer mitigates the electric current leakage between adjacent semiconductor device components, thus enhancing the circuit performance.

III. A 3.3-TO-70 V BOOST CONVERTER PROTOTYPE

To validate the GaN2BCD™ technology, an open-loop 3.3-to-70 V high conversion-ratio boost converter is designed, fabricated, and measured.

As shown in Fig. 5, the prototype comprises the sawtooth generator and comparator circuits in BCD process, two EPC2036 GaN devices, and off-the-shelf inductors and capacitors. Following the design procedures in Fig. 2, the sawtooth generator and comparator are firstly designed to provide the square-wave gate driving signal. External pins V_H and V_L tunes the frequency of the sawtooth waveform, which is 9.5-100 kHz in this design. The V_{CM} is the comparison reference of the sawtooth waveform and determines the duty cycle of the driving signal. Using 5-V MOSFET, the circuits provides a 0-5 V rail-to-rail duty-cycle controllable driver for the power transistors. A testing pin (TP) is reserved to check the functionality of the BCD chips.

The low-side GaN FET is the power transistor, and the

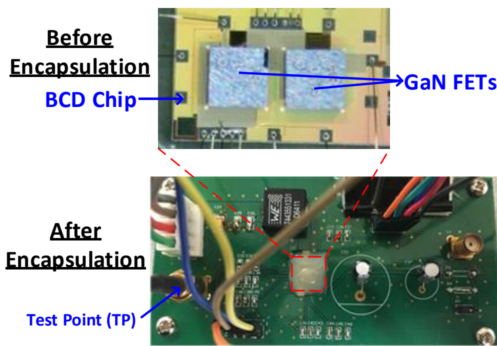

Fig. 6 Photographs of the boost converter prototype IC before encapsulation (top) and its evaluation board (bottom).

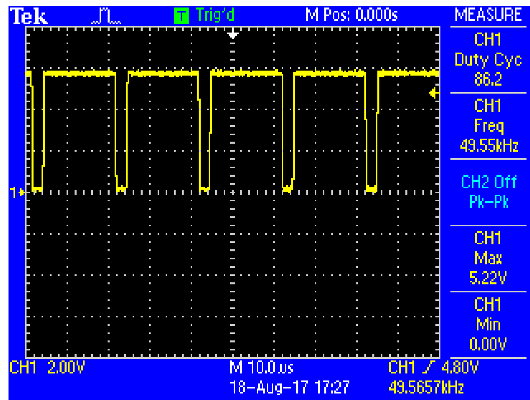

Fig. 7 Measured driving signal example at 86% duty-cycle and 49.5 kHz.

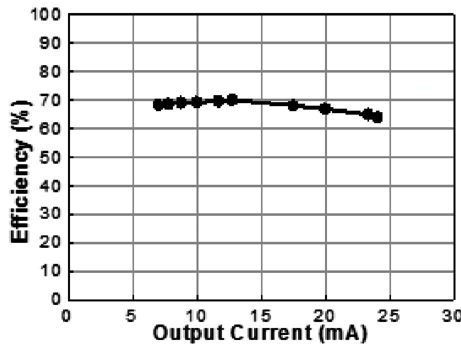

Fig. 8 Measured conversion efficiency versus output current.

high-side one is configured as boost diode with G-S connection for Anode and D for Cathode. Off-the-shelf components are used as boost inductor and filtering capacitors. Rheostat and resistor in series is used for testing the output voltages under various output current conditions. After UBM and D2W assembly, the converter prototype IC is obtained as in Fig. 6. It occupies an area of 0.32×0.18 cm^2 including wire-bonding pads.

The measurement is performed with dc power supplies and high-impedance oscilloscopes. At normal operation, the BCD driver circuits draws 2.1 mA current from a 5-V supply. Measured at the reserved TP in Fig. 5 and 6, Fig. 7 shows a driving signal example at 86% duty-cycle and 49.5 kHz generated by the BCD driver. By varying the duty-cycle and load resistance, the testing input/output currents are recorded under 3.3 V input and 70 V output voltages. Based on the raw data, the conversion efficiency is calculated and plotted in Fig. 8, which is 63.6% to 70.3%. The maximum power delivery capability is 1.68 W.

TABLE II
COMPARISON WITH OTHER INTEGRATED DC-DC BOOST CONVERTERS

Ref	Tech.	Boost Diode	V_{IN}/V_{OUT} (V/V)	$P_{OUT,MAX}$ (W)	η_{MAX} (%)	Area (cm×cm)
[1]	GaN + CMOS + IPD	Int. #	12/18	4.16	47.3	0.94× 0.98
[6]	80 V BCD	OTS *	3.3/80	0.35	53	0.1× 0.1
[7]	80 V BCD	OTS *	3.3/70	0.3	52	not mentioned
This Work	GaN + BCD	Int. #	3.3/70	1.68	70.3	0.32× 0.18

Integrated * Off-the-shelf

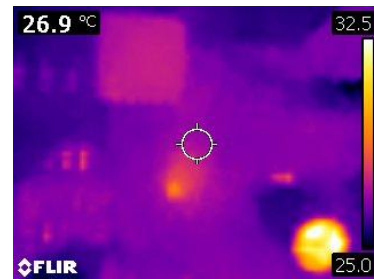

Fig. 9 IR image of the evaluation board top view after 30 mins operation.

IV. COMPARISON AND DISCUSSION

Table II shows the performance comparison with other integrated DC-DC boost converters. This work demonstrates the advantages of high integration level, high conversion ratio, large output power, high efficiency, and compact size. In fact, one key advantage of this heterogeneous integration technology is that the gate driver is placed in very close proximity to the gate of the GaN HEMT and thus the parasitic inductance between the driver and the gate of the HEMT is reduced by more than one order of magnitude, achieving parasitic inductance values under 0.1 nH compared to several nH for a typical PCB-integrated solution.

However, two concerns arise during our circuit design and implementation. First, the heat dissipation of both the BCD and GaN transistors must be handled by the BCD substrate/package. To fully consider the influences, we used thermal management software *ANSYS Icepak* to simulate the temperature changes on the BCD chip surface due to GaN devices, and incorporate the changes in the driver design process. In Fig. 9, the IR image shows a maximal surface temperature is 32.5 ℃, which is acceptable in industrial applications.

The second concern is the total thickness of stacked GaN transistors and BCD may pose packaging limitations. In this prototype, the added thickness of GaN transistor and solder

bump is 815 μm. Thinning of the BCD and/or GaN transistor substrates may be required depending on the final packaging solution.

V. Conclusion

In this paper, a DC-DC boost converter was designed and fabricated using the GLOBALFOUNDRIES GaN2BCD^{TM} technology. It features direct integration of a silicon BCD control circuit with two GaN power transistors, high conversion ratio (3.3-to-70 V), large output power, high conversion efficiency, and compact size. The GaN2BCD^{TM} technology is a promising platform for power conversion applications.

References

[1] M. J. Liu and S. S. H. Hsu, "A miniature 300-MHz resonant DC-DC converter with GaN and CMOS integrated in IPD technology," *IEEE Trans. Power Electron.,* vol. PP, pp. 1-1, 2018.

[2] E. Aklimi, D. Piedra, K. Tien, T. Palacios, and K. L. Shepard, "Hybrid CMOS/GaN 40-MHz maximum 20-V input DC-DC multiphase buck converter," *IEEE J. Solid-State Circuits,* vol. 52, pp. 1618-1627, 2017.

[3] D. S. Green, C. L. Dohrman, J. Demmin, Y. Zheng, and T. H. Chang, "A revolution on the horizon from DARPA: Heterogeneous integration for revolutionary microwave/millimeter-wave circuits at DARPA: Progress and future directions," *IEEE Microw. Mag.*, vol. 18, pp. 44-59, 2017.

[4] T. Ishibashi, M. Okamoto, E. Hiraki, T. Tanaka, T. Hashizume, D. Kikuta, et al., "Experimental validation of normally-on GaN HEMT and its gate drive circuit," *IEEE Trans. Ind. Appl.*, vol. 51, pp. 2415-2422, 2015.

[5] T. E. Kazior, R. Chelakara, W. Hoke, J. Bettencourt, T. Palacios, and H. S. Lee, "High performance mixed signal and RF circuits enabled by the direct monolithic heterogeneous integration of GaN HEMTs and Si CMOS on a silicon substrate," in *Proc. IEEE Compound Semic. Integ. Circuit Symp.*, 2011, pp. 1-4.

[6] Y. Y. Yang, S. W. Wang, C. Y. Hsieh, T. C. Huang, Y. H. Lee, and K. H. Chen, "Power management with a low-ripple high-conversion-ratio 80-V output voltage boost converter for avalanche photodiode system," *IEEE Trans. Ind. Electron.,* vol. 60, pp. 2627-2637, 2013.

[7] *76V, 300mW boost converter and current monitor for APD bias applications (3 ed.)* [online]. Available: https://datasheets.maximintegrated.com/en/ds/MAX15059.pdf

[8] D. Disney, F. Meng, X. Yi, and C. C. Boon, "Integrated DC-DC boost converter with gallium nitride power transistor " US Patent 15/648,105, Dec. 2017.

[9] E.P.C. Corporation, "EPC2036 – Enhancement Mode Power Transistor," *EPC2036 datasheet,* April 2015.