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A Design Methodology and Analysis for Transformer-Based Class-E Power Amplifier

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Abstract: This paper proposes a new technique and design methodology on a transformer-based Class-E complementary metal-oxide-semiconductor (CMOS) power amplifier (PA) with only one transformer and two capacitors in the load network. An analysis of this amplifier is presented together with an accurate and simple design procedure. The experimental results are in good agreement with the theoretical analysis. The following performance parameters are determined for optimum operation: The current and voltage waveform, the peak value of drain current and drain-to-source voltage, the output power, the efficiency and the component values of the load network are determined to be essential for optimum operation. The measured drain efficiency (DE) and power-added efficiency (PAE) is over 70% with 10-dBm output power at 2.4 GHz, using a 65 nm CMOS process technology.

Keywords: Class-E; transformer-based; silicon CMOS; wireless communication; power amplifier

1. Introduction

With the explosive growth of wireless and mobile communication systems adoption, the demand for compact, low-cost and low power portable transceiver has increased dramatically. One of the technical issues that is generally encountered for the portable transceivers is the limited lifetime of the battery. The power amplifier (PA) is typically the most power-hungry building block in the transceiver. Therefore, the design of a high-efficiency radio frequency (RF) PA is the most important solution to overcoming the battery lifetime limitation in portable communication systems. The class-E PA as depicted in Figure 1 has a maximum theoretical efficiency of 100%. It consists of a single output transistor that is driven as a switch and a passive load network. The passive load network is designed to minimize the drain voltage and current waveforms from overlapping [1], which causes output power loss. The major difference between class-E PA and others (e.g., Classes A, B, AB, C, D and F) is that it incorporates the parasitic drain-source capacitance [2] as part of the passive load network design, which is an advantage especially in CMOS design. In class-E PA, the circuit operation is determined by the transistor when it is on, and by the transient response of the load network when the transistor is off [2]. It greatly reduces the transistor power losses during the off-to-on transition of the device, resulting in high efficiency. To minimize these power losses, the following two conditions need to be met [1–3]:

$$V_{DS}(t = t_1) = 0 \quad (1)$$

$$\frac{dV_{DS}}{dt}|_{t=t_1} = 0 \quad (2)$$

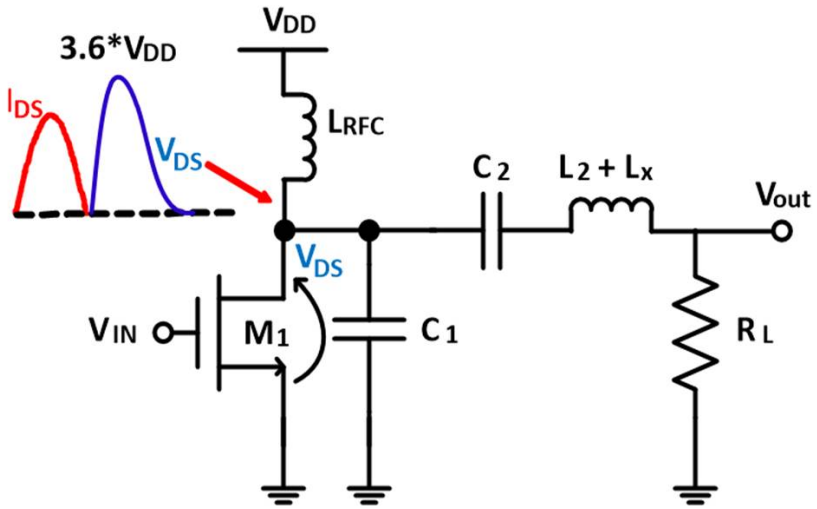


Figure 1. ConventionalClass-E power amplifier (PA) using NMOS transistor with radio frequency RF-choke and series LC network.

In the conventional class-E PA, the RF-choke (RFC) is assumed to have a sufficiently high reactance and the output current through the load resistor R_L is essentially a sinusoid at fundamental frequency. Under these conditions, the analytical design equations can be derived and are given by [4]:

$$R_L = 0.5768 \cdot \frac{V_{DD}^2}{R_L} \tag{3}$$

$$C_1 = 0.1836 \cdot \frac{1}{\omega R_L} \tag{4}$$

$$L_x = 1.1525 \cdot \frac{R_L}{\omega} \tag{5}$$

where $\omega = 2\pi$f, and f= 2.4 GHz, V_{DD} and Pout are the operating frequency, supply voltage and the desired output power, respectively. The combination of $L_2 = 0.34$ nH and $C_2 = 12.88$ pF forms a harmonic filter that is tuned to the operating frequency of the class-E PA. The major drawback of the class-E PA is the presence of high drain voltage when the switch is opened. This value is, in the ideal case, given by [5]

$$V_{DS,max} = 2\pi[\frac{\pi}{2} - arctan(\frac{\pi}{2})] \cdot V_{DD} \approx 3.562 \cdot V_{DD} \tag{6}$$

and the value of $V_{DS,max}$ threatens the transistor's reliability, especially in CMOS technology, due to its low breakdown voltage. The maximum drain voltage can be alleviated by using a finite inductance instead of RF-choke, whereby the peak voltage can be reduced to $2.5 \cdot V_{DD}$ [6]. This paper presents an analysis and design methodology on transformer-based class-E PA involving the circuit equations, the relationships among the transistors switching "on-off" and the load quality factor (Q) at the resonant frequency (f_o) of the load network, The basic performance and design parameters are discussed in this paper as well. Experimental results are demonstrated and they are in good agreement with the theories.

2. Methodology and Implementation on Transformer-Based Class-E PA

2.1. Design of the Inductors with Magnetic Coupling

The proposed transformer-based class-E PA with a finite DC-feed inductor is shown in Figure 2. The two coupled inductors (DC-feed and output series inductors) are inter-wound to form a

transformer. The amount of coupling between the two inductors is quantified by defining a mutual magnetic coupling denoted as k, which can take on any value between one and zero. For the two coupled inductors (L_{DC} and $L_2 + L_X$), k and mutual inductance (M) are related by:

$$k = \frac{M}{\sqrt{L_{DC}(L_2 + L_X)}} \tag{7}$$

A simplified transformer model is shown in Figure 3. This is modeled as two inductors, but with the addition of k between them and inter-winding capacitance C_{IW} from input to output [7].

Note that the open-circle dots on inductors in Figure 2 are placed such that if current flows in the indicated direction, then there is a summation of magnetic fluxes [8]. Thus, the inductance reinforces itself and for a given inductance, the designs of both the L_{DC} and $L_2 + L_X$ have shorter lengths (shortened approximately by 437 um) which implies lesser series resistance R_S. This would allow a higher quality factor Q to manifest in the on-chip inductors, which translates to higher efficiency. In basic physics, the Q is defined as (8), where Z_{ind} is the impedance of the inductor.

$$\begin{aligned} Q &= 2\pi \frac{Energy\ Stored}{Energy\ Dissipated\ per\ Cycle} \\ &= \frac{|Im(Z_{ind})|}{|Re(Z_{ind})|} \\ &= \frac{\omega L}{R_S} \end{aligned} \tag{8}$$

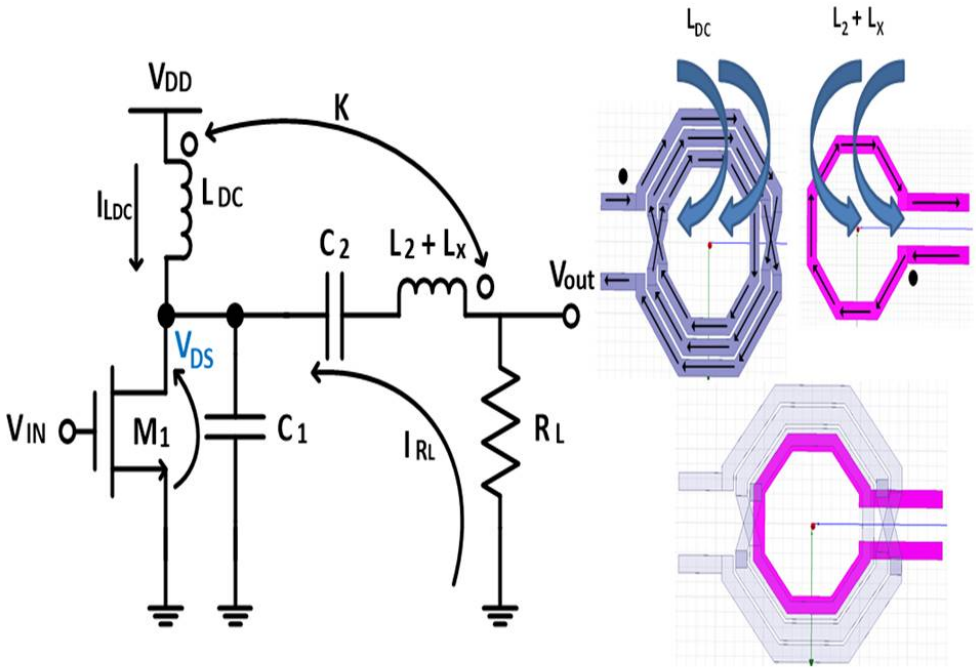


Figure 2. Transformer-Based Class-E PA: magnetic coupling and determining correct dot placement.

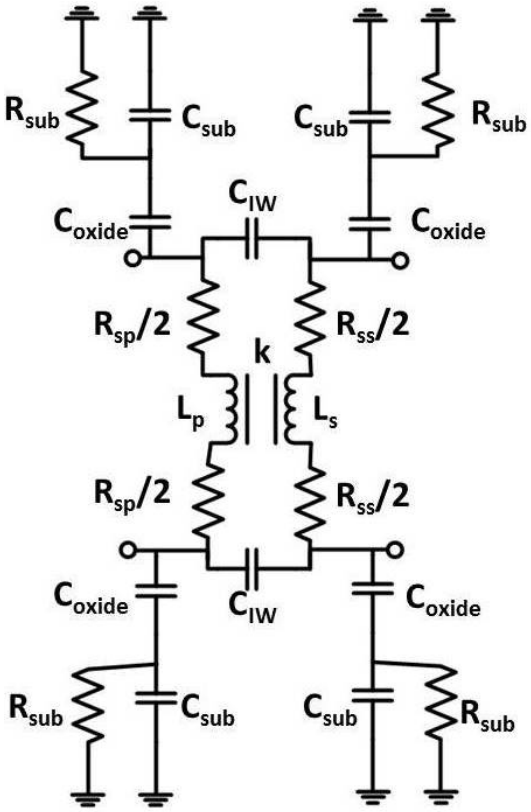


Figure 3. Basic model of transformer.

According to Faraday's law of induction [9] states that the induced electro-motive-force (ε) through a coil is equal to the negative of the time rate of change of the magnetic flux (ϕ_B):

$$\varepsilon = -\frac{d\phi_B}{dt} \tag{9}$$

The ϕ_B through the coil is proportional to the magnetic field (B), which in turn is proportional to the current I in the coil.

$$\phi_B \propto B \quad ; \quad B \propto I \quad \Rightarrow \quad \phi_B \propto I \tag{10}$$

From Equations (9) and (10), we conclude that the induced ε is proportional to the negative of the time rate of change of the current.

$$\varepsilon \propto -\frac{dI}{dt} \quad \Rightarrow \quad \varepsilon = -L\frac{dI}{dt} \tag{11}$$

where L is the inductance of the coil. For a given rate of change of the current, the induced back emf increases with the inductance. Therefore, the inductance of a coil is a measure of its opposition to a change in current. Using Equation (11), we can express the inductance as:

$$L = -\frac{\varepsilon}{dI/dt} \tag{12}$$

Equating Equations (9) and (11)

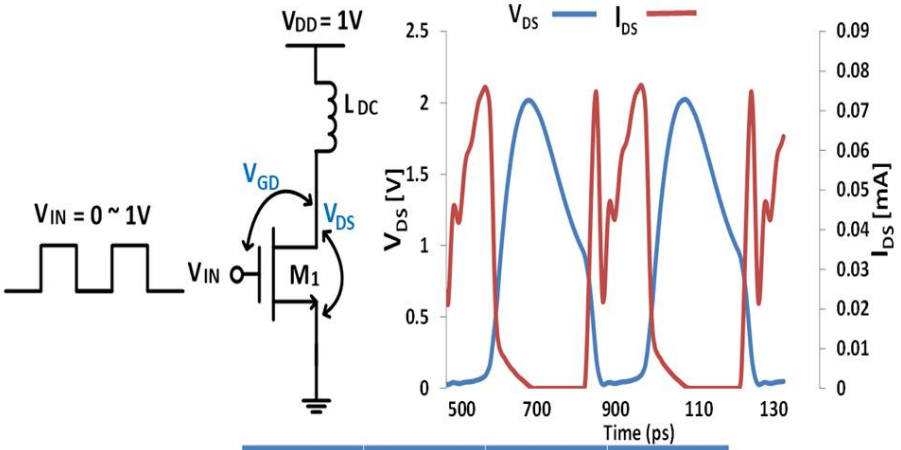
$$\varepsilon = -\frac{d\phi_B}{dt} = -L\frac{dI}{dt} \quad \Rightarrow \quad \frac{d\phi_B}{dt} = \frac{dLI}{dt} \quad \Rightarrow \quad \phi_B = LI \tag{13}$$

Therefore, the inductance of a coil is also given by

$$L = \frac{\phi_B}{I} \tag{14}$$

2.2. Design of the DC-Feed Inductance

There are two main reliability issues in the design of power amplifiers in submicron CMOS, namely oxide breakdown and the hot carrier effect. They increases the threshold voltage and, consequently degrades the devices' performance. The key property of class-E PA is separation of drain voltage and drain current in the time domain. In this regard, high voltage and high current never coincide and when the transistor starts to conduct current, the drain voltage is close to zero due to the load network. As such, the class-E PA is limited by the oxide breakdown but not the hot carrier effect. This will set limits for the maximum drain voltage equal to the oxide breakdown voltage of the NMOS transistor. A major drawback is the maximum voltage stress on the transistor, $V_{DS,max}$, which can be as high as $3.57 \cdot V_{DD}$. Using a finite inductance instead of an RF-choke, the peak voltage can be reduced to $2.5 \cdot V_{DD}$ as shown in Figure 4 [6]. A common practice [10] is to keep the maximum voltage drop across the transistor below two times the nominal supply voltage (V_{DDnom} = 1.2 V) to ensure reasonable device and circuit life-time.



	$V_{GS\,max}$	$V_{DS\,max}$	$V_{GD\,max}$
ON	V_{IN}	0	V_{IN}
OFF	0	$2.5*V_{DD}$	$2.5*V_{DD}$

Figure 4. Maximum voltage stresses on transistor M1 in both on and off states.

The class-E PAs can be categorized into two types according to the inductor's function: Class-E PA with RF-choke inductor or with DC-feed inductor. The proposed PA with a finite DC-feed inductor is shown in Figure 2. Using a finite DC-feed inductor instead of a large RF-choke in the class-E PA has several advantages [11] including:

- Greatly reduce the loss due to a smaller electrical series resistance
- A reduction in overall size and cost
- Simplifying the design of the matching network

2.3. Design of Inductors and Transformers

Among all the passive structures used in RF circuits, high-quality inductors and transformers are the most difficult to realize monolithically. In silicon, they suffer from the presence of lossy substrate and high-resistivity metal. Therefore, well-designed inductors and transformers are very crucial and they must exhibit the following properties [12]:

- Low series resistance in the primary and secondary windings
- High magnetic coupling between the primary and the secondary coils
- Low capacitive coupling between primary and the secondary coils
- Low parasitic capacitances to the substrate

To obtain an optimum design of monolithic transformer on silicon we must follow closely the suggestions and guidelines provided as follows:

1. To minimize the series resistance and the parasitic capacitance, the spiral is implemented in the top metal layer (which is the thickest) [13]
2. It is desirable to minimize the outer dimensions of inductors, and this can be accomplished by decreasing W (line width) or incresing N (numbers of turns) [14]
3. A diameter of 5 to 6 times W should be chosen for the inner opening to ensure negligible coupling [15]
4. Differential geometry (driven by differential signals) also exhibits a higher Q [16], because each half experiences its own substrate loss and it will be reduced by a factor of two
5. Choose a line spacing S of approximately three times the minimum allowable value for the particular technology being used to fabricate the design
6. As a general rule of thumb, Din (inner dimension) lower than 50 μm should be avoided unless it is mandatory to obtain very low inductance values ($L < 0.5$ nH) [17]
7. For multi-turn inductors, do not use very tight metal spacing (i.e., coil thickness/line spacing < 3) to limit the performance degradation as this will cause the proximity effects to become worse [18]

ANSYS High Frequency Structure Simulator (HFSS) was used to design and simulate the transformer structure and is shown in Figure 5. The primary inductor has an outer dimension of 187 μm and a thickness of 3.3 μm while the secondary inductor has an outer dimension of 122 μm and a thickness of 0.9 μm. Both of them have a line width of 12 μm. This geometry has better symmetry compared with traditional inductors (its S parameters look the same from either side).

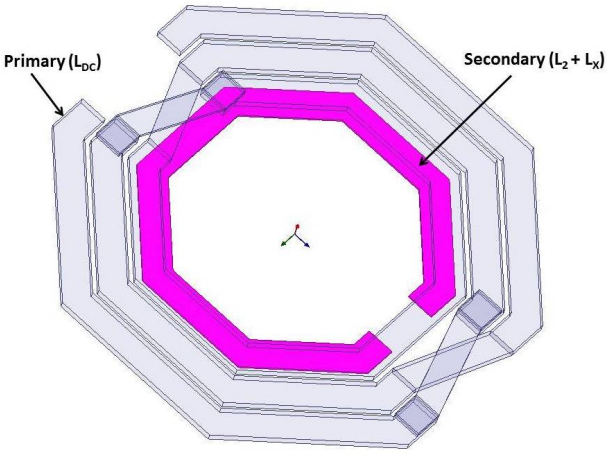


Figure 5. Schematic of on-chip transformer 3-D view

2.4. Transformer Layouts in Class-E PA

Another important aspect is to choose an appropriate transformer configuration to maximize the coupling between coils. Only two types provide acceptable performance; stacked [19] and interleaved [19,20] transformers. An interleaved transformer is built by two inductors fabricated using the same metal layer whose coils (i.e., metal layers) are laterally interleaved. The interleaved topology provides full symmetry but has poor magnetic coupling. A stacked transformer is made up of two identical inductors fabricated using different metal layers placed on top of each other. Stacked topology gives higher coupling factors, but the two inductors have different electrical parameters due to different metal layers.

The main advantages and drawbacks of these two configurations are presented in Table 1. The magnetic coupling between winding is measured by the magnetic coupling factor (k), which is typically around 0.7–0.9 for a monolithic transformer due to poor confinement of the magnetic flux.

Table 1. Advantages and drawbacks of interleaved and stacked configurations.

Configurations	Area	k	f_{SR}	Capacitance	Electrical Symmetry
Interleaved	Medium	Medium	Excellent	Excellent	Excellent
Stacked	Excellent	Excellent	Medium	Poor	Medium

The stacked transformer is adopted in this design to increase the quality factor Q, but at the expense of increased capacitance to the substrate and a resultant decrease in self-resonant frequency. This technique is of benefit for small inductors for which the substrate loss is not dominant and the design is at low enough frequency, safely away from the self-resonant frequency. Note that the magnetic fluxes through the two windings will renforce one another and the total inductance of the structure will be larger. As a result, the inductors will have a higher quality factor Q. The quality factor Q of the coupled inductors (Q of L_{DC} = 11.4; Q of $L_2 + L_X$ = 16.1), uncoupeld Q of L_DC and $L_2 + L_X$ are about 10 as shown in Figure 6.

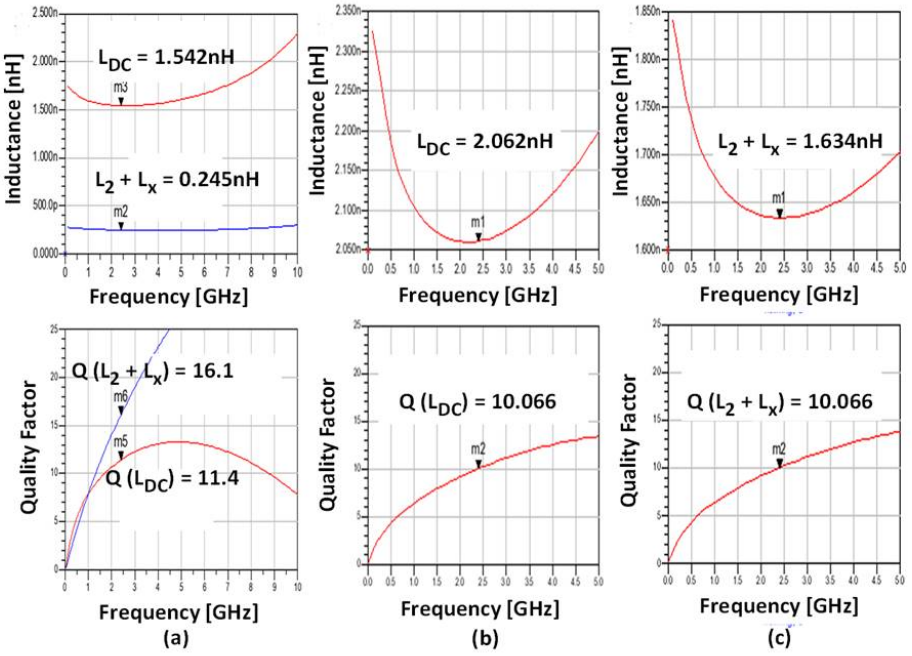


Figure 6. The quality factor plotted versus frequency for the inductors: (**a**) Coupling-inductors; (**b**) DC-feed inductor; (**c**) Output series inductor.

3. Measurement Results

The proposed methodology was implemented with a 2.4 GHz transformer-based class-E PA fabricated in GLOBALFOUNDRIES' 65 nm CMOS process, and it occupies an area of 0.49×0.43 mm^2 including the I/O pads. The microphotograph of the fabricated PA is shown in Figure 7 and the measurement results of the design, i.e., transformer-based class-E PA based on differential inductors topology, and conventional uncoupled class-E PA are illustrated in Figures 8 and 9 respectively. The simulation results are appended in the same figures as well.

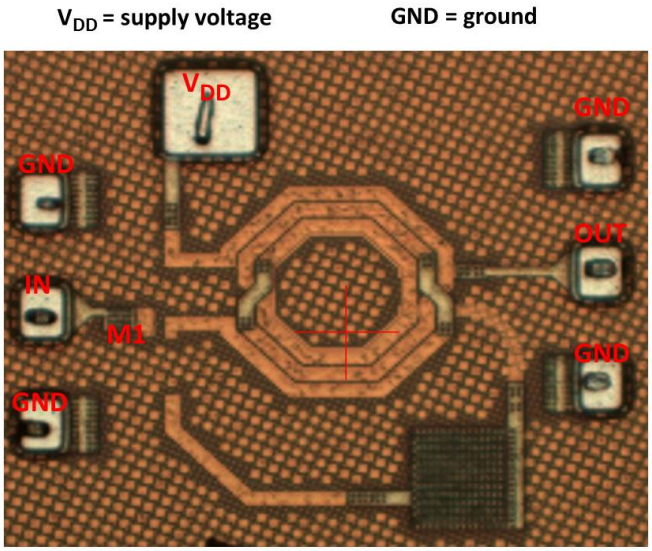


Figure 7. Microphotograph of the implemented power amplifier

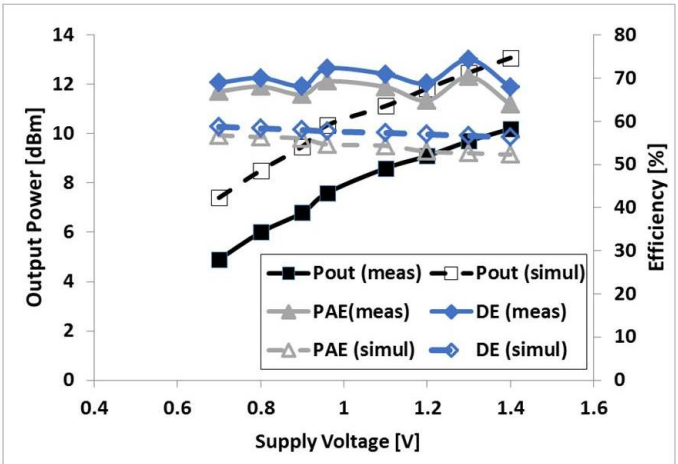


Figure 8. Transformer-based class-E PA: Output power, drain efficiency and power-added efficiency versus the DC supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey).

The measurements are performed for the PA using on-wafer probing with E4407B network analyzer and Cascade Elite 300. The large-signal behavior of the PA is characterized from 1.2 to 3.4 GHz in steps of 0.1 GHz. All large-signal measurements are presented as the mean from 4 die samples with the inclusion of cable and probe loss of 1 dB.

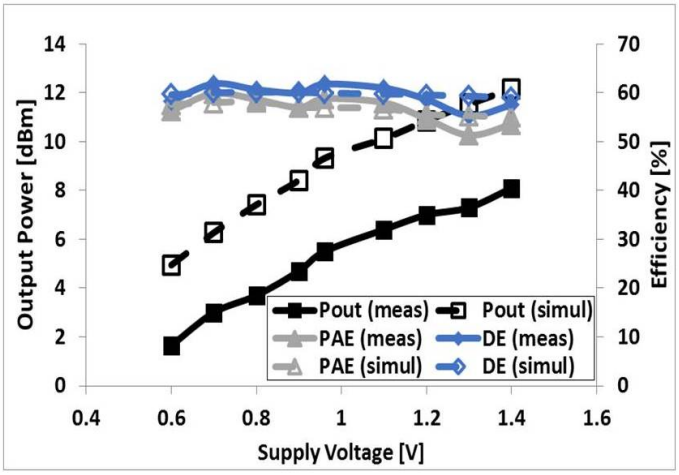


Figure 9. Uncoupled class-E PA: Output power, drain efficiency and power-added efficiency versus the dc supply voltage (measurement: solid black, blue and grey; simulation: dashed white, blue and grey). Drain efficiency (DE) and power-added efficiency (PAE)

In Figure 8 when V_{DD} = 1.4 V, the PA deliver an output power of 10-dBm, and maximum DE and PAE were measured as 74% and 70% at a frequency of 2.4 GHz. Figure 10 shows the output power, DE and PAE over the range from 2.3 to 3.4 GHz. As can be seen in Figure 10, the output power is reduced by 4.8 dBm over the frequency range. The hypothesis of this decrease is that it could be due to the skin effect which results in a higher series resistance at higher frequencies as well as the parasitic drain capacitance but investigation are still ongoing. The following Figure-of-Merit (FoM) [21] is used to compare the performance of the designed chip with state-of-the-art CMOS switch-mode PAs (SMPAs) [21–28]:

$$\text{FoM} = \frac{\text{PAE} \cdot \text{freq}\ [\text{Hz}]^{0.25}}{\text{chip size}\ [\text{mm}^2]} \tag{15}$$

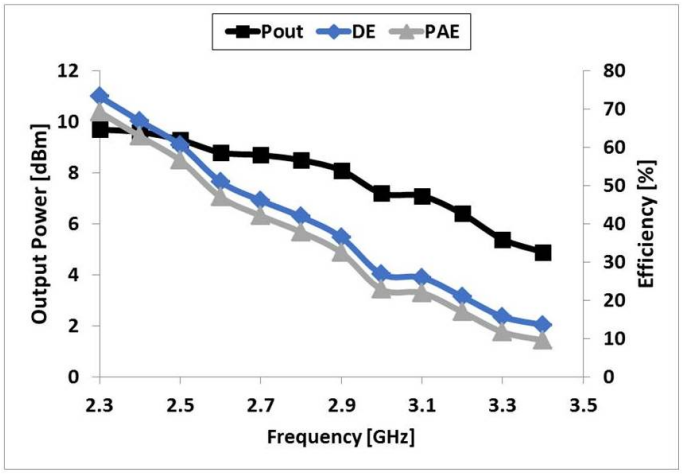


Figure 10. Transformer-based class-E PA: Measured output power, drain efficiency and power-added efficiency versus operating frequency.

Due to its high efficiency (PAE = 70%) as shown in Figure 8 and compact size (die area = 0.21 mm^2) including the I/O pads, the proposed design methodology implemented on this work, has a FoM of 735, which is the highest among all designs in comparison as shown in Table 2.

Table 2. Comparison of state-of-the-art class-E PA designs. Figure-of-Merit (FoM).

Reference	P_{out} [dBm]	PAE [%]	f [GHz]	Die Area [mm^2]	Process [nm]	FoM
[21]	28.7	48	2.3	1.2	90	121.74
[22]	5.7	55	2.4	1	130	100.37
[23]	30	60	2	0.3	65	423
[24]	31.5	51	1.8	1	130	111.23
[25]	29.6	51	1.8	1.5	180	70
[26]	21.7	37.9	2.6	1.21	250	70.7
[27]	22.3	49.5	5	0.235	250	560
[28]	29	38.7	1.8	1.53	350	52
This Work	10.7	70	2.4	0.21	65	735

4. Conclusions

In this paper, we presented a proposed methodology on the design of transformer-based class-E PA implemented in 65 nm CMOS technology. The class-E operating principles were reviewed and the design is based on transformer coupling effect to simultaneously reduce the chip area and improve the quality factor Q of the inductors. The methodology implemented allows the PA to deliver 10-dBm output power with 74% DE and 70% PAE at 2.4 GHz using the 65 nm CMOS process.

Author Contributions: A.L. conceptualized and designed the parameters; A.L. interpreted some results and wrote the paper; A.T. interpreted some of the results; Z.H.K. advised and proof-read the manuscript. K.M. provide simulation resources.

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Conflicts of Interest: The authors declare no conflict of interest.

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