NANYANG TECHNOLOGICAL UNIVERSITY

SINGAPORE

Design of RF Silicon on Insulator (SOI) Switches for Ultra Wideband Wireless Communication Applications

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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A thesis submitted to the Nanyang Technological University in partial fulfilment of the requirement for the degree of Doctor of Philosophy

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SUMMARY

RF switches are one of the key building blocks used in modern communication systems. The ability of RF switches to enable wideband or multi-band systems-on-chip and fully integrate with other circuits in the communication system is becoming increasingly important. On the other hand, the required performances of RF switches have become more stringent as frequency increases. Specifically, it is challenging to have good tradeoffs among insertion loss, isolation, power handling capability and size.

Diverging from the historical mainstream usage of III-V semiconductor-based material or silicon-on-sapphire (SOS) for RF application, high-resistivity trap-rich silicon-on-insulator (HR TR SOI) has emerged as today's substrate of choice, thanks to SOI reduced parasitic capacitance and substrate loss.

This research work focuses on ultra wideband RF switch design based on high-resistivity trap-rich SOI (HR TR SOI). Stress memorization technique (SMT) effects on ultra-wideband RF switch performance are investigated for the first time. Low insertion loss, high isolation, ultra-wideband (dc to 50 GHz) single-pole double-throw (SPDT) switch, single-pole four-throw (SP4T) switch and 2 x 2 double-pole double-throw (DPDT) switch matrix are designed with commercial 0.13-μm high-resistivity trap-rich SOI technology.

Based on the investigation, ultra-wideband SPDT and SP4T switches are designed on 0.13-μm HR TR SOI process, with thorough investigation on the channel mobility, channel length and gate bias effects on switch performance. It is found that SMT helps improve switch insertion loss from dc to 20 GHz for the proposed SPDT switches and from dc to 35 GHz for the proposed SP4T switch by improving the channel mobility and hence reducing

the on resistance. Moreover, the different channel length on the same process has prominent effects on the performance of the RF switches. When compared with the state of the arts, the designed SPDT switch, which is done based on excellent tradeoff among SMT, channel length and design optimization achieves the lowest insertion loss (< 1 dB at 30 GHz, < 2.1 dB at 50 GHz) over dc to 50 GHz, while the designed SP4T switch achieves the lowest insertion loss (< 1 dB at 10 GHz, < 1.4 dB at 20 GHz and < 2.6 dB at 35 GHz) over dc to 35 GHz. The active chip areas of the proposed SPDT and SP4T switches are compact with size of only 0.214 x 0.19 mm^2 and 0.36 x 0.19 mm^2, respectively.

In addition, two types of 2 x 2 double-pole double-throw (DPDT) switch matrixes are designed with the same technology. The legacy generation1 switch matrix (Gen1) in this technology is fabricated using the same SOI top silicon thickness as the proposed SPDT and SP4T switches. It achieves less than 2.5 dB insertion loss and higher than 32 dB isolation up to 30 GHz. Also, a novel generation2 switch matrix (Gen2) fabricated on recessed SOI top silicon is presented. The Gen2 switch exhibits less than 2 dB insertion loss and higher than 34 dB isolation from dc to 35 GHz.

Chapter 1

Introduction

1.1 Motivation

RF switches are widely used in these modern communication systems. From antenna switching, transmit-receive (T/R) switching, test & measurement, phase array, to signal conditioning. As the need of number of radio standards increases, need of the number and complexity of switches also increased. As shown in Figure 1-1 (courtesy of SOITEC), in a modern LTE smartphone front end block, to achieve multiple band application, a lot of switches are used, including antenna swap switch, PA mode switches, RX diversity switches, etc.

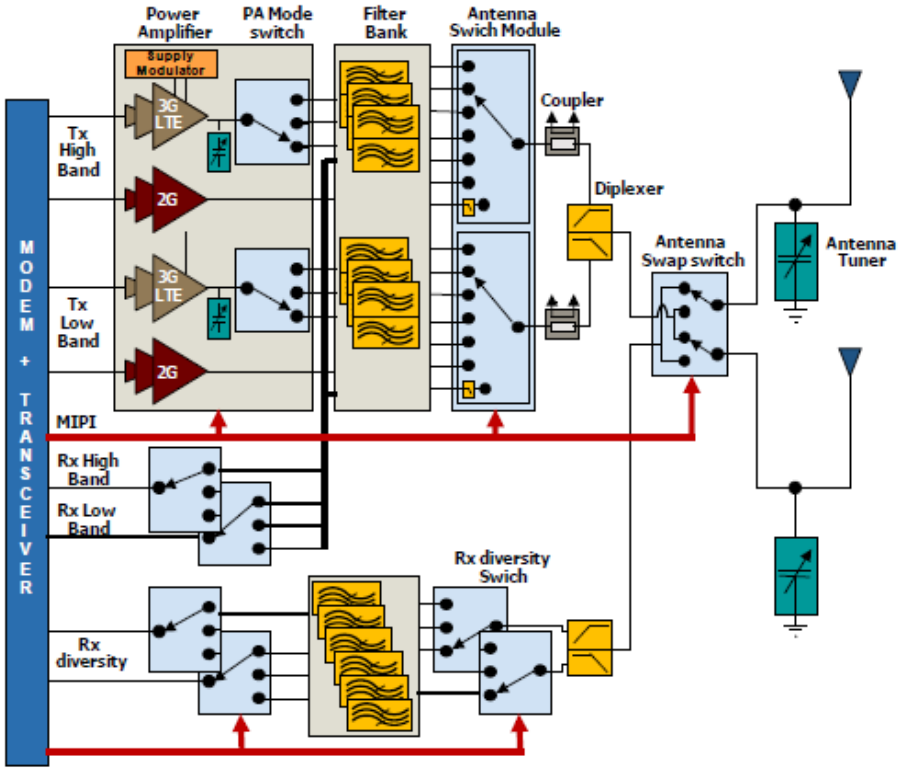


Figure 1-1 Front-end module (FEM) diagram of LTE

The ability of RF switches to fully integrate with other circuits in the communication system and operate over very wide bandwidth is becoming increasingly important to enable wideband or multi-band systems on chip. On the other hand, the required performances for RF switches including lower insertion loss, higher isolation and higher power handling capability and smaller size, which usually have to be tradeoffs among, have become more stringent. It becomes a big challenge to do good tradeoffs among these stringent required performances.

Historically, high performance RF switch design mostly uses GaAs pseudomorphic high electron-mobility transistors (pHEMT) III-V semiconductor-based processes, or silicon-on –sapphire (SOS) technologies. In recent years, by using high resistivity (HR) substrate, silicon-on-insulator (SOI) technology, has started to penetrate in the switch market, thanks to its reduced parasitic capacitance, reduced substrate loss and comparable isolation with GaAs pHEMT. The HR-SOI is now recognized to be one of the mainstream technology options for the RF system on chips, and HR-SOI switch is estimated to be more popular than other switch technologies in near future, as shown in Figure 1-2.

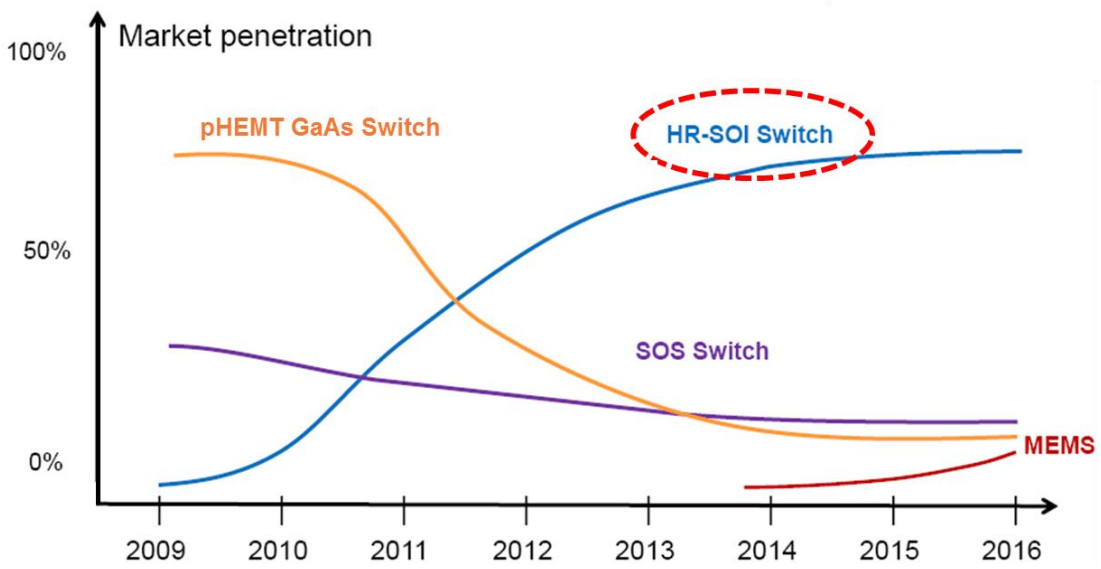


Figure 1-2 Market penetrations of different RF switch technologies

1.2 Thesis organization

In Chapter 1, the background of importance and the motivation of RF switch design are presented.

In Chapter 2, RF switch key parameters are introduced. RF switch type and common switch design techniques, including both low frequency (dc to 10 GHz) and high frequency switch (> 10 GHz) are reviewed.

In Chapter 3, SOI concept and its advantages over bulk substrate are introduced. SOI MOSFET type including partially depleted SOI and fully depleted SOI are presented, SOI substrate techniques including high resistivity and high resistivity trap rich SOI are also presented.

In Chapter 4, ultra wideband single-pole double-throw (SPST) design considerations including switch topology, switch transistor size and matching inductor effect on switch performance are studied. S-parameters of different SPST switches configurations, including series only, series-shunt and series-shunt with input output matching network, are simulated and analyzed. Based on simulation result, to achieve ultra wideband (dc to 70 GHz) application, series-shunt with input output matching network should be adopted, and switch transistor size and matching inductors should be optimized.

In Chapter 5, ultra wideband SPDT switch design are presented. The designed SPDT switches are based on series-shunt configuration with input and output matching network. Stress memorization technique (SMT) implementation on SPDT switch design is reported for the first time. With thorough investigation on the channel mobility, channel length and gate bias effects on switch performance. It is found that SMT helps improve switch insertion loss from dc to 20 GHz for the proposed SPDT switches by improving the channel mobility and hence reducing the on resistance. Moreover, the different channel length on the same process

has prominent effects on the performance of the RF switches. When compared with the state of the arts, the designed SPDT switch, which is based on excellent tradeoff among SMT, channel length and design optimization achieves the lowest insertion loss (< 1 dB at 30 GHz, < 2.1 dB at 50 GHz) over dc to 50 GHz.

In Chapter 6, ultra wideband SP4T switch design based on series-shunt with input and output matching network are presented. Thorough investigations are done on the channel mobility (by implementation of SMT), channel length and gate bias effects on SP4T switch performance. Similar to SPDT switch, it is also found that SMT helps improve switch insertion loss from dc to 35 GHz for the proposed SP4T switch. Compared with the state of the arts, the designed SP4T switch achieves the lowest insertion loss (< 1 dB at 10 GHz, < 1.4 dB at 20 GHz and < 2.6 dB at 35 GHz) over dc to 35 GHz. The active chip areas of the proposed SP4T switches are compact with size of only 0.36 x 0.19 mm^2.

In Chapter 7, ultra wideband double-pole double-throw (DPDT) switch matrix designs are presented. The switches are designed using series-shunt-series configuration in a ring-type structure with input and output matching networks. Two types of DPDT switch matrixes are designed with the same technology. The legacy generation1 switch matrix (Gen1) in this technology is fabricated using the same SOI top silicon thickness as the proposed SPDT and SP4T switches. It achieves the widest bandwidth from dc to 30 GHz with a low insertion loss of 2.5 dB and a high isolation of 32 dB up to 30 GHz, the measured input P1dB of designed switches is higher than 18 dBm, measured input third order intermodulation point (IIP3) is higher than 32 dBm. Also, a novel generation2 switch matrix (Gen2) fabricated on recessed SOI top silicon is presented. It provides about 0.5 to 3 dB lower insertion loss and better isolation from dc to 50 GHz frequency range as compared to Gen1 switch matrix.

In Chapter 8, the conclusion for this research work is drawn and possible future works are proposed.

Chapter 2

Review of RF switch design

2.1 RF switching block

In today's wireless communication system, an RF front-end module (FEM) acts as an interface between the antenna and digital baseband system. An RF front-end module typically consists of power amplifiers (PA), switches, low-noise amplifiers (LNA), control circuitry, and some other passive elements. Transmit/receive (T/R) switch is one of the most important building blocks in RF frond-end. The main function of RF switches is to switch one RF port (usually the antenna port) between the transmitter (TX) and the receiver (RX). As shown in Figure 2-1, the simplified T/R switch block, a SPDT (Single Pole Double Throw) switch is being used to route a RF signal from either a TX path or a RX path to the system antenna. In the TX branch, the switch routes the transmitted RF signals which is amplified by the PA to the antenna port, in the RX branch, the switch routes the received RF signals from the ANT to a LNA.

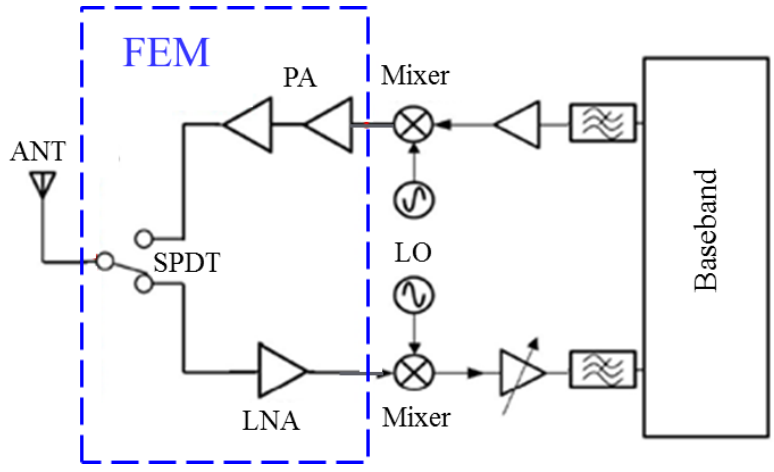


Figure 2-1 Simplified T/R switching block diagram

2.2 Characteristics and properties of RF switches

There are several important parameters the designer should look at when selecting an RF switch, including:

- Insertion loss (IL)

- Isolation (ISO)

- Return loss (RL)

- Power handling

- Linearity

- Switching speed

2.2.1 Insertion loss

The insertion loss of a switch module, which expressed in decibels (dB, as expressed in below formula, either in power loss or voltage loss), is a measure of the power difference between the available power at the input and the power delivered to the output when switch is in the "ON" state.

$$IL = 10log_{10}\left(\frac{P_{out}}{P_{in}}\right) = 20log_{10}\left(\frac{V_{out}}{V_{in}}\right), \quad (2\text{-}1)$$

Insertion loss in RF switches is generally attributed to the following factors:

1) Resistance, parasitic capacitance or inductance losses in the switch branch;
2) Signal leakage through "OFF" path device capacitance;

3) Impedance mismatch at the terminals of the switch, or within the switch. The mismatch loss can be reduced by implementing proper matching techniques, especially at high frequencies.
4) Number of throws, insertion loss increases as the number of throws of the switch increases.
5) Input signal frequency, usually the higher signal frequency is, the higher switch insertion loss is. At low frequencies, insertion loss mainly determines by on state resistance R_{on}, at higher frequencies, off state capacitance C_{off} starts to contribute to the insertion loss.

It is critical to ensure that the switch insertion loss be acceptable at the whole bandwidth requirement of the application for wideband switch.

2.2.2 Isolation

Isolation is a measure of the power difference between the available power at the input and the power at the output when switch is in the "OFF" state. Calculation formula for isolation (in dB) is as shown below

$$ISO = 10log_{10}\left(\frac{P_{out,off}}{P_{in}}\right), \tag{2-2}$$

Good isolation prevents signals from leaking into the undesired signal path, which is crucial in most applications. Isolation in RF switches is mainly affected by the following two factors:

1) “OFF” state device capacitance, including intrinsic capacitance and extrinsic wiring capacitance of the switch;
2) Also varies with frequency of the input signal, usually the higher signal frequency, and the worse switch isolation.

2.2.3 Return loss

Return loss is a measure of signal power loss caused by impedance mismatch between circuits. The return loss of a switch refers to the signal reflected back or returns back from the impedance mismatching point in the switch circuit, can be measured by S_{11} at the input of the switch when switch is in the “ON” state.

$$RL = 10log_{10}\left(\frac{P_{reflected}}{P_{in}}\right), \tag{2-3}$$

2.2.4 Power handling, 1 dB compression point (P1dB)

1 dB compression point (P_{1dB}) is another important parameter of RF switches, in addition to insertion loss, isolation and return loss, which is a measure of the RF power-handling capability of a switch when the switch is in “ON” state. P_{1dB} is defined as the input power at which the insertion loss has increased by 1dB from its low power value (linear region).

When an RF switch is driven into compression it will generate harmonics and insertion loss will increase.

Two major mechanisms of RF switch power compression including:

1) Turning on of the switch transistors in the off state (shunt) branch. A MOSFET will turn on when the gate to source bias exceeds its threshold voltage V_t, switch compression occurs when a transient voltage on the shunt transistor is higher than its V_t, during part of the cycle, input power will be routed to the ground instead of output. P1dB for this case is:

$$\text{P1dB} = 10log_{10}\left(\frac{2(V_t - V_{off})^2}{Z_0}\right) + 30 \text{ (in dBm)}, \quad (2\text{-}4)$$

Where V_{off} is the control voltage used to switch off the transistors, Z_0 is the system impedance.

2) Junction breakdown of the switch transistors in the off state branch. Compression will also occur when the RF voltage swing causes the source drain breakdown voltage (V_{bd}) to be exceeded on part of the cycle, P1dB for this case is:

$$\text{P1dB} = 10log_{10}\left(\frac{{V_{bd}}^2}{2Z_0}\right) + 30 \text{ (in dBm)}, \quad (2\text{-}5)$$

2.2.5 Linearity

Linearity indicates the ability of the RF switch to faithfully transfer a signal without distortion. Parameters such as 2nd and 3rd harmonic distortion, input third order intermodulation point (IIP3) are commonly used to indicate the RF switch linearity.

Harmonic distortion is a single-tone (single-frequency) distortion caused by device nonlinearity. When a non-linear device is stimulated by a signal at a single frequency f_1, spurious output signals are generated at the harmonic frequencies of $2f_1$, $3f_1$, and $4f_1$ ...nf_1.

Intermodulation distortion appears when the nonlinearity of a device with multi-tone (multiple input frequencies), causing the signals in one channel to interfere with adjacent channels. Increasing the switch transistor gate width can improve switch linearity.

2.2.6 Switching speed

Switching speed is defined as the time needed to change the state of a switch arm from “ON” to “OFF” or from “OFF” to “ON”.

Generally, RF switch should be designed to have low insertion loss, high isolation, low return loss (good impedance matching), large P1dB, good linearity and short switching time.

2.3 RF switches

There are basically two types of switches used today:

1) Electromechanical switches
2) Solid-state switches.

2.3.1 RF MEMS switch

Electromechanical switches operation is based on the electromagnetic induction theory. In electromechanical switches, the control signal causes the contact to physically change positions during the switching process. Usually these types of switches are used in industrial, and test and measurement applications.

Electromechanical switches have a number of advantages over solid-state switches. An electromechanical switch can operate over a wide bandwidth with excellent signal linearity, very low insertion loss and the high isolation. Furthermore, an electromechanical system can handle up to a few hundred watts CW (continuous wave) power. However, they are bulky, heavy and slow.

Micro-electro-mechanical systems (MEMS) switch is a new electromechanical technology provided by micromachining. RF MEMS switches use a mechanical movement to achieve a short circuit or an open circuit in the RF transmission-line.

There are basically two types, the capacitive contact and the ohmic contact. In capacitive switches, a metal membrane is pulled down onto a dielectric layer to form a capacitive contact. While in ohmic switches, two metal electrodes are brought together to create a low resistance contact, as shown in Figure 2-2

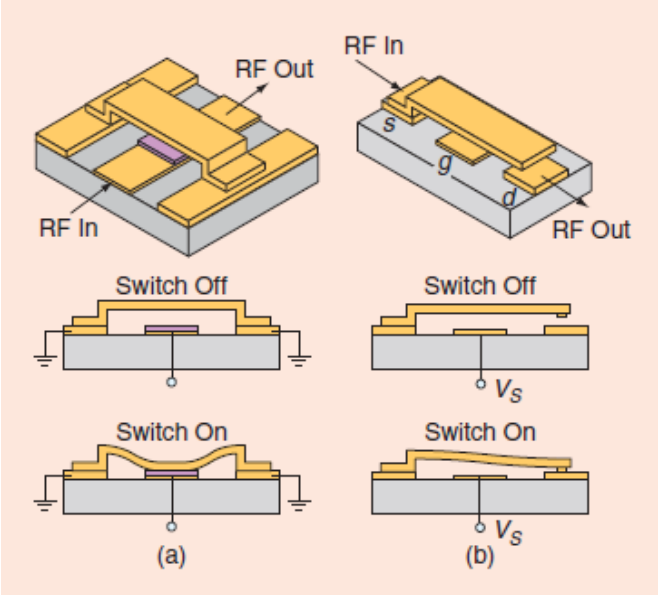


Figure 2-2 RF MEM switches, (a) Capacitive contact, (b) Ohmic contact

In comparison with other types of switches (e.g. PIN-diode switches or FETs switches, which will be touched later), MEMS switches offer the benefits of very high isolation, very low insertion loss, high linearity, potential for low cost. However, MEMS switches also have their disadvantages, including relatively low speed, need high voltage or high current drive, relatively poor reliability and poor integration capability.

2.3.2 Solid state switches

A solid-state switch is an electronic switching device based on semiconductor technology. This makes them faster, smaller, and lighter. Switching times for these parts can be in the nanosecond range.

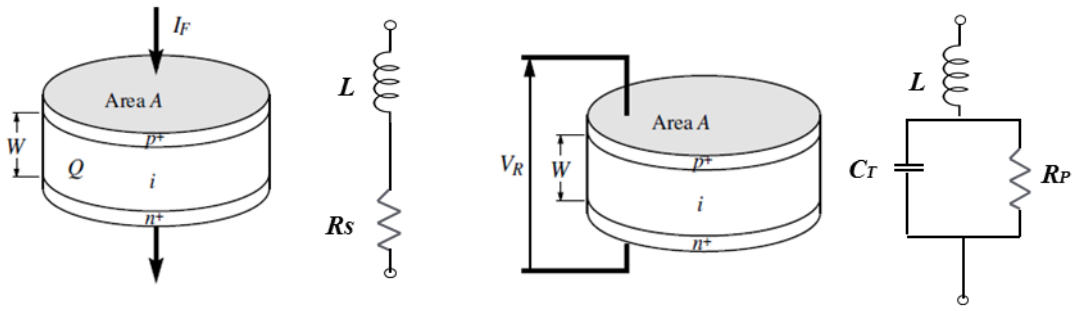
There are two existing technologies suitable for making practical RF switches:

1) P-i-n diode (PIN)
2) Field-effect-transistor (FET), including pHEMT, bulk CMOS, SOS and SOI, etc.

2.3.2.1. PIN diode switches

A PIN diode is a device that operates as a variable resistor at RF frequencies. Its resistance varies from less than 1 Ω in its "ON" state to more than 10 kΩ in its "OFF" state.

A PIN diode in constructed by a high resistivity intrinsic I region, and a p-type and an n-type region as shown in Figure 2-3.



(a) Forward bias equivalent circuits; (b) Reverse bias equivalent circuits

Figure 2-3 Simplified PIN diode structure and the equivalent circuits

PIN diode switches are usually used for high power applications, but they need large biasing current and switch speed is relatively slow, and also has poor integration capability.

2.3.2.2. FETs switches

Traditionally, the mainstream technology choices for RF switches have historically been III-V Compound based GaAs pHEMT, owing largely to its high RF performance

including higher mobility, higher cut-off frequency, higher breakdown fields than silicon and low insertion loss, high isolation for most high frequency and broadband applications.

The HEMT is a heterostructure field-effect transistor (FET). Its principle is based on a heterojunction which consists of at least two different semiconducting materials brought into intimate contact, acting as a donor and an acceptor, respectively. Because of the different band gaps and their relative alignment to each other, band discontinuities occur at the interface between the two semiconducting materials.

A typical AlGaAs/GaAs HEMT structure and the role of each layer in the structure are as shown in Figure 2-4.

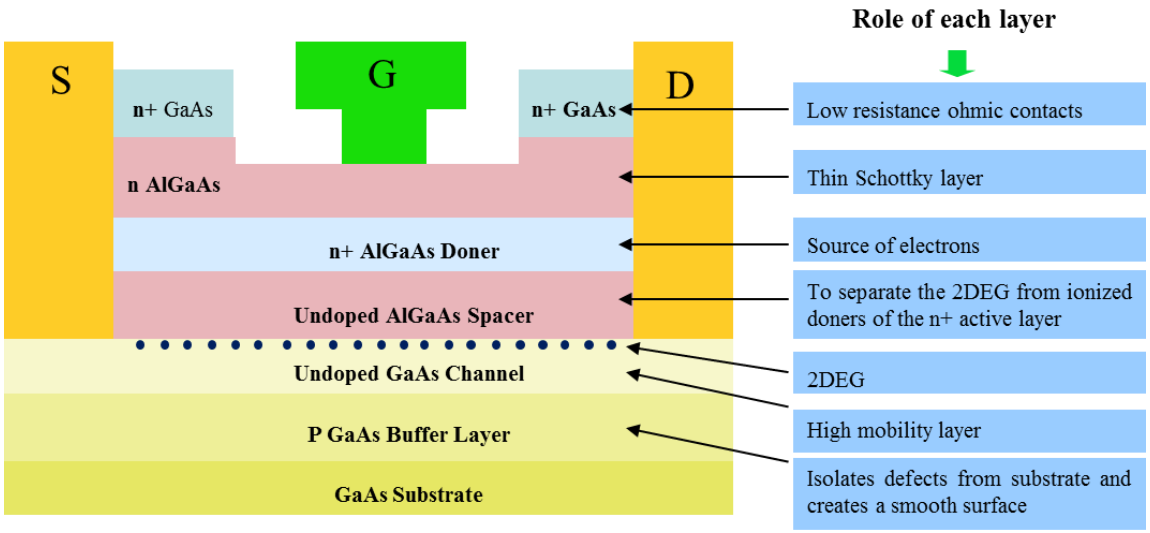


Figure 2-4 AlGaAs/GaAs HEMT structure

The major disadvantages for III-V compound based pHEMT technology are higher wafer cost, and most important, less integration capability when compared to mature silicon technologies.

Thanks to the continuous downscaling of CMOS, making the use of bulk CMOS for RF application is very attractive. The key benefits of using bulk CMOS are standard CMOS

process, high manufacturing yields and high levels of integration. So CMOS appears to be the best solution for the integration of RF, IF, and baseband blocks on the same die.

However, the major issues with bulk silicon substrates for RF applications are poor linearity and high insertion loss. Using triple wells and high-resistivity substrate are options to improve these parameters, but it's still quite challenging to make RF switch with bulk CMOS.

Silicon-on-sapphire (SOS) is formed by depositing a thin silicon layer onto a sapphire substrate. Its main advantage comes from the high insulating sapphire substrate, which virtually eliminates the parasitic drain capacitance that is present in bulk silicon (similar to SOI technology which will be explained later), thus provide outstanding RF performance, including low insertion loss high isolation and high linearity, while still benefits from its similarity to bulk silicon by using same basic CMOS technology, this allows SOS CMOS for high frequency applications, and can provide similar performance to III-V GaAs pHEMT. However, when compared to bulk silicon, SOS wafers are much more expensive.

The key feature of the SOI structure is the buried oxide (BOX) layer between the top Si layer and the underneath silicon substrate. SOI technology detail will be presented in Chapter 3.

2.4 Common switch design techniques

There are varies techniques that have been reported to achieve required switch performance for different end applications, most common techniques used for relatively low frequency application (<10 GHz) include gate biasing, transistor stacking, body floating, etc.

2.4.1 Gate biasing

In order to increase the linearity of a MOSFET switch, the gate is often biased using a large resistor.

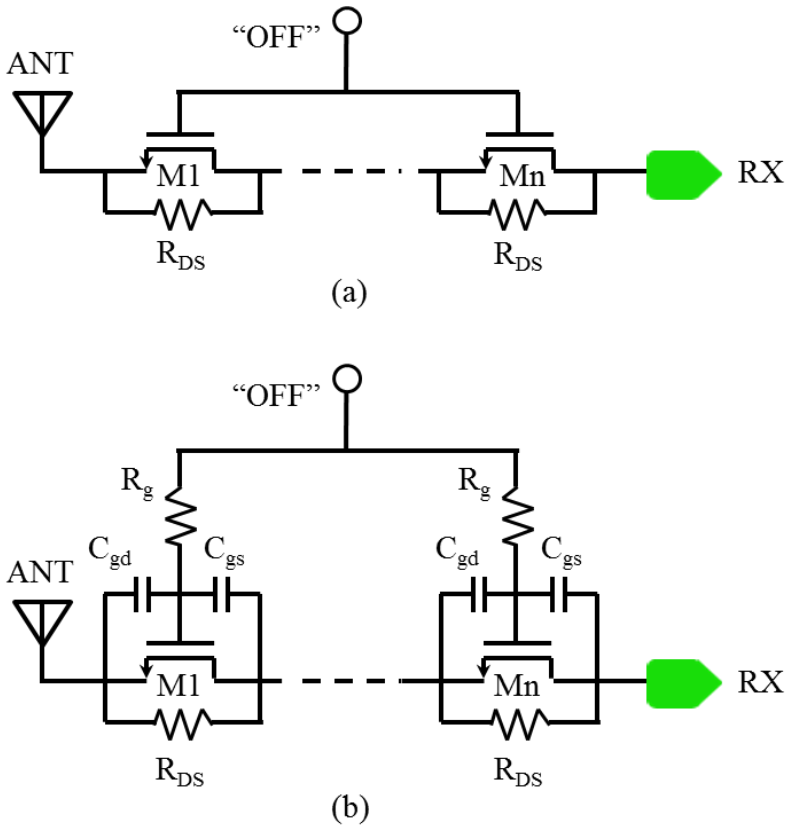


Figure 2-5 Capacitive coupling model of the OFF state FET, (a) Without gate resistors, (b) With gate resistors [1].

The gate resistors are implemented using poly resistors. A typical value for the gate bias resistance is about tens of kΩ. The purpose of the gate bias resistances is to improve dc bias isolation. If the gate bias resistors are not present, the fluctuations of the transistors due to the voltage swing at drain and source of the transistors will be higher and may result in excessive voltage across the gate dielectric and cause breakdown [1].

2.4.2 Transistor stack

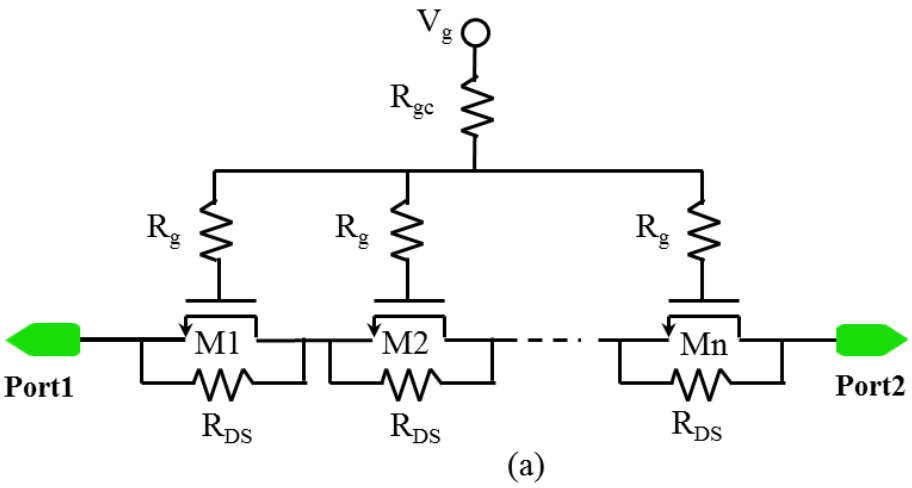


Figure 2-6 Transistors stacking in order to handle high power RF signal. [1]

Maximum RF power handling of stacked transistors is expressed as:

$$P_{MAX} = 2\left(\frac{n(V_t - V_{off})^2}{Z_0}\right), \tag{2-6}$$

The number n is fixed depending on the maximum RF power requirement and reliability transistor constraints, where V_t is the threshold voltage of MOSFETs, V_{off} is the control voltage used to switch OFF the transistors, Z_0 is the system impedance. [2]

2.4.3 Body floating

The body-floating technique is used in order to improve the power performance of the CMOS switch. For a conventional switch, the body of the transistor is connected to the source, when the input power increases, the drain-to-source voltage is so negative as to turn on the diode between drain and body, and the input impedance of the transistor is lower. Taking advantage of the modern triple-well CMOS process, Yeh et al. [3] realized the

resistive body floating simply by using a large resistor to bias the body as shown in Figure 2-7, which can provide the high impedance to decrease the leakage current and obtain a better insertion loss performance. As resistors are intrinsically wideband, the P1dB improvement is also wideband.

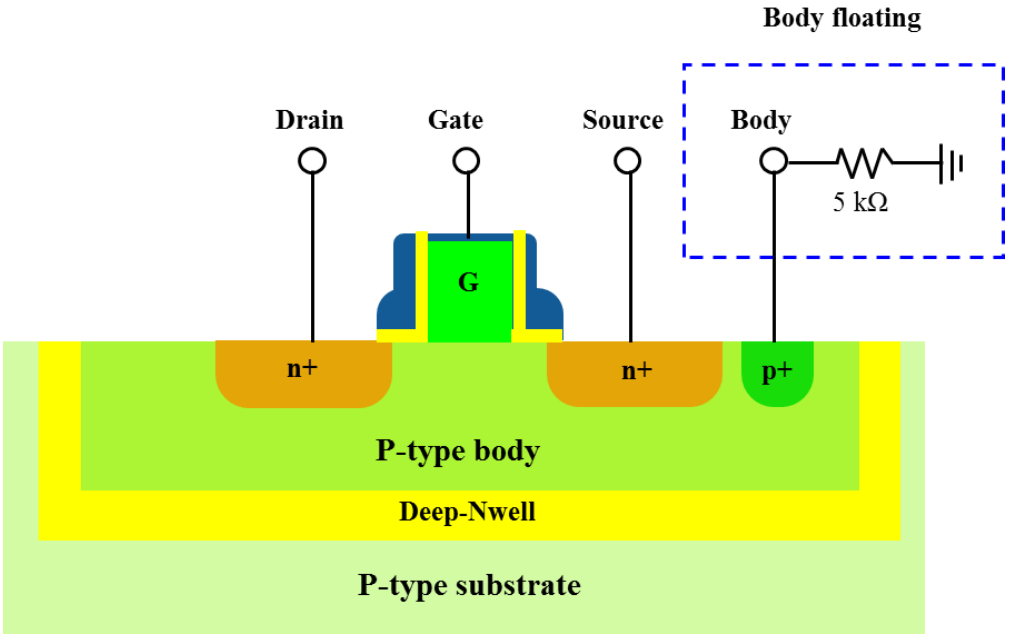


Figure 2-7 CMOS with body floating [3]

Table 2-1 summarizes T/R switches with varies technologies and techniques for application below the millimeter wave region, as can be found from this table, SOI switch basically have lower insertion loss, higher isolation and higher harmonic distortion.

Table 2-1 Switch Performance Comparison

Reference	Technology	Type	Freq.	IL	ISO	P1dB	H2	H3	chip Size	Topology
			GHz	(dB) Tx/Rx	dB	dBm	dBc	dBc	mm2	
[1]	0.18 μm SOI	SP10T	0.9	0.65	37-41	NA	-79	-75	1.52	series-shunt(HR)
			1.9	0.81	31-33		-77	-76		
[2]	0.13 μm SOI	SP6T	0.9	0.7/0.8	40	36	-73	-76	1.23	Symmetric
			1.9	0.7/0.8	30		-74	-71		
[3]	0.18 μm CMOS	SPDT	2.4	0.7	35	21.3	NA	NA	0.19	Symmetric series-shunt, resistive body-floating
			5.8	1.1	27	20				

[4]	GaAs pHEMT	SP6T	0.9	0.21/0.33	37.2	37	-77	-76	2.25	Symmetric
			1.9	0.54/0.65	31.7	36	-71	-72		
[5]	0.18 µm CMOS	SPDT	2.4	1.5/1.6	32	>28	NA	NA	0.56	Asymmetric, LC-Tuned body floating
			5.2	1.5/1.4	30					
[6]	90 nm CMOS	SPDT	24	3.4/3.5	22/16	28.7	NA	NA	0.018	Asymmetric, LC-tuned Rx
[7]	0.18 µm CMOS	SPDT	5.2	2.20/ 1.56	31.05/ 17.15	29.6/ 11.2	NA	NA	0.585	Asymmetric, stepped impedance using LC Resonator
				1.62/1.45	37.5/18. 24	30/11				
[8]	0.18 µm CMOS	SPDT	1.8	0.75/1.1	20/35	33	NA	NA	0.4	Symmetric, feed-forward capacitor
[9]	0.13 µm CMOS	SPDT	0.9	0.5	29	31.3	NA	NA	0.114	Symmetric series-shunt, transistor stacking
			2.4	0.8	24	28				
[10]	0.5 µm CMOS	SPDT	0.9	0.7	42	17	NA	NA	0.31	Symmetric series-shunt, Minimizing RB(substrate resistance)
[11]	0.13 µm CMOS	SPDT	2.4-20	0.9-2	43-21	30	NA	NA	0.17	Symmetric series-shunt, double-well body-floating
[12]	0.18 µm CMOS	SPDT	0.9-6	<2	>15	15	NA	NA	NA	Differential architecture, Optimizing dimensions
[13]	90 nm CMOS	SPDT	2.4	0.40	30	30	NA	NA	0.02	Asymmetric, stepped impedance
[14]	65 nm CMOS	SPDT	2.4	0.80	28	29	NA	NA	0.2	Asymmetric, stepped impedance
[15]	0.18 µm CMOS	SPDT	2.4	1.50	>24	11	NA	NA	0.45	Symmetric series-shunt,
[16]	0.13 µm CMOS	SPDT	16.6	0.8	20	26.5	NA	NA	0.015	Series, asymmetric S/D, switched body floating
			28	1.3	23	25.5				
[17]	0.18um CMOS	SPDT	5	1.44	>22	21.5	NA	NA	<0.1	series-shunt, transistor stacking
[18]	0.18 µm CMOS	SPDT	1.9	1.6	20	33.5	NA	NA	0.4	series-shunt, transistor stacking
[19]	0.13 µm CMOS	SPST	35	2.2	32	23	NA	NA	0.016	series-shunt, transistor stacking
[20]	0.18 µm CMOS	SPST	dc-20	0.7-2.5	25-60	26.2	NA	NA	0.06	series-shunt, artificial transmission line

[21]	0.13 μm CMOS	SPDT	15	1.8	17.8	21.5	NA	NA	0.2	series-shunt, impedance matching
[22]	0.18 μm CMOS	SPDT	0.9	0.97	>39	24.3	NA	NA	0.28	series-shunt, impedance matching
			2.4	1.1	>24	20.6				
[23]	0.5 μm SOS	SP6T	0.9	0.45/0.7	55	43	-91	-85	NA	Symmetric
			1.9	0.5/0.9	40		NA	NA		
[24]	0.25 μm SOI	SPDT	2.4	0.7	>46	12	NA	NA	NA	Symmetric
			5	1	>46		NA	NA		
[25]	0.18 μm SOI	SP14T	0.9	0.55/1	37	28	-85	-85	2.7	Symmetric
			1.9	0.65/1	31		-80	-75		
[26]	0.18 μm SOI	SP4T	0.9	0.42/0.9	40	NA	-82	-79	1.7	Symmetric
			1.9	0.6/0.7	35		-86	-84		
[27]	0.18 μm SOI	SP10T	0.9	0.48/0.71	43.1	>34.2	-84	-88	1.23	Symmetric
			1.9	0.81/1.03	40		-86	-79		
[28]	0.18 μm SOI	SP6T	0.9	0.47/0.56	49	NA	-78	-87	0.76	series-shunt
			1.9	0.58/0.78	38		-76	-80		
[29]	0.18 μm SOI	SP4T	0.9	0.53/0.74	>43	NA	-76	<-74	0.53	series-shunt
			1.9	0.65/0.86	>34		-83	-90		
[30]	0.18 μm SOI	SP9T	0.9	0.42/0.49	>37	NA	-90	-90	1.52	series-shunt
			1.9	0.55/0.69	>31		-83	-80		
[31]	0.18 μm SOI	SP9T	0.9	0.45/0.55	41-58	NA	-95	-84	NA	series-shunt(HR)
			1.9	0.2/0.25	36-45		-85	-82		
[32]	0.18 μm SOI	SPDT	0.9	0.43/0.82	45/32	37.2	-86	-82	0.85	Asymmetric
			1.9	0.75/0.88	37/28	35.6	-85	-80		

The system requirement for the above relatively low frequency antenna switch are given in table 2-2.

Table 2-2 RF antenna switch key requirements

Wireless Standard	Freq.(GHz)	Insertion Loss(dB)	Isolation (dB)	P1dB (dBm)
GSM	0.9/1.9	<1	35	33
WCDMA	0.85/1.9/2.1	<1	35	25
WLAN	2.4/5.8	<1	25	18

At higher frequency (>10 GHz) or mm-wave frequencies, the impedance of the switch in the off state could be comparable to when it is on, as shown in Figure 2-8. [33] As can be seen in this figure, S_{21} for on and off states at 60 GHz are comparable. So the design of high frequency or wideband switches becomes much more challenging due to the increased

coupling of the RF signals to the silicon substrate. Insertion loss is increased and isolation is decreased with the increasing frequency.

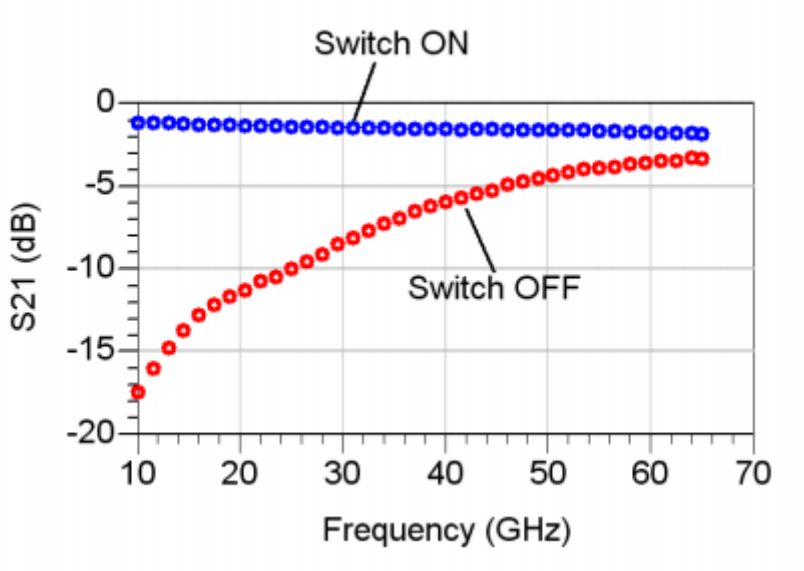


Figure 2-8 Measured S_{21} of an NMOS transistor acting as a series switch [33]

Some wideband or mm-wave switches have been demonstrated using different technologies, including bulk CMOS, SiGe BiCMOS, pHEMT, MEMS, and SOI as well, the major design topologies used include series-shunt plus matching network, traveling wave concept, transmission line based, transformer based, etc. Also some novel structures like standing-wave filtering switch as well.

2.4.4 Series-shunt with input/output matching networks

At higher frequencies, the switch shunt branch will severely degrade the insertion loss, while the lack of a shunt arm results in a low isolation.

Berke et al. [34] presented a dc-70 GHz wideband SP4T switch with performance compared to GaAs or InP technology, and with high isolation between the channels. The configuration of this wideband switch is series-shunt with matching network, as shown in

Figure 2-9. A dc to 60 GHz wideband SPDT switch, with similar series-shunt with matching network configuration was demonstrated based on 45nm SOI technology [35].

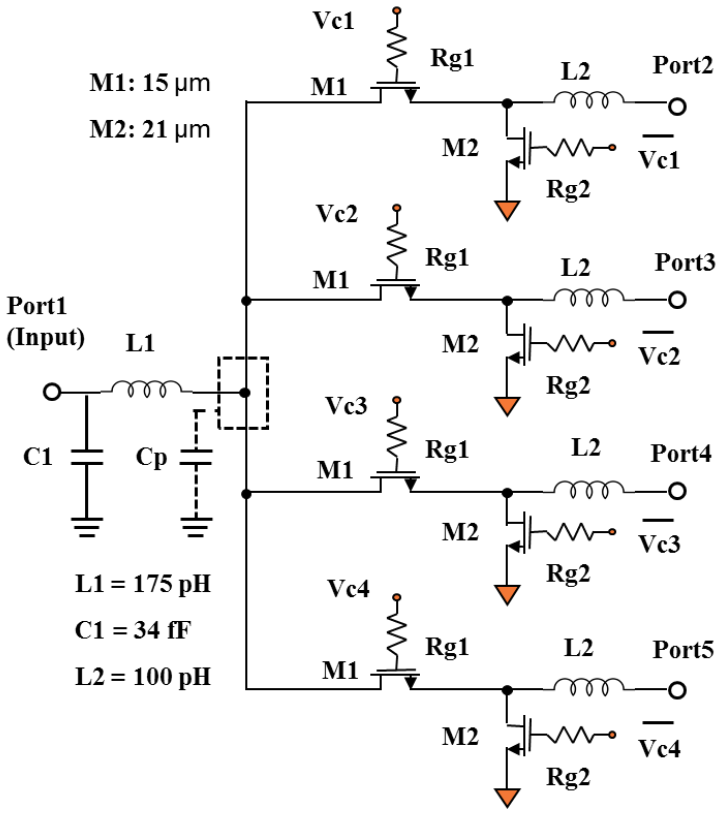


Figure 2-9 Schematic of series-shunt SP4T switch with matching network [34]

2.4.5 Matching network (MN), λ/4 transmission lines

Another widely adopted topology to realize mm-Wave SPDT switches is to use impedance-inverting λ/4 transmission line (T-line) and shunt SPST cells as shown in Figure 2-10, where λ is the guided wavelength [36]. The SPDT schematic is based on a tuned λ/4 transmission-line with a single shunt transistor. In the off-state, the transistor gate and junction capacitances together with the substrate resistance transform into an equivalent resistance and capacitance network. The output matching network consists of a shorted stub that acts as an inductor and cancels the equivalent capacitance of the transistor in the off-state. The major issue of this topology is the bulky size of the λg T-line that makes this SPDT switch not a cost saving solution.

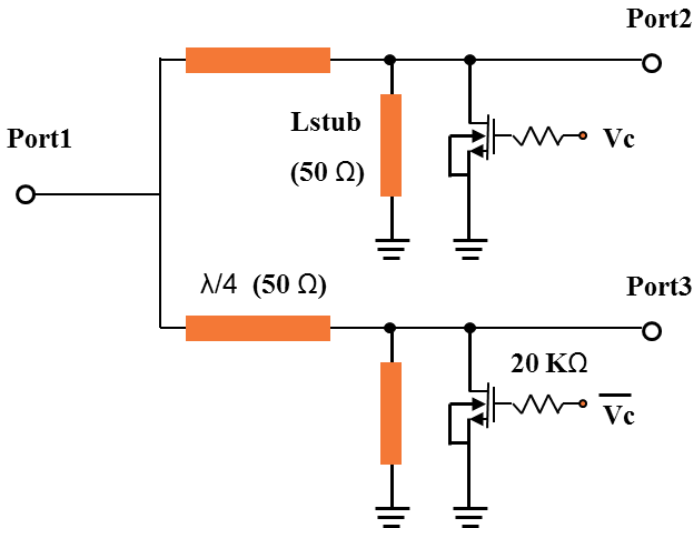


Figure 2-10 Schematic of λ/4-based SPDT switch [36]

2.4.6 Traveling-wave concept

A traveling-wave concept switch has also been reported [37]. As shown in Figure 2-11, the inductive line is periodically loaded by shunt transistors. In the ON state, the inductive line with loaded off-state capacitances functions as a transmission line to pass the millimeter-wave signals, while in the OFF state, the on-resistance shunt transistors short the signal to ground. The traveling-wave concept switches normally have high isolation at the cost of an insertion loss higher than that of the matching-network switch.

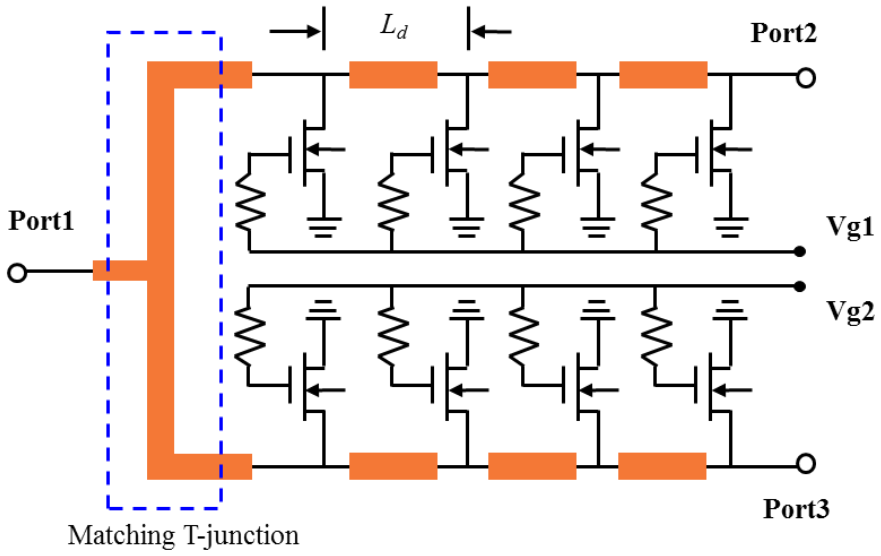


Figure 2-11 Schematic of traveling-wave SPDT switch [37]

Quarter-wave transformer based wideband switches [33] and standing-wave filtering switch were also reported [38]. Table 2-3 summaries various state-of-the-art wideband and millimeter-wave switch performance.

Table 2-3 Wideband Switch Performance Comparison

Reference	Technology	Type	Frequency	IL	ISO	Input P1dB	Chip Size	Topology
			(GHz)	(dB)	(dB)	(dBm)	(mm2)	
[33]	90 nm CMOS	SPDT	50	3.4	19	14	0.0036(core)	transformer based
[34]	130 nm CMOS	SP4T	dc-70	<3.5	>25	9-10	0.24x0.23	series-shunt design with matching networks
[35]	45 nm SOI CMOS	SPDT	dc-60	2.5	>25	7.1	0.18×0.22	Series-shunt, low-resistivity (13.5 Ω − cm) substrate.
[36]	90 nm CMOS	SPDT	50-70	1.5	>25	13.5	0.55x0.5	Matching network, λ/4 transmission lines
[37]	90 nm CMOS	SPDT	50-94	3.3	>27	15	0.57x0.42	traveling-wave concept
[38]	0.18 μm SiGe BiCMOS	SPDT	45-64	3.2	>20	>21	0.0675	artificial-resonator-based standing-wave filtering switch
[39]	90 nm CMOS	SPDT	60-110	<4	>25	10.5	0.45x0.75	Transmission line integrated DS
[40]	130 nm CMOS	SPDT	57-66	<2	>21.1	13(sim.)	0.09x0.22	Matching network(MN)
[41]	90 nm CMOS	SPDT	50-67	1.9	>38	10	0.55x0.55	Unbalanced Double shunt with matching network
[42]	130 nm CMOS	SPDT/ SP4T	45-70	2	>30	13	0.39x0.32	λ/4 transmission lines, C-L-C matching network
[43]	65 nm CMOS	SPST	dc-94	<1.6	>30	>9	0.52x0.29	series inductor placed between the shunt transistors
[44]	130 nm CMOS	SPDT	57-66	4.5-5.8	>24	4.1	0.68X0.325	series-shunt design with input/output impedance

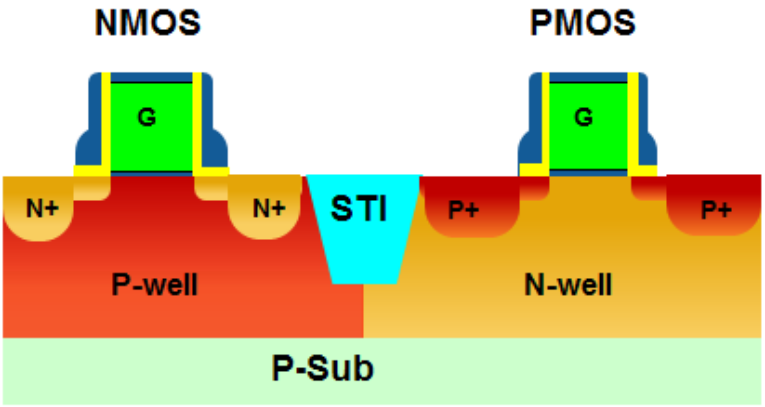
								matching networks
[45]	0.35 μm SiGe	SPDT	42-70	<1.25	>18	1	0.85x0.92	differential
[46]	RF-MEMS	SP4T	dc-70	<1	>15	NA	NA	distributed transmission line
[47]	180 nm SiGe BiCMOS	SPDT	60	2.7	14	13.8	0.19x0.225	transformer based
[48]	90 nm CMOS	SPDT	57-64	<3.5	34	6.5-6.9	0.57 × 0.57	series-shunt+ 90 phase shifter
[49]	0.1 μm HEMT	SPDT	15-80	<3.6	>25	NA	1.5 x 1.5	traveling-wave concept
[50	0.18 μm SiGe BiCMOS	SPDT	dc-30	1.5 – 3.3	80 – 20	23	0.025	series-shunt, with matching network
[51]	0.18 μm SOI	SPDT	dc-40	<5	>17	15	0.28 X 0.09	series-shunt, with matching network
[52]	90 nm CMOS	SPDT	dc-60	<3	>48	17	0.68X0.87	traveling-wave concept
[53]	130 nm CMOS	SP4T	dc-30	<2.7	>26	9	0.25 x 0.18	series-shunt, with matching network
[54]	65 nm CMOS	SPDT	42-134	4	>25	N/A	N/A	traveling-wave concept

Chapter 3

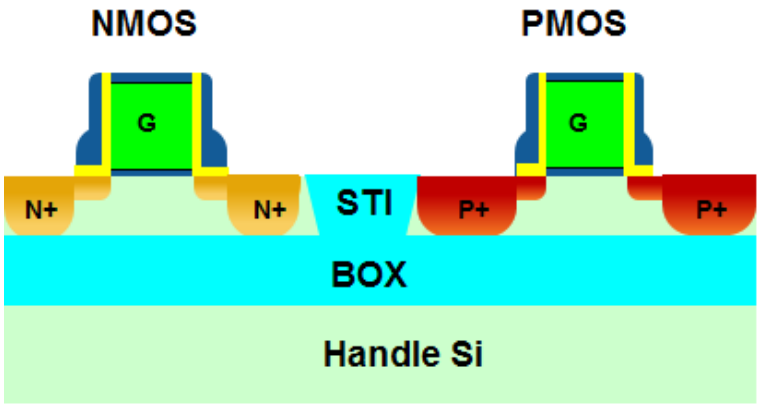
Introduction to SOI

3.1 SOI Benefits

The key difference between bulk Si and SOI transistors are as shown in Figure 3-1. Bulk Si transistors are built on top of the surface of a silicon substrate, in SOI, the top active silicon region is separated from the handle silicon substrate by the buried Oxide (BOX) layer, and the transistors are encapsulated in SiO_2 on all sides,



(a)



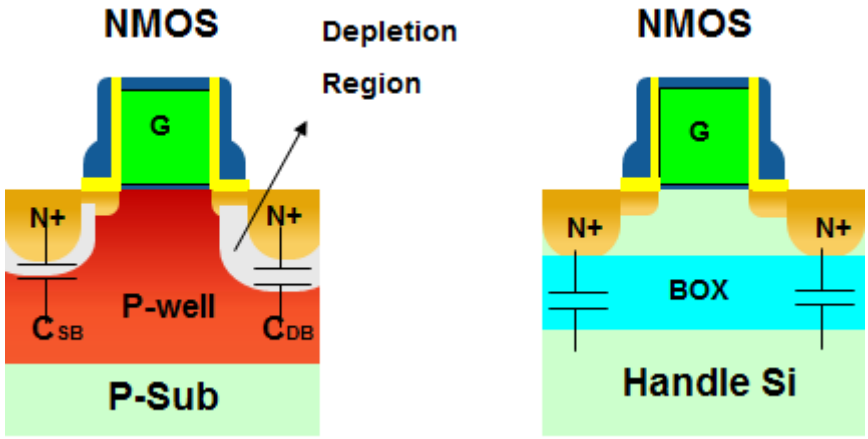
(b)

Figure 3-1 Cross section of (a) bulk CMOS, and (b) SOI CMOS

This difference provides a number of advantageous device and circuit performances when compared to bulk Si.

3.1.1 Reduction of substrate parasitic capacitances

Capacitances are a key factor for RF device (including RF switch) performances. Any reduction of the total capacitance of a MOSFET will increase the cut-off frequency of the transistor, allowing using the device at higher frequency. In bulk transistor, the parasitic source/drain to substrate junction capacitance is high because of the high doping level. In SOI, the maximum capacitance between junctions and the substrate is the capacitance of the BOX layer.



(a) Bulk CMOS (b) SOI CMOS

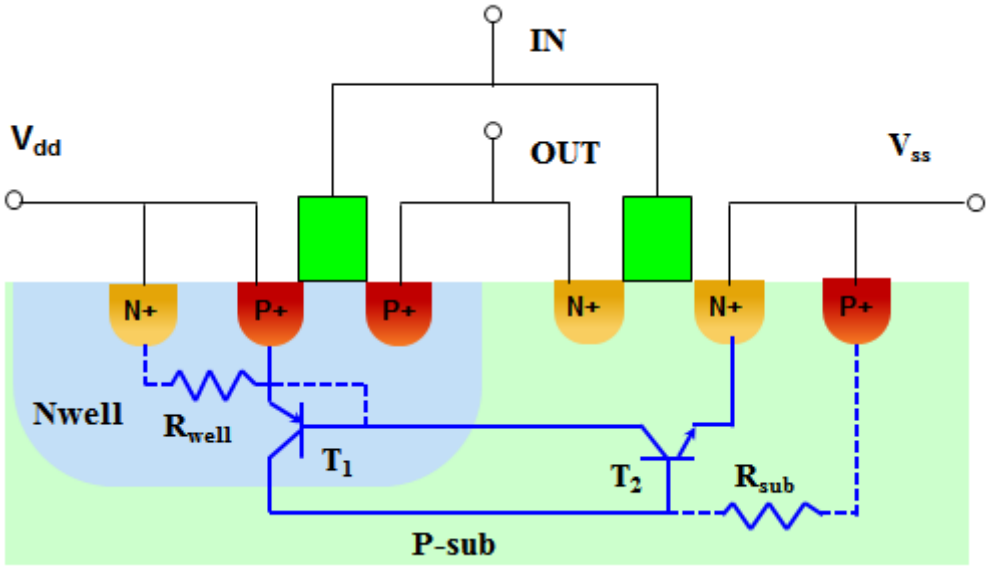
Figure 3-2 Capacitances of (a) bulk CMOS, and (b) SOI MOSFET

Figure 3-2 shows a schematic diagram of the capacitances in a bulk CMOS and a SOI MOSFET. In SOI devices, the junction capacitance is much smaller when compared to bulk CMOS, because of the lower dielectric constant of the BOX layer when compared to the Si depletion layer in bulk CMOS (3.9 vs. 11), and the thick BOX layer (>1kA) when compared to the thin depletion layer. This helps improve the switching speed of CMOS devices and more important, decrease the off-state capacitance (C_{off}), and improves switch isolation.

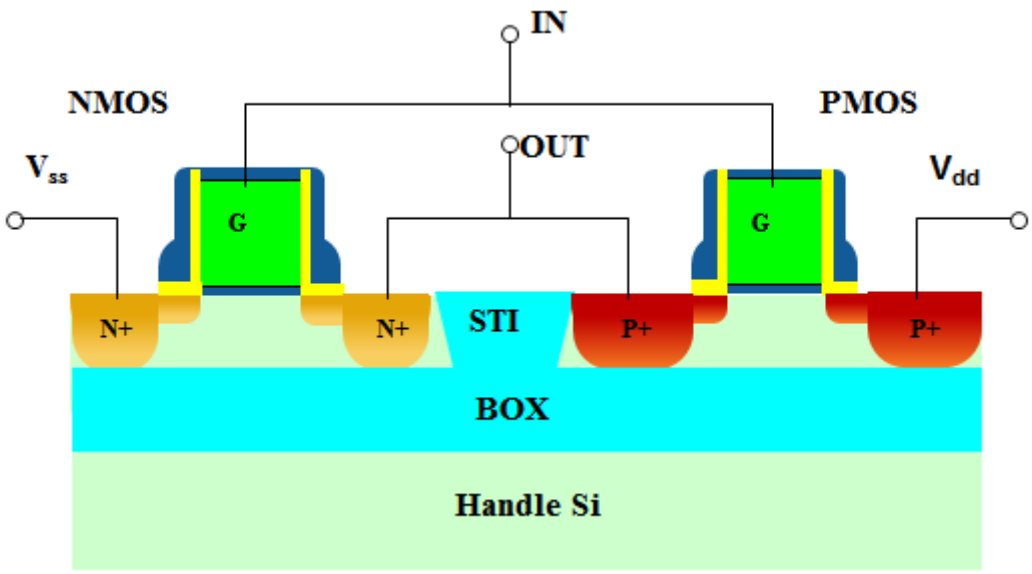
3.1.2 *Ideal device isolation and smaller layout area*

Because SOI devices are laterally isolated from each other by shallow trench isolation (STI), and vertically isolated from the silicon substrate by the BOX layer, so isolation for SOI devices is ideal. And because of this, devices can be layout more closely than bulk ones.

3.1.3 *Latch up elimination*



(a)



(b)

Figure 3-3 Inverter of (a) Bulk CMOS, (b) SOI CMOS

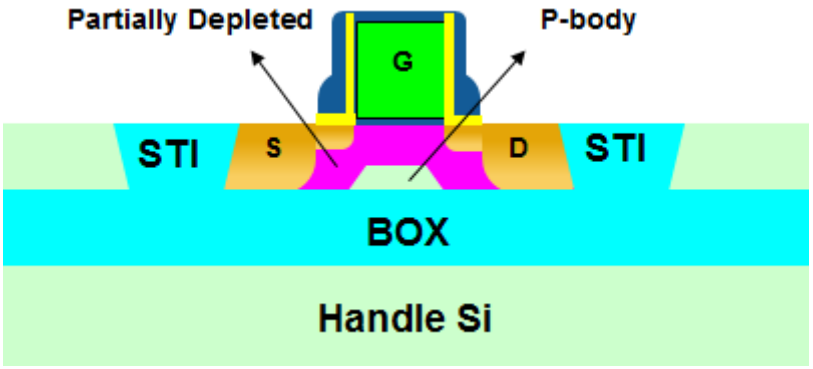
Parasitic npn and pnp transistors can cause “latch up” conditions in bulk CMOS. But latch up does not exist in SOI. Since SOI NMOS and PMOS transistors are separated by the BOX layer, as presented in Figure 3-3, with no access to the substrate, hence there is no path for any current flow between devices, thus latch up will not happen.

3.2 FD SOI and PD SOI

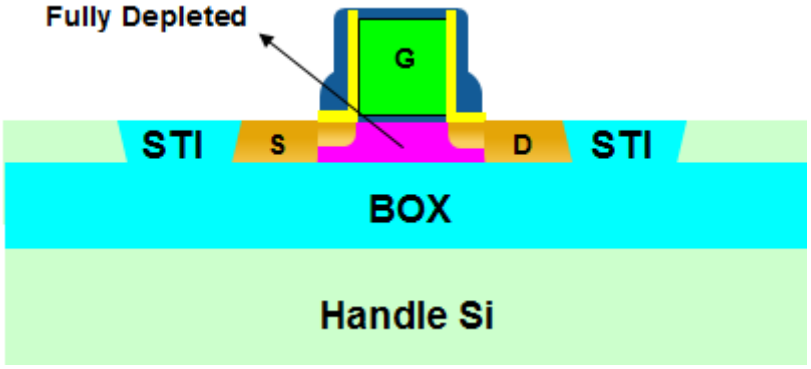
SOI devices can be divided into two types, depending on the operating mode: fully-depleted (FD) and partially-depleted (PD). The difference mainly derives from the thickness of the top silicon, the top silicon thickness in FD SOI is generally much thinner than that in PD SOI.

Take SOI NMOS transistor for example, by applying a large enough positive voltage to the gate, the p-type carriers will be depleted and will induce an n-type inversion layer on the surface of the body. If the top silicon layer is made very thin, the inversion layer fills the full depth of the body. This is called a “fully depleted” SOI (FD SOI). On the other hand, if the top silicon layer is made thicker, the inversion region will not extend the full depth of the body, and leave some of the body un-depleted. Such SOI is called a “partially depleted” SOI (PD SOI).

A simplified schematic comparison between FD SOI and PD SOI is shown in Figure 3-4.



(a)



(b)

Figure 3-4 Cross sections of (a) PD SOI, (b) FD SOI

3.3 Floating body versus body tied SOI

In PD SOI, the un-depleted portion of the body is not connected to anything, in other words, it is floating. The floating body can get freely charged/discharged and hence will affect transistor threshold voltage (V_t) and some other device characteristics.

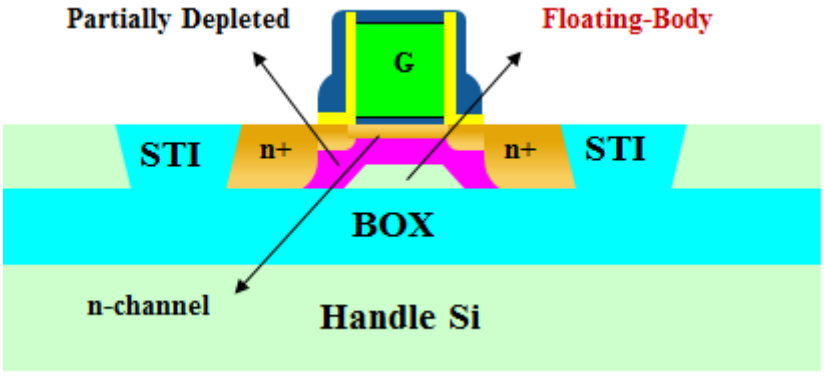


Figure 3-5 Schematic of the floating body SOI

The major of floating body effect is so called “kink” effect or the increase in the output conductance of the device near drain-to-source bias, V_{ds}, as shown in Figure 3-6. When V_{ds} becomes large enough, the impact ionization current (holes) flows to the un-depleted body, which increase V_{bs}, resulting in a decrease of V_t.

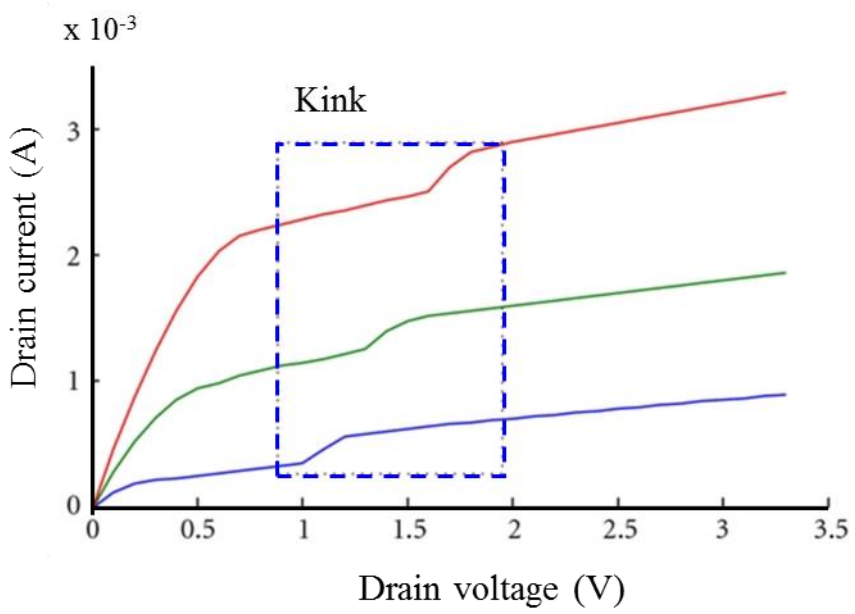


Figure 3-6 The kink effect

The solutions to minimize the kink effect can be either to provide a body contact for the device or to use FD SOI devices. In FD devices, the top active silicon thickness is much thinner than the channel depletion depth, any impact ionization charges flowing into the depleted body will be swept to the source because of the much lower potential barrier.

3.4 HR SOI and HR trap-rich SOI

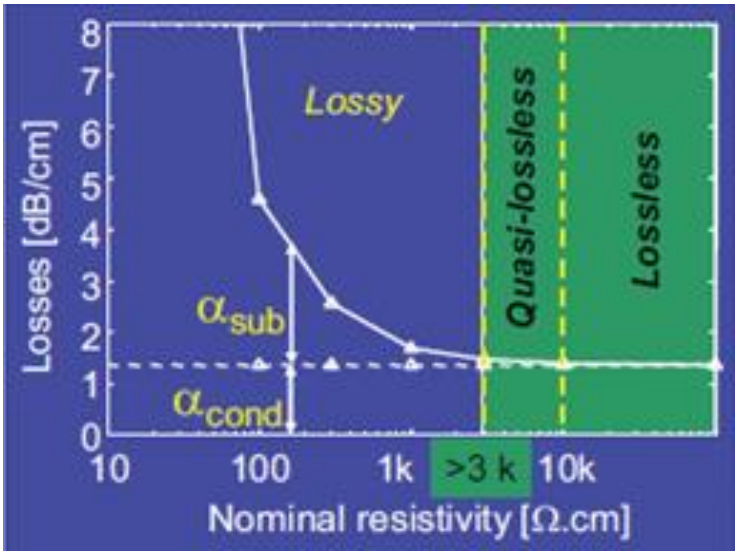
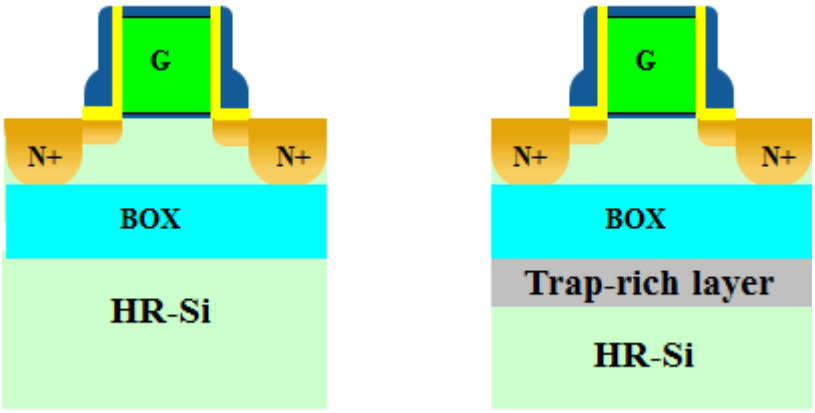


Figure 3-7 Substrate resistivity versus loss

Traditionally, SOI wafers use low-resistivity bulk silicon as handle wafers for logical application. However, for RF applications, the BOX layer is not thick enough to prevent the electrical field from diffusing into the substrate, inducing high-frequency signal losses, non-linearity and crosstalk.

To improve the insertion loss, isolation and linearity performance required for RF switches, bulk silicon is replaced by a high-resistivity silicon substrate, which is higher above 1 KΩ-cm [24]. This high resistivity SOI (HR SOI) substrate is critical to high performance RF integrated circuits, can lead to substantially reduced substrate RF losses and crosstalk, as shown in Figure 3-7.

However, HR SOI wafers still suffer from parasitic surface conduction due to fixed charges (Qox) within the oxide, which attract free carriers near the Si/SiO_2 interface, this will reduce the substrate effective resistivity and increase substrate losses.



(a) HR SOI (b) HR TR SOI

Figure 3-8 Cross-sections of SOI MOSFET on (a) HR SOI, and (b) HR TR SOI

The introduction of a trap-rich layer, as shown in Figure 3-8 (b) has been proved as the most effective technique. The traps created by silicon dangling bonds in the trap-rich layer can capture the free carriers at the Si/SiO_2 interface, thereby enabling the substrate to recover its high resistivity, linearity, eliminating the dc dependency, and leading to a substantial reduction of RF losses and crosstalk [55]–[58].

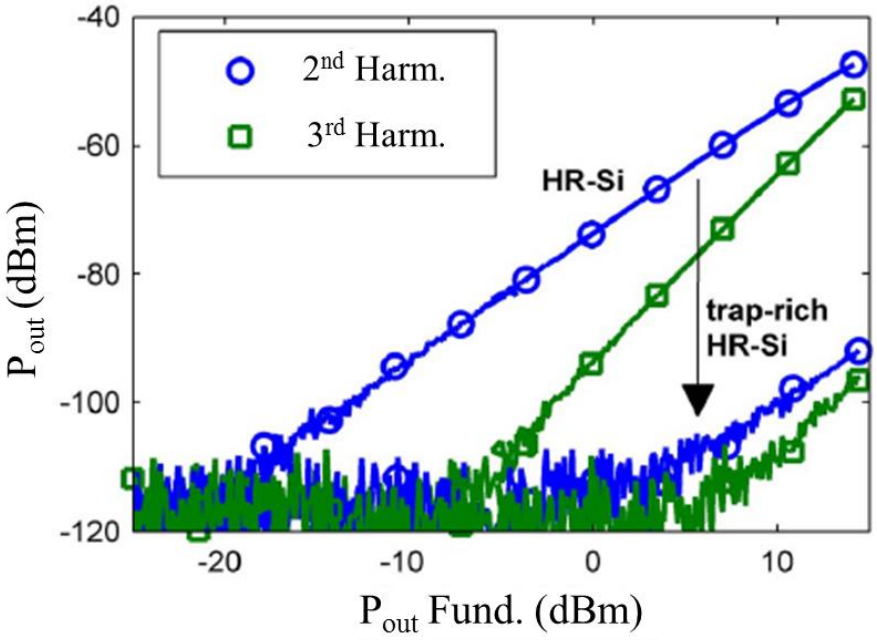


Figure 3-9 Measured H_2 and H_3 of a CPW line on HR Si without and with a trap-rich layer [57]

Figure 3-9 shows the measured harmonic distortion of CPW line on high resistivity silicon substrates, with and without a trap-rich layer. The introduction of a trap-rich layer significantly reduces the CPW line harmonics.

In recent years, thanks to it's excellent performance, SOI technology has rapidly evolved as a mainstream technology for switches used in wireless applications and other RF applications [59]-[66].

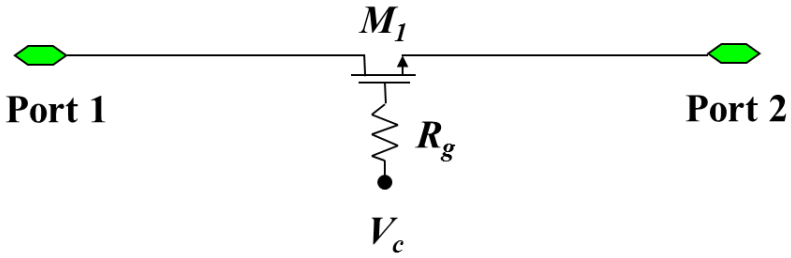
Chapter 4

Ultra wideband SPST switch design considerations

4.1 SPST switch topology

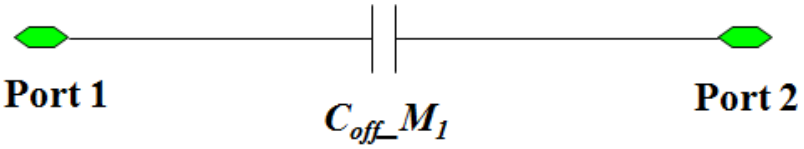
4.1.1 Series only configuration

A single-pole single-throw (SPST) switch can be implemented by simply using a series only NMOS transistor. Schematic of the series transistor only SPST switch is as shown in Figure 4-1 (a). The RF signal presented at Port 1 can be either blocked from or passed through to Port 2, depending on the bias control of V_c. For this 2.5 V switch NMOS M1, when V_c = 2.5 V, this switch is "on", when V_c = 0 V or negative, the switch is "off". Equivalent small signal model of the on and off state are shown in Figure 4-1 (b) and (c). External poly resistor R_g is required in order to prevent signal leaking and gate oxide breakdown.



(a)

(b)



(c)

Figure 4-1 (a) Series only SPST switch, (b) Equivalent model of "on" state and (c) Equivalent model of "off" state

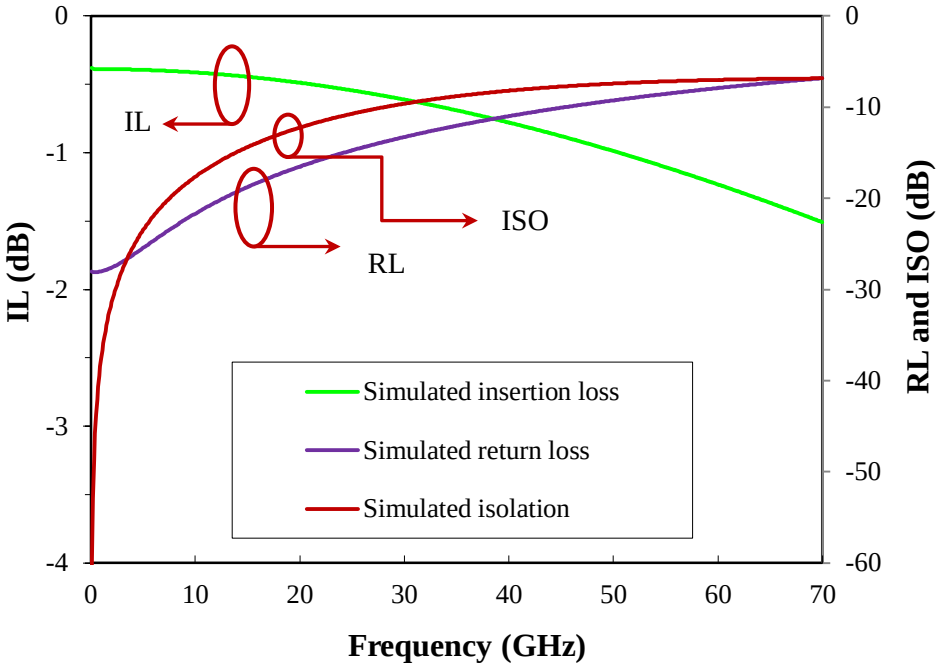


Figure 4-2 Simulated S-parameters of series only wideband switch

Simulated dc-70 GHz S-parameters, including insertion loss (IL), return loss (RL) and solation (ISO) of a series only switch are shown in Figure 4-2. The simulations were done with GLOBALFOUNDRIES's 0.13-µm RFSOI PDK. Simulated IL is quite low in the whole frequency range, less than 0.7 dB at 30 GHz and less than 1.3 dB at 60 GHz, respectively.

However, this series only switch shows poor isolation, simulated isolation is lower than 10 dB at 30 GHz.

Insertion loss and isolation of this series SPST switch can be derived as following. ABCD matrix can be used to analysis the circuit. When switch is on, the network between Port 1 and Port 2 in Figure 4-1 with ABCD matrix is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_{on} \\ 0 & 1 \end{bmatrix} \tag{4-1}$$

The insertion loss between Port 1 and Port 2 can be deduced as:

$$IL_{21} = -20log|S_{21}| = -20log\left|\frac{2}{A + {B}/{Z_0} + CZ_0 + D}\right| \tag{4-2}$$

Where, S_{21} is converted from ABCD. Substituting (4-2) into (4-1),

$$IL_{21} = -20log|S_{21}| = -20log\left|\frac{2}{A + {B}/{Z_0} + CZ_0 + D}\right| = -20log\left|\frac{2}{2 + {R_{on}}/{Z_0}}\right|$$

$$= 20log\left|1 + \frac{R_{on}}{2Z_0}\right| \tag{4-3}$$

So the actual insertion loss in dB can be calculated by:

$$IL = 20\log(1 + \frac{R_{on}}{2Z_0}) = 10\log(1 + \frac{R_{on}}{2Z_0})^2 \quad (4\text{-}4)$$

Where:

R_{on} = the resistance of M_1 when the switch is on,

Z_0 = the impedance of the source and load ports ($50\,\Omega$)

In off state, equivalent model is as shown in Figure 4-1 (c), similarly, the isolation of the series SPST switch can be derived as shown below:

ABCD matrix for the off state is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{j\omega C_{off}} \\ 0 & 1 \end{bmatrix} \quad (4\text{-}5)$$

The isolation between Port 1 and Port 2 can be deduced as:

$$ISO_{21} = -20log|S_{21}| = -20log\left|\frac{2}{A + {}^{B}/_{Z_0} + CZ_0 + D}\right| = -20log\left|\frac{2}{2 + \frac{1}{j\omega C_{off} Z_0}}\right|$$

$$= 20log\left|1 + \frac{1}{j\omega C_{off} Z_0}\right| \quad (4\text{-}6)$$

The actual isolation in dB can be calculated by

$$ISO = 10\log\left[1 + (\frac{R_{on}}{4\pi f C_{off} Z_0})^2\right] \quad (4\text{-}7)$$

Where:

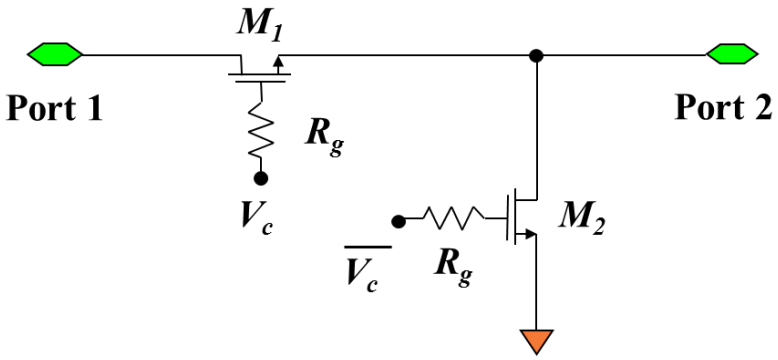
C_{off}=the capacitance of M1 when the switch is off,

Z_0 = the impedance of the source and load ports (50Ω),

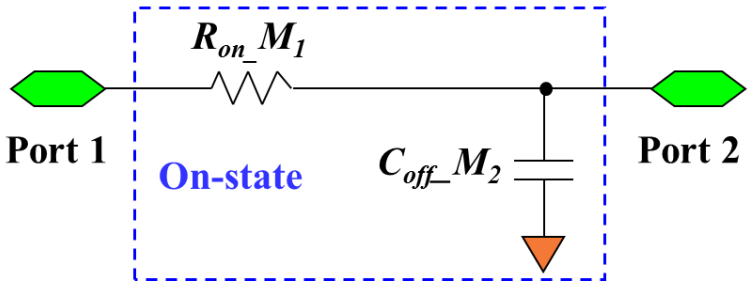
ω = radian frequency of the RF input, and is given by 2πf, where f is the frequency of the RF input.

4.1.2 Series-shunt configuration

To improve the isolation of the switch with transistor in series only in the off-state, a shunt NMOS transistor M_2 need to be added. Schematic and equivalent model of "on" and "off" states of the series-shunt type SPST are illustrated in Figure 4-3. In the normal off-state, M_1 is turned off and M_2 is turned on, so that blocking the input signal from the output node. In the normal on-state, M_1 is turned on and M_2 turned off, thus the input signal can be delivered to output node.



(a)



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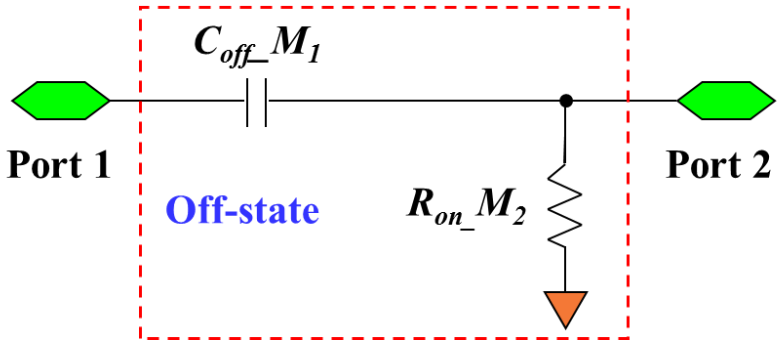
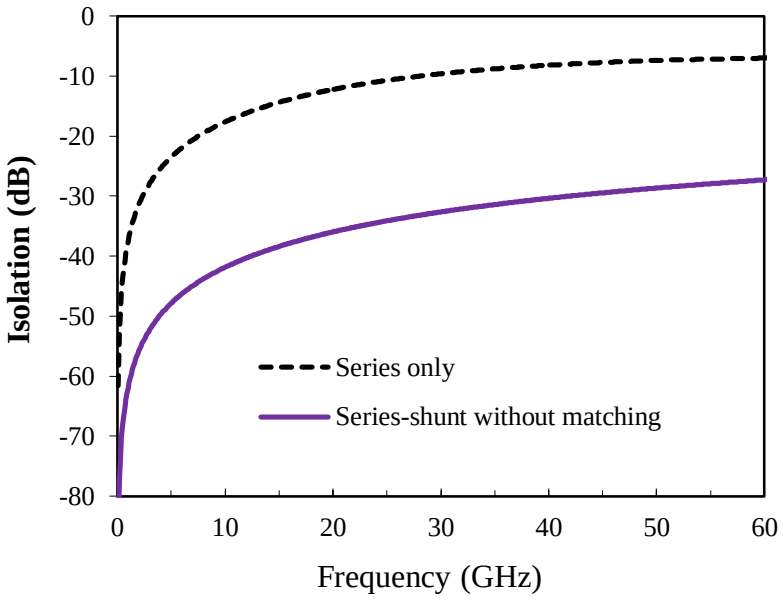


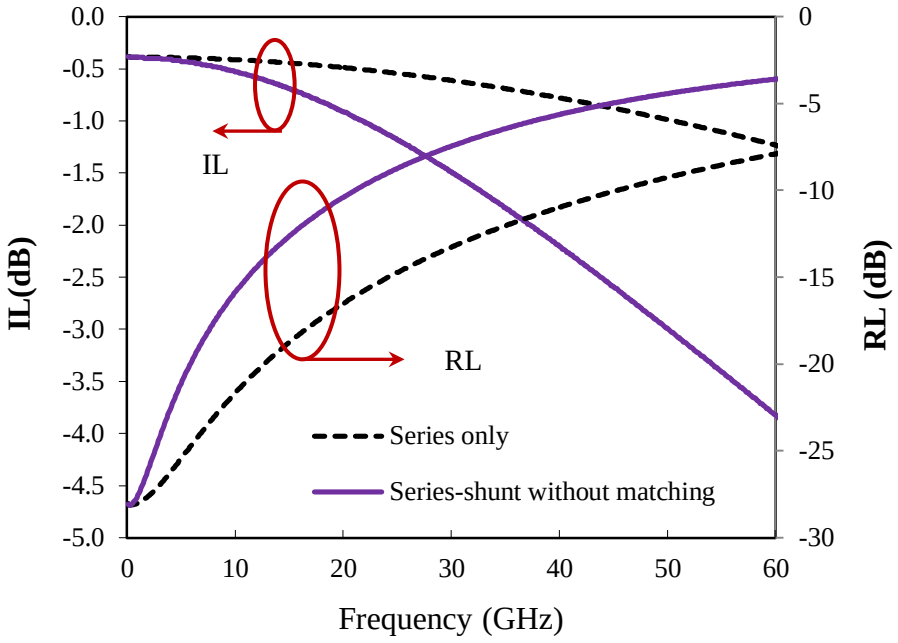
(c)

Figure 4-3 (a) Schematic of series-shunt SPST switch, (b) Equivalent model of "on" state and (c) Equivalent model of "off" state

As can be seen from Figure 4-4, by implementing the series-shunt topology, the simulated isolation is much higher than series only topology. Simulated isolation at 30 GHz is higher than 30 dB, which is 20 dB higher than series only SPST switch.



(a)



(b)

Figure 4-4 Simulated S-parameters of series-shunt wideband switch

Insertion loss and isolation of the series-shunt SPST switch can be derived using similar method as series only SPST switch.

In the on state, based on the equivalent model shown in Figure 4-3 (b), the ABCD matrix between Port 1 and Port 2 is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_{on} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\omega C_{off} & 1 \end{bmatrix} = \begin{bmatrix} 1 + R_{on} j\omega C_{off} & R_{on} \\ j\omega C_{off} & 1 \end{bmatrix} \quad (4\text{-}8)$$

Insertion loss for this series-shunt SPST switch can be deduced as

$$IL_{21} = -20log|S_{21}| = -20log\left|\frac{2}{A + {B}/{Z_0} + CZ_0 + D}\right|$$

$$= -20log\left|\frac{2}{1 + R_{on}j\omega C_{off} + {R_{on}}/{Z_0} + j\omega C_{off}Z_0 + 1}\right|$$

$$= 20log\left|\left(1 + \frac{R_{on}}{2Z_0}\right) + \frac{j\omega C_{off}(R_{on} + Z_0)}{2}\right| \quad (4\text{-}9)$$

So the actual insertion loss in dB can be calculated by

$$IL = 10\log\{\left(1 + \frac{R_{on}}{2Z_0}\right)^2 + [\pi f C_{off}(R_{on} + Z_0)\,]^2\} \quad (4\text{-}10)$$

Where:

R_{on} = the on resistance of M_1 when the switch is on, and

C_{off} = the capacitance of off state M_2 when the switch is on.

In the off state, based on the equivalent model shown in Figure 4-3 (c), the ABCD matrix between Port 1 and Port 2 is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{j\omega C_{off}} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ \frac{1}{R_{on}} & 1 \end{bmatrix} = \begin{bmatrix} 1 + \frac{1}{R_{on}j\omega C_{off}} & \frac{1}{j\omega C_{off}} \\ \frac{1}{R_{on}} & 1 \end{bmatrix} \quad (4\text{-}11)$$

So isolation between Port 1 and Port 2 is

$$ISO = -20log|S_{21}| = -20log\left|\frac{2}{A + {}^{B}/_{Z_0} + CZ_0 + D}\right|$$

$$= -20log\left|\frac{2}{2 + {}^{1}/_{R_{on}j\omega C_{off}} + {}^{1}/_{j\omega C_{off}Z_0} + {}^{Z_0}/_{R_{on}}}\right|$$

$$= 20log\left|\frac{1}{2j\omega C_{off}Z_0}(1 + \frac{Z_0}{R_{on}}) + (1 + \frac{Z_0}{2R_{on}})\right|$$

(4-12)

So the isolation in dB can be calculated by

$$ISO = 10\log\left[\left(\frac{R_{on}}{4\pi f C_{off}Z_0}\right)^2\left(1 + \frac{Z_0}{R_{on}}\right)^2 + \left(1 + \frac{Z_0}{2R_{on}}\right)^2\right] \quad (4\text{-}13)$$

Where:

R_{on} = the on resistance of the shunt transistor M_2 when the switch is off, and

C_{off} = the capacitance of off state M_1 when the switch is off.

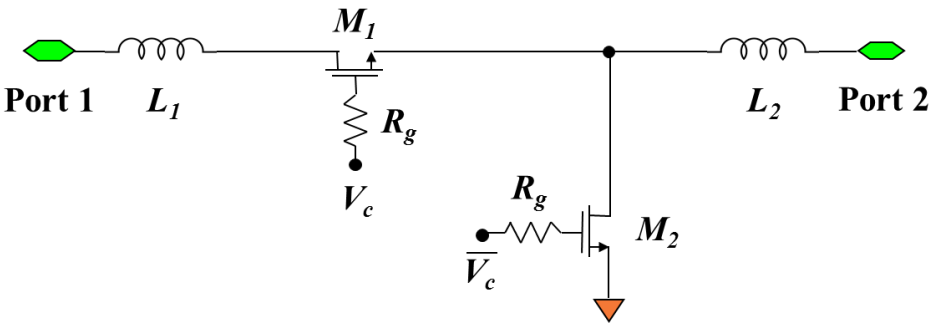
When compared with series only switch isolation, which is shown in Equation 4-7, since R_{on} of the shunt transistor M_2 is much lower than Z_0, isolation for series-shunt SPST

will be much improved. Based on calculation, with same series transistor size, isolation of the series-shunt SPST will be more than 20 dB higher than series only SPST switch, which is consistent with the simulated isolation result, as shown in Figure 4-4 (a). However, the insertion loss for series-shunt SPST will be degraded because of the off state capacitance of the shunt transistor, as can be seen from Equation (4-10), and this trend is also shown in the simulated insertion loss curves as shown in Figure 4-4 (b).

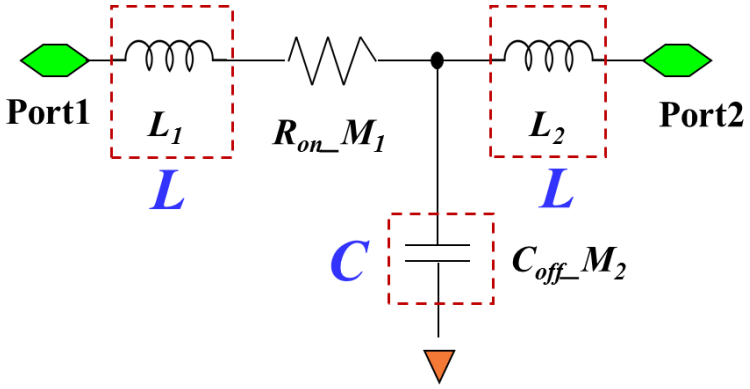
At the same time, for both series only and series-shunt topologies, the simulated return losses are bad, especially for the series-shunt configuration. This will significantly limit the switch's bandwidth, to achieve wideband application, input and output matching network need to be implemented.

4.1.3 Series-Shunt with matching network Configuration

For this design, two on-chip series inductors, L_1 and L_2 are added to the series-shunt SPST switch, placed at the source and drain node of the switch NMOS and act as a *L-C-L* T-matching circuit together with the off-state capacitance of the shunt NMOS M2. Schematic for this switch and equivalent matching network are shown in Figure 4-5. IL, RL and ISO of this switch are simulated. Figure 4-6 shows the performance comparison of the three different SPST topologies, including series only, series-shunt and series-shunt with input/output matching network. As can be seen from Figure 4-6 (b), the return loss is much improved from dc to 30GHz frequency region by implementing the T-matching network. By optimizing the switch NMOS size and the matching inductor value, the return loss can be further improved. And as shown in Figure 4-6 (c), the isolation performance is comparable to the series-shunt topology, while the insertion loss is reduced at dc to 40GHz frequency region as shown in Figure 4-6 (a).

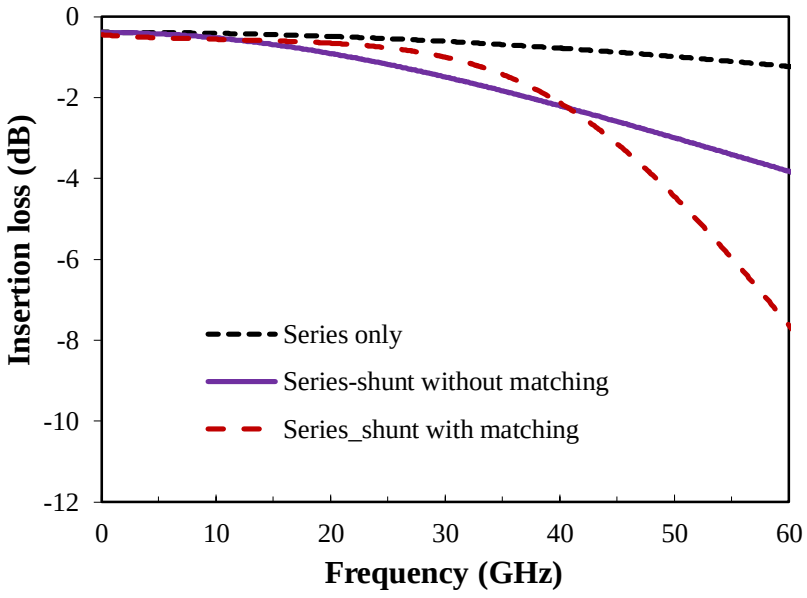


(a)

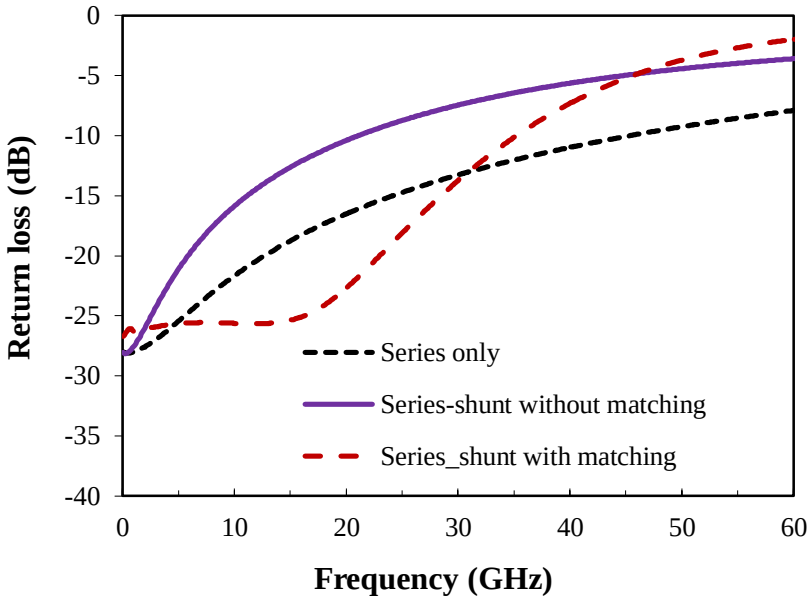


(b)

Figure 4-5 (a) Schematic of series-shunt with matching network SPST switch, (b) Equivalent *L-C-L* T-matching network model



(a)



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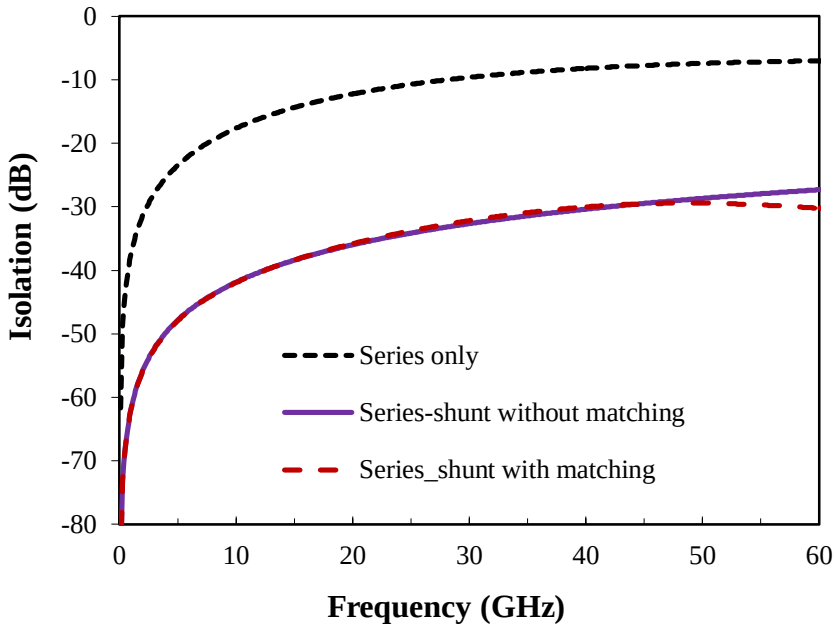


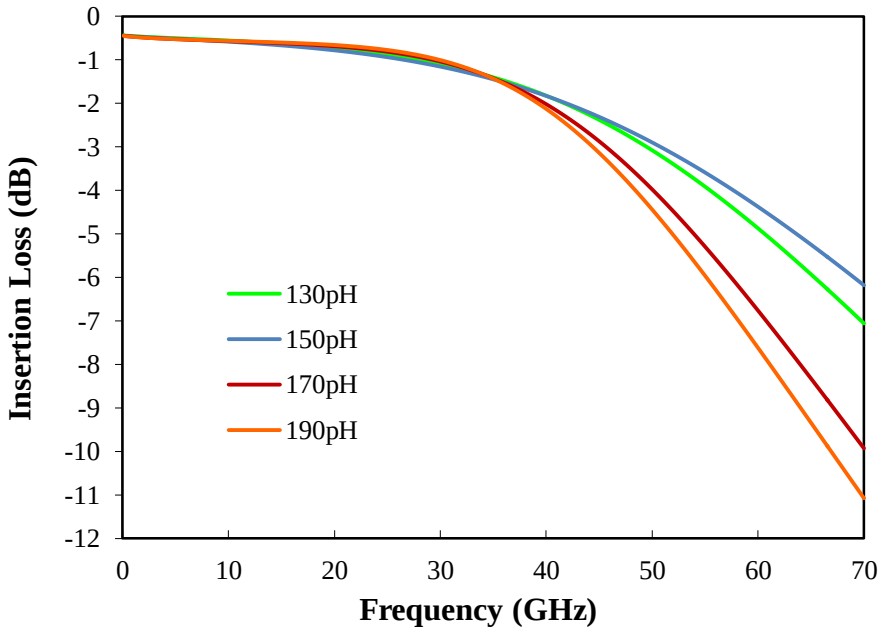
(c)

Figure 4-6 Simulated IL, RL and ISO for different SPST topologies, (a) IL, (b) RL and (c) ISO

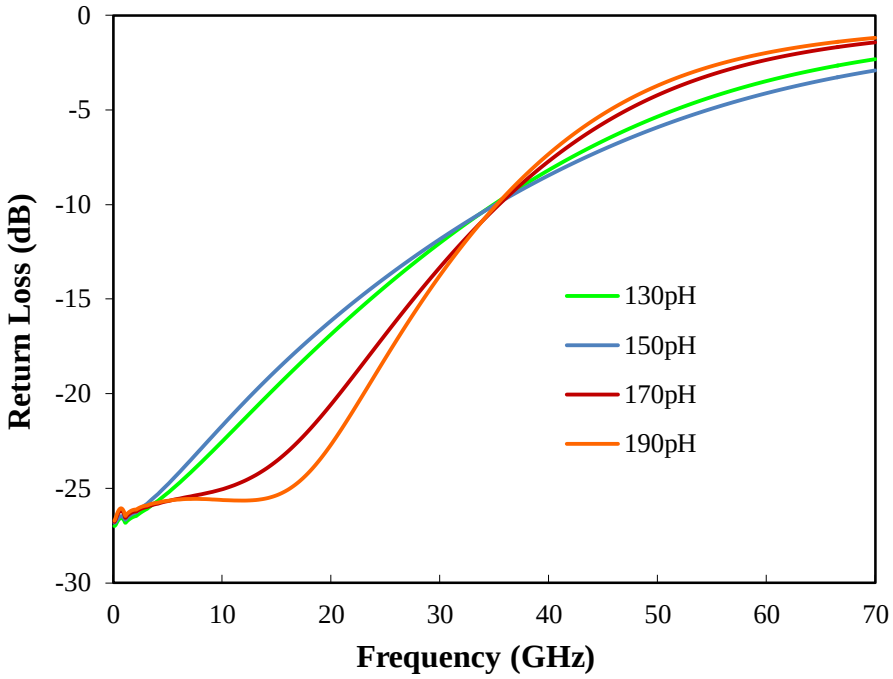
4.2 SPST switch device size selection

4.2.1 Simulation on varying matching inductor value

Impact of the matching inductor on series-shunt SPST switch (W =100 μm for series NMOS and W =150 μm for the shunt NMOS) switch is simulated as shown in Figure 4-7, the isolation performance are comparable for different inductor values (L=130 pH, 150 pH, 170 pH and 190 pH for this comparison). Insertion loss is comparable for all the different inductor values from dc to 35 GHz, but in the higher frequency region, the higher inductor value, the higher insertion loss. For return loss, from dc to 35 GHz, the higher inductor value, the better return loss, while when frequency is higher than 35 GHz, the higher inductor value, the worse return loss. So the inductor value needs to be optimized to maximize the matching bandwidth.



(a)



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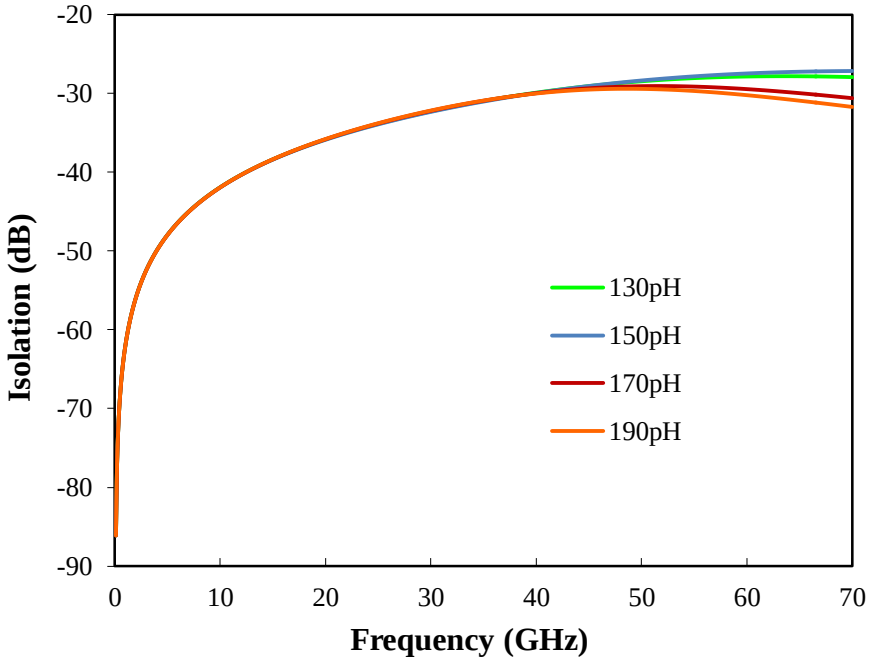
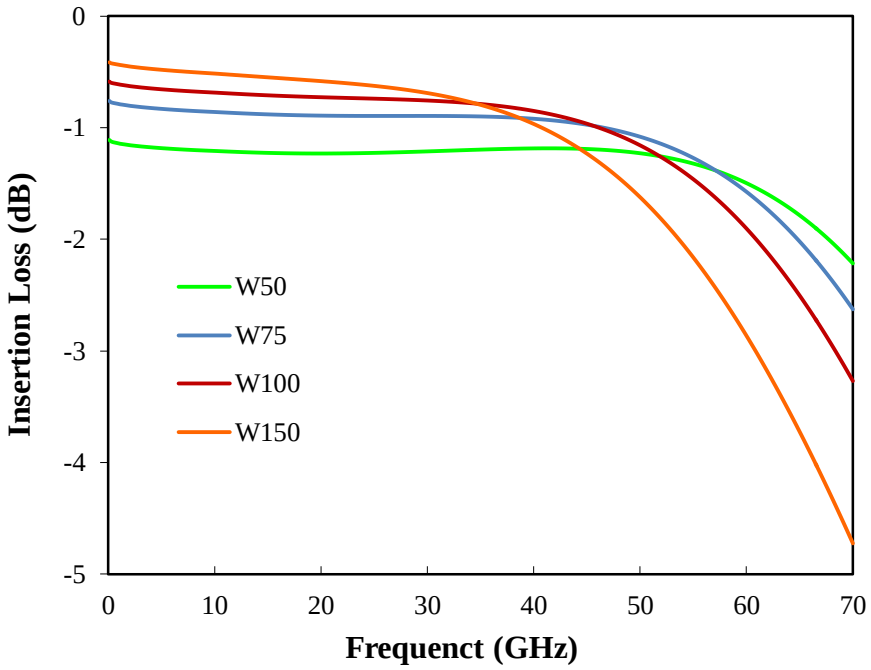


(c)

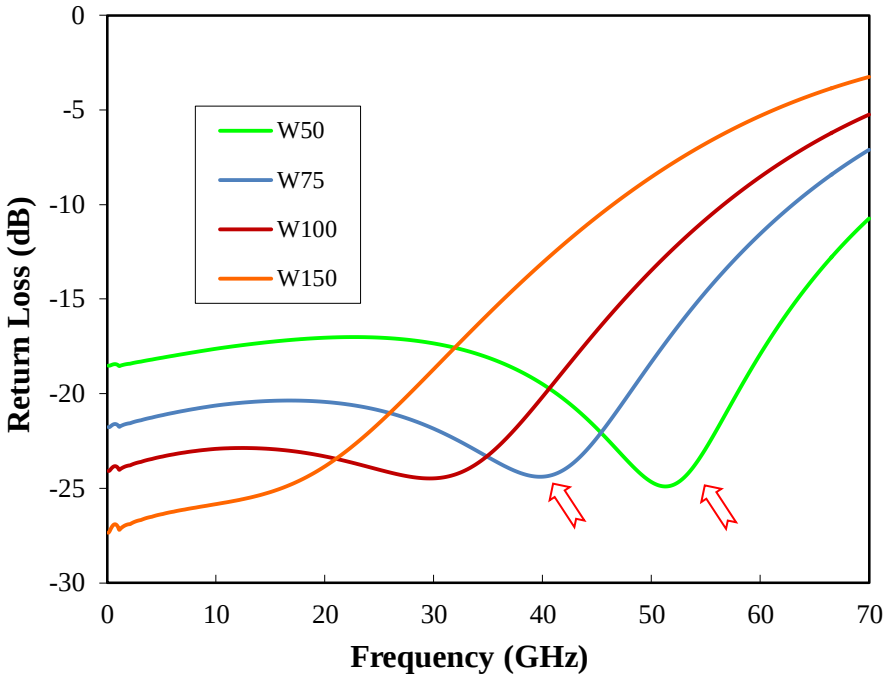
Figure 4-7 Simulated (a) IL, (b) RL and (c) ISO as a function of matching inductor value

4.2.2 *Simulation on varying series transistor width*

Impact of the series transistor width is simulated as shown in Figure 4-8. The simulation was done with a fixed shunt transistor width W =100 μm and fixed matching inductors L_1=L_2=140 pH. As can be seen in Figure 4-8 (a), in a relatively low frequency range, the wider transistor width, the lower switch insertion loss is because of lower transistor R_{on}. While in high frequency range, insertion loss of wider transistor drops faster than that of narrow width switch, because of higher self-capacitance. At the same time, as transistor width increases, the switch isolation becomes worse which is resulted from higher off state parasitic capacitance as shown in Figure 4-8 (c). The matching network introduces a notch in the return loss response, as highlighted by the arrow in Figure 4-8 (b). The location of notch depends on the size of the series transistor, when design the circuit, the notch location need to be considered in order to maximize the application bandwidth.



(a)



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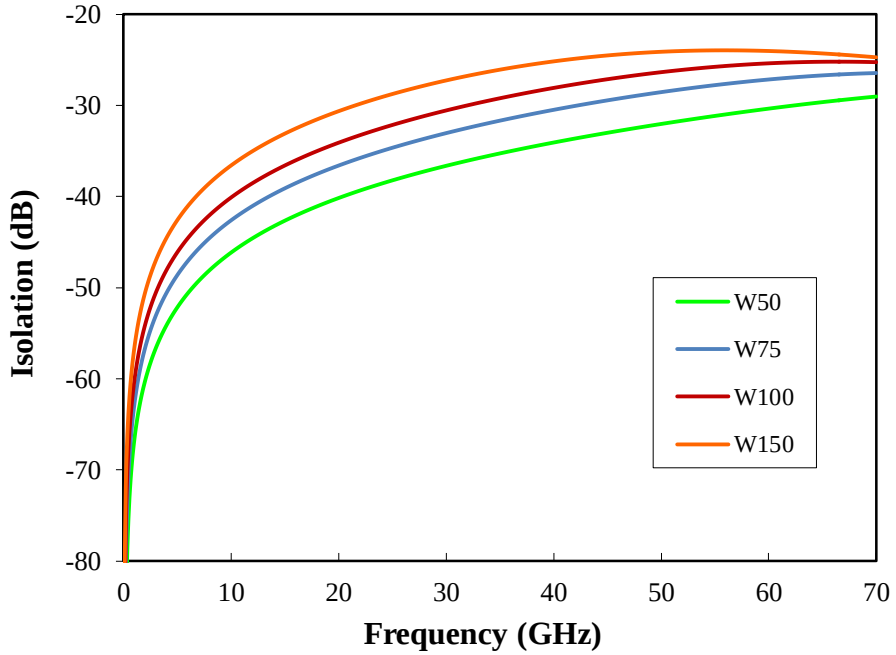
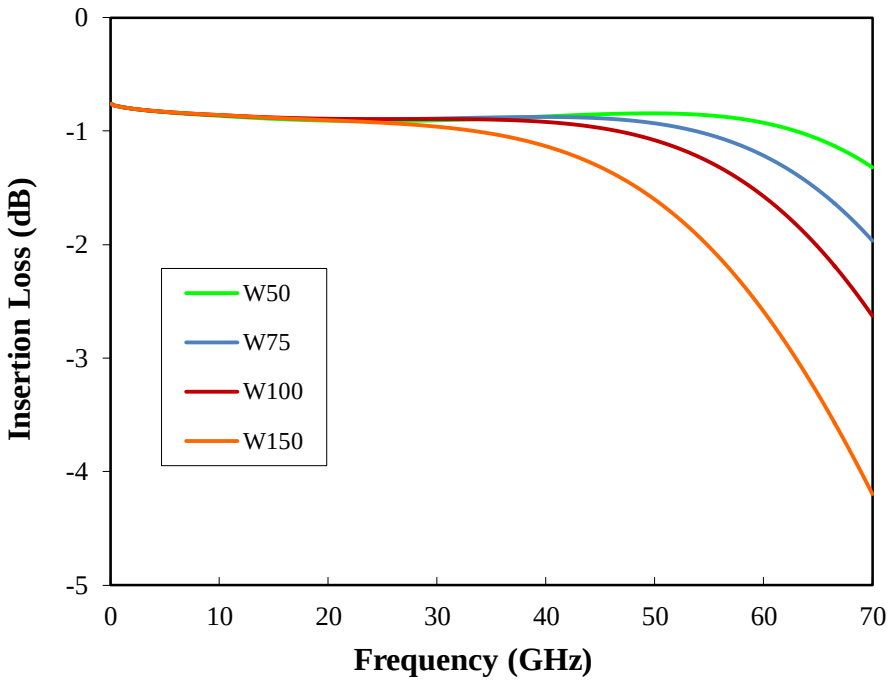


Figure 4-8 Simulated (a) IL, (b) RL and (c) ISO as a function of series transistor width

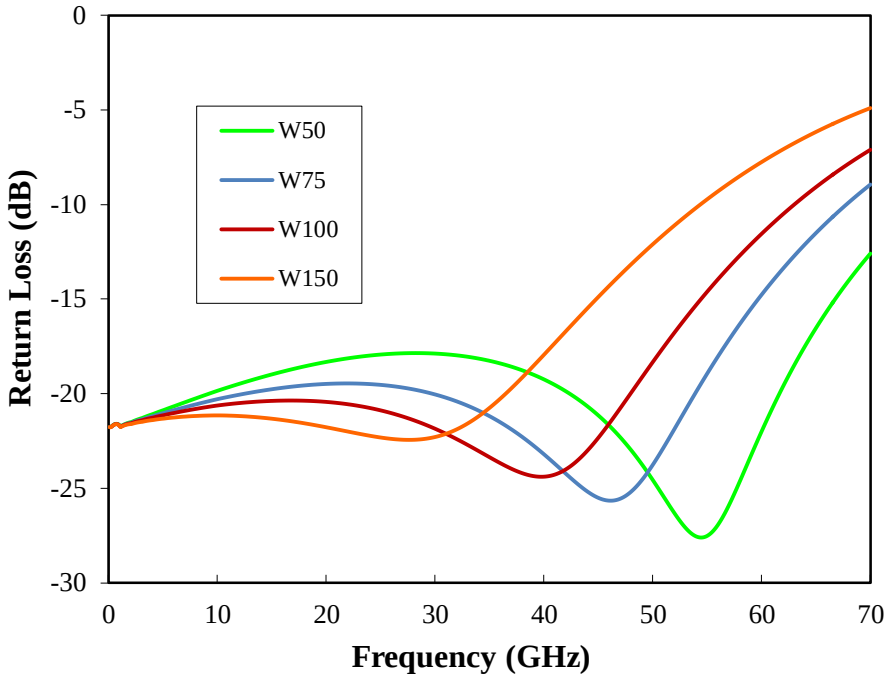
4.2.3 Simulation on varying shunt transistor width

Figure 4-9 shows the simulated S-parameters of different shunt transistor width with same series transistor size (W =75 μm). As predicted by Equation (4-10), when frequency is related low, dc to 30 GHz as shown in Figure 4-9 (a), since insertion loss is dominated by the series transistor, so the insertion loss of switches with different shunt transistor are comparable. When frequency is high enough, C_{off} of the shunt transistor induces more and more insertion loss, as C_{off} of the shunt transistor increases with the transistor width, so the insert loss of switch with wider shunt transistor drops faster.

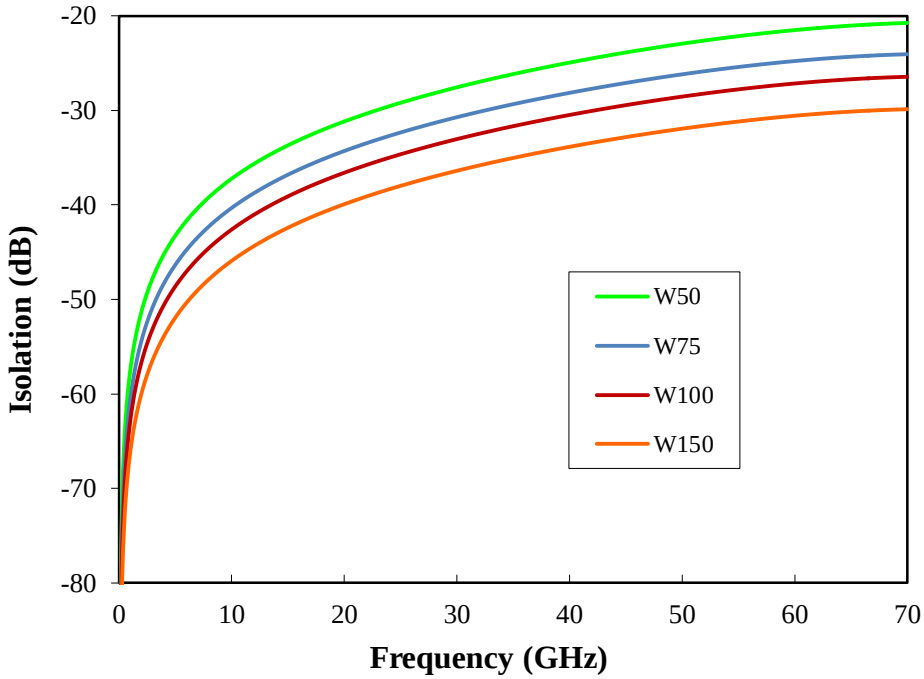
As predicted by Equation (4-13), if the series transistor size is the same, then switch isolation is dominated by R_{on} of the shunt transistor. So switch isolation becomes higher when the transistor width increases from 50 to 150 μm, as shown in Figure 4-9 (c).



(a)



(b)



(c)

Figure 4-9 Simulated (a) IL, (b) RL and (c) ISO as a function of shunt transistor width

4.3 Summary

In this chapter, S-parameters of different SPST switches configurations, including series only, series-shunt and series-shunt with input output matching network, are simulated and analyzed. To achieve ultra wideband (dc to 70 GHz) application, series-shunt with input output matching network should be adopted. Based on the series-shunt with matching network configuration, impact of series transistor size, shunt transistor size, as well as matching inductor value, on the SPST performance are simulated and analyzed. Simulated SPST switch performances under different series and shunt transistor size and matching inductor value are summarized in Table 4-1. The simulation result show SPST switch designed with this SOI technology can achieve very low insertion loss (<1 dB up to 40 GHz), excellent isolation (>30 dB update to 40 GHz) in ultra-wide range of frequency from dc to across millimeter wave by optimizing the size of both series and shunt transistor and matching inductor value.

Table 4-1 Simulated SPST Performance

Type	Series	Shunt	L1	L2	Frequency	IL	Isolation	RL	Input P1dB (dBm)	
	(μm)	(μm)	(pH)	(pH)	(GHz)	(dB)	(dB)	(dB)	@ 1GHz	@ 30GHz
SPST	50	100	140	140	dc-40	<1.2	>34	>17	12.6	12.33
	75	100	140	140	dc-40	<0.92	>30	>20	13.29	12.65
	100	100	140	140	dc-40	<0.85	>28	>20	13.54	12.76
	150	100	140	140	dc-40	<0.97	>25	>13	13.69	12.89
	75	50	140	140	dc-40	<0.92	>27.5	>17.8	13.56	13.1
	75	75	140	140	dc-40	<0.9	>30.5	>19	13.42	12.85
	75	150	140	140	dc-40	<1.15	>33.5	>17.9	13.06	12.36

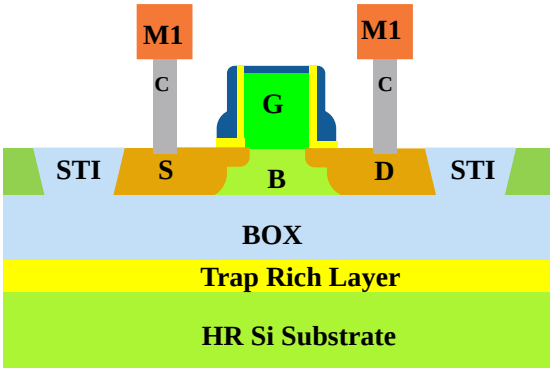
Chapter 5

Ultra wideband SPDT switch design

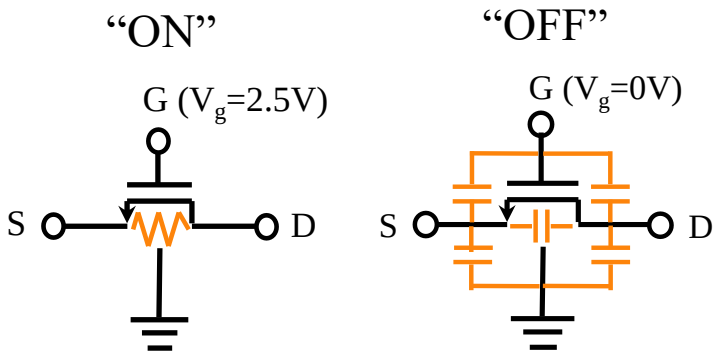
5.1 SOI NMOS schematic and substrate

GLOBALFOUNDRIES's 0.13-μm RFSOI process offers 2.5 V body-tied thick gate oxide NMOS switch transistor (nominal gate length, L_g = 0.2 μm), with a low R_{on}*C_{off} product, the oxide thickness is about 6.5 nm [67]. The schematic of high resistivity trap-rich SOI substrate and simplified model of the SOI NMOS are shown in Figure .The thickness of the top silicon and BOX are around 1600 Å and 4000 Å, respectively, the handle Si substrate has a resistivity of higher than 3000 ohm-cm, the trap rich layer is in between the BOX and handle Si.

Figure 5-2 shows the measured harmonic distortion (HD) outputs at 900 MHz with input power (Pin) from -25 dBm to +25 dBm from CPW lines on high resistivity (HR) bulk silicon wafer and the HR TR SOI wafer, respectively. The CPW metal is a 3μm thick Cu layer on 60 nm of oxide with length of 2.1 mm. The second order harmonics (H_2) of the HR TR SOI substrate is about 10 dB lower than that of the HR bulk silicon substrate over the power range from 0 to 25 dBm, this can enable the device and circuit to meet high linearity requirements.



(a)



(b)

Figure 5-1 (a) Schematic view of an SOI NMOS and (b) Small signal model of SOI MOSFET on “ON” state and “OFF” state

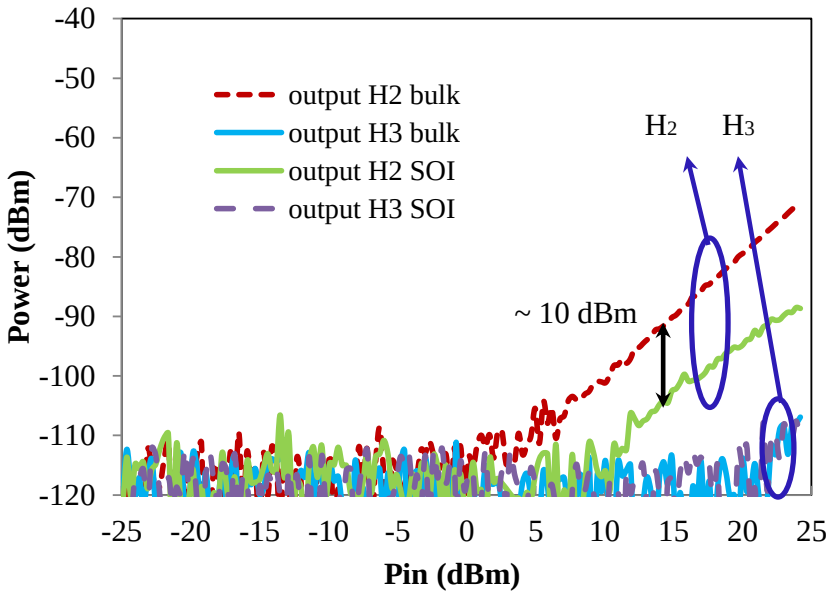


Figure 5-2 Measured H_2 and H_3 for HR bulk and HR SOI substrate with trap-rich layer

5.2 Stress memorization technique (SMT) and device characterization

It is well known, R_{on} *C_{off} is a critical figure of merit for switch, both R_{on} and C_{off} are as low as possible to ensure switches with low insertion loss and high isolation. The on-state channel resistance R_{on} of a transistor can be expressed as:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{5-1}$$

Where μ is the transistor channel mobility, W and L are channel width and length respectively, and V_{GS} and V_T are gate source bias and threshold voltage respectively. So ways to improve R_{on} include channel mobility increase, gate oxide thickness decrease, channel length reduction and using higher gate bias.

Stress memorization technique (SMT) has been used to improve channel mobility for advanced technology nodes [68]–[70]. However, to the best of the author's knowledge, SMT implementations on switch design, especially for ultra wideband switch design is not reported.

For SMT NMOS, typically a tensile capping layer is deposited on the wafer prior to a high temperature anneal, tensile stress is then induced during anneal process, resulting electron mobility improvement in the NMOS channel.

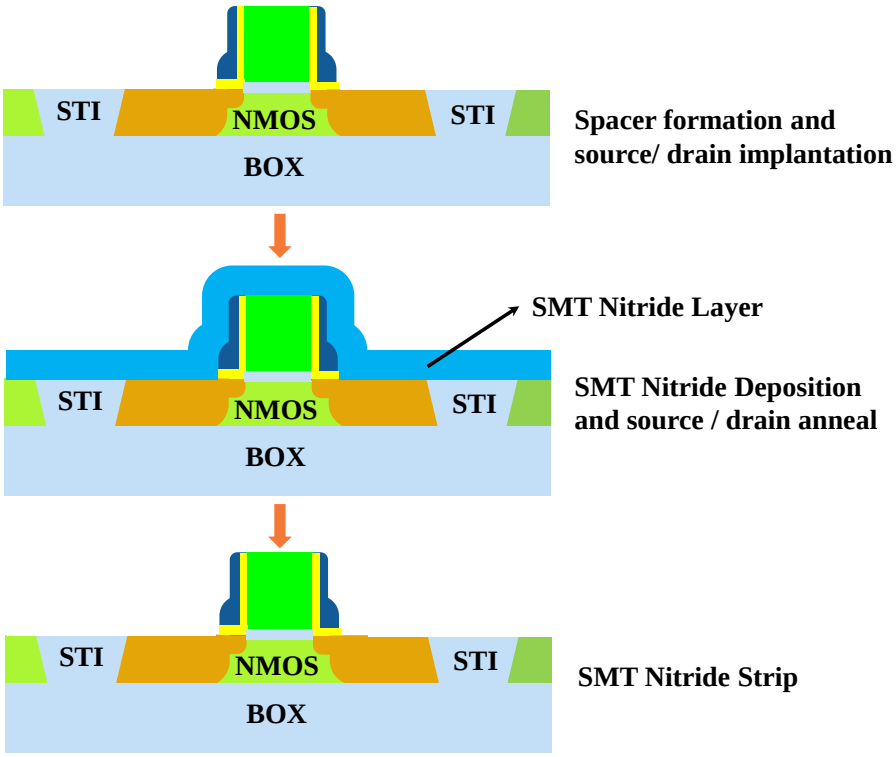
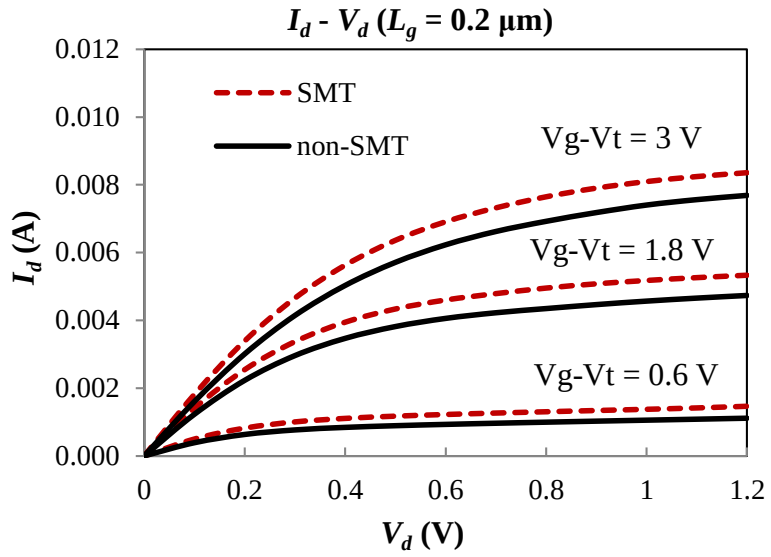
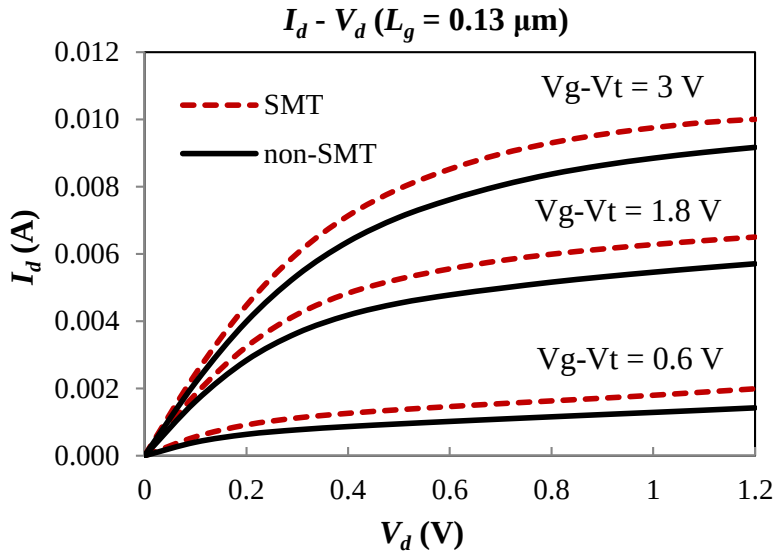


Figure 5-3 Process sequence of SMT integration

The process sequence of SMT integration in this 0.13-μm SOI process is illustrated in Figure 5-3, it involves the deposition of a 900 Å sacrificial tensile nitride film prior to switch NMOS source/ drain anneal, to induce the SMT effect to improve channel mobility during source drain spike anneal, this layer was then stripped after source drain anneal. Normal process (non-SMT) does not have the film deposition and strip steps. The remaining process steps are equivalent to the baseline process.



(a)



(b)

Figure 5-4 SOI Switch NMOS I_d-V_d characteristics, (a) L_g = 0.2 µm, (b) L_g = 0.13 µm

Figure 5-4 shows the measured I_d - V_d curves for switch NMOS transistors fabricated with SMT and non-SMT process for channel length L_g = 0.13 µm and L_g = 0.2 µm. More than 10% improvement in Id are observed from SMT NMOS compared to non-SMT NMOS for both L_g = 0.13 µm and L_g = 0.2 µm NMOS transistor.

5.3 SOI NMOS C_{off} model

C_{off} model of the used SOI switch NMOS is shown in Figure 5-5. Both intrinsic capacitances and extrinsic wiring capacitances contribute to total C_{off}, including gate (G) to source (S) overlap capacitance C_{GSO}, gate to drain (D) overlap capacitance C_{GDO}, source to body (B) junction capacitance C_{SB}, drain to body junction capacitance C_{DB}, source drain to substrate capacitance $C_{SD\text{-}Sub}$, contact (C) to gate capacitance $C_{C\text{-}G}$, 1st metal layer (M1) to gate capacitance $C_{M1\text{-}G}$, and M1 to M1 capacitance $C_{M1\text{-}M1}$. The total C_{off} is as expressed in Equation (5-2)

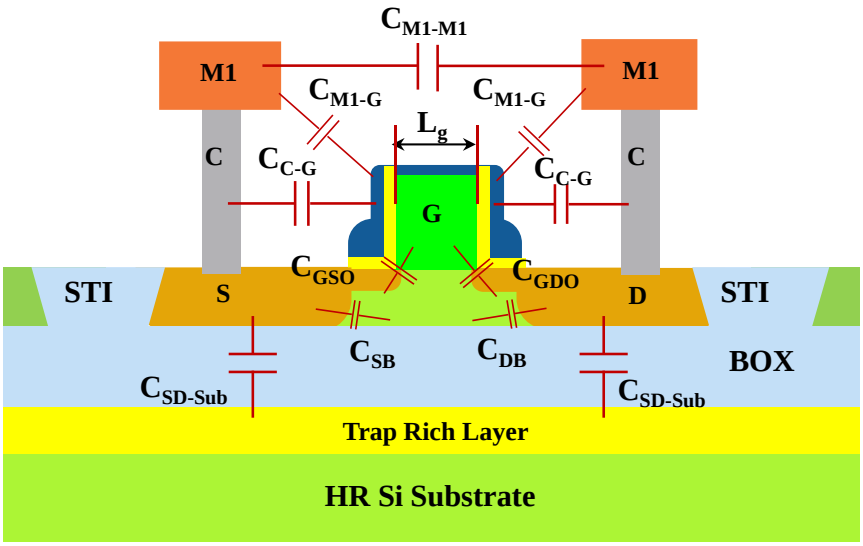


Figure 5-5 C_{off} model of the SOI switch NMOS

$$C_{off} = \frac{C_{SB}.C_{DB}}{C_{SB}+C_{DB}} + \frac{C_{GSO}.C_{GDO}}{C_{GSO}+C_{GDO}} + \frac{C_{SD-Sub}}{2} + C_{M1-M1} + \frac{C_{M1-G}}{2} + \frac{C_{C-G}}{2} \qquad (5\text{-}2)$$

Table 5-1 Performance Summary and R_{on} and C_{off} Comparison (SMT vs. Non-SMT)

Process	L_g = 0.13 µm			L_g = 0.20 µm		
	R_{on} (ohm-mm)	C_{off} (fF/mm)	R_{on}* C_{off} (fs)	R_{on} (ohm-mm)	C_{off} (fF/mm)	R_{on}* C_{off} (fs)
Non-SMT	0.49	180	88.2	0.67	148	99.2
SMT	0.43	186	80.0	0.59	154	90.8

Table 5-1 summarizes the measured R_{on} and C_{off} for both SMT and non-SMT from foundry monitoring structures. R_{on} were from single SOI NMOS, and C_{off} for L_g = 0.13 μm were measured from 1mm/FET 1 stack of switch FETs, C_{off} of L_g = 0.2 μm were measured from 4 mm/FET 12 stacks of switch FETs, respectively, both without external poly resistor connected. The poly shortening from 0.2 μm to 0.13 μm follows the conventional rule, which keeps the source/ drain contact to gate space unchanged. R_{on} of SMT NMOS is about 12% lower than non-SMT NMOS for the same gate length. So in the presence of stressors, NMOS channel mobility is much improved. At the same time, measured C_{off} for SMT NMOS is about 3% higher than non-SMT NMOS. As reported in [70], SMT induces some Boron (B) dose loss during the anneal process, causing overlap capacitance shift. In this work, the slightly higher C_{off} for SMT NMOS should also due to Boron (B) dose reduction in the SOI switch NMOS extension junction, which slightly widens the overlap area, and increases the C_{GSO} and C_{GDO}. As a result, the product of R_{on} *C_{off} of SMT NMOS is about 9% lower than non-SMT NMOS.

5.4 SPDT topology

Based on study on SPST switch in Chapter 4, the ultra-wideband SPDT switches are designed based on series-shunt topology with input and output matching networks, as shown in Figure 5-6. The SPDT switch is constructed by two symmetric SPST switch branches, one SPST branch, with series transistor M_3 and shunt transistor M_4, forms the path between Port 1 and Port 2, and the other SPST branch, combined by series transistor M_1 and shunt device M_2, forms another path between Port 1 and Port 3. The L_1 is used as the matching inductor for the Port 1, and two L_2 inductors are used for Port 2 and Port 3, respectively. The equivalent *L*-*C*-

L T-matching network model is same as that of SPST switch, which is shown in Figure 4-10 (b). When V_C is high (= 2.5 V), M_2 and M_3 are turned on, M_1 and M_4 are turned off, so RF signal can flow between Port 1 and Port 2. When V_C is low (0 V for this design), M_1 and M_4 are turned on, M_2 and M_3 are turned off, so signal can be transferred between Port 1 and Port 3. A gate resistor R_g, is required for each transistor for AC floating to minimize the signal leakage and prevent gate oxide breakdown.

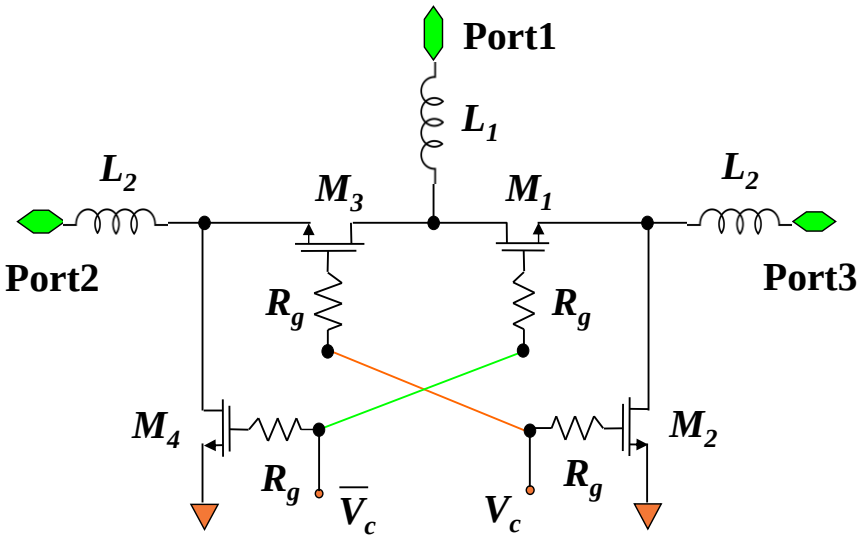
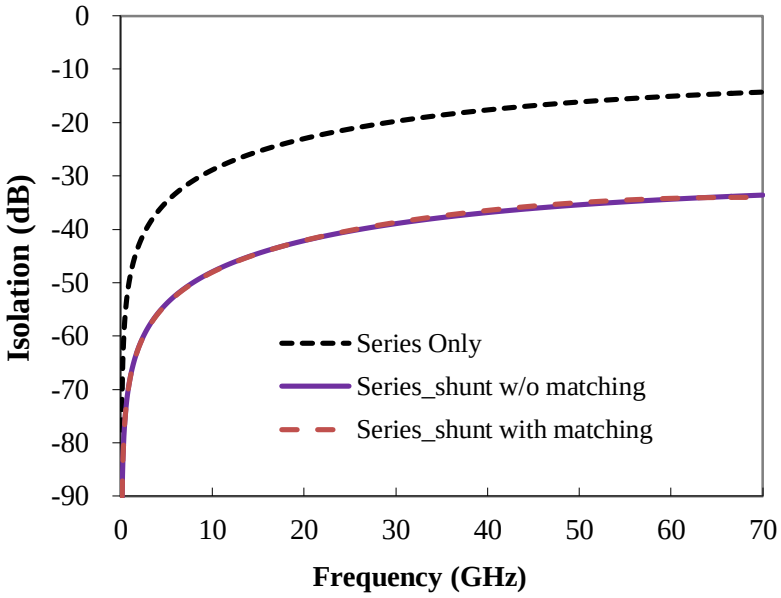
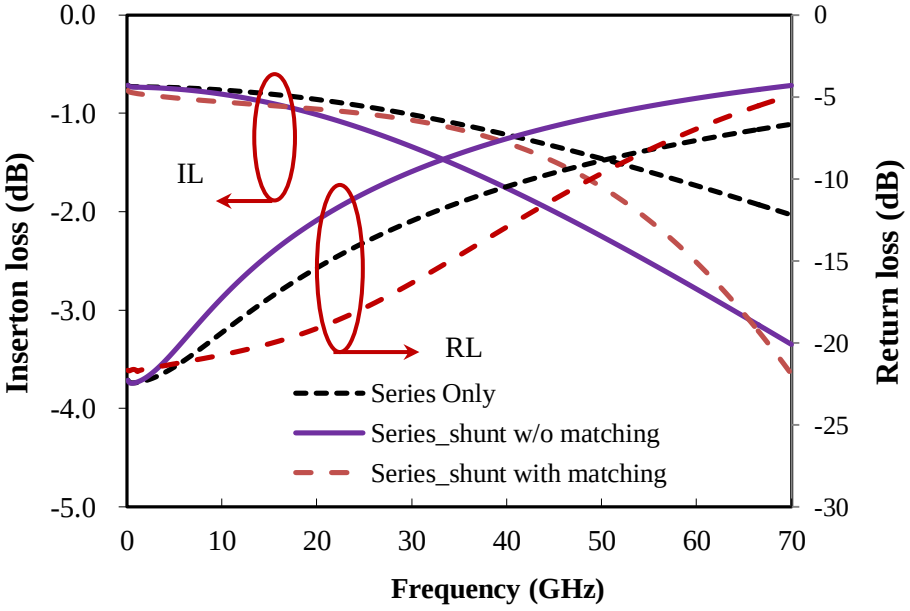


Figure 5-6 Schematic of the designed SPDT switch

Simulation on SPDT switch with different configurations is carried out as shown in Figure 5-7. Similar to SPST switch, the series only SPDT switch shows much lower isolation compared to series-shunt topology. Isolation can be improved by adding shunt transistor, while the return loss and the insertion loss will increase, which will degrade the switch's bandwidth. The series-shunt with matching network switch shows comparable isolation while much improved insertion loss and return loss when compared to series-shunt without matching networks.



(a)

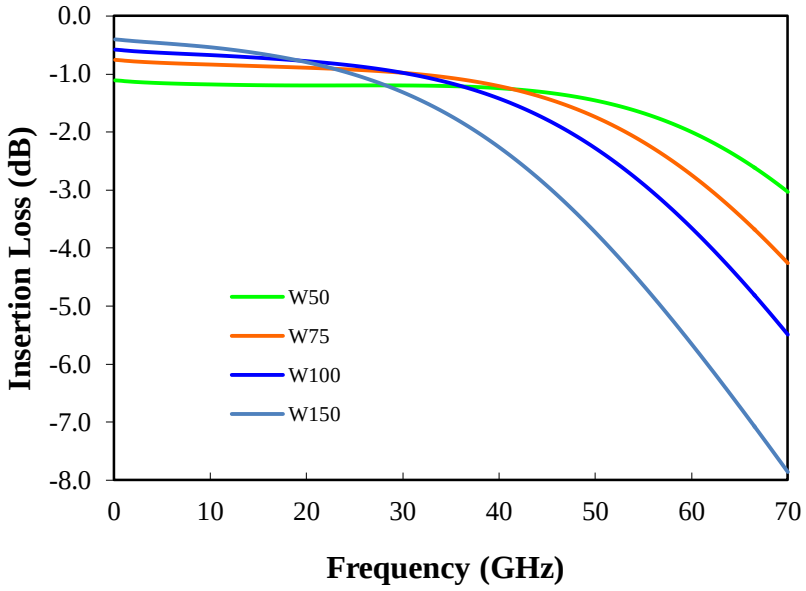


(b)

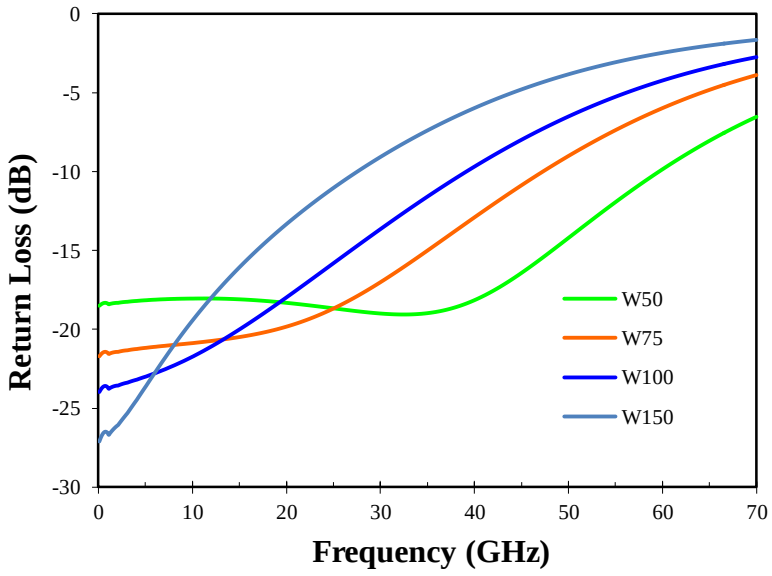
Figure 5-7 Simulated: (a) isolation and (b) insertion loss and return loss of different SPDT switch configurations.

For a given transistor channel length L_g, the wider transistor is used, the lower *Ron* is achieved. But at the same time the parasitic capacitance will be also increased, thus the

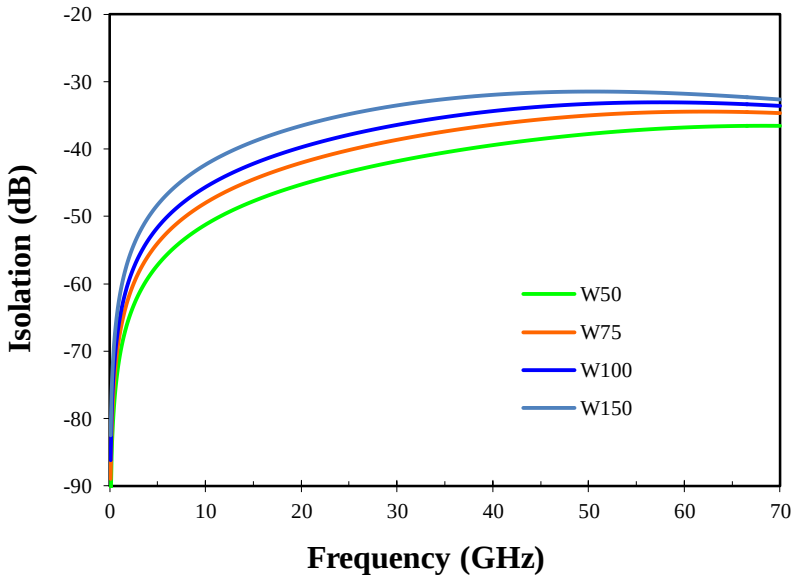
isolation is degraded and signal loss is increased, so transistor width needs to be optimized during circuit design. The matching inductors are also critical for switch performance to maximize the bandwidth. The impacts of series and shunt transistor width and matching inductor on SPDT switch performance are simulated and shown in Figure 5-8, Figure 5-9 and Figure 5-10, respectively.



(a)

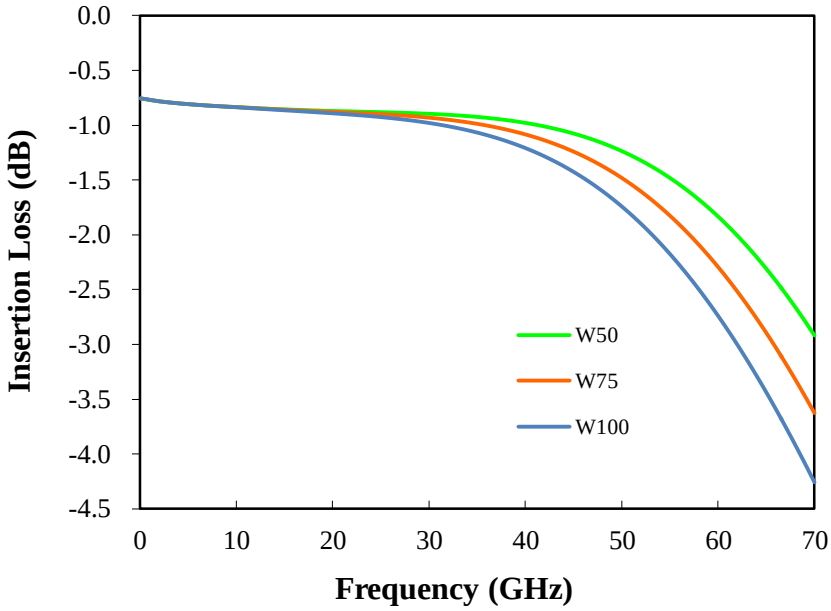


(b)

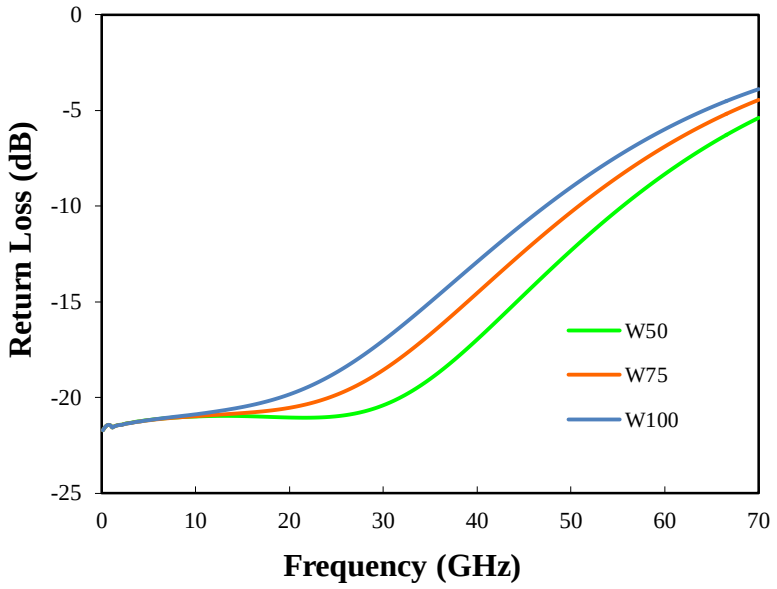


(c)

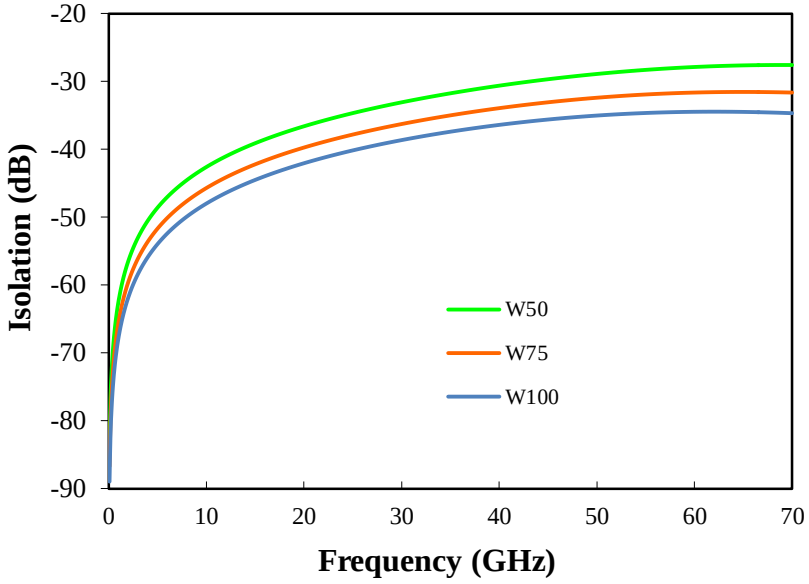
Figure 5-8 Simulated SPDT S-parameters as a function of series FET width, (a) IL, (b) RL and (c) ISO



(a)

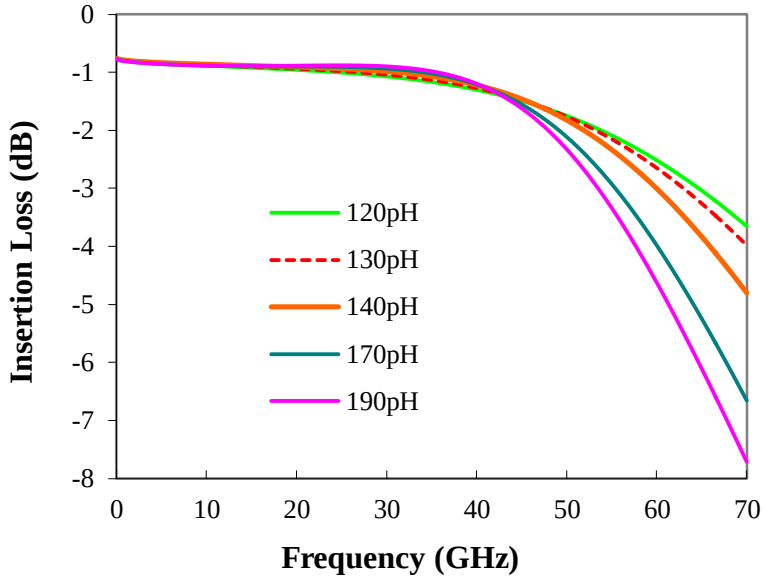


(b)

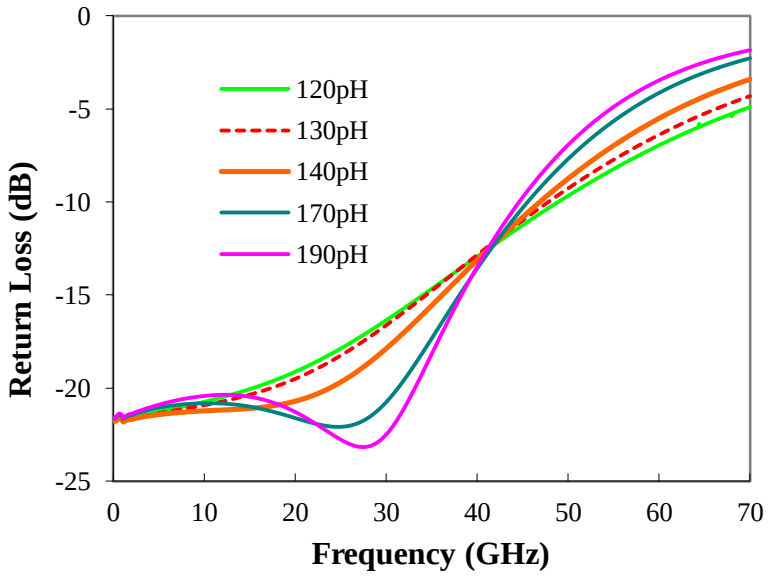


(c)

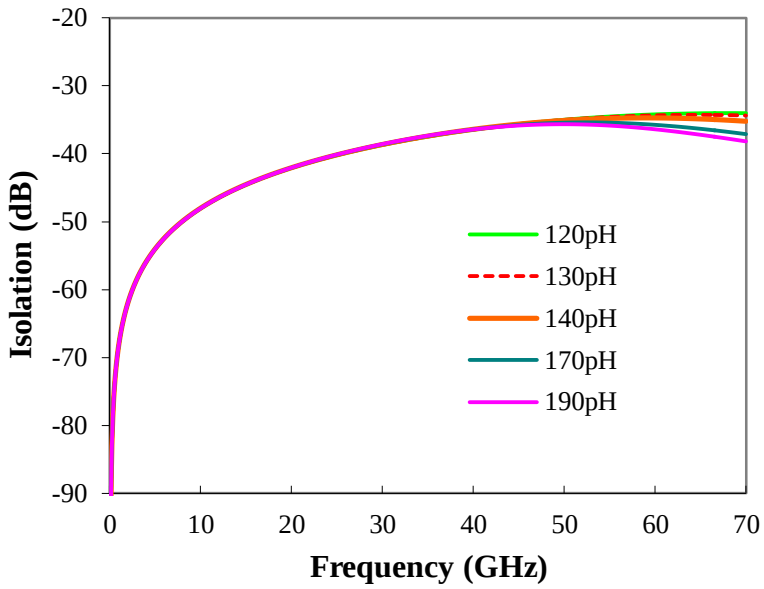
Figure 5-9 Simulated SPDT S-parameters as a function of shunt FET width, (a) IL, (b) RL and (c) ISO


0
-1
-2
-3
-4
-5
-6
-7
-8
Insertion Loss (dB)
120pH
130pH
140pH
170pH
190pH
0
10
20
30
40
50
60
70
Frequency (GHz)

(a)


0
-5
-10
-15
-20
-25
Return Loss (dB)
120pH
130pH
140pH
170pH
190pH
0
10
20
30
40
50
60
70
Frequency (GHz)

(b)



(c)

Figure 5-10 Simulated SPDT S-parameters as a function of matching inductor, (a) IL, (b) RL and (c) ISO

In this design, series transistors M_1 and M_3, with total transistor width of 75 µm (W = 5 µm, 15 fingers), shunt transistor M_2 and M_4, with total transistor width 100 µm (W = 5 µm, 20 fingers), series inductors L_1 = L_2 = 130 pH are designed based on simulation for the final layout of the SPDT switch to achieve low insertion loss while wide bandwidth. The inductors are simulated and optimized using commercial electromagnetic (EM) software HFSS, inductor with quality factor Q = 20 at 40 GHz is chosen to achieve the ultra wideband, while occupies small die area. The matching inductors are designed using 3 µm ultra thick metal (UTM), which is also the last Cu layer in the backend of line (BEOL). R_g = 50 kΩ poly resistors are used for this design.

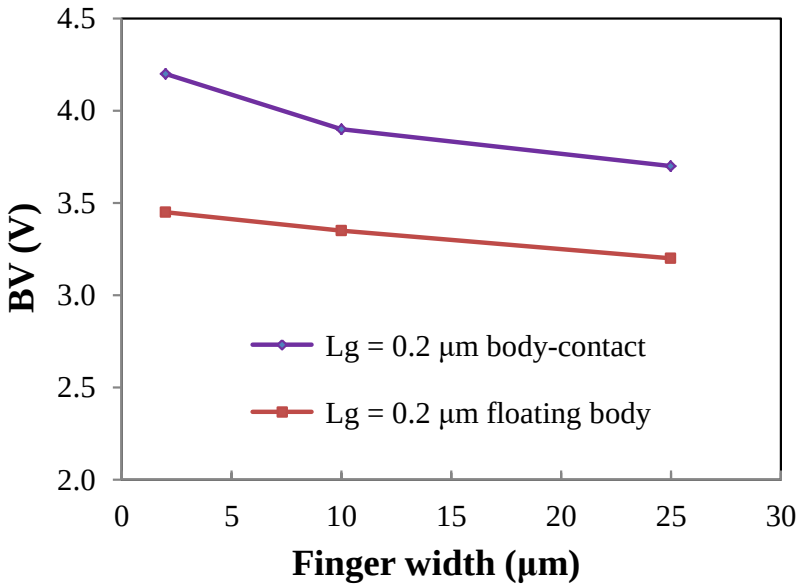


Figure 5-11 Switch NMOS finger width versus breakdown voltage

In this work, floating body NMOS is not adopted for switch design as its transistor breakdown voltage (BV) is about 0.7 V lower than that of body-tied NMOS for the same gate length, as shown in Figure 5-11. The measured data in Figure 5-11 also show when the transistor finger width is wider, transistor BV becomes lower, so a 5 µm finger width is finally selected for the used body-tied switch NMOS as a trade-off between transistor BV and total switch size. This final designed SPDT switch occupies a small chip area of only 0.214 x 0.19 mm^2.

Except for the evaluation of SMT impact on switch performance, switches designed with the same technology node, but with shorter transistor channel length (L_g) than nominal length (L_g = 0.2 µm), while keep same metal 1 to metal 1 (M1 to M1) space and source contact to drain contact space are also designed for comparison and investigation. What's more, a higher gate control bias, V_g = 3.3 V will be applied to designed switches to compare performance with switch under normal gate bias, which is V_g = 2.5 V.

5.5 Simulated and measured results of SPDT switch

The fabricated SPDT switch is shown in Figure 5-12. (take L_g = 0.2 μm non-SMT SPDT for example), GSG pads are connected to RF input port RF IN and two RF output ports RF OUT1 and RF OUT2 in the SPDT switch for RF testing, pad V_{c1} and V_{c2} are used for dc biasing of the series and shunt transistors.

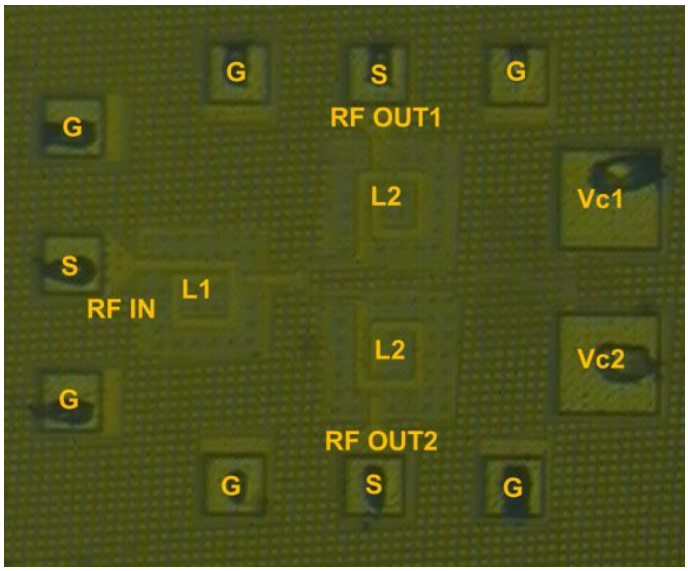
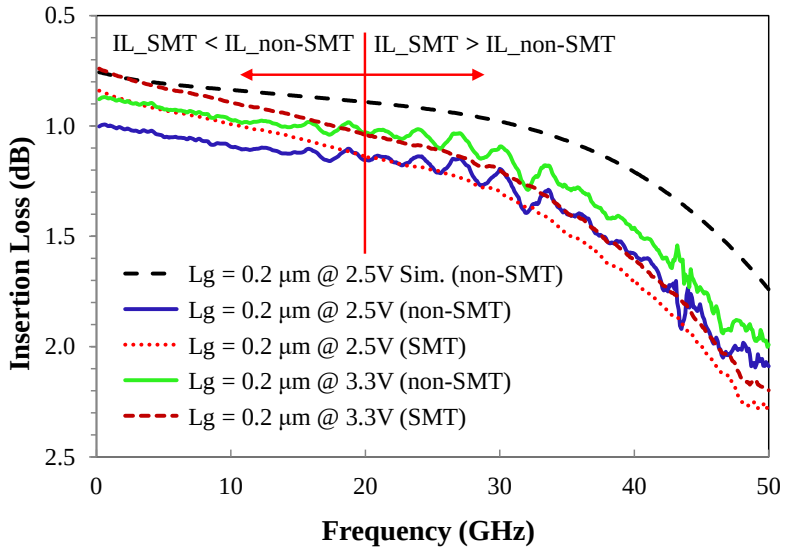


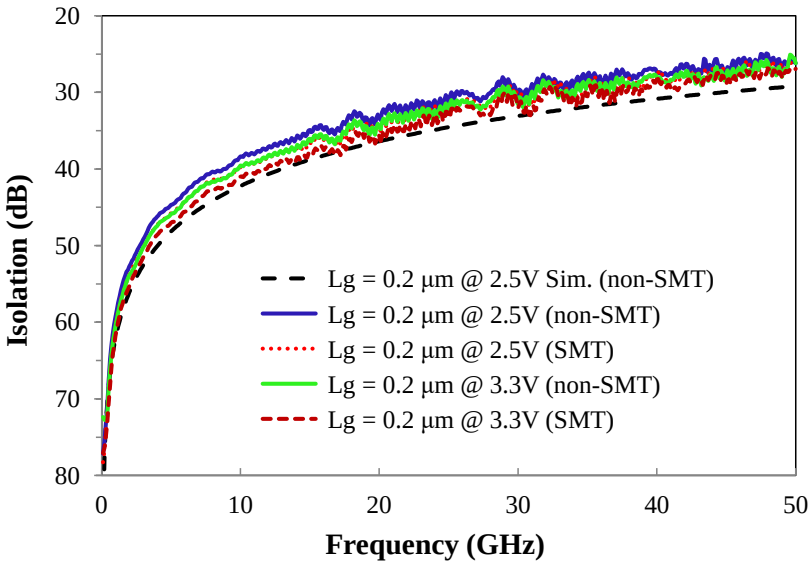
Figure 5-12 Photography of the designed SPDT switch

5.5.1 S-parameters

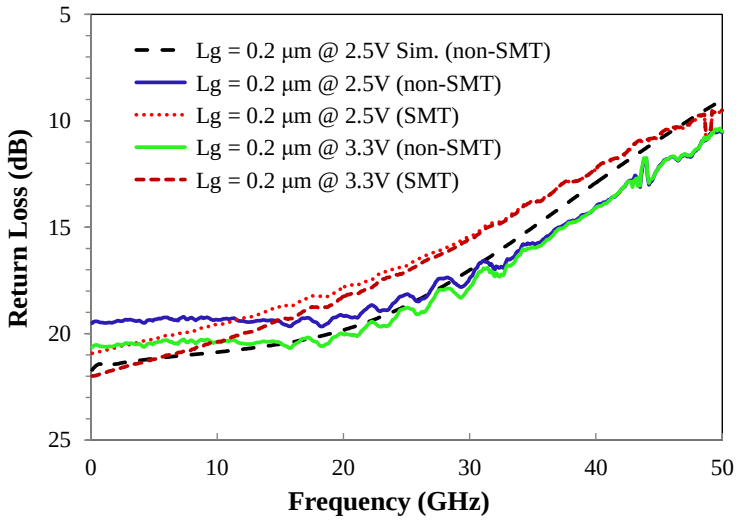
S-parameter measurements were done using the Agilent E8364C (10MHz-50GHz) PNA network analyzer and de-embedded using Short-Open-Load-Reciprocal (SOLR) calibration. Simulated and measured S-parameters of the SPDT switches designed with nominal NMOS (L_g = 0.2 μm) are shown in Figure 5-13. The non-SMT switch shows excellent wideband performance under 2.5 V biasing voltage, with low insertion of 1.1, 1.16 and 2.1 dB from dc to 10, 10 to 20 and 20 to 50 GHz, respectively. And measured isolations are better than 38, 33 and 25 dB from dc to 10 GHz, 10 to 20 and 20 to 50 GHz, respectively.


IL_SMT < IL_non-SMT
IL_SMT > IL_non-SMT
Insertion Loss (dB)
0.5
1.0
1.5
2.0
2.5
0
10
20
30
40
50
Frequency (GHz)
Lg = 0.2 μm @ 2.5V Sim. (non-SMT)
Lg = 0.2 μm @ 2.5V (non-SMT)
Lg = 0.2 μm @ 2.5V (SMT)
Lg = 0.2 μm @ 3.3V (non-SMT)
Lg = 0.2 μm @ 3.3V (SMT)

(a)


Isolation (dB)
20
30
40
50
60
70
80
0
10
20
30
40
50
Frequency (GHz)
Lg = 0.2 μm @ 2.5V Sim. (non-SMT)
Lg = 0.2 μm @ 2.5V (non-SMT)
Lg = 0.2 μm @ 2.5V (SMT)
Lg = 0.2 μm @ 3.3V (non-SMT)
Lg = 0.2 μm @ 3.3V (SMT)

(b)



(c)

Figure 5-13 Simulated and measured results of SPDT: (a) IL, (b) ISO and (c) RL of both SMT and non-SMT SPDT switches

Benefited from improved R_{on} induced by the SMT effect, the SMT SPDT switch results an even lower insertion loss when compared to non-SMT switch in the relatively lower frequency range from dc to around 20 GHz. As also shown in Figure 5-13, measured insertion losses of the SMT SPDT switch under 2.5 V gate bias are less than 1, 1.15 and 2.3 dB from dc to 10, 10 to 20 and 20 to 50 GHz, respectively. SMT switch shows 0.15 dB lower insertion loss at 1 GHz and 0.1 dB lower at 10 GHz when compared to non-SMT switch. When frequency is higher than 20 GHz, insertion loss of SMT switches become slightly higher than non-SMT switch, show around 0.2 dB higher insertion loss at 50 GHz. The slightly higher insertion loss of SMT switches in high frequency range could be resulted from the slightly higher C_{off} of SMT switch. As expressed in equitation (4-10), insertion loss for SMT and non-SMT switch can be expressed as below:

$$IL_{SMT} = 10\log\{\left(1 + \frac{R_{on\_SMT}}{2Z_0}\right)^2 + [\frac{2\pi f C_{off\_SMT}(R_{on\_SMT} + Z_0)^2}{2}]\} \quad (5\text{-}3)$$

$$IL_{non\_SMT} = 10\log\{\left(1 + \frac{R_{on\_non-SMT}}{2Z_0}\right)^2 + [\frac{2\pi f C_{off\_non-SMT}(R_{on\_non-SMT} + Z_0)^2}{2}]\} \quad (5\text{-}4)$$

When input signal frequency (f in Equation (5-3) and (5-4)) is very low, the insertion loss is dominated by R_{on} of the series branch (first part in Equation (5-3) and (5-4)), and the contribution from the shunt branch (C_{off} related) can be ignored, as summarized in Table 5-1, since

$$R_{on\_SMT} < R_{on\_non-SMT} \quad (5\text{-}5)$$

So in low frequency range,

$$IL_{SMT} < IL_{non-SMT} \quad (5\text{-}6)$$

As frequency of the input signal increases, the insertion loss from the C_{off} is also increasing, when f is high enough, the total insertion loss from SMT series-shunt branch is comparable to that of non-SMT series-shunt branch (for this SPDT switch, f is around 20 GHz as illustrated in Figure 5-13(a)). When f is further increased to beyond 20 GHz, the total insertion loss of SMT switch will be higher than non-SMT switch.

Measured isolation of SMT switch is around 0.5 to 1 dB higher than non-SMT switch in the whole measured frequency range. Based on Equation (4-13), the isolation is determined by product of R_{on}*Co_{ff}, as summarized in Table 5-1, R_{on}*Co_{ff} product of SMT

transistor is lower than non-SMT transistor, although C_{off} of SMT transistor is slightly higher than that of non-SMT transistor, the isolation of SMT switch is still slighter better than non-SMT switch.

Measured return loss of both SMT and non-SMT switch are less than 15 dB and 10 dB from DC to 30 GHz and 30 to 50 GHz, respectively.

The S-parameters measured at a higher gate bias voltage (V_g = 3.3 V) are also presented in Figure 5-13 (a) to (c). Compared to the nominal bias voltage (V_g = 2.5 V), 3.3 V bias results about 0.1 dB lower insertion loss, 1 dB higher isolation and slightly better return loss. Improvement of the switch performance at 3.3 V bias is resulted from increased V_{GS} in Equation (5-1), hence decreased $R_{on.}$ Measured insertion losses of the SMT SPDT switch under 3.3 V biasing are 0.9, 1.04 and 2.2 dB from DC to 10, 10 to 20 and 20 to 50 GHz, respectively.

SPDT switches with shorter channel length (L_g = 0.11, 0.13 and 0.15 μm) are also designed to study the channel length impact on switch performance in the same technology node. Measured insertion loss and isolation (with Vg = 3.3 V) of SMT SPDT switches with variable gate lengths are illustrated in Figure 5-14. Switch with shorter L_g shows lower insertion loss, measured insertion loss of L_g = 0.11 μm SMT switch are less than 0.65, 0.8 and 2.15 dB from DC to 10, 10 to 20, and 20 to 50 GHz, respectively. This is expectable, as transistor R_{on} decreases with decreasing channel length.

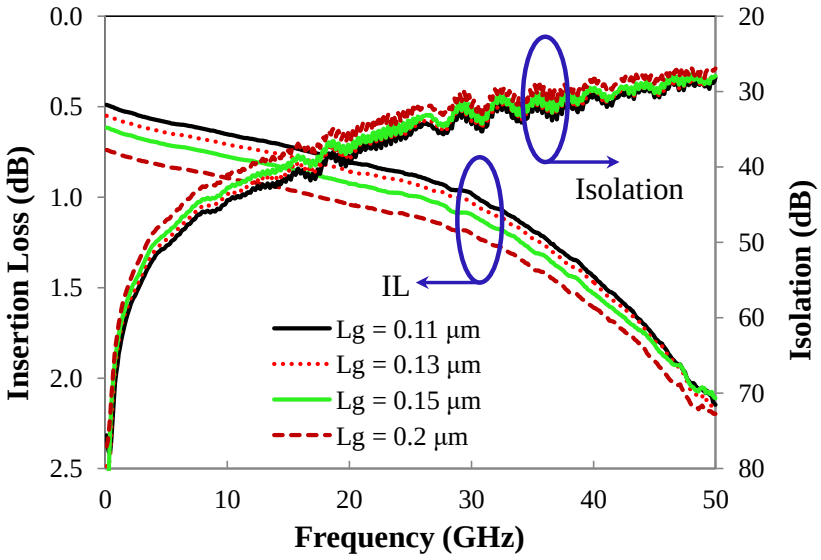


Figure 5-14 Measured insertion loss and isolation of SMT SPDT switches versus channel length.

Usually as transistor gate length is scaling down, R_{on} will be lower, but C_{off} will be increased, so isolation will be getting worse. What interesting for this design is switch with shorter L_g shows higher isolation, measured isolation of the shortest channel length L_g = 0.11 μm switch are higher than 44, 38 and 28 dB from dc to 10, 10 to 20 and 20 to 50 GHz, respectively, which is about 1.5 to 3 dB higher than L_g = 0.20 μm switch. This can be explained based on the C_{off} model in Figure 5-5 and C_{off} physical dimension model shown in Figure 5-15.

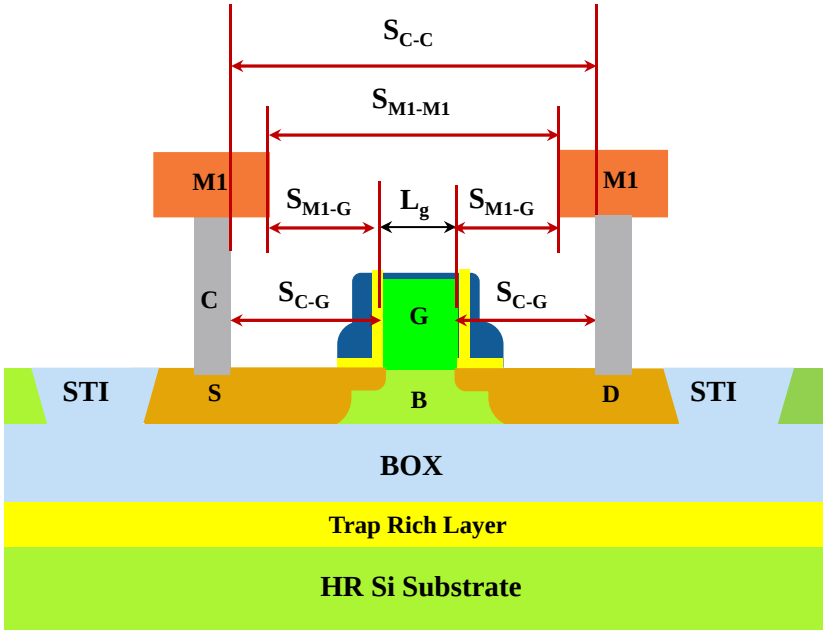


Figure 5-15 C_{off} physical dimension model of the SOI switch NMOS

$$C_{off} = \underbrace{\frac{C_{SB}\cdot C_{DB}}{C_{SB}+C_{DB}} + \frac{C_{GSO}\cdot C_{GDO}}{C_{GSO}+C_{GDO}} + \frac{C_{SD-Sub}}{2}}_{55\%} + \underbrace{C_{M1-M1}}_{22\%} + \underbrace{\frac{C_{M1-G}}{2} + \frac{C_{C-G}}{2}}_{23\%}$$

Figure 5-16 Simulated C_{off} components comparison

Simulation result from a 0.2 μm structure shows about 55% of the total C_{off} is from device capacitance, and the other 45% is from wiring capacitance, including 22% from M1 to M1 capacitance $C_{M1\text{-}M1}$, 23% from M1 and contact to gate capacitance $C_{M1\text{-}G}$ and $C_{C\text{-}G}$, as indicated in Figure 5-16. So wiring capacitance plays a significant role in total C_{off}. For the transistor gate length scaling in Table 5-1, when gate length L_g shortened from 0.2 μm to 0.13 μm, the source and drain contact to gate space $S_{C\text{-}G}$ (as shown in Figure 5-15) and M1 to gate space $S_{M1\text{-}G}$ keep not changed, so M1 to M1 space $S_{M1\text{-}M1}$ and contact to contact space $S_{C\text{-}C}$ will be decreased. Thus contact to gate capacitance $C_{C\text{-}G}$ and M1 to gate capacitance $C_{M1\text{-}G}$ are not changed, but M1 to M1 capacitance $C_{M1\text{-}M1}$ will be higher, hence total wiring capacitance

is higher for 0.13 μm when compared to 0.2 μm, and source drain junction capacitance of 0.13 μm is also higher than 0.2 μm because of shorter effective gate length. As a result, total C_{off} of 0.13 μm structure is higher than 0.2 μm in Table 5-1. In this design, when shortening poly length, we keep M1 to M1 space $S_{M1\text{-}M1}$ and contact to contact space $S_{C\text{-}C}$ not changed. So $C_{M1\text{-}M1}$ is not changed, while $C_{M1\text{-}G}$ and $C_{C\text{-}G}$ will be decreased since M1 to gate space $S_{M1\text{-}G}$ and contact to gate space $S_{C\text{-}G}$ are increased, thus the total wiring capacitance is reduced. The measured isolation result in Figure 5-14 shows isolation is also decreased as channel length reduced, this indicates wiring capacitance dominates the total C_{off} change as compared with junction capacitance change, this explains why isolation of L_g = 0.11 μm switch is higher than that of L_g = 0.20 μm switch. So in this work, by shortening the poly length, we achieved not only lower switch insertion loss, but also higher switch isolation.

5.5.2 Power handling and linearity

Power handling and linearity of switches have been studied before [71]-[74]. Measurements of the input 1-dB compression point (P1dB) for designed switches were performed using R&S SMF100A Signal Generator (100K - 43.5 GHz) and NRP-Z57 Power Meter (DC–67 GHz). The P1dB measurements were carried out from 1 GHz to 25 GHz, due to input power limitation of the test facilities. Figure 5-17 shows measured P1dB versus frequency (measured at 1 GHz, 5 GHz, 15GHz and 25 GHz) for designed SPDT switches. As can be seen, switches with longer gate length result higher P1dB at the same measurement frequency. Take 25 GHz as an example case, the measured P1dB for SMT SPDT switches are 10.7 dBm for L_g = 0.11 μm, 12.6 dBm for L_g = 0.13 μm, 13.4 dBm for L_g = 0.15 μm and 14 dBm for L_g = 0.2 μm, respectively. Measured P1dB for the SPDT switch with shortest

channel length, L_g = 0.11 µm are 10.9, 10.9, 11.3 and 10.7 dBm at 1, 5, 15 and 25 GHz, respectively, this indicates L_g = 0.11 or 0.13 µm NMOS is also a good candidate for ultra-wideband RF switch application without significant performance degradation. The result also shows P1dB for SMT and non-SMT switches with same gate lengths are comparable, and P1dB under 3.3 V is slightly higher than P1dB measured at 2.5 V bias.

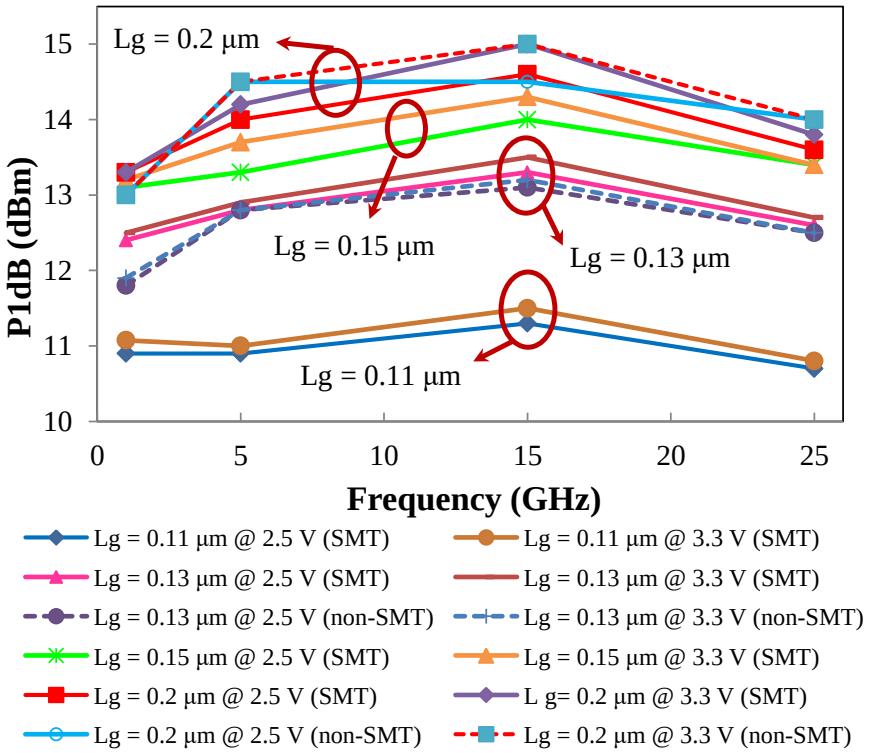


Figure 5-17 Measured P1dB of SPDT switches

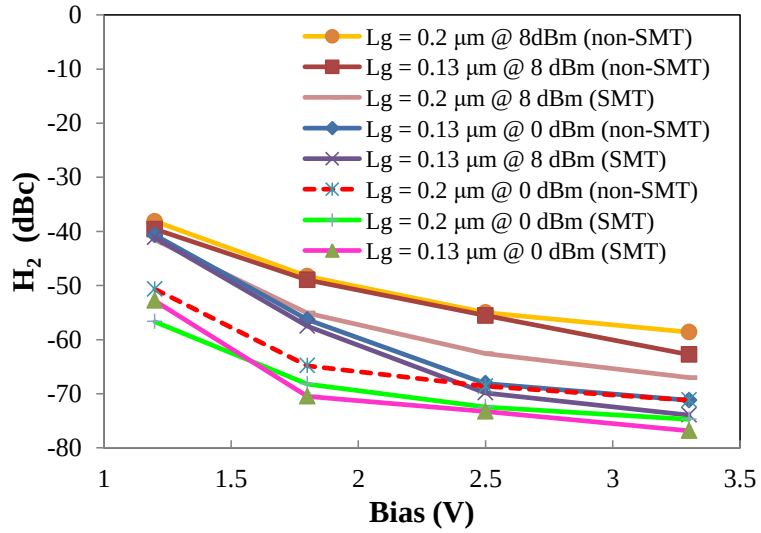
Third-order intermodulation products of fabricated switches were measured with Agilent E8267D PSG Vector Signal Generator (100 kHz to 20 GHz, measured at two-tone mode) at 5 and 10 GHz, respectively, and spaced by 10 MHz. R&S ZVA67 (10 MHz – 67 GHz) is used as spectrum analyzer. Extrapolated input third-order interception points (IIP3) of both SMT and non-SMT SPDT switches (L_g = 0.13 µm and L_g = 0.2 µm, 2.5 V bias) are summarized in Table 5-3. IIP3 of SMT SPDT is slightly higher than non-SMT SPDT for the same gate length at the same measurement frequency. Typical IIP3 of L_g = 0.2 µm switches

are in the range of 25 to 28 dBm at measured frequencies, and typical IIP3 for L_g = 0.13 μm switches are in the range of 23 to 26 dBm.

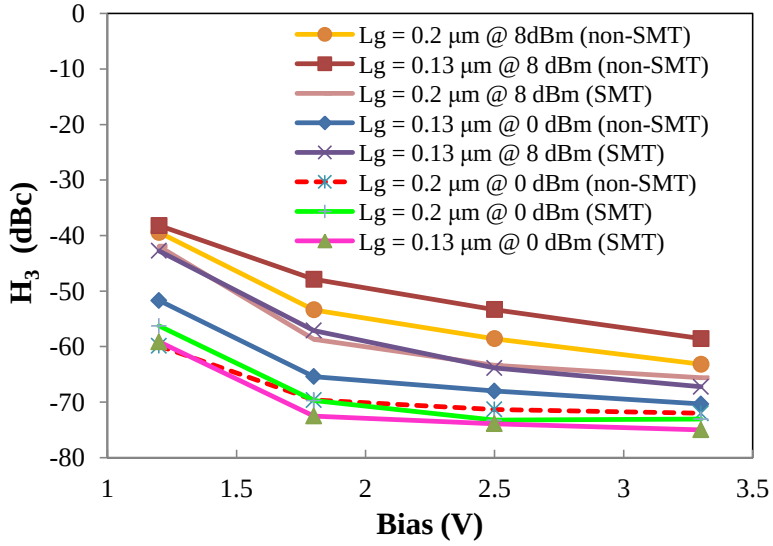
Table 5-2 Extrapolated IIP3 of SPDT Switches

Frequency (GHz)	non-SMT (dBm)		SMT (dBm)	
	0.13 μm	0.2 μm	0.13 μm	0.2 μm
5	23.8	25.5	24.1	26.2
10	24.9	27.4	25.5	27.8

To further investigate higher order nonlinearities in the designed switches, the 2nd harmonic distortion (H_2) and 3rd harmonic distortion (H_3) were measured using R&S SMF100A Signal Generator (100K - 43.5 GHz) and R&S ZVA67 under different gate bias (1.2, 1.8, 2.5 and 3.3 V) and different input power (0 and 8 dBm) at the fundamental frequency of 5 GHz, as shown in Figure 5-18. In general, the measured 2nd and 3rd harmonic distortion levels of SMT switches are lower than non-SMT switches under the same bias condition and same input power. At 0 dBm input power under 2.5 V bias, the measured H_2 are -72.4 and -68.6 dBc (calculated delta between measured H_2 and H_1 output power), measured H_3 are -73.3 and -71.2 dBc (calculated delta between measured H_3 and H_1 output power) for 0.2 μm SMT switch and 0.2 μm non-SMT switch, respectively. L_g = 0.13 μm switches exhibit slightly lower harmonic distortion than L_g = 0.2 μm switches. What's more, the measured harmonic distortions for each switch become lower when the bias voltage increases from 1.2 V to 3.3 V.



(a)



(b)

Figure 5-18 Measured 2nd and 3rd harmonic distortion of SPDT switches: (a) 2nd harmonic H_2, (b) 3rd harmonic H_3

5.5.3 Switch speed

Switching speed of fabricated switches were measured using R&S SMF100A Signal Generator (100K-43.5GHz), Agilent 33600A Waveform Generator, and LeCroy 8600A Oscilloscope (Max. 6GHz). Simulated rise time (RF output to rise from 10% to 90% of the final value) and fall time (RF output to drop from 90% to 10% of the initial value) of the SPDT are 10 ns and 8 ns, respectively, and less than 12 ns and 10 ns for SP4T. Measured

rise and fall time for SPDT at 5 GHz are both around 8 ns, as shown in Figure 5-19 and Figure 5-20, which agree well with simulation.

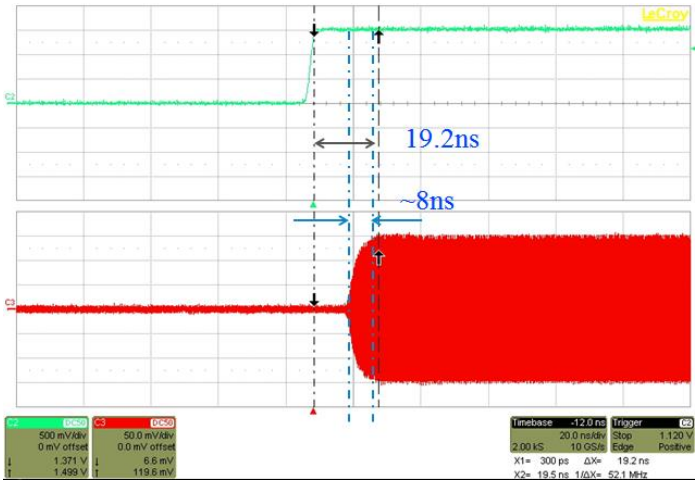


Figure 5-19 Measured rise time of the SPDT switch @5 GHz

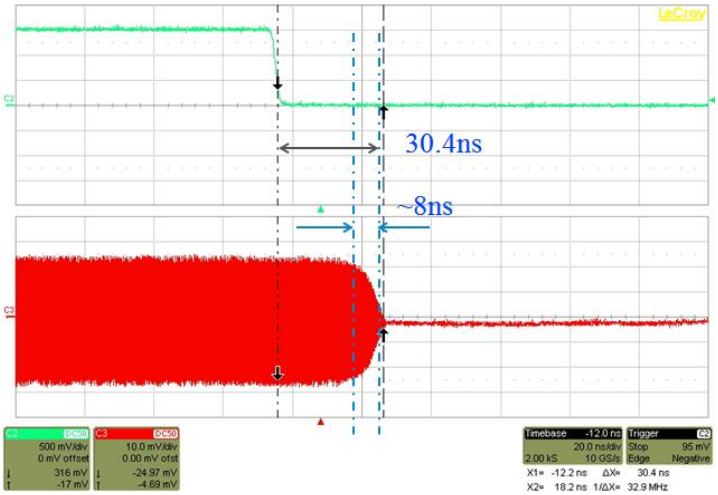


Figure 5-20 Measured fall time of the SPDT switch @5 GHz

5.6 Summary and comparison

A systematic study of the high resistivity trap rich SOI process for the low loss ultra wideband SPDT switch is carried out in this Chapter, SMT process impact on wideband RF switch is studied for the first time. A comparison with the state of the arts is given in Table 5-3, the proposed SPDT switch achieves the best insertion loss and excellent isolation for the switches designed on CMOS or SOI CMOS technology. These excellent performances are

achieved by optimizing the size of both series and shunt transistors, elaborate design of the matching inductors, improved interconnecting line layout to decrease the parasitic coupling. Further improvement of the switch performance is achieved by implementing SMT. It is found SMT can improve both insertion loss and isolation in a certain wide frequency range. Moreover, shortening the channel length and applying higher gate bias can also help improve switch performance. A switch C_{off} model of the used SOI transistor is also proposed, this model indicates all the factors which contribute to the total off capacitance, based on this model, switch layout can be optimized to further reduce total $C_{off.}$ Proposed SPDT switches consume compact die area of only 0.214 x 0.19 mm^2. The fabricated SPDT switches show outstanding performance to be used for fully integrated and cost-effective ultra-wideband applications.

Table 5-3 Comparison of Wideband Switches

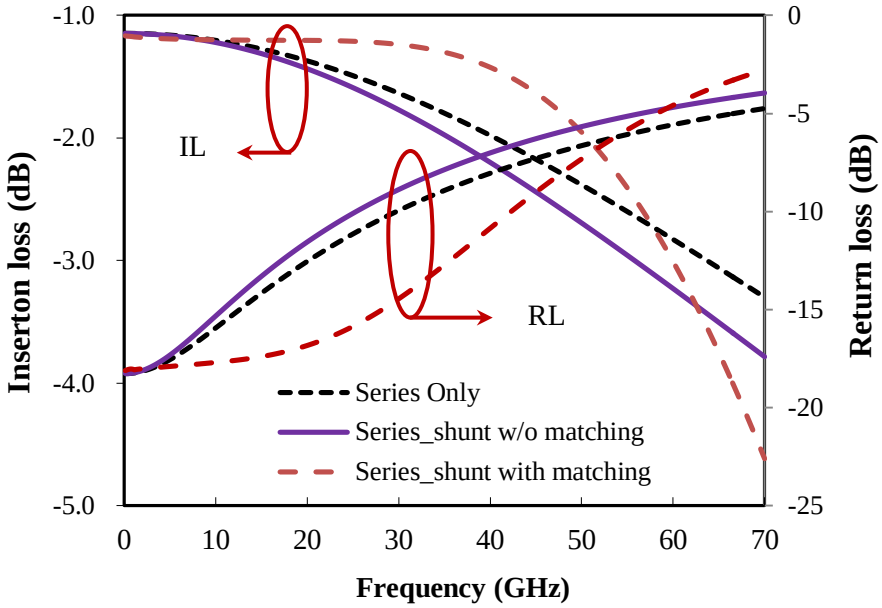
Ref.	Tech.	Type	BW	IL	ISO	Input P1dB	Chip Size	Topology
			(GHz)	(dB)	(dB)	(dBm)	(mm^2)	
[11]	0.13-µm triple-well CMOS	SPDT	2.4-20	0.9-2	43-21	30	0.17	Symmetric series-shunt, double-well body-floating
[34]	0.13-µm CMOS	SP4T	dc-70	< 2.7 at 10 GHz < 3.0 at 35 GHz	30	>9	0.24 x 0.23	series-shunt, with matching networks
[35]	45-nm SOI CMOS	SPDT	dc-60	1.7 at 45 GHz	>25 at 50 GHz	7.1	0.18×0.22	Series-shunt
[45]	0.35-µm SiGe	SPDT	42-70	< 1.25	>18	1	0.85x0.92	Differential SPDT
[46]	RF-MEMS	SP4T	dc-70	<1	>15	NA	NA	distributed transmission line
[49]	0.1-µm HEMT	SPDT	15-80	<3.6	>25	NA	1.5 x 1.5	traveling-wave concept
[50]	0.18-µm SiGe BiCMOS	SPDT	dc-30	1.5 – 3.3	>20	23	0.025	series-shunt, with matching network
[51]	0.18-µm SOI	SPDT	dc-40	<5	>17	15	0.28 x 0.09	series-shunt, with matching network
[52]	90-nm CMOS	SPDT	dc-60	<3	>48	17	0.68 x 0.87	traveling-wave concept
[53]	0.13-µm CMOS	SP4T	dc-30	<2.7 < 3.0 at 35 GHz	>26	9	0.25 x 0.18	series-shunt, with matching network
This work	**0.13-µm SOI**	**SPDT**	**dc-50**	**< 2.1 at 50 GHz** **< 1.7 at 45 GHz** **< 1.0 at 30 GHz**	**> 27 at 50 GHz**	**> 10.5**	**0.214 x 0.19**	**series-shunt, with matching network**

Chapter 6

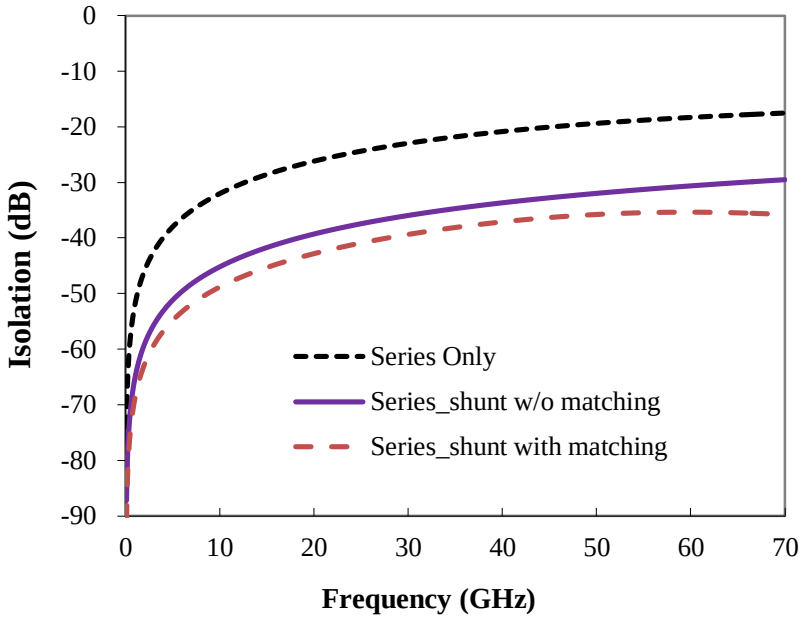
Ultra wideband SP4T switch design

6.1 SP4T topology

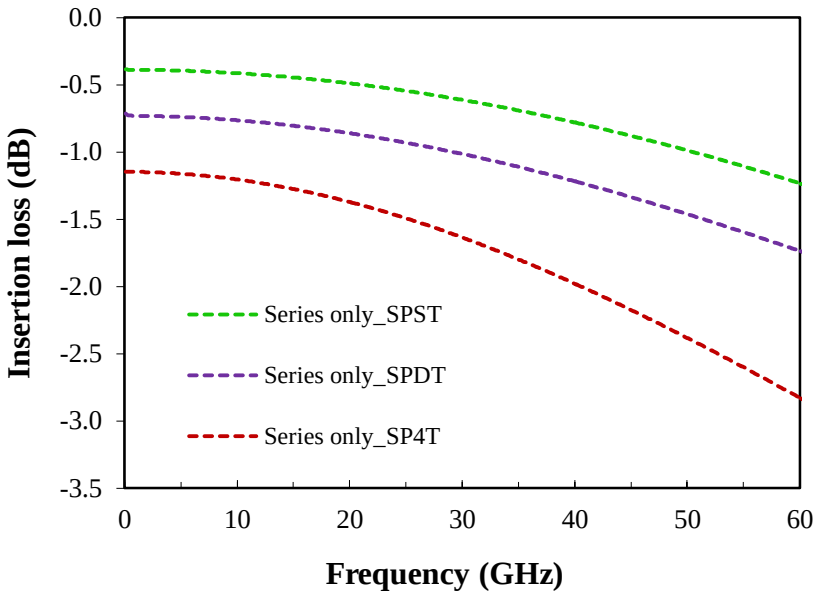
Similar to SPST and SPDT switches, S-parameter of different configurations of SP4T switch, include series only, series-shunt and series-shunt with input and output matching network is simulated as shown in Figure 6-1. Again, the series only topology showed the worst isolation response, shunt transistors are needed to improve the isolation, and matching networks are also needed to decrease the return loss and widen the operation band width. What's more, when compared to SPDT and SPST switches, the insertion loss of the series only SP4T switch increases much faster as shown in Figure 6-1 (c), this is because the increased switch throws provide more RF signal leakage paths from parasitic capacitance of off-state branches, which translates into insertion loss for the on-state arm. By implementing the *L-C-L* matching network, the insertion loss can be decreased much within a wide frequency band, thus can significantly widen the application band width.


-1.0
-2.0
-3.0
-4.0
-5.0
0
-5
-10
-15
-20
-25
Inserton loss (dB)
Return loss (dB)
IL
RL
Series Only
Series_shunt w/o matching
Series_shunt with matching
0
10
20
30
40
50
60
70
Frequency (GHz)

(a)


0
-10
-20
-30
-40
-50
-60
-70
-80
-90
Isolation (dB)
Series Only
Series_shunt w/o matching
Series_shunt with matching
0
10
20
30
40
50
60
70
Frequency (GHz)

(b)



(c)

Figure 6-1 Simulated S-parameters of different SP4T topologies, (a) IL and RL, (b) ISO, (c) IL comparison

The final proposed configuration of SP4T switch is shown in Figure 6-2, which is constructed by four symmetric SPST switches. Each SPST branch is constructed by a series transistor (M_1, M_3, M_5 and M_7) and shunt transistor (M_2, M_4, M_6 and M_8). L_1 is used as the matching inductor for the RF in port, and L_2 is used for all the other ports. When RF signal need to be travelled between Port 1 and Port 2, V_{c1} is high (=2.5V), V_{c2}, V_{c3} and V_{c4} are low (=0 V), so M_1, M_4, M_6 and $M_8$are turned on, while M_2, M_3, M_5 and M_7 are turned off. Similar case when RF signals need to be travelled between Port 1 and other ports. Large gate resistance R_g is used for all the series and shunt transistors to minimize RF signal leakage through the gate and to prevent gate oxide breakdown.

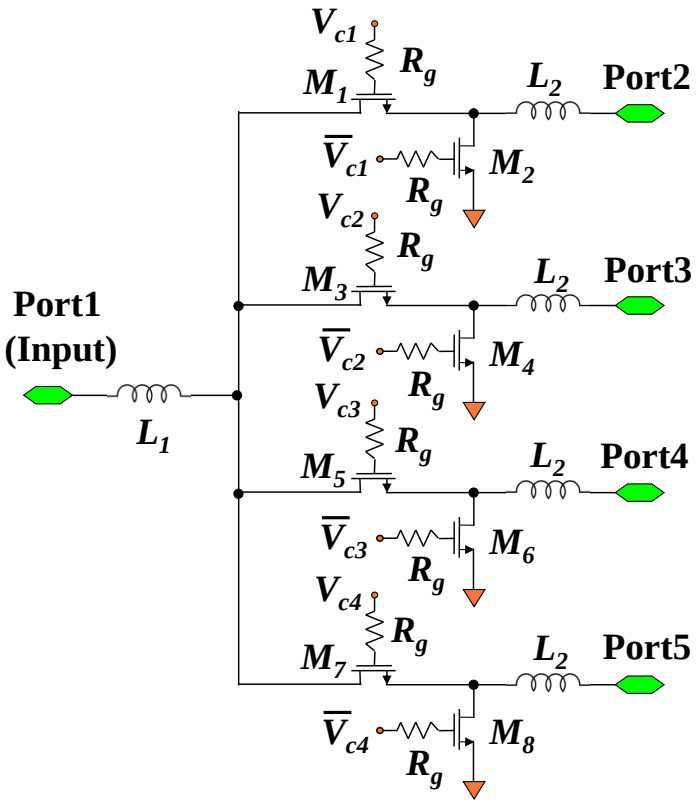
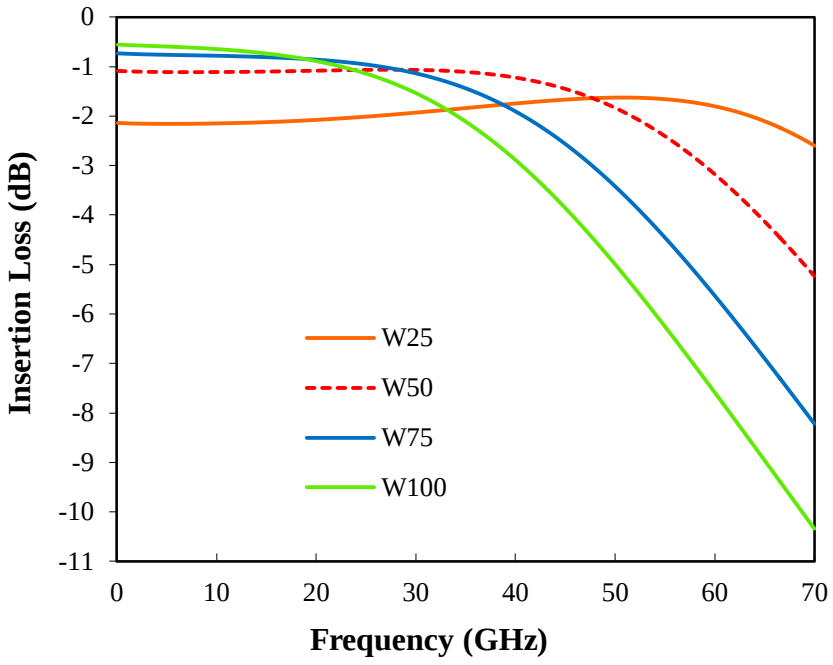


Figure 6-2 Schematic of the SP4T switch

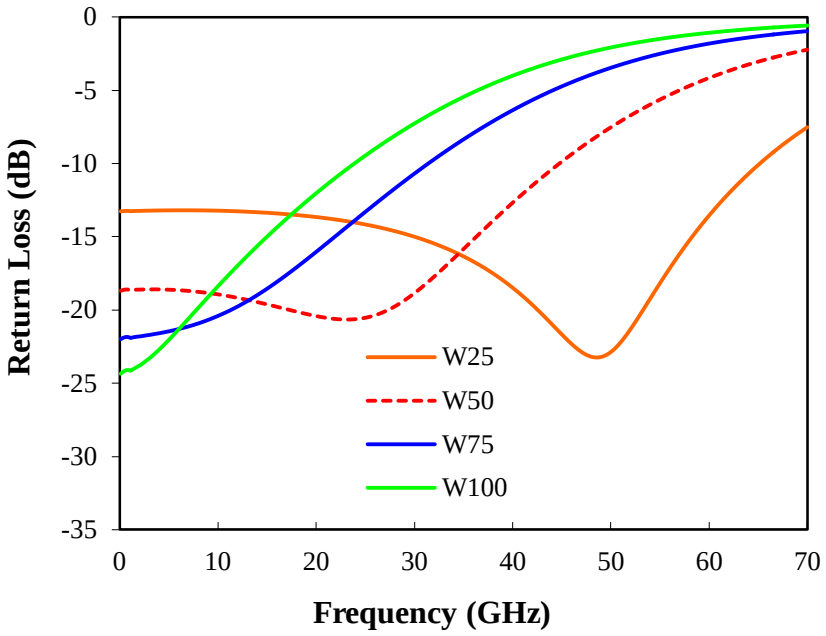
6.2 SP4T switch simulation

The impacts of series and shunt transistor width on SP4T switch performance are simulated and shown in Figure 6-3 and Figure 6-4, respectively.

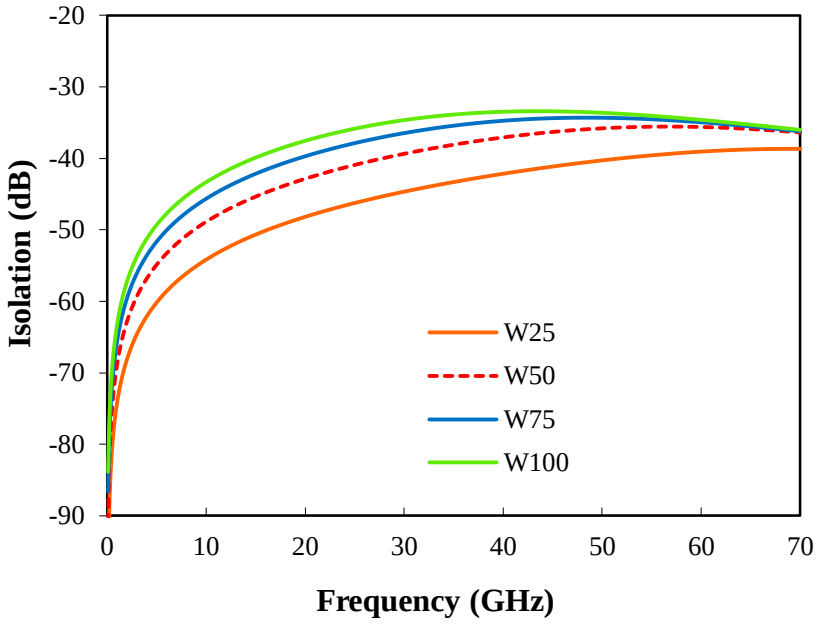
Based on simulation, series transistor M_1, M_3, M_5 and M_7, with optimized size of total width 50 μm (W = 5 μm, 10 fingers), and shunt transistor M_2, M_4, M_6 and M_8, with optimized size of total width of 75 μm (W = 5 μm, 15 fingers), and matching inductors L_1 = L_2 = 140 pH are designed for SP4T switch, the SP4T switch occupies a small chip area of 0.36 × 0.19 mm^2.


0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
Insertion Loss (dB)
W25
W50
W75
W100
0
10
20
30
40
50
60
70
Frequency (GHz)

(a)

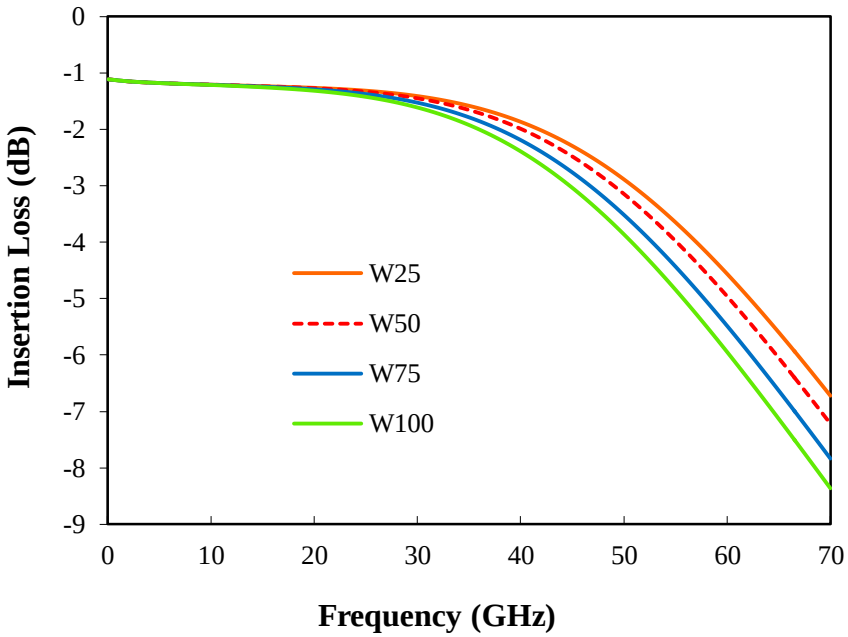

0
-5
-10
-15
-20
-25
-30
-35
Return Loss (dB)
W25
W50
W75
W100
0
10
20
30
40
50
60
70
Frequency (GHz)

(b)

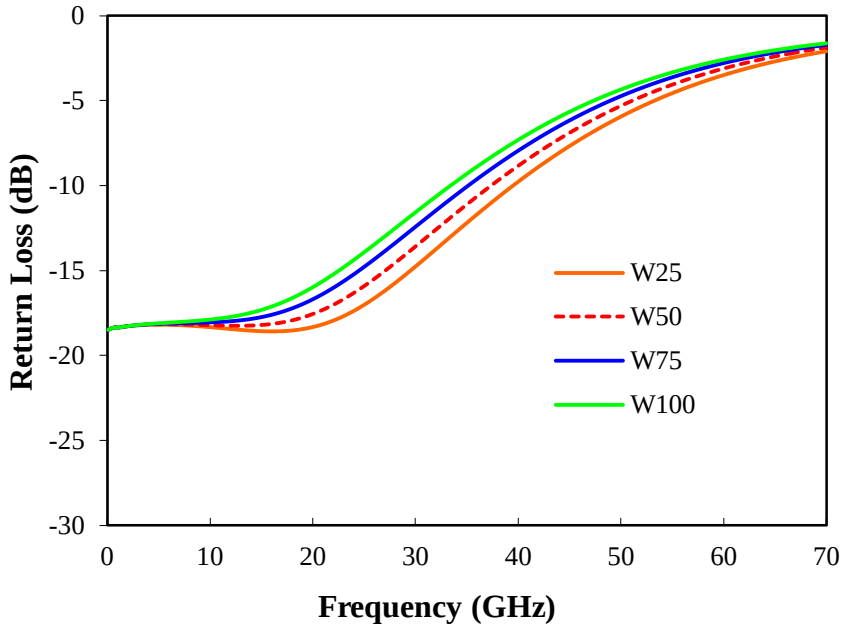


(c)

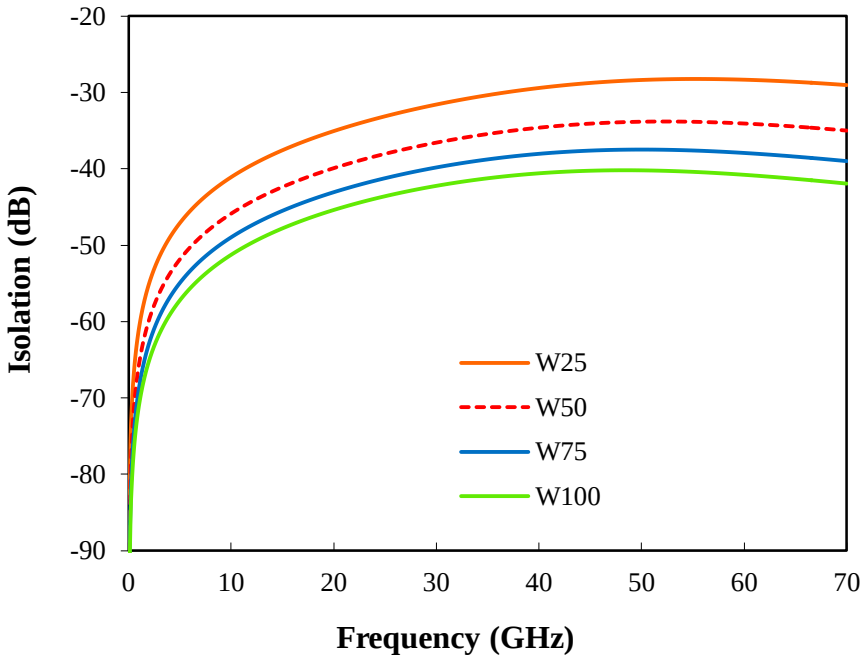
Figure 6-3 Simulated SP4T IL, ISO and RL as a function of series FET width, a) IL, b) RL, c) ISO



(a)



(b)



(c)

Figure 6-4 Simulated SP4T S-parameters as a function of shunt FET width, (a) IL, (b) RL and (c) ISO

6.3 Measured results of SP4T switch

Photography of fabricated SP4T switch is shown in Figure 6-5 (take L_g = 0.2 μm SMT SP4T for example), GSG pads are connected to OUT1 and OUT2 in the SP4T switch for RF testing, V_{c1} and V_{c2} pads are used for dc biasing of the series and shunt transistors. RF OUT3 and OUT4 ports are internally terminated with 50 Ω on-chip poly resistors to avoid two additional RF pads, since they are identical to the OUT1 and OUT2 ports, because of the symmetrical layout, the GND pad is used to ground OUT3 and OUT4.

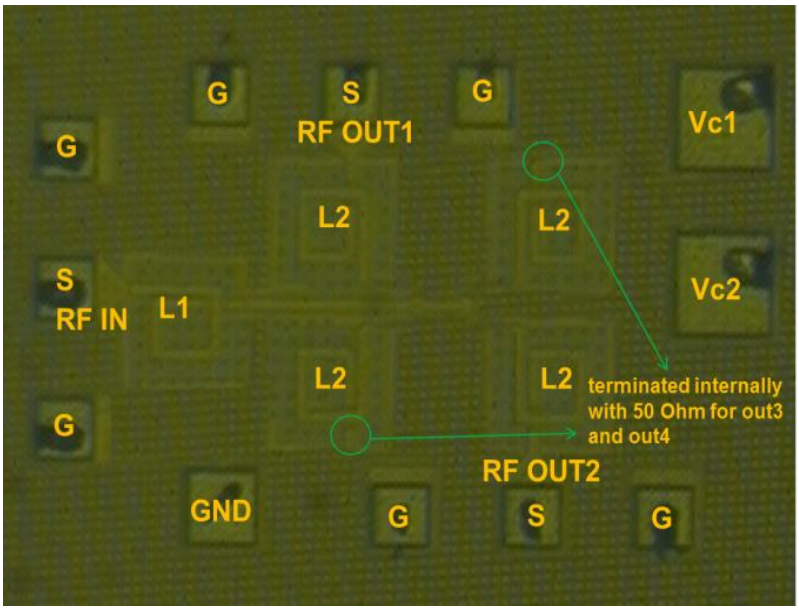


Figure 6-5 Photography of the designed SMT SP4T Switch

6.3.1 S-parameters

Simulated and measured s-parameters of designed SP4T switches with nominal channel length (L_g = 0.2 μm) are shown in Figure 6-6. Measurements were done under both 2.5V and 3.3V gate bias, and include both SMT and non-SMT SP4T switches. As summarized in Table III, for 2.5 V bias, the non-SMT switch results low insertion losses of less than 1.52 dB, 1.69 dB, 2.8 dB and 4.43 dB from dc to 1 GHz, 1 GHz to 10 GHz, 10GHz to 35 GHz and 35 GHz to 50 GHz, respectively. While SMT switch results even lower

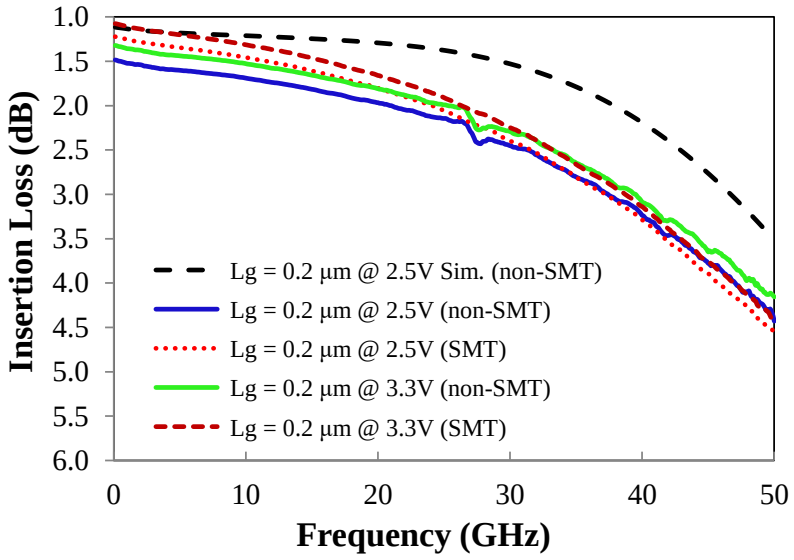
insertion loss of less than 1.25 dB and 1.46 dB from dc to 1 GHz, 1GHz to 10 GHz, respectively, and shows same insertion loss as non-SMT switch at 35 GHz, but slightly higher insert loss when frequency is higher than 35 GHz. So for SP4T switch, similar to SPDT switches, SMT process gives a lower insertion at a relatively lower frequency region because of the lower transistor Ron under SMT process. Also similar to SPDT switch, 3.3 V gate bias results about 0.15 dB to 0.2 dB lower insertion loss when compared to 2.5 V gate bias for both SMT and non-SMT switches over the whole frequency range from dc to 50 GHz.

Table 6-1 Insertion Loss (dB) Comparison (SMT vs. NON-SMT)

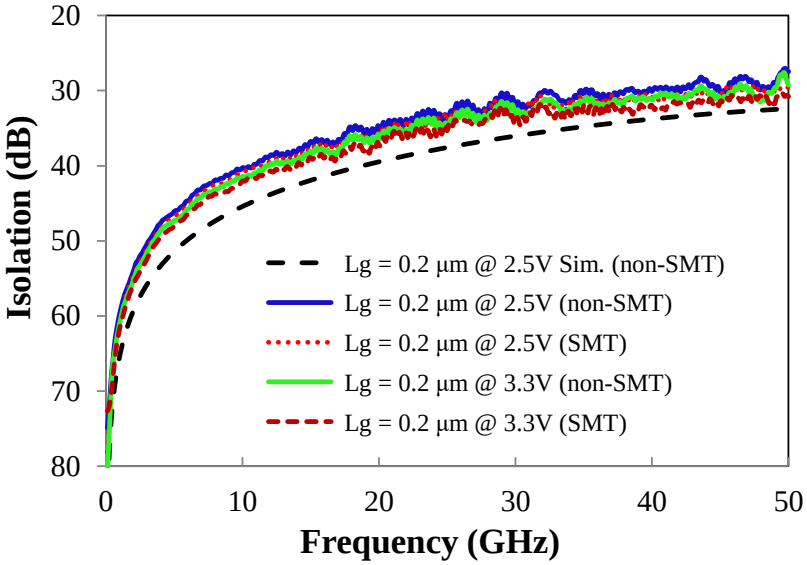
Frequency	non-SMT		SMT	
	2.5V	3.3V	2.5V	3.3V
1 GHz	1.52	1.36	1.25	1.10
10 GHz	1.69	1.53	1.46	1.31
35 GHz	2.80	2.66	2.80	2.65
50 GHz	4.43	4.16	4.54	4.45

Measured isolations for SMT and non-SMT switches are better than 30 dB and 28 dB from dc to 35 GHz and 35 GHz to 50 GHz, respectively. Measured return losses for both SMT and non-SMT switches are better than 10 dB from dc to 35 GHz under both 2.5 and 3.3 V bias.

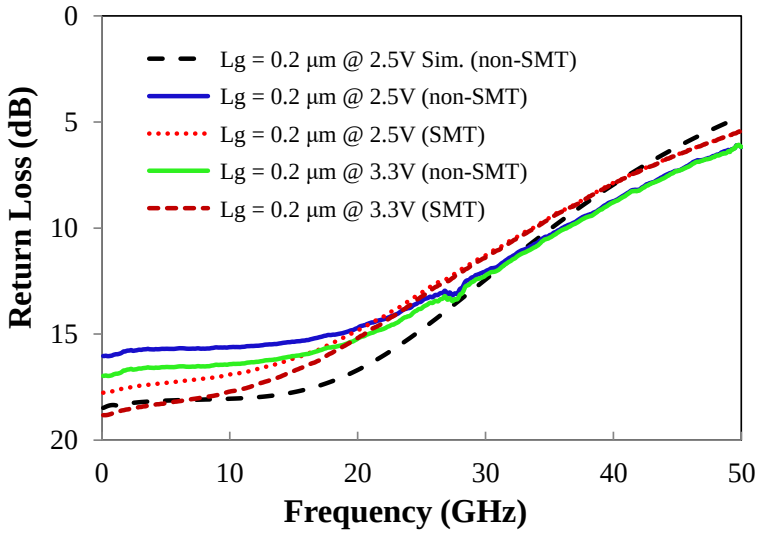
To the best of authors' knowledge, this is the first ultra wideband SP4T switch designed in SOI process and also the first reported SP4T switch performance with SMT process implemented.


Insertion Loss (dB)
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
0
10
20
30
40
50
Frequency (GHz)
Lg = 0.2 µm @ 2.5V Sim. (non-SMT)
Lg = 0.2 µm @ 2.5V (non-SMT)
Lg = 0.2 µm @ 2.5V (SMT)
Lg = 0.2 µm @ 3.3V (non-SMT)
Lg = 0.2 µm @ 3.3V (SMT)

(a)


Isolation (dB)
20
30
40
50
60
70
80
0
10
20
30
40
50
Frequency (GHz)
Lg = 0.2 µm @ 2.5V Sim. (non-SMT)
Lg = 0.2 µm @ 2.5V (non-SMT)
Lg = 0.2 µm @ 2.5V (SMT)
Lg = 0.2 µm @ 3.3V (non-SMT)
Lg = 0.2 µm @ 3.3V (SMT)

(b)



(c)

Figure 6-6 Measured and simulated: (a) insertion loss, (b) isolation and (c) return loss of the SP4T switch

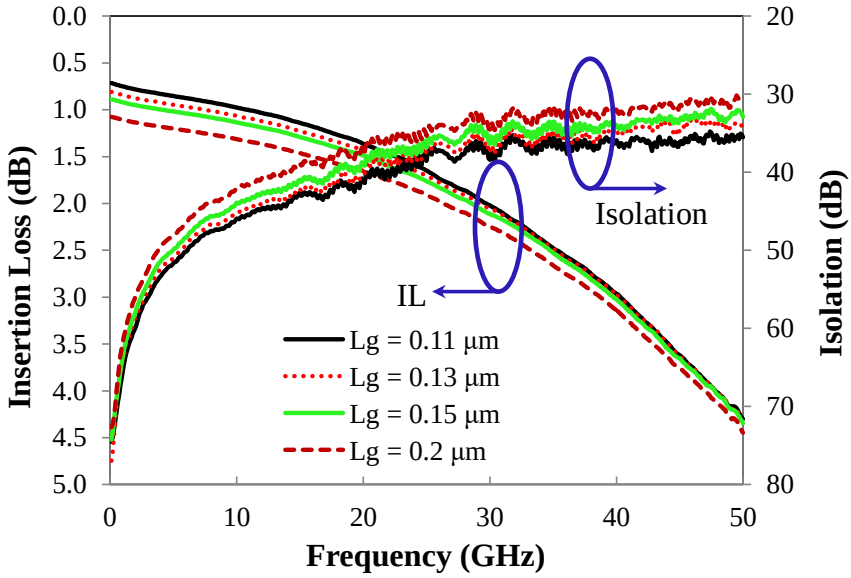


Figure 6-7 Measured insertion loss and isolation of SMT SP4T switches with different NMOS channel length.

Measured S-parameters for SMT SP4T switches with variable gate lengths are shown in Figure 6-7 (L_g = 0.11, 0.13, 0.15 and 0.2 µm). SMT SP4T switch with L_g = 0.11 µm under 3.3 V gate bias achieves low insertion loss of less than 0.96, 2.5 and 4.3 dB from dc to 10 GHz, 10 GHz to 35 GHz, and 35 GHz to 50 GHz, respectively, and high isolation of greater

than 35 dB from dc up to 50 GHz. The trend between SP4T switch performance and channel length are the same as that of SPDT switch. This again indicates that channel length has large effects on both insertion and isolation of the switches.

6.3.2 Power handling and linearity

Measured P1dB (at 1 GHz, 5 GHz, 10 GHz, 15GHz, 20GHz and 25 GHz) for designed SP4T switches are shown in Figure 6-8. Again, switches with longer channel length result higher P1dB. For the same switch, measured P1dB are nearly identical at different frequencies, and 3.3 V gate bias results a slightly higher P1dB (~0.5 dB) than 2.5 V gate bias. In addition, non-SMT switch shows comparable P1dB to SMT switch with same gate length (L_g = 0.2 μm). SP4T switch with L_g = 0.2 μm NMOS results a constant P1dB of ~14 dBm across the measured frequency range from 1 GHz to 25 GHz. SP4T with L_g = 0.11 μm shows a constant P1dB of around 11 dBm, combines with its lower insertion loss and higher isolation when compared to switch with longer channel length, SP4T switch with L_g = 0.11 μm may also be good candidate for ultra-wide RF switch application without performance degradation.

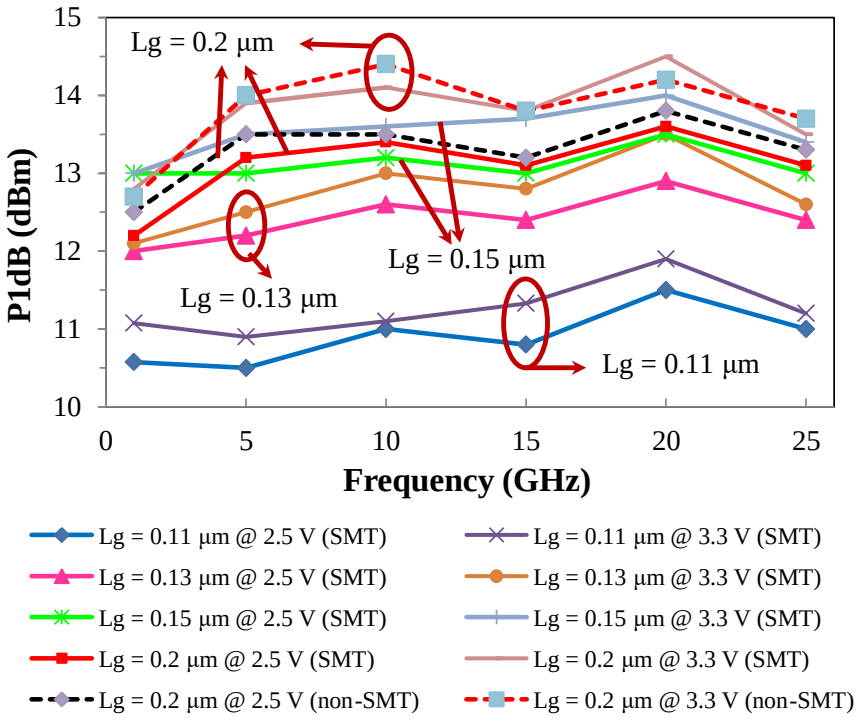


Figure 6-8 Measured P1dB for designed SP4T switches

Extrapolated IIP3 of SP4T switches (L_g = 0.2 µm for non-SMT SP4T, L_g = 0.13 µm and L_g = 0.2 µm for SMT SP4T, 2.5 V bias) are shown in Table 6-2. Similar to SPDT, IIP3 of SMT SP4T switch is slightly higher than that of non-SMT switch. For L_g = 0.2 µm, typical IIP3 is around 25-26 dBm and 24-25 dBm for SMT and non-SMT, respectively, at measured frequencies. Measured IIP3 for L_g = 0.13 µm SMT SP4T switch is around 23-24 dBm.

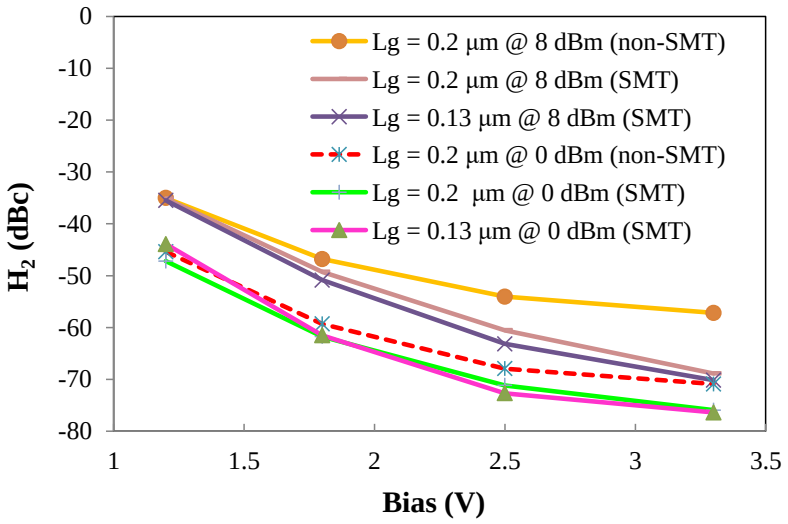
Table 6-2 Extrapolated SP4T IIP3 (SMT vs. Non-SMT)

Frequency (GHz)	non-SMT (dBm)	SMT (dBm)	
	0.2 µm	0.13 µm	0.2 µm
5	24.9	23	25.5
10	24.3	23.5	25.9

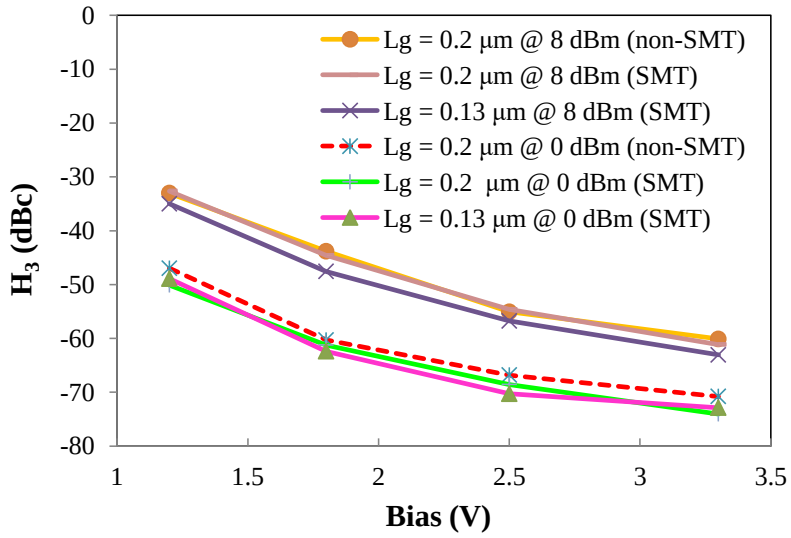
Measured H_2 and H_3 for SP4T switches (L_g = 0.2 µm for non-SMT SP4T, L_g = 0.13 µm and L_g = 0.2 µm for SMT SP4T) are shown in Figure 6-10. For the same gate length L_g =

0.2 μm, SMT SP4T switch shows slightly lower harmonic distortions than non-SMT switch. For measured SMT switches, L_g = 0.13 μm shows slightly lower harmonic distortion than L_g = 0.2 μm. Measured data also show similar gate bias dependence to SPDT switches.

Measured rise and fall time for SP4T switch are less than 15 ns for frequency from 1 GHz to 5 GHz.



(a)



(b)

Figure 6-9 Measured 2nd and 3rd harmonic distortion of SP4T switches at 5 GHz: (a) 2nd harmonic H_2, (b) 3rd harmonic H_3

6.4 Summary and comparison

High resistivity trap rich SOI based low loss ultra wideband SP4T switches are design and analyzed for the first time in this Chapter. A comparison with the state of the arts is given in Table 6-3, the proposed SP4T switches achieve the best combined performance including low insertion loss (< 2.5 dB at 35 GHz) and excellent isolation (>36 dB at 35 GHz) and acceptable power handling capability (> 11 dBm) and good linearity (> 23 dBm IIP3). These excellent performances are achieved by optimizing the size of both series and shunt transistors, and the matching inductor value. Further improvement of the switch performance is achieved by implementing SMT, it is found SMT can improve both insertion loss and isolation in a certain wide frequency range (dc to 35 GHz for designed SP4T switch). Proposed SP4T switches consume compact die area of only 0.36 x 0.19 mm^2. The fabricated SP4T switches show outstanding performance to be used for fully integrated and cost-effective ultra-wideband applications.

Table 6-3 Comparison of Wideband Switches

Ref.	Tech.	Type	BW	IL	ISO	Input P1dB	Chip Size	Topology
			(GHz)	(dB)	(dB)	(dBm)	(mm^2)	
[11]	0.13-µm triple-well CMOS	SPDT	2.4-20	0.9-2	43-21	30	0.17	Symmetric series-shunt, double-well body-floating
[34]	0.13-µm CMOS	SP4T	dc-70	< 2.7 at 10 GHz < 3.0 at 35 GHz	30	>9	0.24 x 0.23	series-shunt, with matching networks
[35]	45-nm SOI CMOS	SPDT	dc-60	1.7 at 45 GHz	>25 at 50 GHz	7.1	0.18×0.22	Series-shunt
[45]	0.35-µm SiGe	SPDT	42-70	< 1.25	>18	1	0.85x0.92	Differential SPDT
[46]	RF-MEMS	SP4T	dc-70	<1	>15	NA	NA	distributed transmission line
[49]	0.1-µm HEMT	SPDT	15-80	<3.6	>25	NA	1.5 x 1.5	traveling-wave concept
[50]	0.18-µm SiGe BiCMOS	SPDT	dc-30	1.5 – 3.3	>20	23	0.025	series-shunt, with matching network
[51]	0.18-µm SOI	SPDT	dc-40	<5	>17	15	0.28 x 0.09	series-shunt, with matching network
[52]	90-nm CMOS	SPDT	dc-60	<3	>48	17	0.68 x 0.87	traveling-wave concept
[53]	0.13-µm CMOS	SP4T	dc-30	<2.7	>26	9	0.25 x 0.18	series-shunt, with matching network
This work	**0.13-µm SOI**	**SPDT**	**dc-50**	**< 2.1 at 50 GHz** **< 1.7 at 45 GHz** **< 1.0 at 30 GHz**	**> 27 at 50 GHz**	**> 10.5**	**0.214 x 0.19**	**series-shunt, with matching network**
This work	**0.13-µm SOI**	**SP4T**	**dc-35**	**< 1.0 at 10 GHz** **< 2.5 at 35 GHz** **< 4.3 at 50 GHz**	**> 36 at 35 GHz** **> 35 at 50 GHz**	**> 11**	**0.36 x 0.19**	**series-shunt, with matching network**

Chapter 7

Ultra wideband DPDT switch design

7.1 Introduction

RF switch matrix is also widely used in modern communication systems such as wireless internet, relay stations and satellite communications, etc., which need route RF signals between multiple inputs and multiple outputs (MIMO). The ability of switches to operate over wide bandwidth is becoming increasingly important to enable wideband or multi-band systems on chip. Design high performance switch matrix including lower insertion loss, higher isolation and acceptable power handling capability and good linearity over an ultra-wide bandwidth from dc to cross millimeter-wave boundary are quite challenging.

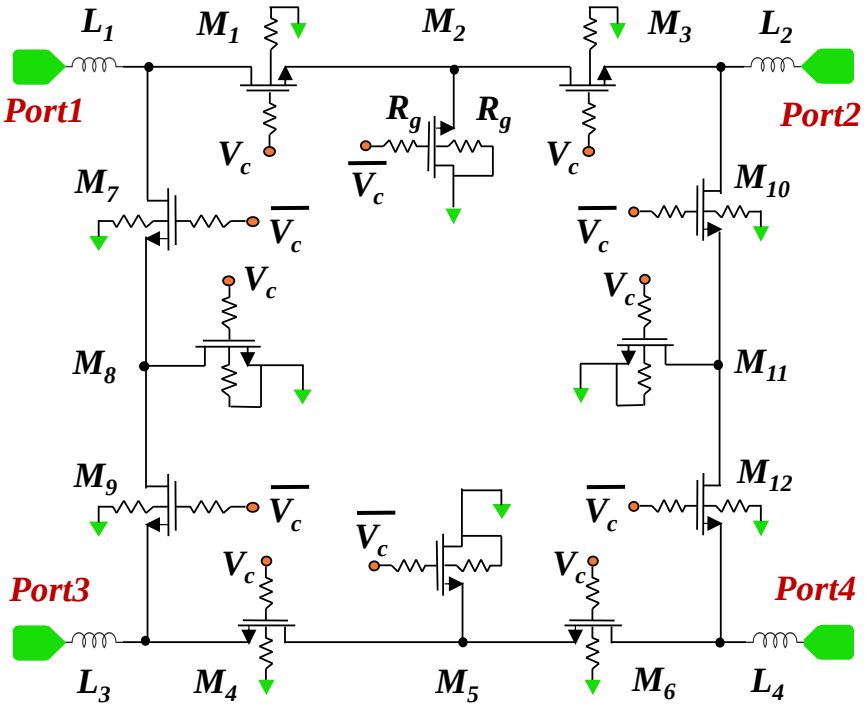
RF switch matrixes for MIMO application have been reported based on various processes and technology nodes previously, including GaAs JFET [75], 0.5 μm pHEMT process [76], PIN diode [77], 0.13 μm CMOS [78], 0.12 μm triple-well CMOS [79], and [80]-[82]. However, all these designs are limited within dc to 12 GHz frequency range.

In this work, 2 x 2 double-pole-double-throw (DPDT) switches based on GLOBALFOUNDRIES's world first commercial 300 mm 0.13 μm high resistivity trap-rich (HR TR) SOI are designed, the designed switches are aimed to achieve the low insertion loss, high isolation, high power handling and good linearity over dc to millimeter wave frequency range.

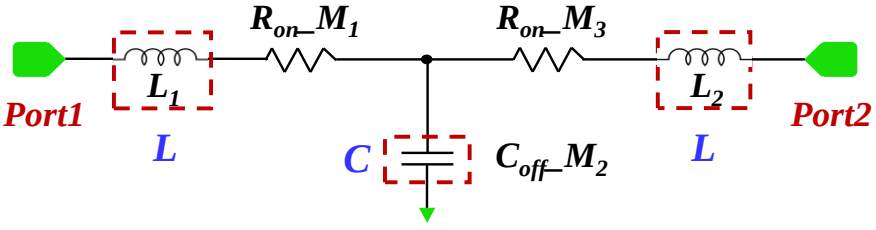
7.2 DPDT switch design considerations

7.2.1 DPDT switch configuration

Same as 200 mm SOI process which adopted for SPDT and SP4T RF switch design presented in Chapter 5 and Chapter 6, GLOBALFOUNDRIES's 300 mm 0.13 μm RFSOI process also offers 2.5 V body-tied thick gate oxide NMOS switch transistor (nominal gate length, L_g = 0.2 μm). The thickness of the top silicon and BOX are around 1600 Å and 2000 Å, respectively. The handle silicon (Si) substrate also has resistivity higher than 3000 Ω-cm, a trap rich layer is also available between the BOX and handle Si layer .The designed DPDT switches are based on series-shunt-series with input and output matching network topology to achieve a wideband operation.



(a)



(b)

Figure 7-1 (a) Schematic of the DPDT switch, and (b) equivalent *L*-*C*-*L* T-matching network model

On-chip series inductors are used and act as *L*-*C*-*L* T-matching circuit using the off-state capacitance of the shunt NMOS as shunt capacitor *C*. The final topology for DPDT switch and equivalent *L*-*C*-*L* T-matching network model are shown in Figure 7-1. The DPDT switch is constructed by four symmetric single-pole single-throw (SPST) switch branches in a ring-type structure. One SPST branch, with series transistors M_1 and M_3, and shunt transistor M_2, forms the path between Port 1 and Port 2, and the other three SPST branches, which also combined by series-shunt-series transistors, forms other paths between Port 1 and Port 3, Port 2 and Port 4, and Port 3 and Port 4, respectively. The L_1, L_2, L_3, and L_4 are used as the matching inductors for each branch. When V_C is high (= 3.3 V), series transistor M_1, M_3, M_4, M_6, and shunt transistor, M_8 and M_{11}, are turned on, at the same time, series transistor M_7, M_9, M_{10}, M_{12}, and shunt transistor, M_2 and M_5, are turned off, so RF signal can flow between Port 1 and Port 2, and between Port 3 and Port 4, while cannot flow between Port 1 and Port 3, and between Port 2 and Port 4. On the contrary, when V_C is low (-3.3 V), RF signal can only be transferred between Port 1 and Port 3, and between Port 2 and Port 4.

Compared with previously designed SPDT switch, which the topology is series-shunt, the challenges involved with going from SPDT to DPDT are as follows:

1) Higher insertion loss (IL) of DPDT than SPDT due to different topologies used. This can be explained by comparing the derived insertion loss equations (using ABCD matrix).

For SPDT, the actual insertion loss (in dB) for the series-shunt branch is as shown in equation (4-10), also as shown in below (7-1):

$$IL = 10\log\{\left(1 + \frac{R_{on}}{2Z_0}\right)^2 + [\pi f C_{off}(R_{on} + Z_0)\,]^2\} \quad (7\text{-}1)$$

While for the proposed DPDT switch, based on the equivalent model of the series-shunt-series branch as shown in Fig. 7-1(b), in the on-state, the insertion loss for this series-shunt-series branch is:

$$IL = 10\log\{\left(1 + \frac{R_{on}}{Z_0}\right)^2 + [2\pi f C_{off}(2R_{on} + Z_0 + \frac{R_{on}^{\ 2}}{Z_0})]^{\ 2}\} \quad (7\text{-}2)$$

As can be seen from equations (7-1) and (7-2), for the same transistors' dimension, more insertion loss is introduced due to the series-shunt-series topology.

2) Higher off-state capacitance of the DPDT. To achieve a low insertion loss in the on state, the series transistors in each series-shunt-series path must be as large as possible. On the other hand, the series transistors must be as small as possible to reduce the parasitic capacitances in the off-state paths to achieve high isolation. Therefore, a trade-off is required for the series transistors' dimension.

3) Higher signal leakage because of the DPDT configuration. For example, as can be seen from the schematic diagram of DPDT switch in Figure 7-1 (a), when the arm between Port1 and Port2 is in the on state, the arm between Port3 and Port4 will also be in the on-state. This will cause some signal leakage from Port1 to Port3 and even Port4. However, SPDT does not have this problem. As a result, the insertion loss and isolation of DPDT are not as good as the SPDT.

7.2.2 *DPDT switch size*

In this work, two groups of series-shunt-series transistors are designed for evaluation. DPDT1 is designed with series-shunt-series transistor widths = 75 µm/100 µm/75 µm, and L_1 = L_2 = L_3 = L_4 = 140 pH, DPDT2 is designed with series-shunt-series transistor widths = 150 µm/100 µm/150 µm, and L_1 = L_2 = L_3 = L_4 = 170 pH. External resistors, R_g = 20 kΩ are connected to gate and body of each transistor for ac floating to prevent signal leakage and gate oxide breakdown.

Same DPDT layout but with shorter channel length (L_g = 0.11 µm and L_g = 0.13 µm) is also designed to investigate the channel length effect on ultra wideband DPDT switch performance.

7.2.3 *Switch design with novel recessed device_Gen2 switch*

The legacy generation1 switch transistor (Gen1) concurrently offered in this technology is fabricated using the global top silicon thickness, which is 1600A. A new generation2 switch device (Gen2) has also been developed which is fabricated on recessed silicon, to provide lower R_{on}-C_{off}. The recessed silicon is achieved through selective localized etching process. A schematic view of the Gen1 switch transistor and Gen2 switch transistor is shown in Figure 7-2.

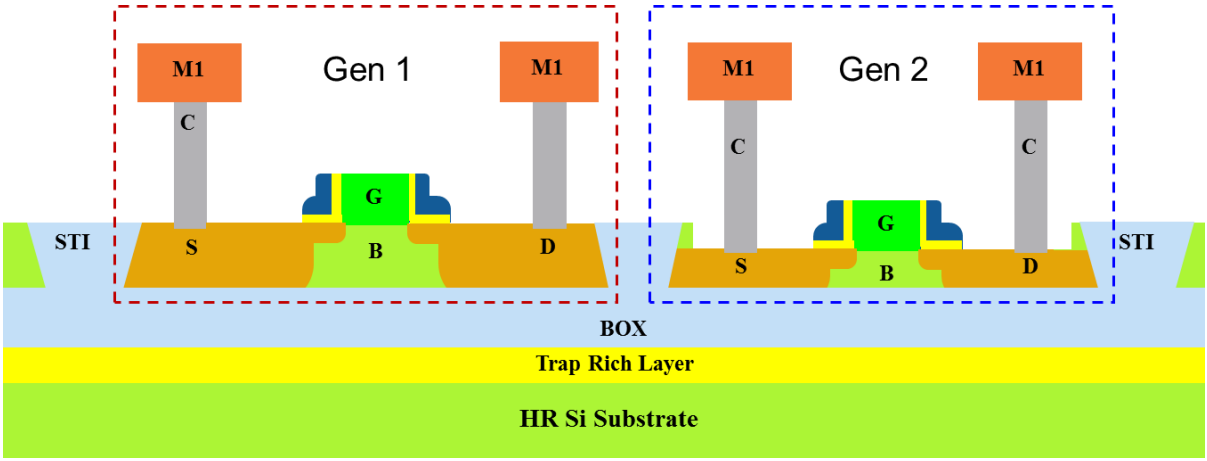


Figure 7-2 Schematic view of Gen1 and Gen2 switch transistors

By fine device tuning, much higher drain current is achieved for Gen2 switch transistor when compared to Gen1 switch, the I_d-V_d curve for both Gen1 and Gen2 switch transistors are shown in Figure 7-3, A 41% improvement, from 193fs to 120fs in R_{on}*C_{off} is achieved as illustrated in Table 7-1. In this work, both Gen1 and Gen2 switch NMOSs are used for DPDT switch design to check switch performance in a wide frequency range.

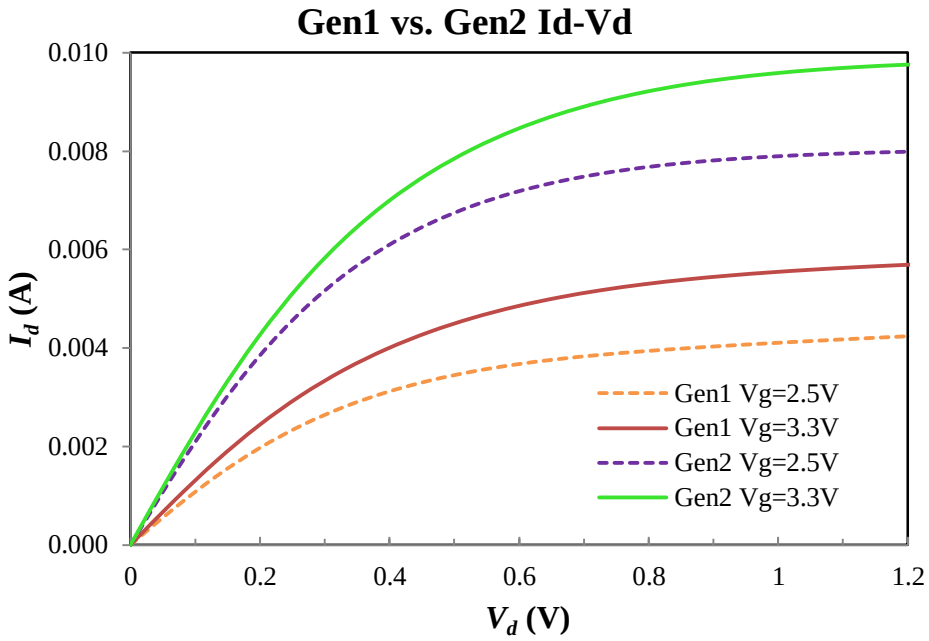


Figure 7-3 I_d-V_d of Gen1 and Gen2 switch transistors

Table 7-1 Comparison between the Gen1 and Gen2 switch

Device	R_{on} (ohm-mm)	C_{off} (fF/mm)	R_{on}*C_{off} (fs)
Gen1	0.71	272	193
Gen2	0.5	239	119.5

7.2.4 DPDT switch design with through BOX contact (TBC)

In SOI, the handle substrate is isolated from the top Si by the BOX insulator layer, in other words, the substrate is electrically floating. During wafer fabricating, there are a lot of

process steps which involve plasma generation, including plasma etch, plasma enhanced thin film deposition, etc. could induce charging and these charges can be trapped by the trap rich layer in between the BOX layer and the handle substrate. Such static build ups can cause a back channel of the SOI devices to turn on, which can disturb performances of normal devices fabricated in the top Si. To solve this problem, a GLOBALFOUNDRIES proprietary method is employed to ground the handle substrate. A through BOX contact (TBC) can be made to connect the substrate to normal transistors via metal wiring, as illustrated in Figure 7-4.

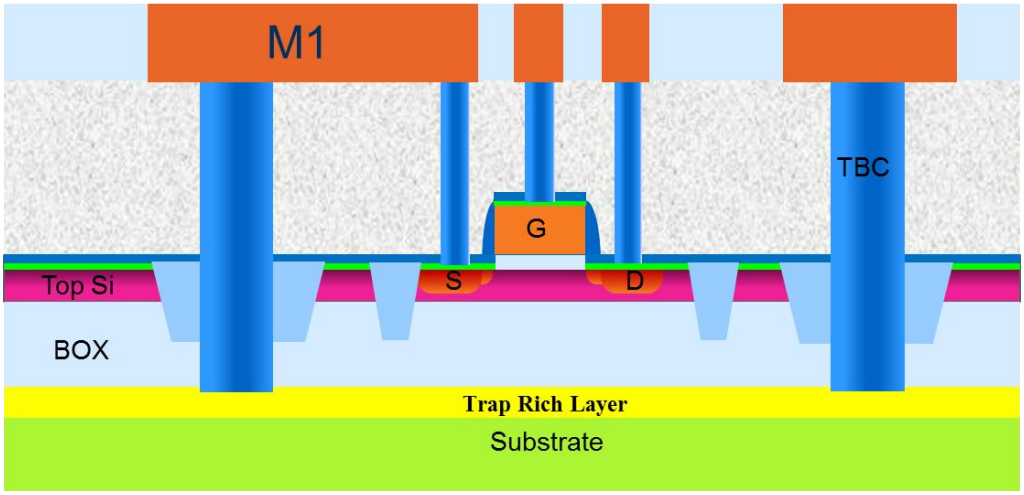


Figure 7-4 Switch transistor connected with through box contact (TBC)

In DPDT switch layout, to study the TBC effect on switch performance, both switches, with and without TBC connection are designed (for Gen2 switch). For DPDT switch with TBC connection, in each series-shunt-series branch, TBCs are added to connect both gate to substrate and body to substrate, as illustrated in Figure 7-5.

The I_d-V_g curves of Gen2 switch transistor (which is more sensitive to plasma charging compared to Gen1 switch due to thin top silicon and negative V_t) with and without TBC connection are illustrated in Figure 7-6. As can be seen, the drain current Id of the switch NMOS without TBC connection is several orders higher than that of NMOS with TBC

connection in the off state region (when $V_g < V_{tlin}$, which is about -0.2 V). When there's no TBC connected to the switch transistor, the process induced plasma charges are stored at the interface between SOI top silicon and BOX, which contributed to the higher leakage. When a switch transistor is connected to TBC, the charges can be discharged to the handle substrate through TBC, so that the plasma charging effect on the normal device performance is minimized.

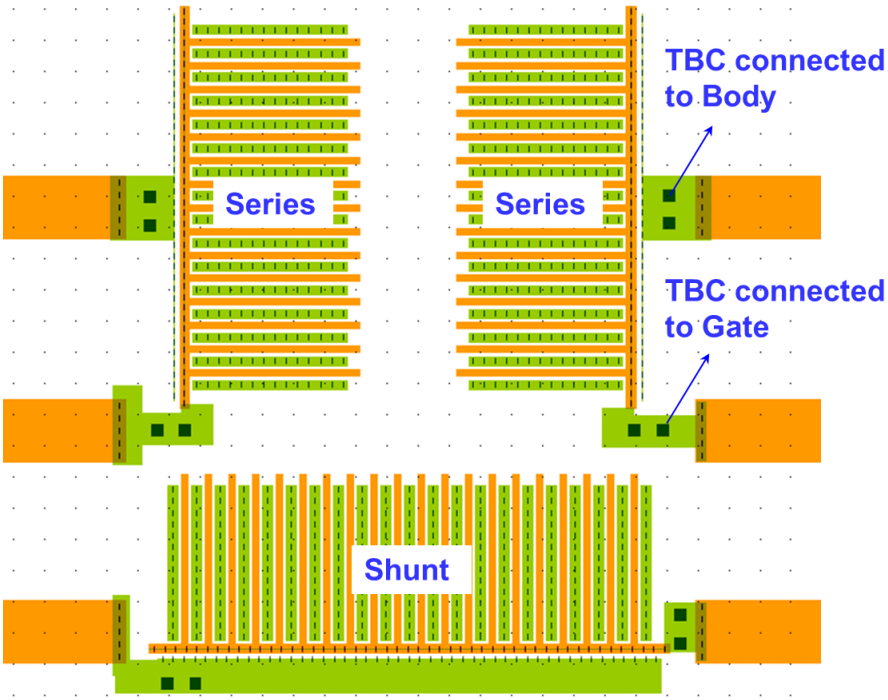


Figure 7-5 Layout of through box contact (TBC) in series-shunt-series switch branch

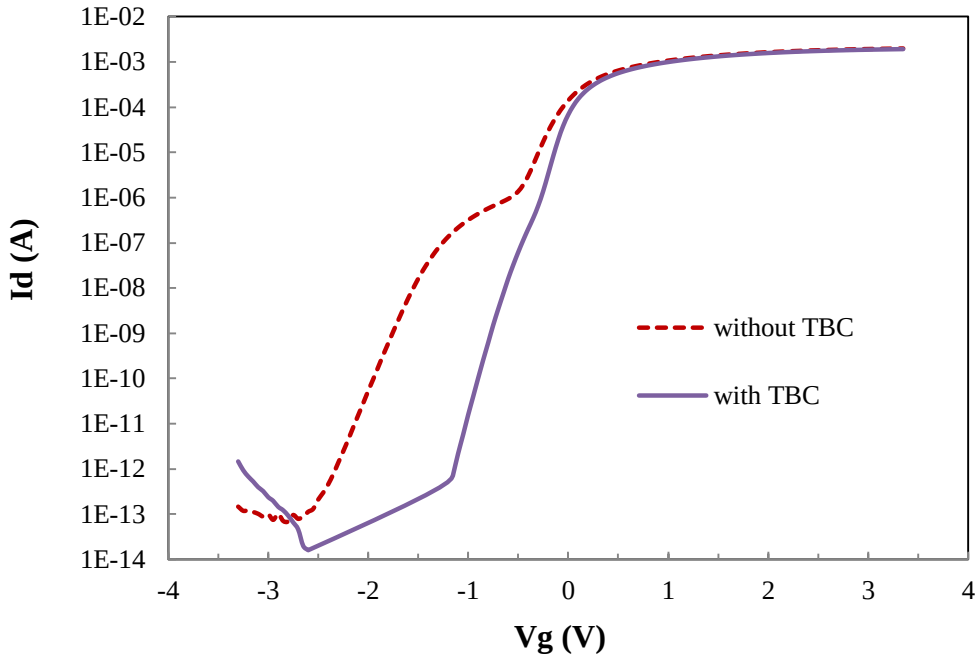


Figure 7-6 Gen2 switch NMOS I_d-V_g Curves (with TBC vs. without TBC)

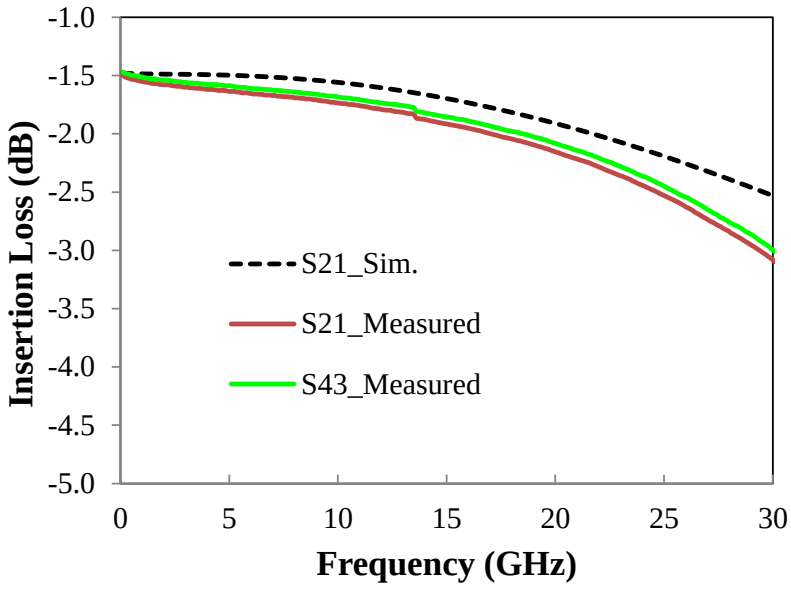
7.3 Gen1 DPDT switch performance

Figure 7-7 Photography of the designed DPDT Switch

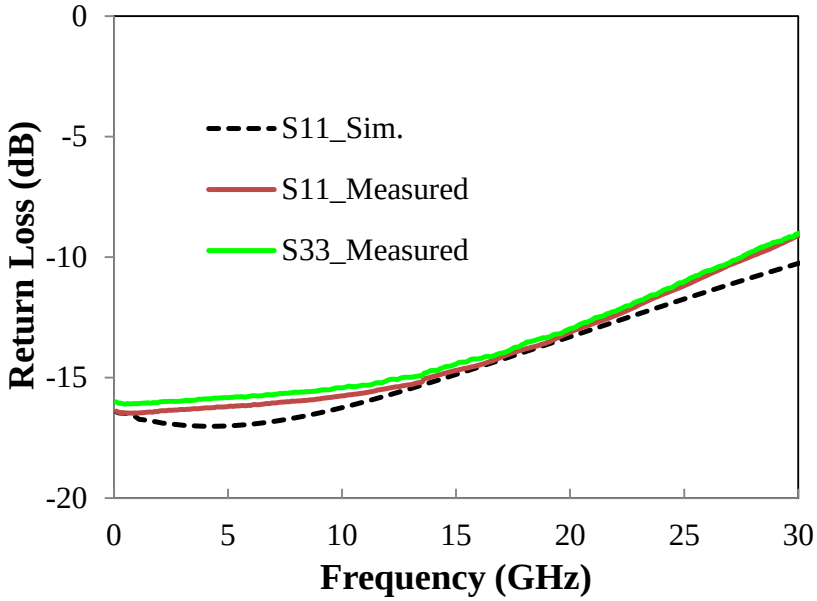
Photography of fabricated DPDT switch is shown in Figure 7-7 (take L_g = 0.2 μm Gen1 DPDT switch for example), two GSGSG pads are used, one GSGSG pad connects to Port 1 and Port 3, the other GSGSG pad connects to Port 2, Port 4 of the DPDT switch for RF testing. V_{c1} and V_{c2} pads are used for dc biasing of the series and shunt transistors.

7.3.1 S-parameters of Gen1 switch with nominal size

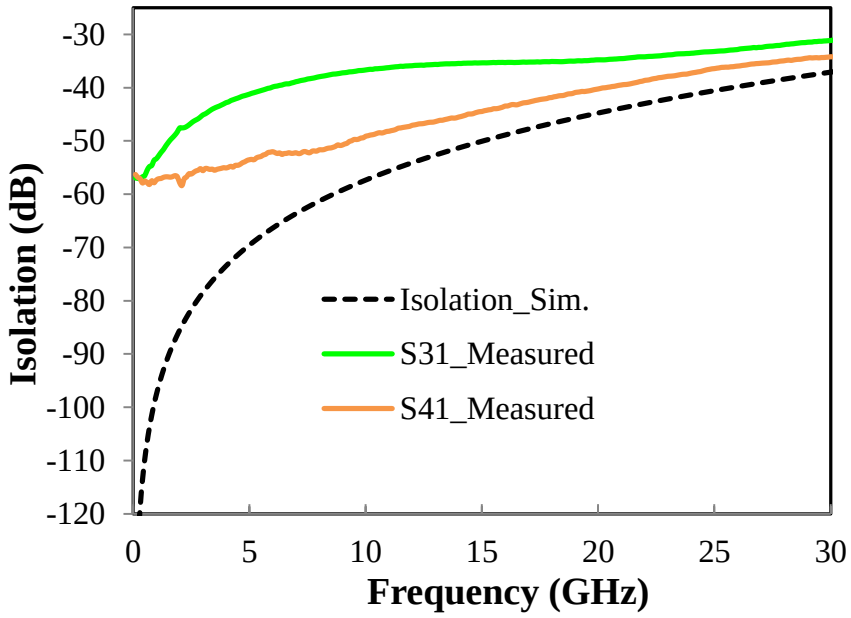
Simulated and measured S-parameters of the Gen1 DPDT switch (series-shunt-series transistor widths = 75 μm/100 μm/75 μm) with nominal gate length L_g = 0.2 μm are presented in Figure 7-8. The measurements are done on chip after a SOLT calibration. The measured insertion loss between Port 1 and Port 2 (S21, take V_C = 3.3 V for example, when V_C = 3.3 V, Port 1 and Port 2, Port 3 and Port 4 are both in "on" state) and insertion loss between Port 3 and Port 4 (S43) are lower than 2.5 dB, measure isolation between Port 1 and Port 3, and isolation between Port 1 and Port 4 are higher than 33 dB and 36 dB, respectively, at 25 GHz. And measured insertion loss S_{21}/S_{43} is lower than 7 dB, isolation S_{31} and S_{41} higher than 29 dB and 31 dB at 50 GHz, respectively. The measured insertion losses don't agree well with simulation when signal frequency is higher than 10 GHz, this should be due to the foundry model are characterized up to 10 GHz only, and the model cannot predict well the switch performance when frequency gets higher. Measured return loss is lower than 11dB at 25 GHz, and about 4 dB at 50 GHz, respectively. When V_C = -3.3 V, Port 1 and Port 3, Port 2 and Port 4 are in "on" state, the switch shows comparable performance and were not included.


-1.0
-1.5
-2.0
-2.5
-3.0
-3.5
-4.0
-4.5
-5.0
Insertion Loss (dB)
S21_Sim.
S21_Measured
S43_Measured
0
5
10
15
20
25
30
Frequency (GHz)

(a)


0
-5
-10
-15
-20
Return Loss (dB)
S11_Sim.
S11_Measured
S33_Measured
0
5
10
15
20
25
30
Frequency (GHz)

(b)



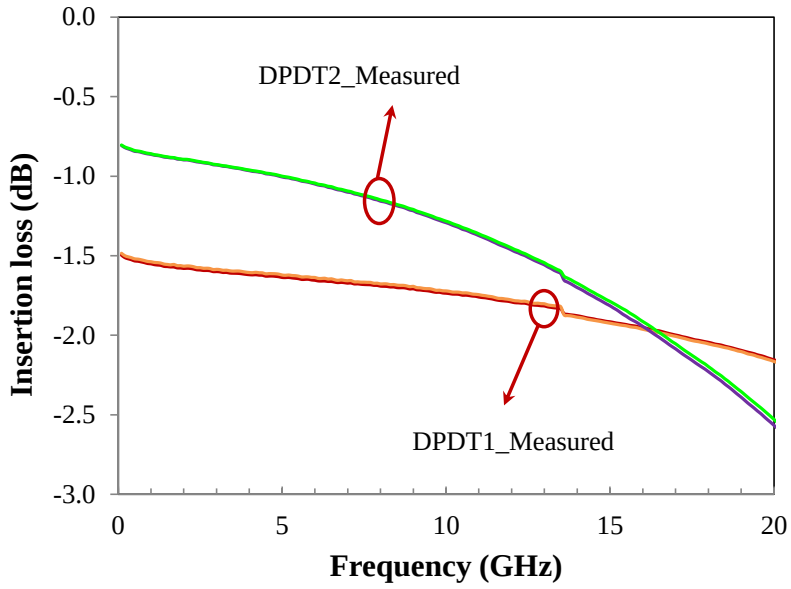
(c)

Figure 7-8 Simulated and measured results of DPDT switch: (a) insertion loss, (b) return loss and (c) isolation (L_g = 0.2 μm)

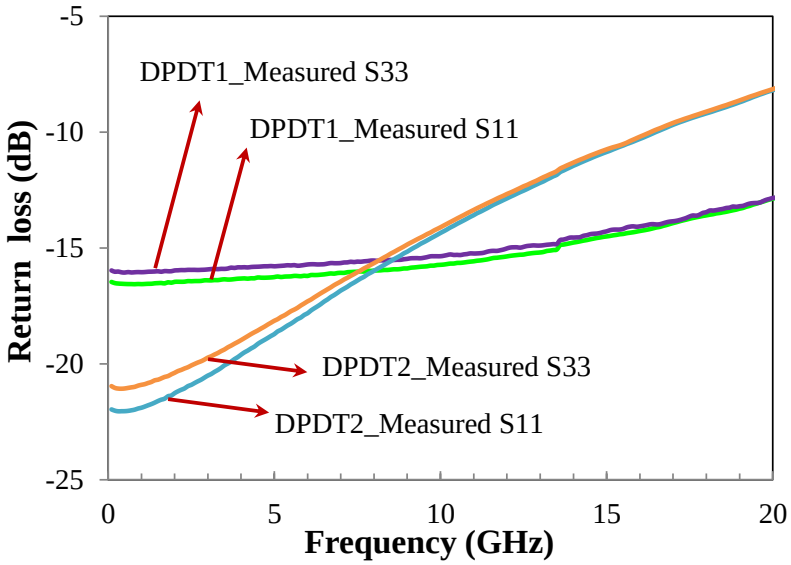
7.3.2 Series transistor width (W) effect

Measured S-parameters of the Gen1 DPDT2 switch (series-shunt-series transistor widths = 150 μm/100 μm/150 μm) with nominal gate length L_g = 0.2 μm and performance comparison with DPDT1 switch are presented in Figure 7-9. As series transistor width increases from 75 μm to 150 μm, transistor R_{on} is reduced as can be deduced from Equation (5-1). The measured insertion loss of DPDT2 is lower than DPDT1 in the frequency range of dc to 16 GHz (0.5 to 0.7 dB lower insertion loss is obtained in the range of dc to 10 GHz). When frequency is higher than 16 GHz, the measured insertion loss of DPDT2 is becoming higher than DPDT1 switch. This is because of the higher C_{off} of DPDT2 which resulted from the wider width. Measured Port 1 to Port 3 isolation S_{31} of DPDT2 is higher than 31 dB at 15 GHz, about 3 dB lower than that of DPDT1, measured Port 1 to Port 4 isolation S_{41} of

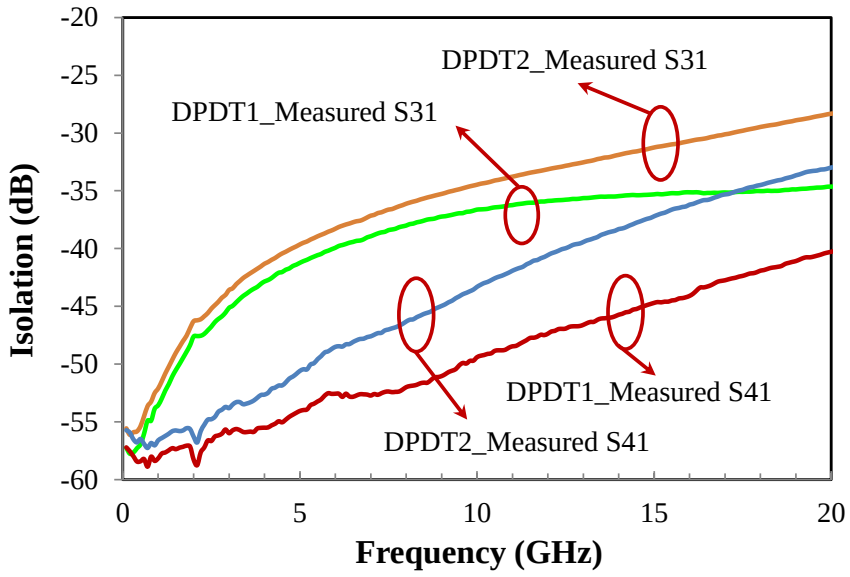
DPDT2 switch is higher than 37 dB at 15 GHz, about 6 dB lower than that of DPDT1 switch. Measured return loss is higher than 11 dB at 15 GHz for DPDT2 switch.



(a)



(b)

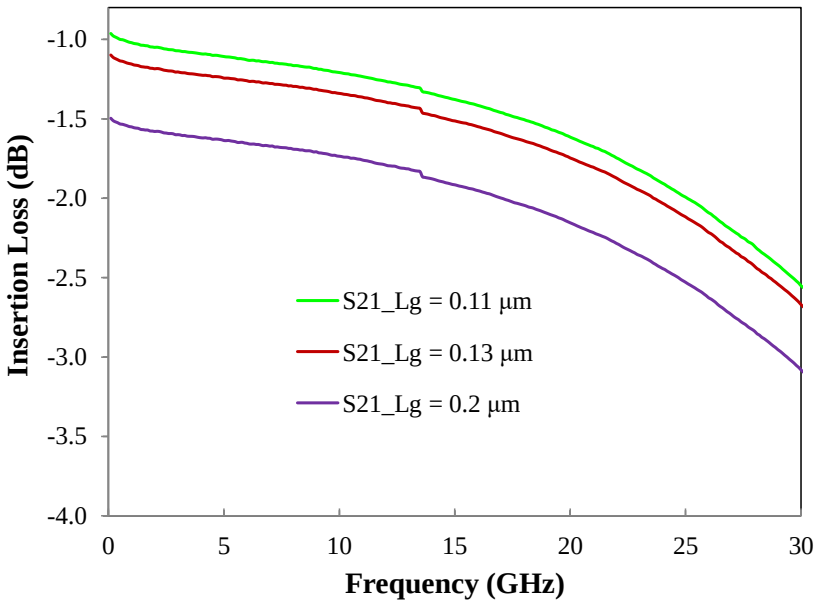


(c)

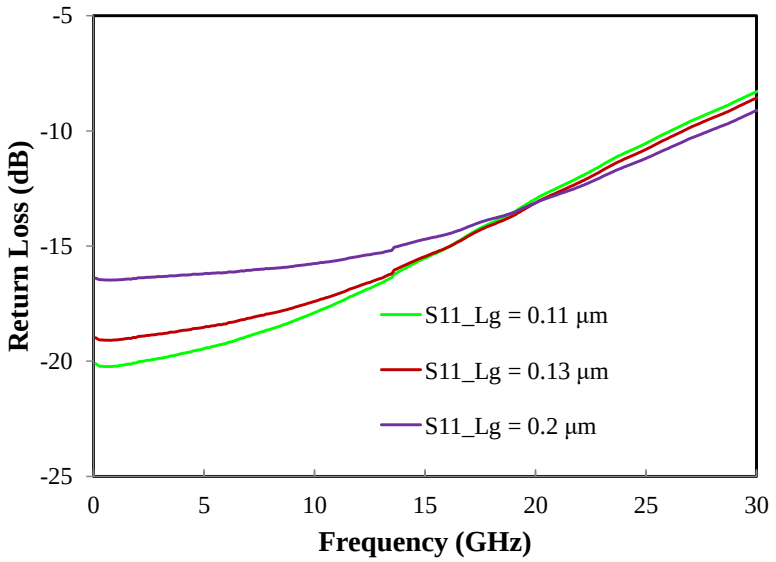
Figure 7-9 Measured results of DPDT switches: (a) insertion loss, (b) return loss and (c) isolation of different channel width

7.3.3 Transistor channel length (L) effect

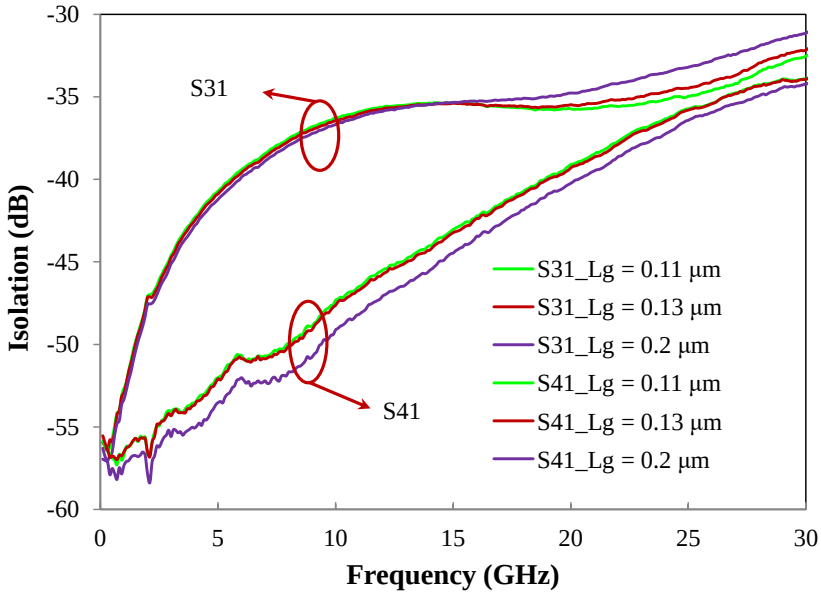
Measured S-parameters of the Gen1 DPDT1 switches with shorter channel length, L_g = 0.11 µm and L_g = 0.13 µm are illustrated in Figure 7-10, and when compared with switch performance fabricated with nominal channel length L_g = 0.2 µm. Switch insertion loss is improved by shortening the channel length, measured insertion loss, S21 and S43 of L_g = 0.11 µm and L_g = 0.13 µm are lower than 2 dB and 2.15 dB at 25 GHz, respectively. Measured isolation S31 of L_g = 0.11 µm and L_g = 0.13 µm are higher than 35 dB and 34.5 dB at 25 GHz, and isolation S41 of L_g = 0.11 µm and L_g = 0.13 µm are higher than 35.7 dB and 35.8 dB at 25 GHz, respectively.


-1.0
-1.5
-2.0
-2.5
-3.0
-3.5
-4.0
Insertion Loss (dB)
S21_Lg = 0.11 µm
S21_Lg = 0.13 µm
S21_Lg = 0.2 µm
0
5
10
15
20
25
30
Frequency (GHz)

(a)


-5
-10
-15
-20
-25
Return Loss (dB)
S11_Lg = 0.11 µm
S11_Lg = 0.13 µm
S11_Lg = 0.2 µm
0
5
10
15
20
25
30
Frequency (GHz)

(b)



(c)

Figure 7-10 Measured results of DPDT switch: (a) insertion loss, (b) return loss and (c) isolation of different channel length

7.3.4 Power handling and linearity

Measured P1dB of both DPDT1 switch and DPDT2 switch are about 19-20 dBm and 20-22 dBm at measured frequency of 1 GHz, 5 GHz, and 10 GHz. Due to measurement system input power limitation, P1dB above 10 GHz are not available. The output power curves of both DPDT1 and DPDT2 (L_g = 0.2 µm) at 10 GHz are shown in Figure 7-11 (a). P1dB of switches with short channel lengths are also measured and summarized in Figure 7-11 (b). Measured P1dB of 0.11 µm and 0.13 µm switches are slightly lower than nominal 0.2 µm switches, and DPDT2 switches show 1-2 dB higher P1dB compared to DPDT1 switches.

There are two major mechanisms of RF switch power compression.

The first one is turning on of the switch transistors in the off-state (shunt) branch. A MOSFET will turn on when the gate to source bias exceeds its threshold voltage V_t, switch compression occurs when a transient voltage on the shunt transistor is higher than its V_t

during part of the cycle, input power will be routed to the ground instead of output. P1dB for this case is as shown in equation (7-2) (in dBm) :

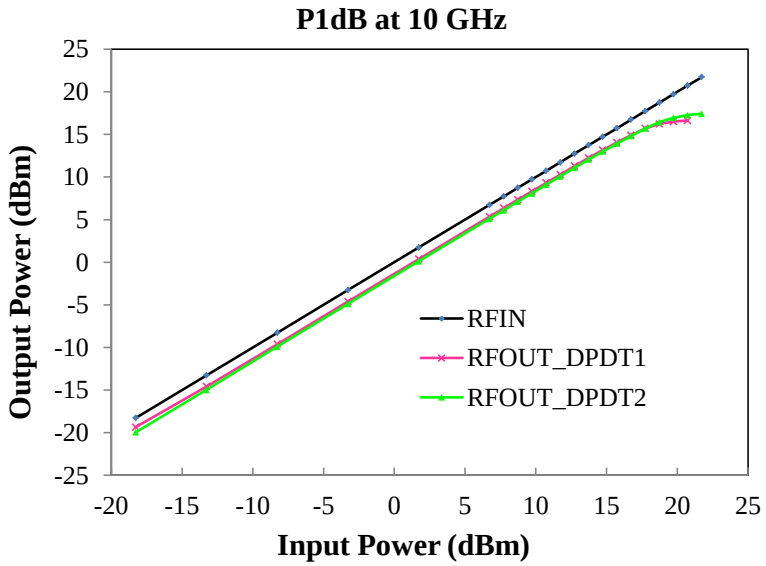
$$P1dB\_V_t = 10\log_{10}\left(\frac{2(V_{on}-V_{off})^2}{Z_0}\right) + 30 \quad (7\text{-}3)$$

Where V_{off} is the control voltage used to switch off the transistors, and Z_0 is the system impedance.

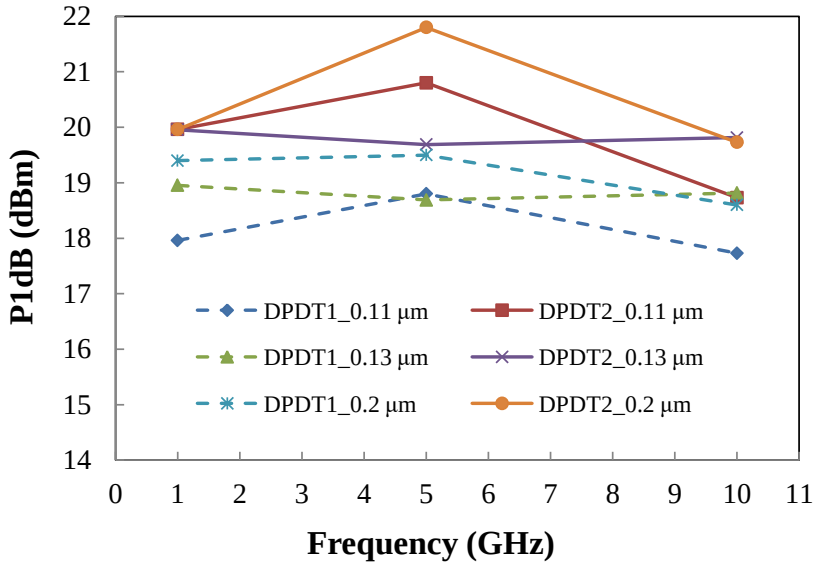
The second characteristic is the junction breakdown of the switch transistors in the off state branch. Compression will also occur when the RF voltage swing causes the source drain breakdown voltage (V_{bd}) to be exceeded on part of the cycle, P1dB for this case is shown in equation (7-3) (in dBm):

$$P1dB\_V_{bd} = 10\log_{10}\left(\frac{{V_{on}}^2}{2Z_0}\right) + 30 \quad (7\text{-}4)$$

In this design, for L_g = 0.2 μm transistor, V_t is about 0.7 V, V_{off} is -3.3 V, and V_{bd} is around 3.2 V. So the calculated P1dB_V_t is around 27-28 dBm, and calculated P1dB_V_{bd} is around 20 dBm. Since P1dB_V_{bd} < P1dB_V_t, the cause of compression will be source drain breakdown and compression will start around 20 dBm. Measured P1dB of switch with L_g = 0.2 μm is around 19-20 dBm, which matches well with that of the calculation. As channel length shortens from 0.2 μm to 0.13 μm or 0.11 μm, the source drain breakdown voltage decreases, so P1dB will also decrease.



(a)



(b)

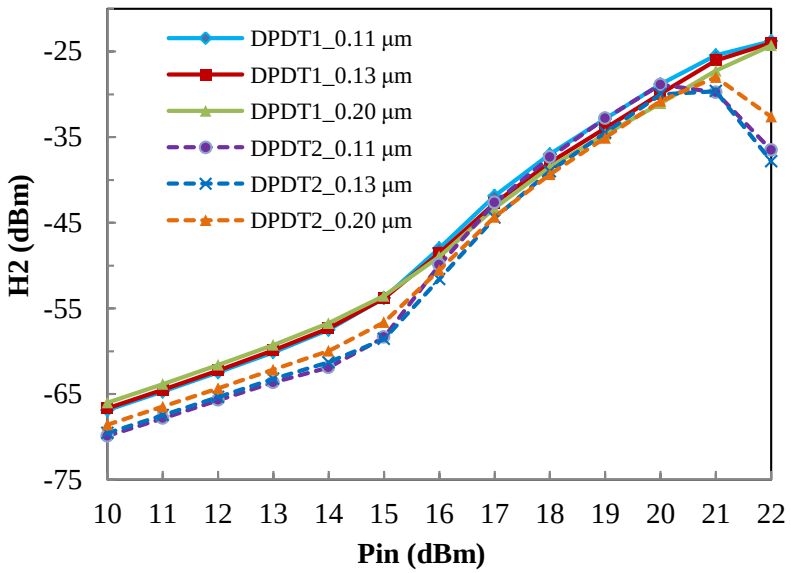
Figure 7-11 a) Measured output power of DPDT1 and DPDT2 switches (L_g = 0.2 µm), (b) measured P1dB of designed switches

Harmonic distortion of both DPDT1 and DPDT2 switches were also measured, as illustrated in Figure 7-12. The measurements were done by sweeping RF power from 10 dBm to 22 dBm to Port 1 and measuring the harmonics received at Port 2. The other two ports,

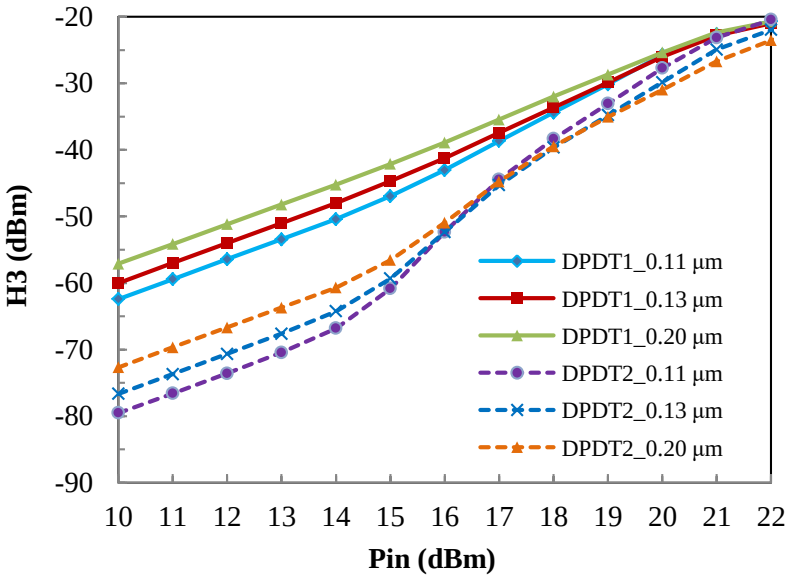
Port 3 and Port 4 are floating during measurement. Due to system limitation, the measurements were carried with fundamental frequency of 900 MHz only.

As shown in Figure 7-12, measured 2nd order harmonic distortions (H_2) of DPDT2 switches are about 2-3 dBm lower than H_2 of DPDT1 switches when input power is lower than 16 dBm. Within each switch group, switches with different channel length show comparable 2nd harmonic distortions. Measured 3rd order harmonic distortions (H_3) of DPDT2 are about 14 dBm lower than DPDT1 switches with same channel length. Within each switch group, switches with shorter channel length show better 3rd harmonics in a certain input power range, measured H_3 of 0.13 μm switches are about 4 dBm lower than 0.2 μm, measured H_3 of 0.11 μm switches show further 2 to 3 dBm lower H_3 as compared to 0.13 μm switches. The measured result indicated that 2nd harmonic distortion can be improved by using wider transistor width, while 3rd harmonic distortion can be improved by using both wider transistor width and shorter transistor channel length in a certain frequency range. The 3rd harmonic H_3 is dominated by Ron of the switch branch. As indicated in equation (5-1), R_{on} can decrease by widening transistor width and shortening transistor channel length. So H_3 of DPDT2 switches (with wider width) are better than those of DPDT1 switches and within each switch group, H_3 of L_g = 0.11 μm is better than those of L_g = 0.13 μm and 0.2 μm switches.

Meanwhile, when input power increases, harmonic of switches with shorter channel length start to rise up earlier than switch with nominal channel length, harmonic of switches with wider width also start to rise up earlier than narrower width switches. So it's a trade-off between maximum power handling and harmonic distortions.



(a)



(b)

Figure 7-12 Measured harmonic distortions of DPDT1 and DPDT2 switches, (a) 2nd harmonic H_2, (b) 3rd harmonic H_3

To further investigate the linearity of the designed switches, the third-order intermodulation products of fabricated switches were measured with Agilent E8267D PSG Vector Signal Generator (100 kHz to 20 GHz, measured at two-tone mode) at 2 GHz, and

spaced by 10 MHz. R&S ZVA67 (10 MHz – 67 GHz) is used as spectrum analyzer. As shown in Figure 7-13, the extrapolated input third-order interception point (IIP3) of the DPDT1 switches (L_g = 0.2 μm) is about 34 dBm. Extrapolated IIP3 of fabricated switches are summarized in Table 7-2. IIP3 of DPDT1 switches are generally comparable to those of DPDT2 switches for the same gate length at the same measurement frequency. Typical IIP3 of L_g = 0.11, 0.13 and 0.2 μm switches are around 32, 32.5 and 34 dBm, respectively.

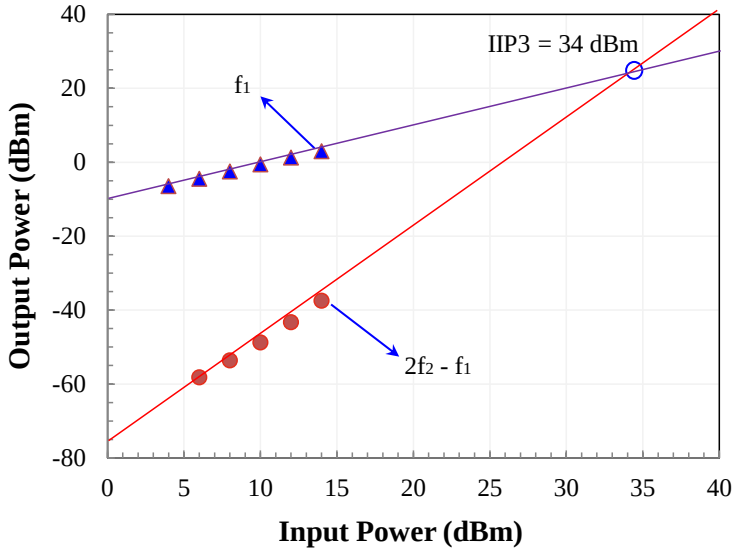


Figure 7-13 Measured IIP3 of DPDT1 switch (L_g = 0.2 μm)

Table 7-2 Extrapolated IIP3 of DPDT switches

Frequency (GHz)	DPDT1 (dBm)			DPDT2 (dBm)		
	0.11 μm	0.13 μm	0.2 μm	0.11 μm	0.13 μm	0.2 μm
2	32	32.5	34	32	33	34.5

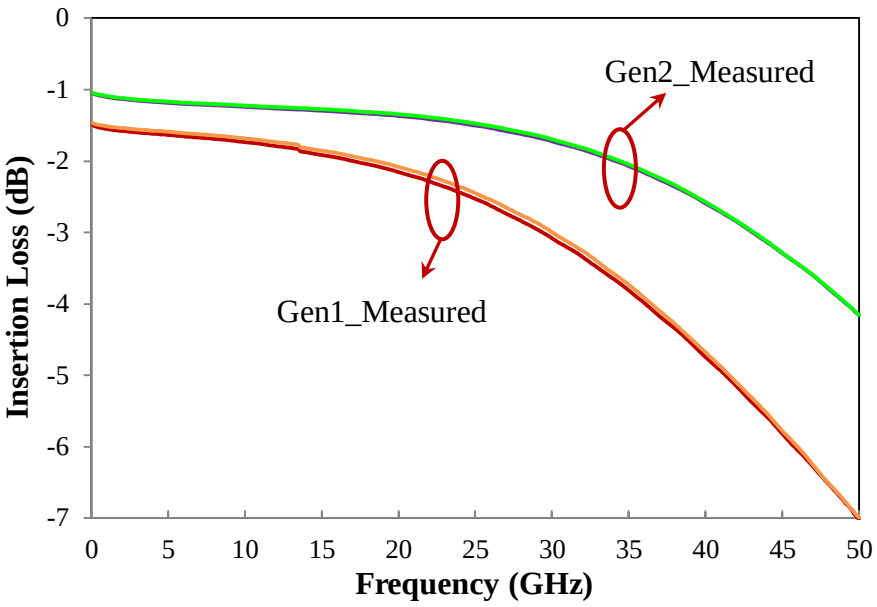
7.4 Gen2 DPDT switch performance

Gen2 switch transistor was developed in order to achieve lower switch R_{on}*C_{off}, through thinning down the SOI top Si thickness and device tuning to change the transistor

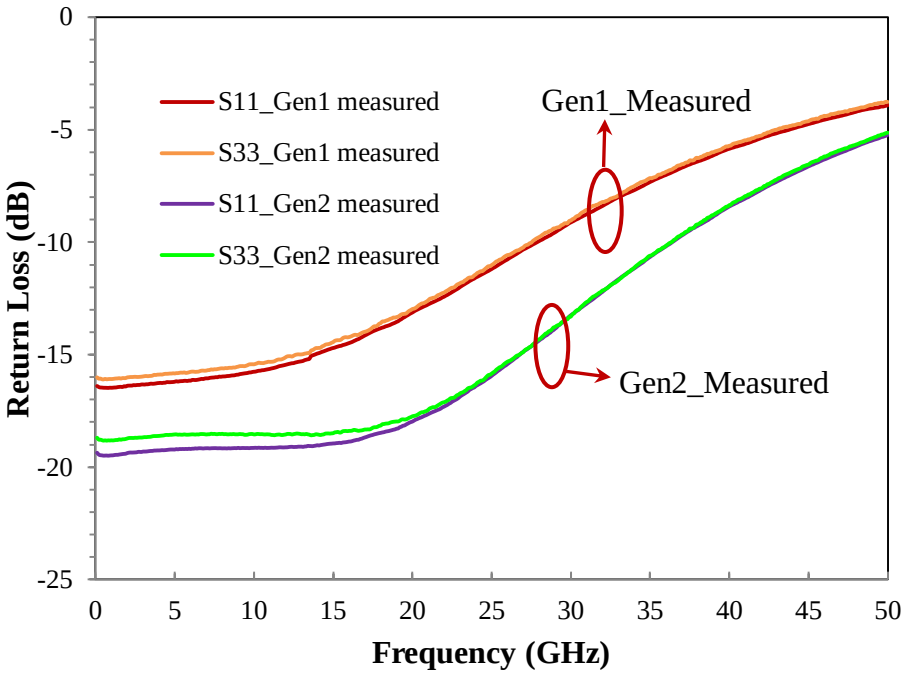
threshold from positive (Gen1 switch) to negative, while maintain a comparable breakdown voltage with Gen1 switch.

7.4.1 S-parameters of Gen2 switch with nominal size

Measured S-parameters of the designed Gen2 DPDT1 switch, with nominal gate length L_g = 0.2 μm and series_shunt_series transistor width 75_100_75 μm are presented in Figure 7-14 and are compared with Gen1 switch performance. Gen2 switch shows much lower insertion loss than Gen1 switch, the measured insertion loss S21 and S43 are lower than 1.5 dB at 25 GHz, 2 dB at 35 GHz and 4.2 dB at 50 GHz, respectively, which is about 1 dB lower at 25 GHz and 3 dB lower at 50 GHz. Measured isolation S31 is higher than 30 dB and isolation S41 is higher than 32 dB over the range from dc to 50 GHz. Measured return loss are lower than -15 dB and lower than -10 dB at 25 GHz and 35 GHz, respectively.



(a)



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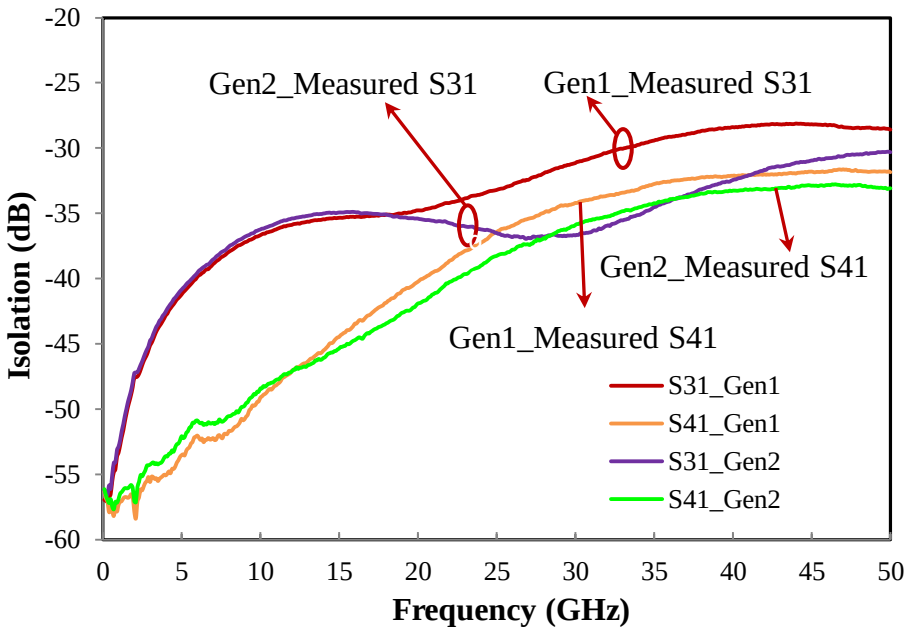
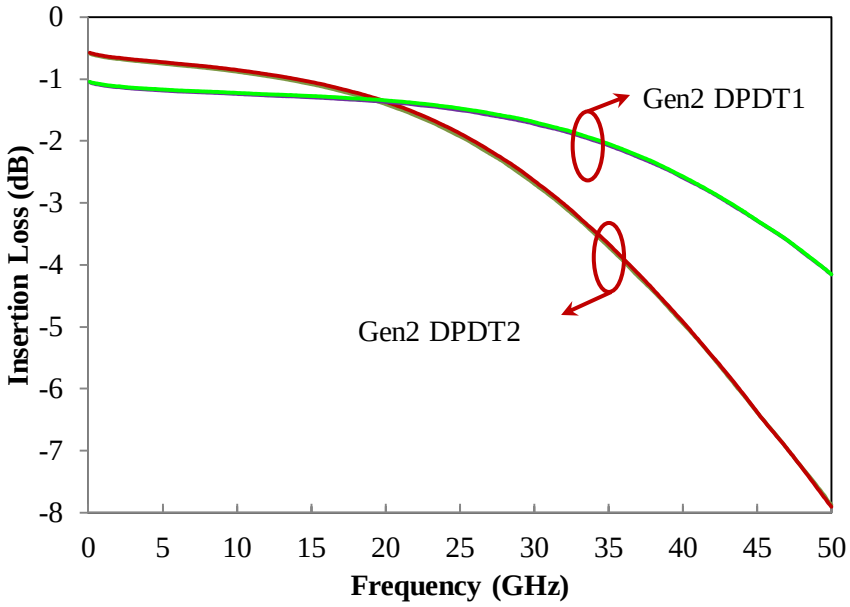


(c)

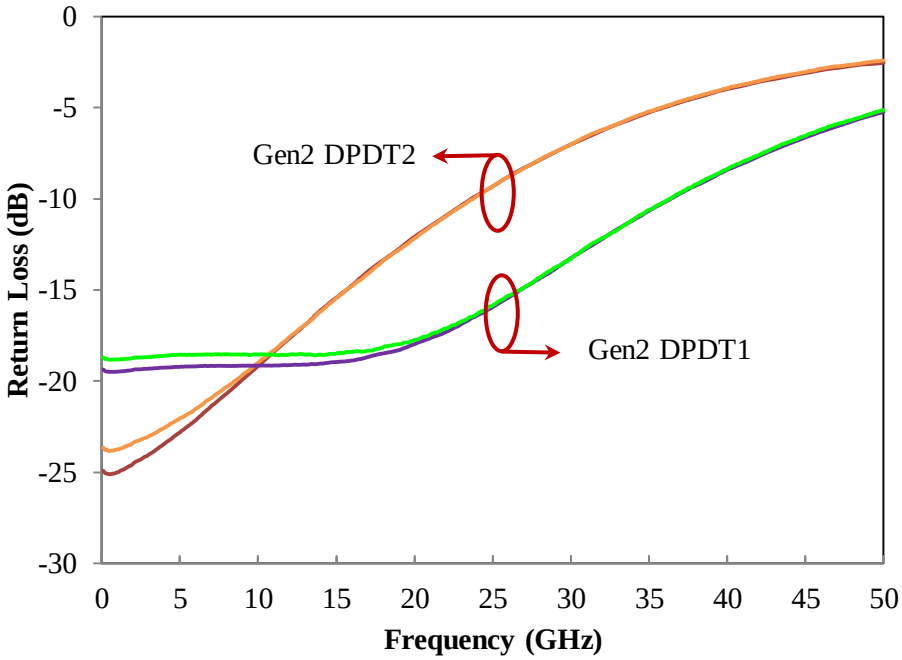
Figure 7-14 Measured results of Gen2 DPDT switches: (a) insertion loss, (b) return loss and (c) isolation

7.4.2 Series transistor width (W) effect

Measured S-parameters of the Gen2 DPDT2 switch (series-shunt-series transistor widths = 150 μm/100 μm/150 μm) with nominal gate length L_g=0.2 μm and the comparison with DPDT1 are presented in Figure 7-15. Similar result to Gen1 switch are observed, in a certain frequency range (dc to 20 GHz for Gen2 switch), DPDT2 switch shows lower insertion loss, while also a little bit lower isolation, so it's a trade-off between application bandwidth and switch performance.



(a)



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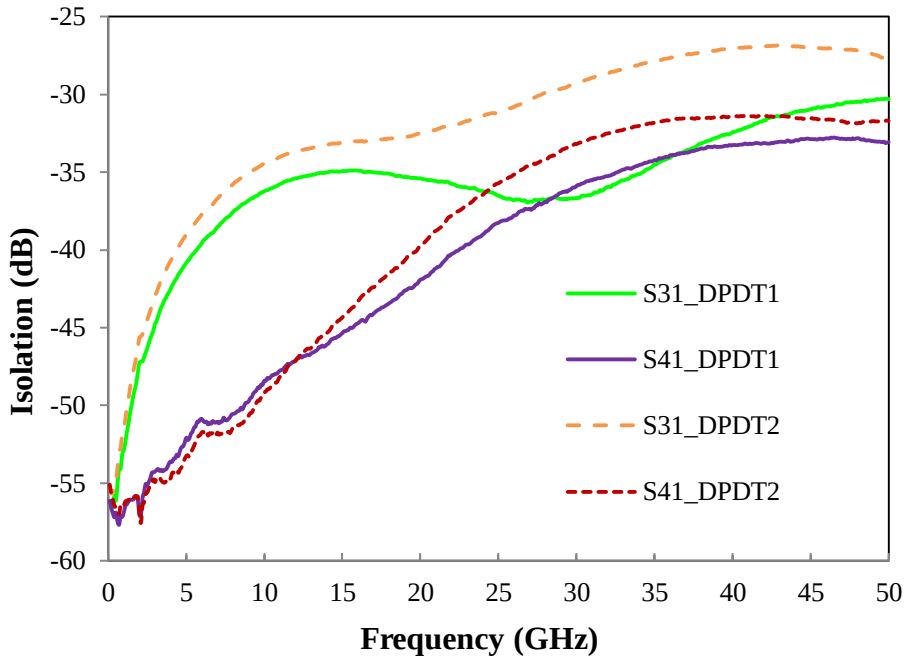
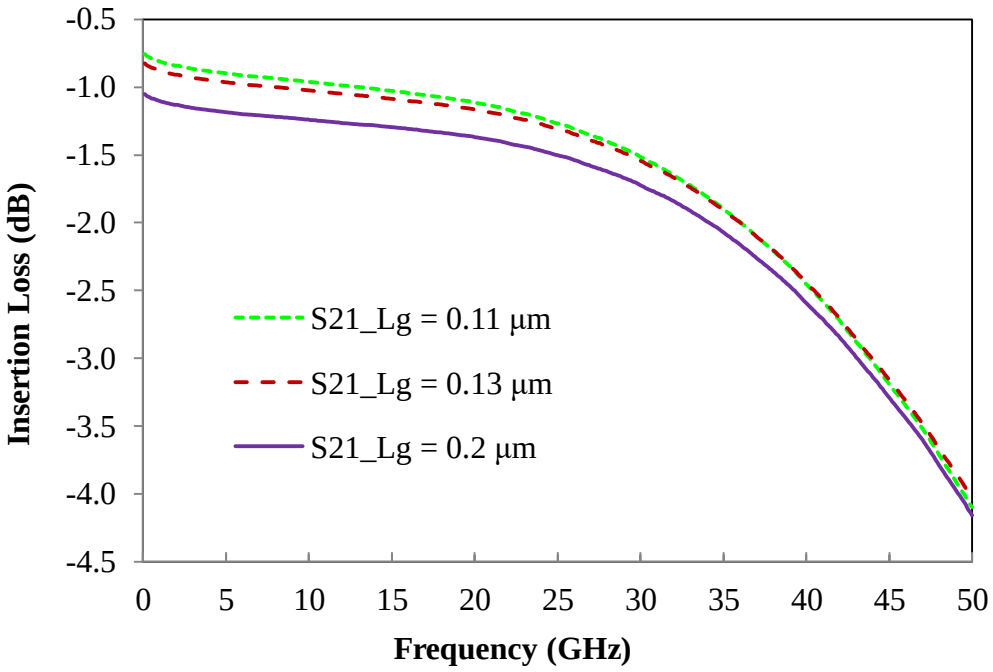


(c)

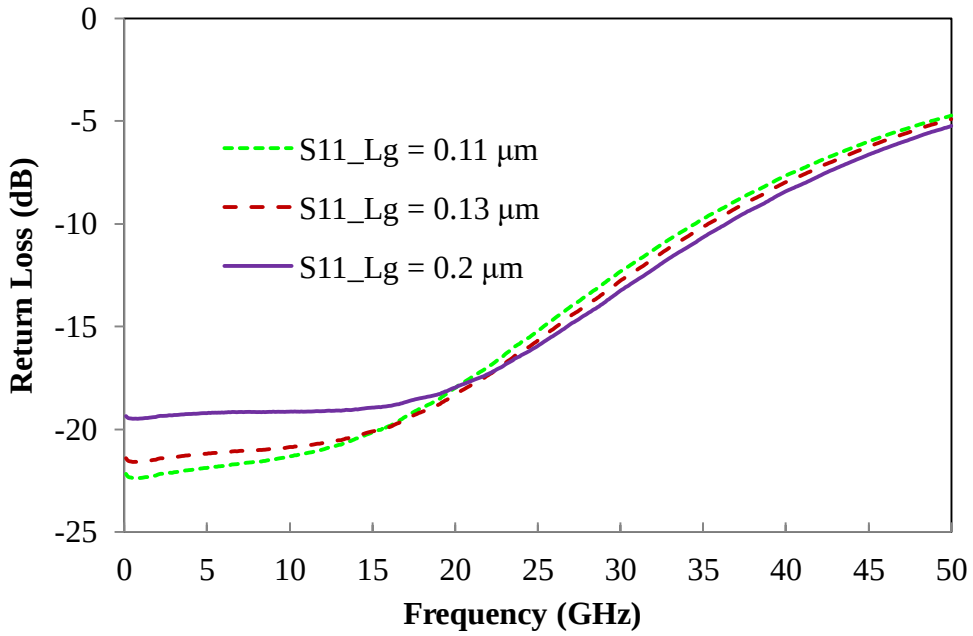
Figure 7-15 Measured results of Gen2 DPDT switches: (a) insertion loss, (b) return loss and (c) isolation of different channel width

7.4.3 Transistor channel length (L) effect

Measured S-parameters of the Gen2 DPDT1 switches with shorter channel length, L_g = 0.11 µm and L_g = 0.13 µm are illustrated in Figure 7-16. Similar to Gen1 switches, switch insertion loss is improved by shortening the channel length, the measured insertion loss S21 of L_g = 0.11 µm are lower than 1.27 dB at 25 GHz, 1.9 dB at 35 GHz and 4.1 dB at 50 GHz, respectively. Measured insertion loss S21 of L_g = 0.13 µm are lower than 1.31 dB at 25 GHz, 1.9 dB at 35 GHz and 4.1 dB at 50 GHz, respectively. Measured isolation S31 and S41 of L_g = 0.11 µm and L_g = 0.13 µm are comparable to L_g = 0.2 µm switch.



(a)



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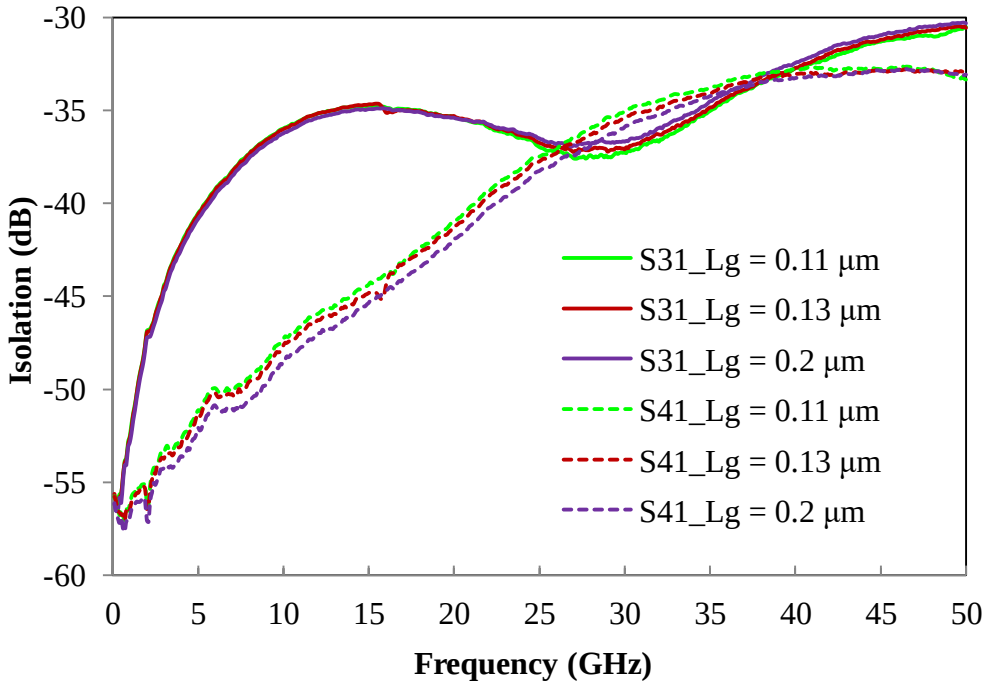
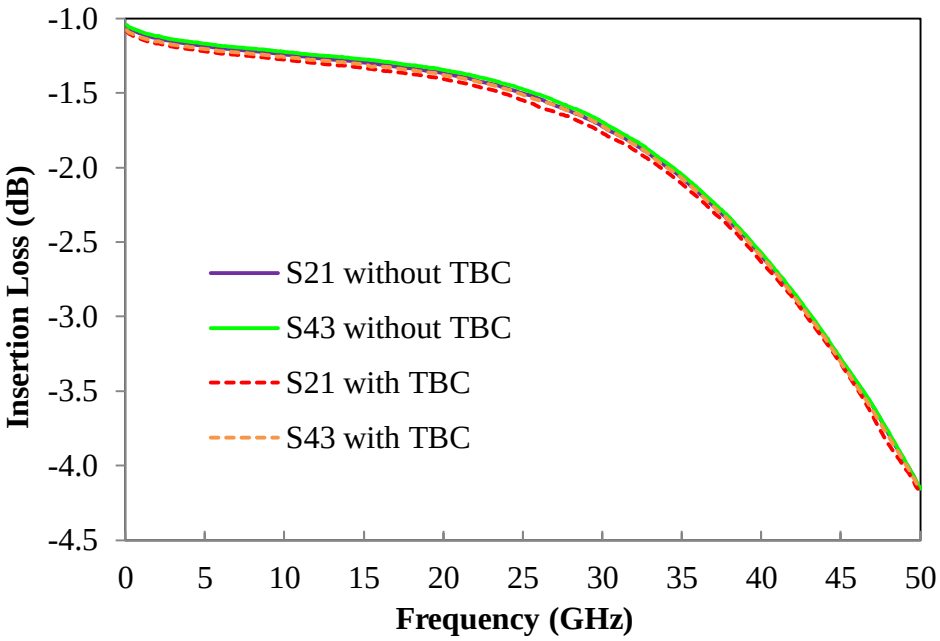


(c)

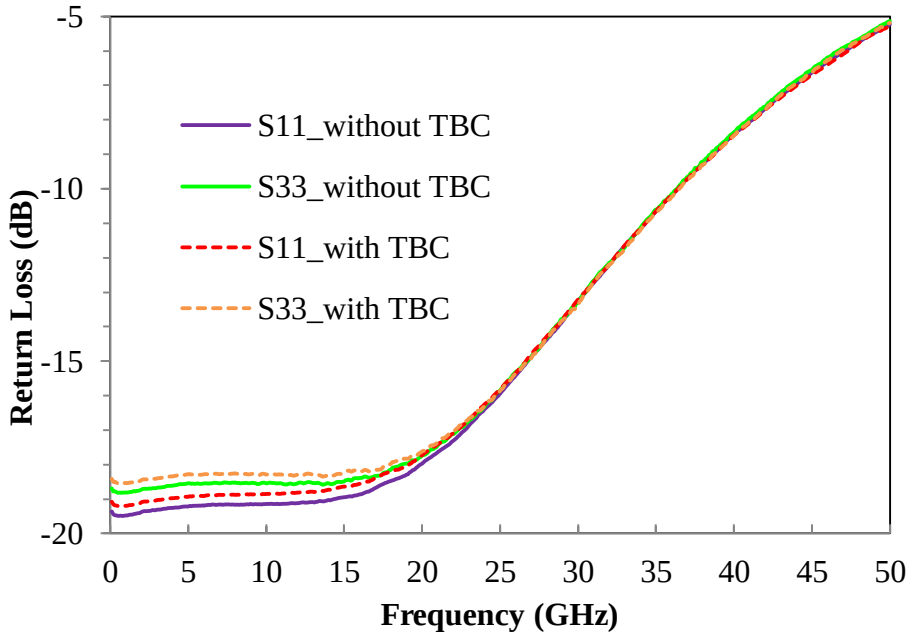
Figure 7-16 Measured results of Gen2 DPDT switches: (a) insertion loss, (b) return loss and (c) isolation of different channel width

7.4.4 TBC connection effect on Gen2 DPDT switch performance

Measured S-parameters of the Gen2 DPDT1 switches with TBC are illustrated in Figure 7-17, performance of switch without TBC are also illustrated for comparison. In general, measured insertion loss, return loss and isolations are comparable between the Gen2 switches with and without TBC connection.



(a)



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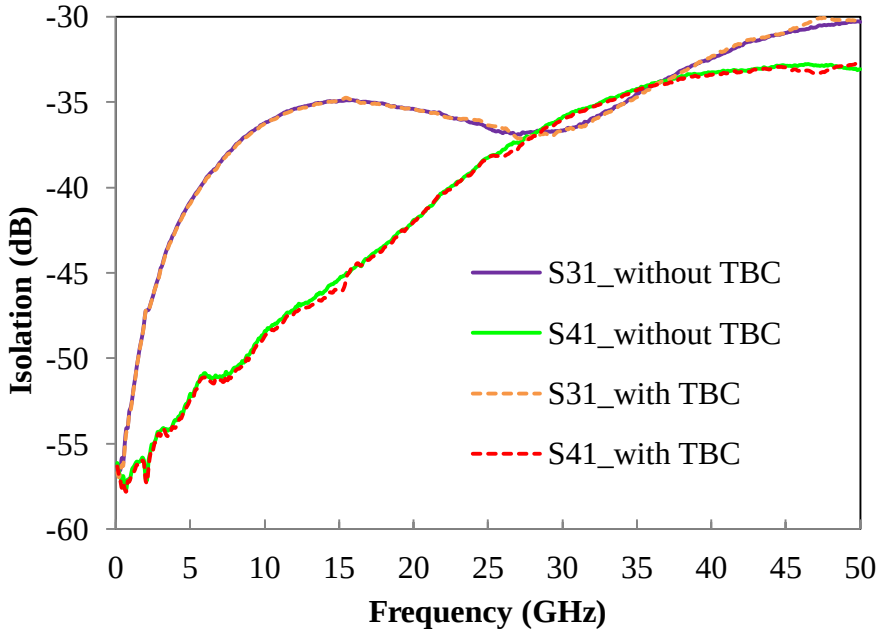


(c)

Figure 7-17 Measured S-parameters of Gen2 DPDT switches with vs. without TBC (L_g = 0.2 μm)

Measured P1dB of Gen2 DPDT1 switches are summarized in Figure 7-18, including both with and without TBC connected switches and both the short channel length switches

(0.11 μm and 0.13 μm). As can be seen, measured P1dB of switches with TBC connected are all higher than switches without TBC for the same channel length. For 0.2 μm channel length, switch with TBC shows about 1.5 dBm higher than non TBC switch, for 0.11 μm and 0.13 μm gate length switches, the difference is about 2-3 dBm. The measured data indicate TBC connection can help improve the Gen2 switch power handling, the reason is Gen2 switch transistor is a negative V_t transistor, which is more prone to be affected by generated n-type plasma charging induced during wafer fabricating when compared to Gen1 switch transistor, which has positive V_t.

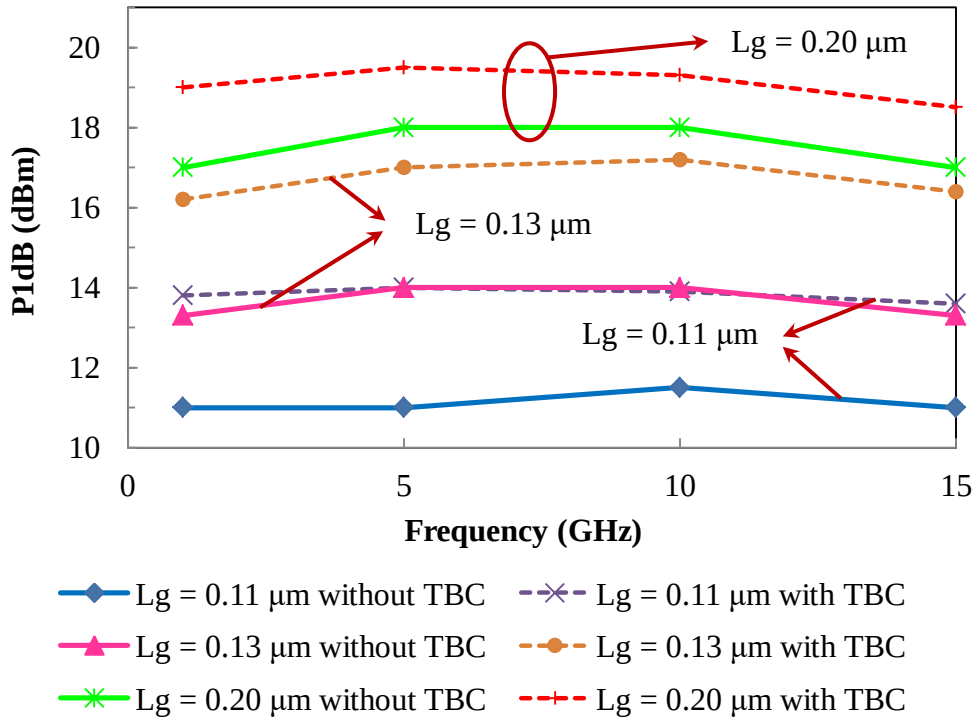
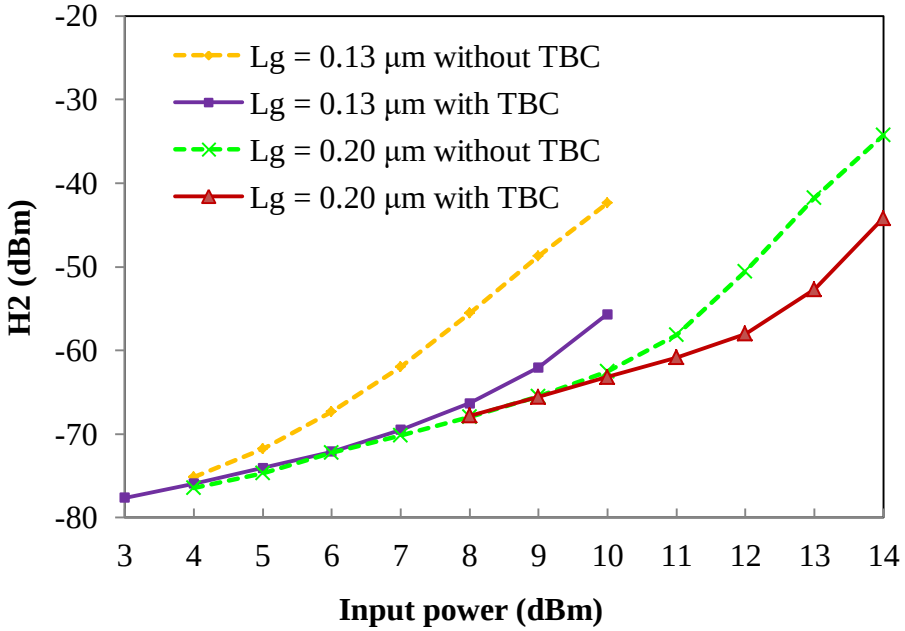


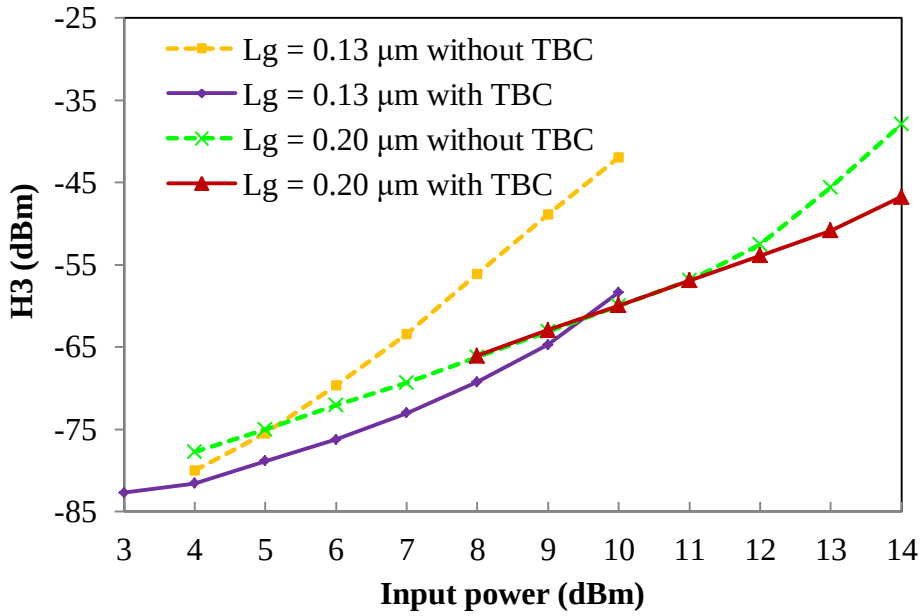
Figure 7-18 Measured P1dB of Gen2 switches (with versus without TBC)

Figure 7-19 illustrate measured 2nd harmonic distortion and 3rd harmonic distortion of 0.2 μm and 0.13 μm Gen2 switches, including both switches with and without TBC connection. Measured H_2 of 0.13 μm switch without TBC starts to rise up even when the input power is as low as 5 dBm, 0.13 μm switch with TBC starts to show non linearity from 7

to 8 dBm input power. For 0.2 µm channel length, H_2 start to rise up at about 11 dBm and 13 dBm for switch without and with TBC connection, respectively. Similar performance was observed from the measured H_3. Better linearity is achieved by increasing the channel length, and TBC connection. As shown in Figure 7-4, TBC helps to discharge the generated n-type charging at the interface of top Si and BOX of Gen2 switch transistor to the trap-rich layer, thus device performance is not shifted from normal behavior, so TBC connection is crucial for Gen2 switch design.



(a)



(b)

Figure 7-19 Measured harmonic distortions of Gen2 switches, a) 2nd harmonic H_2, (b) 3rd harmonic H_3

7.5 Performance summary

In this chapter, high resistivity trap rich SOI based low loss wideband DPDT switches are designed for the first time, the fabricated DPDT switch performance are analyzed. Impact from transistor width (DPDT1 vs. DPDT2), transistor length (0.2 µm vs. 0.13 and 0.11 µm), switch generation (Gen1 vs. Gen2) and switch layout (w/o vs. with TBC) on switch performance are systematically studied.

To summarize, for the legacy Gen1 switch, which is using positive V_t switch transistor and thick SOI top Si thickness, (same as SPDT and SP4T switches presented in Chapter 5 and 6), below results are observed:

1) Wider transistor width (W) switch (DPDT2) provides lower insertion loss in a relatively lower frequency range resulted from lower R_{on}, but narrower bandwidth

due to higher capacitance. Measured P1dB are comparable between DPDT1 and DPDT2. Wider W switch shows better harmonic H_2 (~3 dBm) and H_3 (>13 dBm).

2) Shorter transistor length (L) switches (L_g = 0.11 μm and 0.13 μm) show lower insertion loss and higher isolation in the whole measured frequency range, which is due to both lower R_{on} and C_{off}. Measured P1dB show a relatively weak L dependence. Measured 2nd harmonic H_2 are generally comparable for different L, while 3rd harmonic show strong L dependence (the shorter the better). The measured result indicated that 2nd harmonic distortion can be improved by using wider transistor width, while 3rd harmonic distortion can be improved by using both wider transistor width and shorter transistor channel length in a certain frequency range.

For the innovative Gen2 switch, which is designed with negative V_t switch transistor and a recessed thin top Si thickness, the observations are listed as following:

1) Similar to Gen1 switch, wider transistor width (W) switch (DPDT2) provides lower insertion loss in a relatively lower frequency range resulted from lower R_{on}, but narrower bandwidth due to higher capacitance..
2) Shorter transistor length (L) switches (L_g = 0.11 μm and 0.13 μm) show slightly lower insertion loss and slightly higher isolation in the whole measured frequency range, which is due to both lower R_{on} and C_{off}. Measured P1dB also show strong channel length dependence.
3) Through BOX contact connection did not show significant impact on Gen2 switch S-parameters (small signal measurement). Measured S-parameters are generally comparable between with and without TBC connection. However, P1dB and harmonics are strongly affected by TBC connection. Switches with TBC

connection show 1.5 to 3 dBm higher P1dB than switch without TBC. Switch with TBC also show better H_2 and H_3 harmonics when input power is relatively higher, which also indicate that the maximum power handling capability of Gen2 switches are much improved by TBC connection. This is because Gen2 switches are using negative V_t transistors, which is more sensitive to plasma charging, the source and drain of Gen2 switch transistor are easier to be turned on, as a result, the switch linearity is degraded. So TBC connection is critical for Gen2 switch design.

The performance summary of designed wideband DPDT switches are given in Table 7-3, and are also compared with other state-of-the-art DPDT designs. Compared to state of the arts, the proposed switches achieve widest bandwidth from dc to across millimeter-wave frequency, and exhibit excellent performance including low insertion loss and good isolation while acceptable power handling capability in the frequency range. This DPDT switch only occupies a small chip area of 0.28 x 0.21 mm^2.

Table 7-3 Comparison of Wideband DPDT Switches

	Tech.	**Type**	BW	**IL**	**ISO**	**Input P1dB**	**Chip Size**	**Topology**
			(GHz)	**(dB)**	**(dB)**	**(dBm)**	**(mm^2)**	
[75]	GaAs JFET	2x2	DC-2	< 0.6	> 25	35	0.68 x 0.87	Ring-type
[76]	0.5 µm pHEMT	2x2	DC-6	1.1	> 25	34.5	na	Series only, ring-type
[77]	PIN diode	2x2	3.3-3.8	< 2	80	38.1	na	Shunt only, ring-type
[78]	0.13 µm CMOS	2x2	2-12	1.3 – 2.3	> 40	12	0.84x0.79	series-shunt-series, ring-type with matching networ
This work	**0.13µm SOI Gen1 DPDT1**	**2x2**	**DC-30**	**< 1.4 at 12 GHz < 2.5 at 30 GHz**	**> 32**	**>16 for 0.13µm >18 for 0.2µm**	**0.28 x 0.21**	**series-shunt-series, ring-type, with matching network**
This work	**0.13µm SOI Gen1 DPDT2**	**2x2**	**DC-20**	**< 1.2 at 12 GHz < 2.2 at 20 GHz**	**>30**	**>18**	**0.28 x 0.21**	**series-shunt-series, ring-type, with matching network**
This work	**0.13µm SOI Gen2 DPDT1**	**2x2**	**DC-35**	**< 1.1 at 12 GHz < 2.0 at 35 GHz < 4.1 at 50 GHz**	**> 34**	**>16 for 0.13µm >18 for 0.2µm**	**0.28 x 0.21**	**series-shunt-series, ring-type, with matching network**
This work	**0.13µm SOI Gen2 DPDT2**	**2x2**	**DC-20**	**< 0.9 at 12 GHz < 1.4 at 20 GHz**	**> 32**	**>18**	**0.28 x 0.21**	**series-shunt-series, ring-type, with matching network**

Chapter 8

Conclusion and future works

8.1 Conclusion

The design of ultra wideband RF switches in 0.13 μm RFSOI technology is presented in this work. Motivations and literature reviews of various RF switch designs are presented in the first two chapters.

In Chapter 3, a brief introduction to SOI substrate and technique is presented. The SOI technology has the benefits of lower parasitic capacitance and good isolation which are crucial to wideband RF switch design. The advantage and disadvantage of high resistivity SOI substrate are also presented, as a result, high resistivity trap rich SOI (HR TR SOI) is adopted for this work.

In Chapter 4, different configurations of SPST switch are simulated, including series only, series-shunt without matching network and series-shunt with matching network. Based on simulation result, series-shunt with matching network is proposed for the ultra wideband switch design. Impact of the series transistor size, shun transistor size and the matching inductor value on switch performance are also simulated. The insertion loss and isolation of different switch configurations are also derived based on equivalent “on” and “off” state models. The simulated result can be clearly explained by the derived insertion loss and isolation Equations, proposed SPST branch is used for SPDT and SP4T switch design which presented in Chapter 5 and 6.

In Chapter 5, ultra-wideband SPDT switches are designed in GLOBALFOUNDRIES 0.13-μm HR TR SOI based on SPST simulation result, Si wafers were fabricated with

GLOBALFOUNDRIES 8 inch (200 mm) process. Thorough investigation on the channel mobility (by implementing SMT process), channel length and gate bias effects on switch performance were carried out. It is found that SMT helps improve switch insertion loss from dc to 20 GHz for the proposed SPDT switches by improving the channel mobility and hence reducing the on resistance. Moreover, the different channel length on the same process has prominent effects on the performance of the RF switches. Compared with the state of the arts, the designed SPDT switch achieves the lowest insertion loss (< 1 dB at 30 GHz, < 2.1 dB at 50 GHz) and high isolation >27 dB over dc to 50 GHz.

In Chapter 6, ultra-wideband SP4T switches are designed in GLOBALFOUNDRIES 0.13-μm HR TR SOI for the first time, Si wafers were also fabricated with GLOBALFOUNDRIES 8 inch (200 mm) process. Transistor channel mobility, channel length and gate bias effects on switch performance were also studied. It is found that SMT helps improve switch insertion loss from dc to 35 GHz for the proposed SP4T switches. Similar channel length and gate bias effects as SPDT switches were observed on fabricated SP4T switches. Compared with the state of the arts, the designed SP4T switch achieves the lowest insertion loss (< 1 dB at 10 GHz, < 1.4 dB at 20 GHz and < 2.6 dB at 35 GHz), good isolation (> 36 dB) and acceptable P1dB (> 11dBm) over dc to 35 GHz. The active chip area of the proposed SP4T switch is compact with size of only 0.36 x 0.19 mm^2.

In Chapter 7, ultra-wideband DPDT switches are designed in GLOBALFOUNDRIES 0.13 μm HR TR SOI for the first time, the Si wafer was fabricated with GF 12 inch (300 mm) process. Impact from transistor width (DPDT1 vs. DPDT2), transistor length (0.2 μm versus 0.13 and 0.11 μm), switch generation (legacy Gen1 switch vs. novel Gen2 switch) and switch layout (w/o vs. with TBC connection) on switch performance are systematically studied. Both Gen1 and Gen2 switches show excellent performance in ultra wideband frequency range with

optimized transistor size and layout. Gen1 switches show relatively better linearity and higher power handling capability. Gen2 switches show better insertion loss, higher isolation and wider bandwidth, while relatively worse linearity and lower power handling capability. TBC connection is observed to be crucial to improve Gen2 switch linearity and power handling. This is because when compared to Gen1 switch transistor, Gen2 switch transistor is easier to be affected by plasma charging to induce source drain breakdown. Compared with the state of the arts, the designed Gen1 DPDT switches achieve the lowest insertion loss (< 1.4 dB at 12 GHz, < 2.5 dB at 30 GHz), good isolation (> 30 dB) and good P1dB (> 18dBm) over dc to 30 GHz. The designed Gen2 DPDT switches achieve the lowest insertion loss (< 1.1 dB at 12 GHz, < 2 dB at 35 GHz, < 4.1 dB at 50 GHz), good isolation (> 34 dB) and acceptable P1dB (> 16dBm) and linearity over dc to 35 GHz. The active chip area of the proposed SP4T switch is compact with size of only 0.28 x 0.21 mm^2.

8.2 Future works

Based on the designed SPDT, SP4T and DPDT switch results, and SOI switch R_{on} and C_{off} model, which is shown in Equation (5-1) and (5-2), respectively, several possible future works can be considered.

Firstly, the maximum power handling capability can be increased. This can be done by transistor stacking technique, but transistor size need to be optimized to keep a low insertion loss and high isolation.

Model of SOI switch linearity (especially intermodulation) versus channel length and width need to be further studied.

Secondly, more wideband switches, with more pole and throw numbers can also be designed, like SP6T, SP8T, 4x4 switch matrixes, etc.

Thirdly, different matching network work, including lossless two port network can be tried to further improve switch return loss. In this work, *L-C-L* T matching networks have been adopted for switch design, the return loss at very high frequency is relatively high (> 10 dB when frequency is higher than 30 GHz), which limited the bandwidth.

Fourthly, advanced switch fabrication processes can be adopted to further improve switch R_{on}* C_{off}, including thinning down the SOI top silicon (further reduce top Si thickness based on Gen2 switch), using low-K BEOL dielectrics and implementing air gap process in the BEOL, etc. Both low-K dielectric and air gap techniques (as shown in Figure 8-1) can help to reduce the switch total C_{off}.

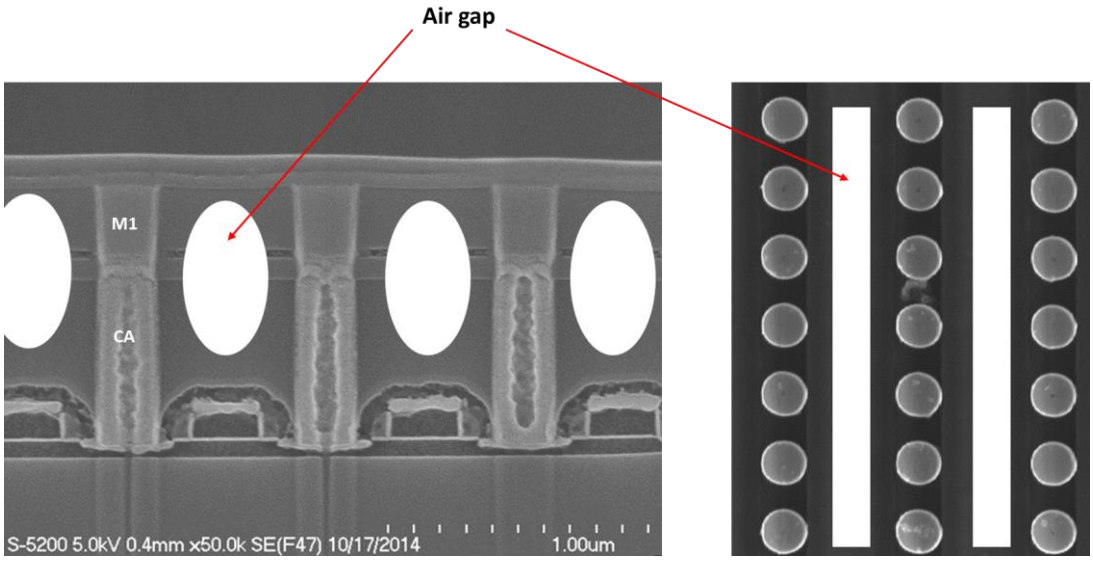


Figure 8-1 Cross-section view of air gap

Finally, with the excellent performance of the proposed ultra wideband switches, high performance of integrated FEM module on trap rich HR SOI can be designed.

PUBLICATIONS

(1) **B. Yu**, K. Ma, F. Meng, K. S. Yeo, P. Shyam, S. Zhang and P. R. Verma, "Ultra Wideband Low Loss Switch Design in High Resistivity Trap-Rich SOI with Enhanced Channel Mobility," in *IEEE Trans. Microw. Theory Techn.*, Year: 2017, Volume: 65, Issue: 10, pp. 3937 - 3949

(2) **B. Yu**, K. Ma, F. Meng, K. S. Yeo, P. Shyam, S. Zhang and P. R. Verma, "DC-30 GHz DPDT Switch Matrix Design in High Resistivity Trap-Rich SOI," in *IEEE Trans. Electron Devices*, Year: 2017, Volume: 64, Issue: 9, pp. 3548 - 3554.

(3) **B. Yu**, K. Ma, K. S. Yeo, F. Meng, S. Zhang, P. R. Verma and W. Yang, "A DC-50 GHz SPDT Switch with Maximum Insertion Loss of 1.9 dB in a Commercial 0.13-μm SOI Technology," *International SoC Design Conference (ISOCC)*, pp. 197-198, Nov. 2015

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