

**CLASS-D AMPLIFIER POWER STAGE WITH PWM
FEEDBACK LOOP**

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Abstract

The introduction of the Class-D power amplifier concept has made a revolutionary impact on today's mobile audio power amplifier industry. This is simply due to its ultra-high power efficiency, which allows longer battery life and smaller heat sinks to be used. The basic open-loop Class-D power amplifier is composed of a pulse modulator, an output power stage, a passive LC low pass filter, and a speaker load. The pulse modulator quantizes the input audio signal into a single-bit high frequency pulse signal. Depending on the implementation of the pulse modulation stage, the Class-D power amplifier can be designed to amplify either analog or digital audio signal efficiently. This is very desirable in the modern trend of audio amplifier market due to the evolutionary development in both digital signal processing as well as the digital storage technology. With digital Class-D amplifier, a fully digital audio amplifier solution is made possible.

Regrettably, the lack of rejection to power supply noise has always been a major drawback for a basic open-loop Class-D power amplifier. Fortunately, negative feedback loop can be implemented in the Analog Class-D power amplifier to mitigate such problem efficiently and effectively. However, such technique is not very efficient for fully digital Class-D implementation due to the circuit complexity. In order to relax the design complexity in digital Class-D solution, an open-loop topology is preferred. The power supply noise can be mitigated by applying a negative feedback loop locally around the output stage.

This thesis proposes a Second-Order direct Pulse Width Modulation (PWM) negative feedback loop for any open-loop PWM Class-D amplifiers with single ended output stage. The proposed design uses GLOBALFOUNDRIES' (GF's) 0.18 μ m CMOS technology. The fabricated chip was measured and it achieves a practical measurement of greater than 80 dB supply noise rejection.

The linearity of the proposed design is reflected by its Total Harmonic Distortion (THD) results which is smaller than 0.04% at a 1 kHz sinusoidal test signal. In addition, a very detailed time domain analysis which quantifies the inherent distortion from the proposed PWM feedback loop is performed.

Chapter 1 Introduction

1.1 Motivation

Thanks to the recent advancement in microelectronic fabrication technology, integrated audio power amplifier solutions for portable devices such as mobile phones and laptop computers are made possible. However, the battery life spans of such devices are rather short due to the limited power resources. Therefore, an ultra-high power efficiency audio amplifier solution is desirable. Audio power amplifiers in Class-D operation mode satisfy the above requirement effortlessly as it offers power efficiency of more than 90%, which is a lot more efficient compared to the traditional linear power amplifiers in Class-AB operation [1]. In addition, the ultra-high power efficiency of Class-D power amplifiers leads to a reduction in the physical form factor of the final products by making the requirement of heat sink unnecessary [1, 2].

Conventional open-loop analog Class-D amplifiers usually consist of a pulse modulation circuit, a CMOS output stage and a low pass filter (LPF) [1-3]. The pulse modulator modulates the input audio band signal into a series of high frequency pulses. Depending on the types of pulse modulation, the typical pulse switching frequency for the most efficient type of pulse modulation scheme is approximately 400 kHz. The output stage then increases the driving strength of the pulse signal to a level that is sufficient to drive the low impedance speaker load. In most of the cases, the amplified switching

pulse signal are required to be demodulated, so that the amplified audio signal can be recovered. To accomplish the task, a simple second-order LC (Inductor and Capacitor) LPF with cut-off frequency slightly higher than the maximum audio band frequency is used. The LC LPF recovers the amplified audio band signal by rejecting the high frequency carrier from the amplified pulses, and allowing only the audio frequency contents to be delivered to the load.

Although such architecture had greatly influenced the development of the audio power amplifier industry due to its advantages of having a simple structure, higher power efficiency, and smaller form factors; there are still some challenges faced by Class-D amplifiers for their adoption in the commercial audio power amplifier market. One of which is related to the revolutionary development of the data storage industry. The successful transformation of analog data storage world into a digital one has imposed a new requirement on the audio power amplifiers market. In fact, such requirement has greatly influenced the way the audio amplifier works. Figure 1 depicts the application of an Analog Class-D amplifier with digitally coded audio input source. A digital-to-analog conversion process is needed prior to the pulse modulation in the analog Class-D amplifier operation. The overall power efficiency and the output audio signal quality are always limited by this power hungry digital-to-analog conversion process [4, 5]. To overcome such constraint, the digital-to-analog conversion requirement in the amplification chain must be completely eliminated. This can only be done if the audio power amplifier is a fully digital one which can amplify digitally coded audio signal directly [5-11]. Figure 2 depicts a principle diagram of an audio power amplification system which employs a Digital Class-D amplifier to take in the digital signal directly from the Digital Signal Processor (DSP). In fact, recent researches have proven this concept and some of which had shown promising results in terms of output signal linearity [12-20].

The major drawback in such a simple Class-D amplifiers structure in Figure 2 is the lack of rejection to switching artefacts and power supply ripple (PSR) in the power switching stage [4, 21-25] as illustrated in Figure 3. For analog Class-D amplifiers, most solutions focus on mitigating such problem by applying negative feedback from the output of the amplifier to its pulse modulation stage [7, 26-36] as depicted in Figure 4. However, such technique can never be a cost-effective solution for digital Class-D amplifiers. This is because an Analog-to-Digital Converter (ADC) is required to convert the analog output signal into digital form before feeding back to the digital pulse modulation stage. This is very different from Analog Class-D amplifiers where both the input and output signals are analog signal. Hence, an open loop topology is preferred in most digital Class-D amplifier audio systems. To mitigate the output signal quality degradation caused by the power supply ripple noise, a bridge tied load (full-bridge) topology for the output stage can be employed. In this way, the ripples at the two outputs become common-mode signals, thus, achieving better power supply ripple rejection (PSRR) performance [37].

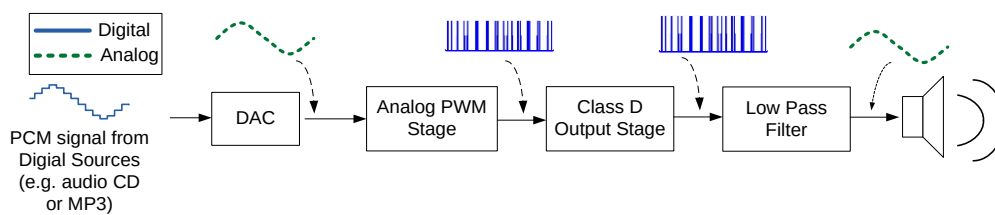


Figure 1. Analog Class-D amplifier in a conventional audio amplification system

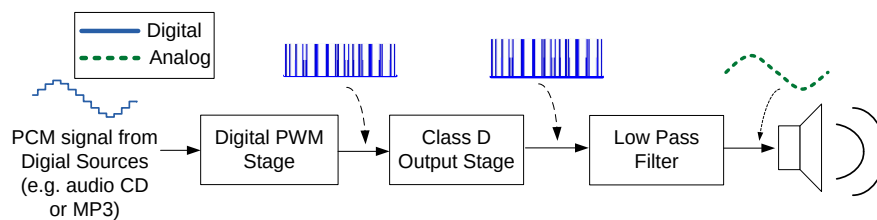


Figure 2. An open-loop Digital Class-D amplifier

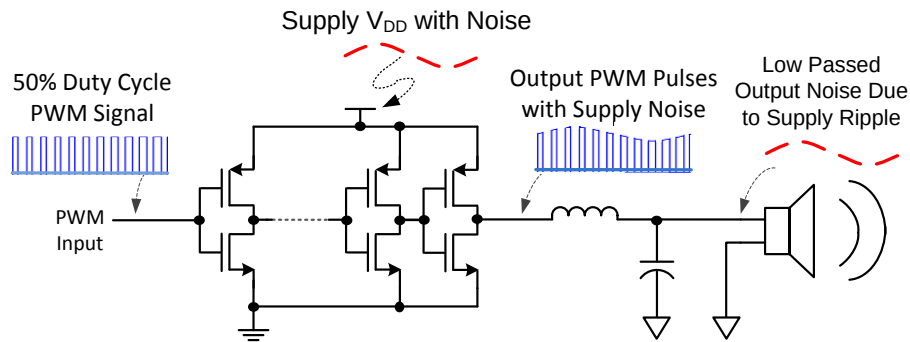


Figure 3. Effects of Supply noise on open loop Class-D output stage

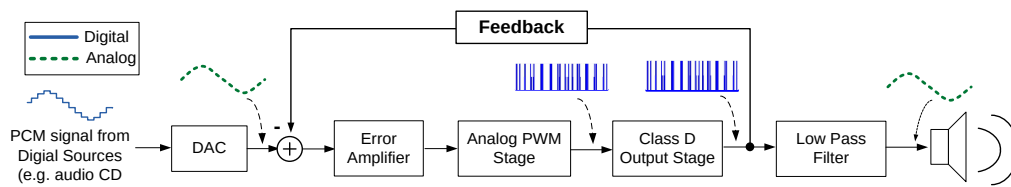


Figure 4. Typical Analog Class-D amplifier with negative feedback

Nevertheless, full bridge Class-D amplifier topology normally consumes huge silicon real estate as the sizes of the output switching devices are relatively large. In addition, it requires complementary or differential driving signals to be developed across the speaker load. Hence, half bridge Class-D amplifier topology would be more attractive in some applications where the form factor of the final product is of major concern, and also, in applications where physical hardware requirements limit the possibility of differential output signal to be developed across the load (i.e. Stereo headphone connectors). However, half bridge Class-D amplifier topology normally results in higher distortion level than its full bridge counterpart. Moreover, the intrinsic PSRR for a basic half bridge Class-D amplifier power stage is found to be only 6dB [21, 23, 25]. This is very undesirable in most of the audio amplifier systems. To address the PSRR and the output signal linearity (in terms of THD)

problems in an open-loop Digital Class-D amplifier, a PWM input Class-D output stage with feedback correction is proposed in this project.

Figure 5 depicts the conceptual block diagram of a Digital Class-D amplifier system with a local PWM negative feedback loop around the power stage to improve both its linearity and rejection to supply noise.

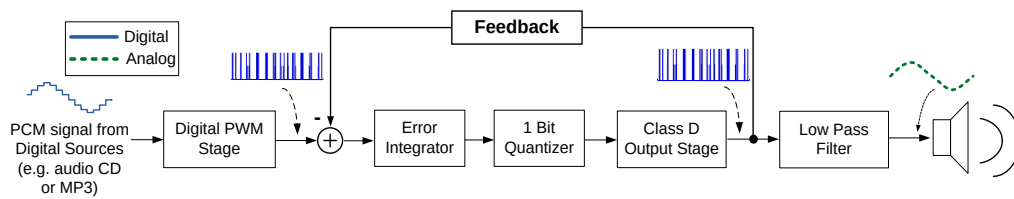


Figure 5. A Digital Class-D amplifier system embodying the proposed Class-D output stage

1.2 Objective

The objectives of this project are as follows:

- i. To design a PWM negative feedback loop for any open-loop Class-D amplifiers to improve its linearity and error suppression capability. To be specific, the proposed design should provide high PSRR and low THD performance.
- ii. To investigate on the parameters affecting the linearity of the proposed supply noise rejection circuit for PWM Class-D amplifier.

In this thesis, a second-order PWM-in and PWM-out negative feedback circuit is presented. The proposed negative feedback loop is an ideal solution to improve the rejection for both the power supply noise and the output signal non-linearities of any open-loop PWM Class-D switching amplifiers. The proposed negative feedback circuit consist of a second-order continuous-time (CT) integrator and a Schmitt trigger comparator. The second-order CT integrator is realized with a single operational amplifier. The solution is efficient, elegant and easy to implement as compared to other reported designs described in Chapter 2 of this thesis.

1.3 Organization of the Dissertation

The rest of this dissertation is organized as follows. A brief literature reviews on the followings are covered in Chapter 2.

- i) a brief review on the four basic classes of linear amplifier,
- ii) analog and digital Class-D switching amplifier and its common error sources,
- iii) the reported techniques to improve the linearity as well as the power supply rejection for Class-D amplifier.

Chapter 3 of this thesis describes the proposed direct PWM feedback loop. In this chapter, the direct PWM feedback loop is analysed in frequency domain to ensure its stability across the whole frequency range. Both the analysis and measured results reveal that the proposed design can effectively mitigate the power supply error without introducing much linearity problems to the output audio signal.

A detailed mathematical analysis on the proposed PWM-in and PWM-out negative feedback circuit for Class-D audio power amplifier is given in Chapter 4. The detailed approach in formulating and solving the differential equations based on the correction signals of the proposed design in different time interval within one PWM cycle is described.

Lastly, the conclusions and future works are described in Chapter 5.

Chapter 2 Literature Review

2.1 Overview of Audio Amplifier

An audio power amplifier refers to any amplifiers that amplify signals (such as music or speech) that are within the typical audible signal frequency band of 20 Hz to 20 kHz [38, 39]. Its primary function is to boost the power of its input signal so that it is sufficient to drive a relatively low impedance passive load, such as an audio speaker [38, 40]. Therefore, the output impedance of any power amplifier output stage must be designed to be sufficiently low. This is to ensure that the signal power can be delivered to the load with minimum loss in gain and output signal linearity. In general, the linearity of the amplifier output signal is measured in terms of its THD [41].

Apart from its output signal linearity requirement, another major concern in designing an amplifier output stage is its power efficiency [42]. The output stage of the power amplifier must deliver the required signal power to the load efficiently. Put differently, the power consumed by the output power transistors must be kept as low as possible. This is particularly important especially in portable devices where the power resources are limited. Besides, the power dissipated in the power transistors is transformed into thermal energy that might permanently damage the output devices. Thus, it imposed a requirement for the use of heat sinks to conduct the heat energy away from

the output transistor. Consequently, the overall bill of material cost and the size of the end product would be increased.

2.2 The Evolution of Audio Amplifier

The history of audio amplifier begins with the invention of audion vacuum tube by Lee De Forest in 1906 [43]. The audion vacuum tube consists of three terminals, namely an anode terminal, a cathode terminal, and a control terminal. Thus, it is also known as triode vacuum tube. The amount of current that flows across the anode and cathode of the audion vacuum tube depends on an electromagnetic signal that is applied at the control electrode. Apart from being used as an AC to DC signal rectifier, the triode vacuum tube can also be used as an amplifier for electromagnetic radiation [43]. In fact, the audion vacuum tubes were widely found in most amplifiers back in the vacuum tube era [39].

In the late 1960s, the commercial introduction of solid-state transistors had successfully transformed the audio amplifier market from the dominated tube-based audio amplifier into a solid-state one [39]. Solid-state or transistors-based amplifiers are relatively inexpensive compared to its tube-based counterpart. Thanks to the advancement of solid-state technology, millions of transistors can be fabricated onto a single tiny chip and making integrated audio amplifier solution possible. The evolution of solid-state technology had thus unveiled a relatively inexpensive and more portable audio amplifier market in that time. However, the unblemished audio quality offered by tube-based audio amplifiers is still attractive to some audio enthusiasts who demand flawless quality music for their auditory enjoyment. In fact, much

research efforts had been spent on narrowing such audio quality gap between the tube-based audio amplifiers and the transistors-based one.

Most audio amplifiers in the earlier stage of the transistor-based amplifier development are linear amplifier. These includes the four basic classes of amplifier namely, Class-A, Class-B, Class-AB, and Class-C amplifier. Each class of amplifiers has their own advantages in terms of linearity and power efficiency. With a reasonably good balance between linearity and power efficiency, Class-AB amplifier had soon become the dominant choice in the transistors-based linear audio amplifier market.

In today's context, the demand for device portability, and high power efficiency had driven the focus of audio amplifier market to Class-D amplifiers. This is mainly due to its simplistic structure, compactness in physical size and the ultra-low power dissipation by the output switching devices. In addition, the mature development of digital data storage technology, and the growth of digital signal processing in the audio market have demanded a fully digital audio amplifier solution [4]. In consideration of the above, Digital Class-D amplifiers become an ideal solution for fully digital audio amplification system due to the digital nature of the switching pulses within the Class-D amplification process.

2.3 Common Classes of Linear Audio Amplifiers

As mentioned in the previous section, the output power efficiency is one of the most important aspects when designing an audio amplifier. The

power efficiency of linear power amplifiers depends very heavily on the percentage of time the output transistors conduct (i.e. conduction angle). In fact, linear amplifiers are conventionally classified based on the biasing condition, and thus, the conduction angle of the output transistors. Put differently, the conduction angle of the power transistors for any arbitrary sinusoidal input waveforms determines which classification [44] the amplifier belongs to. The four typical classes of power amplifiers are Class-A, Class-B, Class-AB, and Class-C.

2.3.1 Class-A Power Amplifier

Figure 6 depicts the simplest form of Class-A amplifier with a single-ended output transistor and a resistive load. It is well-known that amplifiers in Class-A operation are highly linear amplifier. In fact, it is the most linear class of amplifier with the lowest output signal distortion [44, 45]. This is achieved by biasing its output power transistor with a quiescent current to allow for full signal cycle conduction. In order to have full output swing operation, the biasing point of the output transistor is normally chosen to be at the mid-point of the power supply rails. In other words, power is dissipated by its output transistors throughout the entire output signal cycle [39, 44]. Thus, the overall power efficiency is expected to be very low. Theoretically, its maximum power efficiency is around 25% [44, 46-48]. In practice, the actual power efficiency is even lower. The output transistor dissipates the wasted power in the form of heat even when there is no signal applied to its input. Consequently, large heat sinks are normally required to channel the heat energy away from the output transistors in order to avoid permanent damage to the output transistors in the Class-A amplifier.

Nonetheless, Class-A amplifier is still an attractive solution to application where linearity is the uttermost concern compared to the power efficiency as well as the physical device size.

Fortunately, the maximum power efficiency of Class-A amplifiers can be theoretically boosted to 50%. This is done by using either inductively-coupled or transformer-coupled load as depicted in Figure 7 [47, 49]. However, the bulkiness of the inductors and the transformers becomes the major drawback of such amplifiers in most of the portable audio amplifier solutions.

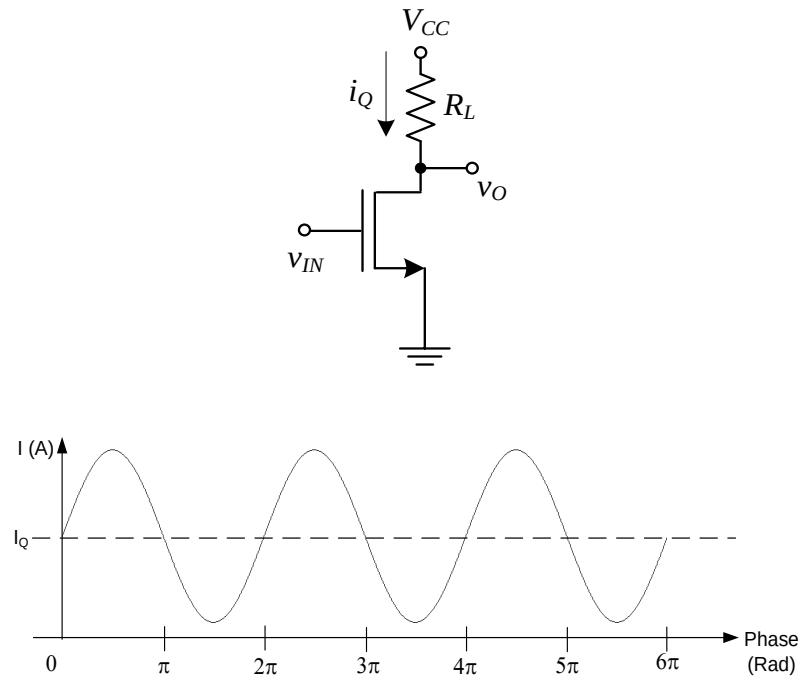


Figure 6. Schematics and conduction current versus time characteristic of Class-A amplifier

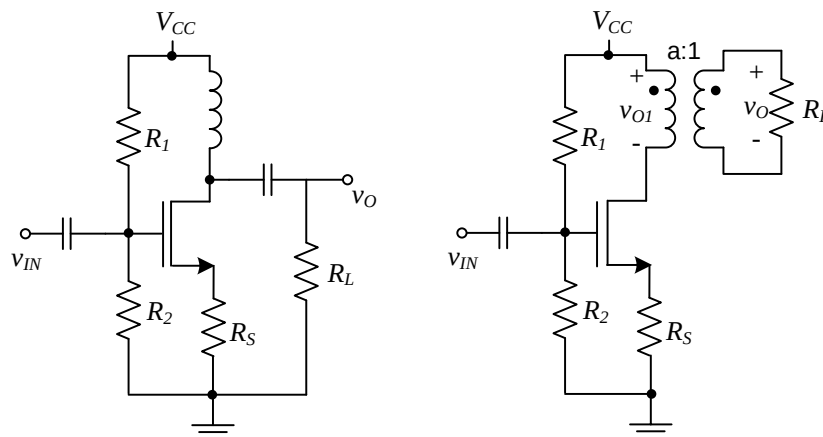


Figure 7. Schematics of Class-A amplifier a) inductively coupled, b) transformer coupled

2.3.2 Class-B Power Amplifier

Unlike Class-A amplifier, no DC biasing current are required to bias the output power transistor in Class-B amplifier operation. Figure 8 depicts a schematic and conduction current characteristic of typical Class-B amplifiers. For any arbitrary sinusoidal input signal, the output power transistor in Class-B operation conducts only for half of the signal cycle. In other words, the conduction angle for Class-B amplifier is around 180 degrees [39, 49]. Therefore, such amplifiers normally require two complementary power transistors to be configured as a “push-pull” structure to allow for full output signal swing. In which, the output power transistors alternatively conduct for the positive and negative half of the input signal. Effectively, it brings up the advantage of Class-B power amplifiers that no power is being dissipated in the output power transistor that is not conducting. Therefore, its overall power dissipation is dramatically reduced as compared to that in the Class-A amplifier.

Theoretically, the maximum achievable power efficiency for Class-B power amplifier is 78.5% [47, 48, 50]. This is significantly higher than the maximum power efficiency that can be offered by Class-A amplifier.

Unfortunately, the biggest problem with Class-B amplifier is that its resulting amplified output signal often suffers from a phenomenon known as crossover distortion [50, 51]. This phenomenon produces a zero voltage “dead zone” on the output signal as depicted in Figure 9. Such distortion occurs when the output signal crosses over from the positive half of the waveform to the negative half. During this transition time, the input voltage is less than the turning-on voltage of the output transistors. Therefore, neither of the output transistors in the push-pull configuration conducts. As a result, nonlinearities are introduced to its output signal [48, 52].

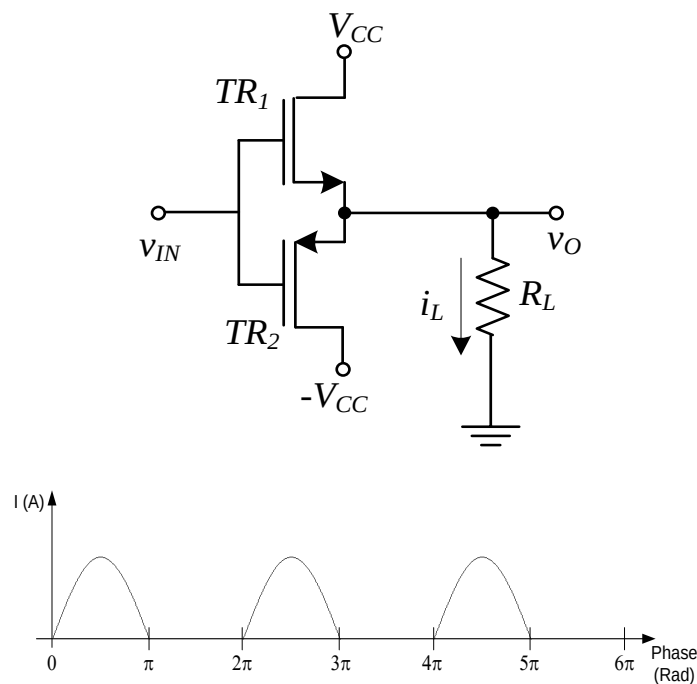


Figure 8. Schematics and conduction current versus time characteristic of Class-B amplifier

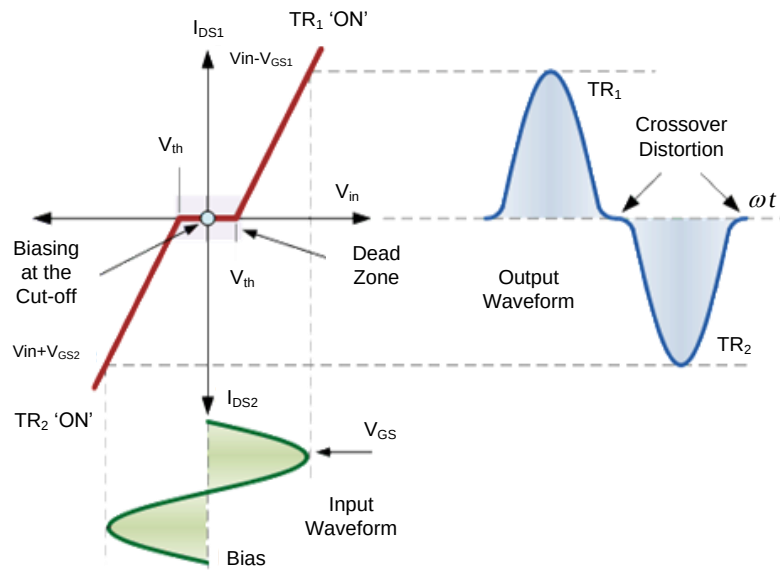


Figure 9. Crossover distortion of basic complementary push-pull output stage.

http://www.electronics-tutorials.ws/amplifier/amp_7.html

2.3.3 Class-AB Power Amplifier

To mitigate the crossover distortion, the output transistors can be biased with a small quiescent current. Consequently, the output transistor is operating at a voltage that is marginally above its turning-on voltage. Thus, the output transistor conducts for slightly more than half of the signal cycle. Such amplifier operation is classified as Class-AB operation [52, 53] as shown in Figure 10. Similar to Class-B amplifier, conventional Class-AB amplifier requires two output transistors to be configured as a “Push-Pull” structure for full voltage swing amplification. The Class-AB operating condition is basically a trade-off of the linearity of Class-A amplifier and the power efficiency of its Class-B counterpart [51]. The small quiescent current in Class-AB amplifier flows through its output transistors even when there is no input signal. Thus,

the average power dissipated in each transistor is slightly higher than that in the Class-B amplifier. However, the extra power dissipated by the output transistors due to the small quiescent current is relatively insignificant as compared to that in the Class-A amplifier configuration. The advantage of mitigating the crossover distortion prevails over the slight disadvantage of power efficiency degradation. Therefore, Class-AB amplifiers are widely used in applications where a good compromise of distortion and power-efficiency is required. In fact, push-pull Class-AB amplifiers were very popular in linear audio amplifier applications in the last century, because of its relatively high linearity performance and power efficiency.

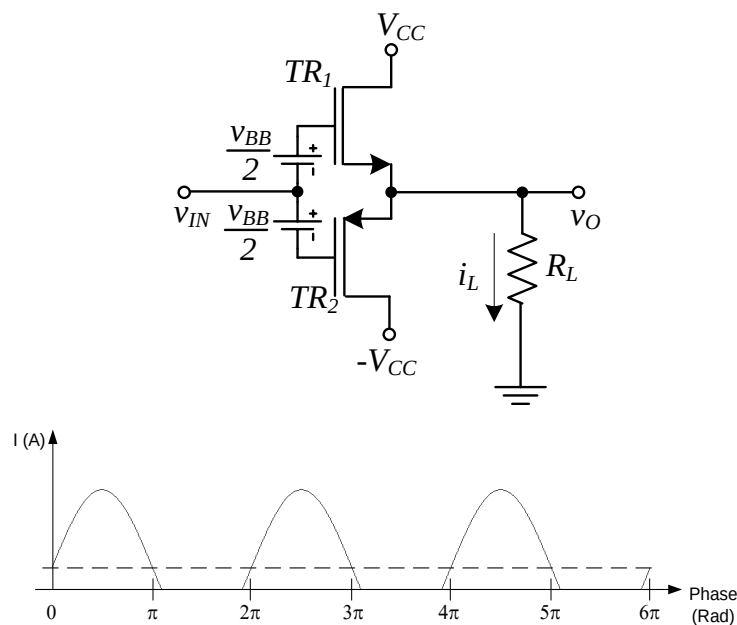


Figure 10. Schematics and conduction current versus time characteristic of Class-AB amplifier

2.3.4 Class-C Power Amplifier

In Class-C amplifier operation as depicted in Figure 11, the output transistor is slightly reverse-biased at quiescent point. Thus, it conducts for less than half of the signal cycle [38, 54, 55]. Put differently, the output transistor conducts only when the input signal is sufficiently high during the positive half-cycle of the signal. Thus, the resulting power efficiency is even greater than that offers by the Class-B amplifier (78.5%). However, the application of such amplifiers in audio amplifier industry is rather limited. This is due to its high input-to-output nonlinearity [38]. In addition, a relatively high-Q resonant output tank circuit is often required to restore the sine wave cycle during the non-conducting portion of the input waveform [54, 55]. These amplifiers are commonly used in radio-frequency (RF) circuits and is also called ‘tuned’ amplifier [38, 54, 55]. In conclusion, such amplifiers are generally not suitable for audio application due to its poor linearity performance.

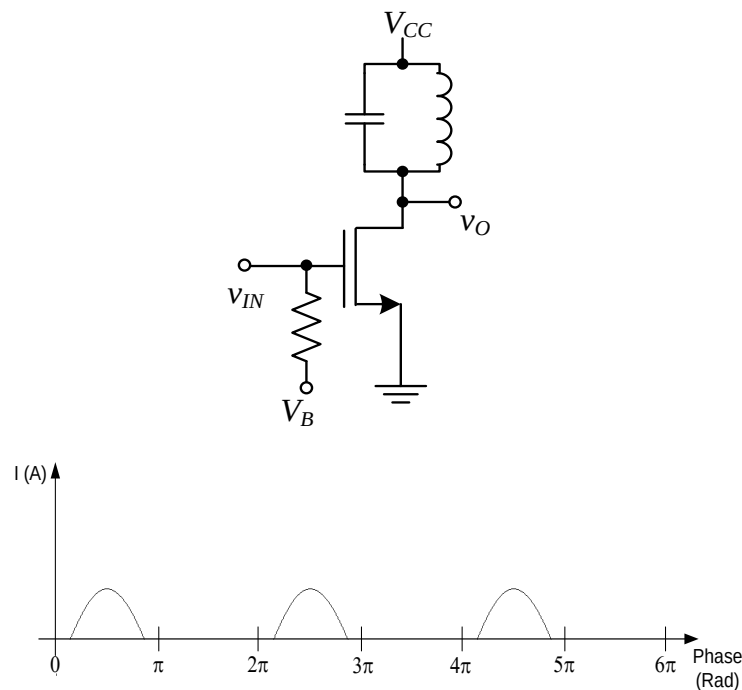


Figure 11. Schematics and conduction current versus time characteristic of Class-C amplifier

2.4 Class-D Power Amplifier

A Class-D audio amplifier or switching amplifier is a non-linear amplifier which can provide very high power efficiency. Thanks to the relatively high frequency switching operation that alternately turning the output power transistors into either fully on or fully off state, the amount of power dissipated in these switching transistors is significantly reduced [1]. Therefore, it is possible for a Class-D amplifier system to achieve power efficiencies of more than 90% [56]. Figure 12 shows the power efficiency curve for a typical Class-D amplifier and Class-AB amplifier over a full dynamic range [57]. From this power efficiency curves, it can be observed that the linear Class-AB amplifier can only exhibit a maximum power efficiency of not more than 60% at full signal swing. The Class-D amplifiers, on the other hand, has a more superior power efficiency performance compared to the Class-AB amplifier throughout the full dynamic range [57].

Despite its remarkably high power efficiency performance, Class-D amplifier does have some shortcomings. The major drawback of Class-D amplifiers is the increased circuit complexity as compared to the traditional linear Class-AB amplifiers. As mentioned in the previous chapter, a typical Class-D amplifier consists of three essential elements which include a pulse modulation circuit, a CMOS output stage and a low pass filter. Depending on its pulse modulation circuit, a Class-D amplifier can be implemented by either digital or analog means. Both the analog and digital open-loop Class-D amplifiers share a common basic architecture as depicted in

Figure 13 [1, 2, 12, 58]. The input audio signal is first being modulated to a high frequency pulse signal in the pulse modulation stage. Subsequently, this high frequency pulse train is amplified by the Class-D output power stage.

The simplest type of Class-D amplifier output power stage usually consists of a P- and N- MOSFET power transistors which operate in either the triode (fully on) or cut-off (fully off) region. In other words, there is no in-between analog state during the Class-D amplifier operation. Therefore, such power stage can achieve much higher power efficiency than any other linear analog power stages. This is because the power dissipated by the output transistors in these operating regions is very small (very small for the triode region and almost zero for the cut-off region). Lastly, the amplified audio signal can be recovered by removing the high frequency carrier of the amplified pulses by a LPF. The 3dB bandwidth of the LPF is normally designed to be slightly above the highest frequency in the audio band (30 kHz to 60 kHz). Conventionally, a simple second-order L-C low pass filter with a butter-worth response and a roll off rate of -40 dB/decade is adopted to attenuate the high frequency carrier of the PWM signal. Thus, the amplified audio information is obtained.

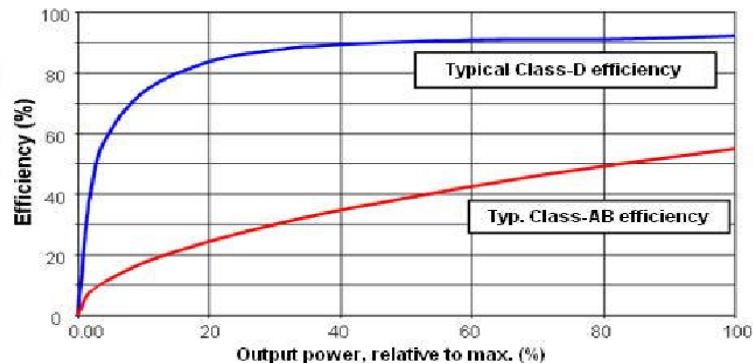


Figure 12. Comparison of typical practical efficiency for Class-D and Class-AB amplifier (Graph extracted from [57])

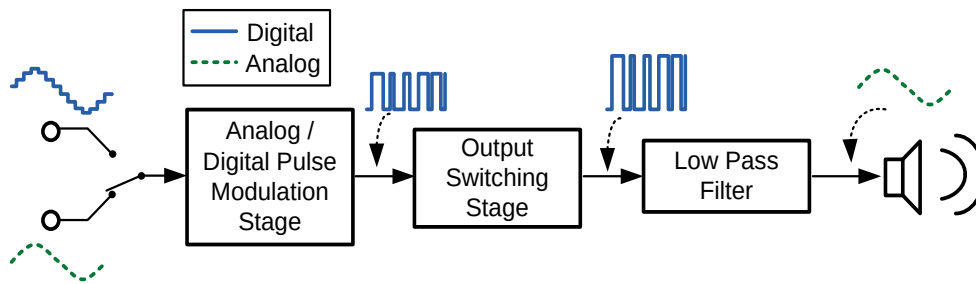


Figure 13. Functional block diagram of open-Loop Class-D amplifier

2.4.1 Pulse Width Modulation (PWM)

There are four basic types of pulse modulation scheme that are suitable for Class-D amplifiers operation, namely, Pulse Width Modulation (PWM), Pulse Density Modulation (PDM), Bang Bang Control Modulation, and the Sliding Mode Control Modulation. Amongst these four, PWM is the most direct and theoretically linear pulse modulation method [24, 25, 37]. It was proven in [59] mathematically using Fourier analysis that PWM signal generally does not add any harmonic distortion into the baseband modulating signal. In fact, [60] had further analysed the harmonic distortion behaviour of PWM Class-D amplifiers using differential equations. Thus, PWM modulation method is being used to produce the high frequency pulse signal for any Class-D amplifiers discussed in this thesis unless otherwise have specified.

Pulse width modulation (PWM) is a modulation scheme that converts a signal into a series of periodic pulses where the pulse width of each PWM pulse period is a function of the input modulating signal. Typically, a PWM signal can be easily generated by comparing the input modulating signal with a triangular carrier as depicted in Figure 14. Despite the highly non-linear nature of the PWM process, its low frequency non-linearity can be greatly suppressed if the carrier frequency is sufficiently greater than the maximum frequency of the audio signal [61]. The average value of the pulses is equivalent to the

corresponding modulating signal at a particular instance [59, 62]. The input signal can be easily recovered with the use of a LPF.

The average power of a typical PWM signal is proportional to its duty cycle. The average value of the PWM waveform in one cycle is:

$$V_{avg} = \frac{1}{T} \int_0^T f(t) dt \quad (1)$$

where - T is the PWM pulse period and

$f(t)$ is a square wave with a high state value of V_{max} for the time interval between $0 < t < (D \times T)$ and a low state value of V_{min} for the time interval $(D \times T) < t < T$,

D is the duty cycle of the square pulse.

By substituting the above conditions into (1), the expression for the average value of PWM waveform in one cycle is:

$$\begin{aligned} V_{avg} &= \frac{1}{T} \left(\int_0^{DT} V_{max} dt + \int_{DT}^T V_{min} dt \right) \\ V_{avg} &= D \cdot T \cdot V_{max} + T(1 - D)V_{min} \\ V_{avg} &= (D)V_{max} + (1 - D)V_{min} \end{aligned} \quad (2)$$

From (2), it can be seen that V_{avg} is directly dependent on the duty cycle D of the square pulses.

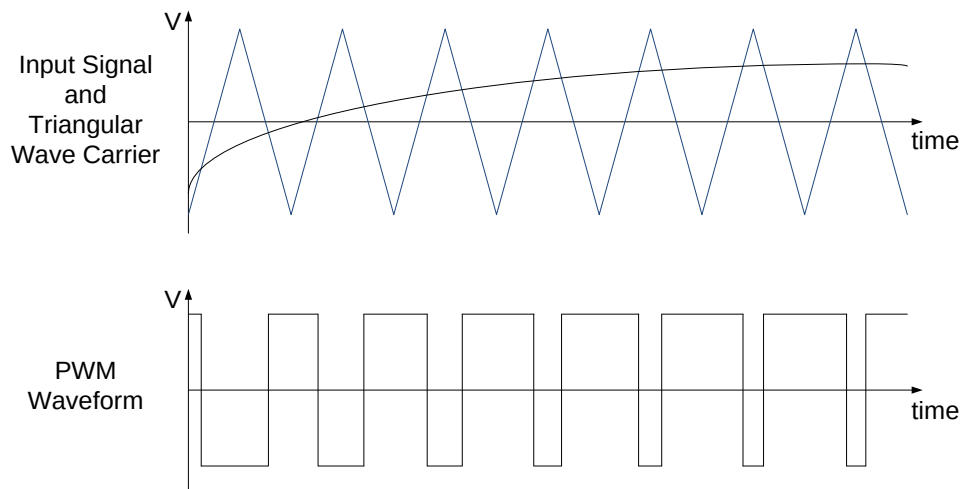


Figure 14. PWM Generation

2.4.2 Analog PWM Class-D Amplifier

2.4.2.1 Analog Open-loop Class-D Amplifier

An analog open-loop PWM Class-D amplifier is the most basic type of PWM Class-D amplifiers. Figure 15 depicts a simple open-loop Class-D amplifier with an analog PWM stage and its respective waveforms at each stage. The audio signal is first being modulated to a high frequency PWM signal in the PWM stage by comparing the input audio signal with a triangular or saw-tooth wave carrier signal [3]. Such modulation process is often known as natural sampling PWM process [2, 12, 63, 64]. Under noise-free conditions, the open-loop Class-D amplifier structure provides a very outstanding power efficiency performance and very high output audio signal quality. However, the lack of error correction mechanisms in open-loop Class-D amplifier has always been the major drawback in modern mobile audio amplifier applications. In other words, any noise or non-linearity appears in the

amplification process would severely degrades the output audio signal quality [26, 28].

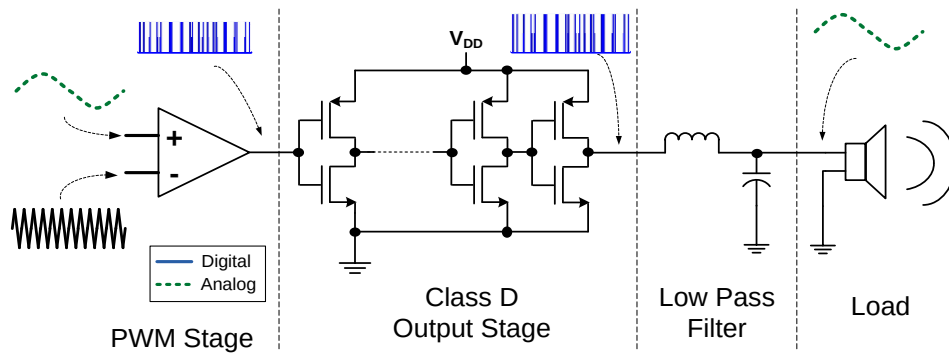


Figure 15. Basic analog open loop Class-D amplifier

2.4.2.2 Analog Closed-loop PWM Amplifier

Most literatures show that negative feedback can be applied to any open-loop Analog Class-D amplifiers to overcome the effect of error and noise on its output amplified signal [4, 28, 65, 66]. Figure 16 shows a general architecture of a closed-loop analog Class-D amplifier. An error correction signal is normally obtained by taking the difference between the feedback signal from the output of the Class-D amplifier output power stage and the input audio signal. The error correction signal is then amplified by the error amplifier. At the PWM stage, the amplified error correction signal is subsequently modulated by a high frequency triangular carrier signal. Hence, negative feedback improves the linearity and the noise rejection capability of the amplifier system. For Analog Class-D amplifiers, a digital to analog conversion process is normally required. As a result, the analog PWM amplifier is generally unsuitable for a fully digital amplification system [4].

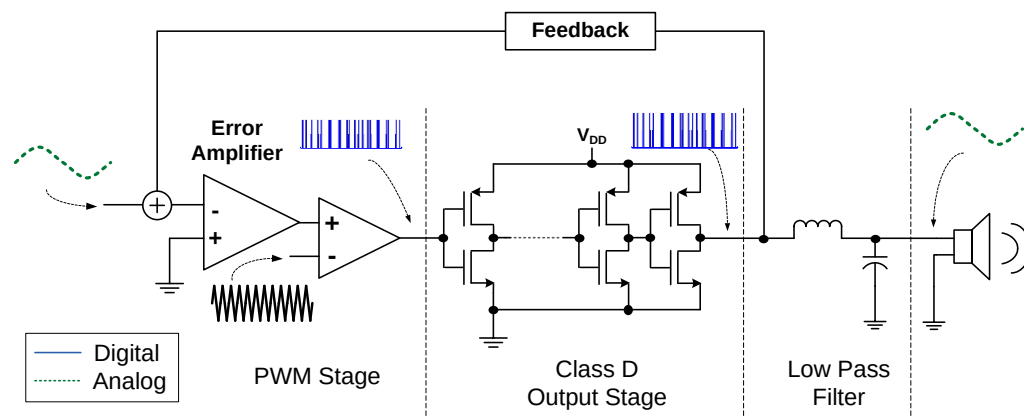


Figure 16. Closed-loop analog Class-D amplifier

2.4.3 Digital PWM Class-D Amplifier

Class-D amplifiers are ideally suitable for the trend of digital amplification as mentioned in [4]. This is due to the unique amplification process of Class-D amplifiers which requires the input audio signal to be modulated to a high frequency pulse signal. Unlike conventional linear amplifiers, the output transistors of Class-D amplifiers switch between just two discrete voltage levels instead of amplifying analog signals. Since most of the musical information are stored in digital format (mostly in pulse code modulated (PCM) format), the inherent signal processing function of Digital Class-D amplifiers somehow enables the amplification process to be remained in the digital domain. This eliminates the requirement for a digital-to-analog signal conversion (DAC) process to transform the digital PCM signal into analog domain prior to the amplification process [4, 67]. Despite the advantages of digital amplification, digital Class-D amplifiers are prone to distortion especially in the digital PCM-to-PWM conversion stage. The conversion of a sampled PCM signal directly into a proportional PWM signal is known as Uniform sampling [4, 12]. Such pulse width generation method is inherently non-linear [61, 63]. It requires a very high switching frequency to produce a high resolution PWM signal. For instance, a 16-bit CD quality signal with 44.1 kHz sampling frequency encoded in PCM format would require a switching frequency of 2.89 GHz in order to reproduce an analog signal equivalent to that resolution [12]. This imposes a very strong limitation on digital Class-D amplifier.

Recently, many solutions have been proposed for digital PCM-to-PWM conversion to enhance the output signal linearity of digital Class-D amplifiers [2, 12, 63-65] with lower switching frequency. The general enhanced high resolution digital PMW Class-D amplifier concept is depicted in Figure 17. In order to reduce the distortion, the sampling rate of a digital input signal is first

being increased to approximately 8 times by an oversampling filter (e.g. from 44.1 KHz to 325.8 KHz). Unfortunately, the original analog waveform is not available in the case of digital input amplifier. This is due to the fact that the PCM input signal is uniformly sampled in a certain time interval (e.g. 44.1 kHz for CD application). Figure 18 illustrates the difference in pulse duration between a Naturally sampled PWM and Uniformly sampled PWM signal due to the difference in the reference signal crossing point. These difference in pulse duration would result in severe distortion in the resulting Uniformly Sampled PWM waveform. To compensate for this inherent non-linearity of a Uniformly sampled PWM signal, a cross-point detector is usually introduced to estimate the naturally sampled point from the uniformly sampled PCM signal. Such estimation often involves some special algorithms and numerical methods. This technique is often known as Pseudo-Natural PWM [12]. Thereafter, a noise shaping filter is used to reduce the effective number of bits that is required to produce the equivalent signal resolution. This is done by mitigating the noise level at the audio band at the expenses of increasing the noise level at the higher frequency band. Doing so reduces the required clocking frequency of the digital PWM stage significantly [8, 12, 65, 66, 68-70].

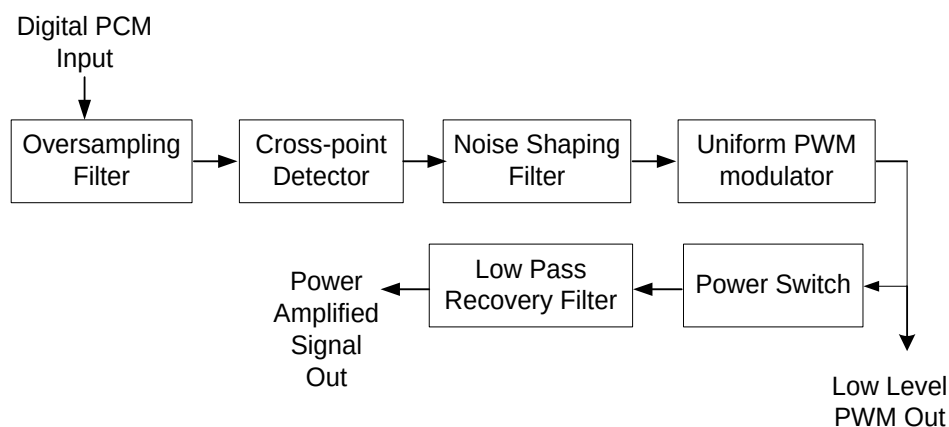


Figure 17. General concept for enhanced high resolution digital PWM amplifier [12]

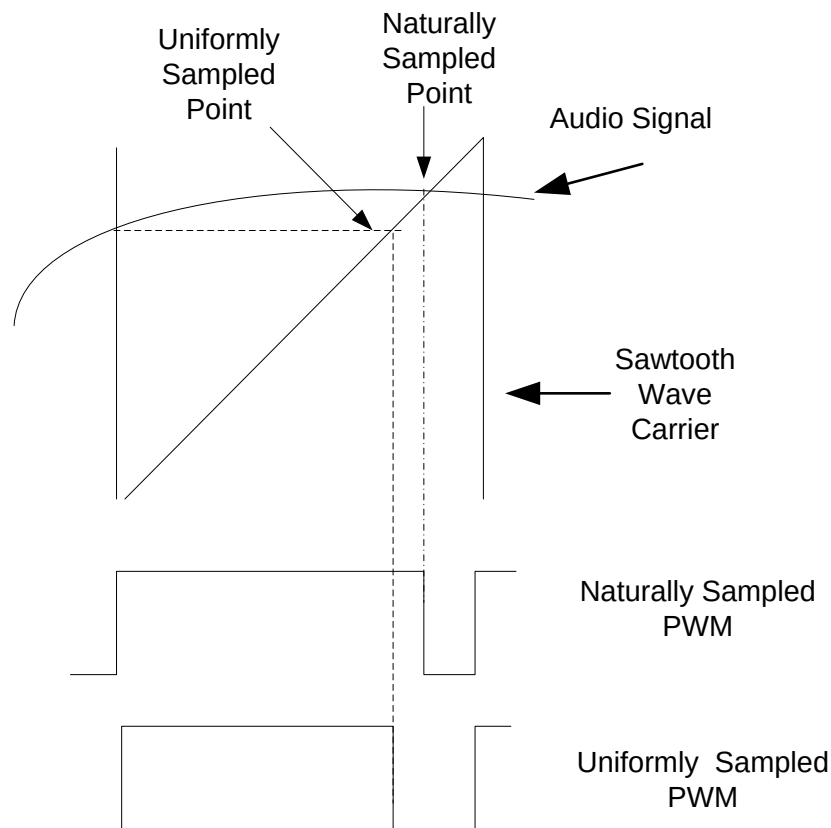


Figure 18. Difference in Naturally Sampled and Uniformly Sampled PWM signal

Although the PCM-to-PWM conversion or the pulse modulation stage can generally be linearized by the above concept, the problems of low PSRR rejection have not been fully addressed. This is because a closed-loop digital Class-D amplifier often demands an Analog-to-Digital Convertor (ADC) to convert the analog audio output into digital form and compares this digital feedback signal with the input PCM reference as depicted in Figure 19 [71]. Such ADC is normally expensive and it often limits the performance competences of digital amplifiers. In addition, the inherent time delay of the ADC would also affect the overall stability of the amplifier system [13]. Till date, there are not many reported solutions [72-78] that had fully addressed the PSRR rejection problems for digital switching amplifier.

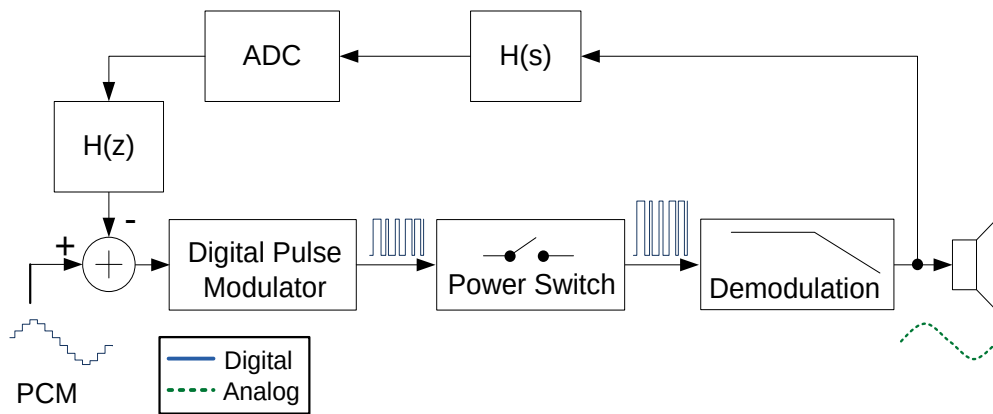


Figure 19. General digital feedback Class-D amplifier

2.5 Class-D Amplifier Output Stage

In audio amplifier systems, the primary function of an output power stage is to provide sufficient energy in the form of current into the speaker load. Therefore, it is extremely important to design an output power stage with superior power efficiency performance.

Unlike the traditional linear amplifier output power stages, the output transistors of a Class-D amplifier system only operate in either the triode or the cut-off region. In the triode region, the voltage across the drain and source terminal is theoretically zero, regardless of the amount of current flowing across the transistor. On the other hand, there is virtually no current flowing through the transistor in the cut-off region and the total supply rail voltage is dropped across the drain and source terminal of the transistor.

Therefore, the net power dissipation within the device is effectively zero. Hence, the Class-D output power stage is very efficient under these operating conditions [1, 2, 42, 56, 79-81]. Figure 20 depicts the two basic Class-D output stage topologies. The half-bridge configuration as shown in Figure 20(a) has the advantages of simplicity and flexibility over the full H-bridge configuration. However, the full H-bridge configuration depicted in Figure 20(b) provides an output power which is four times higher than its half bridge counterpart [2, 3]. Nonetheless, the full H-bridge configuration consumes a huge silicon area as the output switching devices are physically big to handle the large current.

Theoretically, the power stage that are working in Class-D operation can achieve 100% efficiency [2]. However, this is only true for the ideal case. The conduction loss due to some parasitic resistance of the power transistors is inevitable [1]. Figure 20 depicts the respective equivalent circuit for the two common types of Class-D amplifier output stages with R_{ON} , R_P , R_F and R_L representing the finite ON resistance of the power transistors, the parasitic resistance for the combined metal interconnects, bond wires, lead frame, and PCB traces, the parasitic resistance of the filter components, and the load resistance respectively [82]. By first-order analysis, the efficiency of a half and a full H-bridge Class-D output stage can be estimated by the following equations:

$$Efficiency_{HalfBridge} = \eta_{HB}(\%) = \frac{P_{out}}{P_{Supply}} = \frac{R_L}{R_L + R_{ON} + R_F + R_P} \times 100\% \quad (3)$$

$$Efficiency_{FullBridge} = \eta_{FB}(\%) = \frac{P_{out}}{P_{Supply}} = \frac{R_L}{R_L + 2R_{ON} + 2R_F + R_P} \times 100\% \quad (4)$$

As the resistance values of R_{ON} , R_P and R_F are usually small, the power efficiency of a Class-D system is usually more than 90%. Despite the advantage of achieving remarkably high power efficiency performance, such Class-D

amplifier output power stage is very susceptible to noise from the supply rails and switching components mismatch.

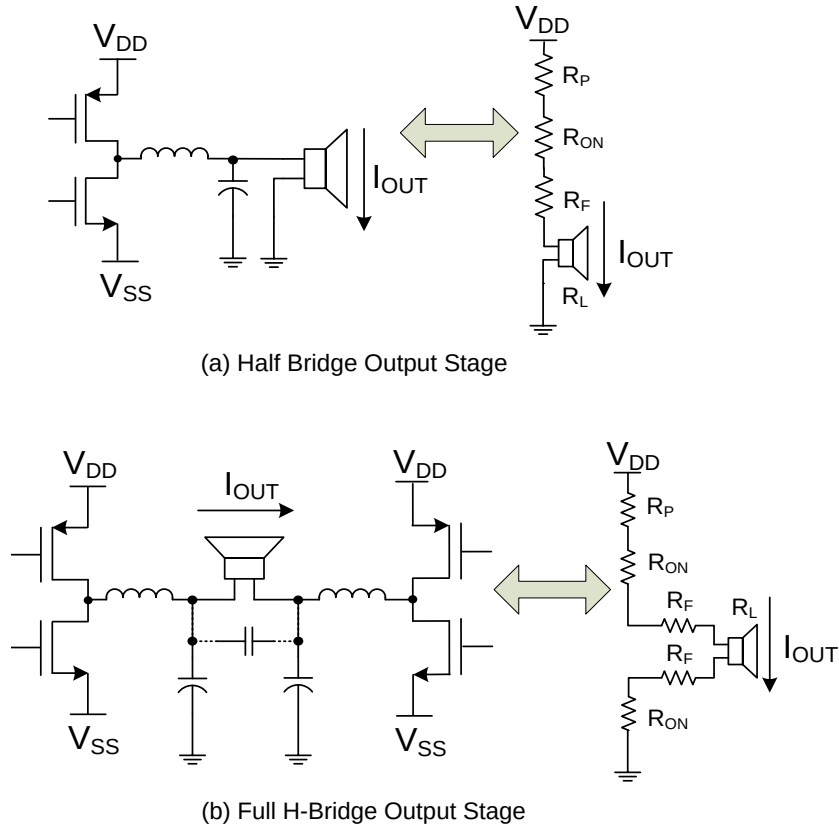


Figure 20. DC equivalent loop of resistive losses in a Class-D output stage.

2.5.1 Error Sources in Class-D Output Stage with Half Bridge Configuration

The conventional Class-D amplifier output power stage is very susceptible to the noise from the supply rails as well as switching components mismatch. Nielsen [2, 74-76] had classified those errors or pulse distortion

introduced by the switching output stage into two main categories, the Pulse Timing Errors (PTE) and the Pulse Amplitude Errors (PAE).

The non-linearities caused by PTE include all the error sources that affect the duration of the pulse width in each PWM pulse cycle. Typical examples of such error sources include the imperfect turning-on and turning-off time delay of the Power MOSFET transistors, the necessary dead-time delay, and the finite rising and falling times of the switching signal.

On the other hand, the PAE are the error sources that distort or modulate the amplitude of the PWM waveform. The two major contributors to PAE are the noise from the supply rail and the finite output impedance of the switching devices [81]. Figure 3 in Chapter 1 illustrates the effect of the power supply perturbation to the switching output power stage. It shows that the positive amplitude of the output pulses is modulated by a low frequency supply ripple. Such ripples often escape from the output LPF as the ripple frequency is within the pass-band of the output LPF. Hence, the output signal gets distorted. Figure 21 summarises the major causes of imperfection in a Class-D half-bridge amplifier system.

As mentioned previously, the output power stage is the most vulnerable block to power supply ripple in any open-loop Class-D amplifiers solutions. Therefore, it is a good practice to connect Class-D amplifiers output power stages to a well regulated power supply to avoid any PAE from affecting the output signal quality of the amplifier. Unfortunately, most amplifier power stages nowadays are often connected directly to the battery of the devices due to the power efficiency consideration as well as the physical size competency of the final products. Power supply ripples within the audible frequency range escape from the output LPF effortlessly and couples directly to its output. This is very undesirable, especially in GSM mobile phone

application where the well-known 217 Hz noise from the RF Transmit and Receive power amplifier, and also the charge and discharge processes of the lithium battery often pollute the power supply sources of the audio amplifier [17, 18].

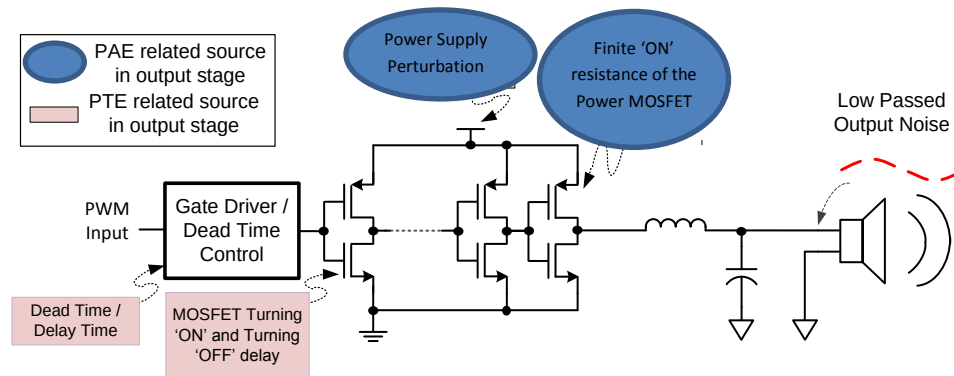


Figure 21. Major Imperfection of Class-D amplifier

In traditional analog Class-D amplifiers solutions, negative feedback correction techniques are often applied to the analog modulation stage to compensate for the PAEs [26-28]. Such technique often requires an ADC to convert the output analog signal into digital form and compare with the digitally generated pulse reference signal. As a consequences, the overall output signal quality will be limited by the amount of quantization errors from the ADC [74, 83, 84]. One may argue that quantization errors can always be minimized by using a higher resolution ADC. Unfortunately, a higher resolution ADC requires higher circuit complexity and consumes more power. The resulting performance competency of the amplifier is again being affected. In most cases, PAEs appeared at the output can be effectively mitigated by a bridge tied load (full H-bridge configuration). Consequently, the power supply ripples at the two outputs become common-mode signals, and therefore, cancelling each other. However, in some applications like stereo headphone amplifier, the hardware connector limits the use of full H bridge output stage. Thus, a more elegant solution to mitigate the pulse error is to create a local

negative feedback loop directly around the output stage itself as depicted in Figure 22. The general approach for this solution within a single PWM cycle is depicted in Figure 23. In this example, the amplitude of the output pulse from the Class-D amplifier output power stage is assumed to be modulated by the power supply ripple that is greater than its nominal value. Therefore, the amplitude of the output pulse is greater than that of the input pulse. In general, a correction circuit performs a cycle to cycle comparison between the input and output pulses, and then generates a pulse-width corrected PWM signal based on the amplitude difference between them. The pulse areas of the resulting corrected PWM signal and that of the input reference PWM signal must be maintained by re-modulating the duty ratio of the corrected PWM signal. This process repeats for each PWM cycle. In this way, the average energy of the output corrected switching pulses would be equivalent to that of the input reference pulses in each cycle. Thus, the error introduced in the output stage can be effectively compensated.

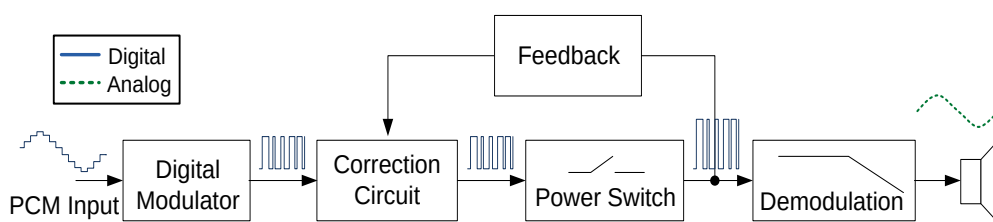


Figure 22. General block diagram of a Class-D amplifier with closed loop output stage

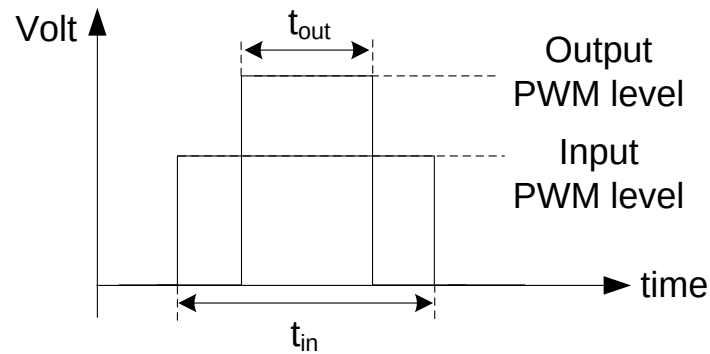


Figure 23. Pulse width correction approach

2.5.2 Delay-Line Correction System

The delay-line correction system for the Class-D output stage was introduced by Logan [73] to minimize the distortion generated by a PWM switching amplifier. Figure 24 shows the functional block diagram for this delay-line correction system. This system is based on pulse re-timing by a digitally controlled analog delay-line and a quantized feedback loop to minimize the distortion in a Class-D power stage. The PWM input signal propagates through the delay line. The output of the delay line is derived from a movable tap and subsequently amplified by the output power stage. The required tap for the delay line would be selected by a decision circuit which consists of a low-resolution Analog-to-Digital Converter (ADC) with an associated address decoder. The input of the decision circuit is obtained from a noise shaped error feedback signal that is generated by subtracting the input signal from the scaled version of the output signal and then noise shaped by the loop filter. In this way, this system allows the pulse edges to be re-timed to compensate for the error introduced by the power amplifier. It is claimed that this system is able to provide a 50dB reduction in the distortion level.

However, such improvement level is subjected to the accuracy of the analog delay line. Any component parameters mismatches or variations would deteriorate the performance of the system greatly.

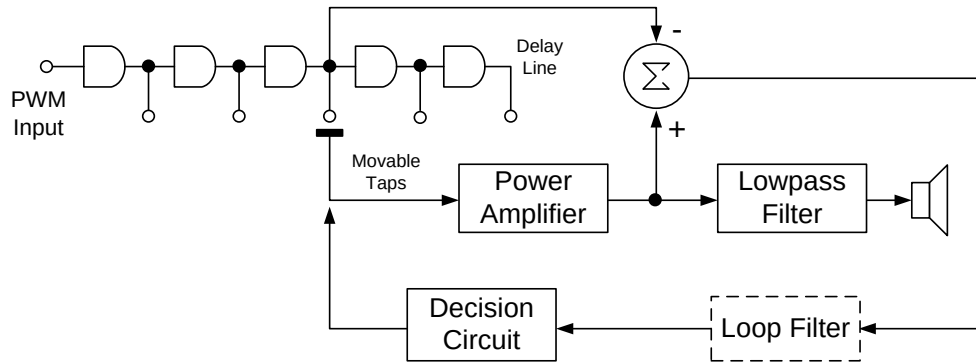


Figure 24. Delay-Line Correction System

2.5.3 Pulse Edge Delay Error Correction (PEDEC)

Inspired by the idea reported by Logan [73], a PEDEC controller for high power Class-D amplifier application was proposed by Nielsen in [74-76]. This system compensates for the errors by applying some control theories to delay the pulse edge of the PWM signal.

Figure 25 depicts a functional diagram of a switching amplifier with the PEDEC controller. This system uses the digital modulated pulse signal as the reference signal. The feedback signal is taken directly after the demodulation stage. Therefore, any noise and nonlinearity in the audio output due to the imperfection of the output stage and LPF can also be corrected. Figure 26 illustrates how the PEDEC unit corrects for the introduced error by re-timing

both the leading edge and the trailing edge positions of each PWM cycle. The PEDEC unit first integrates the incoming (ideal) PWM signal (V_r). Thereafter, this integrated signal (V_i) is compared with the control signal (V_e) to generate the corrected PWM signal (V_c). There are three cases of error corrections depending on V_e and it is summarized in Table 1. The THD performance for the PEDEC system over the audio frequency band is depicted in Figure 27 [74-76]. It can be seen that the PEDEC system could achieve a very outstanding THD performance. However, the amount of PAE correction is only around 40dB in the low frequency (100Hz) for this PEDEC system [74].

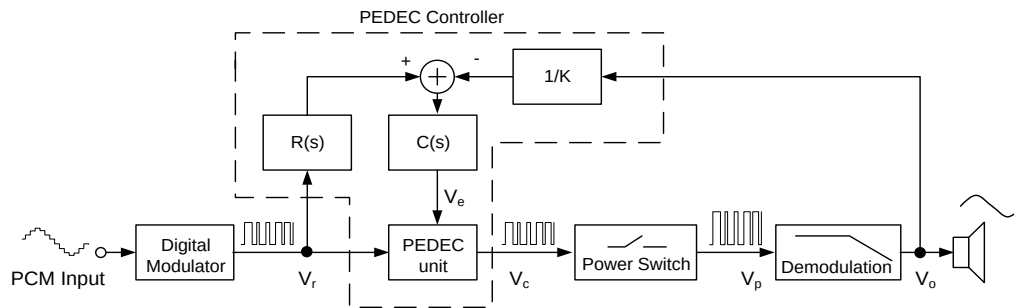


Figure 25. Pulse Edge Delay Error Correction

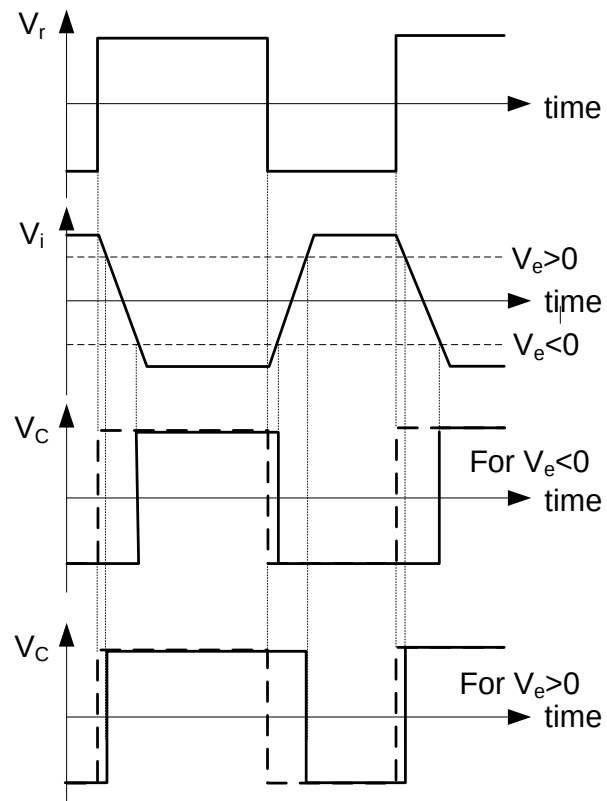


Figure 26. Double sided pulse edge delay correction approach

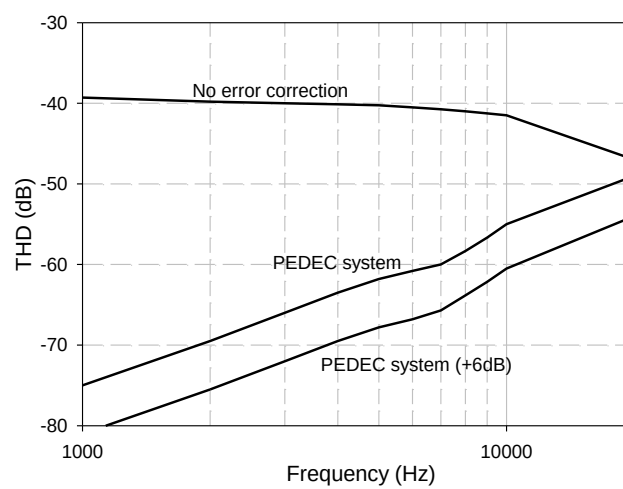


Figure 27. THD vs frequency without error correction and with the PEDEC controller (bottom)

Table 1. Three cases of correction in PEDEC system

Control Signal V_e	Action
$V_e=0$	Pulse Width Unchanged
$V_e>0$	Effective pulse width increased
$V_e<0$	Effective pulse width reduced

2.5.4 Bi-directional Saw-tooth Error Correction (BSEC)

Based on the same PEDEC controller structure proposed by Nielson in [74-76], Park [72] proposed a Bi-directional Saw-tooth Error Correction (BSEC) controller circuit to correct the errors and noise in the PWM signal of the Class-D output stage [72]. Instead of integrating the reference PWM signal, the BSEC controller generates a saw-tooth error correction signal V_m from the same PWM signal V_r . With reference to the PEDEC system in Figure 25, the corrected switching signal is produced by comparing V_m signal generated by the BSEC controller with the error signal V_e . This correction approach is illustrated in Figure 28 and the schematic of the correction circuit is shown in Figure 29. The polarity of V_r determines the direction of the constant slope forming the corresponding positive and negative saw-tooth part of V_m . The BSEC would make V_m zero instantly once the polarity of V_r is changed. From Figure 28, it can be noticed that this circuit is able to provide a wider error correction range (ΔT) as compared to the PEDEC correction approach shown in Figure 26. Nonetheless, Figure 28 illustrated that the BSEC controller would make V_m zero instantly when V_r changes polarity. This implies the need of an

operational amplifier with a very high slew rate requirement and imposed a limitation on the BSEC controller.

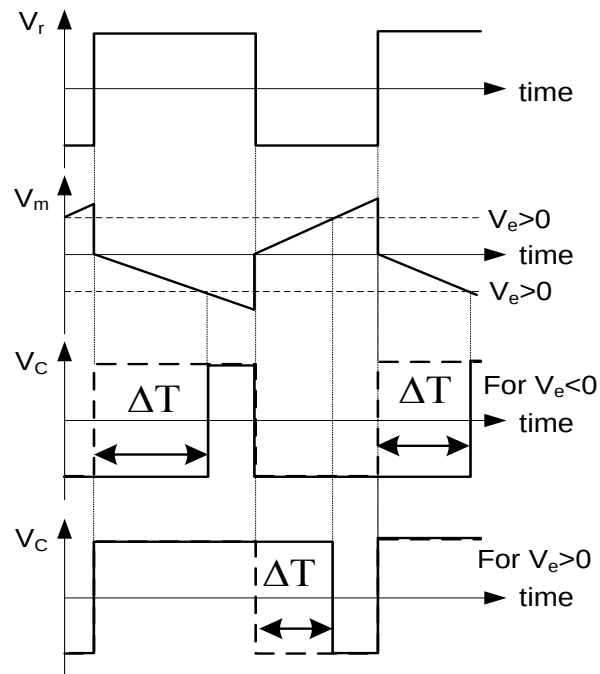


Figure 28. Error correction approach based on BSEC

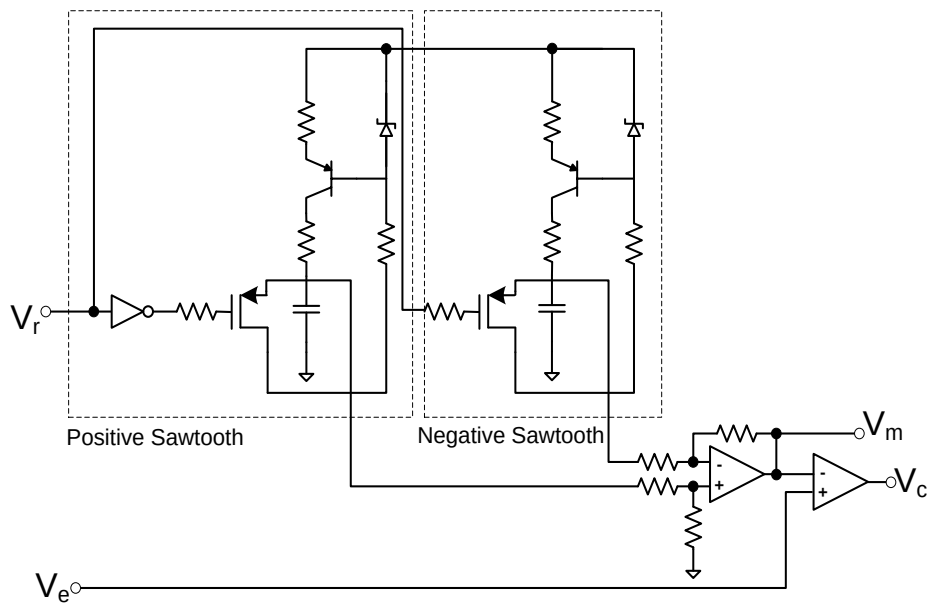


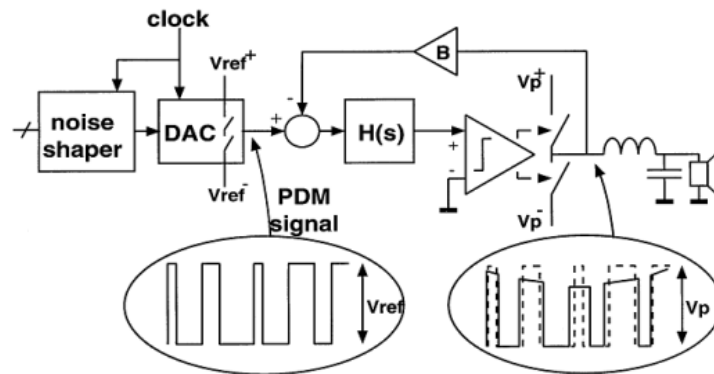
Figure 29. Schematic of BSEC Controller

2.5.5 PowerDAC Output Stage

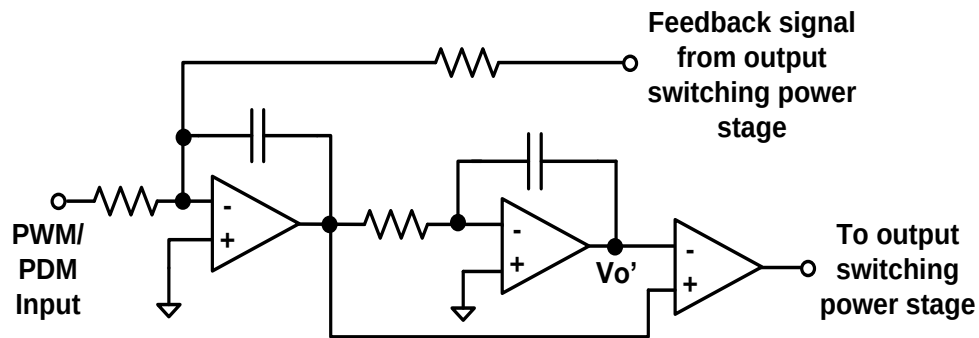
Kathleen [77] has proposed an error correction scheme for the PowerDAC application which can overcome the error introduced in the power stage due to power supply modulation and switching artefacts.

Figure 30 shows the principle and the actual schematic of the error correction scheme for the PowerDAC application proposed by Kathleen. In his design, a PDM signal is generated from a fifth-order noise shaper with idling frequency of approximately 1MHz. The loop filter $H(s)$ used in his error correction circuit is a second-order integrating filter. A feedforward branch was introduced to achieve a first-order roll-off rate for its loop gain around the unity gain frequency for stability consideration. This approach is different from the sigma-delta approach as the comparator used in this scheme can change state at any time instance. In other words, there is no quantised level for the loop and the loop actually remains analog.

By using this technique, the error correction circuit can effectively suppress the effects of the supply ripple and switching artefacts in the low frequency content by modulating the width of the continuous time PWM or PDM signal. Table 2 summarises the performance of the PowerDAC output stage.



a) PowerDAC principle



b) Schematic of PowerDac
Figure 30. PowerDAC Output stage

Table 2. Performance of PowerDAC (with 8 ohms BTL)

Technology:	0.5 μ m CMOS (2PS,3AL)
Supply voltage:	5V
Signal output swing:	4V _{pp}
Output power:	2*1W
Efficiency:	70%
Dynamic range:	>83dB
THD @ 1kHz, 1W:	<0.1%
PSRR @ 1kHz:	>90dB
Active area:	4*0.5mm ² (4 PowerDAC modules) 2mm ² (digital noise shaper)

2.5.6 Digital Amplifier for Car Use

Figure 31 shows the power stage correction circuit for a car audio application digital amplifier proposed by Taura [78]. The correction circuit consists of two analog integrators which integrate a referenced PWM input signal from a digital pulse modulation stage and a PWM feedback signal from the output power stage respectively. A differential amplifier is introduced to obtain the difference between the two integrated signals. Next, a third integrator integrates the output of the differential amplifier. Thereafter, a corrected signal is obtained based on the crossing over point of the difference signal and the integrated version of the difference signal. The working principle of this correction circuit is very much similar to the one proposed by Kathleen [77]. From the simulation results obtained in [78], it shows that this correction system is able to provide a power ripple rejection of more than 60 dB in low frequency range. The reported typical dynamic range and the distortion level for a Class-D amplifier utilizing this correction circuit are 87dB and 0.05% respectively. Figure 32 shows the disturbance suppression and the THD performance of the reported Class-D amplifier with the feedback correction circuit proposed by Taura [78]. It can be seen that this correction circuit can achieve a very good THD+N performance of less than 0.1% at low frequency. However, the amount of power supply ripple rejection is only around 60dB. In addition, this correction circuit requires too many components, which add on to the production cost of the whole systems. The correction circuit would also occupy a larger silicon area and dissipated higher power if it were to be implemented as a single integrated chip.

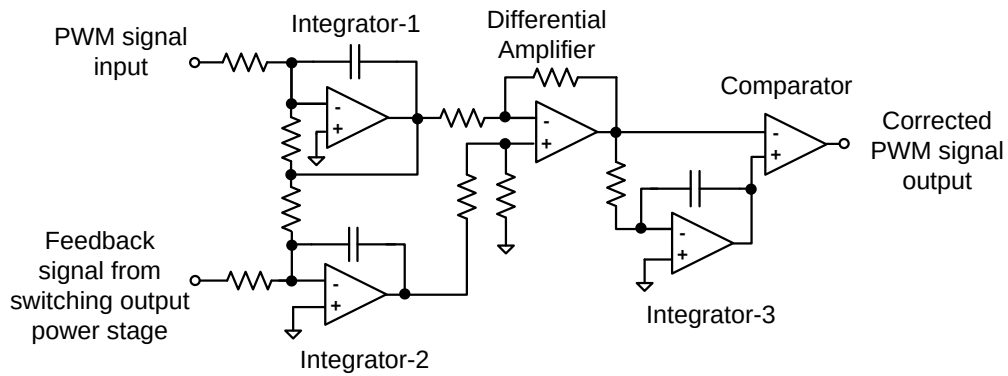


Figure 31. Correction Circuit for Digital Amplifier for Car Use

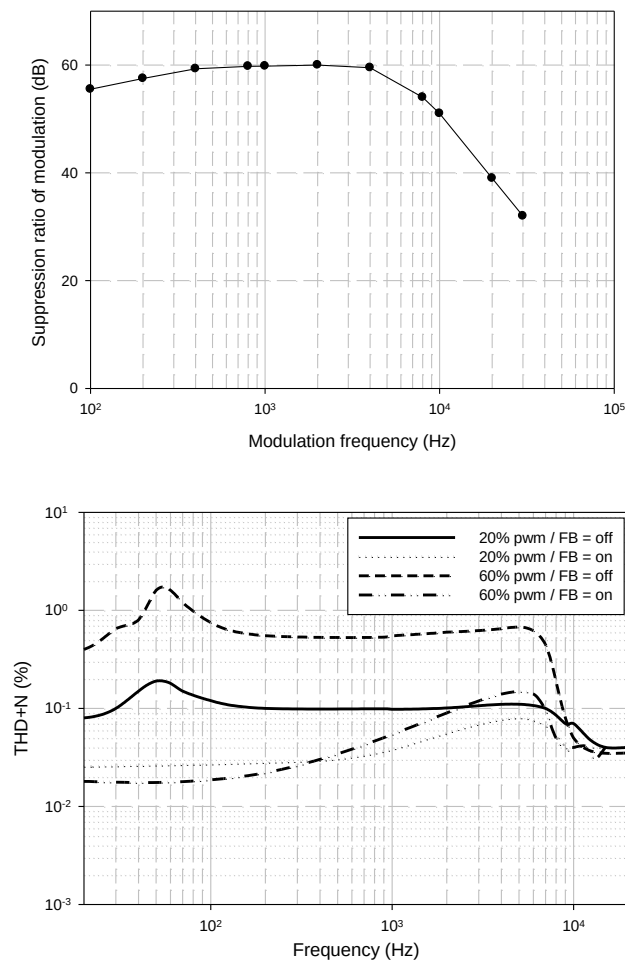


Figure 32. Disturbance suppression and THD performance of the correction circuit

Chapter 3 PWM-in / PWM-out Feedback Loop for Class-D Amplifier Power Stage

In this chapter, a direct PWM-in / PWM-out negative feedback loop is presented to provide good PSRR and THD performance for open-loop Class-D amplifier with half bridge connected output stage. A large portion of this chapter has been published in [85].

3.1 Correction Concept

In the following part of the thesis, the pulse modulation stage of any PWM Class-D amplifiers described will be assumed to be an ideal PWM pulse generator which produces high quality (low distortion) PWM reference signal. As mentioned in the previous chapter, the overall pulse area within each switching period must be maintained to preserve the audio reproduction quality [86]. This phenomenon is best explained with the equation for the average of the output PWM signal of any PWM Class-D amplifiers, $v_o(t)$.

Figure 33 shows a single PWM cycle with a period of T with balanced and constant power supply rails. The average of the output PWM signal $v_o(t)$ for one PWM cycle can be derived as:

$$\begin{aligned} v_o(t) &= \frac{1}{T} \left(\int_0^{dT} v_s dt \right) + \frac{1}{T} \left(\int_{dT}^T -v_s dt \right) \\ &= v_s(2d - 1) \end{aligned} \tag{5}$$

where T = period of one PWM cycle,
 d = duty ratio of the PWM pulse,

v_s = amplitude of the PWM pulse.

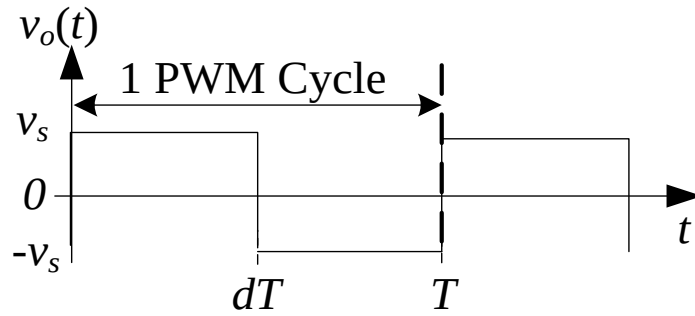


Figure 33. Pulse width correction approach

Inspecting equation (5), it is possible to change the duty cycle of any PWM signal to compensate for any changes in the pulse amplitude in order to achieve the same $v_o(t)$. Therefore, a correction circuit should adaptively alter the duty cycle of the resulting output PWM pulses with respect to the PAE presented in it. In other words, such error correction systems should accept a feedback signal from its output in PWM form, and compares with its input PWM reference signal (assumed to be an ideal PWM signal with no distortion) to generate a correction signal that re-modulates the duty cycle of its output signal.

However, implementing feedback loop to the PWM input and PWM output system is not as straightforward as in the case of linear amplifier. This is due to the followings:

- i) Both the input and the output signals are PWM signal,
- ii) The switching rate of the compensated output PWM signal should preferably maintained for power efficiency consideration, and
- iii) The correction circuit should not generate any non-linearity to its output signal.

3.1.1 Proposed Architecture

To overcome the constraints in applying negative feedback to a system with both the input and output signals are PWM, a negative feedback structure depicted in Figure 34 is proposed. This structure is very similar to that of the hysteresis Self-Oscillating Class-D amplifiers (HSO-Class-D amplifiers). In fact, it can be classified as a special case of HSO-Class-D amplifiers as both of its input and output signals are now PWM signals. In other words, this is a true PWM-in / PWM-out negative feedback structure correcting any PAEs in the amplified output PWM signal in any Class-D amplifier solutions. In addition, the negative feedback loop should not change the switching frequency of the output switching signal, thus, satisfying the power efficiency consideration mentioned earlier. (i.e. both the input and the output signals are switching at the same rate).

Figure 34 depicts a simplified schematic diagram of the proposed PWM-in / PWM-out negative feedback loop for PWM output stage. It includes a continuous-time difference integrator and a Schmitt trigger comparator. The difference integrator first integrates any pulse amplitude differences between the input reference PWM signal and the output PWM signal (i.e. any PAE in the output switching signal). The Schmitt trigger comparator acts as a single bit quantizer to quantize the accumulated errors according to its hysteresis threshold levels. Consequently, the switching edge of the output switching signal is being re-modulated with respect to the accumulated errors (i.e. the output of the integrator).

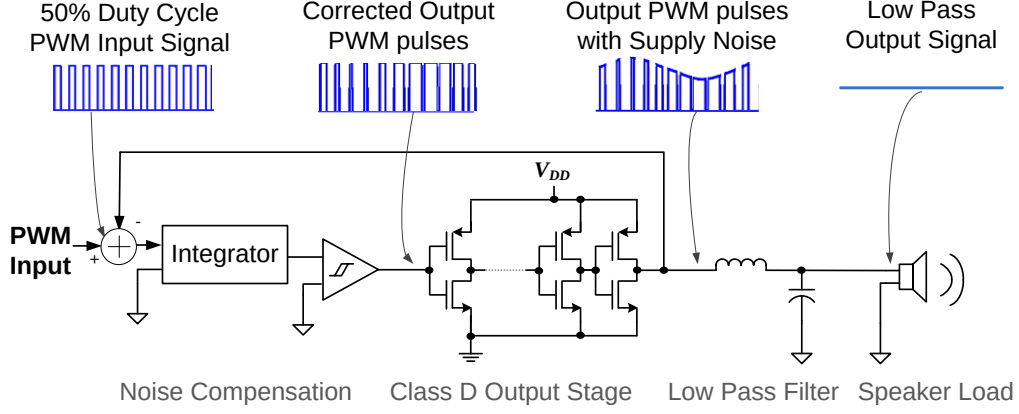


Figure 34. Class-D output stage with negative feedback

3.2 Linear Analysis of the PWM-in / PWM-out PWM Feedback Loop

3.2.1 Linear Analysis of First-order PWM Feedback Loop

In this section, the signal transfer function (STF) as well as the noise transfer function (NTF) of a first-order PWM feedback loop are first derived; and subsequently followed by its second-order counterpart. To simplify the analysis, the Class-D amplifier output stage [27] and the one-bit quantizer (Schmitt trigger Comparator) [79, 87] are assumed to be linear and can be represented by their respective linear time average model with a constant gain value. Figure 35 shows a partial linearized circuit for the proposed PWM feedback loop. The functional block K resembles the combined linearized model of the output power stage (K_{OPS}) together with a one-bit quantizer (K_Q). A comprehensive derivation of the linear model for the comparator gain K_Q

can be found in [87]. Figure 36 depicts an equivalent linear model of Figure 35. The PAE introduced at the switching output stage is denoted as V_n .

It may be worthwhile to note that the characteristics of the operational amplifier are ignored in this analysis (i.e. infinite open loop gain and gain-bandwidth is assumed for the operational amplifier.) This assumption is valid due to the following reasons:

- I. The derivation of the noise transfer function is only a preliminary estimation of the PSRR performance of the proposed architecture. Excluding the open-loop transfer function of the operational amplifier greatly reduces the general complexity of the noise transfer function, and hence, facilitating the derivation process.
- II. As the Gain-Bandwidth (GBW) product of any operational amplifier is normally designed to be much higher than the closed-loop response required in Class-D amplifier operation, the high frequency PSRR response for the proposed PWM feedback loop would be solely governed by its closed-loop response if the GBW of the operational amplifier is sufficiently high (which is normally the case for Class-D amplifier operation).
- III. The only remaining error in the noise transfer function against the PSRR response would be the limited open-loop DC gain for the Operational amplifier, which determines the maximum PSRR at low frequency. However, the PSRR error at low frequency is normally small due to the high DC open-loop gain of the operational amplifier.
- IV. By excluding the open-loop response of the operational amplifier in the derivation, the noise transfer function provides insightful information on the maximum achievable PSRR for the proposed closed-loop architecture. Thus, designers can

efficiently determine the open-loop specification for the operational amplifier base on such information.

Therefore, the equivalent STF ($STF_{1st-Order} = V_o/V_{in}$) and NTF ($NTF_{1st-Order} = V_o/V_n$) is given as:

$$STF_{1st-Order}(s) = \left(\frac{V_o}{V_{in}} \right)_{V_n=0} = \left(\frac{A_1 G K}{1 + G K \beta_2} \right) = -\frac{K}{C_1 R_1} \left(\frac{1}{s + K/C_1 R_2} \right) \quad (6)$$

$$NTF_{1st-Order}(s) = \left(\frac{V_o}{V_n} \right)_{V_{in}=0} = \left(\frac{1}{1 + G K \beta_2} \right) = \left(\frac{s}{s + K/C_1 R_2} \right) \quad (7)$$

where:

$$A_1 = -\frac{(R_1 // R_2) C_1}{R_1 C_1} \left[\frac{1}{(R_1 // R_2) C_1 s + 1} \right],$$

$$G = \frac{(R_1 // R_2) C_1 s + 1}{(R_1 // R_2) C_1 s} \quad \text{and} \quad \beta_2 = \frac{(R_1 // R_2) C_1}{R_2 C_1} \left[\frac{1}{(R_1 // R_2) C_1 s + 1} \right]$$

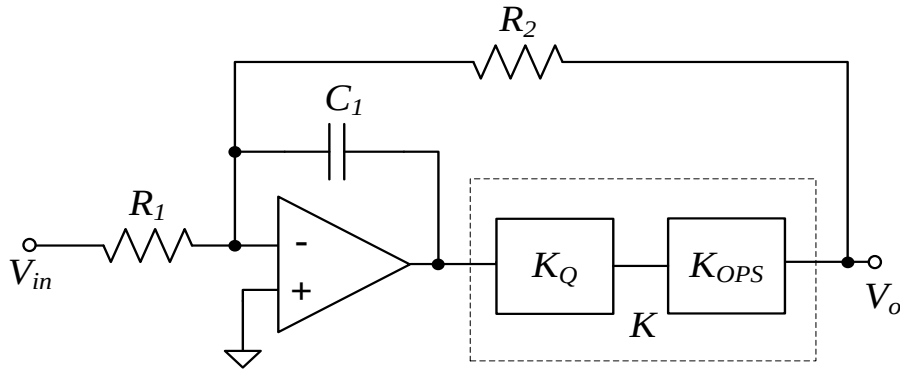


Figure 35. Linearized first-order PWM feedback loop for Class-D output stage

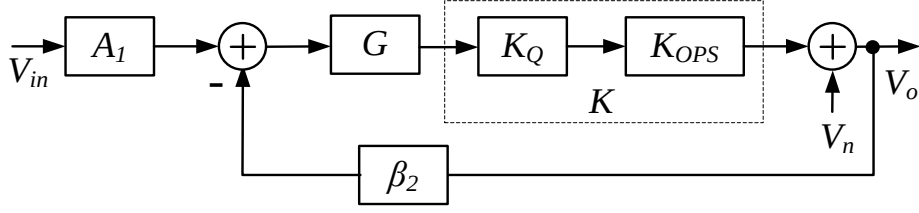


Figure 36. Equivalent linear model of first-order Class-D output stage

It can be noted from (6) and (7) that the low-pass response of the equivalent STF allows the low frequency information of the switching signal to be preserved; whilst, the high-pass characteristics of the NTF effectively shaped the noise spectrum so that the low frequency noise is reduced at the expenses of higher high frequency noise. As a result, any low frequency PAE in the output PWM signal, V_n , are being suppressed and pushed to the higher frequency band, which is beyond the human hearing threshold. Thus, the Power Supply Rejection (PSR) at low frequency band is theoretically improved. However, the amount of noise suppression achieved by this first-order structure might not be adequate to reject the power supply noise to meet the high quality audio requirement nowadays.

3.2.2 Linear Analysis of Second-order PWM Feedback Loop

To further improve the PSR, higher orders PWM feedback systems are considered. Therefore, a second-order integrator depicted in Figure 37 is considered in this section. This integrator topology has been adopted in some commercial Class-D amplifier designs and a very detailed THD analysis for analog Class-D amplifiers utilizing this Second-Order integrator had been done in [27]. However, the input and the output feedback signals in this case are both PWM signals. Due to the digital nature of the PWM signal, the input and output signals of the system are now considered as digital signals. Consequently, the error

correction mechanism, and thus, the analysis technique to be used in this case are totally different.

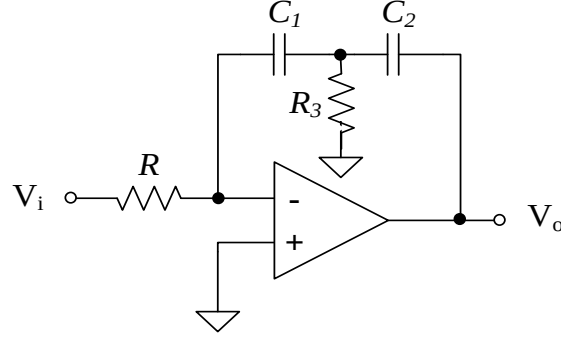


Figure 37. Second order integrator correction circuit

Figure 38 depicts the proposed second-order PWM feedback loop with a simple CMOS output power stage. Its equivalent STF and NTF ($STF_{2nd-Order}(s)$ and $NTF_{2nd-Order}(s)$ respectively) can be derived as

$$STF_{2nd-Order}(s) = \left(\frac{V_o}{V_{in}} \bigg|_{V_n=0} \right) = \left(\frac{1}{R_1 R_3 C_1 C_2} \right) \frac{1 + s R_3 (C_1 + C_2)}{s^2 + s \frac{(C_1 + C_2)}{R_2 C_1 C_2} K + \frac{K}{R_2 R_3 C_1 C_2}} \quad (8)$$

$$NTF_{2nd-Order}(s) = \left(\frac{V_o}{V_n} \bigg|_{V_{in}=0} \right) = \frac{s^2}{s^2 + s \frac{(C_1 + C_2)}{R_2 C_1 C_2} K + \frac{K}{R_2 R_3 C_1 C_2}} \quad (9)$$

It can be noted from (9) that the NTF in this case is a second-order high-pass function. Therefore, a better rejection to PAE is expected from this second-order design as compared to its first-order counterpart.

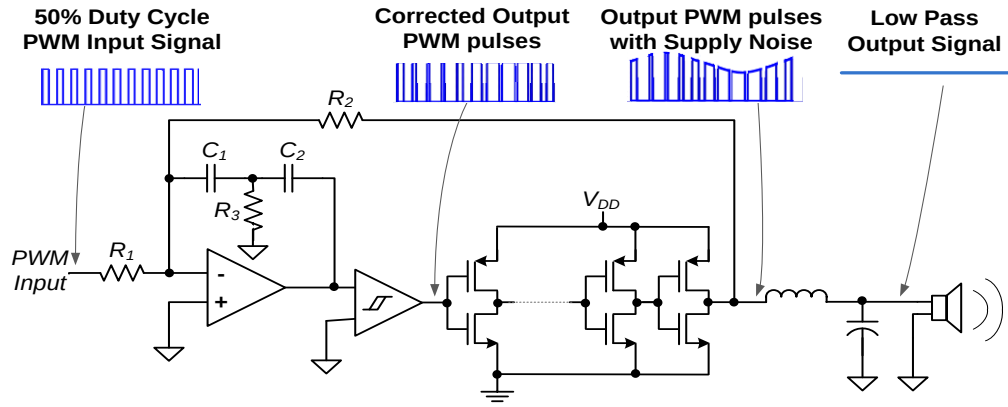


Figure 38. A second-order Closed Loop Class-D output stage

With the above analysis, the NTF and the STF of the proposed first- and second-order design based on Matlab simulation are plotted in Figure 39 and Figure 40 respectively. Figure 39 shows that the second-order design has a much better noise suppression capabilities as compared to its First-Order counterpart, especially in low frequency band. However, this is only a first-order estimation as the combined quantizer gain and Class-D amplifier power stage gain equals to a constant K . A more accurate simulation results obtained from Matlab Simulink and Cadence Spectre simulation software are discussed in the later part of this chapter.

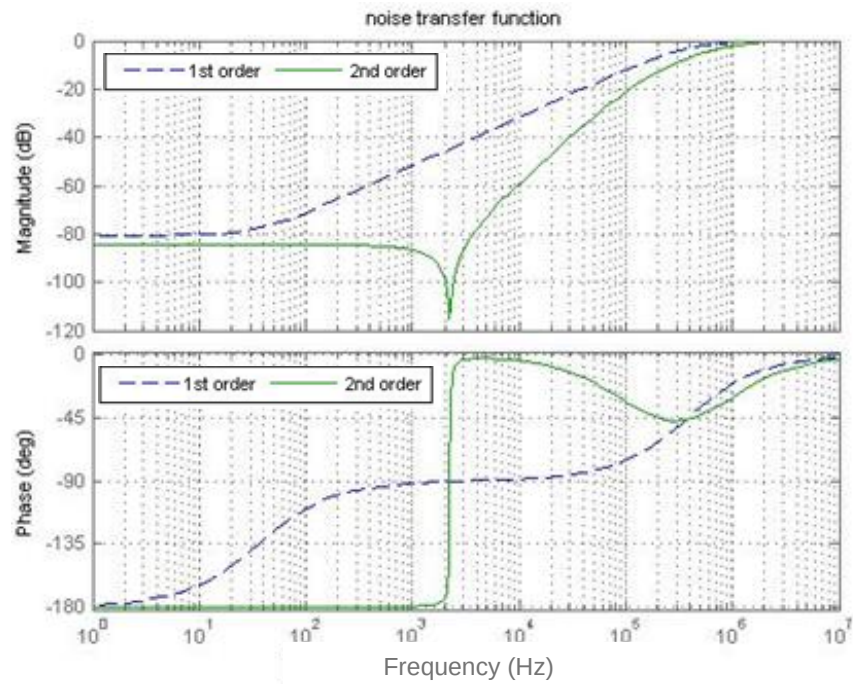


Figure 39. Noise response for the proposed first- and second- order output stage

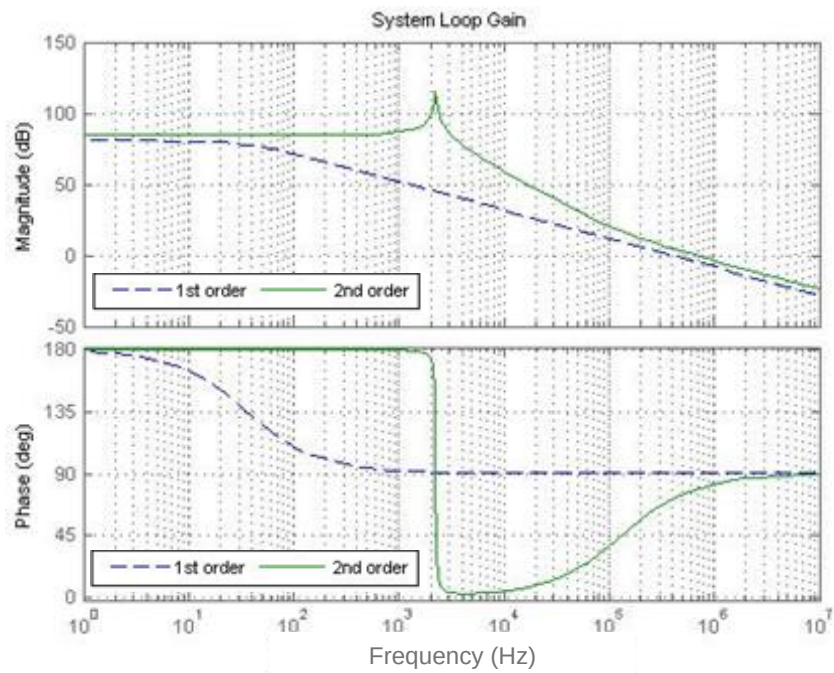


Figure 40. Signal Transfer function of the proposed first- and second- order design

3.2.3 A Note on the Stability of the Second-Order PWM Feedback Loop

Referring to Figure 38, a simplified open loop gain expression for the proposed second-order design is presented in (10). Its corresponding loop-gain plot is depicted in Figure 41.

$$loopgain = \frac{(s + 1/2R_3C)}{s^2} \quad (10)$$

Similar to [88], a LHP zero at $1/(2R_3C)$ is found in (10). To ensure a stable response, this LHP zero is placed slightly below the unity-gain frequency of the system. Doing so improves the overall phase margin at high frequency, and thus, stability is ensured. Also, the unity-gain bandwidth of the operational amplifier must be lower than the switching frequency with adequate margin to avoid pulse splitting problems (i.e. multiple pulse switching occurs within a single PWM cycle). However, it is worth noting that the pulse splitting problem does not necessarily introduce harmonic distortion or non-linearity to the audio output signal. In fact, the ripple instability condition described in [87] resembles the pulse splitting condition described here. It was recorded in [87] that the ripple instability does not lead to an unstable system. Instead, the loop continues to track the input signal and suppresses the audio band error with additional switching in the output PWM signal. Thus, the audio output signal linearity is improved at the cost of higher switching rate. As a result, higher power consumption is expected, and thus, lowering the overall power efficiency. Additionally, an uncontrollably high switching rate often results in circuit reliability problems. Conversely, pulse skipping problems can be one of the most serious considerations for stability analysis of any switching amplifier designs. Pulse skipping is a direct consequence of the insufficient integrator gain in the PWM feedback system. As a result, the integrator is unable to track the input PWM signal, thus, producing low-frequency oscillations in the audio output signal.

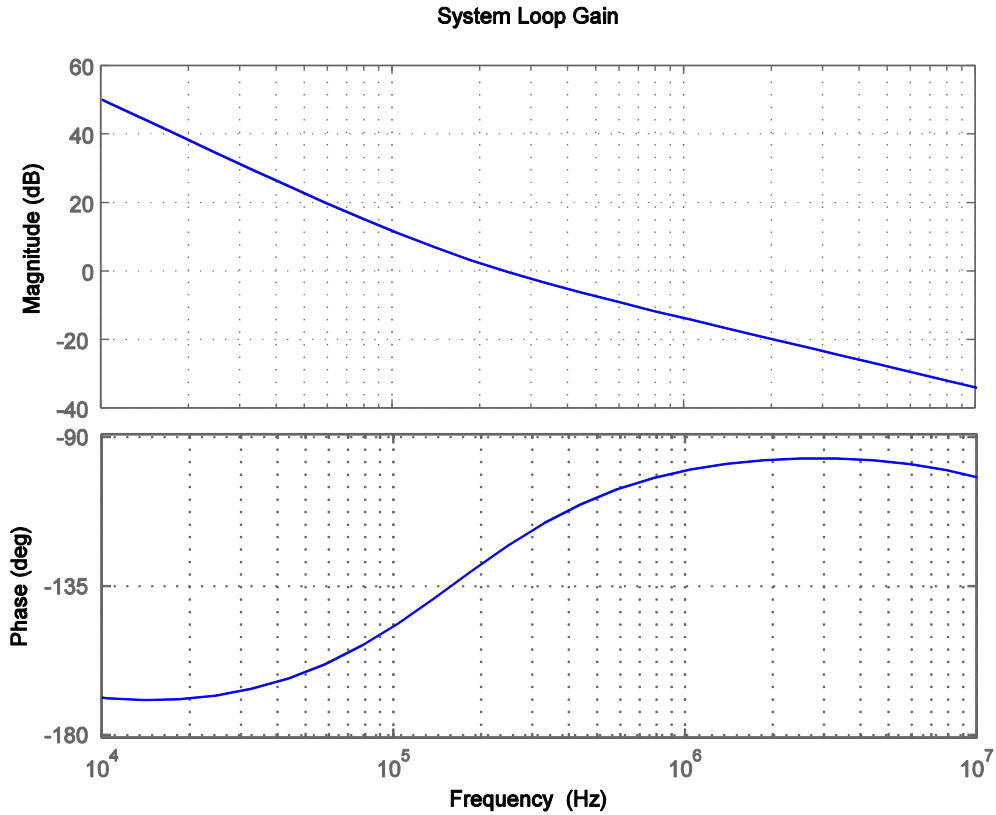


Figure 41. Loop gain transfer function of the optimized second-order PWM feedback design.

3.3 Time Domain Analysis for First-Order PWM Feedback Loop

Figure 42 shows the PWM waveforms and the integrator output signal. In the absence of supply noise as illustrated in Figure 42(a), the output switching waveform is a linear time delayed version of its input. Figure 42(b) and (c) demonstrates the corresponding correction process for negative and positive PAE in the output switching pulse respectively. For instance, a

negative PAE depicted in Figure 42(b) is corrected by increasing the pulse-width of the output switching signal. Conversely, a positive PAE is compensated by reducing the pulse-width of the same signal. Based on such observations, it agrees to (5) that the output pulse area in each full switching period is always maintained, and thus, the output audio signal quality is preserved.

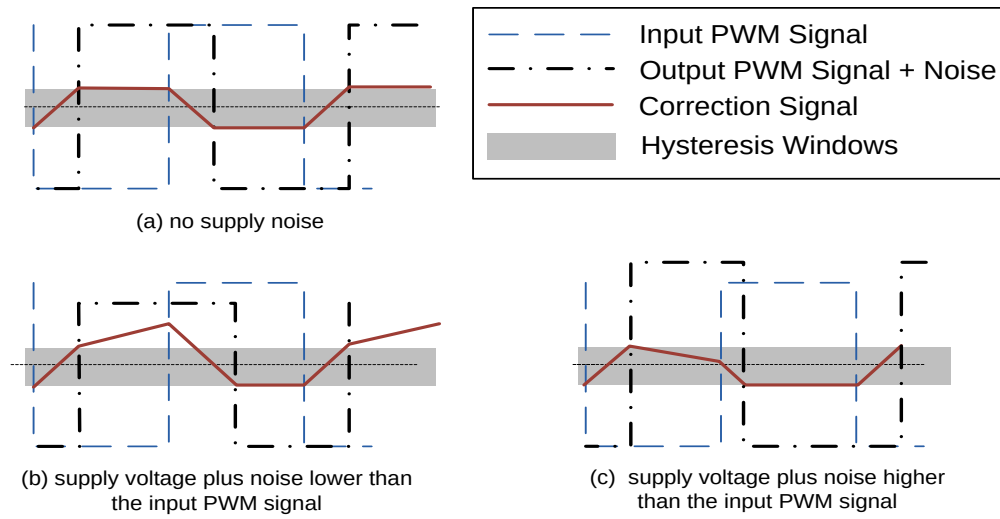


Figure 42. Simulated waveforms for a single supply First-Order PWM feedback loop for Class-D amplifier power stage

3.3.1 Mathematical Analysis for First-Order PWM feedback loop

In this section, a detailed study on the linearity of the First-Order PWM feedback loop is performed. The mathematical analysis described in this section is derived based on the Matlab Simulink model depicted in Figure 43. In order to isolate any potential harmonic distortion or other non-linearities contributed by the PWM negative feedback circuit, the incoming reference PWM signal is assumed to be a distortion free Naturally Sampled PWM

(NSPWM) signal. The integrator integrates the difference between the input and output switching signals with a first-order integrating function, producing $h_o(t)$ at the integrator output. Subsequently, the relay in Figure 43 resembles the hysteresis comparators in Figure 38 which quantizes $h_o(t)$ into two discrete levels (i.e. ± 1) based on its hysteresis threshold values. For the purpose of this analysis, the delay unit resembles the Class-D amplifier output CMOS power stage. All signals magnitudes in this model are normalized within the range of ± 1 . It can be observed from Figure 43 that this model utilizes an adder to obtain any amplitude differences between the input and output switching signals. This is because an inverting integrator is being used in the actual implementation. With the negative gain of the integrator, the overall system operates as a negative feedback system.

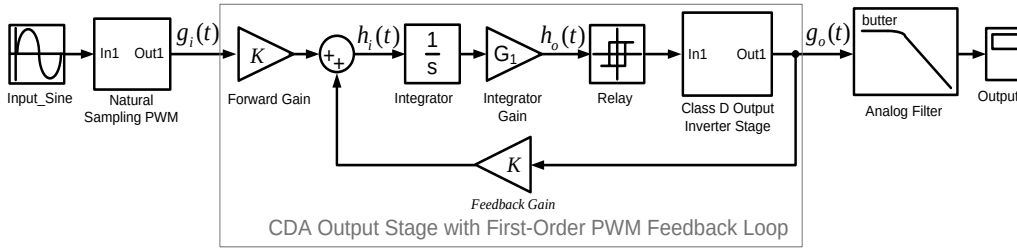


Figure 43. Matlab Simulink model of the proposed First-Order PWM feedback loop

Figure 44 depicts the time domain waveforms of the relevant signals from the first-order PWM feedback loop within one PWM period. The input PWM signal $g_i(t)$ to the feedback loop is assumed to be a 50% duty cycle pulse train. On the other hand, the output PWM signal $g_o(t)$ switches its state depending on the integrator output $h_o(t)$ and the hysteresis threshold values of the relay (i.e. $\pm V$). The integrator input $h_i(t)$ is obtained by simply taking the amplitude difference between $g_i(t)$ and $g_o(t)$.

Before proceeding further, it is useful to divide the PWM cycle into four different phases as illustrated in Figure 44. Both the PWM signals $g_i(t)$ and $g_o(t)$ have the same magnitude in phase 1 and 3. Hence, the resulting $h_i(t)$ is a high amplitude constant voltage. Subsequently, the integrator integrates $h_i(t)$ and the resultant $h_o(t)$ is a ramp signal with a negative gradient with respect to the sign of $h_i(t)$ due to the inverting gain of the integrator. Once $h_o(t)$ increases or decrease through the respective threshold voltage of $+V$ and $-V$, $g_o(t)$ switches to its corresponding state. On the other hand, the opposite polarity in $g_i(t)$ and $g_o(t)$ (but equal in magnitude) during phase 2 and 4 results in $h_i(t) = 0V$. Consequently, $h_o(t)$ remains at the particular voltage level defined by the hysteresis threshold of the comparator until further switching of $g_i(t)$.

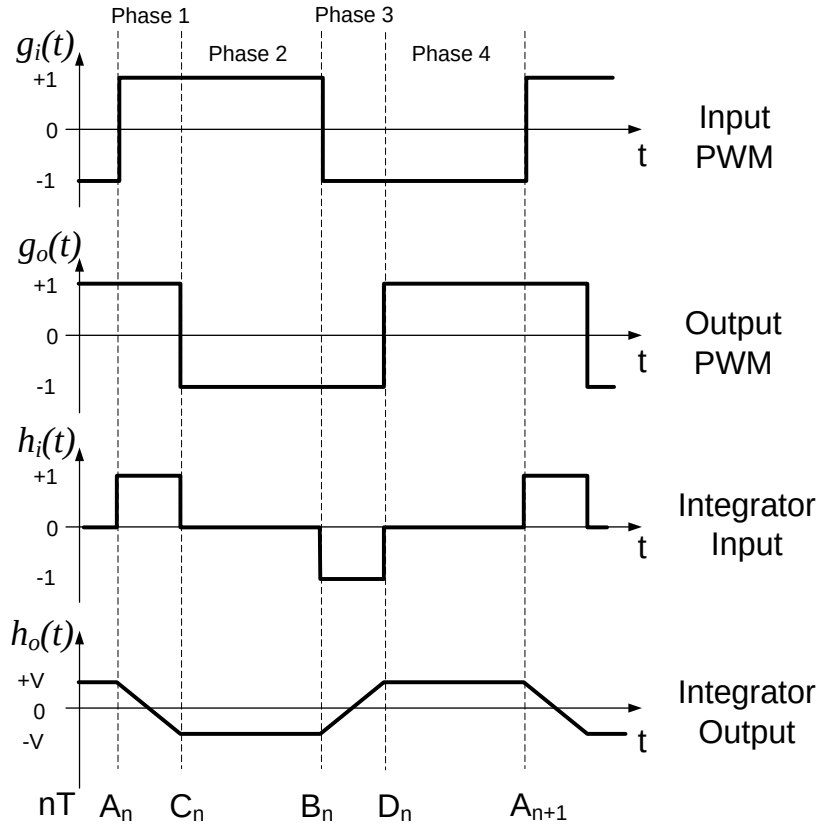


Figure 44. PWM input, PWM output, Integrator input and Integrator output of the proposed First-Order PWM feedback loop for Class-D amplifier power stage without error.

Under noise-free conditions, $g_o(t)$ is a precise replica of $g_i(t)$ with only a constant phase shift. This can be mathematically proofed by deriving the time domain expressions of the various signals using a similar approach that was introduced in [60].

With reference to the threshold voltages of the hysteresis comparator, the expression of $g_o(t)$ can be denoted as:

$$g_o(t) = \begin{cases} +1 & \text{when } h_o(t) > +V \\ -1 & \text{when } h_o(t) < -V \end{cases}, \quad (11)$$

where

+V = upper threshold voltage level,

-V = lower threshold voltage level.

As mentioned earlier, $g_i(t)$ is assumed to be generated by NSPWM scheme with a switching pulse period of T . Hence, the switching instants of $g_i(t)$ and $g_o(t)$ with reference to Figure 44 is denoted by (12). Table 3 summaries the expressions of $g_i(t)$, $g_o(t)$ and $h_i(t)$ for the time intervals between each switching instants A_n , B_n , C_n and D_n indicated in Figure 44.

$$\begin{aligned} A_n &= (nT + \alpha_n), & B_n &= (nT + \beta_n), \\ C_n &= (nT + \gamma_n), & D_n &= (nT + \delta_n). \end{aligned} \quad (12)$$

where

n is an integer,

$nT + \alpha_n$ = an up-switching instant when $g_i(t)$ switches to +1,

$nT + \beta_n$ = a down-switching instant when $g_i(t)$ switches to -1,

$nT + \gamma_n$ = a down-switching instant when $g_o(t)$ switches to -1,

$nT + \delta_n$ = an up-switching instant when $g_o(t)$ switches to +1.

Figure 43 shows that the expression for $h_o(t)$ is equivalent to:

$$h_o(t) = -G_1 \int h_i(t) dt \quad (13)$$

where G_I = DC gain of integrator.

Table 3. Input condition for each time interval.

	$A_n < t < C_n$ (Phase 1)	$C_n < t < B_n$ (Phase 2)	$B_n < t < D_n$ (Phase 3)	$D_n < t < A_{n+1}$ (Phase 4)
$g_i(t)$	+1	+1	-1	-1
$g_o(t)$	+1	1	-1	+1
$h_i(t)$	+1	0	-1	0
$h_o(t)$	$-G_I[t - (n + \alpha_n)T] + V$	$-V$	$-G_I[t - (n + \beta_n)T] - V$	$+V$

Figure 44 shows that the initial condition of phase 1 (when $t = nT + \alpha_n$) for $h_o(t)$ is $+V$. Thus,

$$h_o(A_n) = h_o(nT + \alpha_n) = V. \quad (14)$$

By substituting the initial condition of (14) into (13), $h_o(t)$ in phase 1 becomes:

$$h_o(t) = -G_I[t - (nT + \alpha_n)] + V \quad (15)$$

Figure 44 illustrates that $h_o(t)$ reaches $-V$ at $t = nT + \gamma_n$. Thus, the final condition for (15) is

$$h_o(C_n) = h_o(nT + \gamma_n) = -V. \quad (16)$$

The expression for the timing interval between $A_n < t < C_n$ can be found by substituting (16) into (15), thus,

$$[(nT + \gamma_n) - (nT + \alpha_n)] = C_n - A_n = \frac{2V}{G_I}. \quad (17)$$

Likewise, the expression for the timing interval between $B_n < t < D_n$ can be found by applying the similar approach,

$$[(nT + \delta_n) - (nT + \beta_n)] = D_n - B_n = \frac{2V}{G_I}. \quad (18)$$

Referring to [17], the mathematical representations of $g_i(t)$ and $g_o(t)$ can be written as:

$$g_i(t) = -1 + 2 \sum_{n=-\infty}^{\infty} H_n(t) \quad (19)$$

$$g_o(t) = 1 + 2 \sum_{n=-\infty}^{\infty} H'_n(t) \quad (20)$$

where $H_n(t) = H(t - (nT + \alpha_n)) - H(t - (nT + \beta_n))$

$H'_n(t) = -H(t - (nT + \gamma_n)) + H(t - (nT + \delta_n))$

$H(t)$ is a step function ($H(t) = 0$ for $t < 0$ and $H(t) = 1$ for $t > 0$)

With (17) and (18), (20) can be re-written as

$$\begin{aligned} g_o(t) &= 1 + 2 \sum_{n=-\infty}^{\infty} -H' \left(t - (nT + \alpha_n) - \frac{2V}{G_1} \right) + H' \left(t - (nT + \beta_n) - \frac{2V}{G_1} \right) \\ &= 1 - 2 \sum_{n=-\infty}^{\infty} H_n \left(t - \frac{2V}{G_1} \right) \end{aligned} \quad (21)$$

Comparing (21) against (19), it shows that $g_o(t)$ is an accurate duplication of its input ($g_i(t)$) with a constant time shift of $2V/G_1$. Put differently, the first-order design is theoretically linear with a condition that the delay of $2V/G_1$ does not cross over to the next input switching instant. In this way, the linearity of the output audio signal depends only on the quality of the input pulse width modulation scheme that was used, which is beyond the scope of this work. In order to satisfy such condition, the constant time shift between $g_i(t)$ and $g_o(t)$ are advised to be kept to its minimum possible value by maximizing the gain of G_1 as depicted in (21), and/or minimizing the hysteresis windows, V . In fact, doing so maximizes its NTF in (7), and thus, improving its theoretical PSRR performance. However, Figure 45 shows some constraints in maximizing G_1 , and minimizing the hysteresis windows. Figure 45(a) illustrates the case when $h_o(t)$ saturates at the positive supply rail while the PWM feedback loop is correcting for a negative PAE due to the excessively high gain of G_1 . On the other hand, a narrow hysteresis window might

contribute to output pulse splitting as shown in Figure 45(b) when the PWM feedback loop is compensating for a positive PAE in $g_o(t)$.

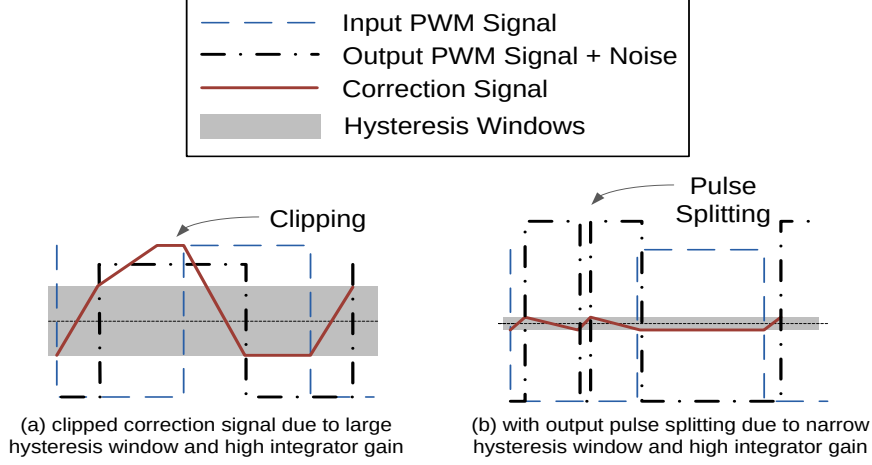


Figure 45. Simulated waveforms for a single supply First-Order PWM feedback loop for Class-D amplifier power stage

3.3.2 Causes of Inherent Harmonic Distortion for Second-Order PWM Feedback Loop

The Matlab Simulink model for the Second-Order PWM feedback loop is depicted in Figure 46. In this model, all the components, except for the integrator, are identical to that of its first-order counterpart in Figure 43. Instead, $h_o(t)$ are now obtained by adding up the first- and second-order integration of $h_i(t)$. As indicated in Figure 46, the first-order integrator gain is denoted as G_1 , whilst, the second-order integrator gain is denoted as G_2 . The NTF plot shown in Figure 39 reveals that the Second-Order PWM feedback loop can theoretically attain a much better supply rejection compared to its first-order counterpart. However, higher order feedback loop generally results in higher distortion in the output audio signal for Class-D amplifier applications [13, 21-23]. Thus, an investigation on the main sources of non-linearities specifically in the proposed second-order design will be discussed in Chapter 4.

Equation (22) denotes the transfer function of the second-order integrator depicted in Figure 37. By comparing this transfer function against Figure 46, it reveals the respective expressions for G_1 and G_2 , and are recorded in (23) and (24).

$$\frac{H_o(s)}{H_i(s)} = -\frac{(R_3(C_1 + C_2)s + 1)}{s^2 R R_3 C_1 C_2} = -\left(\frac{1}{s C R} + \frac{1}{s^2 R R_3 C_1 C_2} \right) \quad (22)$$

$$G_1 = -\frac{1}{C R} \quad (23)$$

$$G_2 = -\frac{1}{R R_3 C_1 C_2} \quad (24)$$

where $R = \frac{R_1 \times R_2}{R_1 + R_2}$ and $C = \frac{C_1 \times C_2}{C_1 + C_2}$

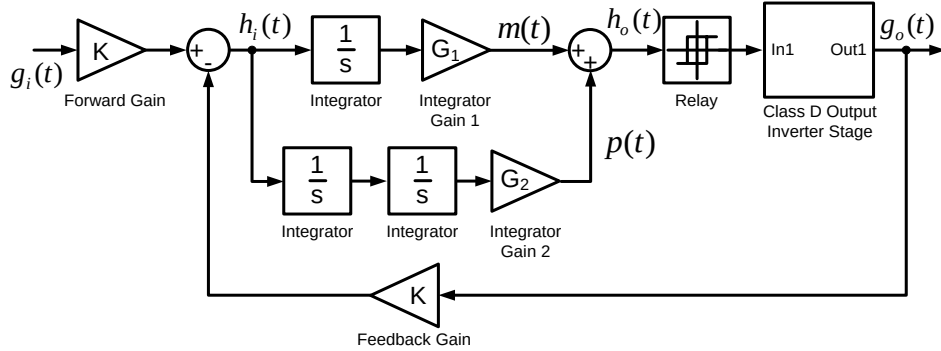


Figure 46. Matlab Simulink model of the proposed Second-Order PWM feedback loop

The relevant time domain waveforms for the proposed second-order PWM feedback loop with the absence of PAE in the output PWM signal is depicted in Figure 47(a). Likewise, the single PWM cycle is again divided into four phases depending on its input and output combinations. In this second-order PWM design, the first-order integrator output $m(t)$ is piecewise constant (phase 2 and 4) or linear in time (phase 1 and 3), and correspondingly, the second-order integrator output $p(t)$ is piecewise linear or quadratic in time.

The time domain analysis for the proposed First-Order design in the previous section was relatively easy due to the fact that the corresponding initial and final conditions for $h_o(t)$ at each of the phases are known, (to a good approximation), and are consistent for every PWM cycle regardless of the depth of modulation for $g_i(t)$ under noise-free conditions. However, the mathematical derivation for the second-order model is extremely tedious. For that reason, a highly comprehensive mathematical analysis quantifying the amount of inherent non-linearities in this second-order loop is covered in Chapter 4. It is found in Chapter 4 that for a sinusoidal audio input signal, $\sigma(t) = \sigma_0 \sin(\omega t)$, the audio output, $g^a(t)$, can be expanded as a Fourier sine series of odd harmonics:

$$g^a(t) = \sum_{k=0}^{\infty} G_{2k+1} \sin(2k+1)\omega t \quad (25)$$

where,

k is a positive integer,

ω is the angular frequency of the input audio signal

$$G_1 = \sigma_0 + O((\omega T)^2),$$

$$G_{2k+1} = O((\omega T)^2), \text{ and}$$

σ_0 is the output audio magnitude.

Equation (25) reveals that $g^a(t)$ contains the original $\sigma(t)$ with distortion of order $(\omega T)^2$. In other words, the corresponding audio output contains non-linearities that increase proportionally with the audio signal frequency. Broadly speaking, the above equation provides a better understanding of the non-linearities of the proposed second-order design; however, it is also helpful to intuitively analyse the causes of its harmonic distortion from engineering point of view.

Figure 47(b) and (c) illustrate the second-order integrator output waveforms, $h_o(t)$, with two different input modulation indexes. The difference between the instantaneous voltage at $t = A_n$ and that at $t = C_n$ is denoted as

$|\Delta V_{ACn}|$. On the other hand, the difference between the instantaneous voltage at $t = B_n$ and that at $t = D_n$ is denoted as $|\Delta V_{BDn}|$. It can be observed in Figure 47(b) and (c) that both $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ (consequently, the time durations of phase 1 and 3) vary proportionally with the modulation index of $g_i(t)$. In addition, the time durations in phase 1 and 3 in this case are not the same for every PWM cycles even when there is no power supply noise. This is very different from the case in its first-order counterpart. Thus, the $g_o(t)$ is not an exact replica of its $g_i(t)$. This is due to the time duration variations in phase 1 and 3, which is dependent on the modulation index of $g_i(t)$ in every single PWM cycles. In fact, the resultant harmonic distortion due to the time duration variations in phase 1 and 3 are not prominent for $g_i(t)$ with only low audio frequency components. The relatively small changes in pulse-width between the adjacent pulses lead to a small magnitude variations of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ with reference to the next consecutive cycle. On the other hand, the output harmonic distortion for higher audio frequency components increases because the duty ratio changes (consequently, the magnitude variations of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$) between adjacent PWM cycles for such PWM signals are significantly large.

Besides, pulse skipping in $g_o(t)$ is another source of non-linearities. This occurs when the corresponding switching of $g_i(t)$ at $t = B_n$ and $t = A_{n+1}$ switches before $h_o(t)$ hits the respective boundary of the hysteresis windows and causes $g_o(t)$ to switch at $t = C_n$ and $t = D_n$ respectively. For example, the switching order becomes $\dots A_n, B_n, C_n, D_n \dots$ instead of $\dots A_n, C_n, B_n, D_n \dots$ under normal operation. This happens when the values of $|\Delta V_{ACn}|$ or $|\Delta V_{BDn}|$ is sufficiently high and give rise to a relatively long time interval in phase 1 or phase 3 respectively. Put differently, non-linearities in the audio output signal would be expected for $g_i(t)$ with sufficiently high modulation index. In addition, this effect is cumulative to the following switching cycle. Thus, the

non-linearities caused by pulse skipping in $g_o(t)$ becomes severe for relatively low frequency input audio signal as there are large number of consecutive high duty ratio pulses in the resultant PWM signal.

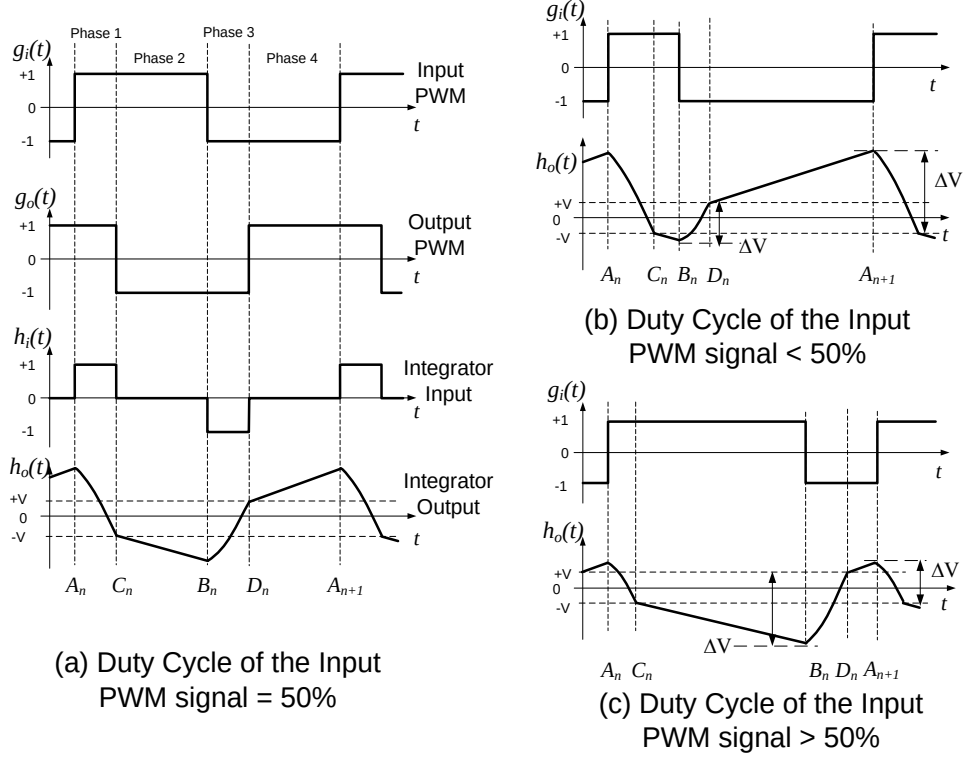


Figure 47. PWM input, PWM output, Integrator input and Integrator output of the Second-Order PWM feedback loop for Class-D amplifier power stage without supply error.

3.3.3 Proposed THD Enhancement of the Second-Order PWM Feedback Loop

One of the options to reduce the output non-linearities for the proposed second-order design is to decrease the gain of G_2 , hence, the maximum value of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ are reduced. In addition, the tendency of pulse skipping is also reduced. According to (22), (23) and (24), G_2 can be

reduced without affecting the gain of G_1 by increasing the value of R_3 depicted in Figure 38. However, doing so would shift the zero of its transfer function (22) to a lower frequency. For sufficiently high value of R_3 , the resultant NTF in (9) becomes first-order.

In fact, the observation in the previous section reveals that another possibility to improve the output signal linearity is to reduce the time interval of phase 1 and 3 by minimizing $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$. In addition, the added advantage of this is that the overall PSRR performance would not be affected as its NTF are preserved.

With the correction mechanism of the second-order PWM feedback loop, $|\Delta V_{ACn}|$ can be minimized by increasing the constant output pulse amplitude of $g_o(t)$ by a magnitude of V_c , thus, creating a DC error between the pulse amplitude of $g_i(t)$ and the pulse amplitude of $g_o(t)$. Consequently, the second-order PWM loop corrects for this intended constant amplitude error by producing a negative curve in phase 4. Hence, the resultant magnitude of $|\Delta V_{ACn}|$ is reduced. Thus, the time durations in phase 1 for each PWM cycles are also reduced. On the other hand, the magnitude of $|\Delta V_{BDn}|$ is reduced by lowering the pulse amplitude of $g_i(t)$ by the same magnitude to produce a positive curve in phase 2 as shown in Figure 48. However, the pulse splitting problem in $g_o(t)$ similar to the case in Figure 45(a) might occur if the magnitude of V_c is sufficiently large, and this is undesirable for power consumption and reliability consideration as discussed earlier. Generally speaking, the value of V_c should be optimized such that the resultant instantaneous voltage of $h_o(A_n)$ and $h_o(B_n)$ is around the respective voltage level of $+V$ and $-V$ for a 50% duty ratio input PWM signal with no PAE in $g_o(t)$ as depicted in Figure 48. Hence, the resulting $h_o(t)$ is similar to that of its first-order counterpart as shown in Figure 44, and the resultant time durations in phase 1 and 3 are shortened. Consequently, the harmonic

distortion is greatly reduced without affecting its NTF derived in (9) (and hence, the PSRR performance).

With reference to Figure 46 and Figure 48, the expressions for the governing switching conditions to achieve optimum V_c are

$$k_1 p(D_n) + k_2 m(D_n) = k_1 p(A_{n+1}) + k_2 m(A_{n+1}) = \frac{1}{2} \Delta, \quad (26)$$

$$k_1 p(B_n) + k_2 m(B_n) = k_1 p(C_n) + k_2 m(C_n) = -\frac{1}{2} \Delta. \quad (27)$$

From Figure 48, the expressions for $h_o(t)$ during each phase to obtain the optimum V_c according to the above criterion are summarized in Table 4. By solving the $h_o(t)$ equations in Table 4, it is found that V_c satisfy a cubic equation

$$2k_1^2 V_c^3 - k_1 k_2 T V_c^2 - 8k_2 V_c - 8k_1 \Delta = 0. \quad (28)$$

where Δ defines the hysteresis of the comparator.

Thus, the optimum value of V_c is obtained by finding the roots for (28). For example, with $k_1 = 2.67 \times 10^6$, $k_2 = 1.67 \times 10^{10}$, $T = 250 \mu s$, and $\Delta = 1.25$, the resultant roots for (28) are $V_c = 0.289$, $V_c = 2.3$, $V_c = -1.801$. In fact, the Matlab Simulink and Cadence Spectre simulation results reveal that the optimum value of V_c satisfying the above described condition is $V_c = 0.3$. The negative value of V_c is trivial and the high value of V_c results in pulse splitting problems, which is undesirable as discussed earlier.

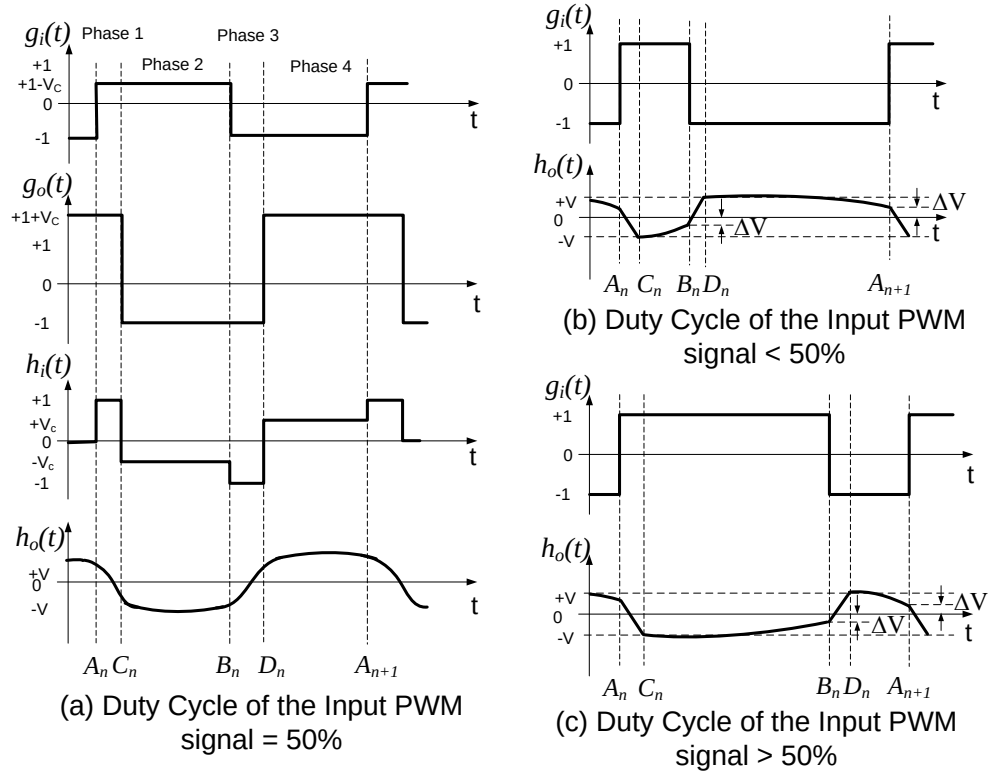


Figure 48. PWM input, PWM output, Integrator input and Integrator output of the proposed Enhanced Second-Order PWM feedback loop for Class-D amplifier power stage without supply error.

Table 4. Definition of the Second-Order PWM Feedback Loop Output at different phases within one PWM cycle.

	$A_n < t < C_n$ (phase 1)	$C_n < t < B_n$ (phase 2)
$s(t)$	$1 - V_c$	$1 - V_c$
$g(t)$	$1 + V_c$	-1
$h_i(t)$	$+1$	$-(\frac{1}{2})V_c$
$m(t)$	$m(t) = m(A_n) + (t - A_n)$	$m(t) = m(C_n) - \frac{1}{2}V_c(t - C_n)$
$p(t)$	$p(t) = p(A_n) + m(A_n)(t - A_n) + \frac{1}{2}(t - A_n)^2$	$p(t) = p(C_n) + m(C_n)(t - C_n) - \frac{1}{4}V_c(t - C_n)^2$

	$B_n < t < D_n$ (phase 3)	$D_n < t < A_{n+1}$ (phase 4)
$s(t)$	-1	-1
$g(t)$	-1	$1 + V_c$
$h_i(t)$	-1	$(\frac{1}{2})V_c$
$m(t)$	$m(t) = m(B_n) - (t - B_n)$	$m(t) = m(D_n) + \frac{1}{2}V_c(t - D_n)$
$p(t)$	$p(t) = p(B_n) + m(B_n)(t - B_n) - \frac{1}{2}(t - B_n)^2$	$p(t) = p(D_n) + m(D_n)(t - D_n) + \frac{1}{4}V_c(t - D_n)^2$

3.4 Simulation and Measurement Results

In this section, the circuit implementation of the proposed first- and second-order PWM feedback loop is realized using GF's 0.18 μm . The results obtained using Matlab Simulink Model (refer to Figure 43 and Figure 46) are verified with both Cadence Spectre simulation (refer to Figure 35 and Figure 38) as well as measurement results. The micrograph of the fabricated test chip is shown in Figure 49. The supply voltage is 3.3V and the maximum unclipped power efficiency with 16 Ω load condition is 89.5%.

For the convenience of the readers, the second-order negative feedback loop discussed in Chapter 3.3.2 is denoted as second-order design, whilst, the second-order feedback loop with enhanced THD performance as introduced in Chapter 3.3.3 is denoted as Enhanced second-order Design. The PSRR performance of the amplifier within the audible signal band (from 100 Hz to 20 kHz) is depicted in Figure 50. A 50% NSPWM signal with switching frequency of 400kHz was generated as an input signal to the feedback loop. To simulate the power supply noise, a sinusoidal signal was superimposed onto the positive supply rail of the Class-D amplifier output stage, thus, producing a PWM signal with a sinusoidal PAE on its positive amplitude. Figure 51 illustrates the test setup for PSRR measurement. A single tone sinusoidal signal is generated by a signal generator, and is added into the power supply rail of the output power stage (V_{DD2} in Figure 51) through the 'ADJ' pin of the Low-Dropout (LDO) voltage regulator (LM317). It is worth noting that no decoupling capacitor is connected to V_{DD2} when conducting PSRR measurement, so that the output of the test chip suffers from maximum supply ripple coupling. The PWM stage is implemented with an off-chip operational amplifier (OPA365). One of its inputs is connected to a function generator which generates a triangular carrier signal with a frequency of 400kHz. The other input of the operational amplifier is ac grounded with a dc voltage value equivalent to half

of its dc supply voltage to generate a 50% duty cycle PWM signal. In order to generate a clean reference PWM signal for the test chip, a separate LDO voltage regulator LM317 is used to provide the supply voltage to the PWM stage. The output signal is then captured with a spectrum analyser and the amplitude of the corresponding frequency component is recorded. The PSRR is then obtained by taking the amplitude ratio of the output signal and the sinusoidal test tone riding on the supply rail of the output power stage. In addition, it is worth noting that the integrator of the proposed PWM feedback loop was implemented with an ACBC-DPZ operational amplifier topology presented in [89], and it is powered by an additional LDO voltage regulator through V_{DD1} as depicted in Figure 51. To ensure optimum PSRR performance, decoupling capacitors are connected to the V_{DD} of the analog PWM stage and the V_{DD1} of the test chip. With reference to Figure 50(a) and (b), the followings are observed.

- 1) *The PSRR performance of the proposed designs follows the high-pass noise shaping behaviour in (7) and (9). As the frequency of the sinusoidal supply noise increases, the amount of supply rejection is reduced.*
- 2) *The main contributor to the slight difference in the simulation and measurement readings is the noise floor therein.*
- 3) *Figure 50(a) shows excellent agreements between the PSRR readings gathered from the Spectre simulation, the Matlab Simulink Model and the corresponding Noise Transfer Function plot as shown in (7). It is worth noting that the PSRR for the first-Order design is greater than -60 dB at 217 Hz.*
- 4) *Since both the second-order and the enhanced second-order designs share a common circuit topology, their noise transfer functions are basically the same. Thus, a similar PSRR performance is expected for both of these designs as shown in Figure 50(b).*

- 5) *Figure 50(b) indicates that the simulated PSRR at 217 Hz is close to -100 dB, while the measured PSRR shows -80 dB at the same frequency.*
- 6) *The open-loop gain of the operational amplifier was not included while deriving the noise transfer function (9). This explains the difference between the noise transfer function plot compared to the corresponding simulation and measurement results for the second-order designs at the lower audible frequency band.*

In short, the noise shaping effect of the proposed architecture effectively improves the PSRR performance of the traditional Class-D amplifiers. In addition, the second-order noise shaping effect contributes to a better PSRR results throughout the whole audible signal band compared to its first-order counterpart.

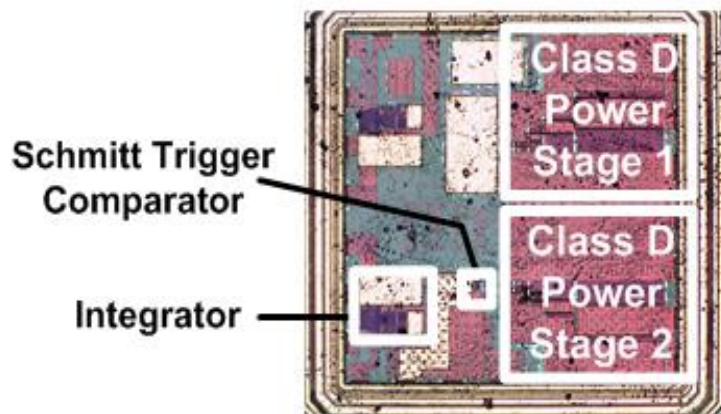


Figure 49. Die photo of the fabricated chip for the proposed Class-D amplifier power stage with PWM feedback

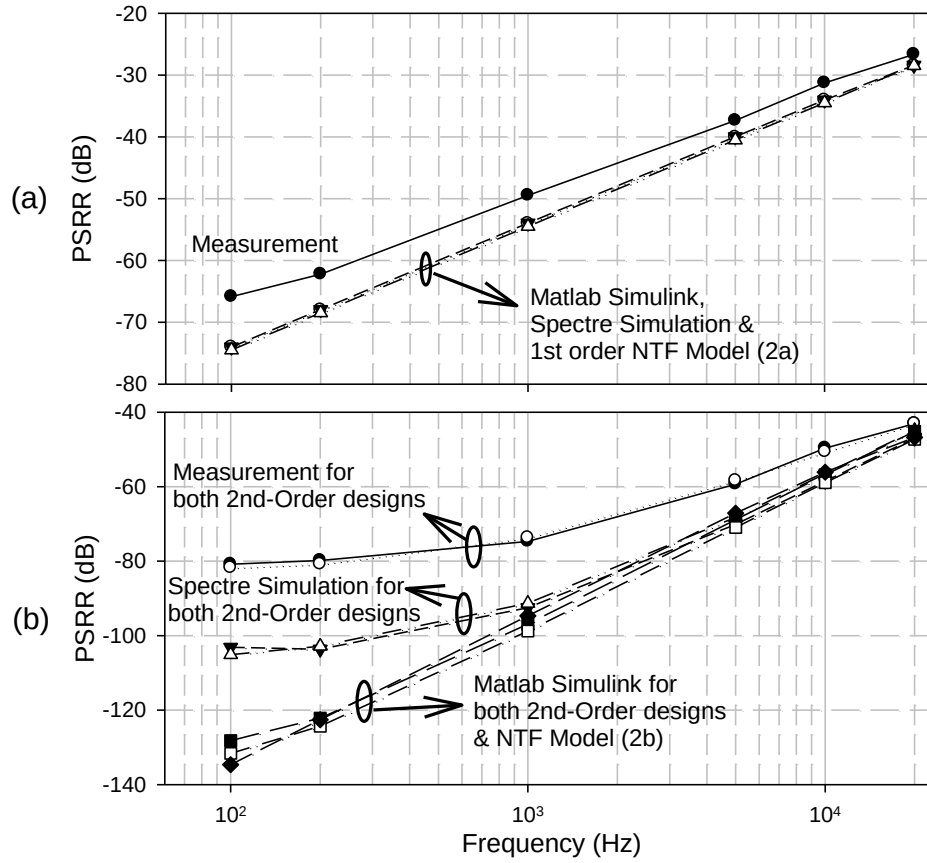


Figure 50. Comparison of PSRR for the proposed power stage with (a) 1st-Order PWM feedback loop, and (b) 2nd-Order PWM feedback loop.

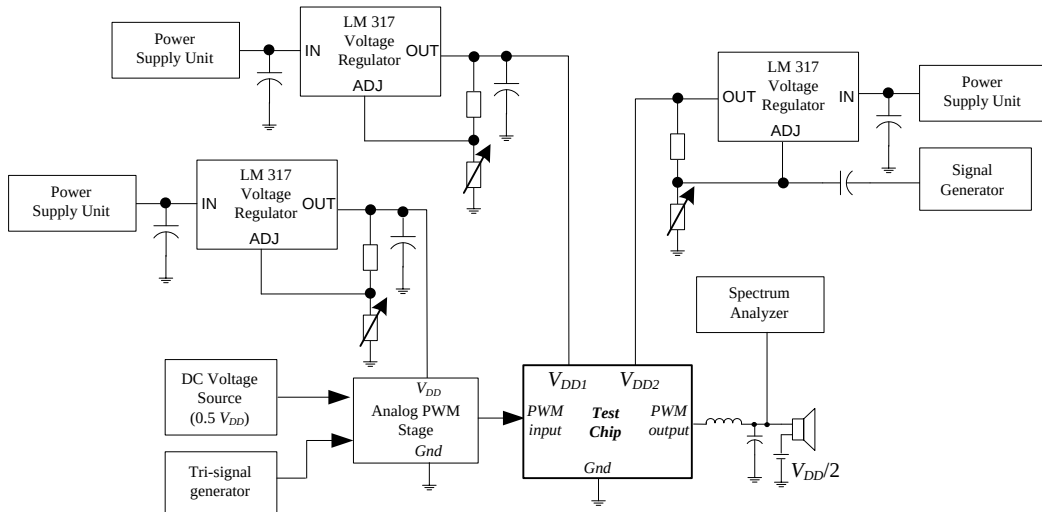


Figure 51. Testing environment for PSRR measurement

The THD plots for the proposed design across the whole audio signal frequency band (from 100Hz to 20 kHz) are depicted in Figure 52. In this test, a sinusoidal signal is modulated with NSPWM scheme with a carrier frequency of 400 kHz. In addition, a zero dead time CMOS Class-D amplifier output stage is used. The reason for using NSPWM modulation stage and a zero dead time Class-D amplifier power stage is to minimize any sources of non-linearities other than those inherently generated from the proposed designs itself.

Figure 53 depicts the THD measurement setup. In order to avoid internal coupling of the switching noise from the output power stage, three different LDO voltage regulators are used to power the PWM stage, the feedback circuitry (V_{DD1}) and the output power stage (V_{DD2}). In addition, decoupling capacitors are connected to the respective supply pin (V_{DD} for the off-chip PWM stage, V_{DD1} and V_{DD2} for the test chip) to further minimise any supply noise coupling to the output signal. As illustrated in Figure 53, the sinusoidal test tone in this test is generated by a signal generator and the analog PWM stage compares it with a triangular carrier signal to generate a reference PWM signal. This reference PWM signal serves as an input to the test chip. The demodulated output signal is then measured by a Spectrum analyser which computes the corresponding THD result. With reference to Figure 52, the followings are observed.

- 1) *Figure 52(a)-(b) shows excellent agreement between the THD plots for the Matlab Models and the Spectre Simulation.*
- 2) *Figure 52(a)-(b) depicts that the first-order design achieves lowest THD among the three. This is consistent with the earlier conclusion that the first-order PWM feedback loop generates no inherent THD to the audio output signal under ideal and noise-free conditions.*
- 3) *The simulated THD results in Figure 52(b) verify the prediction that THD for both of the second-order designs increases with the audio signal frequency.*

- 4) *Following 3), the THD plots reveal that the proposed enhancement technique leads to a significant reduction of non-linearities in the output audio signal.*
- 5) *The possible contributors to the deviations between the measured and simulated results are the noise floor, the quality of the LC low-pass filter, process variation, $1/f$ and thermal noise, power supply spike, ground bounce, substrate noise due to the high switching current, the linearity of the triangular carrier for the PWM stage, the rise and fall time of the PWM signal, and the quality of the measuring equipment etc, that was being used in the measurement.*
- 6) *The drop in the THD measurement results in the upper frequency range of the audible signal band is mainly due to the embedded low-pass filter within the measuring equipment. Hence, the harmonics of higher audio signal frequency were suppressed.*

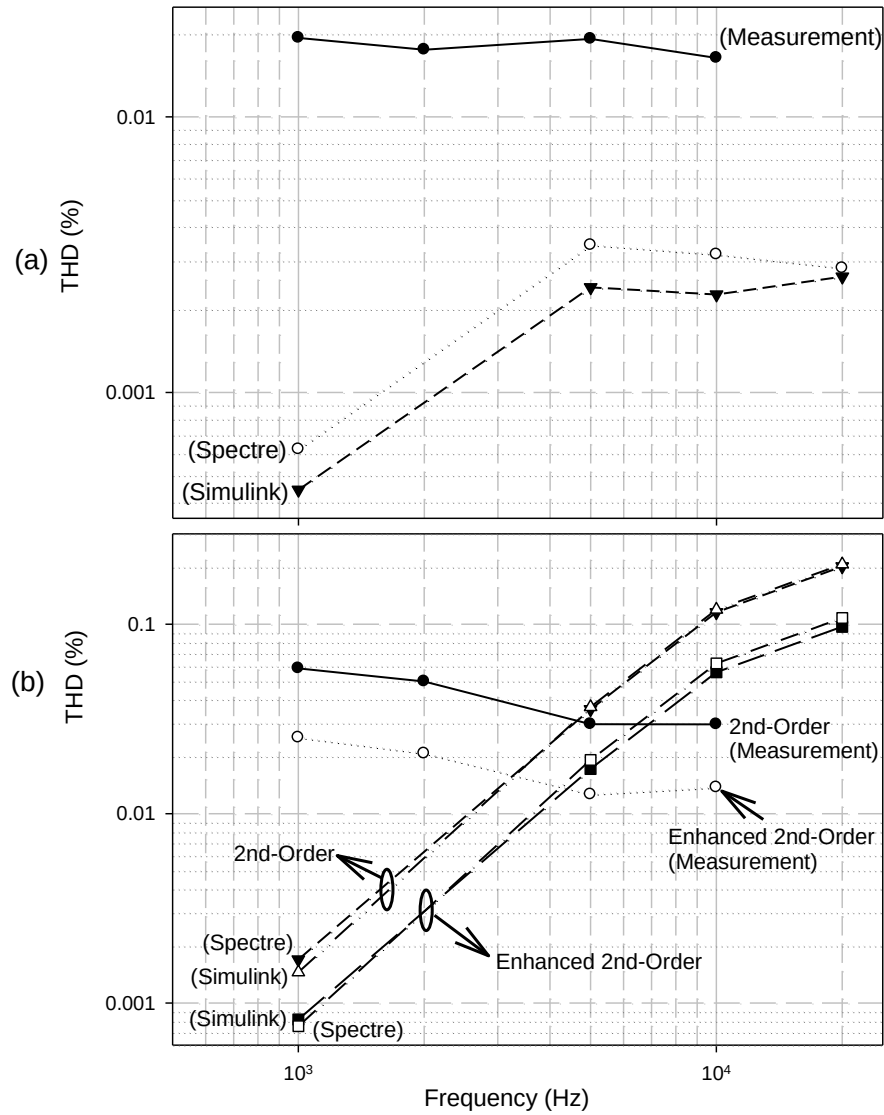


Figure 52. THD Performance over different input frequencies at input modulation index of 80% for (a) 1st-Order design, (b) 2nd-Order Designs

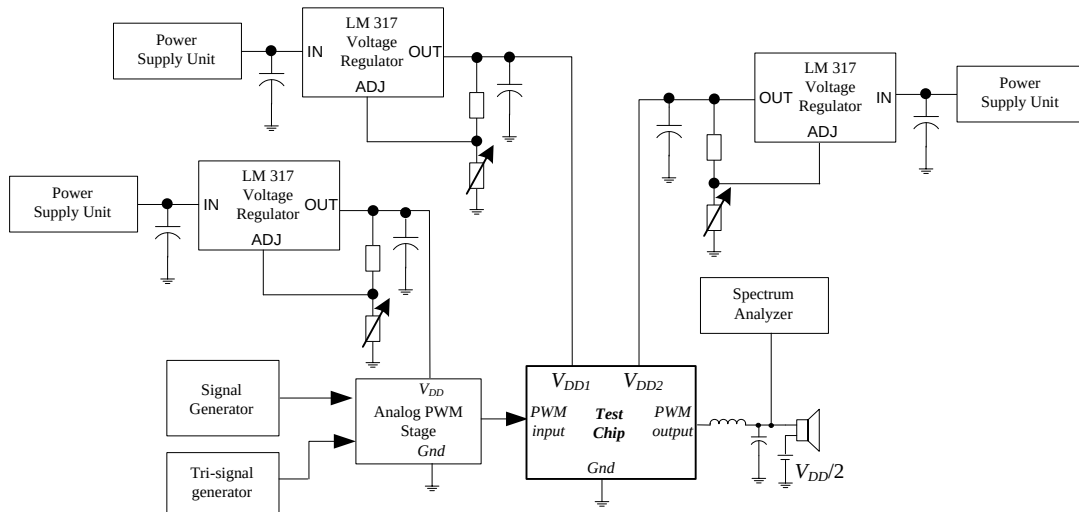


Figure 53. Testing environment for THD measurement.

Figure 54 shows the THD plots for the proposed designs versus a full output power range. The test setup are similar to the one described in the previous paragraph, except that the input sinusoidal test tone is fixed at 1 kHz. The followings are observed.

- 1) *In general, the Matlab model shows a much better THD as compared to both the Spectre simulated results as well as the measured THD results. This is mainly due to the fact that the actual operational amplifier behaviour and the process characteristics of the switching devices are not taken into account in modelling the proposed design in Matlab.*
- 2) *The simulation results in Figure 54(a) shows that the linearity of the output audio signal of the first-order design improves with increasing output power. Whilst, the simulated THD plot in Figure 54(b) shows the opposite trend.*
- 3) *From Figure 54(b), there is an abrupt increase in the simulated THD results for the second-order PWM design at output power level of 54 mW and above (correspondingly, the modulation index is greater than 0.9). The possible explanation for this is related to*

the large magnitudes of $|\Delta V_{ACn}|$ and $|\Delta V_{BDn}|$ as explained in the earlier section.

- 4) Following 3), both the simulated and measured THD plot for the enhanced second-order design is generally lower than those of the second-order counterpart. Furthermore, the THD plot for the enhanced second-order design shows a major linearity improvement in terms of THD at higher output power level as compared to its second-order counterpart.

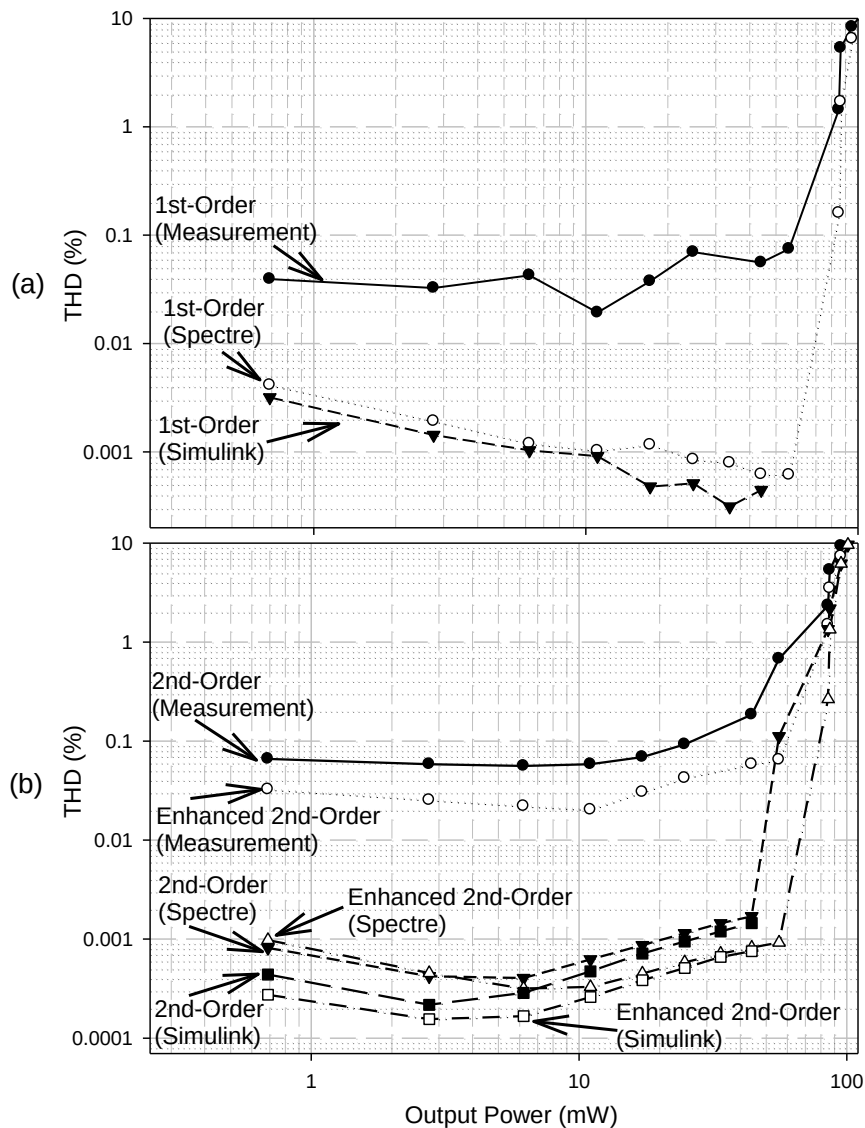


Figure 54. THD (%) Performance vs output power (mW) with input signal frequency of 1kHz for (a) 1st-Order design, (b) 2nd-Order Designs

Generally, the impedance for most headphone speakers varies as the input audio frequency varies. Hence, it is worth investigating the effects of load variations on the proposed designs. In this test, the load resistance is reduced by 4 times and the circuit setup are similar to those in the previous tests. The LPF bandwidth for the respective output load remained at 35 kHz. Figure 55 depicts the THD plots against different input audio frequencies with two different output load (4Ω and 16Ω).

- 1) *The simulated THD plot for the Open-Loop Class-D amplifier output power stage in Figure 55(a) depicts a huge variation in the THD results when the load is varied. The THD results with a 4Ω loading condition is approximately 17 times greater than that with a 16Ω loading condition. Hence, it reveals that higher harmonic distortion are resulted with decreasing output load resistance for Open-Loop Class-D amplifier.*
- 2) *Similar comparsion for the first-order design is shown in Figure 55(b). It can be observed that the output THD plot are still relatively sensitive to the output load variations. The THD plot for the 4Ω loading condition is close to 14x greater than that for the 16Ω output loading condition.*
- 3) *Following 2), the conclusion drawn from the mathematical expressions derived for the first-order design suggests that its THD performance are determined solely by the quality of the input switching signal. In fact, both the simulated and measured THD plots suggest that the non-linearities within the Class-D amplifier output stage also affects the THD of the output audio signal. The operating mechanism of the first-order design would not introduce any non-linearities to the audio output.*
- 4) *Figure 55(c) reveals that the load resistance variations have insignificant effects on the performance of both the second-order and the enhanced second-order PWM feedback loop. In other*

words, the second-order PWM feedback architecture are rather insensitive to the output load variations.

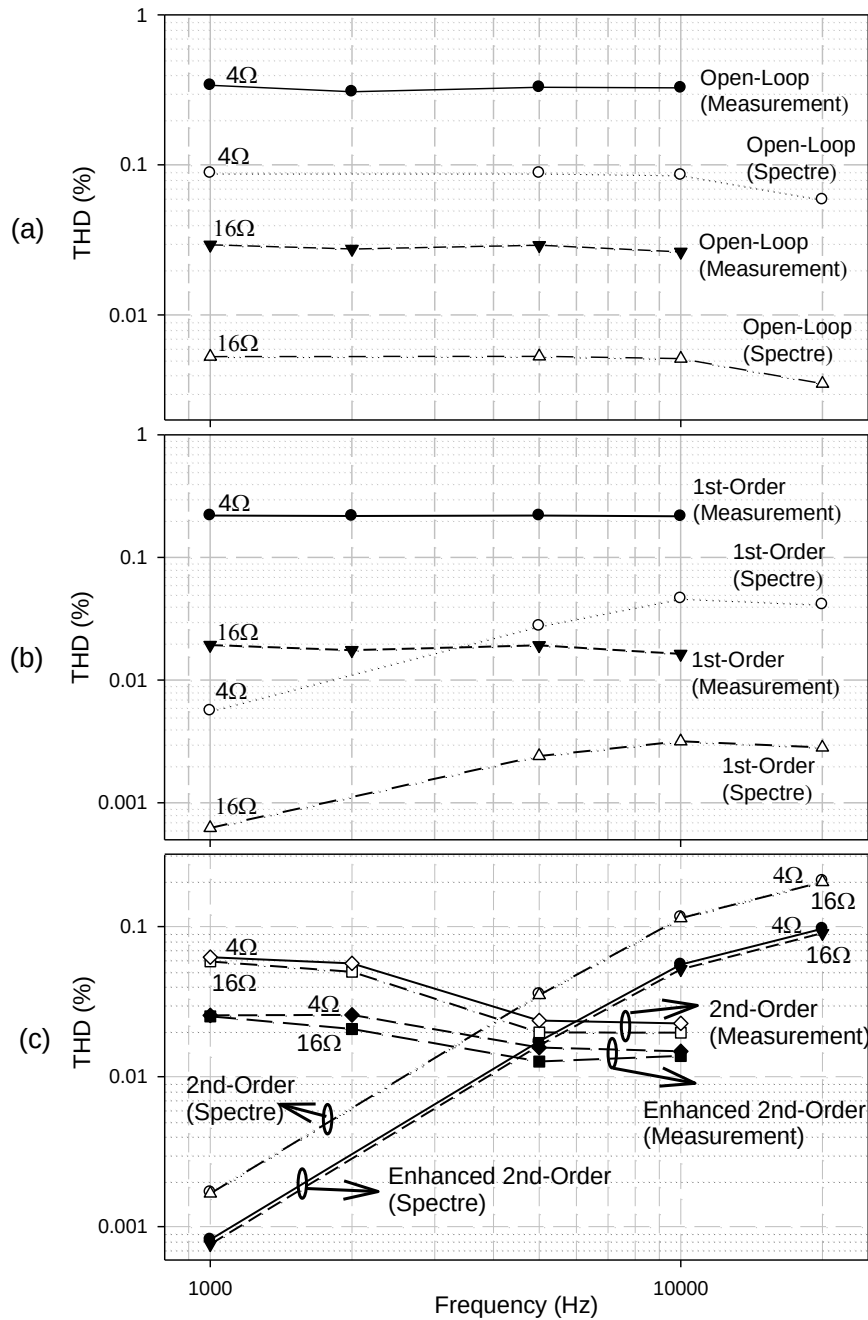


Figure 55. THD vs Frequency plot for different load resistance, R_L for (a) Open Loop Class-D amplifier power stage, (b) 1st-order design (c) 2nd-order designs

Figure 56 depicts the four corners simulation results for the proposed PWM feedback loop. The objective for this test is to investigate the effects of

transistor variations on the proposed PWM feedback architecture. Figure 56 shows that the sf condition depicts the worst case variation for the open-loop Class-D amplifier power stage. The corresponding THD results deviate from its typical condition by approximately 160%. On the other hand, the worst case THD variation for the first-order design is less than 30%, whilst the worst case THD variation for both of the second-order designs are no more than 20% under the four corners simulation test.

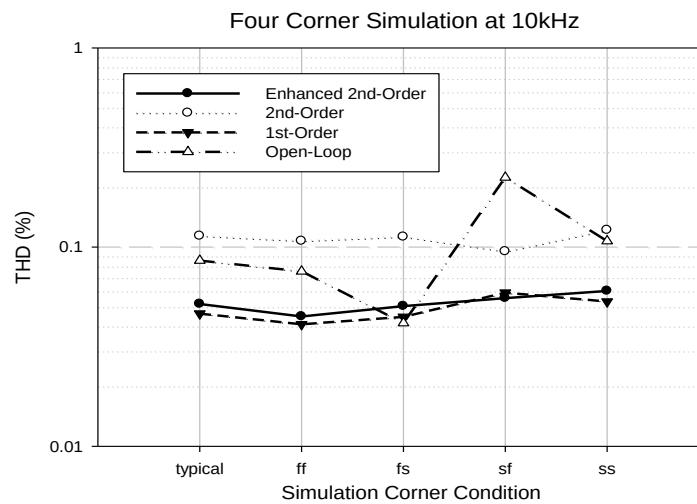


Figure 56. Four Corner simulation for input signal frequency of 10kHz

In summary, both the simulation and measurement results show that the THD readings for the first-order design is below 0.01% with properly sized output switching transistors. However, the load resistance variation have a relatively great impact on its THD performance. In addition, the PSRR measurement results at 217 Hz of the first-order design is only -60 dB, which is inadequate for today's mobile audio amplifier application. Conversely, the PSRR readings obtained from both of the proposed second-order designs are impressively high (the measured PSRR is about -80 dB at 217 Hz, while both the theoretical and simulated results shows more than -100 dB at the same frequency). Furthermore, the output load variations have negligible influence on output THD for the second-order designs. By applying the proposed technique to reduce the inherent harmonics distortion, the resultant THD

improves by more than 2 times. The simulated THD plots shows that the maximum THD obtained for the enhanced second-order design is below 0.1% across the whole audible signal band, and also, the full output power range. Therefore, the proposed enhanced second-order design has the best compromise of PSRR and THD performance.

Table 5 compares the performance of the proposed Second-Order design against some of the reported works in literature as well as some state-of-the-art designs in the industry.

The first three architectures have already been discussed in the literature review in Chapter 2. Although the comparison of these three architectures against the proposed design is not an apple-to-apple comparison, they are the closest match that could be found in literature. The supply voltage and power of the first two designs (the PEDEC architecture and BSEC architecture) are way too high compared to the proposed work. As these two designs are realized in discrete components, filtering capacitor can be inserted to improve the PSRR. On the other hand, the proposed is realized in a single-chip. Therefore, components counts are important in order to minimize the silicon real-estate. Hence, a more relevant comparison would be the PowerDAC design which was implemented in a single chip. For the commercially available product, the closest match that could be found is a product from Texas-Instrument (TI). The TAS 5602 from TI is a Closed-loop Class-D amplifier power stage with PSRR improvement. To the best of the author's knowledge, this is currently the only commercially available Class-D amplifier power stage with a Closed-loop architecture to improve its PSRR performance. However, the power stage voltage and the output power are much higher than the proposed design. Its low frequency PSRR is around 60dB, which is comparable to the proposed First-order design (refer to Figure 50). The PSRR of the proposed Second-order design is 30dB higher. Another product that is included in the table is BU7839GVW from ROHM Semiconductor. It is an open-loop design (without any negative feedback). Therefore, the respective data sheet does not contain any information on the

PSRR. It is worth noting that the switching frequency for most of the designs in Table 5 is around 400 kHz (except for the PowerDAC design), this is the typical switching frequency for audio amplifier.

The proposed design achieved one of the highest PSRR at 217Hz and a good THD performance. The results are comparable to the PowerDAC design. However, the high switching frequency in the PowerDAC design is one of the most critical shortcomings as compared to the proposed work.

Table 5. Performance comparison

Industrial Available Products							
	PEDEC (PCB)	BSEC (PCB)	Power DAC (IC)	Texa Instrument	ROHM Semi- conductor	This Work	
	1998	2004	1999	2008	2010	(2 nd Order)	
Technology:	-	-	0.5um CMOS (2PS,3AL)	TAS 5602	BU7839GVW	0.18 CSM CMOS	
Correction Stage Supply voltage:	5V	5V	5V	3.3	1.5V	3.3V	Simulation Measurement
Power Stage Supply Voltage	40V and -40V	80V	5V	10V-26V	2.5-3.0V	3.3V	3.3
Load (Ohms)	-	4	6.6	8(SE)	16	16	16
Switching Frequency	350kHz	-	1MHz	400kHz	400kHz	400kHz	400kHz
Output power:	350W	100W	2*1W	2W	-	70mW	52.8mW
Efficiency:	-	82%	70%	90%	-	89.50%	-
THD @ 1kHz	-	<0.2%	<0.112%	<0.04%	0.10%	<0.03%	<0.1%
PSRR @ 217Hz:	>40dB	-	>90dB	60dB	0	<90dB	80dB

3.5 Conclusions

A detailed mathematical analysis for the THD performance of the proposed first-order PWM feedback loop is presented. In addition, an instinctive way to understand the non-linearities generated within the second-order PWM feedback loop is also provided. With such understanding, its output harmonic distortion is then effectively reduced by creating a constant amplitude difference between the input and output switching pulses. The corresponding PSRR and THD results are verified using simulation tools such as Matlab Simulink, and Cadence Spectre Simulation. The designs are fabricated with Globalfoundries 0.18 μm CMOS process. The simulation results shows that the proposed enhanced second-order design attains more than -100 dB PSRR at 217 Hz, while the measured PSRR reading is -80 dB at the same frequency. In addition, the THD readings are less than 0.1% from 1 kHz to 20 kHz irrespective of any load condition and process variation. In other words, the proposed PWM feedback loop provides great PSRR and THD performance for Class-D amplifier power stage feedback applications. Hence, it is an ideal candidate for Class-D amplifier applications that require high PSRR and THD performance.

Chapter 4 Time Domain Analysis of Second- Order PWM-in / PWM-out Feedback Loop

In this chapter, a very detailed mathematical analysis on the harmonic distortion behavior of the proposed Second-Order PWM-in / PWM-out negative feedback loop discussed in the previous chapter is derived. Recently reported analysis in [87] had attempted to quantify the amount of inherent harmonic distortion for negative feedback loop in Class-D amplifiers application. However, such method is based on some form of quasi-stationary approximation. Such approximation always affects the precision of the analysis. On the contrary, this work provides an accurate and precise analysis method to provide a better understanding on the harmonics behavior of the proposed second-order PWM negative feedback loop. The mathematical analysis in this work involves iterative time domain integration of the amplitude difference between the input and output. The resulting difference equations algebraically relate the sampled values at specific time in each switching cycle. It is worth noting that this mathematical analysis does not involve any quasi-stationary approximation. A large portion of this chapter has been published in [90].

Figure 57 depicts the mathematical model of the proposed second-order PWM negative feedback loop which is similar to Figure 46. With this

mathematical model and the simulation data collected, a mathematical expression of the output signal is derived and verified. As the mathematical analysis involved negative feedback in a non-linear system (a negative feedback system with PWM input and PWM output signals), the mathematical expansion works are extremely complicated. Hence, the mathematical expansions works are done in collaboration with Professor Stephen M. Cox from the University of Nottingham (a mathematical expert) and the mathematical expansion works for the second-order PWM negative feedback loop are contributed by Prof Cox. After obtaining a closed form mathematical solution, the results obtained from the expression are compared against those obtained with Matlab simulation which was done by the author.

To be specific, the author has formulated the mathematical model for the proposed first-order design. Based on the mathematical model, the author has derived and solved a set of time domain mathematical expressions and presented the solution in Chapter 3. The author has also drawn some important conclusion relating to the linearity of the proposed first-order design based on the mathematical derivations. In this Chapter, the author has extended the time domain linearity analysis to the proposed second-order design based on similar analysis approach done on the proposed first-order design. The author has formulated a similar mathematical behavior model for the proposed second-order design as shown in Figure 57. After obtaining the closed form solution from Prof Cox., the author has verified the mathematical workings with Matlab simulation.

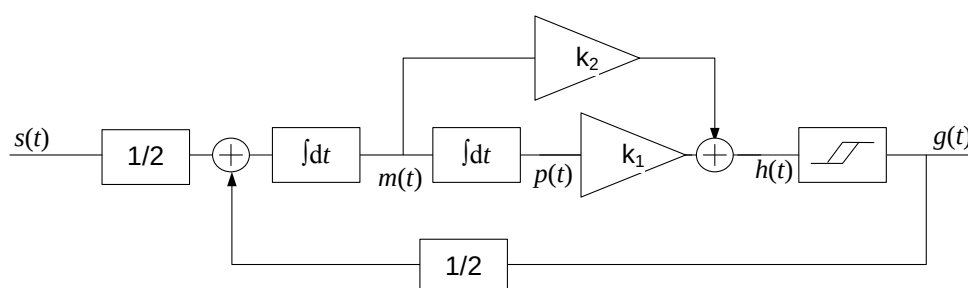


Figure 57. Mathematical modeling of the proposed PWM feedback loop

4.1 Mathematical Formulation

4.1.1 Input PWM Signal $s(t)$

To begin the analysis, the reference PWM input signal to the amplifier $s(t)$ has to be first characterized. The amplitudes of $s(t)$ are first normalized to be ± 1 . Also, $s(t)$ is assumed to be generated by an ideal symmetrical natural sampling PWM (NSPWM) modulator with minimum distortion to the input audio signal $\sigma(t)$. Due to the architecture of the proposed Second-Order direct PWM negative feedback loop, the input audio signal is inverted at its output. Consequently, the input audio signal applied to the PWM modulation stage should be negated. Therefore, the notation for the input audio signal becomes $-\sigma(t)$ in order to reproduce $\sigma(t)$ at the amplifiers output for analysis purposes.

To generate the input reference PWM signal, $-\sigma(t)$ is compared with a high-frequency triangular carrier wave $\theta(t)$ as depicted in Figure 58. Therefore,

$$s(t) = \begin{cases} +1 & \text{when } -\sigma(t) > \theta(t) \\ -1 & \text{when } -\sigma(t) < \theta(t) \end{cases} \quad (29)$$

where the carrier wave $\theta(t)$ can be found and as defined in [60]:

$$\theta(t) = \begin{cases} 1 - 4(t \bmod T)/T & \text{for } 0 < t \bmod T < \frac{1}{2}T \\ -3 + 4(t \bmod T)/T & \text{for } \frac{1}{2}T < t \bmod T < T \end{cases} \quad (30)$$

and $\theta(t)$ is a periodic signal with a period of T .

The down-switching times of $s(t)$ is denoted by $t = A_n$ (when $s(t)$ switches to -1). On the other hand, the up-switching times of $s(t)$ is denoted by $t = B_n$ (when $s(t)$ switches to +1). For any arbitrary integers n ,

$$s(t) = \begin{cases} +1 & \text{for } B_n < t < A_{n+1} \\ -1 & \text{for } A_n < t < B_n \end{cases} \quad (31)$$

Subsequently, the switching instances, A_n and B_n , can be further defined by introducing two new variables α_n and β_n .

$$A_n = (n + \alpha_n)T, \quad B_n = (n + \beta_n)T, \quad (32)$$

$$\text{where } 0 < \alpha_n < 1/2 < \beta_n < 1. \quad (33)$$

With (29) and (30), the down- and up-switching times of the input PWM signal is found by $\sigma(A_n) = \theta(A_n)$ and $\sigma(B_n) = \theta(B_n)$ respectively (as shown in appendix A). Hence,

$$A_n = nT + \frac{1}{4}T(1 - \sigma(A_n)), \quad B_n = nT + \frac{1}{4}T(3 + \sigma(B_n)), \quad (34)$$

To reproduce a high-quality audio signal, the frequency ratio between the carrier signal to that of the input audio signal must be sufficiently high [60]. Typically, the audio frequencies range from 20Hz – 20kHz, while the practical carrier frequency may be around 400kHz or higher.

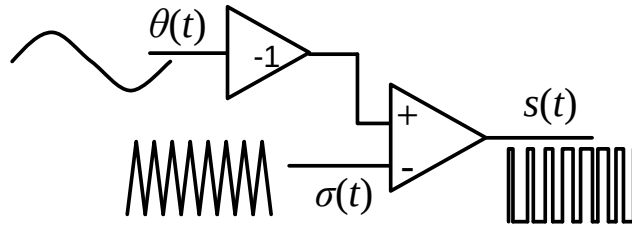


Figure 58. The generation of input PWM signal, $s(t)$

4.1.2 Circuit Operation and the Respective Signal Representation

The output of the Second-Order PWM negative feedback amplifier is a PWM signal $g(t)$ which normally switches between two voltages (i.e. the power supply rails) that may vary with time due to the potential power supply ripples. Thus, these two voltages should be expressed mathematically as a function of time, $V(t)$ and $W(t)$. In other words, $g(t)$ switches between $V(t)$ and $-W(t)$. In noise-free conditions, $V(t) = W(t) = 1$. To simplify the analysis, it is helpful to introduce the functions $v(t)$ and $w(t)$ such that

$$V(t) = \frac{d^2 v(t)}{dt^2}, \quad W(t) = \frac{d^2 w(t)}{dt^2}, \quad (35)$$

Next, the output down- and up-switching times are denoted by C_n and D_n , and therefore, $g(t)$ is defined as:

$$g(t) = \begin{cases} V(t) & \text{for } D_n < t < C_{n+1} \\ -W(t) & \text{for } C_n < t < D_n \end{cases} \quad (36)$$

During normal operation as depicted in Figure 59, the output $g(t)$ switches to $V(t)$ when the combined integrator output $h(t)$ increases and crosses the upper threshold value ($\Delta/2$) of the Schmitt trigger comparator at $t = D_n$. It then remains at $V(t)$ until the input switches its state at $t = A_{n+1}$. Once the difference integrator senses the change in the input polarity, $h(t)$ starts decreasing. The output $g(t)$ then switches to $-W(t)$ once $h(t)$ crosses the lower threshold value ($-\Delta/2$) at $t = C_{n+1}$ and stays in the state until $h(t)$ increases through $\Delta/2$ again in the next PWM cycle. In short, the switching conditions of the output $g(t)$ are dependent on $h(t)$ and the switching operation repeats itself from one PWM cycle to the next. Hence, the switching conditions for the output $g(t)$ in terms of $h(t)$ are described as:

$$h(C_n) = -\frac{1}{2}\Delta, \quad h(D_n) = \frac{1}{2}\Delta, \quad (37)$$

where $h(t) = k_1 p(t) + k_2 m(t)$.

Note that $m(t)$ and $p(t)$ are the output of the First- and Second-Order integrator respectively, which satisfy the following differential equations:

$$\frac{dm}{dt} = \frac{s(t) + g(t)}{2}, \quad \frac{dp}{dt} = m, \quad (38)$$

In order to provide negative feedback to the system, both the First- and Second-Order integrator gain (k_2 and k_1 respectively) must be negative such that

$$k_1, k_2 < 0 \quad (39)$$

For the rest of this chapter, the parameter values depicted in Table 6 would be utilized for illustration of the mathematical results in a specific case.

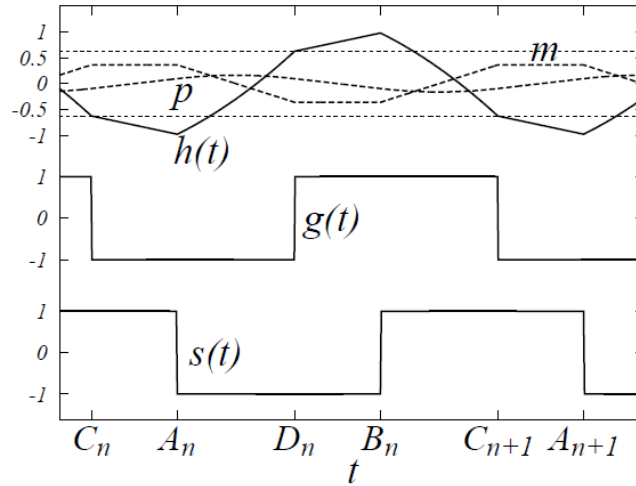


Figure 59. Relevant waveforms for the mathematical model in Figure 57 under noise-free conditions

Table 6. Typical parameter values that is being used in the numerical example through this thesis

$T(s)$	k_1	k_2	Δ
2.5×10^{-6}	-1.85×10^{12}	-2.22×10^6	1.25

4.1.3 An Illustration of the Normal Operation of the Amplifier

Figure 47 illustrates the normal operation of the proposed direct PWM negative feedback loop with constant and balanced power supply rails. The first-order integrator output $m(t)$ is alternately piecewise constant and linear in time; and correspondingly, the output of the second-order integrator $p(t)$ is alternately piecewise linear and quadratic in time. The down- and up-switching times (A_n and B_n respectively) of $s(t)$ depend on the input audio signal. On the other hand, the down- and up-switching times (C_n and D_n) of $g(t)$ are determined by the combined output of the First- and Second-Order integrator, $h(t)$, decreasing and increasing to the corresponding thresholds level ($\pm\Delta/2$) respectively, denoted by dotted lines in Figure 59. It can be observed that for each down-switching of $s(t)$ at $t = A_n$ generates a subsequent up-switching of $g(t)$, at $t = D_n$; similarly, each up-switching of $s(t)$ at $t = B_n$ produces a subsequent down-switching of $g(t)$ at $t = C_n$. Hence, the Second-Order PWM feedback loop inverts the audio signal at the amplifier's output as mentioned in the earlier part of this chapter.

4.1.4 A Brief Discussion of Output Pulse-skipping

In the case of extremely large input audio signal amplitude near clipping conditions, the output $g(t)$ might experience some pulse-skipping due to the corresponding short pulse durations in the resultant $s(t)$. As a consequence, $s(t)$ switches before $h(t)$ crosses the corresponding threshold voltage set by the hysteresis comparator, and thus, no switching occurs at $g(t)$. This is very undesirable as it degrades the quality of the amplified audio

output signal. In fact, the definition of α_n, β_n above and the condition defined in (33) is valid only when there is no occurrence of pulse skipping in $g(t)$. For the case of pulse skipping, the definitions of α_n and β_n have to be redefined and are given in (40). A more detailed discussion will be covered in the later part of this chapter.

$$\alpha_n = (A_n \bmod T)/T, \quad \beta_n = (B_n \bmod T)/T, \quad (40)$$

It is worth noting that with no pulse skipping occurring in $g(t)$, the definitions in (40) are actually identical to (32). The analysis throughout this chapter is derived on the basis of zero pulse skipping occurrence in $g(t)$.

4.2 Derivation of Difference Equations for Iteration of the Mathematical Model

The objective of this section is to derive a system of numerical solutions to iterate the state of the amplifier from one input switching period to the next. This is done by solving the ODEs defined in (38) successively between the input and output switching intervals. To facilitate the analysis, it is useful to mathematically define the state of the amplifier at time A_{n+1} in terms of its state at time A_n . The switching sequence governing the normal operation of the PWM negative feedback loop depicted in Figure 47 is defined in (41). With that, the equations in (38) for each of the inter-switching interval shall be investigated in turns.

$$\dots < C_n < A_n < D_n < B_n < C_{n+1} < \dots \quad (41)$$

During the interval $A_n < t < D_n$, $s(t) = -1$ and $g(t) = -W(t) = -w'(t)$.

By integrating (38) across this interval, the followings are obtained.

$$m(D_n) = m(A_n) - \frac{1}{2}(D_n - A_n) - \frac{1}{2}(w'(D_n) - w'(A_n)) \quad (42)$$

and

$$\begin{aligned} p(D_n) = & p(A_n) + m(A_n)(D_n - A_n) - \frac{1}{4}(D_n - A_n)^2 \\ & - \frac{1}{2}[w(D_n) - w(A_n) - w'(A_n)(D_n - A_n)] \end{aligned} \quad (43)$$

In the interval $D_n < t < B_n$, $s(t) = -1$ and $g(t) = V(t) = v'(t)$. Again, integrating (38) across this interval with the corresponding input conditions, the following expressions are obtained.

$$m(B_n) = m(D_n) - \frac{1}{2}(B_n - D_n) + \frac{1}{2}(v'(B_n) - v'(D_n)) \quad (44)$$

and

$$\begin{aligned} p(B_n) = & p(D_n) + m(D_n)(B_n - D_n) - \frac{1}{4}(B_n - D_n)^2 \\ & + \frac{1}{2}[v(B_n) - v(D_n) - v'(D_n)(B_n - D_n)] \end{aligned} \quad (45)$$

In the interval $B_n < t < C_{n+1}$, $s(t) = 1$ and $g(t) = V(t) = v''(t)$. Hence, integrating (38) across this interval,

$$m(C_{n+1}) = m(B_n) + \frac{1}{2}(C_{n+1} - B_n) + \frac{1}{2}(v'(C_{n+1}) - v'(B_n)) \quad (46)$$

and

$$\begin{aligned} p(C_{n+1}) = & p(B_n) + m(B_n)(C_{n+1} - B_n) + \frac{1}{4}(C_{n+1} - B_n)^2 \\ & + \frac{1}{2}[v(C_{n+1}) - v(B_n) - v'(B_n)(C_{n+1} - B_n)] \end{aligned} \quad (47)$$

In the interval $C_{n+1} < t < A_{n+1}$, $s(t) = 1$ and $g(t) = -W(t) = -w'(t)$. Hence, integrating (38) across this interval,

$$m(A_{n+1}) = m(C_{n+1}) + \frac{1}{2}(A_{n+1} - C_{n+1}) - \frac{1}{2}(w'(A_{n+1}) - w'(C_{n+1})) \quad (48)$$

and

$$\begin{aligned} p(A_{n+1}) = p(C_{n+1}) + m(C_{n+1})(A_{n+1} - C_{n+1}) + \frac{1}{4}(A_{n+1} - C_{n+1})^2 \\ - \frac{1}{2}[w(A_{n+1}) - w(C_{n+1}) - w'(C_{n+1})(A_{n+1} - C_{n+1})] \end{aligned} \quad (49)$$

To facilitate the derivation, it is useful to define the following notations as:

$$m_n = m(A_n), \quad p_n = p(A_n). \quad (50)$$

To solve for the ODEs in (38) at A_{n+1} in terms of A_n , the intermediate terms of $m(t)$ and $p(t)$ at times $t = D_n$, B_n and C_{n+1} shall be eliminated by utilizing the equations (42) to (49). Hence, the following set of equations for both of the integrator outputs at the input switching instant A_{n+1} can be obtained (refers to appendix B).

$$\begin{aligned} m_{n+1} &= m_n - (D_n - A_n) + (C_{n+1} - B_n), \\ p_{n+1} &= p_n + m(A_n)T - \frac{1}{2}(D_n - A_n)(A_{n+1} + T - D_n) \\ &\quad + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1}) \end{aligned} \quad (51)$$

The input switching instants A_n and B_n in (51) can be easily obtained using equation (34). On the other hand, the output switching instants D_n and C_{n+1} in (51) can be obtained from the two switching conditions as described in (52) and (53) below.

$$k_1 p(D_n) + k_2 m(D_n) = \frac{\Delta}{2} \quad (52)$$

where $m(D_n)$ and $p(D_n)$ can be found from (42) and (43), and from

$$k_1 p(C_{n+1}) + k_2 m(C_{n+1}) = -\frac{\Delta}{2} \quad (53)$$

where $m(C_{n+1})$ and $p(C_{n+1})$ can be found using (42) – (47).

In conclusion, the input switching times A_n and B_n , and the equations (51) – (53) are sufficient to obtain the iteration of the amplifier state forwards in time, as long as condition (41) is satisfied.

4.3 Solution for Steady-state Input

Before proceeding further, it is worth noting that the state of the amplifier repeats itself at every PWM period for a steady-state input signal (i.e. constant audio input). Mathematically, a steady-state input can be recognized as having an constant duty cycle input PWM signal with period of T , and its switching instances satisfy $A_{n+1} = A_n + T$ and $B_{n+1} = B_n + T$. In other words, the input PWM signal is periodic with period T with its average voltage corresponding to a constant (DC) audio input value $\sigma(t) = \sigma_0$. To have a better understanding of the behavior of the proposed PWM negative feedback loop, the mathematical analysis for steady-state input conditions is first investigated.

To facilitate the mathematical derivation, the input switching instants defined in (32) are rearranged and solved together with (34) for the condition of constant audio input σ_0 . Additionally, two new variables (γ_n and δ_n) relating the output switching instants are introduced in (54) in a similar manner.

$$\begin{aligned}
\alpha_n &= \frac{A_n - nT}{T} = \frac{1}{4}(1 - \sigma_0), & \beta_n &= \frac{B_n - nT}{T} = \frac{1}{4}(3 + \sigma_0), \\
\gamma_n &= \frac{C_n - nT}{T}, & \delta_n &= \frac{D_n - nT}{T},
\end{aligned} \tag{54}$$

With reference to (41), the following relationship is defined.

$$\gamma < \alpha < \delta < \beta < \gamma + 1 \tag{55}$$

4.3.1 Balanced, Constant Power Supply

Under the normal operating condition with balanced and constant power supply rails (i.e. $V=1$ and $W=1$), equations (51)-(53) are solved to obtain the followings solutions (see Appendix C for the derivation of δ and M)

$$\delta = \frac{1}{2}(1 - \sigma_0) + \gamma \tag{56}$$

$$m(A_n) = \frac{1}{8}T(1 + \sigma_0)(1 - \sigma_0 + 4\gamma) \tag{57}$$

$$p(A_n) = \frac{1}{64k_1}T(1 - \sigma_0 + 4\gamma)\{k_1T[1 - \sigma_0 - 4\gamma(1 + 2\sigma_0)] - 8k_2\sigma_0\} \tag{58}$$

where γ satisfies the quadratic equation below:

$$\gamma^2 + \left\{ \frac{2k_2}{k_1T} - \frac{\sigma_0(1 - \sigma_0)}{2} \right\} \gamma + \frac{2\Delta}{k_1T^2} + \frac{1 - \sigma_0}{16k_1T} [8k_2 - k_1T(1 - \sigma_0)(1 + 2\sigma_0)] = 0 \tag{59}$$

Equation (55) suggests that the relevant root for (59) must satisfy the switching conditions of $\beta - 1 < \gamma < \alpha$. In fact, the inequality $\beta - 1 < \gamma$ is always true. However, the inequality $\gamma < \alpha$ can only be fulfilled if the following condition is met.

$$\Delta < \frac{1}{8}T(1 - \sigma_0)(-4k_2 + k_1T\sigma_0(1 - \sigma_0)) \equiv f(\sigma_0) \tag{60}$$

Likewise, the switching condition of $\alpha < \delta < \beta$ in (55) must be maintained when finding the relevant root from (59). Again, the condition of $\alpha < \delta$ is always true, while the condition $\delta < \beta$ can be satisfied only if

$$\Delta < \frac{1}{8}T(1+\sigma_0)(-4k_2 - k_1T\sigma_0(1+\sigma_0)) \equiv f(-\sigma_0). \quad (61)$$

By substituting the minimum and the maximum values in the permitted input range for σ_0 into the right-hand side of (60) (with $\sigma_0 = -1$) and (61) (with $\sigma_0 = 1$) respectively, the following inequality for Δ can be found.

$$\Delta < -k_2T - \frac{1}{2}k_1T^2 \quad (62)$$

For any fixed values of Δ satisfying (62), an input amplitude threshold σ_c satisfying (60) and (61) can be found with the conditions of $-1 < \sigma_0 < \sigma_c$ and $-\sigma_c < \sigma_0 < 1$ respectively. The value of σ_c is determined by substituting $\sigma_0 = \sigma_c$ into (60). It is worth noting that σ_c must be greater than 0 in order to fulfill (60) and (61) simultaneously, i.e.,

$$0 < \Delta < -\frac{1}{2}k_2T \quad (63)$$

In other words, the switching sequence in (41) is satisfied as long as the input amplitude falls within the range of $-\sigma_c < \sigma_0 < \sigma_c$. In fact, the switching order in (41) must be maintained in order to preserve the quality of the input audio signal at the amplifier's output. Once the ordering in (41) is disturbed, the quality of the output signal degrades significantly. Thus, it is very important to satisfy both (60) and (61) simultaneously, and to ensure that the switching order in (41) is always preserved. In addition, it is always desirable to keep $|\sigma_c|$ as large as possible to maintain the widest possible range of σ_0 . Figure 60 depicts the three possible graphs for $f(\sigma_0)$ defined in the right hand side of the inequality (60) for $\sigma_0 \geq 0$. Amongst these three possibilities, condition (c) should be well avoided as it conflicts with (63). Figure 60 suggests

that condition (a) for $f(\sigma_0)$ have no local maxima or minima. Thus, by analyzing the first derivative of (60)

$$f'(\sigma_0) = \frac{1}{2}k_2T + \frac{1}{8}k_1T^2(1-\sigma_0)(1-3\sigma_0), \quad (64)$$

the following condition must be met.

$$-k_1T < -12k_2T^2 \quad (65)$$

In order to gain more insight into the case for $\sigma_0 > \sigma_c$, the analysis has to be re-worked and the switching order shown in (41) is substituted with

$$\dots < A_n < C_n < D_n < B_n < A_{n+1} < \dots \quad (66)$$

The amplifier iteration from $t = A_n$ to $t = A_{n+1}$ in (51) is reformulated with reference to the switching order in (66). Together with (52) and (53), the new expression for $m(A_n)$ and δ under the condition $\sigma_0 > \sigma_c$ is

$$\delta = \frac{1}{2}(1-\sigma_0) + \gamma, \quad (67)$$

$$m(A_n) = \frac{1}{8}T(1-\sigma_0)(3+\sigma_0-4\gamma) \quad (68)$$

where γ now satisfies a linear equation with the following solution

$$\gamma = \frac{-16\Delta + T(1-\sigma_0)(-8k_2 + k_1T(1-\sigma_0^2))}{4k_1T^2(1-\sigma_0)^2} \quad (69)$$

(The expression for $P(A_n)$ in this case is considerably more complicated than the one derived in (58), thus, it is not recorded here.) Likewise, the switching order for the case of $\sigma_0 < -\sigma_c$ is re-defined in (70), and the derivation details are not shown here.

$$\dots < C_n < A_n < B_n < D_n < C_{n+1} < \dots \quad (70)$$

In all the three segments of input amplitude (namely $-1 < \sigma_0 < -\sigma_c$, $-\sigma_c < \sigma_0 < \sigma_c$, and $\sigma_c < \sigma_0 < 1$), the output is a constant duty ratio PWM signal with an average value of

$$\langle g(t) \rangle = [+1 \times (\gamma + 1 - \delta)] + [-1 \times (\delta - \gamma)] = \sigma_0, \quad (71)$$

which is the exact replica of the constant input audio signal. In other words, any time varying audio signal $\sigma(t)$ should be expected at the output of the amplifier by low-pass filtering the output PWM signal $g(t)$ if the maximum audio signal frequency is sufficiently lower than the switching frequency of $g(t)$.

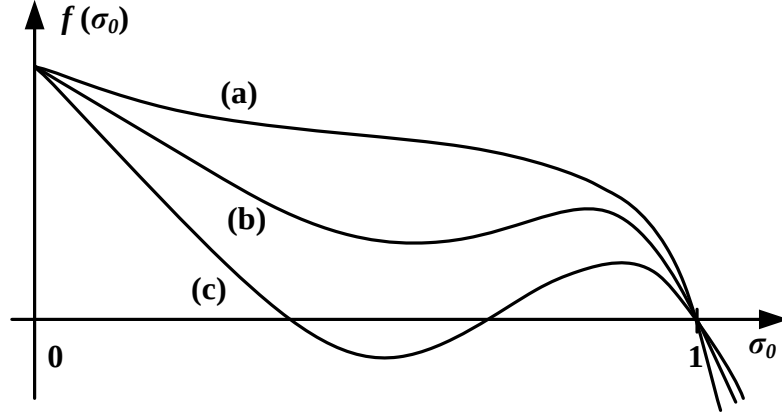


Figure 60. Schematic illustration of the three possible forms of $f(\sigma_0)$, for $\sigma_0 \geq 0$ in (60)

4.3.2 Unbalanced, Constant Power Supply

For the case of constant, but unbalanced power supply rails where $V \neq 1$ and/or $W \neq 1$, the output switching instant can be derived as

$$\delta = \frac{V - \sigma_0}{V + W} + \gamma \quad (72)$$

(For consistency, the range of audio input amplitude of σ_0 is now limited to $-W < \sigma_0 < V$.) Therefore, the average of the amplifier output for unbalanced power supply is

$$\langle g(t) \rangle = [V \times (\gamma + 1 - \delta)] + [-W \times (\delta - \gamma)] = \sigma_0. \quad (73)$$

It can be seen in (73) that the average amplitude of the amplifier output under unbalanced power supply condition is equivalent to its constant input amplitude σ_0 . In short, the PWM negative feedback loop is able to reject the low-frequency power supply noise and accurately reproduce the input information at its output without much distortion added to the amplifier's output under steady state input condition.

4.3.3 Stability and Pulse-skipping for Steady-State Input

The analysis for the amplifier with constant power supply and steady-state input condition was derived based on the assumption that the amplifier is stable to small perturbations. Hence, it is worthwhile to investigate the stability of the amplifier. Considering infinitesimal perturbations to the steady-state solution, thus,

$$\begin{aligned} m_n &= M + \lambda^n \bar{M}, & p_n &= P + \lambda^n \bar{P}, \\ C_n &= (n + \gamma)T + \lambda^n \bar{C}, & D_n &= (n + \delta)T + \lambda^n \bar{D}. \end{aligned} \quad (74)$$

By examining those terms in the above notation and equations (51)-(53), it was found that the resulting eigenvalue problem for λ is extremely algebraically messy. In short, the eigenvalues satisfy a quadratic equation; the steady state operation is considered stable if and only if both of the roots for λ lie within the unit circle ($|\lambda| < 1$).

For steady-state audio input where $|\sigma_0| < \sigma_c$, the amplifier is stable as long as the output switching sequence follows (41). In the case of $\sigma_0 > \sigma_c$ with switching sequence that follows (66), instability that leads to oscillation in the output PWM signal might occur. In fact, the calculation shows that the possibility for an eigenvalue to exceed the unit circle lie at the point $e^{j\pi}$. In other words, the only possibility for the amplifier to become unstable is when an eigenvalue passes through -1. And correspondingly, the instability threshold $\sigma_0 = \sigma_i$ at which $\lambda = -1$ can be found as

$$\sigma_i = 1 - \frac{2\Delta}{-k_2 T}. \quad (75)$$

Note that this equation is valid when both the power supply rails are balanced and fixed $V = W = 1$. In short, the analysis so far reveals that the amplifier becomes unstable when the steady-state input audio signals amplitude is larger than the instability threshold defined in (75).

For time-varying input audio signal $\sigma(t)$, the amplifier is generally stable during the intervals where $|\sigma(t)| < \sigma_i$. Under such condition, the time varying input audio signal is expected to be reproduced at the amplifier's output without much distortion. On the other hand, the system becomes unstable during the intervals when $|\sigma(t)| > \sigma_i$.

In summary, the perturbations due to system instability are relatively small and decay quickly if the duration of $\sigma(t)$ exceeding σ_i is sufficiently short. Thus, the impact on the output audio signal is relatively small. On the other hand, the longer the duration for which the amplitude of $\sigma(t)$ stays beyond σ_i , the greater the perturbation is expected to grow. In the case of input signal having sufficiently long duration of $|\sigma(t)| > \sigma_i$, pulse skipping might be developed in the output audio signal. Hence, higher distortion is expected in the audio output signal.

4.4 Non-steady-state Inputs and Effects of Power Supply Noise

The analysis in the previous section shows that the amplifier's output is an exact replica of its input under steady-state condition. In this section, the amplifier behavior with time-varying audio input signal $\sigma(t)$ is considered. The objective in this section is to investigate the followings:

- i) the inherent distortion within the amplifier with no power supply noise, and
- ii) the noise in the amplifier output resulted from the power supply noise within the audible frequency range.

The analysis in this section is performed with the assumption of the smallness ratio between the input audio frequency (or the power supply noise frequency) and the PWM switching frequency. Hence, the following small parameter is defined with ω being the angular frequency for $\sigma(t)$ or for the power supply noise, and T being the input switching period.

$$\varepsilon \equiv \omega T \ll 1 \quad (76)$$

Practically, the range for ε is from 0.00005 to 0.05. It was found that the solution to (51)-(53) is a slowly varying function of n , and hence, it is useful to denote the switching instants as

$$\begin{aligned} a(\varepsilon n) &= \alpha_n = \frac{A_n - nT}{T}, & b(\varepsilon n) &= \beta_n = \frac{B_n - nT}{T}, \\ c(\varepsilon n) &= \gamma_n = \frac{C_n - nT}{T}, & d(\varepsilon n) &= \delta_n = \frac{C_n - nT}{T}, \end{aligned} \quad (77)$$

Also, the slowly varying functions M and P that sample the two integrator outputs are denoted as:

$$M(\varepsilon n) = m(A_n) \quad P(\varepsilon n) = p(A_n) \quad (78)$$

In order to generalize the solution to accommodate for the power supply noise, the following expressions for the power supply rail voltage are defined

$$v(t) = \frac{1}{2} \bar{V} t^2 + \tilde{v}(t) \quad w(t) = \frac{1}{2} \bar{W} t^2 + \tilde{w}(t) \quad (79)$$

where $V(t) = v''(t)$ and $-W(t) = -w''(t)$ as defined earlier in (35),

$$\bar{V} = \langle V(t) \rangle, \quad \bar{W} = \langle W(t) \rangle \text{ and also,}$$

$\tilde{v}(t)$ and $\tilde{w}(t)$ represent the time average fluctuations of the respective power supply rail.

In fact, the practical frequency range for the power supply noise is relatively low as compared to that of the input PWM signal. Therefore, $\tilde{v}(t)$ and $\tilde{w}(t)$ are considered as slowly varying functions. Hence, it is useful to introduce the dimensionless time variable

$$\tau = \omega t = \mathcal{E} / T. \quad (80)$$

With the above notation, it is also useful to introduce

$$\mathcal{V}(\tau) = \frac{\mathcal{E}^2}{T^2} \tilde{v}(t), \quad \mathcal{W}(\tau) = \frac{\mathcal{E}^2}{T^2} \tilde{w}(t). \quad (81)$$

Now, the difference equations in (51)-(53) can be reformulated with the above notation and the resultant difference equation for m_n is

$$\begin{aligned} M(\mathcal{E}n + \mathcal{E}) &= M(\mathcal{E}n) + \frac{1}{2} T (1 + a(\mathcal{E}n + \mathcal{E}) - 2b(\mathcal{E}n)) \\ &\quad + \frac{1}{2} T [\bar{W} (a(\mathcal{E}n) - a(\mathcal{E}n + \mathcal{E}) - 1) + (\bar{V} + \bar{W}) (1 + c(\mathcal{E}n + \mathcal{E}) - d(\mathcal{E}n))] \\ &\quad + \frac{T}{2\mathcal{E}} [-\mathcal{W}'_{a+} + \mathcal{W}'_a + \mathcal{V}'_{c+} - \mathcal{V}'_d + \mathcal{W}'_{c+} - \mathcal{W}'_d] \end{aligned} \quad (82)$$

$$\begin{aligned} \text{where } \mathcal{W}'_a &\equiv \mathcal{W}'(\mathcal{E}n + \mathcal{E}a(\mathcal{E}n)), & \mathcal{W}'_{a+} &\equiv \mathcal{W}'(\mathcal{E}n + \mathcal{E} + \mathcal{E}a(\mathcal{E}n + \mathcal{E})) \\ \mathcal{W}'_{c+} &\equiv \mathcal{W}'(\mathcal{E}n + \mathcal{E} + \mathcal{E}c(\mathcal{E}n + \mathcal{E})) & \mathcal{W}'_d &\equiv \mathcal{W}'(\mathcal{E}n + \mathcal{E}d(\mathcal{E}n)), \\ \mathcal{V}'_{c+} &\equiv \mathcal{V}'(\mathcal{E}n + \mathcal{E} + \mathcal{E}c(\mathcal{E}n + \mathcal{E})) & \mathcal{V}'_d &\equiv \mathcal{V}'(\mathcal{E}n + \mathcal{E}d(\mathcal{E}n)). \end{aligned} \quad (83)$$

Likewise, a similar expression corresponding to the difference equation for p_n may be defined to associate $P(\varepsilon n + \varepsilon)$ to $P(\varepsilon n)$. However, the expression is rather lengthy and provides limited insight. Thus, it is not recorded here. Also, the switching conditions denoted in (52) and (53) can be re-written as

$$k_1 P_d + k_2 M_d = \frac{1}{2} \Delta, \quad k_1 P_c + k_2 M_c = -\frac{1}{2} \Delta \quad (84)$$

$$\begin{aligned} \text{where } M_c &= M(\varepsilon n + \varepsilon c(\varepsilon n)), & M_d &= M(\varepsilon n + \varepsilon d(\varepsilon n)), \\ P_c &= P(\varepsilon n + \varepsilon c(\varepsilon n)), & P_d &= P(\varepsilon n + \varepsilon d(\varepsilon n)). \end{aligned}$$

With the above notation, the reformulated difference equations can be viewed as sampled versions of continuous-time function equations. By replacing the discrete variable ' n ' with a continuous variable ' t/T ', the governing difference equations can now be extended to hold even at the intermediate times between the sampling intervals. Thus, the following functional equations can be obtained.

$$\begin{aligned} M(\tau + \varepsilon) &= M(\tau) + \frac{1}{2} T(1 + a(\tau + \varepsilon) - 2b(\tau)) \\ &\quad + \frac{1}{2} T[\bar{W}(a(\tau) - a(\tau + \varepsilon) - 1) + (\bar{V} + \bar{W})(1 + c(\tau + \varepsilon) - d(\tau))] \\ &\quad + \frac{T}{2\varepsilon} [-W'(\tau + \varepsilon + \varepsilon a(\tau + \varepsilon)) + W'(\tau + a(\tau)) + V'(\tau + \varepsilon + \varepsilon c(\tau + \varepsilon)) \\ &\quad - V'(\tau + \varepsilon d(\tau)) + W'(\tau + \varepsilon + \varepsilon c(\tau + \varepsilon)) - W'(\tau + \varepsilon d(\tau))] \end{aligned} \quad (85)$$

Correspondingly, an equation relating $P(\tau + \varepsilon)$ to $P(\tau)$ can be defined in a similar manner, however, it is again not recorded here due to its complexity. In addition, the switching conditions in (52) and (53) can now be re-written as

$$k_1 P(\tau + \varepsilon d(\tau)) + k_2 M(\tau + \varepsilon d(\tau)) = \frac{1}{2} \Delta,$$

$$k_1 P(\tau + \varepsilon c(\tau)) + k_2 M(\tau + \varepsilon d(\tau)) = -\frac{1}{2} \Delta. \quad (86)$$

Again, the information of the input switching-time function, $a(\tau)$ and $b(\tau)$, are assumed to be known. Thus, $M(\tau)$, $P(\tau)$, $c(\tau)$ and $d(\tau)$ are the four function that are required to be determined.

Obviously, it is infeasible to establish a general solution to this system. However, in the limit $\varepsilon \rightarrow 0$, a perturbation solution may be developed by first expressing each of the four unknown function mentioned in the previous paragraph as a power series in ε , for instance,

$$\begin{aligned} M(\tau) &= \sum_{n=0}^{\infty} \varepsilon^n M_n(\tau) & P(\tau) &= \sum_{n=0}^{\infty} \varepsilon^n P_n(\tau) \\ c(\tau) &= \sum_{n=0}^{\infty} \varepsilon^n c_n(\tau) & d(\tau) &= \sum_{n=0}^{\infty} \varepsilon^n d_n(\tau) \end{aligned} \quad (87)$$

After applying Taylor series expansion about the dimensionless time variable τ , the resulting system of equations are analyzed successively in terms of the orders in ε . In fact, the leading order reveals the same conclusion that was drawn in the previous section for the analysis of the amplifier under the steady-state operation with constant power supply. In general, the solutions for higher orders in ε require extremely strong computational power to solve for the algebraically messy equations.

Amongst the four unknown functions in the above equations, the switching-time functions ' c ' and ' d ' are the main components contributing to the harmonic behavior of the amplifier output. Hence, it is worth investigating the problem by determining the audio components in the amplifier output based on the output switching-time functions.

4.4.1 Recovering the Audio Input

In general, the output PWM signal $g(t)$ contains both the high-frequency switching signal as well as the low-frequency audio signal (or the low-frequency power supply noise, if any). Although the analysis here focuses on exploring the low-frequency audio contents of $g(t)$ in terms of its harmonic distortion, the analysis below could also be extended to high-frequency spectrum of $g(t)$. This can be very useful in determining the output filter requirement.

The output of the amplifier can be described as

$$g(t) = V(t)g_+(t) - W(t)g_-(t), \quad (88)$$

where

$$g_+(t) = \sum_{n=-\infty}^{\infty} \psi(t; D_n, C_{n+1}), \quad g_-(t) = \sum_{n=-\infty}^{\infty} \psi(t; C_n, D_n), \quad (89)$$

and where ψ is an impulse function denoted by

$$\psi(t; t_1, t_2) = \begin{cases} 1 & \text{for } t_1 < t < t_2, \\ 0 & \text{for otherwise.} \end{cases} \quad (90)$$

Note that

$$g_+(t) + g_-(t) = 1. \quad (91)$$

By applying Fourier Transform on $g_+(t)$, the following expression relating to the harmonic behavior of $g_+(t)$ can be obtained

$$\hat{g}_+(\omega) = \int_{-\infty}^{\infty} e^{-j\omega t} \sum_n \psi(t; D_n, C_{n+1}) dt = \sum_n (-j\omega)^{-1} e^{-j\omega nT} (e^{-j\omega Tc(\varepsilon n)} - e^{-j\omega Td(\varepsilon n)}), \quad (92)$$

where the second equality is limited to the case $\omega \neq 0$.

Applying Poisson re-summation, i.e.

$$\sum_{n=-\infty}^{\infty} h(n) = \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} e^{2\pi j n \phi} h(\phi) d\phi \quad (93)$$

to (92), the following expression is obtained.

$$\hat{g}_+(\omega) = \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} e^{2\pi j n \phi} (-j\omega)^{-1} e^{-j\omega \mathcal{T}} \left(e^{-j\omega T c(\varepsilon \phi)} - e^{-j\omega T d(\varepsilon \phi)} \right) d\phi \quad (94)$$

The summation variable 'n' in (94) represents the frequency spectrum for ω around the n th multiple of the switching frequency. Therefore, it must be set to 0 to explore the low frequency contents of $g_+(t)$. Using Taylor series expansion, the exponential terms involving the output switching-time functions c and d can be further expanded and the following can be obtained.

$$\begin{aligned} \hat{g}_+^a(\omega) &= \frac{T}{\varepsilon} \int_{-\infty}^{\infty} e^{-j\omega \mathcal{T} / \varepsilon} \sum_{m=1}^{\infty} \frac{(-j\omega T)^{m-1}}{m!} (c^m(\tau) - d^m(\tau)) d\tau \\ &= \int_{-\infty}^{\infty} e^{-j\omega \mathcal{T}} \sum_{m=1}^{\infty} \frac{(-T)^{m-1}}{m!} \frac{d^{m-1}}{dt^{m-1}} (c^m(\mathcal{T}/T) - d^m(\mathcal{T}/T)) dt \end{aligned} \quad (95)$$

Note that a superscript a is introduced in the above equation to denote the low-frequency component in $g_+(t)$ (i.e. audio signal). Thus, the time-domain expression for $\hat{g}_+^a(\omega)$ (i.e. $g_+^a(t)$) can be found by performing Inverse Fourier Transform on (95). Thus,

$$g_+^a(t) = 1 + \sum_{m=1}^{\infty} \frac{(-T)^{m-1}}{m!} \frac{d^{m-1}}{dt^{m-1}} (c^m(\mathcal{T}/T) - d^m(\mathcal{T}/T)). \quad (96)$$

Hence, together with (88) and (91), the output audio component is given as

$$\begin{aligned} g^a(t) &= V(t)g_+^a(t) - W(t)[1 - g_+^a(t)] \\ &= V(t) + [V(t) + W(t)] \sum_{m=1}^{\infty} \frac{(-T)^{m-1}}{m!} \frac{d^{m-1}}{dt^{m-1}} (c^m(\mathcal{T}/T) - d^m(\mathcal{T}/T)). \end{aligned} \quad (97)$$

The above equation relates the output switching-time functions to the audio output of the amplifier. Equation (97) indicates that $V(t)$ and $W(t)$ affects only the audio components of $g(t)$. In addition, $V(t)$ and $W(t)$ do not contain high-frequency component that could potentially inter-modulate with the high-frequency terms of $g(t)$ to distort the output audio band spectrum.

Using perturbation expansion, $g^a(t)$ can be expanded as follow:

$$g^a(t) = g_0^a(t) + \varepsilon g_1^a(t) + \varepsilon^2 g_2^a(t) + \dots \quad (98)$$

The above expansion was computed algebraically with a computer package and the results show that $g_0^a(t)$ in the above equation is actually the input audio signal $\sigma(t)$. In addition, $g_2^a(t)$ represents the first distortion terms as $g_1^a(t) = 0$.

However, a full generality solution to this problem is way too complicated, such that even the computer algebra package is unable to derive the expansions. The computer algebra package runs out of memory before reaching the first non-trivial result for $g_2^a(t)$ for the following generality calculations:

- a) arbitrary mean power supply voltages V and W ,
- b) arbitrary power supply noise, and
- c) arbitrary input audio signal.

Due to the computational power constraints, the mean power supply voltages is then fixed and normalized to 1 for the analysis in the remainder of this chapter, such that

$$V = W = 1. \quad (99)$$

4.4.2 Sinusoidal Audio Input

For the analysis with sinusoidal audio input signal $\sigma(t)$ with clean power supply rails, $\sigma(t) = \sigma_0 \sin \omega t$ and $\tilde{v}(t) = \tilde{w}(t) = 0$.

The various mathematical expressions are extremely complicated, and with little contribution to record them here. However, it is realize that the expression for $g^a(t)$ can be expanded using Fourier series expansion, and thus,

$$g^a(t) = \sum_{k=0}^{\infty} G_{2k+1} \sin(2k+1)\omega t \quad (100)$$

with

$$G_1 = \sigma_0 + O(\varepsilon^2) \quad (101)$$

and

$$G_{2k+1} = O(\varepsilon^2) \quad \text{for } k \geq 1. \quad (102)$$

It can be observed from (100) that the Fourier sine series of $g^a(t)$ contains the original audio signal with distortion of order ε^2 (i.e. the distortion is $O((\omega T)^2)$ in dimensional terms), as well as its odd harmonics. In fact, the $O(\varepsilon)$ correction is precisely zero.

Figure 61 and Figure 62 depict the results obtained using the parameter values in Table 6. These figures show excellent agreement between the simulation results obtained by Matlab Simulink and the theory.

Figure 61 shows that coefficients G_{2k+1} in (100) each vary approximately proportional to σ_0^{2k+1} as long as the input amplitude is less than $\sigma_c \approx 0.48$. For $\sigma_0 \approx \sigma_c$, significant harmonic distortion would be expected at the amplifier's output due to the increase in the magnitude of the fifth harmonic in both analytical and numerical results. For the amplitude of the input sinusoidal signal greater than σ_c (i.e. $\sigma_0 > \sigma_c$), the switching order remains as (41) as

long as the instantaneous input amplitude is less than σ_c . When the instantaneous amplitude grows nearer to the positive or the negative peaks of the input sinusoidal signal, the switching order becomes (66) and (70) respectively. The output of the amplifier is significantly distorted once the switching order becomes that described either in (66) or (70). The Matlab Simulink simulation shows that pulse skipping occurs at the $g(t)$ when the input amplitude is greater than approximately 0.6. This is consistent with the earlier prediction in Section 4.3.3 for the linear instability threshold with the parameters in Table 6 (i.e. $\sigma_i = 0.55$). Consequently, pulse skipping is expected for any input amplitudes that are sufficiently greater than this instability threshold level. Since pulse skipping was not taken into consideration in the derivation of the analytical model, the disagreement between theory and numeric simulation becomes more noticeable for input amplitude beyond 0.6 (i.e. $\sigma_0 \geq 0.6$). However, it is worth mentioning that the results obtained from both the theory and the numeric simulations are closely matched for the fundamental frequency even for the largest input amplitude.

Figure 62 shows that the amplitude of the harmonics are all proportional to ω^2 , where ω is the audio frequency; as reflected in (101) and (102), and the relationship $\varepsilon = \omega T$. In fact, the results obtained by Matlab Simulink Simulation show excellent agreement with this theoretical ε^2 scaling. However, deviations arises as frequency increases (i.e., for higher ε). Fortunately, the third and fifth harmonics for such frequency range are inaudible by human ears.

In general, the performance of most audio amplifiers is often measured in terms of the $THD\%$ of its amplified output signal. This parameter may be defined as

$$THD\% = \left(\frac{\omega \int_0^{2\pi/\omega} (g^a(t))^2 dt}{\pi G_1^2} - 1 \right)^{1/2} \times 100\% \quad (103)$$

Based on the observation, the THD% results obtained from the theoretical prediction are well agreed with that obtained from Matlab Simulink Simulation. For a sinusoidal input signal at 5 kHz, the *THD*% obtained from both theory and simulation are 0.003%, 0.006%, 0.013% and 0.022% for $\sigma_0 = 0.1, 0.2, 0.3$ and 0.4 respectively. For fixed amplitude sinusoidal signal ($\sigma_0 = 0.4$), the *THD*% results obtained from the theoretical prediction derived earlier are, $3.54 \times 10^{-5}\%$, $1.4 \times 10^{-4}\%$, $5.57 \times 10^{-4}\%$ and $8.72 \times 10^{-4}\%$ at frequencies 200, 400, 800 and 1000 Hz respectively (with only slight variances in the least significant digit for the results obtained from simulation).

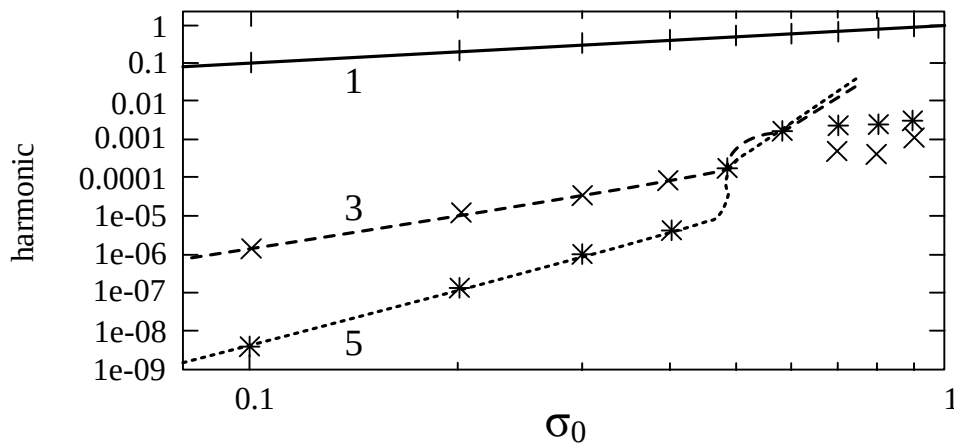


Figure 61. Amplitude of 1st, 3rd and 5th harmonic in the audio output of the amplifier, for a 5kHz sinusoidal audio input, with various values of the amplitude σ_0 . Lines represent the analytical results; symbols mark results of Matlab Simulink simulation

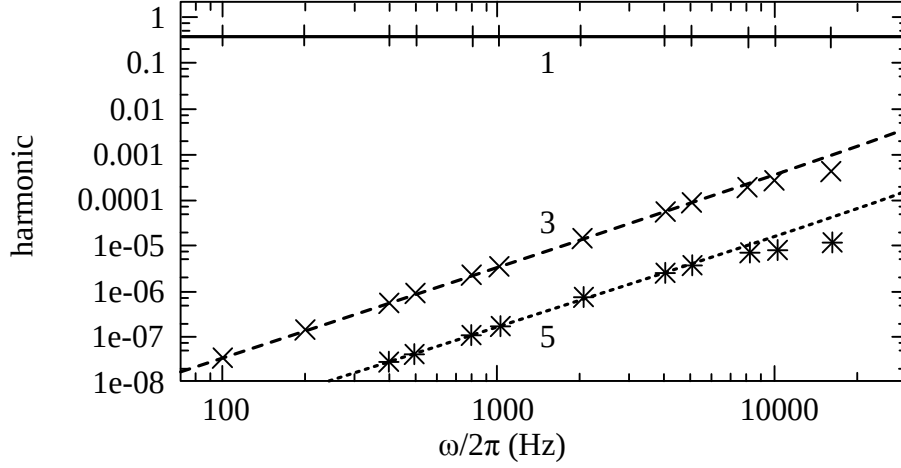


Figure 62. Amplitude of 1st, 3rd, 5th harmonic in the audio output of the amplifier, for an audio input $0.4\sin\omega t$, plotted against frequency. Lines represent the analytical results; symbols mark results of Matlab Simulink simulation

4.4.3 Power Supply Noise Effect on Constant Input

In this section, the impact of the noise from the supply rails on a constant audio signal is investigated. Due to the constraints of the practical computational power, the following analysis focuses on the case where the noise appears only on the positive power rail. Hence,

$$\tilde{w}(t) = 0 \quad (104)$$

For simplicity, a sinusoidal signal is superimposed on the positive power supply rail to emulate the power supply noise to the amplifier. Thus, the sinusoidal power supply noise with amplitude of V and frequency of ω can be expressed as

$$\tilde{v}(t) = V \sin \omega t. \quad (105)$$

Figure 63 depicts the theoretical prediction based on the analysis derived earlier and the simulation results for the harmonics behavior of the amplifier output signal with positive supply noise at 5 kHz and 200 Hz. The supply rail with a test signal described in (105) is used to power the Class-D amplifier output power stage. The amplitude of the sinusoidal test signal is then varied from 0.2 to 0.8 V. As depicted in Figure 63, the PWM feedback loop effectively suppressed the power supply fluctuations at the amplifier's output. For instance, the amplitude of the fundamental component of the amplifier output signal is 3×10^{-4} (for noise at 5 kHz) and 5×10^{-7} (for noise at 200 Hz) when $V = 0.8$. It is worth mentioning that Figure 63 shows excellent agreement between the theoretical results (represented by lines) and the Matlab Simulink simulation results (represented by crosses) of the amplifier.

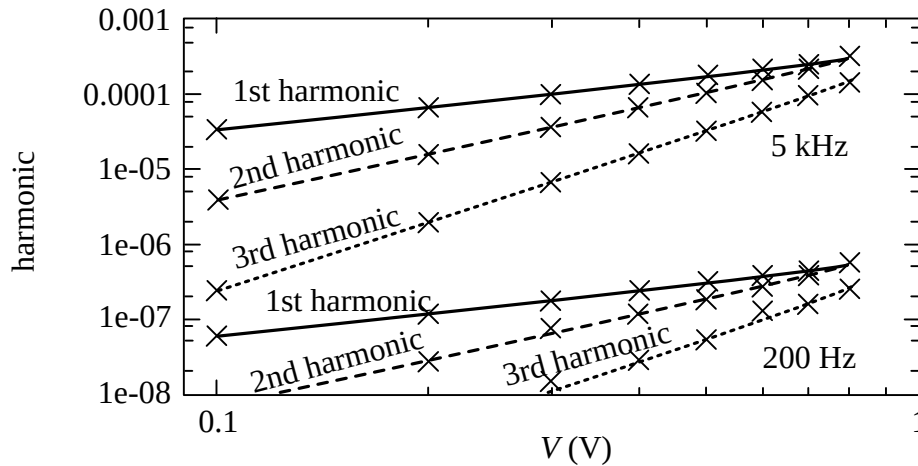


Figure 63. Amplifier output ripple amplitude against the peak power-supply ripple with amplitude V , with ripple frequency of 200 Hz and 5 kHz. The curves show the theoretical prediction; crosses give corresponding results from Matlab Simulink simulations.

4.5 Conclusions

An in-depth analysis of a mathematical model based on the proposed PWM feedback loop is presented. This proposed PWM feedback loop aims to effectively suppress the low-frequency power supply noise without introducing distortion in its audio output. This analysis verifies the high PSRR performance of PWM feedback loops, and also quantifies its inherent distortion. The fact that both the input and output signals of this feedback loop are PWM signal, hence, the analysis of its mathematical model is extremely complicated, and requires significant computation efforts. The complexity of the algebraically intensive equations, and also, the constraints of the present computing power limit the possibility to provide a full generality to the solution at this stage. Even for the case of sinusoidal input signal with no power supply noise, the corresponding expression for the audio output of the proposed PWM feedback loop cannot be simply expressed in terms of its input signal and a few low-order harmonics representing the leading-order distortion. In fact, the full expression for the audio output is a complicated time varying function, which may be expanded as a Fourier sine series of odd harmonics. With such Fourier decomposition, it was found that the original audio signal is reproduced at the amplifier's output, but with some distortion with the order of ε^2 .

Chapter 5 Conclusions and Future Works

5.1 Conclusion

The conventional linear amplifier such as Class-A and Class-AB power amplifier can no longer satisfied the requirement of portable electronics audio devices in the consumer industry, such as MP3, cellular phones and PDA, due to their low power efficiency. Therefore, the demands for the high efficiency low power amplifier solutions are dramatically increasing. As the musical information are mostly stored in digital media (in PCM format), Class-D amplifier is an ideal solution for digital amplification for battery operated portable devices. This is mainly because of its high power efficiency and its capability of handling the whole amplification process in the digital domain without the need of converting the digitally stored information into analog form.

Many researchers have focused on the generation of high precision PWM signal from a PCM signal with the most efficient digital techniques. However, the findings on ways to minimize the noise and harmonics distortion in the Class-D power stage for a digital open loop system were still limited. This report presents a very detailed literature review on the current-art techniques of the error correction circuits that are proposed for the Class-D switching power stage. Also, a feedback correction circuit is proposed in this report to improve the linearity (in terms of THD) and the noise suppression capability (in terms of PSRR) for a digital Class-D system. Thus, the design complexity of PCM-to-PWM converter can be more relaxed.

The proposed PWM negative feedback loop for Class-D amplifier application mitigates the power supply ripple and harmonic distortion by re-

modulating the duty ratio of the output PWM signal. The PWM negative feedback circuit first integrates the difference between a high precision reference PWM signal as input and the output PWM signal. The Schmitt trigger comparator acts as a single bit quantizer to quantize the analog integrated difference signal into a corrected PWM signal with only two discrete amplitude levels. The circuit is implemented and fabricated using GF's 0.18 μm CMOS technology. The second-order PWM feedback loop achieve a measured PSRR of -80 dB at 217 Hz and the measured THD reading is well below 0.1% from 1 kHz to 20 kHz. This shows that the proposed Class-D output stage with second-order negative feedback can effectively reduce the impact of supply noise and non-linearities on the output audio signal.

5.2 Future Works

The analysis and simulation that are done in this report are based on single-ended half-bridge Class-D amplifier output stage solution. The investigation on the constraints in the application of this solution to the full H-bridge output stage topology is recommended for the future work. In addition, the solution to the mathematical analysis for the proposed second order solution is rather incomplete due to the limited computational resources. Hence, another recommendation for further works is to provide full generality solution to the mathematical model for the second-order PWM feedback loop.

Author's Publications

Journal Publications

- M. T. Tan, P. K. Chan, C. K. Lam, and C. W. Ng, "AC-Boosting Frequency Compensation with Double Pole-Zero Cancellation for Multistage Amplifiers," *Circuit, Syst., and Signal Processing*, vol. 29, No.5, pp. 941-951, 2010.
- S. M. Cox, C. K. Lam, and M. T. Tan, "A second-order PWM-in/PWM-out class-D audio amplifier," *IMA J. Appl. Math.*, June, 2011.
- C. K. Lam, M. T. Tan, S. M. Cox, and K. S. Yeo, "Class-D Amplifier Power Stage With PWM Feedback Loop," *IEEE Transactions on Power Electronics*, vol. 28, pp. 3870-3881, 2013.

Conference Publications

- C. K. Lam and M. T. Tan, "A Class D amplifier output stage with low THD and high PSRR," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 1945-1948.
- A. T. Do, C. K. Lam, Y. S. Tan, K.-S. Yeo, J. H. Cheong, X. Zou, L. Yao, K.-W. Cheng, and M. Je, "A 160 nW 25 kS/s 9-bit SAR ADC for neural signal recording applications," in *IEEE 10th International New Circuits and Systems Conference (NEWCAS)*, 2012, pp. 525-528.
- A. T. Do, C. K. Lam, Y. S. Tan, K. S. Yeo, J. H. Cheong, L. Yao, M. T. Tan, and M. Je, "A 9.87 nW 1 kS/s 8.7 ENOB SAR ADC for implantable epileptic seizure detection microsystems," in *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2012, pp. 1-4.

References

- [1] Wolfson Microelectronics Application Note, *Class D amplifiers empower mobile multimedia*.
- [2] K. Nielsen, "Linearity and efficiency performance of switching audio power amplifier output stage," presented at the 105th AES Convention, San Francisco, CA, Sep. 1998.
- [3] W. M. Leach, *Introduction to Electroacoustics and Audio Amplifier Design*: Kendall/Hunt Publishing Company, 2001.
- [4] B. Putzeys, "Digital audio's final frontier," *IEEE Spectrum*, vol. 40, pp. 34-41, 2003.
- [5] C. Pascual, Z. Song, P. T. Krein, D. V. Sarwate, P. Midya, and W. J. Roeckner, "High-fidelity PWM inverter for digital audio amplification: Spectral analysis, real-time DSP implementation, and results," *IEEE Transactions on Power Electronics*, vol. 18, pp. 473-485, 2003.
- [6] K. P. Sozanski, R. Strzelecki, and Z. Fedyczak, "Digital control circuit for class-D audio power amplifier," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference*, 2001, pp. 1245-1250 vol.2.
- [7] H. Seo Weon and K. Jongsun, "Double edge trailing PWM based full digital audio amplifier design," in *IEEE International Conference on Consumer Electronics (ICCE)*, 2012, pp. 251-252.
- [8] L. Risbo and T. Mørch, "Performance of an all-digital power amplification system," presented at the 104th AES Convention, Amsterdam, The Netherlands, May 1998.
- [9] J. M. Goldberg and M. B. Sandler, "Pseudo-natural pulse width modulation for high accuracy digital-to-analogue conversion," *Electronics Letters*, vol. 27, pp. 1491-1492, 1991.
- [10] K. M. Smith, K. M. Smedley, and M. Yunhong, "Realization of a digital PWM power amplifier using noise and ripple shaping," in *26th Annual IEEE Power Electronics Specialists Conference*, 1995, pp. 96-102 vol.1.
- [11] F. Hui, Y. Zeqi, H. Zhigang, and F. Fan, "System Level Design of a Digital Audio Class D Power Amplifier," in *International Conference on Multimedia Technology (ICMT)*, 2010, pp. 1-5.
- [12] V. Adrian, G. Bah-Hwee, and J. S. Chang, "A novel combined first and second order Lagrange interpolation sampling process for a digital class D amplifier," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, Vol.3, pp. III-233-60
- [13] M. Smedegaard, "A simple Non-Feedback Switching Power Output Stage," presented at the 101st AES Convention, Los Angeles, CA., Nov. 1996.
- [14] M. Wang, X. Jiang, J. Song, and T. Brooks, "A 120dB dynamic range 400mW class-D speaker driver with 4th-order PWM modulator," in *IEEE Custom Integrated Circuits Conference*, 2009, pp. 13-16.
- [15] R. Cellier, G. Pillonnet, A. Nagari, and N. Abouchi, "An review of fully digital audio class D amplifiers topologies," in *Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference*, 2009, pp. 1-4.

-
- [16] S. Luo and D. Li, "A Sixth-Order PWM Modulator for Digital Input Class-D Audio Amplifiers," in *Fifth International Conference on Computational and Information Sciences (ICCIS)*, 2013, pp. 1253-1256.
 - [17] M. Berkhout, "Class-D audio amplifiers in mobile applications," in *IEEE International Symposium on Circuits and Systems*, 2009, pp. 1169-1172.
 - [18] M. Berkhout and L. Dooper, "Class-D Audio Amplifiers in Mobile Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, pp. 992-1002, 2010.
 - [19] L. Lin, X. Wu, J. Zhao, and M. Zhao, "Design of a fully-digital class-D audio power amplifier based on open-loop configuration," in *IEEE International Conference on Electron Devices and Solid State Circuit*, 2012, pp. 1-3.
 - [20] S. Saponara, L. Fanucci, and P. Terreni, "Oversampled and Noise-Shaped Pulse-Width Modulator for High-Fidelity Digital Audio Amplifier," in *13th IEEE International Conference on Electronics, Circuits and Systems*, 2006, 2006, pp. 830-833.
 - [21] G. Tong and J. S. Chang, "Modeling and Technique to Improve PSRR and PS-IMD in Analog PWM Class-D Amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, pp. 512-516, 2008.
 - [22] M. Bloechl, M. Bataineh, and D. Harrell, "Class D Switching Power Amplifiers: Theory, Design, and Performance," in *Proceedings. IEEE SoutheastCon, 2004*, 2004, pp. 123-146.
 - [23] M. Berkhout, "Integrated Class-D Amplifier," in *112th Convention of Audio Engineering Society*, Germany, May 2002.
 - [24] G. Tong, J. S. Chang, and S. Wei, "Modeling and analysis of PSRR in analog PWM class D amplifiers," in *IEEE International Symposium on Circuits and Systems*, 2006, pp. 1386-1389.
 - [25] S. Wei and J. S. Chang, "Power Supply Noise in Analog Audio Class D Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, pp. 84-96, 2009.
 - [26] J. S. Chang, B. H. Gwee, Y. S. Lon, and M. T. Tan, "A novel low-power low-voltage Class D amplifier with feedback for improving THD, power efficiency and gain linearity," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. 1, pp. 635-638.
 - [27] H. C. Foong and M. T. Tan, "An Analysis of THD in Class D Amplifiers," in *IEEE Asia Pacific Conf. on Circuits and Systems*, 2006, pp. 724-727.
 - [28] K. Nielsen, "MECC-A novel control method for high end switching audio power amplification," presented at the 105th AES Convention, San Francisco, CA, Sep. 1998.
 - [29] L. Risbo and C. Neesgaard, "PWM Amplifier Control Loops with Minimum Aliasing Distortion," in *AES 120th Convention* Paris, France, May, 2006, p. 6693.
 - [30] Y. Xu, F. Zhao, Y. Wu, R. Min, Z. Sun, and L. Tang, "Single chip design of closed-loop class D audio power amplifier," in *International Conference on Wireless Communications and Signal Processing (WCSP)*, 2010, pp. 1-5.
 - [31] B. Krabbenborg and M. Berkhout, "Closed-Loop Class-D Amplifier With Nonlinear Loop Integrators," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1389-1398, 2010.
 - [32] M. Berkhout, "An integrated 200-W class-D audio amplifier," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1198-1206, 2003.
 - [33] E. C. Dijkmans and J. A. T. M. van den Homberg, "PWM amplifier with feedback loop integrator," 6300825 B1 US Patent.
-

-
- [34] Y. Choi, W. Tak, Y. Yoon, J. Roh, S. Kwon, and J. Koh, "A 0.018% THD+N, 88-dB PSRR PWM Class-D Amplifier for Direct Battery Hookup," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 454-463, 2012.
 - [35] M. Berkhout and B. Krabbenborg, "Pulse Width Modulation Circuit and Class D Amplifier Comprising the PWM Circuit," 8067980, US Patent, 2011.
 - [36] P. Adduci, E. Botti, E. Dallago, and G. Venchi, "PWM Power Audio Amplifier With Voltage/Current Mixed Feedback for High-Efficiency Speakers," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 1141-1149, 2007.
 - [37] G. Tong, J. S. Chang, and S. Wei, "PSRR of bridge-tied load PWM Class D Amps," in *IEEE International Symposium on Circuits and Systems, 2008*, 2008, pp. 284-287.
 - [38] D. Self, *Audio Power Amplifier Design Handbook*: Taylor & Francis, 2013.
 - [39] A. Singmin, *Practical Audio Amplifier Circuit Projects*, 2000.
 - [40] R. G. Gupta, *Audio and Video Systems: Principles & Troubleshooting*, 1995.
 - [41] D. M. Thompson, *Understanding Audio: Getting the Most Out of Your Project Or Professional Recording Studio*: Berklee Press, 2005.
 - [42] M. T. Tan, J. S. Chang, Z. H. Cheng, and Y. C. Tong, "Analysis and two proposed design methodologies for optimizing power efficiency of a class D amplifier output stage," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, pp. 281-284 vol.1.
 - [43] L. D. Forest, "Device for amplifying feeble electrical currents," 841387 A, US Patent, 1907.
 - [44] B. Duncan, *High Performance Audio Power Amplifiers*, 1996.
 - [45] J. L. Hood, *Valve and Transistor Audio Amplifiers*, 1997.
 - [46] J. C. Whitaker, *The Electronics Handbook*, 2nd ed., 2012.
 - [47] V. K. Mehta and Rohit Mehta, *Principles of Electronics*, 2005.
 - [48] A. P. Godse and U. A. Bakshi, *Electronic Devices And Circuits*: Technical Publications, 2009.
 - [49] R. F. Graf, *Modern Dictionary of Electronics*, 1999.
 - [50] U.A.Bakshi and A.P.Godse, *Electronic Devices And Circuits - II*, 2009.
 - [51] G. Ballou, *Handbook for Sound Engineers*, 4th ed., 2008.
 - [52] U.A.Bakshi and A.P.Godse, *Electronic Circuits*, 3rd ed., 2008.
 - [53] D. Self, B. Duncan, I. Sinclair, R. Brice, J. L. Hood, A. Singmin, D. Davis, E. Patronis, and J. Watkinson, *Audio Engineering: Know It All*, 2009.
 - [54] M. Albulet, *RF Power Amplifiers*: Institution of Engineering and Technology, 2001.
 - [55] A. Grebennikov, N. O. Sokal, and M. J. Franco, *Switchmode RF Power Amplifiers*: Elsevier Science, 2011.
 - [56] J. S. Chang, M. T. Tan, Z. Cheng, and Y. C. Tong, "Analysis and design of power efficient class D amplifier output stages," *IEEE Trans. Circuits Syst. I: Fundam. Theory and Appl.*, vol. 47, pp. 897-902, 2000.
 - [57] Sergio Sánchez Moreno, *Class D audio amplifiers: theory and design*, Jun. 2005.
 - [58] R. Esslinger, G. Gruhler, and R. W. Stewart, "Digital audio power amplifier using sigma delta modulation linearity problems in the class d power stage," presented at the 110th AES Convention, Amsterdam, Netherlands, May 2001.
 - [59] H. S. Black, *Modulation Theory*, 1953.
 - [60] S. M. Cox and B. H. Candy, "Class-D audio amplifiers with negative feedback," *SIAM J. Appl. Math.* 66, pp. 468-488, 2005.
 - [61] R. E. Hiorns, J. M. Goldberg, and M. B. Sandler, "Developments in realizing an all Digital Power Amplifier," presented at the 90th AES Convention, Paris, Feb. 1991.
 - [62] W. R. Bennett, *Spectral of Quantised Signals*, April 1941.
-

-
- [63] R. E. Hiorns and M. B. Sandler, "Power digital to analogue conversion using pulse width modulation and digital signal processing," *IEE Proc. G Circuits, Devices and Syst.*, vol. 140, pp. 329-338, 1993.
- [64] M. B. Sandler, "Digital-to-analogue conversion using pulse width modulation," *Electronics & Communication Engineering Journal*, vol. 5, pp. 339-348, 1993.
- [65] N. Anderskov, K. Nielsen, and M. A. E. Andersen, "High-Fidelity Pulse-Width Modulation Amplifiers based on a Novel Double Loop Feedback Techniques," presented at the 100th AES Convention, Copenhagen, May 1996.
- [66] A. J. Magrath, I. G. Clark, and M. B. Sandler, "Design and implementation of a FPGA sigma-delta power DAC," in *IEEE Workshop on Signal Processing Systems - Design and Implementation*, 1997, pp. 511-521.
- [67] J. L. Melanson, "Real time correction of a digital pwm amplifier," 2005.
- [68] B. P. Brandt and B. A. Wooley, "A 50-MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion," *IEEE Journal of Solid-State Circuits*, vol. 26, pp. 1746-1756, 1991.
- [69] D. B. Ribner, "A comparison of modulator networks for high-order oversampled $\Sigma\Delta$ analog-to-digital converters," *IEEE Transactions on Circuits and Systems*, vol. 38, pp. 145-159, 1991.
- [70] M. Streitenberger, H. Bresch, and L. Mathis, "Theory and implementation of a new type of digital power amplifier for audio applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2000, pp. 511-514 vol.1.
- [71] K. Nielsen, "PEDEC - A novel pulse referenced control method for high quality digital PWM switching power amplification," *29th Annual IEEE Power Electronics Specialists Conference*, vol. 1, pp. 200-207, May 1998.
- [72] P. Jong-Hu, C. G. Kim, J. Jae-Hoon, and B. H. Cho, "A novel controller for switching audio power amplifier with digital input," in *IEEE 33rd Annu. Power Electronics Specialists Conf.*, 2002, pp. 39-44 vol.1.
- [73] S. Logan and M. O. J. Hawksford, "Linearization of class D output stages for high-performance audio power amplifiers," in *Second Int. Conf. on Advanced A-D and D-A Conversion Techniques and their Appl.*, 1994, pp. 136-141.
- [74] K. Nielsen, "PEDEC-A novel pulse referenced control method for high quality digital PWM switching power amplification," in *Proc. 29th Annu. IEEE Power Electron. Spec. Conf.*, 1998, vol. 1, pp. 200-207.
- [75] K. Nielsen, "Digital Pulse Modulation Amplifier (PMA) Systems Based on PEDEC Control," presented at the 106th AES Convention, Munich, Germany, May 1999.
- [76] K. Nielsen, "Pulse Edge Delay Error Correction - A Novel Power Stage Error Correction Principle For Power Digita-Analog Conversion," presented at the 103rd AES Convention, New York, USA, Sep. 1997.
- [77] K. Philips, J. van den Homberg, and C. Dijkmans, "PowerDAC: a single-chip audio DAC with a 70%-efficient power stage in 0.5 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1999, pp. 154-155.
- [78] K. Taura, Tsuji, Masayuki, Ishida, Masayuki, and Nakada Tsuyoshi, "Development of digital amplifier for car use," presented at the 115th AES Convention, New York, USA, Oct. 2003.
- [79] F. Nyboe, C. Kaya, L. Risbo, and P. Andreani, "A 240W Monolithic Class-D Audio Amplifier Output Stage," in *IEEE Int. Solid-State Circuits Conf.*, 2006, pp. 1346-1355.
- [80] F. Nyboe, L. Risbo, and P. Andreani, "Efficient performance simulation of class D amplifier output stages," in *Proc. 23rd NORCHIP Conf.*, 2005, pp. 32-35.
-

-
- [81] M. T. Tan, J. S. Chang, H. C. Chua, and B. H. Gwee, "An investigation into the parameters affecting total harmonic distortion in low-voltage low-power Class-D amplifiers," *IEEE Trans. Circuits Syst. I: Fundam. Theory and Appl.*, vol. 50, pp. 1304-1315, 2003.
- [82] Maxim Integrated. (Sep 20, 2010). *High-Efficiency Class D Audio Amplifiers Extend Battery Life in Portable Applications* [Online]. Available: <http://www.maximintegrated.com/app-notes/index.mvp/id/1760>
- [83] J. Tol, R. Rutten, D. Reefman, A. Biallais, L. Dooper, J. V. D. Boom, and R. D. Saint-Moulin, "A Digital Class-D Amplifier with Power Supply Correction," presented at the 121st AES Convention, San Francisco, CA, Oct. 2006.
- [84] L. Zhang, J. Melanson, J. Gaboriau, M. Hagge, and R. Boudreaux, "Real-time Power Supply Compensation for Noise-Shaped Class D Amplifier," presented at the 117th AES Convention, San Francisco, CA, Oct. 2004.
- [85] C. K. Lam, M. T. Tan, S. M. Cox, and K. S. Yeo, "Class-D Amplifier Power Stage With PWM Feedback Loop," *IEEE Transactions on Power Electronics*, vol. 28, pp. 3870-3881, 2013.
- [86] P. Midya, B. Roeckner, and S. Bergstedt, "Digital correction of PWM switching amplifiers," *IEEE Power Electronics Letters*, vol. 2, pp. 68-72, 2004.
- [87] L. Risbo, "Discrete-time modeling of continuous-time pulse-width modulator loops," presented at the 27th Int. AES Conf., Hillerød, Denmark, Sep. 2005.
- [88] R. Cellier, G. Pillonnet, N. Abouchi, R. M'Rad, and A. Nagari, "Analysis and design of an analog control loop for digital input class D amplifiers," in *IEEE Int. Conf. Electron., Circuits Syst.*, 2011, pp. 105-108.
- [89] M. T. Tan, P. K. Chan, C. K. Lam, and C. W. Ng, "AC-Boosting Frequency Compensation with Double Pole-Zero Cancellation for Multistage Amplifiers," *Circuit, Syst., and Signal Processing*, vol. 29, No.5, pp. 941-951, 2010.
- [90] S. M. Cox, C. K. Lam, and M. T. Tan, "A second-order PWM-in/PWM-out class-D audio amplifier," *IMA J. Appl. Math.*, June, 2011.

Appendix A

At $t=A_n$ and B_n the audio signal $\sigma(t)$ is equal to the triangular carrier signal $\theta(t)$.

$$\sigma(A_n) = \left(1 - \frac{4A_n}{T}\right)$$

$$\sigma(A_n)T = T - 4A_n$$

$$A_n = \frac{1}{4}T(1 - \sigma(A_n)) + nT$$

$$\sigma(B_n) = \left(-3 + \frac{4B_n}{T}\right)$$

$$\sigma(B_n)T = -3T + 4B_n$$

$$B_n = \frac{1}{4}T(3 + \sigma(B_n)) + nT$$

Appendix B

Expressing m_{n+1} in terms of m_n ,

Figure 59 shows that $m(A_{n+1}) = m(C_{n+1})$.

Together with (48), (46), (44) and normalized supply of $V(t) = 1$ and $W(t) = -1$,

$$m(A_{n+1}) = m(B_n) + (C_{n+1} - B_n)$$

$$m(A_{n+1}) = m(A_n) - (D_n - A_n) + (C_{n+1} - B_n)$$

Expressing p_{n+1} in terms of p_n for (49) with normalized supply of $V(t) = 1$ and $W(t) = -1$,

$$p(A_{n+1}) = p(C_{n+1}) + m(C_{n+1})(A_{n+1} - C_{n+1})$$

Substituting eqn. (46) & (47) into the above equation,

$$\begin{aligned} p(A_{n+1}) &= p(B_n) + m(B_n)(C_{n+1} - B_n) + \frac{1}{2}(C_{n+1} - B_n)^2 \\ &\quad + [m(B_n) + (C_{n+1} - B_n)](A_{n+1} - C_{n+1}) \end{aligned}$$

$$\begin{aligned} p(A_{n+1}) &= p(B_n) + m(B_n)(C_{n+1} - B_n + A_{n+1} - C_{n+1}) + \frac{1}{2}(C_{n+1} - B_n)^2 \\ &\quad + (C_{n+1} - B_n)(A_{n+1} - C_{n+1}) \end{aligned}$$

$$\begin{aligned} p(A_{n+1}) &= p(B_n) + m(B_n)(A_{n+1} - B_n) \\ &\quad + \frac{1}{2}(C_{n+1} - B_n)(C_{n+1} - B_n + 2A_{n+1} - 2C_{n+1}) \end{aligned}$$

$$p(A_{n+1}) = p(B_n) + m(B_n)(A_{n+1} - B_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

Substituting eqn. (44) & (45) into the above equation,

$$\begin{aligned} p(A_{n+1}) &= p(D_n) + m(D_n)(B_n - D_n) + m(D_n)(A_{n+1} - B_n) \\ &\quad + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1}) \end{aligned}$$

$$p(A_{n+1}) = p(D_n) + m(D_n)(B_n - D_n + A_{n+1} - B_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

$$p(A_{n+1}) = p(D_n) + m(D_n)(A_{n+1} - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

Substituting eqn. (42) & (43) into the above equation,

$$p(A_{n+1}) = p(A_n) + m(A_n)(D_n - A_n) - \frac{1}{2}(D_n - A_n)^2 + [m(A_n) - (D_n - A_n)](A_{n+1} - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

$$p(A_{n+1}) = p(A_n) + m(A_n)(D_n - A_n + A_{n+1} - D_n) - \frac{1}{2}(D_n - A_n)^2 - (D_n - A_n)(A_{n+1} - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

$$p(A_{n+1}) = p(A_n) + m(A_n)(A_{n+1} - A_n) - \frac{1}{2}(D_n - A_n)(D_n - A_n + 2A_{n+1} - 2D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

$$p(A_{n+1}) = p(A_n) + m(A_n)(A_{n+1} - A_n) - \frac{1}{2}(D_n - A_n)(2A_{n+1} - A_n - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

Since $A_{n+1} - A_n = T$,

$$p(A_{n+1}) = p(A_n) + m(A_n)T - \frac{1}{2}(D_n - A_n)(A_{n+1} + T - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

Appendix C

$$m(A_{n+1}) = m(A_n) - (D_n - A_n) + (C_{n+1} - B_n)$$

Solving $m(A_{n+1}) = m(A_n)$ for balanced power and steady state input,

$$0 = -(D_n - A_n) + (C_{n+1} - B_n)$$

$$0 = -(\delta_n - \alpha_n) + (1 + \gamma_n - \beta_n)$$

$$\delta_n = 1 + \alpha_n + \gamma_n - \beta_n$$

$$\delta_n = 1 + \frac{1}{4}(1 - \sigma_o) + \gamma_n - \frac{1}{4}(3 + \sigma_o)$$

$$\delta_n = 1 + \frac{1}{4}(1 - \sigma_o - 3 - \sigma_o) + \gamma_n$$

$$\delta_n = \frac{1}{2}(1 - \sigma_o) + \gamma_n$$

For steady-state input noise-free conditions,

$$\begin{aligned} p(A_{n+1}) = p(A_n) + m(A_n)T - \frac{1}{2}(D_n - A_n)(A_{n+1} + T - D_n) \\ + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1}) \end{aligned}$$

Solving for $p(A_{n+1}) = p(A_n)$,

$$0 = m(A_n)T - \frac{1}{2}(D_n - A_n)(A_{n+1} + T - D_n) + \frac{1}{2}(C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})$$

$$m(A_n)T = \frac{1}{2}[(D_n - A_n)(A_{n+1} + T - D_n) - (C_{n+1} - B_n)(2A_{n+1} - B_n - C_{n+1})]$$

Substituting eqn (54) into the above equation,

$$m(A_n) = \frac{T}{2}[(\delta_n - \alpha_n)(\alpha_{n+1} + 1 - \delta_n) - (\gamma_{n+1} - \beta_n)(2\alpha_{n+1} - \beta_n - \gamma_{n+1})]$$

$$m(A_n) = \frac{T}{2}[(\delta_n - \alpha_n)(\alpha_n + 2 - \delta_n) - (\gamma_n + 1 - \beta_n)(2\alpha_n + 2 - \beta_n - \gamma_n - 1)]$$

$$m(A_n) = \frac{T}{2}[(\delta_n - \alpha_n)(\alpha_n + 2 - \delta_n) - (\gamma_n + 1 - \beta_n)(3\alpha_n - \gamma_n)]$$

Substituting $\alpha_n = \frac{1}{4}(1 - \sigma_0)$ and $\delta_n = \frac{1}{2}(1 - \sigma_0) + \gamma_n$

$$m(A_n) = \frac{T}{2} \left\{ \left[\gamma_n + \frac{1}{4}(1 - \sigma_0) \right] \left[2 - \gamma_n - \frac{1}{4}(1 - \sigma_0) \right] \right. \\ \left. - \left[\gamma_n + \frac{1}{4}(1 - \sigma_0) \right] \left(\frac{3}{4}(1 - \sigma_0) - \gamma_n \right) \right\}$$

$$m(A_n) = \frac{T}{2} \left(\frac{4\gamma_n + 1 - \sigma_0}{4} \right) \left[2 - \gamma_n - \frac{1}{4}(1 - \sigma_0) - \frac{3}{4}(1 - \sigma_0) + \gamma_n \right]$$

$$m(A_n) = \frac{T}{8} (4\gamma_n + 1 - \sigma_0)(1 + \sigma_0)$$