DIRECT METAL TO METAL BONDING METHOD FOR HETEROGENOUS 3D INTEGRATION

CHUA SHEN LIN

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DIRECT METAL TO METAL BONDING METHOD FOR HETEROGENOUS 3D INTEGRATION

CHUA SHEN LIN

(B. Eng., Nanyang Technological University)

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

12 January 2020

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Chua Shen Lin

Supervisor Declaration Statement

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11 January 2020

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Date   Tan Chuan Seng

Authorship Attribution Statement

This thesis contains material from 5 paper published in the following peer-reviewed journal(s) from papers accepted at conferences in where I was the first author.

Chapter 3 and 4 are published in the following papers:

[1] S. L. Chua, J. M. Chan, S. C. K. Goh, C.S. Tan, “Cu-Cu Bonding in Ambient Environment ArN2 Plasma Surface Activation and Its Characterization”, IEEE Transactions on Components, Packaging and Manufacturing Technology, Preprint, Oct 2018, DOI: 10.1109/TCPMT.2018.2875460

[2] S. L. Chua, G. Y. Chong, Y. H. Lee, C. S. Tan, “Direct copper-copper wafer bonding with Ar/N2 plasma activation”, Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 1-4, 2015

[3] S. L. Chua, C. S. Tan, “Cu-Cu Die to Die Surface Activated Bonding in Atmospheric Environment Using Ar and Ar/N2 Plasma”, Pacific Rim Meeting on Electrochemical and Solid-State Science, Hawaii, USA, October 2-7, 2016

[4] S. L. Chua, L. Hu, J. Tao, C. S. Tan, “Process Development and Reliability Study on Ar/N2 Plasma Activated Cu- Cu Wafer-Level Bonding”, The International Conference on Wafer Bonding – WaferBond’19, Halle/Saale, Germany, December 2- 4, 2019

The contributions of the co-authors are as follows:

- Prof Tan Chuan Seng provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I design and fabricated the test samples in School of EEE, Clean room 1 and 2.
- J.M. Chan performed TCT test and preparation of manuscript drafts.
- S. C. K. Goh performed shear test, leak test and preparation of

manuscript drafts.

- G. Y. Chong performed different plasma pre-treatment on the samples
- Y. H. Lee, J. Tao and L. Hu performed water contact angle, AFM and assisted in the fabrication of samples and preparation of manuscript drafts

Chapter 5 are published in the following papers:

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- Prof Tan Chuan Seng provided the initial project direction and edited the manuscript drafts.
- Asst Prof Holden Li provided the MEMS design advice
- Asst Prof Hao Yu provided the readout circuit design advice
- I prepared the manuscript drafts.
- I performed MEMS fabrication and integration of device
- A. Razzaq designed the readout circuit and testing of the integrated device

12 January 2020

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Date Chua Shen Lin

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Executive Summary

The integration of CMOS and MEMS (sensor) in a small package is essential for IoT. By using 3D integration or packaging, it enables heterogeneous integration of CMOS and MEMS which is difficult by monolithic integration (due to process incompatibility). In 3D integration or packaging, interconnects from both chips are required to be joined with low electrical resistance and sufficient mechanical strength to withstand forces experienced in the normal usage of the device. In this dissertation, Cu-Cu fusion bonding with plasma surface treatment and Al-Au thermo-compression bonding were investigated for 3D integration and packaging. Both bonding methods allow the use of metals commonly used in semiconductor manufacturing without the need of specialized in-situ alignment with plasma pretreatment equipment enabling ease of adaptation of the bonding methods. The bonding methods were evaluated for short bonding duration and with option of batch anneal to improve the properties of the bonds.

On Cu-Cu fusion bonding with pre-treatment plasma, the effects of plasma pre-treatment on bonding surface were investigated with X-ray photoelectron spectroscopy (XPS). The XPS results concur that the Ar + N_2 plasma was able to form Cu_3N compound. Copper oxides were also observed to decrease with increasing pre- treatment duration. Hydrophilicity and surface roughness of treated surface were measured. Ar + N_2 plasma parameters yielding the best hydrophilicity results was used for the Cu-Cu fusion bonding subsequently. Atomic force microscopy (AFM) showed that the pre-treatment was able to reduce surface roughness of as-deposited Cu potentially improving the bond quality.

Blanket wafer Cu-Cu fusion bonding was demonstrated. Microstructure studies were performed on the bonded samples at their bonding interface before and after temperature cycling test. No delamination or oxidation were observed of all samples. N was not observed in TEM/EES showing that the Cu_3N compound has decomposed. Zig-zag bonding interface was observed for

sample with Ar + N_2 plasma pre-treatment before and after the temperature cycling test (TCT). Shear strength test have been performed. Dummy dies without plasma pre-treatment were fusion bonded but failed, indicating that the pre-treatment is essential in the Cu-Cu fusion bonding process. 20.3 MPa was achieved with post-annealing temperature of 290 °C for 2 h. Hermetic sealing achieved below 5×10^{-8} atm.cc/s He leak rate. Daisy chain bonds did not fail after 1000 cycles TCT. Cross bridge kelvin resistor (CBKR) structure showed that the dies were able to be uniformly bonded with the Cu-Cu fusion bonding method.

On Al-Au thermo-compression bonding, shear strength and hermetic sealing were investigated. Al and Au were shown to be completely inter-diffused. The Al-Au thermo-compression bonding was used to demonstrate a novel CMOS-MEMS integration where the CMOS die act as an active capping to the MEMS. Al pads were used on the CMOS dies while Au pads were used on the MEMS. This allows direct Al-Au bonding without additional layers. For this demonstration, Silicon on insulator (SOI) single axis accelerometer dies were fabricated to have matching I/O pads and sealing ring design with the MPW CMOS dies for readout and hermetic sealing (active cap). . The stacked chip has thickness of 1155 μm and underwent mechanical shock test for reliability test which the samples have passed. This shows that Al-Au thermocompression bonding can achieve 3D integration of CMOS and MEMS reliably with lower thickness compared to traditionally packaged device.

In this dissertation, Cu-Cu fusion bonding demonstrated good shear strength and hermetic sealing without the need of long bonding time (5 min for die to die bonding). Al-Au thermo-compression bonding has demonstrated a 3D integrated CMOS and MEMS working device with mechanical reliability with a bonding time of 10 min. Both solid state technologies are promising in 3D integration with bonding time of 5 to 10 min whilst being easily adapted with semiconductor manufacturing equipment.

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Chapter 1 **Introduction**

1.1 Background

Transistor is becoming smaller through transistor scaling, where channel length, gate dielectric thickness and junction depth are reduced. The scaling of transistor has improved the device to become more energy efficient, increased in performance, and reduced chip size as shown in Figure 1 and Figure 2 [1]. Figure 1 shows increased performance and decreased power consumption when the node size decreases. Figure 2 shows the reduction of chip area with scaling. With better energy efficiency and smaller chip size, more capabilities like sensing, processing of sensor readings and communication to network can be included to devices without noticeable increase in size or power consumption. This allowed manufacturers to transform their products into internet of things (IoT) where their products are connected to the network enabling feedback to the user or control by the user through the network. Scaling also allows manufacturers to create IoT products that was not feasible before.

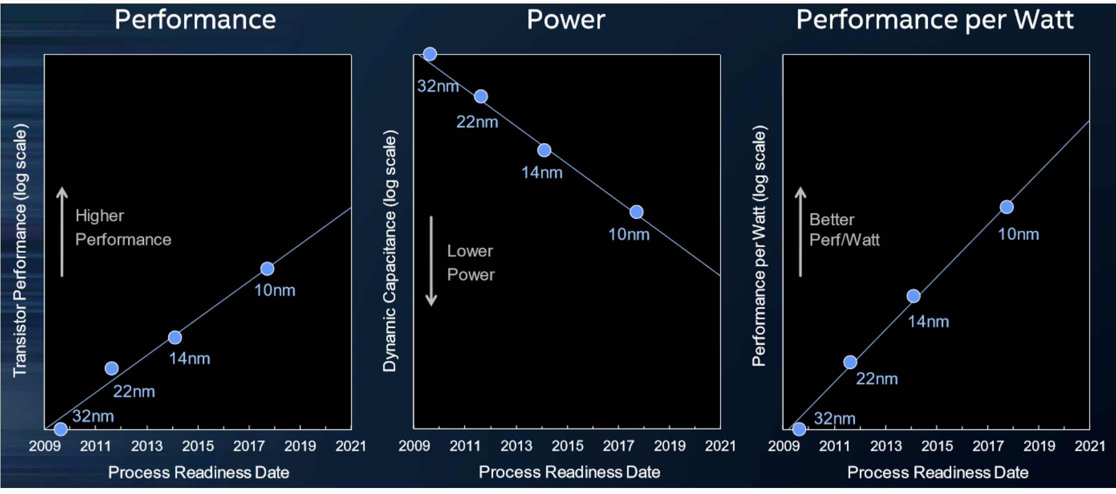

Figure 1 : Graphs showing transistor performance and power with scaling by Intel. [1]

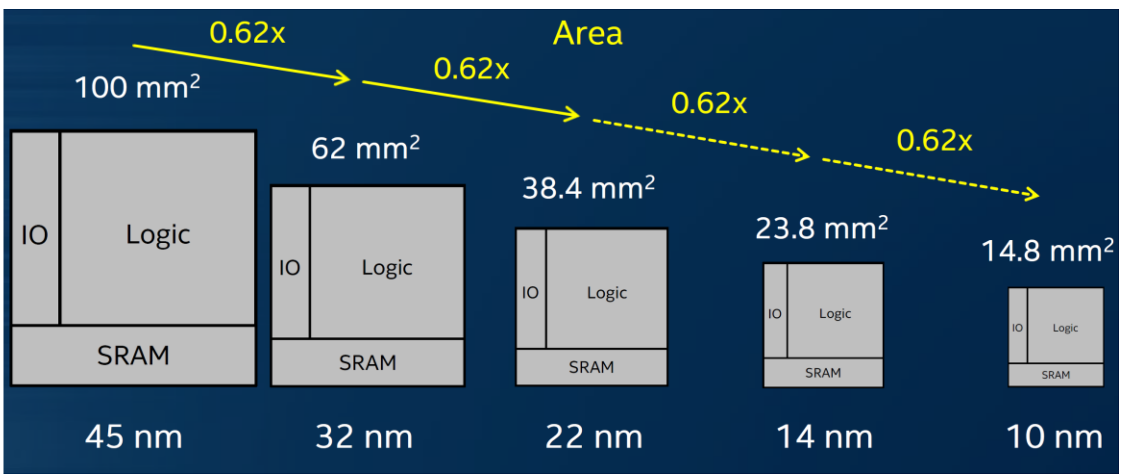

Figure 2 : Schematics showing chip area reduction with scaling by Intel. [1]

However, Cu interconnects is unable to scale with the process technology due to surface electron scattering and grain boundary scattering which increases the line resistance of interconnects. With decreasing linewidth of Cu metal lines, resistivity increase sharply below 100 nm due to side wall and grain boundary electron scattering as shown in Figure 3 [2]. Furthermore, as process technology scales, effect of resistance-capacitance (RC) delay from global interconnects becomes increasingly predominant as shown in Figure 4 [2]. However, without global interconnect scaling, overall chip size will not be reduced substantially with only transistor scaling. This results in large packaged device size unfavorable for IoT. Hence innovative integration and packaging technologies are required to reduce RC delay and interconnects resistance. Three-dimensional (3D) integration and packaging have the capability to reduce overall footprint of packaged device through the stacking of dies. Reduction in interconnects length from the stacking of dies also improve energy efficiency and performance.

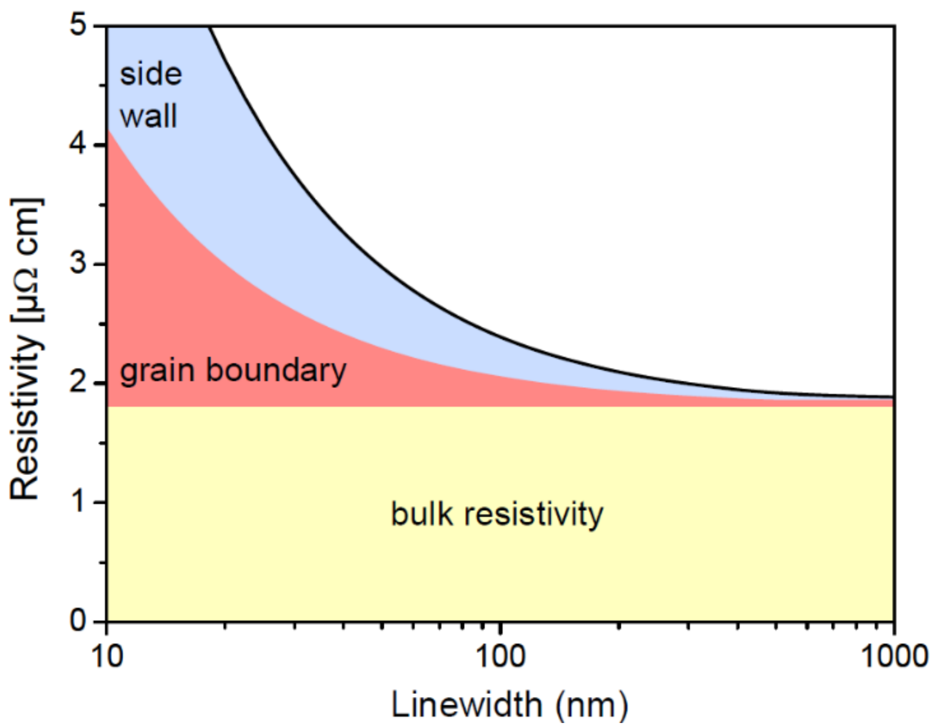

Figure 3 : Electron scattering effects on Cu resistivity in decreasing linewidth. [2]

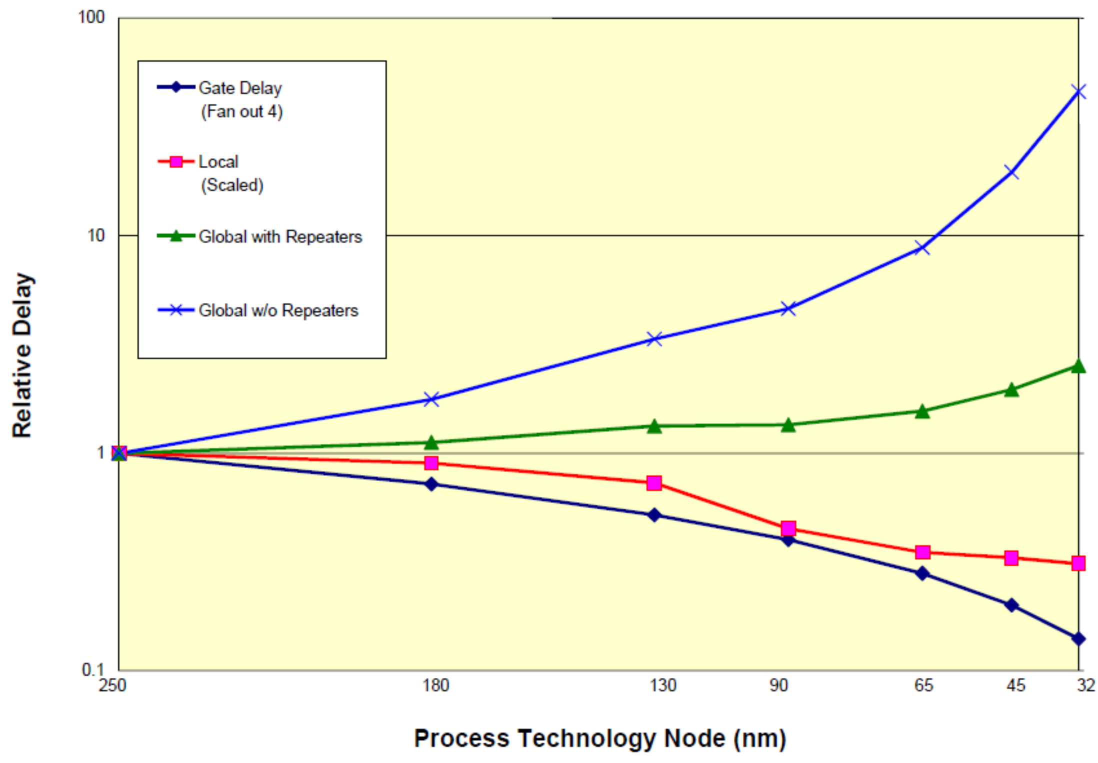

Figure 4 : Delay for Metal 1 and Global Wiring versus Feature Size. [2]

The International Technology Roadmap for Semiconductors (ITRS) has assessed 3D integration and packaging to allow functional diversification ("More than Moore") in future integrated systems[3]. Figure 5 from ITRS shows the

direction of the semiconductor industry. Continuous transistor scaling is represented in the Y axis while increasing diversified capabilities to a device is represented in X axis. This coincide with the needs of IoT which requires addition of networking of machine-to-machine and data-gathering sensors to traditional device (functional diversification) without much increase in size and power consumption (scaling). 3D packaging will allow sensors and communicating devices to be packaged with the main computing device in a small and low power consumption package [5]. Instead of placing and connecting devices side by side, the devices are placed vertically and connected with shorter vertical interconnects as shown in Figure 6 [6]. The reduction of interconnect wire length from 3D integration leading to significant reduction in interconnect delay has been simulated by various studies [7] [8] [9].

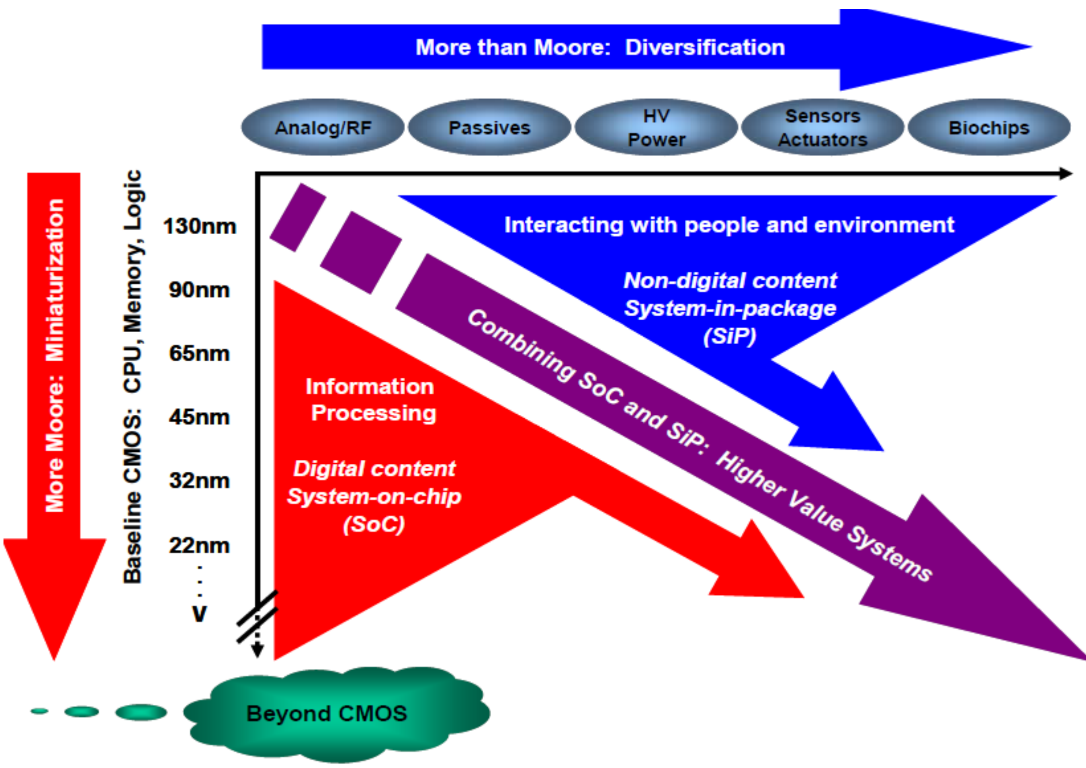

Figure 5 : The dual trend for the combined need for digital and non-digital functionalities in an integrated system. [3]

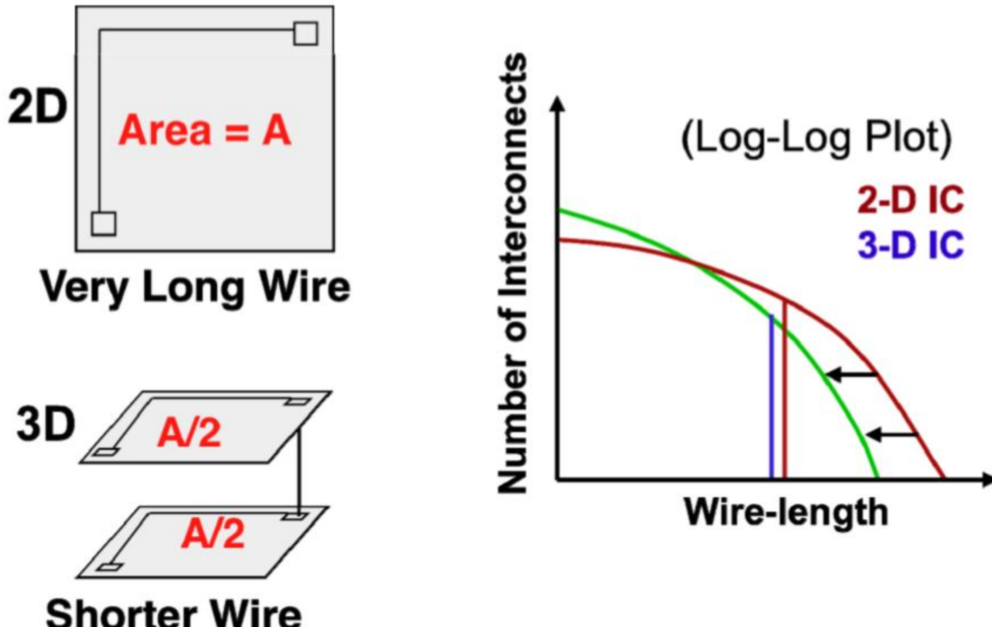

Figure 6 : Comparison of chip footprint, wire length and distribution in a a 3-D vs. 2-D system [6]

1.2 Motivation for Direct Metal Bonding

The integration of CMOS and MEMS (sensor) in a small package is essential for IoT. By using 3D integration or advance packaging (for example, system in package, system on package or multi-chip module), it enables heterogeneous integration of CMOS and MEMS which is difficult by monolithic integration (due to process incompatibility). In 3D integration, CMOS and MEMS dies which are fabricated from different processes can be stacked vertically and connected together into a package that is smaller compared to a traditional side by side placement. Interconnects from both chips are required to be joined with low electrical resistance and sufficient mechanical strength to withstand forces experienced in the normal usage of the device for 3D integration.

Figure 7 shows the different bonding technologies available. Of all bonding methods, only direct metal to metal solid-state bonding, eutectic bonding and solder bonding can provide good electrical contact for the interconnects. However, with liquid phase bonding, there is a limitation to the pitch size of the interconnects. Therefore direct metal to metal bonding chosen in this thesis as it potentially have good electrical and mechanical characteristics whilst allowing fine pitch interconnects.

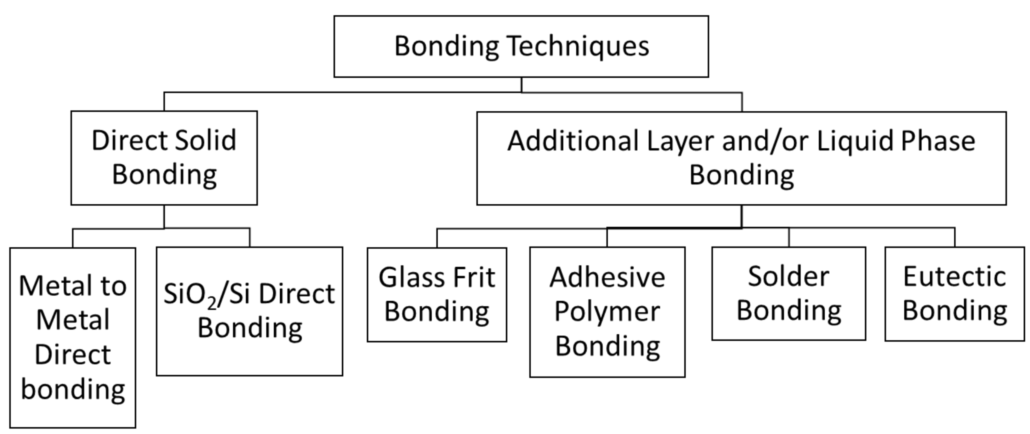

Figure 7 : Different bonding techniques available

Metallic bump interconnection for integrated circuit (IC) chips has long been realized as a practical and necessary method for high performance, high data rate electrical signal transmission [10]. As early as 1969, IBM has demonstrated the use of copper ball joints solder in place for interconnects for logic circuits shown in Figure 8 [11]. The idea of Integrating in the Z dimensional was also conceived by IBM as a way to increase component packing density. Shown in Figure 9, metal pins were solder in place to connect the top and bottom chip [11]. These technologies improved and evolved into the current flip chip bonding technologies.

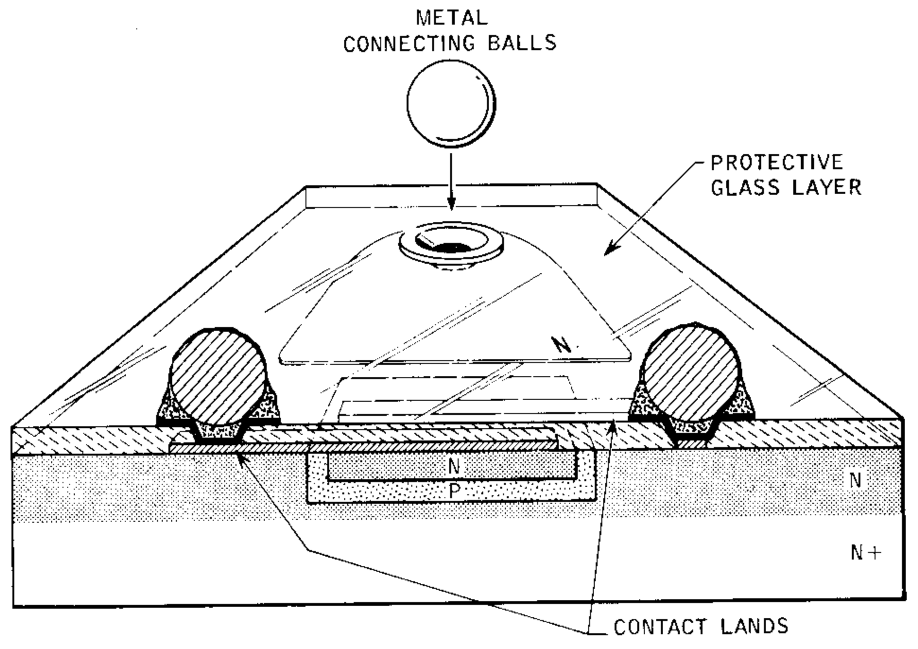

Figure 8: Cross section of transistor with Cu ball joints [11]

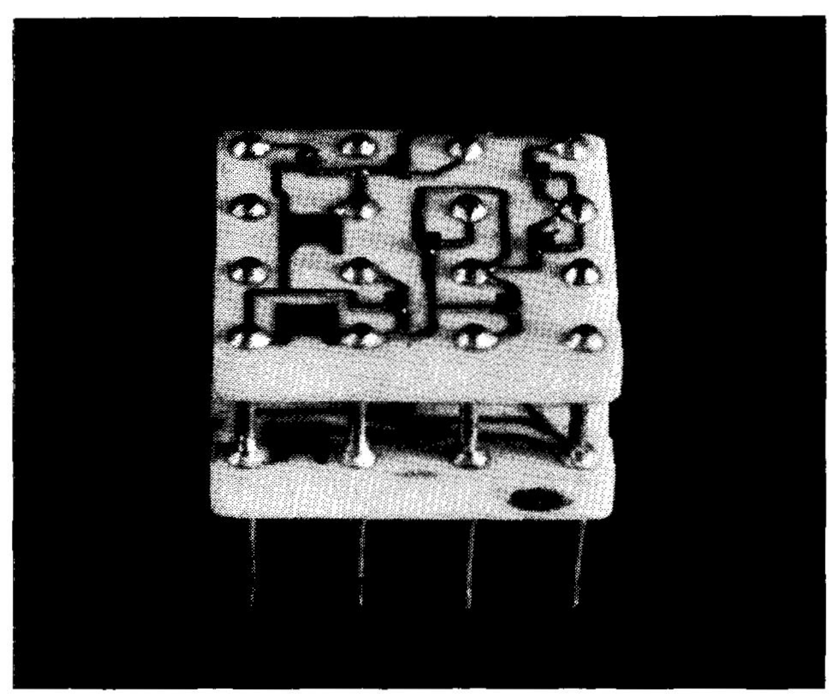

Figure 9: Stacked logic module [11]

Figure 10 shows the evolution of bump/pad bonding technologies [12]. Current flip chip bonding uses Cu pillars with solder caps, which replaced solder bumps to improve reliability of the interconnects when scaled down. Bumpless direct metal to metal bonding uses actual interconnect metal layers for bonding without additional depositing and patterning processes to deposit additional bonding material. Solid-state bonding also enables smaller pitch for interconnects compare to solder and eutectic bonding. Hence a high throughput solid state bonding technology that requires only a short bonding duration will be attractive for 3D integration. Hence bumpless direct metal to metal solid state bonding technology are important as interconnects shrinks.

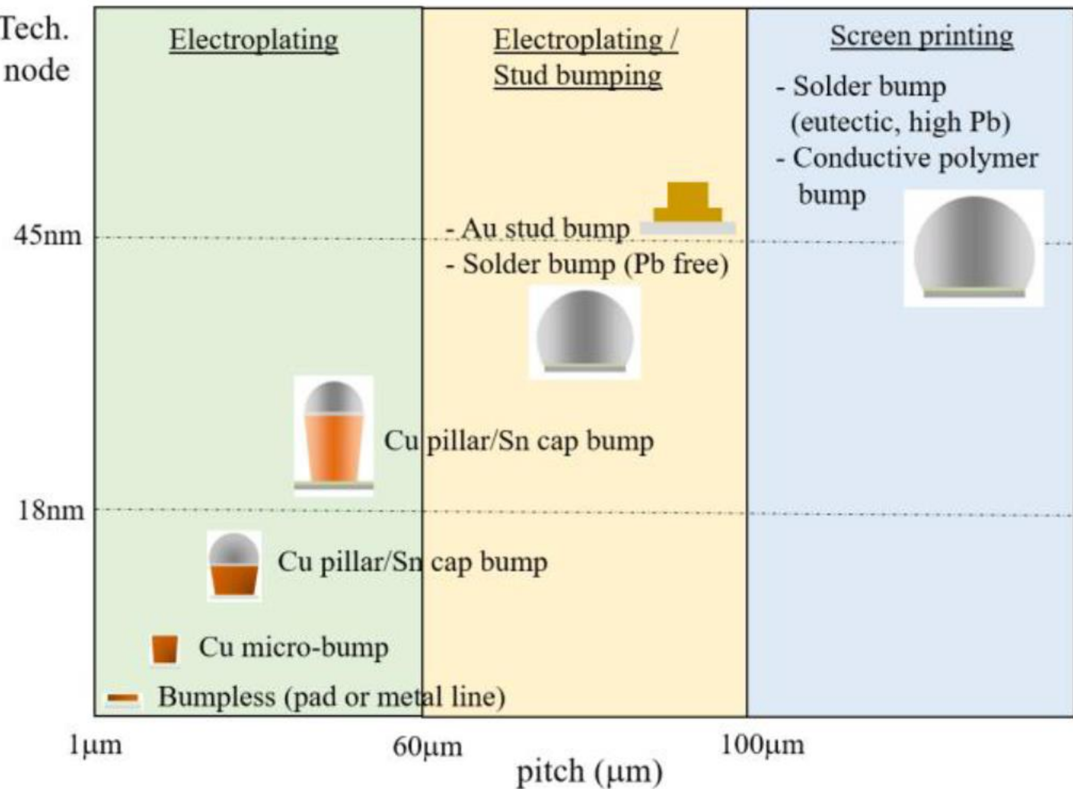

Figure 10: Evolution/shrinking of solder/bump material and structure [12]

Various methods for direct solid-state metal to metal bonding were explored in different studies. These methods includes Cu-Cu thermo-compression, Cu-Cu thermo-compression with different pre-treatments to improve the bonding interface and reduce bonding time, Cu-Cu fusion bonding, hybrid bonding of both dielectric to dielectric and Cu to Cu, and solid state bonding of dissimilar metal. Among these methods, Cu-Cu fusion bonding demonstrated short bonding duration and potentially high strength and reliability as the bonded Cu layers were similar to bulk Cu. For some MEMS dies, Cu is not suitable due to HF etching processes in the fabrication. Al-Au thermo-compression bonding could be used. Al-Au thermo-compression bonding has been demonstrated with short bonding time and the intermetallic properties are well investigated by various studies for wire-bonding.

In this dissertation, Cu-Cu fusion bonding with plasma surface treatment and Al-Au thermo-compression bonding were investigated for 3D integration and packaging. Both bonding methods allow the use of metals commonly used in semiconductor manufacturing without the need of specialized in-situ

alignment with plasma pretreatment equipment enabling ease of adaptation of the bonding methods. The bonding methods were evaluated for short bonding duration and with option of batch anneal to improve the properties of the bonds.

1.3 Scope and Objective

In this dissertation, two different direct metal to metal bonding methods were explored to meet the demands of 3D CMOS and MEMS die to die integration and packaging. Cu-Cu fusion bonding with plasma pre-treatment and Al-Au thermo-compression bonding are the two methods studied as the metals are commonly used as interconnects in modern devices (Cu and Al in CMOS devices and Au in MEMS) and no changes to the fabrication process is required for the adaptation of 3D integration and packaging using the two direct metal to metal bonding methods. Effect of plasma pre-treatment on Cu surface and Cu-Cu fusion bonding were investigated. Electrical and mechanical characteristics, and hermetic sealing capability of the Cu to Cu bonds were investigated. Hermeticity and mechanical properties were also investigated for Al-Au thermo-compression bonding. This will allow a novel 3D integration method of MEMS hermetically sealed with an active CMOS cap using the Al-Au thermo-compression bonding. Lastly a MEMS sensor with a CMOS readout circuit integrated by the novel 3D integration is demonstrated.

The main objectives of this research are:

- To characterize the effect of plasma pre-treatment on Cu surface and Cu-Cu fusion bonding interface.
- To characterize the effect of annealing temperature on mechanical strength and hermeticity for Cu-Cu fusion bonding.
- To demonstrate good mechanical characteristic and hermeticity for Cu-Cu fusion bonding with plasma pre-treatment.
- To show good mechanical characteristic and hermeticity for Al-Au thermo-compression bonding.

- To demonstrate integration of MEMS sensor with a CMOS readout circuit using novel 3D integration method with Al-Au thermo-compression bonding shown in Figure 11.

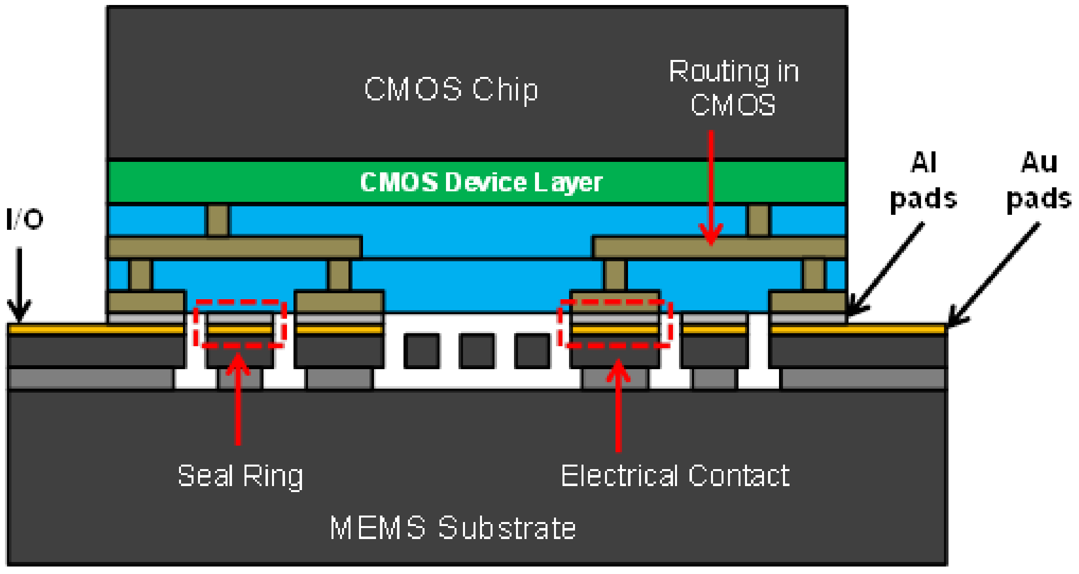

Figure 11: Novel MEMS-CMOS active hermetic cap integration

1.5 Major Contribution of the Thesis

The major contribution of this thesis is listed below:

- Study on plasma effect on surface elemental composition was done on different plasma composition and duration. Effectiveness of the passivation of the plasma were shown in the XPS results. It was found that inclusion of N_2 gas provides passivation effects.
- Study on plasma effect on surface hydrophilicity and roughness was performed. Effectiveness of the plasma in creating hydrophilicity were shown in water contact angle tests while the plasma effect on surface roughness were characterized by AFM. A short plasma duration reduces surface roughness of as-deposited Cu.
- Blanket wafer to wafer Cu-Cu fusion bonding was demonstrated. Wafers were place face to face in a double aligner where they were held in contact using vacuum contact mode at -70 KPa gauge pressure for 1 min. The bonded samples were batch annealed at 300°C for 1 h in a furnace with normal air environment. Microstructures studies on the bonding interface were done and zig-zag patterns were observed for Ar + N_2 plasma pre-treated sample.
- Study on plasma and annealing temperature effects on the bond strength were done. Shear strength test was performed and highest mean shear strength of 20.3 MPa was achieved. Hermetic sealing with Cu-Cu fusion bonding was demonstrated and the daisy chain Ar + N_2 plasma pre-treated sample survived 1000 cycle temperature cycling test.
- Cu-Cu fusion bonding with Ar + N_2 plasma pre-treatment was demonstrated in this thesis with a short bonding time of 1 min for wafer to wafer bonding and 5 min for die to die bonding and ability to be batch annealed. No voids were observed in the bonding interface after annealing.

- Study on process temperature effects on the bond strength were done for Al-Au thermo-compression bonding. Hermetic sealing with Al-Au thermo-compression was demonstrated
- SOI single axis accelerometer MEMS were fabricated and bonded to a CMOS readout chip using a novel active hermetic cap 3D integration method. The integrated device survived mechanical shock test carried out as specified in JEDEC standard.
- Al-Au thermocompression bonding was demonstrated in this thesis with an integrated CMOS-MEMS device that is significantly thinner than traditionally integrated device by the removal of a passive capping layer.

1.6 Organization of the Thesis

The organization of this thesis is outlined below:

i. In Chapter 1, a brief introduction to the device scaling of microelectronics was given, followed by the motivation, objectives, and major contribution of this thesis.

ii. In Chapter 2, a literature review was presented on the bonding technologies for 3-D integration and packaging.

iii. In Chapter 3, Cu-Cu fusion bonding with plasma treatment and the effects on the Cu surface and bonding interface were studied.

iv. In Chapter 4, evaluation of mechanical, electrical and hermeticity properties of Cu-Cu fusion bonding with plasma treatment were presented.

v. In Chapter 5, Al-Au thermo-compression bonding of CMOS and MEMS with novel 3D integration method was demonstrated.

vi. In Chapter 6, a summary of this thesis and recommendations for future work were provided.

Chapter 2 Overview and Benchmark of Bonding Methods

2.1 Introduction

Various methods for direct solid-state metal to metal bonding were explored in different studies. These methods includes Cu-Cu thermo-compression, Cu-Cu thermo-compression with different pre-treatments to improve the bonding interface and reduce bonding time, Cu-Cu fusion bonding, hybrid bonding of both dielectric to dielectric and Cu to Cu, and solid state bonding of dissimilar metal. In this chapter, the bonding mechanism for the various methods, solid-state diffusion bonding, is presented. After which, the methods were reviewed with their bonding temperature, force and time needed. Lastly, they are compared with the direct solid-state metal to metal bonding used in this thesis.

2.2 Solid-State Diffusion Bonding

Diffusion bonding is a solid-state welding process by which two prepared surfaces are joined at 0.5 to 0.8 of the absolute melting point of the material and under applied pressure [13]. Diffusion bonding involves a sequence of stages [14]. Firstly, the surfaces to be joined are brought in contact, in which the pressure broke up the surface oxides at the contact points. Secondly, the surface layers are deformed, and volumetric diffusion processes take place followed by recrystallization of the grains. These stages in the diffusion bonding continued repeatedly and overlappingly as the asperities become smaller and continuously new surfaces are bought to contact from the deformation caused by the pressure applied.

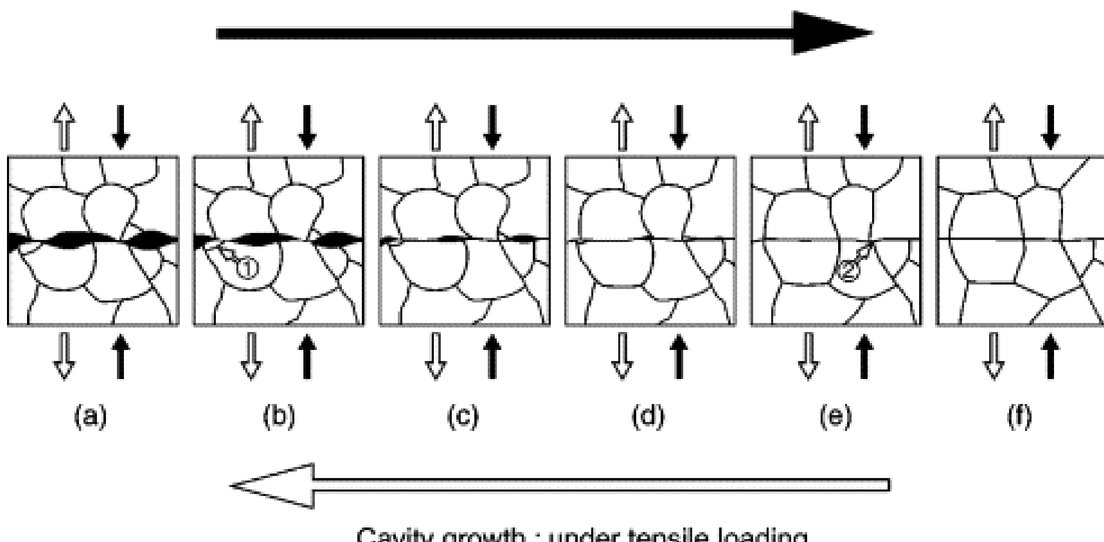

Figure 12: Schematic view of the formation mechanism of the diffusion-bonding process [15].

Diffusion coefficient can be expressed as a function of temperature as follows:

$$D = D_0 e^{\left(\frac{-Q}{kT}\right)} \tag{1}$$

Where

- D is the diffusion coefficient at bonding temperature (T),
- D_0 is the constant of proportionality,
- Q is the activation energy for diffusion,
- T is the absolute bonding temperature, and
- k is the Boltzmann's constant.

From equation 1, the higher the temperature, the higher the diffusion coefficient. This will result in shorter bonding time, or increased intermixing of metal grains and increase grain size. Traditional diffusion bonding temperature is approximately 50-70% of the absolute melting temperature of the materials. This temperature is too high for CMOS devices (melting point of Cu is at 1358 K, Al at 933.5 K and Au at 1337 K). However, using CMOS device acceptable temperature for bonding, the resultant bonding duration required will be unacceptably long.

2.2.1 Cu-Cu Thermo-compression Bonding

Low temperature Cu-Cu bonding methods are highly sought after as Cu is a common material used for the back end of line (BEOL) interconnects. Since solid state diffusion bonding consist of deformation of the surface due to pressure applied and diffusion, by reducing deformation required (smaller asperities between the bonding surface), bonding duration can be reduced. With smaller gaps between the surfaces, less deformations and volumetric diffusion are required to bring all bonding surfaces together. With chemical mechanical polishing (CMP), low roughness value in single digit nanometer range can be obtain in CMOS and MEMS devices, thus reducing bonding duration required with the lowered bonding temperature. Cu-Cu thermo-compression bonding has been demonstrated by various studies at temperature ranging from 100 °C to 300 °C [16] [17] [18] [19] [20].

2.2.2 Cu-Cu Thermo-compression Bonding with Self-Assembled Monolayer

Further improvement to the bonding surface condition can be made by removing the surface oxides and preventing such oxides from forming before bonding. One such solution is to use self-assembled monolayer such as alkane-thiol to protect the Cu surface immediately after the removal of its oxides. The self-assembled monolayer will be desorbed in-situ when annealing, exposing the pristine Cu surface for bonding. Cu-Cu Thermo-compression Bonding with self-assembled monolayer is demonstrated by various studies as shown in Figure 13 [21] [22] [23]. Bonding interface using self-assembled monolayer protection have a more pronounced zig-zag boundaries as compared to those without protection as shown in Figure 14 by L. Peng el at. [24].

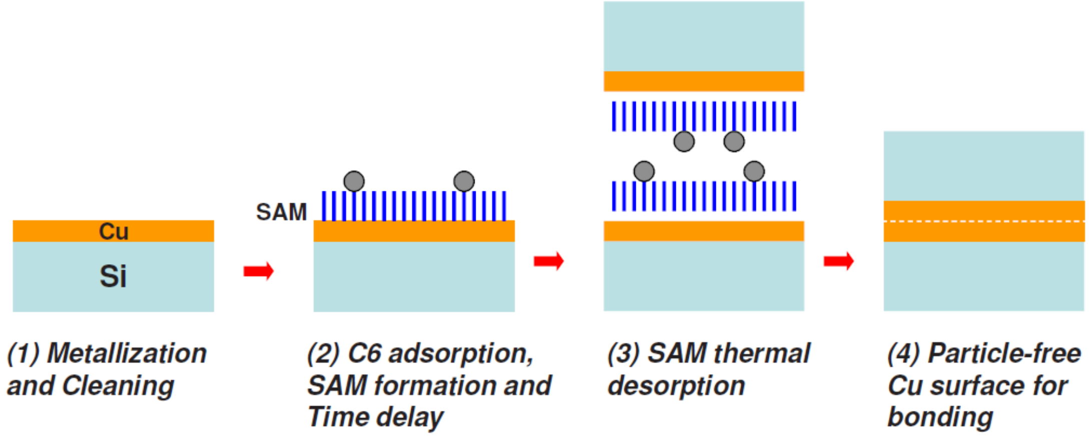

Figure 13: A summary of process flows on using SAM of alkanethiol as a passivation layer on Cu surface [21]

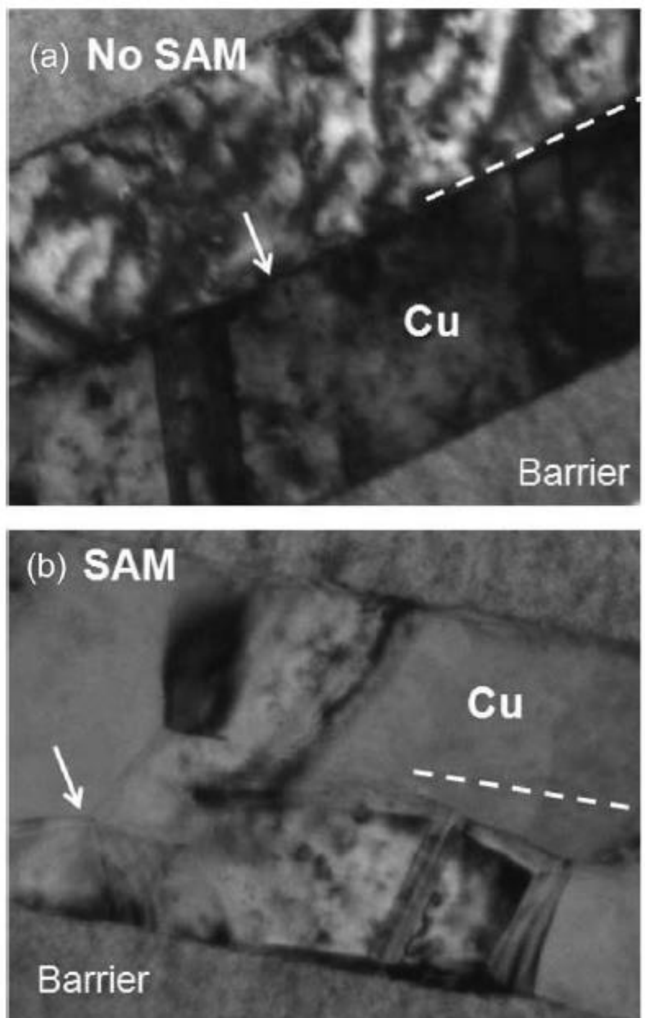

Figure 14: Transmission electron microscopy images Cu grain structures across the bonding interface, (a) without SAM and (b) with SAM treatment [24]

2.2.2.1 Cu-Cu Thermo-compression Bonding with Copper Nitride Passivation

Studies have used metastable copper nitride that was created with Ar + N_2 plasma treatment to passivate the copper surface and prevent it from oxidation [12] [25] [26]. One advantage of copper nitride passivation over SAM is that the nitrogen from the decomposed copper nitride can diffuse through the Cu when the surfaces are in contact unlike the alkane-thiol, which is required to be purged from the Cu surface before contact.

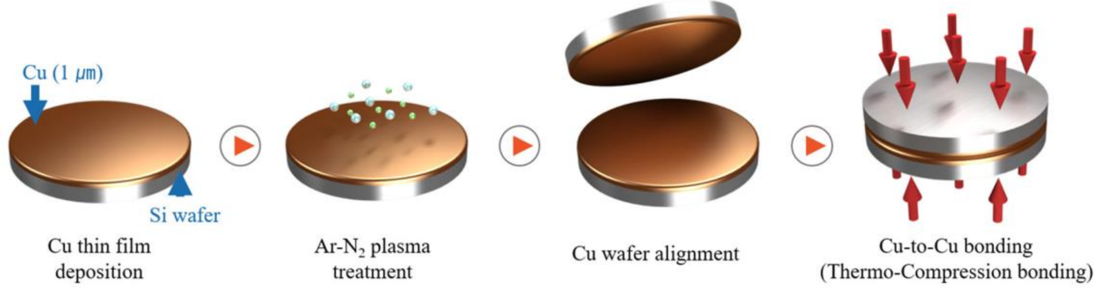

Figure 15: Schematic diagram of process flow [25]

2.2.2.2 Cu-Cu Thermo-compression Bonding with Formic Acid or Forming Gas Pretreatment

Other than protecting the surface from oxidation after clean, in situ cleaning prior to bonding can be performed. Various studies have used formic acid (HCOOH) vapor [27] [28] [29] [30]or forming gas (N_2 + H_2) [31] to reduce the Cu surface oxide and have shown lower bonding temperature and/or bonding duration. SivaChandra Jangam et al have demonstrated an die assembly process using thermo-compression with formic acid vapor pretreatment ifor 15 s as shown in Figure 16 [27].

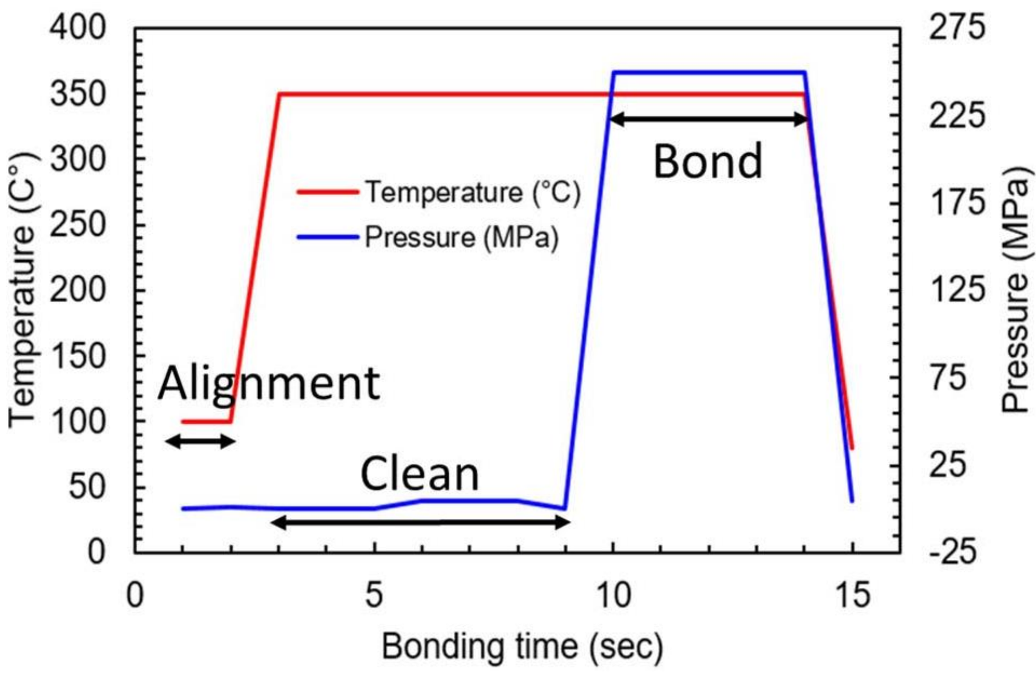

Figure 16: Assembly process flow showing the bonding of a single die [27]

2.2.2.3 Cu-Cu Thermo-compression Bonding with Plasma Cleaning

Plasma can be used to remove the surface oxide and contaminants from the bonding interface. Various studies have used Ar plasma [32] or Ar + H2 plasma [33] for the cleaning. One advantage of plasma cleaning over formic acid or forming gas is that the physical bombardment of ions can not only remove surface oxides, it can also remove other contaminants. However, without a specialized equipment that can perform both plasma cleaning and bonding with alignment in situ, the samples will be exposed to the atmospheric environment during the transfer from the plasma chamber to the bonding chamber. The brief exposure of Cu surface to the atmosphere will cause oxidation on the bonding surface, thus reducing the effect of the plasma cleaning.

2.2.3 Cu-Cu Fusion Bonding

When the bonding surface roughness is further reduced to nanometers and below, asperities become so small that with pressure applied, most of the bonding surface will be close enough to experience van der Waals forces that pull them together [34]. Van der Waals forces is described in Lennard-Jones potential shown in Equation 2. In the equation, attraction or repulsion force is

relative to the distance between the atoms. Figure 17 shows a plotted Lennard-Jones potential. At far distances, right side of the graph, the attraction force is very low, as the distance between the atoms or molecules reduces below 2 r_0 (towards the left), the attraction force increases drastically. This will pull them closer together until Pauli repulsion starts to come into effect, preventing the atoms or molecules from overlapping electron orbitals.

$$\Phi_{LJ}(r) = 4\epsilon \left[\left(\frac{r_0}{r}\right)^{12} - \left(\frac{r_0}{r}\right)^{6} \right] \quad (2)$$

Where:

- Φ_{LJ} is the intermolecular potential between the two atoms or molecules,
- ϵ is the well depth and a measure of how strongly the two particles attract each other,
- r_0 is the distance at which the intermolecular potential between the two particles is zero (σ gives a measurement of how close two nonbonding particles can get and is thus referred to as the van der Waals radius. It is equal to one-half of the internuclear distance between nonbonding particles.), and
- r is the distance of separation between both particles (measured from the center of one particle to the center of the other particle).

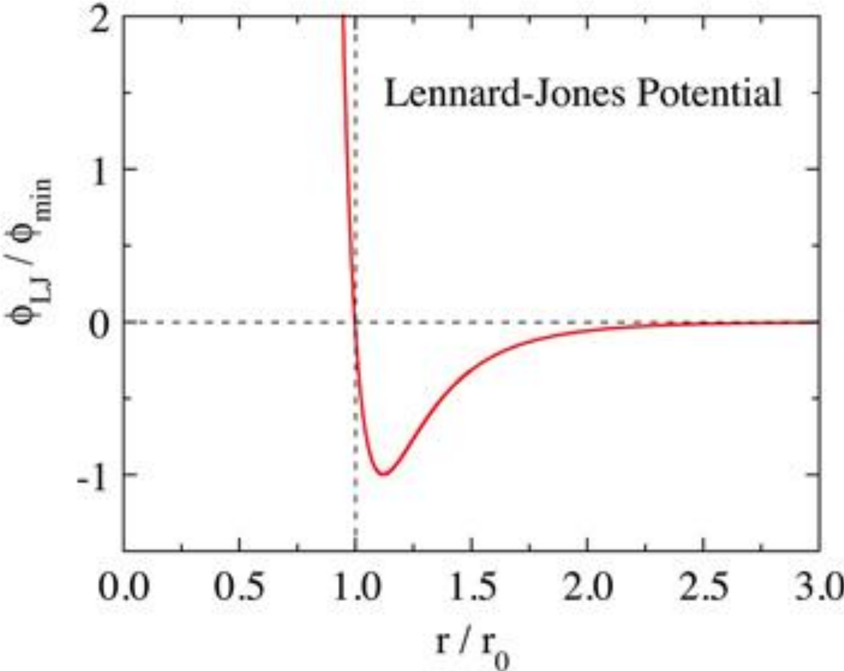

Figure 17: Lennard-Jones potential energy. The depth of the potential well is Φ_{min} and the zero of the potential energy is at $r = r_0$. [35]

When the surface roughness is low enough, van der Waals force are able to hold the bonding samples together after the initial pressure applied, continual pressure is not required for diffusion bonding. This allows the bonding process to be separated into two portion, pre-bonding (alignment of samples and force applied to allow sufficient van der Waals force) and post-bonding annealing (heat is applied to promote diffusion across the bonding interface).

2.2.3.1 Chemical Mechanical Polishing Cu-Cu Direct Bonding

Using CMP optimized for Cu polishing, low root mean square (RMS) roughness (< 0.5 nm) can be achieved [36] [37]. Contaminants and surface oxides are removed during the CMP process. After the CMP process, the wafers are cleaned and pre-bonded in atmospheric environment. As the samples are smooth and planar, very low force is required for pre-bond. Post-bonding annealing is applied to diffuse the newly formed oxides and promote grain growth across the bonding interface [38].

2.2.3.2 Surface Activated Bonding in Room Temperature with Ar Ion Beam Cleaning

With smooth Cu bonding surface from CMP process, and a specialized setup (shown in Figure 18) for transferring the samples from the cleaning chamber to the bonding chamber in ultra-high vacuum (UHV) at approximately 10^{-8} Torr, surface activated bonding (SAB) can be achieved [39] [40] [41]. With smooth Cu surface, the bonding only requires pressure to be applied to create sufficient van der Waals force. Moreover, due to the clean surface, annealing is not required to diffuse the oxides from the bonding interface. Hence the bonding is completed with just force application.

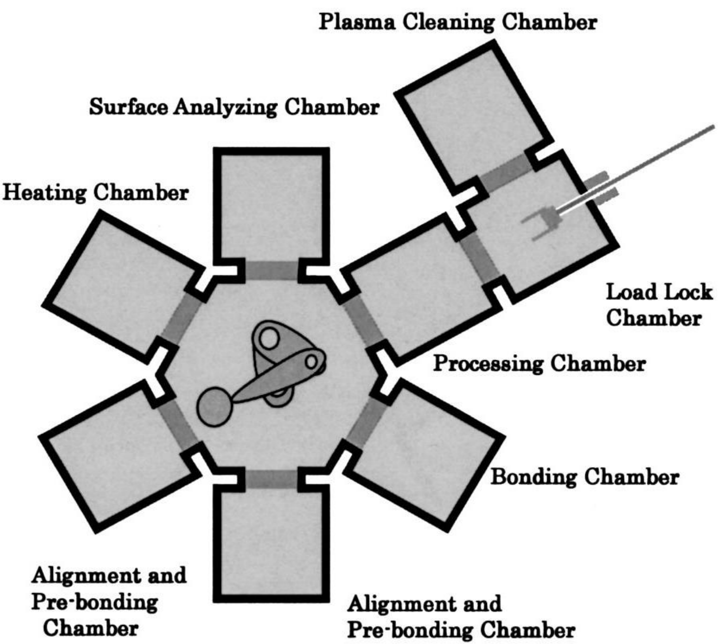

Figure 18: Schematic view of surface activated bonding machine [39]

2.2.4 Cu-Cu Hybrid Bonding

Cu-Cu hybrid bonding combine short bonding duration dielectric and slow diffusion bonding of Cu-Cu bonding. Dielectric bonding with short bonding duration and low temperature are firstly performed to hold the samples together. Dielectric bonding of either adhesive bonding such as benzocyclobutene (BCB) [42] [43] or SiO_2 – SiO_2 fusion bonding [44] [45] [46] [47] as shown in Figure 19, were used. In Figure 19, CMP were performed on both wafers to obtain low surface roughness. Typically, surface roughness for SiO_2 / SiO_2 fusion bonding requires low surface roughness much alike to Cu-Cu fusion bonding [48] [49] [50]. After which, plasma activation was applied on both surfaces (to reduce the annealing temperature required for SiO_2 – SiO_2 fusion bonding to CMOS device acceptable temperature). The wafers were aligned brought together allowing the SiO_2 surface to fusion bond. The dielectric bonds hold the samples together, and when heated during annealing while the Cu expands. The expansion of the Cu presses the Cu bonding surface together, thus resulting in diffusion bonding. This method eventually bonds both the dielectric and interconnect providing a stronger attachment. Cu surface roughness requirement is not as high compared to Cu-Cu fusion bonding. However, as BEOL interconnects densify, more Cu bonding pads are required. Without increasing the chip size, the Cu

bonding pads will replace dielectric area which causes reduction in the dielectric bonding area. Hence the bonding method will restrict on the density of BEOL interconnect in order to have enough dielectric bonding area to hold the samples together for Cu-Cu bonding during annealing.

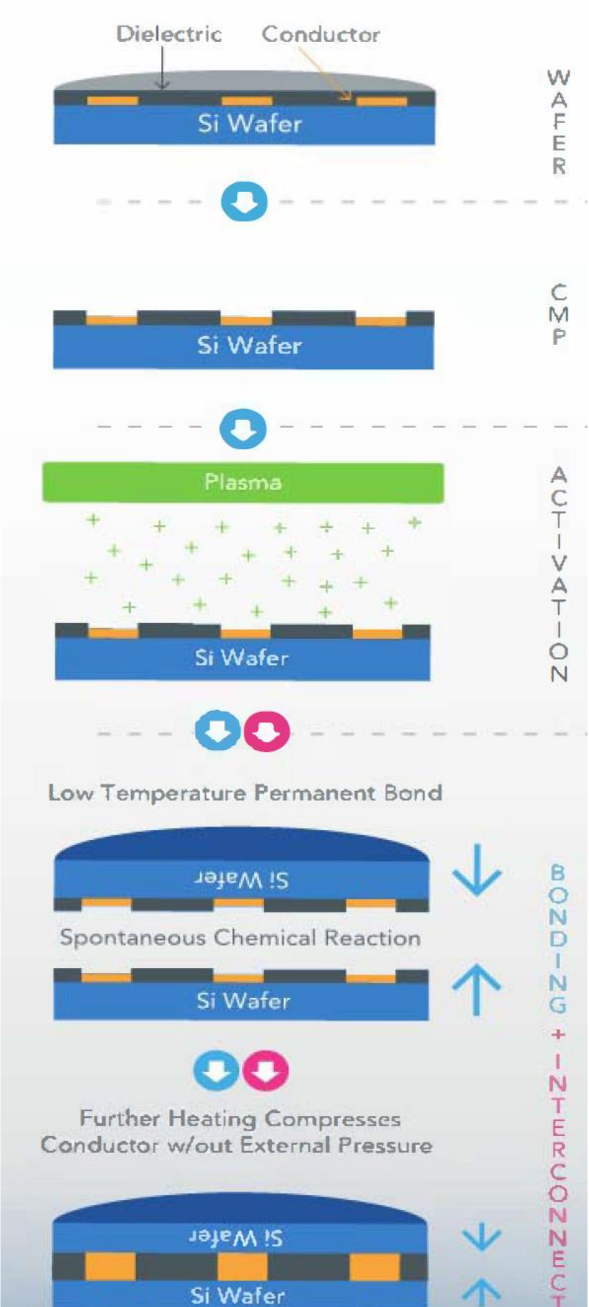

Figure 19: DBI bonding process flow [45]

2.2.5 *Ag-Ag Bonding with Ag_2O Reduction*

Other metals bonding methods were explored by different studies to achieve lower bonding and annealing temperature and/or shorter bonding and

annealing duration. Ag-Ag bonding was achieved in a study at 210 °C with 1.38 MPa static pressure for 30 min [51]. Firstly, Ag_2O on the surface was created from O_2 plasma. The Ag_2O decomposed into Ag atoms in form of gas at temperature higher than 186 °C. The as produced gaseous Ag condenses on the bonding interface resulting on a smooth surface. The study demonstrated lower bonding temperature and shorter duration compared to Cu-Cu thermocompression bonding.

Figure 20: Ag-Ag bonding structure design [51]

2.2.6 Al-Al Surface Activated Bonding

Al-Al bonding has also been studied. Studies have demonstrated Al-Al SAB in place of Cu-Cu [52] [53]. Al is also one of the commonly used BEOL interconnect materials. Samples with a roughness of maximum height difference of about 8 nm and spatial distances of about 5 to 50 nm were used for the bonding demonstration. Similar to SAB Cu-Cu bonding, ion bombardment was used to clean the surface from oxides. The samples are bonded together with only force applied in UHV like Cu-Cu SAB described previously.

2.2.7 Cu-Au Solid-State Bonding

Instead of similar metal solid-state bonding, dissimilar metals solid-state bonding can be performed. The metals can be chosen to have higher diffusivity within each other as compared to self-interdiffusion hence allowing even lower bonding temperature and/or duration. Cu commonly used for CMOS and Au commonly used in MEMS can be solid-state bonded together without additional material. A study has demonstrated for Cu-Au bonding at 200 °C for 5 min where Au was deposited onto columns to prevent oxidation of Cu [54]. However, the

Cu bonding interface (unprotected surface) must be cleaned before bonding to remove copper oxides which will cause the bonding to fail.

2.2.8 Cu-Sn Solid-State Bonding

Cu-Sn solid-state bonding was performed in studies achieving low bonding temperature from 150 to 200 °C [55] [56]. By bonding below the eutectic temperature, reflow is prevented to allow small bump pitches. Flux or plasma cleaning was used for the removal of oxide on both Cu and Sn surfaces.

2.2.9 Al-Ag Solid-State Bonding

A study has demonstrated Al-Ag solid-state bonding for bonding chips to direct bond aluminum (DBA) substrates [57]. DBA substrates are better than direct bond copper (DBC) substrates in thermal cycling tests as there is lower thermomechanical stress at the aluminum/ceramic interface and less strain hardening during thermal. Metal that can inter-diffused through the thin aluminum oxide layer are required. When bonding with Ag, Ag and Al atoms inter-diffused through the thin aluminum oxide layer to react and form Ag_2Al and Ag_3Al at bonding temperature of 425 and 450 °C.

2.2.10 Al-Au Solid-State Bonding

Other than Cu, Al is also commonly used in CMOS backend metallization. Hence for CMOS and MEMS heterogenous integration, Al (used in CMOS) to Au (used in MEMS) bonding can be used. A study has demonstrated Al-Au solid-state bonding for vacuum sealing of MEMS devices at bonding temperature of 250 °C [58]. Al-Au thermocompression bonding has also been studied for use in flip-chip applications [59]. Au and Al inter-diffused through the thin aluminum oxide layer to form Al-Au intermediate metal compound (IMC) at the bonding temperature. Special care have to be taken in the bonding process to prevent brittle $AuAl_2$ from forming.

2.3 Summary and Comparison of Solid-State Bonding

Table 1 summarized the different bonding methods reviewed in this chapter and compared with the bonding method in this work. The parameters

compared in the table are namely surface roughness, bonding temperature, bonding time and reliability. Since fusion bonding requires low surface roughness (less than 1 nm), the surface requirement for fusion bonding will be depicted as high (☹) with other bonding method low (☺). Since similar metal bonding methods, like Cu-Cu and Ag-Ag bonding, produces bonding interface similar to bulk material, their reliabilities are potentially higher than dissimilar metal bonding. Hence for reliability, similar metal bonding methods are depicted as attractive (☺) while dissimilar metal bonding are not (☹). Bonding or annealing temperatures above 300 °C are categorized as unattractive (☹). All bonding methods have a trade-off between surface roughness requirement and bonding duration. However, with CMP processes, low surface roughness is achievable and a trade-off that is acceptable if the bonding throughput is high.

The Cu-Cu fusion bonding method demonstrated in this thesis presents a few advantages as compared to the methods reviewed. Namely high throughput (with wafer to wafer bonding and batch annealing), potentially high reliability with no intermetallic, ease of adaption with commonly used material, dry process and no requirement of specialized equipment (ultra-high vacuum or special gases) for the bonding.

Advantage of Cu-Cu fusion bonding method using plasma pre-treatment demonstrated in this thesis over Cu-Cu fusion bonding with CMP and hybrid bonding is that the plasma pre-treatment Cu-Cu fusion bonding method allows die-to-die bonding, die-to-wafer bonding, and wafer-to-wafer bonding. Cu-Cu fusion bonding with CMP only allows wafer-to-wafer bonding as the bonding must occur right after the CMP process. Die-to-die and die-to-wafer bonding were also not demonstrated by hybrid bonding.

The Al-Au thermocompression bonding demonstrated in this thesis is attractive for the novel active cap MEMS CMOS integration method as the combination of material can be commonly found on CMOS and MEMS dies. No additional layers and processing are required for the bonding.

Bonding Technologies	Surface Requirement	Bonding Duration	Temperature	Reliability
Cu-Cu Thermo-compression (TC)	☺	☹ (1 h)	☺300 °C	☺
Cu-Cu TC with Copper Nitride	☺	☹ (1 h)	☺300 °C	☺
Cu-Cu TC with Formic Acid or Forming Gas	☺	☺ (5 s)	☹350 °C	☺
Cu-Cu TC with Plasma Cleaning	☺	☹ (1 h)	☺250 °C	☺
Cu-Cu Fusion Bonding with CMP	☹	☺ (pre-bond, few s)	☺ (Post-bonding anneal, 200 °C)	☺
SAB	☹	☺ (few s)	☺N.A.	☺
Cu-Cu Hybrid Bonding	☹	☺ (pre-bond, few s)	☺ (Post-bonding anneal, varies)	☺
Ag-Ag Bonding with Ag_2O	☺	☹ (30 min)	☺210 °C	☺
Cu-Au Solid-State Bonding	☺	☺ (5 min)	☺200 °C	☹
Cu-Sn Solid-State Bonding	☺		☺150 °C	☹
Al-Ag Solid-State Bonding	☺	☺ (10 min)	☹450 °C	☹
Al-Au Solid-State Bonding	☺	☹ (45 min)	☺250 °C	☹
Cu-Cu Fusion Bonding (This work)	☹	☺ (pre-bond, 5 min)	☺(Post-bonding anneal, 250 °C)	☺
Al-Au TC Bonding (This work)	☺	☺ (10 min)	☺300 °C	☹

Table 1: Summary of process parameters of literature review bonding methods with ☹ depicting unattractive parameters and ☺ depicting attractive parameters.

Chapter 3 **Study on Plasma Treatment Effects on Cu Surface and Bonding Interface**

3.1 Introduction

In this chapter, plasma pre-treatment effects for Cu bonding surface were investigated. Various studies have used plasma for preparation of Cu surface for bonding, however none have performed Cu-Cu fusion bonding in ambient environment. Cu-Cu fusion bonding in ambient environment is attractive as the pre-bonding step do not require heat, only require a short duration, and do not need specialized in situ bonding equipment. Although long annealing is required to improve the bonding strength, it can be done in batches, saving time and cost. The objective of this chapter is to evaluate different plasma pre-treatments to achieve clean surface with possibility of passivation to allow Cu-Cu fusion bonding in ambient environment. Commonly used gas sources for plasma are O_2, N_2 and Ar. However, O_2 will oxidize Cu instead of cleaning or passivated it. Hence, only N_2 and Ar plasma will be evaluated in this dissertation.

Firstly, Ar plasma and Ar + N_2 plasma were investigated for their effect on Cu surface elemental composition as Ar + N_2 plasma may produce Cu_xN_y compounds. Effects on Cu surface elemental composition from variation of duration and gas composition of Ar + N_2 plasma were also investigated. It was found that the plasma pretreatment reduces the copper oxides and produced copper nitride compound when N_2 was introduced in the plasma. Water contact angle and surface roughness of treated surface were measured. Plasma pretreatments were able to reduce both water contact angle and surface roughness of the as deposited Cu. Lastly, blanket wafer Cu-Cu fusion bonding was demonstrated with both Ar plasma and Ar + N_2 plasma. Transmission electron microscopy and electron energy loss spectroscopy (TEM/EELS) were performed on the bonded samples at their bonding interface before and after temperature cycling test to study the microstructures.

3.2 Experimental Preparation Procedures

All samples in this chapter were fabricated from single side polished, P-

type, 150 mm diameter, 675 +/- 25 µm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm. Electron-beam physical vapor deposition (EB–PVD) were used to deposit 10 nm of Ti (barrier and adhesion layer) followed by 100 nm of Cu. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. The deposited layers are shown in Figure 21. The wafer was spin coated with S1813 resist and soft baked at 100 °C to protect the surface from contamination by the dicing process. After resist coating, the wafer was diced into 10 mm by 10 mm dies. The dies were cleaned with acetone followed by IPA and DI water before the plasma pre-treatment.

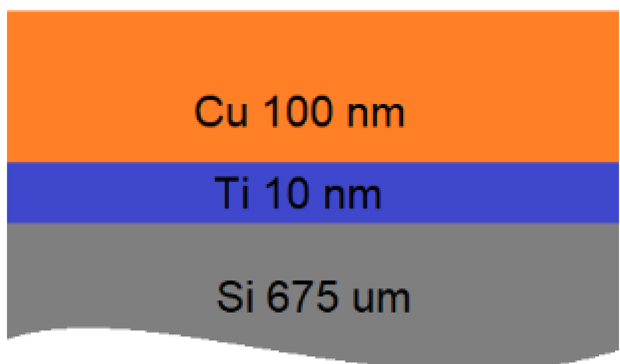

Figure 21: Layers of metals deposited on Si wafer (exaggerated for clarity)

Four types of plasma pre-treatment were evaluated, one with Ar plasma only and three with Ar and Ar + N_2 plasma. Different durations and Ar to N_2 ratios were investigated. The plasma pre-treatments parameters are shown in Table 2. All plasma pre-treatments consist of two steps. Step 1 is similar for all plasma pre-treatment which consist of a cleaning step by Ar plasma only. Step 2 is the passivation step with Ar + N_2 plasma. For the plasma pre-treatment with Ar plasma only, the passivation step is performed with Ar only plasma instead. Plasma pretreatment with passivation are named as Passivation Type 1, 2 and 3 in this dissertation for easy reference. Step 2 in Passivation Type 1 have the same duration of 10 s as the plasma pre-treatment without passivation. Type 1 has an Ar gas flow of 50 cm^3/min and N_2 gas flow of 100 cm^3/min. Passivation Type 2 increased step 2 duration from 10 to 50 s. Passivation Type 3 have the same duration with 50 s, however N_2 gas flow was increased to 140 cm^3/min while Ar gas flow was decreased to 10 cm^3/min.

	No Passivation	**Passivation Type 1**	**Passivation Type 2**	**Passivation Type 3**
Step 1	Cleaning			
Time (s)	7			
Pressure (Pa)	20			
RF Power (W)	200			
Ar (cm^3/min)	100			
Step 2	Dummy	Passivation Type 1	Passivation Type 2	Passivation Type 3
Time (s)	10	10	50	50
Pressure (Pa)	20	20	20	20
RF Power (W)	200	200	200	200
Ar (cm^3/min)	150	50	50	10
N_2 (cm^3/min)	0	100	100	140

Table 2: Plasma treatment parameters for evaluation of passivation plasma treatment

3.3 Study on Plasma Pre-treatment Effects on Cu Surface Elemental Composition

X-ray photoelectron spectroscopy (XPS) was performed on all four samples to identify elemental composition of the Cu surface after the plasma pre-treatment. Wide scan results from the XPS is shown in Figure 22. Figure 23, Figure 25, Figure 28 and Figure 29 shows the XPS scan at Cu 2p, O1s, N1s and C1s respectively. All XPS results were shifted using adventitious carbon as reference (energy shift of +2.4 eV to 282.8 eV).

From the O1s scan in Figure 25, two distinct peaks are observed from the no passivation plasma pre-treatment sample and the lower energy peak at 530.2 eV decreases in counts from Type 1 to Type 3. The deconvolution of the O1s scan for Type 2 and Type 3 plasma are shown in Figure 26 and Figure 27. The peak at 530.2 eV is attributed to Cu (I) oxide [60] [61]. The higher energy peak at 531.5 eV can be associated with copper carbonate [62], organic C [63],

or copper hydroxide [64]. The higher energy peak can be correlated with the results in the C1s scan shown in Figure 29. Two peaks are observed for all samples. A high peak is associated with adventitious carbon at 284.8 eV (reference) and a lower peak with ~289 eV is observed. The 289 eV is associated with copper carbonate. While in Figure 24, the lower peak at Cu $2p_{3/2}$ have a binding energy of approximately 934.7 eV which is also associated with $Cu(OH)_2$ stabilized by $CuCO_3$ [65]. Therefore, the O1s peak at 531.5 eV is attributed to $Cu(OH)_2/CuCO_3$.

From the N1s scan in Figure 28, no peak is observed from the plasma pre-treated samples with no passivation while single or multiple peaks are observed for the plasma treatment with passivation. This shows that the Ar + N_2 plasma has effect on the Cu surface in terms of elemental composition with the addition of N_2 or N compounds. It can also be observed that the lower peak at higher binding energy (403.7 eV) decreases from Type 1 to Type 3. The higher peak at lower binding energy (397.6 eV) is observed for all plasma with passivation pre-treated samples. From literature, the higher peak with lower energy is attributed to the formation of Cu_3N [66] [67] while the lower peak at higher energy is attributed to chemisorbed nitrogen [12].

Table 1 shows the summary of the composition of the surface with different plasma process. $Cu(OH)_2/CuCO_3$ and Cu (I) oxide are present on all samples with Cu (I) oxide decreasing with increasingly N_2 flowrate and duration. Cu_3N and chemisorbed nitrogen are only found in samples with N_2 plasma. Chemisorbed nitrogen decreased with increasingly N_2 flowrate and duration. Hence to get lower Cu (I) oxide and chemisorbed nitrogen, higher N_2 flowrate and longer passivation plasma duration is required.

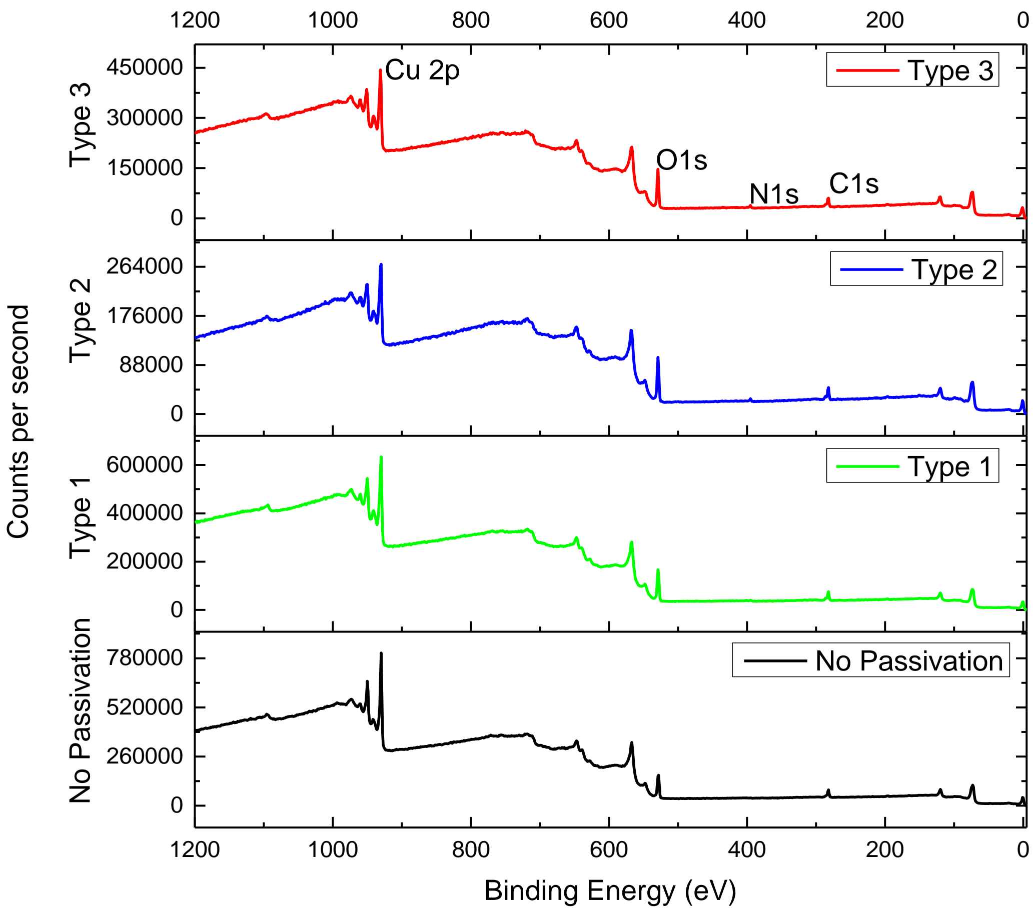

Figure 22: XPS wide scan for all samples with Cu 2p, O1s, N1s, C1s labeled

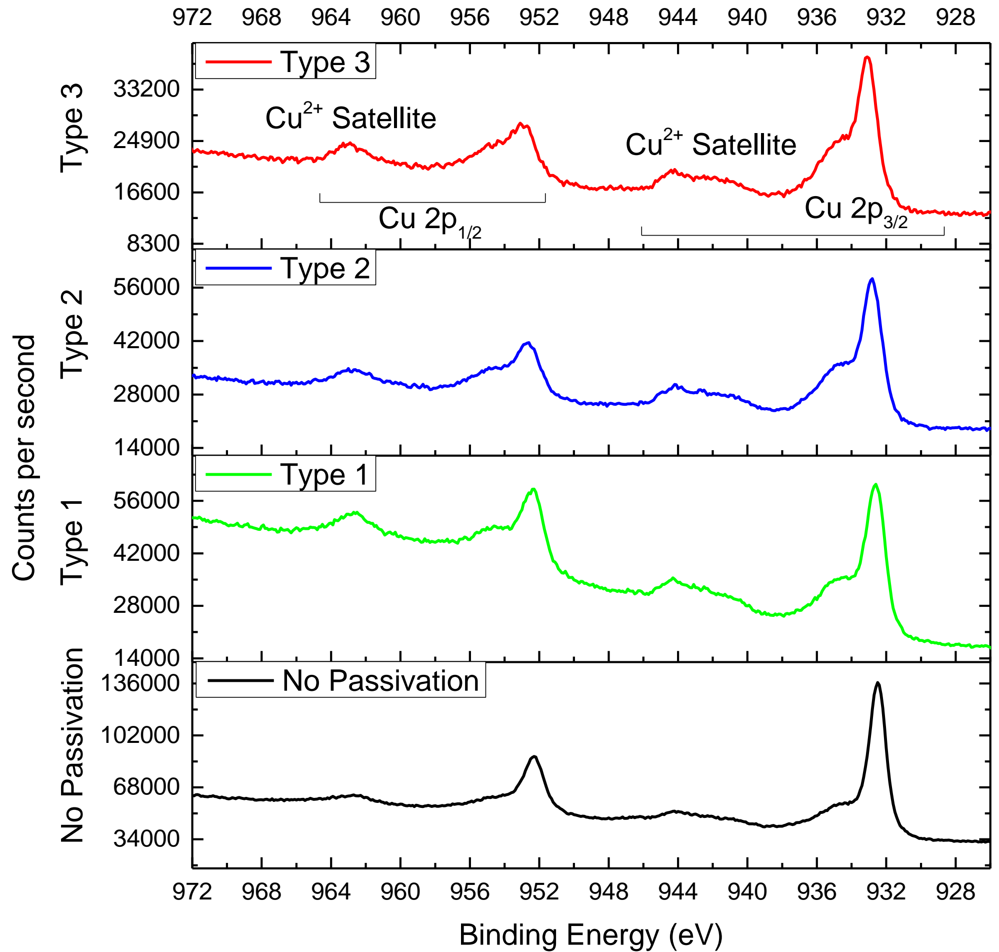

Figure 23: XPS scan for all samples at Cu 2p

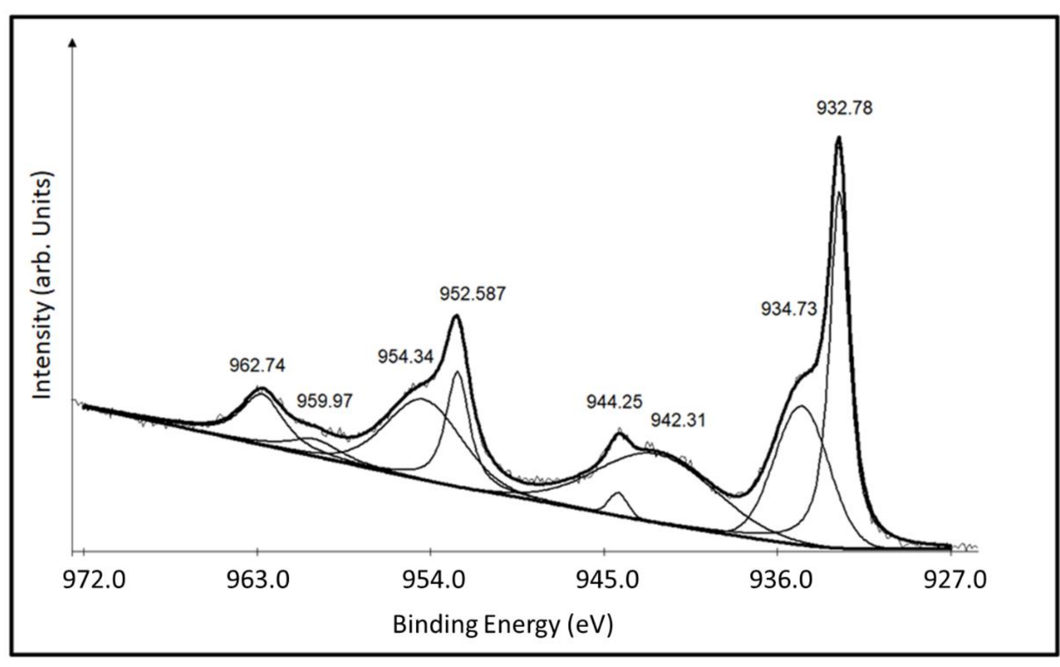

Figure 24: Deconvolution of Cu2p scan for Type 2 with peaks labeled

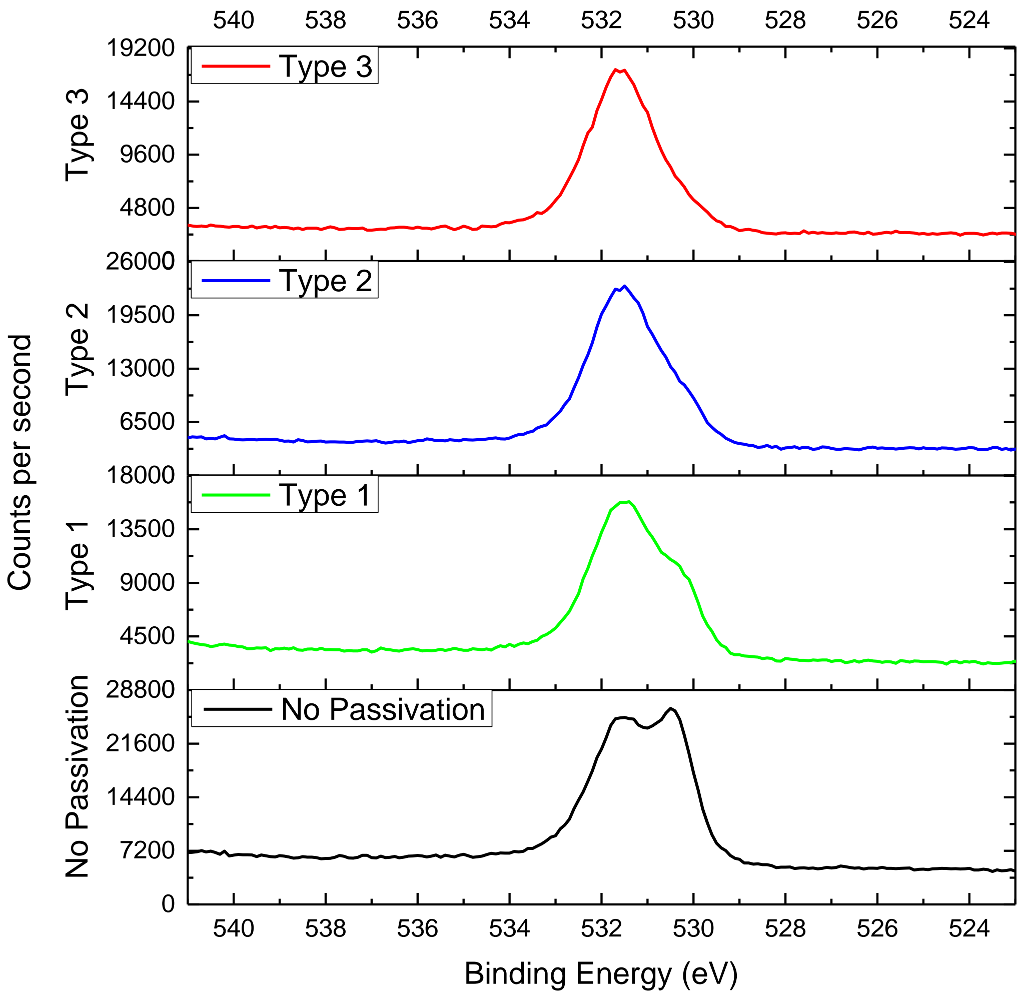

Figure 25: XPS scan for all samples at O1s. 2 peaks are observed for the 'No Passivation' sample. The lower energy peak is observed to reduce from 'Type 1 to Type 3'

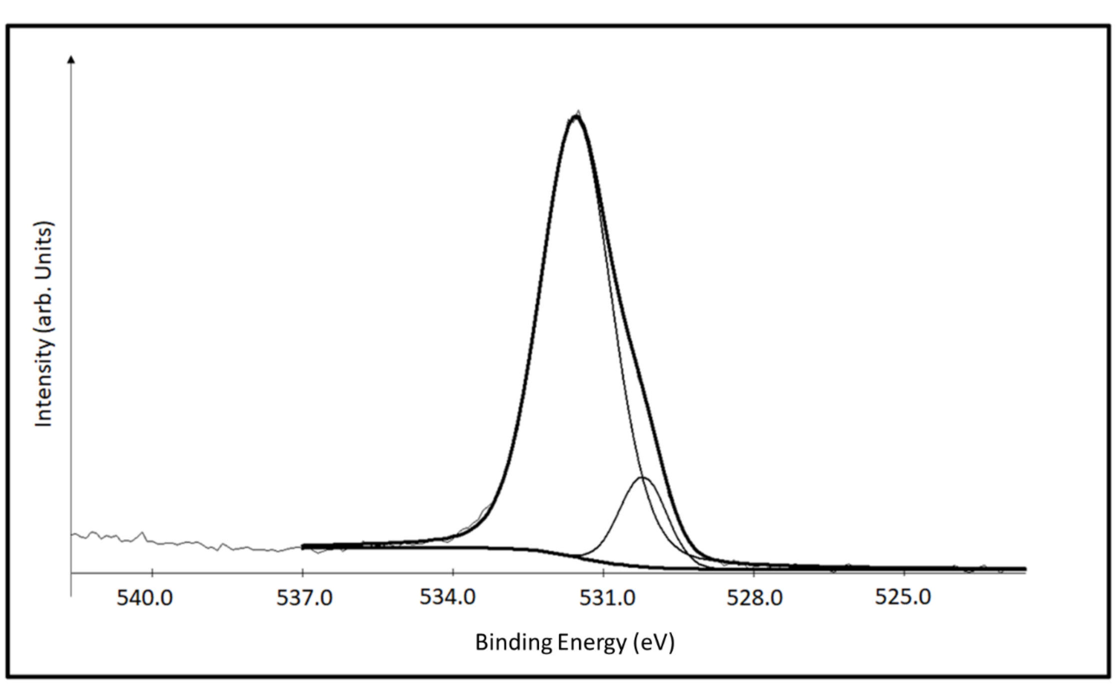

Figure 26: Deconvolution of O1s scan for Type 2 with peaks at 531.5 ($Cu(OH)_2/CuCO_3$) and 530.2 eV (Cu (I) oxide)

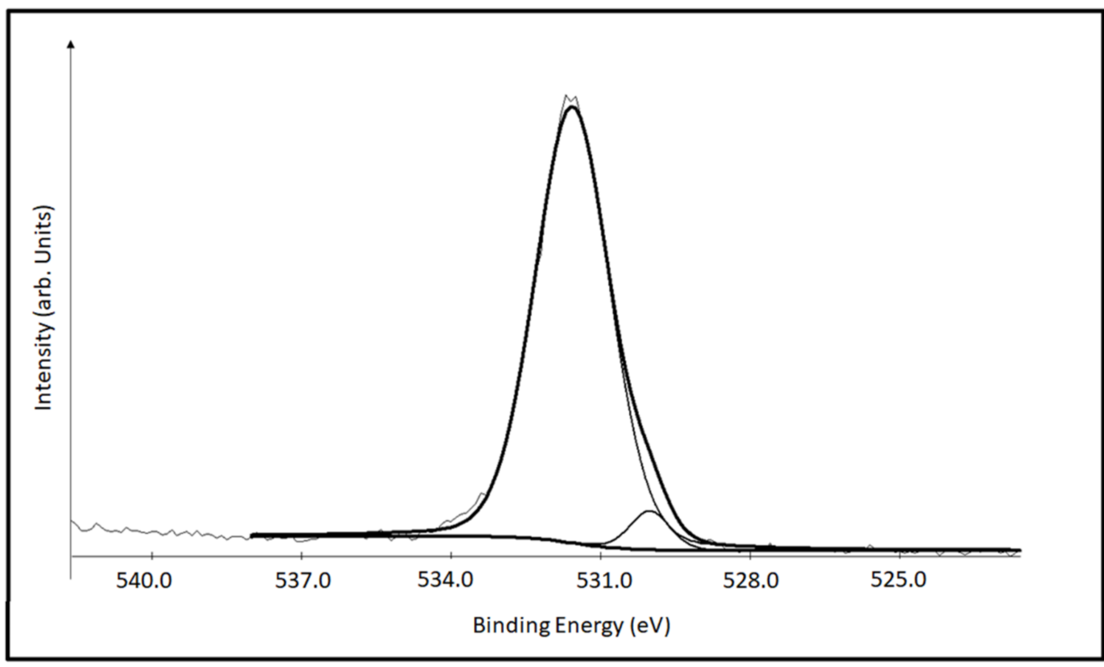

Figure 27: Deconvolution of O1s scan for Type 3 with peaks at 531.5 ($Cu(OH)_2/CuCO_3$) and 530.2 eV (Cu (I) oxide)

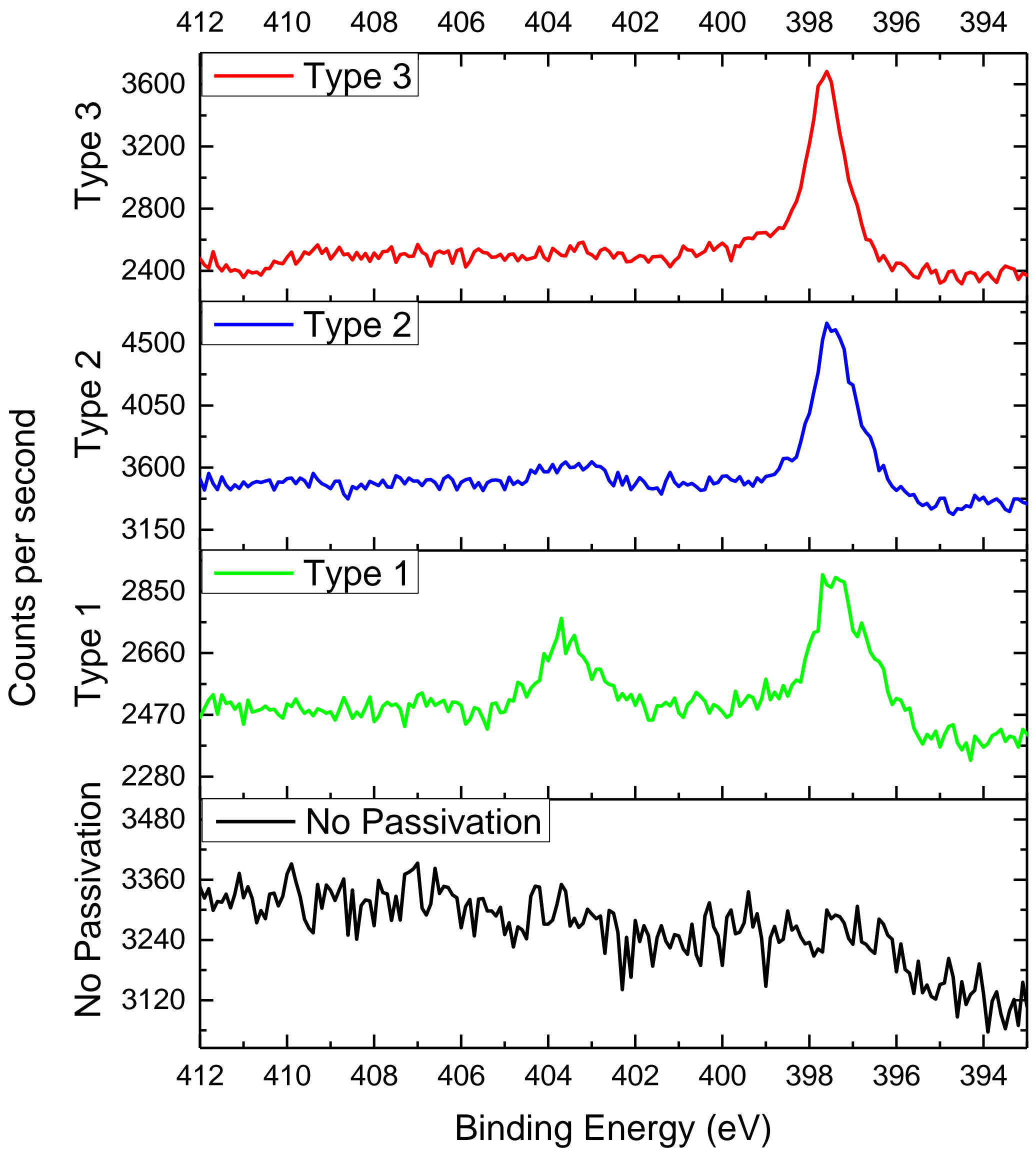

Figure 28: XPS scan for all samples at N1s. 'Type 1' to 'Type 3' shows two peaks, 397.6 eV (Cu_3N) and 403.7 eV (chemisorbed nitrogen)

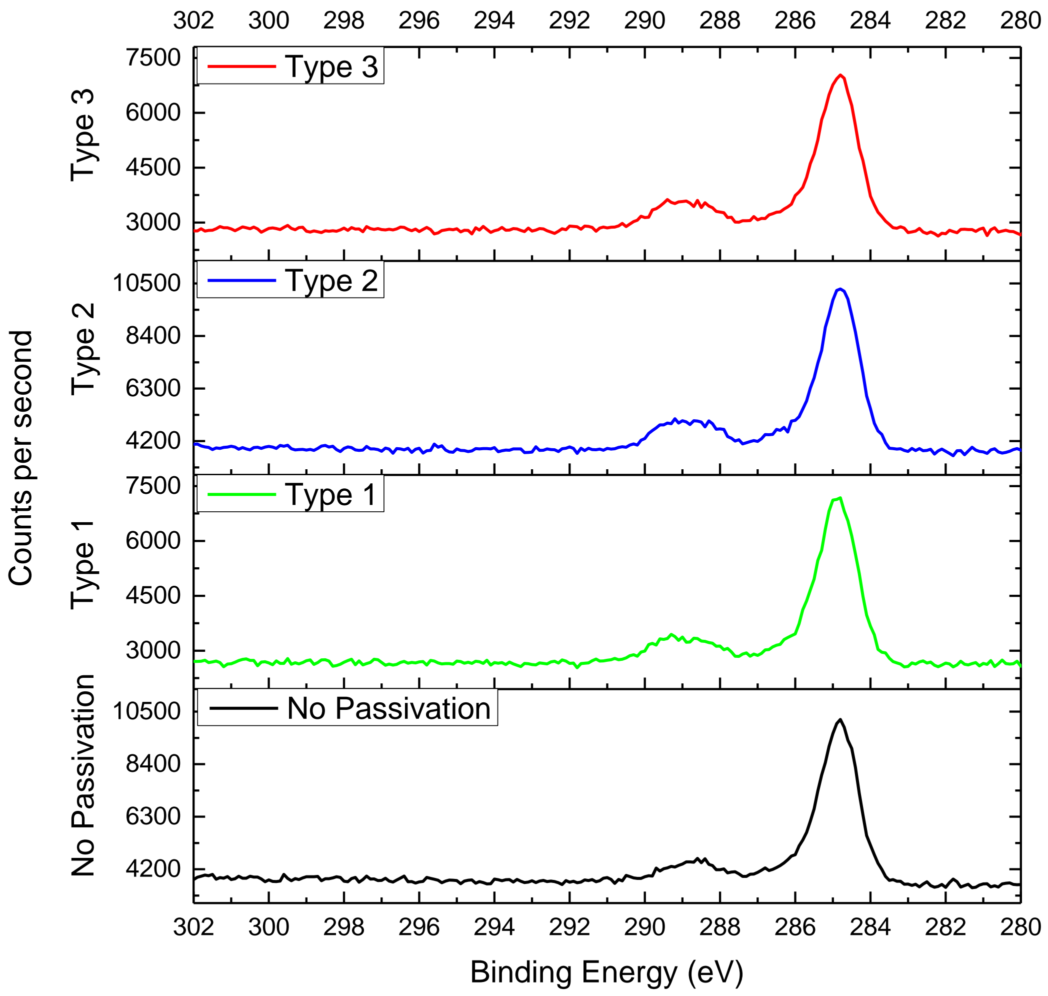

Figure 29: XPS scan for all samples at C1s show 2 peaks, 284.8 eV (adventitious carbon) and 289 eV ($Cu(OH)_2/CuCO_3$)

Composition	Dummy	Passivation Type 1	Passivation Type 2	Passivation Type 3
Cu (I) oxide	Highest	Decreasing		Lowest
$Cu(OH)_2/CuCO_3$	Present	Present	Present	Present
Cu_3N	Not Present	Present	Present	Present
Chemisorbed Nitrogen	Not Present	Highest	Decreasing	Lowest

Table 3: Summary of composition of surface with different plasma treatment

3.4 Study on Plasma Pre-Treatment Effects on Water Contact Angle

Solid surfaces with high surface free energy will be able to adhere to each other strongly to achieve a state of free energy that is as low as possible (reduction of surface area will reduce total surface energy). Since solid surfaces with high surface free energy will have high wettability, low water contact angle can be used to indicate high surface free energy. Water contact angle on the surface of pre-treated samples were measured with a contact angle goniometer and recorded with time. Type 1 and Type 2 plasma pre-treated samples were evaluated, and results are shown in Figure 30. Water contact angles for sample without pre-treatment were also measured in 1 h interval as there were little change in contact angle with time. Type 1 was able to achieve less than 4 ° right after the plasma treatment. However, after 5 min, the contact angle started to increase and plateaued near the end of 1 h. For the Type 2 plasma pre-treatment, the water contact angle was 13 ° right after the treatment. The pre-treatment did not turn the surface hydrophilic even though there was less oxidation on the sample as observed by XPS. Since low contact angle is usually an indicator of high surface free energy of the bonding surface resulting in good fusion bonding capability, plasma pretreatment Type 1 was selected with low water contact angle compromising for passivation ability.

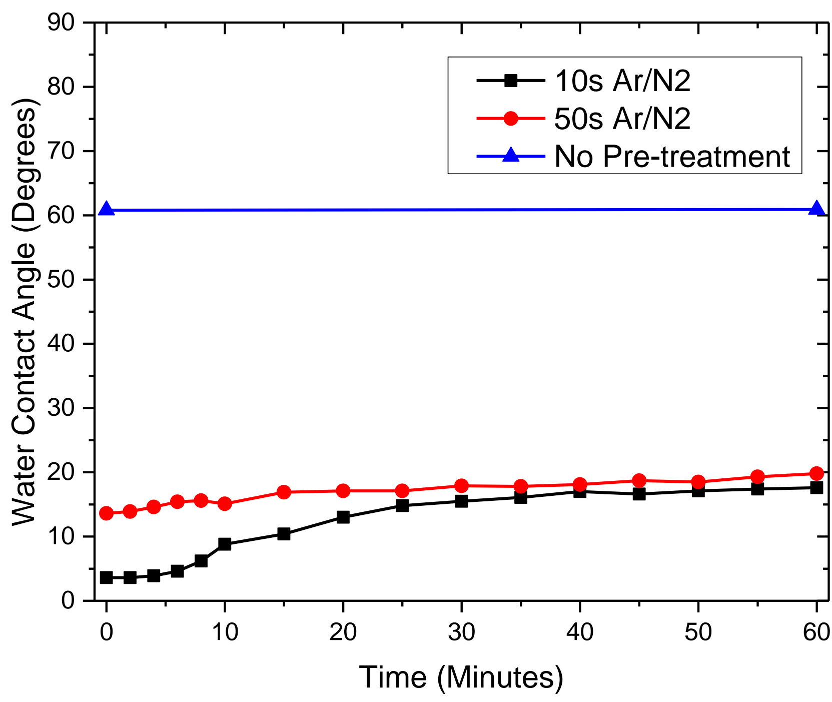

Figure 30: One-hour water contact angle after plasma pre-treatment

3.5 Study on Plasma Pre-Treatment Effect on Surface Roughness

Low surface roughness is important in achieving good bonding interface for Cu-Cu fusion bonding. Typically, fusion bonding requires low surface roughness of less than 1 nm [68]. Atomic force microscopy (AFM) was used to characterize the surface roughness of the Type 1 and Type 2 pre-treated samples. AFM scan of 5 μm by 5 μm for the as-deposited sample was shown in Figure 31 while the AFM scans for the Type 1 and Type 2 pre-treated samples are shown in Figure 32 and Figure 33 respectively. The root mean square (RMS) roughness is 3.15 nm before and 0.774 nm after the Type 1 plasma pre-treatment. Type 2 plasma pre-treatment reduced the roughness to 1.74 nm which is higher than Type 1 plasma pre-treatment. This shows that the plasma pre-treatments have reduced the surface roughness which will be beneficial to the Cu-Cu fusion bonding and Type 1 plasma has the most effect.

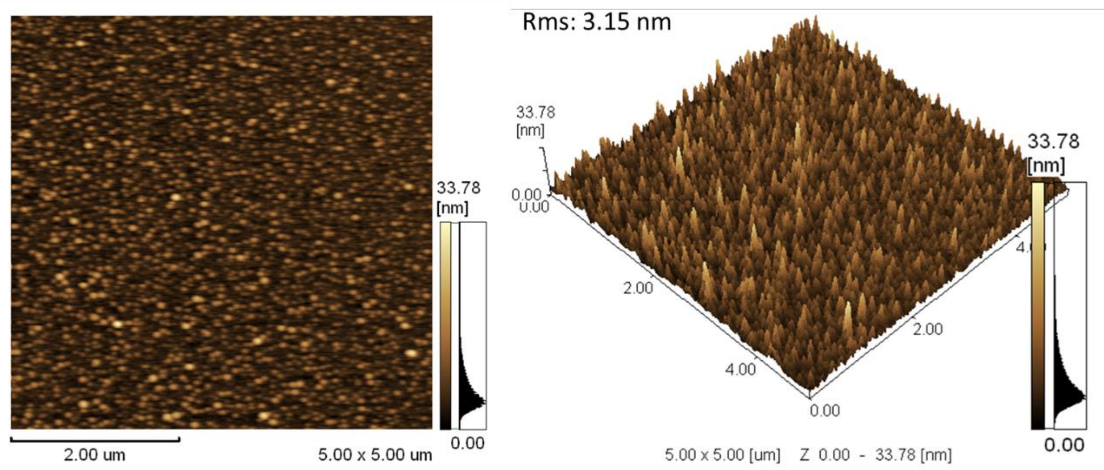

Figure 31: Image of AFM scan and roughness of as-deposited Cu (RMS of 3.15 nm)

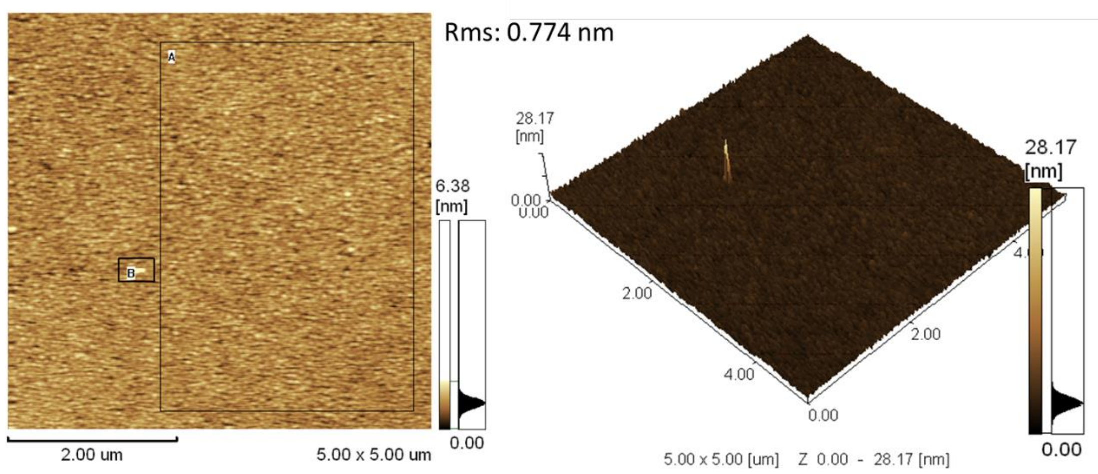

Figure 32: Image of AFM scan and roughness of Cu after plasma pre-treatment Type 1 (RMS of 0.77 nm)

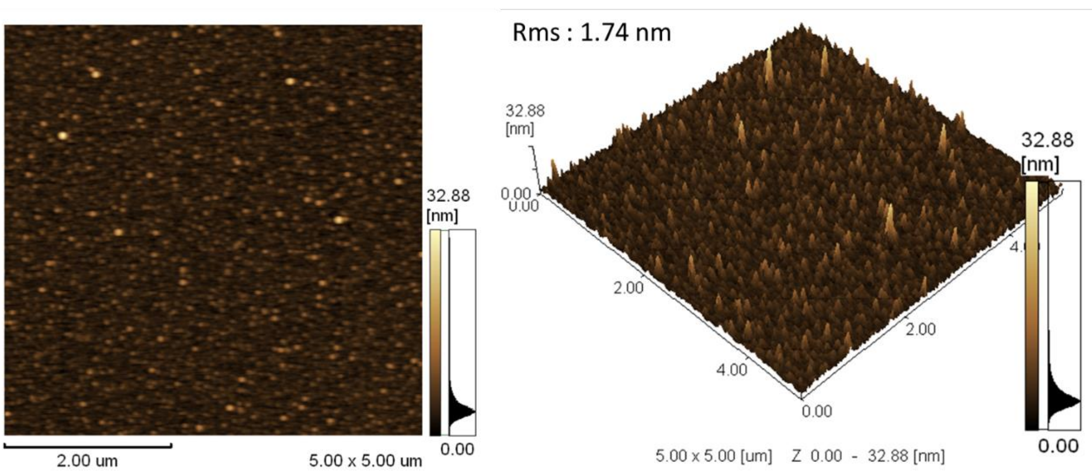

Figure 33: Image of AFM scan and roughness of Cu after plasma pre-treatment Type 2 (RMS of 1.74 nm)

3.6 Study on Plasma Pre-Treatment on Cu-Cu Fusion Bonding

For the bonding evaluation in this section, blanket wafer to wafer Cu-Cu fusion bonding were performed and the bonding interface were investigated with TEM/EELS. P-type Si <100> wafers of 150 mm in diameter, 675 +/- 25 μm thickness, bow/warp of less than 30 μm and resistivity range of between 0 to 100 Ω.cm were firstly EB–PVD deposited with 10 nm of Ti (barrier and adhesion layer) followed by 100 nm of Cu. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. Plasma pre-treatment without passivation and plasma pre-treatment with passivation Type 1 were used for Cu-Cu bonding as Type 1 plasma achieved high surface free energy required for the fusion bonding. After the plasma pre-treatment, each pair of wafers were placed face to face in a mask aligner with double aligning capabilities. The wafers were held in contact using vacuum contact mode 1 min. During the vacuum contact mode, the wafers were held together, and air was pumped out between the wafer at -70 KPa gauge pressure. The pressure difference between the atmosphere and between the wafers forces the bonding surface together. The wafers will be bonded together by van der Waals force from the vacuum contact process.

The bonded samples (both without passivation and Type 1 samples) were batch annealed together at 300°C (safe for CMOS device) for 1 h in a furnace with normal air environment. Since only very little amount of Cu (at the edges of the wafers) were exposed to the surrounding environment, inert environment was not required in the annealing furnace. Figure 34 shows the confocal scanning acoustic microscopy (CSAM) image of bonded wafer with Type 1 plasma pre-treatment. The center of the wafer shown as light grey are bonded while the black spots are voids. Darker grey surrounding the bonded area and the voids are water that have entered the gap between the unbonded area.

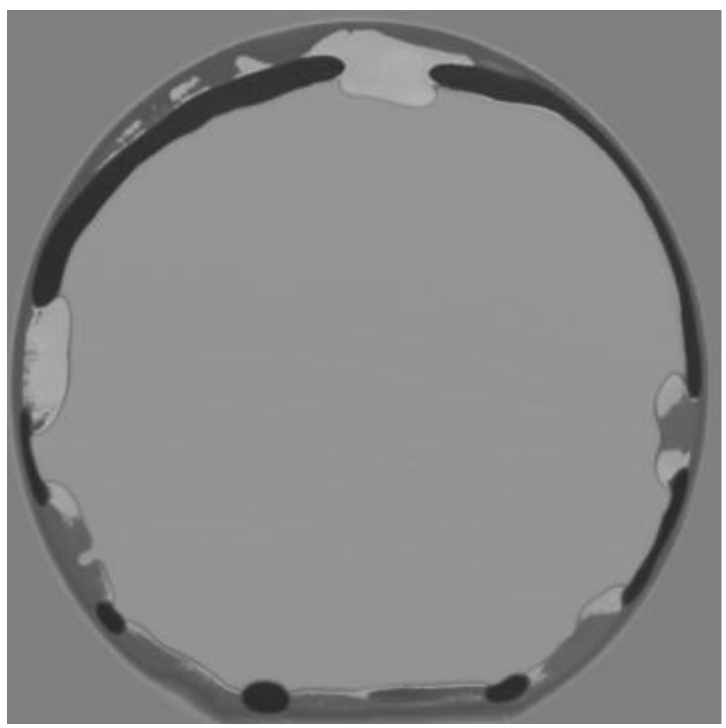

Figure 34: CSAM image of wafer bonded with Type 1 plasma pre-treatment, middle light grey areas are bonded while black areas are voids (air)

The bonded wafers were diced into 10 mm by 10 mm samples and the bonding interface microstructure and elemental composition were investigated by transmission electron microscopy and electron energy loss spectroscopy (TEM/EELS). Temperature cycling test (TCT) with 1000 cycles from -40 to 125 ^{0}C was performed on the diced samples cycles according to JEDEC standard, JESD22-A104 using test condition G [69]. This is to demonstrate the advantages of same metal bonds over intermetallic bonds which may produce Kirkendall voids after TCT. The bonding interface microstructure and elemental composition were observed and compared.

Figure 35 and Figure 36 shows the TEM/EELS images before and after 1000 cycles TCT for bonded sample using plasma pre-treatment without passivation and bonded sample using plasma pre-treatment with passivation Type 1 respectively. Both type of pre-treatment bonded the sample well with no delamination observed. No oxygen and nitrogen was detected in the EELS mapping before and after TCT for both samples showing that the Cu_3N compound have decomposed at the annealing temperature [70] [71] [72]. However, the original bonding interface remained a straight line for the sample

bonded with pre-treatment without passivation even after the TCT. Bonding interface for the sample bonded with pre-treatment with passivation were observed to be in zig-zag pattern showing more changes in grain boundaries and potentially better bond quality. This is likely due to lower copper oxides at the bonding interface allowing greater diffusion of Cu shifting the grain boundaries.

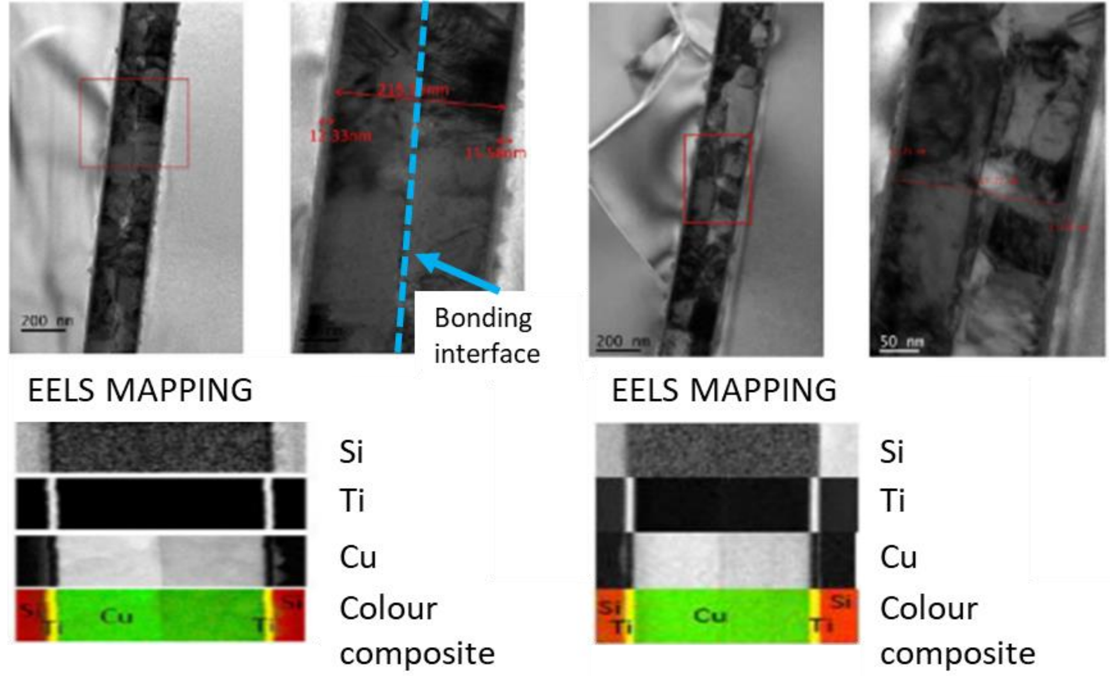

Figure 35: TEM image and EELS mapping of bonding interface of 'no passivation' sample before and after 1000 TCT cycles. In the EELS mapping, white represents presence of element stated on the right and black represents the lack of the element. Bonding interface is outlined with blue dashed line.

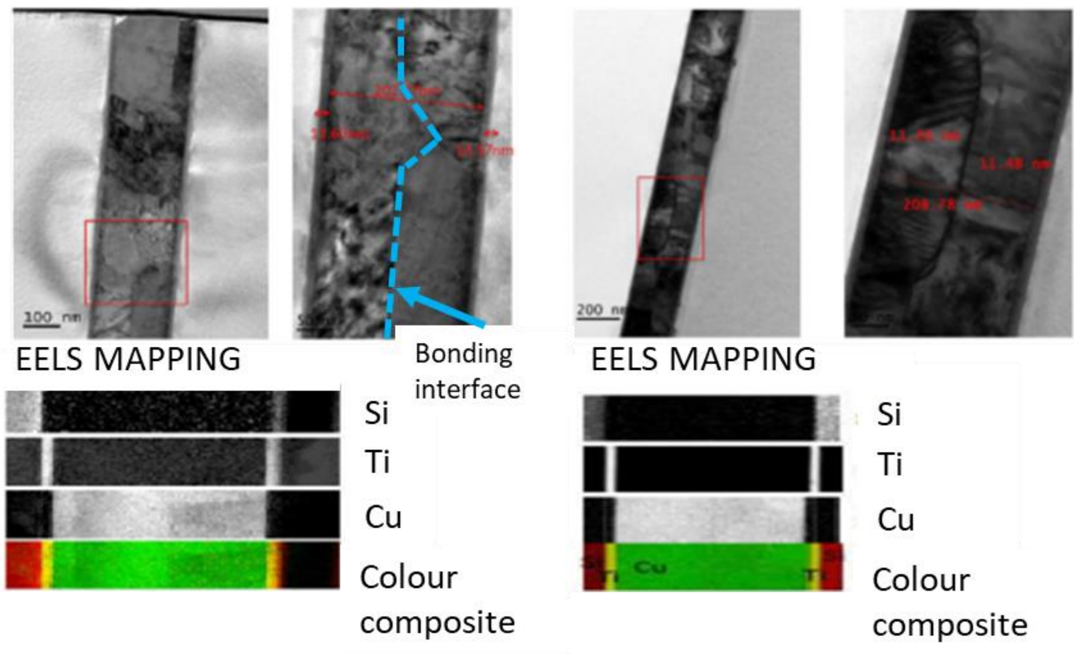

Figure 36: TEM image and EELS mapping of bonding interface of 'with passivation' sample before and after 1000 TCT cycles. Bonding interface is outlined with blue dashed line.

Auger electron spectroscopy (AES) depth profiling were also performed to verify the decomposition of the Cu_3N compound. Type 3 plasma pre-treatment was performed on a sample as it produces the highest Cu_3N compound observed in the XPS. AES depth profiling was performed before and after annealing of the sample in vacuum for 2 h at 300 °C. The results of the elemental depth profiling before annealing (solid lines) and after annealing (dashed lines) are shown in Figure 37. Although the concentration of N (red line) at the surface is low before annealing, there is a significant decrease in the result after annealing to conclude the Cu_3N has indeed been decomposed. O has also decreased after annealing resulting in higher concentration of Cu near the surface after annealing.

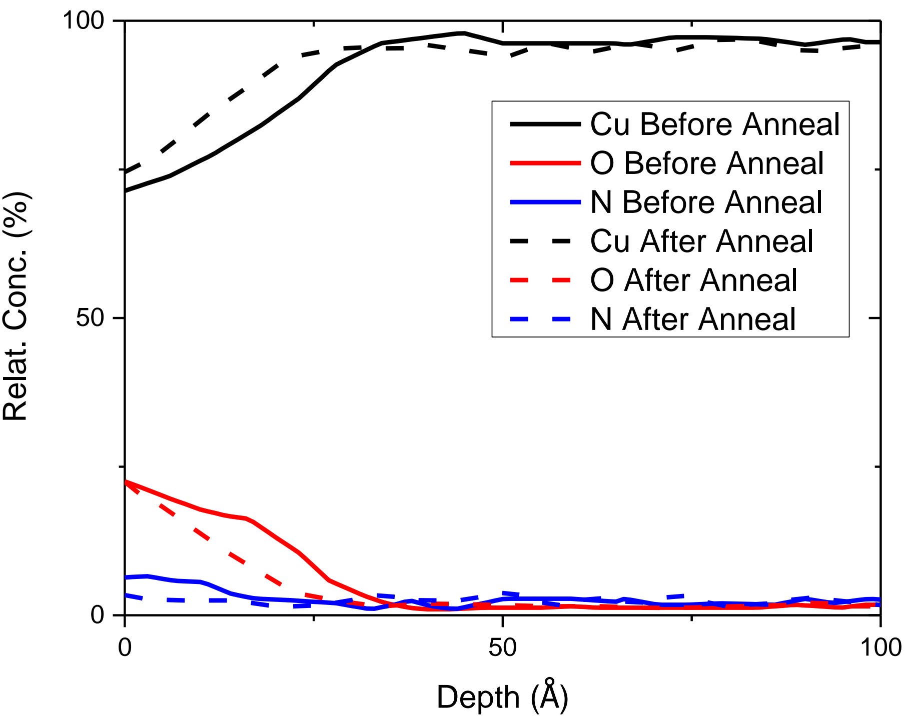

Figure 37: AES depth profiling of Type 3 pre-treated sample before annealing (solid lines) and after annealing (dashed lines). N (blue) at the surface decreased after annealing.

3.7 Summary

In this chapter, different variation of duration and gas composition of Ar + N_2 plasma were investigated for their effect on Cu surface elemental composition. The inclusion of N_2 gas in the plasma for passivation was observed to form Cu_3N compound from the XPS results. The Cu_3N compound increases in concentration as duration of pre-treatment increased, however the increase of ratio of N_2 gas to Ar gas did not produce significant increase in Cu_3N compound. Copper oxides were also observed to decrease with increase with treatment duration.

Water contact angle and surface roughness of treated surface were measured. Unfortunately, Type 2 plasma which have lower copper oxides has higher water contact angle which could result in lower pre-bonding forces. Hence, it was decided that a Type 1 plasma pre-treatment was to be used for the Cu-Cu fusion bonding for the subsequent chapter. AFM showed that Type

1 pre-treatment was able to reduce surface roughness of as-deposited Cu from RMS roughness of 3.147 nm to 0.774 nm. However, Type 2 have higher RMS roughness compared to Type 1 at 1.74nm. This is likely due to long duration of Ar ion bombarding the Cu surface damaging the surface and increasing the roughness.

Hence it can be concluded that the plasma pretreatment reduces the copper oxides on the bonding surface which will improve the bonded interface and reduces the roughness and water contact angle allowing the Cu surface to be fusion bonded.

Lastly, blanket wafer Cu-Cu fusion bonding was demonstrated with both pre-treatment without passivation and pre-treatment type 1. Microstructure studies were performed on the bonded samples at their bonding interface before and after temperature cycling test. No delamination or oxidation were observed of all samples. Zig-zag bonding interface was observed for sample with pre-treatment type 1 before and after the TCT which potentially have better bond properties compared to the sample bonded with pre-treatment without passivation.

Chapter 4 **Cu-Cu Fusion Bonding Characterization**

4.1 Introduction

In this chapter, with different plasma pre-treatment effects in bond strength were investigated. Shear strength test was used for the bond strength evaluation. No substantial difference in bond strength were observed between plasma with passivation and plasma without passivation. However, exposed Cu surface was found to have more oxidation in the samples pre-treated by plasma without passivation.

Bonding and annealing temperature effects in bond strength and hermetic sealing capability were also investigated. He leak test and gross leak test (bubble test) were performed to evaluate hermetic sealing capability. Samples bonded and annealed at 250 °C performed the best in the shear strength test and He leak test. Lastly electrical characterizations were performed on Cu-Cu fusion bonded samples to test the bonding uniformity of the dies.

4.2 Study on Effects of Plasma Pretreatment on Bond Strength

In this section, shear strength tests were used to evaluate the mechanical strength of the Cu-Cu bond with different variation of plasma pre-treatment. High mechanical strength is required for the Cu-Cu bond as it is the holding the top and bottom die together in 3D integration. Die to die bonding was used for the fabrication of the shear strength test samples to obtain a larger bottom die. Adhesive were used to mount the samples onto glass slides for shear testing. Since the bond strength of the adhesive used was weaker than the Cu-Cu fusion bond, the bottom dies need to be much bigger than the bonding area to ensure the sample failed before the adhesive. Two different plasma pre-treatments (with and without passivation) were evaluated for the shear strength of the bonded samples.

4.2.1 Shear Strength Test Sample Fabrication (Effects of Plasma Pretreatment)

Single side polished, P-type, 150 mm diameter, 675 +/- 25 µm thick, Si

<100> wafers with resistivity of 0 to 100 Ω.cm were used. The wafer was patterned by lithography and etched by deep reactive-ion etching (DRIE) for 8 µm to form 2 mm by 2 mm protruding square features. After DRIE, the remaining resist was stripped and 200 nm of SiO_2 was deposited by TEOS-PECVD. EB–PVD were then used to deposit 10 nm of Ti (barrier and adhesion layer) followed by 100 nm of Cu. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. The wafer was coated with resist again to protect from dicing debris and contaminations. 3 mm by 3 mm samples were diced out with the 2 mm by 2 mm by 8 µm in the center as shown in Figure 38. This formed the top dies for the shear strength test sample. The bottom dies for the shear strength test have the same metal layers as the top die without the DRIE structures as shown in Figure 39. The dies will be place face to face during bonding with the final bonded structure shown in Figure 40.

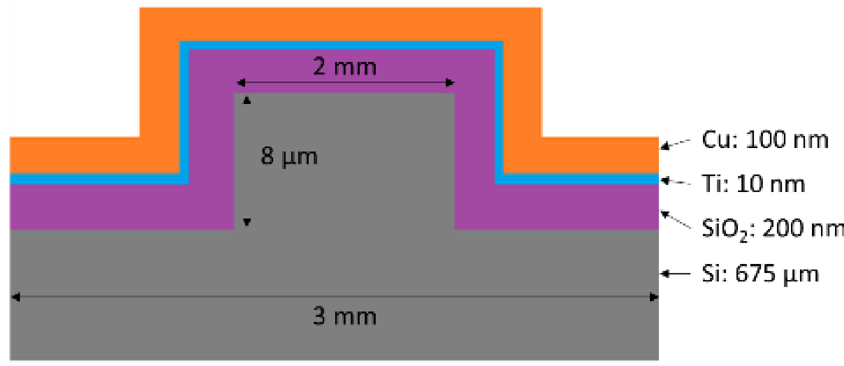

Figure 38: Top die for shear strength test (not drawn to scale)

Figure 39: Bottom die for shear strength test (not drawn to scale)

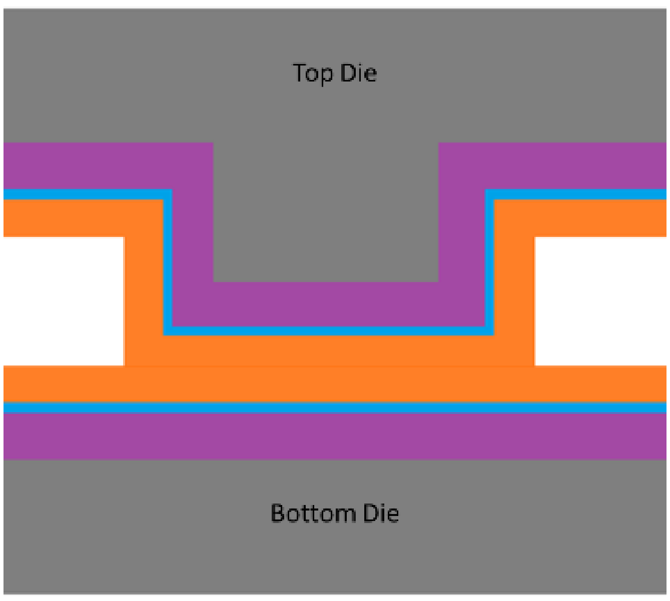

Figure 40: Final bonded structure (not drawn to scale)

4.2.2 Shear Strength Test Sample Bonding (Effects of Plasma Pretreatment)

After dicing, the top and bottom dies were cleaned with acetone followed by IPA and water to remove the protective resist. The clean dies were dried with a N_2 gun and subjected to plasma pre-treatment. Two types of plasma pre-treatment were evaluated, one with passivation from Ar + N_2 plasma and one without passivation. The plasmas parameters are shown in Table 4. Each plasma pre-treatment is separated into two steps. Step 1 is a cleaning step by Ar plasma only and is similar for both type of pre-treatment. Step 2 is the passivation step with Ar + N_2 plasma. For the pre-treatment without passivation, a dummy passivation step is performed with only Ar plasma.

With Passivation		Without Passivation	
Step 1: Cleaning		Step 1: Cleaning	
Time (s)	7	Time (s)	7
Pressure (Pa)	20	Pressure (Pa)	20
RF Power (W)	200	RF Power (W)	200
Ar Gas Flow (cm^3/min)	100	Ar Gas Flow (cm^3/min)	100
Step 2: Passivation		Step 2: Passivation (Dummy)	
Time (s)	10	Time (s)	10
Pressure (Pa)	20	Pressure (Pa)	20
RF Power (W)	200	RF Power (W)	200
Ar Gas Flow (cm^3/min)	50	Ar Gas Flow (cm^3/min)	150
N_2 Gas Flow (cm^3/min)	100	N_2 Gas Flow (cm^3/min)	0

Table 4: Plasma treatment parameters for shear strength test

After the plasma pre-treatment, the dies were transferred to a wafer bonder while exposing to clean room atmosphere environment (room temperature, normal atmosphere pressure and air) within 5 min from the plasma pre-treatment. The dies were manually placed face to face in the bonder. Force was applied to the dies at 125 MPa (500 N for each die with 4 mm^2 bonding area) for 5 min to pre-bond the dies. After the pre-bonding, the top chuck that applied the force was moved away from contact to the dies to ensure no force was applied for the post-bonding annealing process.

The air in the chamber was pump down to 10 Pa and purged with N_2 gas for 3 cycles. Post-bonding annealing was carried out with N_2 at atmospheric pressure in the chamber. The top chuck and bottom were slowly ramped up to 300 °C for post-bonding annealing. N_2 environment was used instead of vacuum to allow convection heating as the top chuck was not in contact with the dies. The dies were kept at 300 °C for 1 h before cooling down to room temperature in bonding chamber. The post-bonding annealing temperature profile is depicted in Figure 41 and the bonding steps are shown in Table 5. Dies without any

plasma pre-treatment were also prepared and bonded with the same process.

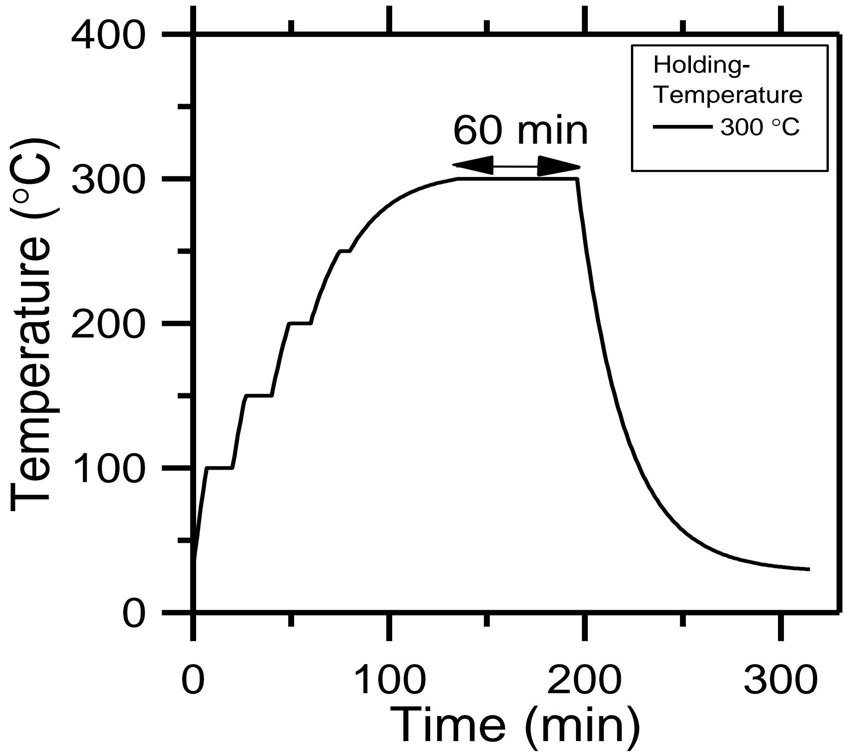

Figure 41: Post-bonding annealing temperature profile

Depiction	Steps
	Plasma pre-treatment: • Ar plasma was applied to both the top and bottom dies to remove surface oxides and contaminates. • Ar+N_2 plasma was applied to one batch of dies for passivation.
	Pre-bonding: • The dies were transferred from the plasma chamber, while exposed to clean room environment, to the bonding chamber. • The dies were placed face to face with 125 MPa of pressure applied for 5 min. • Top chuck was removed from contact after 5 min.
	Post-bonding annealing: • The chamber was pump down to 10 Pa and purged with N_2 for 3 cycles. • Post-bonding annealing was performed in N_2 atmospheric pressure for 1 h at 300 °C. • Bonded samples were cooled down in the chamber before removing.

Table 5: Cu-Cu fusion bonding of shear strength sample

After cooling down to room temperature, the samples were removed from the chamber and prepared for the shear strength test. Discoloration of the bottom die Cu surface was observed on the samples without passivation and

the samples without plasma pretreatment as shown in Figure 42. All the sample without plasma pre-treatment were not bonded successfully showing that the plasma pre-treatment regardless of passivation was essential for Cu-Cu fusion bonding. The discoloration of the Cu was due to oxidation from the post-bonding annealing as the pump-purge cycles was not thorough enough to reduce O_2 significantly. It is hypothesis that the copper nitride compound had slowed down rate of oxidation in a rich N_2 environment.

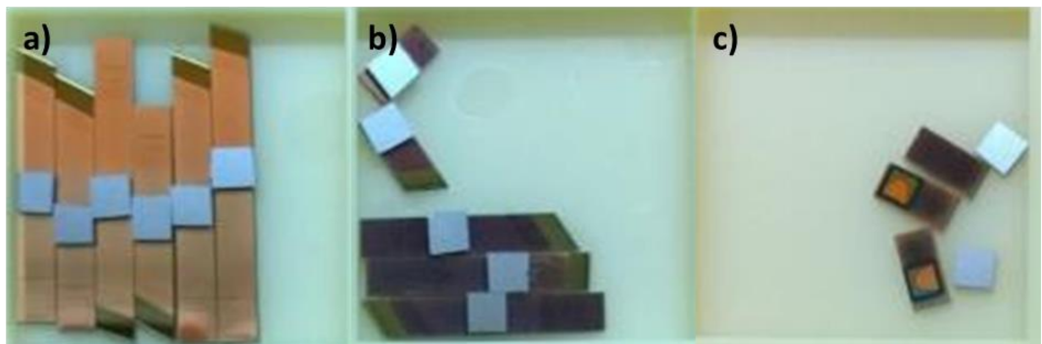

Figure 42: Samples after Cu-Cu fusion bonding process: a) with passivation, b) without passivation and c) with no plasma pre-treatment

To confirm this, plasma pre-treatment effect on mean sheet resistances were investigated. Blanket wafers with similar layer were fabricated (200 nm of SiO_2, 10 nm of Ti and 100 nm of Cu). The wafer was annealed in vacuum at 300°C first to eliminate effects from the Cu grain growth. Mean sheet resistance of the sample, measured by a four-point probe machine, decreased after annealing vacuum from 0.3069 Ω/sq to 0.2911 Ω/sq. After annealing, the wafer was split into quarters and one quarter were treated with pretreatment with and one without passivation. The samples along with an untreated quarter were subjected to the same post-bonding annealing process in the wafer bonder. After the post-bonding annealing, the samples were measure with the four-point probe machine at multiple point with the results shown in Figure 43. Pre-treatment without passivation shows the highest average increased in sheet resistance at 0.097 Ω/sq which agrees with the daisy chain results while without pretreatment and with passivation have an average increased at 0.012 Ω/sq and 0.017 Ω/sq respectively.

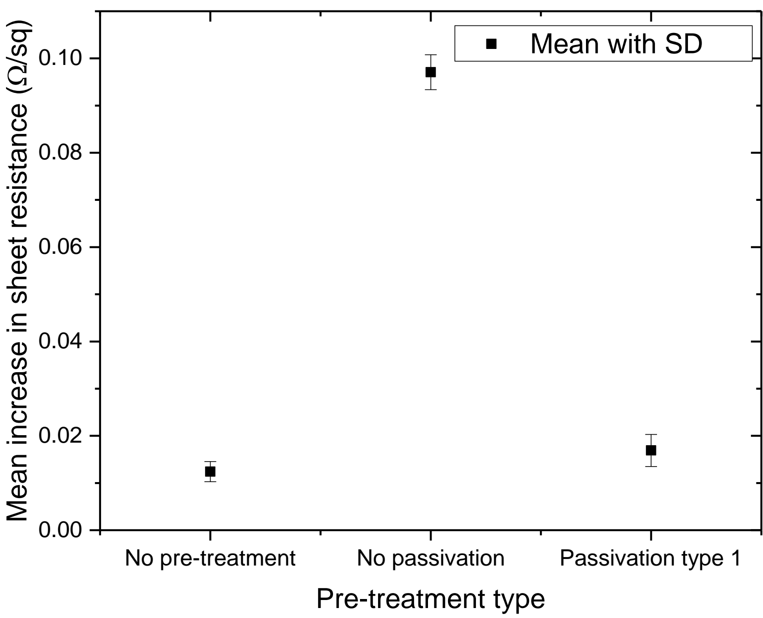

Figure 43: Plasma pre-treatment effect on mean sheet resistance

4.2.3 Shear Strength Test (Effects of Plasma Pretreatment)

To prepare for the shear strength test, each bonded sample (bottom die) were glued to a microscope glass slides with cyanoacrylates. This step was required as the bottom die was too small to be held on by the shear tester. The microscope slide will be held by the shear tester instead. A total of 20 sample were tested, 10 with passivation and 10 without passivation. The shear test was performed as per MIL-STD-883E [73]. The movement speed of contact tool was set at 0.1 mm/min.

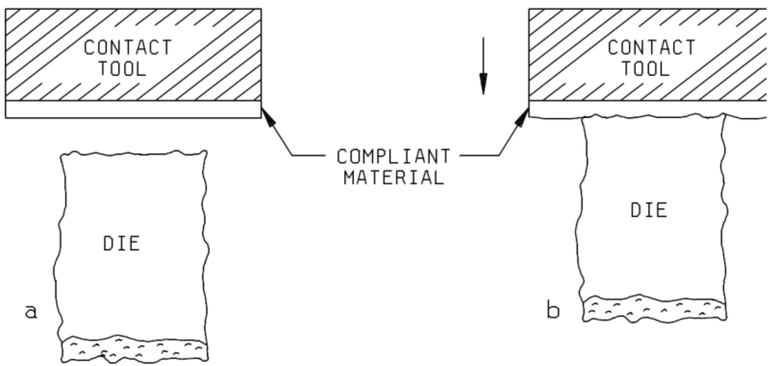

FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

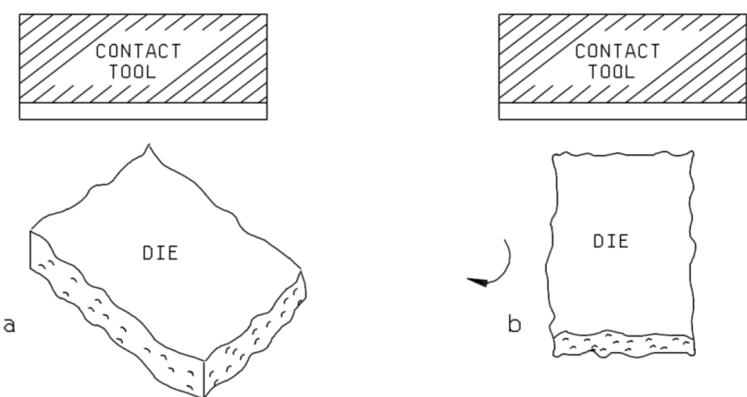

FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

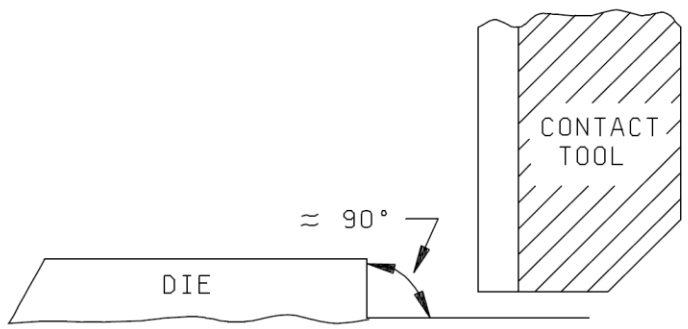

FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle ≈ 90° with the header/substrate.

Figure 44: Shear strength test standards [73]

4.2.4 Shear Strength Test Results and Discussion (Effects of Plasma Pretreatment)

The shear strength test results are shown in Figure 45. The mean shear strength of plasma pre-treatment with passivation is 18.38 MPa while of plasma pre-treatment without passivation has a mean shear strength of 18.85 MPa. No significant difference in shear strength is observed between the two plasma pre-treatment. The standard deviation is observed to be quite large due to partial substrate breakage from the shear test, resulting in lower shear force in the shear test. The partial breakage could be caused by the rough dicing edge on the Si substrate.

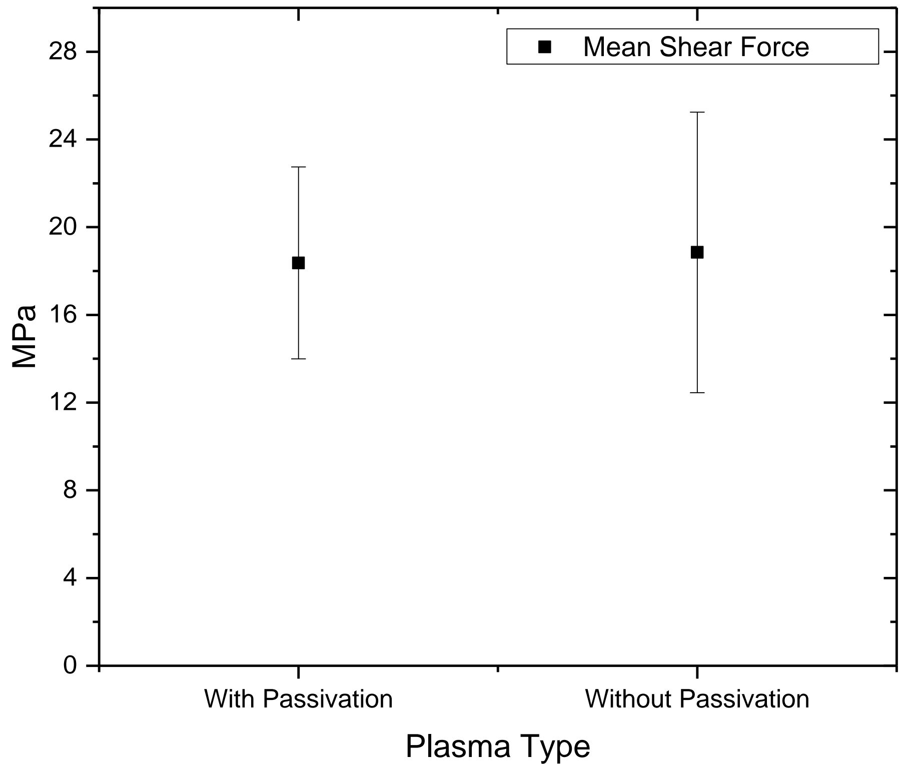

Figure 45: Mean shear strength of bonded samples with standard deviation for different plasma pre-treatment

4.3 Bond Strength Study on Effects of Post-Bonding Annealing Temperature

In this section, different post-bonding annealing temperature were evaluated for plasma pre-treatment with passivation. Only plasma pre-treatment

with passivation was used in this section as samples with either plasma pre-treatments shown comparable shear strength in previous section, however the pre-treatment with passivation have lower oxidation on the exposed Cu surface from the post-bonding annealing process.

4.3.1 Shear Strength Test Die Fabrication (Effects of Post-Bonding Annealing Temperature)

Due to machine availability, the bonding area of the samples had to be reduced as the new shear tester has a load cell with a smaller load capability. Single side polished, P-type, 150 mm diameter, 675 +/- 25 μm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm was used. The wafer was patterned by lithography and etched by deep reactive-ion etching (DRIE) for 8 μm to form 1.5 mm by 1.5 mm protruding square features. After DRIE, the remaining resist was stripped and 200 nm of SiO_2 was deposited by TEOS-PECVD. EB–PVD were then used to deposit 10 nm of Ti (barrier and adhesion layer) followed by 100 nm of Cu. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. The wafer was coated with resist again to protect from dicing debris and contaminations. 3 mm by 3 mm samples was diced out with the 1.5 mm by 1.5 mm by 8 μm in the center. This formed the top dies for the shear strength test sample. The bottom dies for the shear strength test have the same metal layers as the top die without the DRIE structures. The dies were placed face to face during bonding with the final bonded structure shown in Figure 46.

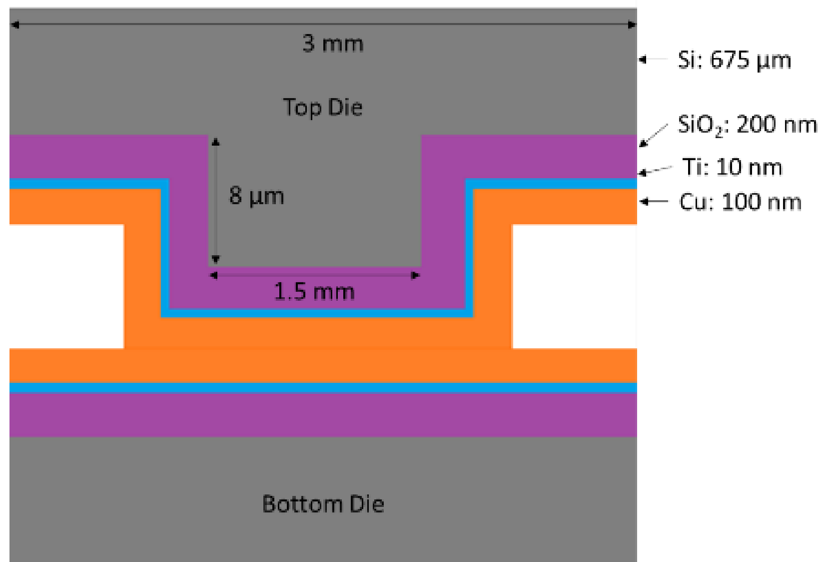

Figure 46: Final bonded structure (not drawn to scale)

4.3.2 Shear Strength Test Sample Bonding (Effects of Post-Bonding Annealing Temperature)

After dicing, the top and bottom dies were cleaned with acetone followed by IPA and water to remove the protective resist. The clean dies were dried with a N_2 gun and subjected to plasma pre-treatment with passivation. Plasma parameters used were the same as the one used in shear strength test sample bonding part 1 as shown in Table 4.

Pre-bonding procedures were the same as shear strength test sample bonding part 1. However, force applied was increased to 166.7 MPa (375 N for each die with 2.25 mm^2 bonding area) for 5 min to pre-bond the dies as there was a decrease in pre-bonding yield when using 125 MPa as before. The decrease in yield is observed with increase in bond surface edges ratio to bonding area, hence larger bonding force was required. It is hypothesized that the van der Waals forces are lower due to lower ratio of bonding area to the edges of the bonding feature.

For this section, different post-bonding annealing temperatures were used. The temperature used were 150, 200, 250 and 300 °C. Total post-bonding annealing duration of 300 °C with 2 h dwelling time, including the time taken for heating and cooling, was used as the base point. Lower temperatures will have longer dwelling durations to ensure overall post-bonding annealing process

duration were similar as the one at 300 °C, as shown in Figure 47.

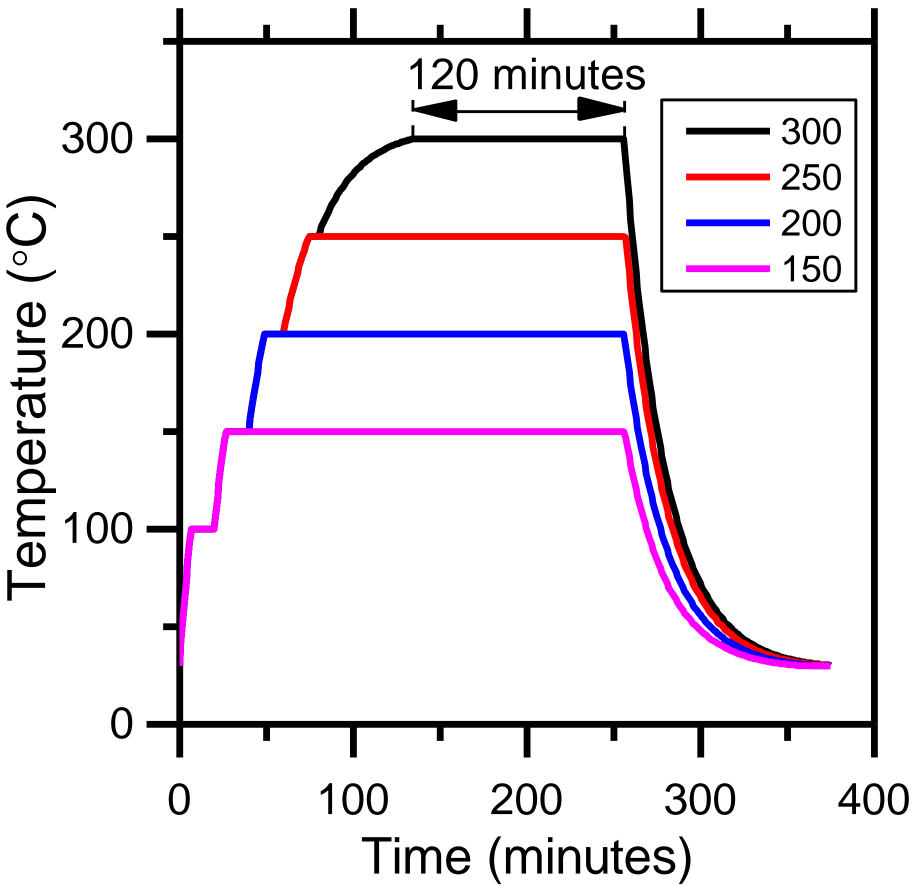

Figure 47: Post-bonding annealing temperature profile

4.3.3 Shear Strength Test (Effects of Post-Bonding Annealing Temperature)

Shear strength test preparation was similar to Shear strength test preparation part 1 as per MIL-STD-883E [73]. 10 samples for each post-bonding annealing temperature were tested. The movement speed of the contact tool was set at 0.1 mm/min.

4.3.4 Shear Strength Test Results and Discussion (Effects of Post-Bonding Annealing Temperature)

The shear strength test results are shown in Figure 48. Highest shear strength was observed at 20.3 MPa for samples annealed at 250 °C and the lowest for samples annealed at 150 °C. With higher temperature at the same annealing duration, more grain boundary diffusion happened at the bonding

interface which introduced greater zig-zag patterns which will increase the shear strength of the bond. However, mean shear force is lower for 300 °C as compared to 250 °C. Observation of the failure point from the shear test shows most of the samples failed at the SiO_2-Ti interface. It is hypothesized that the Ti layer oxidizes with the oxygen from SiO_2 during annealing. With higher post-bonding annealing temperature, higher amount of oxidation occurs at the Ti adhesion layer which results in a lower adhesion strength. This causes 300 °C annealed samples to have lower mean shear strength as compared to 250 °C annealed samples. Shear strength of 300 °C annealed samples are comparable to shear strength test in section 4.2.4 at 18.6 MPa.

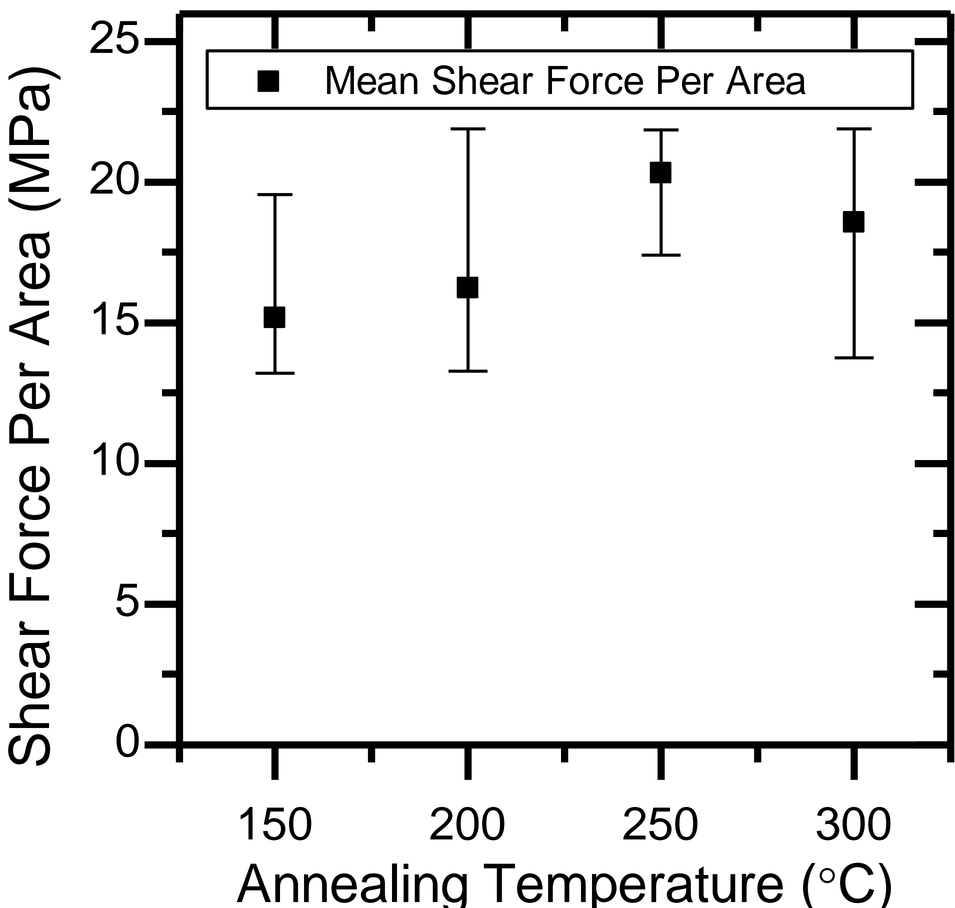

Figure 48: Mean shear strength of bonded samples with standard deviation for different annealing temperature

Simulations (2D) on COMSOL program were performed to determine the highest stressed location in the shear test (due to limitation of the program,

shear strength of the sample and failure location cannot be simulated). SiO_2 with 100 nm thickness was modeled as the substrate due to limitation of the number of mesh computable on the computer. Die sizes were also reduce drastically to reduce amount of mesh. Top die has a length of 200 nm with 100 nm of SiO_2 as the substrate where a distributed force of 3 MPa is acted upon. 10 nm Ti and 100 nm Cu were modeled for the top and bottom die. The bottom SiO_2 has a length of 400 nm and the base is fixed. Dimensions of the model is shown in Figure 49 and the mesh generated is shown in Figure 50.

Von Mises stress results are generated from the simulation with the mesh and shown in colour plot in Figure 51. Figure 52 showing the highly stressed area on the left side using the same colour scale. Both colour plots shows the highly stressed area as red and the low stress areas as blue. From the colour plots, it can be observed that the highest stress area is the edges of the bonding interface with the rest of the model experiencing less than half of the stress. This results shows that the Cu-Cu fusion bonds in demonstrated in the shear test were much stronger than the test results shown as the samples fails at the SiO_2-Ti interface which did not experienced as much stress as the bonding interface.

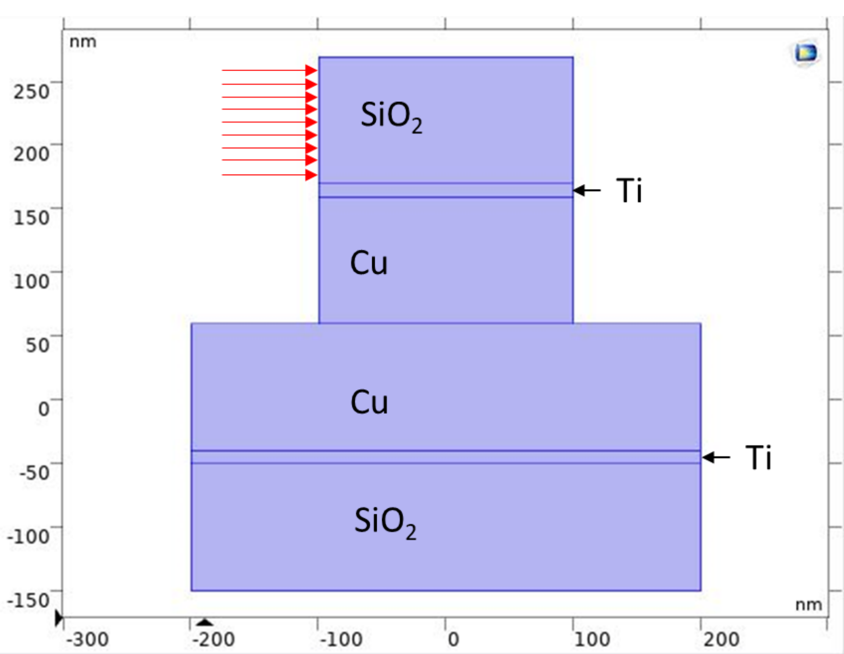

Figure 49: Model for simulation in COMSOL with distributed force applied at the array of red arrows

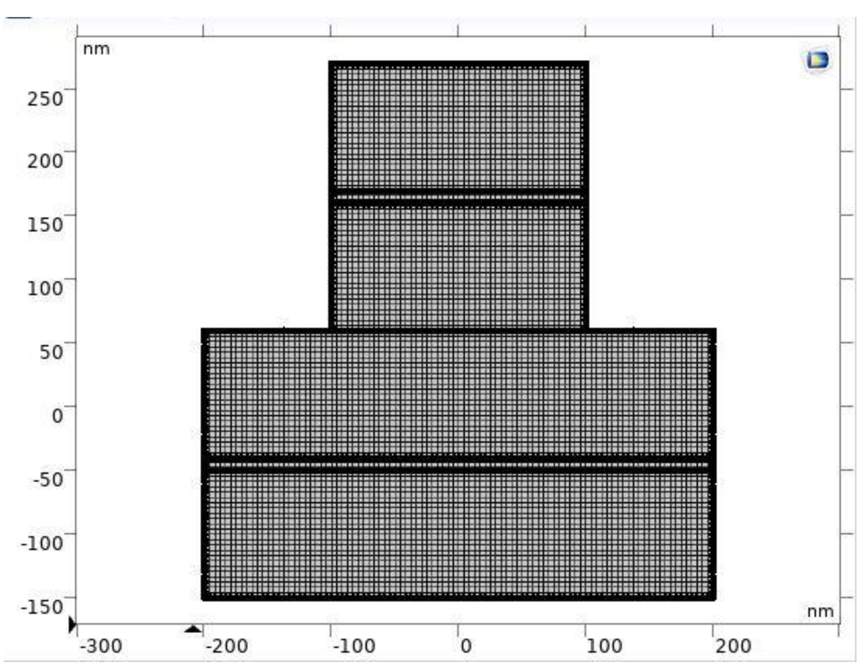

Figure 50: Mesh distribution of model in COMSOL

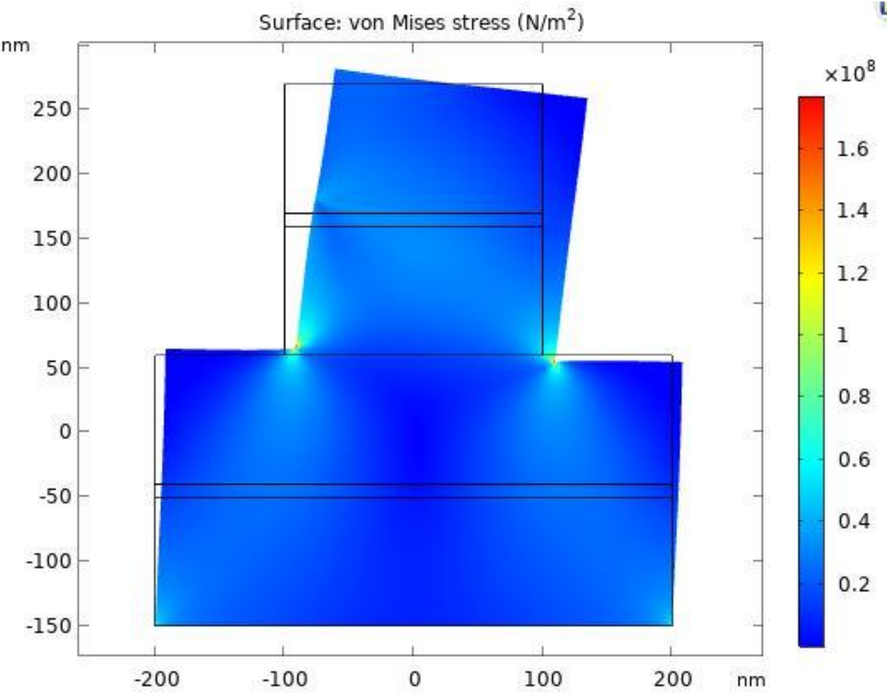

Figure 51: Colour plot of von Mises stress from simulation with red depicting the highly stressed areas and blue depicting low stressed areas

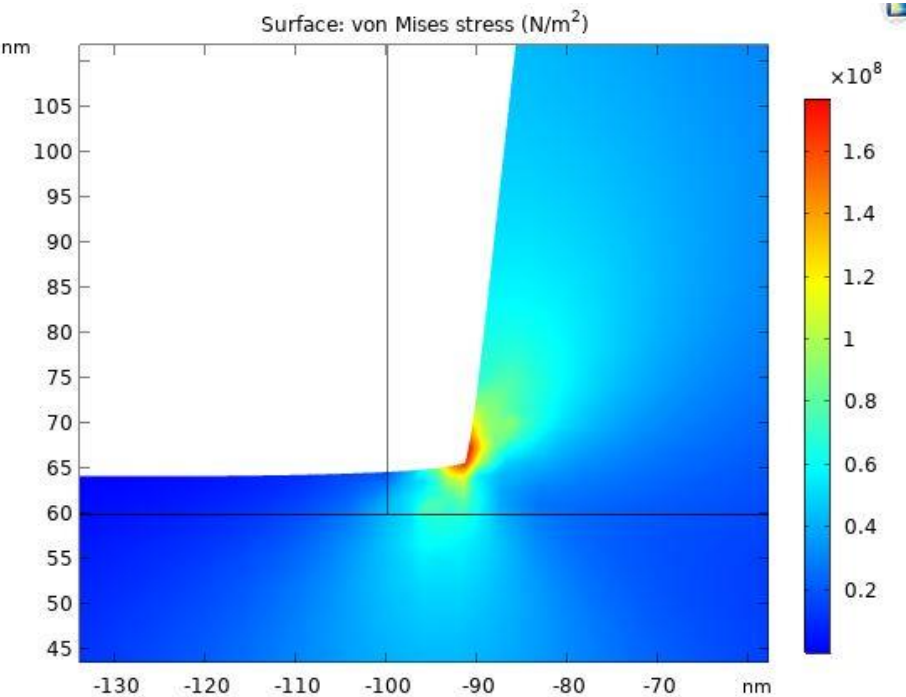

Figure 52: Zoomed in colour plot of von Mises stress of the high stress area on the left of the model. Red depicting the highly stressed areas and blue depicting low stressed areas

4.4 Cu-Cu Fusion Bonding Hermetic Sealing Evaluation

Hermetic sealing is essential for 3D integration and packaging of MEMS devices. Hence, it is advantageous for a bonding method to be capable of achieving hermetic seals. In this section, hermetic sealing capability of Cu-Cu fusion bonding was evaluated. Only plasma pre-treatment with passivation used with different post-bonding annealing temperature similar to shear strength test part 2.

4.4.1 Hermetic Seal Test Die Fabrication

Single side polished, P-type, 150 mm diameter, 675 +/- 25 µm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm was used. The wafer was patterned by lithography and etched by deep reactive-ion etching (DRIE) for 80 µm to form sealing rings with 4.973 mm by 3.12 mm internal dimension. This resulted in a cavity volume of 1.24 mm^3, more than the 1 mm^3 required for accurate He leak testing as investigated in a study [74]. Cavity volume of less than 1 mm^3 will results in He leak rate that does not represent the actual leak rate required to maintain hermeticity. The width of the sealing ring is 150 µm.

After DRIE, the remaining resist was stripped and layers similar to the shear strength test dies were deposited (200 nm of SiO_2, 10 nm of Ti and 100 nm of Cu). The wafer was coated with resist again to protect from dicing debris and contaminations. The wafer was diced into dies with 1 mm gap from the sealing ring as shown in Figure 53. This formed the top dies for the hermetic seal test samples. The bottom dies were 10 mm by 10 mm blanket dies with the same metal layers as the top die. The dies will be place face to face during bonding as shown in Figure 53.

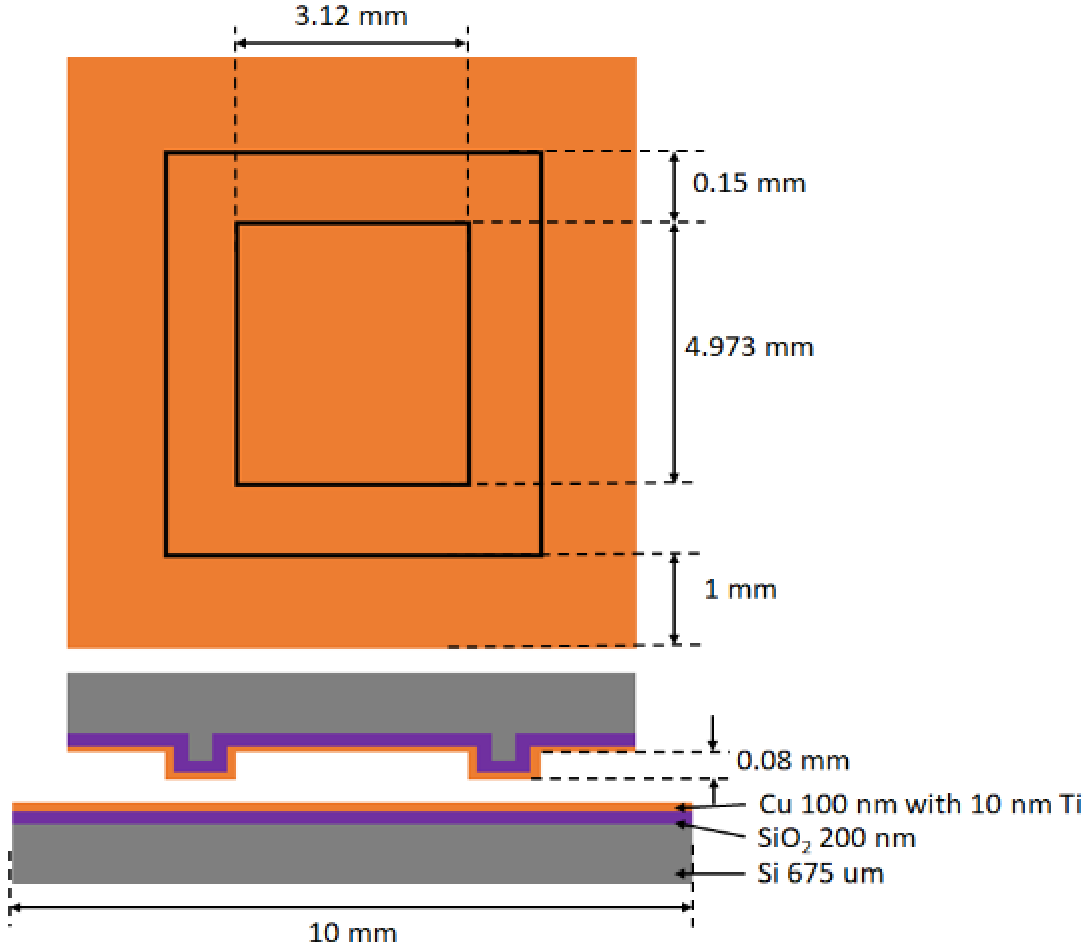

Figure 53: Hermetic seal test sample schematic with sealing ring dimensions and top and bottom dies configuration (not drawn to scale)

4.4.2 Hermetic Seal Test Sample Bonding

After dicing, the top and bottom dies were cleaned with acetone followed by IPA and water to remove the protective resist. The clean dies were dried with a N_2 gun and subjected to plasma pre-treatment with passivation. Plasma

parameters used were the same as the ones used in the shear strength test sample bonding shown in Table 4. After the plasma pre-treatment, the dies were transferred to a wafer bonder while exposing to clean room atmosphere environment (room temperature, normal atmosphere pressure and air) within 5 min from the plasma pre-treatment. The dies were manually placed face to face in the bonder. Unlike the shear strength test samples, the air in the chamber was pump down to 10 Pa before the pre-bond. This was to allow the air in the cavity to be drawn out preventing internal pressure to de-bond the samples in subsequent pump down. Force was applied to the dies at 385.24 MPa (970 N for each die with 2.518 mm^2 bonding area) for 5 min to pre-bond the dies. Much higher force was used for these samples. It is hypothesized that the van der Waals forces are lower due to lower ratio of bonding area to the edges of the bonding feature, as compared to the shear test samples in previous sections. After the pre-bonding, the top chuck that applied the force was moved away from contact to the dies to ensure no force was applied for the post-bonding annealing process.

The air in the chamber purged with N_2 gas after the pre-bond step. The chamber was subsequently pump down to 10 Pa and purged with N_2 gas for 2 more cycles to achieve inert annealing environment. Post-bonding annealing was carried out with N_2 at atmospheric pressure in the chamber. For this section, different post-bonding annealing temperatures were used. The temperature used were 150, 200, 250 and 300 °C using post-bonding annealing profile shown in Figure 47. Five samples were fabricated for each annealing temperature.

4.4.3 Fine Leak Test

To test for hermeticity, both fine leak test and gross leak test were performed on the samples. For fine leak test, He leak test was used. The hermetic test samples were placed in a bombing chamber with helium gas at a pressure 0.52 MPa for more than 4 hours as specified in MIL-STD-883E [75]. After the pressure of the chamber was released, the samples were tested one by one with a vacuum He leak detector machine (an integrated vacuum chambers and a mass-spectrometer-type leak detector calibrated for helium).

The samples were then analyzed by the leak detector for the presence of helium, leak rates of the helium were recorded when the test chamber reaches below 0.134 Pa (0.001 Torr). The samples must complete the leak rate test within an hour from the release of He pressure from the chamber.

4.4.4 Gross Leak Test

In order to ensure the fine leak test results were reliable, a gross leak test was performed. Samples with gross leaks will have low He leak rate as the He gases in the test cavity would have escaped in the test chamber before 0.134 Pa had been reached. Perfluorocarbon bubble (gross leak) test was performed by submerging the dies in fluorocarbon C_6F_{14} in a pressurized chamber of 0.52 MPa for 3 h. The dies were taken out and allowed to dry for at least 1 min but not more than 3 min, allowing C_6F_{14} on the surface to be removed. The dried dies are place in a beaker of fluorocarbon $C_{12}F_{27}N$ at 125 °C. As the boiling temperature of C_6F_{14} is at 56 °C, it will boil within the cavity and escape as bubbles. If a stream of small bubbles or a single big bubble is observed, the sample would have failed the gross leak test. The samples have to pass both the helium fine leak test and the gross leak test.

4.4.5 Hermetic Seal Test Results and Discussion

The results of the fine and gross leak are shown in Figure 54. Lowest mean leak rate was observed on the samples that were post-bonding annealed at 250 °C with all samples passing the gross leak test. All samples that were post-bonding annealed at 300 °C passed the fine and gross leak test. Only one sample annealed at 200 °C failed the fine leak test, which is also the only one that failed the gross leak test. Although the results of the fine leak rate for the 150 °C annealed sample are lower than the passing leak rate, all five samples failed the gross leak test. Hence annealing at 250 °C yields the best hermetic seal with mean leak rate of 8.78×10^{-9} atm-cc/s while 300 have mean leak rate of 2.4×10^{-8} atm-cc/s.

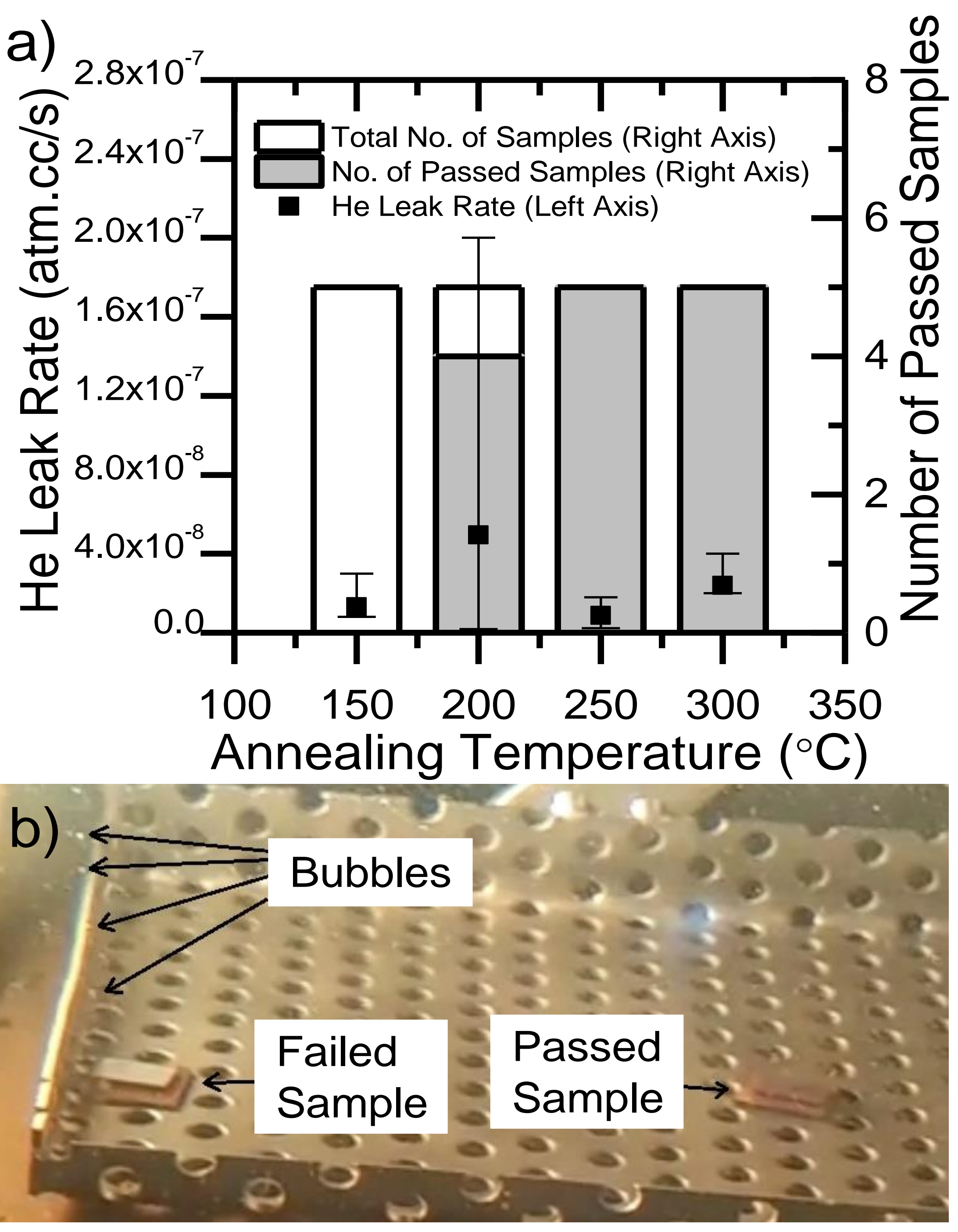

Figure 54: a) Mean He leak rate error bars depicting highest and lowest value (left axis), number of samples that passed both fine and gross leak test (right axis) and b) stream of bubbles observed from failed sample

4.5 Cu-Cu Fusion Bonding Electrical Characterization

Good electrical characteristics from the bonding are essential for BEOL interconnects. In this section, the structures from our Cu-Cu fusion bonding process were electrically characterized for resistance of the structure after

bonding. Plasma pre-treatment with passivation and without passivation were characterized to identify the effects of passivation on electrical characteristics. Daisy chain structures were used for the characterization. Temperature cycling tests (TCT) were also performed on the daisy chain samples for reliability study on the Cu-Cu fusion bonding. Cross bridge kelvin resistor (CBKR) structures were also fabricated to test the repeatability of the die to die Cu-Cu Fusion Bonding.

4.5.1 Daisy Chain Fabrication

The mask design for the daisy chain structures are shown in Figure 55. The light green features are the top die electrodes and the teal features are the bottom die electrodes. The bottom die electrodes extend out to form multiple probing pads (not shown in figure) for measurement at each segment of the daisy chain. Each contact area between the top and bottom dies is 20 µm by 20 µm. This large contact area is required to have enough bonded strength while being far apart to prevent shorting due to low accuracy of the die bonder (+/- 5 µm). there is a total of 224 contacts in the mask design with 28 contacts between two measurement pads.

Single side polished, P-type, 150 mm diameter, 675 +/- 25 µm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm was used. The wafers were patterned by lithography to the mask design shown in Figure 55, green patterns were the metal lines for the top and teal patterns for bottom structures with the contact pads extending out to enable probing. Both wafers were etched by reactive-ion etching (RIE) for 3 µm to form a stand-off gap that prevent dicing edges from affecting the bonding. After RIE, the remaining resist was stripped and 200 nm of SiO_2 is deposited by TEOS PECVD. The wafers were coated with negative resist (ma-N 1440) patterned with lithography with the exact mask design as the previous RIE process. 10 nm of Ti and 100 nm of Cu were deposited by EBPVD and metal lift-off was performed to form the electrodes. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. The wafers were coated with resist again to protect the surface from dicing.

Dummy daisy chain structures were also fabricated with the same processes to act as control. The electrodes were connected in on a single die without the need to bond the top and bottom dies to form the daisy chain.

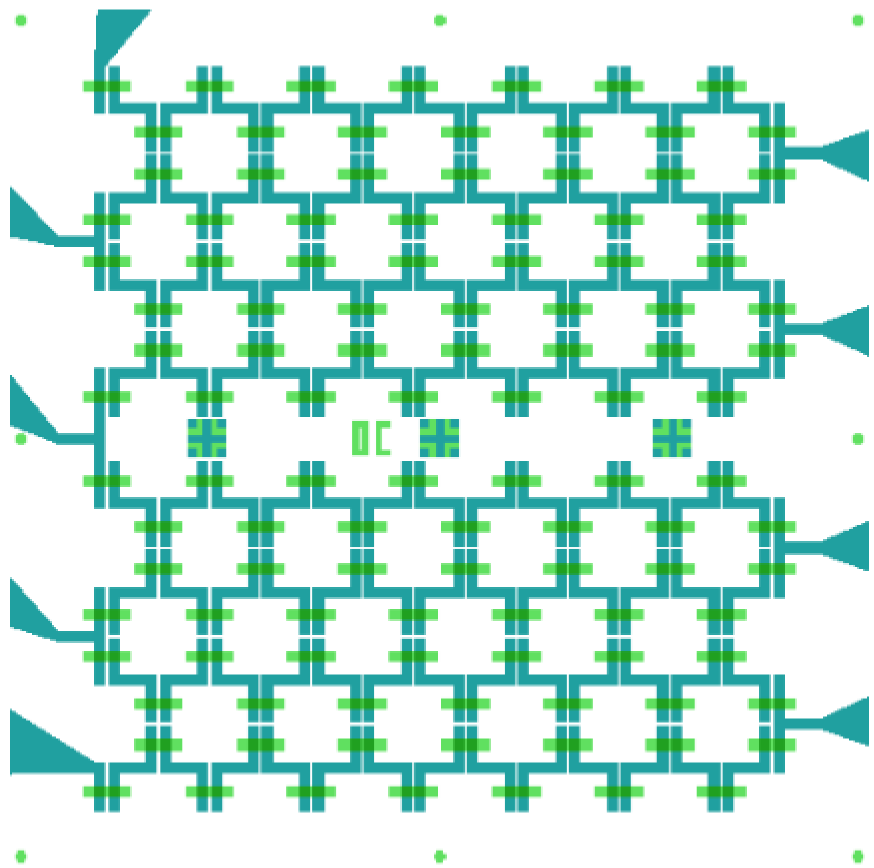

Figure 55: Daisy chain mask design

4.5.2 Daisy Chain Sample Bonding

After dicing, the top and bottom dies were cleaned with acetone followed by IPA and water to remove the protective resist. The clean dies were dried with a N2 gun and subjected to plasma pre-treatment. Two types of plasma pre-treatment similar to the ones used in the shear strength test were evaluated, one with passivation from Ar + N2 plasma and one without passivation. The plasmas parameters are shown in Table 2.

After the plasma pre-treatment, the dies were transferred to a die bonder with alignment accuracy of +/- 5 µm. The top and bottom dies were aligned, and place together face to face with 2343.75 MPa force in clean room atmosphere environment (room temperature, normal atmosphere pressure and air) within 5 min from the plasma pre-treatment for 5 min to pre-bond the dies. After the pre-

bonding, the dies were transferred to the wafer bonding for batch post-bonding annealing. The air in the chamber was pump down to 10 Pa and purged with N_2 gas for 3 cycles to form a N_2 at atmosphere within the chamber. Post-bonding annealing was carried out with N_2 at atmospheric pressure in the chamber. The top chuck and bottom were slowly ramped up to 300 °C for post-bonding annealing. 300 °C were chosen to stimulate harsher oxidation environment compared to 250 °C. N_2 environment was used instead of vacuum to allow convection heating as the top chuck was not in contact with the dies. The dies were kept at 300 °C for 1 h before cooling down to room temperature in bonding chamber.

Three dummy samples were also processed. The first sample was not subjected to any plasma pretreatment, the second sample was subjected to plasma pretreatment with passivation and the last sample was subjected to plasma pretreatment without passivation. All three sets of dummy samples also underwent the same post-bonding annealing as the bonded samples.

4.5.3 Daisy Chain Characterization

An electrical probing machine was used to measure the resistance of the daisy chain structures as shown in Figure 56. The measurement current was set to sweep from -1 mA to 1 mA with 0.02 mA step size. In this probing configuration, 168 contacts in the daisy chain were measured with the measurement pads labeled V1 and V2 in Figure 51.

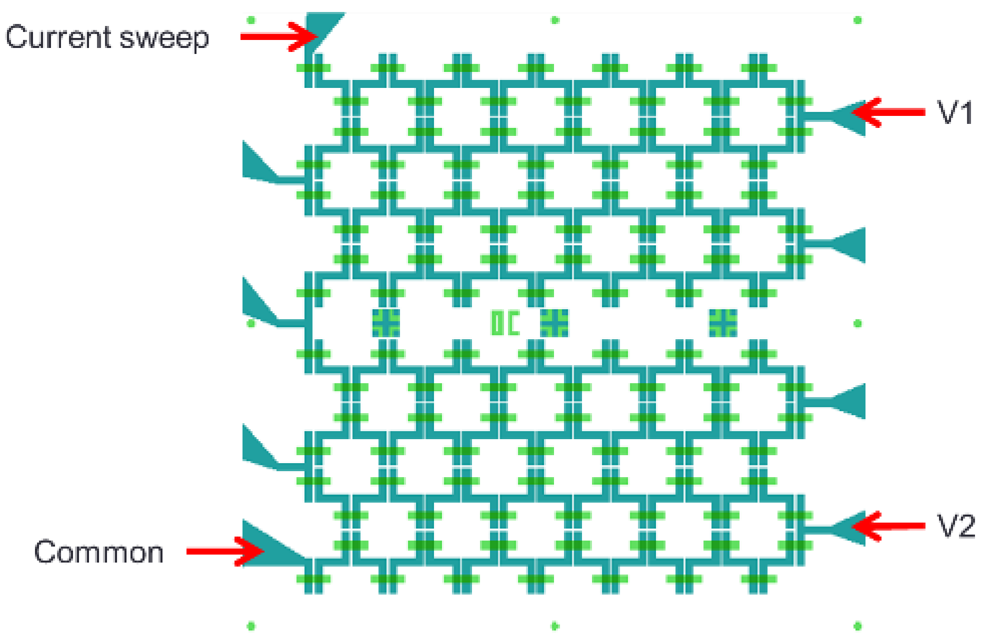

Figure 56: Probing of daisy chain

4.5.4 *Daisy Chain Results and Discussions*

Figure 57 shows the measured results for the daisy chain samples. Dummy samples (non-bonded non-heated) prior to any processes have the lowest resistance. After heating, the dummy samples that had plasma pre-treatment with passivation (non-bonded Ar/N2) has the lowest increased in resistance as compared with the plasma pre-treatment without passivation (non-bonded Ar) sample and without any pre-treatment (non-bonded heated) sample. This shows that more oxidation had occurred on the dummy sample with the plasma pre-treatment without passivation, hence, stipulating that the passivation is able to reduce oxidation during the post-treatment annealing process. It can also be observed that the pre-treatment without passivation has increased rate of oxidation compared to without pre-treatment.

Bonded samples showed higher measured resistance compared to the dummy samples (47 Ω for the pre-treatment with passivation and 134 Ω for the pre-treatment without passivation). The increase in resistance could be due to misalignment or oxidation at the bonding interface. The plasma pre-treatments effect on sheet resistance were evaluated.

TCT were performed on all the samples with temperature cycling from -40 to 125 °C for 1000 cycles according to JEDEC standard, JESD22-A104 using

test condition G. The samples were measured twice, once after 500 cycles and after 1000 cycles.

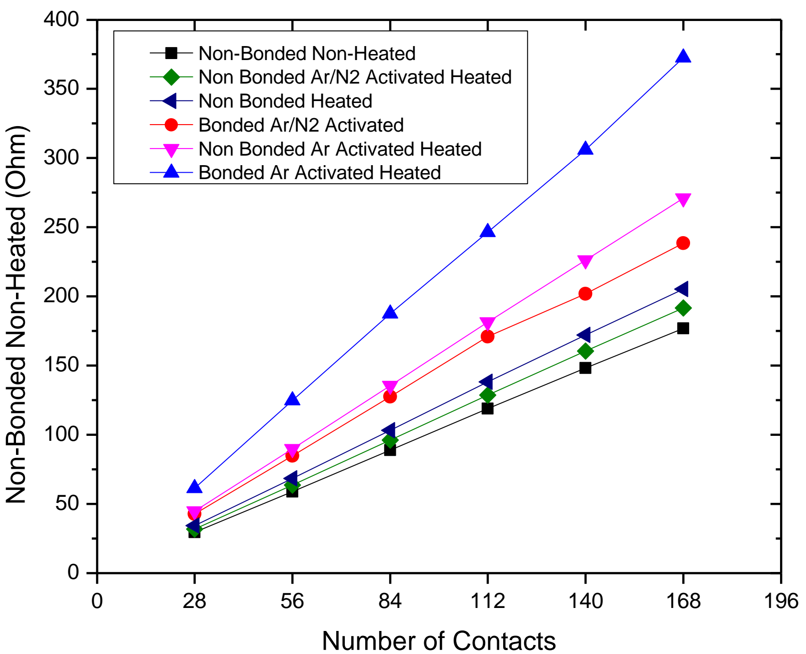

Figure 57: Resistance of various daisy chain samples

The resistance of the samples measured after 500 and 1000 cycles of TCT were compared with the respective measurements prior to TCT in Figure 58, Figure 59 and Figure 60. The plots are standardized to show before TCT with dotted lines, after 500 cycles with dashed lines and after 1000 cycles with solid lines. Figure 58 shows the resistance changes to the dummy sample that did not undergo any pre-treatment. The resistance increases after each 500 cycles with the second 500 cycles causing higher degradation to the daisy chain structures. These results will serve as a control to the rest of the samples for comparison.

Figure 59 shows the resistance of dummy (after annealing) and bonded samples that underwent pre-treatment without passivation before and after TCT. The bonded sample failed after 1000 cycles; hence no data was included. It can also be observed that the result for the bonded sample after 500 cycles is no longer linear after the 112nd contact measurement point. This could be due to uneven oxidation rate across the sample or the bonds at that location had

started to fail due to expansion and contraction of die from the TCT. Figure 60 shows the resistance of dummy (after annealing) and bonded samples that underwent pre-treatment with passivation before and after TCT. The samples after 500 cycles display similar characteristic as the samples without passivation. Large increases of resistance are observed for both the bonded and dummy samples with the bonded sample exhibiting non-linear characteristic after the 112nd contact measurement. However, the bonded samples survived all 1000 cycles and has lower resistance compared to the dummy samples which also shows non-linearity after 1000 cycles.

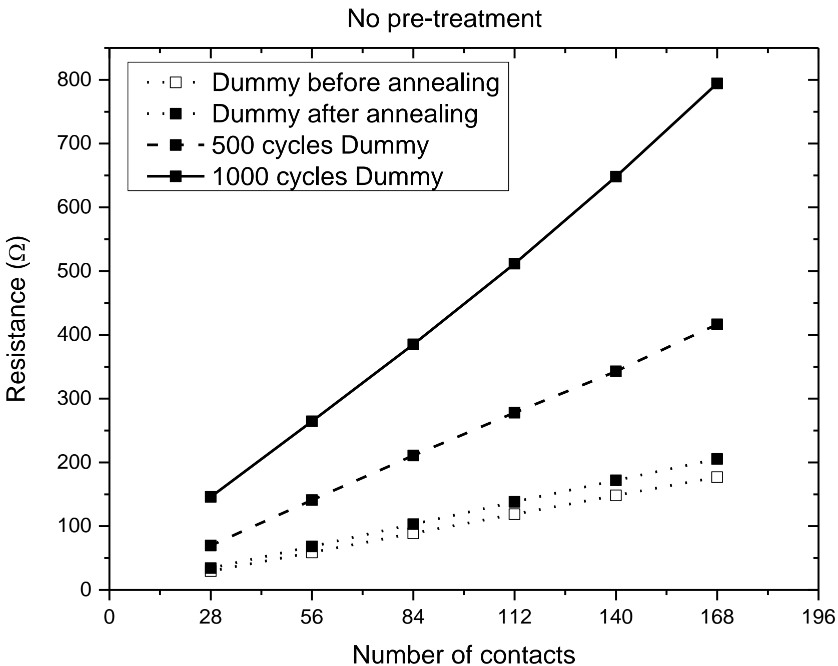

Figure 58: Resistance of dummy sample without pre-treatment before and after TCT

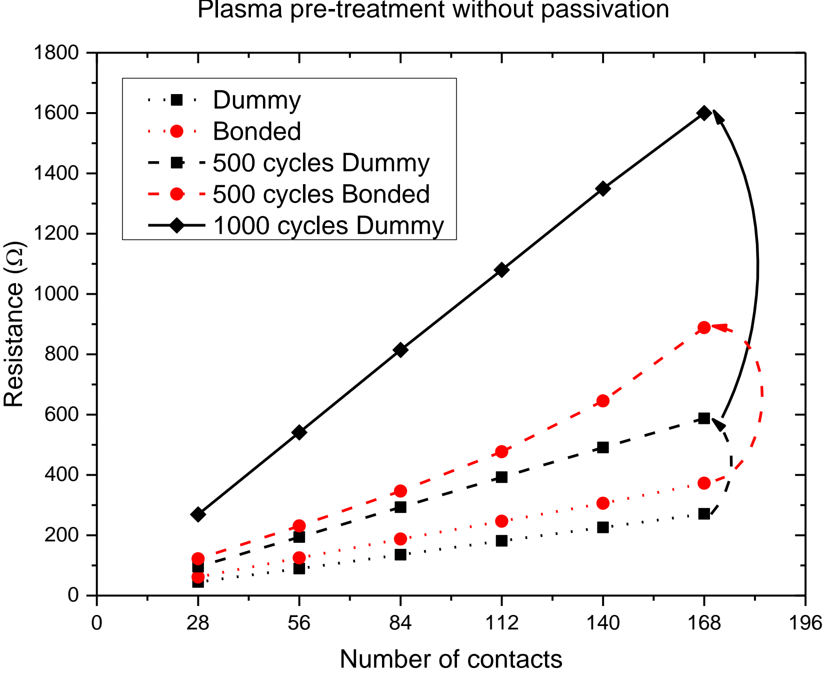

Figure 59: Resistance of dummy and bonded samples with pre-treatment without passivation before and after TCT

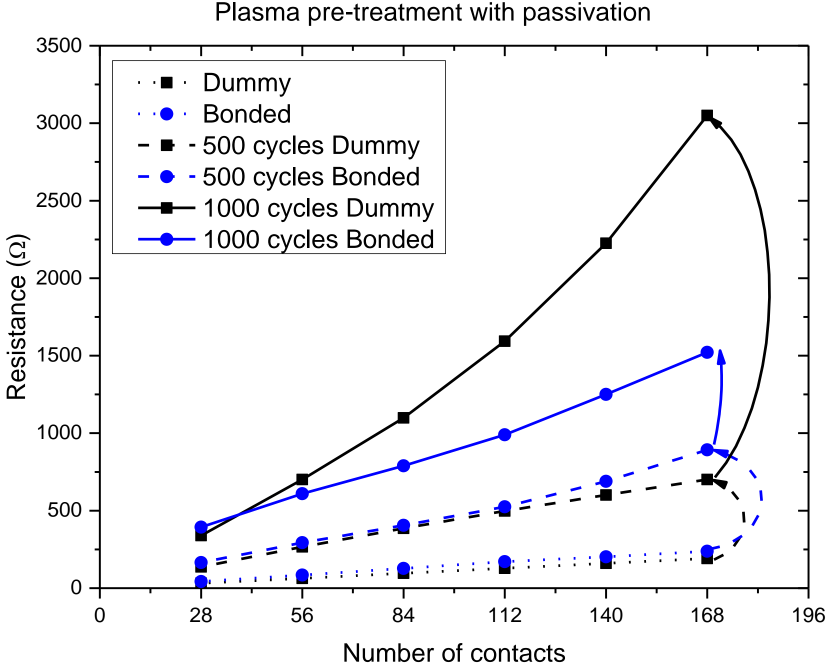

Figure 60: Resistance of dummy and bonded samples with pre-treatment with passivation before and after TCT

Due to the design of the daisy chain structures, measurements were taken row by rows. Only the difference in resistance from each row is being

measured across the two measuring pads. Hence it is important to note that a linear plot may not necessarily means the resistance is uniform across all the daisy chain. Figure 61 illustrates the variation that will cause non-linearity to be observed in case A while variation along the rows will shows linear results due to the design of measurement points. The non-linearity observed for the three samples in Figure 59 and Figure 60 shows that there were increase in resistance on one side of the samples as described as case A. A non-linear rise in resistance on one side of the dummy sample (pre-treatment with passivation) after TCT, can only be caused by different oxidation rate across the die. This could be due to non-uniform heating or air flow in the TCT chamber.

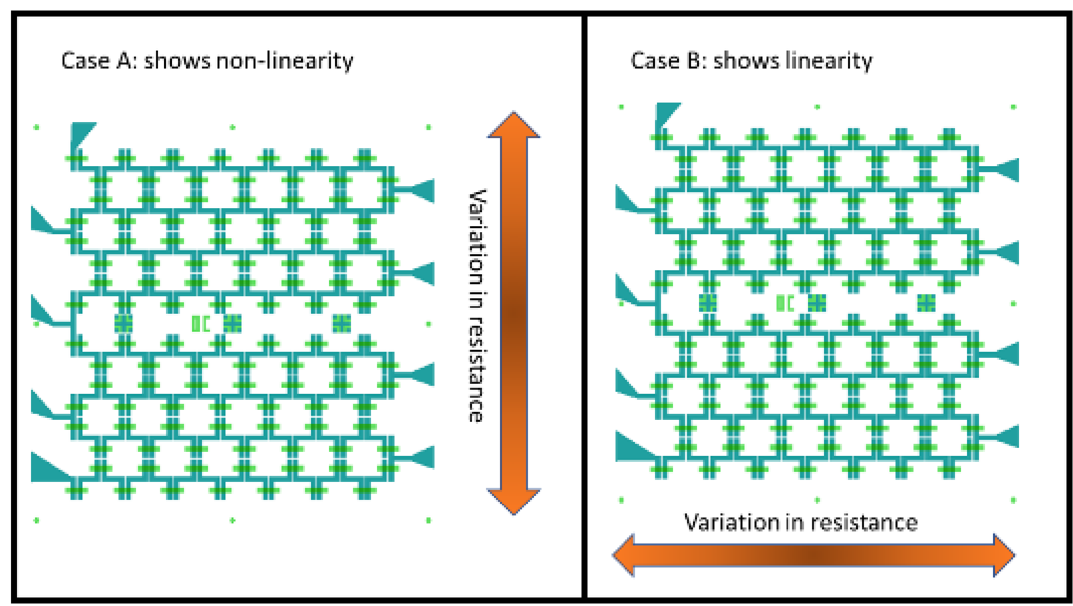

Figure 61: Illustration of variation in resistance effect on linearity

Figure 62 compares the resistance of all samples after 1000 cycle TCT. It can be concluded that the plasma pre-treatment, with or without passivation, caused the surface to easily oxidize in cyclic temperatures situations. However, the bonded sample with plasma pre-treatment with passivation have shown resistance comparable to the dummy sample with pre-treatment without passivation which shows that the large increase in resistance is the result of the oxidation of Cu line that was not bonded. To confirm this hypothesis, the bonded sample was broken apart to observe the failure interface. Figure 63 shows the optical image of the broken sample. It can be observed that most of the failure occurs at the Si stand-off and at the substrate that was DRIE etched. Large misalignment is also observed. This is suspected to be caused by the bottom

die shifting during the pre-bond when the top die was placed in contact as there was no clamping capabilities from the bottom chuck. The misalignment could have caused the increase in resistance right after the annealing.

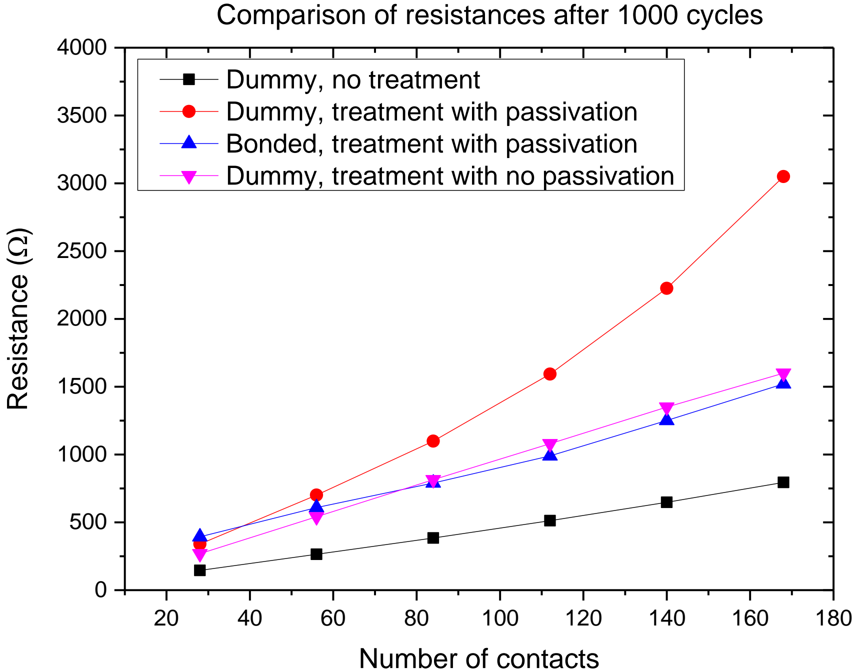

Figure 62: Comparison of samples resistances after 1000 cycle TCT

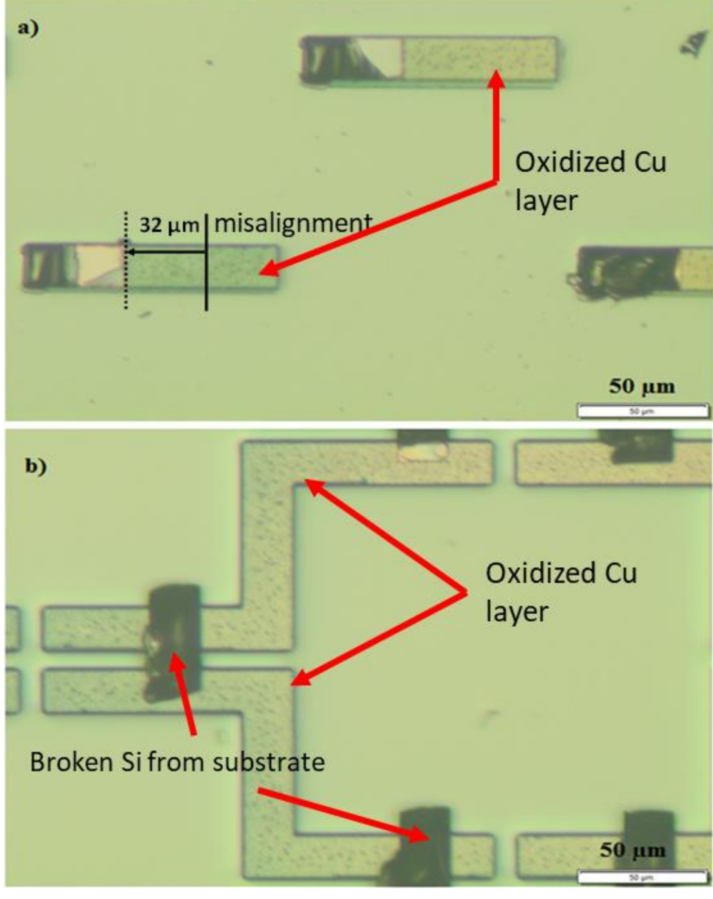

Figure 63: Optical microscope image of separated a) top die with misalignment from original design and b) bottom die of bonded sample

4.5.5 Microstructure and Elemental Composition Characterization of TCT Samples

Since it was concluded that the higher increase in resistance for the samples that underwent plasma pre-treatment was due to higher oxidation. The bottom die of the bonded sample and the dummy without pre-treatment unbonded area were observed by transmission electron microscopy and energy-dispersive X-ray spectroscopy (TEM/EDX) line scan. Pt was deposited as a protection layer for FIB milling to prepare the TEM lamella. Figure 64 and Figure 65 show the TEM/EDX line scan of the dummy and bonded sample bottom die at the unbonded metal layers, respectively. The line scan in Figure 64 (dummy) shows that the bonded sample has a lower thickness of the Cu layer as compared to the line scan in shown in Figure 65 (bonded sample). This shows that the oxidation rate of Cu is higher after plasma pre-treatment. This increase in oxidation consumes larger amount of Cu and increases the

resistance of the daisy chain. A TEM image of the bonded sample in Figure 66 shows varying depth of oxidation along the metal line with one portion of Cu severely oxidized. This is a likely cause of the large increase of resistance compared to the dummy sample.

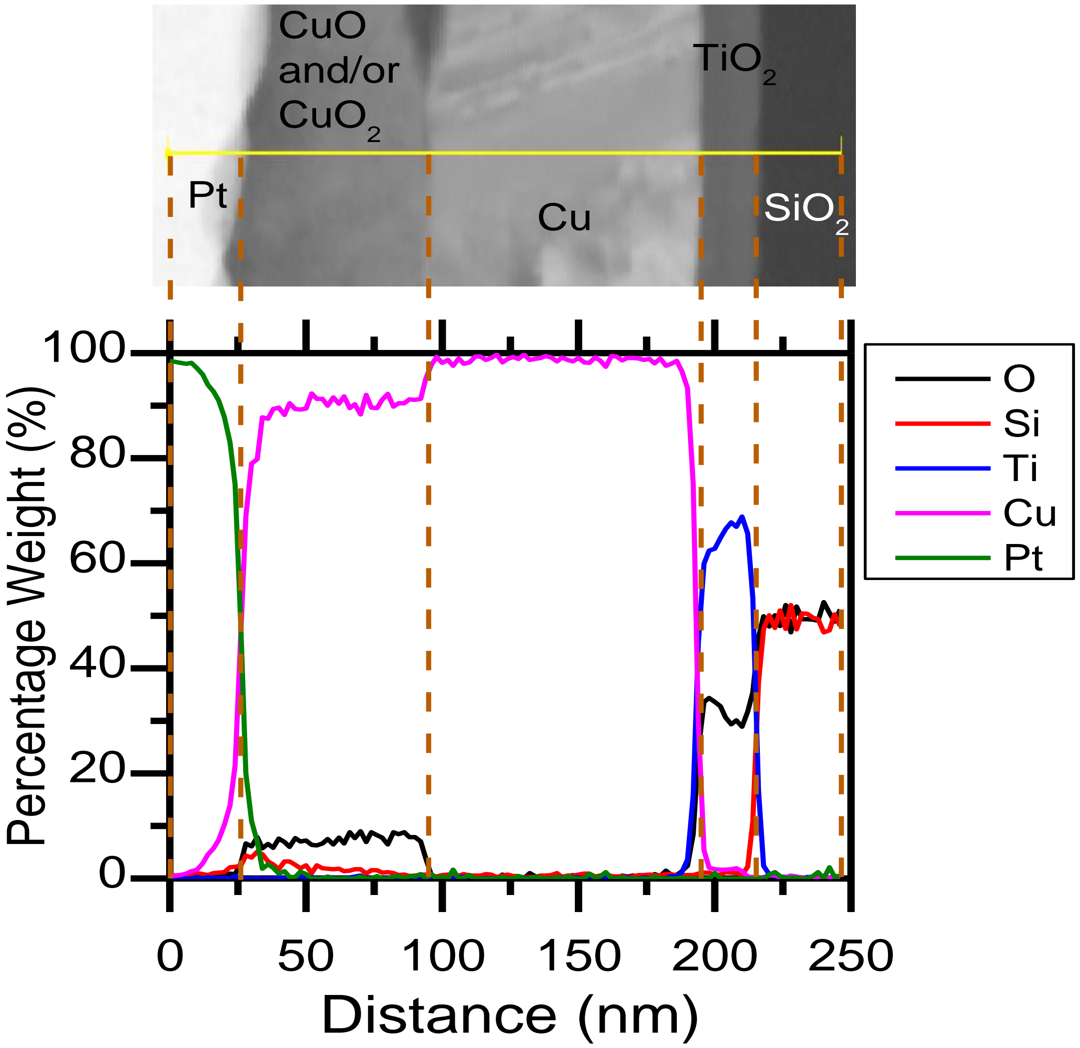

Figure 64: TEM/EDX linescan of dummy sample at its unbonded metal layers after 1000 cycle TCT

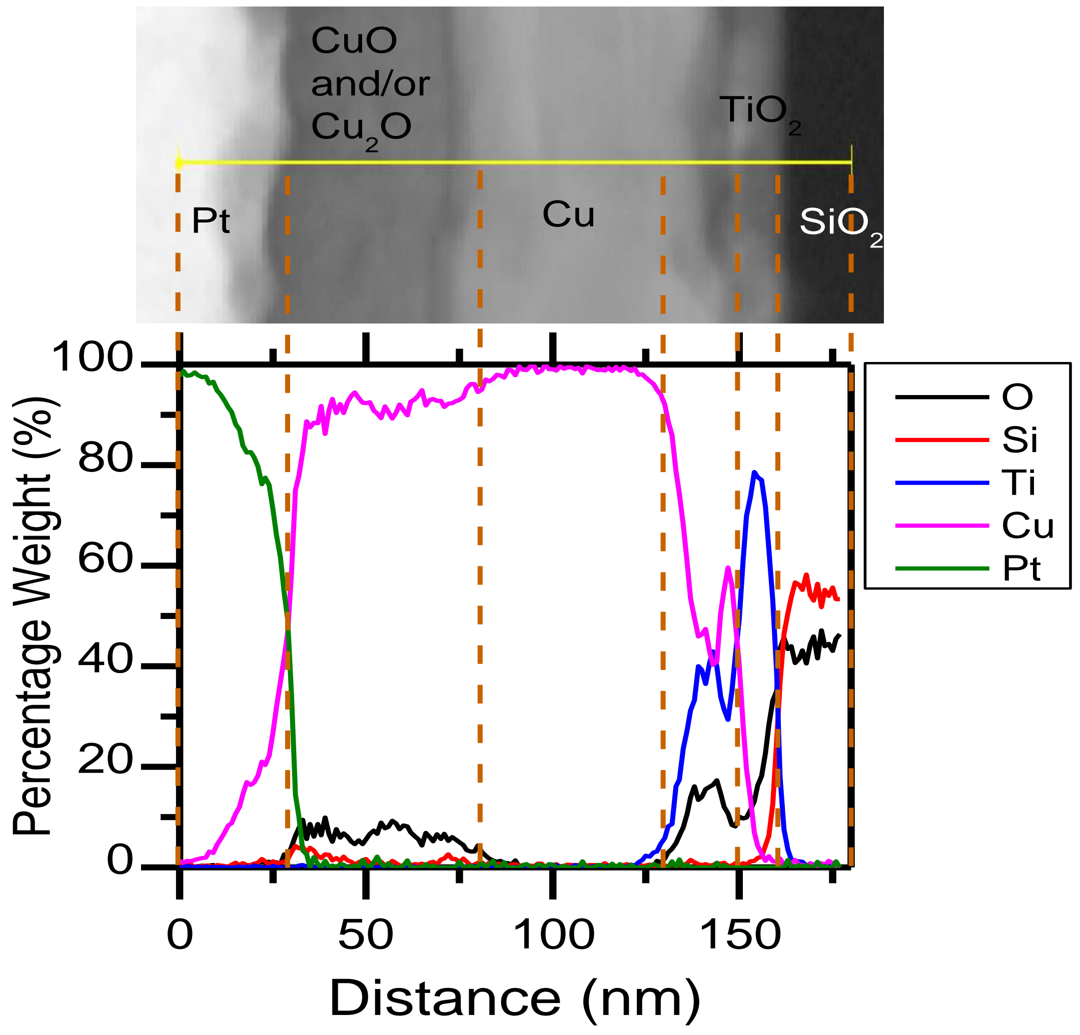

Figure 65: TEM/EDX linescan of bottom die of bonded sample at its unbonded metal layers after 1000 cycle TCT.

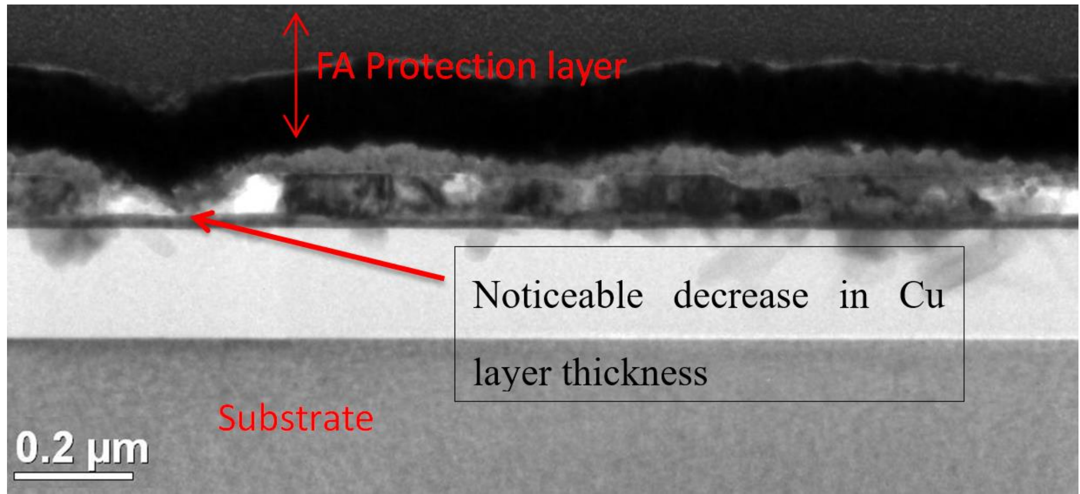

Figure 66: TEM of bonded sample bottom die at its unbonded metal layers

4.6 Cross Bridge Kelvin Resistor Fabrication

To determine the uniformity of the bonding throughout the die, cross bridge kelvin resistor (CBKR) structures for bonding were designed at each quadrant of the die. Single side polished, P-type, 150 mm diameter, 675 +/- 25 μm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm was used. The wafer was patterned by lithography as shown in Figure 67a) for the bottom die and Figure 67b) for the top die. There are four sets of CBKR in a single die after being bonded. The bonding area from the top and bottom dies are 100 μm by 100 μm for each CBKR. Both wafers were etched by reactive-ion etching (RIE) for 3 μm to form a stand-off gap that prevent dicing edges from affecting the bonding. After RIE, the remaining resist was stripped and 200 nm of SiO_2 is deposited by TEOS PECVD. The wafers were coated with negative resist (ma-N 1440) patterned with lithography with the exact mask design as the previous RIE process. 10 nm of Ti and 100 nm of Cu were deposited by EBPVD and metal lift-off was performed to form the electrodes. Only 10 nm Ti and 100 nm Cu were deposited to prevent increase of surface roughness from the EB–PVD process as Cu CMP was not available. Figure 68 shows the different layers (SiO_2 and Ti/Cu) in a bonded sample. The wafers were coated with resist again to protect the surface from dicing. Top dies were diced into 2 mm by 2 mm while the bottom dies were diced into 5 mm by 5 mm. With the top dies smaller that the probing pads, the pads will be exposed after bonding for probing.

Dummy CBKR structures were also fabricated with the same process, however, the CBKR electrodes were connected in a single layer similar to Figure 67c) without the need to bond the top and bottom dies. Figure 69 shows the schematics of the bonded sample and the dummy sample. The Cu layer at the bonded area of the bonded samples were twice as thick as that of the dummy structures.

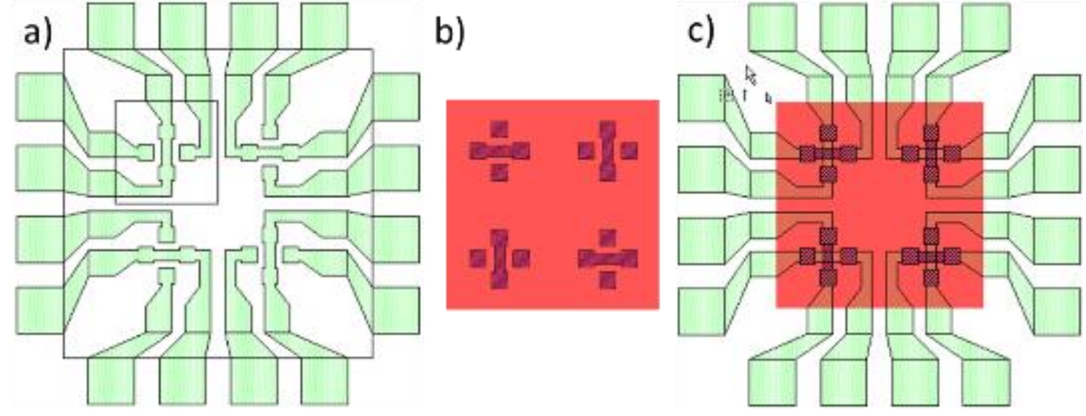

Figure 67: Mask design for CBKR structures: a) bottom die electrodes, b) top die electrodes, c) electrodes after bonding

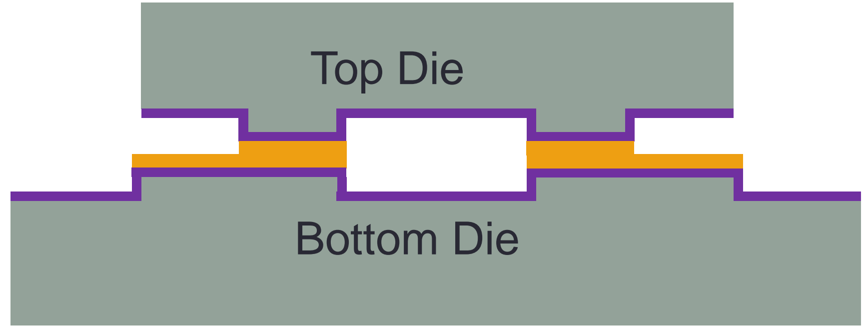

Figure 68: Illustration of the different layers in a bonded sample

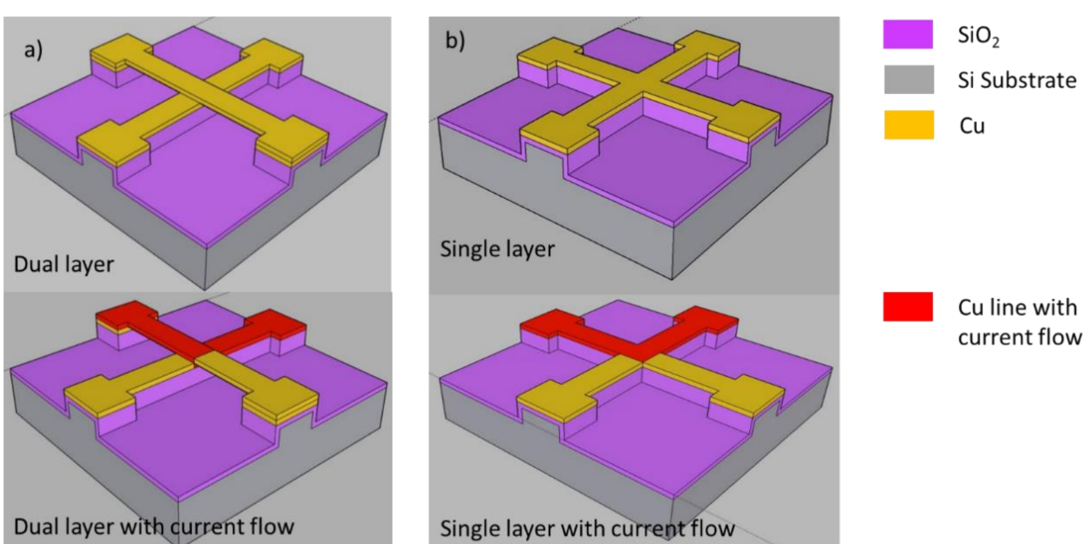

Figure 69: Schematic of a) bonded sample with double metal layers and b) dummy sample with single layer

4.6.1 *Cross Bridge Kelvin Resistor Bonding*

After dicing, the top and bottom dies were cleaned with acetone followed

by IPA and water to remove the protective resist. The clean dies were dried with a N_2 gun and subjected to plasma pre-treatment with passivation from Ar + N_2 plasma. The plasmas parameters are shown in Table 4.

After the plasma pre-treatment, the dies were transferred to a die bonder with alignment accuracy of +/- 5 µm. The top and bottom dies were aligned, and place together face to face with 5,250 MPa force in clean room atmosphere environment (room temperature, normal atmosphere pressure and air) within 5 min from the plasma pre-treatment for 5 min to pre-bond the dies. After the pre-bonding, the dies were transferred to the wafer bonding for batch post-bonding annealing. The air in the chamber was pump down to 10 Pa and purged with N_2 gas for 3 cycles to form a N_2 at atmosphere within the chamber. Post-bonding annealing was carried out with N_2 at atmospheric pressure in the chamber. The top and bottom chuck were slowly ramped up to 300 °C for post-bonding annealing. N_2 environment was used instead of vacuum to allow convection heating as the top chuck was not in contact with the dies. The dies were kept at 300 °C for 1 h before cooling down to room temperature in the bonding chamber. The bonded samples are shown in Figure 70.

Figure 70: Bonded CBKR samples

4.6.2 Cross Bridge Kelvin Resistor Characterization

An electrical probing station was used to measure the resistance of the CBKR with the current passing through the top metal layer to the bottom layer.

Current was set to sweep from -50 mA to 50 mA with 5 mA steps. Two probes were used as voltmeter units to measure the voltage difference between the top and bottom die at the bonding interface as shown in Figure 71a). The probes positions for the dummy sample are shown in Figure 71b). Bonded samples and dummy CBKR structures measured area from voltmeter unit V1 and V2 are the same (100 μm × 100 μm). However, the bonded structures have twice the cross-sectional area as compared to the dummy samples due to double layer of metal at the bonding interface as shown in Figure 69.

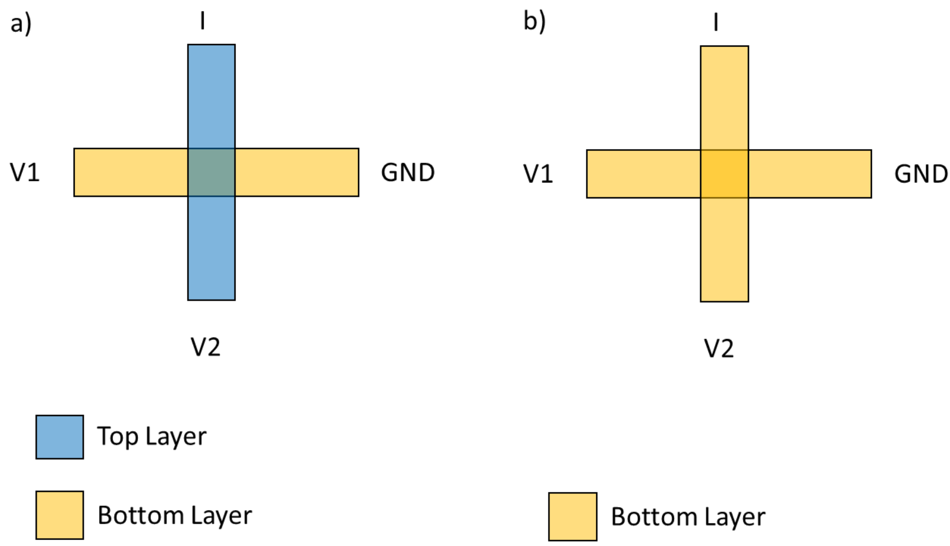

Figure 71: Schematic showing the probes for the four-point contact measurement: a) bonded sample and b) dummy sample

4.6.3 Cross Bridge Kelvin Resistor Results and Discussion

Both plasma pre-treatment with and without passivation shows good uniformity in bonding with all four CBKR well connected. The dummy samples measured a mean resistance of 0.0691 Ω while the plasma pre-treatment with passivation have a mean resistance of 0.0348 Ω. Figure 72 shows the normal probability plot of the resistances of the bonded samples. The resistances formed a nearly linear pattern, which indicates that they are normal distributed. No outliners were present which shows that all CBKR structures are well bonded. The bonded samples have approximately half of the resistance which correlated with twice the amount of cross-sectional area of the dummy sample.

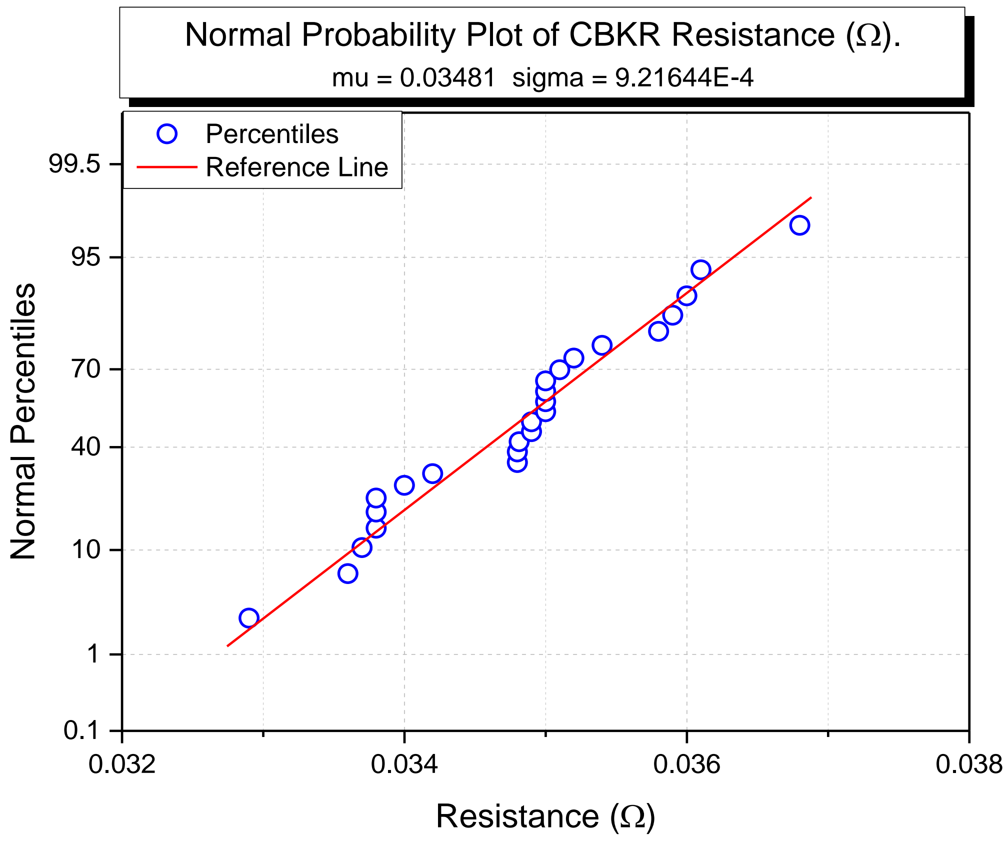

Figure 72: Normal probability plot of CBKR resistance

4.7 Summary

Shear strength tests have been performed on samples pre-treated with and without passivation. Although the previous chapter have shown better bonding interfaces for the pre-treatment with passivation (zig-zag interface), the shear strength test was unable to differentiate them. This was likely due to the failure interface at the Ti adhesion layer. Different annealing temperature effect on the shear strength and hermetic sealing were also investigated. According to the diffusion equation, shear strength and hermetic sealing should be better with higher annealing temperature. However, it was not shown to be the case in this work. This could be due to the failure at the Ti adhesion layer. The highest mean shear strength from the test was 20.3 MPa, from pre-treatment with passivation and post-annealing temperature of 290 °C for 2h.

The exposed Cu surface pre-treated with plasma was also discovered to show high oxidation in TCT daisy chain samples. Hence it is important to passivate the exposed Cu in devices that has undergo plasma treatment.

However, it is important to note that the sample with Cu-Cu fusion bonding from pre-treatment with passivation did not fail after the TCT. Lastly, CBKR structures on four quadrants of the dies were bonded with low variation in resistance demonstrating that the dies were able to be uniformly bonded with the Cu-Cu fusion bonding method.

Although the results are promising, due to lack of fabrication capability for MEMS devices with Cu pads, CMOS MEMS 3D integration was not demonstrated in this thesis.

Chapter 5 Al-Au Thermo-Compression Bonding

5.1 Introduction

Al and Au are common material for the BEOL interconnects (Al in CMOS and Au in MEMS) other than Cu. Al or Au is used when a device fabrication process (for example MEMS fabrication process) is incompatible with Cu. Usually in those fabrication process, HF etching is required and it will etch and remove Cu. Hence Al-Au thermo-compression bonding is investigated and demonstrated with a 3D integration of CMOS and MEMS device. Traditionally, passive caps are bonded to MEMS devices to form a hermetic seal. Figure 73 shows two different 3D integration methods of CMOS and MEMS; system-in-package and chip-scale package. Although both methods reduced the integrated device's footprint laterally, due to the stacking of the dies and passive caps, the vertical footprint of the integrated device increases significantly. In this thesis, a novel MEMS-CMOS active hermetic cap integration method was demonstrated. Figure 74 shows the novel MEMS-CMOS integration method which uses the CMOS dies as the hermetic sealing cap, this only have 2 layer of dies (1 CMOS and 1 MEMS dies) compared to traditional methods which have 3 or more layers (1 cap, 1 CMOS and 1 MEMS dies). This remove the need of an extra passive hermetic cap therefore reduces the thickness of the whole package. The hermetic sealing will be formed by Au sealing ring on the MEMS and Al sealing ring on the last metal layer on the CMOS. This reduction in thickness will be desirable in the modern world of thinner and thinner consumer devices. In this chapter, bond strength and hermetic sealing of the Al-Au bonds was investigated. Microstructures of the Al-Au intermetallic were observed with TEM/EELS. CBKR structures were fabricated to investigate different bonding and annealing temperatures effect on the electrical characteristics.

Additionally, the novel MEMS-CMOS active hermetic cap integration was demonstrated with a self-fabricated Si on insulator (SOI) single axis MEMS accelerometer. Finally shock test was performed on the integrated device for reliability test.

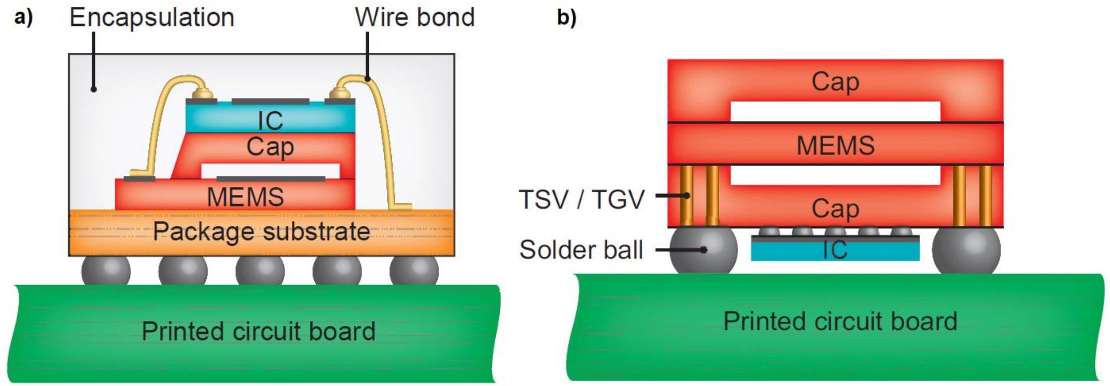

Figure 73: Current MEMS and CMOS 3D integration methods; a) System-in-package solution with wire bonded interconnects and b) Chip-scale packaging with the MEMS and IC chips attached via face-to-face flip-chip bonding [76].

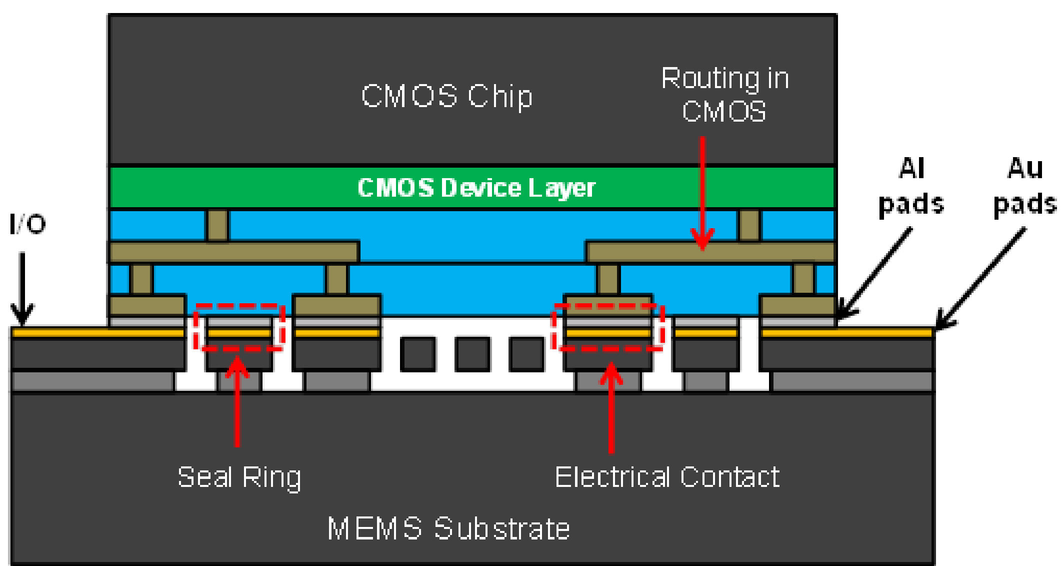

Figure 74: Novel MEMS-CMOS active hermetic cap integration (same as Figure 11)

5.2 Bond Strength Study on Al-Au Bonds

Die shear strength test was used in this chapter to characterize the bond strength of Al-Au thermo-compression bonding at different temperatures.

5.2.1 Shear Strength Test Die Fabrication

Since the novel MEMS-CMOS active hermetic cap integration uses fan out Au pads on the MEMS die for external communication and power input, the MEMS dies is much larger than the CMOS dies. With two different sized dies, it will be more economical to use die-to-die or die-to-wafer bonding instead of wafer-to wafer bonding where the CMOS wafer area will be wasted as those

areas will be discarded to expose the fan out pads. Hence die-to-die bonding was used for the shear strength test. Single side polished, P-type, 150 mm diameter, 675 +/- 25 µm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm was used. For the top dies, 500 nm of SiO_2 was deposited by TEOS-PECVD. Subsequently, sputtering was used to deposit 150 nm of Al. The wafer was spin coated with resist to protect the surface from the dicing process and was diced into 5 mm by 5 mm dies. For the bottom dies, 50 nm of Cr (adhesion and barrier layer) followed by 150 nm of Au were deposited with EBPVD. The wafer was spin coated with resist to protect the surface from the dicing process and was diced into 10 mm by 10 mm dies. Figure 75 shows the different layers of SiO_2 and metals, and the dimensions of the dies.

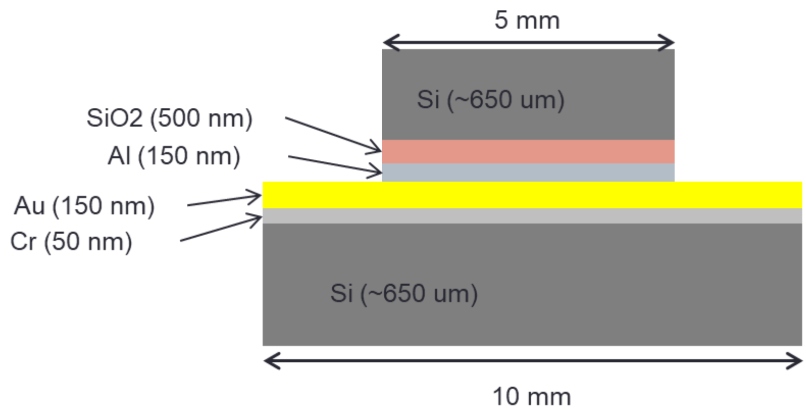

Figure 75: Schematics showing the different layers of material deposited for Al-Au thermo-compression sample (not to scale)

5.2.2 Shear Strength Test Sample Bonding

After dicing, the dies were cleaned with acetone, IPA and water. The samples were bonded die to die with a die bonder. The dies were placed face to face as shown in Figure 75 with 8.4 MPa (210 N on 25 mm^2 bonding area) force applied. Temperatures of the top and bottom chucks were heated to the required bonding temperature for 10 min. Four different bonding temperature were used. The bonding temperatures were 280, 290, 300, temperatures that are safe for CMOS dies and 340 °C, the highest stable temperature achievable by the die bonding machine used. The force applied was released after the chucks had cooled down. After all dies were bonded, each sets of bonded samples were placed in the wafer bonder for annealing at their respective

bonding temperature for 1 h in N_2 environment.

5.2.3 Test Results and Discussions

The samples were glued to microscope glass slides with cyanoacrylates. The shear test was performed as per MIL-STD-883E [73]. Movement speed of contact tool was set at 0.1 mm/min.

The shear strength results are shown in Figure 76. Samples bonded and annealed at 280 °C have the lowest shear strength while increasing the process temperature by 10 °C improved the shear strength significantly. 300 °C exhibited the highest mean shear strength while 350 °C has lower mean shear strength even though it has higher process temperatures. It can also be observed that the standard deviation is large for all samples. This was caused by uneven bonding as observed from the shear dies as shown in Figure 77 and with CSAM shown in Figure 78. Due to reflective surface of bottom dies, the samples were tilted in Figure 77. This were to prevent the bottom dies from shining directly into the camera which will cause underexposure of the de-bonded area. Hence the samples appear black at the bottom dies.

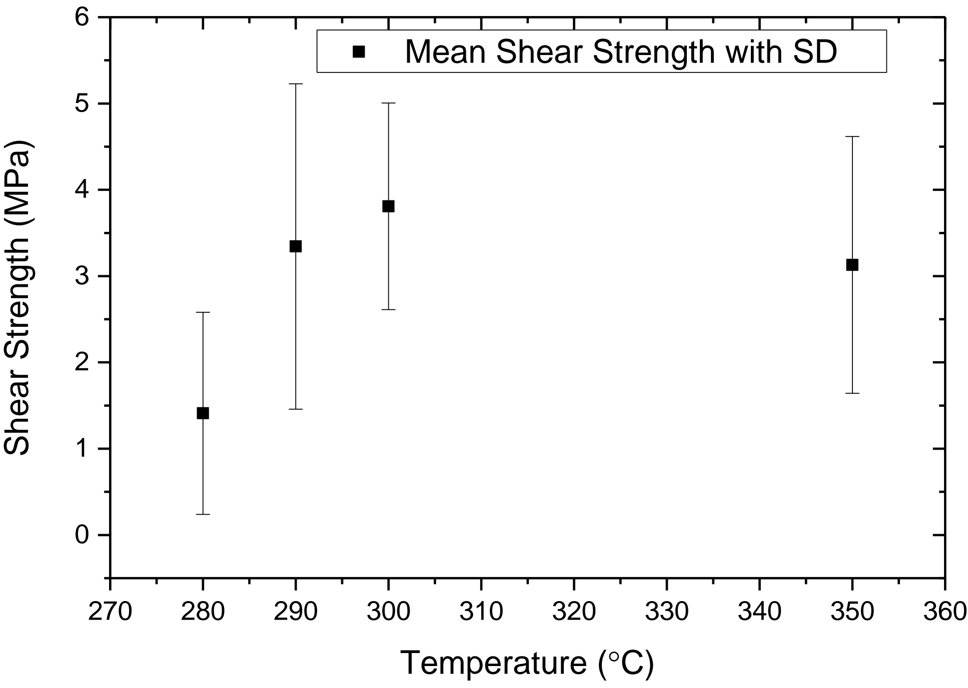

Figure 76: Shear strength of Al-Au bonded samples at different process temperatures

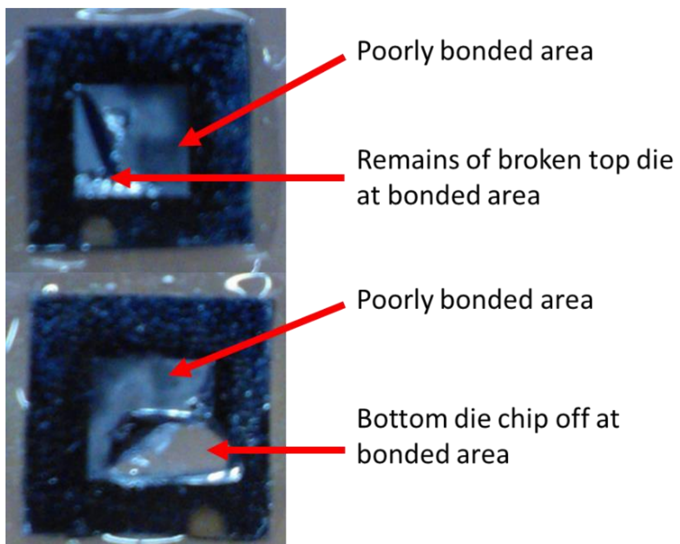

Figure 77: Examples of shear tested sample showing uneven bonding strength

Figure 78: CSAM image of 290 °C bonded samples (white: bonded areas, grey: unbonded areas)

5.3 Investigation of Elemental Composition and Microstructures of Al-Au Thermo-compression Bonds

A shear strength test sample was bonded using a bonding force of 56.4 MPa (1200N on 25 mm^2) and bonding temperature of 300 °C in a wafer bonder. Equal amount of Al and Au (150 nm) on the bonding samples were chosen for ease of characterization of the extend of diffusion. The increase of force was used to improve bond uniformity of the sample. The sample was bonded for 10 minutes and annealed at 300 °C for 1 hour in N_2 environment.

This sample was inspected with TEM and EDX. Figure 79 shows the location of observation marked by the dotted line. Figure 80 shows the TEM and HRTEM image of the Al-Au interface of the sample at the observation location. There is a crack line near the substrate on the left image. However, no distinct bonding interface is observable. This shows that the thermo-compression process can create indistinguishable bonds that potentially have mechanical

strength similar to that of the bulk intermetallic formed.

EDX line scan was performed in the location shown in Figure 81 and the result of the line scan is shown in Figure 82. It can be observed that Al and Au are evenly distributed throughout the original Au and Al layer. This shows that all the original Al and Au layers have mixed and formed intermetallics. From the EDX linescan, it can also be observed that the resultant thickness of the intermetallic layer is approximately 400 nm, a 100 nm increase from the original 300 nm (150 nm of Al and Au each).

EDX elemental mapping images of the sample are shown in Figure 83. The mapping at the crack line shows that the Al and Au were inter-diffused, suggesting that the crack occurs after the bonding.

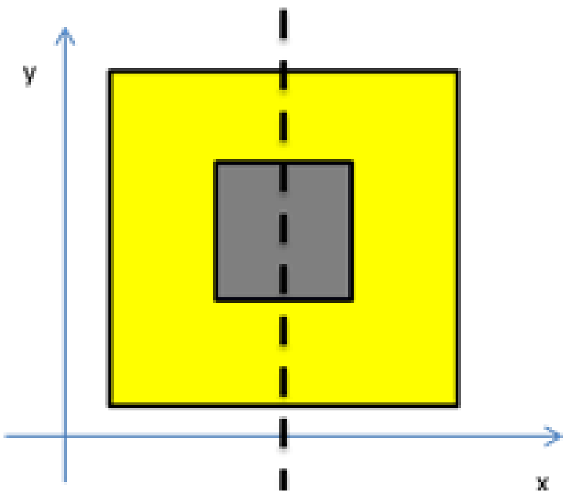

Figure 79: Location of TEM and EDX observation on the sample

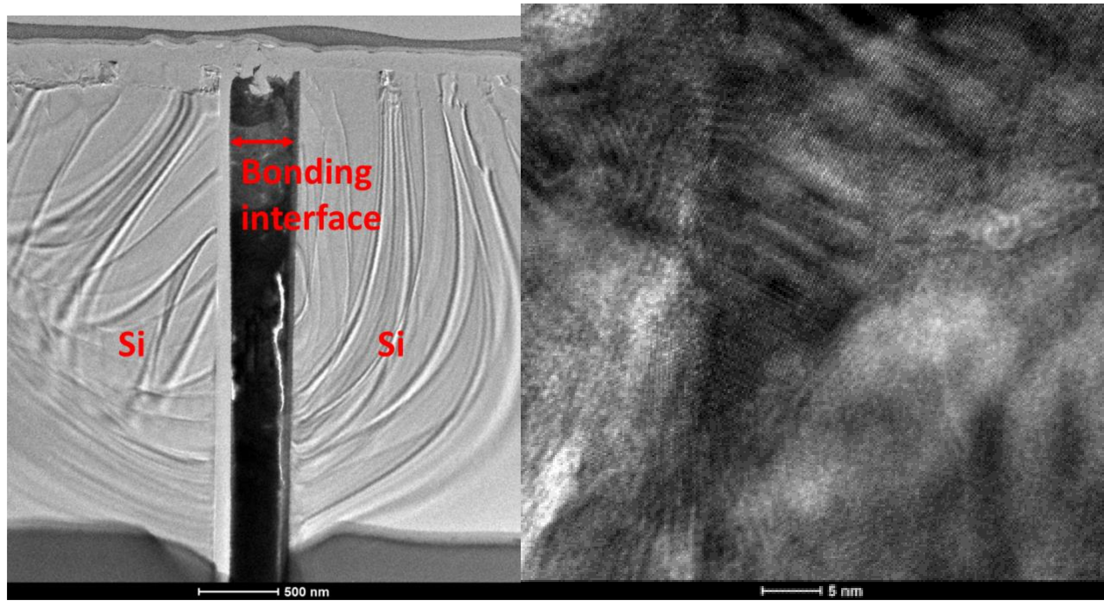

Figure 80: TEM image of Al-Au thermocompression sample on the left and HRTEM on the right

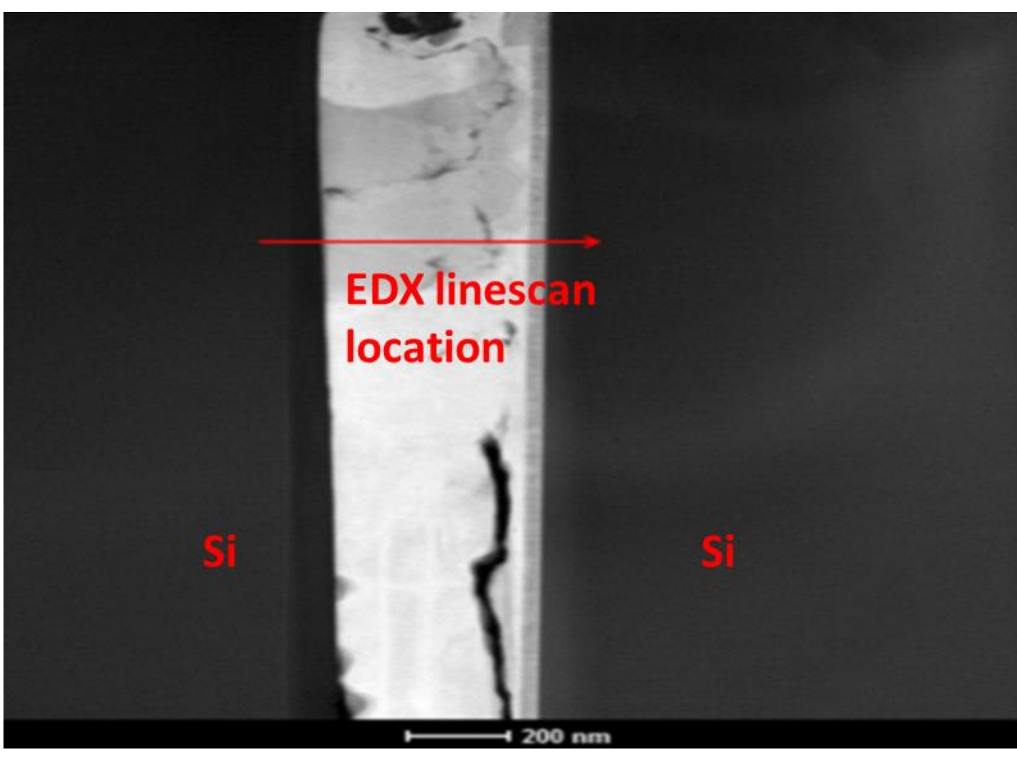

Figure 81: EDX linescan location

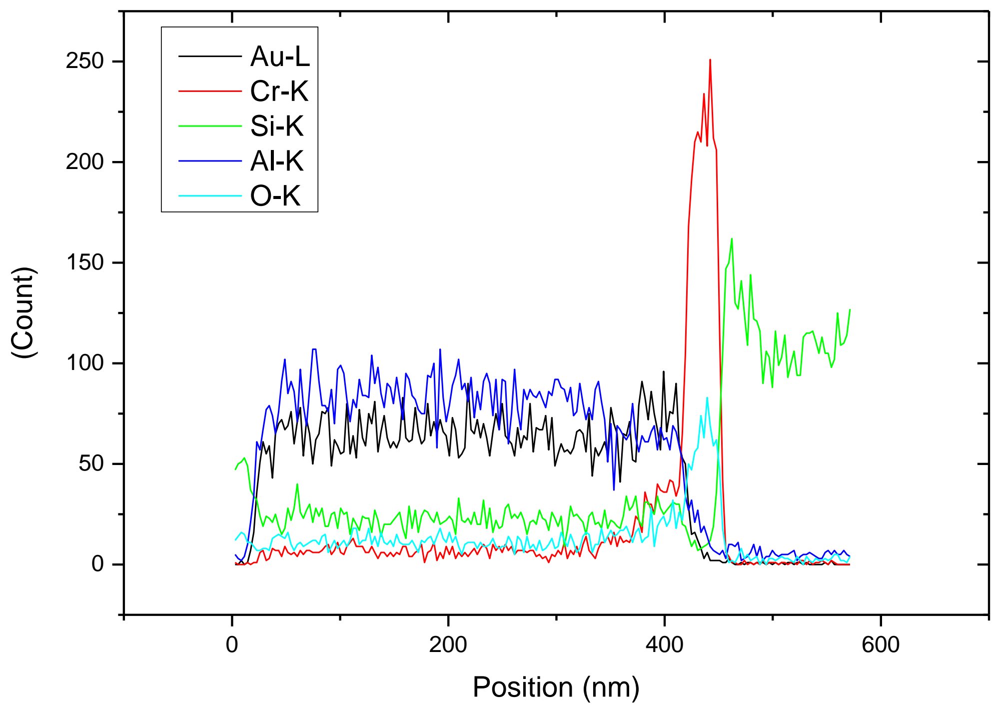

Figure 82: EDX linescan results

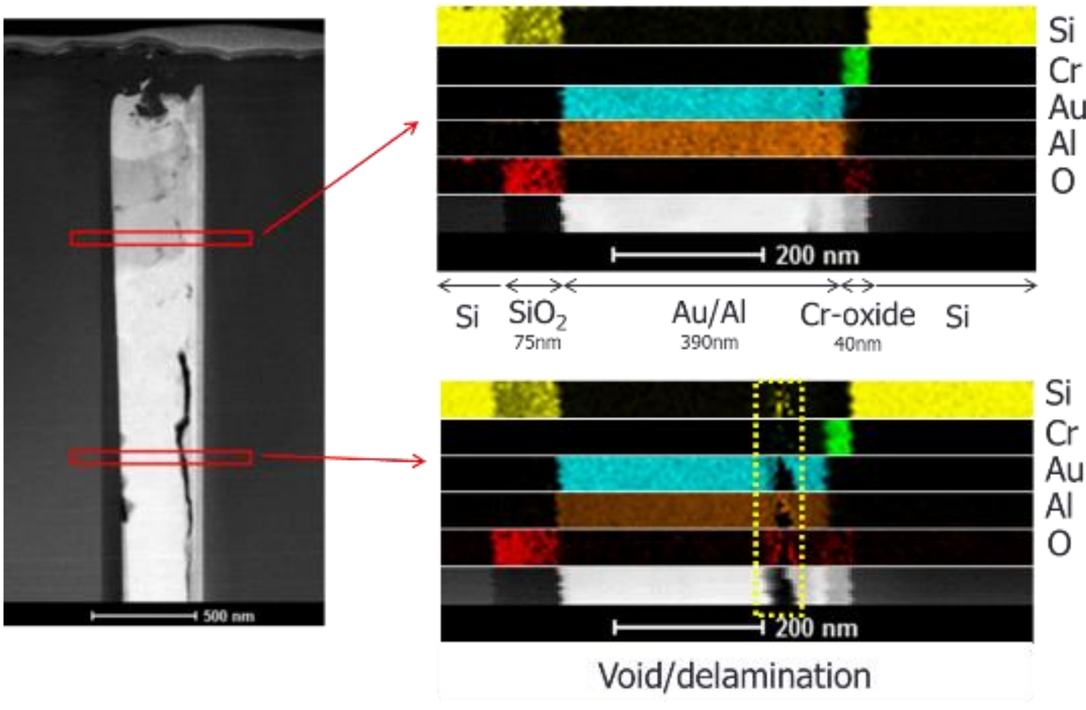

Figure 83: EDX element mapping showing the inter-diffused Al-Au and void

5.4 Hermetic Sealing Evaluation for Al-Au Thermo-compression

Hermetic sealing capability of Al-Au thermo-compression bonding is

critical for the novel method of MEMS-CMOS active hermetic cap integration. In this section, Hermetic seal test samples were fabricated and tested according to MIL-STD-883E [75].

5.4.1 Hermetic Test Sample Fabrication

Single side polished, P-type, 150 mm diameter, 675 +/- 25 μm thick, Si <100> wafers with resistivity of 0 to 100 Ω.cm were used. For the top dies, DRIE was used to form the cavities and the seal rings to a depth of 120 μm with lithography with mask design shown in Figure 84. Sealing rings are 20 μm thick with internal dimension of 4 mm by 3 mm. With a etch depth of 120 μm, the cavities form a volume of 1.4×10^{-3} cm^3. The surrounding air channel was formed to separate the sealed cavities from the dummy area and to provide a path for helium gas flow during bombing and leak test. After DRIE, the patterned wafer is deposited with 50 nm of Cr and 150 nm of Au. Dicing of the wafer is done to produce 10 mm by 10 mm sized dies with the cavity in the center.

For the bottom dies, a wafer was deposited 500 nm of SiO_2 with PECVD TEOS and sputtered to form Al layer of 150 nm. This wafer is diced into 15 mm by 15 mm dies. Figure 85 shows a schematic of the process flow for the fabrication of the hermetic seal dies and subsequent bonding die placement.

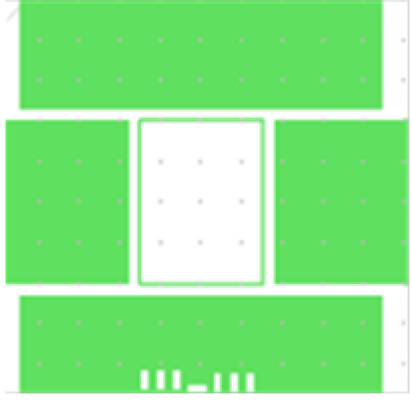

Figure 84: Seal cavity mask design for DRIE for hermetic test dies

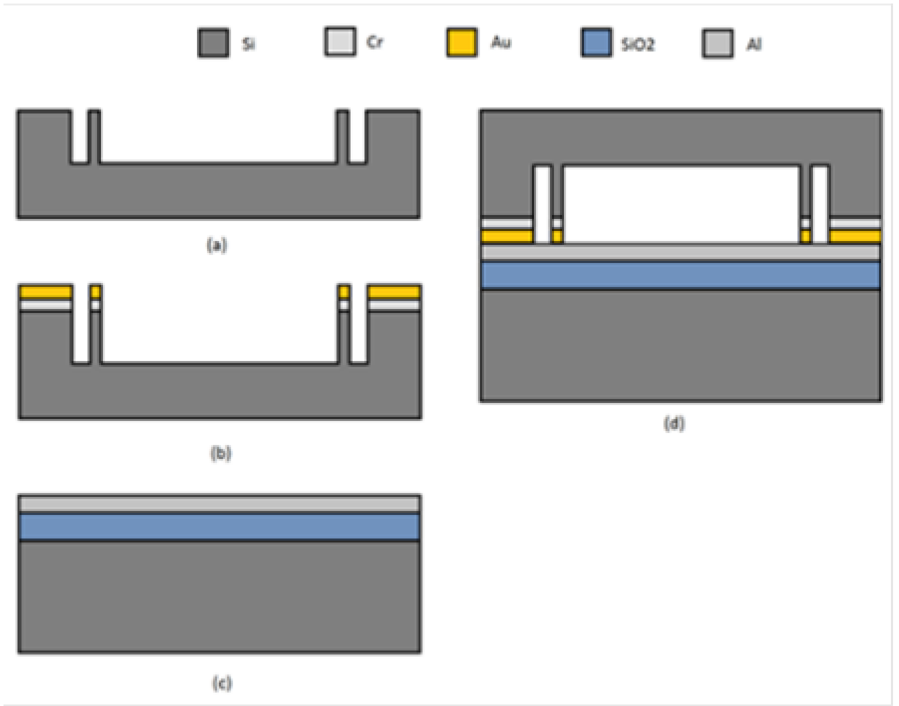

Figure 85: Schematics of the formation of sealed cavity for helium leak rate detection: (a) forming of cavities, seal rings and air channel using DRIE etching; (b) sequential deposition of Cr layer and Au bonding layer in DRIE wafer; (c) deposition of SiO2 isolation and Al bonding layer on capping wafer; (d) dicing of wafer into dies and Au-Al thermo-compression bonding of the cavity die to the capping die.

5.4.2 Hermetic Test Sample Bonding

The samples were bonded in a wafer bonder at 300 °C for 10 min with 28.6 MPa (2100 N on 73.5 mm^2 bonding area) force applied. Post-bonding annealing were performed at 300 °C for 1 h in N_2 environment.

5.4.3 Hermetic Test Results and Discussions

Fine and gross leak tests similar to Cu-Cu fusion bonding were performed. Only samples with complete bonding of the sealing ring observed by CSAM were tested (example shown in Figure 86). Figure 87 shows a poorly bonded sample with different shades in the cavity. Black and dark grey are present in the cavity area showing that water (dark grey) from the CSAM have entered the cavity. The acoustic wave of CSAM is lost when passing through air, hence no signal will be detected, thus showing black in the scanned image. Sealing rings that kept the water out will shows distinct black rectangles. The leak rates for the samples are less than the rejection limit (5×10^{-8} atm-cc/s) stated in the

MILSTD-883E standard with a mean leak rate of 2.7×10^{-8} atm-cc/s. These samples have also passed the bubble test. The mean fine leak test results of 2.7×10^{-8} atm-cc/s are comparable to that of 300 °C annealed Cu-Cu fusion bonded samples mean leak rate of 2.4×10^{-8} atm-cc/s. However, 250 °C annealed Cu-Cu fusion bonded samples performed better at mean leak rate of 8.78×10^{-9} atm-cc/s.

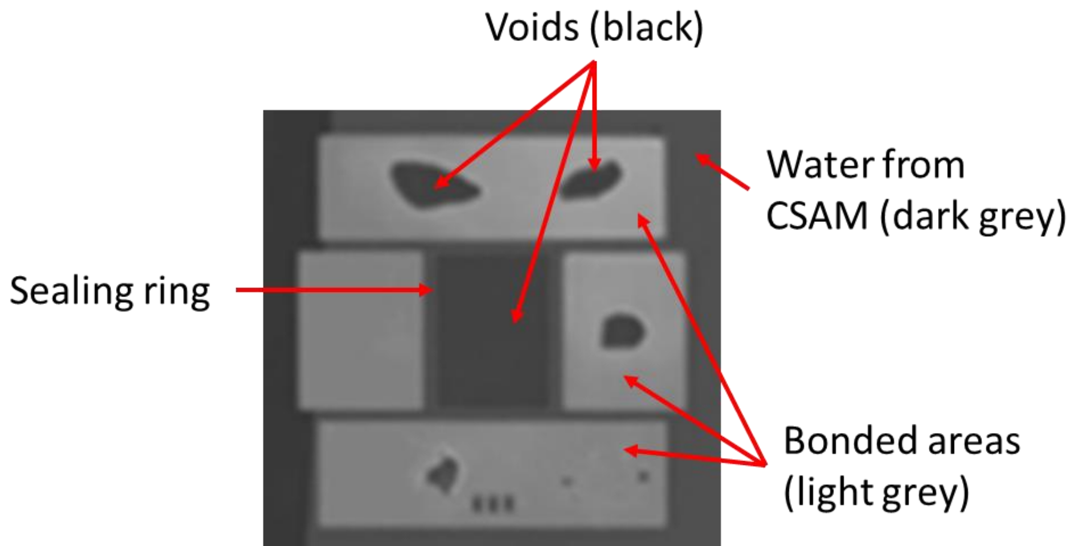

Figure 86: CSAM of good bonded sealing ring samples with black rectangle in the center

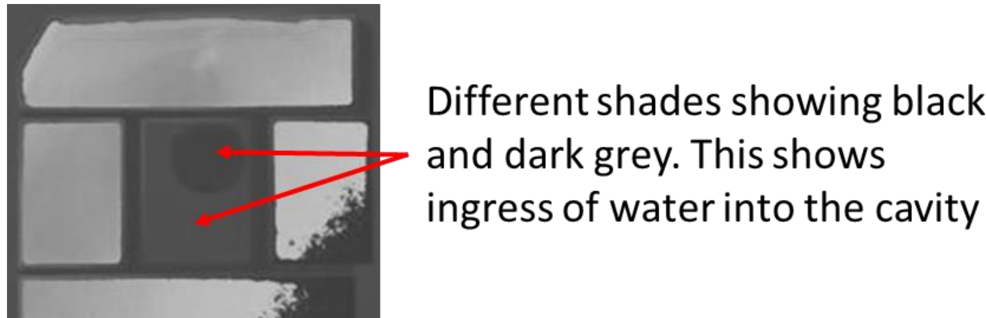

Figure 87: CSAM of poorly bonded sealing sample with water (dark grey) and air bubble (black) in cavity

5.5 MEMS-CMOS active cap integration

In this thesis, a single axis silicon-on-insulator (SOI) capacitive accelerometer is integrated with a CMOS die that provide the modulation and readout of the MEMS sensing results. The circuit for MEMS readout comprises of a low noise, band-pass gain stage, a fully differential synchronous demodulator and an off-chip, low-pass filter. The block diagram for the readout

circuit is shown in Figure 88. The readout circuit CMOS was fabricated through a multi-project wafer (MPW) with 0.35µm, two-poly four-metal (2P4M) process. The low-pass filter was implemented off-chip in the final design to save on-chip space. Figure 89 shows the key components of the last layer metal (Al) on the CMOS die which include the seal ring, mechanical support and alignment marks to assist the MEMS-CMOS bonding. These components were essential for the novel MEMS-CMOS active hermetic cap integration. Additionally, special request was made to recess the final passivation layer to create a stand-off gap for the metal pads to facilitate thermo-compression bonding as shown in Figure 90.

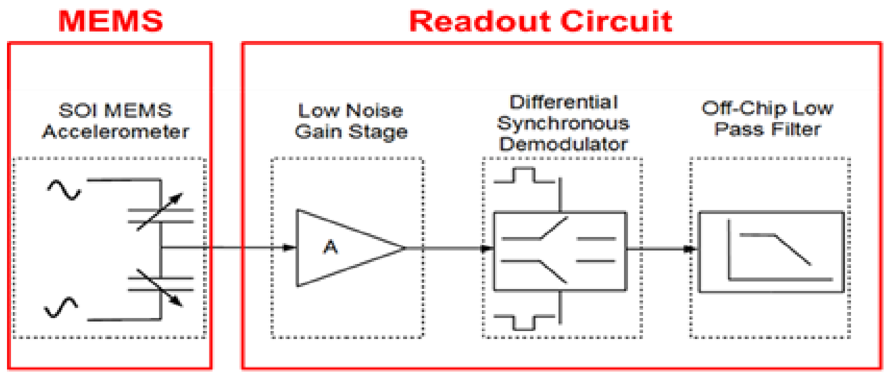

Figure 88: System block diagram for the readout circuit.

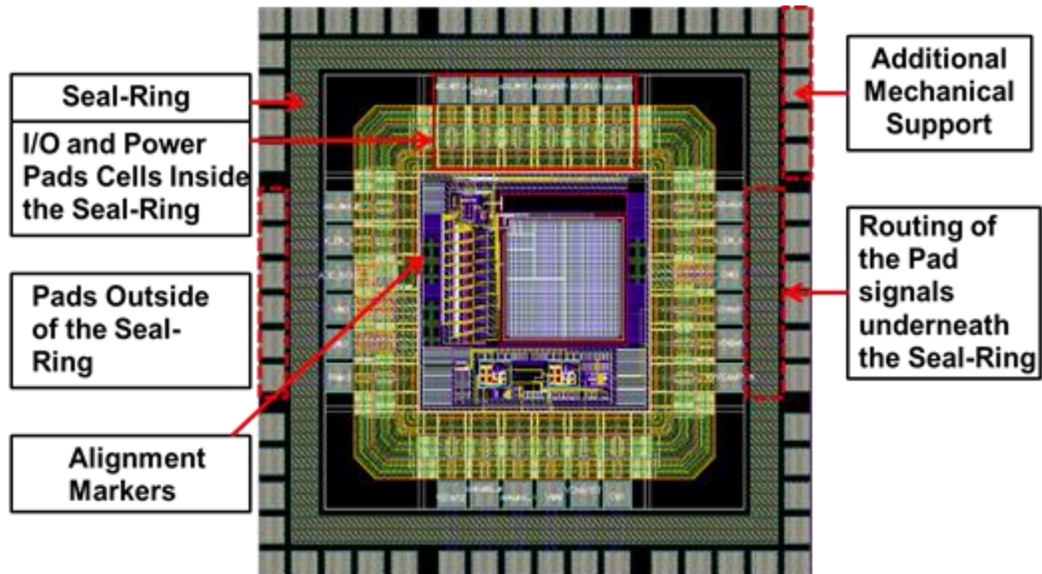

Figure 89: Die Micrograph of the readout circuit fabricated through MPW (0.35µm, 2P4M process)

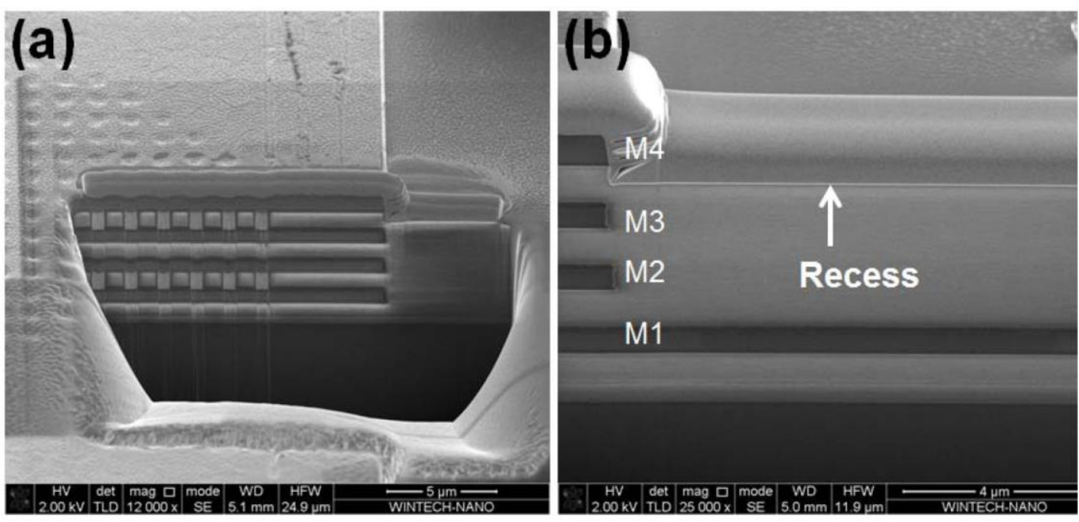

Figure 90: (a) FIB/SEM image showing the on-chip metal layers in the CMOS chip, b) recessed passivation layer to create stand-off gap for the bonding of metal pads.

5.5.1 MEMS Fabrication

SOI MEMS single axis accelerometer dies were fabricated to match the sealing ring, input/output and mechanical support pads of the CMOS dies. A capacitive MEMS accelerometer, with sensitivity of approximately 4.88fF/g is designed to fabricate from 150 mm SOI wafer with specifications shown in Table 6. Negative resist was spin coated onto the wafer and patterned with the metal pads and sealing ring design. 50 nm Cr and 150 nm Au were deposited with EBPVD and subsequently lifted-off. Next, DRIE was used to etch the Si device layer to form the accelerometer with lithography. Lastly, HF was used to etch the oxide layer releasing the accelerometer. Liquid CO_2 at its triple point was used to dry the MEMS to prevent the floating structure from adhering to the handle layer. Figure 91 shows the SEM image of the fabricated MEMS accelerometer.

Device layer	
Orientation	<100>
Doping	N/Phosphorus
Resistivity	0.001 - 0.002 ohm/cm
Thickness	20 µm +/- 0.5 µm
Finish	Polished
Oxide layer	
Thickness	1 µm +/- 5%
Handle layer	
Doping	N/Phosphorus
Resistivity	1 - 20 ohm-cm
Thickness	600 µm +/- 10 µm

Table 6 : SOI wafer specifications

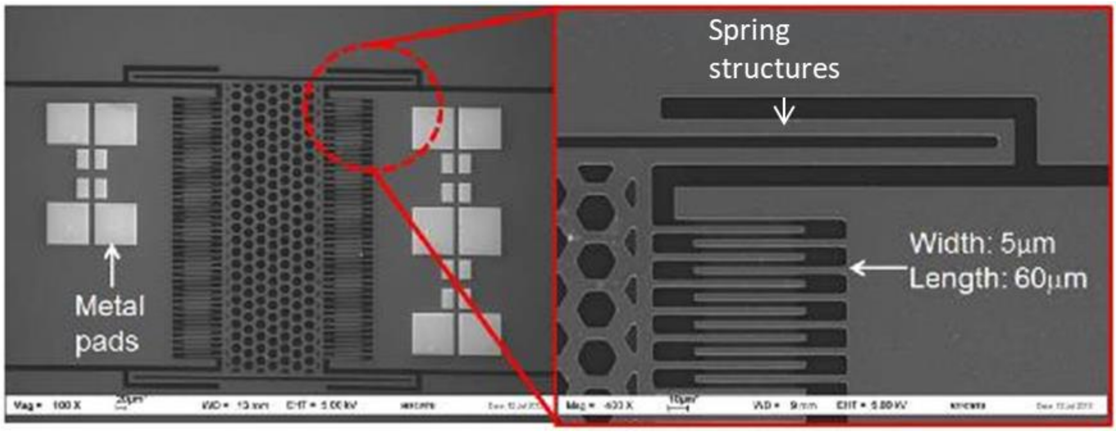

Figure 91: SEM image of fabricated MEMS die showing the metal pads, DRIE etched comb structures that that provides the capacitive sensing and spring structures that allows movement in one axis

5.5.2 Integration of MEMS-CMOS with Al-Au thermo-compression

Al-Au thermo-compression were performed on the dies with a die bonder as shown in Figure 92. Bonding temperature was 300 °C for 10 min with 50 MPa (50 N force applied on 1 mm^2). Annealing was performed at 300 °C for 1

h. The surrounding of the bonding was constantly purged with N_2. Cavity of the MEMS will be filled with mostly atmospheric pressure N_2. The vertically stacked CMOS and MEMS chip has a thickness of 1155μm. The integrated device was packaged inside 44-pin J-leaded ceramic package for electrical testing as shown in Figure 93.

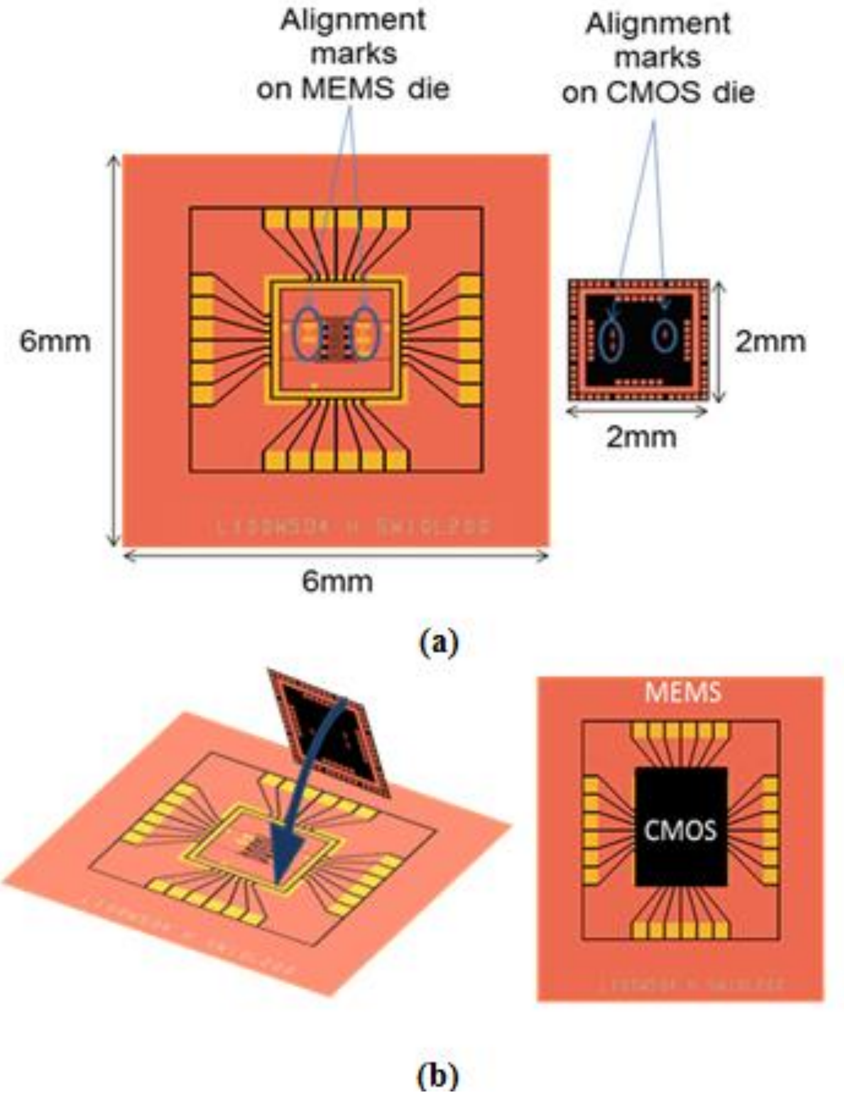

Figure 92: Schematic showing the face to face placement for bonding

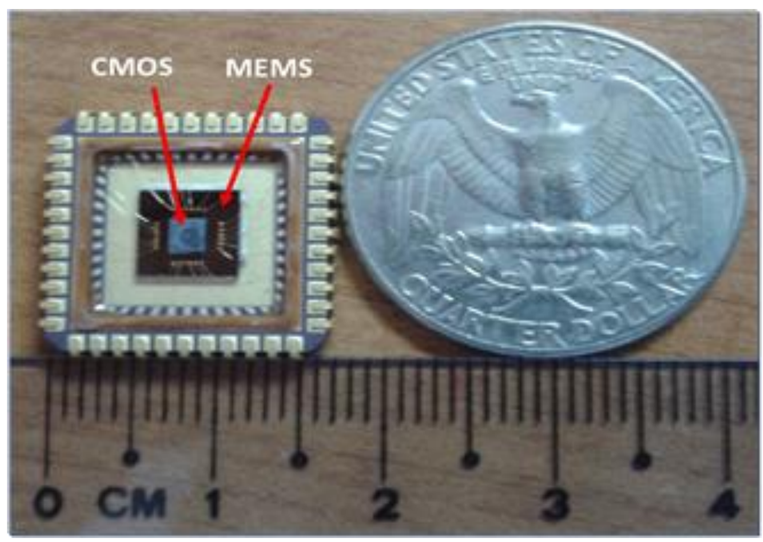

Figure 93: Integrated device packaged in a 44-pin J-leaded ceramic package with a U.S. quarter and ruler as size comparison

5.5.3 Shock test

Accelerometers are usually used in mobile phones which are subjected to accidental drops. Hence the integration method used will be required to withstand those accidental drops and the device should continue to function. Shock test was performed on the packaged samples. The J-leaded ceramic packaged sample was subjected to shock test prescribed in JESD22-B104C (500g, 1ms, 10 cycles) to ensure its reliability [77]. The packaged sample was clamp in place with a jig which will be dropped at a precise height. The setup of the shock test is shown in Figure 94. Upon impact, 500g of acceleration will be experience by the sample as recorded by an external sensor shown in Figure 95.

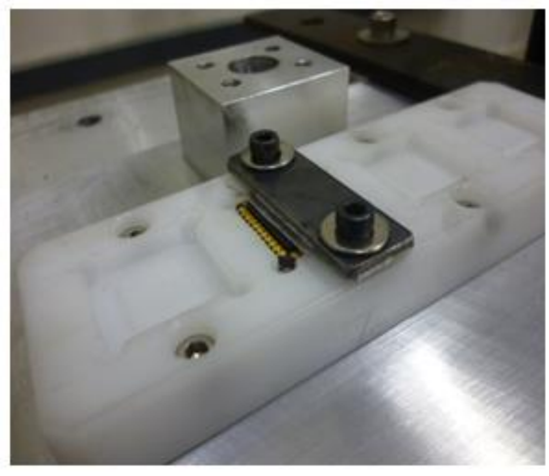
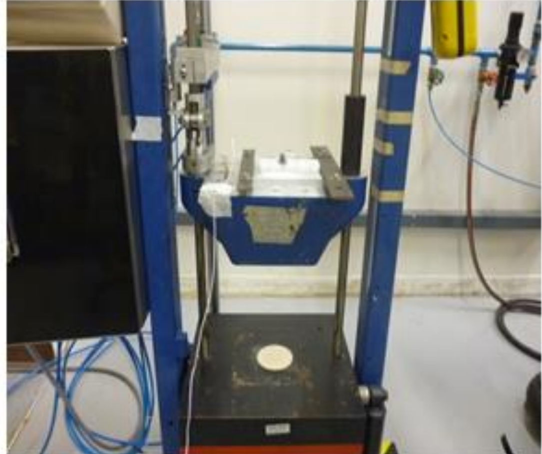

Figure 94: Picture of the package in the shock test setup

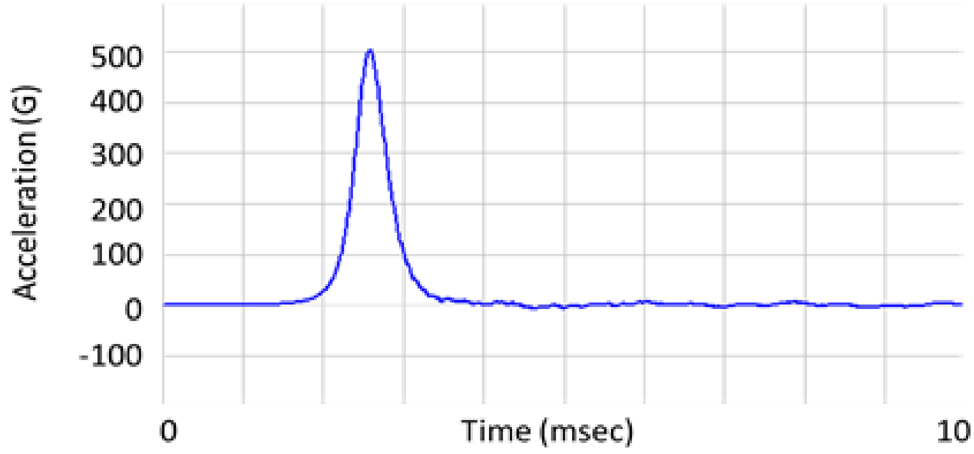

Figure 95: Acceleration experienced by the sample in G

After the mechanical shock test, the sample was excited by 1Vpp, 50kHz differential sinusoids for operation check. The variation in the peak to- peak amplitude of the gain stage output with respect to an excitation carrier is observed as the chip is flipped between -1 g and +1 g orientations as shown in Figure 96. The amplitude of the gain stage output grows in-phase and anti-phase in respect to the input carrier signal in positive g and negative g flip directions, respectively, which suggests that the bonded chip is working as desired. The maximum amplitude (pp) observed in the two flip directions is an indication of the symmetrical behavior of the accelerometer. The mean value of one of the differential rectified sinusoids at the demodulator output is recorded within the measurement range -1 g to +1 g at various carrier frequencies and plotted in Figure 97.

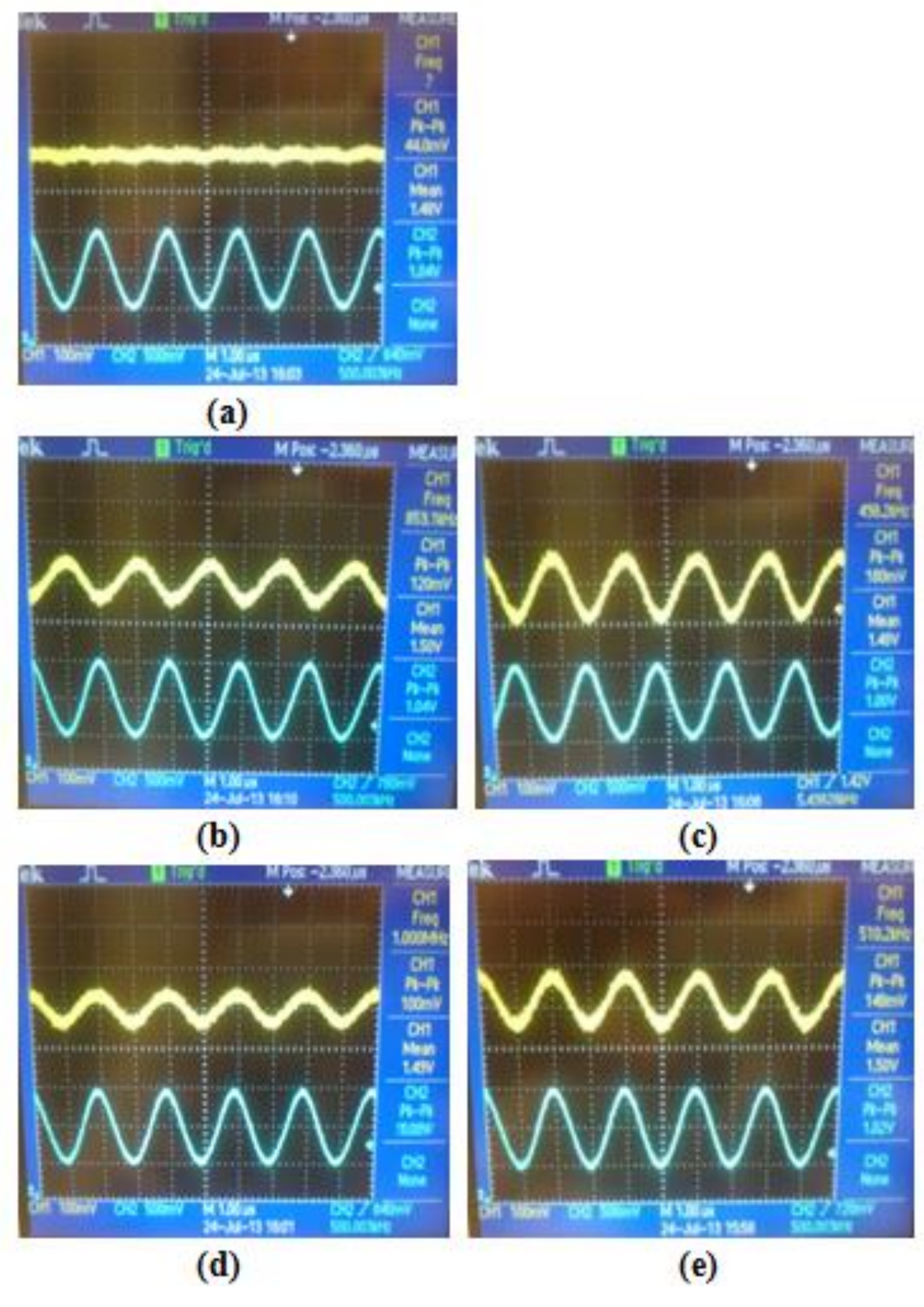

Figure 96: The gain stage output in yellow (grid division of 100 mV) and carrier input in blue (grid division of 500 mV), orientation of the sample at (a) 0g, (b) -0.707g, (c) -1g, (d) +0.707g and (e) +1g orientation

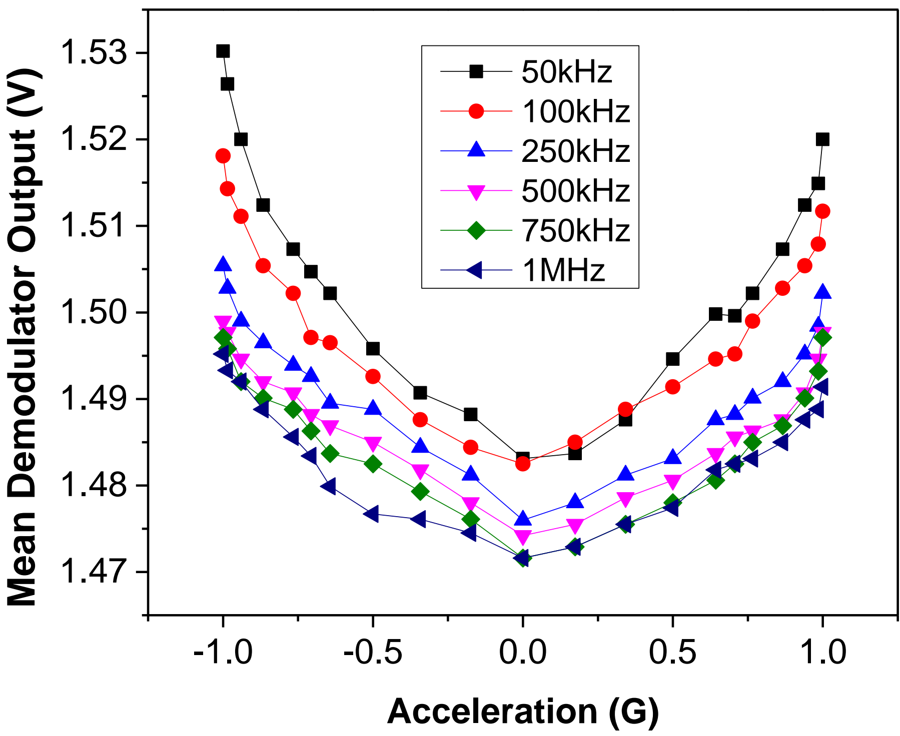

Figure 97: Variation in the mean demodulator output with g at various carrier frequencies for the bonded chip

5.6 Summary

In this chapter, shear strength and hermetic sealing investigation were performed on Al-Au thermo-compression bonding. The SOI single axis accelerometer with matching I/O pads with the MPW CMOS die was fabricated. The novel active cap CMOS-MEMS integration have been demonstrated with Al-Au thermo-compression bonding with the fabricated MEMS die. The stacked chip has thickness of 1155µm and underwent mechanical shock test for reliability test which the samples have passed.

Chapter 6 **Conclusion and Future Work**

6.1 Conclusion

To conclude, Cu-Cu fusion bonding with plasma pre-treatment for 3D integration or packaging has been proposed and carried out in this thesis. A novel active cap MEMS-CMOS 3D integration was also demonstrated with studies on the Al-Au thermo-compression bonds.

Firstly, plasma effect on bonding surface were investigated with XPS. Different variation of duration and gas composition of Ar + N_2 plasma were investigated for their effect on Cu surface elemental composition. The XPS results concur that the passivation plasma was able to form Cu_3N compound. The Cu_3N compound increases as duration of pre-treatment increased, however the increase of ratio of N_2 gas to Ar gas did not produce significant increase in Cu_3N compound. Copper oxides were also observed to decrease with increase with treatment duration.

Hydrophilicity and surface roughness of treated surface were measured. Unfortunately, Type 2 plasma pre-treatment, which have lower copper oxides from the surface study, was unable to create a hydrophilic surface. Hence, it was decided that a Type 1 plasma pre-treatment was to be used for the Cu-Cu fusion bonding subsequently. AFM showed that Type 1 pre-treatment was able to reduce surface roughness of as-deposited Cu potentially improving the bond quality.

Blanket wafer Cu-Cu fusion bonding was demonstrated with plasma pre-treatment without passivation and pre-treatment type 1. Microstructure studies were performed on the bonded samples at their bonding interface before and after temperature cycling test. No delamination or oxidation were observed of all samples. N was not observed in TEM/EES showing that the Cu_3N compound has decomposed. Zig-zag bonding interface was observed for sample with pre-treatment type 1, which was not observed for sample bonded with pre-treatment without passivation. Hence sample with pre-treatment type 1 potentially have better bond properties compared to the sample bonded with pre-treatment

without passivation.

Shear strength test has been performed on sample pre-treated with and without passivation. Additionally, in the fabrication process, dummy dies without plasma pre-treatment were bonded with similar process but failed proving that the pre-treatment is essential in the Cu-Cu fusion bonding. Although the previous chapter had shown better bonding interface for the pre-treatment with passivation (zig-zag interface), the shear strength test was unable to differentiate them. This was due to the failure interface at the Ti adhesion layer. Different annealing temperatures were also investigated on the effect of the shear strength and hermetic sealing which according to the diffusion equation, should be better with higher temperature. However, it was not the case, possibility be due to the failure at the Ti adhesion layer.

The exposed Cu surface with pre-treatment was also discovered to show high oxidation during TCT for the daisy chain samples. Hence passivation is required to protect the exposed Cu to prevent oxidation. The Cu-Cu fusion bonding from pre-treatment with passivation did not fail after the TCT. CBKR structures showed that the dies were able to be uniformly bonded with the Cu-Cu fusion bonding method.

This concluded the work on Cu-Cu fusion bonding with plasma pre-treatment. Plasma pre-treatment with passivation showed potential for 3D integration. It has high throughput capability (wafer to wafer bonding) with pre-bond time of 5 min and allows batch annealing, potentially high reliability due to no intermetallic, ease of adaption with commonly used materials, dry processes and no requirement of specialized equipment (ultra-high vacuum or special gases) for the bonding. Bond strength of 20.3 MPa was achieved with pre-treatment with passivation and post-annealing temperature of 290 °C for 2h. Hermetic sealings of multiple samples with He leak rate below the required 5×10^{-8} atm.cc/s were achieved. Daisy chain bonds did not fail after 1000 cycles TCT.

On Al-Au thermo-compression bonding, shear strength and hermetic sealing were investigated. Al and Au were shown to be completely inter-diffused. The SOI single axis accelerometer with matching I/O pads and sealing ring

design as the MPW CMOS die was fabricated. The novel CMOS-MEMS integration has been demonstrated with Al-Au thermo-compression bonding using the fabricated MEMS die. The stacked chip has thickness of 1155μm and underwent mechanical shock test for reliability test which the samples have passed.

6.2 Future work

Beyond the scope of this study, the following recommendations are suggested for future work:

Thorough study in plasma effects

More types of plasma gases, duration and power should be investigated to create a better plasma pre-treatment recipe resulting in a good compromise between passivation and hydrophilicity for Cu-Cu fusion bonding.

Better microstructure and elemental composition study

Due to the thin layer of Cu_xN_y formed, it is difficult to properly characterize the layer. Further study on the passivation effects of the Cu_xN will also be needed to understand how it reduce oxidation in the annealing process. Grain structures before and after plasma treatment should be investigated to understand and if possible, prevent the high increase in resistance when the sample underwent TCT.

Wafer to wafer level bonding with TSV and active devices

Cu-Cu fusion bonding shows high potential in wafer to wafer bonding. Wafer to wafer level bonding with TSV should be demonstrated to entice industry adaption of the bonding technology. With EUV lithography being available, devices will continue to scale, increasing the need for small pitch interconnects.

Fine pitch interconnect demonstration

Various studies on solid state bonding have demonstrated fine pitch (6 to 10 μm pitch) of interconnects bonding. Since Cu-Cu fusion bonding is also solid state bonding, it should be able to achieve fine pitch bonding of interconnects. Fine pitch bonding should be demonstrated with Cu-Cu fusion bonding.

Thermal study on Cu-Cu fusion bonding

Since Cu has good thermal conductivity, additional dummy pads can be fabricated on a device and bonded to increase heat dissipation. The effects of additional pads on thermal dissipation could be studied.

Integration of power source and antenna of novel 3D integrated device

The novel 3D CMOS-MEMS device should be further integrated with source and antenna to allow remote operation and communication. This will further demonstrate as an integration technology for an IoT.

Publications

Journal Papers:

[1] “Cu-Cu Bonding in Ambient Environment ArN2 Plasma Surface Activation and Its Characterization”, IEEE Transactions on Components, Packaging and Manufacturing Technology, Preprint, Oct 2018, DOI: 10.1109/TCPMT.2018.2875460

Conference Papers:

[1] “TSV-less 3D stacking of MEMS and CMOS via low temperature Al-Au direct bonding with simultaneous formation of hermetic seal”, Electronic Components and Technology Conference, Orlando, USA, May 27-30, 2014

[2] “3D CMOS-MEMS Stacking with TSV-less and Face-to-Face Direct Metal Bonding”, VLSI Technology, Honolulu, USA, June 9-12, 2014

[3] “Direct copper-copper wafer bonding with Ar/N2 plasma activation”, Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 1-4, 2015

[4] “Cu-Cu Die to Die Surface Activated Bonding in Atmospheric Environment Using Ar and Ar/N2 Plasma”, Pacific Rim Meeting on Electrochemical and Solid-State Science, Hawaii, USA, October 2-7, 2016

[5] “Process Development and Reliability Study on Ar/N2 Plasma Activated Cu- Cu Wafer-Level Bonding”, The International Conference on Wafer Bonding – WaferBond’19, Halle/Saale, Germany, December 2- 4, 2019

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