A 40 GHz CMOS PLL With −75-dBc Reference Spur and 121.9-fs_{rms} Jitter Featuring a Quadrature Sampling Phase-Frequency Detector

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***Abstract*—The high phase noise of CMOS millimeter-wave oscillators has encouraged the adoption of wide loop bandwidth for an integer-*N* phase-locked loop (PLL). This paper proposes a quadrature sampling phase-frequency detector (QS-PFD) to disengage the trade-off between spur rejection and loop bandwidth. With the introduction of an auxiliary path for phase detection, the spur generated by the main path is canceled without incurring extra power or degrading the loop stability. The high gain of the QS-PFD attenuates its jitter contribution to the loop. The QS-PFD enables fast frequency detection as well as lock detection. Implemented in 40 nm CMOS technology, the proposed PLL shows a −75 dBc reference spur, –101.5 dBc/Hz phase noise at 1 MHz offset, and a minimum integrated jitter of 121.9 fs_{rms} (10 k – 100 MHz) at 38.2 GHz, with a division ratio of 128. The lock detection time is at the microsecond level. The proposed PLL consumes 23.6 mW from a 1.1-V power supply, leading to a figure of merit (FoM) of −245 dB.**

***Index Terms*—CMOS PLL, phase-frequency detector, millimeter wave, reference spur, spur reduction, sampling phase detector, lock detector, integrated jitter, phase noise.**

I. Introduction

FUTURE wireless network demands have increased bandwidth and data rate to support emerging applications and big data communications. According to a recent projection by the Federal Communications Commission, a 3-GHz licensed bandwidth will be allocated to the 39-GHz band with a data rate higher than 1 GS/s. This has motivated the effort toward the development of wide bandwidth, low spurious tone, and low-noise millimeter-wave (mm-wave) circuits and systems. Among the most critical building blocks of modern mm-wave chipsets are phase-locked loops (PLLs), which generate high-frequency, stable carriers for wireless connections. The phase noise and spurious tones of mm-wave PLLs limit the network performance, reducing the achievable data rate [1]. To support modulation orders up to 64-QAM in a mobile network such as 5G, an mm-wave PLL must exhibit excellent jitter performance and minimized self- and adjacent-channel mixing, with strong attenuation of reference spurs for fulfilling stringent out-of-band emissions and minimized aliased energy.

Due to the absence of high-quality passives in an mm-wave integrated PLL, the phase noise of a voltage-controlled oscillator (VCO), which is high-pass filtered in a PLL will significantly degrade the PLL's jitter performance. The RMS phase error contribution, derived from the single-sideband phase noise S_{SSB} of the VCO evaluated at the offset Δf from the carrier and the PLL loop bandwidth (f_{BW}) is based on [2]

$$\sigma_{\phi}^{PLL} = \Delta f \sqrt{\frac{\pi \cdot S_{SSB}^{VCO}}{f_{BW}}} \tag{1}$$

suggesting the need to increase the loop bandwidth for the sufficient attenuation of the VCO noise. Although a wider loop bandwidth effectively attenuates more VCO noise, extending the PLL frequency roll-off to a higher frequency makes the PLL less effective in suppressing the reference spur, leading to a fundamental trade-off between the PLL loop bandwidth and the level of rejection to the reference spur.

In this article, a new phase-frequency detector (PFD), coined "quadrature sampling PFD (QS-PFD)" that is evolved from an *RC*-loaded exclusive-OR (XOR)-gate phase detector (PD), has been proposed to offer an additional degree of freedom in the Type-I PLL design to break the aforementioned trade-offs. Put simply, it introduces a current-reuse complementary path for phase detection such that the spur it generates neutralizes that generated by the main path in the current domain without the need for shrinking the f_{BW}. The output disturbance current due to the circuit mismatches between these two paths operates at a rate of $4f_{REF}$, and it gets further suppressed by the loop filter (LF). Consequently, a wide f_{BW} and low spur can be obtained concurrently. The proposed QS-PFD also enables fast locking.

This paper is organized as follows. Section II reviews spur reduction techniques in recent PLLs and propose the QS-PFD from the top-level description. Section III details the design of the QS-PFD at the transistor level. Millimeter-wave circuits and PLL designs are described in Section IV, and the measurement results are provided in Section V. Section VI summarizes this article.

II. Phase Detectors with Spur Reduction Techniques

The classical single loop type-I PLL is unconditionally stable and has the most potential to realize a wide f_{BW} required by high-frequency mm-wave PLLs [3]. An effective approach to suppress the reference spur is to attenuate the large ripple of the

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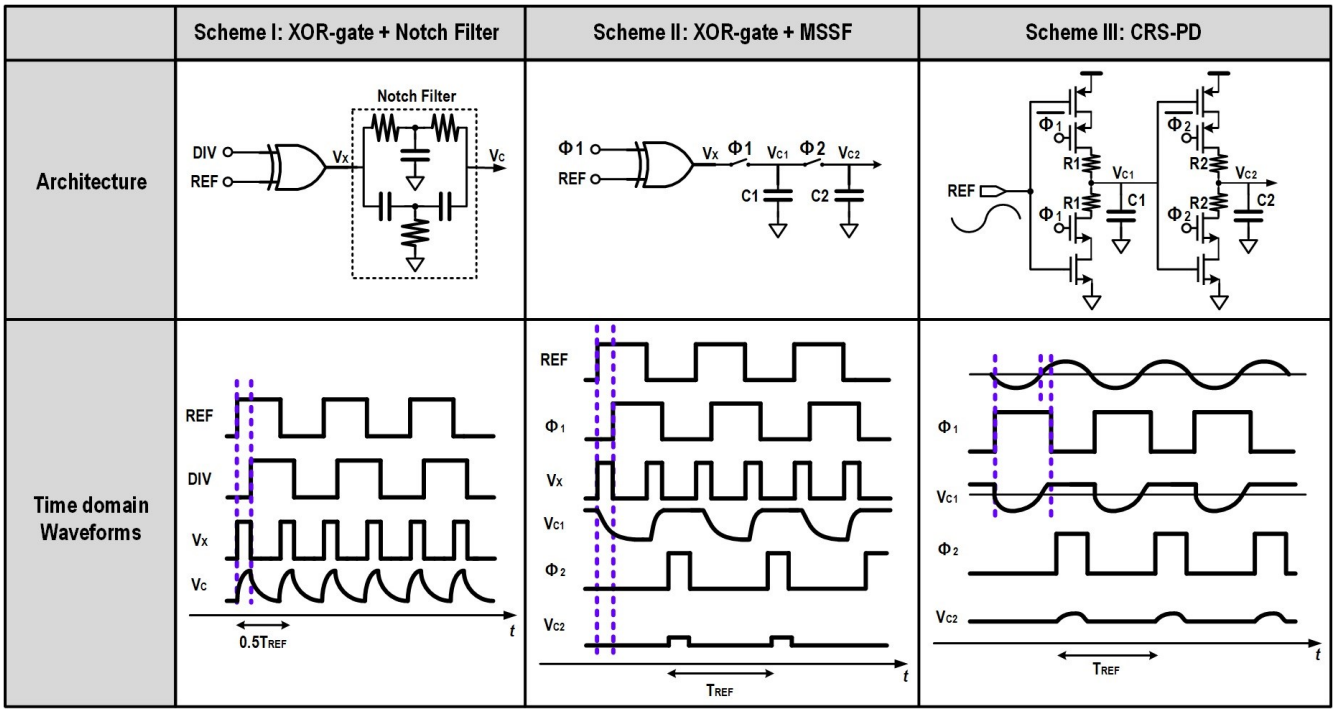

Fig. 1. Comparison of PD architectures: XOR-gate with notch filter [6] , XOR-gate with MSSF [4], and CRS-PD [7].

XOR PD output by shrinking the f_{BW}. Nevertheless, if the XOR output is heavily attenuated, the capture range is reduced and the PLL may not tend to lock. In contrast, if a wide f_{BW} of >10 MHz is assigned to allow for a wide capture range with more attenuation to the VCO noise, the spur level could be as high as the VCO output power [4].

A. Prior Arts

Traditional Type-I PLLs employing the XOR-gate PD typically have large reference spurs even when a multi-gigabit reference frequency (f_{REF}) is used. For instance, in [5], with an f_{REF} / f_{BW} > 25, the reference spur is –33 dBc. Fig.1 (left) depicts a continuous-time twin-T *RC* notch filter following the XOR-gate for spur suppression [6]. The twin-T notch filter combines a low-pass and a high-pass filter in parallel, and presents a low quality-factor band-stop notch region at the f_{REF}. Although the notch filter attenuates the spur at f_{REF} without introducing noticeable noise to the loop, it comes at the cost of degrading the loop stability with a longer settling time. The level of spur rejection improved by this notch filter is 7 dB, beyond that the phase margin is degraded. Using this twin-T notch filter, the PLL achieves a reference spur of –62.1 dBc with an f_{BW} of < 100 kHz.

The continuous-time filter can be replaced by a discrete-time counterpart, aiming to isolate the VCO from the large XOR jumps. A discrete-time filter formed by a master-slave sampling filter (MSSF) is illustrated in Fig. 1 (middle) [4]. The MSSF creates multiple notches at f_{REF} and its harmonics, relaxing the trade-off between f_{BW} and spur suppression. However, since the second switch carries large transient currents and can potentially generate high flicker noise [4], its size should be larger to prevent the in-band noise degradation, hereby resulting in large ripples on V_{C2} induced by the leakage, charge injection, and clock feedthrough. The MSSF also suffers from C2/C1-related loop bandwidth. Even with large sampling capacitors (e.g., C1 = 1 pF and C2 = 16 pF), the spur level is –47 dBc. Such a spur issue is further addressed by a subsequent harmonic traps circuit formed by *LC* equivalences. Although the resulting spur level drops from –47 dBc to –65 dBc, the harmonic traps increase the phase noise peaking by 1 dB due to their additional phase shift. Moreover, it necessitates extra off-chip calibration.

The above two approaches require a reference buffer to shape a slow-slope sinewave from an off-chip reference and deliver a square wave to the XOR-gate. A current-reuse sampling phase detector (CRS-PD) evolved from the master-slave sampling PD (MSS-PD) directly samples the sinusoidal wave from the external signal source without the need for a reference buffer [7], as shown in Fig. 1 (right). The design adopts current-reuse complementary devices in both sampling switches to cancel the clock feedthrough and charge injection, thus attenuating the ripple on the VCO control line. Using this PD, the PLL achieves a reference spur of –63.9 dBc with an f_{BW} of ~20 MHz. Nevertheless, the PD gain (K_{PD}) is proportional to the amplitude of the sinusoidal reference signal, and the PD adopts two first-order *RC* LF in both samplers for attenuating the ripple and linearizing the K_{PD}, potentially shrinks the capture range. Moreover, the conditions required for canceling the charge injection and clock feedthrough are both subject to the matching between the complementary devices, which is susceptible to process spread and temperature variations. Peaking in the phase noise near the f_{BW} can be observed as well.

Spur suppression techniques have been reported for Type-II PLLs as well. A negative feedback loop was introduced in the charge pump (CP) for developing a CP-PLL to attenuate the current mismatch between the PMOS pull-up and NMOS pull-down network [8], achieving a –61 dBc reference spur. However, a small f_{BW} of ~500 kHz (f_{REF} / f_{BW} ≈ 4560) was adopted. In [9], a spur-frequency boosting block was added in between the PFD and the CP to boost the CP's input frequency. Using this technique, the spur at f_{REF} is frequency boosted to a

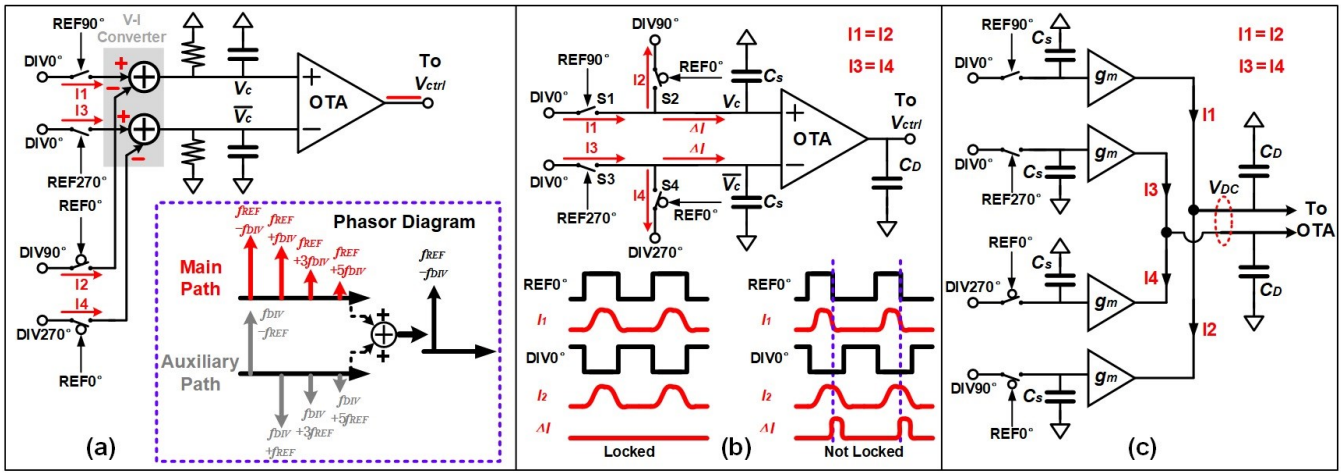

Fig. 2. Spur-canceling sampling PD architectures and the condition for spur canceling.

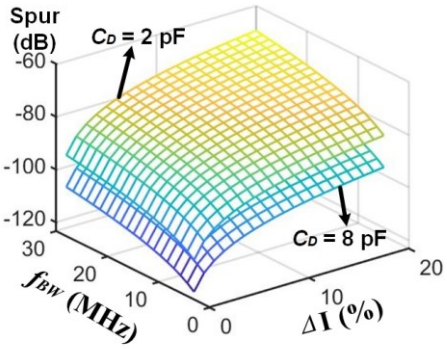

Fig. 3. Analytical reference spur against ΔI, f_{BW}, and C_D.

higher frequency at which the PLL's gain is much smaller, leading to a greater spur suppression. However, the spur-frequency boosting block may consume high power when a high-frequency reference is adopted, which is often the case with recent low-jitter PLLs for suppressing the N^2 in-band noise multiplication [5], [10], [11], where N is the PLL feedback divider ratio. Moreover, the loop bandwidth was 335 kHz for attaining < –60 dBc reference spur. A sampling PLL incorporated with a sampling phase detector (SPD) is introduced in [12]. Compared with designs utilizing a high-resolution multibit time-to-digital converter (TDC) to digitize the phase error, this design employs an SPD and keeps the signal path to avoid the quantization error associated with the TDC. Yet, since the SPD suffers from limited linear operation range, and a first-order *RC* filter is still required to attenuate the reference spur, a frequency-locked loop (FLL) is necessary to assist the phase-locking and reduce the acquisition time from hundreds of microseconds to within 5 μs. Moreover, the sample-and-hold switches are designed with thick-oxide transistors to reduce the switch ON-resistance variation over input voltage ramp, demanding their non-overlap pulse generators to be level-shifted up to 1.8 V, potentially increasing the power consumption in the reference signal path. The injection-locked PLLs [13]–[15] and subsampling PLLs (SSPLLs) [16]–[17] both demonstrate superior jitter performance, but with worse reference spurs of ~ −40 dBc.

In summary, the above PDs can suppress the reference spur with good jitter performance, but they either 1) degrade the loop's phase margin due to the introduced extra poles, or 2) incur peaking to the phase noise, or 3) have limited acquisition range and require an extra FLL to assist the phase-locking.

B. Sampling PD with Spur Canceling

The two sampling PDs (MSSF and CRS-PD) in Fig. 1 simultaneously attain wide f_{BW} and spur reduction, yet they rely on filtering to suppress the reference spurs. Since the sampling switch generates spurs at f_{REF} and its harmonics, it would be helpful to examine the polarity of each harmonic term at the sampling switch output. By applying two square-pulses each with frequency ω_1 and ω_2 to a switch, the switch time-domain output is expressed by

$$y_1(t) = \varepsilon \frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\sin\left[(2k-1)\omega_1 t\right]}{2k-1}\times\frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\cos\left[(2k-1)\omega_2 t\right]}{2k-1} \quad (2)$$
$$= \varepsilon\frac{16V_m^2}{\pi^2}\left[\frac{1}{2}\sin\left((\omega_1-\omega_2)t\right)+\frac{1}{2}\sin\left((\omega_1+\omega_2)t\right)+\bullet\bullet\right]$$

where ε is the switching loss. The output contains a near-DC term and even harmonic terms. If our goal is to eliminate the spurious tones while retaining the near-DC term, we should simply subtract a quadrature version from (2) as follows:

$$y_2(t) = \varepsilon \frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\sin\left[(2k-1)\omega_1 t\right]}{2k-1}\times\frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\cos\left[(2k-1)\omega_2 t\right]}{2k-1} -$$
$$\varepsilon\frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\cos\left[(2k-1)\omega_1 t\right]}{2k-1}\times\frac{4V_m}{\pi}\sum_{k=1}^{\infty}\frac{\sin\left[(2k-1)\omega_2 t\right]}{2k-1} = \varepsilon\frac{16V_m^2}{\pi^2}\times \quad (3)$$
$$\left[\sin\left((\omega_1-\omega_2)t\right)+\frac{1}{3}\sin\left((\omega_1+3\omega_2)t\right)-\frac{1}{3}\sin\left((\omega_2+3\omega_1)t\right)+\bullet\bullet\right]$$

Obviously, the second harmonics is perfectly canceled, leaving the near-DC term. Other terms such as the fourth harmonics are negligible as they too are either canceled out or heavily attenuated by the LF. It should be noted that adding the quadrature version would not impede PLL loop convergence since the near-DC term $\sin[(\omega_1-\omega_2)t]$ still drives the loop to lock by eliminating the frequency error $\Delta\omega = |\omega_1-\omega_2|$ through the negative feedback of the loop.

The aforementioned observation promotes the spur-canceling technique enabled by a sampling PD as shown in Fig. 2(a). The PD is composed of two pairs of switches where the input REF0º, REF90º, etc. denote the quadrature reference

signals, and DIV0º, DIV90º, etc. denote the quadrature divider output. The operational transconductance amplifier (OTA) converts the near-DC output voltage to the current and drives the VCO control line. The PD operates in such a way that the spur generated by one pair of the switch will be canceled out by the other at the OTA input. In this example, REF0º and DIV180º have are in phase. Consequently, these two signals produce the in-phase spurs at the OTA input, and the OTA generates an output current to be free of any ripple if full symmetry is assumed. The phasor diagram of this canceling process is illustrated in Fig. 2(a). As shown, only the near-DC term is distilled. When locked, $f_{REF} = f_{DIV}$; thus, all spurious tones are canceled.

This canceling of spurs can be recognized from another perspective. As the quadrature replica incurs consecutive glitches whose phase is also 90º concerning the main path, the OTA eventually produces glitches that are four times on the VCO control line in one reference cycle. In that sense, the reference spur undergoes a frequency-boosting from $2f_{REF}$ to 4 f_{REF}, eliminating the spur at $2f_{REF}$ and suffering from stronger attenuation due to the LF like [9]. Nonetheless, this approach is much simpler, and the power consumption is low. It must be noted that adding the auxiliary path for spur-canceling does not affect the loop stability as no extra poles are introduced.

Nevertheless, such a spur-canceling PD requires two pairs of switches in parallel, thereby doubling the power consumption. Moreover, the loading resistor contributes nonnegligible noise to the loop. This scheme is evolved to what is shown in Fig. 2(b), where two pairs of switches are utilized but without doubling the power consumption. The idea here is that the glitch current generated by the main path is bypassed through the auxiliary path, i.e., $I_1 = I_2$ at lock state. The PD gain is not reduced by the bypassing paths since $I_1 \neq I_2$ during the phase alignment, and the net current $\Delta I = |I_1 - I_2|$ charges the sampling capacitor C_s and allows the OTA to inject proportional current to the LF. The timing diagram of the spur canceling is illustrated in Fig. 2(b). As shown, the spur current generated through switch S1 is bypassed by switch S2, nulling the spur. In the presence of circuit mismatches, such that $I_1 \neq I_2$ at lock state, the sampling PD will create a constant phase shift between the reference signal and the divider output, neutralizing the charge at C_s. The nonoverlap generator in [4], [7], and [12] is not necessary here since the spur reduction relies on mutual canceling instead of the master-slave sampling operation.

In practice, spur canceling operates in the current domain. A practical implementation of Fig. 2(b) is represented in Fig. 2(c), where the g_m-cell (i.e. V-I converter) in each path converts the respective sampling voltage on C_s to current. Similarly, the glitch produced by the main path (I1 and I3) is canceled out by the auxiliary path (I2 and I4) since they both generate the in-phase glitch.

The PLL spur can be evaluated against ΔV_{ctrl} as follows, where ΔV_{ctrl} is the voltage disturbance on the VCO control line [6].

$$\mathrm{Spur}_{\mathrm{PLL}} = 20\log\left(\frac{K_{VCO}\times\Delta V_{ctrl}}{2\pi\times f_{REF}}\right) \tag{4}$$

If there is a current mismatch between the two paths, the unbalanced current ΔI degrades the spur canceling as illustrated in Fig. 3. While a smaller f_{BW} attenuates the spur arising from the mismatch, as expected, using a larger capacitance C_D at the load of PD also helps reduce the reference spur with a negligible impact on f_{BW}.

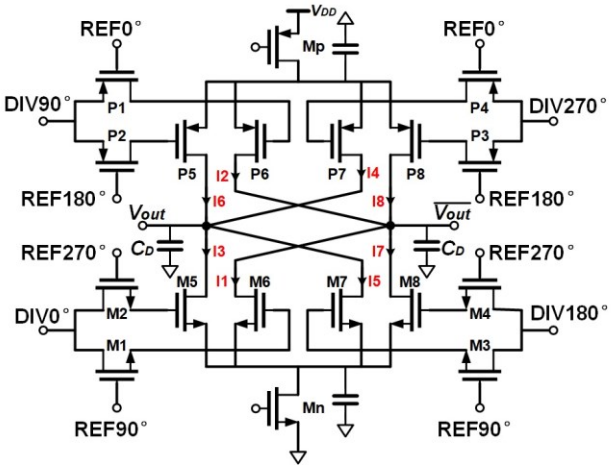

Fig. 4. Proposed QSPD.

At first glance, the topology in Fig. 2(c) seems to double the power consumption. However, as will be described in the next Section, the auxiliary path reuses the current from the main path and, thus, does not consume extra power.

III. Proposed QS-PFD

A. Topology

A quadrature sampling PD (QSPD) has been proposed for spur canceling as depicted in Fig. 4. Transistors P1–P4 are differential switches. Once a switch is turned on by the reference, the switch output follows the divider output, and drives the subsequent V-I converter (P5–P8) to conduct current to charge the output capacitor C_D. When the switch is turned off, the instantaneous voltage of the divider output is held at the switch drain capacitor. Since our goal was to maintain the same power consumption, complementary devices, including NMOS switches M1–M4 and NMOS-based V-I converter M5–M8 were utilized. The input signals of the PMOS path (P1–P8) have a constant phase shift of 90º concerning the NMOS path (M1–M8). The current from each path is added up at the C_D. As each complementary pair (e.g., P6 and M6) in the V-I converters simultaneously conducts current for a quarter reference cycle, the transistors M_p and M_n provide current to each path for spur canceling and also inhibit a short-circuit path from the supply to the ground. Therefore, the NMOS path reuses the current from the PMOS path, consuming half of the power compared with the sampling topology depicted in Fig. 2(a).

B. Spur Canceling

The spur canceling operates in such a way that the charge incurred from the switches in the PMOS path is expected to be neutralized by the charge coming from the switches in the NMOS path within an identical period of time. For example, Upon the falling edge of REF0º, the signal DIV90º passes through P1 and triggers P6 to inject current, intending to charge the sampling capacitor at $\overline{V_{out}}$ by the current $I2$. Meanwhile, since REF0º and DIV0º are out of phase at lock state (assuming full symmetry), DIV0º triggers M6 when M1 is conducting to source the current $I1$ from $\overline{V_{out}}$. The net effect is the charge

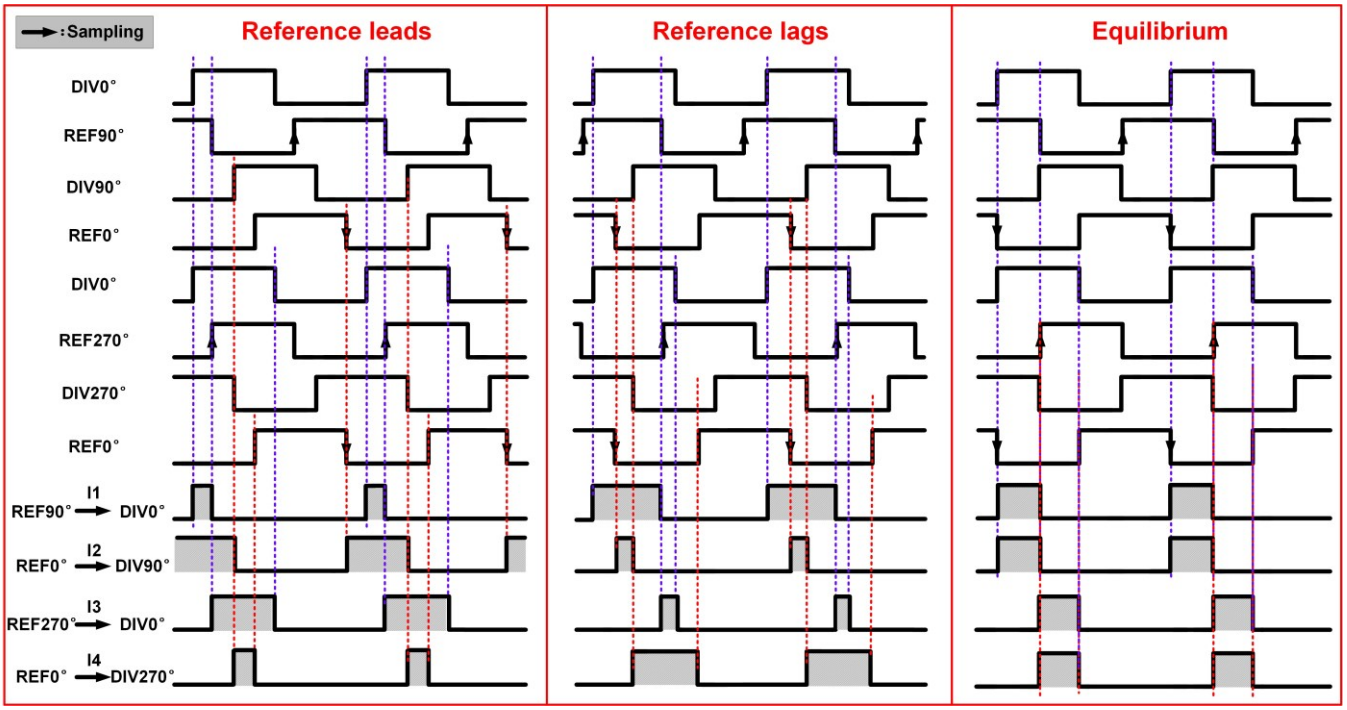

Fig. 5. Timing diagram of the proposed QSPD.

injected by P6 being neutralized by its complementary device M6. At the next half-cycle, REF180º turns on P3, injecting current $I8$ to $\overline{V_{out}}$ through P8. This current is however compensated by M8 through M4 with a current of $I7$. Similar processes apply for P7–M5 and P7–M7 pairs. The differential output is a near-DC voltage that drives the subsequent OTA.

As stated in Section II. B, if the PLL is not locked, REF0º and DIV180º would have a phase offset and different pulse widths such that $I_1 \neq I_2$. The net current ΔI charges/discharges C_D and drives the PLL toward phase-locked by eliminating ΔI. The detailed timing diagram of the proposed QSPD is illustrated in Fig. 5. Here, the symbol "→" means the sampling operation. As shown, depending on the phase offset ($\Delta\Phi$) between the reference signal and the divider output, the PD eventually generates a net current of $\sum I_i = (I1 - I2) - (I3 - I4)$ whose magnitude is proportional to $\Delta\Phi$. Such a net current injects to C_D and converts to a near-DC differential voltage $V_{PD} = \sum I_i \cdot T_{REF} / 4C_D$. The polarity of V_{PD} implies whether the reference signal is leading or lagging. This aspect renders the QSPD to generate an unattenuated current that passes through the LF as a baseband signal, strongly modulates the VCO, and gradually drives the VCO toward lock even when the VCO initial startup frequency is far away from $N{\cdot}f_{REF}$.

At phase-locked, each switch generates a constant current to C_D whose pulse width is equal to a quarter reference cycle. Interestingly, if the PD is free of circuit mismatch, I1 is canceled by I2, while I3 is canceled by I4, and the net effect is the spur canceling such that no current is injected to the LF for a full reference cycle. The same canceling process applies to currents I5–I8, i.e., I5 is canceled by I6, and I7 is canceled by I8.

The proposed QSPD is firstly compared with the topology as shown in Fig. 6, wherein only half of the QSPD (i.e., only NMOS path or PMOS path) exists. Since no complementary path jointly participates in the spur canceling, such a half-circuit should employ RC loads. By inspecting the timing diagram in Fig. 5 (i.e., by observing the logic that generates I1 and I3 only, or I2 and I4 only), such a half-circuit essentially behaves likes a traditional XOR-gate. Similar to the topology shown in Fig. 1 (left) and (middle), wherein an XOR-gate is utilized as the PD, at the steady-state the charge injected (e.g., through either I1 or I5) to C_D in a quarter reference cycle must be compensated by the charge injected (e.g., through either I3 or I7) in the next quarter-cycle, thus introducing large ripples running at $2f_{REF}$. The resulting spur level is dependent on the design parameter including the value of C_D, the OTA conversion gain g_m, and f_{BW}. However, in the proposed QSPD, since the two paths cause the net effect to mutually cancel the respective spur, the reference spur level is independent of the said design parameters.

Compared with the topology in Fig. 1 (left), the QSPD incurs no extra poles to the loop, thus achieving spur reduction without the need for shrinking the f_{BW} or scarifying the phase margin. Compared with the XOR-gate + MSSF PD in Fig. 1 (middle), since the spur reduction relies on spur canceling instead of filtering the ripples, the harmonic traps circuit and its calibration are not necessary, thereby omitting the noise and phase delay introduced by the harmonic traps. Compared with the CRS-PD in Fig. 1 (right), the proposed QSPD preserves the advantage of current-reuse and canceling the clock feedthrough and charge injection, while the first-order RC filters are not necessary for further spur suppression. The QSPD, therefore, has a wider acquisition range that can cover the entire operating range of the VCO without an FLL. As will be described in Section III. D, since the push-pull configuration has a sharp transition in terms of the voltage conversion characteristic [7], the K_{PD} is large such that it can effectively suppress the PD phase noise ($\mathcal{L}_{PD,in\text{-}band} = S_{i,PD}/2K_{PD}^2$). Furthermore, the variation of the ON-resistance of the sampling switches induces signal-dependent aperture delay time, causing distortion. This can be addressed by designing the switches with large devices or

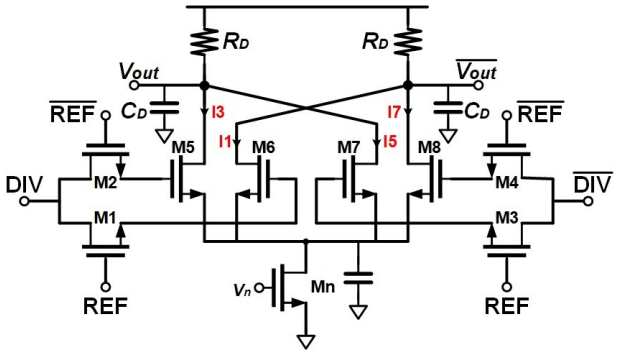

Fig. 6. Half-circuit of the QSPD equivalent to an XOR-gate PD.

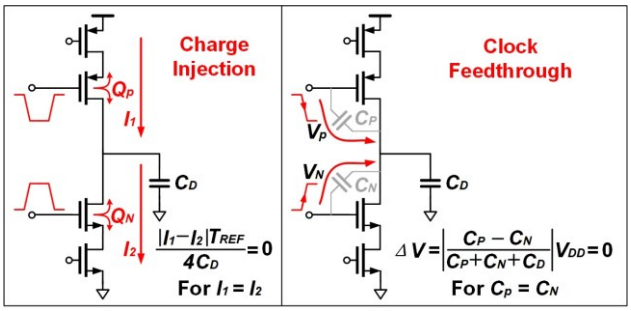

Fig. 7. Condition for spur cancelling in the QSPD.

complementary devices [18], yet both methods exacerbate the clock coupling via its gate-drain capacitance. Fortunately, the clock feedthroughs via the switches are mutually compensated in the V-I converter as well. These two aspects benefit the QSPD and its associated clock buffers to be designed under the normal voltage as opposed to the sample-and-hold circuit in [12], which requires a level-shifted up to 1.8 V for reducing the ON-resistance of the switches.

The conditions are summarized in Fig. 7, respectively, for charge injection and clock feedthrough by the V-I converter, where only one branch of Fig. 4 is exemplified. The principle of compensating the charge injection and clock feedthrough here is essentially the same as the complementary PMOS-NMOS switch [18]. As for the dummy combined switches topology, the removal of the channel charge from the sampling switch is absorbed by the dummy switches, whereas for the complementary switch topology and the QSPD, the removal of the channel charge from a switch is compensated by the opposite channel charge from its complementary switch. Regarding the clock feedthrough of the dummy combined switch, the feedthrough signals coming via the source-drain capacitances of the very short switches are compensated by always-off devices, whereas in the complementary switch and the QSPD, the feedthrough via the gate-drain capacitance of the complementary switch cancels out each other. The difference between the QSPD and the complementary switch is that, the complementary switch itself performs the charge injection and clock feedthrough canceling, whereas in our QSPD, it's the V-I converter (M5–M8 and P5–P8 in Fig. 4) that perform the charge injection and clock feedthrough canceling.

It is imperative to choose proper sizes for each path such that the two conditions are satisfied concurrently. Since the capacitive load seen by the VCO is almost constant for a full reference cycle, the binary frequency shift keying (BFSK) modulation effect is negligible. Furthermore, as indicated in Fig. 7, increasing C_D helps dampen both the effects in the presence of circuit mismatches. Yet, C_D and the ON-resistance of the switch establish a pole to the loop, which should have orders of magnitude larger than the f_{BW} to not degrade the loop stability.

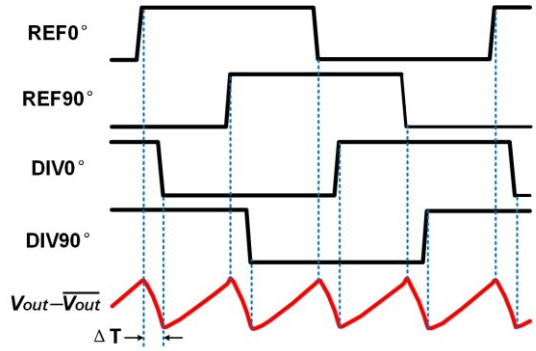

Fig. 8. Waveforms of QSPD in the presence of circuit mismatches.

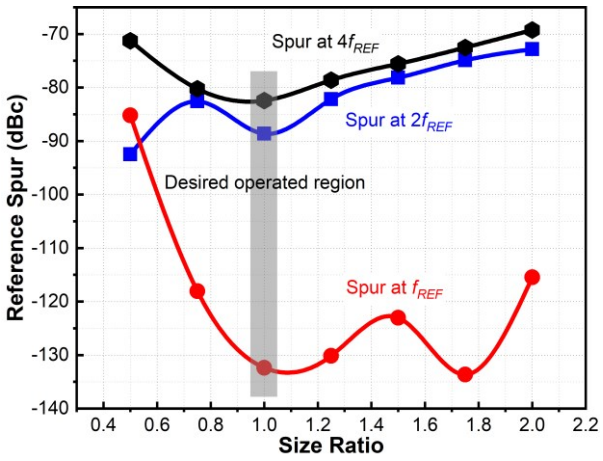

Fig. 9. Simulate reference spur against the size ratio of the QSPD.

In practice, the current mismatch of the OTA and the gate leakage current of the varactor used in the VCO and/or the LF introduce static currents. The proposed PD, therefore, has to create a static phase error between the reference signal and the divider output at the PD input to compensate for those static currents. An illustration of this effect is presented in Fig. 8. As shown, the misalignment of the edge between REF0º and DIV0º creates a timing mismatch of ΔT, during which either the PMOS or NMOS path injects the current to C_D. After ΔT, C_D gets discharged. In the equilibrium state, it satisfies that $I_1\Delta T = I_{dis}(T_{REF}/4 - \Delta T)$, where I_{dis} is the C_D discharge current.

The proposed QSPD produces spurs mainly at f_{REF}, $2f_{REF}$, and $4f_{REF}$, while the spur level at f_{REF} is much smaller than those at $2f_{REF}$ and $4f_{REF}$. The spur at f_{REF} may be caused by the direct coupling of the input pulse through the gate-drain capacitance of the V-I converter [M5–M8, and P5–P8 in Fig. 4], or by the crosstalk through wires, while the third harmonic is the mixing product. Due to this aspect, the size of the V-I converter in the proposed PD cannot be arbitrarily large. Alternatively, we can reduce the source impedance of the V-I converter such that the coupling through C_{GS} is bypassed to the ground. This can be accomplished by enlarging the width of M_P and M_N or, if necessary, by placing bypass capacitors in parallel with M_P and M_N as represented in Fig. 4. The spur at $2f_{REF}$ is due to the sampling operation of each path similar to conventional XOR-

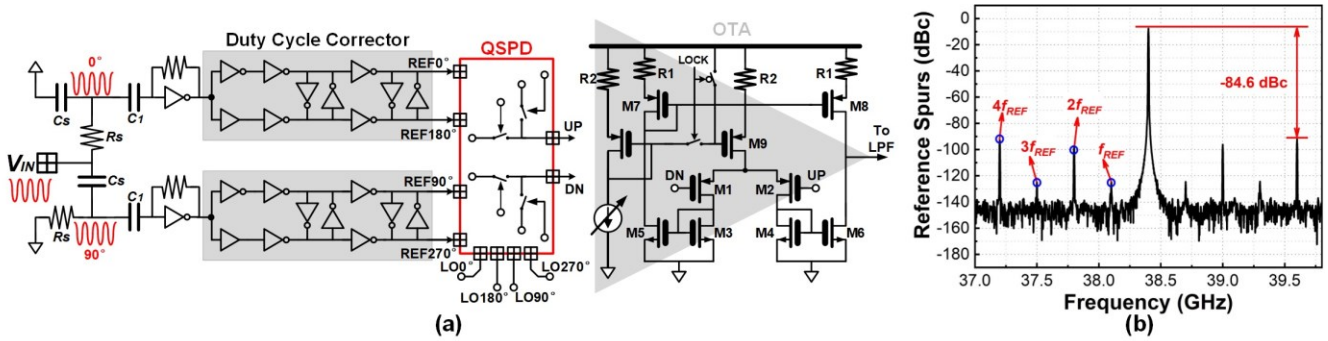

Fig. 10. (a) Complete portrait of the proposed QSPD. (b) Simulated PLL output spectrum ($f_{BW} \approx$ ~10 MHz).

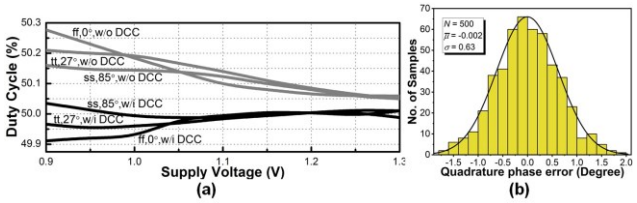

Fig. 11. (a) Simulated duty cycle distortion w/i and w/o the DCC. (b) Monte Carlo statistic of the quadrature-phase error.

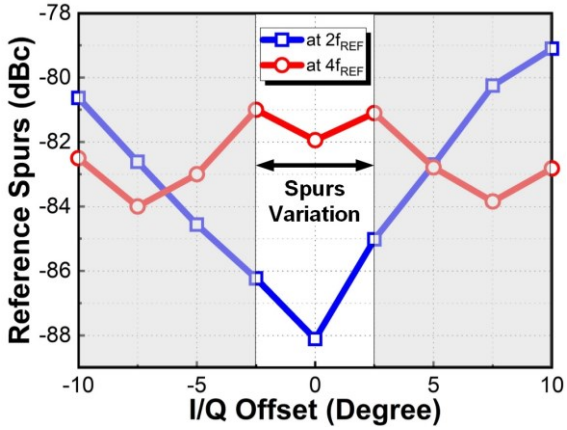

Fig. 12. Simulated reference spur degraded by I/Q mismatch.

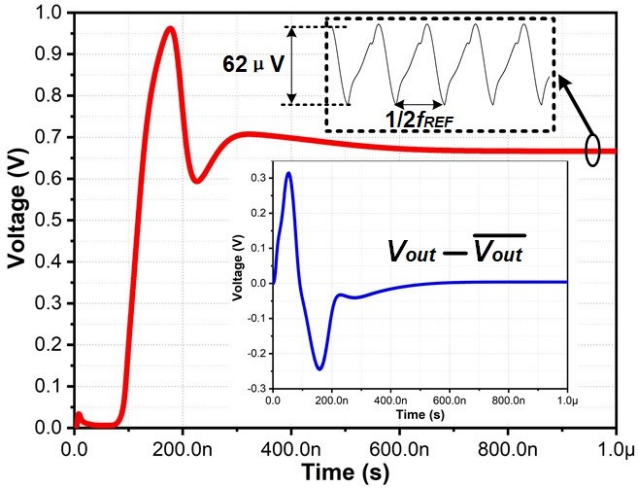

Fig. 13. Settling behavior of the PLL exploiting the QSPD.

gate, and it is, in principle, eliminated by the proposed operation. The spur at $4f_{REF}$ is due to the quadrature operation with spur-frequency-boosting conducted in a way that is similar to the topology in Fig. 2(a). The spur at $4f_{REF}$ is substantially attenuated by the LF.

The spur level against the size ratio (α) of the NMOS path (M5–M8) to the PMOS path (P5–P8) in the V-I converter is indicated in Fig. 9. Here, a loop bandwidth of ~ 5 MHz and a K_{VCO} of 420 MHz/V are chosen for the PLL. As shown, the size ratio of ~ 1 can be chosen for achieving both optimal spur levels at $2f_{REF}$ and $4f_{REF}$. The optimal α varies from 0.72 to 1.4, considering the process spread and temperature variation. By fixing α = 1, the mismatch between the two paths can be partially alleviated by tuning the current through the tail current source M_P and M_N.

C. Complete Structure

The complete schematic of the proposed QSPD is shown in Fig. 10. It consists of an *RC* polyphase filter, two paths of duty-cycle correctors (DCC), the proposed sampling topology in Fig. 4, and the OTA. With a single-tone sinusoidal wave as the input signal, the polyphase filter comprises resistor R_S and capacitor C_S. By choosing C_S = 2 pF, R_S would be about 265 Ω to achieve a 90º phase shift and 0 dB magnitude error at 300 MHz. The resistor, made by p+ polysilicon resistor, is put beneath the MOM capacitor to save area and has dummy resistors surrounding it. The mismatch occurs mainly because of the variation of the resistor, trading off the area for better matching. Since the polyphase filter introduces 15.2 dB insertion loss, a subsequent self-bias inverter with high gain amplifies and rectifies the sinusoidal wave to square waves. Unfortunately, both the polyphase filter and the self-bias inverter incur phase/amplitude imbalance that distorts the rise/fall time and the pulse width of the quadrature signals, leading to duty cycle distortion and a worse reference spur. The phase/amplitude imbalance is alleviated by the DCC circuit, consisting of a chain of inverters with latch-type inverters to correct for the clock edge. With the DCC circuit, the simulated duty cycle is summarized in Fig. 11(a) considering the corners and temperature variations. The DCC circuit reduces duty cycle distortion to below 0.1%. The Monte Carlo statistic of the quadrature error including the *RC* polyphase filter and the DCC circuit is represented in Fig. 11(b), showing a maximum variation of ±2º. Using the proposed QSPD, Fig. 10(b) shows the simulated PLL output spectrum. In addition to the second and the fourth harmonics, the spectrum contains mixing products at the first and the third harmonics, but their power levels are at least a hundredfold smaller than those at the second and the fourth harmonics. The largest reference spur appears at $f_{VCO} \pm 4f_{REF}$, which is –84.6 dBc, verifying the effectiveness of

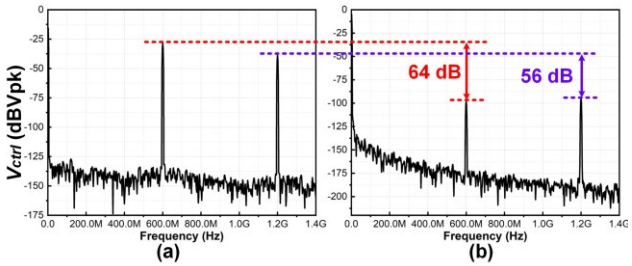

Fig. 14. Simulated PLL control line voltage frequency response for (a) conventional sampling PD, and (b) proposed QSPD.

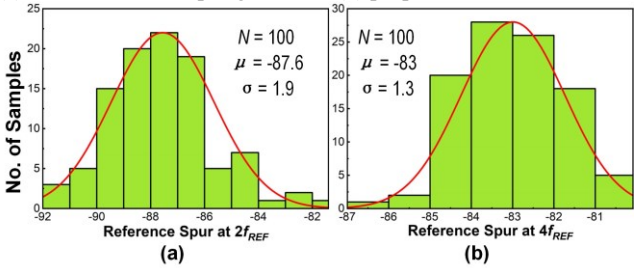

Fig. 15. Monte Carlo statistics of the QSPD spur level at (a) the second harmonic, and (b) the fourth harmonic of f_{REF}, respectively.

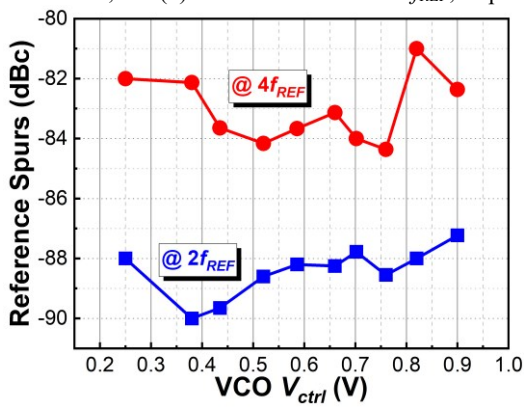

Fig. 16. Reference spur against the VCO control line voltage.

the proposed PD in terms of spur canceling. Fig. 12 illustrates the reference spur degraded by the I/Q phase error. With an I/Q mismatch of ±2.5º, the spur at $4f_{REF}$ is degraded by 1 dB, while the spur at $2f_{REF}$ is degraded by 5 dB. Yet, the spur level at $2f_{REF}$ is still smaller than –84 dBc. As such, no calibration is required for the I/Q generator. All the inverters in the QSPD are designed with thick-oxide transistors.

The PLL convergence curve is provided in Fig. 13, showing about 62 μV peak-to-peak voltage operating at $4f_{REF}$ on the VCO control line. In contrast to the SPD adopted in [12], FLL is not necessary here to assist the phase-locking or to speed up the acquisition. Furthermore, the QSPD outputs converge to a near-DC value upon phase-locked, rather than producing consecutive narrow pulses as is the case in CP-PLLs. This property is particularly useful for multi-supply systems in which the VCOs are designed with higher supply voltages [5], [11], [12]. To serve this purpose, the PMOS differential pair should be utilized as the input stage of the OTA, and, if necessary, all transistors in the OTA should be designed with thick oxide transistors. The channel length chosen for PMOS and NMOS in OTA (M3–M8) is 400 nm and 450 nm, respectively, for reducing the channel length modulation effect, while their widths are chosen to be sufficiently wide to reduce their flicker noise. The OTA is disabled by the "LOCK" signal during lock detection (VCO band-searching). Upon the completion of lock detection, the "LOCK" signal releases the OTA and starts the phase alignment.

Fig. 14 compares the ripple on the VCO control line voltage (V_{ctrl}) for the half-circuit of the QSPD (Fig. 6) and the proposed QSPD. The QSPD suppresses the ripple at $2f_{REF}$ and $4f_{REF}$ by 64 dB and 56 dB, respectively. The Monte Carlo statistics including the reference spur at $2f_{REF}$ and $4f_{REF}$ are provided in Fig. 15. The reference spur at $2f_{REF}$ is smaller than –81 dBc for all cases, while the reference spur at $4f_{REF}$ mainly locates between –85 dBc and –81 dBc. The spur at $2f_{REF}$ primarily arises from the I/Q imbalance and the mismatch between the PMOS and the NMOS path. However, as stated previously, tuning the tail current through M_p and M_n in Fig. 4 partially alleviates the spur degradation without calibration. Using wider transistors in the V-I converter also helps reduce the process variation.

Fig. 16 summarizes the simulated reference spurs against the V_{ctrl}. In this loop simulation, the VCO and dividers are Verilog-A model, and the resistor and capacitor in the LF are ideal components. The DCC, QSPD, and OTA are designed at the transistor level. The reference frequency is swept such that the VCO locks to different frequencies within the same control bank, and the V_{ctrl} converges accordingly to the respective voltage. As shown, the reference spur level at $2f_{REF}$ and $4f_{REF}$ remain relatively constant over a wide range of V_{ctrl}, indicating that the spur canceling maintains its effectiveness against V_{ctrl}.

D. Noise Consideration

The design should be such that the proposed QSPD's intrinsic noise falls below the reference input clock noise level near the f_{BW}. Once the QSPD noise becomes negligible, the PLL's in-band noise is dominated by the reference clock noise. Meanwhile, as stated previously, the PLL's out-of-band noise, dominated by the VCO noise level, is suppressed by widening f_{BW} without affecting the level of rejection to the reference spur.

Random jitter (RJ) contributed by the QSPD is described by

$$\text{Noise}_{\text{OTA}} = 20\log\left(\frac{2\cdot\pi\cdot I_N\cdot N}{K_{PD}}\right) \tag{5}$$

where I_N represents noise current from the OTA in amperes. It is, therefore, preferable to choose a small N and enlarge the PD gain. To minimize the noise contribution of the QSPD in Fig. 4, the PMOS and NMOS devices are sized with W/L = 16 µm/40 nm and 10 µm/40 nm, respectively, and all the devices in the V-I converter are sized with 16 µm/80 nm, achieving a phase noise of −159 dBc/Hz at 5 MHz offset while consuming 216 µW. This leads to an in-band phase noise at the PLL output equal to −159 dBc/Hz + 20log$N$ = −116.9 dBc/Hz. Since the QSPD output converges to a DC value upon phase-locked, the input differential pair in the OTA is sized as large as 64 µm/240 µm to reduce its flicker noise. The source degeneration resistors *R1* and *R2* in the OTA further lower the flicker noise by 39%, according to the simulation. With a high PD gain of K_{PD} = 5.4 mA/rad, the in-band phase noise of the complete QSPD (including OTA) is −108 dBc/Hz at 1 MHz offset, which is ~ 3 dB below the reference noise level.

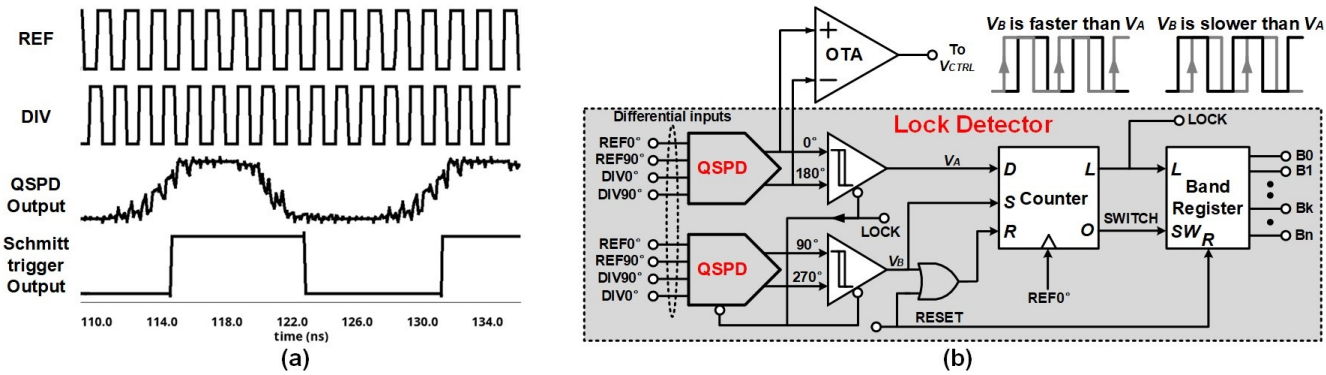

Fig. 17. (a) Waveforms showing the beating signal when $f_{REF} \neq f_{DIV}$. (b) Proposed QS-PFD extended from the QSPD.

E. QS-PFD and Lock Detection

According to (3), assuming VCO operates at an initial frequency of f_v, the QSPD generates a "beat" component of $|f_v/N - f_{REF}|$. This beat component passes through the LF as a baseband signal, providing nearly a rail-to-rail voltage swing to the VCO. The VCO is, thus, strongly modulated at a rate of $f_v/N - f_{REF}$, producing a strong sideband at the divider output located at f_{REF}. This sideband creates a DC component at the QSPD output, leading to acquisition. Simulation confirms that the capture range is much wider than the frequency tuning range in each VCO band. In this regard, no FLL is required in this design to assist the frequency locking.

In type-I PLLs, the high K_{PD} of the proposed QSPD can be exchanged for a reduced K_{VCO} for a given PLL loop gain while maintaining the required phase margin. To satisfy the mm-wave PLL's wide tuning range, coarse tuning and lock detection are preferred. Fortunately, the proposed PD can distill the beating frequency $f_B = |f_{DIV} - f_{REF}|$ for lock detection. Due to the sampling operation, the beating signal contains many glitches in its output waveform, potentially confusing the subsequent digital circuits. This is solved by using a Schmitt trigger since it cannot respond to a fast-varying signal because of its hysteresis characteristic, yet providing high gain to the slow-varying signal. The simulation results provided in Fig. 17(a) confirm these predictions.

The proposed QSPD is extended to the QS-PFD as represented in Fig. 17(b). Two QSPDs and two Schmitt triggers serve as the frequency detector (FD). Whether the reference signal is leading or lagging can be determined using the signal V_B to continuously sample its counterpart V_A. The subsequent counter, clocked by the reference signal, counts the period of f_B. The band register records and assigns the band for VCO. Simulation reveals that the maximum tolerable f_B of the QS-PFD ranges from 58.6 to 63 MHz, considering the corners and temperature variations (0 – 85ºC), which is much higher than $|f_v/N - f_{REF}|$ for all VCO bands in our design.

Lock detection is explained in the flowchart in Fig. 18. In detail, the VCO control line is tied to the supply (V_{DD}) upon the circuit startup such that the VCO operates in the highest frequency in each band. The VCO band searching starts from the lowest band. Once V_B samples a "0", which indicates that the reference signal is still faster than the divider output, the band register jumps to a higher VCO band such that the VCO operates on a higher frequency, gradually eliminating f_B. This process continues until V_B samples a "1", indicating the reference signal is slower than the divider output. If the counter overflows, meaning f_B is sufficiently small, the VCO control line is released from V_{DD}, finalizing the lock detection. Otherwise, error may occur due to the overjump of the band switching, and lock detection starts from the beginning.

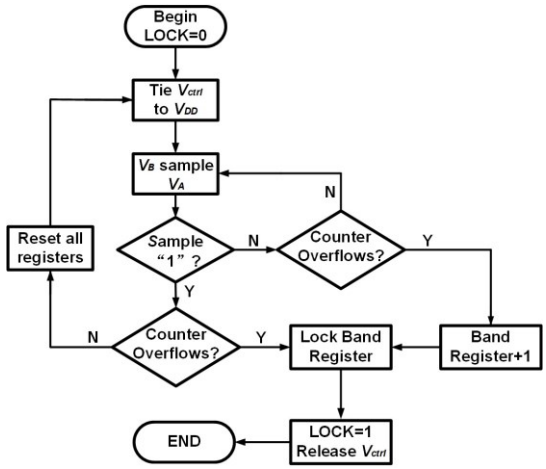

Fig. 18. Flowchart of the lock detection.

Lock detection time is independent of the loop components. However, in conventional designs using two comparators to measure the VCO control voltage [19], lock detection may take over 1 millisecond if the loop incorporates an external capacitor.

IV. Millimeter-Wave Circuits and PLL

A. VCO

A traditional cross-coupled VCO is utilized, including an inductor ($L1$) and negative resistances (M1 and M2), as shown in Fig. 19. A wideband VCO is preferred for mm-wave applications, and it is also suitable for overcoming process, voltage, and temperature (PVT) variation and electromagnetic (EM) extraction errors. Unfortunately, oscillators operating on the mm-wave frequency are sensitive to supply variations, which causes the oscillation frequency to drift. The supply variation also degrades the phase noise (PN). To overcome this issue, a supply-independent circuit constructed by transistors M5−M9 and resistor $R1$ are employed to ensure that the current I_{vco} flowing into M1−M2 remains nearly constant. This can be fulfilled by letting the variation rate of I_s be equal to that of $I_s - I_{vco}$. M10 is introduced here to absorb the extra current variation caused by channel-length modulation to further reduce the supply noise. With proper design, the power penalty

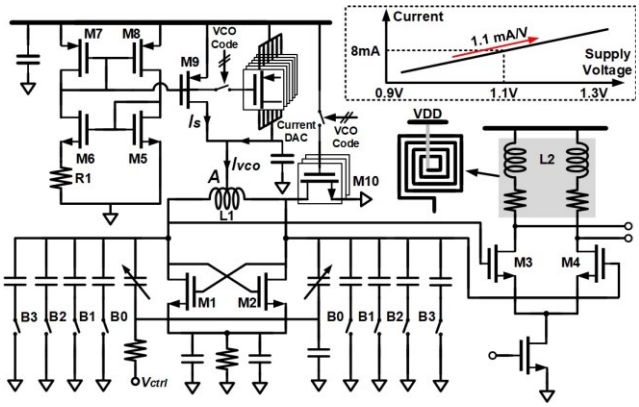

Fig. 19. Cross-coupled *LC* VCO with a supply-independent circuit.

of M10 can be restrained to 20%. The simulation reveals that the supply-insensitive circuit provides the power supply rejection ratio (PSRR) of 19 dB, 28 dB, and 43 dB at 10 Hz, 1 kHz, and 1 MHz respectively.

The four-bit coarse tuning from 36.4 to 40.6 GHz is applied here. Thick oxide varactors are employed for fine-tuning and for reducing the leakage current under the large swing of the VCO. As the VCO tank's quality factor (*Q*-factor) gets undermined when turning on more capacitor bank switches (because of the switches' series resistance), a 4-bit binary-weighted current digital-to-analog converter (DAC) is incorporated in parallel with the VCO current bias (M9 in the supply-independent circuit) to compensate for the tank *Q*-factor degradation and maintain the VCO output swing almost consistent for all VCO bands. Doing so also ensures the VCO has a sufficiently large output swing to lock the subsequent prescaler throughout its entire operating range. The current DAC receives a 4-bit word, the same as the capacitor bank's, resulting in a proportional increase of the VCO bias current when more capacitor banks are selected. Lastly, the buffer stages M3 and M4 are placed in between the VCO and the next stage to avoid overwhelming capacitive loading.

B. Mm-Wave Prescaler

To accommodate a wide tuning range, a Miller divider realized by transistor M1−M6 is used as the prescaler, as shown in Fig. 20. M1 and M2 are the input differential pair. M3 and M4 form a diode-connected transistor, M5 and M6 establish the regeneration pair, and the output port directly feedbacks to M3 and M4. Note that the output can also feedback to M1−M2 but doing so will increase the capacitive loading of the preceding stage. Moreover, doubling the capacitive loading to the output lowers the tank quality factor, and therefore extends the operating range to some extent.

The operating bandwidth $f_{BW\text{-}M}$ of the Miller divider is critical for covering the entire VCO tuning range and also accommodating the possible process variation. $f_{BW\text{-}M}$ can be determined through loop gain. To evaluate this, the output feedback loop is cut, and a sinusoidal signal with a frequency of $f_0/2$ is applied to M3 and M4. The loop gain is thereby evaluated as the power gain from the input differential pair M1−M2 to the output. The simulation result is provided in Fig. 21, using PAC analysis with PVT variation considered. The maximum operating frequency range of the Miller divider is twice the open-loop unity-gain bandwidth. Here, parameter N_M

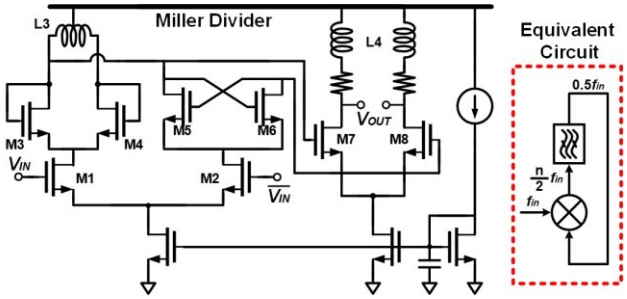

Fig. 20. Miller divider.

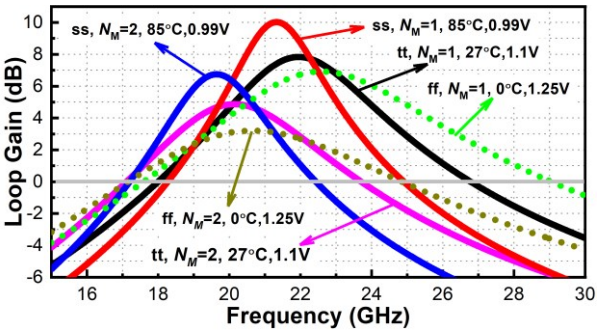

Fig. 21. Simulated open loop gain of the mm-wave Miller divider.

denotes the ratio of width from M5,6 to M3,4. As indicated, increasing N_M from 1 to 2 decreases the gain and does not increase the unity-gain bandwidth. Particularly, the smallest $f_{BW\text{-}M}$ is found for the ss corner when $N_M = 1$ and $V_{DD} = 0.99$V, which is from 34 to 45 GHz, still capable of covering the whole VCO frequency tuning range. The Miller divider stops dividing at a lower frequency because the third harmonic ($1.5f_0$) has not been sufficiently attenuated in the feedback loop. As a result, by choosing $N_M = 1$, more than 11 GHz operation range is achieved for every PVT. The load inductor *L3* has a differential inductance of 1.5 nH at 20 GHz, with a peak differential quality factor of ~19. The power consumption is 4.5 mW.

C. Other Dividers

The above Miller divider may exhibit a self-resonance frequency if $N_M > 1$, evolving to an injection lock frequency divider (ILFD). ILFD features low-power operation and high input sensitivity. Yet, *LC*-based ILFD has a narrow locking range. Alternatively, inverter-based ILFD owns a much wider operating range. Fig. 22(a) illustrates an inverter-based divide-by-4 ILFD circuit. Current starving inverters I1 – I8 form the eight-stage ring oscillator, while transistors M1 – M6 constitute the double-balanced active mixer. The ILFD output contains the odd harmonics of $(1/4)f_{in}$, mixing with the harmonic mixer input to generate the sidebands. Particularly, the third harmonic mixes with the input signal and generates the mixing product at $(1/4)f_{in}$, which passes through the low-pass filter and is then amplified by a self-bias inverter. With other mixing products filtered out, the strong signal at $(1/4)f_{in}$ locks the ring oscillator, achieving low-power operation and a wide locking range. A voltage DAC has been utilized to bias the current (and hence, the delay) of I1 – I8, for coarse frequency tuning. With 4-bit coarse tuning, the simulated frequency locking range is 15 – 26 GHz, covering the whole desired operating range. Simulation reveals that the structure can operate at 40 GHz as well, but the power consumption is ~10 mW, higher than the Miller divider.

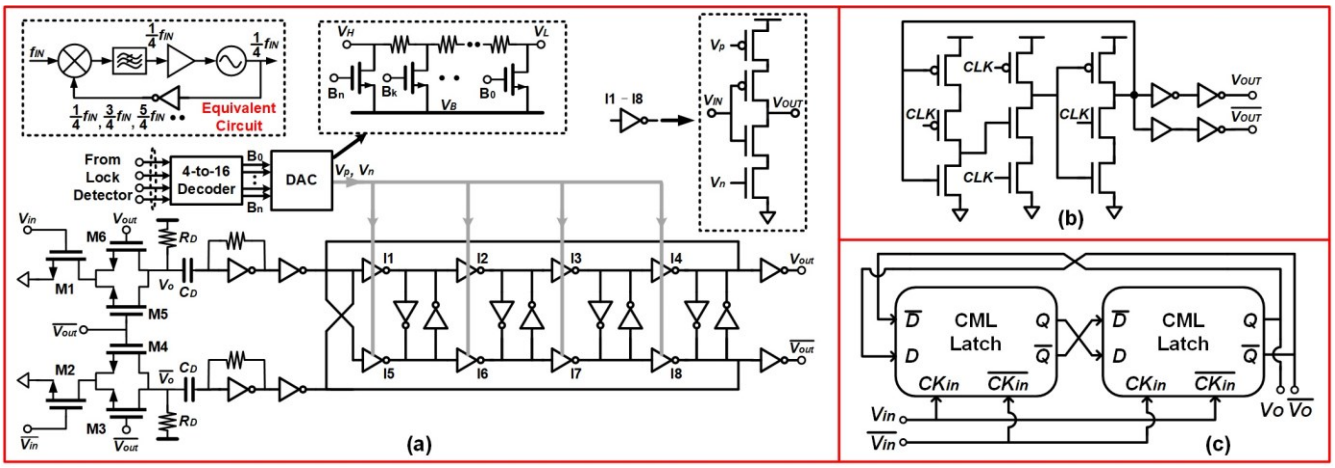

Fig. 22. (a) Divide-by-four injection-locked frequency divider based on ring oscillator. (b) TSPC divider. (c) Static divider.

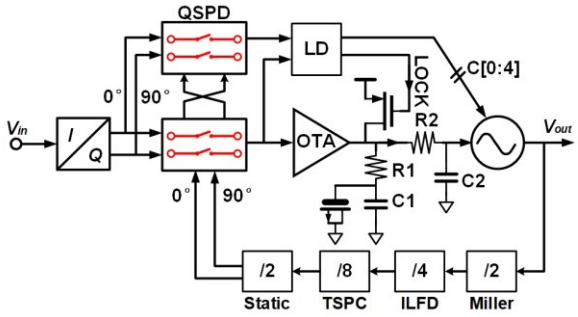

Fig. 23. Block diagram of the proposed PLL.

The subsequent divide-by-4 divider is realized by two stages true single-phase clock (TSPC) divider [Fig. 22(b)]. A static frequency divider [Fig. 22(c)], which provides the quadrature-phase output for the QSPD, serves as the final stage of dividers. Monte Carlo statistic shows that the standard deviation of the quadrature-phase error is only 0.02°.

D. PLL and Loop Dynamic

Fig. 23 shows the block diagram of the proposed PLL. It consists of an I/Q generator, two QSPDs, an OTA, an LF, a VCO, an LD, and dividers. The QSPD used for lock detection and the LD are turned off upon the completion of the lock detection. The LF consisted of a resistor *R1* and a capacitor *C1* provides a zero to compensate for the phase drop of the OTA. *C1* is constructed by stacking the MOM capacitor onto the thick-oxide NMOS varactor, to save area. The secondary capacitor is not necessary because of the pole already introduced by the QSPD's equivalent ON-resistance and C_D in Fig. 4. *R2* and *C2* further attenuate the high-frequency spurs.

The PLL open-loop gain is expressed by

$$H_{open} = \frac{K_{QSPD}}{1+sR_SC_D} \times g_m(r_o \,||\, Z_{LF}) \times \frac{K_{VCO}}{N \times s} \qquad (6)$$

where K_{QSPD} (V/rad) is the gain of the QSPD, g_m is the transconductance of the OTA, r_o is the output impedance of OTA, Z_{LF} is the transfer function of the LF. The open-loop gain transfer function presents five poles at 38.4 GHz, respectively at the origin, 1.3×10^9, 4.8×10^7, 2.7×10^7, and 1.9×10^6 rad/s, whereas one zero cancels out one of the poles at 2.7×10^7 rad/s. The remaining zero is at 4×10^6 rad/s, between the two dominant poles. The loop bandwidth is ~4.9 MHz and the worst-case phase margin of 53º. The 300-MHz I/Q reference signal can be extracted from another low-frequency PLL in future work.

V. Measurement Results and Discussion

The proposed PLL was fabricated in a 40-nm CMOS process; a die photograph with the testing setup is shown in Fig. 24. The chip occupies a core area of 0.34 mm^2. The spectrum and phase noise were measured using the R&S spectrum analyzer (R&S FSW 67). The reference signal was provided by R&S SMF 100A. An 8-channel precision voltage source was used as the power supply.

The measured VCO tuning curve is provided in Fig. 25, covering the frequency tuning range from 36.4 to 40.6 GHz. In this measurement, the loop components, including the dividers and QS-PFD, were turned off. A feeding path to the capacitor *C1* in Fig. 23 provided the voltage and drove the VCO control line. Fig. 26 shows the measured PN plot of the VCO near the mid-band carrier frequency of 38.4 GHz with a PN of −93.4 dBc/Hz at 1 MHz offset and −118 dBc/Hz at 10 MHz offset, respectively. The simulated result fits closely with the measurement result.

The PLL output spectrum measured at 38.56 GHz is provided in Fig. 27. Since the PLL output power was weak, and the noise floor of the spectrum was high (span = 2.4 GHz), the reference spurs were buried below the noise floor. For this reason, the reference spurs were found by zooming in the spectrum and measured with a much smaller resolution bandwidth (RBW ≤ 50 Hz) and span = 10 kHz. Fig. 28 shows the measured spectrum at 38.4 GHz (f_{REF} = 300 MHz). The output power at 38.4 GHz was −15.5 dBm, while the highest spur level appeared at $f_{OUT} - 4f_{REF}$, translating to the maximum reference spur of −75 dBc. Interestingly, the spurs level at $f_{OUT} \pm 2f_{REF}$ were smaller than those at $f_{OUT} \pm 4f_{REF}$. This in turn verified the spur-canceling achieved by the proposed QSPD. The spurs at $f_{OUT} \pm f_{REF}$ were at least 10 dB smaller than those at $f_{OUT} \pm 2f_{REF}$ and $f_{OUT} \pm 4f_{REF}$. Fig. 29 summarizes the measured maximum reference spurs collected for the entire operating frequency over 5 samples. The worst-case was –74.8 dBc, with 1.7 to 2.1 dB variation for the entire operating range.

To avoid introducing noise to the sensitive loop control voltage node, the voltage source was disconnected from *C1* during PLL phase noise measurements. The measured PN of –88.7 dBc/Hz at 10 kHz offset and –103.3 dBc/Hz at 1 MHz

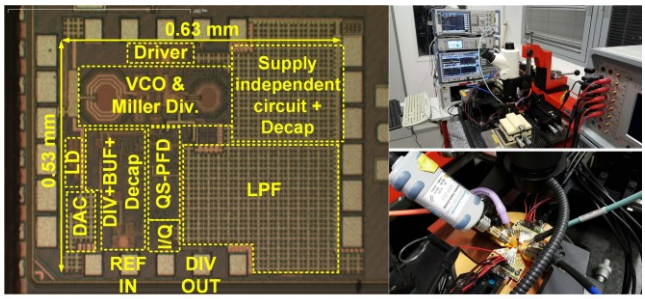

Fig. 24. PLL die photo and testing setup.

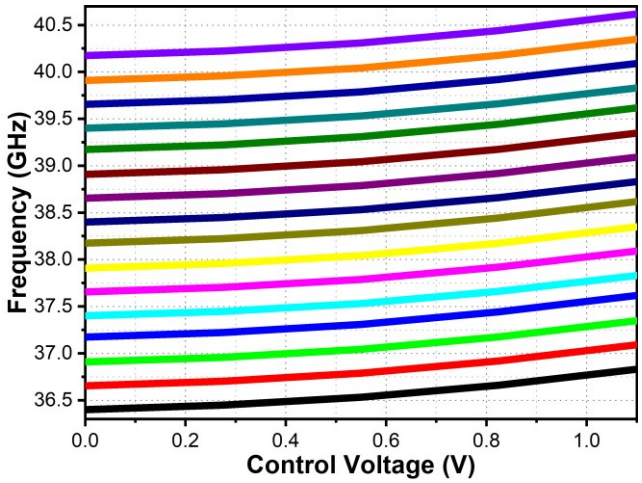

Fig. 25. Measured VCO tuning curves.

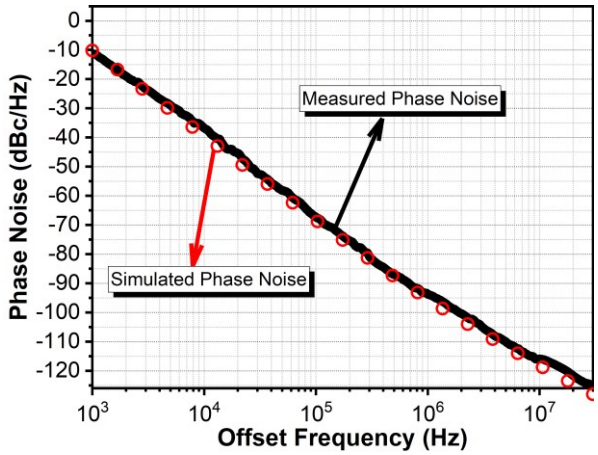

Fig. 26. Measured and simulated VCO phase noise at 38.4 GHz.

offset, respectively, was found at 38.56 GHz, measured directly at the VCO output, as shown in Fig. 30. The resulting jitter, integrated from 10 kHz to 100 MHz which is the same range most other prior-art uses, was 134.5 fs_{rms}. Here, $\mathcal{L}_{REF\_Meas.}$ denotes the measured reference phase noise, whereas $\mathcal{L}_{PD}$ represents the overall simulated phase noise from the *RC* polyphase filter, the DCC, the QSPD, and the OTA. Simulation result shows that the phase noise of *RC* polyphase filter plus DCC contributes ~17% to $\mathcal{L}_{PD}$, which is dominated by the flicker noise of OTA. The noise/jitter decomposition verified the PD in-band noise to be ~10 dB smaller than the reference noise level near the f_{BW}, and thus no longer the dominant factor. The analytical result exhibits a good agreement with the measured result, and the achievable integrated jitter was limited

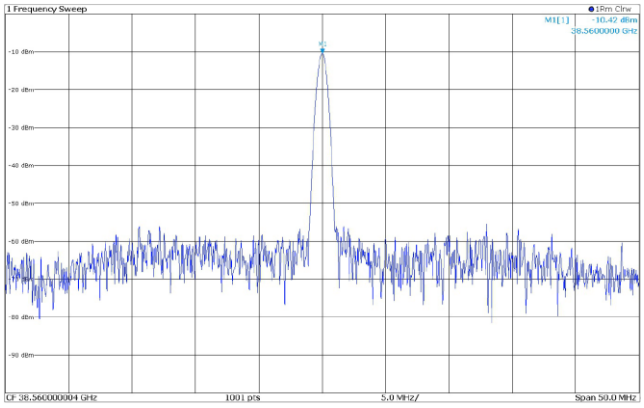

Fig. 27. PLL spectrum measured at 38.56 GHz.

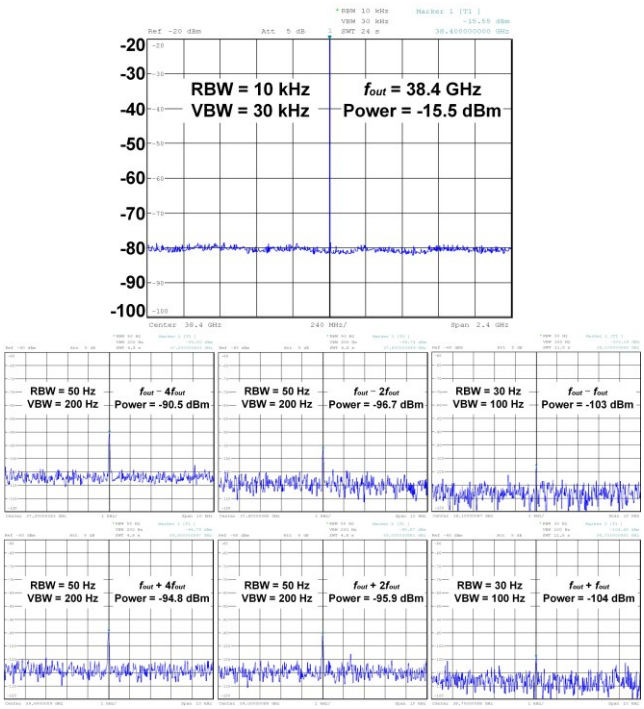

Fig. 28. Measured PLL reference spurs at 38.4 GHz.

by the reference signal source (40% jitter contribution). The peaking can be reduced by lowering K_{QSPD}, or using a smaller C_D. If the reference is provided by a clean crystal, such as CRBSCS-01-250.000 [20] whose integrated jitter is ~22 fs_{rms} (1 k-to-40 MHz), the expected PLL integrated jitter will be reduced from 134.5 fs_{rms} to 104 fs_{rms}. In this case, the noise contribution of VCO, PD, dividers, and reference are 58.4%, 30.8%, 10%, and 0.1%, respectively. The PD noise now dominates the in-band phase noise, which can be lowered by using wider devices in the OTA. Future work should also reduce the VCO phase noise.

As analyzed in the last Section, the peaking located at about the loop bandwidth ($f_{BW} \approx 4.9$ MHz) can be reduced by lowering the open-loop gain, but doing so degrades the PLL in-band phase noise according to (5). This effect is illustrated in Fig. 31, where the open-loop gain was slightly reduced by lowering the OTA output current. As shown, the peaking disappeared, but the PLL in-band phase noise degraded as well. Reducing the OTA output current also shrank the loop bandwidth down to ~ 3.5 MHz. Despite this, the integrated jitter (10 k-to-100 MHz)

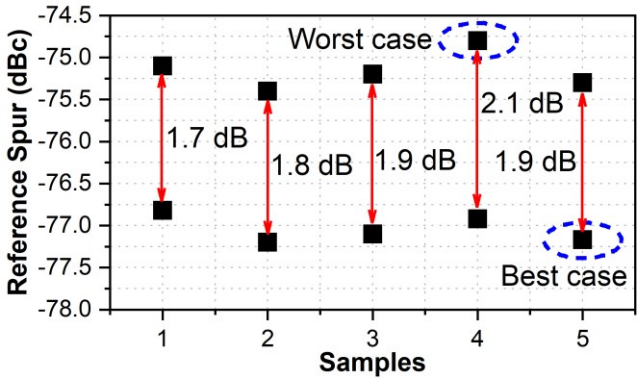

Fig. 29. Measured PLL reference spur over frequency and samples.

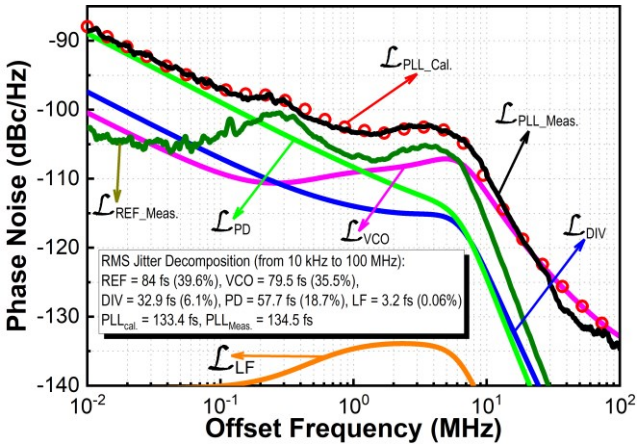

Fig. 30. Measured PLL phase noise at 38.56 GHz with MATLAB-simulated noise/jitter decomposition.

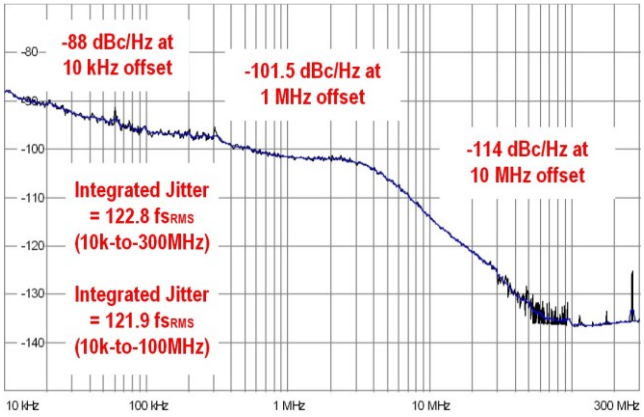

Fig. 31. Measured PLL phase noise at 38.2 GHz when K_{PD} is reduced to remove the peaking near the loop bandwidth.

was reduced to 121.9 fs_{rms}. This is because noise contributes the most at the offset frequency closest to the PLL bandwidth. Fig. 32 summarizes the integrated jitter over the entire frequency range. Integrated jitter smaller than 169.4 fs_{rms} was achieved for the entire operating frequencies.

Fig. 33(a) shows the measured PLL settling behavior measured at the 5-GHz divider output upon the switching of the reference frequency within the same VCO band (with the LD turned off). Since a finite time was required for the switching of the reference frequency, there was an uncertain state between such a short period, causing the PLL to flip at ~ –9.5 µs and –6 µs. The acquisition time was ~ 800 ns closed to both the

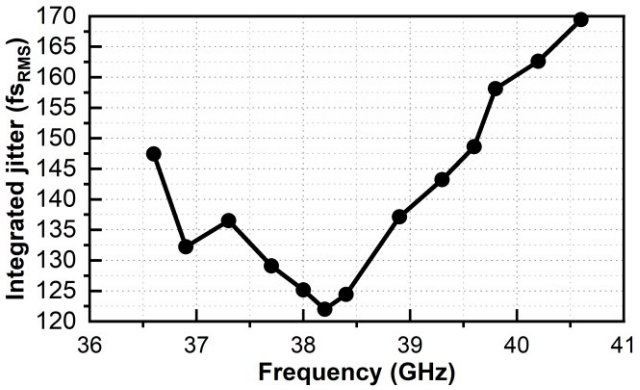

Fig. 32. Measured PLL RMS jitter over the entire operating range.

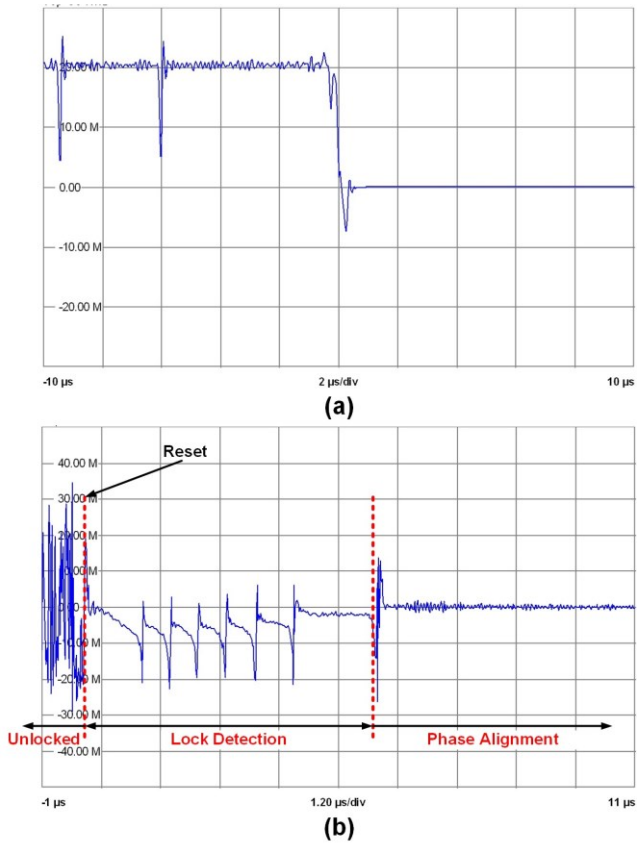

Fig. 33. (a) Measured PLL acquisition. (b) Measured PLL acquisition assisted by the proposed lock detector.

analytical/simulated result. With the LD turned on, Fig. 33(b) demonstrates the VCO band-searching enabled by the proposed LD. A "reset" signal was provided as a triggering signal, such that the LD started the band-searching from the lowest-frequency band. The LD switched the VCO band upward gradually toward the desired frequency, eliminating the frequency error. As shown, the overall convergence time was at the microsecond level (~ 6 μs).

The PLL power consumption breakdown is provided in Fig. 34. The VCO (w/i buffer), dividers (w/i buffer), QSPD, I/Q generator (w/i DCC), and the OTA consume 9 mW, 10.8 mW, 216 µW, 1.9 mW, and 1.6 mW, respectively. Since the LD only operates for several microseconds, the power without accounting for the LD (including the additional one QSPD, two Schmitt triggers, and the subsequent digital circuits) will be

TABLE I

MILLIMETER-WAVE PLLS PERFORMANCE COMPARISON

	JSSC'18 [1]	*ISSCC*'19 [22]	*ISSCC*'20 [23]	*TMTT*'17 [24]	*ISSCC*'16 [25]	*TMTT*'20 [26]	*ISSCC*'19 [27]	**This work**
Technology	28 nm CMOS	65 nm CMOS	28 nm CMOS	0.18 µm SiGe	65 nm CMOS	0.12 µm SiGe	65 nm CMOS	**40 nm CMOS**
f_{ref} (GHz)	0.4915	0.103	0.25	0.12	3.5	0.1552	0.1	**0.28–0.32**
f_{out} (GHz)	23.3–30.2	25.4–29.5	21.7–26.5	29.5–33.4	25.3–30.4	20.5–24.88	30.6–34.2	**36.4–40.6**
PN@10 kHz Norm. to 38.2 GHz	−86	−96.6	−91.7	−77.9	/	−73.5	−81.8	**−88**
PN@1 MHz Norm. to 38.2 GHz	−100	−109.58	−107	−94.9	−103.3	−104.5	−97.4	**−101.5**
$\mathcal{L}_{norm}$ (dBc/Hz²) @1 MHz Norm. to 38.2 GHz	−192	−238	−233	−224	−217	−229	−228	**−228**
Ref. spur (dBc)	−65.1	−63.2	−45	−40	/	−70	−67.5	**−75**
Integrated jitter [Integ. Range]	115 fs_{rms} [20 kHz −500 MHz]	71 fs_{rms} [1 kHz −100 MHz]	75.9 fs_{rms} [10 kHz −30 MHz]	700 fs_{rms} $ [1 kHz −100 MHz]	103.9 fs_{rms} [100 kHz −100 MHz]	198.6 fs_{rms} [1 kHz −10 MHz]	197.6 fs_{rms} [30 kHz −10 MHz]	**121.9 fs_{rms} [10 kHz −100 MHz]**
Power (mW)	31	15.3	16.5	63	261	120#	35	**23.6**
Area (mm²)	0.11	0.24	0.5	5.2	2.4	1.23	0.79	**0.34**
FoM (dB)	−244	−251.1	−250.2	−225	−235.5	−233.3	−238.6	**−245**
FoM_{JRP} (dB)	−237	−251	−246.2	−214.3	−220	−231.3	−238.6	**−239.8**

$: extracted from the published phase noise plot #: excluding the buffer power of 30 mW

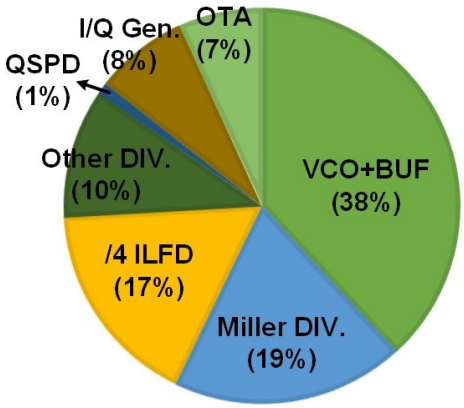

Fig. 34. PLL power consumption breakdown.

presented as the PLL power consumption. The LD consumes ~ 4.6 mW power during lock detection. LD will be automatically shut down upon the competition of VCO band-searching. In addition to LD, the 40-GHz output driver consumes additional 8 mW power for overcoming the cable loss and driving the external instruments for testing. Since the PLL is intended to deliver its output signal to a transceiver on the same chip in the future prototype, and this mm-wave buffer is mainly for testing purposes, its power has not been counted.

The standard metrics for PLL performance quality are $\mathcal{L}_{norm}$ [16], FoM [1], and FoM_{JRP} [21] described as follows:

$$L_{norm} = L_{in-band} - 20\log(N) - 10\log(f_{REF}) \quad (7)$$

$$\text{FoM} = 10\log\left[\left(\frac{\text{RMS\_Jitter}}{1\,s}\right)^2 \cdot \left(\frac{\text{Power}}{1\,\text{mW}}\right)\right] \quad (8)$$

$$\text{FoM}_{\text{JRP}} = 10\log\left[\left(\frac{\text{RMS\_Jitter}}{1\,s}\right)^2 \cdot \left(\frac{\text{Power}}{1\,\text{mW}}\right) \cdot \left(\frac{f_{REF}}{100\text{MHz}}\right)\right] \quad (9)$$

Table I summarizes state-of-the-art mm-wave CMOS PLLs performance. The proposed PLL achieves the lowest reference spur of –75 dBc, which is at least 5 dB better than other works listed in Table I. Although the CP-PLL in [26] attains a reference spur of –70 dBc, its power consumption is 5X of our work. The achieved $\mathcal{L}_{norm}$, FoM, and FoM_{JRP} are compared favorably with state-of-the-art.

VI. CONCLUSION

This article proposes a novel quadrature sampling phase-frequency detector (QS-PFD) for suppressing PLL spurious tones. By introducing an auxiliary path for spur canceling, the proposed QS-PFD eliminates the need for sacrificing the loop bandwidth and/or sacrificing the VCO gain to obtain higher spur suppression. The auxiliary path reuses the current from the main path, incurring no extra power, and enables fast settling. Fabricated in a 40 nm CMOS technology, the proposed 40 GHz PLL demonstrates –75-dBc spurious tone, minimum 121.9-fs_{rms} integrated jitter when the jitter is integrated from 10 kHz to 100 MHz, with compelling FoM of −245 dB and FoM_{JRP} of −239.8 dB. Therefore, the proposed PLL has the potential to be employed for recent emerging high-performance millimeter-wave applications.

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