NANYANG TECHNOLOGICAL UNIVERSITY

A LOW-OFFSET SMALL-AREA MICROPOWER CHOPPER-STABILIZED INSTRUMENTATION AMPLIFIER DEDICATED TO SENSOR APPLICATIONS

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LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
AFE	Analog Front-End
DTMOS	Dynamic Threshold Metal Oxide Semiconductor Transistor
Op Amp	Operational Amplifier
DDA	Differential Difference Amplifier
IA	Instrumentation Amplifier
LPF	Low Pass Filter
CMRR	Common-Mode Rejection Ratio
$CMRR_d$	Differential Common-Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
PSR	Power Supply Rejection
INS	Injection-Nulling Switch
ICMR	Input Common-Mode Range
SNR	Signal-to-Noise Ratio
GBW	Gain-Bandwidth Product
CSR	Current Source Replica

SUMMARY

This dissertation presents a new low-offset, small-area micropower chopper-stabilized instrumentation amplifier (IA) dedicated to sensor or sensor array interface circuitry in commonly-used sensors such as the Wheatstone bridge and two-input floating sensing element. The IA system comprises a differential difference amplifier (DDA) to sense floating small signals, a current source replica (CSR) circuitry which facilitates the pair matching layout for all critical pairs in DDA input stage such as the input transistors, current sources as well as the current mirror transistors for better matching characteristics, continuous-time injection-nulling switch (INS) with modified control clock choppers to reduce residual offset. The advantage of the proposed DDA with CSR facilitating the pair matching layout over conventional DDA design is that the pair matching layout is not limited to the input transistors pairs. An analysis on common-mode signals and differential common-mode signal in chopper-stabilized DDA is given. The proposed CSR serves dual functions: (1) to reduce the output ripple by generation the offset current nulling operation, (2) to improve input offset by enhancing the differential common-mode rejection ($CMRR_d$) of the DDA, so that it offers better immunity to the differential-common mode signal that is not modulated by the chopping operation. Besides, high power supply rejection (PSR), low noise, micropower regulators are proposed in the work as the regulated power supply to power the proposed IA. The proposed regulators are based on op-amp-less architectural design which embodied the Brokaw bandgap regulator circuit in an additional feedback control loop so as to achieve high efficiency in terms of referenced PSR bandwidth per current. Another proposed regulator uses native composite power transistor and an on-chip native MOS capacitor in the pre-regulator to enhance broadband high PSR performance. Besides, a pseudo-resistor based low-

pass filter is used to reduce the Brokaw's voltage regulator circuit nosie. The IA system and high PSR regulators were fabricated using GLOBALFOUNDRIES 1.8V/3.3V CMOS 0.18µm process. The IA includes CSR circuit, biasing circuit and clock generator occupies an area of only 0.125mm^2 whilst drawing 22µA at a supply of 1.8V. The IC has been experimentally tested. It achieves an input-referred dc offset of 1.78µV (mean+standard deviation) at the chopping frequency of 10kHz. For a closed-loop gain of 40.17dB, the output ripple is reduced by more than 3 times with respect to the reference INS chopper DDA without CSR circuit. At 10Hz, the DDA exhibits an open loop gain of 89dB, a phase margin of 54.1º at a unity gain bandwidth of 225kHz and a load of 220kΩ//56pF, a CMRR of 120dB and an input-referred noise of 62nV/√Hz. The proposed DDAs are dedicated to sensor circuit applications. They are compact whilst providing well-balanced performance metrics in area, offset, noise, power and bandwidth efficiency. Lastly, the proposed IA with the high PSR regulator has been tested with an emulated strain-gauge sensor to show its functionality as a data-acquisition block for small-signal amplification. The proposed IA system is able to achieve an input-referred noise of 3.76µVrms for 2kHz bandwidth, a SNR of 64.4dB and excellent power rejection capability of more than -46dB even at a high frequency of 500kHz. This indicates that the proposed IA system is suitable for use in micropower sensor applications that require low-power, low-noise, low-offset as well as small-area performance whist providing excellent immunity against the power supply fluctuation from external environmental influence. Therefore, the proposed strain gauge sensory system will be very useful for environmental monitoring system.

CHAPTER 1

INTRODUCTION

1.1. Motivations

Recent study reported growing demand for sensors in the US market, which is expected to increase from $9.7 billion in 2009 to $13.1 billion in 2014 [1]. With the advanced pace of development in integrated circuit and micro-system technology, the use of on-silicon precision sensor applications have expanded towards multiple new transducer applications. The importance of accurate measurement of process parameters during the past few decades is highlighted by the application of electronics to instrumentation technology, producing unparalleled diversity of measurement. The development of microprocessor controllers for multi-input and continuous-operation systems makes even greater demands for parallel, reliable and accurate measurement process. The recent neuroprosthetic device [2, 3] makes use of brain signals to control an external computer through the brain-machine interface, showing that the mind-controlled machine concept is no longer a dream with highly stringent amplifiers readily available.

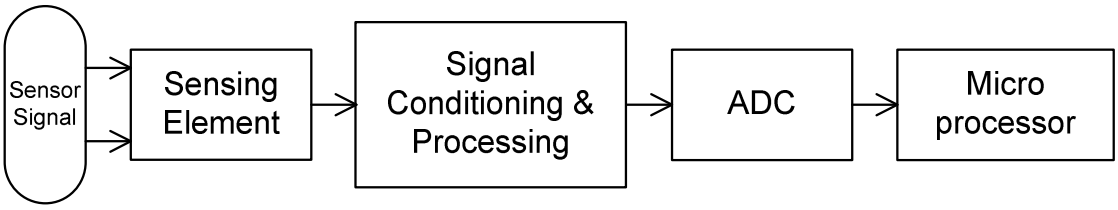


Figure 1.1 Generic integrated sensor system

A generic integrated smart sensor system is shown in Figure 1.1. In a sensor system, the sensing element or the transducer such as resistor, capacitor, transistor, piezo-electrical material, photodiode, or resistive bridge is used to acquire physical, biological or chemical input and converts them into an electrical or optical signal for monitoring. Different kinds of sensor are developed to allow optimal extraction of information about the state of variable quantities such as temperature, pressure, force, strain, velocity, acceleration and displacement in application. However, the collected weak physiological signals produced from the sensing element are easily influenced by noise or interference.

Hence these signals need to be processed and conditioned to be usable. These functions are carried out by the instrumentation system. The signals will be amplified, linearized and filtered through various blocks, necessary to provide the corresponding measurement. The conditioning circuitry involved will govern the performance of the sensor based on appropriate parameters to the application e.g. gain, offset, linearity and sensitivity. Subsequently the signal, now usable, will then be transformed into digital format by ADC (analog-to-digital converter) so that it can be processed and analyzed efficiently by a microprocessor or computer. The information can be used by either a person or an intelligent device monitoring the activity to make decisions that maintain or change a course of action.

As a result, the signal conditioning or data acquisition system requires a carefully designed precision amplifier in practice. Precision amplifiers used for specific measurement purposes are commonly known as instrumentation amplifiers (IAs) which have the basic requirements as follows:

1. The physiological process to be examined is not influenced by the amplifier (or system).

2. The measured signal should be handled by the amplifier having good quality signal-conditioning, which means that input signal should not be degraded after the amplification process. Hence, low noise, low offset, high CMRR, and high gain for the amplifier are very crucial.

3. The amplifier needs great immunity against supply voltage variation in context of measuring minute input signal under continuous fluctuation of environmental noise.

4. The amplifier should have good ESD (electrostatic discharge) protection as well as other safety precautions against damages due to high input voltages.

Realization of different types of instrumentation amplifier in the sensor signal conditioning system can provide readout function with respect to individual sensor properties and applications. Figure 1.2(a) illustrates an example of the standard amplifier circuit for the Wheatstone bridge pressure sensor [4]. Pressure sensors are widely used in manufacturing process industries to control machinery and in commercial flight for airflow measurement. Another sensor application example of the precision amplifier is shown in Figure 1.2(b) for use in sensing signals from a micromachined soil moisture sensor [5]. This sensing application requires a good sensitivity instrumentation amplifier to sense very small change in the voltage signal arising from the moisture information. Hence this imposes stringent requirements in designing a high gain, low noise and low offset sensing preamplifier.

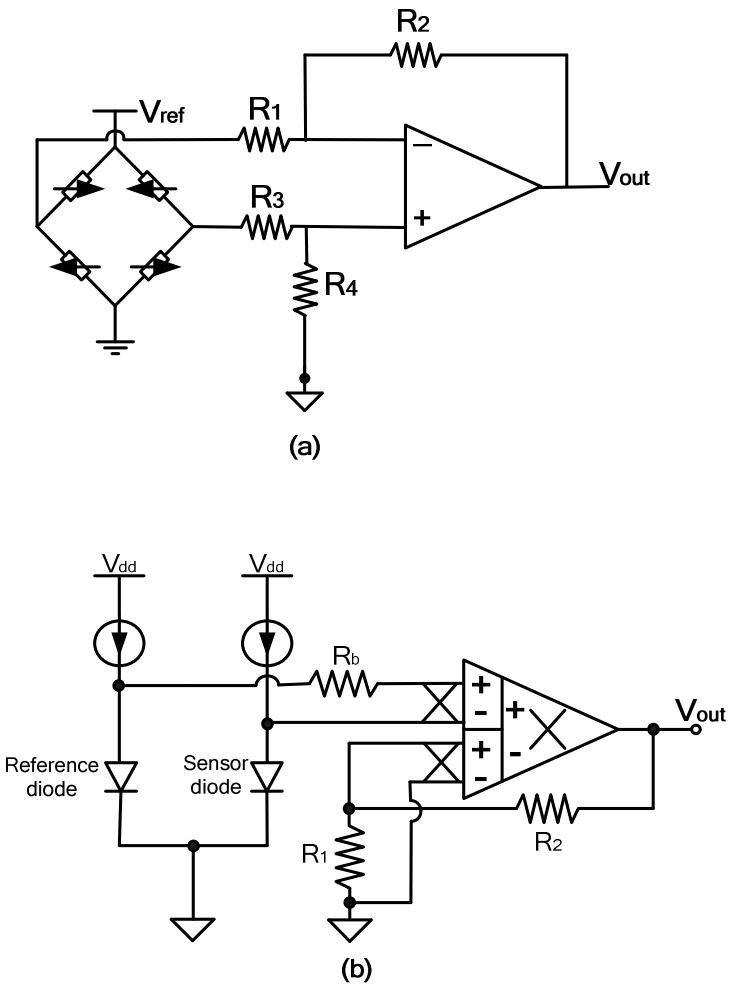


Figure 1.2 (a) Wheatstone bridge pressure sensor with standard difference amplifier circuit (b) Micromachined soil moisture sensor with chopper-stabilized differential difference amplifier (CHSDDA)

CMOS instrumentation amplifiers (IA) are highly demanded for sensor circuit applications, for example integrated biosensors [6, 7], integrated strain sensors [8] and MEMS sensor arrays [9]. These sensor microarrays consist of sensing elements with more than one front-end circuit for accurate parallelism of signal processing. In addition, low power dissipation in the microarrays is highly desirable to prolong battery life especially for implantable or portable devices. Hence this leads to the need for low power and small area IA design, which are particularly important for the development of chip scale sensor arrays with multi-channel sensing systems [10, 11].

Apart from the essential characteristics of being small area and low power, other characteristics such as low offset, low noise and high common-mode rejection ratio (CMRR) are also critical in implementation of precision instrumentation amplifiers of the data acquisition system. As the IA dictates the dominant noise, offset performance, the chopper-stabilization technique can be used to reduce the low frequency 1/f noise and the DC offset. However, the amplifier's initial DC offset is modulated to chopping frequency, appearing as ripple at the amplifier's output. The chopping operation will also cause an additional residual offset at the output of IA.

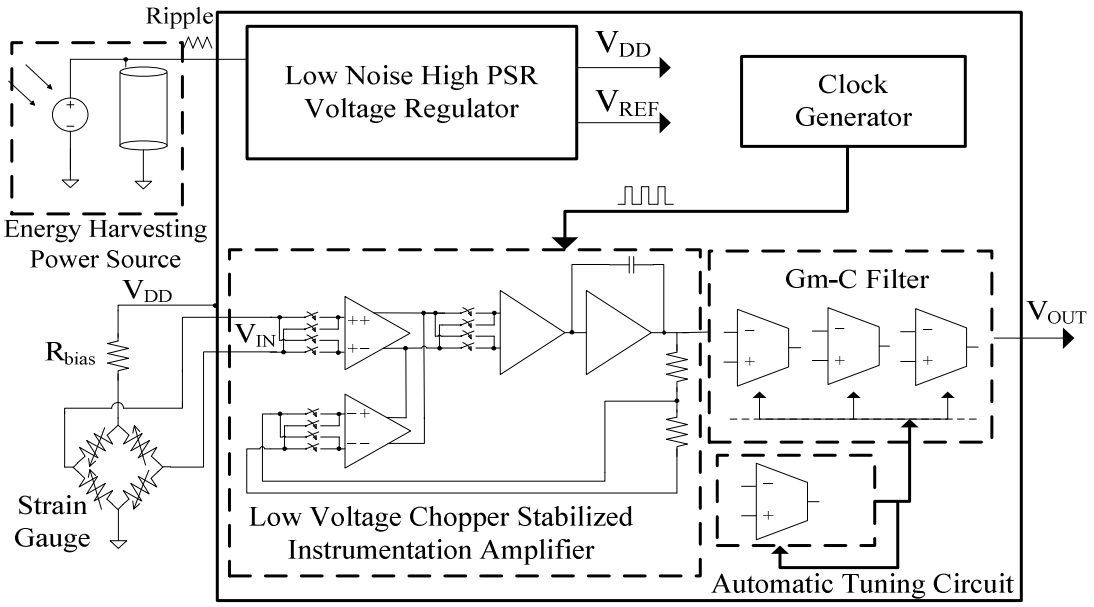


Figure 1.3 Example of an energy harvesting sensory system for environmental monitoring application

Figure 1.3 shows the block diagram of an energy harvesting sensory system for environmental monitoring. The instrumentation system consists of a regulator, chopper stabilized IA, as well as several other auxiliary blocks. In emerging applications such as a wireless sensor node that relies on environmental energy harvesting technologies, the power source may not be stable all the time. For small signal sensing, the front-end interface should have strong immunity against supply disturbances as much as possible. As a result, the

instrumentation amplifier system needs high power-supply-rejection (PSR) to enable the amplifier circuit to operate reliably under different levels of energy source. This could be achieved by having the high PSR regulator block consume small quiescent current and low noise performance. However, the micropower design always conflicts with high PSR performance metric. These two conflicting requirements present the design challenges of a micropower regulator for achieving the high PSR in sensory systems.

1.2. Objectives

The objectives of this thesis are to investigate circuit techniques for the design and realization of a resistive-based micropower chopper-stabilized instrumentation amplifier with low-offset, low-noise, small-area and good PSR for sensor signal-processing applications. They are given as follows:

1. Review and foundation study on low noise, low offset design techniques for precision analog circuit design. This leads to the proposed micropower instrumentation amplifier system which will utilize the chopper-stabilization technique on the basis of its significant advantage over its counterparts in the context of low-noise design as the primary emphasis factor.

2. Investigate circuit techniques and an architecture that can reduce the residual offset and output ripple which appear at the output of the micropower CMOS chopping instrumentation amplifier, with the ultimate goals of achieving low noise, low DC offset, small area, high precision, and good power-bandwidth efficiency, emphasising on small sensor signal processing applications.

3. Investigate different innovative high-performance blocks that support the operation of the instrumentation amplifier in the system. This leads to the analysis of new circuit blocks such as the high power rejection and low noise regulator.

4. Design, simulate, layout and test the proposed instrumentation amplifier. The performance of the chopper-stabilized instrumentation amplifier will be compared with other state-of-art works.

5. Integrate and test the proposed instrumentation amplifier, the supporting blocks i.e. high power rejection regulator together with an emulated Wheatstone-bridge sensor for functionality verification for sensor applications.

1.3. Major Contributions of the Thesis

A number of contributions have been made. The contributions of this dissertation are summarized as follows:

1. Two novel micropower high PSR voltage regulators dedicated to the proposed instrumentation amplifier system has been designed, fabricated and tested. They are on the basis of op-amp-less architecture design with the embodiment of the Brokaw bandgap reference circuit in an additional feedback control loop to achieve high efficiency in terms of referenced PSR bandwidth per current. In another regulator design, output noise reduction technique with pseudo-resistor based low-pass filter and broadband PSR design consideration have been proposed in the circuitry. This further improved the noise performance of the regulator.

2. Small-signal analysis of the power noise ac signal to regulator's output is provided in the thesis which gives the insight of high PSR with respect to design parameters.

3. A dual gate-bulk driven input differential pair with folded-telescopic cascade structure is proposed for low noise, high gain differential difference amplifier design. The effective transconductance of the differential pair is enhanced for noise performance whilst consuming the same power dissipation as in classical differential pair design. Besides, the power-bandwidth efficiency gain structure is proposed for low-power low noise design.

4. An analysis on common-mode signals and differential common-mode signal in chopper-stabilized DDA is given in the thesis.

5. A micropower low offset chopper-stabilized differential difference amplifier with ripple reduction circuitry having area efficiency is proposed. The proposed chopping differential difference instrumentation amplifier uses an injection-nulling switch chopper to reduce offset, a proposed current source replica (CSR) circuit that facilitates the pair matching layout for all critical pairs in DDA input stage. Therefore, it suppresses the output offset ripple.

1.4. Organization of the Report

Following this introduction, the subsequent chapters are organized as follows. Chapter 2 reviews different instrumentation amplifiers and low noise circuit techniques such as the auto-zero and chopper-stabilization techniques. This is then followed by residual offset reduction methods. Lastly, ripple-reduction techniques are reviewed.

Chapter 3 presents a review of PSR performance in op-amp based and op-amp-less based CMOS regulators. A high PSR, low quiescent voltage regulator is proposed. The small signal-analysis on the PSR frequency response is conducted. Furthermore, it proceeds to another low noise, low quiescent regulator but having broadband high PSR for micropower sensors as the second proposed design. High broadband PSR design considerations as well as low noise design techniques are discussed.

Chapter 4 presents the proposed low offset and ripple reduction chopper stabilized IA architecture. An analysis of common-mode signals and differential common-mode signal in the chopper-stabilized differential difference amplifier is given. Finally, the continuous-time injection nulling switch (INS) chopper modulator is presented.

Chapter 5 describes the proposed gate-bulk driven DDA with folded telescopic cascade topology DDA design. The chopper-stabilized DDA comprising the gate-bulk driven DDA, folded telescopic cascode gain stage, and a pseudo class AB output stage as well as a proposed current source replica (CSR) circuit that facilitates the pair matching layout for all critical pairs in DDA input stage.

Chapter 6 shows the digital blocks, specifically the non-overlapping clock design, as well as the injection nulling switch (INS) control clock circuits.

Chapter 7 discusses the layout considerations, including the mixed-signal layout issues such as matching and noise shielding, as well as floor planning and chip layout.

Chapter 8 presents the results and discussions. They are the measurement results and discussions for the regulators, the statistical simulation verifications, the measurement results for the proposed chopper-stabilized IA as well as the strain gauge sensory system using a

Wheatstone bridge with the proposed micropower regulator and chopper-stabilized DDA with ripple reduction.

Chapter 9 draws the conclusions, and discusses the future work.

CHAPTER 2

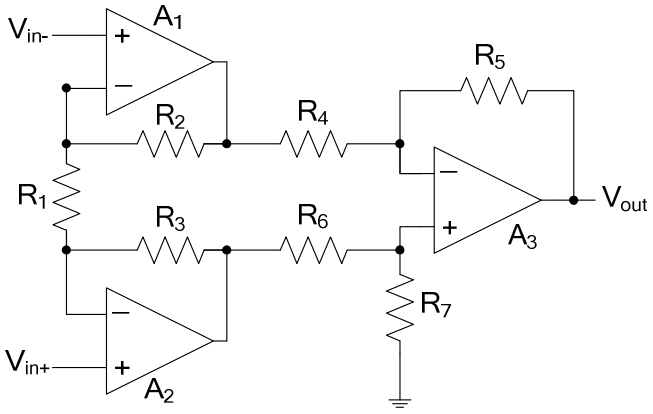
LITERATURE REVIEW FOR LOW-NOISE, LOW-OFFSET INSTRUMENTATION AMPLIFIERS

The challenge in building a readout front-end system is the instrumentation amplifier (IA), the most important building block in the interface circuit. This is because characteristics such as the input-referred noise, offset performance as well as the common-mode rejection ratio (CMRR) of the front-end data acquisition system are determined in the IA. Realization of different types of instrumentation amplifier in the sensor signal conditioning system can provide readout function with respect to individual sensor property and application.

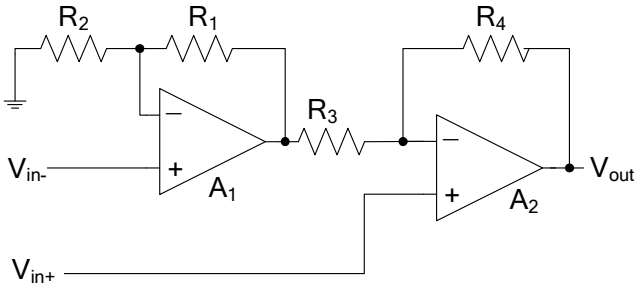
2.1. Review of Instrumentation Amplifier Architectures

A quality IA should exhibit very small DC offset voltage as well as high rejection to the common-mode signals from the sensors. IA architectures can be broadly classified into either resistive-based [12, 13] or capacitive-based IAs [14]. The capacitive coupling instrumentation amplifiers with capacitor feedback [15-17] are examples of power efficient capacitive-based IA as they only need a single input pair to provide floating signal sensing. Meanwhile, examples of the resistive-based IA include the traditional 3 op-amp IA, 2 op-amp IA and the differential difference amplifier (DDA), which is also known as the indirect current feedback IA. Resistive-IAs have the advantage of being less sensitive to capacitive parasitics. They are also flexible with gain setting using external resistive components.

2.1.1. Conventional Resistive Feedback Instrumentation Amplifier



(a)



(b)

Figure 2.1 Conventional resistive-feedback instrumentation amplifiers (a) The conventional 3 op-amp resistive feedback IA (b) The 2 op-amp resistive feedback IA

The traditional 3 op-amp topology is shown in Figure 2.1(a). A 2 op-amp IA, shown in Figure 2.1(b), can be used to provide high input resistance. In the 3 op-amp topology, two op-amps are used to implement a floating gain stage, followed by a third one configured as a differential amplifier [18]. The first gain stage provides unity common-mode gain and majority of the differential gain whereas the second stage provides either unity or small differential-mode gain and all of the common-mode rejection. The overall gain is given by

$$A_d = (1 + \frac{2R_2}{R_1})\frac{R_5}{R_4} \tag{2.1}$$

Consider the traditional 3 op-amp configuration, it needs highly matched resistors for high CMRR. Since the output impedance of the output stage should be low to drive the resistors of the instrumentation amplifier network, this results in large current consumption and power drain in the operational amplifiers. This is undesirable in low power design.

In resistive feedback, the CMRR is limited by the degree of matching in the resistors. Hence, any mismatch in resistive value will degrade the CMRR performance of the circuit. In the case where a high pass filter is added at the input of the 3 op-amp IA to reduce dc offset, the CMRR performance will be even worse. This is due to having to match capacitors and resistors [19]. Trimming is therefore employed for high CMRR application but it increases the test cost substantially.

2.1.2. Current Feedback Instrumentation Amplifier

A typical current feedback IA consists of an input transconductor (i.e., voltage-to-current converter), an output transconductor, and one or more high gain feedback loops using resistor-feedback network. If a single feedback loop is applied around both transconductors, the IA may be classified as either direct or indirect current feedback. In the current feedback IA design approach, higher operating bandwidth is possible when compared to the conventional resistive feedback approach. [19] Besides, it can achieve higher CMRR performance when both isolation and balancing techniques are employed [20] in the feedback loop.

2.1.2.1. Direct Current Feedback IA

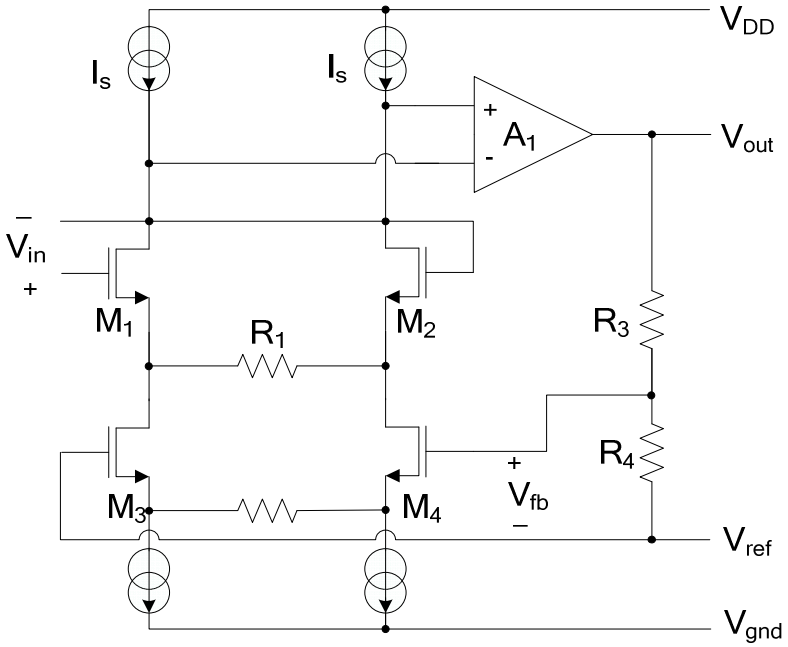


Figure 2.2 Direct current feedback IA

An example of the direct current feedback IA is shown in Figure 2.2 where the resistive-feedback voltage is fed to the transconductor (bottom one) in the main input branch [21]. The differential input amplifier that used to sense the input signal is formed by the transistor pair M_1 and M_2. The transistors M_3 and M_4, which are the current sources for the input transconductor formed the feedback transconductor. However, in the direct current feedback IA, the two transconductors are stacked and this limits the input common-mode voltage range and the minimum supply voltage [22]. The disadvantage of this setup is that two accurate V-to-I converters are needed to obtain an accurate and linear transfer function. The stacking of the two V-to-I converters reduces the input common-mode range.

2.1.2.2. Differential Difference Amplifier (Indirect Current Feedback IA)

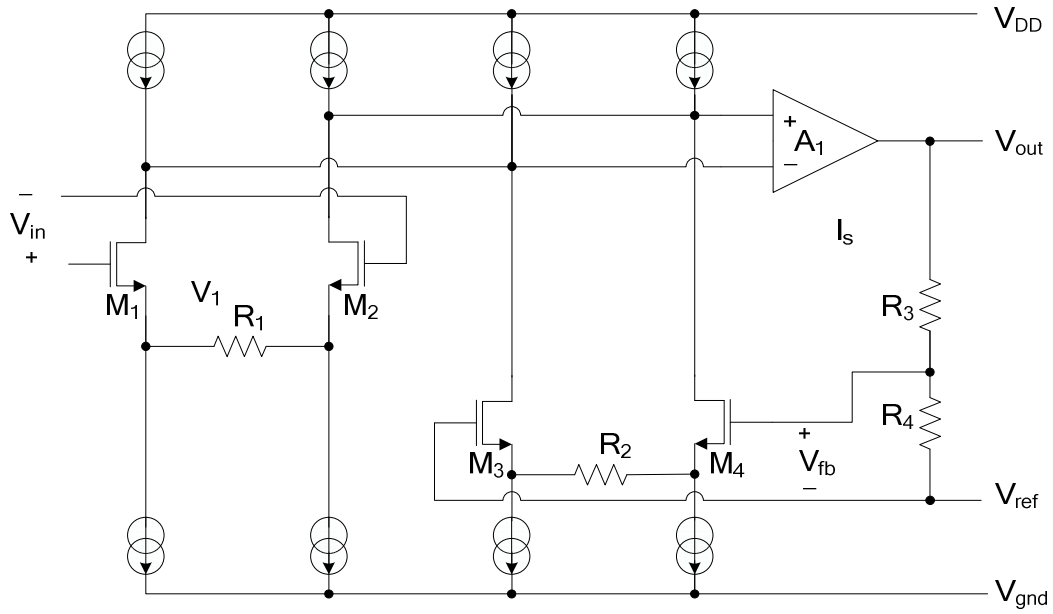


Figure 2.3 Indirect current feedback IA

The differential difference amplifier, DDA [23] first introduced in 1987 has been widely used in analog circuits such as voltage comparator with floating inputs, level shifter, voltage inverter without external resistors and instrumentation amplifier [23, 24]. It is also known as indirect current feedback IA [22], shown in Figure 2.3. The term "indirect current" is used because the output voltage is not directly fed back to the input of the amplifier, but to the input of a second stage feedback transconductor as compared to the direct current feedback method.

The symbol for the DDA proposed by Sackinger, with 4 input terminals V_{PP}, V_{PN} , V_{NP} and V_{NN} is shown in Figure 2.4. V_{PP} and V_{PN} are designated as the input terminals for the non-inverting input port whereas, V_{NP} and V_{NN} are designated as the input terminals for the inverting input port.

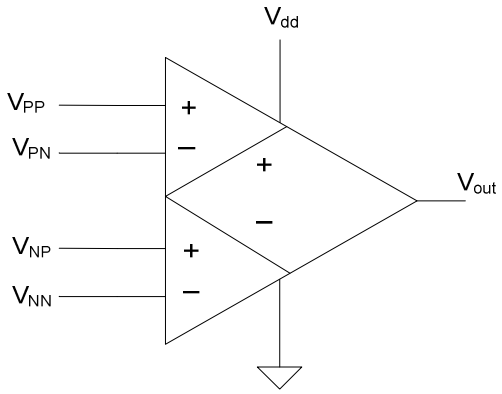


Figure 2.4 Symbol for the differential difference amplifier

Analogous to a normal operational amplifier, DDA compares the difference of the non-inverting input port (V_{PP} and V_{PN}) and the inverting input port (V_{NP} and V_{NN}) under the condition of negative feedback. The functional relationship of the input ports is

$$V_{PP} - V_{PN} = V_{NP} - V_{NN} \tag{2.2}$$

The ideal DDA compares the floating voltages, and amplifies the differential voltage between them with its open loop gain. The output is given as

$$V_O = A_O[(V_{PP} - V_{PN}) - (V_{NP} - V_{NN})] \tag{2.3}$$

where A_O is the open loop gain of DDA.

The inherently differential inputs of DDA are suitable for instrumentation amplifiers. The inverting resistor feedback topology is employed in the implementation of the IA as shown in Figure 2.5. The closed-loop gain can be conveniently set by the overall feedback resistor ratio. This yields

$$V_{out} = V_{in}\left(\frac{R_2}{R_1} + 1\right) \tag{2.4}$$

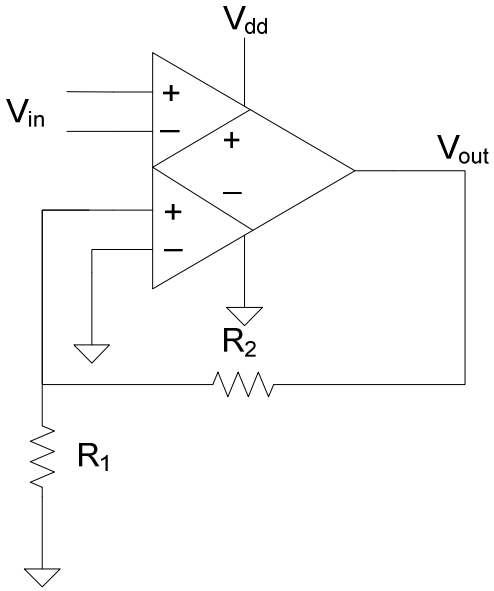


Figure 2.5 Instrumentation amplifier using DDA

The advantages of the differential difference amplifier over the conventional resistive-feedback structures are that it eliminates the resistor matching as well as simplifies the front-end circuit design. However, the matching for CMRR is now translated from the resistor pair to the critical device pairs such as the input differential pair and the active load pair inside the DDA.

In short, although the resistive-based amplifier architectures suffer from relatively larger power consumption than their capacitive-based counterparts, they display relatively less dependence on capacitive parasitics whilst permitting ease of external gain programming function. In this work, we will focus on the DDA for instrumentation amplifier applications.

2.2. Review of Low-Noise and Low-Offset Circuit Techniques for IAs

The instrumentation amplifier, as the most important block of the front-end data acquisition systems dictates the dominant noise. The low-frequency sensor signal amplification design in CMOS circuits is subject to contamination due to the 1/f noise and DC offset voltage. As the 1/f noise dominates at frequencies below the corner frequency, it has more impact on the performance in low frequency applications when compared to the thermal noise. Hence extra techniques are necessary to reduce the influence of 1/f noise.

Furthermore, an offset voltage of 10mV to 30mV is typical for CMOS amplifiers which cannot be tolerated in small signal sensing applications. It is normally caused by the mismatch of the devices parameters i.e. size, threshold voltage and bias current. Classical approaches for low-offset MOS op-amps through device optimization are inefficient and have performance limitations. As a result, this led to the invention of some dynamic offset cancellation techniques to reduce the effect of these contaminations. Currently, there are two popular circuit techniques for the design of low-offset low-noise amplifiers, namely the Auto-Zero (AZ) technique [25] (or its variant, known as Correlated-Double Sampling (CDS) technique) and Chopping Stabilization (CHS) technique [25, 26]. There are distinctions between the two methods. Although each technique has claimed its relative advantages and disadvantages, both AZ and CHS aim to eliminate the 1/f noise.

2.2.1. Auto-Zero Technique

The auto-zero technique was introduced for designing high precision amplifiers especially in switched-capacitor transducer designs. The auto-zeroing method [25] uses sampling technique to cancel out the noise/DC offset of the amplifier where the unwanted noise is sampled and subtracted from the input or output of the op-amp. Utilizing the sample and hold idea, the auto-zeroing method is particularly useful for application of switched-capacitor based instrumentation amplifier designs [27, 28].

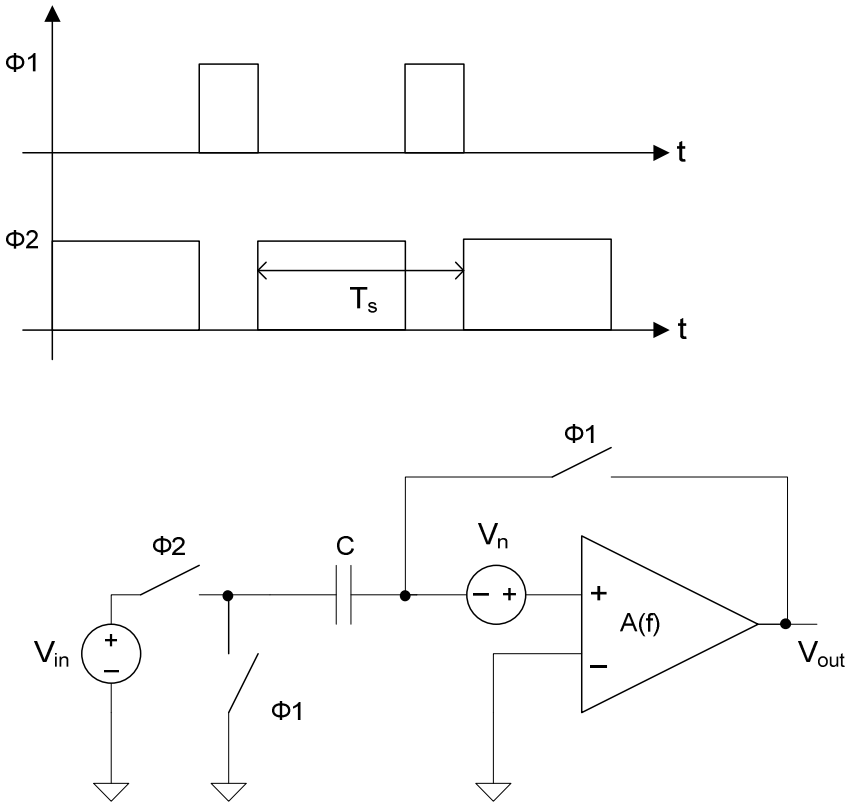


Figure 2.6 Auto-zero amplification principle [26]

The basic auto-zero amplification principle along with the two clock phases (Φ1 and Φ2) are shown in Figure 2.6. There are two phases involved in the process, namely the sampling phase (Φ1) and amplification phase (Φ2). In the sampling phase Φ1, the output and input of the amplifier are shorted together. Hence, the amplifier's offset error is sampled and stored in capacitor C. In the amplification phase Φ2, the error signal sampled is cancelled

during the operation. As the sampled noise during Φ1 and the low-frequency continuous noise at the phase Φ2 are highly correlated during a sampling period, the l/f noise is removed.

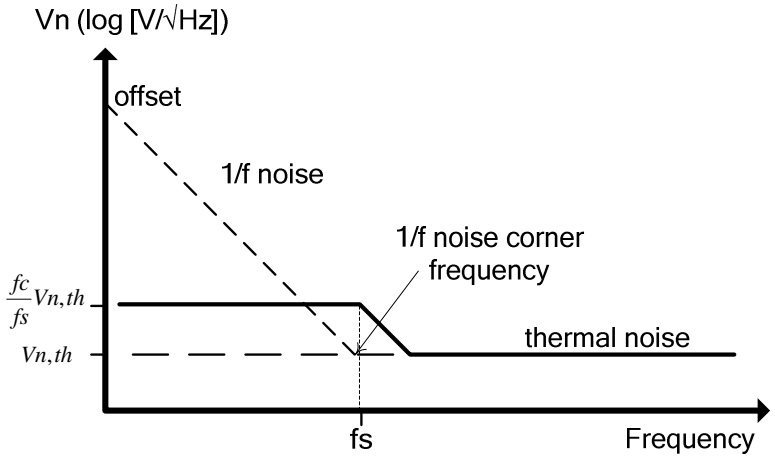


Figure 2.7 Noise power spectrum for operational amplifier using Auto-zero technique

However there is a disadvantage of using the auto-zeroing technique. As shown in Figure 2.7, the residual noise at low frequency, f_s is not equal to the thermal noise floor even though it is almost white. It is increased by the ratio of the unity gain bandwidth of the amplifier f_c and the auto-zeroing frequency f_s.

$$V_{n,low_{frequency}} = \frac{f_c}{f_s} V_{n,th} \tag{2.5}$$

The reason for this increased residual noise is the high-frequency components being folded back to the baseband during sampling phase. As a result, higher sampling rate is needed to reduce the noise-folding problem. This in turn requires a relatively fast op-amp that consumes higher power. Thus, it may not meet the primary low-noise and low-power design objectives.

2.2.2. Chopper-Stabilization Technique

The other method used in the design of low offset instrumentation is the chopper stabilization (CHS) method introduced by Goldberg in 1949 [29], with the idea of modulating the signal to high-frequency band, amplifying it and then demodulating back to the baseband in continuous-time operation. It provides a stand-alone op-amp with an advanced effective input offset characteristic.

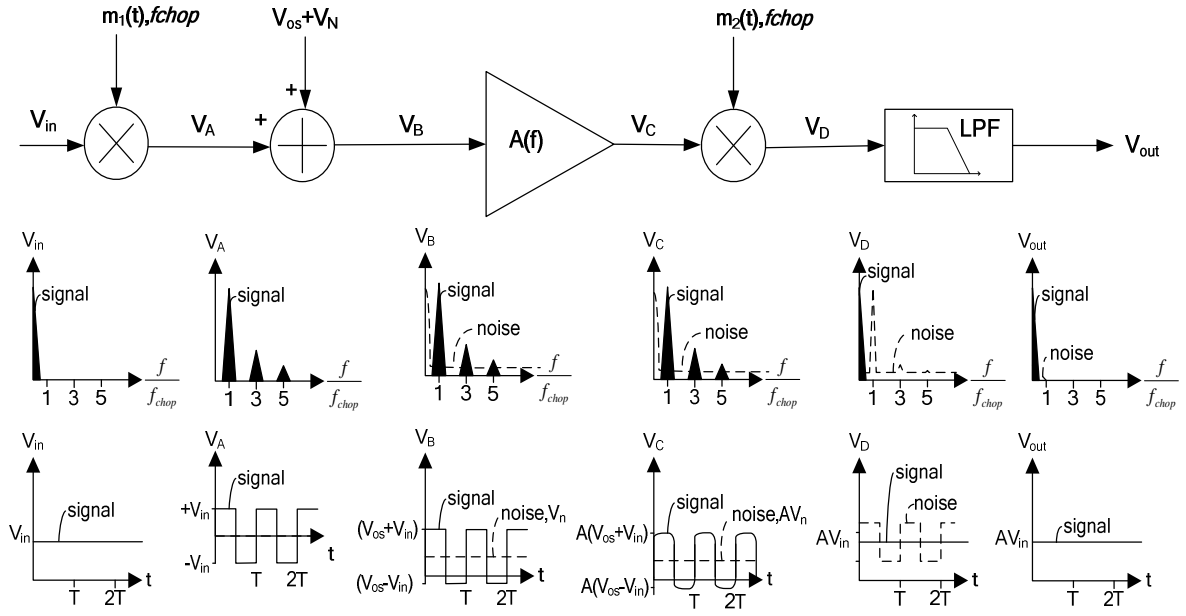


Figure 2.8 Basic chopper implementation and working principle

The basic chopper implementation and its working principle are shown in Figure 2.8 [25, 26]. The low frequency input signal V_{in} is modulated with the chopping frequency, f_{chop} of the square wave signal, $m_1(t)$ to higher frequencies of the odd harmonic of f_{chop}. After that, the signals will be amplified by the amplifier A(f), and demodulated back to baseband frequency as the output voltage, V_{out}. The DC of

fset and noise is modulated only once, and appears only at the chopping frequency and its odd harmonic. The amplified baseband signal will be obtained after passing through a

low pass filter whereas the high frequency components, such as noise and interference will be filtered out.

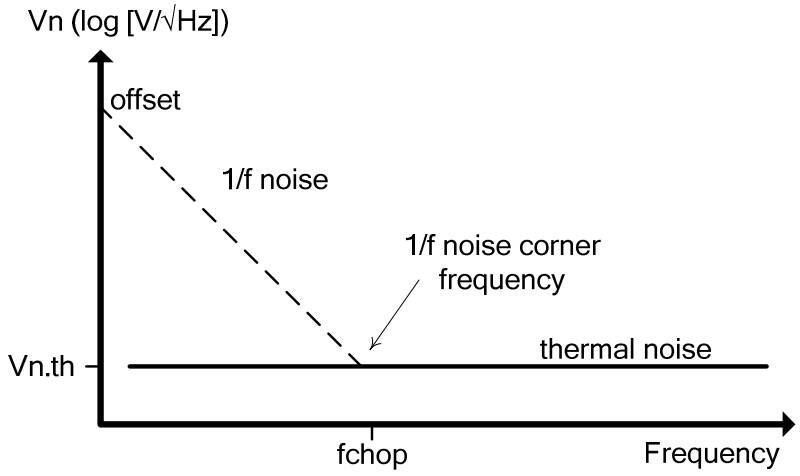


Figure 2.9 Noise power spectrum of operational amplifier using chopper stabilization

From Figure 2.9 it can be seen that the baseband noise is almost equal to the wideband thermal noise. It has a smaller low frequency noise compared to Figure 2.7 which has higher baseband noise caused by the noise fold-back problem. This is because the input signal of the chopper amplifier is not sampled. Hence, wideband thermal noise is not folded back into the baseband as discussed in auto-zero technique. Although it does not suffer from the noise-folding problem like the auto-zero technique, the high frequency amplification consumes significant power. More importantly, the chopping amplifiers tend to be more complex to tradeoff precision. This means that the circuit will have larger area for meeting high performance requirements. The increased power and area are due to the fundamental problems caused by the chopping operation and this will be discussed in sections that follow.

2.3. Review of Residual Offset Reduction in Chopper Stabilized IA

The chopper-stabilization dynamic offset cancellation technique is useful in applications requiring low offset and low noise characteristics as it can remove the DC offset and low frequency 1/f noise effectively as discussed in the previous section. However, the chopper-stabilization circuit suffers from residual offset caused by the non-idealities of the chopping amplifier [25]. The residual offset issue arises from the charge injection effect of input modulator switches. This residual offset due to the first switching event will go through the low pass filter un-cancelled. As a result, several offset reduction techniques are reported to bring the offset to micro or sub-micro volt levels.

2.3.1. High-Q Selective Bandpass Filter for Spike Filtering

The residual offset is generated mainly due to the chopping spike at the first modulator being demodulated to the baseband. As reported by Menolfi et al.[30], reduction of this parasitic offset can be done by inserting a high-Q selective bandpass filter before the output demodulator. With this arrangement, the energy content of the spikes which is mainly located at higher harmonics of the chopping frequency will be removed, while only suffering a little signal loss.

Figure 2.10 shows the block diagram of an instrumentation amplifier with a high-Q bandpass filter together with a matching oscillator. Both modulator and demodulator are controlled by the signals generated from the on-chip oscillator. The center frequency of the bandpass filter is always locked to match the chopping clock frequency generated from the matching oscillator. The bandpass filter is designed to lock its center frequency at the chopping frequency to achieve an offset reduction with a factor of $8Q/\pi$ where Q is the quality factor of the bandpass filter [30, 31]. This technique filters out the spikes generated

from the input modulator and able to achieve a several hundred nano-volt input offset on the basis of having a high quality factor bandpass filter with matched the chopping frequency and the filter's center frequency. However, the gain accuracy in the design is traded-off with the reduction in residual offset.

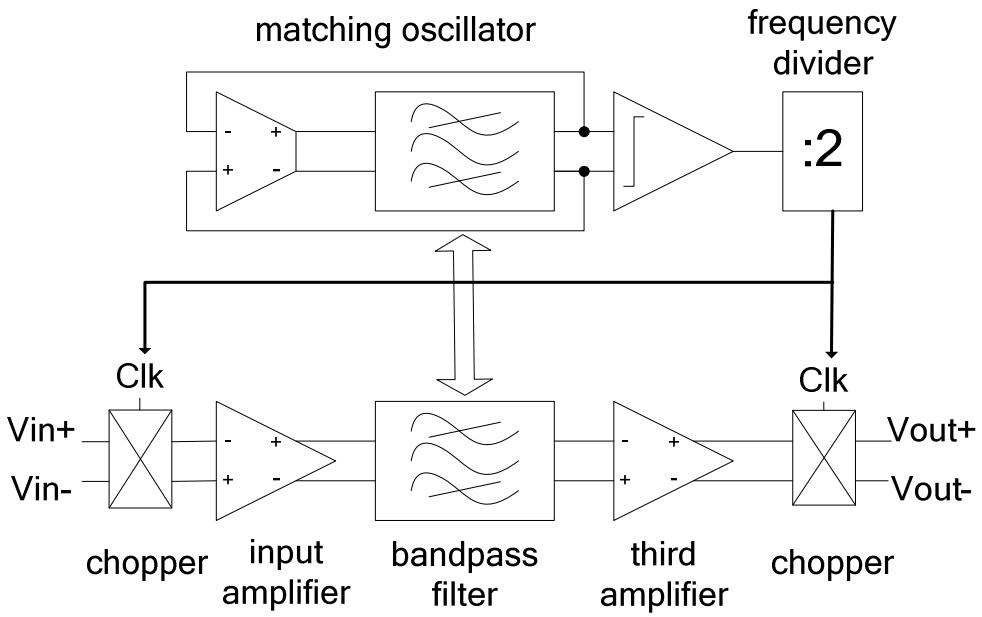


Figure 2.10 Block diagram of instrumentation amplifier with bandpass filtering

2.3.2. Nested Chopper

The nested-chopper was introduced by Baker et al. [32] to achieve low offset performance in chopping instrumentation amplifiers. In addition to the conventional chopper amplifier with single chopping frequency, an extra low-frequency chopper pair is inserted into the conventional one.

Figure 2.11 shows a nested-chopped instrumentation amplifier built by two chopping amplifiers with two chopping frequencies which are $f_{chophigh}$ and $f_{choplow}$. The inner chopper pair is controlled by the higher chopping frequency which is used to remove the 1/f noise and the amplifier's DC offset, while the outer chopper pair with a much lower chopping frequency is for reducing the residual offset. The spikes generated by the high chopping

frequency are modulated by the output chopper at the output without affecting the desired signal and finally a low pass filter is used to remove the undesired high frequency modulated signal. However, this topology limits the maximum input signal frequency to be half of the low chopping frequency $f_{choplow}$ which restricts the bandwidth of the input signal.

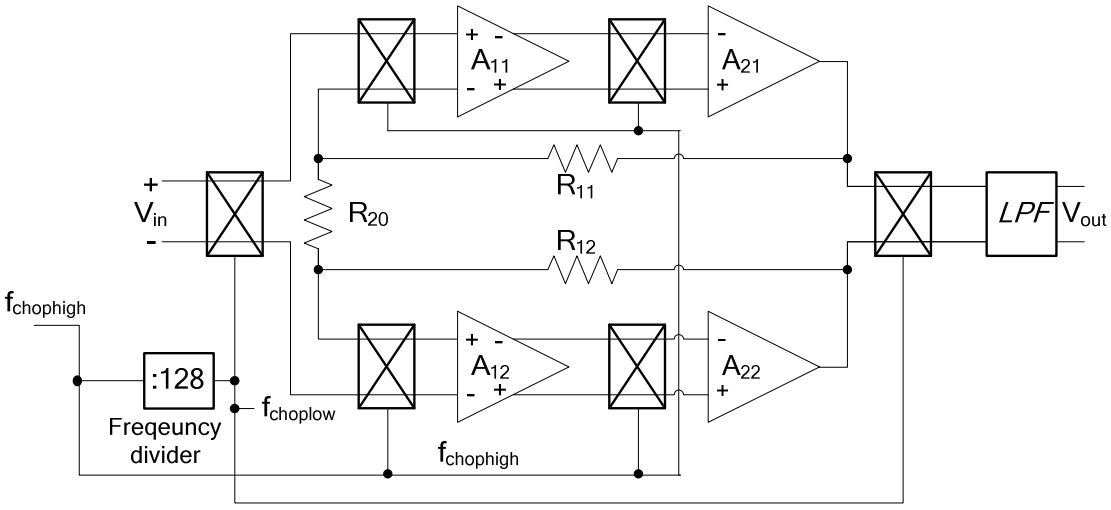


Figure 2.11 A nested-chopper instrumentation amplifier [32]

2.3.3. Multipath Current-Feedback Offset Cancellation

Recent works reported by Witte et al. [33] and Fan et al. [34] have suggested that the chopper offset-stabilized technique in the current feedback instrumentation amplifier make use of high frequency and low frequency paths to achieve very small residual offset performance. Figure 2.12 shows the block diagram of a current feedback instrumentation amplifier with multiple paths i.e. high frequency and low frequency paths. The low frequency path is used to provide low frequency characteristic of the IA where the 1/f noise and DC offset are modulated to the chopping frequency while the high frequency path determines the IA's gain bandwidth product [33]. An integrator G_6 is added in the low frequency path to integrate the difference of output current from G_7 and G_8 such that the integrated output voltage will eventually be injected to the high frequency path to compensate the offset from G_3 and G_4. With this method, the DC offset in the IA will be cancelled.

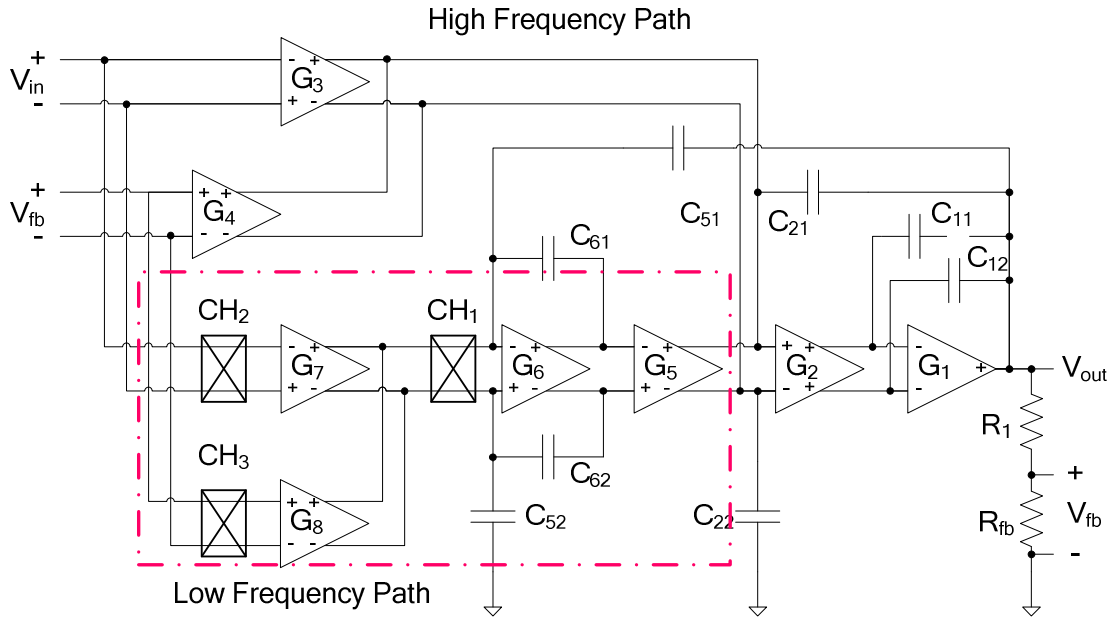


Figure 2.12 Block diagram of a multipath current feedback instrumentation amplifier

However, this comes at the cost of significant increase in design complexity, silicon area and power consumption. Nested Miller compensation network can be used to ensure stability of the instrumentation amplifier. The interaction between the chopped offset of the integrator G_6 and the capacitances at node A and B will cause potential extra residual offset in the design [34]. These circuit architectures are suitable for single sensor circuit but are difficult to extend to large scale sensor array circuits and systems where area is of most concern.

2.3.4. Ping-Pong Architecture with Auto-Zeroing and Chopping Technique

As discussed in Section 2.2.1, the auto-zeroing scheme is useful for switched-capacitor applications to achieve low offset. However, it is not suitable for continuous-time applications. Besides, aliasing occurs in auto-zeroing which increases the DC noise floor in comparison to the chopping operation. In ping-pong architecture, both auto-zeroing and chopping techniques are combined to give low noise as well as low offset performance.

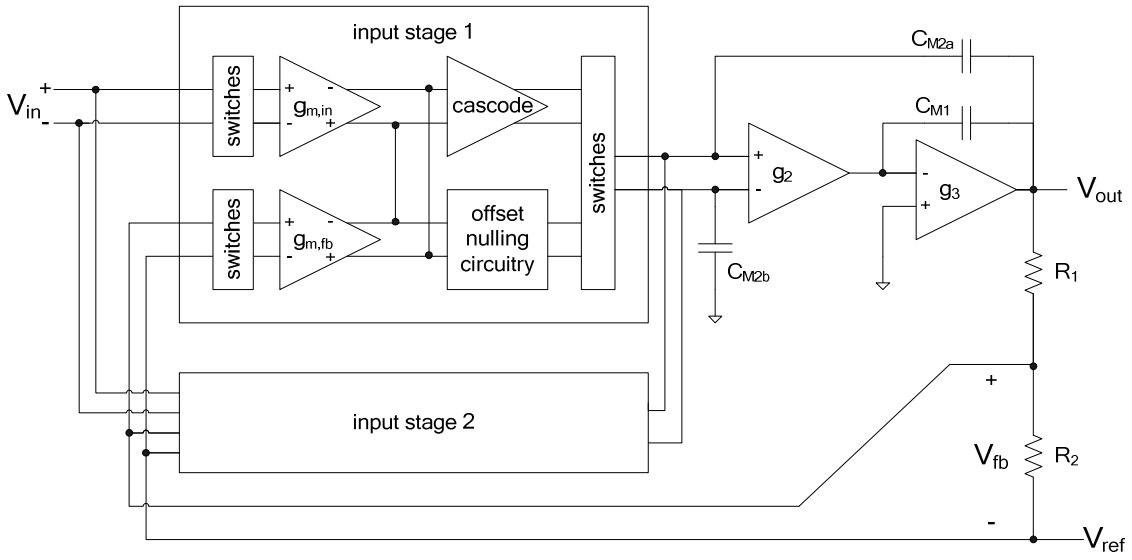


Figure 2.13 Block diagram of the ping-pong auto-zeroing and chopping

Figure 2.13 shows the ping-pong architecture proposed by Pertijs et al. [35] to achieve low residual offset without increasing the low frequency noise density in the auto-zero operation. It consists of 2 identical auto-zero input stages i.e. input stage 1 and input stage 2. They operate in ping-pong fashion as illustrated in the figure. Each of these input stages has 2 input transconductor $g_{m,in}$ and $g_{m,fb}$ for differential signal sensing and offset-nulling circuitry respectively. When the input stage 1 is in auto-zero operation, the input stage 2 will provide the output signal.

However, the large overhead in current consumption is not optimal for micropower applications as the ping-pong topology consumes larger die area and power of the additional input stage. Besides, these circuit architectures may not be suitable for large scale sensor array circuits and systems. This raises the motivation for the investigation and design of a small-area IA.

2.4. Review of Ripple-Reduction Techniques in Chopper Stabilized IA

Besides the residual offset appears at the output of the chopping IA, another issue that comes from the chopper stabilization technique is that it shifts the undesired DC components to the odd harmonics of the chopping frequency which appear as a ripple signal at the output. This section will review various conventional ripple reduction methods.

2.4.1. Internal Low Pass Filter

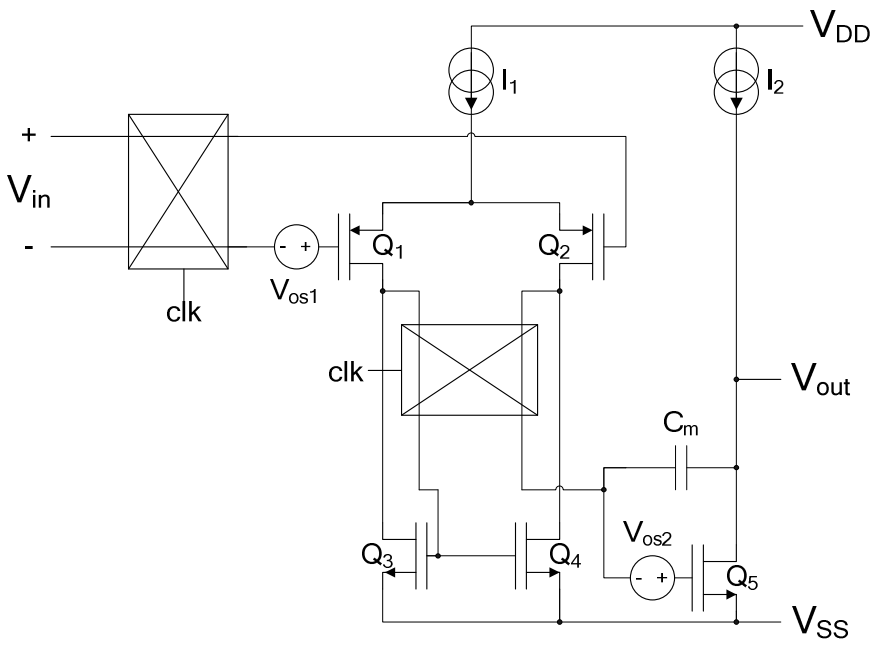


Figure 2.14 Internal filter in conventional chopper-stabilized amplifier

In conventional design, the up-modulated DC offset and 1/f noise can be attenuated by a low pass filter [36]. The low pass characteristic of the operational amplifier can be used as the low pass filter. This can be shown in a multistage amplifier design where the Miller compensation capacitor of the second stage will act as an internal low pass filter [37] illustrated in Figure 2.14. As a result, the output ripple at the V_{out} after the second stage is given by:

$$V_{o,ripple} = V_{os1} \frac{g_{m1}}{\pi f_{chop} C_m} \tag{2.6}$$

where V_{os1} and g_{m1} are the offset and transconductance of the first stage respectively, f_{chop} is the chopping frequency. For a larger chopping frequency, it will result in smaller output ripple but it will cause higher residual offset.

2.4.2. Switched-capacitor Notch Filter

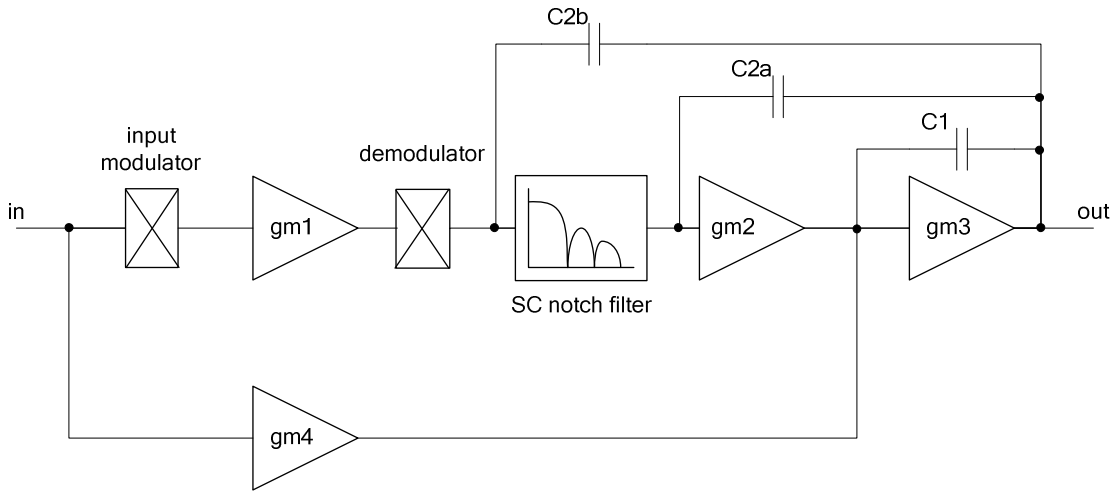


Figure 2.15 Block diagram of the chopper-stabilized op-amp with switched-capacitor notch filter [38]

A number of circuit techniques have been proposed to suppress the output ripple of the chopping amplifier. Burt et al. [38] proposed a switched-capacitor notch filter with synchronous integration inside the continuous-time signal path to null the chopping offset signal for a reduced output ripple. Figure 2.15 shows the block diagram of switched-capacitor notch filter integrated in a high-gain 3-stage operational amplifier with multipath nested Miller compensation. The elimination of the ripple is achieved by integrating the output of gm1 synchronous to the chopping before transferring the signal to the next stage gm2.

Although the filter provides a deep notch for the ripple, a delay during the sample and hold operation which creates the concern in signal transfer operation. Besides, the extra delay

in the switched-capacitor operation also increases design complexity in ensuring the local loop stability in the design [38]. Furthermore, the three-stage amplifier with multipath nested Miller compensation topology reduces the bandwidth efficiency in the design on the basis of many stages are cascaded to obtain high gain which increases the design complexity. Of most important, in the realization of an instrumentation amplifier, two of such amplifiers are required, which will double the silicon area. This may not be the favourable topology for small area IA implementation.

2.4.3. AC-coupled Ripple Reduction Loop

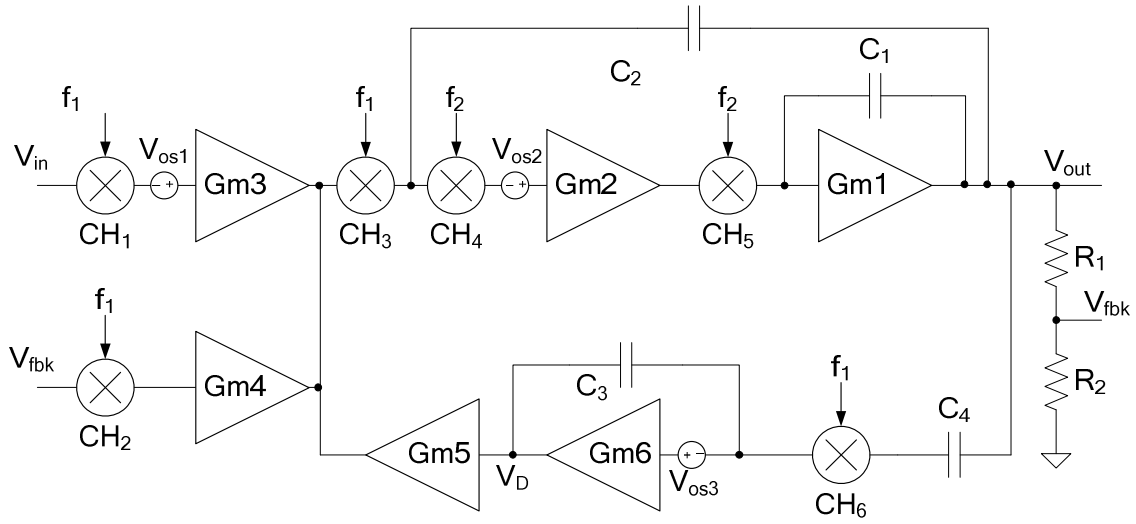


Figure 2.16 Simplified block diagram of an instrumentation amplifier with an AC-coupled ripple reduction loop [39]

Current research works [34, 39] have demonstrated the use of a continuous-time ripple reduction loop to demodulate the amplifier's output ripple and null it by cancelling with the offset of the input stage. The idea of ac-coupled ripple reduction loop is shown in Figure 2.16. The output ripple current is sensed by the extra loop via sensing capacitor C_4. It is then demodulated back with an extra demodulator. Subsequently, the signal is integrated through a current buffer to generate an offset compensation current that is injected to the input of the cascode stage to cancel the DC offset from the input transistors. The design

suppresses the output ripple effectively at the expense of increased design complexity. Hence, it imposes larger silicon area and power consumption for the overall circuit.

2.5. Chapter Summary

This chapter reviewed the resistive-feedback instrumentation amplifier architectures which include the traditional three op-amps IA, direct current feedback IA as well as the differential difference amplifier (indirect current feedback IA). Differential difference amplifier is chosen as the focus of this work over the conventional resistive-feedback structures. It is mainly because it eliminates the resistor matching as well as simplifies the front-end circuit design. Besides, auto-zeroing and chopping techniques have been reviewed in this chapter for low offset and low noise design. Lastly, various published circuit techniques for chopping resistive-feedback instrumentation amplifier have been reviewed in this chapter. These circuit techniques suffer from different problems such as high power consumption and increased design complexity. All these drawbacks suggest that the main task of the instrumentation amplifier is not only to improve CMRR, reduce 1/f noise and offset but also to avoid unnecessary power consumption and address simplicity for area-efficient implementation. These are particularly important especially for large scale of duplication in sensing applications. Therefore, further research work needs to be conducted to devise new architecture together with appropriate circuit techniques which not only permit low-noise low-offset amplifier design, but also provide high precision whilst occupying small silicon area, dissipate as little power as possible and attain high power-bandwidth efficiency. An instrumentation amplifier system having small-size and high-performance will serve as a quality discrete IC product or provide a useful IA circuit block in SOC environment.

CHAPTER 3

LOW QUIESCENT BIAS CURRENT, HIGH PSR VOLTAGE REGULATORS

3.1. Importance of High PSR in Sensor Systems

Recent advancement in integrated circuit technologies is continuously pushing sensory systems towards low-power or autonomous self-powered micro-systems for system-on-chip (SoC) solutions. Following this, sensor systems will tend to migrate from discrete, expensive and inflexible units to smart low-power silicon-based units. This is visible from recent review [40] of various types of sensor and high-performance electronic interfaces which aim at monolithic integration for power-aware and area-efficient smart systems, for example wireless body sensor networks [41].

However, as sensor systems continue to shrink, the battery size is reduced with less battery energy is available on board, leading to shorter device lifetime. To overcome this, various energy harvesting techniques [42-44] have been developed to extract power from solar energy, thermal gradients, vibrations as well as human movement, providing long-lasting solutions for infinite sensor lifetime while decreasing the maintenance cost. This is particularly advantageous in sensor systems with limited accessibility such as wearable, biomedical implants electronics [45, 46] and embedded remote micro-sensors [47]. Since the energy harvesting methods may not be efficient, the micro-system based SoC usually addresses power-aware design and for the analog building blocks of the system.

The power source from energy harvesting technologies tends to be irregular, changing with the environmental conditions. Unlike the power supply from a battery, the energy harvested power source may contain many ac components, including the ripples caused by the charging and discharging of the storage capacitor or the unwanted coupled noise through the switching regulator or the environmental noise picked up through the harvesting devices. As a result, the potentially huge fluctuation that appears in the power source will be harmful to highly-sensitive sensor interfaces [48], instrumentation amplifiers [49, 50], biasing circuits [51] and so on. Besides, in the single chip solution, more than one system resides in the single die all sharing the same supply. With this, the coupling noise from each system will introduce more noise and ripple to the supply line. Hence, it is important to have high power supply rejection ability for the noise sensitive blocks. Figure 3.1 illustrates a general energy harvesting source system that provides power to different types of electronic building blocks needed by a typical sensory system. In this chapter, a new regulator dedicated to micropower sensor circuits is proposed to overcome the problem.

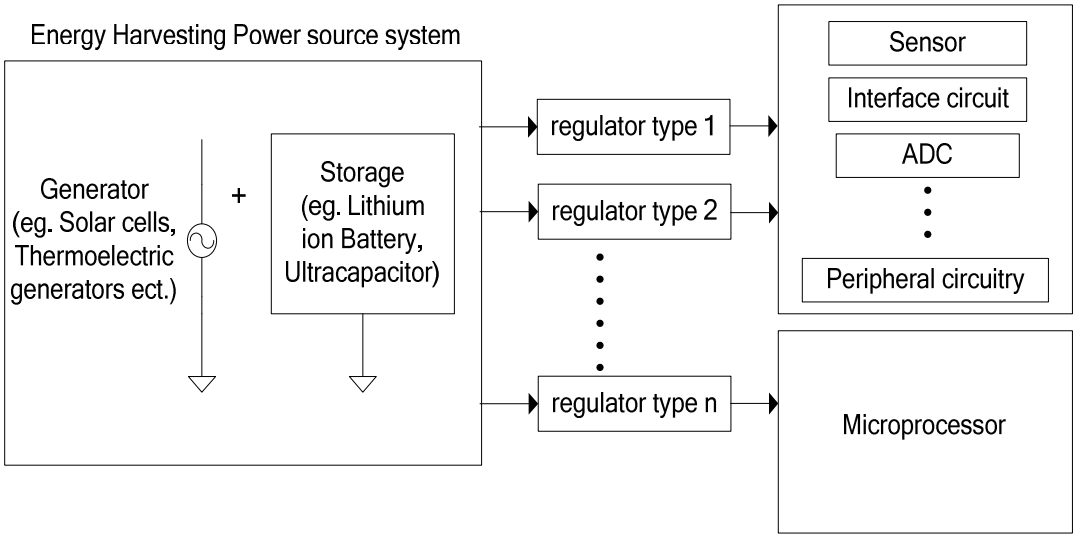


Figure 3.1 Exemplary energy harvesting power source system that powers the electronic building blocks of a sensory system

3.2. CMOS Regulators

The voltage regulator functions to provide a stable power supply independent of load impedance, input voltage variations, and temperature. Hence, regulators are common blocks in the system design for consistent performance with regulated power supply. As mentioned previously, a sensory system requires a voltage regulator to regulate the supply to the internal analog circuitry i.e. instrumentation amplifier which is sensitive to the environmental noise. Table 3-I shows the design specifications for a voltage regulator designed for instrumentation amplifier:

Table 3-I Voltage regulator design specifications for an instrumentation amplifier.

Parameter	Value	Units/Comments
Supply Voltage	1.7 – 3.3	Volts
Quiescent Current	<20µ	Amperes
Output Current	>500µ	Amperes
Output Voltage	1.2 – 2.0	Volts
Output Accuracy	±5	%
Functional Range	-40 to 120	Degree Celsius
Temp. Coefficent	<200	ppm
PSR (<1MHz)	>-40	dB

The dc output of the regulator is designed to be 1.8V in this work with an operating temperature range of -40°C to 120°C. The voltage regulator requires an output accuracy of ±5% which refers to its sensitivity to transistor mismatch and process variation. Some of the critical matching transistors for exemplary current mirror transistors, input pairs and so forth have to be sized with longer channel length to enhance the matching characteristics and improve the output DC accuracy. The voltage regulator refers to a bandgap scaled voltage reference to output a temperature independent output whilst providing the capability for

sourcing current. Low quiescent current consumption is needed as the system aims to achieve low power. Wide bandwidth voltage regulator normally has an advantage in giving good transient response as well as fast settling time in the design. However, this will trade off with larger power consumption. As this voltage regulator supplies to the analog block that has no speed requirement, there is no fast transient response requirement. Besides, voltage regulators with high rejection to power supply variations are necessary for accurate or critical analog signal processing blocks. This is especially important for high precision micropower sensor systems. In implementing voltage regulators, the linear regulator has several advantages over the switching regulator in terms of simplicity, cost, switching noise and electromagnetic compatibility. The PSR performance and output noise performance are the main focus in the voltage regulator design as it used in sensor system with energy harvesting power source.

The low-power SoC micro-system often imposes several strict requirements on the regulator, such as (i) the voltage regulator should be operated with low quiescent current because of the micropower system and (ii) the voltage regulator should exhibit high PSR for immunity against the huge fluctuation of supply. The same issues apply to the voltage references except without sourcing current capability. Much work has been done on bandgap voltage references and voltage regulators. Recent work [52] suggested the difficulty of obtaining high PSR at high frequency, for instance, 1MHz with a very low quiescent biasing current. Similarly, although an ultra low power CMOS voltage reference [53] consumes 0.24µA, it has a PSR performance of only -28.5dB at 1kHz. On the contrary, a voltage reference [54] having a current consumption of 300µA can achieve a PSR of -40dB at 1MHz. It can be seen that higher PSR bandwidth at -40dB can be achieved with larger quiescent current. This shows the design challenges of a micropower regulator for achieving high PSR performance metric in sensory systems.

There are two types of linear regulator implementation, namely the operational amplifier (op-amp) based regulator and the op-amp-less based regulator. They are discussed next on the effect of PSR performance with different architecture designs.

3.2.1. PSR Performance of Operational Amplifier Based Regulators

A typical CMOS bandgap voltage regulator [55] is shown in Figure 3.2. It comprises a driving transistor, an op-amp, a bandgap reference circuit and a feedback resistor network to obtain the desired regulated output. The op-amp senses the difference between the bandgap reference voltage and the fraction of output voltage, establishing a feedback loop to provide a regulated output voltage. The op-amp, together with the transistor feedback loop provides immunity against supply noise because it serves as a negative feedback structure with respect to the supply path. However, the supply noise of the bandgap voltage reference will be directly amplified and coupled to the output of the regulator through the error amplifier and the series pass transistor. Hence, the PSR performance metric of the bandgap reference is crucial in the regulator design. Recent improvement adopts the feedforward technique [56] at the expense of increased complexity.

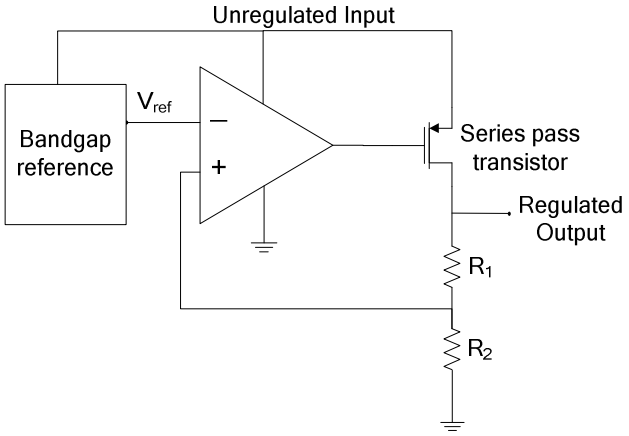


Figure 3.2 Typical linear regulator using op-amp based design

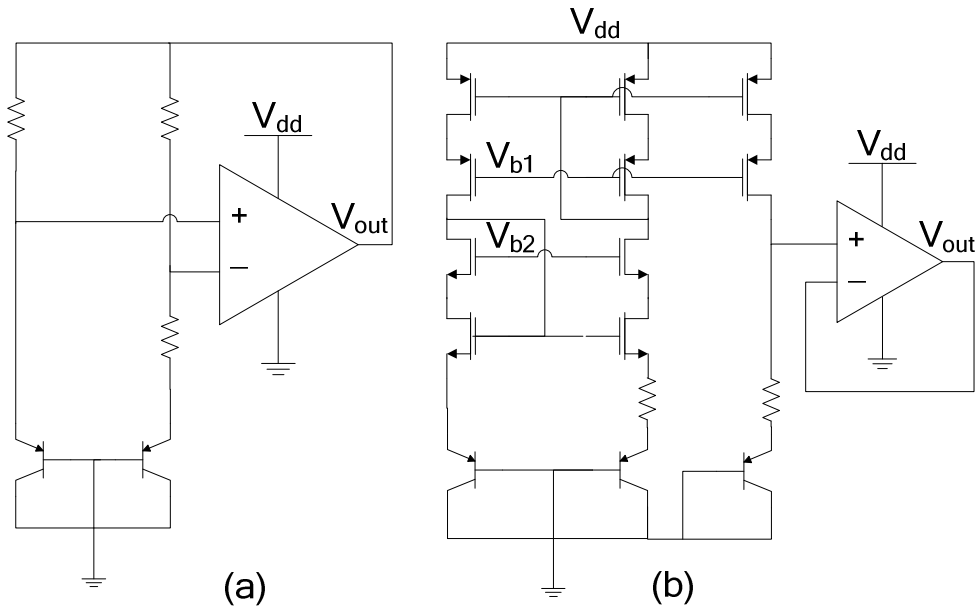


Figure 3.3 Other op-amp based regulator designs (a) op-amp clamp with self-bias (b) self-biased cascode transistor clamp plus op-amp buffer

Op-amps used in the voltage references [57-59] maintain the equal node voltages and constant drain currents whilst providing sourcing capability. An example is depicted in Figure 3.3(a) [58, 59]. It provides a negative feedback to improve the supply sensitivity of the voltage reference. At dc, high PSR performance will be improved with a large loop gain in the negative feedback path. However, the PSR of voltage reference will also depend on the PSR characteristics of the op-amp. As we can observe from Figure 3.4, the capability of the op-amp and bandgap reference in rejecting the PSR noise will also limit the overall PSR performance at the output of an op-amp based regulator.

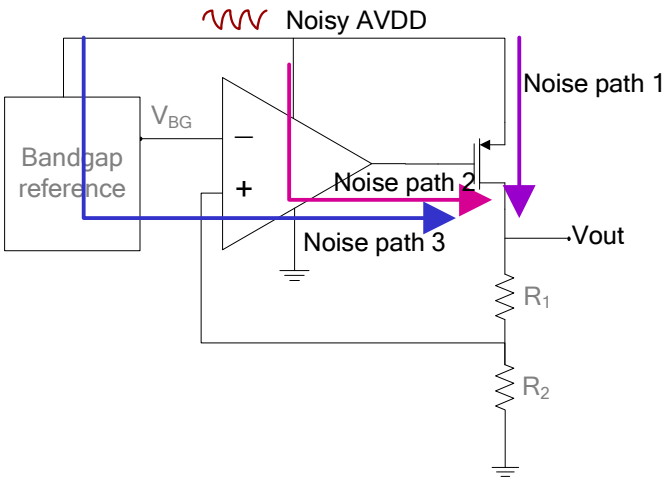


Figure 3.4 Supply noise coupling paths in a typical op-amp based design

Due to the reduction in loop gain at high frequencies, spurious signal can easily penetrate into the circuit, strongly limiting the high-frequency PSR. Therefore, one should be able to lower the positive power supply gain of the op-amp at these frequencies. This adds more stringent requirements to the op-amp based regulator design. Similarly, in Figure 3.3 (b) [57], an op-amp buffer is added to provide sourcing capability for the core bandgap circuit output. The use of self-biasing structure in conjunction with cascode technique is able to provide good PSR in the core bandgap voltage reference. However, the final PSR performance of complete regulator will be dominated by the added op-amp itself.

3.2.2. PSR Performance of Operational Amplifier-less Based Regulators

The monolithic, op-amp-less voltage reference or voltage regulator are shown in the designs proposed by Wildar [60] and Brokaw [61]. For low-power high-PSR voltage regulator design, it is preferably op-amp-less to minimize design complexity as well as current dissipation. However, a good broadband PSR figure is achieved with the tradeoff of higher current consumption since the transconductance g_m of the transistors is increased with biasing current. Wildar's circuit is used as an example to explain the phenomenon. Figure 3.5(a) shows the well-known Wildar regulator [62] that is realized by a triple-well CMOS

process technology having vertical NPN devices. Its simplified circuit for small-signal analysis is depicted in Figure 3.5(b).

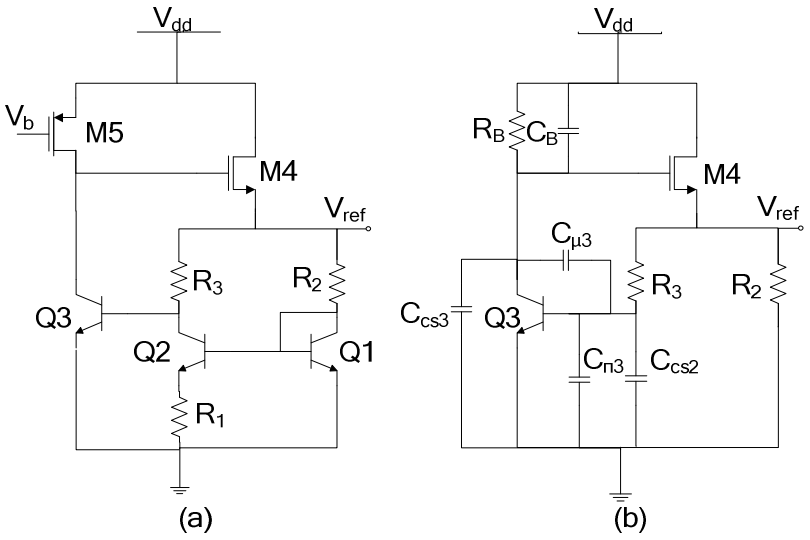


Figure 3.5 (a) Representative op-amp-less regulator: Wildar's circuit (b) Simplified circuit for small-signal analysis

As analyzed by [63], the PSR transfer function of the Wildar power supply circuit can be obtained as follows:

$$\frac{V_{ref}}{V_{dd}}(s) = PSR(s) \approx PSR(0) \cdot \frac{\left(1+\frac{s}{z_1}\right)\cdot\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{P_1}\right)\cdot\left(1+\frac{s}{P_2}\right)} \tag{3.1}$$

$$PSR(0) \approx \frac{R_3 + r_{\pi 3}}{r_{\pi 3} g_{m3}[g_{m4} r_{o4}(R_B // r_{o3}) // R_B]} \approx \frac{R_3 + r_{\pi 3}}{r_{\pi 3} g_{m3} R_B} + \frac{R_3 + r_{\pi 3}}{r_{\pi 3} g_{m3} g_{m4} r_{o4}(R_B // r_{o3})} \tag{3.2}$$

$$z_1 \approx -\frac{1}{R_B \cdot \left(\frac{C_{cs3}}{g_{m4} r_{o4}} + C_B\right)} - \frac{1}{[g_{m4} r_{o4}(R_B // r_{o3})] \cdot \left(\frac{C_{cs3}}{g_{m4} r_{o4}} + C_B\right)} \tag{3.3}$$

$$z_2 \approx -\frac{1}{(R_3 // r_{\pi 3}) \cdot (C_{cs2} + C_{\pi 3})} \tag{3.4}$$

$$P_1 \approx -\frac{g_{m3}}{C_{cs3} \cdot \left(1 + \frac{R_3}{r_{\pi 3}}\right)} \tag{3.5}$$

$$P_2 \approx -\frac{1}{(R_3 // r_{\pi 3}) \cdot (C_{cs2} + C_{\pi 3})} \tag{3.6}$$

$$PSR(\infty) \approx \frac{(C_{cs3}/g_{m4}r_{o4}) + C_B}{C_{cs3}} \tag{3.7}$$

where the symbols have their usual meanings. At low frequencies, the PSR is improved by the negative feedback loop formed by Q3, M4 and bandgap network. The feedback mechanism reduces the output impedance at node V_{ref}. Its dc behavior is mainly governed by the value of R_B and r_{o3}.

To achieve minimum PSR, the term $\frac{R_3+r_{\pi 3}}{r_{\pi 3}g_{m3}R_B}$ has to be minimized, and hence R_B should be made as large as possible. The dominant zero z_1 increases with biasing current as suggested in (3.3) because it is inversely proportional to resistor value of R_B. The dominant pole P_1 depends on g_{m3} and C_{cs3}. The non-dominant zero z_2 and pole P_2, tend to cancel each other. As a result, the transfer function of the PSR can be approximated by one zero and one pole in the first order analysis. Besides, the PSR(∞) is mainly governed by C_B as it is much larger than $C_{cs3}/g_{m4}r_{o4}$. It can be been that the broadband PSR performance can also be achieved with high gain $g_{m4}r_{o4}$ of key power driving transistor. Indirectly, it is linked to biasing current as well as process technology. In micropower circuit design, it is difficult to achieve high g_m for the power driving transistor because of finite biasing current constraint. Hence, this presents the design challenge in micropower regulator.

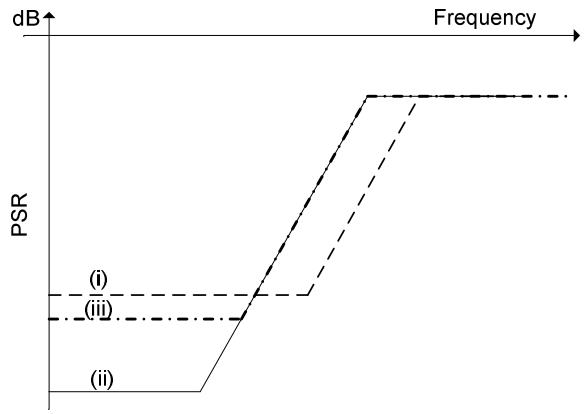


Figure 3.6 Frequency behaviour of the PSR(s) for the Wildar regulator: (i) high (ii) low biasing current (iii) low biasing current with higher circuit intrinsic noise

Figure 3.6 illustrates the PSR behavior for the CMOS Wildar voltage reference based on (3.1) for different biasing current cases. For curve (i) which has a higher biasing current, the dominant zero and pole are pushed to higher frequencies, thus improving the high frequency PSR. When the biasing current is decreased, the PSR curve will be represented by curve (ii) instead of curve (i). As implied in (3.2), decreasing biasing current will increase the circuit dc PSR. However, at this juncture, its dominant zero is shifted to lower frequency, causing the PSR starts increase with a gradient of 20dB per decade at the lower frequency. This will lead to poor PSR figures at high frequencies.

Furthermore, an intuitive point of view not revealed by the above analytical equations is given in the following explanation. The PSR value can be improved at low frequency through reducing the biasing current. However, the continued reduction in biasing current will increase the circuit intrinsic noise in the voltage reference. When the intrinsic noise becomes the dominant noise source with respect to the supply noise source, the effective PSR curve will change from curve (ii) to curve (iii). This is another observed phenomenon in micropower regulator or voltage reference design. Hence, careful circuit design is needed to optimize the PSR performance in the context of power consumption versus low-frequency PSR.

In short, higher biasing current will improve the bandwidth of the PSR but at the expense of higher power consumption. Although the op-amp-less regulator supports low-power consumption as well as simplicity, which are favorable attributes for micropower regulator design, the improvement of PSR bandwidth-power efficiency becomes the key focus in the following proposed work.

3.3. Proposed Low Quiescent, High-PSR Micropower Regulator

For the Brokaw bandgap design [61], the PSR bandwidth versus biasing current is similar to that of the Wildar's power supply circuit. However, the classical Brokaw power supply circuit has been shown to exhibit reasonable good wideband PSR [64]. In order to achieve the micropower high-PSR regulator dedicated to micropower sensory circuits and systems, this chapter introduces a low-power PSR improvement circuit technique to the Brokaw's voltage reference without occupying large silicon area.

The main concept of the proposed high PSR regulator is to add one more negative feedback control structure between the main supply line and the supply line of a Brokaw circuit, as shown in Figure 3.7. The new circuit can be regarded as the feedback-controlled Brokaw circuit. The control circuit is used to stabilize a regulated voltage which acts as the pseudo-supply to the bandgap core circuit. The core of the bandgap voltage reference is based on a Brokaw bandgap circuit that produces a feedback path to the control circuit whilst providing its reference voltage being scaled to higher output voltage for use as a voltage source. At the same time, in order to reduce the headroom incurred by the stacked structure, the power driving transistors (M5 and M10) are realized using native devices which have approximately zero threshold voltages.

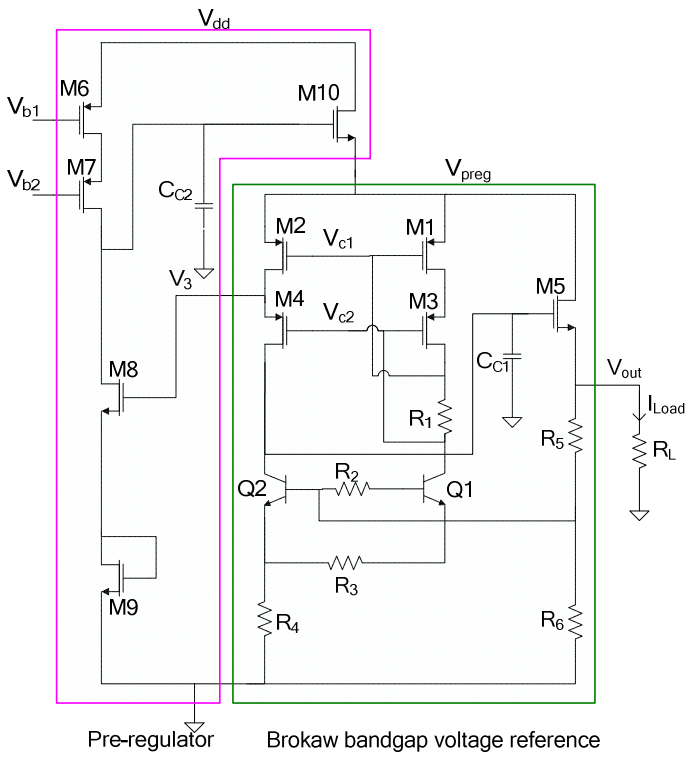


Figure 3.7 Proposed micropower regulator

When the pre-regulator or feedback control circuit in Figure 3.7 is introduced to enhance the PSR performance of the Brokaw bandgap reference, it shields the output voltage from ac fluctuation coming from the supply voltage significantly. In the design, the pre-regulator transistors M6-M10 establish a negative feedback loop with the bandgap circuit to the V_{preg} node. Any ripple that appears at the V_{preg} node through the variation of supply V_{dd} node will be sensed at the drain of M2 through a series of source-follower-like structures existent in the self-biased PMOS high-swing cascode mirror in the bandgap circuit, and is then negatively amplified by M8 with a dc level-shifted transistor M9 and a cascode current source formed by M6 and M7. Hence, the negative feedback mechanism counteracts the change of ac ripple by the loop gain.

Finally, the transistor M10 will act as a source follower transistor to drive V_{preg} to a stable value. At the same time, M10 provides a low impedance node at its source so that the circuit can respond to any variation of the current being sourced at the output. Instead of a

normal NMOS transistor for M10, a native transistor with almost zero threshold voltage is used to relax the higher gate biasing voltage condition. Besides, a compensation capacitor Cc_2 is added at the gate of M10 to create a pole to improve the pre-regulator PSR performance at high frequency. To maintain the operation of the pre-regulator, a supply independent current generator is built to bias the negative feedback circuit. Transistors M6 and M7 establish a cascode configuration and are designed to have larger channel length to enhance matching, reduce noise and increase gain.

3.3.1. PSR Frequency Response Small Signal Analysis

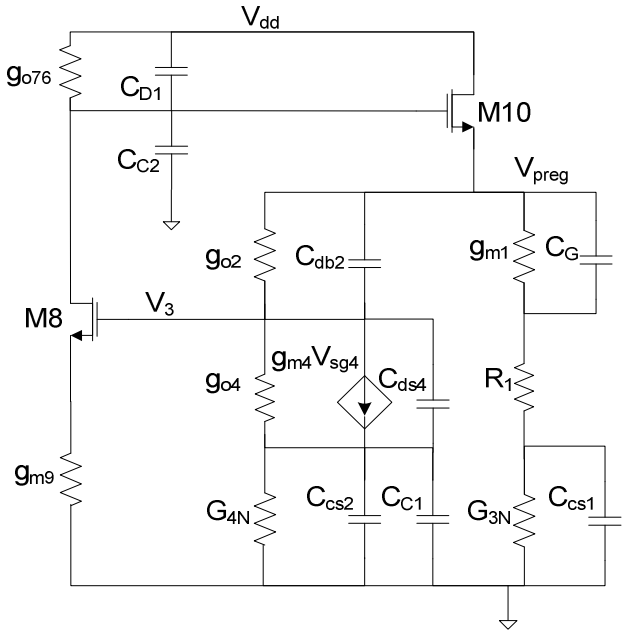


Figure 3.8 Simplified small-signal model for pre-regulator loop

With this, the small-signal analysis of the pre-regulator circuit based on the model depicted in Figure 3.8 is derived and shown as follows:

$$\frac{V_{preg}}{V_{dd}}(s) \approx \frac{A_{dc\_preg}\left(1+\frac{s}{z_{1\_preg}}\right)\left(1+\frac{s}{z_{2\_preg}}\right)}{\left(1+\frac{s}{R_{Pole\_preg}+I_{Pole\_preg}\cdot j}\right)} \times \frac{1}{\left(1+\frac{s}{R_{Pole\_preg}-I_{Pole\_preg}\cdot j}\right)} \tag{3.8}$$

$$A_{dc_{preg}} = PSR(0)_{pre\_regulator} \approx \frac{g_{076}}{g_{m8}^{'}} + \frac{g_{010}(g_{o8}^{'}+g_{076})}{g_{m8}^{'} \cdot g_{m10}} \tag{3.9}$$

$$z_{1\_preg} \approx -\frac{g_{076}}{C_{D1} + Cc_2 \frac{g_{010}}{g_{m10}}} \tag{3.10}$$

$$z_{2\_preg} \approx -\frac{g_{m4}}{C_3} \tag{3.11}$$

$$R_{Pole\_preg} \approx -\frac{1}{2}\frac{g_{m4}}{C_3+C_{cs1} \cdot R_1 \cdot g_{m4}} \tag{3.12}$$

$$I_{Pole\_preg} \approx \frac{1}{2}\sqrt{\frac{g_{m4}(4g_{m8}^{'}C_3 + 4g_{m8}^{'}C_{cs1}R_1g_{m4} - Cc_2g_{m4})}{Cc_2(C_3+C_{cs1}R_1g_{m4})^2}} \tag{3.13}$$

where the degenerated transconductance of M8 is $g'_{m8} \approx \frac{g_{m8}}{1+g_{m8}/g_{m9}}$; the effective output resistance of M8 is $g'_{o8} \approx \frac{g_{m9} \cdot g_{o8}}{g_{m8}}$; the effective capacitance at the gate of M8 is $C_3 \approx (g'_{m8}g'_{o8})\, C_{gd8}$; g_{o76} and C_{D1} are the admittance and capacitance from V_{dd} to the gate of M10. Note that $C_{D1} \approx C_{dg10}$; the effective capacitance between V_{preg} and the gate of M2 is $C_G \approx C_{sg1} + C_{sg2}$; G_{3N} and G_{4N} are the admittance looking from the collector of BJT Q1 and Q2 to the ground respectively.

The PSR transfer function of the pre-regulator circuit is obtained by considering dominant poles and zeros. The transfer function is approximated by two left-hand-plane zeros and one complex conjugate pole pair. Similar to the Wildar regulator, the dc PSR as well as the dominant zero of the pre-regulator increases with biasing current since they are both proportional to g_o. The dominant poles are complex in nature. The second zero, z_{2_preg} is approximated to be $-\frac{g_{m4}}{C_3}$ which is close to the complex pole generated at node V_3. Hence, the peaking effect of the complex poles will be reduced by the zero.

The core circuit of the bandgap reference works under the internal regulated supply. The Brokaw bandgap exhibits good behavior over a wide range of frequencies and can be improved by adding a compensation capacitor Cc_1 [64]. Besides, there is another negative feedback loop formed in the Brokaw design. Any ripple that appears at the V_{out} node through the variation of pre-regulator V_{preg} node will be sensed at the base of BJT Q2 through the potential divider from source-follower output stage. The signal will be amplified negatively by an inverting amplifier formed by the driving transistor Q2, degenerated resistor R_4 and cascode load M2 and M4. The negative feedback mechanism counteracts the change and hence the output V_{out} node becomes insensitive to the variation at the pre-regulator V_{preg} node.

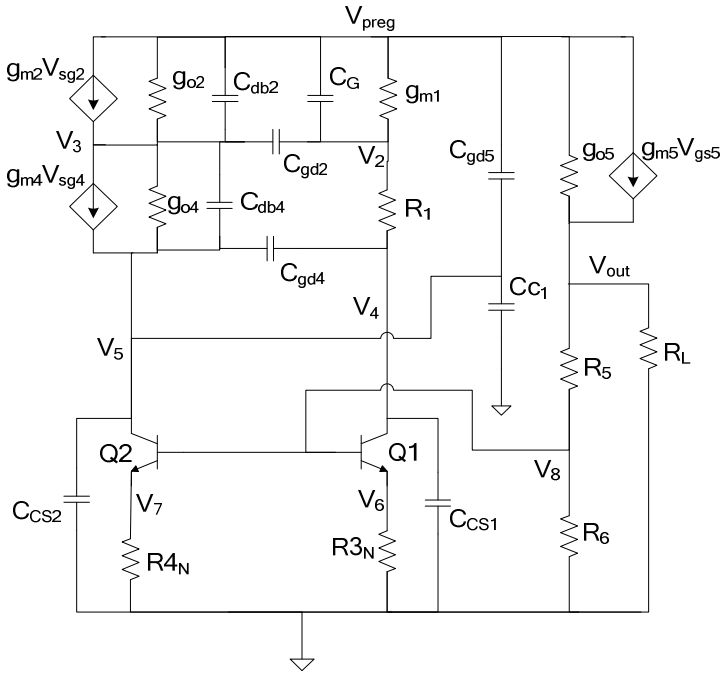


Figure 3.9 Simplified small-signal model for Brokaw bandgap reference

The small-signal analysis of the Brokaw bandgap core in Figure 3.9 is obtained as follows:

$$\frac{V_{out}}{V_{preg}}(s) \approx \frac{A_{dc\_BG}\left(1+\frac{s}{z_{1\_BG}}\right)\left(1+\frac{s}{R_{Z\_BG}+I_{Z\_BG}\cdot j}\right)}{\left(1+\frac{s}{P_{1\_BG}}\right)\left(1+\frac{s}{P_{2\_BG}}\right)} \times \frac{\left(1+\frac{s}{R_{Z\_BG}-I_{Z\_BG}\cdot j}\right)\left(1+\frac{s}{z_{4\_BG}}\right)}{\left(1+\frac{s}{P_{3\_BG}}\right)\left(1+\frac{s}{P_{4\_BG}}\right)} \tag{3.14}$$

$$A_{dc\_BG} = PSR(0)_{Brokaw\_bandgap} \approx \frac{g'_{oQ1}(R_6+R_5)}{(g'_{mQ2}-g'_{mQ1})R_6} + \frac{g_{o2}g_{o4}(R_6+R_5)}{g_{m4}(g'_{mQ2}-g'_{mQ1})R_6} \tag{3.15}$$

$$z_{1\_BG} \approx -\frac{g'_{oQ1}}{C_{cs1}+Cc_1\frac{g_{o5}}{g_{m5}}} \tag{3.16}$$

$$R_{Z\_BG} \approx -\frac{C_{cs1}R_1g_{m1}g_{m5}\left(2C_{gd2}+C_{db2}\right)+Cc_1g_{o5}C_G}{2\cdot R_1C_{cs1}C_G(Cc_1g_{o5}+g_{m5}C_{db2}+g_{m5}C_{gd2})} \tag{3.17}$$

$$I_{Z\_BG} \approx \left[\frac{C_{cs1}g_{m2}g_{m5}+Cc_1g_{m1}g_{o5}}{R_1C_{cs1}C_G(Cc_1g_{o5}+g_{m5}C_{db2}+g_{m5}C_{gd2})} - \frac{1}{4}\left(\frac{C_{cs1}R_1g_{m1}g_{m5}\left(2C_{gd2}+C_{db2}\right)+Cc_1g_{o5}C_G}{R_1C_{cs1}C_G(Cc_1g_{o5}+g_{m5}C_{db2}+g_{m5}C_{gd2})}\right)^2\right]^{1/2} \tag{3.18}$$

$$z_{4\_BG} \approx -\frac{g_{m4}}{Cc_1\frac{g_{o5}}{g_{m5}}} - \frac{g_{m4}}{C_{gd2}+C_{db2}} \tag{3.19}$$

$$P_{1\_BG} \approx -\frac{(g'_{mQ2}-g'_{mQ1})\cdot R_6}{Cc_1(R_6+R_5)} \tag{3.20}$$

$$P_{2\_BG} \approx -\frac{1}{(C_G/g_{m1})+R_1\cdot C_{cs1}} \tag{3.21}$$

$$P_{3\_BG} \approx -\frac{1}{R_1\cdot C_{cs1}} \tag{3.22}$$

$$P_{4\_BG} \approx -\frac{g_{m4}}{C_{gd2}+C_{db2}} - \frac{1}{R_1\cdot C_{cs1}} \tag{3.23}$$

where the degenerated transconductance of BJT Q1 and Q2 is $g'_{mQ1} = \frac{g_{mQ1}}{1+(2R_4+R_3)g_{mQ1}} \approx \frac{1}{2R_4+R_3}$; $g'_{mQ2} = \frac{g_{mQ2}}{1+2R_4g_{mQ2}} \approx \frac{1}{2R_4}$; the degenerated output impedance of BJT Q1 and Q2 are $g'_{oQ1} = \frac{1}{g_{mQ1}(2R_4+R_3)r_{oQ1}}$; $g'_{oQ2} = \frac{1}{g_{mQ2}(2R_4)r_{oQ2}}$; the effective capacitance between V_{reg} and

the gate of M2 is $C_G \approx C_{sg1} + C_{sg2}$; R_{3N} and R_{4N} are the equivalent resistance looking from the emitter of BJT Q1 and Q2 to the ground respectively.

From the PSR transfer function of the Brokaw bandgap core, the circuit has two real zeros and two complex zeros. $\mathrm{PSR}(0)_{Brokaw\_bandgap}$ can be affected by both g_m and g_o values. In the design, the cascode current mirror is used for M2 and M4 to increase the impedance from V_{preg} to V_5. Hence the $\mathrm{PSR}(0)_{Brokaw\_bandgap}$ is improved with lower biasing current of the circuit. However, its dominant zero increases linearly with the biasing current. For better PSR bandwidth design purposes, z_{1_BG} should be pushed to a higher value, but with the tradeoff of higher current consumption. To avoid the drawback, a compensation capacitor Cc_1 is added to shift the dominant pole closer to the dominant zero, hence improving the PSR of the design. As the overall PSR is the summation of both pre-regulator and bandgap core circuit, the overall PSR is improved significantly. It is given as

$$PSR_{overall} = \frac{V_{out}}{V_{dd}}(s) = \frac{V_{preg}}{V_{dd}}(s) \times \frac{V_{out}}{V_{preg}}(s) \tag{3.24}$$

$$PSR_{overall}|_{dB} = PSR_{pre\_regulator}\big|_{dB} + PSR_{Brokaw\_bandgap}\big|_{dB} \tag{3.25}$$

As mentioned previously, the high PSR figure is normally achieved with tradeoff of power consumption. To avoid the unnecessary increase of biasing current or static power consumption, the two negative feedback loops, one in the Brokaw circuit and another one in the control circuit, enable the resultant PSR of the micropower regulator to be excellent over a wide range of frequency whilst drawing only very low quiescent biasing current.

3.3.2. Regulator Output Voltage

The temperature compensation at the output voltage of the Brokaw voltage reference depends on the base-emitter voltage (V_{be}) and the proportional-to-absolute temperature

(PTAT) voltage. The area ratio of Q1 and Q2 is N, which is set to 8 for better matching and ease of layout. In the bandgap voltage reference, its voltage reference output is a typical value of 1.2V. It is the combined temperature effect of a scaled V_{ptat} having positive temperature coefficient and a V_{be} having negative temperature coefficient. The final output voltage is obtained by scaling the bandgap voltage to 1.8V. The output expression is given as

$$V_{out} = \left(1 + \frac{R_6}{R_5}\right) V_{BG} = \left(1 + \frac{R_6}{R_5}\right) \left(V_{beQ1} + 2\frac{\Delta V_{be}}{R_3} R_4\right) \tag{3.26}$$

It is a first order bandgap reference. However, it has limitations in compensating the nonlinear component of the V_{be} voltage [65]. The temperature performance of bandgap voltage reference normally can be further improved by either resistor trimming or second-order curvature correction techniques [53, 66].

As the BJT used is a parasitic vertical BJT in triple-well CMOS process technology, its current gain β is very small (around 10-30) compared to a normal BJT having a gain of typically 100-200. Hence, the resistor R_2 is added to cancel the effect of finite base current due to this small β. The first-order temperature compensation can be achieved by adjusting the ratio of R_3 and R_4. Finally, the output stage operates as a source follower which provides a low impedance output to cater for resistive or capacitive or their combined load in the applications that require sourcing currents. M5 is implemented with a native transistor which relaxes the headroom requirement. V_{out} can be almost the same as gate voltage of M5. As a result, the regulator is designed to operate from -40°C to +125°C whilst offering reasonable supply range.

3.3.3. Start-up Circuitry

Figure 3.10 shows the startup circuit and bias current generator for the proposed design. Transistors M11-M16 and resistors R7, R8 form a supply independent bias current

generator to provide a constant biasing current to the negative feedback network for the pre-regulator design. Meanwhile, for low power design, the startup circuitry adopts capacitive-coupled startup circuit [67]. It is formed by M17-M20, Cs1 and Cs2. This circuit is favorable for low power design since it does not consume static power. The bias current generator and the Brokaw bandgap core circuit will remain off if there is no startup circuit that provides a current path from V_{dd} to ground. Drains of the transistors M18-M20 are connected to the node V_{b1}, V_{c1}, V_{c2} of the self-biased transistors in the bias current generator and the Brokaw bandgap core circuit in Figure 3.7 and Figure 3.10 respectively.

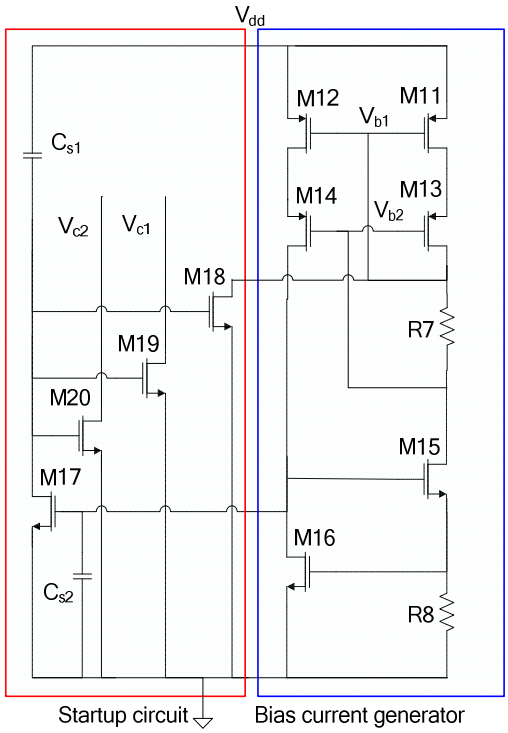


Figure 3.10 Startup circuit and bias current generator for the proposed design

In the initial state where the supply voltage V_{dd} is at zero, capacitors, C_{s1} and C_{s2} are uncharged. At startup, when the supply surges high, the uncharged C_{s1} causes the gate voltage of NMOS transistors, M18-M20 to reach V_{dd}. Thus, M18-M20 transistors are turned on and they start to draw respective current from the self-biased transistors M1, M3, M11 and M13 in the bandgap core circuit (Figure 3.7) as well as the supply independent current generator

(Figure 3.10), hence starting up the circuit. Once the current starts to flow in the bias current generator, the gate voltage of transistor M17 will rise, thus turning on M17. Eventually, transistors M18-M20 are turned off and they no longer affect the bias loop.

3.4. The Importance of Low-Noise, Broadband High PSR in Regulator Design

As discussed in Section 3.2, under a limited low-power supply source, there is great difficulty obtaining high power supply rejection (PSR) in regulator circuits. The broadband high PSR is even more difficult to achieve in a compact and integrated solution. Besides, with ultra-low level biasing currents, the regulator noise will increase significantly as it is always a design conflict or trade-off. A low-noise regulator will benefit the low-noise sensor circuit design by reducing the requirement for immunity against noise. For small signal sensing, the front-end interface should have strong immunity against supply disturbances as much as possible.

Additional op-amps in [56] will increase the design complexity, current consumption as well as intrinsic noise at the output node. This gives a difficult trade-off between noise and current consumption. The recent work [68], realised in a bipolar process achieved high PSR up to 10MHz with current sampling feedback loop, but requires an off-chip compensation capacitor which may not be suitable for an integrated solution. In short, the voltage regulator plays an important role as a high quality internal supply to the micropower sensor interface circuit that is noise sensitive. It is desirable for the regulator itself to consume very small quiescent current whilst providing broadband high PSR as well as low noise performance metrics.

3.4.1. Noise Sources in a Regulator

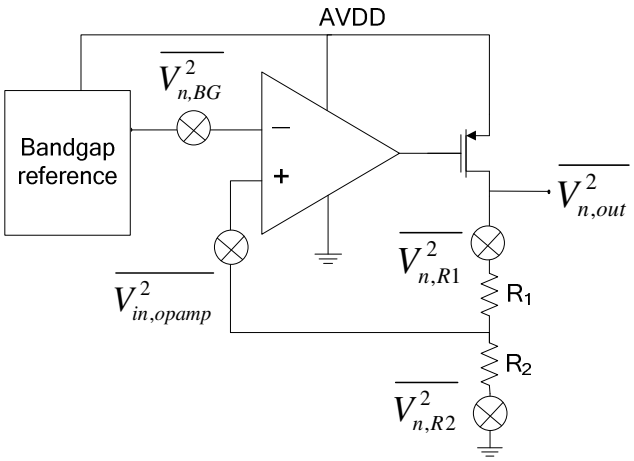


Figure 3.11 Noise sources in an op amp-based regulator

The noise at the output of the regulator is usually dominated by the op-amp and the bandgap reference in the design. The noise sources contributing to the output of the regulator are illustrated in Figure 3.11, identified as $\overline{V_{n,BG}^2}$, output noise of the bandgap reference, $\overline{V_{in,opamp}^2}$, input-referred noise of the error amplifier, as well as $\overline{V_{n,R1}^2}$ and $\overline{V_{n,R2}^2}$ which are the noise of the feedback resistors. With this the output noise, $\overline{V_{n,out}^2}$ can expressed by:

$$\overline{V_{n,out}^2} \approx \left[1+\frac{R_1}{R_2}\right]^2 \left(\overline{V_{n,BG}^2}+\overline{V_{in,opamp}^2}\right)+\overline{V_{n,R1}^2}+\left(\frac{R_1}{R_2}\right)^2 \overline{V_{n,R2}^2} \tag{3.27}$$

As a result, there is a need to minimize the number of noise sources in the low noise design. Noise, power and area are always trade-off among one another to achieve optimum performance. In the next section, an ultra-low power, low noise voltage regulator with broadband PSR performance is proposed and discussed.

3.5. Proposed Low-Noise, Broadband High PSR Regulator

Figure 3.12 illustrates the proposed regulator design which makes use of an op-amp-less voltage regulator structure to minimize the quiescent current consumption with

simplicity to minimize the output noise for the voltage regulator design. The circuit comprises a capacitive-coupling start-up circuit as discussed in Section 3.3.3, the bias current generator, the pre-regulator with the proposed native composite power transistor (M10 and M11) plus a circuit sandwich decoupling capacitor Cc_3, the CMOS based Brokaw voltage regulator core with the proposed pseudo-resistor based noise filter (MP1, MP2, Cc_1). The output gives a stable 1V dc voltage with a maximum of 2mA output current driving capabilities. To minimize the power dissipation, the current on each branch was designed to be in nA level. Therefore, weak inversion operation is employed to generate the subthreshold currents. The current biasing generator shown in Figure 3.12 is designed to generate a 184nA current to the pre-regulator circuit.

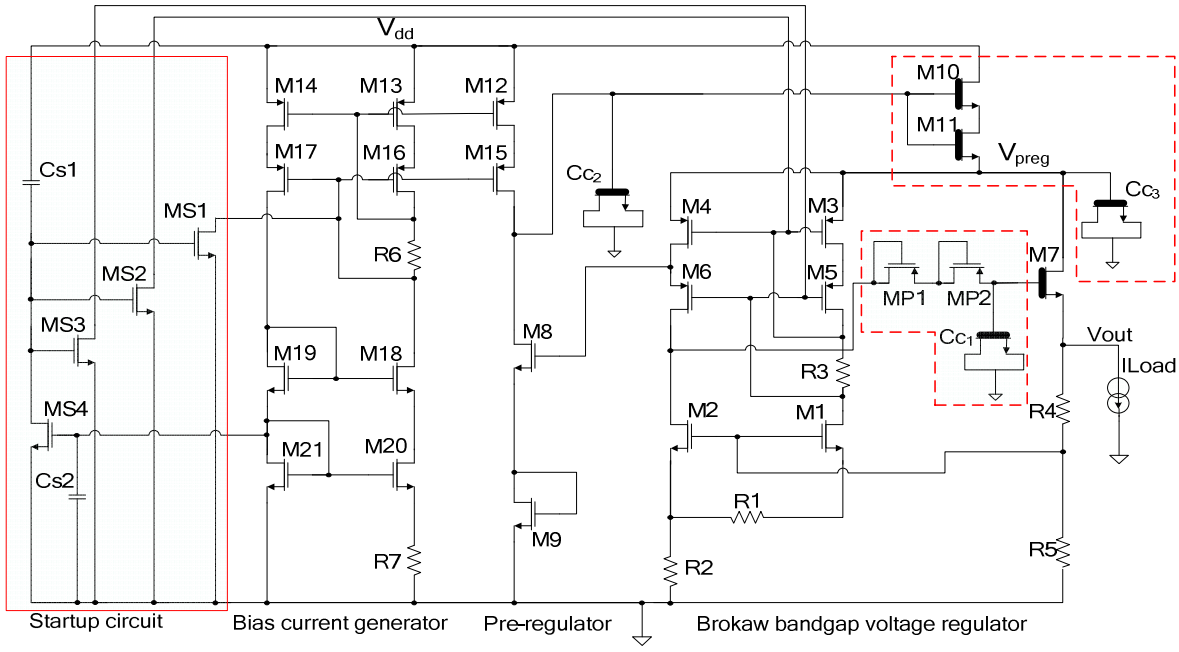


Figure 3.12 Schematic of the proposed low noise, high PSR voltage regulator

It is shown that the pre-regulator can improve the PSR in the regulator design [69] via establishing a negative feedback loop from the voltage reference circuitry to the pre-regulated node V_{preg} in Chapter 3. However, when the biasing current continues to reduce, the zeros in

the PSR transfer function of the pre-regulator will shift to lower frequencies. This may not be favorable for broadband high PSR performance.

To alleviate the problem, in the proposed ultra-low power regulator design, the native devices (M10 and M11) form a composite power transistor which acts as a source-follower power driving transistor and establishes a high impedance path to the supply so as to offer better shield on the supply noise in the pre-regulator side. When a circuit sandwich decoupling capacitor, Cc_3, formed by a native MOS capacitor, is added at the pre-regulated supply output node V_{preg}, a low-pass filter is created from the source of composite transistor and the on-chip native MOS capacitor. This leads to effective filtering at high frequencies by means of using finite impedance of the pre-regulator output. As a result, high PSR is sustained at high frequencies due to the intentionally added pole in the frequency band of interest.

3.5.1. CMOS Brokaw Bandgap voltage reference

In the design, M1-M2 working in the sub-threshold region are used to produce the voltage reference to the pass transistor because they offer lower power alternatives compared to using parasitic bipolar devices in CMOS technology. Due to the sub-threshold operation, the gate-source voltage of transistor in weak inversion region can be represented as

$$V_{GS} \approx V_{th} + nU_T \ln(\frac{I_D}{I_s}) \tag{3.28}$$

where $I_s \approx n\mu_n C_{ox}(W/L){U_T}^2$, $U_T = \frac{kT}{q}$. The temperature-dependent threshold voltage exhibits an almost linear relationship which decreases with temperature, and can be approximated by

$$V_{th}(T) = V_{th}(T_r) - k(T - T_r) \tag{3.29}$$

where k is usually between 0.5mV/K and 3mV/K [70], T_r is room temperature in K. For transistors working in weak inversion region, the inversion coefficient, $IC = \frac{I_D}{I_s}$ is always <<1. Hence, the second term in (3.28) is also inversely proportional to temperature. Consequently, V_{GS} of the subthreshold transistor displays a negative temperature coefficient effect.

The overall temperature dependency of the output voltage will be the sum effect of the temperature coefficients. The output voltage is given by

$$V_{OUT} = (1 + \frac{R_4}{R_5})\left[V_{GS,M1} + \frac{3(\Delta V_{GS,M2-M1})R_2}{2R_1}\right] \quad (3.30)$$

where $\Delta V_{GS,M2-M1}(T) \approx nU_T(\mathrm{T})\ln(\frac{S_{M4}S_{M1}}{S_{M3}S_{M2}})$ giving a positive temperature coefficient. For ultra-low power design, the biasing current ratio for transistors M2:M1 is set to 1:2. Thus, $S_{M4}: S_{M3}$ is 1:2, where $S_{M1}: S_{M2}$ is 4:1 where S represents the W/L ratio of the transistor.

3.5.2. Broadband High PSR Frequency Small Signal Analysis

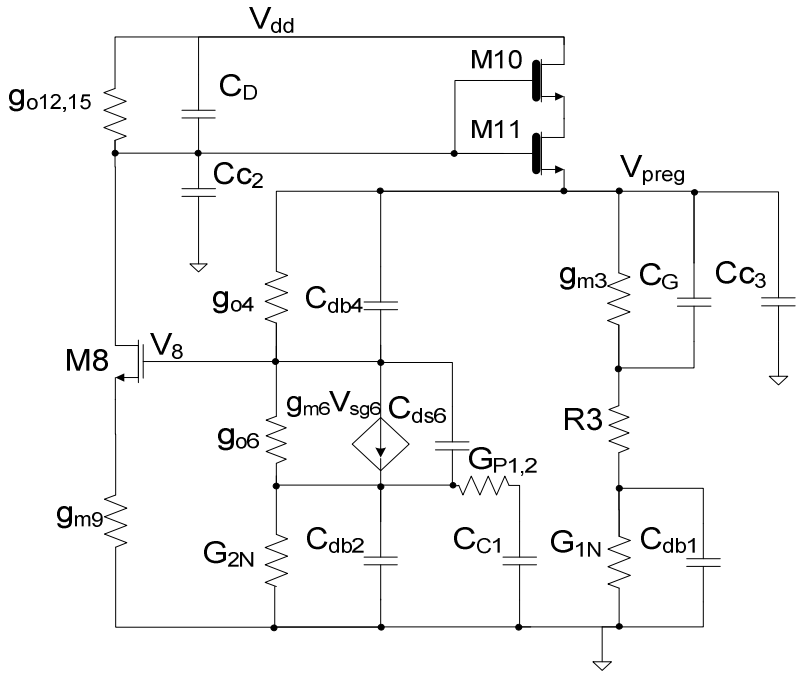


Figure 3.13 Simplified small-signal model for pre-regulator loop

The simplified small-signal model of the proposed design is shown in Figure 3.13, where the broadband PSR pre-regulator transfer function is approximated as

$$\frac{V_{preg}}{V_{dd}}(s) \approx \frac{A_{dc\_preg}\left(1-\frac{s}{z_{1\_preg}}\right)\left(1-\frac{s}{z_{2\_preg}}\right)}{(a\cdot s^2+b\cdot s+1)\left(1-\frac{s}{P_{3\_preg}}\right)} \tag{3.31}$$

$$A_{dc\_preg} \approx \frac{g_{o12,15}}{g_{m8}^{'}}+\frac{g_{o10}^{'}\left(g_{o8}^{'}+g_{012,15}\right)}{g_{m8}^{'}\cdot g_{m10}^{'}} \tag{3.32}$$

$$z_{1\_preg} \approx -\frac{g_{o12,15}}{C_D+Cc_2\frac{g_{o10}^{'}}{g_{m10}^{'}}} \approx -\frac{g_{o12,15}}{C_D} \tag{3.33}$$

$$z_{2\_preg} \approx -\frac{G_{2N}g_{m6}+g_{o6}g_{o4}}{C_{db2}g_{m6}+C_8g_{o6}} \tag{3.34}$$

$$a \approx \frac{Cc_1Cc_2(C_{db2}g_{m6}+C_8g_{o6})}{g_{m8}^{'}G_{P1,2}(G_{2N}g_{m6}+g_{o6}g_{o4})} \tag{3.35}$$

$$b \approx \frac{Cc_1(Cc_2G_{2N}g_{m6}+Cc_2g_{o4}g_{o6}+C_{db2}g_{m8}^{'}g_{m6})}{g_{m8}^{'}G_{P1,2}(G_{2N}g_{m6}+g_{o6}g_{o4})} \tag{3.36}$$

$$p_{3\_preg} \approx -\frac{g_{m10}^{'}}{Cc_3} \tag{3.37}$$

where the composite transconductance of M10-M11 is $g'_{m10} \approx g_{m11}$; the effective output resistance of M10-M11 is $g'_{o10} \approx \frac{g_{o10}\cdot g_{o11}}{g_{m10}}$; the degenerated transconductance of M8 is $g'_{m8} \approx \frac{g_{m8}}{1+g_{m8}/g_{m9}}$; the effective output resistance of of M8 is $C_8 \approx (g'_{m8}g'_{o8})\,C_{gd8}$; $g_{o12,15}$ and C_D are the admittance and capacitance from V_{dd} to the gate of M10-M11 where $C_D \approx C_{dg10}$; the effective capacitance between V_{preg} and the gate of M4 is $C_G \approx C_{sg3}+C_{sg4}$; G_{1N} and G_{2N} are the admittance looking from the drain of M1 and M2 to the ground respectively and $G_{P1,2}$ is the admittance of the pseudo-resistor MP1-MP2. The PSR transfer function of the pre-regulator circuit is obtained by considering dominant poles and zeros in

the frequency band of interest (up to few ten MHz). The transfer function is approximated by two left-hand-plane zeros, one complex conjugate pole pair and one high frequency real pole. Their relative locations are illustrated in Figure 3.14.

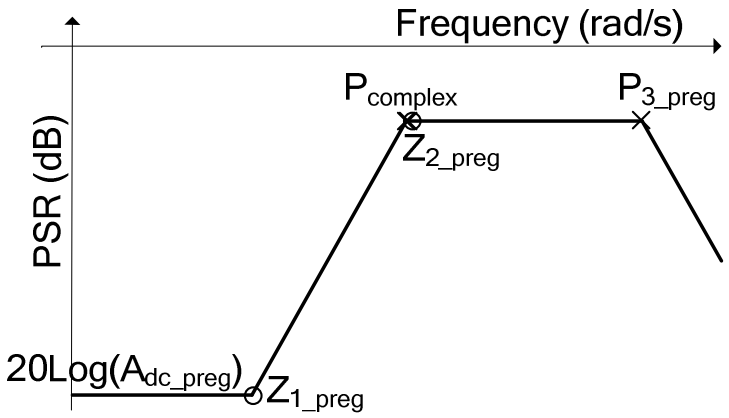


Figure 3.14 Asymptotic approximation bode plot for the pre-regulator PSR transfer function

A conventional MOS transistor has limitations in terms of finite output resistance and small transconductance parameter. In the design, the composite transistor M10-M11 with a common gate gives an output impedance enhancement while permitting the use of short-channel devices for obtaining good transconductance parameter. The threshold voltage of the native transistors is close to zero. The native transistors are designed to operate in the saturation region for most of the input voltage conditions. The effective impedance of the composite transistor M10-M11, r'_{o10}, is increased with the cascoding effect, hence $g'_{o10} \approx 1/g_{m10}r_{o10}r_{o11}$. Therefore, a good DC PSR, A_{dc_preg} can be obtained. Moreover, the dominant zero, z_{1_preg} is also pushed to a higher frequency, thus improving the high frequency PSR with the help of the composite structure, as the $\frac{g'_{o10}}{g'_{m10}}$ term in (3.33) becomes negligible.

Since the second zero, z_{2_preg} is very close to the complex pole, the flatted PSR curve at z_{2_preg} frequency is expected. The circuit sandwich decoupling capacitor, Cc_3, gives

another pole at few ten MHz. This permits improving the pre-regulator PSR at high frequency by damping down the PSR response using p_{3_preg}. The native MOS capacitor, Cc_3 is 31pF with $(\frac{W}{L})_{Cc3} = \frac{400\mu m}{15\mu m}$, occupying 0.00713mm^2 in the chip. It is useful in achieving broadband PSR performance without consuming extra current whilst offering the integrated solution.

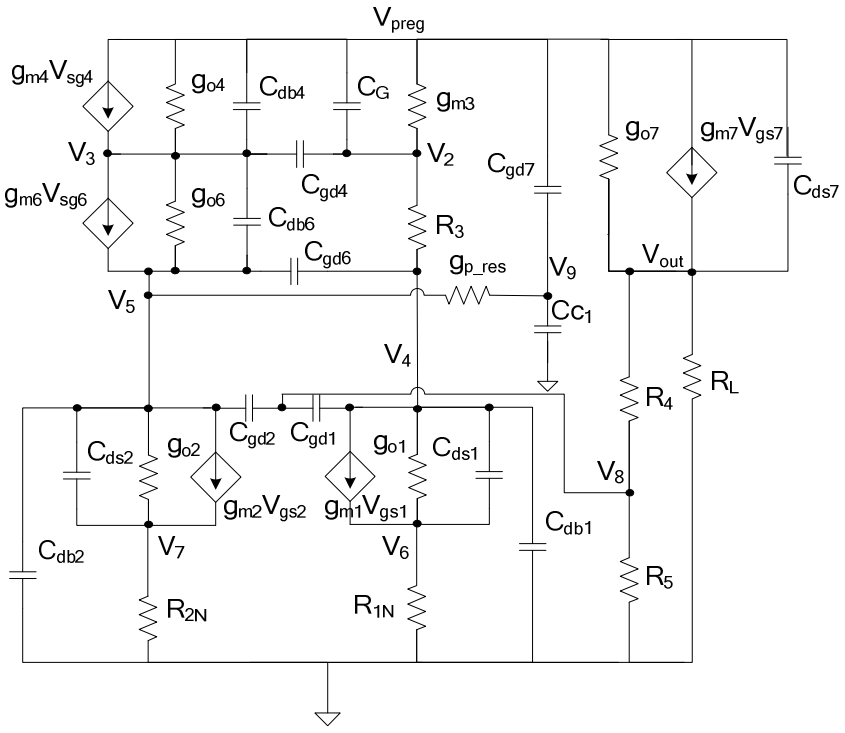


Figure 3.15 Simplified small-signal model for Brokaw bandgap reference with NMOS transistors

The PSR small signal analysis for the proposed Brokaw bandgap using NMOS transistors (M1 & M2) working in subthreshold region instead of the BJTs is given as follows:

$$\frac{V_{out}}{V_{preg}}(s) \approx \frac{A_{dc\_BG}\left(1+\frac{s}{z_{1\_BG}}\right)}{\left(1+\frac{s}{P_{1\_BG}}\right)} \tag{3.38}$$

$$A_{dc\_BG} = PSR_{Brokaw\_bandgap}(0) \approx \frac{g'_{o1}(R_5 + R_4)}{(g'_{m2}\frac{g_{m3}}{g_{m4}} - g'_{m1})R_5} \tag{3.39}$$

$$z_{1\_BG} \approx -\frac{g_{o7}}{C_{ds7}} \tag{3.40}$$

$$P_{1\_BG} \approx -\frac{g_{\mathrm{m}7}}{C_{ds7}} \tag{3.41}$$

where the degenerated transconductance of NMOS M1 and M2 is $g'_{m1} = \frac{g_{m1}}{1+R_{1N}g_{m1}}$; $g'_{m2} = \frac{g_{m2}}{1+R_{2N}g_{m2}}$; the degenerated output impedance of NMOS M1 and M2 is $g'_{o1} = \frac{1}{g_{m1}R_{1N}r_{o1}}$; $g'_{o2} = \frac{1}{g_{m2}R_{2N}r_{o2}}$; the effective capacitance between V_{reg} and the gate of M2 is $C_G \approx C_{sg3} + C_{sg4}$; in the design the biasing current ratio for transistors M2:M1 is set to 1:2 hence $R_{1N} = \frac{3}{2}R_2 + R_1$ and $R_{2N} = 3R_2$ are the equivalent resistance looking from the source of M1 and M2 to the ground respectively. It shows a broadband PSR performance for the Brokaw bandgap reference with NMOS devices for obtaining the bandgap voltage.

3.5.3. Output Noise Analysis

The main contributors to the regular noise components are the voltage reference devices, M1-M2. Hence, they are designed to be large enough to minimise flicker noise. In the proposed regulator, two PMOS pseudo-resistors (MP1 and MP2) along with the MOS capacitor, Cc_1 are introduced to form a noise filter having an ultra-low pole frequency (0.05mHz) to suppress the noise from voltage reference as shown in Figure 3.12. The pseudo-resistors are implemented using diode-connected transistors working in cut-off region which gives Tera-Ω resistance values without substantially increasing the noise level. The dimensions of transistors MP1-MP2 and native MOS capacitor, Cc_1 are: $(\frac{W}{L})_{MP1} = \frac{0.5\mu m}{12\mu m}$; $(\frac{W}{L})_{MP2} = \frac{1\mu m}{3\mu m}$;$(\frac{W}{L})_{Cc1} = \frac{400\mu m}{15\mu m} \approx 30.5$pF. This gives small silicon area for realizing

very large resistor value in the low-pass RC filter design and thus, majority of the flicker and thermal noise from the major noise contributor through the Brokaw voltage reference will be shielded from the output node.

3.6. Summary of Regulator Designs

Two CMOS low power high PSR voltage regulators are presented in this chapter. Both regulator designs are based on op-amp-less architecture with additional control circuitry in Brokaw bandgap reference to provide temperature independent output voltage. The small-signal analyses on PSR frequency behaviors in the design are derived. A low noise design technique is proposed in the second regulator design in Section 3.5. Some noise analysis is provided to understand the main noise contributor in the design. The measurement results for both proposed regulators will be discussed in Chapter 8.

CHAPTER 4

CHOPPER STABILIZED INSTRUMENTATION AMPLIFIER ARCHITECTURE

4.1. Introduction

The differential difference amplifier (DDA) discussed in Chapter 2 [19, 23, 46] is identified as one of the solutions with floating differential input structure whilst displaying simple differential-to-single-ended circuit architecture for commonly-used sensors such as the Wheatstone bridge and two-input floating sensing element. In addition, its resistive-feedback network allows ease of external gain programming function. This chapter focuses on a low offset resistive-feedback based chopper stabilized instrumentation amplifier with reduced output ripple for small signal sensing application.

4.2. Analysis of Common-Mode Signals and Differential Common-Mode Signal in Chopper-Stabilized DDA

As introduced in Chapter 2, applying the chopper-stabilized technique, the input offset and low frequency noise of the amplifier will be modulated to the chopping frequency, whereas the input differential signals will remain at the signal frequency band at the output. However, in practice there are common-mode signals to be considered too. The analysis of common-mode signals and differential common-mode signal in chopping DDA will be given.

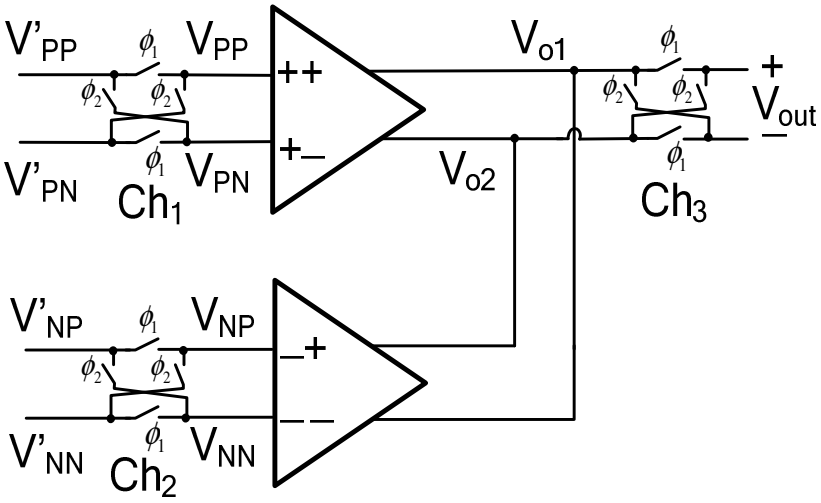


Figure 4.1 Block diagram of front-end chopping differential difference amplifier

In a chopping differential difference amplifier, there are 4 terminal input voltages at one instant of time, as shown in Figure 4.1. The output of a DDA can be represented by 4 voltage modes, namely; the differential-mode voltage V_d, common-mode voltage V_{cp} for positive port, common-mode voltage V_{cn} for negative port, and differential common-mode voltage V_{cd} between positive and negative ports. As a result, without chopping activity, the DDA's output V_{out} can be represented as follows:

$$\begin{aligned} V_{out} &= V_{o1} - V_{o2} \\ &= A_d V_d + A_{cp} V_{cp} + A_{cn} V_{cn} + A_{cd} V_{cd} \\ &= A_d[(V_{PP} - V_{PN}) - (V_{NP} - V_{NN})] \\ &+ A_{cp}\,(V_{PP} + V_{PN})/2 + A_{cn}\,(V_{NP} + V_{NN})/2 \\ &+ A_{cd}\,[(V_{PP} - V_{PN}) + (V_{NP} - V_{NN})]/2 \end{aligned} \tag{4.1}$$

where A_d is the differential-mode gain; A_{cp} and A_{cn} are the common-mode gains for positive and negative port respectively; while A_{cd} is the differential common-mode gain.

On the other hand, the common-mode voltages for the positive and negative ports are examined during clock ϕ_1 and ϕ_2 when there are chopping activities involved. Assuming

that $V'_{PP} = V'_{PN} = V_{cp}$, $V'_{NP} = V'_{NN} = V_{cn}$, the DDA will be characterized by the common-mode gains A_{cp} and A_{cn} for the positive and negative ports, respectively. During clock ϕ_1,

$$\begin{aligned} V_{out,\phi1} &= V_{o1} - V_{o2} \\ &= A_{cp}\,(V'_{PP} + V'_{PN})/2 + A_{cn}\,(V'_{NP} + V'_{NN})/2 \\ &= A_{cp}V_{cp} + A_{cn}V_{cn} \end{aligned} \tag{4.2}$$

During clock ϕ_2, the input and output signals are switched by the choppers, Ch_1 to Ch_3. Now, the output of DDA is

$$\begin{aligned} V_{out,\phi2} &= V_{o2} - V_{o1} \\ &= -A_{cp}\,(V'_{PN} + V'_{PP})/2 - A_{cn}\,(V'_{NN} + V'_{NP})/2 \\ &= -A_{cp}V_{cp} - A_{cn}V_{cn} \end{aligned} \tag{4.3}$$

As can be seen from (4.2) and (4.3), the output alternates between positive and negative values when the clock changes between ϕ_1 and ϕ_2. The switching between two polarities indicates that each common-mode signal is modulated to chopping frequency.

Consider the differential common-mode voltage between ports in a chopper stabilized DDA, examined during clock ϕ_1 and ϕ_2. Similarly, assuming that $V'_{PP} = -V'_{PN} = V'_{NP} = -V'_{NN} = V_{cd}/2$, the output of DDA will be characterized by the differential common-mode gain A_{cd} only. During clock ϕ_1,

$$\begin{aligned} V_{out,\phi1} &= V_{o1} - V_{o2} \\ &= A_{cd}\,[(V'_{PP} - V'_{PN}) + (V'_{NP} - V'_{NN})]/2 \\ &= A_{cd}V_{cd} \end{aligned} \tag{4.4}$$

During clock ϕ_2, the input and output signals are switched by the choppers, Ch_1 to Ch_3. Now, the output of DDA is

$$\begin{aligned} V_{out,\phi 2} &= V_{o2} - V_{o1} \\ &= -A_{cd}\left[(V'_{PN} - V'_{PP}) + (V'_{NN} - V'_{NP})\right]/2 \\ &= A_{cd}V_{cd} \end{aligned} \tag{4.5}$$

As observed from (4.4) and (4.5), the outputs remain the same polarity despite the control clocks switching between ϕ_1 and ϕ_2, meaning that the differential common-mode signal is not modulated to the chopping frequency. Hence, it is essential to make the differential common-mode gain as small as possible.

4.3. Proposed Chopper-Stabilized Instrumentation Amplifier Architecture

Figure 4.2 shows the block diagram of the proposed micropower chopper-stabilized differential difference amplifier (DDA). To avoid uneven charge injection in the two input ports, the influence of charge injection must be minimized, thus reducing the residual offset at the output caused by the chopping activities. This is achieved by adding the injection-nulling switch (INS) with modified control clock input choppers and a balancing resistor [5], R_b=R_1//R_2 to equalize the impedance difference between the two input ports. As such, the residual charge injection offset due to impedance unbalance is further minimized. Demodulator Ch_3 is used to modulate the desired signal back to baseband and up-modulate the unwanted DC offset and 1/f noise to the chopping frequency.

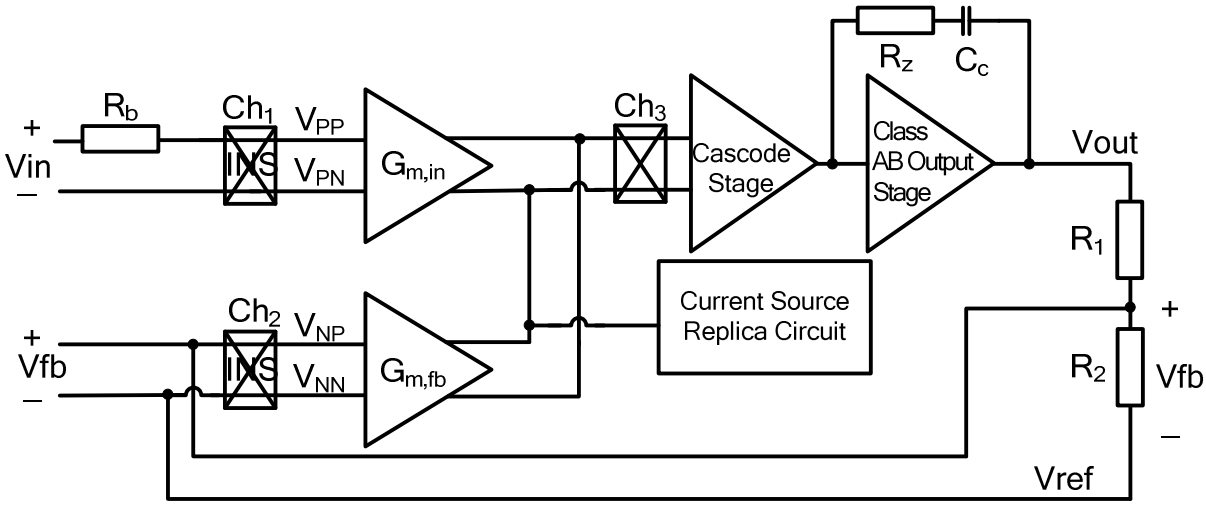


Figure 4.2 Block diagram of the chopper-stabilized differential difference instrumentation amplifier.

In this work, a low noise gate-bulk driven inputs, $G_{m,in}$ and $G_{m,fb}$ with folded telescopic cascade stage differential-difference amplifier is proposed to achieve very high gain in 2-stage design. A current source replica (CSR) circuit is designed to serve dual functions in the design. First, it is used to reduce the output ripple by generating similar level of mismatch offset current to nullify the mismatch offset current arising from the input stage of DDA. As a result, the net difference between two similar levels of mismatch offset current tends to be very small. Secondly, it enhances the differential common-mode rejection ($CMRR_d$) by improving the matching of critical devices in the input stage design, hence minimizing its contribution to the input offset.

Lastly, the output stage is implemented with a pseudo-class AB configuration, to allow maximum output swing. It also acts as an integrator with compensation capacitor C_C to filter the modulated DC offset which will appear as a triangular wave output ripple at the Vout. Therefore, the proposed instrumentation amplifier which employs resistive feedback has an intended closed-loop gain as follows:

$$A_{cl} = \frac{R_1 + R_2}{R_2}\frac{G_{m,in}}{G_{m,fb}} \tag{4.6}$$

where $G_{m,in}$ is the transconductance of the input port, and $G_{m,fb}$ is the transconductance for the feedback port. In the design, both $G_{m,in}$ and $G_{m,fb}$ are designed to be equal.

4.4. Chopper Modulator

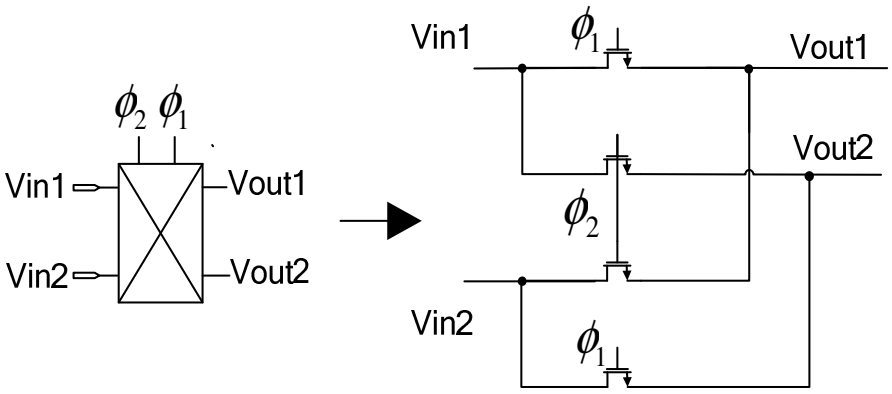


Figure 4.3 A chopper with NMOS switches.

A front-end chopping instrumentation amplifier stage employs the input chopper to modulate the signal to the chopping frequency. The operation is controlled by two non-overlapping phases clock signal to the input chopper. A conventional chopper with NMOS switches is shown in Figure 4.3.

In chopper operation, the DC offset and 1/f noise components of CMOS amplifier can be cancelled effectively. However, the switching of choppers may have significant impact on the circuit's actual performance which causes residual offset at the output of a chopping amplifier. This residual offset stems from the unbalanced or imperfectly compensated switch charge injection at high impedance nodes. An ideal chopping instrumentation amplifier with infinite bandwidth and perfect matching characteristics will give minimum residual offset with smaller switching glitches [71, 72]. However, in practice the limited bandwidth and devices mismatch cause unwanted spikes as well as non-zero residual offset.

4.4.1. Review of Switches for Chopper Design

In the input modulator, charge injection and parasitic coupling will cause spikes to appear. For instance, when the non-ideal pairs of switches open at the input of the IA, they cause imperfect dumping of the stored channel charges, leading to spikes at the input signal. The spikes then cause residual offset at the amplifier output. Despite the spikes being common-mode signals, the common-mode rejection of the amplifier is still limited at high frequencies. Therefore, after amplification and demodulation, these spikes generate residual offset.

The conventional single switch chopper implementation shown in Figure 4.4 uses MOS transistors operating in non-saturation region in the design. The switch turns on when V_{GS} is greater than the threshold voltage of the NMOS device. When the clock signal ϕ_1 turns off, half of channel charge distributed on C_{h1} causes an error voltage which is proportional to the size of the switches.

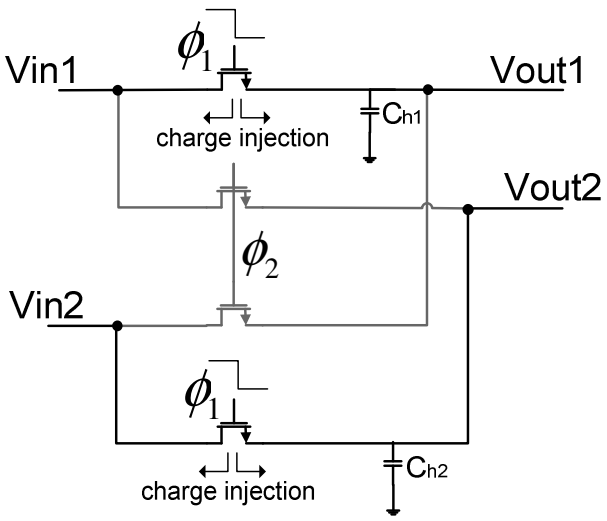


Figure 4.4 Simple chopper with NMOS switches showing charge injection.

Circuit techniques can be used to reduce the switch errors caused by the charge injection as well as clock feedthrough effect of the switches. One can use the complementary

devices also known as transmission gates [73], building its channel to reduce the effect of charge injection. However, the poor matching between the channel charges of the NMOS and PMOS switches in association with signal dependency makes it less efficient in cancellation.

Alternatively, a half-sized dummy switch can be added to each side of the MOS switch transistor for absorption of charge injection [73]. Each dummy MOS transistor is driven by an inverse clock phase with respect to the clock phase of single switch. However, there are limitations to the dummy switches. The source and drain impedance of the main switch is different and will cause unequal split of channel charges when the main switch turns off. Hence, the charge cancellation using dummy switches will be degraded.

4.4.2. Proposed Continuous-time Injection-Nulling Switch (INS) with Modified Control Clock Chopper

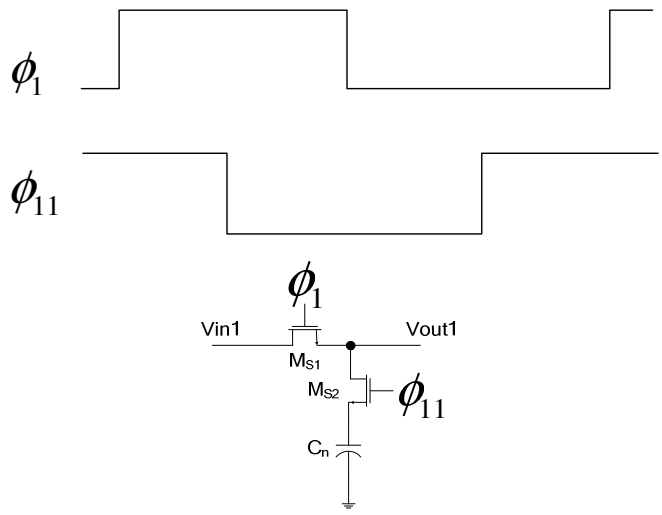
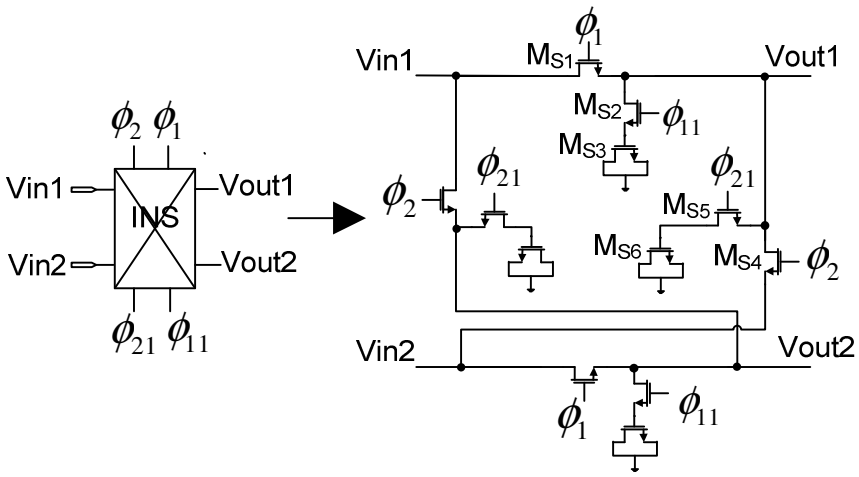


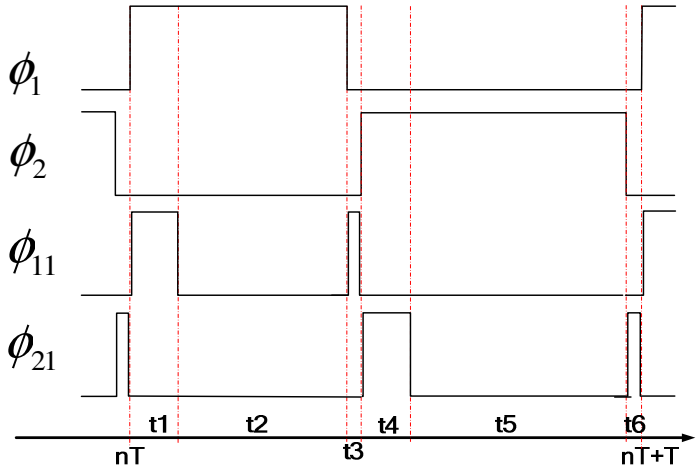
Figure 4.5 Original INS circuit and its clocking phase for switched-capacitor application. [74]

The switched-capacitor application injection-nulling switch (INS) [74] shown in Figure 4.5 has shown considerable reduction of switch errors using two identical MOS transistors and a capacitor compared to the standard dummy switch technique [57]. The INS switch, M_{s1} and M_{s2} have the main clocking phase ϕ_1 and phase-shift clock phase ϕ_{11} as

illustrated in Figure 4.5. M_{s2} makes use of the sample phase to store the input at the capacitor and hold phase to cancel the charge injection without jeopardising the output voltage. When switch M_{s1} is turned off during the hold phase, switch M_{s2} is turned on for injection charge cancellation. The output of switches M_{s1} and M_{s2} will only be valid as final output during hold phase. However, the long time gap between the main clock and the phase-shift clock jeopardizes the continuous-time operation when implemented in continuous-time chopper. As a result, the original INS is not suitable for continuous-time operation in the chopper implementation. This leads to the proposal of INS with modified control for clock continuous-time operation in Figure 4.6.



(a)



(b)

Figure 4.6 (a) Input chopper with INS with modified control clock (b) Modified clocking phase for INS chopper in continuous-time application.

As shown in Figure 4.6, there are four clocking signals for the implementation of the proposed chopper design. ϕ_1 and ϕ_2 are non-overlapping clock signals whereas ϕ_{11} and ϕ_{21} are injection nulling clock phases for the switches. Note that the clock signals ϕ_{11} and ϕ_{21} are not drawn to scale, with their duration time being very small compared to the half a clock period in the design. Referring to the continuous-time chopper design, four INS with modified control clocks are connected in cross-coupling manner where output of 2 switches eg. M_{s1} & M_{s4} are connected at the same node i.e. Vout1. Similarly, the switches M_{s7} & M_{s8} have the same output node of Vout2. The signals at Vout1 and Vout2 are read continuously.

The proposed continuous-time INS chopper with modified control clocks consists of four INS switches, each INS having two identical NMOS transistors and a MOS capacitor. Consider the main switches M_{s1} and M_{s4}, controlled by the complementary clock phases. The switches operate in the triode region with approximately zero-voltage drop across the drain and source terminals when they are turned on. Native transistors M_{s3} and M_{s6} are used to realize the MOS capacitors to take advantage of better area efficiency as well as closer matching characteristic to the gate oxide of input transistor pairs. The same applies for the other switch transistor pair. In particular, the continuous-time INS choppers are deployed at the input transistors of the instrumentation amplifier which are sensitive to the switch errors.

Consider the first INS with modified control clock in Figure 4.7; when the switch M_{s1} turns on at time nT, the switch M_{s2} will turn on via the clock ϕ_{11} to charge up the MOS capacitor, M_{s3} which has an equivalent capacitance of C_n, to the input voltage for the later nulling phase. Therefore, the charge stored at the capacitors C_n and C_{h1} respectively during $nT + \tau_1^-$ are:

$$Q_{Ch1}(nT + \tau_1^-) = V_{in1}(nT + \tau_1^-)C_{h1} \tag{4.7}$$

$$Q_{Cn}(nT+\tau_1^-) = V_{in1}(nT+\tau_1^-)C_n \tag{4.8}$$

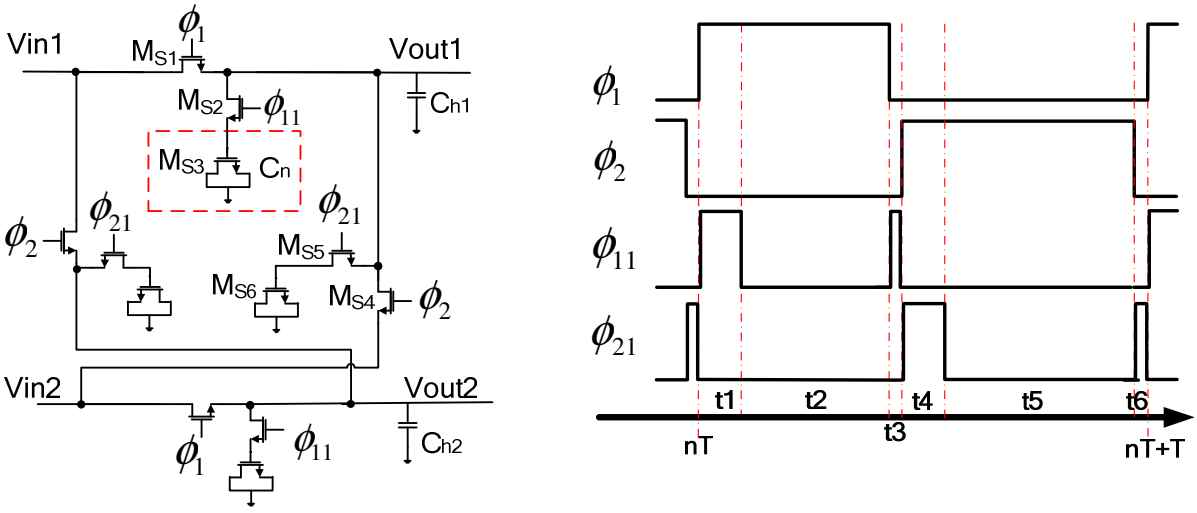


Figure 4.7 Input chopper with INS with modified control clock

Upon transiting into τ_2 , M_{s2} switch turns off and the switch error charges from M_{s2} will be injected to C_n and Vout1 node. Hence, at the end of τ_2 period, the charges in C_n and C_{h1} are:

$$Q_{Ch1}(nT+\tau_1+\tau_2^-) = V_{in1}(nT+\tau_1+\tau_2^-)C_{h1} \tag{4.9}$$

$$\begin{aligned} &Q_{Cn}(nT+\tau_1+\tau_2^-) \\ &\quad = V_{in1}(nT+\tau_1)C_n - \alpha_{n\_\tau 2}WLC_{OX} \\ &\quad \cdot [V_{DD} - V_{in1}(nT+\tau_1) - V_T] - \frac{(V_{DD}-V_{SS})C_p}{C_n+C_p}C_n \end{aligned} \tag{4.10}$$

where $-\alpha_{n\_\tau 2}WLC_{OX} \cdot [V_{DD} - V_{in1}(nT+\tau_1) - V_T]$ is the fractional charge being inject to capacitor C_n during M_{s2} turning off; $-\frac{(V_{DD}-V_{SS})C_p}{C_n+C_p}C_n$ is the charge due to the clock feedthrough effect; C_p is the parasitic capacitance between the gate of the switch and the capacitor C_n.

The non-overlapping clock, ϕ_1 falls to zero, turning off main switch M_{s1} when entering τ_3 , causes the charge injection takes place. The charge errors rises from the turning off the main switch are dumped into the capacitor C_{h1} and the input source. Hence the charge stored in C_{h1} and C_n becomes:

$$\begin{aligned} &Q_{Ch1}(nT+\tau_1+\tau_2+\tau_3^-) \\ &\quad = V_{in1}(nT+\tau_1+\tau_2)C_{h1}+\varepsilon_{switch}C_{h1} \end{aligned} \tag{4.11}$$

$$\begin{aligned} &Q_{Cn}(nT+\tau_1+\tau_2+\tau_3^-) \\ &\quad = V_{in1}(nT+\tau_1)C_n-\alpha_{n\_\tau 2}WLC_{OX} \\ &\quad \cdot\left[V_{DD}-V_{in1}(nT+\tau_1)-V_T\right]-\frac{(V_{DD}-V_{SS})C_p}{C_n+C_p}C_n \end{aligned} \tag{4.12}$$

$$\begin{aligned} &\varepsilon_{switch} \\ &\quad = \frac{-\alpha_{i\_\tau 3}WLC_{OX}}{C_{h1}}\left[V_{DD}-V_{in1}(nT+\tau_1+\tau_2)-V_T\right] \\ &\quad -\frac{(V_{DD}-V_{SS})C_p}{C_{h1}+C_p} \end{aligned} \tag{4.13}$$

After a delay, the M_{s2} switch turns on for charge nulling operation. The error charge arising from the turning off action of full switch M_{s1} will be absorbed effectively by turning on the full switch M_{s2}, cancelling the effect of a given charge injected into a capacitor by injecting an equal and opposite amount of charge from the MOS capacitor M_{s3} to the terminal. The effective charge in C_{h1} is:

$$\begin{aligned} &Q_{Ch1}(nT+\tau_1+\tau_2+\tau_3) \\ &\quad = V_{in1}(nT+\tau_1+\tau_2)C_{h1}-\alpha_{i\_\tau 3}WLC_{OX} \\ &\quad \cdot\left[V_{DD}-V_{in1}(nT+\tau_1+\tau_2)-V_T\right]-\frac{(V_{DD}-V_{SS})C_p}{C_{h1}+C_p}C_{h1} \\ &\quad +\alpha_{n\_\tau 4}WLC_{OX} \\ &\quad \cdot\left\{V_{DD}-\left[V_{in1}(nT+\tau_1+\tau_2)+\varepsilon_{switch}\right]-V_T\right\} \\ &\quad +\frac{(V_{DD}-V_{SS})C_p}{C_{h1}+C_p}C_{h1} \\ &\quad \approx V_{in1}(nT+\tau_1+\tau_2)C_{h1} \end{aligned} \tag{4.14}$$

A similar operation applies to the other cross-coupled switch pair M_{s4}–M_{s5} with control clock signals, ϕ_2 and ϕ_{21}. Since both switch transistors have almost identical matching characteristics, the residual error charge is significantly reduced even under mismatch of two switch transistors through process variation.

Furthermore, the floating input characteristic of DDA allows the cancellation of spikes as they appear at both differential inputs, Vpp–Vpn and Vnp–Vnn. The spikes will appear in the form of common signals at their respective input transistor and will be rejected by the common-mode rejection of the amplifier. This suggests that the balance based matching layout of critical transistor pairs is also critical for input offset reduction in the design of chopping instrumentation amplifiers. It is mainly because the matching between the two input ports directly affects the $CMRR_d$ which cannot be suppressed by chopper stabilization.

4.5. Chapter Summary

This chapter presents the analysis of the common-mode signals and differential common-mode signal in the chopper-stabilized differential difference amplifier which gives more insight of the chopping operation effect to the output of an indirect current feedback instrumentation amplifier. It shows that the differential common-mode signal is not modulated at the output, hence there is a need to ensure that the differential common-mode gain to be very small. Besides, the proposed chopper stabilized instrumentation amplifier architecture and proposed continuous-time INS chopper are presented. Some theory and explanations on INS chopper operation are discussed.

CHAPTER 5

A LOW OFFSET AND RIPPLE REDUCTION CHOPPER STABILIZED DIFFERENTIAL DIFFERENCE AMPLIFIER

5.1. Introduction

Following the introduction of the proposed IA architecture and the choppers in the previous chapter, a new micropower gate-bulk driven DDA, incorporating a folded telescopic cascode gain structure and its replica tracking bias circuit as well as the economical class-AB output stage, is discussed here. This also involves the circuit techniques for design of low-power, low-noise instrumentation amplifier to handle small floating sensing signals.

The proposed current source replica (CSR) circuit in the DDA design facilitates the pair matching layout for all critical pairs in DDA input stage to achieve low offset and reduced ripple performance. This is in contrast with the conventional design where the stated layout technique can only be applied to the input transistor pairs, but not others such as the current sources and current mirrors in the input stage of DDA. Through the proposal on the addition of Current Source Replica (CSR), it permits full application of pair matching layout technique to all the critical pairs in whole input stage. This is in contrast to conventional DDA where the pair matching layout only applies for the four input transistors but not on the two current source transistors and two current mirror transistors. The proposed ripple reduction technique is implemented by generating the nulling offset current and this improves the input offset by enhancing the $CMRR_d$ of the chopping DDA.

5.2. Gate-Bulk Driven DDA with Folded Telescopic Cascode Topology

For accurate analog signal processing, amplifiers having very high-gain and low-noise characteristics are required. The importance of having a high gain and low noise front-end IA has been highlighted in Chapter 1. Since all the gain has been allocated to the IA, it is essential to have high gain in the front end circuit.

Generally, the very high-gain amplifier design always leads to more than two or three gain stages which may consume larger power and area, in addition to increased design complexity. In micropower sensor system design, simple single stage amplifier with low power consumption, high gain and low noise performance is desirable. Cascode technique is common for improving the output impedance or gain of amplifiers such as the telescopic amplifier or folded cascode amplifier [62]. However, the conventional telescopic amplifier and folded cascode amplifier still hardly achieve gain of >100dB in a single stage design.

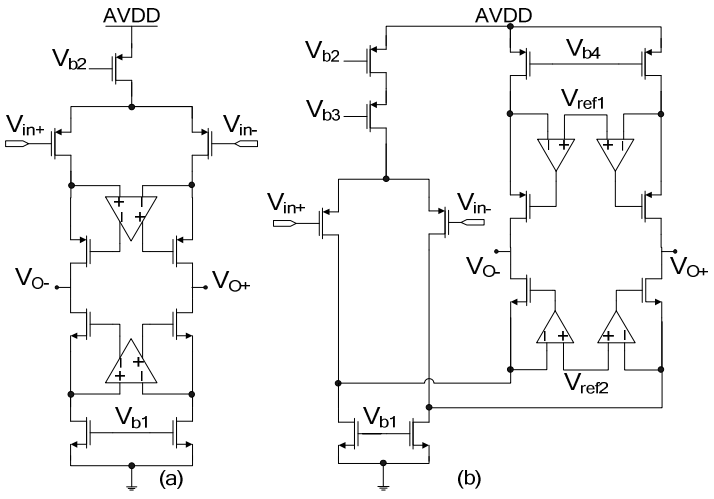


Figure 5.1 (a) Gain-boosted telescopic amplifier (b) Gain-boosted folded cascode amplifier

In order to further increase the output impedance, cascode gain boosting technique was introduced. Figure 5.1 shows the gain-boosted telescopic amplifier [75] and gain-boosted

folded cascode amplifier [76]. Although the output impedance is significantly boosted by the gain of the amplifier through negative feedback mechanism, the price paid for that will be extra power consumption and stability issue under limited power constraint despite an increase in silicon area.

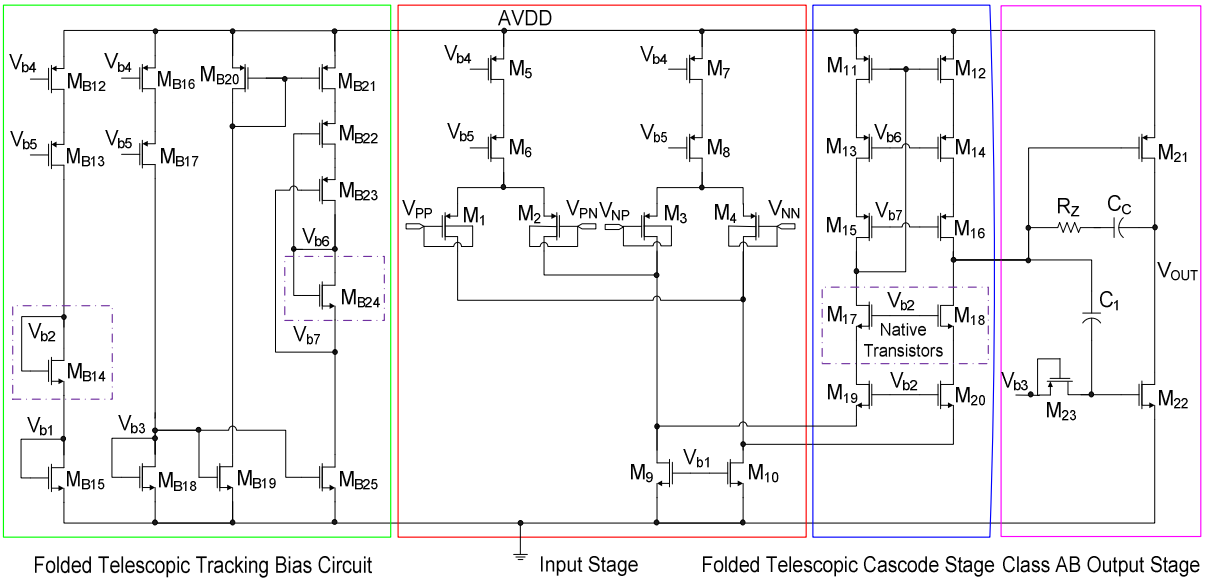


Figure 5.2 Proposed micropower gate-bulk driven DDA having front-end folded telescopic cascode stage and class-AB output stage

The proposed very high gain DDA is shown in Figure 5.2. In this DDA the input differential pairs are designed using gate-bulk driven input pairs where the input signals are connected to both gate and bulk terminals of the transistors [77]. This arrangement improves the noise performance of the DDA due to the higher input transconductance. Also, a new single-stage folded telescopic cascode topology is proposed in order to achieve very high gain at very low power and low noise based on noise optimization. The cascode transistors are properly biased to sustain their operation against variations of process, supply and temperature (PVT) by incorporating the proposed replica tracking bias circuit. The single high-gain stage is then followed by a very economical class AB output stage [78] which provides driving capability as well as rail-to-rail output swing.

5.2.1. Dual Gate-Bulk Input Stage

The gate-bulk driven MOSFET, known as Dynamic Threshold Voltage MOSFET (DTMOS) [77], has been applied in low-voltage analog circuits such as simple differential input stage [79], digital circuits like SRAM [80] and so on. In this work, the DTMOS technique is extended to the high-gain, low-noise DDA design. For the gate-bulk driven architecture, the channel current is controlled by dual gate and bulk voltages. Although the source bulk junction is slightly forward biased, there is hardly any substantial conducting pn-junction current. This results in reduction of threshold voltage in the MOSFET, enhancing the transconductance of the transistor. Therefore, the gate-bulk driven transistors in the DDA are suitable for amplification of small floating sensor signals in view of their higher transconductance characteristic. More importantly, the small input signal does not introduce significant forward biasing effect.

5.2.1.1. Effective Input Transconductance

There are two input differential stages which are formed by M_1–M_4 PMOS transistors in the DDA architecture, which operate in the weak inversion region. In the proposed DDA input stage, the transconductance-enhanced differential-pair transistors can reduce the total input-referred noise of the circuit, as illustrated in the drain current expression below:

$$\begin{aligned} I_d &= g_{m1}(v_s - v_g) + g_{mb1}(v_s - v_b) \\ &= (g_{m1} + g_{mb1})(v_s - v_{in}) \\ &= g_{m1}(1+\eta)(v_s - v_{in}) \end{aligned} \tag{5.1}$$

where g_{m1} and g_{mb} are the gate-source and bulk-source controlled transconductances, respectively. η is the ratio of g_{mb1} to g_{m1}, having a range of 0.1 to 0.2. Hence the transconductance of the input transistors are boosted and denoted as $g'_{m1} = g_{m1}(1+\eta)$.

5.2.1.2. Noise Analysis

Consider the thermal noise analysis, the input-referred noise of the DDA can be obtained as follows:

$$\overline{V^2}_{ni,thermal} = \left[\frac{16kT}{3g'_{m1}}\left(2+\frac{g_{m9}}{g'_{m1}}+\frac{g_{m11}}{g'_{m1}}+\frac{G_{m14}}{g'_{m1}}+\frac{G_{m16}}{g'_{m1}}+\frac{G_{m18}}{g'_{m1}}+\frac{G_{m20}}{g'_{m1}}\right)\right]\Delta f + \frac{8kT}{3}\left(\frac{1}{(g_{m21}+g_{m22})(g'_{m1}r_{out1})^2}\right)\Delta f \quad (5.2)$$

where r_{out1} is the output resistance at first stage, expressed as $r_{out1} \approx \frac{{g_m}^2{r_o}^3}{2}$ and G_m is the effective transconductance for cascode transistors having source degeneration. The source degenerated transconductance is reduced significantly compared to the normal g_m. Besides, the larger g'_{m1} arising from gate-bulk driven technique will further minimize the total input-referred noise.

5.2.2. Folded Telescopic Cascode Gain Stage

The folded telescopic cascode topology is introduced to achieve very high gain in a single stage design, thereby allowing reduced current consumption and gain error. This is in contrast to the prior-art works [50, 81] which make use of multiple gain stages to achieve high gain characteristic. Besides, by having the folded-telescopic cascode structure, the frequency response and settling time are improved by elimination of phase shift of the extra stage, with power dissipation reduced.

Transistors M_1–M_{20} of Figure 5.2 constitute the folded telescopic cascode structure for the first stage of the DDA. The transistors M_5–M_{10} act as current sources that provide biasing currents to the circuit. Long channel length is employed to enhance matching and amplifier common mode rejection ratio (CMRR). A cascoded mirror converts the differential signal to a single-ended one at the output of the first stage amplifier design. Of particular importance to solve the headroom problem, the wide-swing cascode active load formed by

M_{11}-M_{16}, is realized in the upper side whereas the cascode structure in the lower side incorporates a Native NMOS cascode transistor pair (M_{17} and M_{18}). As the threshold voltage of a Native transistor is close to zero, M_{17} and M_{18} can be turned on easily and biased in the correct operating region. The cascode transistors are biased by a dedicated micropower replica tracking bias circuit which will be discussed in the next section.

The output impedance of the cascode stage is economically boosted using native transistors. Therefore, it saves significant quiescent power consumption without relying on cascading many high-gain stages, which requires advanced frequency compensation to obtain better tradeoff between bandwidth and power.

5.2.3. Replica Tracking Bias Circuit

In the biasing circuit design of Figure 5.2, a subthreshold reference current generator in conjunction with the proposed replica tracking bias circuit formed by transistors M_{B12}–M_{B25} is employed. They ensure reliable cascode operation with PVT variations. The replica biasing voltages are established as:

$$V_{b6} = V_{sdMB21} + |V_{Tp}|_{MB22} + V_{effMB22} \tag{5.3}$$

$$V_{b7} = V_{sdMB21} + |V_{Tp}|_{MB22} + V_{effMB22} + V_{gsMB24} \tag{5.4}$$

$$V_{b7} = V_{sdMB21} + V_{sdMB22} + |V_{Tp}|_{MB23} + V_{effMB23} \tag{5.5}$$

For identical size and biasing current design, M_{B20}–M_{B21} matches with M_{11}–M_{12}. Similarly, M_{B22} matches with M_{13}–M_{14} whereas M_{B23} matches with M_{15}–M_{16}. M_{B24} is a Native NMOS that serves as a replacement of usual passive resistor. Referring to (5.4), for any increase of PTAT biasing current due to PVT variations, V_{b7} is less sensitive to increase in potential that stresses cascode transistors because the square root increase of V_{gsMB24} is less than the direct increase in passive resistor. Since $V_{effMB22} = V_{effMB23}$, V_{sdMB22} in (5.5)

is forced to be equal to V_{gsMB24} and hence it is easier to satisfy the condition for saturation region. With a tracking bias from V_{b6} (5.3), it turns out that M_{11}–M_{12}, M_{13}–M_{14} and M_{15}–M_{16} are always in the saturation region while tracking with the changes in PVT.

5.2.4. Pseudo Class AB Output Stage

A power efficient Class AB stage [78] is employed as the output stage for the DDA. In the design, transistors M_{21} and M_{22} form a structure similar to the conventional Class A structure. The capacitor C_1 serves as the floating battery source for ac coupling. The transistor M_{23} that operates in cut-off region provides a very large resistance for passing dc bias voltage, but blocking the ac signal from the capacitor C_1 to the dc biasing circuit. In the pseudo class AB operation, ac signal will couple through capacitor C_1 to the gate of M_{22}. The C_1 and M_{23} behave like a high pass filter at the gate of M_{22}. The DC value of gate M_{22} is determined by the DC from the biasing circuit. The pole of the high pass filter is designed to be very low. To have a lower corner frequency, one can further increase the resistance of the pseudo resistor by cascade another pseudo PMOS resistor with M_{23}. With this, it forms an economical rail-to-rail Class AB output stage. This pseudo-class AB output stage is suitable for sensor applications.

The Miller RC frequency compensation technique is adopted by the compensation capacitor C_C and resistor R_Z to stabilize the amplifier. The open loop gain A_v of the complete DDA can be obtained as:

$$A_v = g'_{m1} r_{out1} \cdot (g_{m21} + g_{m22}) r_{out2} \tag{5.6}$$

where the symbols have their usual meanings. The input common mode range is limited by transistors M_5–M_8 and M_9–M_{10}. To ensure the amplifier is never off, the maximum common mode value is no more than $V_{dd} - 2V_{eff\_M5} - V_{th\_M1}$.

5.3. Chopper-Stabilized DDA Design

As discussed in Section 4.3, the proposed chopping instrumentation amplifier architecture making use of DDA structure has 4 input terminals which form 2 input ports, $G_{m,in}$ and $G_{m,fb}$. The input signals are modulated by INS input choppers Ch_1 and Ch_2. The signals are then modulated at odd harmonics of the chopping frequency while the demodulation is conducted at the low-impedance nodes by chopper Ch_3 as shown in Figure 5.3. Having the demodulation at the low impedance node, the residual offset caused by the demodulation activity can be minimized.

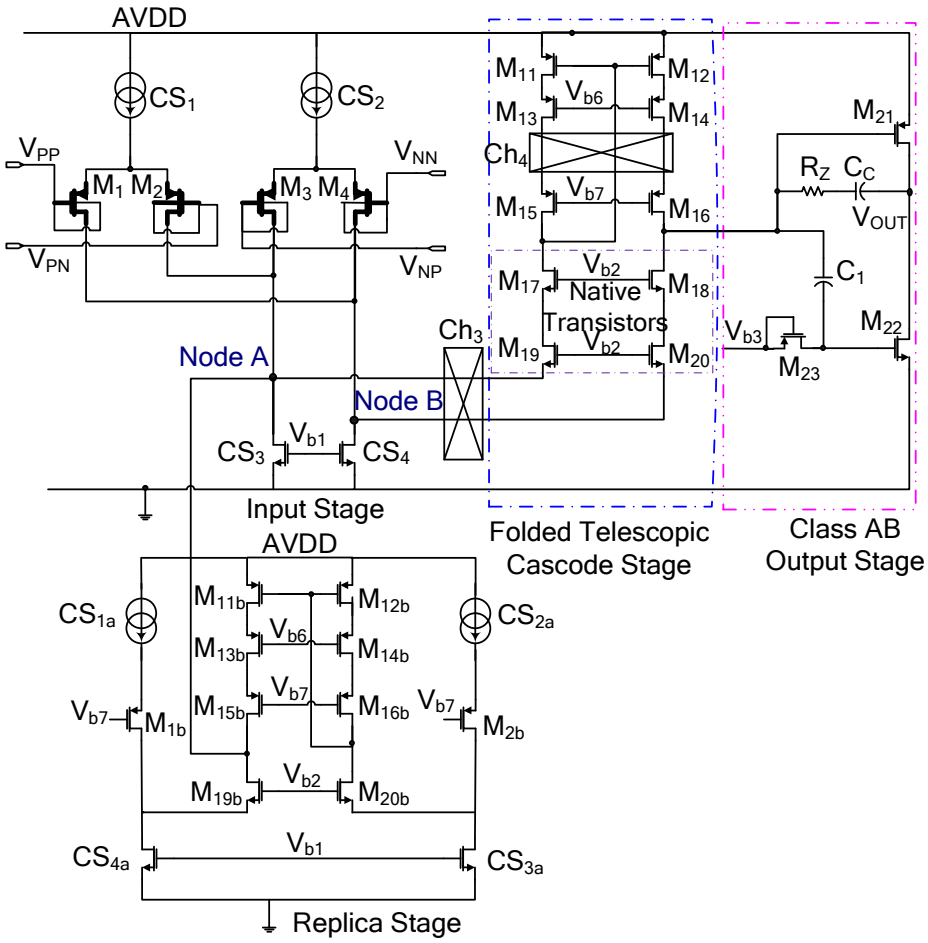


Figure 5.3 The proposed differential difference amplifier and its replica for offset current reduction.

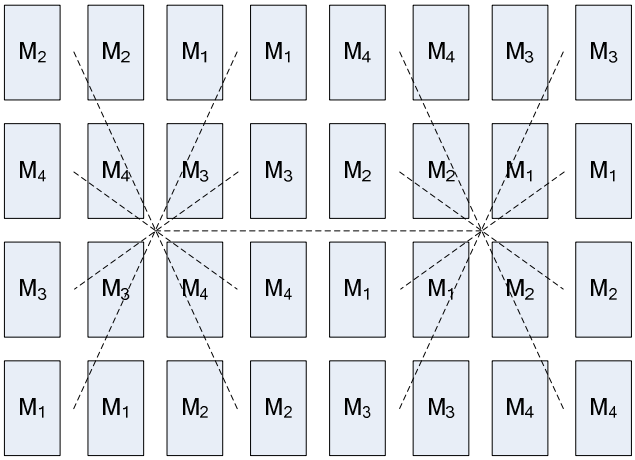
The fourth chopper, Ch_4 is embedded within the self-biased cascode current mirror to up-modulate the errors from them [72]. The ratio gm_1/gm_{11} is designed to be high enough to limit the noise and offset voltage contributed from the upper cascode current mirror. In the design, the output ripple contributed by the mismatch of the cascode current mirror is less than 0.15 times of the output ripple caused by the mismatch of input transistors.

In chopping DDA design, the differential common-mode signal, V_{cd} [23] is not modulated by the chopping operation as discussed in Section 4.2, despite the common-mode signals being suppressed by chopper operation,. As a result, highly symmetrical DDA with balanced input and output current in the first gain stage ensures good differential common-mode rejection ratio, $CMRR_d$ performance [82]. However, due to mismatch of the device pairs, $CMRR_d$ becomes significant. It will affect suppression of V_{cd} which is not modulated to chopping frequency, hence increasing the input-referred offset. To reduce the output offset ripple arising from mismatches of the critical component pairs, a simple current source replica structure employing the pair matching layout technique [83] is added. The input transistor pairs and current source pairs drawn bold in Figure 5.3 make use of the dedicated pair matching layout technique which will be discussed next.

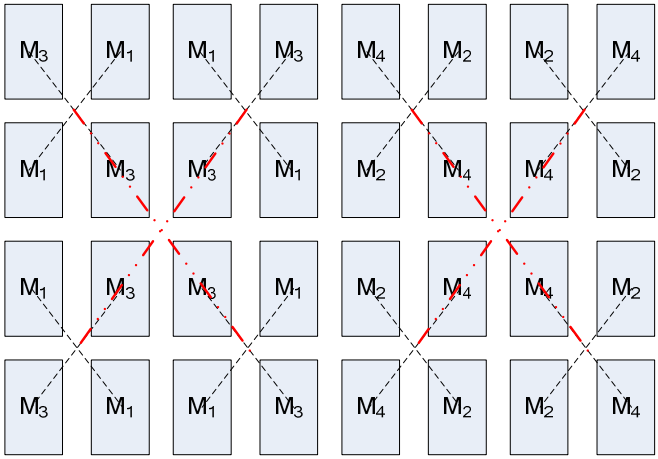
5.4. Pair Matching Layout Technique

In the instrumentation amplifier design, mismatch of the threshold voltage and transconductance factor of the transistor pairs has to be minimized to achieve ultra low offset voltage and smaller output ripple. Any change of process characteristics along the structure causes small variations in closed components known as local inaccuracy between adjacent devices. The use of symmetrical layouts made by two mirrored half-cells ensures an axis of symmetry, but a gradient in the direction orthogonal to that axis still causes mismatch [84].

Since the matching of the input transistor pairs in DDA permits a better balancing characteristic of input ports for better common-mode signals rejection and smaller dc offset, careful layout technique is achieved by placing the critical input transistor pairs and current source pairs in the symmetry and common-centroid layout structure [85]. This permits compensating the gradients to the first order in both directions. However, for multi-input amplifiers, such as DDA, matching the four-input-transistor group accurately is difficult and not necessarily the best solution. Hence, In this work, the pair matching layout [83] is employed.



(a)



(b)

Figure 5.4 (a) Common-centroid in averaging layout for M_1–M_4 (b) Pair matching layout for transistor pairs (M_1, M_3) & (M_2, M_4).

Consider devices M_1 to M_4 that have identical structure and size. The common-centroid averaging layout [86] for the input matching pairs (M_1, M_2) and (M_3, M_4) as shown in Figure 5.4(a), is re-arranged as (M_1, M_3) and (M_2, M_4) in the layout matching pairs, where the bracket denotes the group containing the local matching transistors. Each transistor is split into 8 identical elements to form the common-centroid in common-centroid layout style having the matching pairs as shown in Figure 5.4(b). The offset voltage [83] caused by the input transistors of the DDA can be written as the mismatch effects of the critical parameters of the devices as follows:

$$V_{os,M1-M4} = (V_{th_{M_1}} - V_{th_{M_2}}) - (V_{th_{M_3}} - V_{th_{M_4}}) + S_P^O(\cdot)(\beta_{M_1} - \beta_{M_3}) + S_N^O(\cdot)(\beta_{M_2} - \beta_{M_4}) \quad (5.7)$$

where transistors M_1 and M_3 share the same sensitivity function, $S_P^O(\cdot)$, of the transconductance parameter, while transistors M_2 and M_4 share another sensitivity function, $S_N^O(\cdot)$. In the pair matching layout, M_1 and M_3 are treated as a local matching pair and placed in close vicinity; resulting in beta parameters that have similar values. Thus, the (M_1, M_3) beta-related offset is reduced although beta parameters of M_1 and M_2 may be different. The same goes for M_2 and M_4 as a local matching pair. Consequently, the offset voltage is less sensitive to beta parameters for the case of DDA input pairs. Since the sensitivity factors are small, the product of a sensitivity factor and a difference term tends to be insignificant.

For the biasing current, the offset currents arising from the mismatch of input pair M_1–M_2 tends to counteract that of the M_3–M_4 pair when summing the offset currents at nodes A and B. Due to the cross-couple summing branches and common centroid layout between the current sources CS1 and CS2, the effect of mismatch in bias currents are averaged out. This means that the mismatch of current sources CS1 and CS2 are not of concern to the dc offsets. However, the difference of two current sources CS3 and CS4 will generate an offset

current which will deteriorate the $CMRR_d$ and contribute the ripple at the output. The problems will be relaxed by introducing the current replica circuit in next section.

5.5. Current Source Replica Circuit

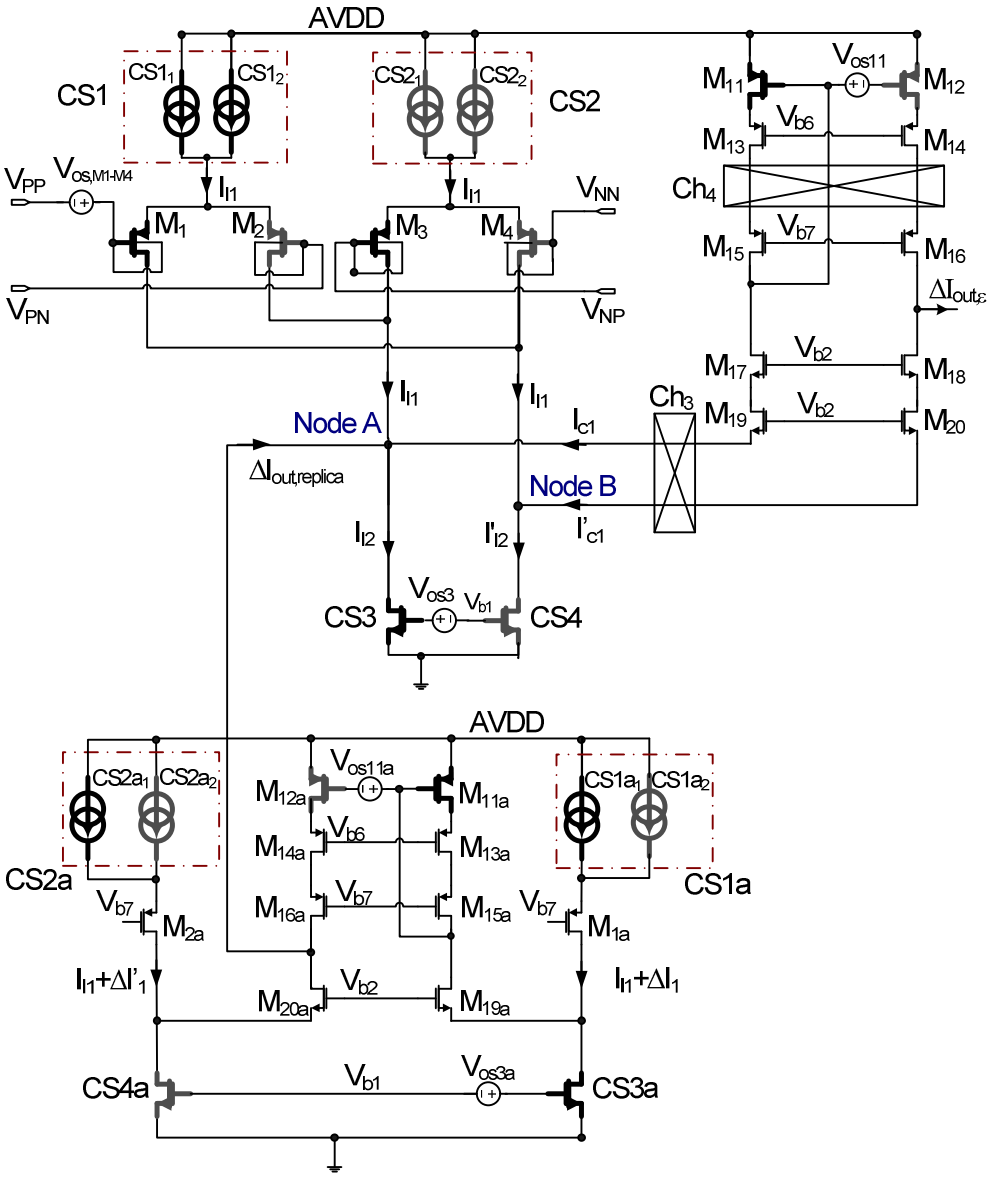


Figure 5.5 Offset current cancellation using current source replica circuit

Minimal output ripple in the proposed differential difference amplifier requires an accurate transistor matching in the input stage as well as the current sources. The current source replica (CSR) circuit is proposed to facilitate the pair matching layout by extending it to other critical transistor pairs, such as current sources and current mirrors in the first gain stage depicted in Figure 5.5. This is in contrast to conventional DDA where the pair matching layout only applies for the four input transistors but not on the two current source transistors

and two current mirror transistors (upper side or lower side). The idea is to generate a counteract offset current to nullify the offset current arising from the critical current sources in the main amplifier's cascode stage on the basis of similar mismatch characteristics between the two blocks.

In the replica stage design, the current sources CS1a–CS2a, CS3a–CS4a and self-biased cascode stage formed by the transistors M_{11a}–M_{16a}, M_{19a}–M_{20a} are designed the same with respect to the corresponding transistor in the main stage on the basis of tracking and matching characteristics. For generation of counteract offset current, the current source transistor pairs, (CS3, CS3a) and (CS4, CS4a), (M_{11}, M_{11a}) and (M_{12}, M_{12a}), are grouped for pair matching layout as described previously. With this arrangement, the corresponding offset voltage V_{OS3} for the transistor pair CS3–CS4 and V_{OS3a} for the replica transistor pair CS3a–CS4a can be represented as

$$V_{OS3} = V_{GS_{CS3}} - V_{GS_{CS4}} \tag{5.8}$$

$$\begin{aligned} V_{OS3a} &= V_{GS_{CS3a}} - V_{GS_{CS4a}} \\ &= (V_{GS_{CS3}} + \sigma_{GS3}) - (V_{GS_{CS4}} + \sigma_{GS4}) \\ &\approx V_{OS3} \end{aligned} \tag{5.9}$$

$$\sigma_{GS3} \approx \sqrt{\frac{{A_{VT_{CS3}}}^2}{(WL)_{CS3}} + \frac{{A_{KP_{CS3}}}^2}{(WL)_{CS3}}\left(\frac{I_{ds_{CS3}}}{gm_{CS3}}\right)^2} \approx \sigma_{GS4} \tag{5.10}$$

where σ_{GS3} and σ_{GS4} are the standard deviation of gate-source voltage mismatch for the matching group pairs (CS3, CS3a) and (CS4, CS4a) respectively; A_{VT} and A_{KP} are the threshold voltage and transconductance mismatch factors, respectively [85]. Careful layout in matching a transistor pair is important to ensure the localised mismatch error to be minimized. As a result, the offset voltage V_{OS3a} for the replica transistor pair CS3a–CS4a will be close to the offset voltage V_{OS3} for the transistor pair CS3–CS4. Similarly, this applies to

the transistor pair M_{11}–M_{12} and the replica pair M_{11a}–M_{12a} which are also arranged in the pair matching layout. Consequently, V_{OS11a} is very close to V_{OS11} in the main amplifier.

To calculate the input DC offset voltage for the amplifier in Figure 5.5, the output error current, $\Delta I_{out,main}$ of the main amplifier due to the mismatch error of the matching transistor pairs without modulation can be approximated as

$$\Delta I_{out,main} \approx gm_1 \cdot V_{os,M1-M4} + gm_{CS3} \cdot V_{os3} + gm_{M11} \cdot V_{os11} \tag{5.11}$$

The effect of mismatch errors contributed from the cascode transistors M_{13}–M_{20} are relatively small, and can be neglected. With the pair matching layout applied to the critical pairs in the design, a corresponding offset compensation current, $\Delta I_{out,replica}$ of the replica stage caused by similar mismatch current sources is injected to the main amplifier circuit at node A to minimize the resultant offset current. It can be described as

$$\Delta I_{out,replica} \approx gm_{CS3a} \cdot V_{os3a} + gm_{M11a} \cdot V_{os11a} + (\Delta I_1 - \Delta I_1') \tag{5.12}$$

where $(\Delta I_1 - \Delta I_1')$ is the current mismatch between CS1a–CS2a. Cross coupling pair matching layout is adopted for CS1a and CS2a in the replica stage with respect to CS1 and CS2 transistors in the main stage. In the replica stage, CS1a is laid out as the sum of current sources obtained from the respective copy branch of CS1 and CS2 (i.e. $CS1a_1$ matches with $CS1_1$ of CS1 whereas $CS1a_2$ matches with $CS2_1$ of CS2). The same applies for CS2a. Note that the respective replica stage sources are placed in close proximity with the main current sources CS1 and CS2. This arrangement ensures good matching among the tail current sources in the replica stage and main stage. Therefore, the offset sensitivity with respect to CS1a and CS2a in the replica circuit is small.

Finally, the reduced residual offset current becomes $\Delta I_{out,main}$–$\Delta I_{out,replica}$ instead of $\Delta I_{out,main}$. It will be up-modulated by chopper Ch_3 and chopper Ch_4 respectively and appear as a smaller output ripple at the output of main amplifier. The reduced residual offset current $\Delta I_{out,\varepsilon}$ can be obtained as

$$\begin{aligned}\Delta I_{out,\varepsilon} &= \left(\Delta I_{out,main} - \Delta I_{out,replica}\right) \cdot m(t) \\ &= \left\{gm_1 \cdot V_{os,M1-M4} + gm_{CS3} \cdot (V_{os3} - V_{os3a})\right. \\ &\left. + gm_{M11} \cdot (V_{os11} - V_{os11a}) - (\Delta I_1 - \Delta I_1')\right\} \cdot m(t)\end{aligned} \tag{5.13}$$

where $m(t)$ represents the chopping function [46] at chopping frequency, f_{Ch}, which can be described in Fourier series: $m(t) = 2\sum_{k=1}^{\infty} \frac{sin(k\pi/2)}{(k\pi/2)} cos(2\pi f_{ch} kt)$. The resultant residual offset current, $\Delta I_{out,\varepsilon}$ is smaller when the pair matching layout is applied to both input transistors and critical current sources in the design. Furthermore, the current mismatch of current sources CS1a–CS2a is insignificant using the cross-coupling pair matching layout as well as the small value of gm_{CS1a} compared to the current sources CS3a–CS4a. Hence, the overall DC offset from the device mismatches will be minimized.

In the proposed chopper-stabilization amplifier design, the output ripple peak-to-peak can be approximated as

$$\begin{aligned}V_{o,ripple} &= \left[V_{os,M1-M4} + \frac{(\Delta I_1' - \Delta I_1)}{gm_1}\right. \\ &+ \frac{gm_{CS3}}{gm_1} \cdot (V_{os3} - V_{os3a}) + \frac{gm_{M11}}{gm_1} \cdot (V_{os11} \\ &\left. - V_{os11a})\right] \frac{gm_1}{\pi \cdot f_{Ch} \cdot C_C} \\ &\approx V_{os,M1-M4} \cdot \frac{gm_1}{\pi \cdot f_{Ch} \cdot C_C}\end{aligned} \tag{5.14}$$

where gm is the transconductance of the transistor, C_C is the compensation capacitor, f_{Ch} is the chopping frequency while $V_{os,M1-M4}$ is the equivalent DC offset arising from the mismatch of identical designed transistors in layout pairs (M_1, M_3) and (M_2, M_4). For the transconductance $gm_1 \gg gm_{CS3} > gm_{CS1a} > gm_{M11}$ as well as the reduced offset current through CSR circuitry, the output ripple becomes dominated by the equivalent DC offset from the input transistors.

5.6. Summary of Chopper-Stabilized Differential Difference Amplifier

In short, the proposed low noise and high gain DDA is realized using gate-bulk driven inputs as well as folded telescopic cascode topology with the help of Native transistors. The DDA gives an improved noise performance and high gain characteristic with minimal area and power consumption. Besides, a simple CSR circuitry is added to reduce the output ripple by generating similar level of mismatch offset current to nullify the mismatch offset current arising from the input stage of DDA. As a result, the difference of two similar mismatch offset currents will be smaller than the offset current from the difference of two current sources in a conventional DDA without CSR.

The proposed CSR has second function. When it permits full application of pair matching layout technique to all the critical pairs in whole input stage, the matching performance of the input stage is enhanced. This avoids the significant deterioration of $CMRR_d$ [82] due to device mismatches which leads to the increase of input offset of DDA. Note that the differential common-mode signal pertaining to $CMRR_d$ is not modulated by the chopping activity as shown in Section 4.2.

CHAPTER 6

DIGITAL CONTROL LOGIC DESIGN

6.1. Introduction

The proposed chopper-stabilized differential difference amplifier in Figure 4.1 contains three modules: the modulators, the differential difference amplifier with its current source replica circuit, and the demodulator. The modulation technique is used to transpose the desired low frequency signal to a higher frequency, fch where the 1/f noise is less. In order to minimize the charge injection effect in the chopping operation, the modulator in the proposed design has discussed in Section 4.4.2 using the continuous-time INS switches with modified control clock to suit the chopping operation.

Digital control logic blocks are required to control the modulator as well as the demodulator to ensure the proper operation of the chopper-stabilization activity. Generally, the working principle of the digital control logic block is to generate the non-overlapping digital clocks that required based on input clock signal applied. In the proposed design, the input clock signal is the chopping clock with a frequency of 10 kHz. Figure 4.6 shows the control signals required in the chopper-stabilized operation. The required clock signals are generated from the digital logic which is basically built up by inverters, delay cell, NAND gates, NOR gates and buffers. The generation of each signal will be discussed next.

6.2. Logic Circuits

6.2.1. Non-overlapping Clock Design

One pair of non-overlapping clocks generated based on the input of the main chopping frequency signal which is named as ϕ_1 and ϕ_2. As discussed, the non-overlapping clocks are needed to control the switches in both the modulator and demodulator. They determine when and where the charge transfer occurs. Therefore, they must be carefully designed to be able to realize the non-overlapping period in order to ensure that the charge is not unintentionally lost or causes false action on the analog part.

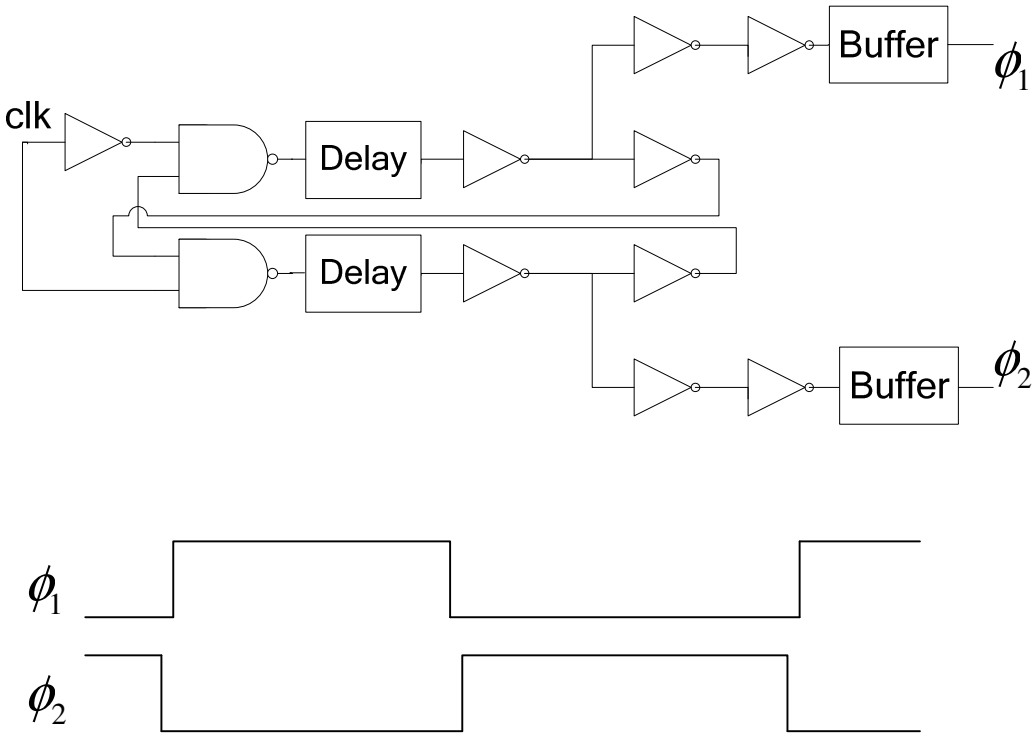


Figure 6.1 Digital logic for non-overlapping clock generation

Figure 6.1 shows the block diagram of the digital logic used to generate the non-overlapping clock. Clk is the input chopping signal, which is 10kHz square wave with a duty cycle of 50%. The delay cell in the diagram is made up by even number of inverters which is used to determine the non-overlapping period between 2 non-overlapping clocks. The main

advantages of this circuit are its simplicity and robustness. Besides, inverter-based buffers are included in the design for some driving capability for the parasitic along the non-overlapping clock signal line. Some margin is added to accommodate the process and temperature variations in the design.

6.2.2. Continuous-time INS Control Clock Signal

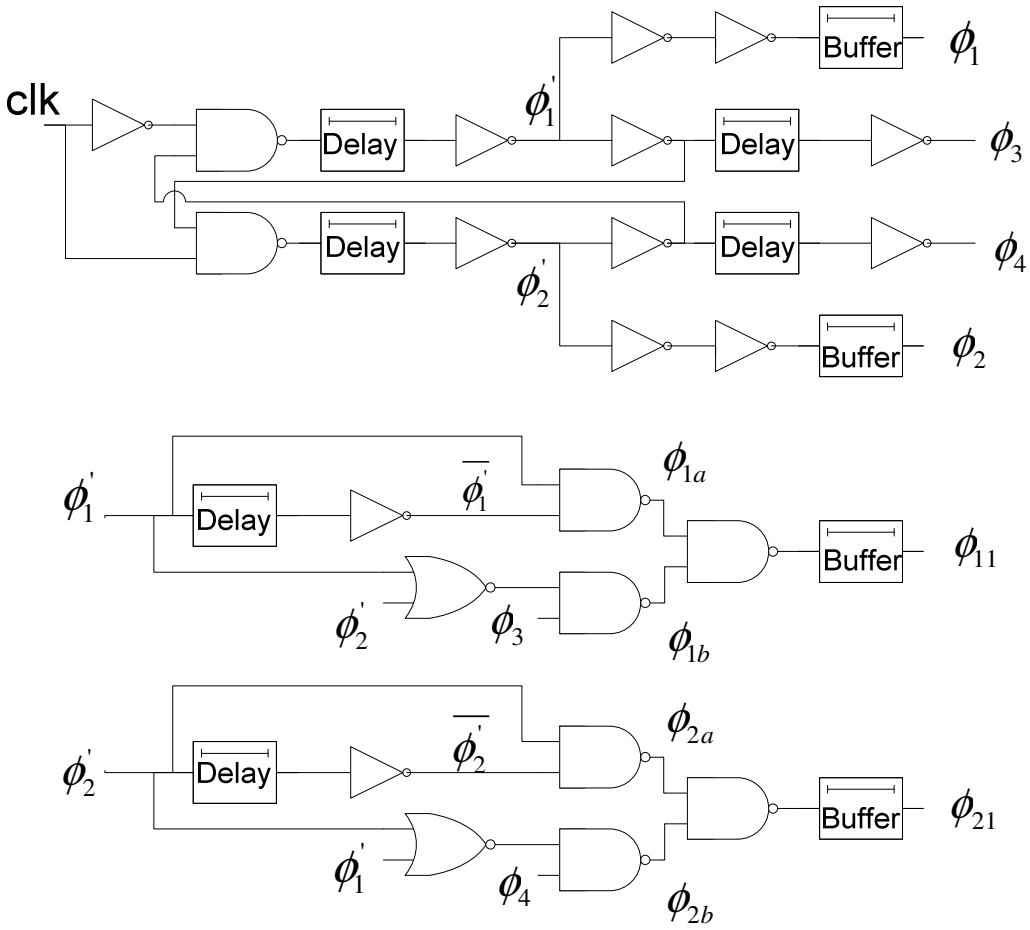


Figure 6.2 Digital logic for INS clock

In addition to the non-overlapping clocks, ϕ_1 and ϕ_2, extra digital control logic circuits are need to generate the continuous-time INS control clock signal, ϕ_{11} and ϕ_{21}. They are used to control the MOS switches in the INS switches for the charge-injection nulling purpose as discussed in Section 4.4.2. Figure 6.2 shows the digital logic used to generate the

required digital control signals where clock ϕ_{11} and ϕ_{21} are used to drive the n-channel switches. The timing diagram of the clock generation for ϕ_{11} is shown in Figure 6.3.

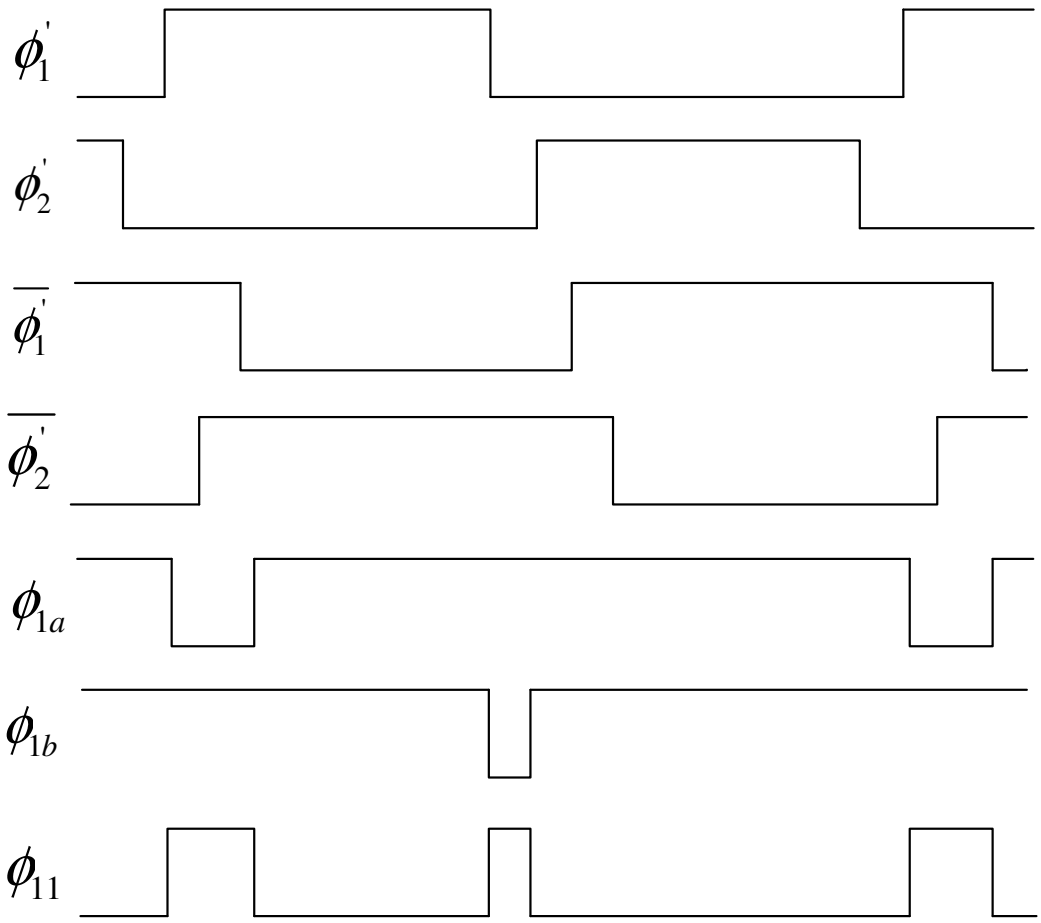


Figure 6.3 Timing diagram of the clock generation for ϕ_{11}

CHAPTER 7

LAYOUT CONSIDERATIONS

7.1. Introduction

In the chopper stabilized instrumentation amplifier design, careful layout is essential to ensure the good performance of the circuit as well as maximize the yield of the design. Good matching properties of critical devices in the circuit always rely heavily on the layout approaches used as there are many practical issues in fabrication environment, for example process variation, parasitic effects etc. Besides, a well-planned layout floor plan will minimize the die area required as well as the possible crosstalk and coupling noise. In this chapter, the layout considerations and floor planning of the proposed chopper-stabilized instrumentation amplifier are discussed.

7.1.1. Chopper layout

The accuracy of the output always affected by the residual offset generated during the chopping activities. Hence it is important to take extra care in the layout of the input chopper. In the chopping operation, the spikes appearing at each input of the differential difference amplifier is related to the symmetrical of the switches. When placing the switches in the chopper, the metal routing from switch to the inputs of the DDA is also important.

The input chopper consists of 4 cross-coupled NMOS with minimum size as shown in Figure 7.1. The mismatch of parasitic capacitors, cp1 (from ϕ_1 to Vout1) and cp2 (from ϕ_1 to Vout2) caused by the metal routing and asymmetric layout will give rise to asymmetric

spikes at the input port. Due to the non-identical spikes, the spikes will not be cancelled well as the common-mode signal at the input ports, and this will cause the increase in residual offset. Therefore, in the chopper layout, the metal routing and switches placement have to be symmetrical as shown in Figure 7.2. Parasitic capacitors, cp1 has to be matched with cp2 whereas, while cp3 has to be matched with cp4. The distance of the matched switches to each input line should be the same.

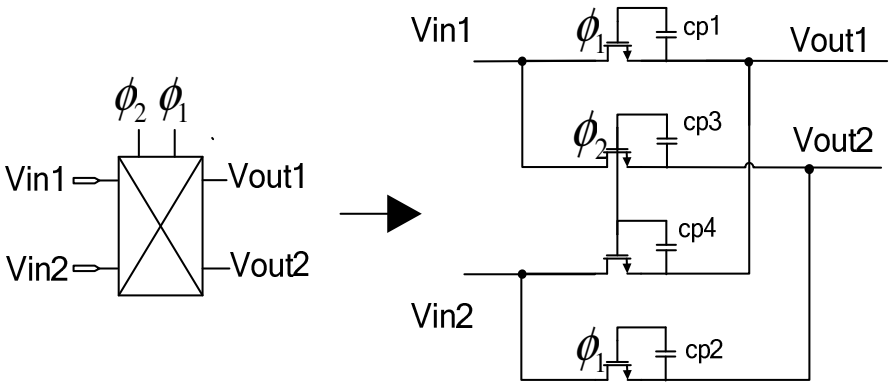


Figure 7.1 Illustration of switches in a chopper with parasitic capacitors from clock lines to inputs of amplifier

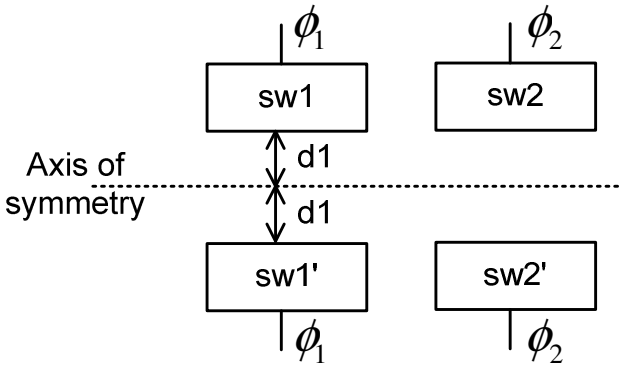


Figure 7.2 Symmetry placement of switches in layout

7.1.2. Matching Consideration

As discussed in the Chapter 5, matching of the critical transistors are essential to ensure high precision in analog circuit. The random mismatch effect is the non-ideal effect in layout consideration. It will impact the circuit performance if the layout is not considered

critically from the perspectives of devices placement. In the proposed design, pair matching layout is used associated with the proposed current source replica circuit to enhance matching characteristics of the current mirrors as well as the differential input pairs. The common-centroid technique is utilized in order to reduce the mismatch of the matching devices.

Besides, the boundary dependent etching of silicon gates will also cause mismatch in layout. This lateral etching effect in CMOS process can be serious for precision circuit design but it can be eliminated by adding the dummy polysilicon or dummy transistors around the critical transistors to protect the boundary etching.

7.1.3. Noise Consideration

Besides, the chopper-stabilized amplifier requires digital clock generator for control signal generation. These control signals switch at chopping frequency can be highly noisy if they are coupled to analog signal lines, causing the degradation of system performance. With this arrangement, proper isolation of analog blocks from digital part is required. Other than that, the guard rings are also added around each transistor group to prevent the circuit from coupling the substrate noise and to prevent the possibility of latch-up.

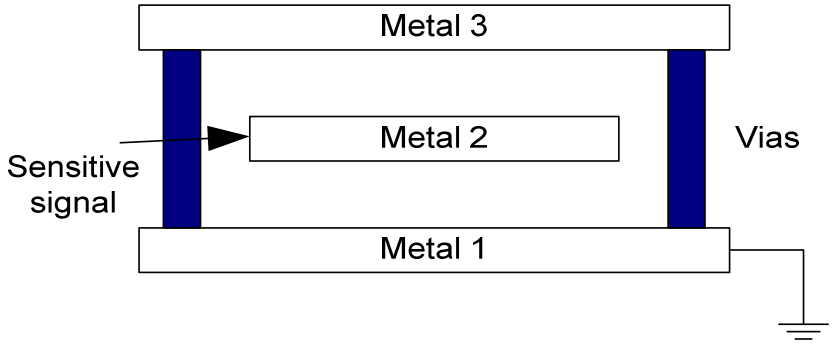


Figure 7.3 Illustration of noise shielding of sensitive signal line

In order to minimise the noise coupling at the inputs of the amplifier, noise shielding layout technique is applied. This is done by having 2 grounded metal layers on top and below

the sensitive signal line as illustrated in Figure 7.3. With this layout structure, the sensitive signal line is shielded from any coupling noise as it is isolated from external environment.

7.2. Floor Planning and Power Rails Layout

High frequency switching of digital signals will be coupled to the analog sections through the power supply or substrate or control signal lines if careful layout consideration is not applied to minimize these noise coupling effects. Hence, in the layout, the digital block i.e. clock generator is placed apart from the noise sensitive analog blocks. Besides, in the routing of the analog and digital signal lines, an addition metal line connected to ground is added to give a better isolation as well as to reduce the crosstalk effect as shown in Figure 7.4.

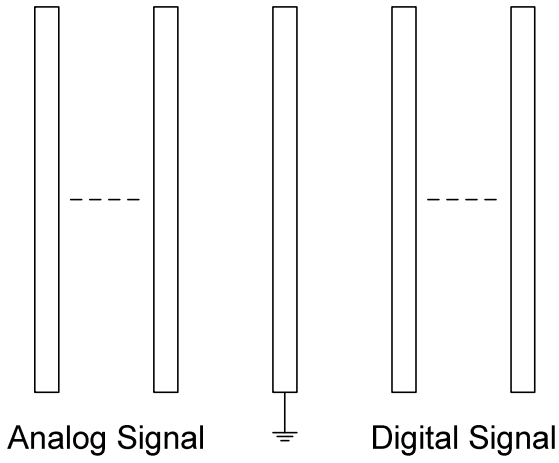


Figure 7.4 Isolation of analog and digital signal lines using a ground line

The power supply is another source of noise coming into the analog section. If the analog and digital parts share the same power supply, the noisy power would limit system resolution. The solution would be for both digital and analog parts to have separate power supplies, where DVDD and DVSS are for the digital circuit, whereas AVDD and AVSS are for the analog circuit. In the layout, the width of each power line is determined by the

maximum current and voltage drop allowable in the design to prevent electromigration. The supply rails are connected to the pads in a star configuration as illustrated in Figure 7.5.

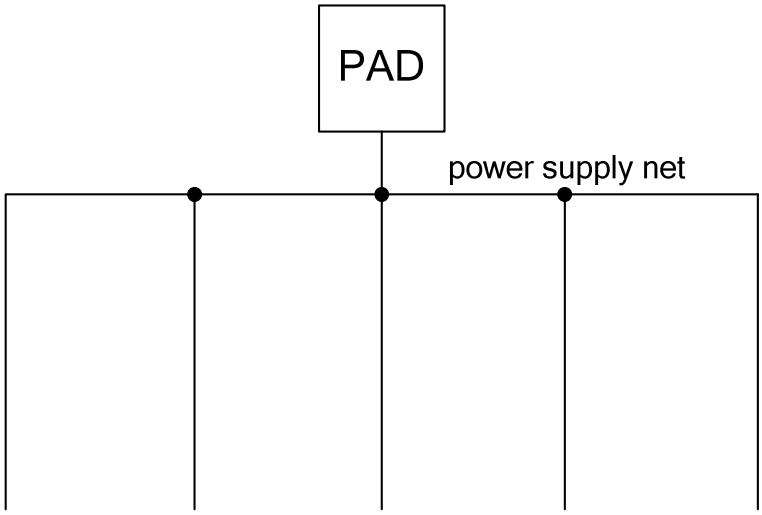


Figure 7.5 Power supply distribution

CHAPTER 8

RESULTS AND DISCUSSIONS

8.1. Introduction

In this chapter, the performance of the proposed high PSR regulator in Section 3.3, low noise broadband PSR regulator in Section 3.5 are discussed and verified in 0.18µm CMOS process. Each design is compared with other prior-art works in terms of PSR or noise performance. This will be followed by the measurement results and discussions for the proposed instrumentation amplifier and DDA in Chapters 4 and 5 respectively.

The proposed instrumentation amplifier is useful as the analog front-end (AFE) circuit such as to amplify the strain-gauge sensor output signal which is usually in the millivolt or microvolt range to a point where it falls within the input voltage range of the next circuit block, ADC. In order to verify the proposed low offset, ripple reduction chopper-stabilized instrumentation amplifier, a series of simulation and experimental results are presented and discussed. A comparison on the measured performance of the proposed chopper-stabilized instrumentation amplifier with other published work is shown.

Finally, the integration of: the proposed high PSR voltage regulator, digital clock generator, low offset small area differential-difference instrumentation amplifier circuit blocks described in the previous chapters is presented in this chapter for strain gauge based sensor data acquisition application. The proposed system measurement results with emulated strain-gauge pressure sensor in Wheatstone bridge configuration are discussed. A comparison with other AFEs dedicated for strain-gauge transducer published in the literature is shown at the end of this chapter.

8.2. Low-Power, High PSR Regulator

The proposed high PSR regulator in Section 3.3 is designed to achieve high PSR performance while consuming small quiescent current. The model frequency behaviour is plotted based on the analysis done in Section 3.3.1 and the experimental results are presented.

8.2.1. Model Frequency Behaviour

A design example of Figure 3.7 is illustrated using CSM 0.18µm CMOS process technology by employing transistors with the following dimensions, $(W/L)_{M1,M2} = 36\mu m/4\mu m$; $(W/L)_{M3,M4} = 30\mu m/0.3\mu m$; $(W/L)_{M5} = 24\mu m/1.2\mu m$; $(W/L)_{M6} = 12\mu m/12\mu m$; $(W/L)_{M7} = 8\mu m/1\mu m$; $(W/L)_{M8} = 70\mu m/5\mu m$; $(W/L)_{M9} = 1\mu m/4.5\mu m$; $(W/L)_{M10} = 65\mu m/3\mu m$; Let the quiescent currents be $I_{M8} = 1\mu A$; $I_{Q1} = I_{Q2} = 0.5\mu A$; $I_{M5} = 2\mu A$ and the choice of component values as $Cc_1 = 4.3\text{pF}$; $Cc_2 = 4.5\text{pF}$; $R_1 = 217\text{k}\Omega$; $R_2 = 38.4\text{k}\Omega$; $R_3 = 129.2\text{k}\Omega$; $R_4 = 596.6\text{k}\Omega$; $R_5 = 263.3\text{k}\Omega$; $R_6 = 577.9\text{k}\Omega$; $R_L = 50\text{k}\Omega$.

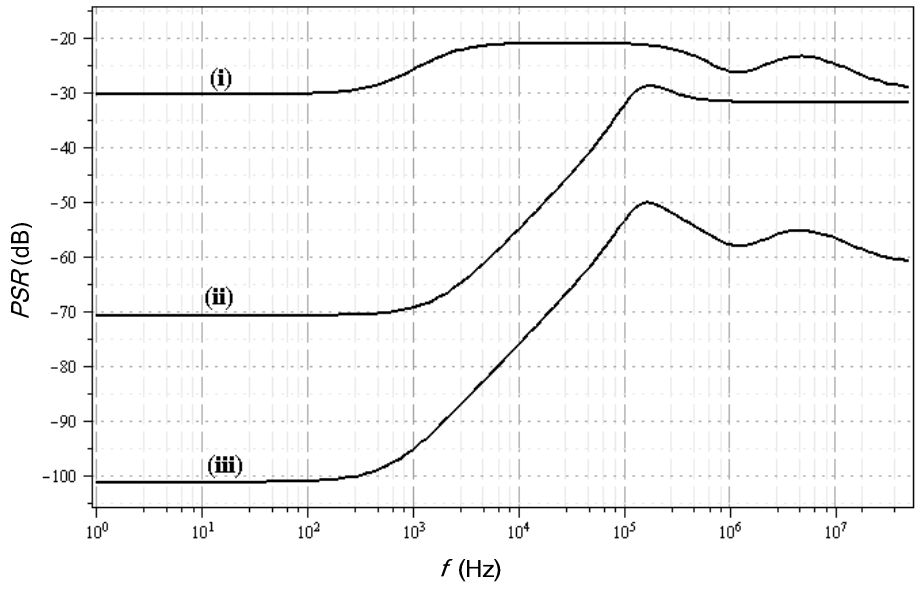


Figure 8.1 Frequency behavior of the PSR curves (i) $PSR_{Brokaw\_bandgap}$ (ii) $PSR_{pre\_regulator}$ (iii) $PSR_{overall}$

The model frequency behavior of the PSR curves for $PSR_{Brokaw\_bandgap}$ and $PSR_{pre\_regulator}$ is based on the small-signal analysis of Figures 3.8 and 3.9 with exemplary design values are shown in Figure 8.1. The overall circuit PSR performance, $PSR_{overall}$ is the summation of the curve (i) and curve (ii). It is visible that the overall circuit PSR is improved significantly over wide frequency range.

8.2.2. Measurement Results

The proposed high PSR reference voltage regulator in Figure 3.7 with its startup circuit and bias current generator in Figure 3.10 were fabricated in CSM 1.8V/3.3V 0.18µm triple-well CMOS process technology. The micrograph of the chip is shown in Figure 8.2, occupying a silicon area of 0.047mm^2.

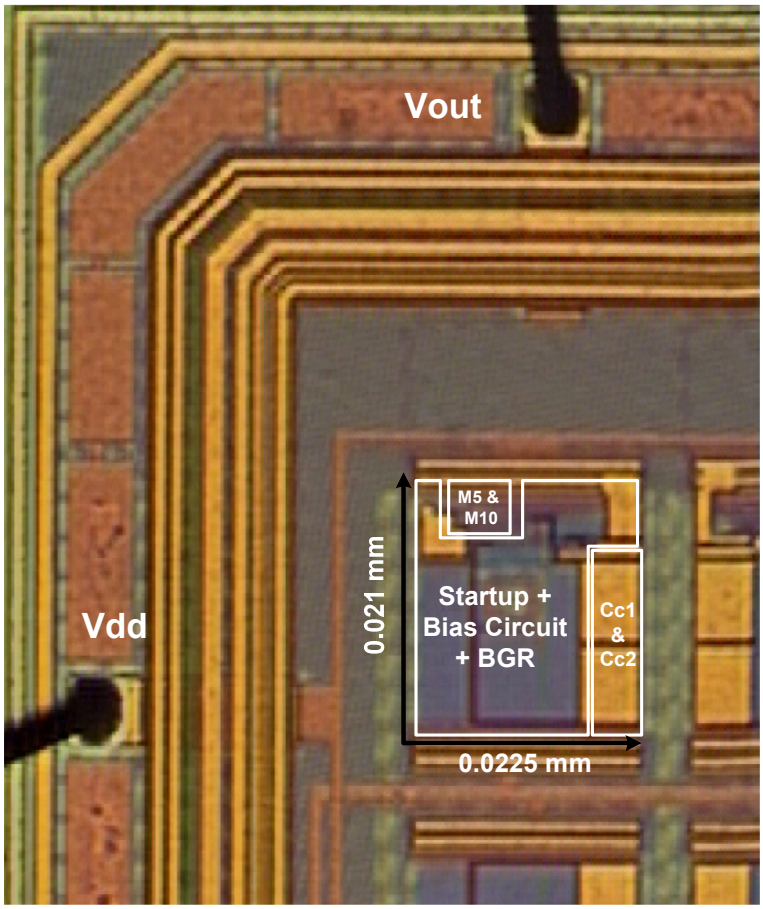


Figure 8.2 Micrograph of proposed regulator

The performance of the micropower regulator is verified by the experimental results: The regulator gives an output voltage of about 1.8V at 300K. It consumes a current of only 5.65μA, with a power dissipation of 16.95μW at a single supply of 3V. When the supply voltage changes from 2V to 3.3V, the output shows an increment of 11mV as illustrated in Figure 8.3 which indicates the line regulation of about 8.46mV/V.

The measured temperature coefficient from -40°C to 125°C for the circuit in the temperature chamber without trimming was 117ppm/°C which is acceptable for a voltage source used for sensor applications. However, this measured result was higher than the simulated result of 25ppm/°C. This might be caused by the incomplete cancellation of temperature effect that is largely due to the inaccuracy of vertical BJT models; mismatch effects associated component pairs and the bootstrapped voltage design of regulator. Trimming for internal monolithic resistors can be applied to obtain better temperature coefficient.

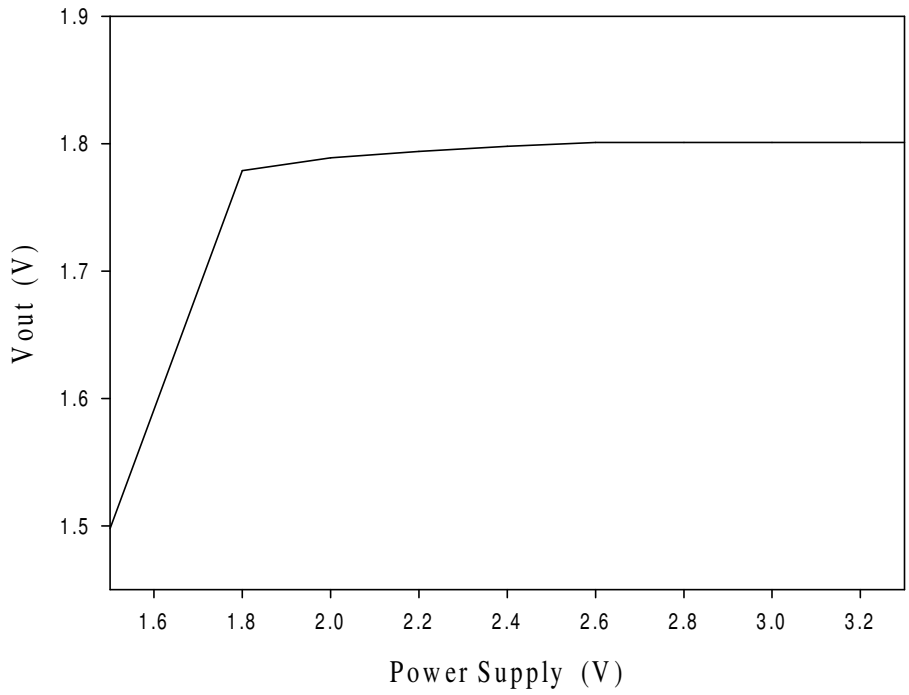


Figure 8.3 Measured output voltage versus supply voltage

The PSR performance of the regulator was validated using a network analyzer (HP 4395A) and an active probe (HP 41800A). Figure 8.4 shows the measured as well as post-layout simulated PSR results for the proposed design with a 50kΩ nominal resistive load. The post-layout simulated PSR curve for the proposed design without the output pad suggests that it is not difficult to maintain the PSR of at least -50dB for few MHz range. However, when the output pad was used for prototype testing, the measured result displayed some degradation at high frequencies. A similar plot with the post-layout simulation result of the proposed circuit incorporating the output pad can be used to explain this, also shown in Figure 8.4. The degradation at high frequencies is due to the existence of 300fF parasitic capacitance associated with the output ESD pad and supply rail. At high frequencies, the effect of feedback loop in the circuit is degraded, and any parasitic from V_{dd} to V_{out} will allow the supply noise to couple directly to the output node through the parasitic capacitance.

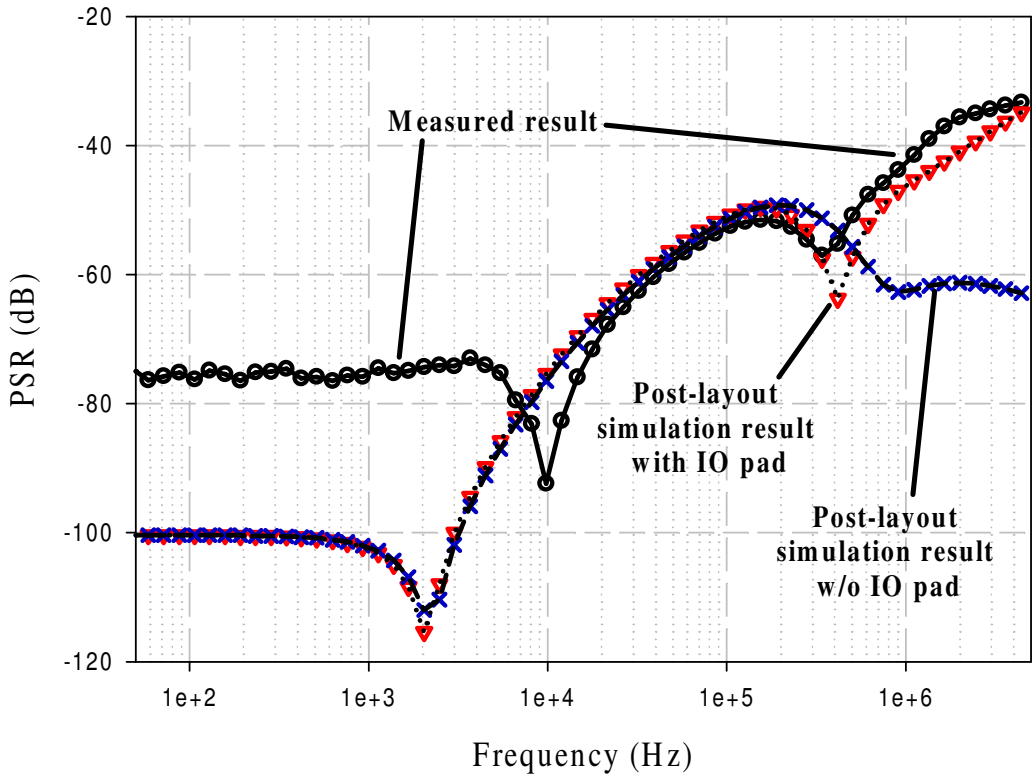


Figure 8.4 Measured and post-layout simulated PSR performance

This degradation can usually be relaxed by adding a big output capacitor from the regulator output to ground but is not desirable because of the cost and space invoked. The measured PSR figures, neither using any supply decoupling capacitor nor adding any output capacitor, were -76dB at 1kHz and -43dB at 1MHz. Herewith, without both types of capacitor, the achieved PSR figures are still very good in the current PSR test even incorporating the output pad.

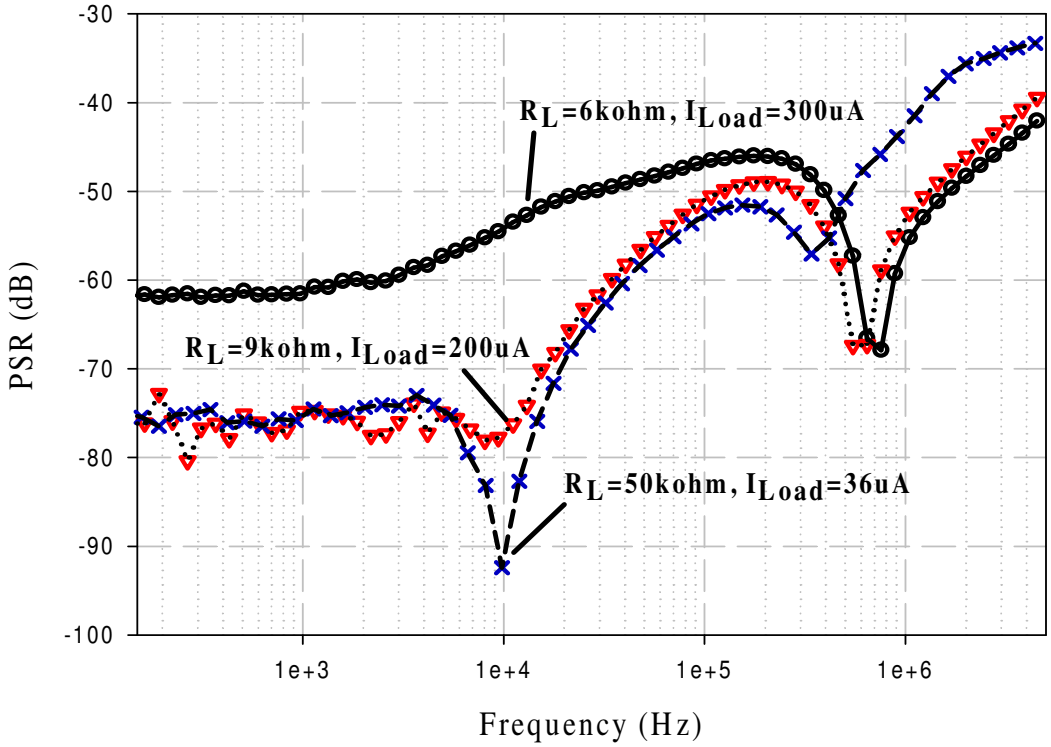


Figure 8.5 Measured PSR results at different output loads

In practical applications, the proposed regulator is a supply source to the critical blocks and it will not be connected to the ESD pad. Hence, its PSR performance will not be degraded at high frequencies. Referring to Figure 8.4, the measured low-frequency PSR value exhibited -76dB whereas the simulated low-frequency PSR value exhibited -100dB. The deviation is caused by the effect of intrinsic noise generated from the micropower circuit

itself. However, as discussed in Section 3.2.2, the intrinsic noise from the circuit will limit the low-frequency PSR performance.

The measured PSR performance under different loading conditions is shown in Figure 8.5. As load current increases, the PSR at low frequencies is degraded 8.46mV/V and improved at high frequencies. The measurement results show that the PSR can attain below -40dB when the loading current increases to 300μA. The experimental results have confirmed that the proposed regulator still maintains reasonable good PSR performance at high frequency (ie 1MHz) without using any external capacitor while sourcing out the current. Higher sourcing current (> 300μA) is feasible but at the expense of reduced PSR.

8.2.3. Comparisons with Other Prior-Art Works

Table 8-I compares and summarizes the performance of the proposed design with the previously published works.

Table 8-I Performance comparison of measured results of prior-art works

	[54] Year 1995	[87] Year 2003	[88] Year 2007	[89] Year 2007	[56] Year 2009	This work
Process	0.9µm CMOS	0.6µm CMOS	0.35µm CMOS	0.6µm CMOS	0.13µm CMOS	0.18µm CMOS
Key Driving Transistor	PMOS	PMOS	PMOS	PMOS	PMOS	NMOS Native with thick oxide
Supply Voltage	2.7V-5.5V	1.5-4.5V	3V	>1.8V	>1.15V	2V -3.3V
Supply Current	300µA	38µA	65µA	70µA	50µA	5.65µA
Power	900µW @ 3V	56µW @1.5V	195µW @3V	126µW @1.8V	57.5µW @1.15V	16.95µW @3V
Vout	1.236V	1.3V	2.8V	1.2V	1V	1.8V
PSR	-95dB@1kHz -80dB@10kHz -55dB@100kHz -40dB@1MHz	-60dB@1kHz -30dB@1MHz	-57dB@1kHz -40dB@800kHz	-70dB@1kHz -40dB@1MHz -27dB@10MHz	-67dB@100kHz -80dB@1MHz & estimated -40dB@40MHz	-76dB@12kHz -50dB@150kHz -43dB@1MHz
T.C.	85ppm/°C	38ppm/°C	NA	NA	NA	117 ppm/°C
Load regulation	NA	0.0325mV/mA	NA	34.2mV/mA	0.0489mV/mA	26.3mV/mA
Line regulation	NA	1.08mV/V	<90mV/V	NA	NA	8.46mV/V
Chip area	0.07mm^2	0.307mm^2	0.29mm^2	NA	0.128mm^2*	0.047mm^2
FOM_{PSRIdd} MHz/mA	13.33	15.79	4.92	14.29	106.7	196.6
Current sourcing capability	No	Yes	Yes	Yes	Yes	Yes
Off Chip Capacitor	No	No	No	No	Yes	No

* With the integrated bandgap circuit. From the micrograph in [56], the bandgap circuit occupied >60% of the total active area of the die.

Since the design objective is to minimize the PSR with minimum biasing current consumption, a figure of merit (FOM) is introduced to quantify the efficiency of a design. A bandwidth of -40dB is used as the reference point in the evaluation of the PSR bandwidth efficiency with respect to the circuit power dissipation. In order to compare different regulators/voltage references having different supply voltages and process technologies, the FOM based on I_{dd} is used whereas technology normalization factor is applied. The technology normalized FOM is defined as follows:

$$FOM_{PSRIdd} = \frac{\text{-40dB Bandwidth PSR}}{\text{Total Supply Current}} \cdot \frac{f_{t\,0.6\mu m\ process}}{f_{t\,\text{process used}}} \tag{8.1}$$

For the FOM_{PSRIdd}, the key driving power transistor design under different CMOS scaling process technologies is pertaining to the achievable device transit frequency, f_t as the key parameter. The FOM_{PSRIdd} is normalised to the transit frequency, f_t of 0.6um CMOS process, mainly because significant number of the works in the comparison was fabricated in 0.6µm CMOS process. The other reason is that the technology is about the midpoint scaling between 2µm and 0.13µm process technology. The nominal transit frequency for 0.6µm PMOS transistor is assumed to be 4GHz, whereas for 1µm, 0.35µm and 0.13µm CMOS process, their PMOS transistors' f_t are about 1GHz, 10GHz and 30GHz respectively. In the proposed micropower regulator, native NMOS is used to relax the headroom problem. However, the thick oxide native device available in the process has a minimum channel length of 1.2µm. Therefore, the transit frequency for the native transistor used in the design is 4.5GHz. With the values, the FOM for the related works are calculated. The higher the FOM_{PSRIdd}, the better the PSR bandwidth efficiency for a given current consumption is.

Table 8-I summarizes the performance comparison of the proposed work with other reported state-of-art works. Of particular interest, it can be seen that the proposed voltage reference exhibits the highest values in FOM. This confirms that the proposed feedback-controlled Brokaw regulator achieves high PSR bandwidth-power efficiency. Moreover, the proposed regulator does not need any off chip capacitor; it is suitable for fully integration. Finally, with the measured maximum sourcing current of 300µA to sustain better than -40dB PSR figures at 1MHz, it is adequate for many micropower sensor circuits. More importantly, it demonstrates that the use of circuit techniques permits the use of lower f_t NMOS thick oxide native transistors without jeopardizing the PSR performance of micropower regulator for sensor applications.

8.3. Low-Noise, Low-Power High PSR Regulator

The design intent of the low noise regulator proposed in Section 3.5 is to achieve high PSR, low noise performance while consuming small quiescent current. This section presents the frequency behaviour of the model plotted using the analysis in Section 3.5.2 followed by the measured experimental results.

8.3.1. Model Frequency Behaviour

Based on the small-signal analysis of the proposed broadband high PSR regulator design shown in Section 3.5.2 using the simulation device parameters, the model frequency behaviour of the PSR curves is plotted in Figure 8.6. The PSR frequency response for the Brokaw bandgap with CMOS transistors only is shown as curve (i) in Figure 8.6 which shows a broadband PSR performance where the high frequency PSR performance is almost same as the low frequency one. By adding a The overall circuit PSR shown in curve (iii) is able to achieve below -65dB over wide up to 50MHz.

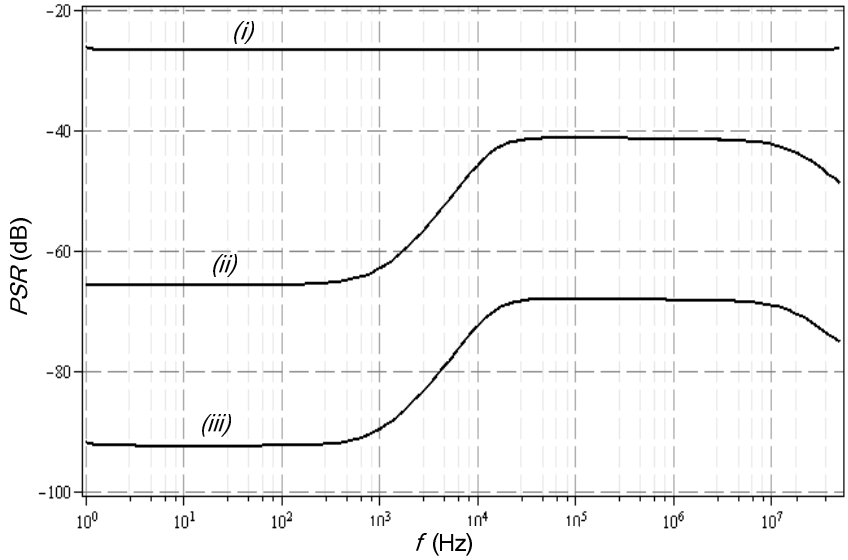


Figure 8.6 Frequency behavior of the PSR curves (i) $PSR_{Brokaw\_bandgap\_withNMOS}$ (ii) $PSR_{pre\_regulator}$ (iii) $PSR_{overall}$

8.3.2. Measurement Results

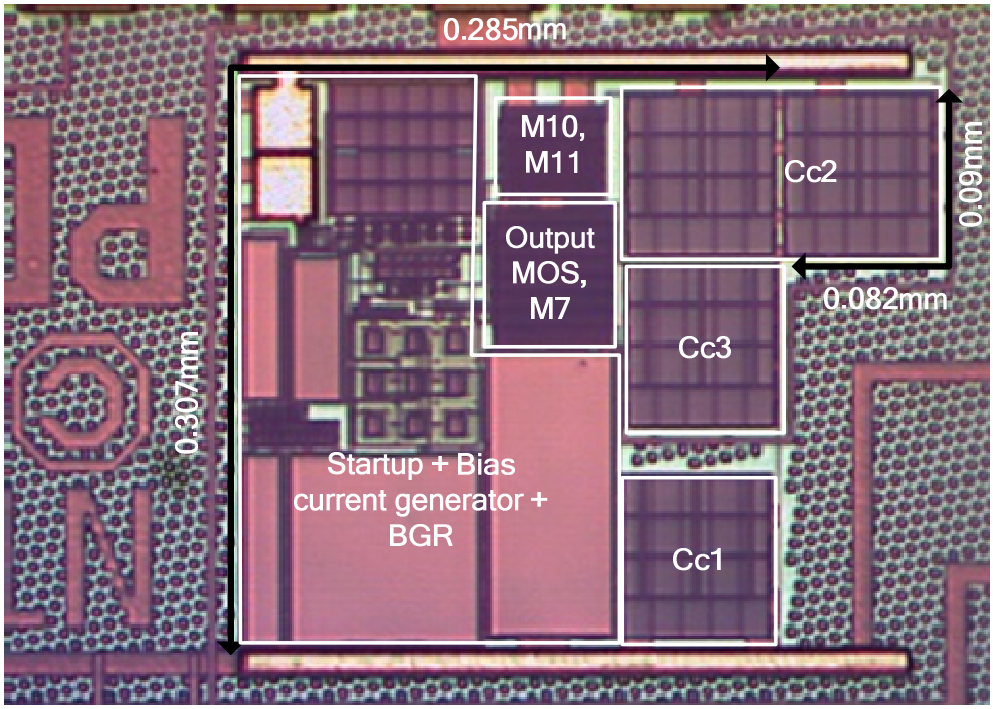


Figure 8.7 Micrograph of proposed ultra-low power high PSR regulator

The proposed regulator shown in Figure 3.12(a) of Section 3.5 was implemented using GlobalFoundries 1.8V/3.3V 0.18µm CMOS process, its micrograph shown in Figure

8.7. It occupies a silicon area of 0.095mm^2 and consumes a total quiescent current of only 1.28µA while giving a measured mean output voltage of 0.992V for 8 samples. The measured line regulation is 0.297%/V from a 1.5V to 1.8V while the measured output voltage has a temperature coefficient (TC) of 130 ppm/ºC within the −20°C to 100°C range without trimming. Better TC can be obtained by resistor trimming.

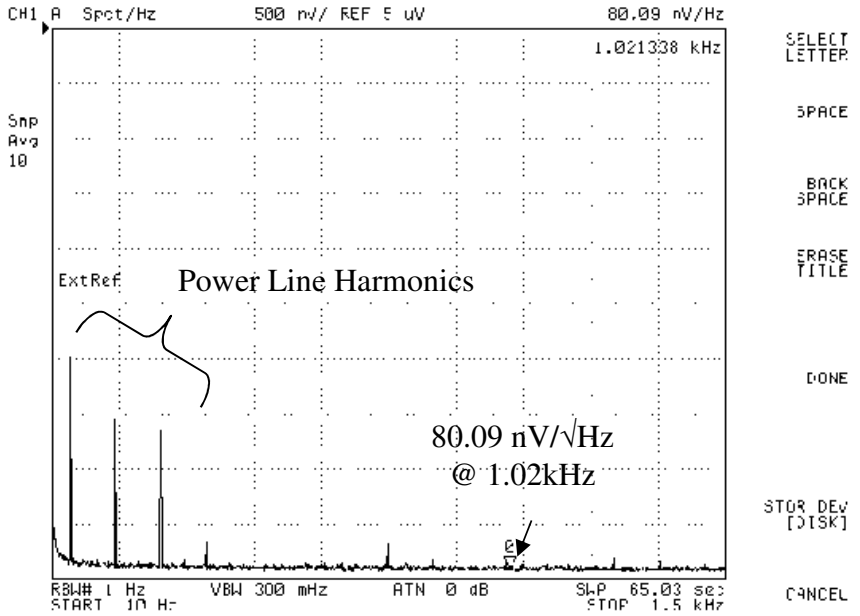


Figure 8.8 Measured output noise spectral density

The output noise spectral density of the proposed design is measured using a spectrum analyzer (HP 4395A) and an active probe (HP 41800A). Figure 8.8 shows the measured output noise spectral density. The proposed low-noise regulator exhibits 80.1nV/√Hz at 1kHz and 14.2nV/√Hz at 100kHz. The integrated output noise over 10Hz-100kHz bandwidth for the regulator is 13.88µVrms. This suggests low noise performance in micropower regulator design.

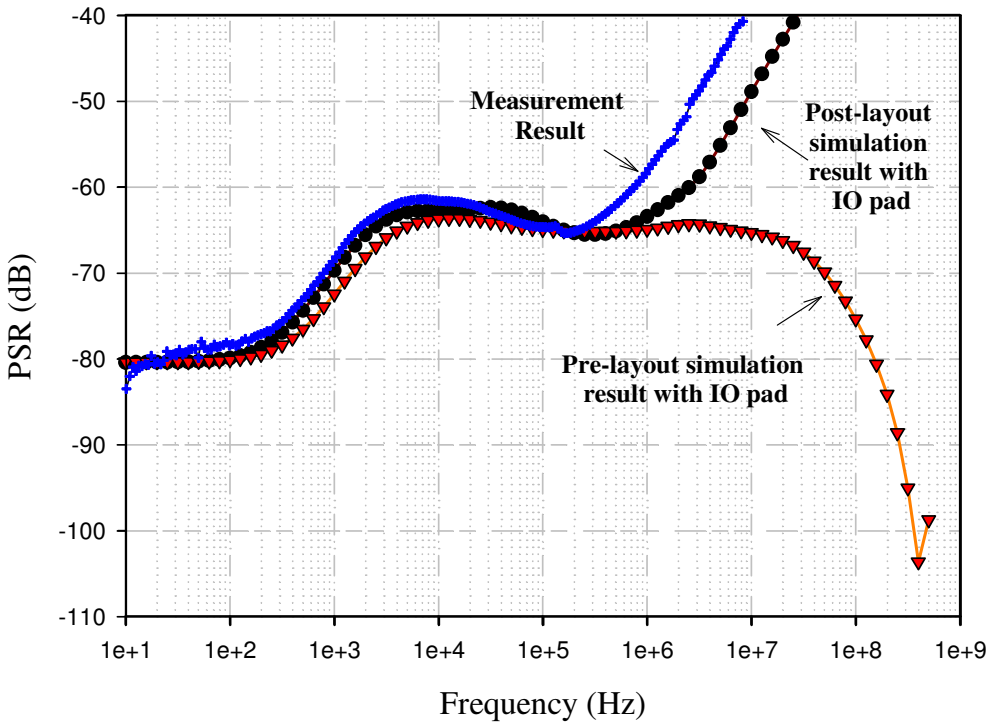


Figure 8.9 Measured, post-layout and pre-layout simulated PSR performance comparison

Figure 8.9 shows the PSR of the entire regulator (pre-regulator plus Brokaw's voltage regulator core), which was measured using network analyzer HP 4395A and active probe HP 41800A. The figure compared the measured PSR result with the post-layout and pre-layout simulation results. As discussed in Section 8.2.2, due to the existence of the parasitics in the output ESD pad to the Vdd power line in the die, it causes the degradation of PSR at high frequencies. The pre-layout simulation result with IO pad does not see the parasitic capacitors caused by the metal routing in the ESD power ring layout, hence showing the broadband PSR curve as analysed in the Section 3.5.2. In the post-layout simulation result with IO pad where the parasitic in the IO pad exists, the PSR performance degrades at about 1M Hz. With this, the ESD pad with minimum decoupling parasitic capacitance to the supply rail is required practically in order to measure high frequency PSR performance.

Nevertheless, the regulator still achieves less than −40dB PSR at 10MHz. Thus the low-power, low-noise and broadband high PSR performance objectives are met. It will be useful for monolithic micropower sensor applications. Figure 8.10 shows the measured PSR

performance for different loading conditions for the proposed low noise regulator. The measured PSR is −79.1dB at 10Hz, −55.3dB at 1MHz and −41.6dB at 10MHz with a full-load output current of 2mA. This suggests that the proposed sandwich capacitor based pre-regulator offers very good wideband PSR while consuming minute quiescent current.

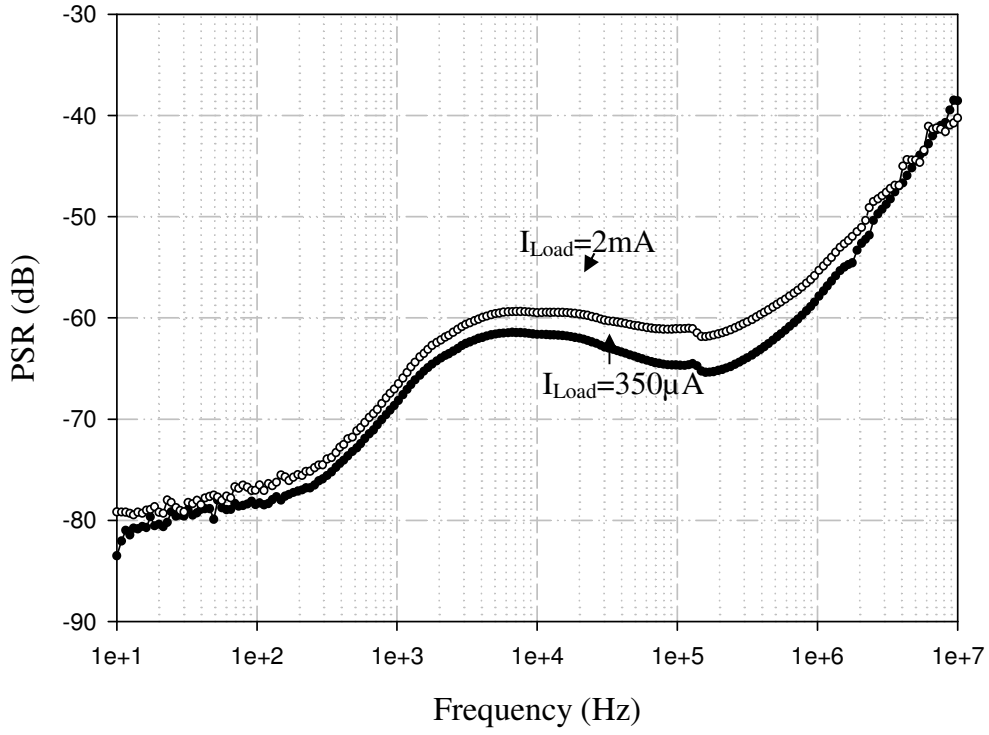


Figure 8.10 Measured PSR with different output loading currents

8.3.3. Comparisons with Other Prior-Art Work

Table 8-II summarizes the performance comparison with the prior-art works. The proposed work has demonstrated comparable results in ultra-low power design. The experimental results have confirmed that the proposed design provides good broadband PSR performance metric while consuming ultra-low quiescent current. The regulator in CMOS process has achieved low output noise by adding the pseudo-resistor based low-pass filter at the gate of the source follower. The proposed structure is simple and occupies not significant silicon area for integrated solution; hence it is very useful in micropower sensor applications.

Table 8-II Performance comparison of the prior-art works

Parameter		*[89] Year 2007*	*[90] Year 2008*	*[91] Year 2009*	*[92] Year 2010*	***This work***
Process		0.6µm CMOS	0.25µm BiCMOS	0.35µm CMOS	0.13µm CMOS	**0.18µm CMOS**
Supply Voltage (V)		>1.8	1.2-2.75	1.6	0.95-1.5	**1.5-1.8**
Quiescent Current (µA)		70	7.6	70**	45	**1.28**
Vout (V)		1.2	1	1.2	0.6-1	**0.992 ***
Iout,max (mA)		5	1	10	2	**2**
Noise (nV/√Hz)	@ 1kHz	NA	NA	NA	NA	**80.1**
	@ 100kHz			NA		**14.2**
Integrated Output Noise (µVrms)		NA	1365 (1Hz-100kHz)	NA	NA	**13.88** (10Hz-100kHz)
PSR (dB)	@ 1MHz	−40	NA	-25	−55	**−55.3**
	@ 10MHz	−27	NA	-22.7	−56	**−41.6**
Line Regulation		NA	2.71 mV/V	0.25 mV/V	0.15-0.44 %	**0.297 %/V**
Load Regulation (mV/mA)		34.2	1.64	0.32	< 0.5	**20.5**
Chip Area (mm^2)		NA	0.18	0.066	0.025	**0.095**

*Measured value is based on a mean of 8 samples **At full load, 10mA

8.4. Low-offset, Small-Area, Reduced Ripple Instrumentation Amplifier Results and Discussions

In this section, the analytical simulation and discussion on the input-referred offset performance for the proposed chopper-stabilized INS-based DDA with CSR is given. This is followed by the experimental results of the fabricated chopper-stabilized instrumentation amplifiers as well as the comparison with recently published works.

8.4.1. Statistical Simulation Results

A Monte Carlo Analysis (MCA) was run with 50 samples on the proposed continuous-time INS chopper DDA with CSR in Chapter 5 under the mismatch of critical

transistor pairs. The MCA with 1–σ mismatch of M_1–M_4, CS1–CS2, CS1a–CS2a, CS3–CS4, CS3a–CS4a, M_{11}–M_{12}, M_{11a}–M_{12a} and the INS switches is conducted with defined correlation between the matching pairs (M_1, M_3), (M_2, M_4), (CS3, CS3a), (CS4, CS4a) and other matching pairs as discussed in Section 0 at the chopping frequency f_{ch}=10kHz. The 1–σ mismatch refers to the standard deviations of process variation for parameters which include V_{th}, β and so forth from the device characterization report. Figure 8.11 shows a statistical input-referred offset of 1.50μV (mean + standard deviation). It confirms that the pair matching layout reduces the overall circuit's DC offset because of the selective grouping of pairs among the devices on the basis of mismatch sensitivity.

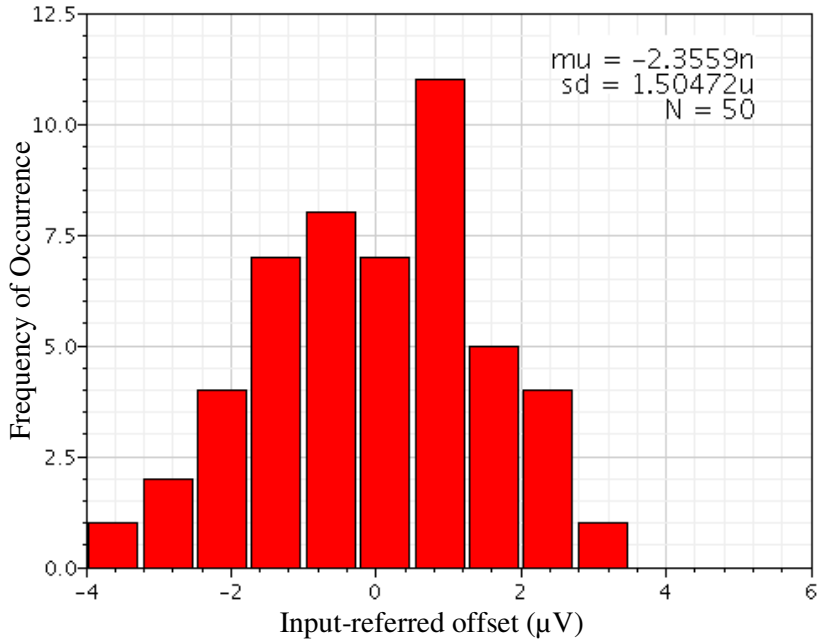
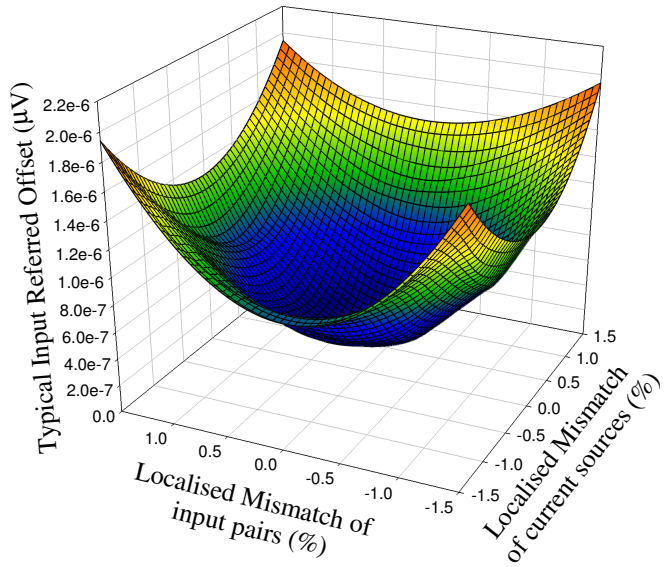


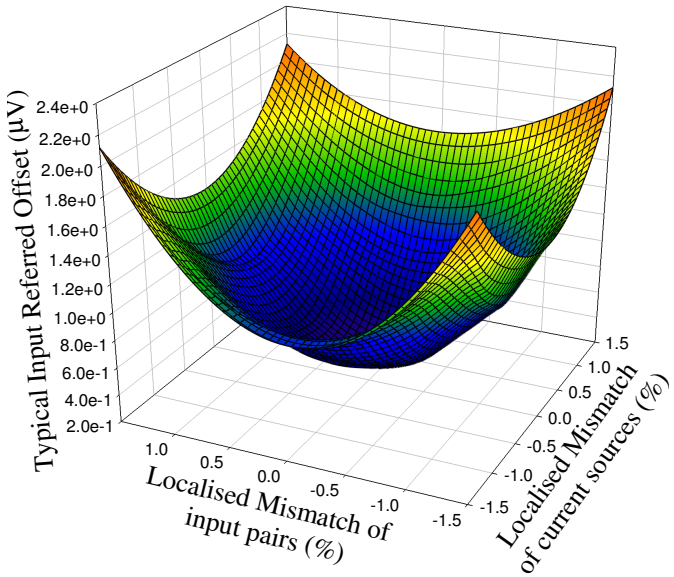
Figure 8.11 Monte Carlo Analysis on the input-referred offset with defining correlation value between the pair matching pairs for proposed DDA3.

In order to examine the input offset variations from localised mismatch under different cases of group mismatch, the critical transistors, M_1–M_4., CS3–CS4, CS3a–CS4a in the input stage are considered in the Monte-Carlo simulation study. To evaluate the realistic device mismatch, consider the typical current mismatch errors. For a simple CMOS current mirror layout, the typical current mismatch error is few %. However, with careful layout in

current mirror pair, with reasonable size, splitting devices, long channel length and dedicated layout technique, the typical mismatch error will range from about 6-bit to 8-bit, which translates to a worst case of 0.5%. Hence, the assumption of variation from 0.5% to 1.5% as a lumped error for current sources or input pairs in large sizes will be realistic.



(a)



(b)

Figure 8.12 Simulated typical input-referred offset with group mismatch (a) +4% (b) +8% whilst varying mismatch percentages between devices in the localized input pair and the localized current source pair.

In the simulation, the mismatch of aspect ratio is treated as a lumped parameter for the non-ideal effects in a transistor pair, where intentional W/L mismatches are applied for the critical matching pairs (input pair transistors, M_1–M_4, and current source pairs, CS3–CS4 & CS3a–CS4a). A group mismatch of +4% or +8%, is applied between (M_1, M_3) and (M_2, M_4) as well as (CS3, CS3a) and (CS4, CS4a); whilst the localized mismatches of ±0.5%, ±1% or ±1.5% are applied for the local matching pairs M_1 & M_3, M_2 & M_4, CS3 & CS3a as well as CS4 & CS4a. With these settings, a series of Monte Carlo simulations are conducted by manually varying the W/L mismatch in each mismatch combination for current sources and differential pairs from the above mismatch criteria in conjunction with 1–σ variation for parameters in all small-size INS switches in the choppers of the DDA. The random statistical variables include the key parameters, V_{th} (±45mV) and β (±7.5%) according to the foundry manual.

The simulated typical input offset voltage with a group mismatch of (a) +4% (b) +8% under varying localized mismatches (±0.5%, ±1%, ±1.5%) are plotted in Figure 8.12. The simulation results reveal that the input offset voltage is closely related to localised mismatch effects of M_1 & M_3, M_2 & M_4, CS3 & CS4 and CS3a & CS4a whereas it is almost insensitive to the group variation as shown in Figure 8.12(a) and (b). With a localized mismatch of ±1.5% for both the input transistors and current sources group pairs, the input-referred offset is about 2μV, which is considered low. The simulation results confirm the technical merits of pair matching layout strategy as discussed previously and allow reasonable prediction of input offset based on different degree of mismatches on critical device pairs.

8.4.2. Fabrication

Experimental circuits for different INS chopper-stabilized DDAs were designed and fabricated using GLOBALFOUNDRIES 0.18μm triple-well CMOS process technology. The

micrograph of the chip is shown in Figure 8.13. It was packaged in a 28-pin DIP package. The top part of the die photo contains the shared clock generator to the 3 types of the INS-based DDAs. This includes the proposed INS chopper-stabilized differential difference amplifier (DDA3) with CSR circuit. The balancing resistor R_b mentioned in Section 4.3 is implemented off-chip for the impedance matching between 2 input ports.

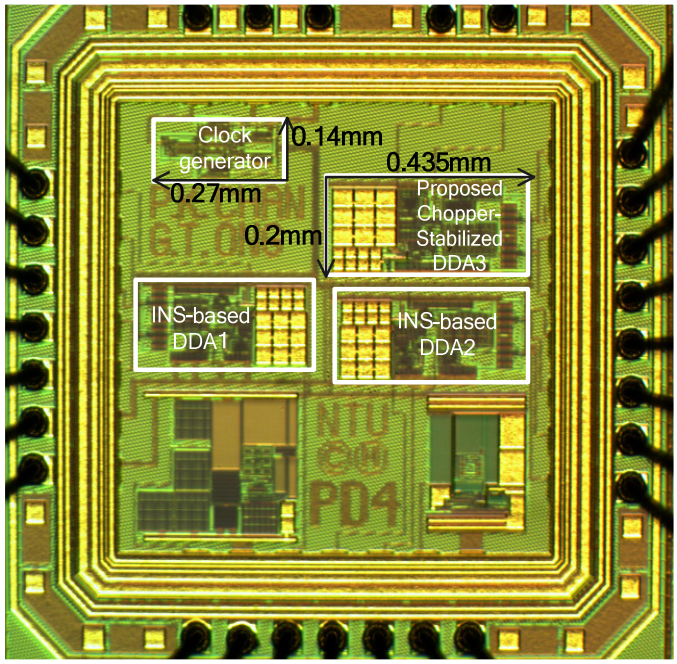


Figure 8.13 Micrograph of three INS chopper DDAs with shared clock.

Table 8-III Comparison of the measured input-referred offset for INS chopper DDAs

Parameters	DDA1	DDA2	DDA3
Layout Technique	Common-centroid in Averaging	Pair Matching	Pair Matching
With Current Source Replica	No	No	Yes
Supply Current	14.5μA	14.5μA	22μA
|Max/Min Input Offset|	12.6μV	6.75μV	3μV
Input Offset (Mean+Standard Deviation)	9.84μV	4.46μV	1.78μV
Silicon Area	0.103mm^2	0.108mm^2	0.125mm^2

To evaluate the offset effect in each INS chopper DDA, different input transistors layout techniques are implemented. DDA1 and DDA2 are identical INS chopper DDAs without CSR. DDA1 employs the common-centroid in averaging layout as shown in Figure 5.4(a) for the four input transistors whereas DDA2 employs the pair matching layout technique in Figure 5.4(b) for the input transistor pairs. Last is DDA3 which is an INS chopper DDA with CSR whilst employing the pair matching layout technique. Each DDA has its own biasing circuit. The silicon area occupied by each DDA design is summarized in Table 8-III, taking into account the silicon area contributed by the biasing circuit and clock generator.

8.4.3. Input-Referred Offset Measurement

Table 8-III compiles the experimentally observed input-referred offset for eight samples of the INS-based DDAs, compared at 10kHz chopping frequency. The key aspect for reducing the input offset and minimizing the output ripple in chopping DDA is the matching of selective critical transistors in the first stage design. Its symmetry and balance geometry are also crucial in enhancing the $CMRR_d$ of the DDA to obtain low input offset for the chopper-stabilized DDA design.

Extra care is taken on the layout of the input choppers, differential signals and clocking paths as well as the noise shielding of the input signals. Table 8-III shows that the measured input-referred offset for INS chopper DDA2 is smaller than that of INS chopper DDA1. This can be explained by the pair matching layout providing larger tolerance than the common-centroid in averaging layout in the context mentioned in Section 5.4 implemented off-chip for the impedance matching between 2 input ports.

By adding the CSR stage in the DDA3 design, the mismatch of the current sources and cascode current mirror are further improved. This validates that the proposed design can

achieve the objectives of low input offset using the proposed continuous-time INS chopper in conjunction with the CSR circuitry that facilitates the full pair matching layout scheme for critical transistor pairs in DDA.

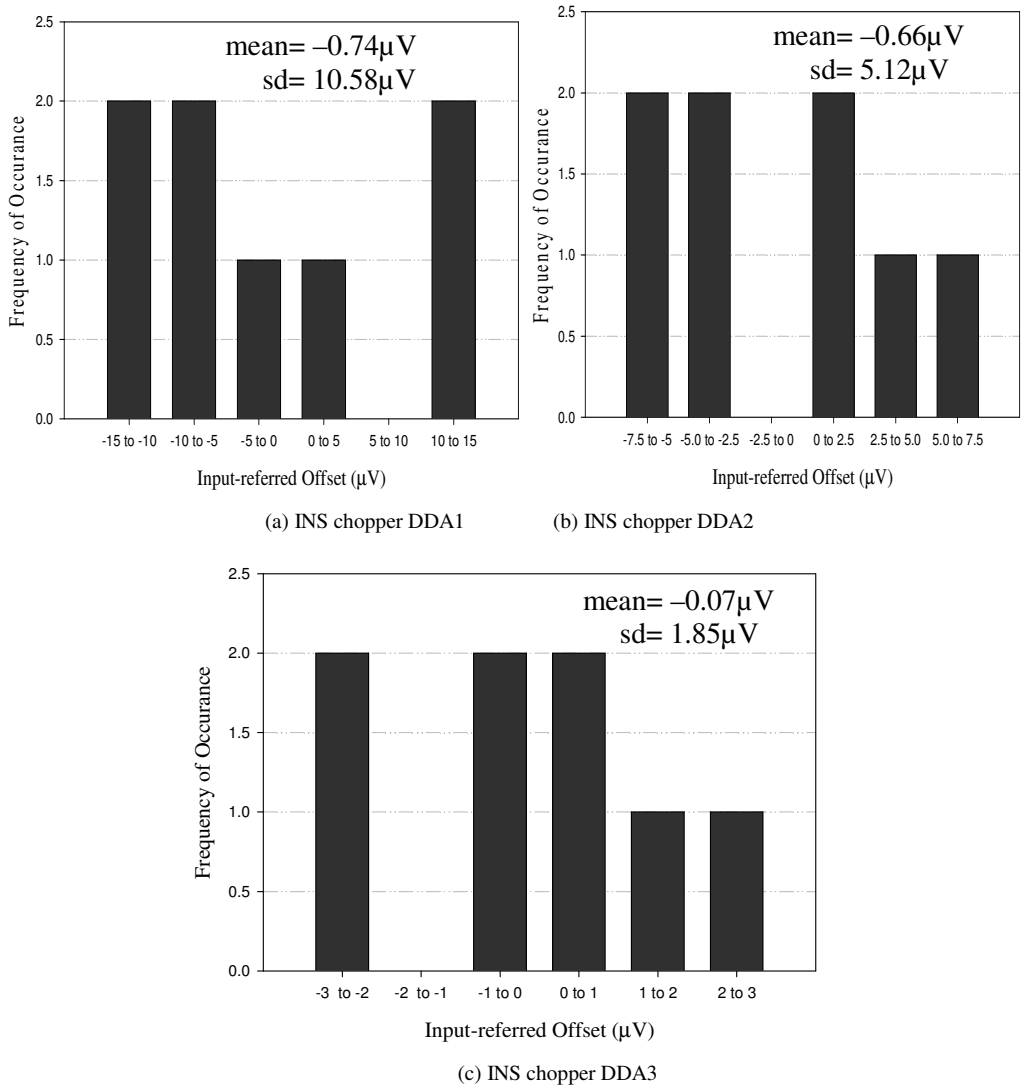


Figure 8.14 Measured input offset distribution of INS chopper DDAs.

Figure 8.14 shows the measured offset voltage distribution of 3 types of chopper DDAs for eight chips. Table 8-IV summarizes the measured mean and standard deviations of the input offset for each DDA in 8 samples, with chopper off.

Table 8-IV Measured input offset with chopper off for the three DDAs

	DDA1	DDA2	DDA3
Mean Input offset (chopper off)	-198.6μV	-58.2μV	15.5μV
Standard Deviation Input offset (chopper off)	998.9μV	534μV	353.4μV

Conventionally, the input-referred offset of a transistors pair is related to the standard distribution of the threshold mismatch: $\sigma(VT) \approx \sqrt{A_{VT}^2/WL}$, where A_{VT} is a technology-dependent constant; W and L are the gate width and length respectively. Hence, increasing the size of the critical transistors will enhance the matching characteristics. Besides, the input-referred offset in the chopper stabilized DDA is also contributed by the spikes generated during the chopping activities and unbalanced input ports matching characteristic. Lowering the chopping frequency will reduce the input residual offset, but this comes with a trade-off of higher output ripple caused by the modulated input offset. In this work, CSR is introduced incorporating pair matching technique for all critical transistors to enhance port matching characteristics, hence improving the input-referred offset performance.

8.4.4. Output Ripple Measurement

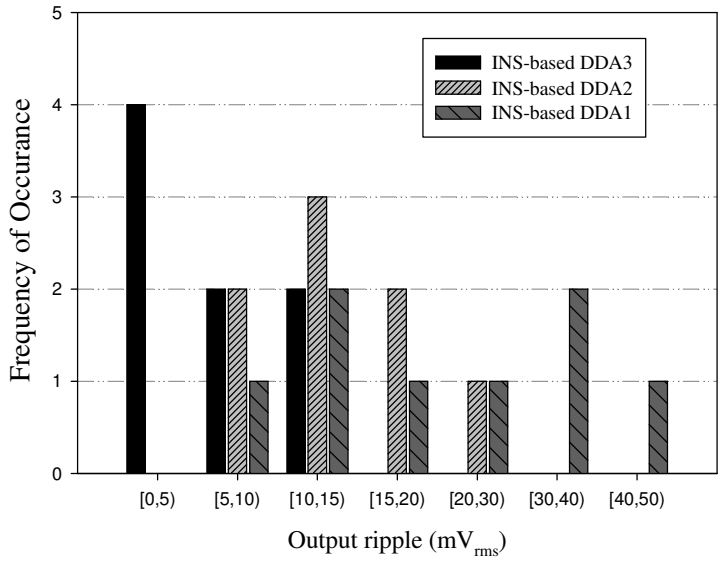


Figure 8.15 Measured output ripples from the three INS chopper DDAs.

Figure 8.15 compares the measured output ripple voltage of DDA3 with those of the DDA1 and DDA2 without CSR circuit. It confirms that the measured output ripple of DDA2 is smaller than DDA1. The experimental results also demonstrate that the pair matching layout technique better tolerates the mismatch of the input transistors. In comparison, the proposed DDA3 design achieves more than 3 times better ripple reduction than the DDA1 design using pair matching layout and additional current source replica circuit. The measured output ripple at 10kHz of DDA3 can achieve 1.15mV$_{rms}$. More importantly, this enables the output filter design in the DDA3 itself to be relaxed. Of particular interest for sensor applications, the DDA3 can be operated in absence of output low-pass filter because the use of sensor bandwidth limiting filter will further suppress the output ripple arising from DDA3. This suggests the economical application of DDA3. If the ADC is made to sample at the minimum ripple time of the output, the filter may not be needed. The hardware and power consumption is not necessarily increased from sensor system level design perspective.

8.4.5. AC Frequency Response Measurement

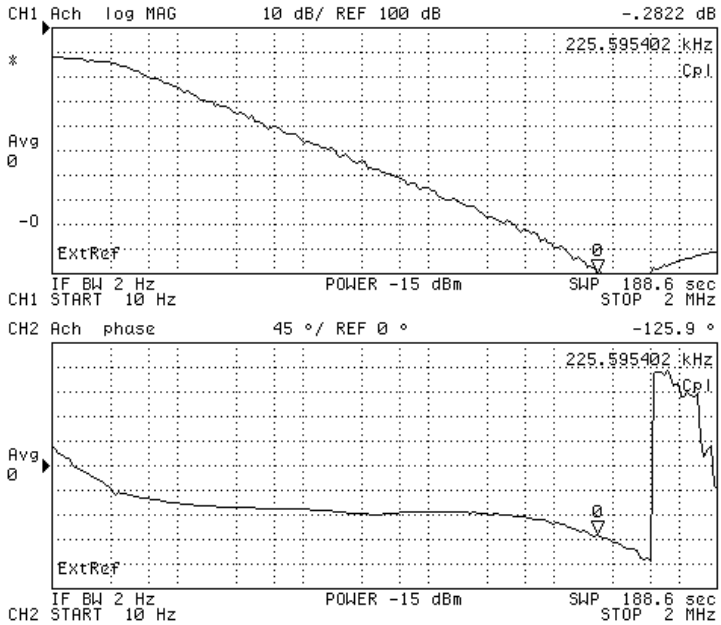


Figure 8.16 Measured open-loop frequency response and phase response of DDA3.

The proposed INS chopper amplifier DDA3 was verified using the network analyzer (HP 4395A) and the active probe (HP 41800A) with the measurement results given and discussed next. Figure 8.16 shows the Bode plot for the measured open-loop gain and phase response from the proposed INS chopper DDA3. For a measured total current of 22µA, the core DDA3 consumes 15.5µA whereas the biasing circuit consumes 6.5µA in a 1.8V power supply.

At 10Hz, it achieves 89dB and phase margin of 54.1º with a unity gain bandwidth of 225kHz at the output loading of 220kΩ//56pF. The folded telescopic cascode topology has demonstrated that very high gain is achieved with the use of Native transistors whilst saving additional gain stage. The measured CMRR is more than 120dB. Meanwhile, Figure 8.17 shows the frequency response of the closed-loop gain of the instrumentation amplifier in which the dc closed-loop gain is designed to be 100 with the off-chip resistors R_1=990kΩ, R_2=10kΩ, R_b≈10kΩ in the measurement setup. The common-mode input range is 1.4V–0.2V. Hence with a closed-loop gain of 100, for an output swing of close to 1.8V, the small-signal input range is ≈ ±9mV.

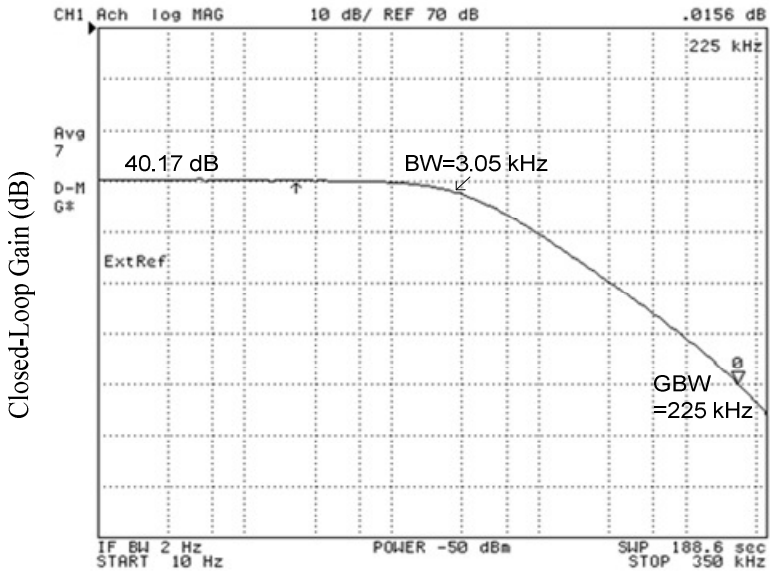


Figure 8.17 Measured closed-loop frequency response of DDA3 with dc gain designed at 100.

8.4.6. Input-Referred Noise Measurement

The measured input-referred noise spectrum for both without and with chopping operation at chopping frequency, f_{ch}=10kHz, is illustrated in Figure 8.18. It shows an input-referred noise spectral density of 62nV/√Hz at 10Hz where the 1/f noise has been removed compared to the noise density curve when the choppers are off. The spikes appear in the noise spectrum at the frequencies 50Hz, 100Hz, 150Hz and the rest of the harmonics components. These power line harmonics are generated from the power source. The power line harmonics can be reduced by careful layout, shielding and grounding in the PCB design.

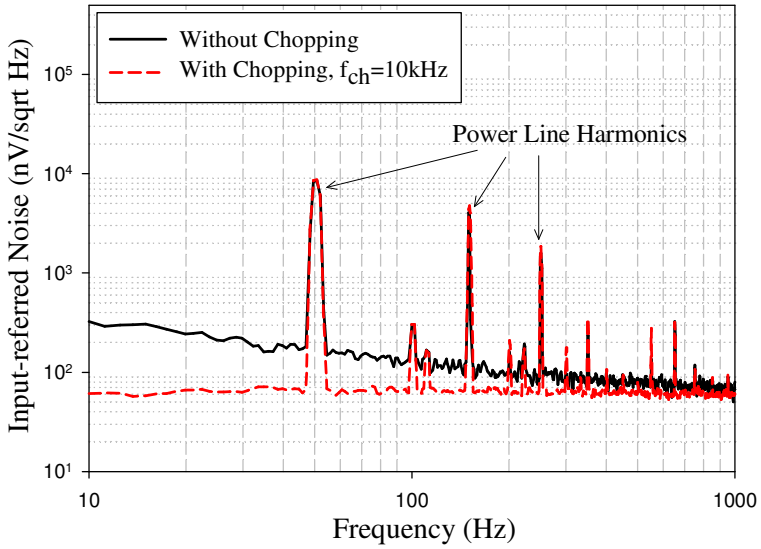


Figure 8.18 Measured input-referred noise spectral density from a closed-loop gain of 40.17dB for both with and without chopping in DDA3.

8.4.7. Comparisons with Other Prior-Art Works

In short, the experimental results confirm the performance for the proposed low noise and low offset design. The measured results of the proposed INS chopper-stabilized differential difference amplifier with current source replica (DDA3) are summarized and compared with other published current feedback instrumentation amplifiers in Table 8-V. It has shown that the proposed simple instrumentation circuit architecture and circuit techniques have achieved comparable input offset voltage, good power-bandwidth efficiency and

significantly smaller silicon area, demonstrating the effectiveness of the structure for small-signal sensor applications.

Table 8-V Performance comparison with recently published chopper-stabilized IAs

Parameters	[5] Year 2008	[39] Year 2009	[35] Year 2010	[34] Year 2010	DDA3
CMOS Process Technology	0.6µm	0.7µm	0.5µm	0.7µm	0.18µm
Supply Voltage	3V	5V	3V–5.5V	5V	1.8V
Supply Current	150µA	230µA	1.7mA	143µA	22µA
Input Offset Voltage	<20µV	<5µV	2.8µV	<2µV	<3µV
Input Noise Spectral Density	62nV/√Hz	15nV/√Hz	27nV/√Hz	21nV/√Hz	62nV/√Hz
CMRR	NA	>120 dB	140dB	137dB @DC	120dB @10Hz
Closed-loop Gain @ DC	20dB	NA	60dB	40dB	40.17dB
Unity Gain Bandwidth, GBW	1.3MHz	800kHz	800kHz	900kHz	225kHz
Silicon Area	0.24mm^2	4.8mm^2	2.5mm^2	1.8mm^2	0.125mm^2
GBW/Isupply (kHz/µA)	8.67	3.47	0.47	6.3	10.23
NEF	25.89	8.8	43.5	9.6	11.18

In the proposed DDA design, the main goal is to achieve low power consumption. However, low noise performance is always traded off with higher current consumption. Hence, it is necessary to have balance between power and noise performance. One of the figure of merits used in comparison is the noise efficiency factor (NEF) [93], which combines performance metrics from noise, GBW and current consumption of the design. The noise efficiency factor (NEF) is given as below:

$$NEF = V_{rms,in}\sqrt{\frac{2I_{tot}}{\pi U_T \cdot 4kT \cdot BW}} \quad (8.2)$$

where $V_{rms,in}$= total equivalent input-referred noise

BW=Bandwidth of system in Hz

I_{tot}= Total current consumed

U_T=thermal voltage

NEF is normally used to measure or justify the efficiency of the noise performance in the circuit. The figure achieved is comparable to others' designs, as observed in Table 8-V. Besides, a figure of merit for bandwidth and current efficiency, which is defined as GBW/Isupply, is also compared in Table 8-V. The proposed work has achieved the highest GBW and current consumption efficiency when compared to other state-of-the-art results.

Table 8-VI Comparison with reported small-area switched-based IAs

Reference	Techniques	Process	Current Consumed	Silicon Area	Input offset
[Yen 2004] [94]	Switched-capacitor, 3 op-amp resistive-feedback	0.5µm CMOS	61µA	0.2mm^2	160µV
[Yazicioglu 2007] [95]	Chopping, indirect current feedback IA with chopping spike filter	0.5µm CMOS	14.3µA	0.69mm^2*	NA
[Chan 2008] [5]	Chopping DDA with resistive feedback	0.6µm CMOS	150µA	0.24mm^2	<20µV
[Fan 2011] [15]	Chopping, capacitive-feedback IA	65nm CMOS	1.8µA	0.1mm^2	1µV
[Michel 2012] [96]	Chopping , direct current feedback IA with automatic resistor matching	0.13µm CMOS	20 µA	0.168 mm^2**	<5 µV
DDA3	INS Chopping, DDA with CSR, resistive-feedback	0.18µm CMOS	22µA	0.125mm^2	< 3µV

* Estimated area for instrumentation amplifier and bias circuit based on the die diagram in the paper [95].
** Estimated area for IA core only based on the die diagram [96].

Table 8-VI summarizes other reported small-area instrumentation amplifiers with the proposed work. It can be seen that the proposed work gives a reasonably good performance

metrics in terms of power, area and offset. As discussed in Chapter 2, this work focuses on the resistive feedback indirect feedback instrumentation amplifier architectures which need to drive resistors at the output stage. Although the resistive-based amplifier architectures may suffer from relatively larger power consumption than their capacitive-based counterparts [15], they display relatively less dependence on capacitive parasitics whilst permitting ease of external gain programming function. More importantly, they are robust with good immunity to the environmental effects such as Electromagnetic Interference (EMI).

8.5. Sensory System Architecture

The overall chopping IA is suitable for sensing applications such as in strain gauge measurements. Placing all the blocks together with an emulated strain-gauge sensor, the measurement results of the chopping instrumentation amplifier system are obtained. In this section, the specifications of the strain gauge pressure transducer are briefly described. This is then followed by the measurement results as well as comparison with other published works.

8.5.1. Strain Gauge Pressure Transducer Specifications

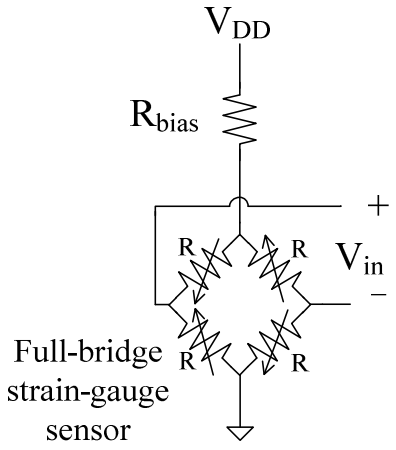


Figure 8.19 Strain-gauge based sensor in Wheatstone bridge configuration

Strain is a measure of deformation, and can be represented by displacement of a point relative to a reference length. The strain gauge is used to measure strain caused by forces, pressures, moments, heat, structural changes of the material and the like [97]. The most commonly used pressure sensor is the piezoresistive pressure sensor which makes use micro-machined silicon diaphragm with piezoresistive strain gauge diffused on it. It requires comparatively smaller area and is easy to read out. Its resistance changes range from 10kΩ to 200kΩ. The piezoresistive strain gauge can be connected in full-bridge of Wheatstone bridge configuration as shown in Figure 8.19.

The output of the Wheatstone bridge sensor can be represented by the equation below:

$$V_{in} = V_{DD} \frac{R}{(R_{bias}+R)} \left(\frac{\partial R}{R}\right) \quad (8.3)$$

where ∂R is the change in resistance caused by the mechanical strain. Resistor, R_{bias} is used to limit the power consumed in the strain gauge which will set the input common-mode voltage of the IA at lower signal magnitude.

Table 8-VII Example of a full- bridge piezoresistive strain gauge based pressure sensor [98]

Parameter	Value
Bridge Resistance	12kΩ
Operating Temperature	-40-125ºC
Temp. Coeff. (@ 25ºC)	$1.5x10^{-3}$/ºC
Operating Pressure	0 - 200kPa
Sensitivity	128µV/VkPa

In the test setup, the inputs of proposed instrumentation amplifier are connected to external Wheatstone bridge resistors. The piezoresistive strain gauge characteristic were emulated in Wheatstone bridge configuration using variable resistors based on a typical piezoresistive strain gauge pressure sensor specification [98] as shown in Table 8-VII.

With R_{bias} set to be 6kΩ and a supply V_{DD} of 1.8V, the bias voltage supply to the Wheatstone bridge is 1.2V. Hence, the common-mode voltage at the inputs of the instrumentation amplifier is 0.6V. The sensitivity of the emulated bridge pressure sensor is 153.6μV/kPa with 1.2V bias voltage for the strain gauge. The bridge output is zero at pressure of 100kPa assuming the strain-gauge bridge is compensated for zero offset by calibration of the resistors parallel to the bridge. Meanwhile, the maximum input signal is ±8.8mV, for a maximum measured pressure of ±57.5kPa. The IA is configured for a gain of 100 for 1.76V peak-to-peak signal at the output.

Table 8-VIII Emulated half- bridge strain gauge specification in the test setup

Parameter	Value
Bridge Resistance	12kΩ
Rbias	6kΩ
V_{DD}	1.8V
Common-mode Voltage	0.6V

The noise at the IA's inputs contributed by the strain gauge resistors and R_{bias} is:

$$v_{n,strain\_gauge} = \sqrt{4kTR\Delta f} \tag{8.4}$$

where Δf is the signal bandwidth. For a 12kΩ bridge resistor, this corresponds to 14.1nV/√Hz input noise voltage density, which will contribute to the output noise. This will be discussed in the next section. The strain gauge resistors and R_{bias} do not contribute to the noise at the output of the IA since their noise appears as common-mode signal and will be rejected by the IA. Hence, it can be concluded that the strain gauge is not the limiting factor in SNR.

8.5.2. Measurement Results

The overall system block diagram is shown in the Figure 8.20. The system consists of an INS-based differential-difference instrumentation amplifier, a high PSR op-ampless voltage regulator, a clock generator as well as an RC passive low pass filter with 2kHz cut-off frequency at the IA output. In a standard laboratory environment, the system was tested with the emulated strain-gauge pressure sensor with specification as discussed in the previous section.

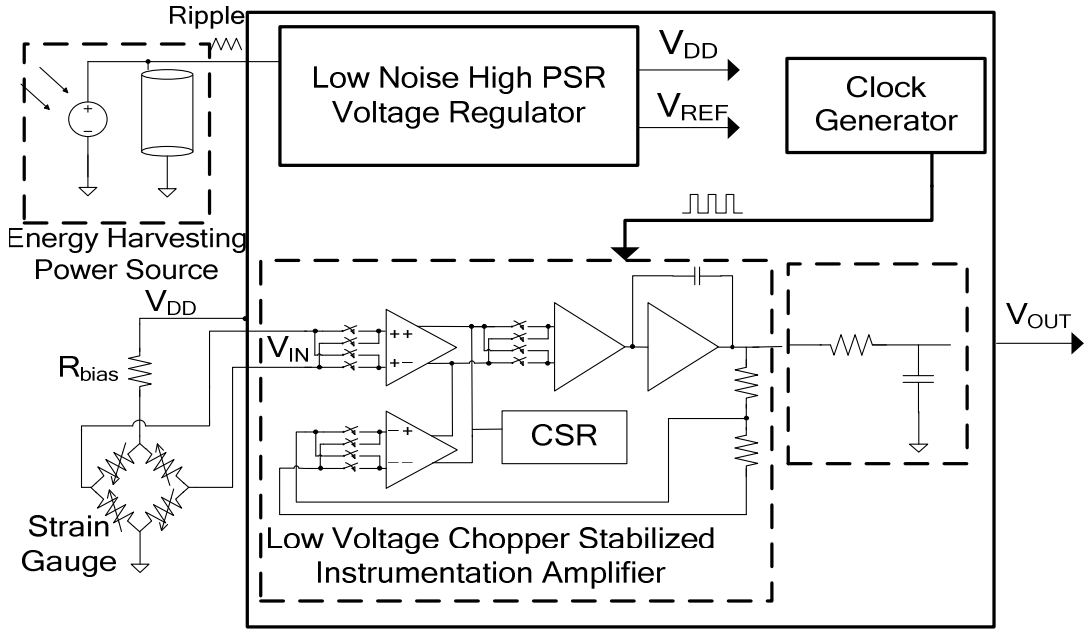


Figure 8.20 Proposed low power low-noise analog front-end block diagram for strain gauge based sensor in environmental monitoring application

8.5.2.1. Power supply rejection

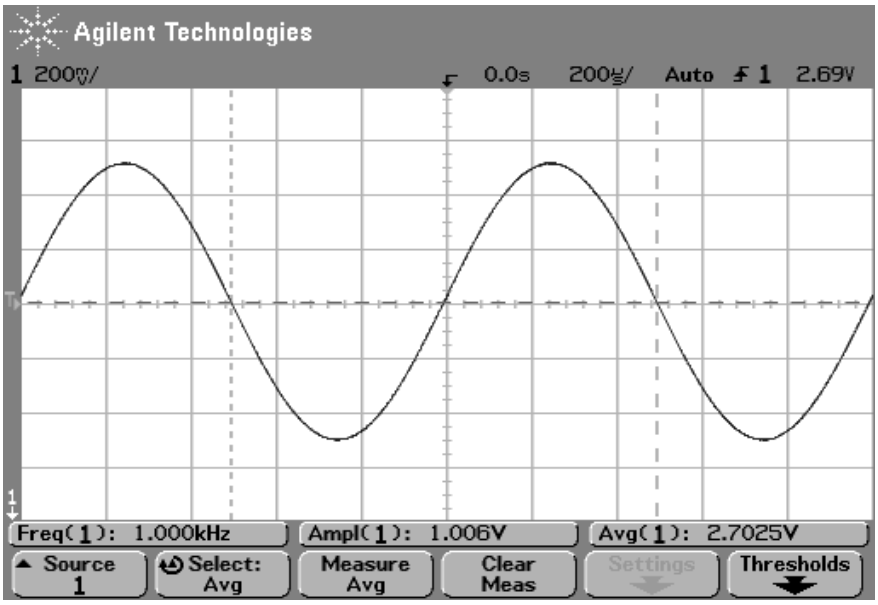


Figure 8.21 Large input ripple of 1kHz injected to the regulator input

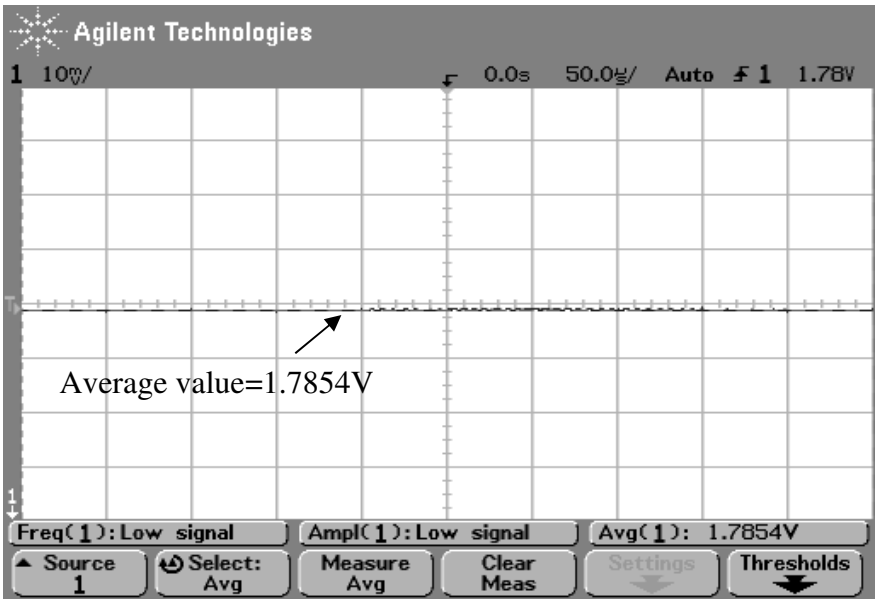


Figure 8.22 Output of the voltage regulator connected to the input of the instrumentation amplifier

Powered at a supply of 2.7V to the voltage regulator, a regulated supply of ≈1.8V is supplied to the noise sensitive block i.e. instrumentation amplifier block. As discussed in Chapter 3, the proposed voltage regulator can reject noise from supply source. In the test, a

large sine wave signal is injected to the supply of the voltage regulator and the output of the voltage regulator which serves as the regulated supply of the IA is observed.

The measured PSR shown in Figure 8.3 in the previous section gives 1kHz PSR performance of -76dB showing that any 1kHz ripple from supply line will be attenuated by a factor of 6309. Figure 8.21 shows a large sine signal of 1kHz with peak-to-peak value of 1V being injected to the supply of voltage regulator. As observed in Figure 8.22, the output of the voltage regulator with this large supply ripple injection is almost DC with an average value of 1.785V and a very small noise amplitude < 200μV, showing that the ripple is suppressed effectively by the high PSR regulator.

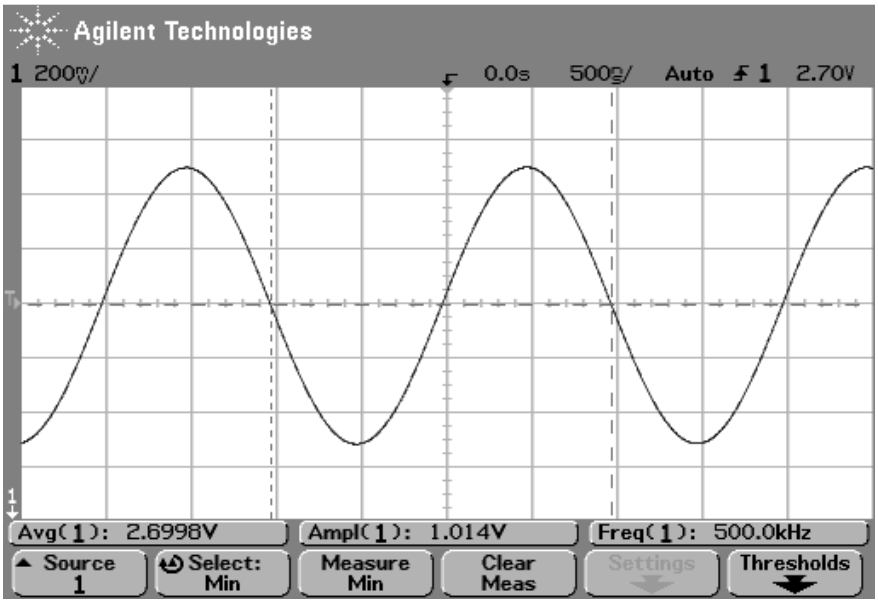


Figure 8.23 Large input ripple of 500kHz injected to the regulator input

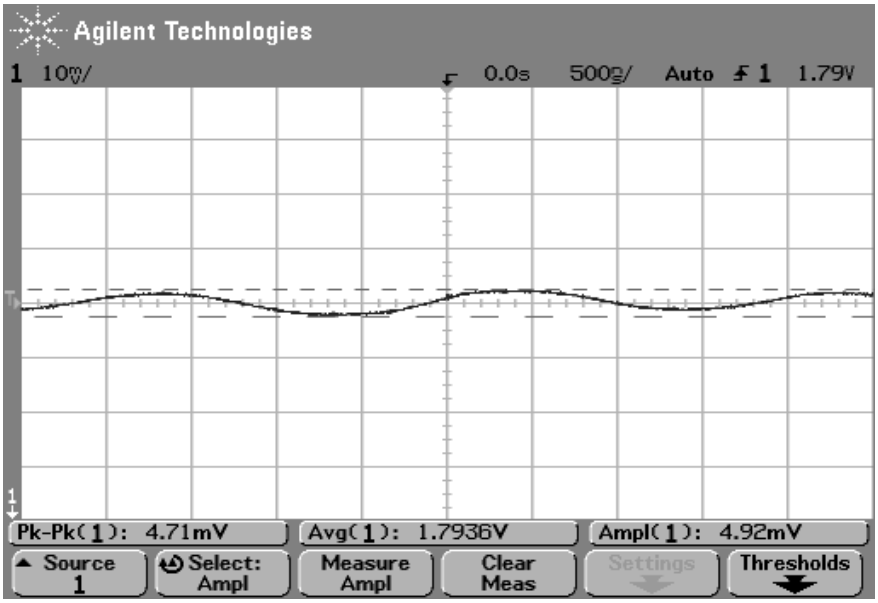


Figure 8.24 Output of the voltage regulator connected to the input of the instrumentation amplifier

The ripple frequency is further increased to examine the effectiveness of the supply ripple rejection at high frequency, i.e. 500kHz as shown in Figure 8.23. The 500kHz ripple of 1V peak-to-peak was suppressed to a very small signal of 4.92mV peak-to-peak in Figure 8.24, showing a PSRR of -46.2dB at 500kHz which further verifies the supply noise rejection capability of the system.

8.5.2.2. Output Noise Measurement

The output noise spectral density of the overall system with chopper stabilization is shown in Figure 8.25. From the figure, the integrated output noise from 10Hz to 2kHz is 376.2μVrms. Hence, the output SNR for an output signal 1.76V peak-to-peak (0.622Vrms) is 64.4dB.

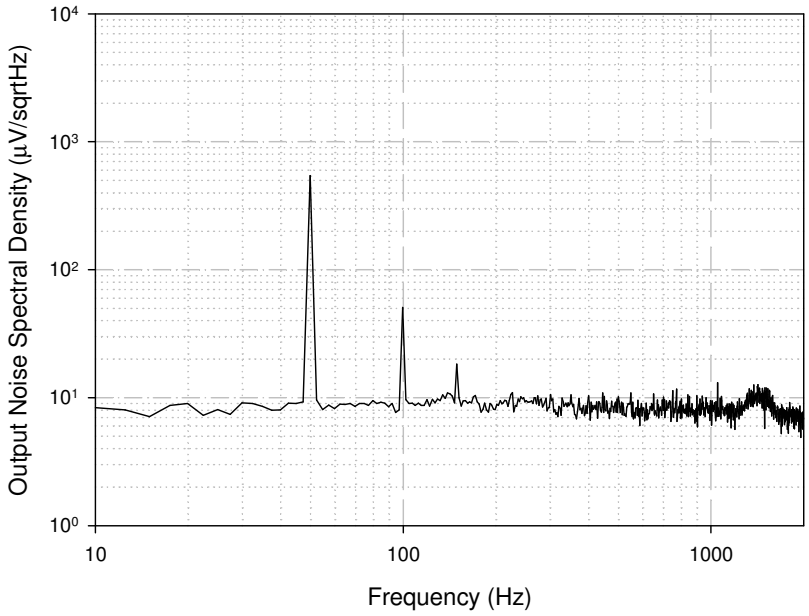


Figure 8.25 Measured output noise spectral density

As the integrated output noise is 376.2µVrms with an IA gain of 100, the input-referred noise over 10Hz to 2kHz is 3.76µVrms. Since noise sources have amplitudes vary randomly with time, the amplitude is estimated by 6 times of the Vrms value. In this case, the noise amplitude will be 22.56µV peak-to-peak. In this system, the minimum resolution of the strain gauge measurement is 25µV which is equal to 162Pa with a sensitivity of 153.6µV/kPa.

8.5.2.3. DC Measurement

The DC performance at the output of the system was tested based on the change in the resistance value of the emulated strain-gauge induced input voltage to the instrumentation amplifier as shown in Figure 8.26.

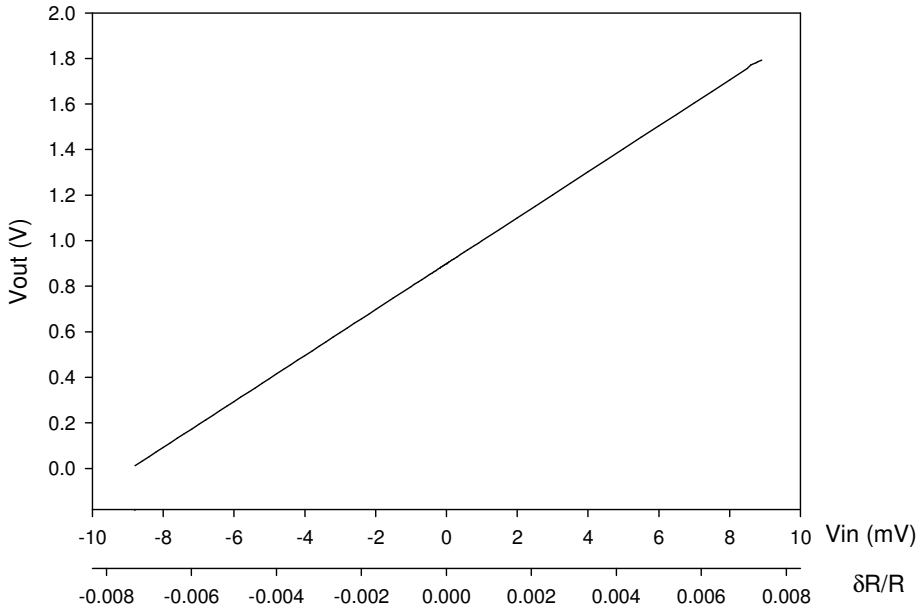


Figure 8.26 DC performance at the system output with respect to the change of input signal caused by the change in resistance value of the emulated strain-gauge

8.5.2.4. Power Consumption

The overall system consumes 127.65µA. where the emulated strain-gauge biased with 100µA, the high PSR regulator consumes 5.65µA and the proposed IA with the biasing circuit draws 22µA. With a supply of 2.7V, the overall power consumption is 344.66µW.

8.5.3. Comparison with other published works

The performance of the proposed instrumentation amplifier system tested with the emulated strain gauge in Wheatstone-bridge configuration is then compared with other

published analog front-end (AFE) circuit designed for strain gauge or Wheatstone-bridge applications as shown in Table 8-IX.

Table 8-IX Comparison with other published work for strain gauge or Wheatsone-bridge applications

Parameters	[82] Year 1992	[99] Year 1997	[100] Year 2002	[101] Year 2005	[102] Year 2011	This Work
Process Technology	2.0µm CMOS	2.0µm BiCMOS	0.7µm CMOS	0.8µm CMOS	0.7µm CMOS	0.18µm CMOS
Supply Voltage	±5V	4V	3.1V	5V	5V	2.7V
Supply Current to AFE only	3mA	3mA	603µA	10mA	220µA	27.65µA
Supply Current to sensing element	NA	800µA	308µA	NA	NA	100µA
SNR	100dB	60dB	NA	78dB	NA	64.4dB
Bandwidth	20Hz	200-600Hz	2kHz	520Hz	1m –10Hz	2kHz
Amplitude at the Input (Vppk)	50mV	8mV	NA	8mV	80mV	17.6mV
Gain	100	NA	70	640	100	100
Other features	ADC, Calibration, Digital Filter	Voltage Regulator, RF Transmitter	ADC, Oscillator	ADC	ADC	Voltage Regulator

This work is aimed to achieve low power consumption with reduced circuit complexity whilst maintaining good signal-to-noise ratio (SNR) performance with a reasonable broad bandwidth of 2kHz for sensor applications. Although the maximum input range is mainly limited by the lower supply voltage as well as the single-ended configuration in the design. However, it is sufficient for environment monitoring sensor applications where the input signal variations are small.

As a final remark, the proposed IA circuit is able to perform excellent power rejection capability, low-power, small-offset performance without sacrificing the area. This is achieved through (i) the proposed high PSR regulator for supply noise rejection, (ii) the chopper-stabilization technique for low noise performance at low frequency (iii) the chopping DDA

with continuous-time INS chopper for reduced charge-injection effect and hence reduced residual offset, (iv) pair matching layout technique for input transistors as well as the critical current sources in the chopping DDA which incorporating with the proposed CSR circuit for improved $CMRR_d$ performance and smaller offset. These attributes permit the IA system suitable for Wheatstone-bridge sensor applications which demand low-noise, low-offset, small-area and low power consumption.

CHAPTER 9

CONCLUSIONS AND RECOMMENDATIONS

In the demand of low-power, high-sensitive sensory systems, a fully integrated precision amplifier that achieves high performance in signal-to-noise ratio, dc offset, yield of low dc offset, high gain, PSR, flexibility and stability against process, temperature and supply voltage is of paramount importance. In this chapter, conclusions are drawn, and recommendations are made for future work on the chopper stabilized DDA in IA systems.

9.1. Conclusions

This thesis presents the design work and experimental results for a low-offset, small-area micropower chopper-stabilized instrumentation amplifier (IA) dedicated to sensor or sensor array interface circuitry. As a review, the various instrumentation architectures and circuit techniques for low noise and low offset were discussed. The chopper stabilized DDA was chosen for its good input offset characteristics and simplicity for implementation of instrumentation amplifier. This was followed by a review of residual offset reduction methods, as well as ripple-reduction techniques in chopper stabilized IAs.

High power supply rejection (PSR), low noise, micropower regulators are designed as regulated power supply to power the proposed IA. The high PSR regulators are fabricated using GLOBALFOUNDRIES 1.8V/3.3V CMOS 0.18μm process. Even without the use of a decoupling capacitor or an output capacitor, the power supply circuit displays good low-frequency and high-frequency PSR performance metrics while drawing very small quiescent biasinig current. the performance of the regulators is measured, displaying low noise and

broadband high PSR suitable for micropower sensor applications. The performance comparison with prior-art works has demonstrated high efficiency in terms of PSR bandwidth per current. It validates the effectiveness of the proposed feedback-controlled Brokaw circuit architecture. Therefore, it is useful for operation as a robust regulator that sources supply current to the micropower instrumentation amplifier.

The proposed IA system consists of a differential difference amplifier (DDA) a current source replica (CSR) circuitry that facilitates the pair matching layout for all critical pairs in DDA input stage and continuous-time injection-nulling switch (INS) with modified control clock choppers. The common-mode signals and differential common-mode signal in chopper-stabilized DDA are analyzed. The proposed DDA with gate-bulk driven input circuit technique incorporating pair matching layout is proposed. For the DDA, the use of pair matching layout that is not limited to the input transistor pairs, unlike conventional DDAs. Besides, the proposed CSR allows the pair matching layout in critical current sources to reduce output ripple by generating similar level of mismatch offset current, thus nullifying mismatch offset current arising from the input stage of the DDA. Furthermore, the CSR enhances $CMRR_d$ by improving the matching of critical devices, thus minimizing contribution to the input offset. The proposed INS chopper with modified clock control allows for balance based matching layout, resulting in reduction of input offset. This allows low offset and reduced ripple which will be useful for low-noise micropower instrumentation amplifier design. As the IC prototype was intended for mixed-signal circuit and system design, the digital blocks are discussed in detail, with the control waveforms illustrated. The layout considerations involved is also discussed.

The proposed IA was fabricated in GLOBALFOUNDRIES 1.8V/3.3V CMOS 0.18µm process. It shows good performance when measured for input-referred offset, output

ripple, AC frequency response and input-referred noise. The mean input-referred offset is -0.07µV with a standard deviation of 1.85µV. The output ripple achieved 1.15mV_{rms}, showing 3 times better ripple reduction when the pair matching layout and additional current source replica circuit is employed. The core DDA3 consumes 15.5µA whereas the biasing circuit consumes 6.5µA in a 1.8V power supply for a total current of 22µA. The measured results have confirmed a better offset performance with small area design while the noise performance is maintained good. The proposed IA demonstrated good improvement when compared to other based prior-art resistor-based IA.

The final work of the proposed IA and the high PSR regulator was tested together with an emulated strain-gauge sensor to validate the functionality of the IA system. The proposed IA system was compared to other published analog front-end circuits for strain gauge or Wheatstone-bridge applications. It is successfully demonstrated that it is able to sense very small signal, with a SNR of 64.4dB for 2kHz bandwidth while consuming only 27.65 µA at a supply voltage of 2.7V. In all, with the combination of all the new circuit techniques and circuit blocks, it leads to a high precision IA system prototype that achieves low-noise, low-offset, small-area and low power consumption.

9.2. Recommendations for Future Work

With the CMOS fabrication technology continuous scaling down, the analog front-end circuit will be pushed to even lower voltage and lower power for industrial applications. The technology miniaturization causes the supply voltage to have to be decreased in order for the device to remain reliable. This is especially important when the supply voltage is reduced to sub-1V level, while the noise performance has to remain low. Circuit techniques for low noise performance in ultra-low voltage instrumentation amplifier are to be continuously explored in order to sustain good performance in analog front-end design. Noise cancellation

techniques can be introduced to maintain good noise performance in the overall circuit system.

Besides, aggressive device scaling also leads to various issues such as the increase in the leakage current, hot carrier injection issue in device and so on especially when operating in a higher supply. However, the reduced supply voltage will cause headroom issue in the circuit design. All this will lead to further architectural modifications together with new circuit techniques in order to solve the potential design obstacles in the context of deep-submicron CMOS technologies and hence enhance the circuit's yield and robustness. Moving into deep-submicron technology, some special devices i.e. LDMOS, dual-gate MOSFET and others available devices can be explored in overcoming the design challenge.

In the regulator design, the temperature coefficient obtained from the measurement deviated from the simulation results due to inaccuracy in transistor model for temperature characterizations. Off-chip trimming method can be added for better output voltage calibration in the view of temperature drifting effect. Besides, there is challenge in measuring high frequency PSR performance i.e. -60dB @ 1MHz in the regulator design due to the existence of parasitic capacitor to the power supply rail in the ESD pad ring. Although the high frequency PSR of the regulator can be improved by having external capacitor at the output, this will impose an extra cost on the design where an output capacitorless regulator design is still favourable. Hence, a dedicated pad with minimal parasitic capacitor can be developed in the future for better PSR performance measurement.

In addition, in this work the differential common-mode performance in the chopping differential difference amplifier has been introduced. New circuit techniques can be explored to further improve the differential common-mode rejection ratio in the chopping differential difference amplifier besides using the proposed technique in this work as the continuation of

this project. Other design parameters which also related to the differential common-mode performance such as the gain accuracy can be studied and researched further.

The proposed instrumentation amplifier system has demonstrated an area and power efficient way to implement a low-offset, low-noise analog front-end interface circuit. However, the data-acquisition system will require ultra-low power ADC for the amplified signals to be processed and analysed in digital domain by the microprocessor. It is worthwhile to investigate the possibility of small area and good signal-to-noise distortion (SNDR) ADC topologies for sensor applications as a continuation of this project.

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1. G.T. Ong and P.K. Chan, "A Low Quiescent Biased Regulator With High PSR Dedicated to Micropower Sensor Circuits ",IEEE Sensors Journal , vol. 10, pp. 1266-1275, July 2010.

2. G.T. Ong and P.K. Chan, "A Micropower Gate-Bulk Driven Differential Difference Amplifier with Folded Telescopic Cascode Topology for Sensor Applications", Presented at IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2010), Aug 2010, pp. 193-196.

3. G.T. Ong and P.K. Chan, "A Low Noise, 1.28µA Quiescent Regulator with Broadband High PSR for Micropower Sensors", accepted by IEEE International Symposium on Circuits and Systems (ISCAS 2012).

4. G.T. Ong and P.K. Chan, "A Chopper-Stabilized Instrumentation Amplifier with 3µV Offset and 0.125mm^2 Area in 0.18µm CMOS", submitted to IEEE journal for review.

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