

A 311.6 GHz Phase-locked Loop in 0.13 μm SiGe BiCMOS Process with -90 dBc/Hz in-band Phase Noise

Yuan Liang^{1,2*}, Chirn Chye Boon^{1*}, Qian Chen¹, Zhe Liu¹, Chenyang Li¹, Thomas Mausolf²,
Dietmar Kissinger³, Yong Wang^{4*}, and Herman Jalli Ng^{5*}

¹Nanyang Technological University, Singapore 639798

²IHP, Innovations for High Performance Microelectronics, Germany 15236

³Ulm University, Ulm, Germany 89081

⁴University of Electronic Science and Technology of China, China 611731

⁵Karlsruhe University of Applied Sciences, Karlsruhe, Germany 76133

*Contact author: yliang017@e.ntu.edu.sg, ECCBoon@ntu.edu.sg, yongwang@uestc.edu.cn, herman.j.ng@ieee.org

Abstract—Using a quadrature XOR-gate (QXOR) reduces the second order harmonic term at the output, making it suitable to be used as a phase/frequency detector in high-frequency phase-locked loops. This paper introduces a 320 GHz PLL employing QXOR to cancel the reference spur, suppress in-band noise, and also reduces the power consumption of the frequency tracking loop (FTL). The beat frequency of FTL enables the lock detector (LD) to search the right band for VCO operation. The proposed PLL was implemented in IHP 0.13 μm SiGe BiCMOS process. Measured results show that the PLL achieves a locking range from 307.45 GHz to 321.28 GHz, while consuming 372 mW DC power, with -113.7 dBc/Hz phase noise at 1 MHz offset measured at 40.96 GHz. This leads to an integrated RMS jitter (1k–30MHz) of 72 fs. The measured phase noise at 311.6 GHz is -90 dBc/Hz at 1 MHz offset, with a total division ratio of 512. The measured maximum probed output power is -3.3 dBm. The PLL occupies a 1.4 mm² area.

Index Terms—Terahertz, Quadrature XOR phase detector, Miller divider, mm-wave applications, phase-locked loop (PLL), phase noise, voltage-controlled oscillator (VCO).

I. INTRODUCTION

Systems operating from millimeter-wave (mm-wave) to terahertz frequency have recently been demonstrated and implemented for various applications. For example, 60-GHz transceivers are used for multi-Gb/s wireless communication [1–2]. 94 GHz is used for medical imaging system [3]. 140 GHz and 320 GHz transceivers are developed toward short-range yet high-speed data communication [4–12]. All these mm-wave and terahertz systems require an accurate and robust high-frequency signal generator, which becomes increasingly challenging to meet the stringent noise requirement.

In this paper, we present a terahertz phase-locked loop by exploiting a quadrature XOR-gate (QXOR) to be used as the phase/frequency detector. The operation and in-band noise suppression of PD will be discussed. The frequency tracking loop (FTL) employs QXOR as well

and enables the lock detector (LD) to perform band searching for VCO. Circuit blocks will be described.

II. PLL ARCHITECTURE.

An attractive approach to suppress the N^2 in-band noise multiplication is to use higher reference frequency f_{ref} . This call for a high-frequency PLL to be locked by a low-frequency signal generator. Such an architecture is conceptualized in Fig. 1, where an 80 GHz VCO is phase-locked in a closed loop, with the reference signal provided by a delay-locked loop whose output frequency is an integer multiplication factor of the crystal frequency. The 320 GHz signal is extracted from a frequency quadrupler. In this work, we report the performance of the proposed 320 GHz PLL.

For an XOR-gate operating as a typical large-signal PD, the output waveform exhibits a behaviour involving a beat frequency Δf equal to the frequency error of the inputs. This allows Δf to be extracted by passing the PD to a low-pass filter (LPF). The proposed QXOR inherently enhances the first harmonic at Δf and suppresses the second harmonic $2\Delta f$. The LPF corner frequency can be hereby roughly set to $2\Delta f$ to suppress higher harmonic terms. As Δf is extracted, the proposed QXOR can be used for both frequency detection and phase alignment. In Fig. 1, the quadrature reference signal is generated by a static divider. A transconductance amplifier (TA) converts the QXOR PD output voltage to current and locks the VCO.

The 320 GHz frequency quadrupler involves a quadrature RC polyphase filter, multiple buffer stages and two-stage push-push frequency doubler. The simulated quadrature error is less than 1° from 76 GHz to 82 GHz.

III. CIRCUIT DESIGN

A. Mm-wave building block

The 80 GHz VCO is depicted in Fig. 2(a). A fundamental frequency differential Colpitts VCO is chosen for low phase noise and wide tuning range. Tail

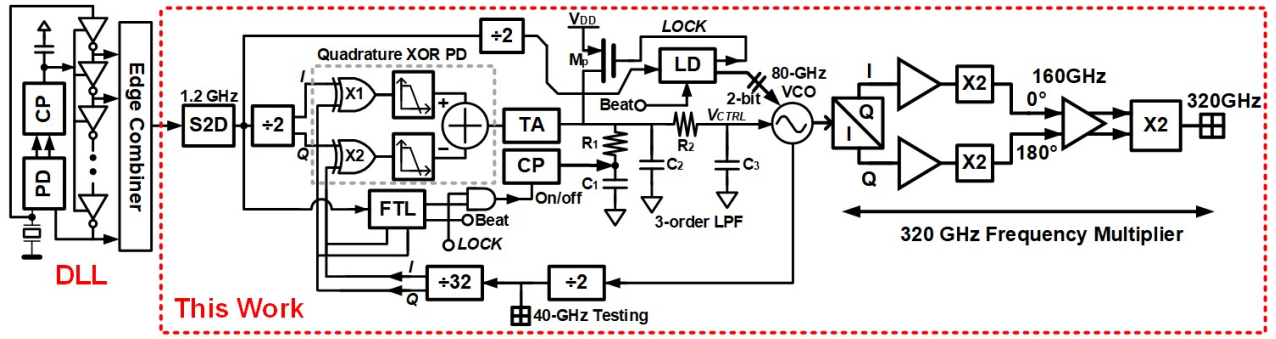


Fig. 1. Proposed 320 GHz PLL architecture involving an 80 GHz loop and a 320 GHz frequency quadrupler.

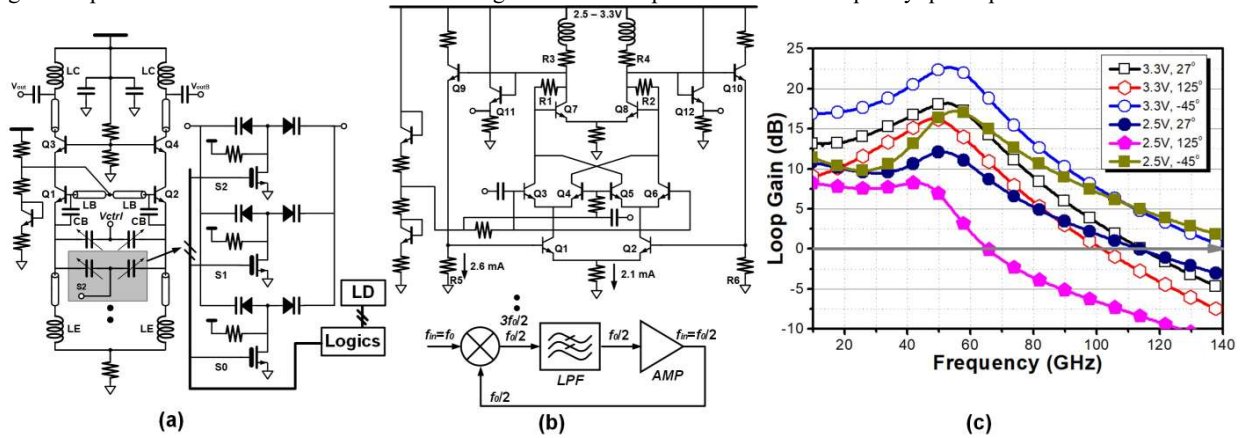


Fig. 2. (a) Colpitts VCO, (b) Miller divider, and (c) post-layout simulated loop gain of the miller divider.

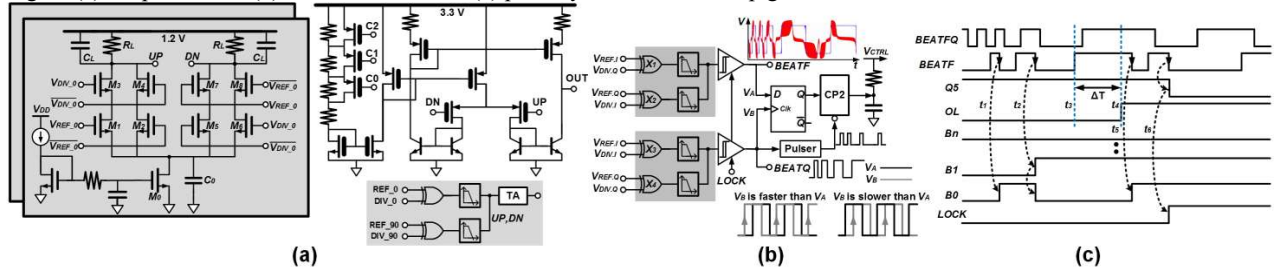


Fig. 3. (a) Quadrature XOR-gate (QXOR) based PD and the transconductance amplifier (TA), (b) FTL using dual QXOR-gate, and (c) the band-searching and settling behavior of the PLL.

current source has been removed to prevent flicker noise up-conversion. The size of transistor and the common mode voltage are determined toward the highest f_{max} of HBT. The VCO incorporates a 2-bit coarse tuning with fine tuning gain of $K_{VCO} = 620 \text{ MHz/V}$.

The prescaler is illustrated in Fig. 2(b). Miller divider is chosen for its low power yet wide bandwidth operation. Here, Q_1 - Q_6 form the harmonic mixer, $Q_{7,8}$ and $R_{1,2}$ constitutes the transimpedance amplifier (TIA), and a source follower by $Q_{9,10}$ and $R_{5,6}$ establishes the feedback. The locking range of Miller divider can be evaluated by cutting the feedback and observe the loop gain from $Q_{1,2}$ input to the emitter of $Q_{9,10}$. The simulated loop gain over frequency is summarized in Fig. 2(c). Clearly, the high gain of the TIA allows the DC supply to be reduced from

3.3 V to 2.5 V. A minimum lock frequency of roughly 135 GHz is found at 125°, which is feasible for frequency division at 80 GHz under PVT variation. The I/Q signal is generated through a static divider.

B. QXOR phase detector

Fig. 3(a) shows the QXOR PD and transconductance amplifier. Though passive XOR-gate does not consume DC power, it generates high flicker noise in the current summer, degrading PLL in-band phase noise. Instead, an active XOR-gate featured by CML is used. Noise simulation implies that the tail current source M_0 dominates in-band noise. A 20-pF capacitor is used to bypass the thermal noise current of M_0 during each clock

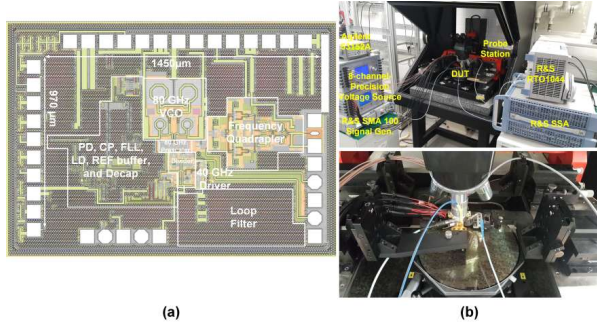


Fig. 4. Die photo of the proposed 320 GHz PLL, and (b) on-wafer testing with measurement setup.

edge without affecting the loop dynamics. As the TA operates continuously at locked, the noise of TA must be suppressed as well. Fortunately, the QXOR output is a near-DC voltage upon locked, and thus allows the TA to be implemented using large thick-oxide PMOS and HBT.

C. QXOR FTL/LD

The FTL is illustrated in Fig. 3(b) by using dual QXOR. As the frequency error is extracted by QXOR, Schmitt trigger are used to recover the signal to consecutive bits. Whether the reference clock is leading or lagging can be determined by using the signal BEATF to sample BEATFQ, and the charge pump (CP) is triggered for only a short period of time. Upon locked, no pulse is generated, and the FTL shuts down automatically.

Based on above, the band-searching and lock detection can be realized as shown in Fig. 3(c). The VCO operates at the lowest band at the beginning. As long as BEATF sample a “1”, which means the reference frequency is still higher than the divider frequency, the band register switches to the next band. To avoid false lock, a counter accumulates the rising edge of the beat signal, and overflows when $\Delta f \rightarrow 0$, then asserting the signal “OL”. After a “0” is sampled by BEATF, LD asserts, releasing M_p (see Fig. 1) and handovers the loop to PD and FTL.

IV. MEASUREMENT RESULTS

The PLL chip was implemented in IHP 0.13- μm SiGe BiCMOS featured by $f_{Tf_{max}} = 300/500$ GHz. The die photo is shown in Fig. 4(a). Excluding pads, the die size is $1450 \mu\text{m} \times 970 \mu\text{m}$. On-wafer measurement and setup are given in Fig. 4(b). The spectrum is measured by R&S SSA and the PLL reference clock is fed by R&S SMA 100.

The spectrum is measured at the first prescaler’ output. The total locking range of the 80 GHz loop is from 76.8 GHz to 83 GHz. Fig. 5 illustrates the measured spectrum at 41.28 GHz. No reference spur is observed, confirming the spur cancelling of the proposed QXOR PD. Fig. 6 demonstrates the measured -113.73 dBc/Hz phase noise at

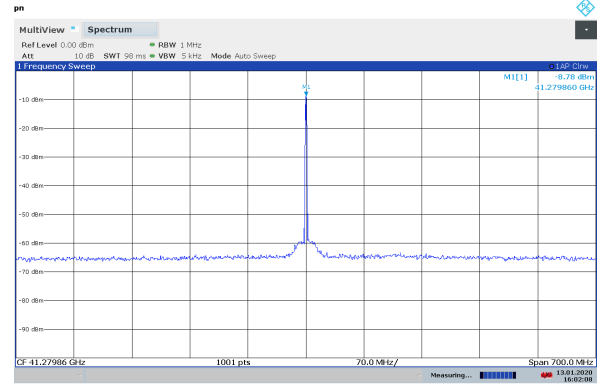


Fig. 5. Measured PLL spectrum at prescaler’s output.



Fig. 6. Measured phase noise at 40.96 GHz.

1 MHz offset at 40.96 GHz. This corresponds to an integrated RMS jitter of 72 fs (1k–30M).

PLL settling behaviour is observed from R&S RTO 1044 oscilloscope, triggered by the power supply. When LD is off, as shown in Fig. 7(a), only the PD and FD lock the loop. When LD is on, the loop is governed by LD first, then manipulated by PD and FD, as verified in Fig. 7(b).

The 320 GHz phase-locking is verified by the measured spectrum as shown in Fig. 8. The measured phase noise is -90 dBc/Hz at 1 MHz offset at 311.55 GHz, as shown in Fig. 9. A 5-dB noise degradation compared to theoretical result may come from the base resistance of the buffer stages in the frequency quadrupler. The calibrated probed output power is summarized in Fig. 10, measured by an Erickson PM5 power meter. State-of-the-art terahertz closed-loop signal sources are summarized in Table II.

V. CONCLUSION

A 307.4 to 321.3 GHz PLL is reported. Quadrature XOR-gate (QXOR) is proposed for both frequency detection and low-noise phase alignment. Based on the beat frequency of QXOR, the lock detector searches the right band automatically for VCO operation. Fabricated in IHP 0.13- μm SiGe HBT technology, the proposed PLL demonstrates a wideband phase-locking with -90 dBc/Hz phase noise at 311.55 GHz and maximum -3.3 dBm output power, consuming 372 mW DC power.

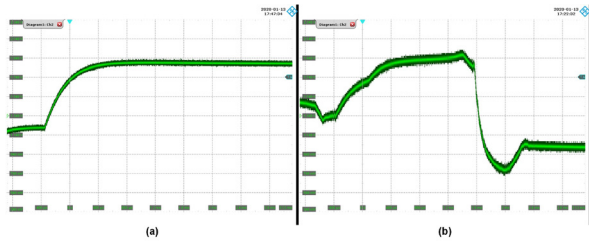


Fig. 7. Settling behavior of PLL: (a) with lock detector (LD) turned off, and (b) with LD turned on.

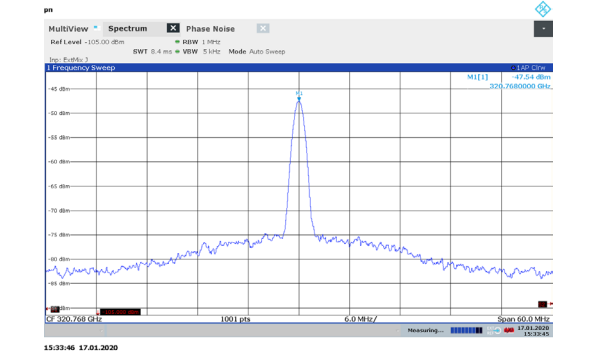


Fig. 8. Measured PLL spectrum at 320.76 GHz.



Fig. 9. Measured PLL phase noise at 311.55 GHz.

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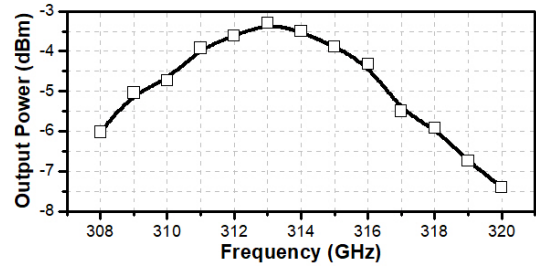


Fig. 10. Measured 320 GHz PLL probed output power.

TABLE II TERAHERTZ SOURCE PERFORMANCES SUMMARY

Ref./Para.	[9] ISSCC 2014	[10] ISSCC 2015	[11] ISSCC 2016	[12] ISSCC 2018	This work
Silicon Process	90nm SiGe	130nm SiGe	65nm CMOS	130nm SiGe	130nm SiGe
Frequency [GHz]	280~303	317	539~560	302~332	307.4~321.3
Tuning range [%]	7.9	\	3.8	9.5	4.4
Probed Output Power [dBm]	-14	5.2 [#]	-27 [#]	-13.9	-3.3
Phase Noise @ 1 MHz [dBc/Hz]	-82.5	-79	-74	-78.5	-90
DC Power [mW]	376	610	172	51.7	372
Peak DC-to-RF Efficiency [%]	0.01	0.54	0.001	0.078	0.126
Area [mm ²]	2.56	2.08	2.79	0.85	1.4

[#]: Radiated power

IEEE Radio Freq. Integr. Circuits Symp. (RFIC), Philadelphia, Pennsylvania, USA, June 2018, pp. 352–355.

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