Accurate and Scalable RF Interconnect Model for Silicon-Based RFIC Applications

Choon Beng Sia, Beng Hwee Ong, Kiat Seng Yeo, Jian-Guo Ma, *Senior Member, IEEE*, and Manh Anh Do

***Abstract*—A new figure of merit, intrinsic factor for interconnects, is proposed to provide insights as to how back-end metallization influences the performance of radio frequency integrated circuits. An accurate and scalable double-π radio frequency interconnect model, continuous across physical dimensions of width and length, is presented to demonstrate reliable predictions of interconnect characteristics up to 10 GHz. Using this interconnect model in gigahertz amplifier and voltage-controlled oscillator circuit simulations yields excellent correlations between simulated and on-wafer measured circuit results.**

***Index Terms*—Inductance, interconnects, intrinsic factor, metallization, parasitics, quality factor, radio frequency (RF), series resistance, skin effects, SPICE models, substrate loss.**

I. Introduction

GREAT advances in silicon-processing technologies over the past ten years have generated a remarkable surge in research, as well as immense commercial interest, in using these established and cost-effective technologies for radio frequency (RF) applications. Silicon technology is, at present, the most popular choice for radio frequency integrated circuit (RFIC) designs, due to huge cost savings and the possibility of achieving higher chip integration, with the RF front-end and digital/analog baseband coexisting on a common platform. Enhanced device characteristics, such as higher cutoff frequencies for transistors, allow traditional digital technologies to cope with stringent RF specifications set forth in popular communication standards, such as Bluetooth and IEEE 802.11a/b/g, etc. Nevertheless, low-resistive bulk silicon, which helps improve latch-up immunity at tighter design rules and huge resistive loss associated with the back-end-of-line metallization, are still major road blocks to achieving high circuit performance at gigahertz frequencies [1]–[3]. Hence, exploiting the cost-effective silicon technologies necessitates that circuit designers understand the technology limitations and required design tradeoffs for their RFICs.

Silicon-based RF designs are now conceptualized on computer-aided design (CAD) tools that use feature-rich process design kits (PDKs) with accurate and scalable device models developed based on extensive and reliable on-wafer RF device characterization [4]. Despite having accurate device models capable of predicting device behavior at RF, a typical RFIC still requires several design iterations before it can comply with the product specifications. These design iterations can be avoided if substrate and metallization losses at gigahertz frequencies have been carefully considered when circuits are in the design-optimization and layout phase. Introduced to provide electrical connections between devices, interconnects have detrimental effects on circuits, and as frequency increases, undesirable parasitic responses, both inductive and resistive in nature, as well as capacitive coupling to the substrate, become even more pronounced, leading to significant deterioration in circuit performance as well as shifts in circuit frequency response. Experienced RFIC designers often have to overdesign their circuits to cater to performance degradation, and subsequent costly design iterations are required for their designs to be within specifications. With accurate, scalable, and SPICE-simulator-compatible RF interconnect models, circuit designers can easily take preventive measures prior to circuit fabrication if the RF interconnects are found to have adverse effects on their circuits during postlayout simulations, thereby reducing the number of design iterations, saving development costs as well as shortening the product time-to-market cycle.

II. Test Structures and Experimental Setup

In this paper, an accurate and scalable RF interconnect model is presented. This subcircuit model is developed using a streamlined set of 25 top metal (Metal 6) interconnect test structures designed with lengths of 50, 100, 200, 400, and 800 μm and widths of 1.5, 3, 5, 10 and 20 μm, respectively. The test structures are fabricated using an industry-compatible 0.18-μm radio frequency complementary metal–oxide–semiconductor (RFCMOS) processing technology with thick top metal (2 μm) back-end-of-line process flow. On-wafer RF device measurements are carried out using Agilent 8510C Vector Network Analyzer and Cascade Microtech RF Infinity probes. The wafer and probes are shielded within the microchamber of the Cascade Microtech S300 semiautomated probe station. Two-port S-parameters of the interconnects are measured over the frequency range from 50 MHz to 10.05 GHz. Substrate taps near the top metal lines are included in all ground pads of the six-pad ground–signal–ground (GSG) configuration to ensure that the substrate is effectively grounded. Parasitics of the test pads are accurately de-embedded by subtracting Y parameters of the open calibration structures from those test structures with the interconnects [5]. Fig. 1 shows die photos taken in the course of characterizing the interconnect test structures.

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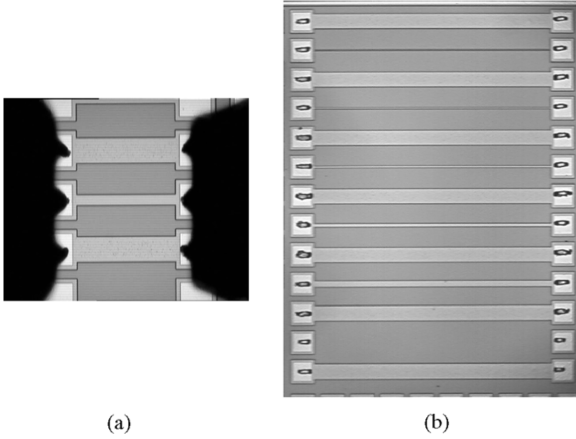

Fig. 1. Die photos. (a) Interconnect test structure with Cascade Microtech RF Infinity Probes. (b) Interconnects 800 μm in length with different widths and open calibration structure.

III. Figures of Merit and RF Subcircuit Model

To quantify the detrimental effects of interconnects on circuit performances, this paper has made a first attempt to define figures of merit, which are very useful to circuit designers when they decide on the interconnect dimensions for their RF circuits. The interconnect's figures of merit, parasitic inductance (L), and intrinsic factor (I_F) adopted for this paper are derived from the de-embedded Y-parameters in the following discussions. Although interconnects are not magnetic energy storage elements, to a certain extent, they can be regarded as on-chip inductors, and therefore, their parasitic inductance L (units in Henry) can be defined as

$$L = \frac{\text{Imag}\left[\frac{1}{Y_{11}}\right]}{2 \times \pi \times \text{Frequency}}. \tag{1}$$

Proceeding in this direction, the quality factor Q, shown in (2) for an inductor, can also be used to correlate how interconnects would influence the circuit performance

$$Q = -\frac{\text{Imag}[Y_{11}]}{\text{Real}\,[Y_{11}]}. \tag{2}$$

L and Q are both extracted from the Y_{11} and not the Y_{12} parameter, since it is important to include and consider the effects of the lossy silicon substrate when evaluating the performance of interconnects. Examining (2), the quality factor Q is defined as a ratio of imaginary $[Y_{11}]$ over real $[Y_{11}]$. This suggests that at a fixed resistive loss, when the inductance increases, the quality factor increases. However, for the case of interconnects, desirably low loss metallization should possess negligible parasitic inductance and resistance. In this paper, for RF applications, a more suitable figure of merit to describe interconnects, the intrinsic factor I_F (units in S^2, for frequency > 0), is proposed for the first time, as follows:

$$I_F = \frac{1}{\text{Imag}\left[\frac{1}{Y_{11}}\right] \times \text{Real}\left[\frac{1}{Y_{11}}\right]} \tag{3}$$

$$R_S = \text{Real}\left[-\frac{1}{Y_{12}}\right]. \tag{4}$$

From (3), interconnects with large intrinsic factors insinuate that they have small resistive and inductive parasitics. On the contrary, parasitic series resistance R_S, associated with the metallization, is extracted from the Y_{12} parameter [6], as shown in (4), to exclude losses associated with the substrate, showing the skin effects of metallization at RF.

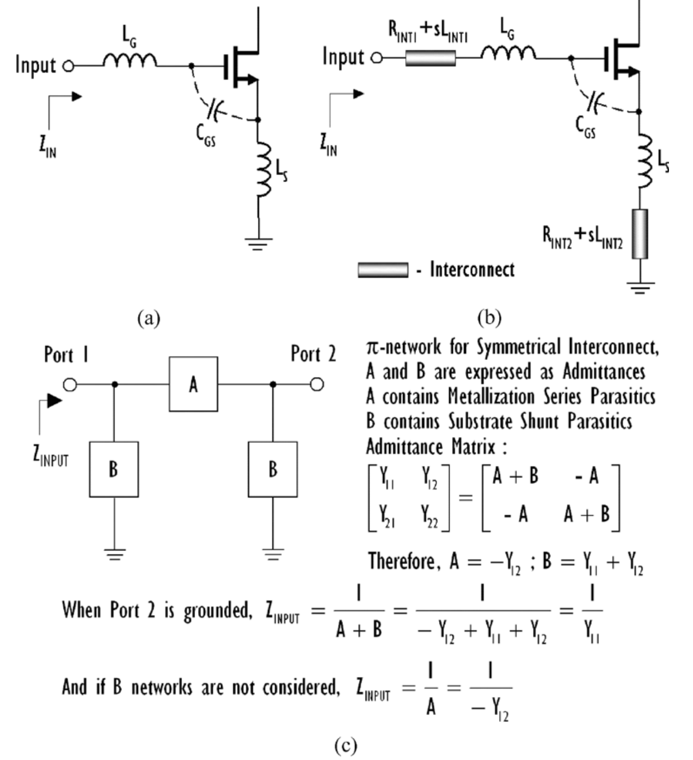

Fig. 2. Inductive source degeneration impedance matching (a) without and (b) with consideration of interconnect metallization. (c) A π-network and its corresponding admittance matrix representing a two-port symmetrical interconnect.

Schematics in Fig. 2 help illustrate, with an inductive source-degeneration impedance-matching example, how I_F can be used as a performance indicator for interconnects. Fig. 2(a) shows the ideal input matching circuit with lossless inductors L_S and L_G providing optimal matching for the nMOSFET, and only its transconductance and gate-source capacitance are considered [7] in the following discussions. As such, the input impedance Z_{IN} can be expressed as

$$Z_{\text{IN}} = s(L_G + L_S) + \frac{1}{sC_{GS}} + \left(\frac{g_m}{C_{GS}}\right) L_S \tag{5}$$

where g_m is the transconductance of the nMOSFET, and C_{GS} is the gate-source capacitance of the nMOSFET and $s = j^*2\pi^*$ frequency.

For maximum power transfer to occur at the operating frequency, real $[Z_{\text{IN}}]$ have to match the source resistance R_{SOURCE}, which is typically 50 ohms

$$\left(\frac{g_m}{C_{GS}}\right) L_S = R_{\text{SOURCE}} \tag{6}$$

and the imaginary impedances must satisfy the following condition:

$$s(L_G + L_S) = \frac{1}{sC_{GS}}. \tag{7}$$

From (6) and (7), values of L_S and L_G are first determined, so that the ideal impedance-matching criteria can be fulfilled. In the schematic-design phase, effects from the interconnect structures required to provide necessary electrical continuity between devices are not taken into account. If only metallization series resistive and inductive parasitics are considered in this example, as shown in Fig. 2(b), the new input impedance Z_{IN} can be formulated as

$$\begin{aligned} Z_{\text{IN}} = s(L_G + L_S) + s(L_{\text{INT1}} + L_{\text{INT2}}) + \frac{1}{sC_{GS}} \\ + \left(\frac{g_m}{sC_{GS}}\right) R_{\text{INT2}} + R_{\text{INT1}} + R_{\text{INT2}} \\ + \left(\frac{g_m}{C_{GS}}\right) (L_S + L_{\text{INT2}}). \end{aligned} \quad (8)$$

For impedance matching at the operating frequency, real $[Z_{\text{IN}}]$ will have to match the source resistance

$$R_{\text{INT1}} + R_{\text{INT2}} + \left(\frac{g_m}{C_{GS}}\right) (L_S + L_{\text{INT2}}) = R_{\text{SOURCE}} \quad (9)$$

and the imaginary impedance will have to satisfy the new condition

$$s(L_G+L_S)+s(L_{\text{INT1}}+L_{\text{INT2}}) = \frac{1}{sC_{GS}} + \left(\frac{g_m}{sC_{GS}}\right) R_{\text{INT2}}. \quad (10)$$

To achieve maximum power transfer, real $[Z_{\text{IN}}]$ must be matched to the source resistance, but evaluating (6) and (9) reveal that additional components of $(R_{\text{INT1}} + R_{\text{INT2}})$ and $L_{\text{INT2}*}(g_m/C_{GS})$ have impeded the performance of the original matching inductor L_S. Comparing (7) and (10), the resonant frequency of the impedance-matching network differs by the extra components of $s(L_{\text{INT1}} + L_{\text{INT2}})$ and $R_{\text{INT2}*}(g_m/sC_{GS})$. These parasitic components from the interconnects contribute to an unfavorable shift in the frequency response of the circuit, as opposed to when input matching is performed using L_S and L_G without considering effects from the interconnects. Therefore, without prior knowledge of the parasitic resistances and inductances introduced by the interconnects, operating frequency in this narrow-band RFCMOS design is altered, and power is not transferred efficiently into the nMOSFET. If both interconnects in Fig. 2(b) are identical, i.e., $R_{\text{INT1}} = R_{\text{INT2}} = R_{\text{INT}}$ and $L_{\text{INT1}} = L_{\text{INT2}} = L_{\text{INT}}$, (9) and (10) simplify to

$$2R_{\text{INT}} + \left(\frac{g_m}{C_{GS}}\right) (L_S + L_{\text{INT}}) = R_{\text{SOURCE}} \quad (11)$$

$$s(L_G + L_S) + s(2L_{\text{INT}}) = \frac{1}{sC_{GS}} + \left(\frac{g_m}{sC_{GS}}\right) R_{\text{INT}}. \quad (12)$$

In this example, for simplicity, the interconnects used are assumed to have only metallization series parasitics, and the substrate shunt parasitics are excluded. From Fig. 2(c), without having any shunt parasitics (emulated by B networks), the symmetrical interconnect, which is represented by a π-network, can be described with just the -Y_{12} parameter from its two-port admittance matrix (i.e., A network only) [8]. Hence, I_F for the interconnects in this example can be written as

$$\begin{aligned} I_F &= \frac{1}{\text{Imag}\left[\frac{-1}{Y_{12}}\right] \times \text{Real}\left[\frac{-1}{Y_{12}}\right]} \\ &= \frac{1}{2 * \pi * \text{Frequency} \times L_{\text{INT}} \times R_{\text{INT}}}. \end{aligned} \quad (13)$$

From (13), when I_F is very large, it suggests that both R_{INT} and L_{INT} are negligibly small, and hence, (11) and (12) tend to the original matching conditions described in (6) and (7)

$$2R_{\text{INT}}^{\nearrow 0} + \left(\frac{g_m}{C_{GS}}\right) (L_S + L_{\text{INT}}^{\nearrow 0}) \rightarrow \left(\frac{g_m}{C_{GS}}\right) L_S$$

$$\begin{aligned} &s(L_G + L_S) + s(2L_{\text{INT}}^{\nearrow 0}) \\ &= \frac{1}{sC_{GS}} + \left(\frac{g_m}{sC_{GS}}\right) R_{\text{INT}}^{\nearrow 0} \rightarrow s(L_G + L_S) = \frac{1}{sC_{GS}}. \end{aligned}$$

Therefore, using interconnects with high I_F will have less significant impact on circuit performance, as they allow fabricated circuits to have smaller frequency shifts and minimal degradation on the transfer of power, previously optimized in circuit schematic simulations, when interconnects are not taken into consideration. Monitoring the parasitic resistance, inductance, and capacitive substrate loss individually, i.e., real and imaginary impedances, is very cumbersome, and exploiting the proposed I_F provides a quick performance benchmarking indicator for circuit designers. More importantly, having accurate and scalable interconnect models which are SPICE-simulator compatible allow circuit designers to take evasive action before product fabrication, reducing design iterations if postlayout simulations reveal that additional metallization causes circuits to perform out of specifications.

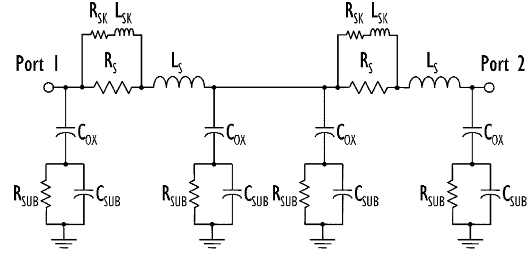

Fig. 3. Double-π RF subcircuit model for interconnects.

In this paper, a scalable double-π RF subcircuit model for interconnects is proposed, as shown in Fig. 3. L_S and R_S describe the parasitic self-inductance and resistive loss on the metallization, respectively. L_{SK} and R_{SK} model the skin effects of the metallization at RF. Substrate loss for interconnect is modeled by the resistor–capacitor (RC) network that consists of C_{OX}, C_{SUB}, and R_{SUB}. These three elements describe the oxide capacitance between the silicon substrate and metallization, the capacitive losses, and resistive losses in the silicon substrate, respectively. The double-π model is symmetrical, and values for the model elements are identical for the two π networks. It is also SPICE-simulator compatible, and does not contain any elements, especially resistors, which are described by frequency-dependent functions or equations, currently not supported in commercial SPICE circuit simulators. Fig. 4 illustrates a flowchart that summarizes an extraction strategy to obtain values of the model

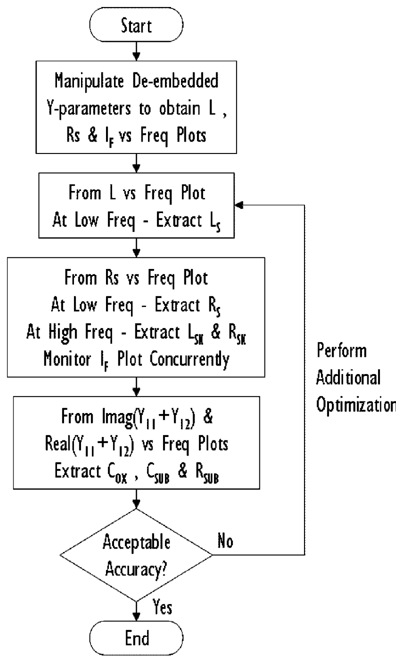

Fig. 4. Parameter-extraction procedure for double-π RF interconnect model.

parameters accurately. For example, L_S is extracted only at low frequencies of L versus frequency plot, since L from (1) contains substrate loss effects, which are apparent at high frequencies. To extract $R_{\rm SK}$ and $L_{\rm SK}$, dominant at high frequencies, R_S from (4) is used because lossy effects from substrate are excluded when Y_{12} instead of Y_{11} parameters are used to define R_S.

IV. Accuracy and Continuity of the RF Interconnect Model

The extraction routine described in Fig. 4 is implemented in IC-CAP (Agilent's device characterization and modeling software) using parameter-extraction language (PEL) to obtain values of the components in the RF subcircuit model. These model parameters are then each formulated with empirical functions that best emulate their relationships in terms of the interconnects' width W and length L (both in μm), valid only within the physical-design boundaries described in this paper ($1.5 \leq W \leq 20$ and $50 \leq L \leq 800$ μm). As an example, the parasitic inductance can be predicted using $L_S = -5.95E-12+9.28E-12^{*}\log(W)+5.51E-13^{*}L-2.70E-12^{*}(\log W)^2-2.68E-18^{*}L^2-6.95E-14^{*}\log W^{*}L$. Fig. 5, on the other hand, demonstrates how well SPICE simulated (.s) two-port S-parameters of this double-π model can predict the measured (.m) L, R_S, Q, and I_F, for an interconnect with length and width of 800 μm and 20 μm, respectively. In Fig. 5(c), Q increases as frequency increases. Fig. 5(d), on the contrary, reveals that I_F is more appropriate to describe the performance of interconnects, since it decreases as frequency increases, describing the proliferation of parasitic inductance, resistance, and substrate losses associated with interconnects as operating frequency escalates.

A single-π lumped-element RF subcircuit model, shown in Fig. 6, can also be used to model interconnects operating at giga-

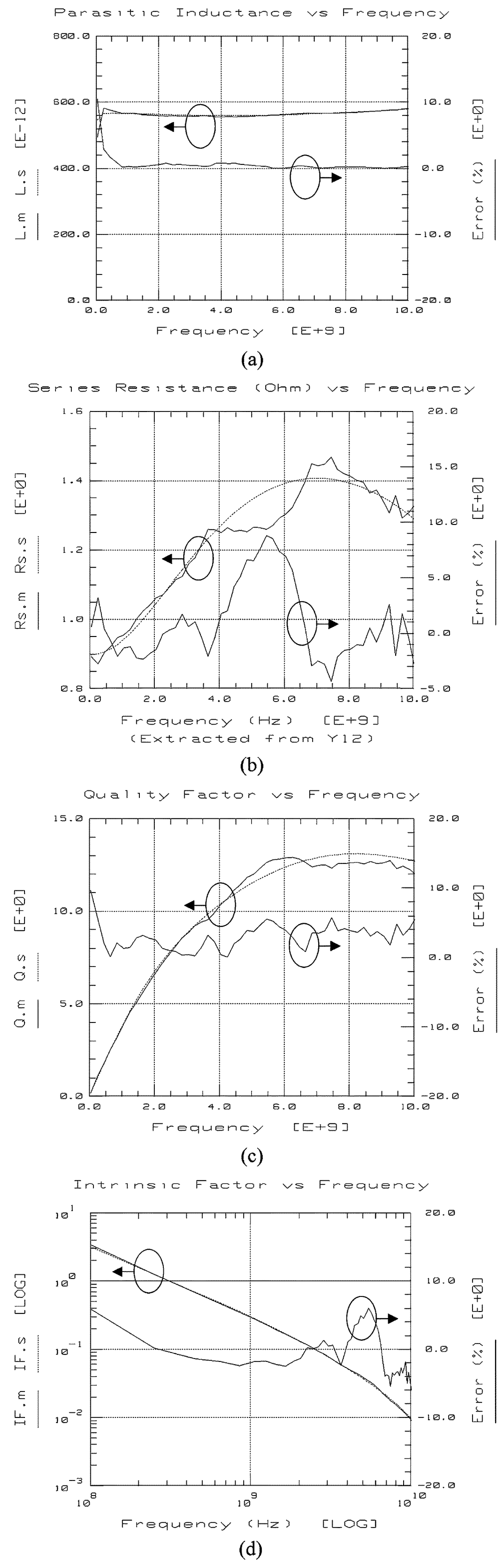

Fig. 5. (a) Measured versus simulated parasitic inductance. (b) Series resistance extracted from Y_{12}. (c) Quality factor Q. (d) Intrinsic factor I_F versus frequency for interconnect with length and width of 800 μm and 20 μm, respectively, using the proposed double-π RF interconnect model.

hertz frequencies. However, there is a limitation to this approach at the higher RF regime, and this model inadequacy is even more evident for long interconnect lines, whereby the single-π model is not able to predict the reduction of the extracted series re-

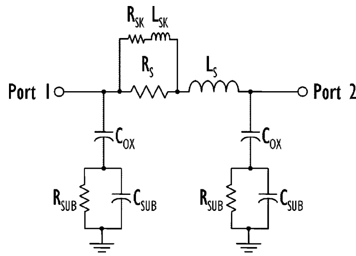

Fig. 6. Single-π lumped-element RF subcircuit model for interconnects.

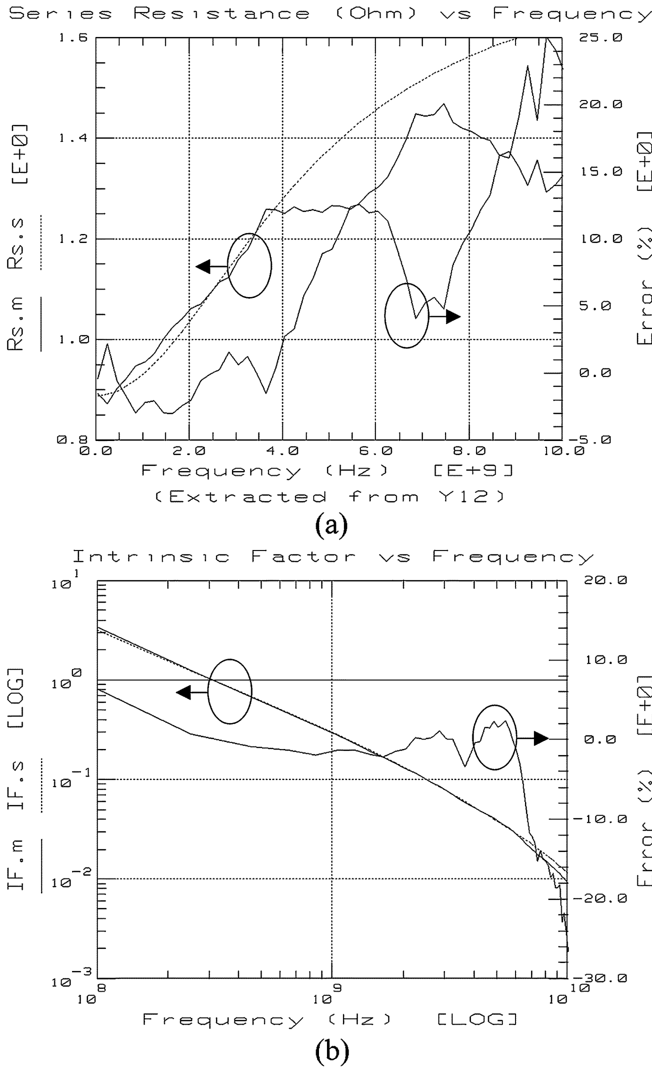

Fig. 7. (a) Measured versus simulated series resistance extracted from Y_{12}. (b) Intrinsic factor I_F versus frequency for interconnect with length and width of 800 μm and 20 μm, respectively, using a single-π lumped-element RF subcircuit model.

sistance R_S revealed in Fig. 7(a). This phenomenon can be attributed to the fact that as frequency increases, interconnects behave like transmission lines with distributed characteristics, and hence, a simple lumped-element π model is insufficient to describe its behavior. When a single-π lumped-element model is adopted for the same interconnect in Fig. 5, the error between the measured and simulated values for R_S and I_F worsen from about $\pm$ 8% to more than $\pm$ 25%, as shown in Fig. 7.

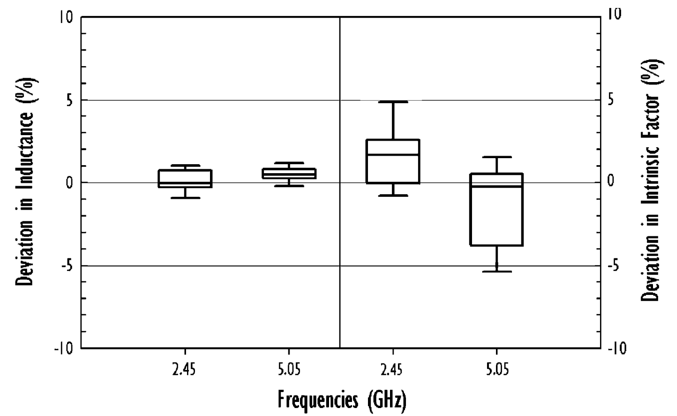

Fig. 8. Box plots showing deviation between simulated and measured parasitic inductance and intrinsic factor I_F at 2.45 and 5.05 GHz for the Metal-6 interconnect test structures.

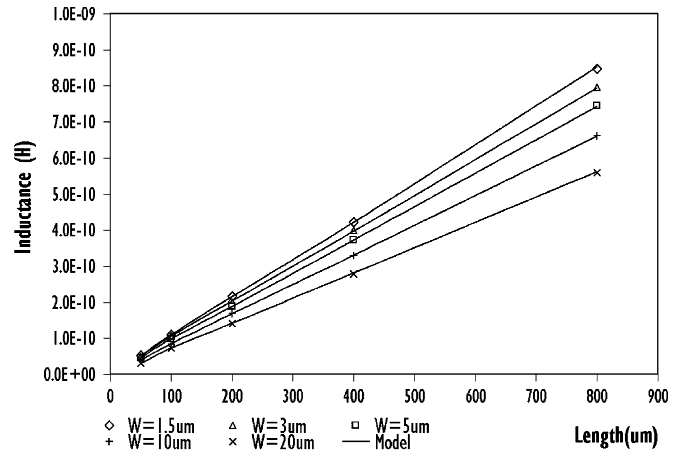

Fig. 9. Double-π RF interconnect model continuity. Simulated and measured interconnect inductance versus length for different widths at 2.45 GHz.

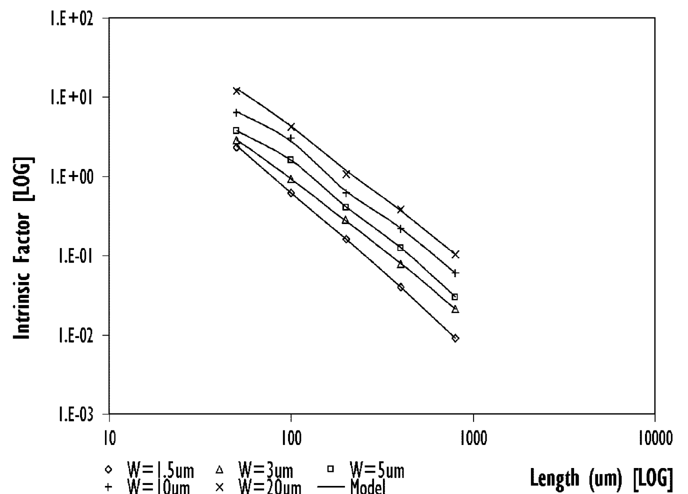

Fig. 10. Double-π RF interconnect model continuity. Simulated and measured intrinsic factor I_F versus length for different widths at 2.45 GHz.

Up to 10 GHz, employing models with multiple $\pi(> 2)$ networks are less likely to provide any significant improvement in accuracy for predicting these interconnects. Such complex

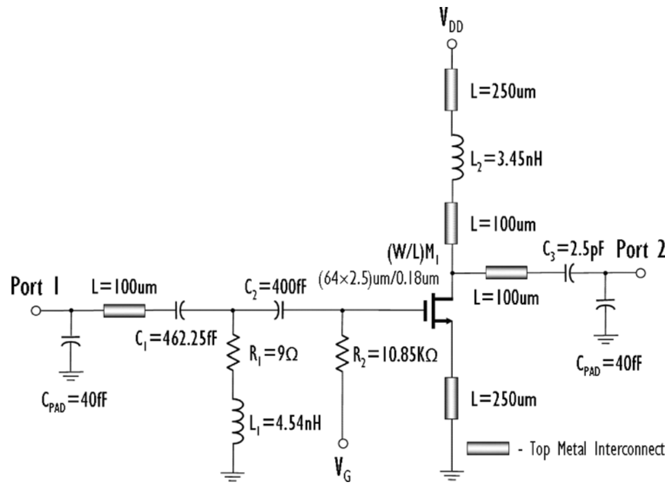

Fig. 11. Schematic of a simple gigahertz amplifier circuit to verify the accuracy of the double-π RF interconnect model. Lengths of interconnects in various parts of the circuit are also included.

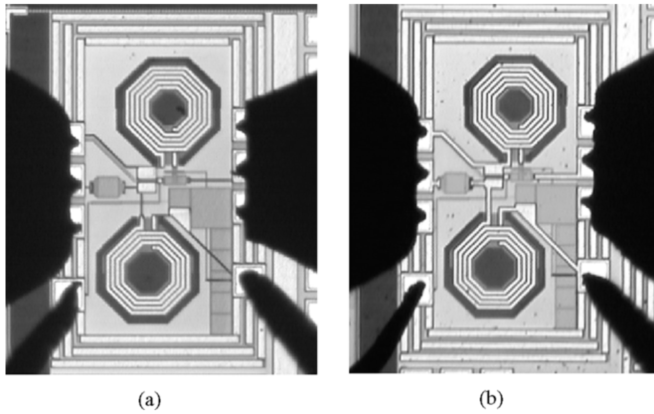

Fig. 12. Die photos showing on-wafer circuit characterization of gigahertz amplifiers with different interconnect widths. (a) 1.5 μm. (b) 10 μm.

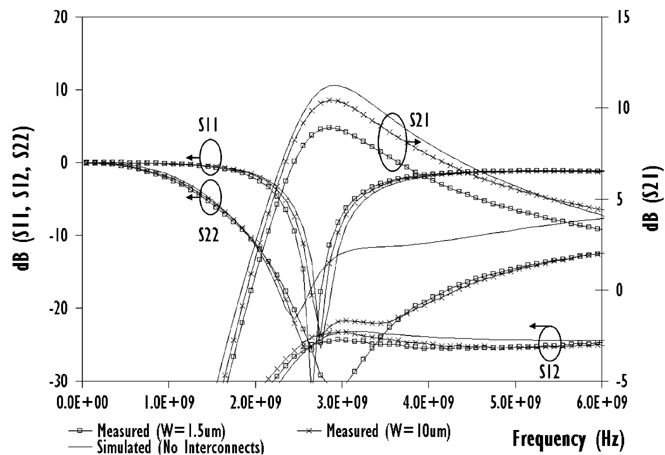

Fig. 13. Magnitude of measured S-parameters versus frequency for the two amplifier circuits with interconnect widths of 1.5 and 10 μm, respectively.

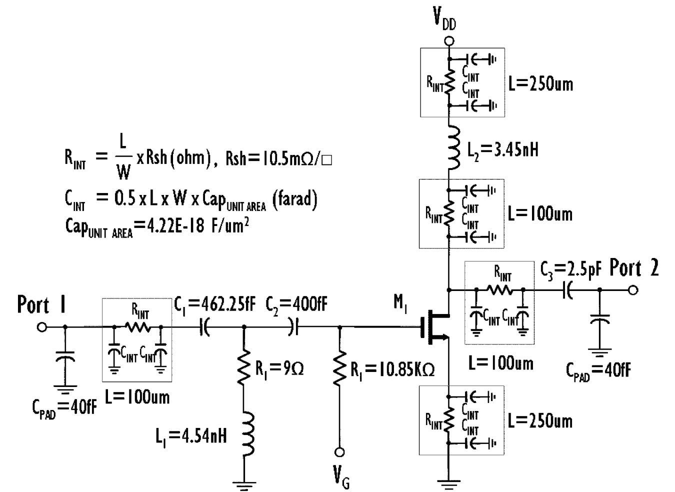

Fig. 14. Schematic of the gigahertz amplifier circuit showing representation of metallization interconnects with conventional RC extraction.

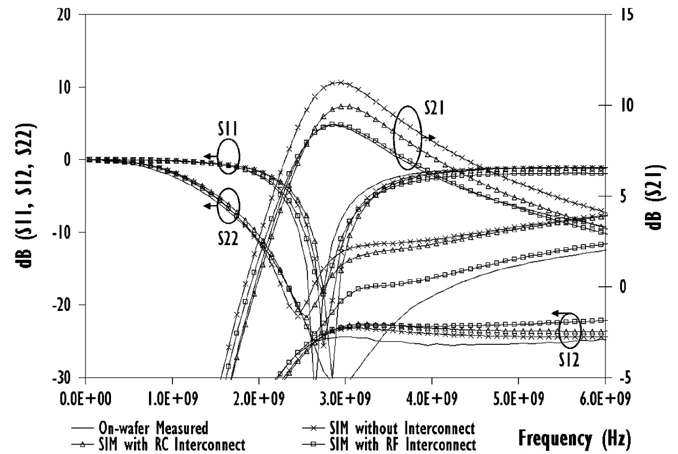

Fig. 15. Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 1.5 μm using different interconnect schemes.

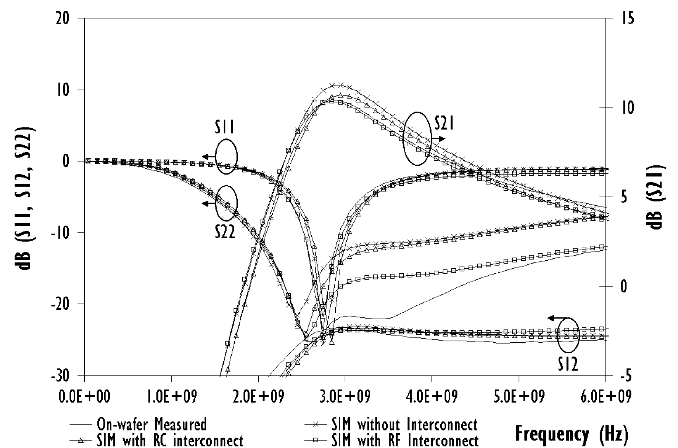

Fig. 16. Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 10 μm using different interconnect schemes.

models are more difficult to extract, and the amount of simulation time required when they are used in circuit-level simulation is most likely to increase. When compared with the frequency-independent circuit model for spiral inductors in [9], the proposed interconnect model is less complicated, with no capacitive coupling network between the input and output device terminals, and it possesses a much simplified substrate network.

TABLE I
MEASURED VERSUS SIMULATED GAIN AND PEAK GAIN FREQUENCY FOR GIGAHERTZ AMPLIFIERS WITH DIFFERENT INTERCONNECT WIDTHS

Interconnect Width in the Amplifiers Layout (μm)	Amplifiers' Measured Max. Gain(dB) [Peak Gain Frequency (GHz)]	Simulated Gain at Peak Gain Frequency Using Different Interconnect Modeling Schemes					
		No Interconnect Model		With RC Interconnect Model		With Double π RF Interconnect Model	
		Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)	Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)	Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)
1.5	8.93 [2.85]	11.25 [2.93]	25.98	9.95 [2.97]	11.42	8.92 [2.85]	-0.11
10	10.43 [2.87]	11.25 [2.93]	7.86	10.70 [2.95]	2.59	10.34 [2.87]	-0.86

The double-π model is not only adequate in emulating high-frequency effects with excellent accuracy, but also scalable and continuous across various physical dimensions of the interconnects. Examining the model accuracy in predicting the test structures at popular application frequencies such as Bluetooth and wireless LAN applications, the box plot in Fig. 8 consolidates the deviation between the measured and simulated parasitic inductances for majority of the 25 interconnect test structures to be within $\pm 1\%$ at 2.45 and 5.05 GHz. It also shows that the proposed double-π model has an intrinsic factor I_F accuracy of within $\pm 5\%$ at 2.45 and 5.05 GHz.

Fig. 9, on the other hand, demonstrates that at 2.45 GHz, the scalable interconnect model can accurately predict the measured inductances, and is continuous for all the RF interconnects with various metallization widths and lengths. Fig. 10 examines the simulated versus measured interconnect intrinsic factor I_F for all the interconnects at 2.45 GHz, and further assures that the scalable double-π model is incessant and precise. It also reveals that long-length narrow-width interconnects must be avoided in RFICs, since short-length wide-width interconnects are less lossy with relatively much larger I_F values.

V. MODEL VERIFICATION USING GIGAHERTZ AMPLIFIER AND VOLTAGE-CONTROLLED OSCILLATOR

Conventional gigahertz amplifier and voltage-controlled oscillator (VCO) circuits are designed and fabricated in the same 0.18 μm RFCMOS technology to demonstrate accuracy, scalability, and SPICE-simulator compatibility of the double-π RF interconnect model. The amplifier design, consisting of a RF nMOS thin gate transistor with input and output matching networks, is expected to operate at 2.45 GHz with a gain of about 10 dB. With reference to the gigahertz amplifier circuit schematic shown in Fig. 11, C_1, C_2, R_1, and L_1 are used to provide narrow-band (2.45 GHz) 50-ohm input matching at the gate of the transistor M_1. R_1 is employed to marginally reduce the quality factor of L_1, so that a large input-matching bandwidth can be achieved. Output matching network to the external test system is made up of L_2 and C_3. R_2 is used to isolate the DC biasing from a high-frequency signal path at the gate of the transistor. Last but not least, for the amplifier to operate, 0.9 V and 1.8 V DC biases are applied to V_G and V_{DD} terminals, respectively.

To verify the validity and precision of the proposed RF interconnect model, two device-identical gigahertz amplifier circuitries are fabricated using the same interconnect lengths, but with interconnect widths of 1.5 and 10 μm. Experimental control of maintaining the same interconnect length helps minimize unfavorable effects on circuit performances associated with signal coupling and device-layout placement, which may lead to a biased experimental comparison. Fig. 12 shows die photos of the device-identical amplifier circuits with different interconnect widths. On-wafer RF circuit characterization for the amplifiers are performed on a "golden" or typical die, selected using data obtained from full wafer map device measurements of RF scribe-line test structures to account for variations in the fabrication process [10]. A similar experimental setup, described in Section II, has been used, taking into consideration the selection of source power on the network analyzer. The two amplifiers' measured two-port S-parameters consolidated in Fig. 13 reveal that an amplifier with interconnect width of 1.5 μm has a much smaller gain and lower peak gain frequency, compared with the amplifier with interconnect width of 10 μm.

These observations are attributed to the fact that 1.5 μm-width metal lines introduce both larger RF resistive losses and parasitic inductances along the RF signal path of the amplifier circuitry, compared with 10 μm width interconnects, and hence, they resulted in larger gain reduction and a shift in circuit operating frequency, respectively. The experimental circuit results presented in this section have reiterated that interconnects with large I_F values are preferred for routing RFICs during the mask layout phase, since across various corresponding lengths, 10 μm-width interconnects have I_F values at least twice as large as 1.5 μm-width interconnects (see Fig. 10). More notably, Fig. 13 has disclosed the existence of intolerable discrepancies between simulated and measured circuit performances, even when very accurate RF device models are used for circuit simulations. Without prior knowledge of the interconnects' intrinsic factor, as well as SPICE-compatible interconnect models, there is no way RFIC designers can quantify the detrimental effects of postlayout interconnects; costly and time-consuming design iterations will be necessary for the circuit to perform within specifications.

The double-π RF interconnect model proposed in Section III is deployed in the postlayout back-annotated schematic in Fig. 11 to predict the overall circuit degradation contributed by the inter-

connects at high frequencies. Fig. 14, on the other hand, shows the amplifier schematic with a typical RC approach to investigate the effects of the interconnects. These two schematics allow multiple SPICE simulations of the amplifiers to be performed, so that meaningful comparisons can be made between existing RC and the proposed RF interconnect modeling methodologies. The measured and simulated S-parameters of the amplifier with interconnect width of 1.5 μm are evaluated in Fig. 15. Simulated gain (11.25 dB) at peak gain frequency (2.93 GHz) of this amplifier without any interconnects is very much higher, compared with the actual measured gain (8.93 dB) and peak gain frequency (2.85 GHz). With RC interconnects, simulated results only managed slight improvement in predicting the measured gain, because this model does not account for the increase in the interconnect's series resistance due to skin effects at high frequency. In addition, the absence of metallization self-inductance in the RC model also results in over-predicting the peak gain frequency by about 120 MHz.

On the other hand, when the double-π RF interconnect model is used, the simulated results correlate well with the measured amplifier performance in terms of absolute gain and peak gain frequency, with the input and output matching characteristics within acceptable limits. This outstanding agreement is possible because the parasitic inductance, as well as high-frequency resistive loss, associated with the interconnects are well emulated by the double-π RF interconnect model. Similar improvements between the measured and simulated S-parameters are also noted for the amplifier with 10 μm-width interconnects in Fig. 16. The RC interconnect approach is inadequate in predicting the measured gain and peak gain frequency of the amplifiers. Using the RF interconnect models generates excellent agreement between the measured and simulated two-port characteristics for the amplifiers with different interconnect widths, demonstrating proficient model accuracy, continuity, and scalability. Table I summarizes and compares the measured versus simulated maximum gain and peak gain frequency for the two amplifiers using the RC and RF interconnect models.

Accuracy and reliability of the double-π RF interconnect model is further scrutinized using a conventional gigahertz VCO design. The postlayout back-annotated schematics illustrating the addition of interconnect metallization in the VCO and buffer amplifier designs are summarized in Fig. 17(a) and (b), respectively. In Fig. 17(a), the VCO tank circuitry comprises L_1, L_2, C_1, C_2, C_3, and C_4 to define the oscillation frequency of the differential signal pairs at terminals $-V_{\rm OSC}$ and $+V_{\rm OSC}$. These two terminals are then each connected to the buffer amplifier with low output impedance for higher load-driving capability, shown in Fig. 17(b).

In Fig. 17(a), the crossed-coupled nMOSFETs for the VCO design, M_1 and M_2, generate negative resistance to counteract the resistance from the inductor-capacitor (LC) tank, thereby launching the VCO into oscillation. MOS varactors C_3 and C_4, operating in the accumulation mode, are used to vary the oscillating frequency of the VCO. Reference and control DC voltages, applied on terminals $V_{\rm REF}$ and $V_{\rm CTRL}$, respectively, are used to change the capacitances of the MOS varactors. Finally,

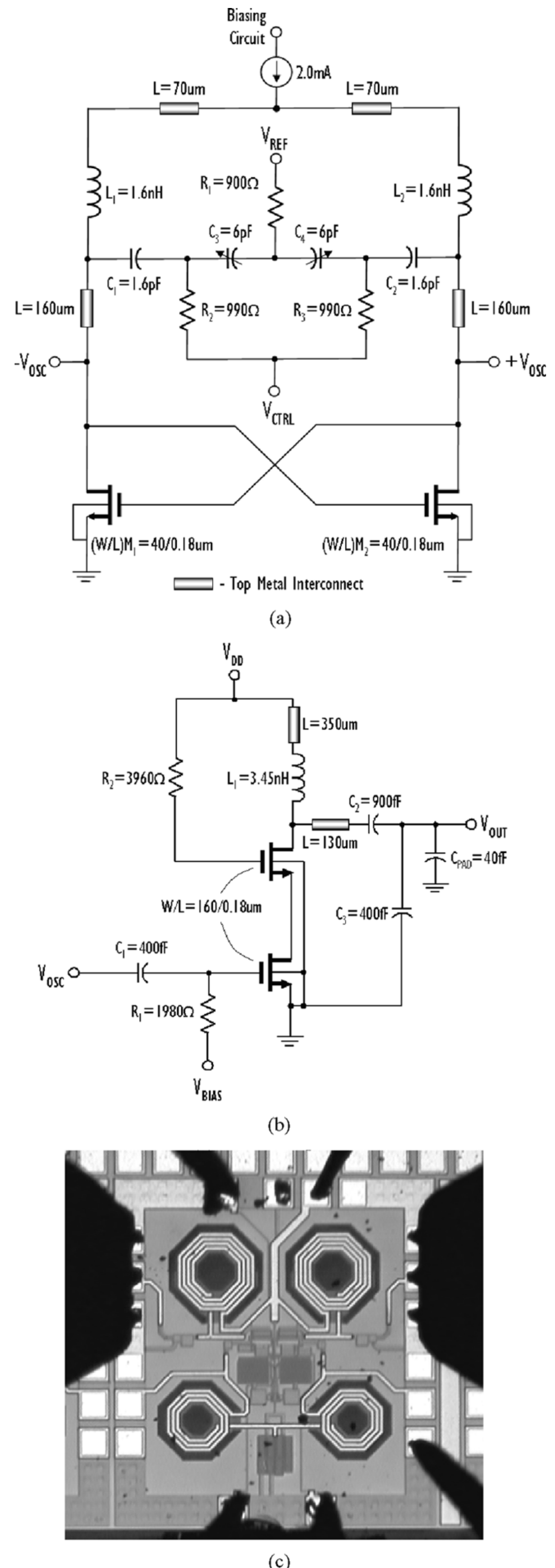

Fig. 17. Schematics (a), (b), and die photo (c) of a simple gigahertz voltage-controlled oscillator with interconnect width of 10 μm to verify the accuracy of the double-π RF interconnect model. (a) VCO. (b) Buffer amplifier. (c) VCO die photo.

isolation of the DC biasing from the RF oscillating signal is achieved using R_1, R_2, and R_3. Die photos capturing the VCO

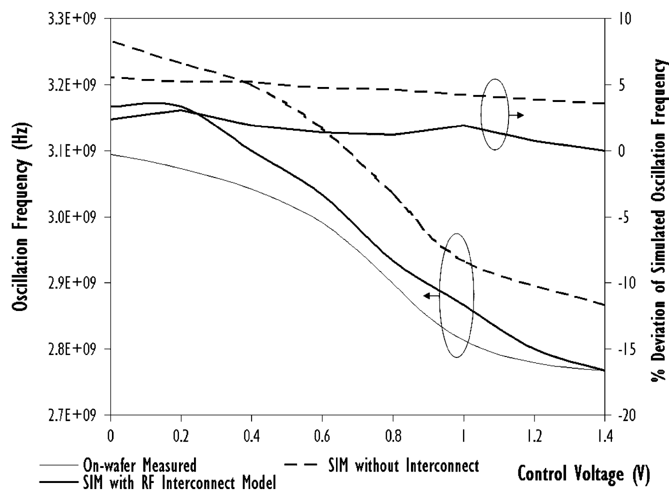

Fig. 18. Measured and simulated oscillation frequency versus control voltage for gigahertz voltage-controlled oscillator using double-π RF interconnect model.

with the RF and DC probes for on-wafer circuit characterization is shown in Fig. 17(c). The double-π interconnect model is used to perform a second VCO circuit simulation. With the RF interconnect model, the SPICE-simulated oscillation frequencies, with respect to the control voltages, have excellent associations with the on-wafer measured results. From Fig. 18, it is observed that the percentage error between the simulated and measured oscillating frequency for the VCO has improved from about 5.6% when interconnects are not considered to within 3 % when RF interconnect models are used, indicating excellent reliability of the proposed double-π RF interconnect model, even for circuit transient simulations.

VI. Conclusion

In this paper, RF interconnect test structures are designed, characterized, and modeled to predict their inductive, resistive characteristics, as well as substrate losses, at gigahertz frequencies. A new figure of merit, interconnect intrinsic factor I_F, proposed in this paper, provided a convenient quantitative indication as to how interconnects affect the performance of RFICs. The recommended SPICE-simulator-compatible double-π interconnect model accurately emulates the RF characteristics of metal lines, exhibiting continuity and scalability across physical dimensions of the interconnects. Circuit verifications using gigahertz amplifiers and VCO revealed that the RF interconnect model outperforms the conventional RC approach, achieving excellent correlations between SPICE-simulated and on-wafer measured circuit characteristics. This paper has demonstrated that it is possible to achieve cost-effective one-pass design success for silicon-based RFICs when accurate devices as well as interconnect SPICE models are adopted in RFIC design flows.

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