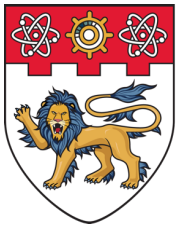
Studies on the Performance Bounds and Design of Current-Steering DACs



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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

2022

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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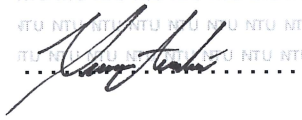

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Assoc Prof. Liter Siek

Authorship Attribution Statement

This thesis contains material from 4 papers published in the following peer-reviewed journal and conferences in which I am listed as an author.

Paper A is published as Oscar Morales Chacón, Jacob Wikner, Liter Siek and Atila Alvandpour. A 10-bit 3.75-GSps Binary-Weighted DAC with 58.6-pJ Energy Consumption in 65-nm CMOS. DOI: 0.1109/NorCAS51424.2020.9265003. The contributions of the co-authors are as follows:

- I worked on the idea formulation, design and physical implementation of the current-steering (CS) DAC. I also characterized the performance of the CS DAC and wrote the manuscript for publication, respectively.
- Prof Jacob Wikner participated in the edition of the manuscript, direction and supervision at Linkoping University (LiU).
- Prof Liter Siek participated in the direction and supervision at Nanyang Technological University (NTU) for the joint-PhD LiU-NTU programme.
- Prof Atila Alvandpour participated in the edition of the manuscript, direction and supervision at Linkoping University (LiU).

Paper B is published as Oscar Morales Chacón, Jacob Wikner, Christer Svensson, Liter Siek and Atila Alvandpour. Analysis of Energy Consumption Bounds in CMOS Current-Steering Digital-to-Analog Converters. DOI: 10.1007/s10470-022-02013-2. The contributions of the co-authors are as follows:

- I worked on the theoretical analysis with the mathematical formulations as well as the collection of the measurement results for validation. I also wrote the manuscript.
- Prof Jacob Wikner participated in the edition of the manuscript, direction and supervision at Linkoping University (LiU).
- Prof Christer Svensson participated in the direction at Linkoping University (LiU).
- Prof Liter Siek participated in the edition of the manuscript, direction and supervision at Nanyang Technological University (NTU) for the joint-PhD LiU-NTU programme.
- Prof Atila Alvandpour participated in the direction and supervision at Linkoping University (LiU).

Paper C is published as Oscar Morales Chacón, Jacob Wikner, Liter Siek and Atila Alvandpour. A digital switching scheme to reduce DAC glitches using code

dependent randomization. DOI: 10.1109/NorCAS53631.2021.9599651. The contributions of the co-authors are as follows:

- I worked on the idea formulation, software implementation and testing. I also wrote the manuscript.
- Prof Jacob Wikner participated in the edition of the manuscript, direction and supervision at Linkoping University (LiU).
- Prof Liter Siek participated in the edition of the manuscript, direction and supervision at Nanyang Technological University (NTU) for the joint-PhD LiU-NTU programme.
- Prof Atila Alvandpour participated in the direction and supervision at Linkoping University (LiU).

Paper D is published as Oscar Morales Chacón, Jacob Wikner, Liter Siek and Atila Alvandpour. Comparative analysis of CMOS latch-driver circuits for current-steering digital-to-analog converters. DOI: 10.23919/MIXDES55591.2022.9837990. The contributions of the co-authors are as follows:

- I worked on the idea formulation, physical implementation and testing. I also wrote the manuscript.
- Prof Jacob Wikner participated in the edition of the manuscript, direction and supervision at Linkoping University (LiU).
- Prof Liter Siek participated in the edition of the manuscript, direction and supervision at Nanyang Technological University (NTU) for the joint-PhD LiU-NTU programme.
- Prof Atila Alvandpour participated in the direction and supervision at Linkoping University (LiU).

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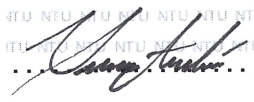

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Oscar Morales Chacón

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It has been a journey since I started off my PhD studies at Linkoping university back in 2017. During this time, I have had the opportunity to meet and work with people who have gave me inspiration, advise, encouragement and support along the way, and for those I would like to give my deepest and sincere gratitude

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Contents

Abstract

Digital-to-analog converters (DACs) are key building blocks in various applications including radar and wireless communications. With the exponential growth of data throughput in modern communication standards, e.g., fifth-generation (5G), DACs has been pushed to achieve direct frequency synthesis in the GHz-range with channel bandwidths preferably beyond 1 GHz. Yet, higher frequency synthesis results in augmented power consumption, which can significantly impact the wireless network if multiple DACs are utilized, e.g., in massive multiple-input and multiple-output (MIMO) antenna systems with digital beamforming as well as in end-user's handheld devices subject to a less prolonged battery life. Moreover, advances in digital signal processing and integrated-circuit fabrication, leading to reduced power consumption and cost as well as more flexibility in software-defined radio transmitters have motivated the displacement of analog/RF circuits to the digital domain. At the same time, driving the DACs to cover the millimeter-Wave (mm-Wave) spectrum, ranging between 30-300 GHz. In this work, high-speed DACs operating in the GHz-range with maintained low power consumption is addressed. The Nyquist-rate DAC is chosen due to its simple conversion approach to facilitate the generation of channel bandwidths in the GHz-range.

A 10-bit current-steering (CS) Nyquist DAC realized in 65-nm CMOS is presented. The design is intended for low-complexity and power consumption while targeting high-speed operation with over 1 GHz channel bandwidth and maintained linearity. The binary-weighted architecture is considered to achieve straightforward digital-to-analog conversion. Next, a theoretical analysis to obtain the energy consumption bounds in CS DACs is presented. The analysis considers the digital, mixed-signal and analog power domains as well as the design corners of noise, speed and linearity. This is validated from reported measurement results in published CS DACs implemented in CMOS technology. Furthermore, design considerations with enhancement techniques are addressed. A digital

switching scheme to avoid complementary switching transitions and counteract for timing errors is presented. The proposed scheme improves also the yield in linearity due to stochastic amplitude errors with reduced switching activity. Then, a comparative analysis of latch-drivers commonly implemented in CS DACs is realized. The comparison includes single- and dual-clocked latch-drivers and an alternative solution is proposed to reduce the switching-delay and power consumption.

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Acronyms

BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BW	Bandwidth
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Current-Steering
DAC	Digital-to-Analog Converter
DC	Direct Current
DEM	Dynamic Element Matching
DNL	Differential Non-linearity
DPD	Digital Pre-Distortion
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure-of-Merit
FRDEM	Full Randomization Dynamic Element Matching
FS	Full Scale
HBT	Hetero-junction Bipolar Transistor
HD	Harmonic Distortion
IM3/IMD3	Third-order Intermodulation Distortion
INL	Integral Non-linearity
LO	Local Oscillator
LSB	Least Significant Bit
MIMO	Multiple-Input Multiple-Output
MSB	Most Significant Bit
NMOS	N-channel Metal-Oxide-Semiconductor

NRZ	Non-Return-to-Zero
OSR	Oversampling Ratio
PMOS	P-channel Metal-Oxide-Semiconductor
PRDEM	Partial Randomization Dynamic Element Matching
PSD	Power Spectral Density
PVT	Process-Voltage-Temperature
RAM	Random Access Memory
RF	Radio Frequency
RZ	Return-to-Zero
SC	Switch Capacitor
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
TI	Time-Interleaved
THD	Total Harmonic Distortion

Chapter 1

Introduction

1.1 Motivation

Digital-to-analog converters (DACs) are essential building blocks in various applications. With the continuous demand on higher data throughput in modern wireless communications, high-speed DACs in radio transmitters have become of significant importance to generate the required channel bandwidths to satisfy the data rate requirements [1]–[3]. As an example, the fifth-generation (5G) communication standard as well as efforts to utilize the millimeter-Wave (mm-Wave) spectrum in the range of 30-300GHz, need carrier frequencies in the GHz range with multi-GHz channel bandwidths [4], [5]. Moreover, with the advent of the sixth-generation (6G), carrier frequencies are expected to reach the THz band with wider specifications in the channel bandwidth [6]. An immediate effect of increasing the sampling frequencies results in augmented power consumption, which motivates the employment of high-speed and energy-efficient DACs. This has special attention in end-users portable devices, where prolong battery-life along with high data throughput is required. Also, with the integration of massive antenna elements each driven by a separate DAC and operating at high-speed in multiple-input multiple-output (MIMO) antenna systems with digital beamforming can lead to a large power dissipation in the wireless network [7]. Therefore, power-savings in DACs with maintain high-speed operation can significantly contribute to the overall reduction in the power consumption in the radio network infrastructure as well as end-user's hand-held devices. Furthermore, the efficient

use of the radio frequency (RF) spectrum aims at the utilization of preferably orthogonal-frequency division multiplexing (OFDM) with high-order digital modulations schemes, e.g., 64- and 256-QAM. This requires high-performance DACs with high spectral purity within the signal bandwidth. However, non-idealities in physical DAC realizations force the integration of mainly calibration and error averaging circuits to improve the DAC's performance at the cost of increased area utilization and power consumption. Also, fundamental limitations such as quantization and thermal noise require to augment the power consumption to satisfy the specifications in signal-to-noise ratio (SNR) [8]. Also, power savings in the DAC design from a circuit and in architectural level become more important in modern and beyond radio transmitters with innovative and simple solutions. In this work a focus on the implementation of high-speed energy-efficient DACs is presented along with an analysis in the energy bounds that limit the reduction of energy consumption to achieve certain design performance metrics in current-steering (CS) DACs.

Background

From prior wireless communications standards (1G-4G) to today's 5G, DACs have also evolved alongside to achieve direct frequency synthesis with larger bandwidth and reduced power consumption. Reported DAC designs include implementations in complementary metal-oxide-semiconductor (CMOS), bipolar CMOS (BiCMOS) and hetero-junction bipolar transistor (HBT) technologies. Realizations in BiCMOS has been explored, reporting multi-GHz sampling frequencies at the cost of significant increase in power consumption. However, CMOS technology has become the preferred option to obtain energy-efficient DACs due to the continuous device scaling, leading to lower power consumption and faster switching transitions. On the other hand, large levels of integration and reduced cost per device motive even more the utilization of CMOS process nodes. Besides, to attain high-speed digital-to-analog conversion, the CS DACs have been largely implemented with respect to other DAC topologies. To exemplify, the energy consumption versus year of publication for CS DACs designed in different technologies over the past 25 years is presented in Fig. 1.1[9], where it is observed that the energy consumption has been declining with time. Al-

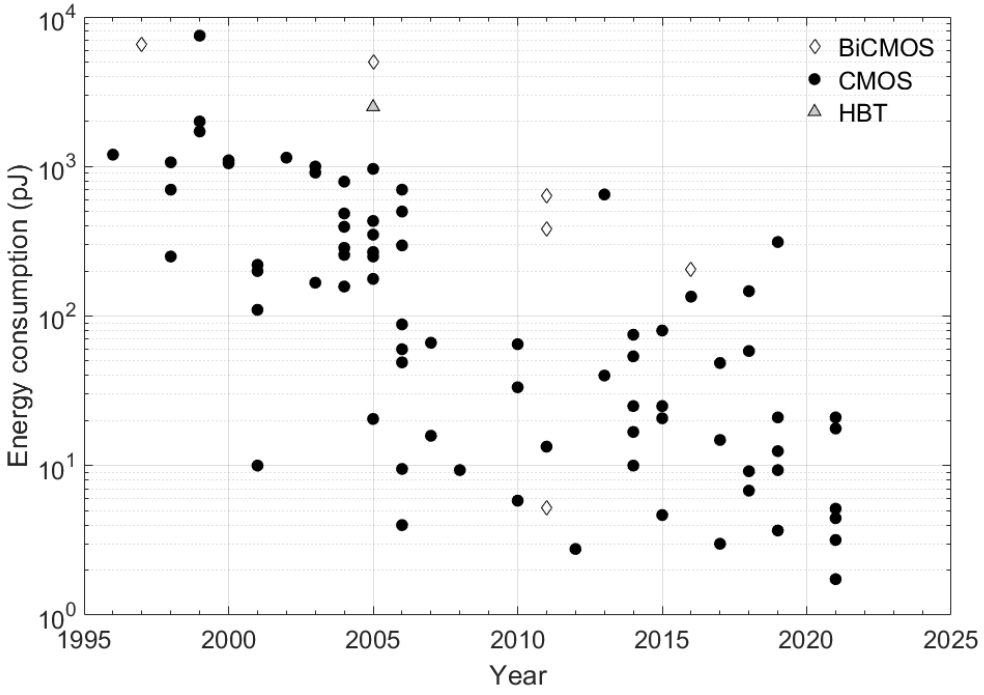

Figure 1.1: Energy consumption versus publication's year of current-steering (CS) DACs implemented in CMOS, BiCMOS and HBT technologies [9].

ternatively, hybrid DAC topologies and architectures have been proposed for high-speed, e.g., resistive R-2R ladder with CS DACs as well as the integration of both Nyquist and $\Sigma\Delta$ DACs to balance between sampling speed and resolution [10], [11]. On the other hand, improvements in CS DAC's performance have come at a cost of increased power consumption and complexity in the design. The solutions to counteract for the performance degradation mainly include error calibration and randomization techniques, with special focus on amplitude errors. Moreover, with augmented sampling frequencies, timing issues become more prominent, degrading the DAC's performance more rapidly. Yet, Nyquist CS DACs have prevailed to maximize the channel bandwidth and satisfy for the demands of high-speed applications.

1.2 Research methodology

The adopted research methodology is classified as applied research [12]. Practical and theoretical problems are addressed towards a feasible implementation.

Relevant issues in the field of CS DAC are considered and practical solutions are proposed. The research is initiated with literature review. Thereafter, with the aim of exploring high-speed operation and low-power consumption in DACs, the binary-weighted CS DAC architecture is chosen for the study. High-level modeling followed with schematic and the physical level design in computer aided design (CAD) tools is carried out. Utilization of industrial 28-nm and 65-nm CMOS processes is considered with the implementation in the latter due to a more suitable lead-time for tape-out. In addition, modeling and theoretical analysis are utilized to identify and understand the relation between the design variables, e.g., formulation that lead to minimum energy consumption in CS DACs and other proposed solutions to reduce power consumption with attained high-speed operation.

Societal aspects

From the first intercontinental radio transmission in 1901 to the deployment of a radio infrastructure in the 1970s and continuing today with advance wireless communications standards, the radio systems have been subject of continuous development to improve signal quality, reduce latency and increase data throughput. This has had a large impact on society with multi-user connectivity between people and software platforms by easing fast communications within long distances. DACs as essential blocks in radio systems and other applications are required to satisfy the communication demands with special focus on energy efficient realizations. As the tendency of higher-speed communications with more connectivity [13], e.g., internet-of-things (IoT) and massive multiple-input multiple-output (MIMO) in modern radio systems and beyond mm-Wave, reduction in power consumption has gained more attention as this impacts the overall power consumption in say the radio network infrastructure and in the end-user handheld devices.

Ethical aspects

The application of ethical aspects during the conduction of the research activity is essential so that it can serve as a platform for further study within the research community and industry. The ethical aspects considered the practice principles of the European Code of Conduct for Research Integrity, including, reliability, honesty, respect and accountability [14]. Moreover, the Swedish Research Council (Vetenskapsrådet) has provided guidelines for a good research practice, which have been also consulted for further guidance [15].

Source criticism

The source criticism consists of evaluating the source of information subject to provide knowledge under a basis of credibility and usefulness [16]. In the present work, peer-reviewed international conferences and recognized journals publications from university and companies are utilized as the platform for investigation, including also books, for comparison and assessment of the different solutions and methods in the area of data converters with main focus on CS DACs. The sources encompass from state-of-the-art to more conventional CS DACs implementations.

1.3 Major contributions of the Thesis

The research work has been focused on high-speed and low-power CS DACs for wideband wireless communications. A test chip of a binary-weighted CS DAC was design and sent for manufacturing in 65nm CMOS process. The design is aimed to achieve a signal bandwidth over 1 GHz with reduced complexity and a favorable trade-off between power consumption, speed and linearity. Further, a theoretical analysis to obtain the energy bounds, considering the fundamental limitations of noise, speed and linearity in CS DACs is realized. The analysis also extends to address other design considerations for low-power consumption and it is validated from reported measurements in published CS DACs in CMOS technology. Moreover, aspects of design considerations to strive for high-speed

operation with reduced power consumption are addressed. A digital switching scheme to avoid complementary switching transitions, leading to faster settling times and lower power consumption as well as counteracting for the effects of timing errors in CS DACs is proposed. In addition, a comparative analysis of conventional static CMOS latch-drivers commonly implemented in CS DACs is presented. The comparison includes single- and dual-clocked latch-drivers and an alternate latch-driver is proposed to further reduce the switching transitions and the power consumption in CS DACs.

Moreover, the publication [17] was carried out during the PhD studies. However, this is not included in the dissertation as it is out of the scope of work.

1.4 Organization of the Thesis

This thesis is organized as follows: In **Chapter. 2** an overview of DACs is presented, considering signal processing aspects as well as DAC categories and circuit implementations. A performance comparison is also included for DAC realizations in CMOS, BiCMOS and HBT technologies. Then, **Chapter. 3** treats in more detail the CS DAC, including fundamental performance limitations and power consumption bounds. Moreover, design considerations in CS DACs regarding high-speed operation, low-power consumption and high-performance are addressed. Next, the design and characterization of a 10-bit high-speed binary-weighted CS DAC implemented in 65 nm CMOS process is presented in **Chapter. 4**. Finally, **Chapter. 5** concludes the thesis.

Chapter 2

Overview of digital-to-analog converters

Digital-to-analog converters (DAC) have kept evolving towards high-speed and low-power solutions with maintained performance. An overview of DACs is initially presented considering aspects of signal processing, architectures, circuit topologies along with a performance comparison in different technologies, including CMOS, BiCMOS and HBT.

2.1 Signal processing aspects

The reconstructed analog output, $\hat{y}(t)$, from the digital-to-analog conversion process for a sampling period, T_s, and the time instance, n, is given by [18]

$$\hat{y}(t) = \sum_{n=-\infty}^{\infty} x(nT_s)h(t - nT_s), \tag{2.1}$$

with $x(nT_s)$ the discrete-time sampled amplitude and mapped to a digital word, $X = [b_N, ..., b_0]$, with $b_i \in [0, 1]$, N the word length and $h(t)$ the impulse response, where for a zero-order hold, $h(t)$ is defined by

$$h(t) \triangleq \begin{cases} 1, & 0 \leq t \leq T_s \\ 0, & \text{otherwise.} \end{cases} \tag{2.2}$$

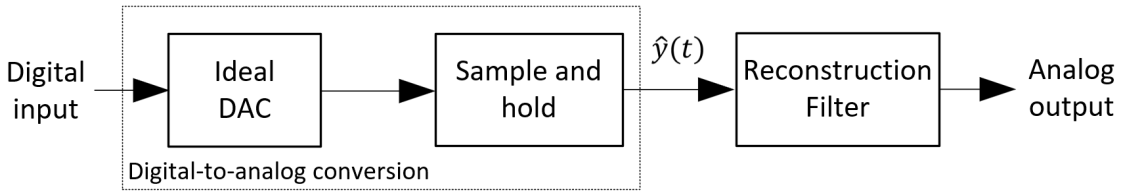

Figure 2.1: Digital-to-analog conversion [19].

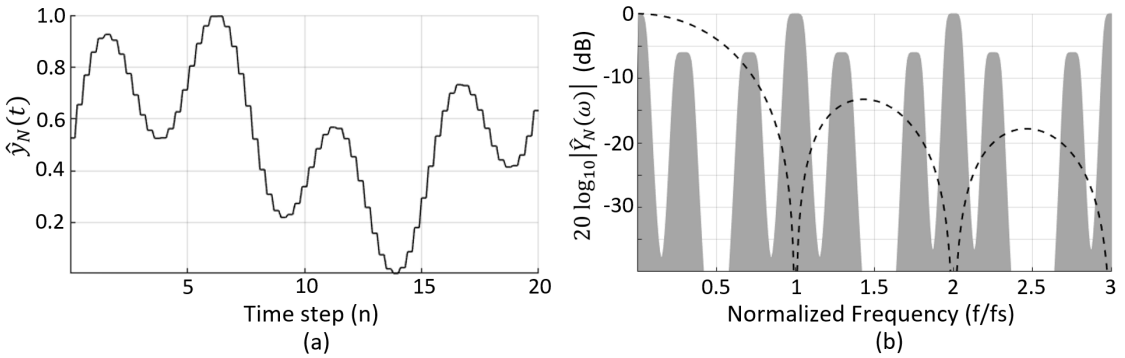

Figure 2.2: Normalized arbitrary signal $\hat{y}_N(t)$ (a) time-domain (b) frequency-domain response.

For an input sequence $x(t) = \sum_{n=-\infty}^{\infty} x_{in}(t)\delta(t - nT_s)$, $\hat{y}(t) = x(t) \circledast h(t)$ with $\delta(t)$ the Dirac's delta function and $\circledast$ the convolution operand. Thus, the Fourier transform of $\hat{y}(t)$ is $\mathfrak{F}\{\sum_{n=-\infty}^{\infty} x_{in}(t)\delta(t - nT_s)\}H(\omega)$, where

$$\begin{aligned}\mathfrak{F}\left\{\sum_{n=-\infty}^{\infty} x_{in}(t)\delta(t - nT_s)\right\} &= \frac{1}{2\pi}X(\omega) \circledast \left[\omega_s \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_s)\right] \\ &= \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X(\omega - k\omega_s),\end{aligned} \tag{2.3}$$

with $\omega_s = 2\pi f_s$ and $f_s = 1/T_s$. For $H(\omega)$, considering $T \leq T_s$, we get

$$H(\omega) = \int_{-T/2}^{T/2} h(t)e^{-j\omega t}dt \; = T\left[\frac{\sin(T\omega/2)}{T\omega/2}\right]e^{-jT\omega/2}. \tag{2.4}$$

From (2.3) and (2.4), we obtain for $\mathfrak{F}\{\hat{y}(t)\} = \hat{Y}(\omega)$ as

$$\hat{Y}(\omega) = \alpha \,\text{sinc}(T\omega/2) \sum_{k=-\infty}^{\infty} X(\omega - k\omega_s)e^{-jT\omega/2}, \tag{2.5}$$

where $\alpha = T/T_s$ and $\text{sinc}(T\omega/2) = \frac{\sin(T\omega/2)}{T\omega/2}$. From (2.5), replicas of $X(\omega)$ are

also present at multiples of f_s with α sinc$(T\omega/2)$ as the envelope. A block diagram of the digital-to-analog conversion process is presented in Fig. 2.1. The reconstruction filter is used to remove the signal replicas beyond the Nyquist bandwidth, $f_s/2$. To illustrate, in Fig. 2.2 an arbitrary signal, $\hat{y}_N(t)$, is presented in both time-domain and frequency-domain with a normalized magnitude response.

Return-to-Zero

In (2.5), if $\alpha < 1$, then $x(nT_s)$ holds its amplitude for a time duration less than T_s and then it is set to 0 within the time interval, $\Delta T = n(T_s - T)$. Thus referring this technique to as return-to-zero (RZ). In Fig. 2.3(a), the time-domain response of an arbitrary waveform whose output is set to zero after a time duration T is presented. Also, the response in the frequency-domain of the envelope α sinc$(T\omega/2)$ for different α values is shown in Fig. 2.3(b). Notice that for $\alpha < 1$, a flatter amplitude response over the signal bandwidth is obtained with the nulls translated to frequencies higher than f_s.

Mixing-Mode

Alternatively, if for each sample the amplitude changes its sign after $nT_s/2$, this is referred to as mixing-mode. In Fig. 2.4(a) this is illustrated for an arbitrary waveform. Hence, a larger magnitude response in the frequency-domain with respect to (2.5) at multiples of $(2m+1)f_s$ for $m \in \mathbb{Z}_0^+$ is obtained. For each sample in the time interval $T_s(n-1) \leq t \leq T_s(n-1/2)$, the impulse response $h(t)$ applies. Yet, for the sample in the time interval $T_s(n-1/2) < t \leq nT_s$ a time-shift, τ, in the impulse response needs to be considered. This translates into a phase-shift in the frequency-domain as

$$H^*(\omega) = H(\omega)e^{-j\omega\tau}. \tag{2.6}$$

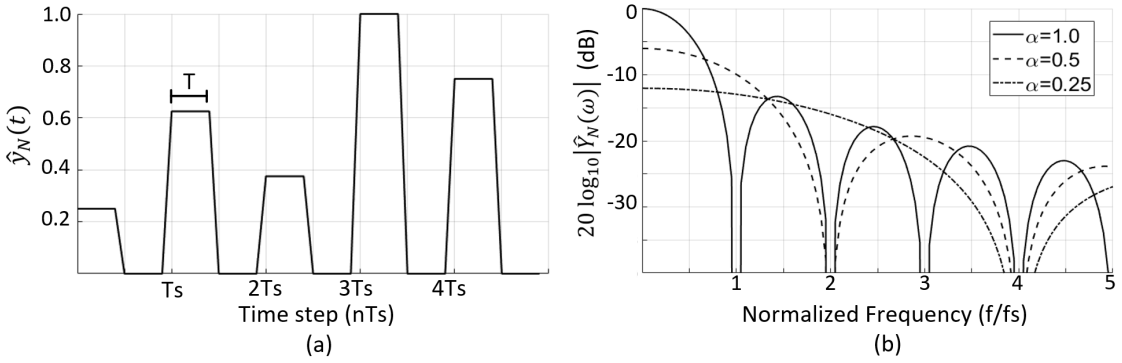

Figure 2.3: Return-to-zero (a) time-domain (b) frequency-domain response.

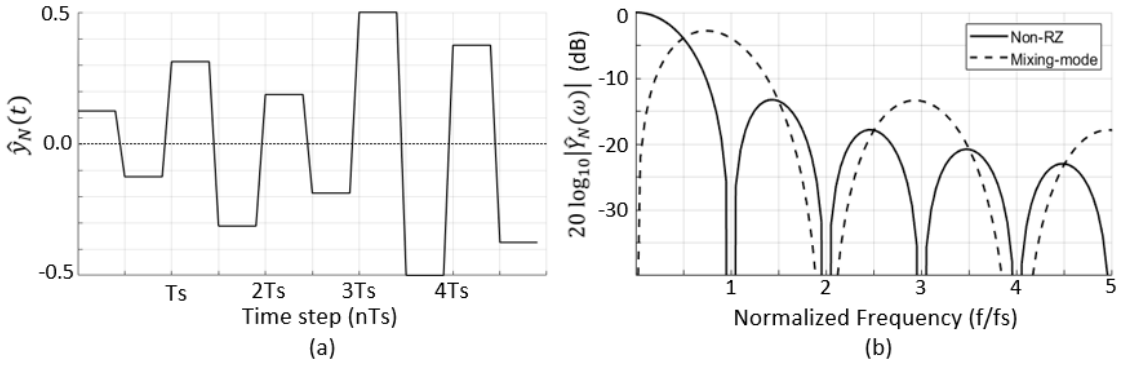

Figure 2.4: Mixing-mode (a) time-domain (b) frequency-domain response.

The superposition of the signed signals in the frequency-domain expressed as $\hat{Y}(\omega) = \hat{Y}^+(\omega) + \hat{Y}^-(\omega)$ yields

$$\begin{aligned}\hat{Y}(\omega) &= \alpha\ \text{sinc}(T\omega/2)e^{-jT\omega/2}\sum_{k=-\infty}^{\infty} X(\omega - k\omega_s)(1 - e^{-j\omega\tau}) \\ &= \alpha\ \text{sinc}(T\omega/2)e^{-jT\omega/2}\sum_{k=-\infty}^{\infty} X(\omega - k\omega_s)\left(1 + e^{-j(\pi+\omega\tau)}\right).\end{aligned} \tag{2.7}$$

Since $2e^{j\theta}\cos\theta = 1 + e^{2j\theta}$, then $\theta = -(\pi + \omega\tau)/2$. Also, $\tau = T$, thus

$$\hat{Y}(\omega) = 2\alpha\ \text{sinc}(T\omega/2)\cos\left((\pi + T\omega)/2\right)e^{-j(\pi/2+T\omega)}\sum_{k=-\infty}^{\infty} X(\omega - k\omega_s). \tag{2.8}$$

In Fig. 2.4(b), the frequency response from (2.5), which is referred to as non-RZ (NRZ), and the mixing-mode from (2.8) with $T = \tau$ are shown. Notice that the utilization of mixing-mode enables direct frequency synthesis at higher frequency bands since no attenuation at $(2m + 1)f_s$ is obtained.

Quantization Error

The reconstruction of the analog signal, $\hat{y}(t)$, is also determined by the DAC's full-scale (FS) signal and the number of quantization steps, M, with the quantization step given by Δ = FS/M. However, the finite number of quantization steps result in a quantization error, e_q. For a large number M uniformly distributed and excited with equal probability and without correlation with the input signal, e_q can be represented as white-noise [20]. The average power of e_q derived for a single-tone signal is $P_{n,q} = \Delta^2/12$ and represents a fundamental performance limitation [21]. For a FS single-tone with an average power given by $P_{sig} = (2^N\Delta)^2/8$, the signal-to-noise ratio (SNR) of an N-bit DAC is given by

$$\text{SNR} = \frac{(2^N\Delta)^2/8}{\Delta^2/12} = \frac{3}{2}2^{2N}. \tag{2.9}$$

Moreover, (2.9) can be extended if the signal bandwidth, f_{sig}, and f_s satisfy the condition $f_s > 2f_{sig}$. This is referred to as oversampling and the SNR then can be expressed in dB as

$$\text{SNR}_{\text{dB}} = 6.02N + 1.76 + 10\log\left(\frac{f_s}{2f_{sig}}\right)\ \text{dB}, \tag{2.10}$$

with $f_s/2f_{sig}$ known as the oversampling ratio (OSR).

Digital encoding

Binary-weighted

The digital-to-analog conversion is simply realized through an N-bit binary-weighted digital word $X = [b_{N-1}, \ldots, b_0]$ with $b_i \in [0, 1]$. Here, each b_i disables or enables an analog unit with a weight scaled by 2^i in the DAC. Thus, a time-discrete analog output, $x(nT_s)$, is expressed as

$$x(nT_s) = \sum_{i=0}^{N-1} 2^i b_i(nT_s), \tag{2.11}$$

This is a straightforward conversion approach with no added decoding logic. Yet, mismatch in the binary-weighted analog units compromises the DAC's performance in physical implementations. Moreover, mid-code bit transitions between the most-significant-bit (MSB) and least-significant-bits (LSBs) can induce large glitches and switching activity. This is represented for a 4-bit word and the transition from 1000 to 0111 with the simultaneous conversion between the MSB and LSBs.

Thermometer-coded

On the other hand, to avoid the mid-code bit transitions and minimize the switching activity, the thermometer-coded representation of the digital signal is the option to consider. Thus, the necessary number of analog units of equal size, unary-weighted, between adjacent word transitions are enabled or disabled, which is given by

$$\Delta(nT_s) = \left\| \sum_{i=0}^{N-1} 2^i b_i(nT_s) - \sum_{i=0}^{N-1} 2^i b_i\left((n-1)T_s\right) \right\|. \tag{2.12}$$

In addition, better accuracy can be achieved as the analog units are of equal size. Naturally, a thermometer decoder is required to generate the digital word with a length equal to $2^N - 1$ and whose complexity grows exponentially, thus compromising its realization.

Decomposition

An alternative solution is known as decomposition [22]. In this case, for an N-bit digital word, the MSB and LSBs are decomposed in a pair of reduced N-1 binary-weighted bit lines and a single line for the LSB. The encoder generates replicas of the MSB that control N-1 binary-weighted bit lines, whereas the LSBs control the remaining ones. Thus, during a mid-code bit transition, the MSB and LSBs exchange their control between the binary-weighted bit pairs so that no change is observed at the output. An example of a 2-layer decomposition is illustrated in Fig. 2.5.

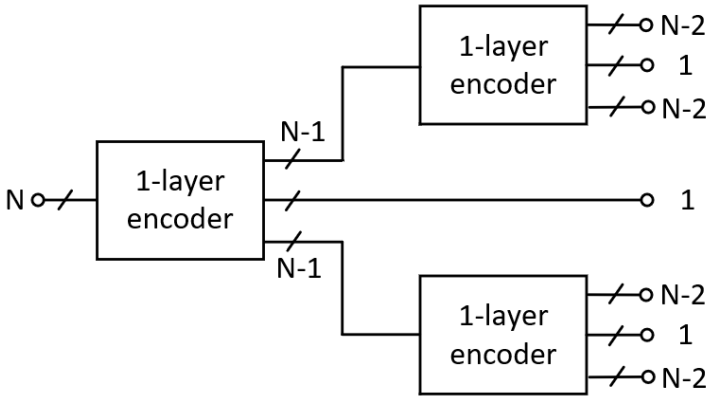

Figure 2.5: Example of a 2-layer decomposition.

2.2 Categories

Nyquist-rate

The Nyquist-rate DAC synthesizes an analog output directly from the digital input sequence for a signal bandwidth $f_s/2$ with f_s the sampling frequency as presented in Section 2.2. The digital-to-analog conversion process is also presented in Fig. 2.1. Further on, with $\alpha = 1$ in (2.5), the envelope response at $f_{sig} = f_s/2$ drops to $2/\pi$ in magnitude, which results in an attenuation of about 3.9 dB in the output signal.

Interpolation

The interpolation DAC is presented in Fig. 2.6 [23]. It integrates and up-sampling stage and interpolation filter. The digital input sequence, $X(n)$, is interpolated to achieve a sampling rate of If_s with $I \in \mathbb{N}$ and $I > 1$. The output of the up-sampling stage, $X_I(m)$ equals $X(m/I)$ if $m = 0, \pm I, \pm 2I, ...$, otherwise, it becomes 0. Thereafter, $X_I(n)$ is filtered out to remove the signal replicas in the frequency-domain, $X_I^F(m)$. This results in a flatter envelope response over the signal bandwidth with the envelope's nulls translated at frequencies above f_s, thus relaxing the design requirements in the reconstruction filter.

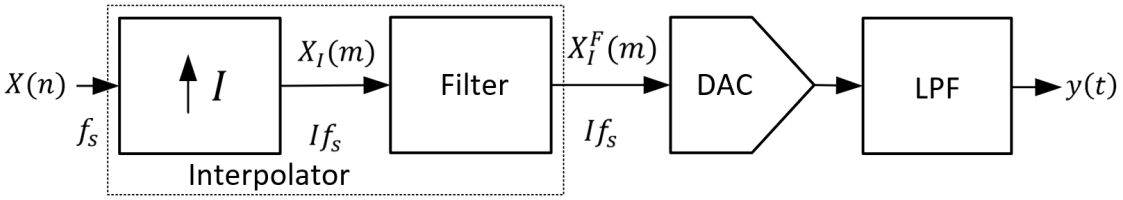

Figure 2.6: Block diagram of the interpolation DAC.

Delta-Sigma ($\Delta\Sigma$)

The $\Delta\Sigma$ DAC exploits the utilization of oversampling with the integration of $\Delta\Sigma$ modulators to shape the quantization noise and translate it out of the signal bandwidth. Also, if a trade-off between the number of input bits and the SNR is considered, this facilitates the DAC's realization with a reduced bit resolution, M, for $M < N$ without compromising the SNR in the signal bandwidth [24]. This results in a DAC implementation with reduced analog circuitry[1]. A simplified block diagram of the $\Delta\Sigma$ DAC is illustrated in Fig. 2.7. The $\Delta\Sigma$ modulators are known as noise-shaping modulators and conventional implementations include signal- and error-feedback, where the quantization noise shaping depends on the $\Delta\Sigma$ modulator and its order. On the other hand, the utilization of oversampling has represented a challenge in high-speed applications such as wireless communications, however, they have been extensively used in audio and video applications. Nevertheless, realizations in CMOS and BiCMOS aimed to operate at high-speed have been reported [10], [26].

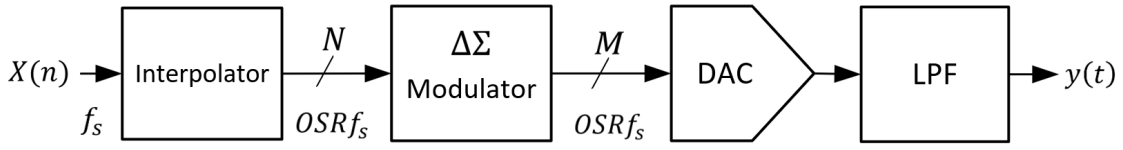

Figure 2.7: Block diagram of the $\Delta\Sigma$ DAC.

[1] With intrinsic benefit in reduced power consumption requirements [25].

Radio-frequency (RF)

With the introduction of digital front-end in radios [27]–[29], offering more flexibility in the configuration, e.g., the use of a large cellular bands' range with the same architecture as well as facilitating error correction have motivated direct-RF frequency synthesis in modern wireless transmitters. Essentially, more of the RF-analog circuitry and signal processing is displaced into the digital domain. DAC realizations with the integration of the mixer stage or its displacement into the digital domain of the transmitter chain have been commonly referred to as RF DACs [30]–[33]. The former translates the channel bandwidth with a carrier frequency, f_c, whereas the latter exploits the use of the first Nyquist zone for a large signal bandwidth, e.g., $\geq$ 1 GHz or higher Nyquist zones through the utilization of signal processing techniques as presented in Section 2.2. To exemplify, a simplified block diagram of a transmitter chain with the utilization of digital intermediate frequency (IF) upconversion in the I/Q channels and the RF DAC with a local oscillator frequency, f_{osc}, for the mixing operation is presented in Fig. 2.8. The RF DAC removes mixers in the RF domain, simplifying the RF transmitter design with only a bandpass filter (BPF) and the power amplifier (PA). Also, imbalance in the I/Q channels can be corrected digitally. Yet, as mentioned, this requires the RF DAC to achieve direct-RF frequency synthesis, which represents a design challenge, specially at multi-GHz carrier frequencies.

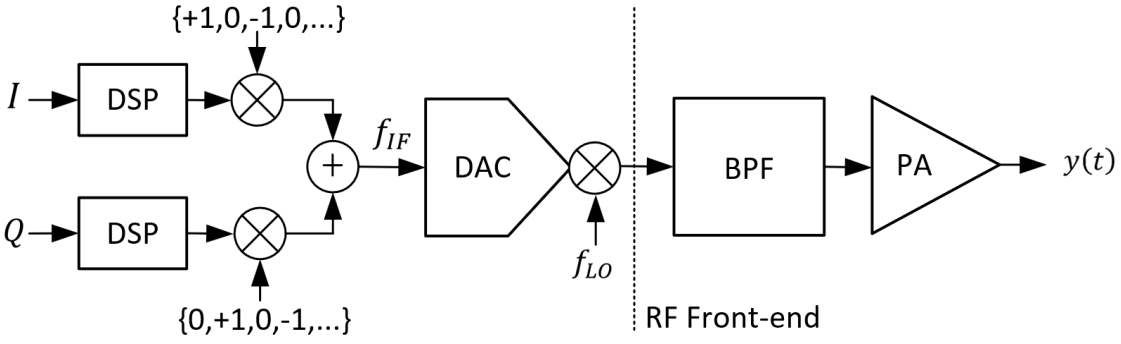

Figure 2.8: Utilization of an RF DAC in a transmitter chain.

2.3 Circuit topologies

Resistor-based

The resistor-based DAC topologies include the R-2R ladder, string voltage-divider and binary-weighted resistive array. The R-2R ladder resistive DAC exploits the intrinsic property to generate an scale binary-weighed analog output from a linear resistive network, making this solution attractive for its simplicity and implementation with either a reference voltage, Vref, (voltage-mode) or current, Iref, (current-mode). For the string voltage-divider, the complexity grows exponentially with the number of bits as this requires an switching network to select the output voltage from the voltage divider. Fig. 2.9 shows the circuit schematics for both solutions with the R-2R ladder DAC operating in current-mode. Naturally, matching in the resistant values are essential to maintain accuracy in the analog output. However, intrinsic parasitic capacitances in physical implementations lead to time constants that can limit the conversion speed with added distortion.

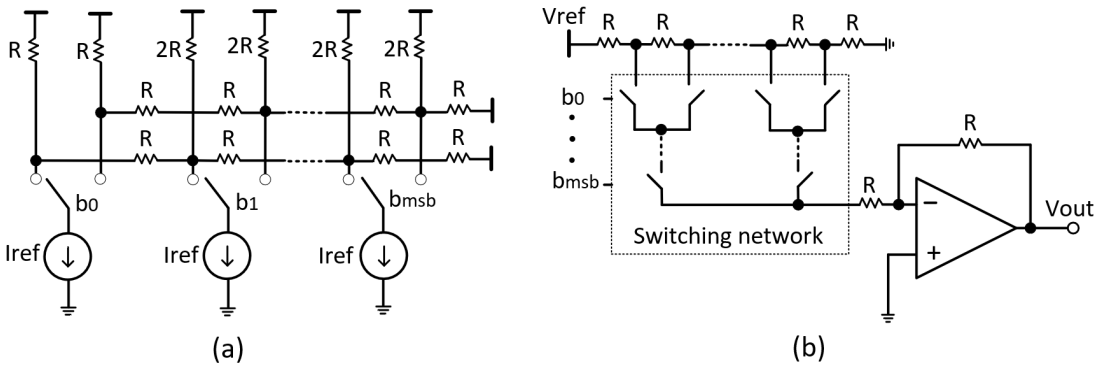

Figure 2.9: Resistor-based DAC (a) R-2R ladder (b) string voltage-divider.

Capacitive-based

The capacitor-based DACs operate under the capacitive divider principle to redistribute the charge and generate the analog output. The re-utilization of the charge during the conversion process leads to low-power solution. However,

weak driving capability of the capacitive DAC and potential charge leakage require the utilization of an output driver. A conventional closed-loop driver with negative feedback to mitigate for the non-linearity in the driver results in limited bandwidth. Alternatively, open-loop solutions have also been proposed at the cost of added complexity to compensate for the output driver's nonlinear response [34], [35]. Common capacitive DAC implementations for the charge-redistribution and switch-capacitor are presented in Fig. 2.10. The charge redis-

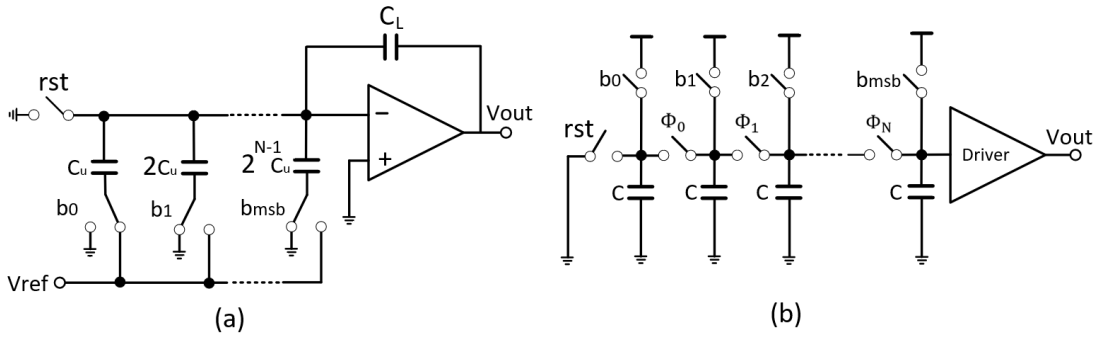

Figure 2.10: Capacitor-based DAC (a) charge-redistribution (b) switch-capacitor.

tribution DAC in Fig. 2.10(a) utilizes a binary-weighted capacitive array with C_u as the minimum capacitance. Despite its simplicity, mismatch in the scaled capacitances in practical applications can constrain its utilization in above moderate DAC resolutions in say 8-bit and more. On the other hand, the switch-capacitor in Fig. 2.10(b) utilizes multiple clock phases to redistribute the charge so that the charge stored in each capacitor C is bisected during the conversion process. Moreover, as the capacitors are of equal size, it leads to better matching properties and the complexity increases linearly with the DAC's resolution, N. However, it requires to add more clock phases, which compromises the conversion speed. To alleviate this issue, pipeline switch-capacitor DACs have been also proposed to reduce the number of clock phases [34], [36].

Current-Steering

The operation of the current-steering (CS) DAC is based on the superposition of current sources at the output node to generate the analog signal. The contribution of each current source is assigned separately through a weighting factor, which for a binary-weighted implementation it scales by $2^n I_{ref}$ with n the subindex of the control bit, b_n. For this purpose, switches controlled by the digital input word are utilized to set or disrupt the path of the current to the output. A simplified circuit schematic of a conventional binary-weighted CS DAC with differential output is illustrated in Fig. 2.11. Since the current is rapidly added after the switching transition, the CS DAC offers a fast conversion speed with intrinsic driving capability, thus making this solution suitable for high-speed applications. The CS DAC is the focus of this work and will be presented in more detail in the next chapter.

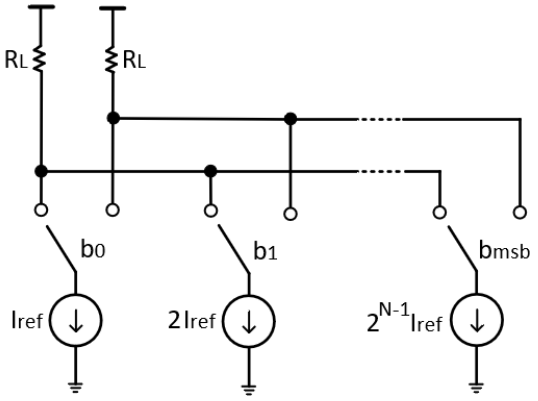

Figure 2.11: Current-steering DAC.

2.4 Performance Metrics

Static Performance

The static performance of a DAC is determined from the DC transfer function by considering devations from the ideal response in the form of gain and offset errors as well as nonlinear input-output characteristics [19], which can be also classified as linear and nonlinear errors, respectively. The latter that determines

the monotonicity of the DAC include the differential non-linearity (DNL) and integral non-linearity (INL), and methods to obtain both are the end-point and the best-fit approximation [37]. The DNL and INL are defined as

$$\text{DNL}(k) = \frac{A_k - A_{k-1}}{\alpha\Delta}, \tag{2.13}$$

and

$$\text{INL}(k) = \sum_{k=0}^{2^N-1} \text{DNL}(k), \tag{2.14}$$

where $A_k - A_{k-1}$ is the amplitude difference between adjacent bit codes with the sub-index k, Δ the ideal step difference and α the scaling factor with $\alpha = 1$ for the end-point method and $\alpha \neq 1$ for the best-fit approximation. Furthermore, to guarantee monotonicity is required that $|\text{DNL}_k| \leq 1$ LSB and $|\text{INL}_k| \leq 0.5$ LSB for $k \in [0, 2^{\text{N}-1}]$ [37], [38].

Dynamic Performance

Harmonic Distortion (HD): For a single-tone signal, the generation of distortion tones located at multiples of the fundamental frequency is referred to harmonic distortion (HD). In dB, this is calculated by

$$\text{HD}_k = 10\log_{10}\frac{PH_k}{P_{sig}}, \tag{2.15}$$

where PH_k and P_{sig} is the average power of the harmonic-k and the signal with k as an integer number. Moreover, the power contribution from the harmonics over P_{sig} is known as total HD (THD) and is expressed as

$$\text{THD} = \frac{\sum_{k=2}^{\infty} PH_k}{P_{sig}}. \tag{2.16}$$

Signal-to-noise ratio (SNR): This is defined as the ratio between the input signal, P_{sig}, and noise, P_{noise}, average power in a channel bandwidth, BW. In dB, this is given by

$$\text{SNR} = 10\log_{10}\frac{P_{sig}}{P_{noise}}. \tag{2.17}$$

Signal-to-noise and distortion ratio (SNDR): This is defined as the ratio between the average power of the input signal, P_{sig}, and noise, P_{noise}, plus HD in a channel bandwidth, BW. In dB, this is given by

$$\text{SNDR} = 10\log_{10}\frac{P_{sig}}{P_{noise} + \sum_{k=2}^{\infty} PH_k}. \tag{2.18}$$

Spurious-free dynamic range (SFDR): This is defined as the ratio between the input signal, P_{sig}, and the strongest spur or distortion component average power in a channel bandwidth, BW. In dB, the SFDR is given by

$$\text{SFDR} = 10\log_{10}\frac{P_{sig}}{\text{max}[P_{spur}]}. \tag{2.19}$$

Intermodulation Distortion (IMD): For a dual- or multi-tone input signal, the emergence of non-harmonic tones at the output is referred to as intermodulation distortion (IMD). This is calculated from the ratio between the distortion tone of an specific nonlinear order, k, P_{IMD_k}, over the signal power, P_{sig}, of the fundamental tone, expressed in dB by

$$\text{IMD}_k = -10\log_{10}\frac{P_{sig}}{P_{\text{IMD}_k}}. \tag{2.20}$$

In a dual-tone signal with frequencies f_1, f_2 and $f_1 \neq f_2$, the distortion terms appear at $f_{k,1,2} = m_1 f_1 + m_2 f_2$ with $m_{1,2}$ as integer numbers from a polynomial expansion [39]. Similar analysis can be applied to the multi-tone case.

2.5 Comparison of high-speed DACs

A comparison of high-speed DACs implemented in CMOS, BiCMOS and HBT technologies are presented next. Table. **??** lists a selected group of published DACs with their design characteristics and performance metrics, including the sampling frequency, f_c, signal bandwidth, BW, maximum output frequency, f_{out}, power consumption and SFDR. While BW can vary in oversampling DACs, e.g, in $\Delta\Sigma$ DACs, f_{out} can be larger from $f_s/2$ in say RF DACs with the integration of the upconversion mixer or if signal processing techniques are utilized. Also, due to the importance of maintaining linearity as the signal frequency increases, the SFDR reported is at f_{out}. From Table. **??**, notice that the switch-capacitor (SC) DACs report an f_s below 1 GHz [34], [36], except in [35], which reaches a BW of 2.5 GHz. Moreover, the sub-nm CMOS CS DACs report an f_s in the GHz-range, reaching up to 100 GHz in [40]. Other implementations report a f_s larger than 3 GHz, thus demonstrating the feasibility to obtain a channel bandwidth over 1 GHz with CS DACs. In addition, the utilization of time-interleaved (TI) has resulted in multi-GHz channel bandwidths in Nyquist DACs as demonstrated in [41], [42], where its employment has been also explored in $\Delta\Sigma$ DACs to augment the channel bandwidth in combination with reduced analog complexity that favors the dynamic performance at high-speed operation [26]. On the other hand, BiCMOS and HBT DAC realizations report an f_s over 1 GHz, but with a significant increase in power consumption. The high transit frequency, f_T, in BiCMOS and HBT technologies permits to achieve higher switching speeds that facilitates the utilization of signal processing techniques with f_s in the GHz-range, thus utilizing the signal replicas at higher Nyquist zones. For instance, this is reported in [43], where for an f_s of 2.7 GHz and with the utilization of RZ, f_{out} reaches up to 10 GHz. Similarly, in [10] a f_{out} of 20 GHz is obtained when operating with an f_s of 3.35 GHz. Yet, f_{out} close to f_s have been reported in CMOS CS DACs with the utilization of the mixing-mode technique [30],[44]. Moreover, the SFDR versus f_s is presented in Fig. 2.12. Note that the DACs achieve an SFDR $\geq$ 40 dBc up to 10 GHz, except for [35]. Thereafter, the SFDR drops rapidly, reaching up to 25 dBc [40], which is attributed due to the mid- and low-resolution DACs implementations at $f_s >$ 10 GHz as well as fast linearity degradation with larger BW. Also, the SFDR versus f_{out} is presented in Fig. 2.13. Here, the data points are mainly shifted to the origin. However, special cases correspond to the $\Delta\Sigma$ DAC

in [26], where f_{out} translates by one decade as well as in [30] with an f_{out} close to f_s due to the utilization of the 2nd Nyquist zone with the mixing-mode technique. On the contrary, other DACs achieve a higher f_{out} with respect to f_s as explained earlier in BiCMOS and HBT technologies. Another case corresponds to the RF DACs [31], where the signal bandwidth is centered at the carrier frequency, f_c.

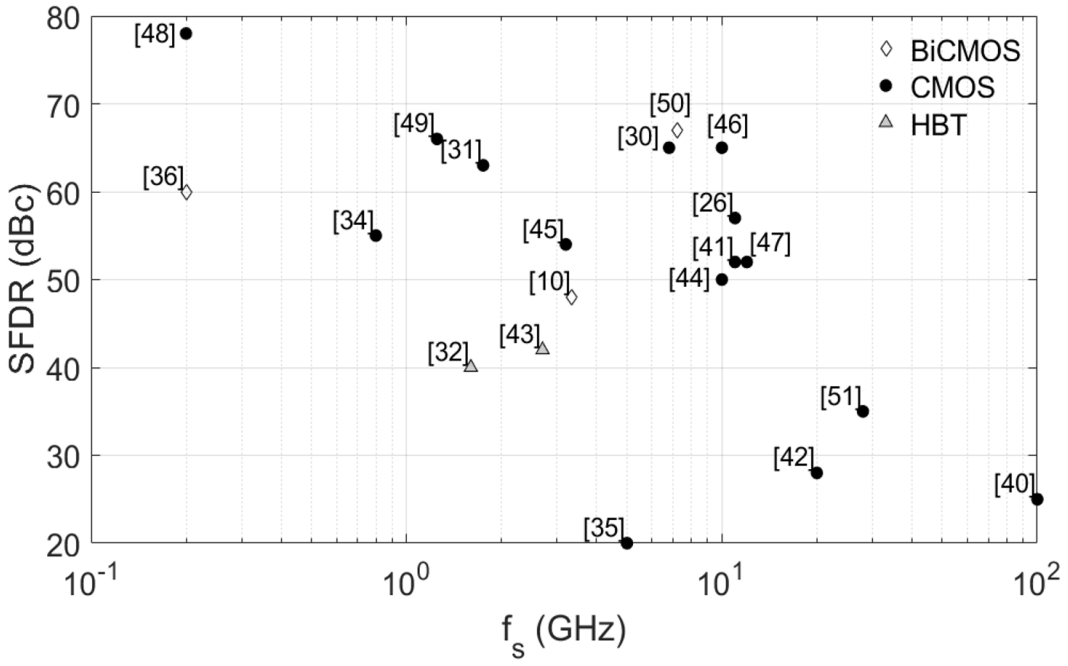

Figure 2.12: SFDR versus the sampling frequency, f_s.

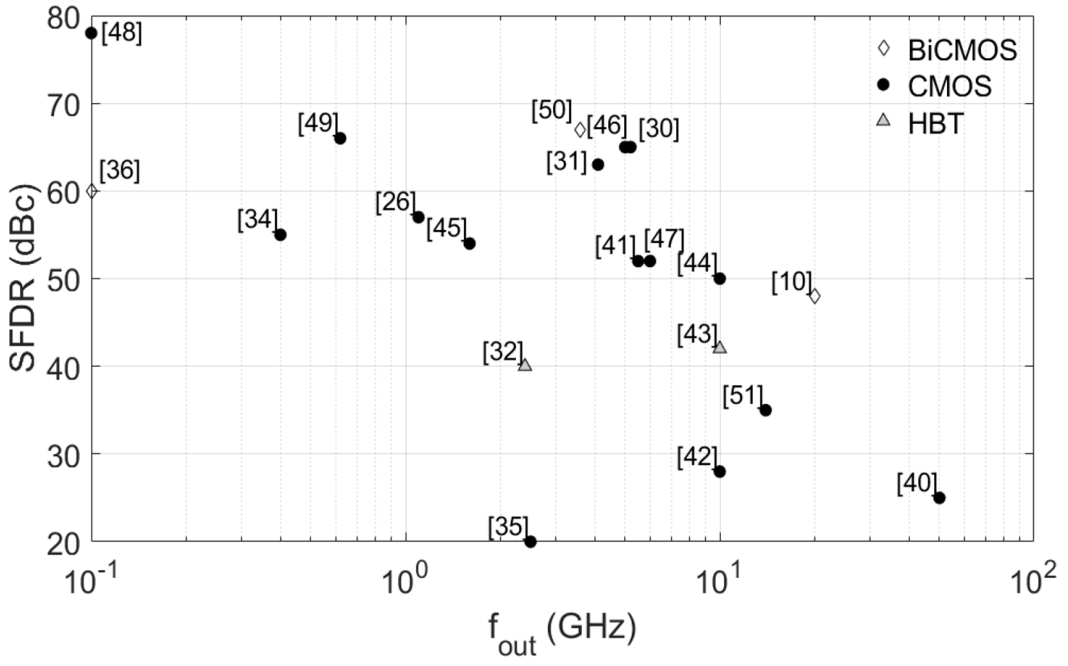

Figure 2.13: SFDR versus the output frequency, f_{out}.

Table 2.1: Performance comparison of reported DACs.

N°	Type	Technology	Resolution	f_s (GHz)	BW (GHz)	f_{out} (GHz)	P_c (mW)	SFDR (dBc)	Reference
1	RZ CS-R2R	0.13μm BiC-MOS	10	3.35	1.67	20	1910	48	[10]
2	TI $\Delta\Sigma$ CS	65nm CMOS	8	11	1.1	1.1	117	57	[26]
3	Mixing CS	16nm CMOS	14	6.8	3.4	5.2	330	65	[30]
4	RF CS	65nm CMOS	16	1.75	0.9	4.1	380	63	[31]
5	RZ CS-R2R	0.4μm^2 HBT	12	1.6	0.8	2.4	1200	40	[32]
6	Pipeline SC	90nm CMOS	12	0.8	0.4	0.4	103	55	[34]
7	Nyquist SC	65nm CMOS	12	5	2.5	2.5	50	20	[35]
8	Pipeline SC	0.5μm BiC-MOS	10	0.2	0.1	0.1	693	60	[36]
9	TI CS	28nm CMOS	8	100	50	50	2500	$25^{(2)}$	[40]
10	TI CS	28nm CMOS	9	11	5.5	5.5	110	52	[41]
11	TI CS	65nm CMOS	6	20	10	10	136	28	[42]
12	RZ CS-R2R	0.5μm HBT	12	2.7	1.35	10	1600	42	[43]
13	Mixing CS	28nm CMOS	14	10	5	10	210	50	[44]
14	Nyquist CS	65nm CMOS	16	3.2	1.6	1.6	240	$54^{(1)}$	[45]
15	Nyquist CS	28nm CMOS	14	10	5	5	162	65	[46]
16	Nyquist-$\Delta\Sigma$ CS	65nm CMOS	16	12	6	6	1760	52	[47]
17	Nyquist CS	0.14μm CMOS	14	0.2	0.1	0.1	270	78	[48]
18	Nyquist CS	90nm CMOS	12	1.25	0.62	0.62	128	66	[49]
19	CS-R2R	0.13μm BiC-MOS	14	7.2	3.6	3.6	4600	67	[50]
20	TI CS	40nm CMOS	6	28	14	14	103	35	[51]

(1): Reported at f_{out} equal to 0.7 GHz. (2): Reported at f_{out} equal to 25 GHz.

Chapter 3

The current-steering DAC

The CMOS current-steering (CS) DAC is presented in more detail in this chapter. The fundamental performance limitations are first discussed and then followed with a theoretical analysis of energy/power consumption bounds. Thereafter, circuit design considerations and enhancement techniques are presented. A simplified block diagram of a differential CS DAC is illustrated in Fig. 3.1. Initially, synchronization between the input bits $[b_{N-1}, .., b_1, b_0]$ is achieved through the timing circuits with clock and data buffer required for signal integrity. The complementary control signals SW and $\overline{\text{SW}}$ are generated to drive the switches in the differential pair, and thus, steer the current to one of the differential outputs. The contribution of all the current at the output node generates the analog signal accordingly.

3.1 Fundamental performance limitations

Physical phenomena, imperfections in the manufacturing process and limitations at the circuit-level bound and deviate the performance of the CS DAC from ideal. The fundamental limitations considered in this section include the stochastic mismatch error in the current sources, nonlinear settling, output resistance/impedance degradation and noise, respectively.

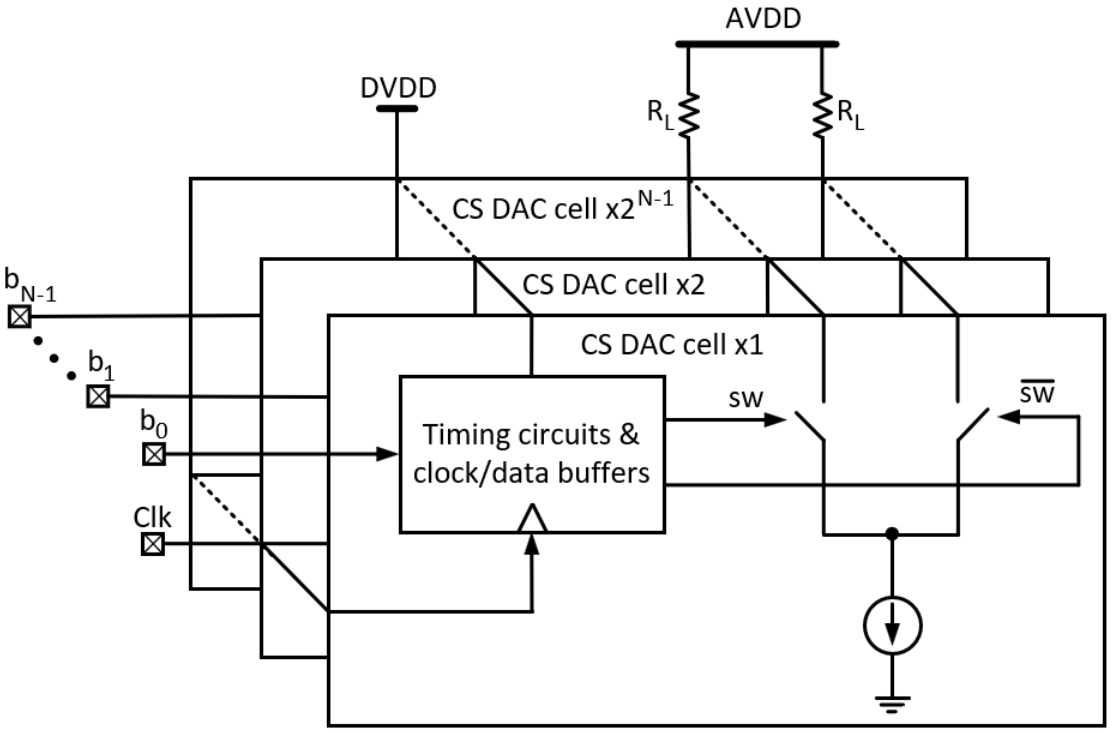

Figure 3.1: Simplified block diagram of a current-steering (CS) DAC.

3.1.1 Stochastic current mismatch

The stochastic mismatch errors in the current sources arise from the manufacturing process as explained next. Inherently, the output current deviates from ideal by an amplitude error that can be expressed for an arbitrary current source as

$$I_{real} = I_{ideal} + I_{err}, \tag{3.1}$$

with I_{err} the amplitude error commonly modeled as a random variable with a Gaussian distribution, $N(0, \sigma^2)$. From the Pelgrom's mismatch model [52], the ratio $\sigma^2(I)/I^2$ with I the output current and $\sigma^2(I)$ its variance for a current source transistor with large dimensions can be approximated by

$$\frac{\sigma^2(I)}{I^2} \approx \frac{\sigma^2_{\Delta\beta}}{\beta^2} + \frac{4[\sigma^2_{\Delta V_{T0}} + \sigma^2_{\Delta V\gamma}]}{(V_{gs} - V_T)^2}, \tag{3.2}$$

where

$$\sigma^2_{\Delta V_{T0}} = \frac{A^2_{VT0}}{WL} + S^2_{VT0}D^2,\ \sigma^2_{\Delta V_\gamma} = \frac{A^2_\gamma}{WL} + S^2_\gamma D^2,\ \frac{\sigma^2_{\Delta\beta}}{\beta^2} \approx \frac{A^2_\beta}{WL} + S^2_\beta D^2, \tag{3.3}$$

with A_β^2, A_{VT0}^2, A_γ^2, S_{VT0}^2, S_γ^2, S_β^2 the process parameters, W and L the width and channel length of the device and D the distance between the devices. From (3.2), $\sigma^2(I)$ is inversely proportional to WL. Thus, increasing the transistor's dimensions is a common approach to reduce the error at the cost of area utilization. Moreover, the overdrive voltage, $V_{gs} - V_{th}$, in the current sources counteracts for both $\sigma^2(\Delta V_{T0})$ and $\sigma^2(\Delta V_\gamma)$, suggesting to increase the voltage headroom in the current sources at the cost of augmented power consumption. Other sources of error are categorized as systematic, including IR-drop in the bias network as well as process, electrical and temperature gradients, which can be mitigated with an appropriate layout design [23], [53]. The static performance degradation due to the stochastic current mismatch has been extensively studied in [22], [37], [53], [54]. For an N-bit binary-weighted CS DAC, the DNL's variance for an arbitrary input code x, $\sigma^2(\text{DNL}_x)$, can be given as [22]

$$\sigma^2(\text{DNL}_x) = \frac{\sigma^2(I_u)}{I_u^2} \sum_{i=0}^{N-1} 2^i |b_i^x - b_i^{x-1}|, \tag{3.4}$$

with b_i an bit of the input code x and I_u the unary-current. From (3.4), the DNL can be derived as DNL=max$[\sqrt{\sigma^2(\text{DNL}_x)}]$, which shows a close agreement with the DNL approximation in [54]. Similarly, DNL formulations for the unary-weighted and hybrid or segmented DAC architectures can be derived [54]. Regarding the INL, yield estimations with Monte Carlo analysis are proposed [53]. An alternative formulation has been presented with the criteria of a functional DAC if the condition INL$<$0.5 LSB is satisfied, where the ratio $\sigma(I_u)/I_u$ is obtained by [53]

$$\frac{\sigma(I_u)}{I_u} = \frac{1}{2\sqrt{2^N C}}, \tag{3.5}$$

with $C = \text{inv-norm}_{(-x,x)}(0.5 + \text{INL-yield}/2)$. Further on, the stochastic mismatch error in the current sources results in either HD if the input signal is periodic or an increased in the noise power if it has a random behaviour. The SFDR for the third-order HD (HD3) case approximates in dB to [37]

$$\text{SFDR} \approx 3(N+3) - 10\log_{10}\left[\frac{\sigma(I_u)}{I_u}\right]^2 \text{dBc}. \tag{3.6}$$

Hence, the CS DAC's dynamic performance can start to degrade considerably from low signal frequencies if no careful attention is given to the stochastic current

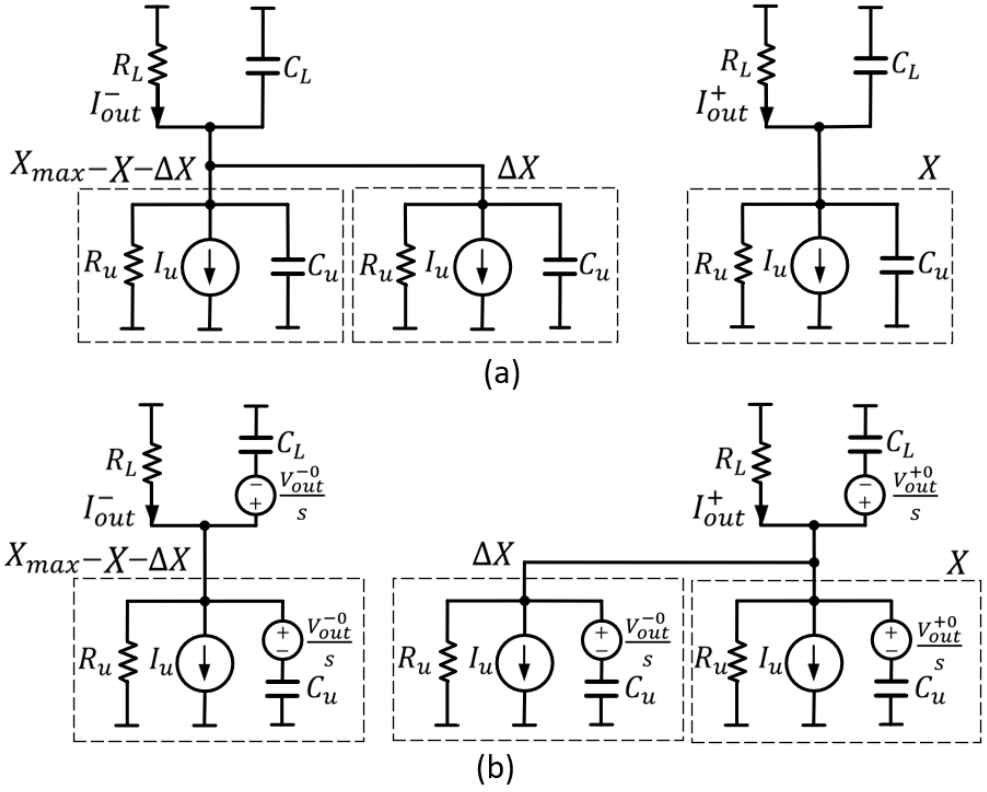

Figure 3.2: Simple model of the CS DAC (a) before (b) after the switching transition [37].

mismatch errors.

3.1.2 Nonlinear settling

To investigate the settling behaviour of a CS DAC, let's consider the circuit model of Fig. 3.2 with the group of current sources ΔX being switched between the differential outputs. Hence, for the complementary input digital codes represented as $X^{\pm} = X_{DC} \pm \tilde{X}$ with X_{DC} and $\tilde{X}$, the DC and AC terms, respectively, it can be shown that the time-domain response of the output currents I_{out}^- and I_{out}^+ at the time instant n are expressed as [37]

$$\begin{aligned} I_{out}^+(n) = I_{DC}\frac{1+\tilde{x}_n}{1+\rho_G^{'}\tilde{x}_n}\left[1-e^{\frac{-t}{\tau_\sigma(X_n^+)}}\right] + I_{out}^+(n-1)e^{\frac{-t}{\tau_\sigma(X_n^+)}} \\ + I_{out}^-(n-1)\frac{\rho_C^{'}\Delta\tilde{x}_n}{1+\rho_C^{'}\tilde{x}_{n-1}}e^{\frac{-t}{\tau_\sigma(X_n^+)}}, \end{aligned} \tag{3.7}$$

and

$$I_{out}^{-}(n) = I_{DC}\frac{1-\tilde{x}_n}{1-\rho_G^{'}\tilde{x}_n}\left[1-e^{\frac{-t}{\tau_\sigma(X_n^{-})}}\right] + I_{out}^{-}(n-1)e^{\frac{-t}{\tau_\sigma(X_n^{-})}}, \tag{3.8}$$

where

$$I_{DC} = \frac{I_{LBS}X_{DC}}{1+\rho_G X_{DC}},\ \rho_G^{'} = \frac{\rho_G X_{DC}}{1+\rho_G X_{DC}} \text{ and } \rho_C^{'} = \frac{\rho_C X_{DC}}{1+\rho_C X_{DC}}, \tag{3.9}$$

with $\rho_G = R_L/R_u$ and $\rho_C = C_u/C_L$ the conductance and capacitance ratios and $\tilde{x} = \tilde{X}/X_{DC}$. Besides,the system's time constant, $\tau_\sigma(X^{\pm})$, is given by

$$\tau_\sigma(X^{\pm}) = \tau_L\frac{1+\rho_C X^{\pm}}{1+\rho_G X^{\pm}}. \tag{3.10}$$

From (3.10), we have that $\tau_\sigma(X^{\pm})$ is code-dependent, thus resulting in a nonlinear settling. Moreover, if $\rho_G = \rho_C$, then $\tau_\sigma(X^{\pm})$ is linearly dependent on τ_L only. On the other hand, in (3.7), the third term is canceled if there is no change in the input code, i.e., $\Delta\tilde{x}_n = 0$, otherwise, $I_{out}^{+}(n)$ is also dependent on the rate of change of the input code. Also, from (3.7) and (3.8), the memory effects from the previous output currents, $I_{out}^{-}(n-1)$ and $I_{out}^{-}(n-1)$ influence the settling of $I_{out}^{-}(n)$ and $I_{out}^{+}(n)$ and contribute with the nonlinear settling. To mitigate for these memory effects and generate a less dependent signal's round-trip from changes in the input code, the terms $I_{out}^{-}(n-1)$ and $I_{out}^{+}(n-1)$ can be cancelled by setting them to zero. This is already presented in Section. 2.2 with the so-called RZ technique. Yet, this requires a faster settling response, e.g., within half of the clock period, which represents a design challenge when aiming to operate at high-speed.

3.1.3 Limited output resistance

The finite output resistance in the CS DAC impacts the static and dynamic performance. To see how, let's consider again the CS DAC model shown in Fig. 3.2. Thus, considering a settling condition and substituting for I_{DC} and $\rho_G^{'}$ in (3.7) and (3.8), the output currents I_{out}^{-} and I_{out}^{+} are reduced to

$$I_{out}^{+}(n) = I_{DC}\frac{1+\tilde{x}_n}{1+\rho_G^{'}\tilde{x}_n} = \frac{I_u X_n^{+}}{1+\rho_G X_n^{+}}, \tag{3.11}$$

and

$$I_{out}^{-}(n) = I_{DC}\frac{1-\tilde{x}_n}{1-\rho_G^{'}\tilde{x}_n} = \frac{I_u X_n^{-}}{1+\rho_G X_n^{-}}. \tag{3.12}$$

From (3.11) and (3.12), if $\rho_G = 0$, the denominator is equal to 1 and as expected the output currents have a linear relation with the complementary input codes, $X^{\pm}$. This can be obtained with $R_u \to \infty$ as ρ_G also equals R_L/R_u. The limitation from achieving an infinite output resistance in the current sources turns into a nonlinear response, which degrades the performance as will be shown next. For the static performance with the DNL and INL expressions (2.13) and (2.14) from Section. 2.4. For an arbitrary input code k with $A_k = I_{out}(k)$, $A_{k-1} = I_{out}(k-1)$ and $\alpha = 1$, the DNL and INL can be given by

$$\text{DNL}_k = (1+\rho_G)\left(\frac{k}{1+\rho_G k} - \frac{k-1}{1+\rho_G(k-1)}\right) - 1 \approx \frac{(1+\rho)}{(1+\rho k)^2} - 1 \text{ [LSB]} \tag{3.13}$$

and

$$\text{INL}_k = \frac{k(1+\rho_G)}{1+\rho_G k} - 0 - k = \frac{k(1+\rho_G) - k(1+\rho_G k)}{1+\rho_G k} \text{ [LSB]}. \tag{3.14}$$

On the other hand, if $\rho_G \neq 0$, the output currents I_{out}^{-} and I_{out}^{+} have a nonlinear dependency with respect to the input code, $X^{\pm}$, which leads to distortion and consequently degrading the dynamic performance of the CS DAC. From (3.11) and (3.12), the differential output current, $I_{out,diff}$, equals

$$I_{out,diff}(n) = I_{out}^{+}(n) - I_{out}^{-}(n) = I_{DC}\frac{2\tilde{x}_n(1-\rho_G^{'})}{1-(\rho_G^{'}\tilde{x}_n)^2}. \tag{3.15}$$

Then, normalizing (3.15) with respect to $2(1-\rho_G')/\rho_G'$, we obtain

$$I_{out,diff}(n) = I_{DC}\frac{\rho_G^{'}\tilde{x}_n}{1-(\rho_G^{'}\tilde{x}_n)^2}. \tag{3.16}$$

By considering the input signal $X = X_{DC}(1 + x\sin(2\pi f_{sig} n)$ with $x = X_{AC}/X_{DC}$. From Taylor series, (3.16) can also be written as

$$I_{out,diff}(n) = I_{DC}\rho_G^{'}\tilde{x}_n \sum_{m=0}^{\infty}(\rho_G^{'}\tilde{x}_n)^{2m} = I_{DC}\sum_{m=0}^{\infty} A^{2m+1}\sin^{2m+1}\theta, \tag{3.17}$$

with $A = \rho_G^{'} x$ and $\theta = 2\pi f_{sig} n$. Also, from series expansion, we get

$$\sin^{2m+1}\theta = \frac{(-1)^m}{2^{2m}} \sum_{n=0}^{m} (-1)^n \binom{2m+1}{n} \sin\left((2(m-n)+1)\theta\right). \tag{3.18}$$

Substituting (3.18) into (3.17) and after reordering terms

$$I_{out,diff}(t) = 2I_{DC} \sum_{m=0}^{\infty} \sum_{n=0}^{m} (-1)^{m+n} \left(\frac{A}{2}\right)^{2m+1} \binom{2m+1}{n} \sin\left(\theta_{m,n}\right), \tag{3.19}$$

where $\theta_{m,n} = (2(m-n)+1)\theta$. For an CS DAC with a differential output, we are interested in HD_3. This corresponds to $\sin(3\theta)$ in (3.19) with $(2(m-n)+1) = 3$ that results in $m = n+1$. Similarly, for the fundamental tone, we have $m = n$. From the previous derivations of m for the fundamental and HD3, the SFDR can be derived from their ratio as [37]

$$\text{SFDR} = \left[1 - \frac{2}{\rho_G^{'} x}\left(\frac{1}{\rho_G^{'} x} + \sqrt{\frac{1}{(\rho_G^{'} x)^2} - 1.}\right)\right]^2. \tag{3.20}$$

Therefore, if $\rho_G^{'} \approx 0$ in (3.20), the SFDR $\approx 16/\left(\rho_G^{'} x\right)^4$. Also, if $x \approx 1$ and $\rho_G X_{DC} << 1$ from (3.9), the SFDR can be approximated in dB as

$$\text{SFDR} \approx -40 \log_{10} \rho_G - 12(N-2) \text{ dB}. \tag{3.21}$$

Without loss of generality, we consider the admittance ratio, ρ_Y, for the output impedance given by [37], [53]

$$\rho_Y = \frac{G_S + j\omega C_S}{G_L + j\omega C_L}. \tag{3.22}$$

From (3.20), the output impedance, Z_{out}, versus the SFDR for different CS DAC resolutions and a load impedance, Z_L, of $50\ \Omega$, is plotted in Fig. 3.3. Notice that the requirement in Z_{out} increases by about 3 dB/bit, i.e, the Z_{out} doubles with increments of 1 bit in the CS DAC for a particular SFDR specification.

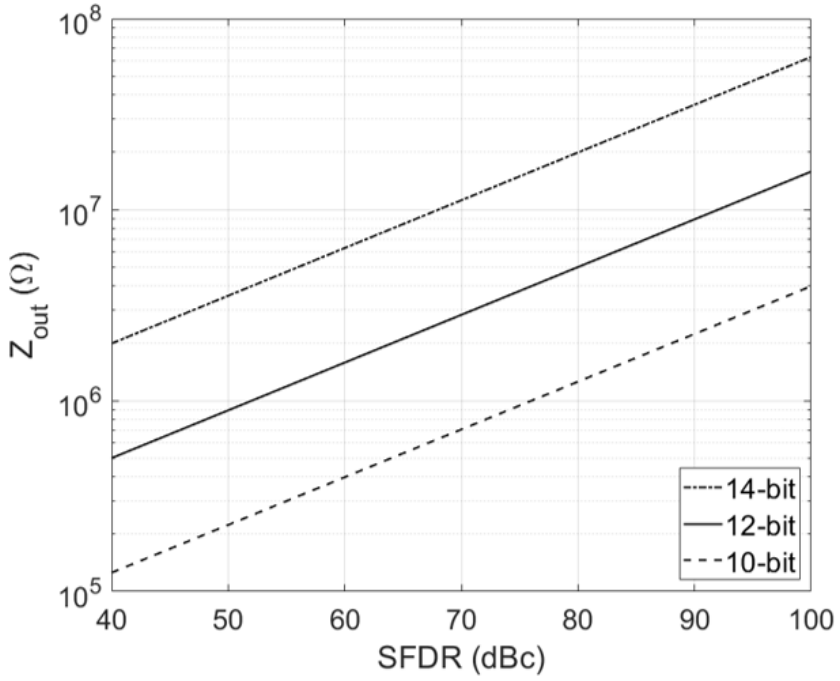

Figure 3.3: Z_{out} versus the SFDR for a load impedance, Z_L = 50 Ω.

3.1.4 Circuit noise

In the CS DAC the noise contribution at the output is mainly attributed to the current sources and the load resistance, R_L. The thermal noise in the cascode transistors can be neglected if their gain is high as well as the thermal noise from the gate resistance, R_G, in the switching transistors [39]. Besides, the flicker noise has relevance only at low-frequencies, hence it can be omitted. Overall, the presence of noise in the CS DAC's output reduces the SNR. For uncorrelated thermal noise sources with a Gaussian distribution, the average noise power at the output in units of amperes^2 can be given for a differential N-bit CS DAC by [8]

$$P_{noise} = 4k_B T \left[(2^N - 1)\gamma g_m + \frac{2}{R_L} \right] \Delta f, \tag{3.23}$$

with k_B the Boltzmann's constant, T the temperature in degrees Kelvin, g_m the transconductance in the current source transistors and Δf the noise bandwidth. Also, for the differential output considering the quantization noise power as $P_q = (2I_u)^2/12$ in amperes^2. The SNR is formulated as the ratio between the average signal power, $P_{sig} = (2^N - 1)^2 I_u^2/2$, and the thermal plus quantization noise

contributions, which for $N \geqslant 6$, this is approximated as

$$\text{SNR} \approx \frac{2^{2N} I_u^2/2}{4k_B T \left(2^N \gamma g_m + 2/R_L\right) \Delta f + (2I_u)^2/12}. \tag{3.24}$$

From (3.24), the noise power increases with Δf, which has more relevance as larger channel bandwidth is required, thus reducing the SNR if the signal power is not increased accordingly.

3.2 Power consumption analysis

The power consumption in CS DACs can be divided into the contribution from the digital, mixed-signal and analog power domains. A separate analysis of each domain provides an insight of the physical and technological limitations that set a bound for the power and energy consumption in CS DACs. For the analysis, the CMOS technology is chosen as this results in faster switching speed, reduce power consumption and area utilization with smaller device geometries. Moreover, a binary-weighted CS DAC is considered due to its straightforward conversion approach without added circuit complexity, which also leads to high-speed operation and low-power consumption.

3.2.1 Digital domain

For a binary-weighted DAC, the digital domain encompasses the timing circuits for data synchronization as well as the input and output drivers for the data and clock signals. Static CMOS and current-mode logic (CML) are commonly utilized in the design of digital circuits. CML is prone to be power hungry due to its static power consumption component, requiring also resistors that increase the area utilization, however, energy-efficient solutions have been reported for high-speed applications [45]. Yet, the static CMOS logic benefits from the device scaling as mentioned, and therefore, it is considered in this analysis. The power consumption of CMOS digital circuits is well-known given by the contribution of the dynamic, static, short-circuit and leakage power consumption components. Nevertheless, for a complementary static CMOS logic with raising and falling

transitions close to zero and omitting the leakage power[1], the power consumption from the digital domain for an N-bit CS DAC reduces to

$$P_{DACd} = (2^N - 1)V_{DVDD}^2(\alpha_{0\to1}C_d + C_{clk})f_s, \tag{3.25}$$

with V_{DVDD} the digital domain's supply voltage, α the switching activity factor, f_s the sampling frequency, C_d and C_{clk} the data and clock load capacitance, respectively.

3.2.2 Mixed-signal domain

The mixed-signal power domain considers the switching transistors as they conform the boundary between the digital and analog domains. Thus, from the mixed-signal domain, P_{DACm}, the power consumption can be given by

$$P_{DACm} = \alpha_{0\to1}(2^N - 1)V_{g,M_{sw}}^2 C_{g,sw} f_s, \tag{3.26}$$

where $C_{g,sw} = 2W_{sw}L_{sw}C_{ox}/3 + 2C_{g,ov}$, with $C_{g,ov}$ the overlap capacitance and $V_{g,M_{sw}}$ the voltage swing at the switching transistors' gate.

3.2.3 Analog domain

The power consumption in the analog domain, P_{DACa}, is obtained from the CS differential pair. For an N-bit CS DAC, it yields

$$P_{DACa} = (2^N - 1)V_{AVDD}I_u, \tag{3.27}$$

with V_{AVDD} the analog domain's supply voltage. Moreover, V_{AVDD} can be split into the single-ended voltage swing, $V_{swd}/2$, with V_{swd} the differential voltage swing, and the headroom voltage, V_{hr}, in the CS cell. The simplest CS cell that leads to a reduced V_{hr} is conformed by two-stacked transistors[2], one operating as a current source, M_{cs}, and the other as a switch, M_{sw} as illustrated in Fig. 3.4. The switch transistors are preferably designed to operate in saturation

[1] Albeit a potentially considerable factor in modern digital circuits.
[2] If the current switch transistors are required to operate in saturation.

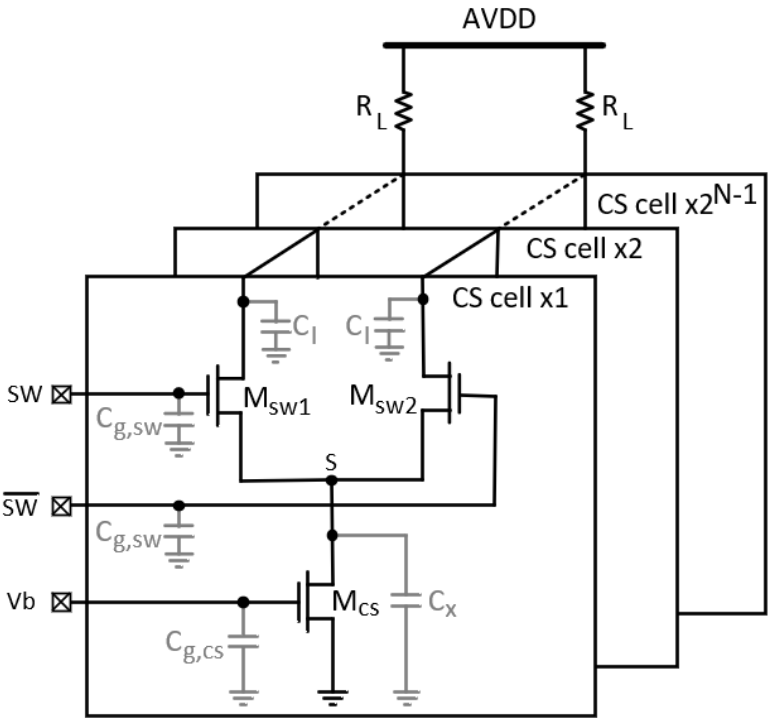

Figure 3.4: A differential CS DAC cell array with the parasitic capacitances.

when switched on to augment the output impedance. For the drain-to-source voltage in M_{cs}, $V_{ds,M_{cs}}$, and considering its effective voltage $V_{eff,M_{cs}}$ that satisfies the minimum saturation condition. By relating the switch transistors drain-to-source voltage, $V_{ds,M_{sw}}$, to $V_{eff,M_{cs}}$ as $V_{ds,M_{sw}} = \alpha V_{eff,M_{cs}}$, the expression (3.27) can also be expressed as

$$P_{DACa} = (2^N - 1)(\beta V_{eff,M_{cs}} + V_{sw,d}/2) I_u, \tag{3.28}$$

with $\beta = (\alpha+1)$ and $\alpha > 0$. Next, we elaborate on $V_{eff,M_{cs}}$ and I_u for the minimum power consumption. For this purpose, the analysis is carried out for the design corners of noise, speed and linearity, respectively.

3.2.4 Power consumption bounds

From the previous discussion, the total power consumption of the CS DAC, P_{DAC}, considering the contribution of each separate domain from (3.25), (3.26) and

(3.28) for $N \geq 6$ approximates to

$$P_{DAC} \approx 2^{N-1}[(2\beta V_{eff,M_{cs}}) + V_{sw,d} I_u + 2V_{DVDD}^2 C_T f_s], \tag{3.29}$$

with $C_T = C_d/2 + C_{g,sw}/2 + C_{clk}$ and considering $V_{g,M_{sw}} = V_{DVDD}$. The analysis of the energy and power consumption bounds for the aforementioned design corners is presented next.

Noise-limited bound

For this analysis, we consider the thermal noise contribution at the output from the current sources as well as the output load resistance. Also, for the sake of simplicity, we assume a large gain in the cascode transistors, thus neglecting their noise contribution. From (3.23), we have the expression for the average noise power rewritten below for convenience

$$P_{Th} = 4k_B T \left[(2^N - 1)\gamma g_m + \frac{2}{R_L}\right] \Delta f. \tag{3.30}$$

Since $g_m = 2I_u/V_{eff,M_{cs}}$ and $R_L = V_{sw,d}/2(2^N - 1)I_u$, P_{Th} in (3.23) is

$$P_{Th} = \frac{8(2^N - 1)k_B T I_u}{V_{sw,d}}(\gamma V + 2)\Delta f. \tag{3.31}$$

In this model, P_{Th} is defined to be equal to the quantization noise power so that

$$P_{Th} \triangleq \frac{(2I_u)^2}{12}. \tag{3.32}$$

From (3.31) and (3.32) with $N \geq 6$ and $\Delta f = f_s/2$, I_u is obtained as

$$I_{u,n} \approx \frac{12k_B T 2^N}{V_{sw,d}}(\gamma V + 2) f_s, \tag{3.33}$$

where $V = V_{sw,d}/V_{eff,M_{cs}}$. The power consumption can then be expressed as

$$P_{DACa,n} \approx \frac{6k_B T 2^{2N}}{V_{sw,d}}(2\beta\gamma + 4\beta V^{-1} + \gamma V + 2) f_s. \tag{3.34}$$

Also, considering the derivative of (3.34) with respect to $V_{eff,M_{cs}}$ an equation for the minimum $P_{DACa,n}$ is obtained and given for an N-bit CS DAC by [8]

$$P_{DACa,n} = 12k_BT2^{2N}(\sqrt{\beta\gamma}+1)^2 f_s. \tag{3.35}$$

Bias network

A bias network conformed by a simple current mirror is considered to analyze its noise contribution to the output. The bias network and the current source transistors in the CS DAC are shown in Fig. 3.5. The total noise contribution at the gate of the current source transistors, V_b, is given by

$$\overline{I_{n,in}^2} = (2^N-1)\overline{I_{n,M_i}^2} + \overline{I_{bias}^2}, \tag{3.36}$$

with $\overline{I_{n,M_i}^2}$ and $\overline{I_{bias}^2}$ the input-referred noise from a current source transistor, M_i, and the bias network, respectively. The output-referred current noise is

$$\overline{I_{n,out}^2} = \left[(2^N-1)\overline{I_{n,M_i}^2} + \overline{I_{bias}^2}\right]|Z_{bias}|^2 g_m^2, \tag{3.37}$$

where $|Z_{bias}| = R_{bias}^2/\left[1+(\omega R_{bias}C_{bias})^2\right]$ and g_m is the transconductance of the current source transistor. Moreover, $\overline{I_{n,M_i}^2}$ can be expressed as

$$\overline{I_{n,M_i}^2} = \frac{\overline{V_{n,M_i}^2}}{|Z_{bias}|^2}. \tag{3.38}$$

Utilizing (3.38) in (3.37) and approximating for $N \geq 6$, we obtain

$$\overline{I_{n,out}^2} \approx 2^N g_m^2 \overline{V_{n,M_i}^2} + \frac{g_m^2 \overline{I_{n,bias}^2 R_{bias}^2}}{1+(\omega R_{bias}C_{bias})^2}. \tag{3.39}$$

In (3.39), the first term is the noise contribution from the current sources. The second term corresponds to the thermal noise coupled from the bias network to the output, which for $(\omega C_{bias})^2 \to \infty$, its effect reduces with augmented speed of operation, resolution and proper decoupling.

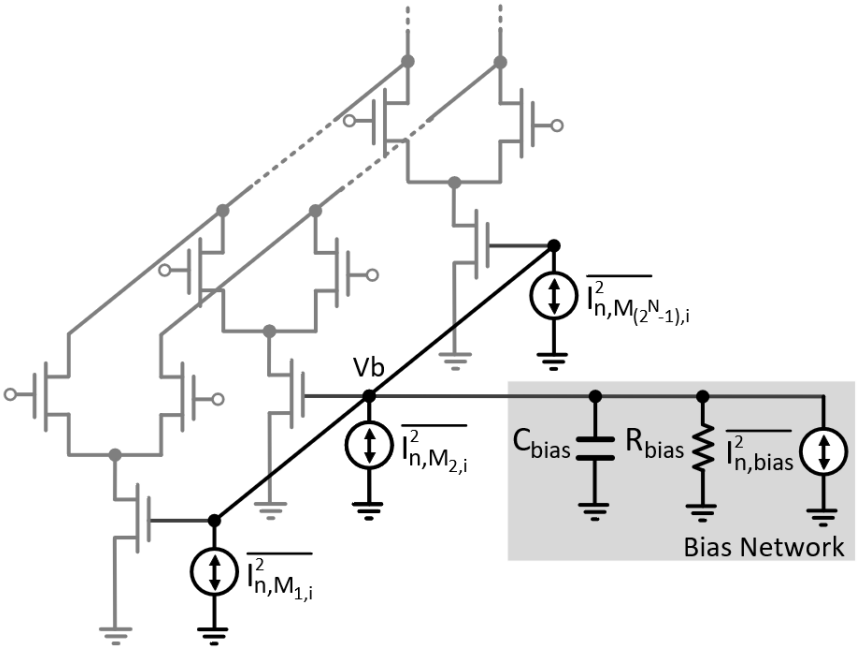

Figure 3.5: Bias network with noise from the current source transistors (input-referred).

Speed-limited bound

In a CS DAC, the speed is mainly dominated by the switching time and the bandwidth of the system, BW. The former benefits from transit frequencies, f_T, in modern CMOS process nodes above 100 GHz [55], whereas the latter takes over as the N-bit CS DAC resolution increases. For this analysis, the speed bound is determined from BW expressed as

$$BW = \frac{1}{2\pi R_L C_L}, \tag{3.40}$$

with C_L and R_L the load capacitance and resistance, respectively. C_L can be obtained from the drain-to-ground capacitance seen at the output of the CS cell, C_l so that $C_L = (2^N - 1)C_l$. Also, R_L is selected in the design. Considering that BW covers the the Nyquist bandwidth, $f_s/2$, then solving for f_s in (3.40), it yields

$$f_s = \frac{1}{(2^N - 1)\pi R_L C_l} \tag{3.41}$$

Moreover, we have that $R_L = V_{sw,d}/(2^N - 1)I_u$. Thus, from (3.41) it leads to

$$I_{u,s} = \frac{\pi V_{sw,d} C_l f_s}{2}. \tag{3.42}$$

From (3.42), we can obtain an expression for the power bound in the analog domain due to the speed limitation, which approximates for $N \geq 6$ by

$$P_{DACa,s} \approx 2^{N-2}\pi C_l(2\beta V_{eff,M_{cs}} V_{sw,d} + V_{sw,d}^2) f_s. \tag{3.43}$$

Linearity-limited bound

As mentioned in Section 3.1, the CS DAC's linearity is subjected to fundamental non-idealities, including the random mismatch errors in the current sources and finite output impedance. The former is counteracted with large device dimensions and reduced distance with no power consumption overhead [52]. Nevertheless, the size of the devices also impact the output impedance response as a result of larger stray capacitances in the internal nodes of the CS DAC. Rewriting the expression of the SFDR in (4.2) for a well-designed current source and extending to the admittance, we get

$$\text{SFDR} \approx \frac{16}{\rho_Y^{'4}}, \tag{3.44}$$

with $\rho_Y^{'}$ as a function of the admittance ratio's magnitude, $|\rho_Y| = |Z_L|/|Z_{out}|$

$$\rho_Y^{'} = \frac{1}{1 + (|\rho_Y| X_{DC})^{-1}}. \tag{3.45}$$

Substituting for $\rho_Y^{'}$ with $X_{DC} = 2^{N-1}$ and solving for $|\rho_Y|$, we obtain

$$|\rho_Y| = \frac{1}{2^{N-1}F(SFDR)} = \frac{|Z_L|}{|Z_{out}|}, \tag{3.46}$$

where $F(SFDR) = \sqrt[4]{SFDR}/2 - 1$. Also, $|Z_L| = R_L/\sqrt{1 + (\omega R_L C_L)^2}$ with $\omega = 2\pi f_{sig}$ and $R_L C_L = 1/\pi f_s$. Hence, if $f_{sig} = f_s/2$, then $|Z_L| = R_L/\sqrt{2}$. Then, substituting for $|Z_L|$ and solving for $|Z_{out}|$ in (3.46), it yields

$$|Z_{out}| = \frac{2^{N-1}F(SFDR)R_L}{\sqrt{2}}. \tag{3.47}$$

Also, $R_L = V_{sw,d}/(2^N - 1)I_u$. Substituting for R_L in (3.47) and solving for I_u

$$I_u = \frac{F(SFDR)V_{sw,d}}{2\sqrt{2}|Z_{out}|}. \tag{3.48}$$

From (3.48), an expression to find I_u from the SFDR and $V_{sw,d}$ for a $|Z_{out}|$ is obtained, where the frequency response of $|Z_{out}|$ depends on the CS cell [53]. For the chosen CS cell in Fig. 3.4, $|Z_{out}|$ is a function of I_u and approximates to $R_{out}/\sqrt{1+(\omega R_{out}C_x)^2}$. Substituting $|Z_{out}|$ in (3.48), it yields

$$I_{u,l} = \frac{\pi f_s C_x F(SFDR) V_{sw,d}}{\sqrt{2}}. \tag{3.49}$$

Finally, the expression for the analog power consumption for the linearity-bound in the CS DAC, $P_{DACa,l}$, is given by

$$P_{DACa,l} = \frac{2^{N-1}\pi F(SFDR) C_x (2\beta V_{eff,M_{cs}} V_{sw,d} + V_{sw,d}^2) f_s}{\sqrt{2}}. \tag{3.50}$$

Validation of the theoretical analysis

The energy consumption bounds of each power domain for the design corners of noise, speed and linearity are plotted together with data points obtained from reported CMOS CS DACs measurements in Fig. 3.6, 3.7 and 3.8, respectively. The design and technology parameters used in the study for a 65 nm CMOS process are listed in 3.1 and the current switch transistors are of minimum size. A range of $V_{ds,M_{sw}}$ voltages with the calculated values for $V_{eff,M_{cs}}/V_x$, β, V_{hr} and V_{AVDD} are listed Table. 3.2. Also, the load resistance, R_L, and full-scale current, I_{FS}, are obtained from the unary-current, I_u and a temperature of 75 °C is used for the noise energy bounds.

Table 3.1: Technology and design parameters [8].

Parameters	Variable	Value
Digital domain supply voltage	V_{DVDD}	1 V
CS cell common-node capacitance	C_x	$\approx 2.0 \cdot 10^{-2}$ fF
CS cell output capacitance	C_l	$\approx 0.5 \cdot 10^{-3}$ fF
CS cell gate capacitance	$C_{g,sw}$	$\approx 1.5 \cdot 10^{-1}$ fF
Capacitance in the digital blocks	$C_d + C_{clk}$	$\approx 13 \cdot 10^{-1}$ fF
Technology excess noise constant	γ	1.5

Table 3.2: $V_{eff,M_{cs}}$ calculation from different $V_{ds,M_{sw}}$ [8].

$V_{ds,M_{sw}}$	$V_{eff,M_{cs}}/V_x$	V_{hr}	β	V_{AVDD}	Plot
100 mV	$\approx$ 565 mV	$\approx$ 665 mV	1.18	$\approx$ 1.17 V	β_1
400 mV	$\approx$ 445 mV	$\approx$ 845 mV	1.90	$\approx$ 1.35 V	β_2

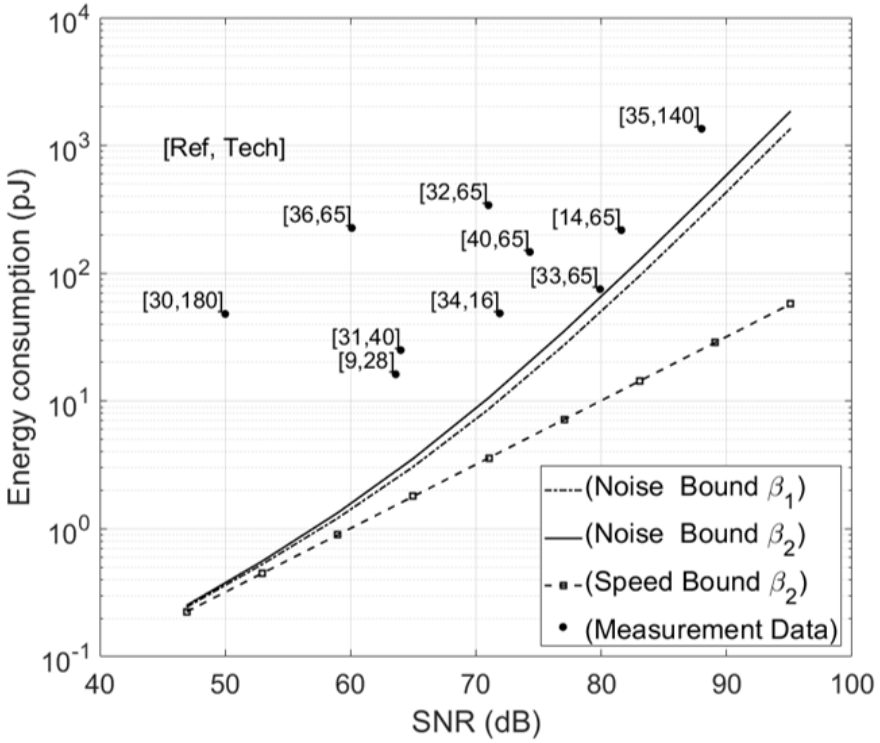

Figure 3.6: Data points plus noise and speed energy consumption bounds versus the SNR in a 65 nm CMOS process. Noise energy consumption bounds corresponding to β_1 and β_2 in Table. 3.2 [8].

The energy consumption bounds versus the SNR when considering the design corners of noise and speed are presented in Fig. 3.6. The energy consumption bound for the noise is plotted for β_1 and β_2 according to Table 3.2. Notice that the noise and speed energy consumption bounds start converging for an energy over 0.1 pJ and an SNR $\leq$ 50 dB since the mixed-signal and digital power domains become more dominant. Thereafter, the noise bound dominates for an SNR > 50 with a rapid increase as the SNR is larger as a result of the ENOB's exponential dependency in (3.35) with a rate of increase by 2^{2ENOB}. Also, the noise plots β_1 and β_2 diverge, showing the result for the different $V_{ds,M_{sw}}$ in Table 3.2. Regarding the speed corner, the digital and mixed-signal energy contributions increase at a rate of 2^{ENOB}, while the analog corner at 2^{ENOB-2} with a linear dependency on C_l from (3.43). Hence, the speed energy consumption bound is mainly dominated by the mixed-signal and digital components, and therefore, it increases proportionaly to 2^{ENOB}. Unlike the speed corner, the analog component of the noise bound does not scale with technology, thus representing the dominant bound condition with smaller device dimensions and larger SNR requirements as seen for an SNR $\geq$ 60 dB in Fig. 3.6. In comparison with the data

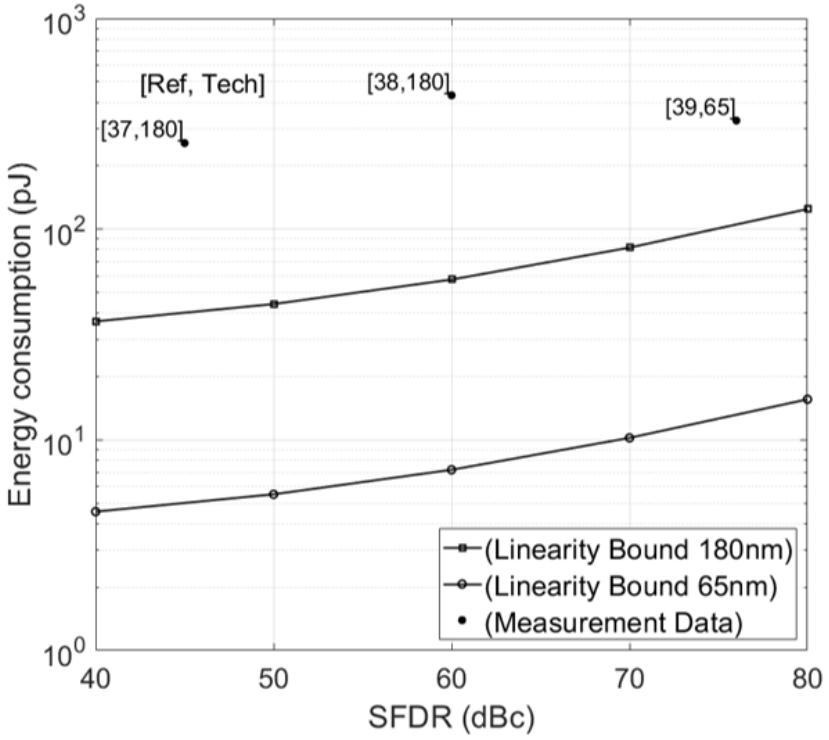

Figure 3.7: Data points and linearity energy consumption bounds vs SFDR for 12-bit CS DACs implemented in 180- and 65-nm CMOS process [8].

points for the noise bounds, notice that they come along with the trend observed for the plots β_1 and β_2, that shows an agreement with the analysis presented.

Further on, the energy consumption bound for linearity with β_2 versus the SFDR and the data points obtained from measurement results in 12- and 16-bit CS DACs are presented in Fig. 3.7 and 3.8, respectively. The linearity energy consumption bound is scaled with the device geometries since it is proportional to the common-node capacitance, C_x. Therefore, this is shown separately for the process nodes 180 nm and 65 nm CMOS. It is important to mention the utilization of enhancement techniques in some DAC implementations to improve the linearity with added cost in increased power consumption. Also, apart from the limited output impedance other amplitude and timing errors contribute with the linearity degradation in the CS DACs. Hence, the plots presented serve as a reference for comparison between the published data with the energy consumption bound for linearity. From Fig. 3.7, the energy consumption from the measurement data is higher when compared with the linearity energy consumption bound for the aforementioned technologies. Notice that a difference of around less than one order of magnitude is obtained for the data points [37,180] [38,180], except for

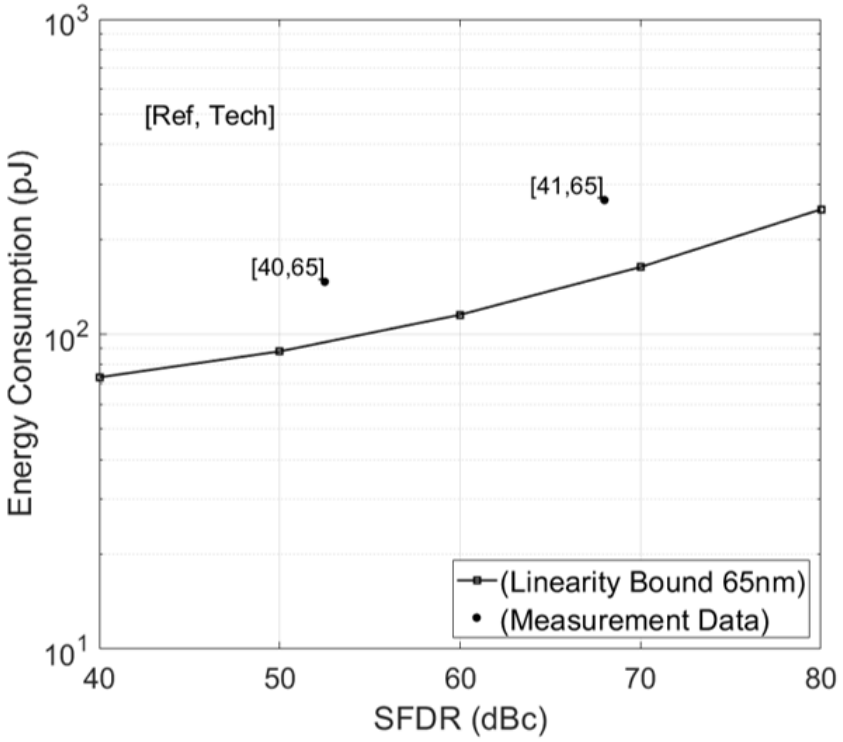

Figure 3.8: Data points and linearity energy consumption bounds vs SFDR for 16-bit CS DACs implemented in 65 nm CMOS process [8].

[39,65] that is larger instead. For instance, [37,180] utilize decoding logic and randomization circuits. Likewise [38,180] integrates master and slave latches, a thermometer decoder with delay equalizers, whereas in [39,65] added digital predistortion in a hybrid $\Delta\Sigma$ CS DAC implementation elevate the power consumption. In addition, the linearity energy consumption bound when considering a 16-bit CS DAC and implemented in 65 nm CMOS process is plotted along with reported data points in Fig. 3.8. Here, the energy consumption from measurement data is higher when compared with the linearity energy consumption bound, which shows a tendency towards higher energy consumption as the requirement in the SFDR increases. Both [40,65] [41,65] utilize signal processing techniques, thus augmenting the power consumption as seen for the measurement data points as well as the energy consumption bound for linearity at Nyquist, $f_s/2$.

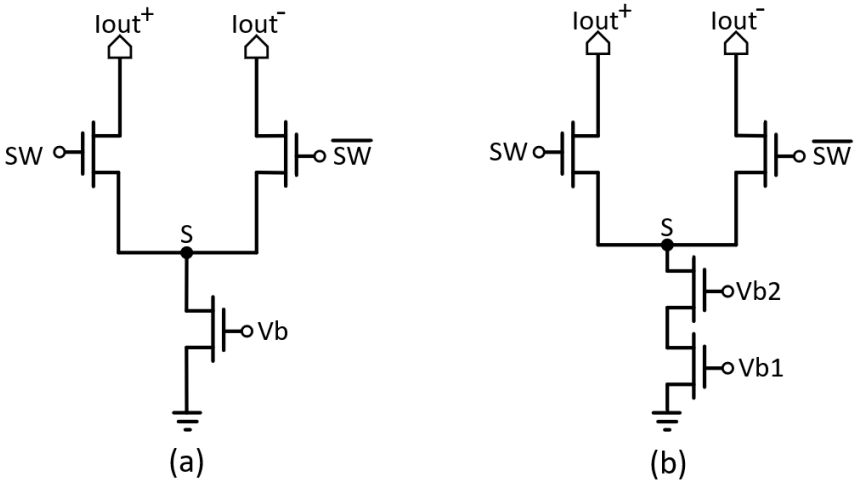

Figure 3.9: N-type CS cell (a) simple (b) cascode current source.

3.3 Circuit design considerations

3.3.1 Current-steering cell

The current-steering (CS) cell is the core of the CS DAC and to a large extend it determines its power consumption and performance as studied in previous sections. The simplest CS cell realization with NMOS transistors (N-type) is illustrated in Fig. 3.9(a). Naturally, other CMOS implementations include the PMOS-type and complementary [23]. As mentioned in Section 3.2, the CS cell of Fig. 3.9(a) is a low-voltage and low-power solution. Yet, if the current source transistor is increased in size to reduce the effect of stochastic mismatch errors [52], its drain-to-ground capacitance seen at the common-node (S) also increases. Moreover, interconnects at the common-node (S) add parasitic capacitance in physical implementations, which compromises the output impedance even from low frequencies and the settling time of this node after complementary switching transitions. To alleviate this problem a cascode current source can be utilized as shown in Fig. 3.9(b). The cascode transistor of reduced sized with respect to the current source transistor not only decreases the parasitic capacitance at the common-node (S), but also augments the output impedance. Moreover, this isolates the current source transistor from abrupt voltage changes during the switching transitions with added cost of voltage headroom and power consumption.

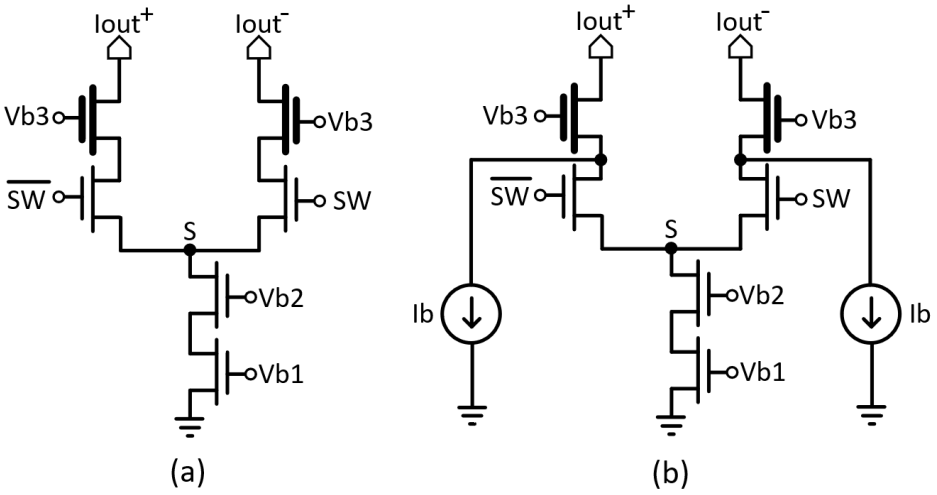

Figure 3.10: N-type CS DAC cell with stacked thick-oxide switch transistors (a) cascode current source (b) cascode current source with bleeding currents.

With the aim to further isolate the output nodes from the switching activity in the CS cell, which is discussed in more detail in Sec. 3.3.2, stacked switch transistors can be utilized as shown in Fig. 3.10(a). Yet, to maintain the a large voltage swing at the output and voltage headroom, thick-oxide transistors with a larger breakdown voltages are commonly utilized to handle supply voltages above the nominal 1.2 V in standard thin-oxide CMOS transistors. Nevertheless, the stacked switch transistors are also switched on and off with changes in their gate-to-source capacitance, C_{gs}, which affect the differential behavior of the CS cell [53]. To avoid switching off the cascode transistors, the so-called bleeding currents, I_b, have been proposed as shown in Fig. 3.10(b) [56]. The current I_b is typically designed to be a fraction of the output current in the CS cell of about 1% or 2% so that their use does not represent an overhead in power consumption. Comprehensive analysis regarding the output impedance and dynamic performance for these structures have been presented in literature [53].

3.3.2 Current switches

The current switch transistors play an important role in the performance of the CS DAC as they are the interface between the digital and analog domains. As discussed in Section 3.3.1, the signals SW and $\overline{\text{SW}}$ control the current switches to steer the output current. During complementary switching transitions, voltage

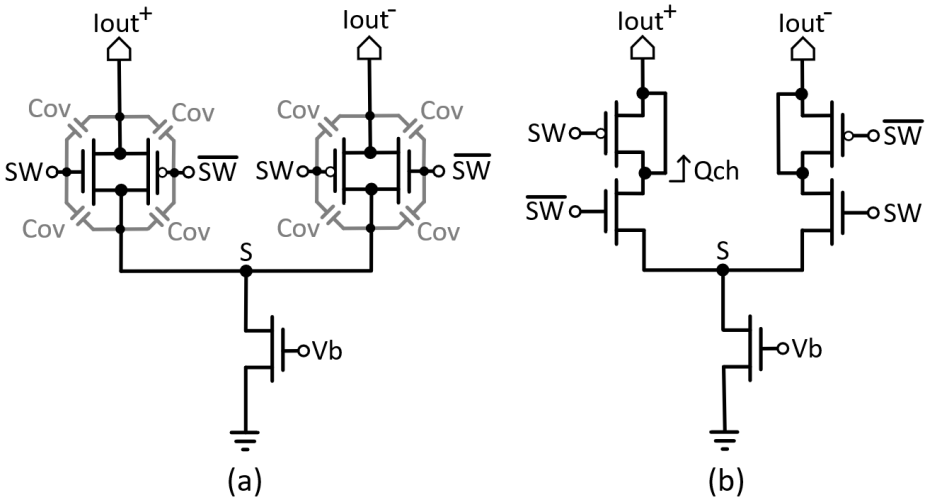

Figure 3.11: N-type CS cell with added current switch transistors to compensate for (a) charge-feedthrough (b) charge-injection.

and current disturbances also arise in the output and internal nodes of the CS cell. Common causes of disturbances include charge-feedthrough and charge-injection [39]. The former originates from the overlap capacitance, C_{ov}, between gate-to-source and gate-to-drain terminals of the device, whose voltage error, ΔV_{ov}, at the drain or source of the current switch transistor with a load capacitance with respect to ground, C_L, and a voltage swing at the gate, V_{sw}, is determined by

$$\Delta V_{ov} = V_{sw} \frac{C_{ov}}{C_{ov} + C_L}. \tag{3.51}$$

For the latter, if the current switch transistor operates in linear region, the voltage error, ΔV_{ch}, from the channel charge-infection to the output is obtained as

$$\Delta V_{ch} = \frac{WLC_{ox}V_{eff}}{2C_L}, \tag{3.52}$$

with W and L the width and length, C_{ox}, the gate capacitance per unit area and V_{eff} the effective voltage of the current switch transistor. Proposed solutions to counteract for the aforementioned disturbances are presented in Fig. 3.11. Here, additional current switch transistors controlled by their complementary signals in each branch are used to cancel out the disturbances if perfect switching alignment between the signals SW and $\overline{\text{SW}}$ is achieved, otherwise, this can lead to remaining disturbances at the output. Nevertheless, the utilization of more current switch transistors results in augmented power consumption and area utilization. Moreover, code-dependent voltage variations in the common-node (S)

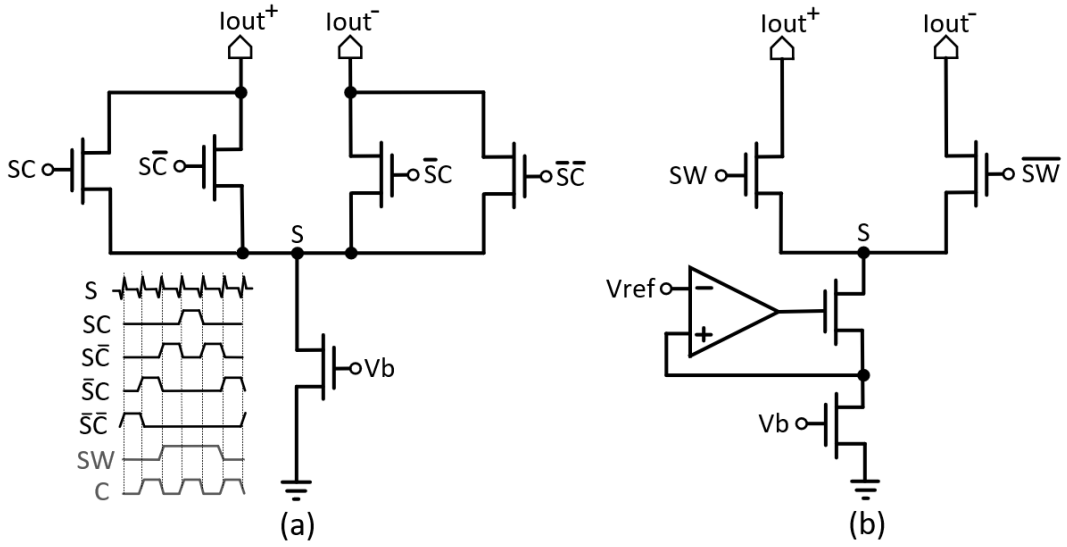

Figure 3.12: (a) CS cell with (a) quad-switching (b) gain boosting technique.

can be observed as a result of finite isolation with respect to the output node. Thus, degrading the dynamic performance with HD, which for the HD_3 case, this is given by [23]

$$\text{HD}_3 = \frac{\pi f Z_L C_u N}{4A_{sw}}, \tag{3.53}$$

with A_{sw} the gain of the current switch transistor, Z_L the load impedance, C_u the capacitance in the common-node (S) with respect to ground and N the CS DAC resolution, N. Since A_{sw} is inversely proportional to g_{ds}^{-1} in (3.53) [23], this suggests to increase the channel length of the current switch transistor so that the linearity is not degraded even from low signal frequencies. A technique that sets an switching activity seen at the common-node (S) twice the sampling rate, $2f_s$, is the so-called differential quad-switching (DQS) [41], [57]. Essentially, the code-dependent distortion is eliminated and the disturbances are translated outside the signal bandwidth. However, this also requires fast settling in the internal nodes to avoid memory effects. The circuit implementation and an example of the signal waveforms are illustrated in Fig. 3.12(a). Yet, the utilization of DQS requires to generate the control signals SC, S$\overline{C}$, $\overline{S}$C and $\overline{SC}$ that increase the area utilization, switching activity and power consumption. Alternatively, the gain boosting technique can be implemented as shown in Fig. 3.12(b). Here, variations in the common-node (S) are sensed by the operation amplifier which controls the cascode transistor to counteract for voltage and current variations at the drain of the current source transistor [58]. Nevertheless, bandwidth limitations in the operation amplifier can constrain its effectiveness at high-speed operation.

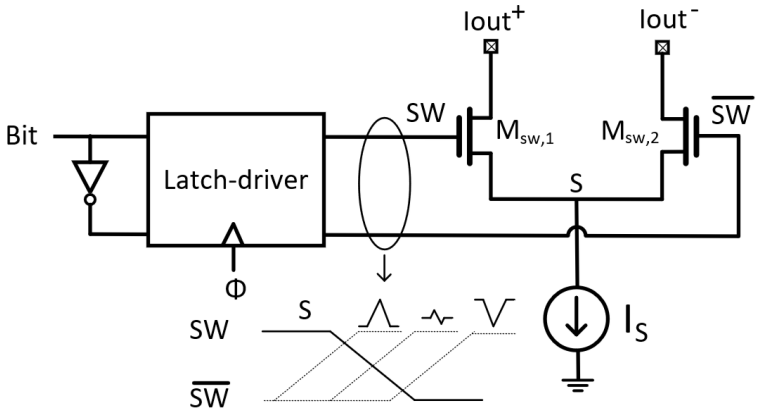

Figure 3.13: Switching transitions and crossing-point scenarios.

On the other hand, it is desired to maintain an optimum crossing point between the complementary switching transitions of the control signals SW and $\overline{\text{SW}}$ that leads to a minimum disturbance in the common-node (S). However, if this is not achieved, then other sources of error originate. This is exemplified with different crossing-point scenarios in the control signals and their effect in the common-node (S) voltage variation in Fig. 3.13. The switching asymmetry between SW and $\overline{\text{SW}}$ can be caused intentionally from the switching drivers or from timing errors associated with time skew and jitter. If large disturbances are seen at the common-node (S), the output voltage is compromised with longer settling times that lead to inter-symbol interference (ISI). Hence, it is preferred to maintain the voltage as constant as possible in the common-node (S). A design consideration consist of avoiding abrupt voltage changes that can also drive into linear region the current source transistor. The voltage in the common-node (S) is set by the gate voltage in the current switch transistors, therefore, the voltage excursion at the gate needs to be large enough such that the current source transistors remain in saturation while the current is steered between the complementary outputs, I_{out}^{+} and I_{out}^{-}. This sets a limit to the voltage level in the control signals to carry out the current switch transitions with minimum perturbation and this is presented in more detail in Section 3.3.3. Overall, it is required to utilize drivers that generate fast and balance complementary switching transitions between the control signals SW and $\overline{\text{SW}}$. Conventional circuit solutions include the current-mode logic (CML) and complementary CMOS logic drivers. The former for a single driver stage is presented in Fig. 3.14(a) with a voltage swing $\Delta V = V_H - V_L$ determined by the supply voltage, V_{dd}, the driver's load resistance, R_L, and the tail current, I_b so that $V_H = V_{dd}$ and $V_L = V_{DD} - I_b R_L$. Yet, CML drivers introduce

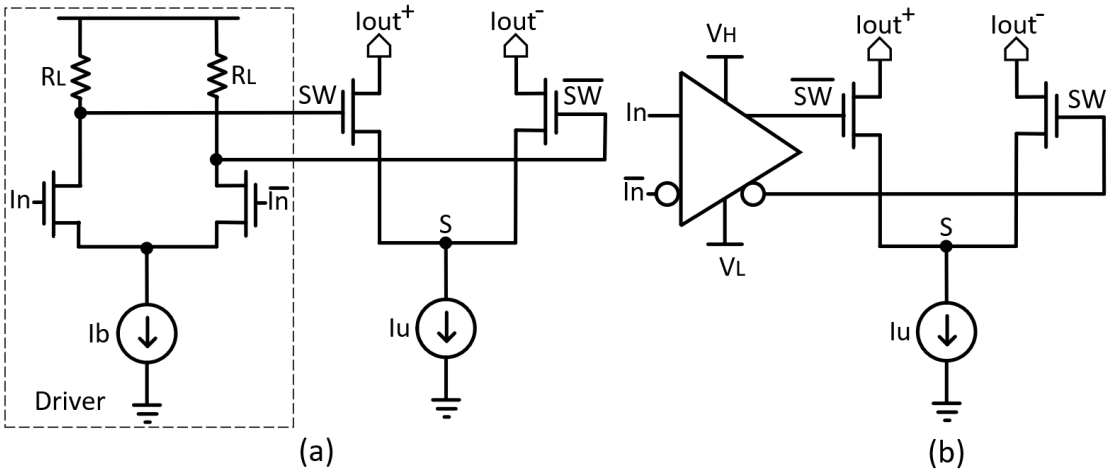

Figure 3.14: Switching drivers (a) current-mode logic (CML) (b) static CMOS logic to generate the control signals SW and $\overline{\text{SW}}$.

static power consumption from I_b, which can considerably increase if more than one driver stage is required to meet the speed specifications [23]. Rather, static complementary CMOS logic can be employed to avoid static power consumption. In Fig. 3.14(b) a simple representation is shown with a differential inverter and supply voltages V_L and V_H.

Another design consideration has to do with the mismatch in the current switch transistors, which translates into a time skew between the complementary switching transitions. The time skew is mainly determined by the variation in the threshold voltage, the gate capacitive of the current switch transistors and the driving capability of the switching drivers. Despite that larger dimensions in the MOS devices lead to a smaller variation in the threshold voltage [52], it increases their gate capacitance. Hence, utilization of current switches of reduced size in combination with strong switching drivers is desired to counteract for this time skew with fast switching control signals [59]. Moreover, the timing circuits and switching drivers are subjected to mismatch, which results in time skews as well as differences in the rising and falling times of the control signals SW and $\overline{\text{SW}}$. Therefore, it is required to attain fast switching transitions in the internal nodes of these circuits to mitigate for these timing issues as well as their propagation to the current switch transistors.

3.3.3 Timing circuits

Timing of the digital input data is essential to maintain synchronization between the switching transitions and avoid distortion in the analog output. Also, with higher demands for signal bandwidth, they become key components in terms of switching speed and power consumption. In addition, as the complexity increases exponentially with the CS DAC resolution N, simple timing circuits are the preferred option. Conventional static timing circuits implemented in CMOS are presented next. From Section 3.2, the power consumption in complementary CMOS digital circuits reduces to

$$P_c = P_{dynamic} + P_{short-circuit} + P_{leakage}. \tag{3.54}$$

In (3.54), P_c approximates to $P_{dynamic}$ and $P_{short-circuit}$ with increments in f_s since they are proportional, whereas $P_{leakage}$ remains constant. Typical timing metrics, include the setup-time, hold-time and propagation-delay. Besides, in CS DACs with complementary outputs, it is important to generate fast switching transitions so that the current can be rapidly steered from one output to the other. Hence, the switching-delay is also introduced in this work. In Fig. 3.15(a), the timing diagram of the input and output voltage transitions of the timing circuit, including the propagation-delay, t_{c2q}, and switching-delay, $t_{d,sw}$ are shown. The synchronization is achieved through the rising-edge of the clock signal, Φ, with SW and $\overline{\text{SW}}$ the control signals driving the switching transistors of the CS cell.

From Fig. 3.15(b), the conditions for I_s to be steered between the complementary outputs I_{out}^- and I_{out}^+ consider the voltage difference between SW and $\overline{\text{SW}}$, ΔV_{sw}, so that $\Delta V_{sw} = V_{sw,h} - V_{sw,l}$ with $V_{sw,h} > V_{sw,l}$ and $t_{d,sw}$. Then, regarding the CS cell shown in Fig. 3.13, if $M_{sw,1,2}$ operate in saturation, the gate voltage $V_{G_{sw,1,2}}$ can be expressed from the square-law model of the transistor as

$$V_{G_{sw,1,2}} = \sqrt{\frac{2i_s}{K}} + V_s + V_{th}, \tag{3.55}$$

with K, V_{th} and V_s the transistor gain factor, the threshold voltage of $M_{sw,1,2}$ and the voltage in the common-node (S), respectively. In (3.55), $V_{sw,l}$ is obtained as $V_{sw,l} = V_s + V_{th}$ with $i_s = 0$ and $V_{sw,h} = V_s + V_{th} + \sqrt{2I_s/K}$ with $i_s = I_s$ Therefore,

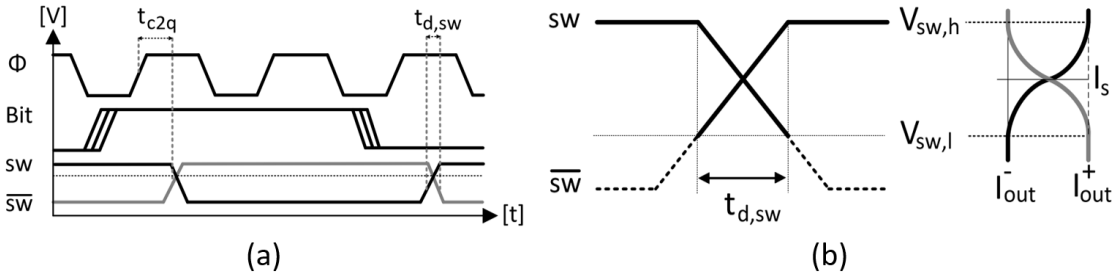

Figure 3.15: Complementary switching transitions (a) timing diagram (b) steering of the output current [60].

ΔV_{sw} becomes

$$\Delta V_{sw} = \sqrt{\frac{2I_s}{K}}. \tag{3.56}$$

Further, $V_{sw,h}$ can reach up to the largest supply voltage for the technology at hand and $V_{sw,l}$ reduce to V_{th} with V_s approximated to zero volts. Hence, the largest range of the voltage, ΔV_{sw}, can be expressed as

$$\max[\Delta V_{sw}] = \lim_{V_s \to 0} \Delta V_{sw} = V_{dd} - V_{th}. \tag{3.57}$$

In a similar manner, the time needed to carry out the voltage excursion $\max[\Delta V_{sw}]$ is referred to as $\max[\Delta t_{d,sw}]$. Although a more linearized response is obtained in short-channel devices, the presented analysis is utilized to compare the performance between different supply voltages. A brief description of the operation of the conventional static CMOS latch-driver circuits is given with t_c and t_d the charging and discharging times of the internal node voltages and with t_p the propagation delay in the output inverters, respectively.

First, the RAM-type circuits are shown in Fig. 3.16. One pull-down network is set by either In or $\overline{In}$ so that the node X or $\overline{X}$ gets discharged. This is followed with the charing of the complementary output node by the cross-coupled inverters, which in turn, generates a delay between the falling and raising transitions. In Fig. 3.16(a), $t_{sw,r}$ is sequential, and therefore, given by

$$t_{sw,r} \approx t_{d,Y} + t_{d,(X,\overline{X})} + t_{c,(\overline{X},X)} + t_p. \tag{3.58}$$

Further, the circuit shown in Fig. 3.16(b) reduces $t_{d,Y}$ in (3.58) since the internal node Y or $\overline{Y}$ begins to discharge prior to evaluation with Φ equal to logic high.

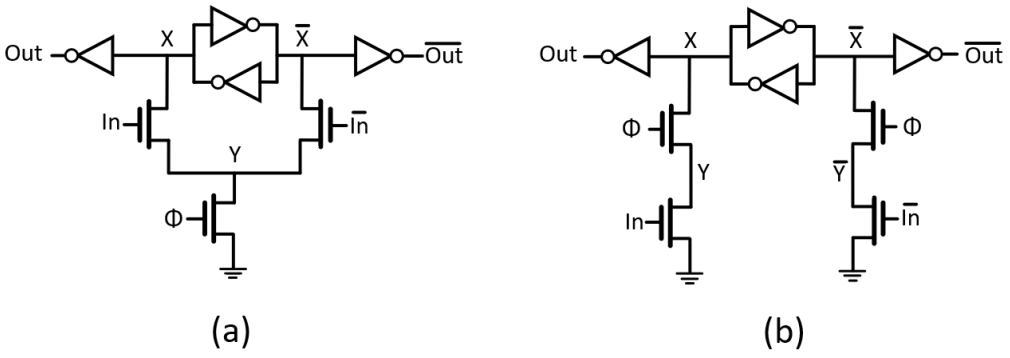

Figure 3.16: RAM-type latch-driver circuits [60]

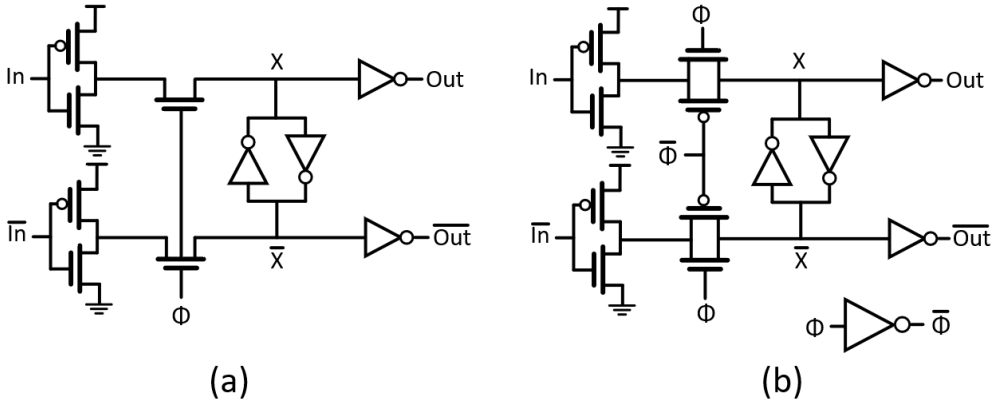

Figure 3.17: PT-type latch-driver circuits [60].

Thereafter, the clocked NMOS transistors are switched on and as the node capacitance Y or $\overline{Y}$ also charges, $t_{c,(X,\overline{X})}$ is then more prolonged.

On the other hand, the pass-transistor (PT) latch-driver circuits are shown in Fig. 3.17 (a) and (b). The former sets a pull-down network to discharge the internal node X or $\overline{X}$ to ground through one NMOS transistor controlled by Φ. Conversely, its counterpart is switched off since the threshold voltage, V_{th} is larger than the gate-source voltage and the cross-coupled inverters assist with the (dis)charge activity in the complementary node. The switching transition $t_{sw,p}$ is given by

$$t_{sw,p} \approx t_{d,c,(X,\overline{X})} + t_{c,d,(\overline{X},X)} + t_p. \tag{3.59}$$

In Fig. 3.17(b), the switches are implemented with transmission gates, which requires a complementary clock signal, $\overline{\Phi}$, thus increasing the power consumption and area utilization. With the alignment in the switching transition between Φ and

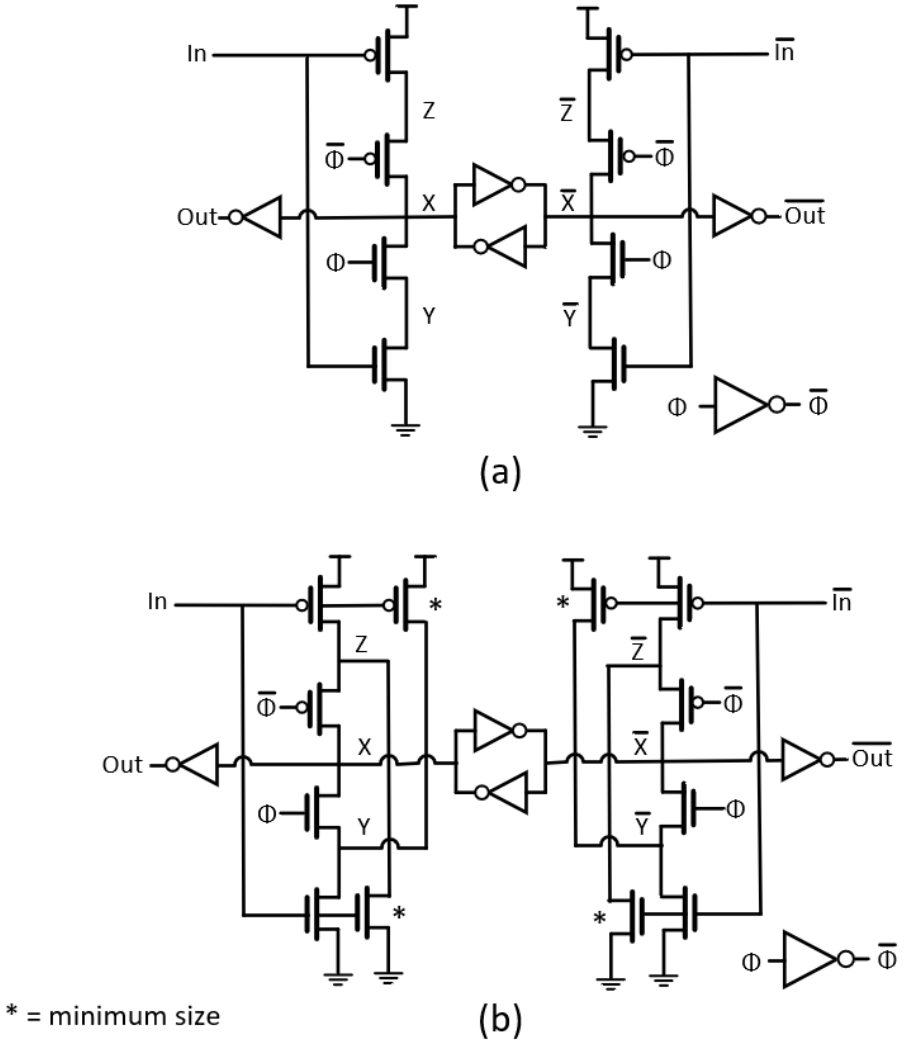

Figure 3.18: C^{2}MOS-type latch-driver circuits [60].

$\overline{\Phi}$, the (dis)charging activity take place in parallel, reducing (3.59) to $t_{d,c,(X,\overline{X})} + t_p$. Since the input drivers integrate the signal path, they are also considered to be part of the latch-driver circuit in the analysis. Lastly, in Fig. 3.18, the clocked CMOS (C^{2}MOS) latch-driver circuits are presented. The C^{2}MOS circuits resemble that in Fig. 3.17(b), but with unfolded nodes Y, Z and $\overline{Y}$, $\overline{Z}$. As the NMOS and PMOS transistors can have different sizes, the raising and falling transitions can differ due to the difference in the node capacitances Y, $\overline{Y}$ and Z, $\overline{Z}$. The asymmetric switching transitions, $t_{sw,c}$, is given by

$$t_{sw,c} \approx \max[t_{d,(X,Y)}, t_{c,(X,Y)}] + t_p. \tag{3.60}$$

Alternatively, the circuit shown in Fig. 3.18(b) incorporates extra NMOS and

PMOS transistors to (dis)charge the internal nodes before evaluation. This results in a reduced $t_{sw,c}$ between the complementary outputs since less time is needed to (dis)charge the internal nodes.

Proposed latch-driver circuit

To strive for fast switching transitions with attained low-power consumption, a proposed latch-driver circuit, utilizing a single clock phase is presented. The circuit solutions are shown in Fig. 3.19(a). The delay in the complementary transitions is reduced since the nodes, X and $\overline{X}$, charge and discharge, or vicevversa, simultaneously. If $\Phi = 0$, the internal nodes Y and Z are charged to V_{dd}, otherwise, one of these nodes is discharged to ground. Then, during a complementary transition either the node X or $\overline{X}$ gets discharged. Moreover, the PMOS in grey and the stacked NMOS transistors in the crossed-coupled inverters are controlled by the nodes Y and Z, thus resulting in a ratio insensitive charging activity. Hence, the size of the transistors can be reduced in comparison with other structures, which leads to less parasitic capacitances in the nodes X and $\overline{X}$ as well as switching-delay. Also, for the NAND gates, the PMOS transistors can be of minimum size. Important to mention that the crossing-point can be adjusted from the NMOS transistors in the NAND gates and the auxiliary PMOS transistors controlled by Y and X [60]. However, a circuit that integrates a control voltage to modify the crossing point between the complementary transitions is shown in Fig. 3.19(b), which permits to dynamically adjust against process-voltage-temperature (PVT) variations. Overall, a reduction in area and power consumption can be attained in comparison with other fast latch-drivers.

Performance comparison

To evaluate the performance, the latch-drivers are implemented in an industrial 65 nm CMOS process. The width of the PMOS/NMOS transistors is 2.16 and 1.08 μm, thus a 2:1 ratio for W_p/W_n is set to match the rising and falling transitions. Minimum size transistors are used for the cross-coupled inverters. For the proposed latch-driver, both the auxiliary PMOS transistors as well as the NMOS transistors in the NAND and are sized with $W_{n,p}$ equal to 0.81 μm. In Fig. 3.20, the

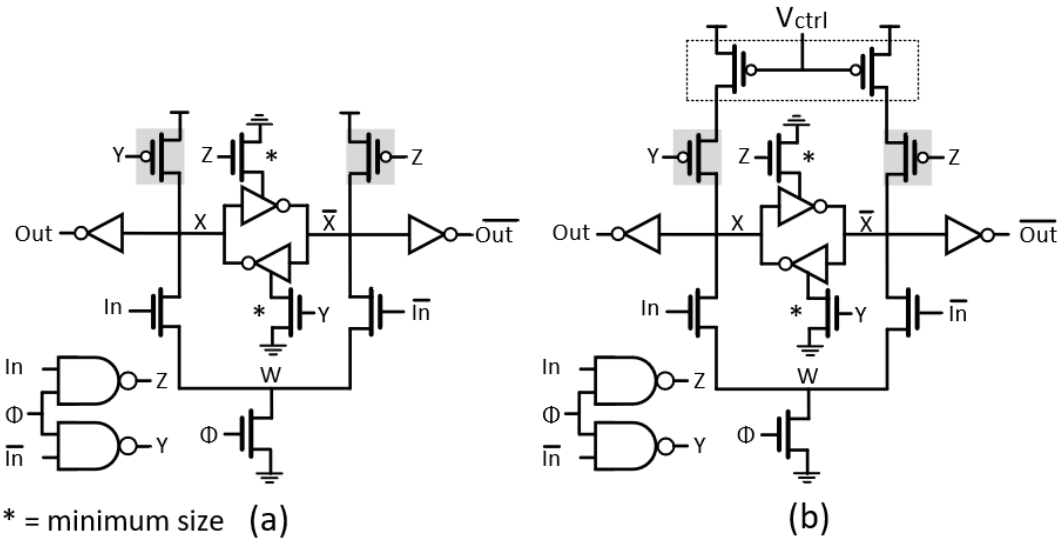

Figure 3.19: Proposed latch-driver circuits [60].

layout of the latch-driver circuits are presented. The latch-drivers characteristics are listed in Table 3.3. A chain of input buffers is used to drive the latch-driver circuits with dimensions with respect to the minimum size by 1×, 3× and 9×. The power consumption is expressed as $P_c = P_{latch} + P_{driver,\Phi} + P_{driver,B}$ with the last two terms including the contribution of the last driver stage for the data and clock signal. The switching-delay, $t_{d,sw}$, is obtained from the time required to reach an output voltage equal to $0.9 \cdot V_{dd} - V_{th}$ with $V_{th} = 0.45\ V$.

Finally, the switching activity, f_s and the capacitive output load are set to 0.5, 1 GHz and FO4, respectively. In Fig. 3.21, the switching-delay, $t_{d,sw}$, versus the supply voltage is presented. The performance of the proposed latch-driver approximates with the fast dual-phase-clocked circuits, *4* and *6*, as a result of parallel rising and falling transitions, and reduce parasitic capacitance to be discharged in the nodes X and $\overline{X}$. Besides, *1* and *2* attain the largest $t_{d,sw}$ due to their sequential operation, whereas for *3* the $t_{d,sw}$ approaches to the fastest solutions. Further, the clock-to-q delay, t_{c2q}, and power consumption versus the supply voltage are shown in Fig. 3.22 (a) and (b). The solutions *2* and *3* present the lowest t_{c2q} as a result of the simple circuit design and reduced parasitic capacitances. On the other hand, from Fig. 3.22 (b), the dual-phase-clocked circuits consume most power consumption with the proposed solution presenting a reduction of 30% in average with respect to *4* and *6*. This shows a significant saving in power consumption since $t_{d,sw}$ is not reduced. In comparison with the

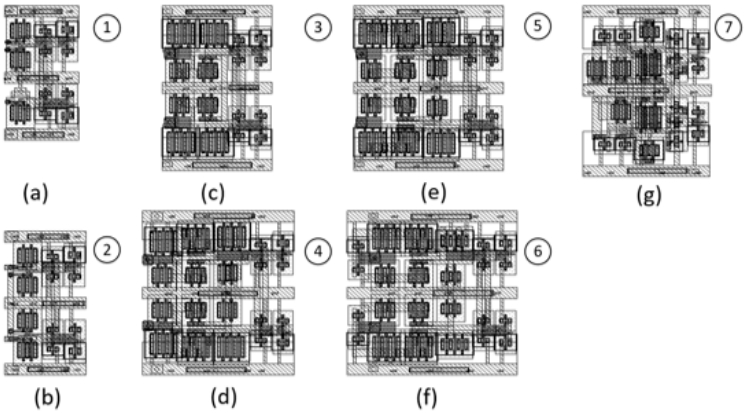

Figure 3.20: Layout RAM (a)-(b), PT (c)-(d), C^{2}MOS (e)-(f), Proposed (g) [60].

Table 3.3: Comparison of latch-driver circuit implementations [60].

N°	Type	T†	CT‡	MT‡	Area (μm^2)	Clocked	Fig
1	RAM	11	1	4	11.9	Single	Fig. 3.20(a)
2	RAM	12	2	4	13.9	Single	Fig. 3.20(b)
3	PT	14	2	4	21.5	Single	Fig. 3.20(c)
4	PT	18	6	4	29.2	Dual	Fig. 3.20(d)
5	C^{2}MOS	18	6	4	29.2	Dual	Fig. 3.20(e)
6	C^{2}MOS	22	6	8	33.2	Dual	Fig. 3.20(f)
7	Proposed	23	5	10	25.7	Single	Fig. 3.20(g)

† T as the total number of transistors. ‡ CT and MT as clocked and minimum size transistors without the output inverters.

RAM latch-drivers, *4* and *6* reach around 2.4$\times$ more power consumption and 5.9$\times$ lower $t_{d,sw}$, while *5* reports around 2$\times$ and 5.4$\times$, respectively.

Also, the product between the power consumption with the propagation-delay, $t_{c2q} \cdot P_c$, as well as the switching delay, $t_{d,sw} \cdot P_c$, are plotted versus the supply voltage in Fig. 3.23 (a) and (b). Note that *4*, *5* and *6* have the largest $t_{c2q} \cdot P_c$ with the proposed solution reducing the energy consumption by 25% approximately. Furthermore, the results for $t_{d,sw} \cdot P_c$ are normalized with 0.95 pJ, corresponding to the minimum obtained value. Note that the proposed latch-driver achieves the lowest $t_{d,sw} \cdot P_c$ in the entire supply voltage range. This shows a favorable trade-off between the power consumption and switching-delay in comparison with *4*, *5* and *6* by about 30% reduction. Besides, regarding the latch-drivers *1* and *2*, the latch-drivers *3*, *4*, *5* and *6* have a lower $t_{d,sw} \cdot P_c$ with a reduction of about 55%, whereas for the proposed latch-driver the reduction is around 70% instead.

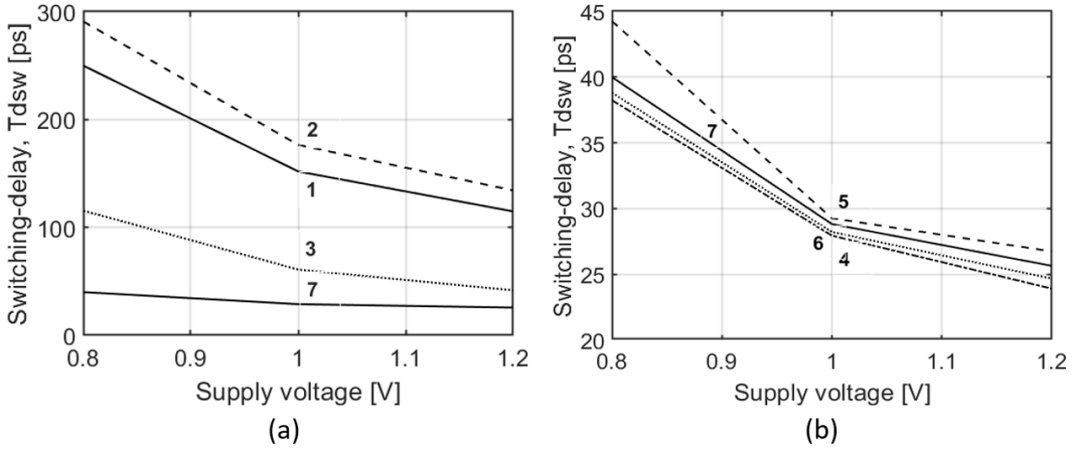

Figure 3.21: Timing circuits switching-delay, $t_{d,sw}$, (a) single- (b) dual-phase-clocked versus the supply voltage [60].

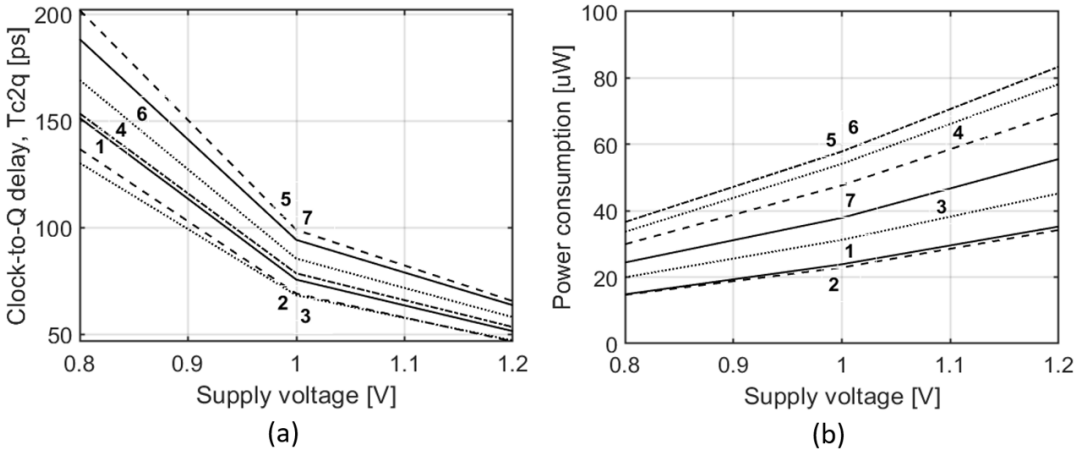

Figure 3.22: Timing circuits (a) clock-to-q delay, t_{c2q}, (b) power consumption versus the supply voltage [60].

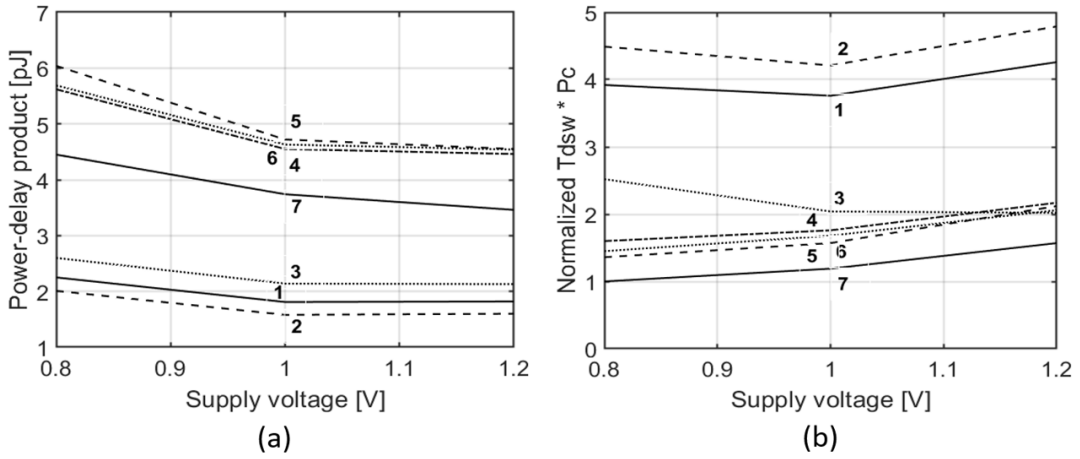

Figure 3.23: Timing circuits (a) power-delay product, $t_{c2q} \cdot P_c$, (b) normalized product $t_{d,sw} \cdot P_c$ versus the supply voltage [60].

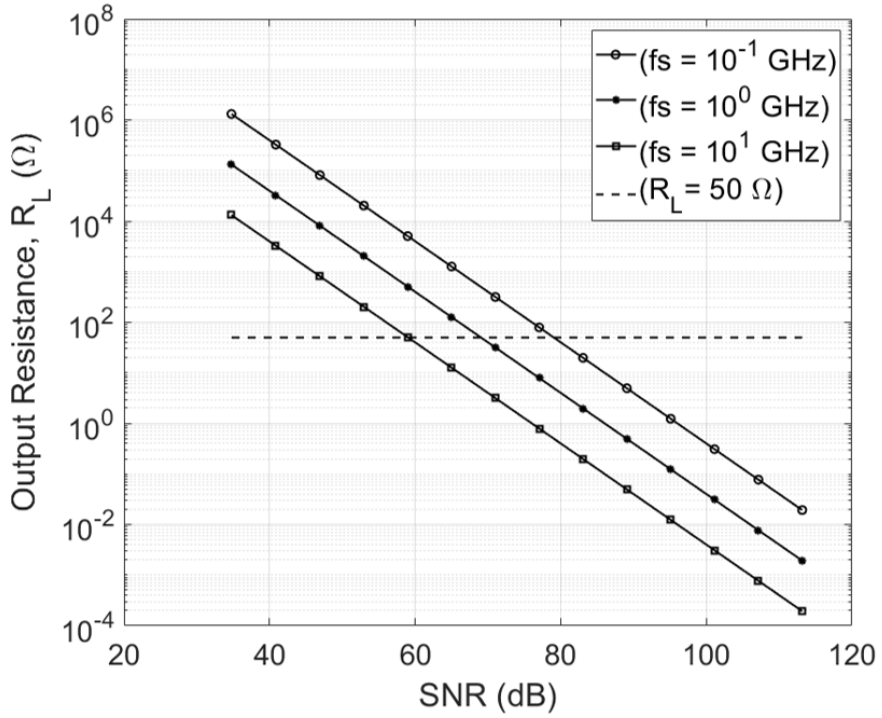

Figure 3.24: R_L versus the SNR for the noise bound and fixed $V_{sw,d} = 1\,V$ for f_s equal to 0.1, 1, and 10 GHz [8].

3.3.4 Output load resistance

Other design aspect corresponds to the selection of the output load resistance, R_L. Commonly, a R_L of 50 Ω is chosen to facilitate the impedance matching with other building blocks, including RF baluns, reconstruction filters. Furthermore, the unary-current, I_u can be calculated by

$$I_u = \frac{V_{sw,d}}{2(2^N - 1)R_L}. \tag{3.61}$$

From (3.61) and with fixed values for R_L and $V_{sw,d}$, the magnitude in I_u is reduced exponentially for a larger CS DAC resolution, N. As presented in Section 3.2, this can compromise the CS DAC performance [8]. Alternatively, I_u can be obtained from the SNR and SFDR requirements to latter find the optimum R_L. The utilization of a matching network can be considered to achieve maximum power transfer and impedance matching between the CS DAC and the other external building blocks. To illustrade, the R_L versus the SNR is plotted for different f_s in Fig. 3.24. The dash line is for R_L = 50 Ω, where the crossing points are obtained with an f_s equal to 10^1 10^0 and 10^{-10} GHz and an SNR of about 60, 70, 80 dB,

respectively. For the SNR values with $R_L \geq 50\ \Omega$, an R_L = 50 Ω can be used as the SNR is not compromised. However, farther than the intersection points with a higher values in the SNR, the R_L should be selected from the energy consumption bound for noise instead. Likewise, the analysis can be extended to the speed and linearity energy consumption bounds.

3.4 Enhancement techniques

Techniques to improve the performance in DACs will be presented in this section. In essence, their utilization requires the integration of more circuitry that augments the complexity, power consumption and area utilization in the DAC. Hence, a trade-off between the aforementioned design aspects and performance needs to be considered. These techniques are classified as randomization, calibration and predistortion.

3.4.1 Randomization

Randomization also referred to as dynamic element matching (DEM) is largely implemented in CS DACs [30], [61]–[63]. It re-shuffles the DAC's elements selection randomly in a sample basis, thus decorrelating systematic and stochastic errors within the signal's period, T. HD as a result of amplitude errors, e.g., the current sources of a CS DAC is transformed into a noise representation, thus improving the SFDR at the cost of increased noise power. The integration of an stochastic network for an unary-weighted DAC is illustrated in Fig. 3.25. Initially, the N-bit binary-weighted digital input word, X, is thermometer decoded. Next, the stochastic network with the utilization of random control signals change the selection of the unit DACs through the input-output mapping between [T_1,..,T_{2^N-1}] and [S_1,..,S_{2^N}]. To explain the effect of randomization in the output signal, let's consider a general case with amplitude errors in the DAC elements. Considering a periodic input sequence X and its period $T = N_T T_s$ with N_T and T_s, the number of samples and the sampling period, respectively, the error function, erf, is also periodic. Hence, erf can be expressed as a Fourier series with $F_s = 1/T_s$,

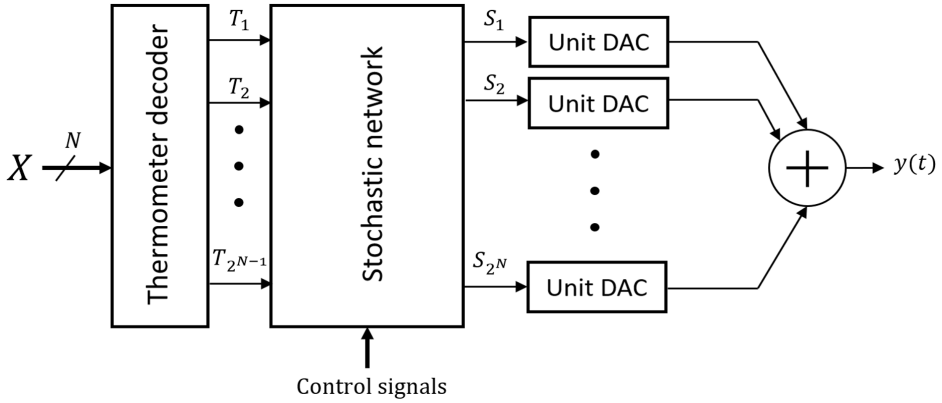

Figure 3.25: Integration of an stochastic network with an array of unary-weighted DACs.

$f_k = kF_s/T$ and $t_n = nT_s$ so that

$$\text{erf}(n) = R_0 + \sum_{k=1}^{N_T/2} R_k \cos(\omega_k t_n + \phi_k), \tag{3.62}$$

with $\omega_k = 2\pi f_k$, $R_0 = \frac{1}{N_T}\sum_{n=1}^{N_T} \text{erf}(n)$, $R_k = \sqrt{(a_k^2 + b_k^2)}$, $\phi_k = \tan^{-1}(\frac{b_k}{a_k})$, $a_k = \frac{2}{N_T}\sum_{n=1}^{N_T} \cos(\omega_k t_n)\text{erf}(n)$ and $b_k = \frac{2}{N_T}\sum_{n=1}^{N_T} \sin(\omega_k t_n)\text{erf}(n)$. R_k^2 is proportional to the power of each tone at ω_k. Then, normalizing R_k^2 by $4/N_T^2$, it yields

$$R_k'^2 = \left[\sum_{n=1}^{N_T} \cos(\omega_k t_n)\text{erf}(n)\right]^2 + \left[\sum_{n=1}^{N_T} \sin(\omega_k t_n)\text{erf}(n)\right]^2. \tag{3.63}$$

Expanding (3.63) and reordering terms, we get

$$R_k'^2 = \text{erf}(n)^2 + \sum_{n=1}^{N_T} \sum_{\substack{m=1 \\ \forall n \neq m}}^{N_T} (\Lambda_{k,nm} + \Gamma_{k,nm})\, \text{erf}_{(n,m)}, \tag{3.64}$$

with $\text{erf}_{(n,m)} = \text{erf}(n)\text{erf}(m)$, $\Lambda_{k,nm} = \cos(\omega_k t_n)\cos(\omega_k t_m)$, and $\Gamma_{k,nm} = \sin(\omega_k t_n)\sin(\omega_k t_m)$. From (3.64), the expectation is obtaned as

$$E\{R_k'^2\} = \overline{\text{erf}(n)^2} + \sum_{n=1}^{N_T} \sum_{\substack{m=1 \\ \forall n \neq m}}^{N_T} (\Lambda_{k,nm} + \Gamma_{k,nm})\, \overline{\text{erf}_{(n,m)}}, \tag{3.65}$$

with $\overline{\text{erf}_{(n,m)}}$ = $E\{\text{erf}(n)\text{erf}(m)\}$ the covariance, $\text{cov}_{n,m}$, of the errors erf(n) and erf(m). Also, $\text{cov}_{n,m}$, relates to the correlation coefficient, $\rho_{n,m}$, by

$$\rho_{n,m} = \frac{\text{cov}_{n,m}}{\sigma_n \sigma_m}, \tag{3.66}$$

where σ_n and σ_m correspond to the standard deviation of the errors for the time instances n and m, respectively. If there is correlation between the errors, the second term in (3.65) is larger than zero along with an increment in the k-th tone's average power. On the other hand, with a decorrelation between the errors at different samples, $E\{R_k^2\}$ is reduced and referred to as $E\{R_k^2\}_{drr}$. Then, from (3.65), $E\{R_k^2\}_{drr}$ is bounded by

$$E\{R_k'^2\}_{drr} < E\{R_k'^2\}. \tag{3.67}$$

Thus, with the sample errors' de-correlation, the power of the HD components is reduced, in turn, improving the SFDR. On the contrary, if the errors are decorrelated, (3.65) is reduced to $\overline{\text{erf}(n)^2}$, corresponding to the variance of the error, σ_e^2. Although improved linearity can be obtained through randomization, it adds hardware overhead with the utilization of pseudo-random number generators (PRNG) and more interconnects that grow exponentially with the DAC resolution, N [64]. In addition, the augmented switching activity due to the random element selection can considerably increase the power consumption and exacerbate the timing errors.

To illustrate, implementations of stochastic network for a 3-bit DAC are presented in Fig. 3.26 and Fig. 3.27 [65], [66]. The tree structure in Fig. 3.26 adds a 0 as the LSB to the input digital word, X. The switching blocks, $S_{l,k}$, with k the block's number in layer l, split the MSB and LSBs between the switching block outputs, whose selection are determined by the control bit, c_k. Then, the process is repeated in the subsequent switching blocks. If the tree is fully extended to one-bit output, this is referred to as full randomization DEM (FRDEM), otherwise, as partial randomization DEM (PRDEM). Then, Fig. 3.27 presents the butterfly network. First, the binary-weighted digital input data is separated between the switching blocks to be distributed to the output according to the state of the control bits c_k and the interconnection between the switching blocks. Simple implementation of the switching blocks correspond to a pair of multiplexers as shown in Fig. 3.27. Alternatively, other types of switching cells are presented in Fig. 3.28.

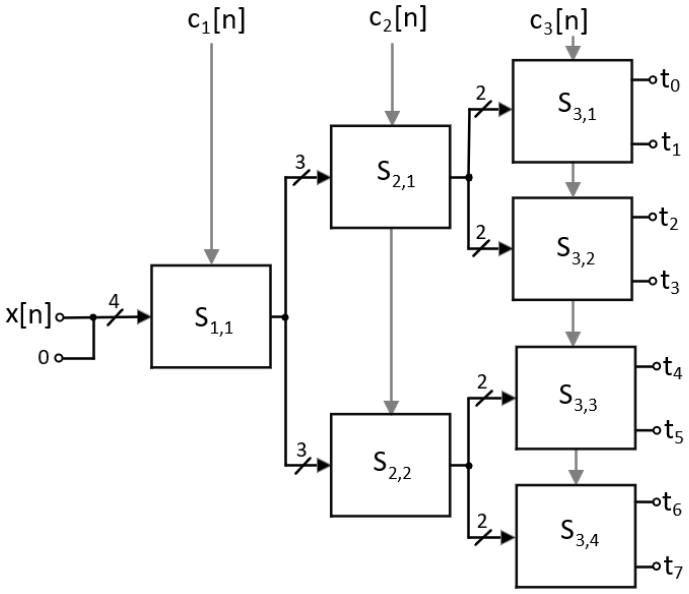

Figure 3.26: Tree stochastic network.

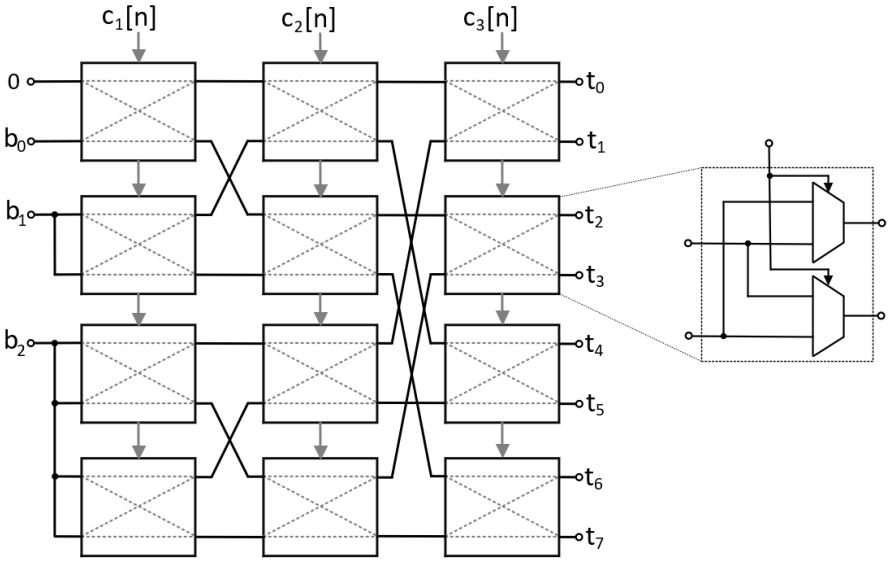

Figure 3.27: Butterfly stochastic network.

To reduce DAC glitches and the switching activity at the output, the switching cell in Fig. 3.28(a) avoids transitions when the input bits differ, i.e., $a_k \neq b_k$, at the same time restraining the random control bit c_k from changing the input-output mapping in the switching cell [68]. Conversely, the switching cell in Fig. 3.28(b) interchanges the input-output mapping if the input bits are the same, in turn, generating a code-dependent randomization [66]. However, it does not avoid complementary bit transitions that lead to DAC glitches. Both implementations require a register to keep the previous state, thus adding extra clock load that

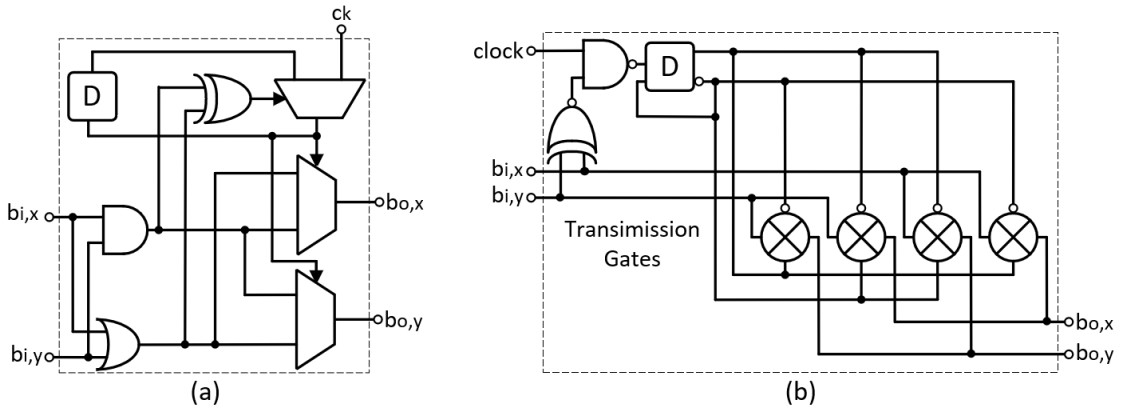

Figure 3.28: Switching block with (a) reduce glitching (b) code-dependent randomization.

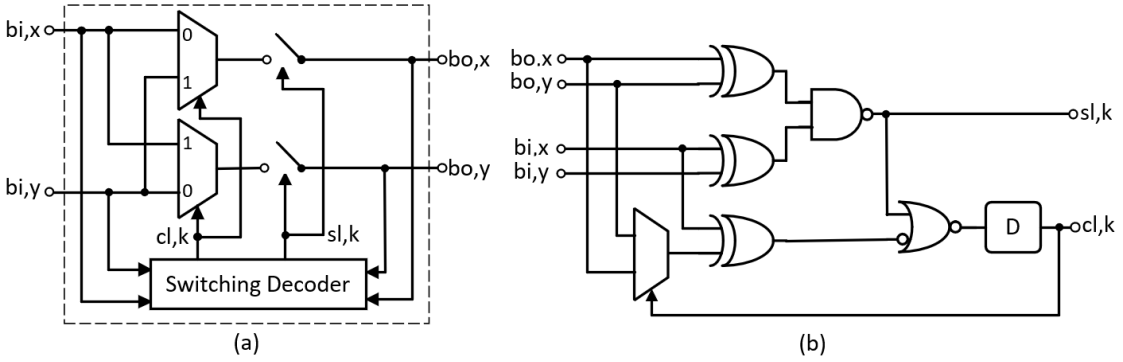

Figure 3.29: Proposed switching (a) block (b) decoder [67]

increases the power consumption.

On the other hand, an switching block to reduce the DAC glitches, switching activity and generate code-dependent randomization with no added clock load has been proposed and presented in Fig. 3.29 [67]. The input-output mapping state is changed once a complementary switching transition is identified by the decoding logic. It operates asynchronously with the register triggered by the rising edge of the decoded signal from the NOR gate. This inverts the state of $c_{l,k}$ that sets the selection in the multiplexers. Thus, the input-output mapping can be formulated as

$$\delta(n) = [b_{i,x(n)} \oplus b_{i,y(n)}][b_{o,x(n)} \oplus b_{o,y(n)}]b_{\Delta(n)}, \tag{3.68}$$

with $b_{\Delta(n)}$ equal to either $[b_{i,x(n)} \oplus b_{o,x(n)}]$ or $[b_{i,y(n)} \oplus b_{o,y(n)}]$. As the input-output mapping can be changed between consecutive bit input sequences, $c_{l,k}$ is assigned to the k^{th} switch in layer l and the input-output mapping is then given

Table 3.4: Truth table of the interchange switch [67].

$b_{ix(n)}$	$b_{iy(n)}$	$b_{ox(n)}$	$b_{oy(n)}$	$s_{l,k(n)}$	$c_{l,k(n)}$
0	0	0	0	1	$c_{l,k(n-1)}$
0	0	0	1	1	$c_{l,k(n-1)}$
0	0	1	0	1	$c_{l,k(n-1)}$
0	0	1	1	1	$c_{l,k(n-1)}$
0	1	0	0	1	$c_{l,k(n-1)}$
0	1	0	1	0	$c_{l,k(n-1)}$
0	1	1	0	0	$c^*_{l,k(n-1)}$
0	1	1	1	1	$c_{l,k(n-1)}$
1	0	0	0	1	$c_{l,k(n-1)}$
1	0	0	1	0	$c^*_{l,k(n-1)}$
1	0	1	0	0	$c_{l,k(n-1)}$
1	0	1	1	1	$c_{l,k(n-1)}$
1	1	0	0	1	$c_{l,k(n-1)}$
1	1	0	1	1	$c_{l,k(n-1)}$
1	1	1	0	1	$c_{l,k(n-1)}$
1	1	1	1	1	$c_{l,k(n-1)}$

by

$$\begin{bmatrix} b_{o,x} \\ b_{o,y} \end{bmatrix} = \begin{bmatrix} b_{i,x} \\ b_{i,y} \end{bmatrix}, \text{ if } c_{l,k} = 0, \tag{3.69}$$

and

$$\begin{bmatrix} b_{o,x} \\ b_{o,y} \end{bmatrix} = \begin{bmatrix} b_{i,y} \\ b_{i,x} \end{bmatrix}, \text{ if } c_{l,k} = 1. \tag{3.70}$$

Besides, if $\delta(n) = 1$, the control bit $c_{l,k}$ changes at the time instant n its state, which is formulated as

$$c_{l,k}(n) = c^*_{l,k}(n-1) \iff \delta(n) = 1. \tag{3.71}$$

Table. 3.4 lists the states of the switching decoder. Additionally, to expose the switching blocks to different input bits from layer-*1* in the array, it is proposed to interleave the segmented binary-weighted digital input bits as shown in Fig. 3.30. Thus, complementary bit transitions between the MSB and LSBs are avoided in the switching blocks with no change in the output data while exchanging the input-output mapping.

A comparison between the number of transitions in the butterfly networks implemented with different number of layers for a 10-bit DAC and the thermometer-decoded is carried out for a 1024-point single-tone vector close to DC. The results are listed in Table 3.5. An $f_{sig} \to DC$ is chosen to generate high switching activity without the utilization of a thermometer decoder. As expected, the

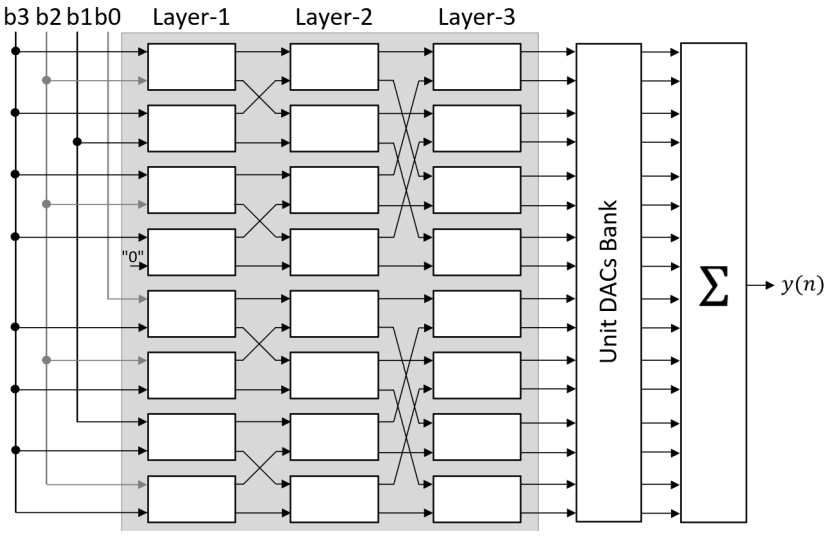

Figure 3.30: Butterfly network with interleaved indirect-binary segmented digital data for a 4-bit DAC [67].

Table 3.5: Transitions count (1000's) for $f_{sig} \rightarrow DC$ [67].

Thermometer decoded	No BN	Proposed BN Layer-3	Proposed BN Layer-6	Proposed BN Layer-9
2.04	15.1	10.1	4.74	3.43

thermometer-decoded output reports less number of transitions, and therefore, it generates less switching activity. Moreover, if no interchange input-output mapping is utilized in the butterfly network with no, the transitions' count increase considerably. On the other hand, with the utilization of the proposed butterfly network array for a layer-3 configuration, the transitions count decrease. Then, if a layer-6 network is considered, then the switching activity is further reduced with less transitions count by around $2\times$ when compared with a layer-3 network. Then, for a layer-9 network the transitions count approximates to the thermometer-decoded's output.

Moreover, a comparison with other switching networks is presented in Table. 3.6. As mentioned, the proposed network reduces the number of switches to $N-1$ with respect to the standard butterfly network. This also benefits with less number of random control signals if they are utilized [3]. Also, independence between the state of the input-output mapping in the switching blocks permit to extend the number of permutations. Regarding the transitions count, a considerable reduction is obtained through the exchange between the complementary bit transitions

[3]This can be integrated through the NOR gate in Fig. 3.29(b) with an extra control input.

Table 3.6: Switching networks and transitions count (1000's) for $f_{sig} \rightarrow DC$ [67].

Switching Network	N° Switches	Control signals	Permutations	Transitions count
FRDEM	$2^{N+1} - N - 2$	N	2^N	259.7
Butterfly	$N \cdot 2^{N-1}$	N	2^N	262.6
Proposed	$(N-1) \cdot 2^{N-1}$	$N-1$	$2^{N \cdot (N-1)}$	3.43

with the proposed solution. The other networks utilized random control bits in a sample basis to generate full randomization at the cost of a considerable increase in the number of transitions.

Regarding the level of randomization through the input digital sequence also referred to as code-dependent randomization, this is treated in more detail next. To further evaluate the performance, the proposed butterfly network with the interleaved binary-weighted input data and the proposed switching cell are implemented in MATLAB. The amplitude errors, ΔI_u, are integrated in the DAC's units and modeled as a Gaussian random variable with $N(0, \sigma^2)$ and σ the standard deviation. The simulation results for DAC resolutions of 8-, 10-, 12- and 14-bit with and without the use of the interchange mapping for a mismatch error in the range from 10^{-4} to 10^{-1} are presented in Fig. 3.31. For the comparison, signal tones set with $f_{sig}/f_s \approx 0.113$ and ≈ 0.475 are utilized. Lastly, each data point corresponds to an extended 400-point Monte Carlo simulation with an FFT of 1024-point. Notice that as N is larger, the dynamic performance is more sensitive to amplitude mismatch errors. This is observed for a 14-bit DAC that shows a decay of about 10 dB between 10^{-3} and 10^{-2}. However,the SFDR remains almost constant for an 8-bit DAC within the same range. Then, a drop of 20 dBc/decade is obtained between 10^{-2} and 10^{-1}. The aforementioned observations agree with (3.6). Overall, an SFDR's improvement of about 4 dB is achieved in average for a mismatch amplitude error of 10% with the utilization of interchange mapping.

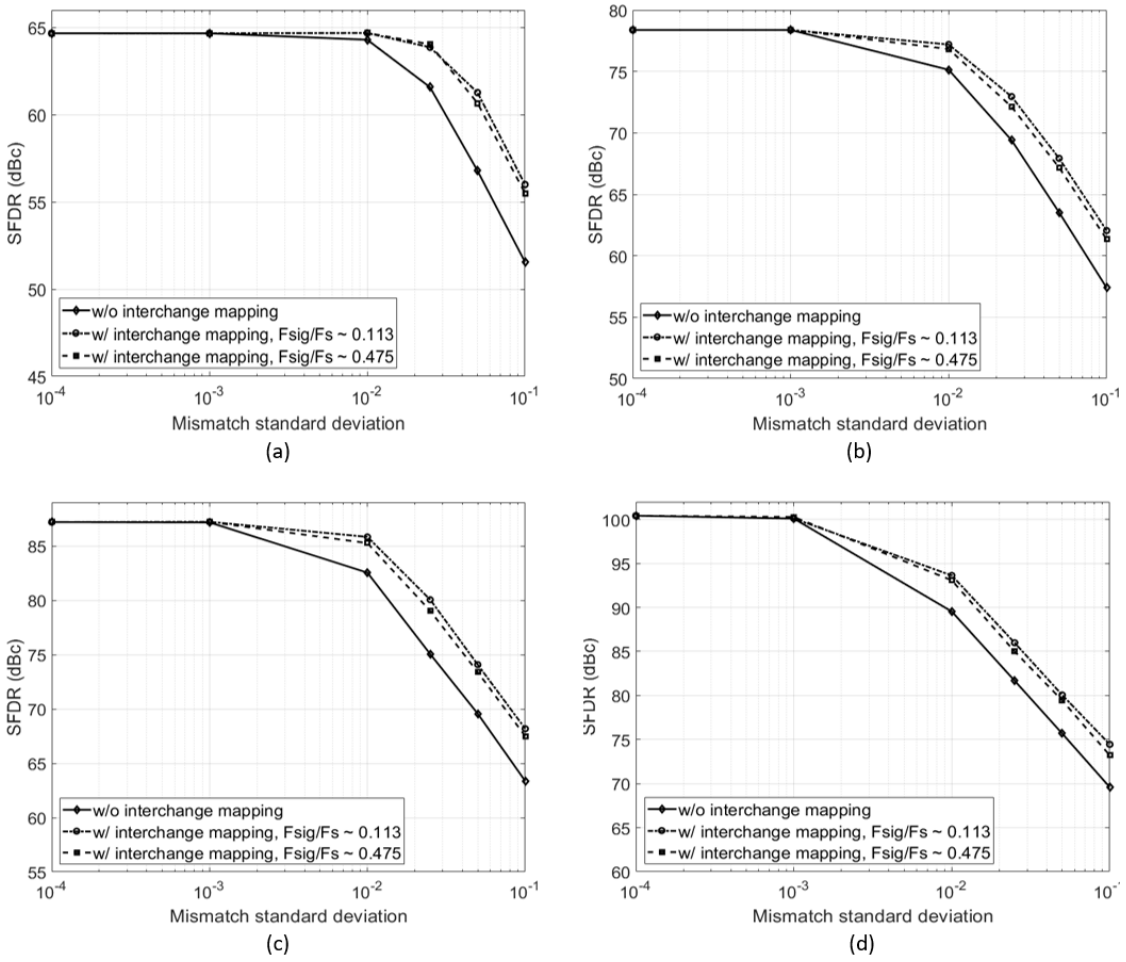

Figure 3.31: SFDR versus amplitude error with and without butterfly network and interchange mapping for $N-1$ layers at $f_{sig}/f_s \approx 0.113$ and $f_{sig}/f_s \approx 0.475$ for a (a) 8-bit (b) 10-bit (c) 12-bit and (d) 14-bit DAC.

3.4.2 Calibration

Calibration is a conventional enhancement technique for error correction in data converters [20]. This has been largely employed to compensate for amplitude errors, however, with increased demands on high-speed operation, calibration for timing mismatch is also reported [10], [69]. Calibration is classified as foreground and background [20], [23]. The former is part of the start-up process and it is executed only once, whereas the latter is implemented to perform recursive calibration during normal operation. In CS DACs, amplitude error correction is carried out through adjustments in the output current either globally or locally as shown in Fig. 3.32. With a global scheme, a calibration DAC (CALDAC) is integrated, thus augmenting the load capacitance [70]. A control unit is required to set the output current compensation as well as an ADC to measure the analog

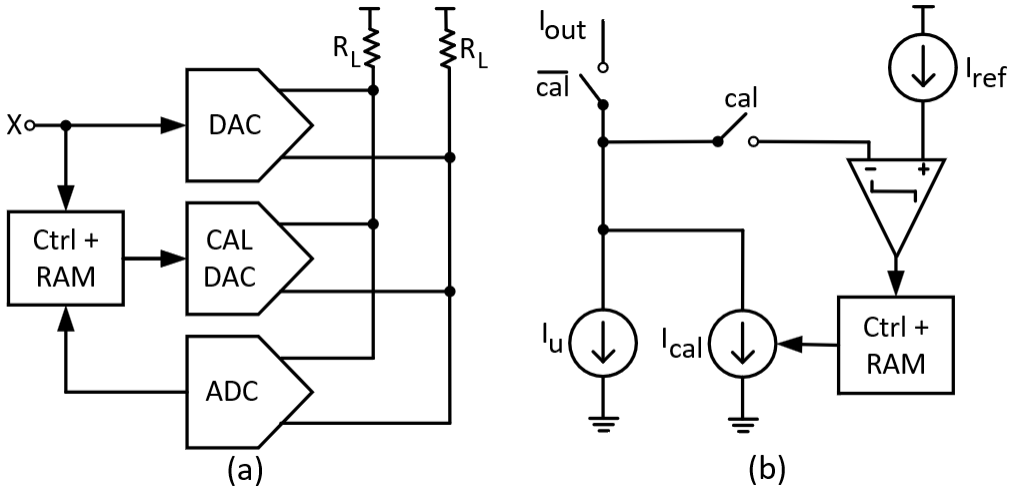

Figure 3.32: Calibration strategies in CS DACs (a) global (b) local.

output, thus forming mixed-signal loop. Yet, the control unit needs to set CAL-DAC with the appropriate output current, which can compromise the operation at high-speed while increasing the power consumption.

Alternatively, with a local calibration scheme each current cell incorporates an auxiliary CALDAC, where the output current, I_{out}, is measured and compared with a reference current I_{ref} to estimate the amplitude error [61], [71]. In addition, an spare current cell can be utilized to substitute the one being calibrated on-the-fly. Furthermore, local calibration can be implemented through a floating current source (dynamically), reducing the complexity of the control logic and no memory utilization [72], [73]. However, this suffers from leakage and requires a fast calibration routine, specially in sub-nm CMOS processes. Other calibration schemes utilize sort-and-combine methods to obtain an switching sequence that results in improved static and dynamic performance [74], [75].

3.4.3 Predistortion

Another technique to linearize the output response of a DAC is known as digital pre-distortion (DPD). In essence, a modified digital input code based on the initial digital sequence, X, is fed into the DAC to compensate for the nonlinear response. A simplified block diagram with the integration of a DPD block at the DAC's input is presented in Fig. 3.33. Hence, for a digital input, $X = [b_{N-1}, ..., b_0]$,

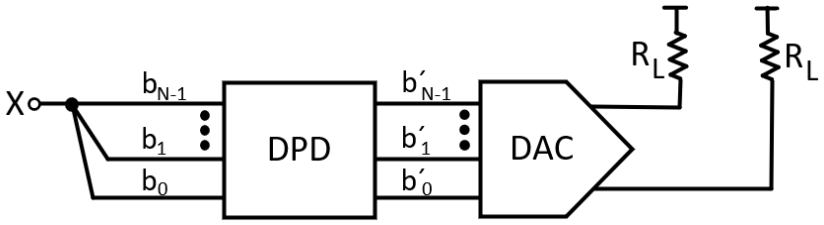

Figure 3.33: Integration of DPD at the CS DAC's front-end.

and a DAC's function, $F_{DAC}(\cdot)$, the distorted analog output, Y_{dist}, can be expressed as

$$Y_{dist}(b_{N-1}, ..., b_0) = F_{DAC}(b_{N-1}, ..., b_0). \tag{3.72}$$

Then, to compensate for Y_{dist} and obtain the ideal output Y, we have

$$Y_{dist}(b'_{N-1}, ..., b'_0) = Y(b_{N-1}, ..., b_0), \tag{3.73}$$

with $(b'_{N-1}, ..., b'_0)$ the modified input bit sequence. From (3.73), it yields

$$b'_{N-1}, ..., b'_0 = Y^{-1}_{dist}[Y(b_{N-1}, ..., b_0)]. \tag{3.74}$$

Thus, the DPD block has to generate $(b'_{N-1}, ..., b'_0)$ according to $Y^{-1}_{dist}[\cdot]$, i.e., $F^{-1}_{DAC}[\cdot]$ from (3.72). Nevertheless, high resolution is required to compensate for the non-linearity. Common implementations of the DPD block utilize look-up tables (LUTs) [34]. However, a chain of comparators have also been proposed to compensate for the nonlinear response due to limited output impedance in CS DACs [37].

Chapter 4

A 10-bit high-speed binary-weighted CS DAC in 65nm CMOS

4.1 Floorplan overview

The block diagram, including the DAC core, on-chip memory with retiming DFFs and clock buffer is illustrated in Fig. 4.1. To counteract for large amplitude and timing mismatch in conventional binary-weighted DAC realizations, the proposed DAC utilizes an unary-weighted approach with the 4 MSBs divided in sub-blocks of equal size. Thus, the switching block is separated in 16 sub-blocks with each containing an array of 64 stacked current cell units of the same size with respect to the LSB for both the digital and analog circuit domains. Indirect binary segmentation, also referred to as pseudo-segmentation [38], is utilized to separate the digital input word for the 4 MSBs, which are split into 15 bit lines. The distribution of the 15 bit lines in the switching sub-blocks are evenly separated for each MSB in an interdigitazed manner to counteract for temperature and process gradients in the physical implementation. Furthermore, to mitigate for disturbances in the analog output as a result of the switching activity of the clock and data signal as well as increase the isolation between the digital and analog domains, local nodes for the output current summation are utilized in the switching blocks, which is presented in more detail in Section. 4.5. Then, the global output node takes

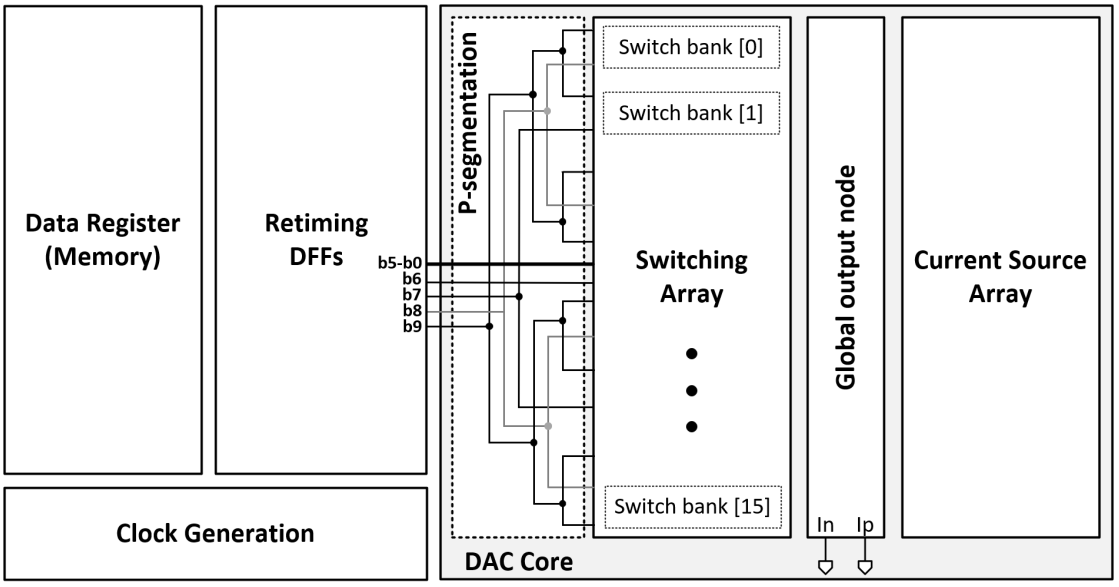

Figure 4.1: Block diagram of the test chip implementation.

the contribution of all current sources accordingly. Moreover, the chip integrates a memory block to store the digital input data and avoid signal integrity issues, e.g., associated with parasitics in the bonding wires. Then, retiming DFFs interface the memory block to the DAC core and send the digital data. Lastly, an external single phase clock signal is utilized and reconstructed on-chip through the clock generation block to drive the other building blocks.

4.2 Current source

The current sources in CS DACs are subjected to systematic and stochastic deviations also referred to as amplitude errors. As mentioned in Chapter. 3, the former can be mitigated with proper layout techniques, the latter is commonly reduced with larger device dimensions [52]. For the static performance, it is desired to bound the DNL and INL in a range of ± 1 LSB and ± 0.5 LSB, respectively, and thus guarantee monotonicity. Yet, in binary-weighted DACs, it is well-known that consecutive mid-code transitions can lead to abrupt variations beyond 1 LSB, thus compromising directly the DNL, which can be approximated for stochastic variations by [53]

$$\text{DNL} \approx \sqrt{2^N - 1}\frac{\sigma(I_u)}{I_u}, \tag{4.1}$$

with I_u and $\sigma(I_u)$, the unary-current and its standard deviation, respectively. Moreover, the stochastic amplitude errors in the current sources translate into HD, thus degrading the dynamic performance from low input frequencies with a reduced SFDR, which is estimated for a differential CS DAC from (3.6) and rewritten below for convenience

$$\text{SFDR} \approx 3(N+3) - 10\log_{10}\left[\frac{\sigma(I_u)}{I_u}\right]^2 \text{ dBc.} \tag{4.2}$$

From the previous expressions, $\sigma(I_u)$ can be estimated to satisfy both the static and dynamic specifications. Also, notice that more stringent requirements need to be attained for $\sigma(I_u)$ as N increases, thus representing a design challenge at high CS DAC resolutions, N. To exemplify, for an SFDR of about 70 dBc in a 10-bit DAC, the normalized standard deviation, $\sigma(I_u)/I_u$, approximates to 2.8%, which results in an DNL close to 0.9 LSB from (4.1) and within the ± 1 LSB range.

On the other hand, a simple global bias circuit shown in Fig. 4.2(a) mirrors the off-chip reference current, I_{ref} to bias the current source array. The mirrored I_{ref} is referred to as I_{global}. Then, local current mirror transistors, evenly arranged in the current array, are utilized to bias the current source transistors. This also counteracts for the mismatch due to the separation between the devices [52]. A reduced circuit schematic of the local bias distribution is presented in Fig. 4.2(b). Moreover, a low impedance analog ground that surrounds the current source array is considered to mitigate for the IR drop.

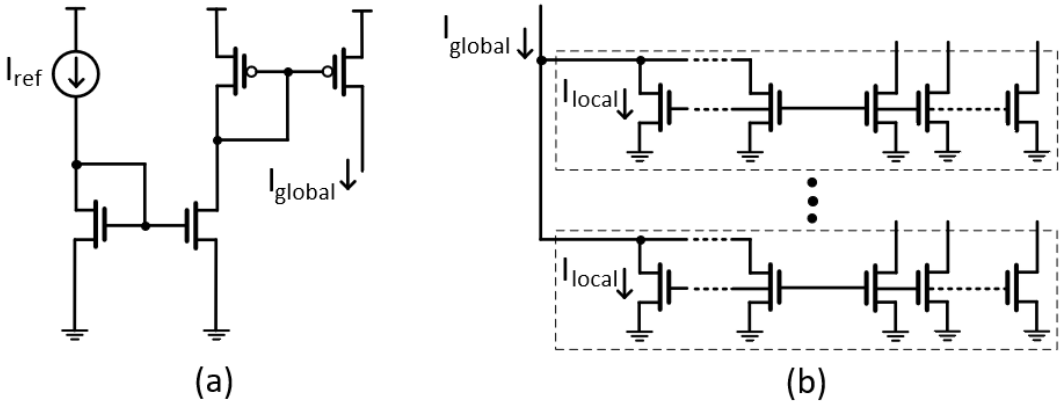

Figure 4.2: Bias network (a) global (b) local distribution.

4.3 Timing circuit and switching driver

Complementary CMOS logic is utilized in the design of the timing circuits and the switching driver. In Fig. 4.3, a simplified schematic of the CS DAC cell is presented. Initially, synchronization of the input bit data is carried out through the timing circuit. Thereafter, the switching driver generates the control signals SW and $\overline{\text{SW}}$ with complementary high-crossing point transitions to drive the switching transistors $M_{sw,1}$ and $M_{sw,2}$ in the N-type CS cell [23]. For the timing circuit, to achieve fast synchronization time as well as generate rapid falling and raising transitions in the output signals Q and $\overline{Q}$, a C^{2}MOS-latch circuit is utilized. However, this requires to generate a complementary clock signal, $\overline{\Phi}$. Further on, the high-crossing point in the switching driver is obtained through the propagation delay of the inverters that control the PMOS transistors in the second stage and with the NMOS transistors controlled by Q and $\overline{Q}$ instead. A low crossing-point is obtained, thus a final stage of inverters is required to reverse the transitions and obtain the high-crossing point accordingly.

The C^{2}MOS-based timing circuit is presented in Fig. 4.4. Since the CS DAC is aimed to operate at high-speed, dynamic CMOS logic is also considered. This avoids to increase the transistors size to counteract for the conventional positive feedback with crossed-coupled inverters in static realizations, and which becomes more relevant in C^{2}MOS latch circuits where stacked NMOS/PMOS transistors are used. As a result, leading to faster switching transitions with less parasitic capacitance in the internal nodes and reduced power consumption. In the C^{2}MOS latch circuits, cross-coupled PMOS transistors of minimum size are utilized to achieve a pseudo-static behavior without requiring to increase the size of the NMOS transistors as well as maintaining one of the complementary output nodes connected to V_{dd}. Yet, design aspects considering current leakage, charge-sharing and charge-feedthrough need to be addressed and will be discussed in more as follows. A critical case is presented in the output node of the C^{2}MOS latch that is discharged to ground during the evaluation period. This can be separated in two scenarios according to the gate input voltage after the evaluation period with $\Phi = 0$ and $\overline{\Phi} = 1$ in the master-latch, or viceversa, in the slave-latch, as explained next.

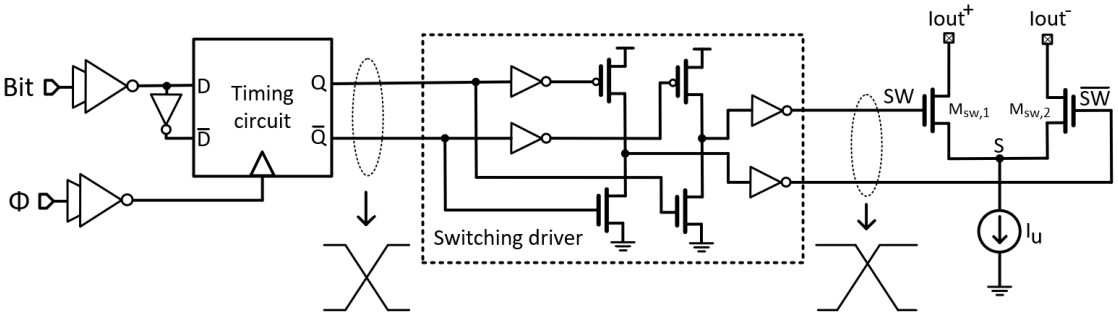

Figure 4.3: Simplified circuit schematic of the CS DAC cell.

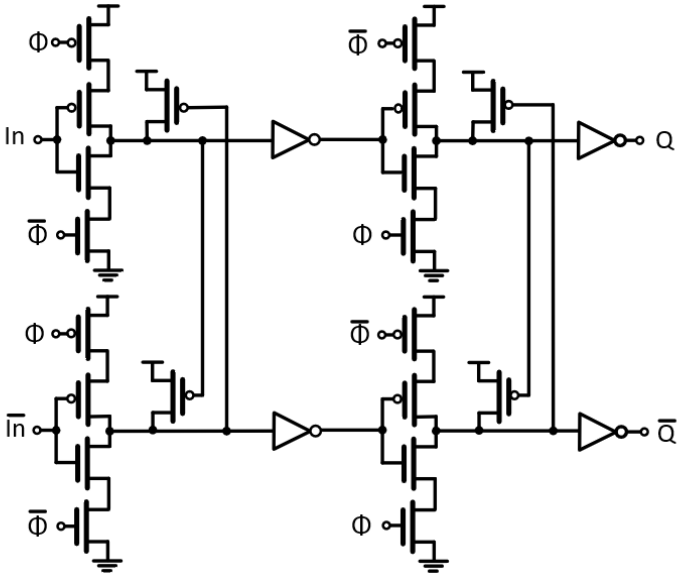

Figure 4.4: C^{2}MOS-based DFF timing circuit.

1) Gate voltage with low-to-high transition in the signal path

In this case, the PMOS transistors are switched off and no charge-sharing between the internal nodes takes place. Nevertheless, voltage in the output node of the C^{2}MOS latch, first discharged to ground, starts to develop as a result of the leakage current, I_{leak}, flowing in the stacked transistor's array. Since, the output node of the C^{2}MOS latch encompasses a larger capacitance to ground with respect to other internal nodes, its voltage response in the time-domain during the hold-on period is then approximated as

$$V_{out}(t) \approx V_{leak}(1 - e^{-t/\tau_o}), \tag{4.3}$$

with $V_{leak} = I_{leak}R_{off,n}$, $R_{off,n}$ the stacked NMOS transistors' off-resistance, τ_o = $R_{off,n}C_o$ and C_o the capacitance at the output node of the C^{2}MOS latch, respectively. Thus, from (4.3), we can derive an expression for the time-off, t_{off}, by

$$t_{off} \approx -\tau_o \ln\left[1 - \frac{V_{out}(t)}{V_{leak}}\right]. \tag{4.4}$$

Moreover, as t_{off} in the worst-case scenario equals half the sampling period, T_s, we can obtain a lower bound for the sampling frequency, f_s, at which we limit $V_{out}(t)$ to a certain output voltage. Therefore, solving for f_s, it yields

$$f_s > -\frac{1}{2\tau_o} \ln^{-1}\left[1 - \frac{V_{out}(t)}{V_{leak}}\right]. \tag{4.5}$$

The critical voltage in $V_{out}(t)$ can be set to the threshold voltage $|V_{th_{n,p}}|$ as this changes the state of the internal voltage nodes, generating an error with a change in the signal code. Hence, this voltage can be considered as a bound condition in (4.5). Furthermore, V_{leak} can develop up to the supply voltage, V_{dd}. As an example, with C_o = 0.1 fF, $R_{n,off}$ = 10^9 Ω, $|V_{th_{n,p}}|$ = 0.4 V and V_{dd} = 1 V, the bound condition from (4.5) results in a f_s of about 100 KHz, which is 4 orders of magnitude farther from the intended f_s.

2) Gate voltage with high-to-low transition in the signal path

Unlike the previous case, charge-sharing occurs between the drain and source nodes in the stacked PMOS transistors while the NMOS transistors are switched off. Since the source node of the PMOS transistor is connected to the output node of the C^{2}MOS latch, the voltage at this node is expected to increase. However, the effect of charge-feedthrough through the miller capacitance in the devices with charge intake from the drain and source nodes in the PMOS transistor as a result of the high-to-low transition, counteracts the charge-sharing effect simultaneously. The overlap capacitance in the NMOS transistors also contribute with the charge intake from the output node. Once the high-to-low transition is completed, I_{leak} starts to charge the output node as explained earlier, where the bound for f_s needs to be considered to avoid undesired changes of the digital data. To illustrade both effects, a transient simulation with the different transitions for an f_s of 1 MHz is presented in Fig. 4.5. Notice that for the case 1, the

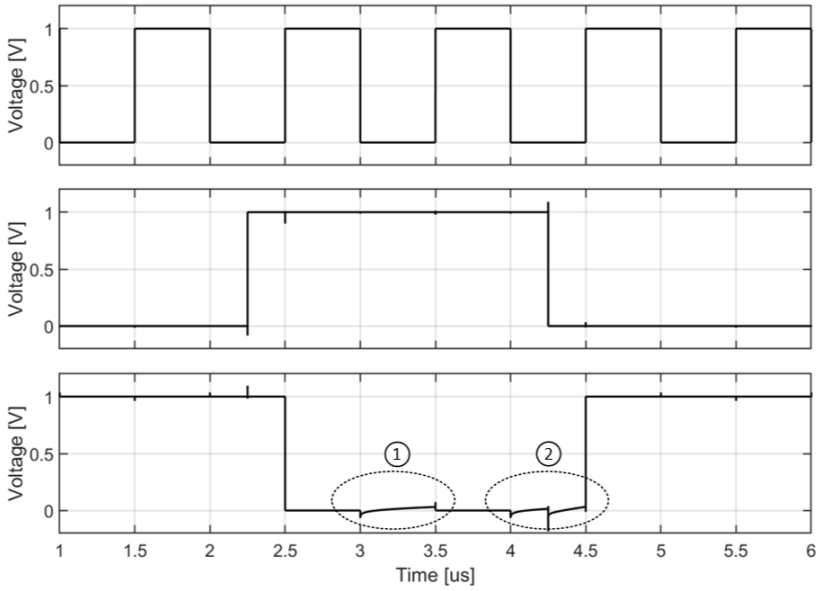

Figure 4.5: Transient simulation of the C^{2}MOS-based latch with the clock (top), input (middle) and output (bottom) signal, at f_s of 1 MHz in 65 nm CMOS.

output voltage starts to increase with $\Phi = 0$. Then, the output node is refreshed to ground with $\Phi = 1$ after half of the clock period, corresponding to 0.5 us. On the other hand, in 2 the output node reaches a negative voltage as the net effect of the charge-feedthrough and charge-sharing. Thereafter, the voltage at the output node starts to increase. In addition, increments in the temperature result in augmented I_{leak} and with the C^{2}MOS-latch structure, we can take advantage of the stack effect to reduce I_{leak} [76].

4.4 Current-steering cell

The N-type CS cell is utilized in the design. To increase the output impedance of the CS DAC without demanding large voltage headroom, a single cascode current source is chosen and presented in Fig. 4.6(a). Minimum size current switch transistors driven into saturation when switched-on are employed, thus contributing with augmented output impedance in the CS DAC. Additionally, this leads to minimum load capacitance, C_L, thus maximizing the signal bandwidth for a load resistance, R_L, and output voltage swing, $V_{o,swing}$. With the CS cell at hand, the voltage variation at the output node, ΔV_o, due to the charge-feedthrough during

the switching transitions can be approximated for $C_L \gg C_{ov}$ as

$$\Delta V_o = V_{sw}\frac{C_{ov}}{C_{ov}+C_L} \approx V_{sw}\frac{C_{ov}}{C_L}, \tag{4.6}$$

where C_{ov} and V_{sw}, are the overlap miller capacitance and the voltage swing at the gate of the current switch transistors, respectively. The ratio C_{ov}/C_L approximates to zero as N is larger, thus counteracting for V_{sw}. On the other hand, the energy consumption due to the switching activity can be approximated for the current switch transistor by [77]

$$E_{sw} \approx W_{sw}L_{sw}C_{ox}V_{sw}^2, \tag{4.7}$$

with $W_{sw}L_{sw}C_{ox}$ and V_{sw}, the gate capacitance and the swing voltage at the gate, respectively. From (4.7), the utilization of switching transistors with reduced size benefit also with less energy consumption, which becomes more significant with larger CS DAC resolution, N. In addition, the utilization of the cascode transistor in the current sources in combination with minimum size switching transistors lead to a reduce parasitic capacitance in the common-node (S) in the CS cell, which benefits with faster voltage settling during the switching transitions, and therefore, less memory effects that degrade the dynamic performance [23], [77]. Nevertheless, careful attention needs to be considered to have large isolation between the output node and the common (S), which can require to increase the size of the switch current transistors and reduce the effect of code-dependent variations in the internal nodes of the CS cell. Similarly, for the physical implementation, it is desired to reduce the parasitic capacitance from the interconnects and mismatch due to the separation of the devices. Hence, the placement of the current switch transistors is in close proximity, which also facilitates to obtain balanced and rapid complementary switching transitions. The voltage levels in the internal nodes of the CS cell are indicated in Fig. 4.6(a). Low threshold voltage devices, $V_{th,l}$ are utilized, resulting in overdrive voltage in the current source transistor, M_{cs}, of about 200 mV. Besides, the layout of the CS cell including the switching and the cascode transistors are presented in Fig. 4.6(b) and with this section being also part of the switching array integrated with the timing circuit and the switching driver. Note that for the common-node (S), the interconnects extends only to the minimum spacing requirements according to the design rules given in the process. The current source transistors are placed in the current

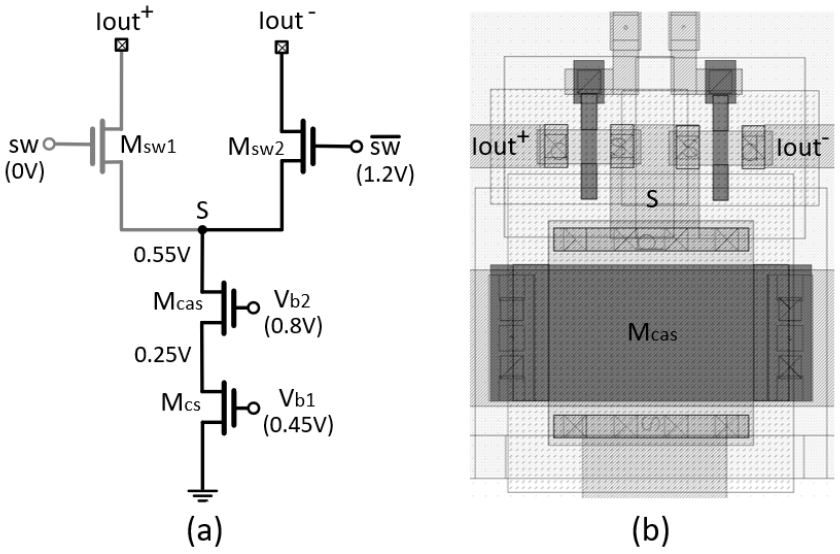

Figure 4.6: The N-type CS cell (a) circuit schematic and (b) layout implementation of the switching and cascode transistors only.

source array. On the other hand, the SFDR for the differential CS DAC can be extended to the impedance case from (4.8) as

$$\text{SFDR} \approx -40 \log_{10} \rho_Y - 12(N-2) \text{ dB}, \tag{4.8}$$

where ρ_Y is the admittance ratio expressed as Z_L/Z_{out} with Z_L and Z_{out}, the load impedance and output impedance of the CS DAC, respectively. From the CS cell, the drain-to-ground capacitance in M_{cs} introduce a pole that due to the dimensions of the current source transistors it locates at low-frequencies. The cascode transistor, M_{cas}, introduces a zero, and therefore, the dimension of the devices are such to approximate the pole and zero location. Thus, to tolerate an SFDR drop of about 15 dBc in the signal bandwidth, $f_s/2$, for a load impedance of 50 Ω and $N = 10$, from (4.8) a Z_{out} of about 300 KΩ is required. Likewise, if the load impedance is reduced then the requirements of Z_{out} are reduced accordingly. In this design, a Z_{out} of about 375 KΩ is obtained at the schematic level for an $f_s/2 \approx 1.9$ GHz.

4.5 Layout considerations

With demands on higher sampling frequencies in the GHz-range, the synchronization between the clock and data signal become more sensitive to timing issues, and therefore, careful attention needs to be considered for these signals' paths in the physical implementation. Since the CS DAC is arranged with an array of interdigitized switching blocks, a balance tree network is selected for the clock signal and illustrated in Fig. 4.7. This is conformed of a global and local tree network with the former being distributed over the switching blocks and the latter distributed in the CS DAC cells of each switching block, respectively. The clock network does not incorporate global repeaters to avoid potential mismatch issues that translate into time skews of in the clock signal and added jitter with both compromising the speed of the CS DAC. Instead, local clock buffers are utilized as shown in Fig. 4.3. Moreover, as the CS DAC cells are of equal size no load balancing techniques are required to reduce timing errors [78], which also leads to less layout complexity and power consumption.

Similarly, the current addition of each CS cell becomes more relevant as the signal frequency increases, where it is desired to achieve a concurrent current superposition at the output, and thus avoid distortion due to current delays. Likewise, the output node is separated into a global and local node implemented as a tree structure with the former being also presented in Fig. 4.7. On the other hand, considering the routing of the digital signal, the MSB attains the critical path with half of the switching blocks evenly distributed under its control. Conversely, the signal's path for the other input bits is shorter. The CS DAC cells in the switching blocks are arranged to avoid overlaps between the digital and analog signals paths, which otherwise, can lead to code-dependent distortion, e.g., as a result of the switching activity in the digital domain. The switching array scheme is presented in Fig. 4.8 with A and D referring to the analog and digital circuitry, respectively. Also, a local output node is implemented in each switching block of the array. To achieve matching between the current addition, the local output node is implemented as a stacked tree structure with the metal layers 1-5. The distribution of the 16 switching blocks is directly mapped to the current sources in the same interdigitized manner, thus mitigating for systematic errors, e.g., temperature and process gradients, as well as simplifying the routing with no complex switching scheme. Further, common practices with the

use of substrate contacts in the switching blocks and in the current source array to isolate the analog domain as well as the utilization of dummy transistors surrounding the current source array are taken into consideration to avoid mismatch issues.

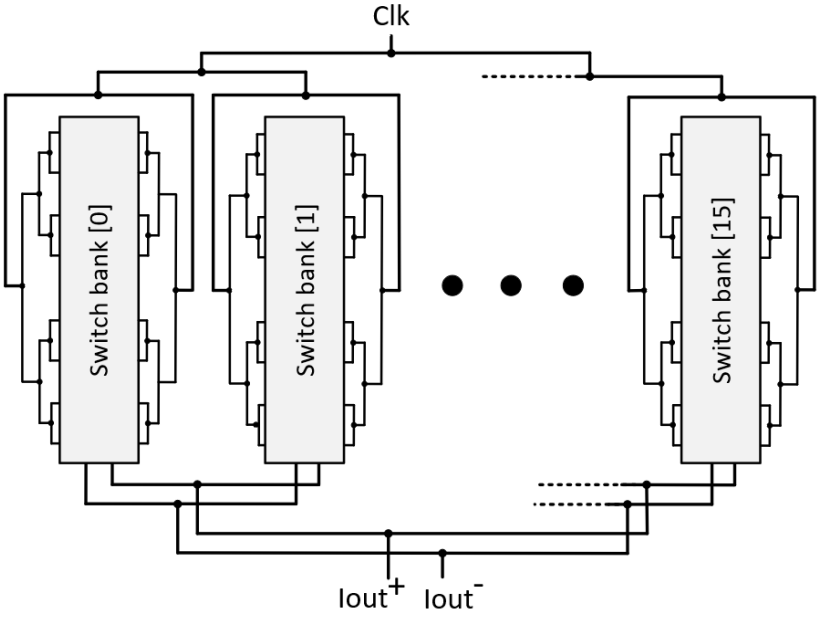

Figure 4.7: Clock network and global output node tree structures sketch of the CS DAC with differential outputs currents I_{out}^{+} and I_{out}^{-}.

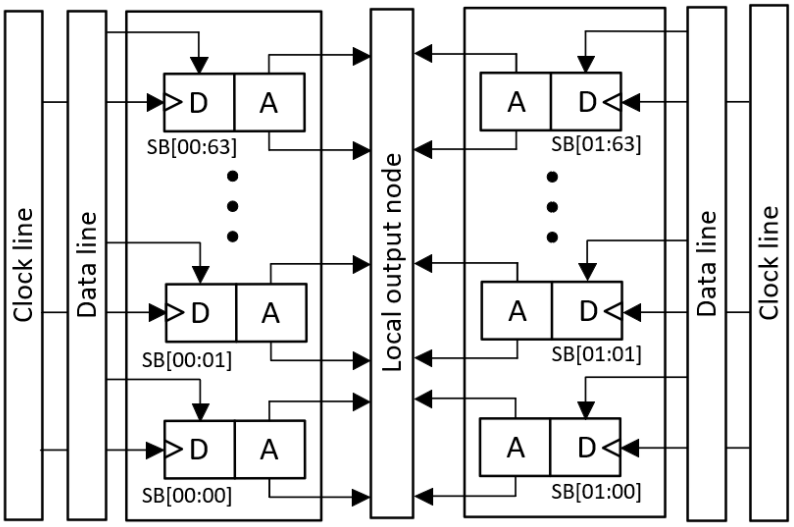

Figure 4.8: Simplified diagram of the digital and analog circuits in the switching blocks array.

4.6 Chip implementation

The 10-bit binary-weighted CS DAC was implemented in an industrial low-power 65 nm CMOS process. The layout of the chip is presented in Fig. 4.9 and occupies a total area, including the I/O ring of about 2.38 mm^2, whereas the area of the DAC core is about 0.67 mm^2. The chip integrates three power/ground supply domains to decouple the noise, including one for the clock generation, on-chip memory and retiming DFFs as well as two more for the digital and analog supplies in the DAC core. Multi-layer of metal-to-metal capacitors are utilized for the decoupling capacitors. The full-scale output current is 16 mA.

4.6.1 Testing methodology

In Fig. 4.10 the on-chip test setup is presented. First, an array of shift registers to achieve high-speed reading operation is implemented and they conform the memory block with a word length of the digital input sequence of 64-bit [79]. Thus,

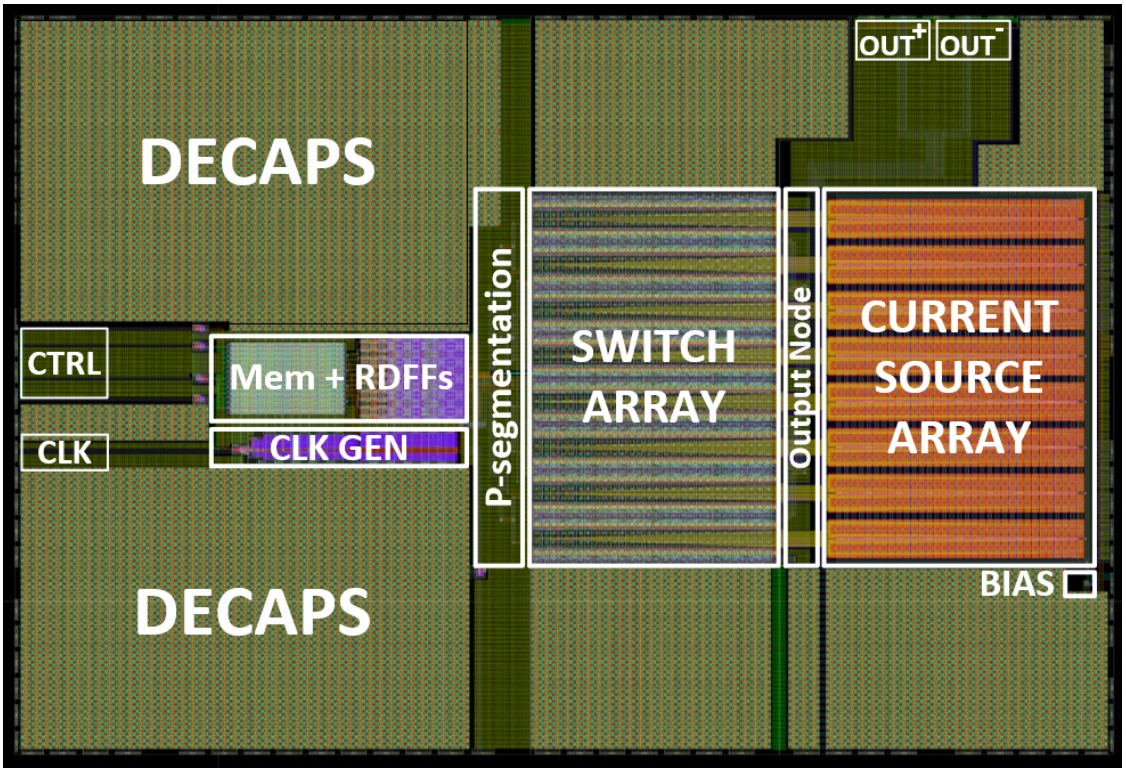

Figure 4.9: Layout of the chip, on-chip memory, retiming DFFs and clock generation (left) and DAC core (right).

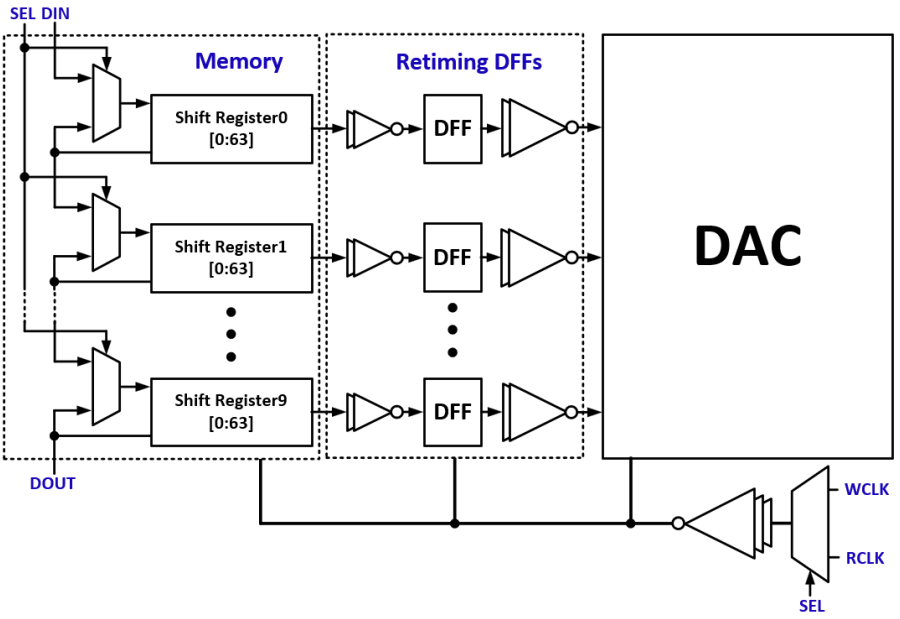

Figure 4.10: On-chip test setup.

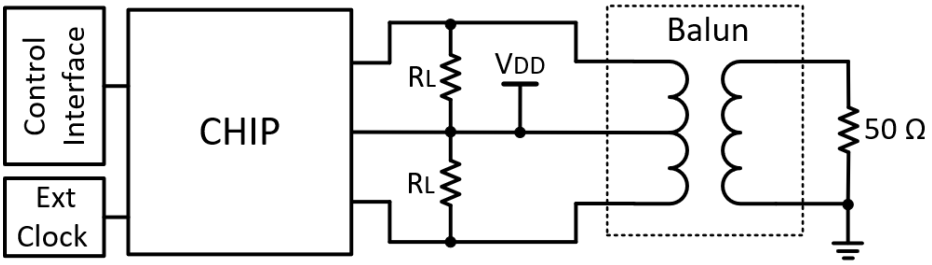

Figure 4.11: Test bench

each input bit stores 8 bytes for a total of 80 bytes storage (10-bit). The writing process is serial through the array from DIN and setup with SEL=0. Otherwise, the digital input data periodically rotates in each separate shift register array during the reading process. Further on, the global clock distribution is realized so that the CS DAC is fed first with the clock signal to avoid timing issues between the clock and data arrival to the switching cells in the CS DAC. Thereafter, the clock signal propagates to trigger the retiming DFF blocks and the on-chip memory, where the clock signals WCLK and RCLK are selected through SEL. The former is the clock signal from an external device that sends data to write in memory, whereas the latter is the input RF clock signal. The test bench of the chip is illustrated in Fig. 4.11. It requires an external clock signal and a digital control interface to send the digital input data and set the read/write operation in the on-chip memory. Also, the output current is terminated with an differential output resistance of 100 Ω. An available ideal balun in Cadence is utilized with

the single-ended output connected to a load resistance of 50 Ω. The integration of the ideal balun reduces the load impedance and results in a differential voltage swing at the output of 0.53 V. In practice an RF balun with 50 Ω impedance terminations can be utilized to obtain a single-ended load resistance of 25 Ω and a differential output voltage of 0.8 V. The supply voltage of the digital and analog domains are set to 1.2 and 1.1 V, respectively. The results are obtained from post-layout simulations with transient noise for the typical process corner and a temperature of 75 °C, unless otherwise specified.

4.6.2 Static performance

To evaluate the static performance, the Monte Carlo analysis is carried out at the schematic level. The DNL and INL are derived from the best-fit line approximation method and their plots obtained for a 100-point Monte Carlo simulation are presented in Fig 4.12. From the simulation results, the DNL and INL in conjunction are within $\pm$ 1 LSB and $\pm$ 0.5 LSB range, which complies with a yield of 99.0% that attains monotonicity. Further on, $|\text{DNL}|_{\text{max}}$ reaches up to 0.935 LSB and the $|\text{INL}|_{\text{max}}$ 0.517 LSB. Also, $|\text{DNL}|_{\text{mean}}$ and $|\text{INL}|_{\text{mean}}$ are in the range of 0.252 and 0.247 LSB, respectively.

4.6.3 Dynamic performance

Initially, the stochastic SFDR variations due to the random mismatch in the current source are obtain from a 100-point Monte Carlo simulation at the schematic level. The results for different f_{sig}/f_s within the Nyquist range, $f_s/2$, are shown in Fig. 4.13. For each data point, the average value (mid-point) and the $\pm 3\sigma$ variation (error-bar) is presented.

Since, the amplitude errors degrade the dynamic performance from low input frequencies, an f_s of 5 MHz is considered. From Fig. 4.13, the SFDR maintains in average a value of about 68.6 dBc for each signal point over the signal bandwidth. This result approximates to the estimation obtained in (3.6). On the other hand, an standard deviation around 1.6 dB is obtained, which results in a $\pm 3\sigma$ deviation in the SFDR with a range from 63.8 dBc to 73.4 dBc. Further

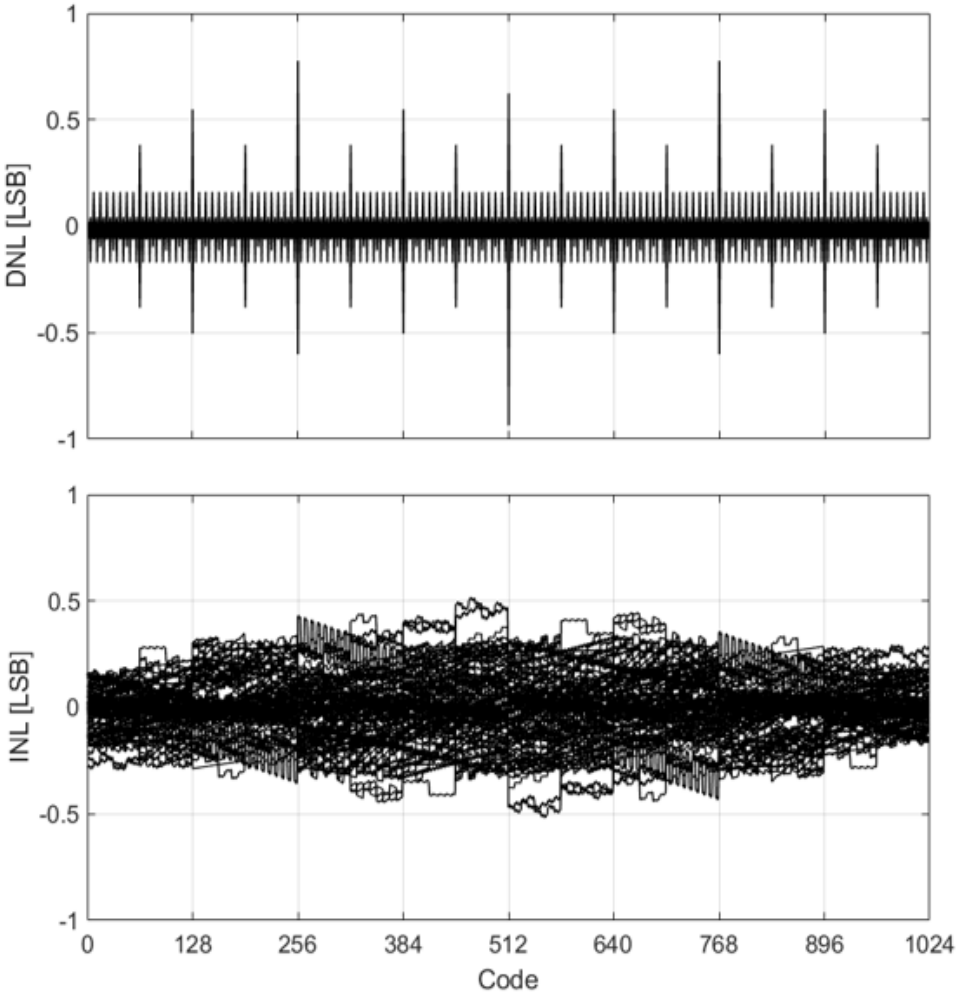

Figure 4.12: Static performance DNL (top) and INL (bottom).

on, the SFDR versus the normalized f_{sig}/f_s for an f_s of 2.5 GHz and 3.5 GHz is plotted in Fig. 4.14. With the former, the SFDR ranges from 60 dBc to 53 dBc approximately.

This results in a drop of about 15 dBc from DC, where interconnects in the layout also contribute with a faster degradation of the dynamic performance in the CS DAC. For the latter, the SFDR drops within a range from 47 dBc to 41 dBc approximately. In essence, with increments in f_s, the dynamic performance in the CS DAC become more sensitive to timing issues, e.g., memory effects as well as nonlinear settling that results in the code-dependent distortion at the output. This also exacerbates with large glitches during mid-code bit transitions in the binary-weighted DAC. Similarly, the ENOB versus f_{sig}/f_s is plotted in Fig. 4.14. Thus, for an f_s of 2.5 GHz, an ENOB of 9 is obtain up to about 500 MHz and then

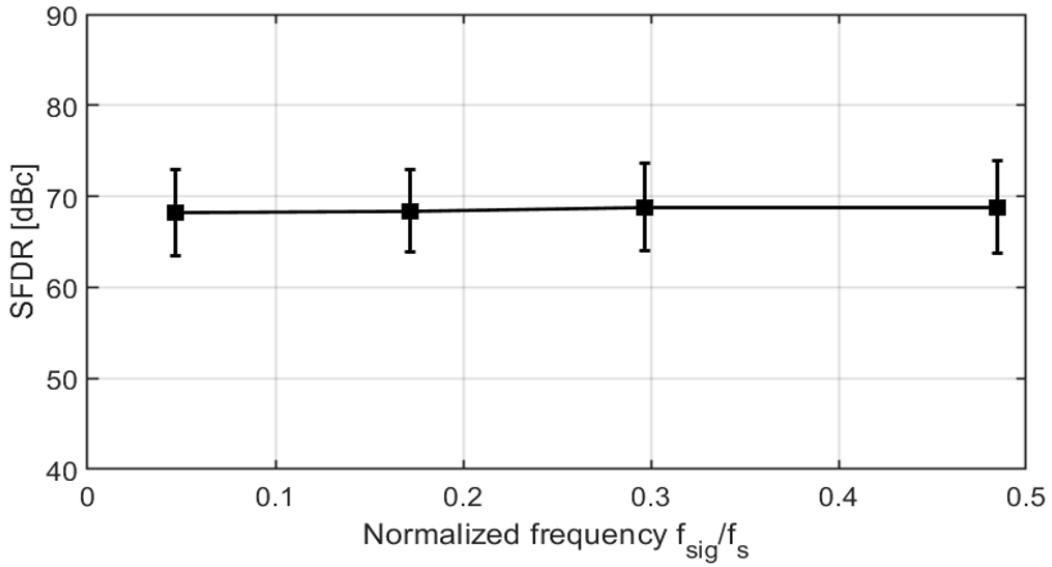

Figure 4.13: SFDR versus f_{sig}/f_s with f_s = 5 MHz.

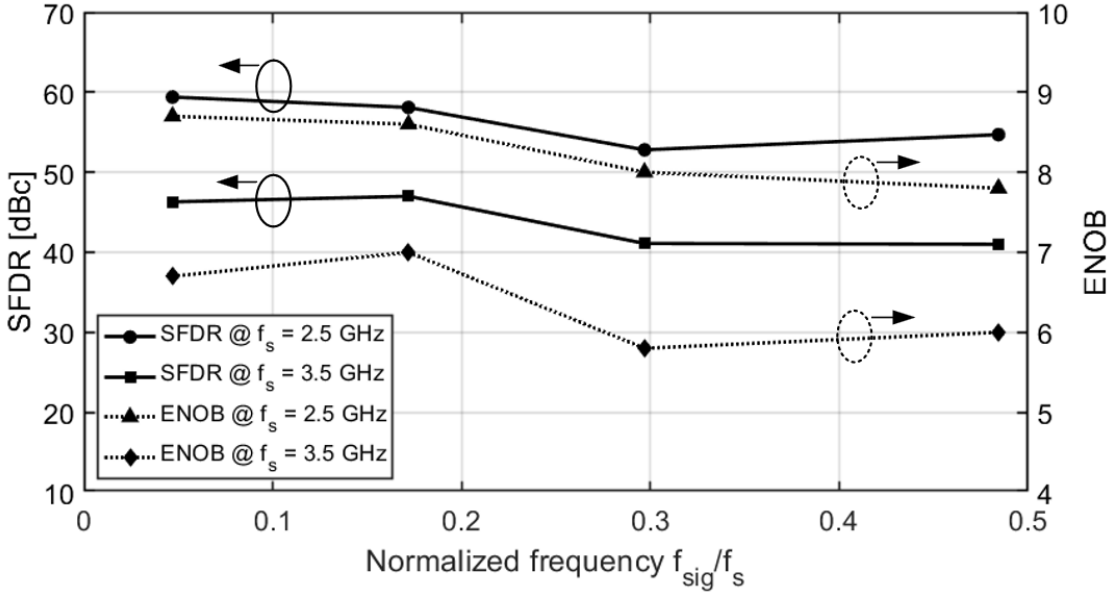

Figure 4.14: SFDR (left) and ENOB (right) versus f_{sig}/f_s with f_s = 2.5 GHz and 3.5 GHz.

it drops to 8 at Nyquist, $f_s/2$. Likewise, for an f_s of 3.5 GHz and with respect to the same normalized frequencies, the ENOB is around 7 and 6. In addition, the output spectrum of single-tone, f_{sig}, approximated to 0.6 GHz and 1.7 GHz with f_s of 3.5 GHz are presented in Fig. 4.15 and Fig. 4.16, respectively. It is observed that the degradation in the SFDR results from harmonic distortion (HD) with the presence of HD2 with a power of -32.12 dBm in the spectrum, whereas for the signal tone at Nyquist, the HD2 is folded back and locates in the spectrum

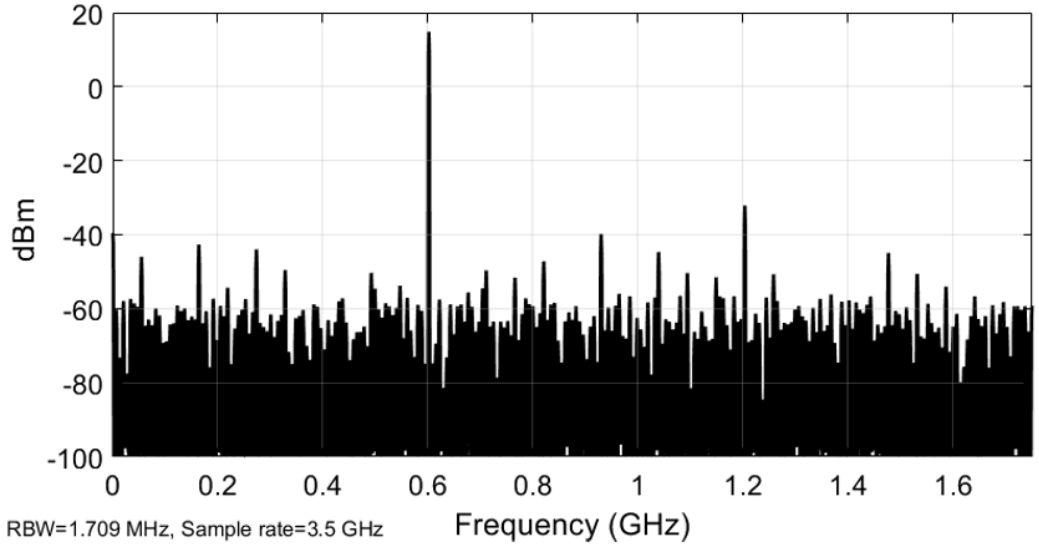

Figure 4.15: Spectrum of f_{sig} $\approx$ 0.6 GHz and f_s = 3.5 GHz.

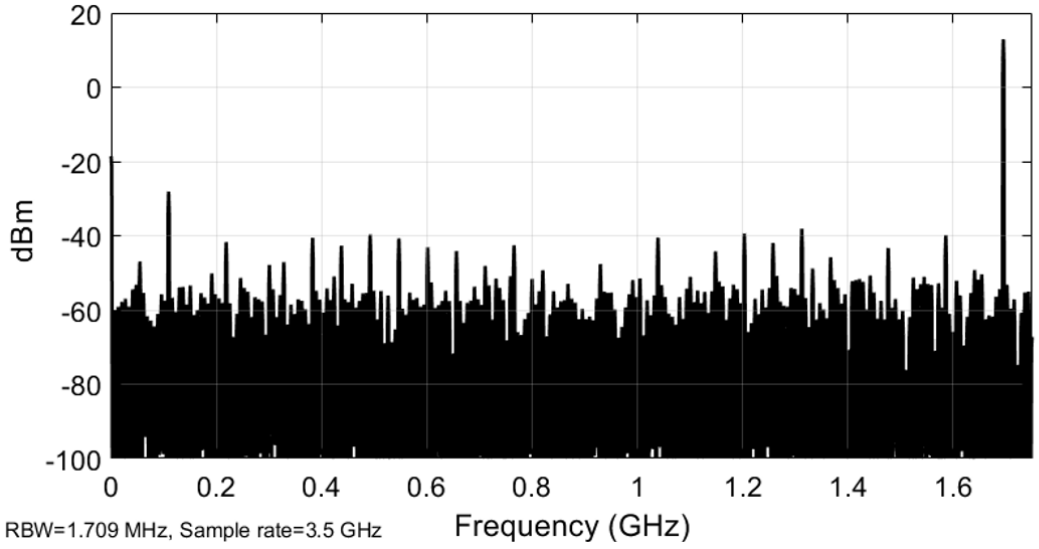

Figure 4.16: Spectrum of f_{sig} $\approx$ 1.7 GHz and f_s = 3.5 GHz.

at 0.11 GHz reaching power of about -28.1 dBm.

On the other hand, the -IMD3 versus f_{sig}/f_s (centered-frequency) for an f_s of 3.5 GHz is plotted in Fig, 4.17, where it reaches up to 65.8 dBc at low frequencies and then drops to about 50 dBc. Due to the limited data vector of 64-point and difficulty to asses the results at Nyquist, the two-tone test is shown until an f_{sig}/f_s of about 0.33. Moreover, the spectrum of a two-tone test also with an f_s of 3.5 GHz and about 0.82 GHz centered-frequency is presented in Fig. 4.18. The first IMD3 product is located in the spectrum around 0.5 GHz with signal power of

-43.51 dBm, whereas the second one is located at 1.15 GHz with signal power of -44.41 dBm, respectively.

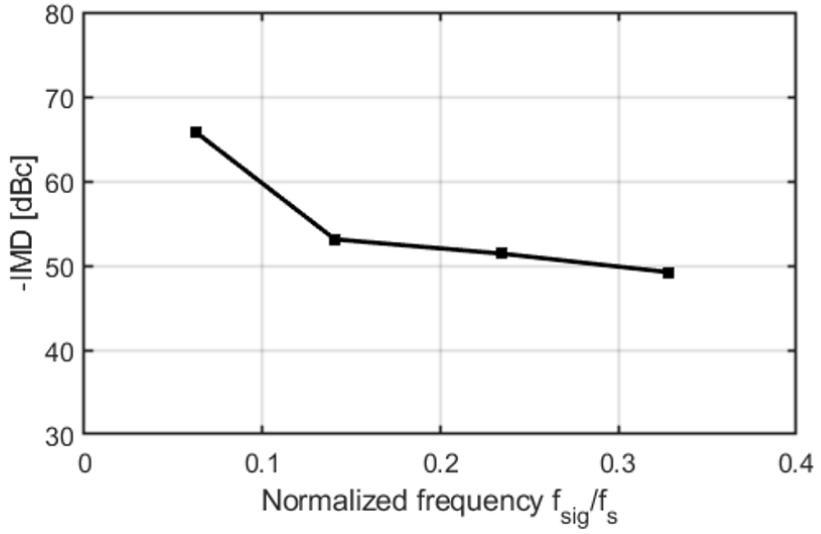

Figure 4.17: -IMD3 versus f_{sig}/f_s with f_s = 3.5 GHz.

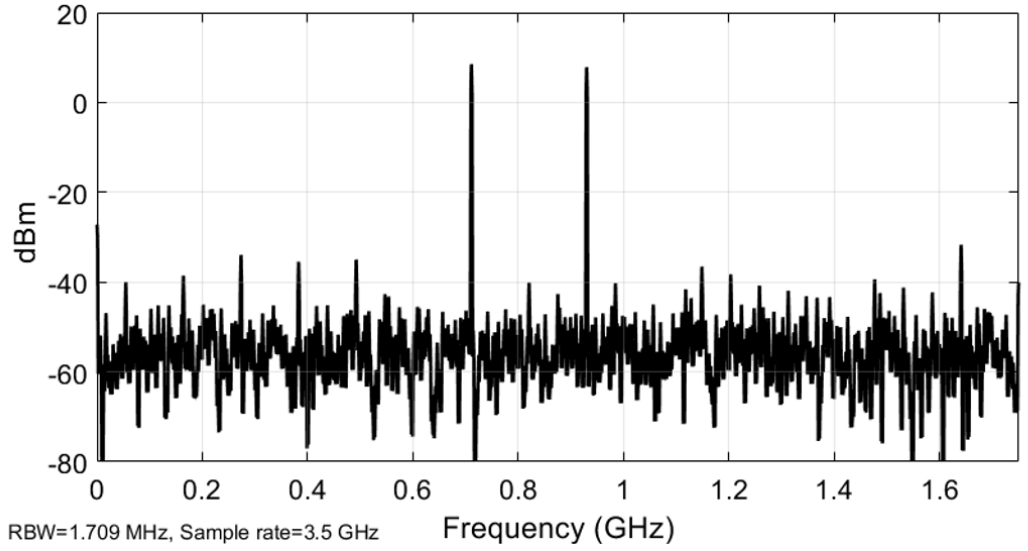

Figure 4.18: Spectrum of $f_{sig,1} \approx$ 0.79 GHz and $f_{sig,2} \approx$ 0.93 GHz with f_s = 3.5 GHz.

4.6.4 Performance comparison

The design characteristics and performance of binary-weighted, segmented and high-speed CMOS CS DAC designs are presented in Table. 4.1 and Table. 4.2. The proposed CS DAC is characterized for an f_s of 2.5/3.5 GHz. Moreover, the Figure-of-Merit (FoM) is given by [80]

$$\text{FoM} = V_{swing} \frac{BW}{P_{total}} 10^{\text{SFDR}/20} \tag{4.9}$$

with P_{total}, V_{swing} and BW, the power consumption, output voltage swing and the signal bandwidth, respectively. From Table. 4.1, the proposed solution presents a signal bandwidth over 10$\times$ larger with respect to the binary-weighed CS DACs reported in [38], [81]. Nevertheless, in [78] a binary-weighted CS DAC with a BW of 1.5 GHz is presented, but for a 9-bit implementation that leads to a reduced power consumption. On the other hand, a high-speed binary-weighed CS DAC with an f_s of 20 GS/s is presented in [82]. This utilizes 2$\times$ TI for a 6-bit CS DAC implementation, which benefits with high-speed of operation and reduced complexity. However, the SFDR for the aforementioned solution drops up to 35.1 dBc at Nyquist, thus compromising the FoM. For an f_s of 2.5 GHz, the proposed CS DAC presents an improved FoM with respect to [81] and approximates to [82] for the reported $V_{swing,diff}$ of 0.53 V. Yet, by considering an $V_{swing,diff}$ equal to 0.8 V, the FoM of the proposed CS DAC can reach up to 2.3 and 0.67 for an f_s of 2.5 and 3.5 GHz, respectively.

Moreover, considering the high-speed CS DACs in Table. 4.2. The FoM is improved for an f_s of 2.5 GHz in comparison with [45], [77]. This is mainly attributed to the linearity performance with an SFDR $>$ 50 dBc over the signal bandwidth, BW. For instance, in [77] an SFDR of 44 dBc is obtained at Nyquist and approximates to the linearity performance when operating at an f_s of 3.5 GHz. On the contrary, in [45], the SFDR is only reported up to 0.7 GHz. This corresponds to less than half the presented characterization at an f_s of 2.5/3.5 GHz in the proposed CS DAC. Finally, high-speed CS DACs with 56 GHz $\leq f_s$ have also been presented with 6 and 8 bit resolutions [40], [83], respectively. Notice that the power consumption augments considerably as shown in [40], reaching up to 2.5 W for a CS DAC implemented in 28 nm CMOS. Furthermore, the SFDR

drops below 30 dBc for both [40], [83], thus compromising its FoM and showing the design challenges to achieve high-speed operation along with reduced power consumption.

Table 4.1: Comparison with binary-weighted CMOS CS DACs.

Reference	This work	JSSC06 [38]	ASSC07 [81]	VLSI11 [78]	TCAS18 [82]
Process [nm]	65	180	180	65	65
Type	Nyq.	Nyq.	Nyq.	Nyq.	TI Nyq.
Bits	10	10	14	9	6
f_s [GS/s]	2.5/3.5	0.25	0.1	3	20
BW [GHz]	1.25/1.75	0.125	0.05	1.5	9.2
Power [mW]	191/234	22$^{(1)}$	84.2	60$^{(2)}$	136
$SFDR_{min}$ [dBc]	53/41	60	46.6	48	35.1
$V_{swing,diff}$ [V]	0.53	1.0$^{(2)}$	1.15	0.4	0.4$^{(3)}$
Area [mm^2]	0.67	0.35	0.74	0.04	0.072
FoM*	1.54/0.44	5.7	0.15	2.51	1.65

(*): $\left[\frac{V \cdot Hz}{W} 10^{12}\right]$, (1): I_{load} of 10 mA, (2): Estimated, (3): Estimated for a single-ended load of 50 Ω.

Table 4.2: Comparison with high-speed CMOS CS DACs.

Reference	This work	TCAS10 [77]	JSSC11 [83]	RFIC14 [40]	ISSC14 [45]
Process [nm]	65	130	65	28	65
Type	Nyq.	Nyq.	TI Nyq.	TI Nyq.	Nyq.
Bits	10	10	6	8	16
f_s [GS/s]	2.5/3.5	1.6	56	100	1.6
BW [GHz]	1.25/1.75	0.8	28	25$^{(1)}$	0.7$^{(1)}$
Power [mW]	191/234	27	750	2500	240
$SFDR_{min}$ [dBc]	53/41	44	20	28	54
$V_{sw,diff}$ [V]	0.53	0.25	0.6	0.4	1.0
Area [mm^2]	0.67	0.5	0.24	0.043	NS$^{(2)}$
FoM*	1.54/0.44	1.17	0.21	0.10	1.46

(*): $\left[\frac{V \cdot Hz}{W} 10^{12}\right]$, (1): Reported BW, (2): Not specified.

Chapter 5

Conclusion

5.1 Conclusions

Digital-to-analog converters (DACs) have been pushed to operate at higher sampling frequencies with improved performance and reduced power consumption in high-speed applications, e.g., wireless communications, this has challenged the DAC design to satisfy more stringent requirements between different design corners. This work has focused on the current-steering (CS) DAC topology due to its intrinsic high-speed and driving capability. A treatment on the different design considerations and corners aimed at achieving energy-efficient CS DAC with maintained performance was presented. Further, the binary-weighted Nyquist DAC was considered to attain a large channel bandwidth with reduced hardware overhead, which has special interest in modern communications standards aiming at channel bandwidths beyond 1-GHz as well as facilitating direct-RF synthesis.

In **Chapter 2** an overview on DACs is presented, including an analysis of additional signal processing techniques commonly utilized to change the frequency response. The chapter is followed by a brief description of conventional DAC categories and topologies. Then, a comparison of high-speed DAC implementations was presented, showing that CMOS current-steering (CS) DACs are among other solutions the preferred option in today's state-of-the-art realizations.

Further on, **Chapter 3** presents the CS DAC in more detailed. The fundamental performance limitations were discussed and a theoretical analysis on power and energy consumption bounds in CS DACs was also presented. The analysis included the power digital, mixed-signal and analog power domains for the design corners of noise, speed and linearity. From the study, it was observed that the analog power domain dominates the CS DAC's performance for an SNR and SFDR of about 60-dB and 50-dBc in 65nm CMOS process. Also, for the noise and speed bounds in the analog domain, the energy consumption grows for an equivalent number of bits (ENOB) at a rate of 2^{2ENOB} and 2^{ENOB-2}, making the noise-bound of special interest to achieve minimum power and energy consumption for a certain SNR. Moreover, for the linearity-bound the energy consumption is found to increase at a rate of 2^{ENOB-1} with respect to the SFDR. Furthermore, design considerations in CS DACs were addressed to aim at high-speed and high-performance. These include, a comparative analysis of conventional CMOS latch-driver circuits, considering the single- and dual-phase clocked solutions. An alternative switching driver was proposed to sustain rapid switching transitions with reduced power consumption and attain an switching-delay approximated to the fastest dual-clocked solutions. Also, enhancement techniques were discussed, where a digital switching scheme was proposed to reduce the switching transitions as well as improve the linearity against stochastic amplitude errors. From high-level simulations the switching scheme showed an improvement in the SFDR of about 4 dB for an amplitude error of 10% in the unary-weighted elements and serving also as an alternative solution for the conventional thermometer decoder with reduced switching transitions.

On the other hand, the design and characterization of a high-speed 10-bit binary-weighted CS DAC was presented in **Chapter 4**. The binary-weighted DAC has been explored as an alternative solution with the aim to reduce complexity and power consumption, while facilitating high-speed operation. The intrinsic binary-weighted nature has challenged its performance with amplitude and timing mismatches as well as large glitches between mid-code transitions. Thus, an extension of the binary-weighted CS DAC with the utilization of a unary-weighted approach has been utilized to counteract for the aforementioned issues. The design considerations and testing methodology were presented. The chip was characterized for the sampling frequencies of 2.5 and 3.5 GHz, where and SFDR over 50 dBc is attained over the channel bandwidth with an f_s of 2.5 GHz and

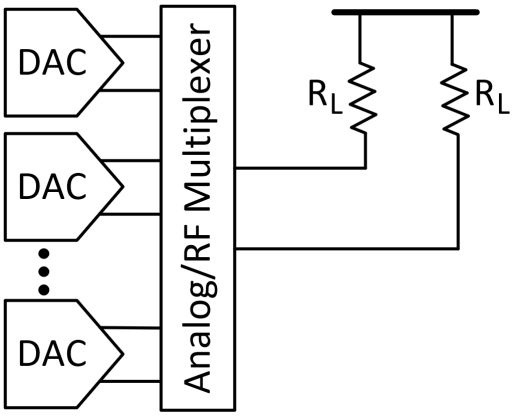

Figure 5.1: Time interleaving of multiple DACs.

40 dBc for an f_s of 3.5 GHz, while consuming a power at Nyquist of 191 and 234 mW, respectively. The results show a favorable trade-off between the design corners, including power consumption speed and linearity among other binary-weighted CS DACs as well as high-speed CS DAC realizations.

5.2 Future work

With the emergence of new high-speed applications, e.g., sixth-generation (6G) and the utilization of the radio frequency spectrum in the tens of GHz with 60-GHz radios, DACs will be relentlessly driven towards higher sampling frequencies with maintained performance and low-power consumption. Despite that DAC design has been favored with the continuous CMOS scaling to satisfy the high-speed and low-power requirements, this trend will face a physical limitation in the future. Hence, further exploration of alternative solutions in the system and circuit level will be required in combination with a reduction of hardware overhead.

Therefore, by aiming at large channel bandwidths, future work considers the use of time interleaving with the integration of multiple Nyquist DACs, which benefits from a reduced sampling rate for each separate DAC while facilitating direct frequency synthesis with multi-GHz channel bandwidth as presented in Fig. 5.1. The reduced sampling rate per DAC leads to improved performance and less power consumption. Also, this can be further explored with the utilization of signal processing techniques to facilitate direct-RF synthesis at higher frequency bands.

List of Author's Publications

Journal Articles

- **O. M. Chacón**, J. J. Wikner, C. Svensson, L. Siek, and A. Alvandpour, "Analysis of energy consumption bounds in CMOS current-steering digital-to-analog converters", *Journal of Analog Integrated Circuits and Signal Processing, 2022*, doi: 10.1007/s10470-022-02013-2.

Conference Proceedings

- **O. M. Chacón**, J. Wikner, A. Alvandpour and L. Siek, "A 10-bit 3.75-GS/s Binary-Weighted DAC with 58.6-pJ Energy Consumption in 65-nm CMOS," *IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2020, pp. 1-4, doi: 10.1109/NorCAS51424.2020.9265003.
- **O. M. Chacón**, J. J. Wikner, A. Alvandpour and L. Siek, "A digital switching scheme to reduce DAC glitches using code-dependent randomization," *IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2021, pp. 1-5, doi: 10.1109/NorCAS53631.2021.9599651.
- **O. M. Chacón**, J. Wikner, A. Alvandpour and L. Siek, "Comparative Analysis of CMOS Latch-Driver Circuits for Current-Steering Digital-to-Analog Converters," *29th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*, 2022, pp. 93-98, doi: 10.23919/MIXDES 55591.2022.9837990.

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