

Physical Layout Design Optimization of Integrated Spiral Inductors for Silicon-Based RFIC Applications

Choon Beng Sia, Beng Hwee Ong, Kwok Wai Chan, Kiat Seng Yeo, Jian-Guo Ma, *Senior Member, IEEE*, and Manh Anh Do

Abstract—A new test structure layout technique and design methodology are used to investigate quantitatively how geometrical layout parameters such as core diameter, conductor spacing, and width would affect the performance of spiral inductors. For the 0.18- μm RFCMOS technology, experimental results in this paper reveal that inductors' core diameters must be adequately large, more than 100 μm , to ensure high quality factor characteristics and their conductor spacing should be minimal to obtain larger per unit area inductance value. A novel design methodology which optimizes the conductor width of inductors allows alignment of their peak quality factor to the circuit's operating frequency, enhancing the gain, input/output matching characteristics and noise figure of a giga-hertz amplifier.

Index Terms—Conductor eddy current, inductance, inductor layout optimization, integrated RF inductor, quality factor, silicon RFICs, skin effects, spiral inductors.

I. INTRODUCTION

PORTABLE wireless communication equipment requires low-cost, high-performance RFICs and silicon technology is currently the most suitable candidate since incessant improvements in processing technologies have continually enhanced the RF performance of silicon-based transistors in every new technology node [1], [2]. Exploitations of silicon technologies require the availability of optimized integrated inductors with high quality factors to enhance the performance of RF circuits but resistive metallization and lossy silicon substrate continue to be major roadblocks. As such, it is essential to develop reliable layout optimization methodologies for spiral inductors either through test chip fabrication or electromagnetic (EM) simulation tools. Availability of such design methodologies for inductors will bring about advantages such as reduction in circuit design iterations, shortening of product time-to-market cycle, cost-effective use of silicon die area as well as improvements in circuit performance to satisfy stringent system level specifications.

Over the last few years, several techniques have been proposed to optimize the physical layout of silicon-based spiral inductors. One popular approach adopted by many research groups is to optimize layout of the inductor by making use of existing lumped-element RF SPICE models [3]–[6]. Such convenient optimization algorithms are however limited by the validity of these SPICE models in making accurate predictions

Manuscript received April 7, 2005; revised August 8, 2005. The review of this paper was arranged by Editor J. N. Burghartz.

C. B. Sia is with the Advanced RFIC (S) Pte. Ltd., Singapore 609930 (e-mail: cb.sia@arfic.com).

B. H. Ong, K. W. Chan, K. S. Yeo, J. G. Ma, and M. A. Do are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798.

Digital Object Identifier 10.1109/TED.2005.859638

of the inductors' behavior at high frequencies when their physical design parameters such as core diameter, conductor spacing and width are modified accordingly. In this paper, a novel and simple to understand technique is proposed for the first time to quantitatively show how each of the physical design parameters would affect the performance of silicon-based spiral inductors. Also, through these experiments, further demonstrate a methodology that optimizes and aligns the inductor's peak quality factor frequency to the operating frequency of the circuit.

II. TEST STRUCTURE, MEASUREMENT SETUP, AND FIGURES OF MERIT

Spiral inductors discussed in this paper are fabricated in a six-metal layer 0.18- μm RFCMOS process technology with 2- μm -thick top metal backend-of-line process flow. The spiral coil of the inductor is constructed utilizing metal 6 while metal 5 is used for its underpass. On-wafer RF device measurements are performed using Agilent 8510C Vector Network Analyzer (VNA) and Cascade Microtech RF Infinity probes. Wafer and RF probes are shielded within the microchamber of Cascade Microtech S300 semi-automated probe station during measurements. P+ taps are included in the ground frame of the six-pad GSG test structures to ensure proper grounding of the substrate. Parasitics of the test pads are accurately de-embedded by subtracting Y -parameters of the open calibration structures from those test structures with the inductors [7].

From the de-embedded Y parameters, inductance L , and quality factor Q of integrated inductors are determined by

$$L = \frac{\text{Imag} \left[\frac{1}{Y_{11}} \right]}{2 \times \pi \times \text{Frequency}} \quad (1)$$

$$Q = - \frac{\text{Imag}[Y_{11}]}{\text{Real}[Y_{11}]} \quad (2)$$

And series resistance R for spiral inductors can be expressed as follows:

$$R = \text{Real} \left[- \frac{1}{Y_{12}} \right] \quad (3)$$

L and Q are both extracted from Y_{11} and not Y_{12} parameters since it is important to include and consider the effects of the lossy silicon substrate when evaluating the overall performance of the spiral inductors. On the contrary, parasitic series resistance, R associated with the metallization is extracted from Y_{12} parameter to show the skin effects of metallization at radio frequencies, excluding substrate losses. However, this is only valid within the frequency range or for small-sized inductors such that

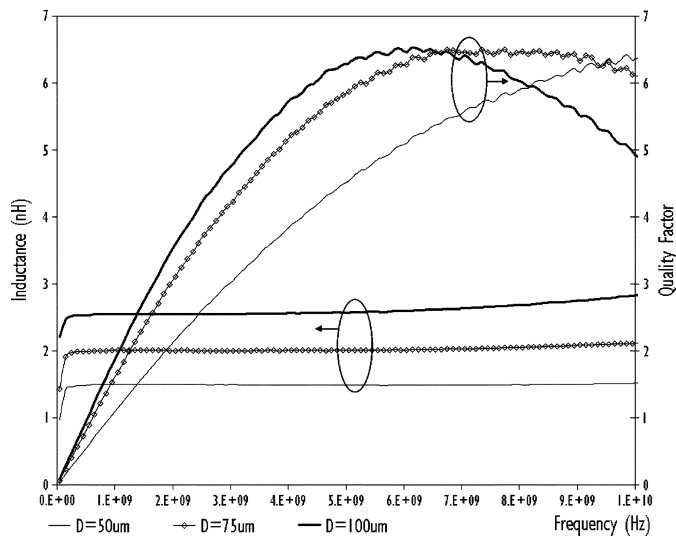


Fig. 1. Inductance and quality factor versus frequency for three-turn spiral inductors with core diameters of 50, 75, and 100 μm .

a simple lumped element π model is sufficient to predict the behavior of the spiral inductors.

III. DESIGN OF TEST STRUCTURES, RESULTS, AND DISCUSSIONS

A novel optimization technique to investigate effects of the core diameter, metallization spacing and width on the performance of integrated spiral inductors will be demonstrated in the following subsections. For each of these three physical design parameters, spiral inductor test structures are designed to yield similar inductance values so that unbiased performance comparisons can be achieved. Experiments that compare characteristics of inductors with very different inductance values offer little understanding as to how these physical design parameters would affect the behavior of the spiral inductors since their quality factors are determined by both the resultant magnetic energy stored and resistive loss as shown in (2).

A. Effects of Core Diameter

Inner core diameter of spiral inductor is an important geometrical layout parameter to consider since it determines the overall size and performance of the inductor and being the largest device in RFICs, the number of inductors used would most probably establish the overall product die size. If three-turn spiral inductors with fixed conductor width but different core diameters are fabricated and characterized, they yield different inductance values as shown in Fig. 1. Because the inductance values are different, effects of core diameter on the performance of inductors cannot be differentiated and determined. As such, to investigate the impact of the core diameter, test structures should be designed with the same width and total conductor lengths, not identical number of turns, to obtain spiral inductors with similar inductance values.

Fig. 2 shows die photos of inductors designed with different core diameter values of 10, 50, 100, and 150 μm but with fixed width, spacing, and total conductor length of 8, 1.5, and 1000 μm , respectively. Due to the design constraint of maintaining

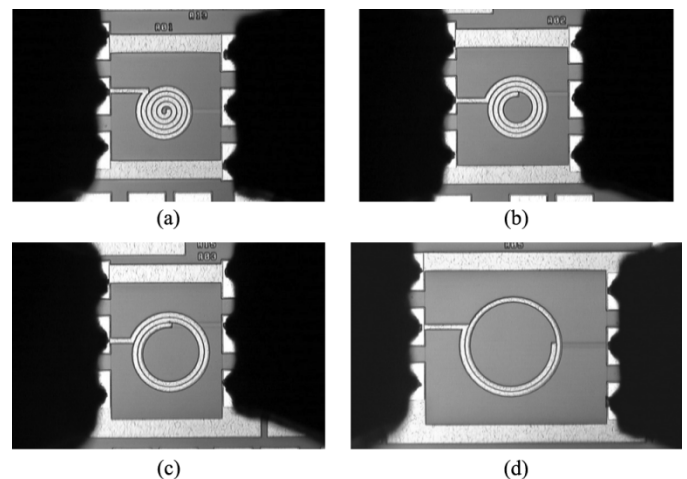


Fig. 2. Die photos of spiral inductors with identical conductor length (1000 μm), and width (8 μm) but different core diameters of (a) 10, (b) 50, (c) 100, and (d) 150 μm .

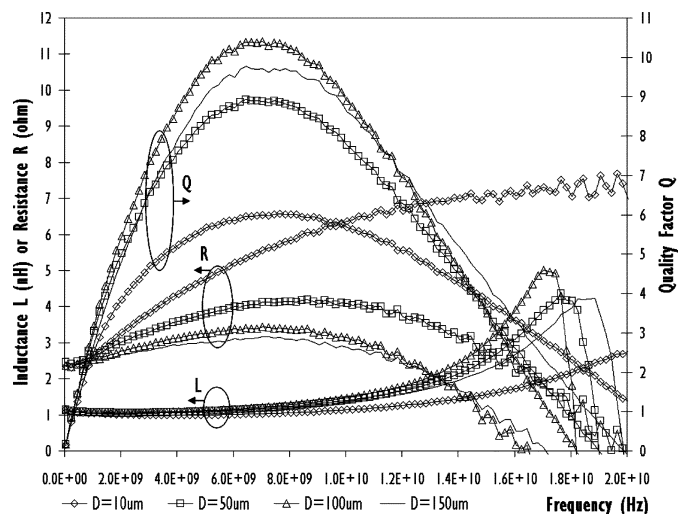


Fig. 3. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length (1000 μm) and width (8 μm) but different core diameters.

same total conductor length, these inductors have different number of turns which result in dissimilar amount of inductive and capacitive coupling within the spiral coil of the inductor. While capacitive coupling is dominant in the higher radio frequency regime, inductive coupling is a second-order effect and since the total conductor length and width are kept constant, all four inductors yield almost the same low-frequency inductance and resistance values as shown in Fig. 3. At 3 GHz, where the inductance values are almost identical, quality factor improves significantly by more than 57% when the core diameter of the spiral inductors increases from 10 to 100 μm .

Fig. 4 shows that when the total conductor length is increased to 2000 μm , similar inductances and low frequency series resistances are also observed for all the integrated inductors with different core diameters. At 3 GHz, 46% increase in quality factor is noted when diameter is increased from 10 to 100 μm . Fig. 5, on the other hand, further demonstrates that for spiral inductors with 3500 μm in total conductor length, at 2 GHz, the quality factor can improve by more than 30% when 100

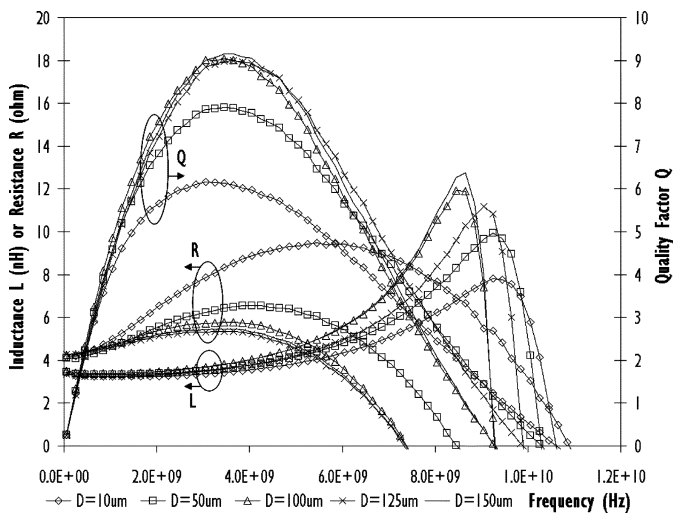


Fig. 4. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length ($2000 \mu\text{m}$) and width ($8 \mu\text{m}$) but different core diameters.

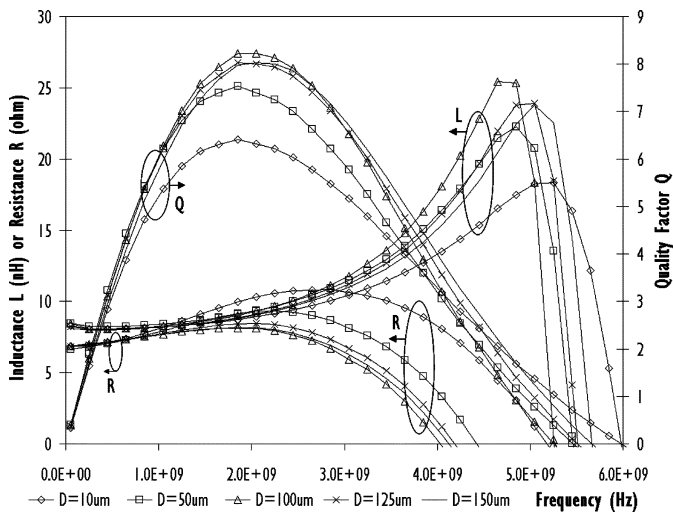


Fig. 5. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length ($3500 \mu\text{m}$) and width ($8 \mu\text{m}$) but different core diameters.

μm as opposed to $10 \mu\text{m}$ is used as the core diameter for the spiral inductors. These experimental results reveal that as the core diameter increases, high frequency series resistance decreases and significantly improve the quality factor of inductors. For the width of $8 \mu\text{m}$, optimal diameter value of $100 \mu\text{m}$ has been noted and further increments of core diameter value do not enhance the quality factor but waste costly silicon real estate. Other than upholding the same inductance values, these experimental comparisons are also meaningful because in each set of the test structures, the inductors have almost similar peak quality factor frequencies and self-resonant frequencies since their total conductor area are identical suggesting that their corresponding substrate losses are also more or less the same.

In general, as frequency increases, series resistance R of the inductor increases due to skin effects. If the total conductor length is sufficiently long R starts to decrease in the higher RF regime because simple lumped element π model cannot

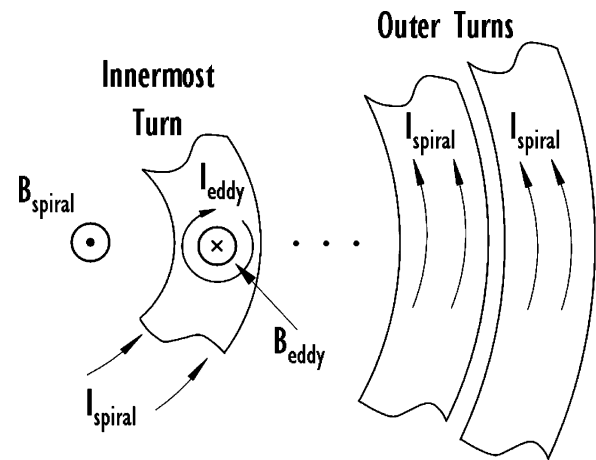


Fig. 6. Formation of conductor eddy current in the inner turns of spiral inductors.

describe the inductor which is behaving more like a transmission line. Nonetheless, interactions between the inductor's core diameter and its high frequency resistive behavior can be explained by the formation of conductor eddy current. The circular inductor shown in Fig. 6 carries a current, I_{spiral} , and generates an associated magnetic field, B_{spiral} that has maximum intensity at the center of the spiral. For the case of a large-width inductor with a very small core diameter, an enormous part of this magnetic field does not pass through the center of the spiral but rather through its inner turns. In accordance to Faraday's and Lenz's laws, an electric field is magnetically induced on these inner turns, producing circular eddy currents, I_{eddy} , which flow in the direction opposing the original change in magnetic field. The magnitude of this induced electric field is proportional to the time derivative of $B(t)$ and hence, this effect becomes very significant at giga-hertz frequencies. Formation of such eddy currents causes a nonuniform current flow in the inner turns of the spiral, increasing the series resistance, which in turn reduce the quality factor of spiral inductors [8]. This experiment has been reported previously [9] using only inductors with $1500 \mu\text{m}$ total conductor length for the copper backend processing technology but the interactions and correlations of conductor eddy current effects with respect to different conductor lengths and widths of the inductors have not been investigated before.

Interestingly, when a smaller conductor width of $4 \mu\text{m}$ is used for inductors with total conductor length of $2000 \mu\text{m}$, the core diameter has little effect on quality factors of the integrated inductors as shown in Fig. 7. However, at 3 GHz, for the same conductor length of $2000 \mu\text{m}$, using $16 \mu\text{m}$ conductor width, quality factor of the inductor improved notably by 34% when diameter increases from 50 to $150 \mu\text{m}$, compared to an improvement of only 14.5% for the case of $8 \mu\text{m}$ conductor width, as summarized in Figs. 4 and 8. This is so because as the conductor width widens, the distance between the outer turns of the inductor and its center hollow core increases extensively. It is then more probable for the inductor's magnetic field to pass through the inner turns instead of its hollow core, resulting in the formation of conductor eddy current. Therefore, in the $0.18 \mu\text{m}$ RFCMOS technology, the core diameter should be sufficiently large, more than $100 \mu\text{m}$, to minimize this adverse effect on the

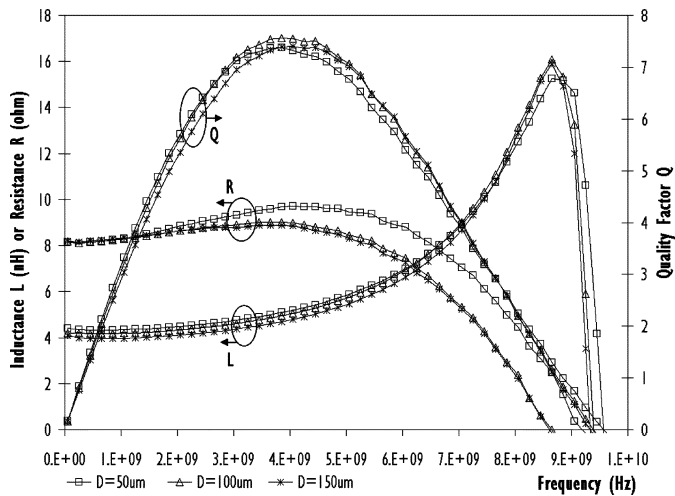


Fig. 7. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length ($2000 \mu\text{m}$) and width ($4 \mu\text{m}$) but different core diameters.

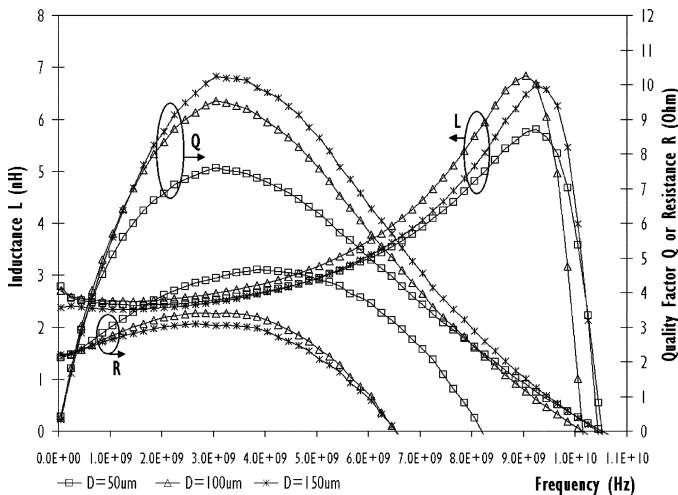


Fig. 8. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length ($2000 \mu\text{m}$) and width ($16 \mu\text{m}$) but different core diameters.

performance of spiral inductors. On the contrary, small inductors with narrow conductor width do not require large core diameters since it would only waste expensive silicon real estate.

B. Effects of Metal Conductor-to-Conductor Spacing

To investigate the effects of conductor-to-conductor spacing on spiral inductors, 4 inductors with identical conductor length, width and core diameter of 2000 , 8 , and $100 \mu\text{m}$ respectively are designed and fabricated having different spacing of 3 , 6 , 9 , and $12 \mu\text{m}$. On-wafer characterization reveals that metallization spacing does not significantly affect the quality factor performance of spiral inductor. As shown in Fig. 9, as conductor spacing decreases, the inductance values increase due to more mutual inductive coupling between the conductors within the spiral coil. At low frequency, all 4 inductors have identical series resistance but in the higher RF regime (2 – 4 GHz), inductor with spacing of $3 \mu\text{m}$ has the largest series resistance and this resistance decreases as the conductor spacing for the inductor increases.

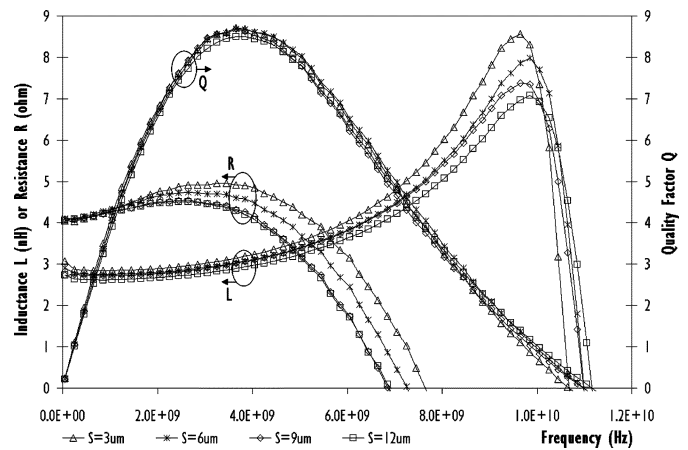


Fig. 9. Inductance, quality factor, and series resistance versus frequency for inductors with identical conductor length ($2000 \mu\text{m}$), width ($8 \mu\text{m}$) and core diameter ($100 \mu\text{m}$) but different spacing.

Such phenomenon could be due to localized proximity effect whereby eddy currents are generated within the metal trace because of nearby current-carrying metal trace. Inductor with the smallest spacing possesses the largest inductance and high frequency series resistance, while the opposite is true for inductor with the largest spacing. Because quality factor is determined by the resultant inductive and resistive behavior of the inductors, counter-compensations between inductance and series resistance are observed and as a result, the quality factor performances for all 4 inductors are almost identical. Therefore, for the $0.18\text{-}\mu\text{m}$ RFCMOS technology, inductor with the smallest spacing is favored over the other three inductors since it offers the highest inductance value and also, among all four inductors, it occupies the least area.

C. Effects of Metal Conductor Width

Typical inductor device libraries offered by silicon foundries contain only inductors designed with different number of turns, having fixed conductor width, spacing and core diameter. In such approach, using a fixed width and core diameter of 12 and $75 \mu\text{m}$, respectively to design spiral inductors, one would observe that as the number of turns for the inductors increases, their resonant frequencies and peak quality factor frequencies decrease as shown in Fig. 10. Although inductance coverage for device libraries is catered in this typical approach, at any frequency of interest, only a few inductors perform well. For this example, at the operating frequency of 2.5 GHz, only four- and five-turn inductors (3 and 4.5 nH) have large quality factors and this is so because their peak quality factor frequency is close to 2.5 GHz.

On the other hand, when the inductor's width is studied in an experiment with four eight-turn spiral inductors having a fixed $75\text{-}\mu\text{m}$ core diameter and $1.5 \mu\text{m}$ spacing but with different conductor widths of 6 , 8 , 12 , and $16 \mu\text{m}$, these four spiral inductors have very different inductance values even at low frequencies, with $16 \mu\text{m}$ width inductor having the largest inductance value, as shown in Fig. 11. However, an interesting point to highlight is that total conductor lengths for the four inductors with widths

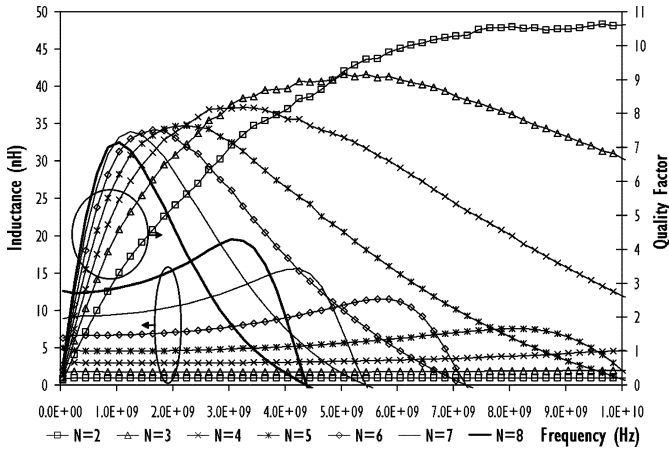


Fig. 10. Inductance and quality factor versus frequency for two-turn to eight-turn inductors with width and core diameter of 12 and 75 μm , respectively.

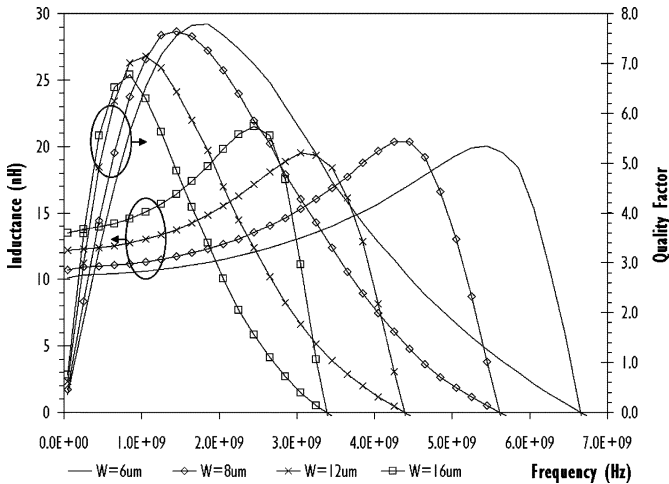


Fig. 11. Inductance and quality factor versus frequency for eight-turn inductors with core diameter and spacing of 75 and 1.5 μm , respectively for widths of 6, 8, 12, and 16 μm .

of 6, 8, 12, and 16 μm are 3699, 4160, 5082, and 6005 μm respectively and their normalized unit length low frequency inductance values are actually 2.73, 2.58, 2.40, and 2.24 $\text{pH}/\mu\text{m}$, correspondingly. These observations show that as width decreases, the unit length inductance value increases and to investigate the effect of conductor width, one has to pay special attention to this so that inductors of different conductor width can be designed to have same inductance values and unbiased experimental comparisons can be facilitated. The results from Figs. 10 and 11 reveal that conventional design approach cannot yield high- Q inductors across a wide range of inductance values and hence circuit designers are left with very few alternatives to enhance the performance and robustness of their circuits.

In this sub-section, peak quality factor of inductors with various inductance values will be aligned to the operating frequency of the circuit through a design methodology summarized in a flowchart shown in Fig. 12. An array of inductors with different widths (2, 4, 8, 12, 16, and 24 μm) and total conductor lengths (750, 1000, 1500, 2000, 2500, and 3000 μm) are designed with fixed spacing and diameter of 1.5 and 100 μm , correspondingly. The same 0.18- μm RFCMOS process is used

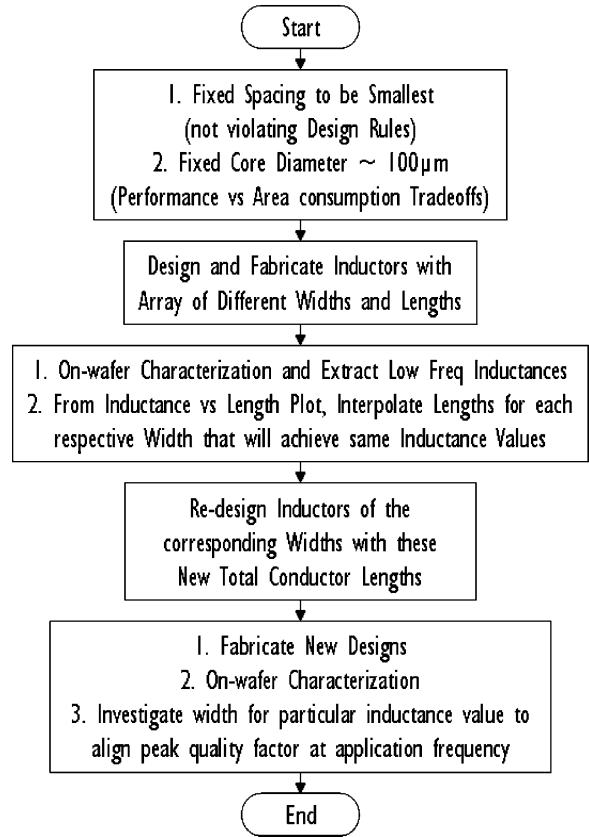


Fig. 12. Flow chart summarizing the design methodology for optimizing the physical dimensions of spiral inductors.

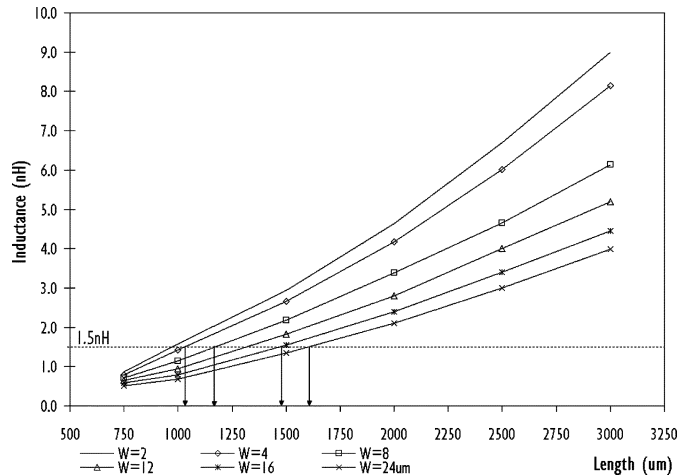


Fig. 13. Inductance at low frequency versus total conductor length for inductors with identical diameter of 100 μm but different widths of 2, 4, 8, 12, 16, and 24 μm .

to fabricate these inductors and they are then measured using on-wafer RF characterization procedure described in Section II. Fig. 13 consolidates the low frequency inductance versus total conductor length plot and again, similar to Fig. 11, it reveals that the per unit length inductance increases when the conductor width is reduced. To investigate the effect of conductor width on the performance of inductors, Fig. 13 is used for interpolation of total conductor lengths such that spiral inductors with different widths will have similar inductance values. As

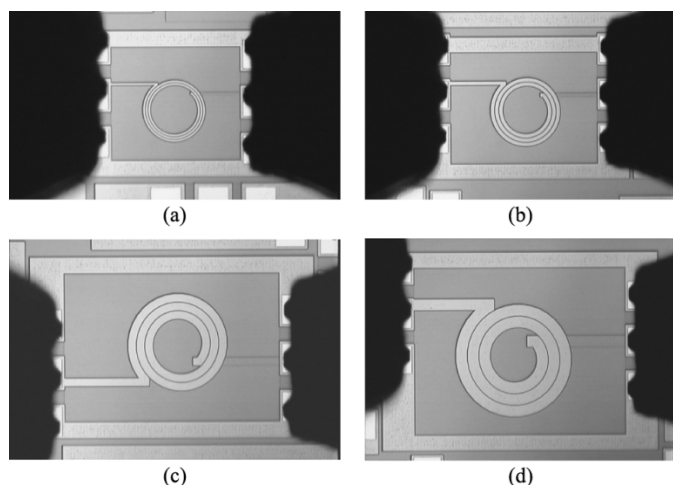


Fig. 14. Die photos of 1.6-nH spiral inductors with identical core diameter ($100\ \mu\text{m}$) but different widths of (a) 4, (b) 8, (c) 16, and (d) $24\ \mu\text{m}$.

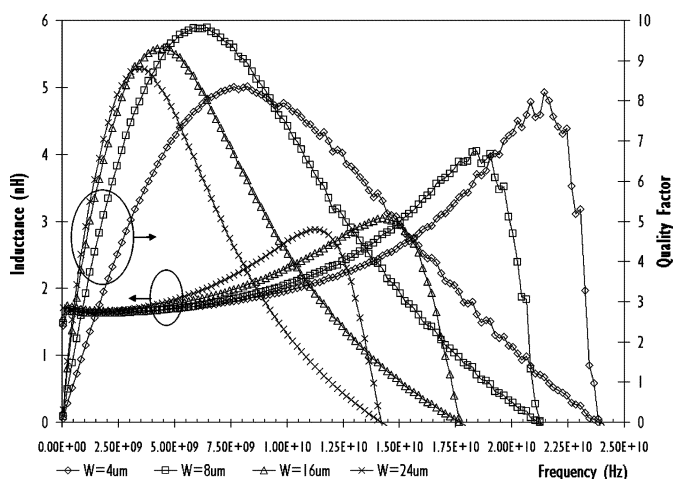


Fig. 15. Inductance and quality factor versus frequency for inductors with identical inductance ($1.6\ \text{nH}$) and core diameter ($100\ \mu\text{m}$) but different widths.

an example, when a $1.5\ \text{nH}$ line is drawn in the inductance versus conductor length plot, four different total conductor lengths for widths of 4, 8, 16, and $24\ \mu\text{m}$ are obtained. The interpolated total conductor lengths allow 4 separate inductors to be redesigned and fabricated such that they yield the same inductance values for studying and understanding the impact of the inductor's conductor width.

Fig. 14 shows die photos of these four inductors with different conductor widths and Fig. 15 compares their inductance and quality factor plots. The measured results reveal that at 2.5 GHz, inductances ($1.6\ \text{nH}$) for all four inductors are very similar and the quality factor improves by more than 84% as the conductor width increases from 4 to $16\ \mu\text{m}$. Although the inductor with metallization width of $24\ \mu\text{m}$ has a peak quality factor frequency closer to 2.5 GHz, its quality factor is only 5.4% more superior and requires an additional 60% more silicon area as compared to the inductor with $16\ \mu\text{m}$ width conductor. From these results, two observations are made, the peak quality factor frequencies of inductors can indeed be adjusted desirably through the proposed optimization technique described in Fig. 12. The quality

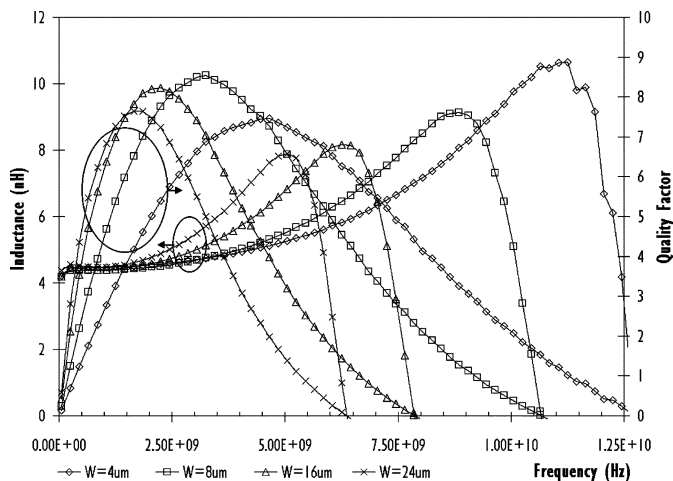


Fig. 16. Inductance and quality factor versus frequency for inductors with identical inductance ($4.4\ \text{nH}$) and core diameter ($100\ \mu\text{m}$) but different widths.

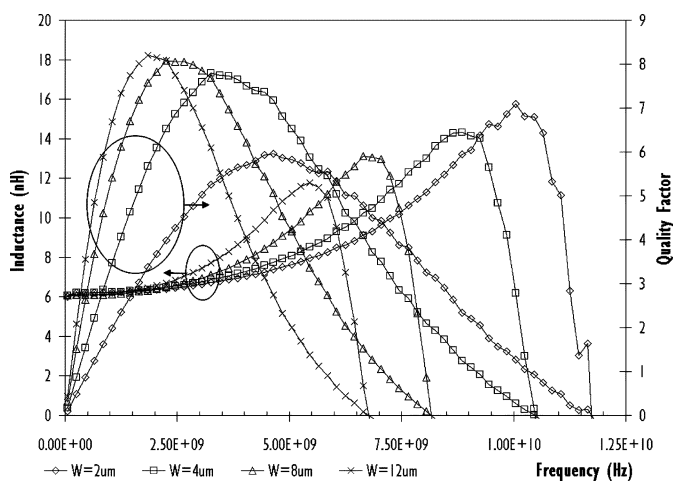


Fig. 17. Inductance and quality factor versus frequency for inductors with identical inductance ($6.2\ \text{nH}$) and core diameter ($100\ \mu\text{m}$) but different widths.

factor versus area consumption tradeoff is an important concept to convey to the industry since it will affect both the final performance as well as the die size of silicon-based RFICs.

More experiments are conducted for larger inductors, Fig. 16 and Fig. 17 show the inductance and quality factor plots for sets of 4.4 and $6.2\ \text{nH}$ inductors. Both plots show that at 2.5 GHz, the inductance values are all very close for the respective sets of 4 inductors and the most suitable width to design inductors with this range of inductance values, is about $8\ \mu\text{m}$ after considering the tradeoffs in quality factor, peak quality factor frequency response as well as the size of the inductors. For larger inductances such as the set of $8.2\ \text{nH}$ spiral inductors shown in Fig. 18, inductors with 4 and $8\ \mu\text{m}$ width both perform well and a conductor width of $6\ \mu\text{m}$ would likely be the optimal value for the inductor to have its quality factor peak at 2.5 GHz.

The experimental results in this subsection conclude that conductor width is an important design parameter to comprehend since it affects the per unit length inductance value, resistive loss as well as the peak quality factor frequency of spiral inductors. When the optimal conductor width is employed, the peak quality factor frequency can be aligned to the circuit operating

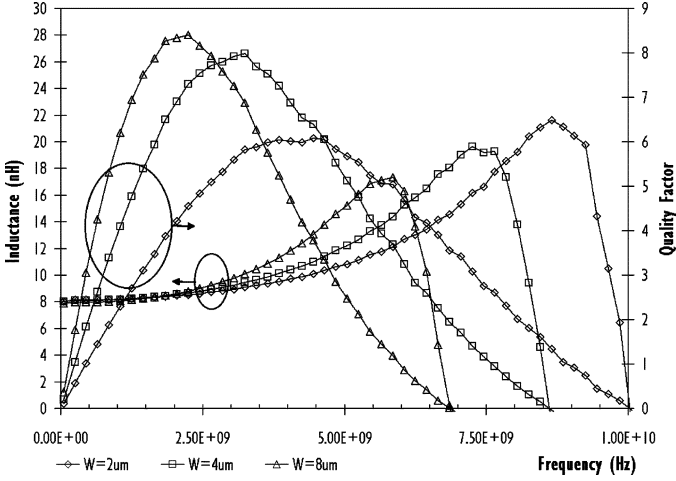


Fig. 18. Inductance and quality factor versus frequency for inductors with identical inductance (8.2 nH) and core diameter (100 μm) but different widths.

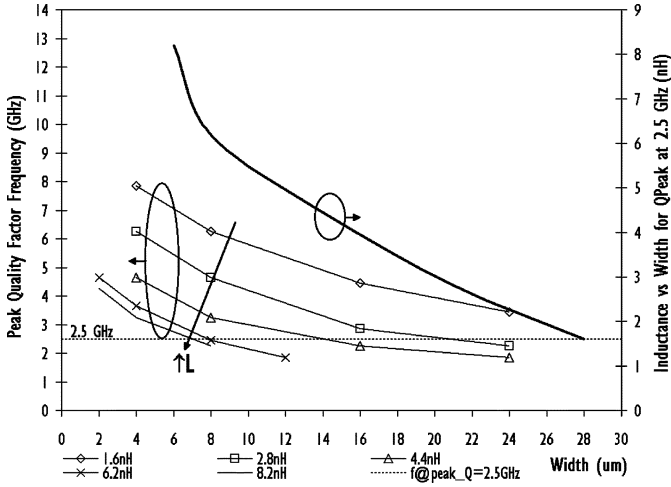


Fig. 19. Quality factor performance versus width for inductors with identical inductances and inductance versus width for inductors with QPeak at 2.5 GHz.

frequency and the spiral inductor's quality factor will be desirably large. Fig. 19 summarizes the peak quality factor frequencies of the respective sets of inductors derived from Figs. 15–18. It also reveals that in order to maintain the peak quality factor frequency at 2.5 GHz, when the inductance increases, the conductor width has to be reduced to minimize the substrate loss which is more dominant than its resistive loss for large inductors. In fact, having smaller widths for large inductors improves their performances and at the same time, reduces the silicon area they require. Small-inductance inductors, on the other hand, should be designed with large conductor width because while their relatively short total conductor length do not constitute to large capacitive parasitics, wide conductor widths result in smaller resistive loss, achieving significant improvement in the quality factor.

Empirical formulae which provide very accurate fit to the experimental data in Figs. 19 and 13 are developed to allow ease of designing inductors with their peak quality factor at 2.5 GHz in the 0.18 μm RFCMOS process. These formulae are shown in (4) and (5) with the boundary conditions of $0.5 \leq \text{IND} \leq 9.0$ nH

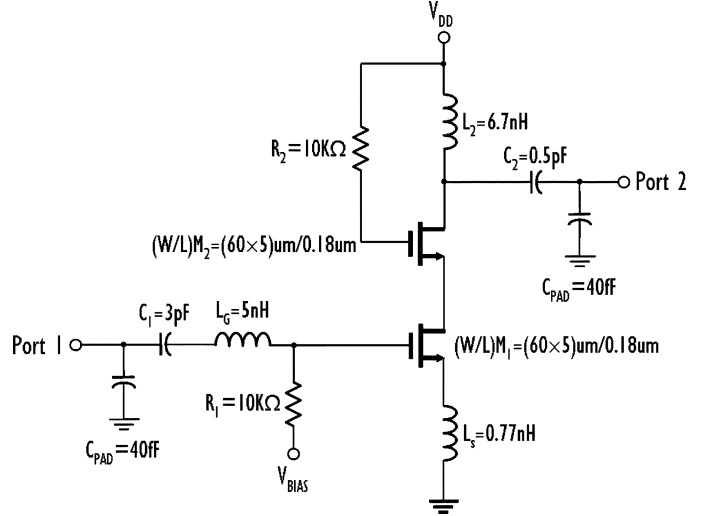


Fig. 20. Circuit schematic of a simple giga-hertz amplifier utilized to demonstrate performance enhancements when optimized inductors are used in the RFIC's design.

and $2 \leq W \leq 28 \mu\text{m}$, where IND and W denote the inductance and conductor width, respectively. To utilize these empirical functions, for a certain required inductance value, the optimal width W can be first evaluated using (4).

$$W(\mu\text{m}) = 4.5445E - 01 \times \text{IND}^2 - 7.8138 \times \text{IND} + 39.386 \quad (4)$$

$$\begin{aligned} \text{Length}(\mu\text{m}) = & 809.624 + 282.245 \times \ln(\text{IND}) \\ & - 3.640 \times W + 159.161 \times (\ln(\text{IND}))^2 \\ & + 2.653 \times W^2 + 46.717 \times \ln(\text{IND}) \times W \\ & + 52.908 \times (\ln(\text{IND}))^3 - 0.07404 \times W^3 \\ & - 1.0283 \times \ln(\text{IND}) \times W^2 \\ & + 4.562 \times (\ln(\text{IND}))^2 \times W \end{aligned} \quad (5)$$

Based on the optimal width from (4) and the required inductance, (5) (developed from Fig. 13) can then be used to determine the required total conductor length for the optimized inductor. These two geometrical parameters together with core diameter of 100 μm and spacing of 1.5 μm allow optimized inductors to be easily generated for use in 0.18 μm RFCMOS circuits operating at 2.5 GHz.

IV. GIGA-HERTZ AMPLIFIER USING OPTIMIZED INTEGRATED INDUCTORS

The proposed methodology for optimizing spiral inductors is evaluated using 2.4-GHz amplifiers with expected gain of about 14 dB. Fig. 20 shows the circuit schematic of the cascode amplifier utilized to demonstrate circuit performance enhancements when optimized spiral inductors are used in RFIC designs as compared to using nonoptimized inductors. Adopting the classical inductive source degeneration input matching technique, the gate-to-source capacitance of the input transistor M_1 , is matched to the external 50- Ω system at 2.4 GHz with L_G , L_S and C_1 . V_{BIAS} provides input biasing to M_1 and R_1 is used for isolation between the RF signal and dc biasing paths. M_2 , in common gate configuration, is employed to improve gain as

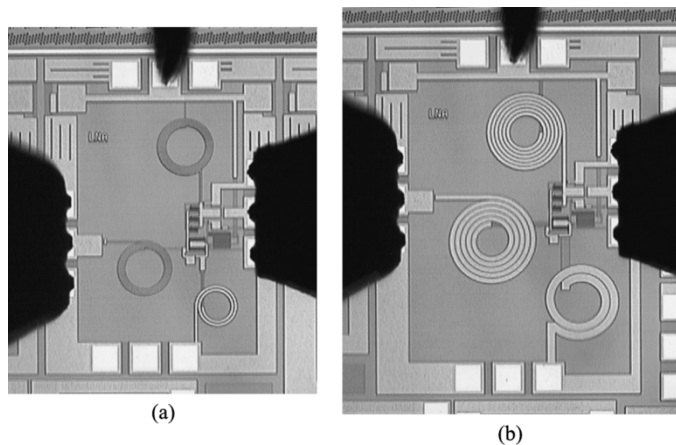


Fig. 21. Die photos showing on-wafer RF S -parameters and high-frequency noise characterization of amplifiers with (a) nonoptimized inductors and (b) optimized inductors.

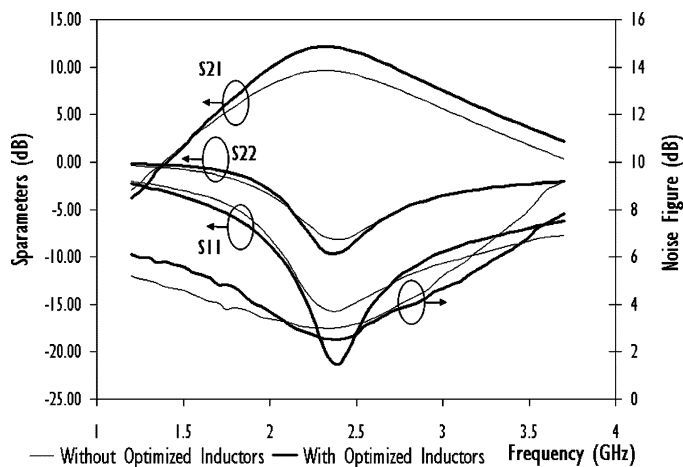


Fig. 22. Measured two-port S -parameters and noise figure of amplifiers with and without optimized spiral inductors.

well as isolation between the input and output port. R_2 provides stable dc biasing to M_2 and at the output stage, L_2 and C_2 are utilized for $50\text{-}\Omega$ load matching.

Two amplifiers have been fabricated, one with normal spiral inductors, another with optimized inductors having peak quality factor at 2.4 GHz. With peak quality factor frequency of 2.4 GHz, optimized inductors generally have quality factors at least 50% more superior than the nonoptimized ones. Die photos depicting on-wafer circuit characterizations of the two amplifiers are shown in Fig. 21. Pad capacitances have been taken into consideration during circuit simulations, as such; pad parasitic de-embedding is not required. Typical dies for circuit tests are selected based on full wafer map device characteristics obtained from RF scribbleline process monitoring test structures [10]. During measurements, overdriving the nMOSFETs into saturation is avoided by having low source power setting of about -20 dBm on the VNA.

Fig. 22 compares the two-port S -parameters and high frequency noise behavior of the two amplifiers. As opposed to using nonoptimized spiral inductors, optimized inductors offer a 26.6% gain improvement equivalent to 2.56 dB at 2.4 GHz.

Although larger die size of 28.6% is required, employing optimized inductors not only enhances the amplifier's gain and its matching characteristics, but also allow the amplifier to operate with a much lower noise figure of about 2.5 dB instead of 3.0 dB at 2.4 GHz. These circuit improvements are made possible because all loss mechanisms that would degrade the quality factor of inductors have been carefully considered and kept minimal at 2.4 GHz. Through this circuit-level verification, the proposed methodology for optimizing the physical design parameters of spiral inductors is shown to be reliable and capable of enhancing the circuit performance of silicon-based RFICs.

V. CONCLUSION

In this paper, spiral inductors were designed with similar inductance values as an experimental control to investigate quantitatively how their core diameter, conductor spacing, and width affect their performances. For the $0.18\text{-}\mu\text{m}$ RFCMOS technology, the inductor's core diameter must be larger than $100\text{ }\mu\text{m}$ to minimize degradation of its performance due to formation of conductor eddy current. Nevertheless, small inductors with narrow conductor widths, such as $4\text{ }\mu\text{m}$, are less susceptible to conductor eddy current effect and hence, employing small core diameters would help reduce the overall size of a circuit. Conductor spacing, on the other hand, should be kept minimal since it offers larger inductance value while consuming a smaller silicon area. Optimization of inductor's width allows peak quality factor of spiral inductors to be tuned at the circuit's operating frequency and in doing so, permits inductors over a wide range of inductance values to have relatively larger quality factors at that particular frequency of interest. This layout methodology has allowed deployment of optimized inductors in a giga-hertz amplifier, enhancing its gain, input/output port matching characteristics and noise performance significantly. Despite the fact that findings in this paper are derived from the $0.18\text{-}\mu\text{m}$ RFCMOS technology, important inductor test structure design considerations have been presented and these techniques can help device modeling and circuit design engineers systematically optimize the layout of their spiral inductors for different silicon processing technologies as well as circuit applications.

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Choon Beng Sia was born in Singapore in 1974. He received the B.E. (with honors) and M.E. degrees in electronics from Nanyang Technological University (NTU), Singapore, in 1999 and 2001, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at NTU.

He was with Chartered Semiconductor Manufacturing, Ltd., during his postgraduate degree and subsequently joined the SPICE Modeling Group as a Device Modeling Engineer in 2001. Currently, he is with Advanced RFIC (S) Pte, Ltd., as the

Engineering Manager in the RF Device Modeling Group. His research interests include design optimization and overtemperature modeling of integrated inductors, interconnects, MIM capacitors, MOS varactors, MOSFETs and SiGe transistors for RFIC applications. His most recent works involve the successful implementations of RF interconnect model and RF scribble process monitoring test structures for silicon technologies. He currently holds seven U.S. patents, with two pending and has authored ten technical publications.



Beng Hwee Ong was born in Singapore in 1975. He received the B.E. degree (with honors) in electrical engineering from the Nanyang Technological University (NTU), Singapore, in 2001.

He joined NTU as Research Staff in 2002, and is currently working on RFCMOS circuit designs.



Kwok Wai Chan received the B.E. (Hons) (Elect) and M.E. (Elect) degrees from Nanyang Technological University, Singapore, in 2001 and 2004, respectively.

He is currently with Advanced RFIC (S) Pte Ltd, Singapore, as an Engineering Manager in the Electronic Design Automation Group. His research interests involve the development of automated RFIC design kits.



Kiat Seng Yeo received the B.E. degree (with honors) in electronics and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 1993 and 1996, respectively.

As Sub-Dean and Associate Professor of Electrical and Electronic Engineering at NTU, he is a recognized expert in CMOS technology and low-power CMOS IC design. He is Consultant to multinational corporations and serves on the program committee of several international conferences. His research interests include device modeling and RF IC design. He holds 11 patents, has published four books and over 200 papers in his areas of expertise.



Jian-Guo Ma (SM'00) received the B.Sc. and M.Sc. degrees (with honors) from the Lanzhou University, China, in 1982 and 1988 respectively, and the Ph.D. degree in engineering from the Gerhard-Mercator University, Germany in 1996.

From 1982 to 1991 he was with Lanzhou University working on RF and microwave engineering. Before he joined Nanyang Technological University (NTU), Singapore, in 1997 he was with the Technical University of Nova Scotia, Canada. He is currently an Associate Professor and Director of the

Center for Integrated Circuits and Systems, NT. His research interests include RFIC designs for wireless applications, RF characterization, and modeling of semiconductor devices, RF interconnects and packaging, SoC, and applications and EMC/EMI in RFICs. He has published more than 130 technical papers and two books in above mentioned areas. He holds six patents in CMOS RFICs.

Dr. Ma is the Associate Editor for IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.



Manh Anh Do received the B.E. degree (with honors) in electronics, and the Ph.D. degree in electronic engineering from the University of Canterbury, New Zealand, in 1973 and 1977, respectively.

Between 1977 and 1989, he held various positions including: Research and Development Engineer and Production Manager at Radio Engineering, Ltd., Research Scientist at Fisheries Research Center, New Zealand, and Senior Lecturer at National University of Singapore (NTU), Singapore. He joined the School of Electrical and Electronic

Engineering (EEE), NTU, as a Senior Lecturer in 1989, and obtained the Associate Professorship in 1996 and the Professorship in 2001. He has been a Consultant for many projects in the Singapore electronic industry, and was the Principal Consultant for the design, testing, and implementation of the US \$200 million electronic road pricing island-wide project in Singapore, from 1990 to 2001. His current research is on digital and mobile communications, RF IC design, mixed-signal circuits, and intelligent transport systems. Before that, he specialized in sonar designing, biomedical engineering, and signal processing. Since 1995, he has been Head of Division of Circuits and Systems, School of Electrical and Electronic Engineering, NTU.

Dr. Do is a Fellow of the Institution of Electrical Engineers (IEE), U.K., a Chartered Engineer (U.K.), a Professional Engineer (Singapore) and Associate Editor for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.