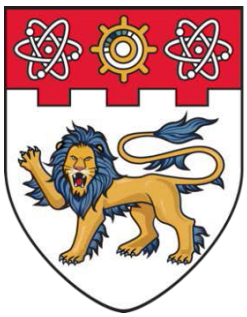

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

High Precision Biomedical Sensor Readout Circuits Design for Wearable Health Monitoring System

ZHOU WEI

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2019

High Precision Biomedical Sensor Readout Circuits Design for Wearable Health Monitoring System

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

3 March 2020	
Date	ZHOU WEI

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

3 March 2020

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Date

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A/P Goh Wang Ling

Authorship Attribution Statement

This thesis contains material from four papers accepted at conferences and two journal papers in peer-review in which I was listed the first author.

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(2) W. Zhou, W. L. Goh and Y. Gao, "Integrated Temperature Sensor with CMOS Relaxation Oscillator Based Sensor Interface for Biomedical Sensing," *2019 Electron Devices Technology and Manufacturing Conference (EDTM)*, Singapore, Singapore, 2019, pp. 416-418.

(3) W. Zhou, W. L. Goh Y. Gao, “A 3-MHz 17.3-μW 0.015% Period Jitter Relaxation Oscillator with Energy Efficient Swing Boosting”, *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, Early Access.

The contributions of the co-authors are as follows:

- A/Prof Goh Wang Ling and Dr. Gao Yuan provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by A/Prof Goh Wang Ling and Dr. Gao Yuan.
- I co-designed the core circuit with Dr. Gao Yuan and Dr. Jia Hao Cheong and performed all the simulation work at the Institute of

Microelectronics (IME), A*STAR, and VIRTUS, the School of Electrical and Electronic Engineering (EEE), NTU.

- All chip die fabrication was supported by A*STAR BMRC (Biomedical Research Council), Singapore under the grant no. IAF311022.
- The chip measurement was conducted in laboratory of the Institute of Microelectronics (IME), A*STAR by me with the assistance from Dr. Gao Yuan. Data collection and analysis were done by me.

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(2) W. Zhou, W. L. Goh, and Y. Gao, “A 1.6 MHz Swing Boosted Relaxation Oscillator with Voltage-to-Delay Feedback,” *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, to be submitted by Aug 2019.

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(2) A journal of W. Zhou, W. L. Goh, Y. Chen, T. Zhang and Y. Gao, "A 100-mV_{pp} Input Range 10-kHz BW VCO-based CT-DSM Neuro-Recording IC in 40-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, to be submitted after chip fabrication and measurement are done.

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- I co-designed the core circuit with Dr. Gao Yuan, Dr. Yi Chen and Dr. Tantan Zhang, and performed all the simulation work at the Institute of Microelectronics (IME), A*STAR, and VIRTUS, the School of Electrical and Electronic Engineering (EEE), NTU.
- All chip die fabrication was supported by A*STAR BMRC (Biomedical Research Council), Singapore under the grant no. IAF311022.

3 March 2020 . . . . . Date

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Abstract

With the fast-growing pace of the aging population, there is increasing need to monitor the elderly health status by continuously tracking their vital signs in daily life. Conventional vital signs monitoring devices are usually bulky, expensive and power-hungry, and thus, the usage is limited to within the hospital and is not suitable for daily use in the home environment.

A miniaturized wearable biomedical signal monitoring system is considered as a game changing technology to enable remote monitoring and diagnosis for personalized home healthcare. However, technology features such as the compatibility of readout circuit with different types of biomedical sensors, low power consumption for prolonged continuous usage, high signal resolution and robust performance against environment changes are all key design challenges that remain to be solved.

In this thesis, time-domain resistive/capacitive sensor readout circuit is explored as an alternative solution to the conventional voltage/current sensor readout circuits. The research can be categorized into two parts. Firstly, RC relaxation oscillators, which are employed as frontends of sensor readout circuit, are presented. A novel energy efficient swing boosting technique is proposed in the first oscillator, while a novel voltage-to-delay feedback with switch capacitor swing boosting technique is proposed in the second oscillator. Experimental measurements had demonstrated their effectiveness in suppressing output phase noise while for the second technique, in achieving high output accuracy too. Secondly, a VCO-based Delta-Sigma Modulator (DSM) readout circuit is proposed for bio-signal recording. A VCO-based frontend and system feedback is proposed to replace the conventional amplifier-based frontend with open-loop structure. It can operate with large input range of up to 100-mV_{pp}, as well as with wide signal bandwidth, high energy efficiency and high output resolution.

Despite the work done, the challenges lying ahead are still exciting. These challenges can be viewed in two parts, the integration of proposed frontends into systems, and the creation of even better readout circuits. Plans to deal with them are constantly being generated and more contributions to the subject matter will certainly be made in the near future.

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Chapter 1

Introduction

This chapter provides the background information and motivation on the proposed research topic, identifies the existing design challenges, specifies the research objectives and the major contributions of this research, and presents the organization of this thesis.

1.1 Background and Motivation

With the fast-growing pace of the aging population, there is an increasing need to monitor the elderly health status continuously. Continuous health monitoring in daily lives is critical and essential to keep track of the real-time elderly health conditions and to detect potential emergencies which can be fatal. According to a recent fact sheet from the World Health Organization (WHO) [1], noncommunicable disease, which is known as chronic diseases, is accountable for the annual death up to 41 million. This is equivalent to 71% of total global death every year. Due to the long-term nature of chronic diseases, it is impractical to provide life-long hospitalization to all the patients suffering from such diseases. Wearable health monitoring system provides a convenient way for continuous health monitoring outside of clinical environment. Therefore, wearable health monitoring for daily lives is a game changing technology, to enable remote monitoring and diagnosis for personalized home healthcare.

A wearable health monitoring system generally consists of multiple wearable biomedical sensor devices, a power supply unit, a data recorder and a wireless transmission unit. A typical system is shown in Fig. 1 [2]. Different types of vital signs and body status data are collected by various wearable biomedical

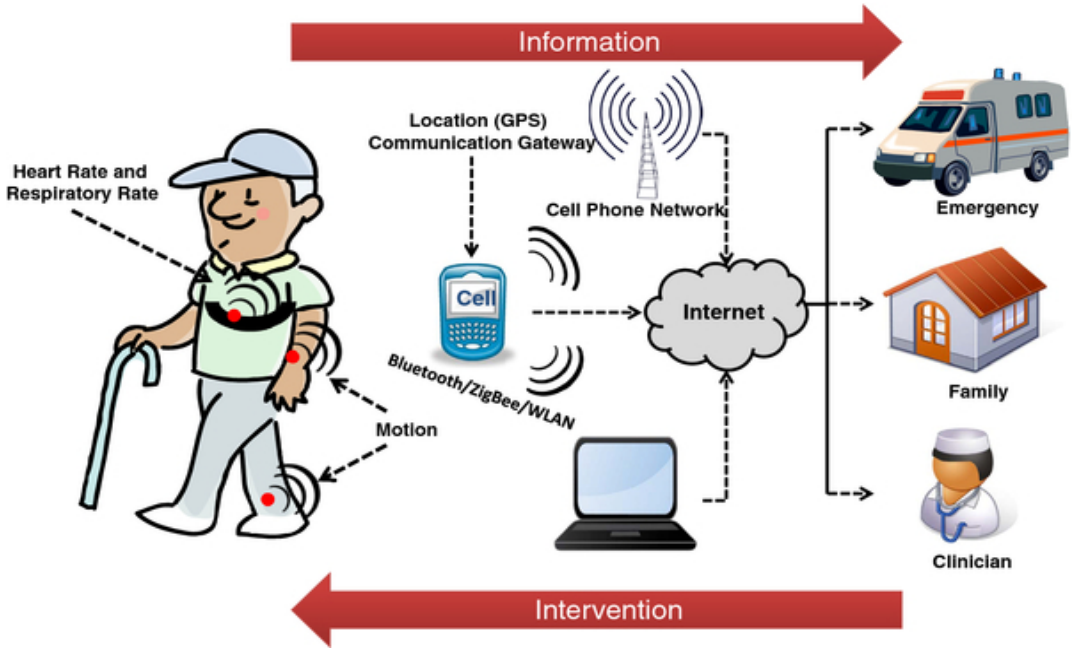

Fig. 1: An illustration on wearable health monitoring system [2].

sensors attached to the human body. The collected data are transferred to a central node such as the smart phone or computer for data processing and then sent to the healthcare providers for status monitoring or diagnosis. As a highly integrated large-scale system, the wearable health monitoring system has drawn lots of attentions from multiple disciplines including the integrated circuit (IC) design community. Instead of focusing on the entire monitoring system, we would like to narrow down the discussion to one of these subsystems, namely the biomedical sensor device system.

As an integral part of a wearable health monitoring system, the wearable biomedical sensor device has inevitably been a popular research topic and consumer product in recent years. The market revenue is predicted to reach 44 billion for year 2020 [3]. Renowned consumer electronics companies such as Phillips and Apple also join the field continuously bringing prosperity to the market. The increase in interests for such devices has not only come from the aforementioned increase in patients with chronic diseases needing continuous health monitoring, but also the expanded public awareness in personal health management. Healthy individuals nowadays are also interested in knowing what is happening in their body for general health maintenance and early disease detection. These devices thus provide a convenient way for people to monitor

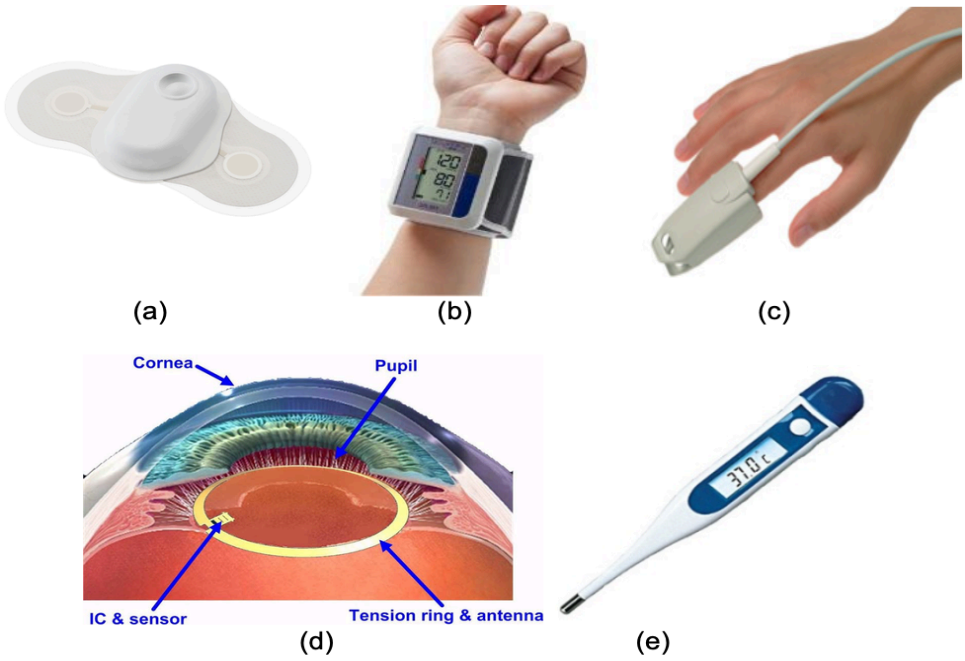

Fig. 2: Various wearable biomedical sensor devices: (a) TAGECG wearable ECG sensor device from Welch Allyn, (b) Blood pressure sensor device, (c) SpO2 blood oxygen saturation sensor device, (d) Intraocular pressure/temperature sensor, (e) Body temperature sensor.

their own body conditions, at anytime and anywhere, without being intensively interfered in their daily activities. The data collected in various daily activities can also better support the overall body performance evaluation, the disease diagnosis or the post-disease/injury recovery [4]. Fig. 2 provides some wearable biomedical sensor devices, such as the electrocardiogram (ECG) sensor in (a), the blood pressure sensor in (b), the blood oxygen saturation sensor in (c), the intraocular pressure sensor in (d) and the temperature sensor in (e). The physical parameters collected by these devices are vital to determine if there are abnormal health conditions. The collected ECG signals reflect if a person is having abnormal heart activities such as arrhythmia which indicates the possibility of having a heart disease. A sudden increase or decrease in body temperature and/or pressure suggests that a person may have infection or experiencing extreme environment. The data on blood oxygen saturation reflects if an unconscious patient is suffering from hypoxia.

The traditional clinical sensor devices for health monitoring, such as Philips bedside patent monitor series, are usually bulky, expensive, power-hungry, and hence inconvenient for daily use. However, with the continuous development

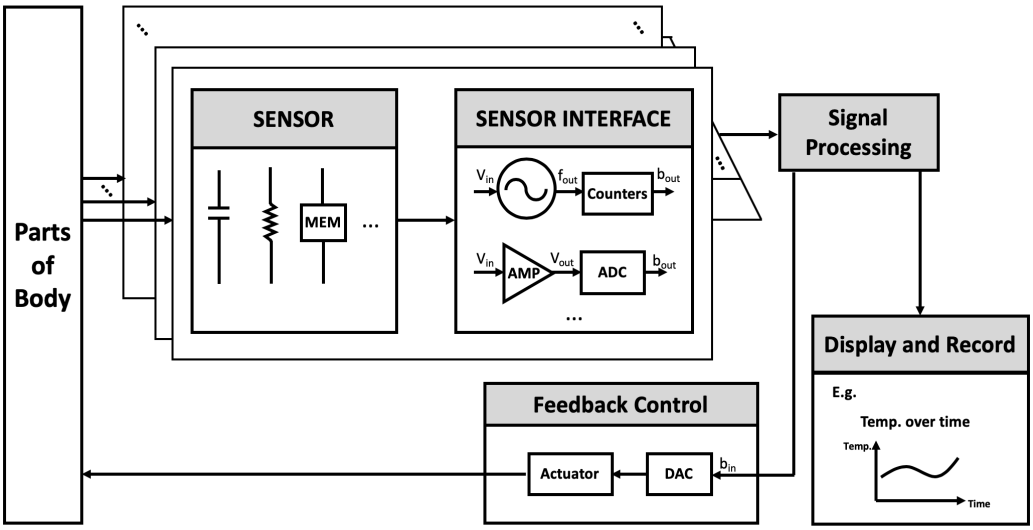

Fig. 3: A general illustration on Sensor System [8] [9].

and innovation in manufacturing process and System-on-Chip (SoC), a complicated sensor system can now be scaled down and fabricated on a single or multiple semiconductor chips. The advance in technology and IC design significantly reduces the size, manufacturing cost, and power consumption as compared to traditional devices, resulting in the development of miniaturized wearable biomedical sensor systems for personalized healthcare.

Various miniaturized wearable biomedical sensor systems are continuously being developed. Some examples of emerging miniaturized wearable sensing technologies are presented in [5] [6] [7]. Despite the different functions, a general illustration of the sensor system can be summarized in Fig. 3 [8] [9]. A sensor array interacts with the sensing target, e.g. parts of human body, and changes its properties according to the measurand. The changing properties can be the sensor impedance, the semiconductor device characteristics, the geometric shape, the heat transfer, the chemical reaction on the sensor surface, etc., depending on the sensing mechanism and types of sensor employed [8]. The change in the sensor property is perceived as a proportional change in electrical parameter by the sensor interface circuit or the sensor readout circuit which generates corresponding digital bitstream as outputs. For some systems with feedback control, the digital bitstream will be converted back to an analog signal which modifies the measurand via an actuator. One example with feedback control is the close-loop neural recording system. This kind of system is usually implemented with the neural stimulator to collect the potential from the

tissue under stimulation, so as to adjust stimulator's signal strength. This prevents possible damage to the tissue by large stimulation signal and improves the treatment outcomes [10].

Many biomedical sensors and sensor systems have been reported in the literature [11] [12] [13] [14] [15]. Due to the different nature of sensors, dedicated sensor readout circuit usually has to be designed for each type of sensor. For example, capacitive and resistive sensors traditionally require different sensor interface architectures, which demands more designing efforts, time and cost. Furthermore, the outputs of these interfaces can be in the form of voltage or current, which complicates the backend data collection. All these problems degrade the robustness of the traditional sensor interface architecture.

The idea of designing a sensor interface compatible to multiple types of sensor has been rising in the recent years. With the extensive use of capacitive and resistive sensors in wearable health monitoring devices, designing a unified sensor interface that is compatible to both types of sensors has become an interesting topic of research. One approach to achieve this goal is by adopting the relaxation oscillator-based sensor interface frontend that is able to convert either capacitance or resistance to frequency output. Previous work such as [6], [7] and [16] have demonstrated the feasibility of this concept. In [6], a system which monitors the blood pressure in the prosthetic vascular graft for early failure detection incorporates the relaxation oscillator as its sensor interface frontend to successfully convert the resistive sensor resistance into frequency. In [7] and [16], instead of resistive sensor, the capacitive sensor is adopted for intraocular pressure sensing [7] and general pressure sensing applications [16]. Both designs also utilize relaxation oscillator as their sensor interface frontend circuit. These examples proved that the relaxation oscillator is an ideal candidate for unified sensor interface frontend, and therefore, it is thoroughly studied in this thesis.

In addition, for sensor interface designed for sensing bio-signals, its desirable input bio-signal will be coupled with large-amplitude artifacts generated from the body tissue movement, electrode offset, and/or stimulation. Due to the large artifacts amplitude, traditional sensor interface frontends such as [17] [18] [19] which can only handle inputs amplitude of a few millivolts can

easily saturate and thus, needing a long time to recover. Therefore, a sensor interface which can accommodate large input range has become a popular topic recently. Instead of adopting power hungry wide input range frontend, the more energy efficient method to achieve this goal is by adopting the voltage-controlled-oscillator (VCO) -based Delta-Sigma modulator (DSM) as the bio-signal sensing interface. Since the VCO's output phase is in phase domain and will theoretically not be limited by voltage headroom, the output of Gm-VCO frontend is inherently resistive to saturation for any given input and therefore suitable as bio-signal sensing interface, providing the output phase frequency is well within the phase quantizer's speed limit. As a result, this architecture is also studied in this thesis.

1.2 Challenges

The following challenges are identified after reviewing the state-of-the-art in chapter 2:

1) Designing relaxation oscillators with low output noise and high output accuracy over supply and temperature variations for sensor interface frontend application.

2) Attaining a high input range energy-efficient VCO-based DSM as bio-signal sensing interface.

1.3 Objectives

In accordance with the key challenges identified, the following research objectives are proposed, encompassing design methodology to circuit block implementation.

1) System level analysis to explore new sensor readout circuit with low noise, low power consumption, and compatibility with capacitive and resistive sensors for general sensing application. Also, new sensor interface with large input range and energy efficiency for bio-signal recording will be studied.

2) Circuit level design of the key building circuit blocks including but not limited to the analog frontend and data converter.

3) Circuit implementation in CMOS technology and chip measurement and

evaluation.

1.4 Major Contribution of Thesis

The major contributions of this thesis are summarized as follows:

1) On the circuit and system level, two novel RC relaxation oscillators are proposed as sensor interface frontend and one VCO-based DSM sensor interface is proposed for bio-signal recording application. The two RC relaxation oscillators achieve excellent noise performance, demonstrating their potential for high precision sensing. The VCO-based DSM sensor interface circuit is capable of quantizing a large input signal up to 100mVpp while consuming a low power, manifesting its ability for low power bio-signal recording application.

2) For the design approach, an energy efficient swing boosting technique is proposed to achieve optimized trade-off between circuit energy efficiency and noise performance. Also, a voltage-to-delay (VDF) feedback with switch capacitor swing boosting (SCSB) architecture is proposed to achieve both low noise and low frequency inaccuracy over temperature and supply variations. Furthermore, a VCO-based voltage-to-phase conversion technique with close-loop configuration is proposed to achieve low power bio-signal recording with high input range.

3) At the circuit implementation level, various design considerations, such as the transistor sizes, types, operating regions, have been made for better circuit performance.

1.5 Organization of the Thesis

Chapter 1—Introduction provides background information on wearable healthcare monitoring system and general sensor devices. From that, the advanced miniaturized sensor devices based on SoC are introduced, which show great potential in replacing the current bulky devices and traditional medical practices. The research topic of the sensor interface is then formulated. The challenges of the subject matter are identified, followed by objectives to be achieved throughout this research. The major contribution of this thesis is summarized at the end, leading to detailed discussions in following chapters.

Chapter 2—Literature Review provides reviews on relaxation oscillators and VCO-based DSMs, which are popular architectures for general impedance sensor interface and bio-signal recording interface, respectively. Detailed discussions on the designs of both interfaces are provided, including existing approaches to resolve current problems, advantages and disadvantages of these approaches, and the enlightenment gained from these literatures.

Chapter 3—Relaxation Oscillator with Low Jitter Energy Efficient Swing Boosting presents the 1st proposed relaxation oscillator design which aims to achieve both low output phase noise and high energy efficiency at the same time. This chapter starts with a brief discussion on previous designs and why they are not suitable for achieving our target. Two typical designs are analyzed, from which new ideas are generated, leading to the next phase of discussion on the proposed design. The system architecture, design techniques proposed, and circuit block implementation of the proposed design are presented later with measurement results which verifies the feasibility of the idea and the functionality of the proposed design.

Chapter 4—Relaxation Oscillator with Voltage-to-Delay Feedback and Switch Capacitor Swing Boosting presents the 2nd proposed relaxation oscillator which aims to improve the frequency accuracy over supply and temperature variations while at the same time reducing the output phase noise. The chapter starts by discussing the cause of frequency inaccuracy over supply and temperature variations, followed by a brief discussion on previous methods proposed in reducing the inaccuracy. From there, the new idea is generated, and the proposed design is presented with system architecture, circuit implementation and measurement results.

Chapter 5—Wide Input Range Wide Bandwidth VCO-based CT-DSM Neuro-Recording Interface presents the 3rd proposed design dedicating to bio-signal recording application. The chapter starts with identifying the existing problems in the subject matter and setting the design target. Some existing designs are summarized with their advantages and disadvantages. The proposed design is presented later in details with simulation results.

Chapter 6—Conclusion summarizes our research work done so far and suggests the direction and focus of our next stage of research, which forms the starting point of our future works.

Chapter 2

Literature Review

Many sensor readout circuit architectures are proposed for general sensing applications in previous literatures. Two widely researched architectures include the analog-to-digital converter (ADC) -based, mostly delta sigma modulator based, capacitance-to-digital converter [20] [21] [22] [23], and oscillator-based impedance-to-digital converter [24] [16] [25] [26] [27]. In this work, the latter is chosen for its potential in low power operation yet high resolution, compatibility to both capacitive and resistive sensors, robustness in scaling under different technology nodes, and simplicity in circuit implementation. As one of the most important building blocks of this type of sensor interface, the oscillator, which is usually the relaxation oscillator, is extensively studied in this thesis because its noise, energy efficiency and frequency accuracy over the supply and temperature variations directly affects the interface's accuracy and resolution in converting the measured value. On the other hand, a dedicated type of sensor interface, namely the bio-signal recording interface, is also studied and is still being studied as an extension of the current research and a beginning to future work. Due to the precision requirement on the conversion result, the bio-signal recording interface is commonly built based on analog front-end amplifier followed by an ADC block [28] [29] [17] [18] [30]. It achieves high to medium conversion accuracy depending on the actual design but suffers drawbacks such as limited input range, supply headroom requirement, and complexity in implementation during process scaling. As a result, the VCO-based neuro-recording interface has become an extremely popular alternative to the traditional architecture [31] [32] [33] [34] [35] recently. This architecture consists

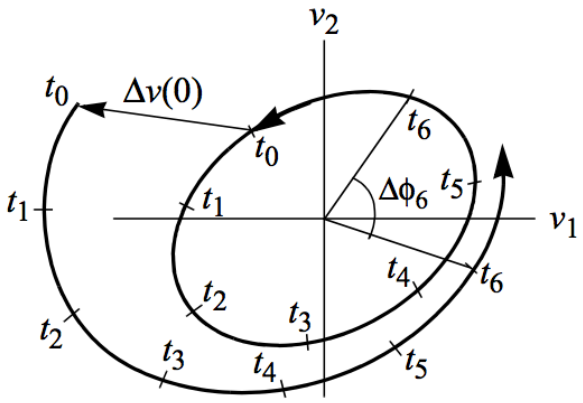

Fig. 4: The trajectory of an oscillator shown in state space with and without a perturbation ∆v.

of mostly digital blocks and therefore, easy to be implemented in different process and supply voltage. It also achieves moderate accuracy which can accommodate different application requirement. Therefore, in this chapter, a literature review on the relaxation oscillators is first presented, followed by a review on the VCO-based neuro-recording interfaces.

2.1 Background Theories

Noise performance is one of the major concerns when designing RC relaxation oscillator. This is because any noise presented in this autonomous circuit takes a chance to cause a distortion of the output frequency, surfaced by the presence of phase noise or timing jitter. This section summarizes oscillator noise which includes background on the oscillator phase noise, the relationship between phase noise and jitter, and the two types of Figure of Merit (FOM) that are commonly adopted for oscillator performance evaluation.

Noise causes both amplitude and phase change in the oscillator output. However, thanks to the rail-to-rail output of the RC relaxation oscillator, the amplitude perturbation due to noise will be naturally suppressed. This phenomenon is graphically explained in Fig. 4 [36]. In Fig. 4, the inner ellipse illustrates the trajectory of an oscillator without any perturbation while the outer arc represents one with both amplitude and phase perturbations. $\Delta v(t)$ represents the vector of change of the oscillator state. It can be seen from the graph that the change of amplitude is suppressed over time while the change in

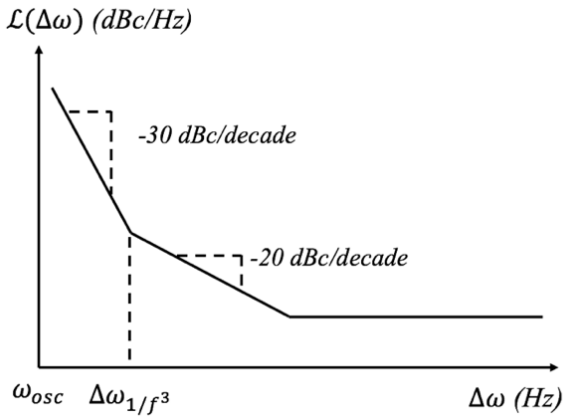

Fig. 5: Phase noise power spectrum.

phase accumulates unboundedly. The theoretical explanation is provided in [37] and [38]. This suggests that the noise performance of the RC relaxation oscillator is mainly limited by its phase noise.

The power spectrum of the oscillator phase noise is illustrated in Fig. 5. Previous studies [38] [39] have suggested that the -30dBc/dec region is due to the frequency modulation of 1/f noise while the -20 dBc/dec region corresponds to the white noise. Therefore, to reduce the oscillator phase noise, both noises should be reduced.

Timing jitter refers to the phenomenon in which the transition of a time domain waveform deviates from its ideal position as a result of the presence of phase noise. Therefore, it is a time-domain representation of phase noise. For comparison between oscillators with different frequencies, instead of the absolute jitter, the relative jitter is commonly used, and is represented by

$$\text{Normalized jitter} = \frac{\sigma}{\mu} \tag{1}$$

where σ and μ are the standard deviation and mean of the oscillation period [40].

To evaluate the overall oscillator performance, two FOMs are commonly adopted. For evaluation of trade-off among oscillator's noise, power and frequency, the parameter used is

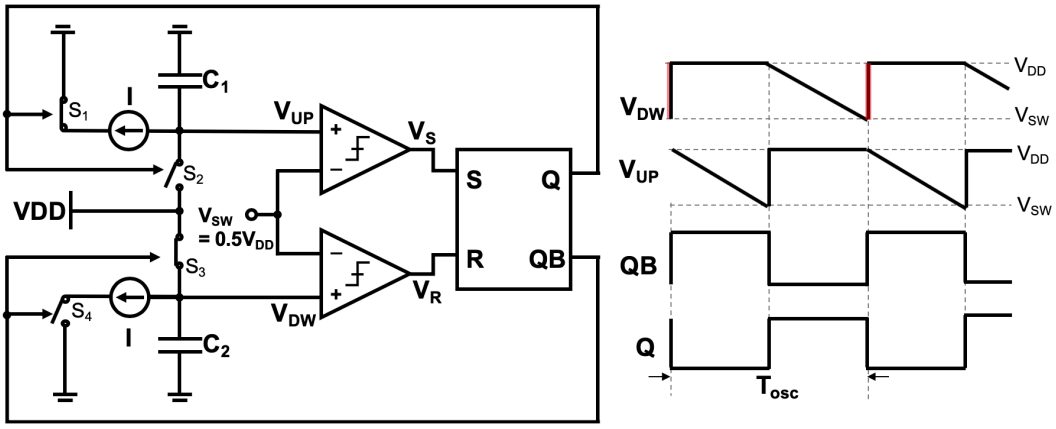

Fig. 6: Conventional relaxation oscillator.

$$\text{FOM}=10\log\left(L(\Delta f)\cdot\left(\frac{\Delta f}{f_{osc}}\right)^2\cdot\left(\frac{P_{total}}{1\ \text{mW}}\right)\right) \quad (2)$$

where f_{osc} is the oscillator nominal frequency, Δf is the frequency offset from the oscillator nominal frequency, $L(\Delta f)$ is the oscillator phase noise at a frequency offset Δf, and P_{total} is the oscillator average power. The other FOM is used for evaluation of the oscillator's energy efficiency. Instead of being named as FOM, it is usually referred as Energy-per-Cycle, which will be discussed in detail in section 3.3 of chapter 3.

2.2 Previous Designs

2.2.1 Conventional Relaxation Oscillator

The system architecture and corresponding timing diagrams of the conventional relaxation oscillator is shown in Fig. 6, which was first proposed in [41]. It consists of two comparators, one SR latch, two timing capacitors C_1 and C_2, and a switch network. With initial conditions specified for oscillator outputs, i.e. Q = LOW and QB = HI, switch S_1 and S_3 are closed while S_2 and S_4 are opened. As a result, timing capacitor C_1 is discharged by the constant current source I and C_2 is charged to the supply V_{DD}. These charging and discharging events are manifested by the decreasing V_{UP} and the step increment of V_{DW}. Since the current source I is constant, the V_{UP} slope is constant and equals to

the value of I/C_1. When V_{UP} drops below the comparator switching threshold V_{SW}, V_S will be set to LOW. By the same token, V_R will be set to HI when V_{DW} rises to equal to V_{SW}. As a result, the SR latch toggles, generating output Q = LOW and QB = HI. These new states of Q and QB will trigger another round of charging/discharging event for the timing capacitors, which then change the states of Q and QB. This process iterates itself, giving a rail-to-rail oscillation output waveform at Q and QB. Assuming negligible circuit delay and all circuit components are ideal, the theoretically output frequency f_{osc} is expressed as:

$$f_{osc} = \frac{I}{2CV_{SW}} \quad (3)$$

where f_{osc} is the oscillation frequency, I is the constant current value, C is the timing capacitance and $C = C_1 = C_2$, and V_{SW} is the comparator switching threshold which is usually chosen as $0.5V_{DD}$.

The advantage of this design is that it integrates the SR latch to generate complementary rail-to-rail outputs which mitigates the output amplitude noise. Also, the use of a constant current source as the discharging pump linearizes the capacitor discharging waveform which permits an easier computation and control of the oscillation frequency.

However, there are also some problems associated with this architecture. The constant current source, which is usually implemented using single CMOS transistor, generally contains more noise power as compared to a single passive resistor, assuming the same voltage (>2kT/q) across both components. This makes this structure less suitable for low noise application. Moreover, the current source may shift its operating regions throughout oscillation, which alters the capacitor voltage slope and causes frequency inaccuracy. Furthermore, two comparators are needed for this structure which translates to additional power, larger chip area, and more layout matching effort. More details are provided in chapter 3, section 3.3.1.

On the other hand, as a non-ideal factor, the circuit delay τ_d is inevitable for all relaxation oscillators. It will be directly added into oscillation period if no compensation is done. Since its value changes with supply voltage and

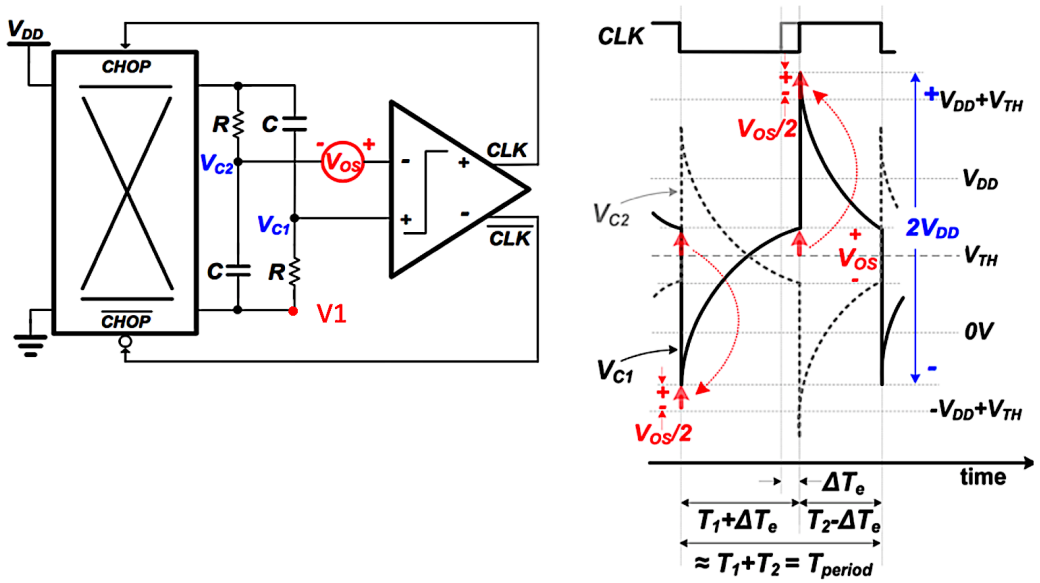

Fig. 7: Relaxation oscillator from [42].

temperature, the frequency accuracy will be undermined. More discussions on circuit delay will be provided in Chapter 4.

2.2.2 Relaxation Oscillators with Low Phase Noise

As proven by previous researches, all noise existing in relaxation oscillator circuit will manifest as phase noise at the output frequency. To design relaxation oscillator for sensor interface application, low phase noise is therefore a target to be achieved.

Many designs have been proposed to reduce the phase noise. There are two main approaches: (1) Direct noise reduction; and (2) Deploying compensation circuit. The direct noise reduction is achieved by either increasing the capacitor voltage slope at the point where the capacitor voltage crosses the comparator switching threshold or reducing the noise seen by the timing capacitor [42] [43] [44]. The compensation method involves designing circuits which mainly focus on reducing long-time frequency fluctuation due to low frequency noise [45] [46] [47].

Fig. 7 illustrates the design in [42]. This design employs an inverter-based comparator together with a chopper which reverses voltages across the RC branch periodically, charging and discharging the timing capacitor C. Referring to the timing diagram, when V_{C1} charges to near the comparator switching

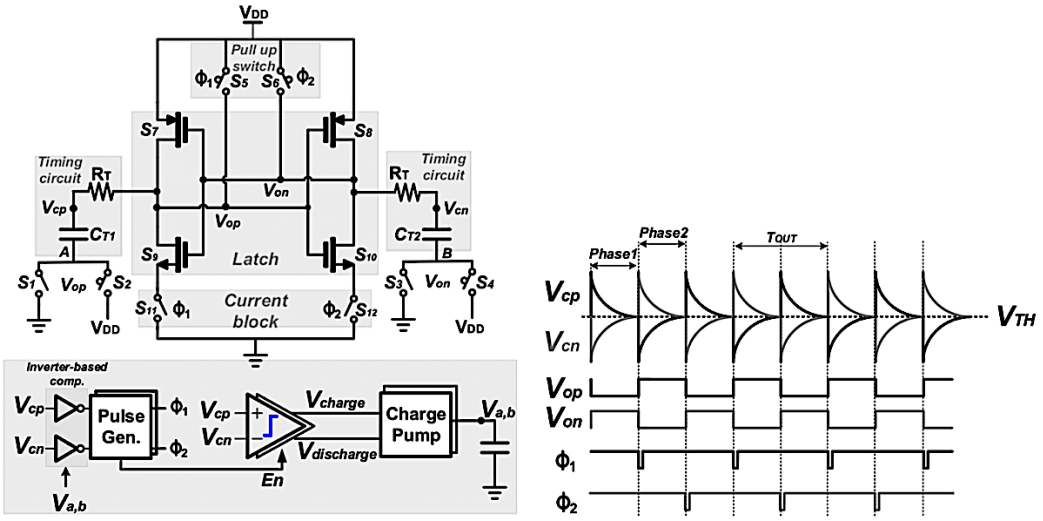

Fig. 8: Relaxation oscillator from [43].

threshold V_{TH}, the comparator toggles and its two outputs are inverted. This reconfigures the chopper and reconnects V1 to V_{DD}, boosting V_{C1} to $V_{DD} + V_{TH}$ before discharging. As a result, V_{C1} discharges from a voltage higher than V_{DD} without affecting the oscillation period. This is equivalent to increasing the capacitor voltage slope and as a result, when V_{C1} crosses V_{TH}, which equals to $V_{DD}/2$, the effective slope is boosted, and the phase noise is suppressed. Similarly, before the charging cycle, V_{C1} is pulled to $-V_{TH}$ by the chopper due to comparator outputs transitions. Therefore, when V_{C1} charges to V_{TH}, the capacitor voltage slope is also boosted. Meanwhile, due to the symmetry between waveforms V_{C1} and V_{C2}, the output clock is naturally resilient to the comparator's offset voltage V_{OS}, though it is still susceptible to layout mismatch among the comparator input transistors. Meanwhile, the comparator used in this design is of inverter-based, which has lower input-referred noise and thus, reduces the noise seen by capacitor. The reported measured FOM is 162.1 dBc/Hz, which is the highest up to date. The frequency inaccuracy over supply and temperature is 0.44%/V over 1.4 V to 2 V and 137 ppm/°C over -40°C to 125°C, which are moderate.

This swing boosting technique is also adopted in [43] with comparator offset cancellation logics added. The circuit and corresponding waveforms are shown in Fig. 8. Similar to previous design [42], the swing boosting is also achieved by switching timing capacitors' terminal voltages. However, other than simply

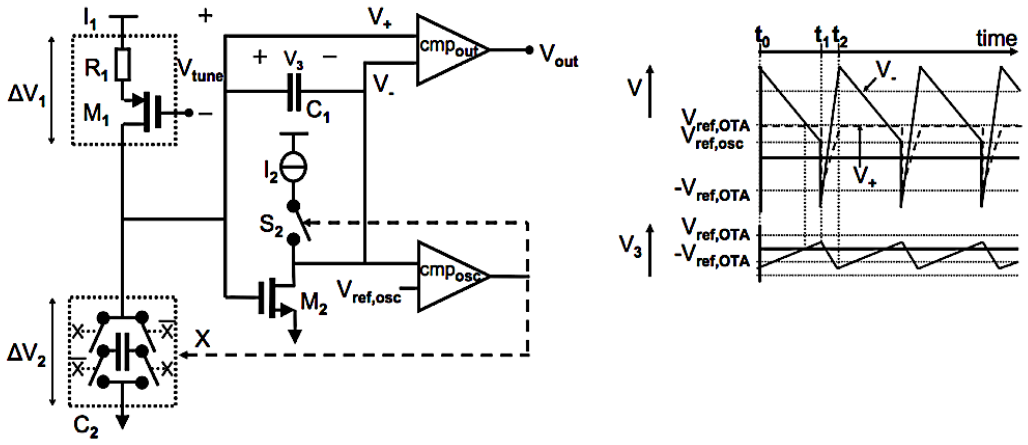

Fig. 9: Relaxation oscillator from [45].

relying on the timing signals' symmetry to achieve comparator offset cancellation, an offset cancellation logic called self-threshold tracking is proposed. When there is an offset between two timing signals V_{cp} and V_{cn}, the body voltage of inverter-based comparator shown is adjusted, resulting in adjusted switching threshold for inverter-based comparator shown. This is equivalent to adjust the output transition point, which in turn regulates and mitigates the difference between V_{cp} and V_{cn} since the output transition decides when V_{cp} and V_{cn} are charged/discharged. Furthermore, it also claims that due to the self-threshold tracking, the comparator will always switch at designed threshold and therefore, the design in inherently resistant to circuit delay. The frequency inaccuracy over temperatures is compensated by adopting 1st order temperature compensated timing resistor. And although the offset of dynamic comparator highlighted in blue will still affect the output frequency, its effect will be negligible when it is much smaller than V_{DD} based on the equations derived in the paper itself.

Another interesting example is shown in Fig. 9. In this design, the anti-jitter technique, which is similar to [48], is adopted for relaxation oscillator phase noise reduction. Referring to the timing diagram when V_+ is charged up and restricting the discussion within very short period of time when noise voltages do not change, V_+ is always charged to a voltage equals to $V_{ref,osc}+\Delta V$, where ΔV denotes the noise voltage added to V_+. Taking an example, when ΔV is positive, V_+ becomes higher than the expected value. This allows a larger

discharging current through M2 and thus, V_- is discharging at a faster rate, causing an earlier crossing with $V_{ref,osc}$. The earlier crossing will reconfigure C_2 connection, pulling V_+ to a voltage of $-(V_{ref,osc}+\Delta V)$, which is lower than the expected value. Since V_+ is then charged up by the constant current source M1, a longer time is necessary for it to return to $V_{ref,osc}+\Delta V$. This longer time compensates the effect of previous earlier crossing on the output, preventing the output to fluctuate and therefore, reducing the output jitter or phase noise and achieving 162 dBc/Hz FOM.

To compensate for the low frequency noise that exists in the comparator and the constant current source charging timing capacitor, respectively, the study in [46] implemented a few compensations. To reduce the comparator flicker noise, which translates to comparator input offset, the proposed comparator offset cancellation helps. To reduce the flicker noise in the current source, theoretical derivation in the paper shows that the mismatch between two timing capacitors will naturally attenuate that noise. Similarly, in another work [47], to reduce flicker noise, chopper is implemented since it is widely proven to be an effective solution to flicker noise.

2.2.3 Relaxation Oscillators with Low Frequency Inaccuracy over Supply and Temperature Variations

Other than output phase noise, the frequency accuracy over supply and temperature variations is another big concern because the oscillation frequency should only depend on the measurand and should not vary with other factors.

Many designs have been proposed to reduce frequency inaccuracy over supply and temperature variations. Existing methods can also be categorized into two groups: (1) Direct circuit block optimization [49] and (2) System level regulation [50] [51] [52] [53].

In [49], to remove the frequency dependency on supply, the oscillation period is designed to be proportional to timing RC constant only. To remove the frequency dependency on temperature, several circuit design techniques had been proposed, namely the resistive temperature compensation, the capacitive temperature compensation, and the comparator gain boosting compensation. The resistive temperature compensation is based on the structure proposed in

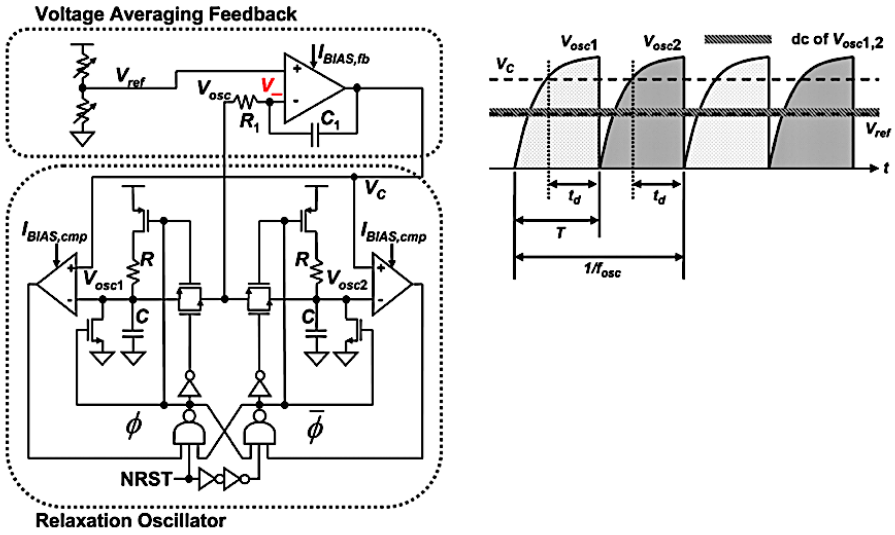

Fig. 10: Relaxation oscillator from [50].

[54], which consists of series connected resistors with opposite temperature coefficient so as to achieve a timing resistor with zero temperature coefficient. The capacitive temperature compensation involves controlling the effective timing capacitance by adding a variable capacitor in parallel with original timing capacitor. The variable capacitor value is adjusted internally by the average of the capacitor voltage such that the capacitance value can compensate the change in original timing capacitor and maintain a constant effective timing capacitance. Meanwhile, since comparator gain, which can also be seen as the comparator propagation delay, reduces at high temperature, a two-stage comparator is proposed to boost comparator gain across the entire targeted temperature range. Although circuit delay variation will also cause frequency inaccuracy, the analysis provided in this work shows that it has negligible impact on the output frequency, and hence no special circuit delay compensation is required for this design. The problem on this type of direct circuit block optimization is that it will largely depend on process variation. Therefore, the system level regulation is more often adopted.

In [50], a voltage averaging feedback (VAF) technique is proposed to continuously adjust the comparator switching threshold voltage based on the integrated value of the timing capacitor voltage. This technique aims to reduce the output frequency variation with supply due to variation in circuit delay. The system architecture and corresponding timing diagram is shown in Fig. 10.

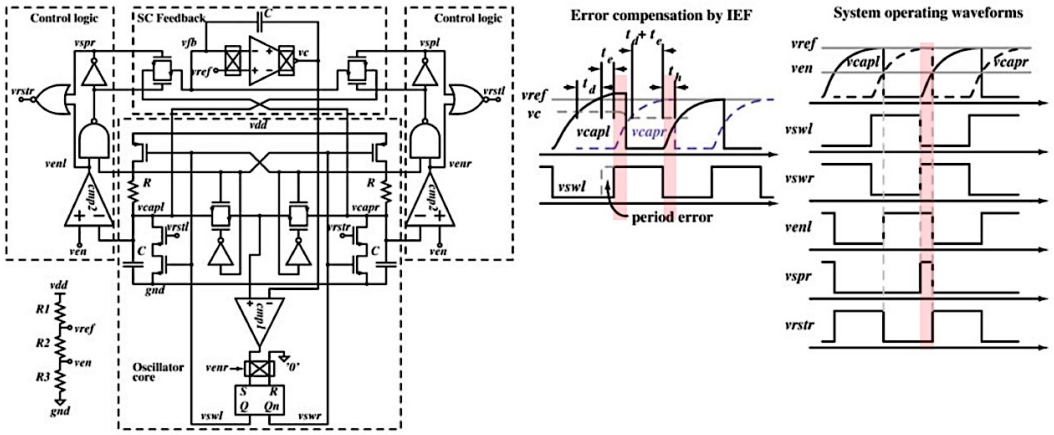

Fig. 11: Relaxation oscillator from [51].

Under nominal condition, the nominal integrator DC output V_C compares with timing capacitor voltage $V_{osc1,2}$, generating nominal output frequency. The output period is the sum of capacitor charging time and the nominal circuit delay t_d. When there is a change in circuit delay t_d due to supply variation, the timing capacitor will continue charging for a longer or shorter period of time after $V_{osc1,2}$ crosses the nominal V_C, resulting in an output period change, i.e. when t_d increases, output period increases. Since the delay change can also be seen as a change in the area under the $V_{osc1,2}$ curve, the integrator will therefore generate a new V_C which allows an earlier or later crossing of $V_{osc1,2}$ with V_C, so as to compensate the initial period change due to t_d. Since the analog integrator works continuously, the output frequency is always being monitored and adjusted in real time. However, as the integration is performed over the entire $V_{osc1,2}$ curve, the power consumption can be large. As a result, a gated integration is proposed in [51].

The system architecture of [51] is illustrated in Fig. 11. Similar to [50], the capacitor voltage is integrated by the SC feedback circuit and the comparator switching threshold is being regulated continuously to compensate the circuit delay that changes with the supply or temperature variation. However, in this design, instead of performing integration over the entire capacitor voltage waveform, the integrated error feedback (IEF) only integrates part of it while achieving similar frequency regulation effect as [50]. Referring to the timing diagram in Fig. 11, the integrator integrates within the gated period of vspr, and hold its input values for new vc generation. However, the gated operation

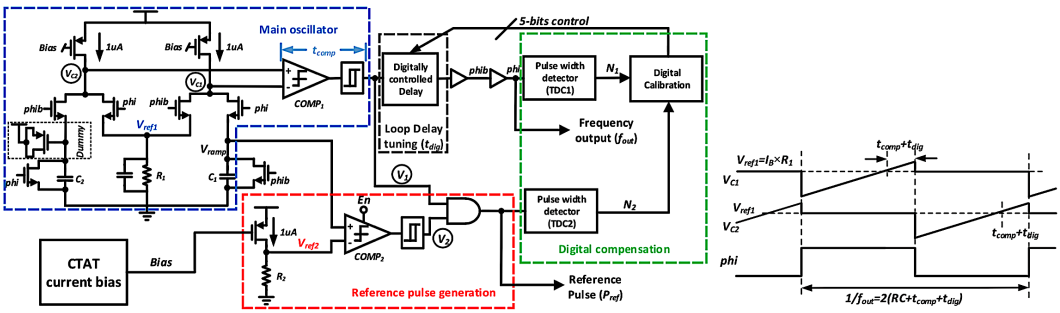

Fig. 12: Relaxation oscillator from [52].

requires integrator with moderate speed and high gain such that the integration can be done within the designed window. This results in amplifier with high power consumption (static current of 20 μA). Also, three comparators are implemented in this design which add up to the power consumption and complicates the layout matching process.

To cut down on the power consumption, instead of using analog integrator as feedback circuit, a digital feedback compensation is proposed in [52] to compensate for circuit delay variation with supply and temperature. The system architecture is shown in Fig. 12. The actual output frequency f_{out} is converted into digital code and compared with an estimated frequency from a constant reference pulse P_{ref} in digital domain. Since the oscillation period is the sum of timing capacitor charging period, comparator delay t_{comp} and designed loop delay t_{dig}, when there is a change in the period due to any of these factors, the digital compensation loop will identify the difference between the actual and estimated frequency, and regulate t_{dig} to resume the nominal frequency. This design effectively reduces the power consumption since the digital compensation block is purely digital and its turn-on occasion can be controlled. Also, it supports process scaling better than analog feedback. However, the drawback is that the feedback resolution is limited by the number of bits implemented and increasing the number of bits brings mismatching problems while decreasing the number of bits worsens the feedback accuracy.

2.3 VCO-based Delta-Sigma Modulator (DSM) for Bio-Signal Recording Interface

When coming to the field of sensing bio-signals, the aforementioned relaxation oscillator-based unified impedance sensing interface may not be adequate. There are two major differences in requirement of these two systems which result in this conclusion: The first difference is in the nature of signal that the system is sensing. Relaxation oscillator-based interfaces are for converting sensor impedance into electrical signal outputs. They are suitable for sensing body's physical properties, such as pressure, temperature, etc., regardless of capacitive or resistive sensors used. DSM based interfaces are able to convert small and noisy body electrical signals, in voltage or current mode, into readable and precise electrical signal outputs. Due to the different nature of signals sensed, different interface architectures shall be chosen. The second difference is the resolution. Due to oversampling and noise shaping, the DSM can theoretically realize higher resolution interface as compared to the relaxation oscillator-based interface. Therefore, for bio-signal sensing interface, the DSM based architecture is studied.

While it is also possible to employ the conventional frontend architecture which consists of an instrumentation amplifier (IA) followed by an analog-to-digital (ADC), the architecture has some limitations. For example, in [17], a chopper-stabilized IA is proposed for neural signal sensing. This frontend achieves low noise floor while operating under with 2-uW power. However, its input range is limited to a few mV, which makes it susceptible to large input artifacts. Also, its signal bandwidth is only up to 100Hz, which is not enough for bio-signals such as slow local field potential (LFP) spanning 1-200 Hz, not mention the even faster action potential (AP) which can go up to a few kHz. With similar IA-ADC architecture, design in [18] doubles the power consumption than design in [17] and boosts the signal bandwidth to 10kHz. However, its input range is still limited to a few mV. In contrast, in [55] [56], both of them employ IA-ADC architecture, achieving 10mV and 28mV input range, respectively. However, their power consumption is both in tens of mW range, pushing up the power budget.

Fig. 13: General VCO-based ADC [57].

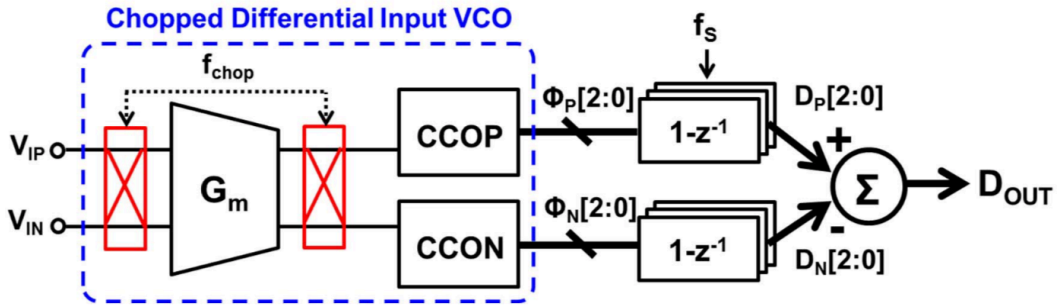

Fig. 14: VCO-based DSM for neuro-recording [32].

The VCO-based DSM as bio-signal recording interface has been a popular topic recently to achieve both large input range and high power efficiency. Many designs with promising results have been proposed. For this application, specifications such as bandwidth, energy efficiency, input signal range and output signal-to-noise-and-distortion-ratio (SNDR) are critical.

In [31], the idea of making use of VCO-based ADC frontend for bio-signal sensing is proposed. Instead of converting the input signal into voltage or current for quantization, the proposed model suggests a voltage-to-phase conversion. The advantage is to increase the dynamic range and input voltage range without causing saturation to the frontend because phase will never saturate. Therefore, artifacts that can be hundreds of milli-volts will not affect normal operation of the interface, making the VCO-based ADC suitable for this application.

The block representation of general VCO-based ADC is shown in Fig. 13. It consists of a VCO which converts the input signal x(t) into output frequency w(t). The phase of w(t) is counted by the counter whose output is sampled by f_s and differentiated to produce y[n] [57]. The design in [32] implements this idea by proposing a VCO-based DSM as neuro-recording frontend. The system architecture is shown in Fig. 14. The frontend G_m cell converts differential inputs V_{IP} and V_{IN} into currents which define two VCOs' output phases Φ_P[2:0] and

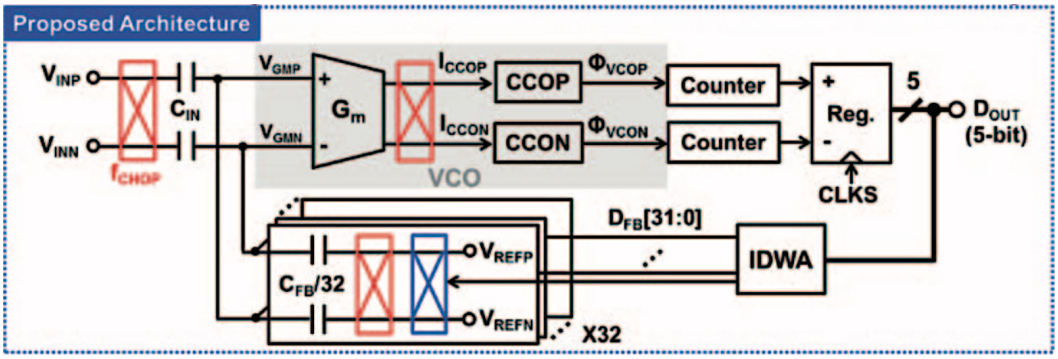

Fig. 15: VCO-based DSM with feedback for neuro-recording [33].

Φ_N[2:0]. The difference in sum of phases from both VCOs is computed by a counter logic and quantized into digital bits output D_{OUT}. Chopping is also implemented in this design for low-frequency noise elimination. The reported results show a moderate SNDR of 61.85 dB and low power consumption of only 17 µW. The reason for this low power is due to the highly digital architecture. The input-referred noise is also minimized by removing the low-frequency noise using choppers. However, this design only achieves a limited input signal range of 8 mV_{pp}.

To improve the input signal range, the design in [33] proposed another architecture with feedback circuit for input signal range enhancement. The architecture is illustrated in Fig. 15. With similar DSM core as the design in [32], a feedback path consisting of a thermal-code-controlled capacitive DAC is added. The thermal code is generated using an IDWA block which minimizes the mismatch among DAC's capacitors. The DAC converts output digital bit stream into corresponding voltage signals to be subtracted from the input signal. As a result, the input signal range is boosted to $\pm$50 mV_{pp} as reported.

Previous examples only implement 1st order VCO-based DSM architecture. In [35], a 2nd order VCO-based DSM is proposed with architecture shown in Fig. 16. The 1st integration is done by CCO+PFD. The CCO converts input voltages into phases, while the PFD cell integrates the differential outputs of CCO, generating a pulse-frequency modulation (PFM) signal which controls the current of second integrator SRO. The SRO outputs are quantized as digital output bitstream. A DAC feedback path is also adopted to increase the input signal range. With this 2nd order architecture, the design achieves 64.2 dB SNDR within a wide bandwidth of 2.5 MHz. However, since this design is not

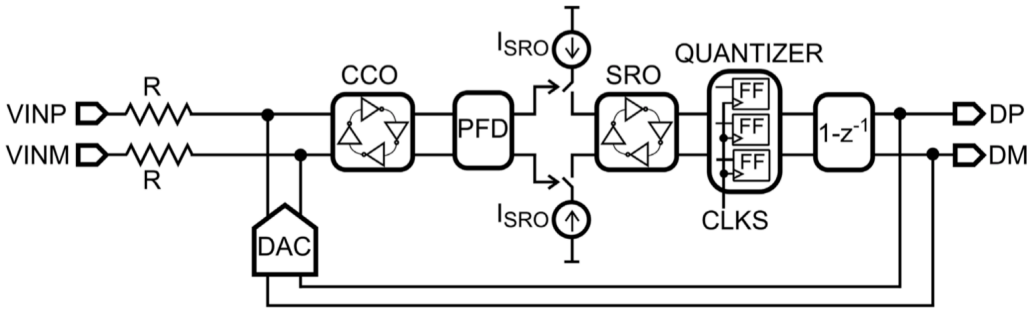

Fig. 16: 2nd order VCO-based DSM [35].

intended for bio-signal sensing, the power consumption is in milli-Watt range and its bandwidth is more than enough for neuro-recording application.

To evaluate the frontend performance, parameters such as input signal range, signal bandwidth, signal-to-noise-distortion ratio (SNDR), FOMs and FOMw are usually used. The input signal range indicates the maximum input signal amplitude that the interface can handle before it becomes saturated, which decides the type of input signal that can be sensed by the interface. The signal bandwidth refers to the passband of the interface, which also decides what kind of signal that can be sensed. The SNDR, which measures the ratio of output signal power to noise-distortion power, evaluates the interface's noise performance which directly relates to the resolution or ENOB of the system. FOMs, which is calculated by FOMs = SNDR + 10log(BW/Power), provides an overall evaluation on trade-off among noise, bandwidth and power. In addition, another commonly used FOM is FOMw. It is calculated by Power/(2BWx2^{ENOB}), which mainly evaluates the system's energy efficiency.

Chapter 3

Relaxation Oscillator with Low Jitter Energy Efficient Swing Boosting

Abstract

This chapter presents a new low-jitter low-power RC relaxation oscillator for biomedical sensor interface application. A novel switch-capacitor based energy efficient swing boosting RC network is proposed to effectively improve the oscillator phase noise and energy efficiency. A low input-referred noise low power inverter-based comparator with replica biasing is employed to enhance the phase noise performance and to reduce output frequency inaccuracy over supply voltage variation. A first-order temperature compensated timing resistor is designed to reduce the output frequency inaccuracy over temperature variations. The prototype relaxation oscillator circuit is designed and fabricated in a commercial 65 nm CMOS process. The measured output frequency is 3 MHz under nominal supply voltage of 1 V, consuming a total power of 17.3 μW. This design achieves an energy efficiency of 5.7 pJ/cycle, and output phase noise of −114 dBc/Hz at 100 kHz offset frequency. The measured relative period jitter is 0.015%. The frequency inaccuracy is ±0.15% over a supply range of 1 V to 1.6 V, and ±0.6% over a temperature range of 0°C to 90°C. The Figure-of-Merit (FOM) is computed to be 161 dBc/Hz, which compares favorably with the benchmark FOM of 162.1 dBc/Hz [42].

Organization of Chapter

This chapter is organized as follows. Section 3.1 provides the background and state the targets to be achieved. Section 3.2 summarizes the existing techniques and the corresponding problems. Section 3.3 evaluates the architectures of conventional relaxation oscillator design and the existing swing

boosting relaxation oscillator design. Section 3.4 presents the proposed design in detail, providing the theories behind the design and also highlights the enhancement made to previous designs in attaining our targets. Section 3.5 presents and discusses the measurement results of the proposed design. Finally, summary of the work detailed in the chapter is given in Section 3.6.

3.1 Introduction

The relaxation oscillator has been a popular topic for System-On-Chip (SoC) in recent years. While it can be implemented as an on-chip clock/timing signal generator [58] [59], it can also be used as the frontend of wearable biomedical sensor readout circuit [60]. Theoretically, the relaxation oscillator frequency is directly proportional to its timing RC constant. Therefore, it provides a direct conversion from sensor's resistance or capacitance value to frequency for easy digitization [60]. Relaxation oscillator has unique advantages of good frequency linearity, wide frequency tuning range and low power consumption. However, the major drawbacks of a relaxation oscillator is its limited jitter and phase noise performances [45]. In sensor interface application, the oscillator jitter will translate to limited sensing resolution. Therefore, improving the jitter or the phase noise performance is the key concern when deploying relaxation oscillator in high resolution time-domain sensor interface. On the other hand, a low power circuit reduces the frequency of battery charging and/or the battery size, which supports the implementation of miniaturized biomedical devices. Furthermore, the interface output should solely be depending on the variation of the sensing parameters. Impact from external factors such as supply voltage and temperature changes on the output should be minimized for ultimate sensing accuracy.

Therefore, the relaxation oscillator design challenges in this work can be summarized as follows:

1) Low output phase noise, or low output jitter, which is essential for high precision conversion.
2) High energy efficiency, which is desirable for miniaturized biomedical device application.

3) Low frequency inaccuracy over supply and temperature variations to ensure the oscillator output frequency stability over these two external factors.

3.2 Concerns on Existing Designs

Many relaxation oscillators had been reported to meet design challenges mentioned in previous section. To improve the oscillator output phase noise performance, a voltage swing boosting technique is proposed in [42]. However, as explained in later part of this chapter, this technique consumes additional power due to the nature of its architecture, which is not desirable for low power applications. The circuit with anti-jitter technique [45] introduced before also achieves excellent phase noise performance. However, redundant circuit blocks increase power consumption. Another innovation in reducing phase noise is the self-chopping technique as proposed in [61], which employs the oscillator output as the chopping signal to suppress the comparator noise. This technique is suitable for kilo-Hz designs, but for mega-Hz and higher frequency, a frequency divider is required to generate a suitable chopping frequency from the high frequency output, which consumes additional power.

Meanwhile, both supply voltage and temperature variations alter circuit delay, which will in turn affect the output frequency. Compensation techniques include voltage averaging feedback (VAF) [50] and integrated error feedback (IEF) [51] as introduced in previous section. This kind of feedback method effectively reduces the frequency variations with supply and temperature changes. In addition, temperature variation also causes parameter variations in components such as the RC value, switching matrix, comparator offset and comparator delay [62], resulting in frequency inaccuracy with temperature. To compensate this, temperature insensitive MIM capacitor together with temperature compensated resistor are implemented in [42] [52] [61]. Design in [62] further proposed an optimized switch matrix and comparator offset cancellation with constant bandwidth comparator to effectively remove the temperature dependent factors from output frequency. To compensate for the even higher order temperature dependency of the timing resistor, the voltage

ratio adjusting (VRA) technique has been proposed in [63] by tuning the ratio of resistors with different temperature coefficients. Other than optimizing the temperature dependency of the RC network to reduce frequency inaccuracy with temperature, system level compensation such as digital compensation [52] and dynamic frequency-error compensation [64] are proposed to improve the overall frequency stability.

Although previous works have demonstrated capabilities in tackling the aforementioned challenges, a gap remains between the high energy efficiency and low phase noise output. Designs with excellent phase noise performance such as [45] [42] suffer from large power consumption, while designs with extremely high energy efficiency such as [65] [66] [67] demonstrate limited phase noise performance. To bridge this gap, new design techniques that can attain both low phase noise and high energy efficiency are researched in this chapter.

3.3 Architectures of Conventional Design and Swing-Boosted Design

3.3.1 Conventional Design

Two commonly seen architectures of the relaxation oscillator with their timing waveforms are shown in Fig. 17(a) and (b). The major difference between these two architectures is the constant current source. Architecture in Fig. 17(a) employs a constant current source and timing capacitors (I-C) as the oscillator's timing network, while architecture in Fig. 17(b) uses passive resistor and capacitors (R-C). Otherwise both architectures are similar, which consist of two comparators and one SR latch.

The basic operation of the architecture of Fig. 17(a) has been described in Chapter 2, and similar operation applies to the architecture in Fig. 17(b) except that the capacitor discharging time now depends on the RC time constant

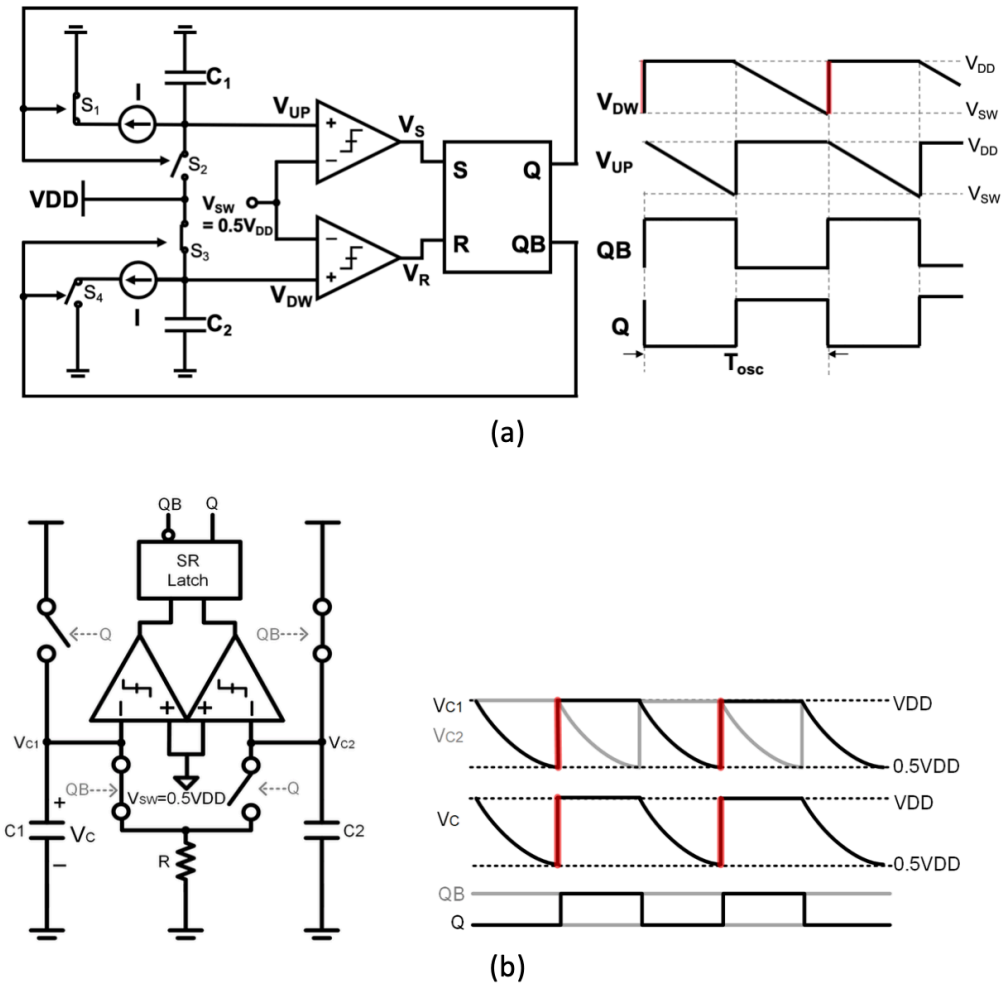

Fig. 17: Conventional relaxation oscillator with (a) I-C architecture; (b) R-C architecture.

instead of a constant current I. The advantage of I-C architecture is that the outputs are inherently resistant to amplitude noise due to its rail-to-rail nature, and the output frequency is linearly proportional to and can be directly controlled by the constant current.

However, the constant current source is susceptible to aging, causing the oscillation frequency to change over time. Also, since this current source is usually implemented using a single CMOS transistor whose drain is directly connected to the timing capacitor discharging node, i.e. V_{UP} and V_{DW} in Fig. 17(a), during the capacitor discharging process, the drain voltage drifts significantly, causing a shift in the transistor operating region which then alters the current value.

Meanwhile, in [68], the author has compared the current noise power

associated with a single passive resistor and a MOSFET transistor, and has proven that current noise power generated by a resistor is less as compared to by a MOSFET transistor in saturation region, assuming the bias voltage and current are the same for both cases. It also proved that in order to have lower current noise power than having the passive resistor, the MOSFET transistor should satisfy two conditions at the same time: (1) the transistor should operate in weak inversion region and, (2) when the bias voltage across the resistor is less than 2kT/q (= 52 mV). While condition (1) is easy to realize in actual design, condition (2) is less practical because a bias voltage across a resistor in actual circuit is equivalent to the capacitor voltage as illustrated by V_{C1} or V_{C2} in Fig. 17(b), which should at least attain the comparator switching threshold. By having the bias voltage across the resistor less than 52 mV and assuming the comparator switching threshold is half of its supply V_{DD}, supply V_{DD} of the comparator is estimated to be less than 104 mV. This ultra-low V_{DD} will complicate the comparator design and worsen the comparator input-referred noise.

Previous studies such as [69] [70] have also proven that the phase noise is inversely proportional to the capacitor voltage slope at the comparator crossing and is directly proportional to the noise source in series with timing capacitor, i.e.

$$\sigma_{\Delta t}^2 \propto \frac{\sigma_{\Delta V_C}^2}{\left(\frac{dV_C}{dt}\right)^2} \quad (4)$$

where $\sigma_{\Delta t}^2$ is variance of the oscillation period error, $\sigma_{\Delta t}^2\sigma_{\Delta V_C}^2$ is variance of the error voltage ΔV_C on the timing capacitor C, and dV_C/dt is the slope of capacitor voltage V_C when V_C crosses the comparator threshold. Therefore, a low $\sigma_{\Delta t}^2$, which translates to a low RMS jitter or low phase noise, can be achieved by decreasing $\sigma_{\Delta V_C}^2$ and increasing dV_C/dt. For better phase noise performance, the conventional design in Fig. 5(a) has to implement a larger constant current for discharging which increases the circuit power consumption.

Due to many demerits of the I-C architecture, we adopt the R-C architecture instead of the I-C for all designs discussed in this thesis.

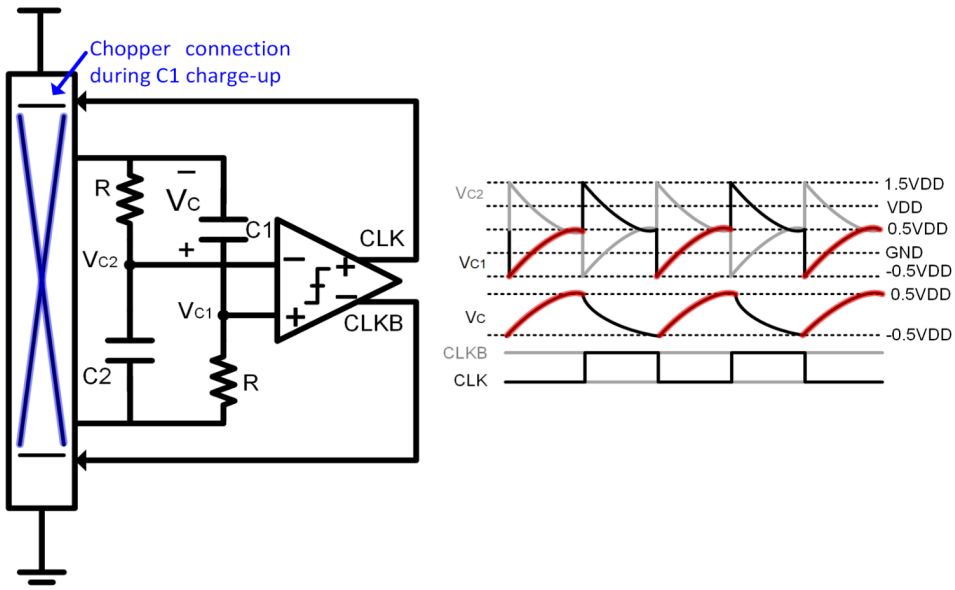

Fig. 18: Swing-boosted relaxation oscillator [42].

3.3.2 Swing-Boosted Design

Swing boosting techniques have been proposed in many designs such as [42] [44] [71].The key idea behind these techniques is to boost the capacitor voltage swing within a given period of time such that the capacitor voltage slope is increased and phase noise is reduced, which are all based on Eq. (4). An example of a swing boosting design [42] together with its waveforms is illustrated in Fig. 18. Although it achieves excellent phase noise performance and the benchmarked FOM value, its power consumption is large. The calculated energy efficiency for this design is as high as 20.9 pJ/cycle, with 70% of its total power of 219.8 μW consumed by its RC block. This shows that the key challenge in reducing the overall power consumption resides in the RC block. By reducing the power consumption of the RC block, the overall energy efficiency can be improved. Hence, the energy efficiency of the RC block is first to be analyzed here.

To evaluate the energy efficiency, a parameter called the energy per cycle E_{Cycle}, is widely adopted in many works such as [59] [62] [64] [44]. It is a normalized value of the total power drawn from the power supply by the oscillator to the oscillation frequency (or the capacitor charging frequency), which ensures that oscillators with different frequencies can be compared fairly.

It represents the energy drawn from the power supply for each oscillation cycle to happen, which demonstrates the oscillator's energy efficiency. E_{Cycle} can be expressed as

$$E_{Cycle} = \frac{\text{Energy}}{\text{No. of cycles}} = \frac{P_{avg}}{f_{osc}} \quad (5)$$

where P_{avg} is oscillator average power consumption, and f_{osc} is the oscillation frequency.

Referring to the general RC block as shown in Fig. 17(b), the energy drawn from the power supply in one oscillation cycle is calculated as twice the product of current drawn from the supply and the supply voltage, integrating over the capacitor charging period. The multiplier of two is because within one oscillation cycle, there are two capacitor charging events. To charge up the RC block, the current drawn from power supply is

$$i(t) = C\frac{dv_c(t)}{dt} = \frac{V_0}{R}\exp\left(\frac{-t}{RC}\right) \quad (6)$$

where C is the timing capacitor, $v_c(t)$ is the capacitor voltage, V_0 equals V_{DD} which is the capacitor final voltage after charging, and R is the resistance in the charging path.

Therefore, the total energy *E* drawn from power supply per oscillation cycle can be expressed as

$$E = 2\int_0^{\tau} i(t)\cdot V_{DD}\,dt = 2\int_0^{\tau}\frac{V_0}{R}\exp\left(\frac{-t}{RC}\right)\cdot V_{DD}\,dt = 2C\Delta V_C\cdot V_{DD} = 2\Delta Q\cdot V_{DD} \quad (7)$$

where τ is the charging period, ΔV_C is the difference in capacitor voltage before and after the charging event, and ΔQ is the total amount of charges drawn from power supply by the capacitor in each charging event.

As a result, Eq. (5) can be re-written as

$$E_{Cycle} = \frac{\text{Energy}}{\text{No. of cycles}} = \frac{P_{avg}}{f_{osc}} = \frac{E}{1} = 2C\Delta V_C\cdot V_{DD} = 2\Delta Q\cdot V_{DD} \quad (8)$$

This shows that higher energy efficiency can be achieved by having smaller ΔQ, which requires innovation in circuit architecture, or by having lower supply V_{DD}. However, by simply reducing V_{DD}, that may require transistors in the

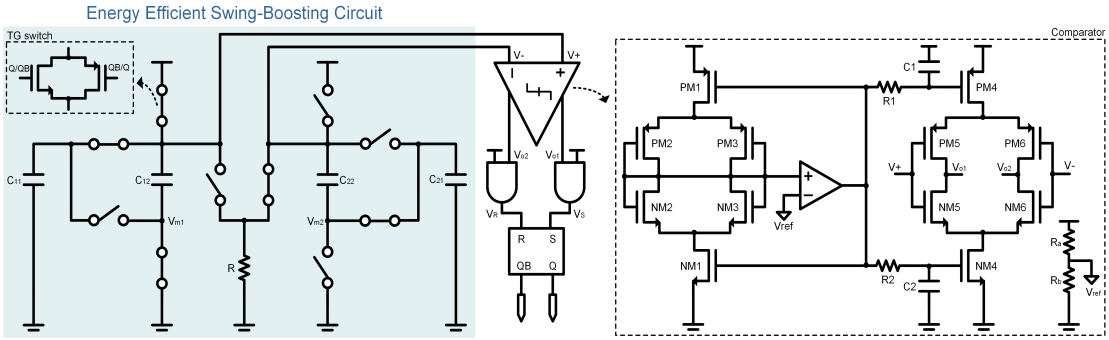

Fig. 19: System block diagram of the proposed swing boosting relaxation oscillator [76].

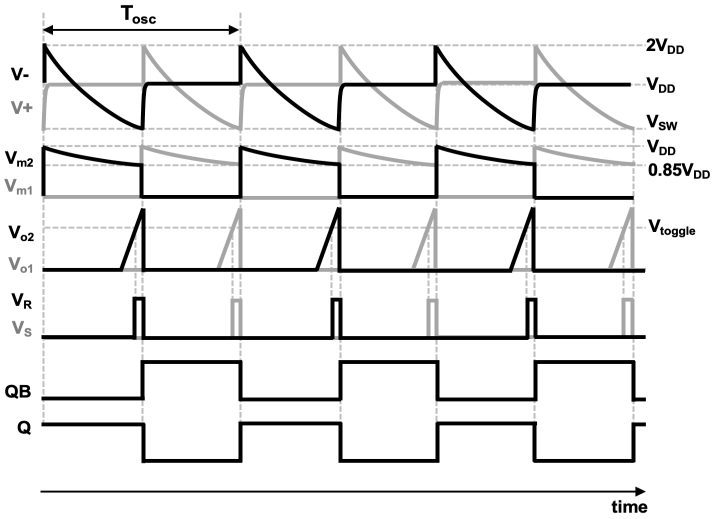

Fig. 20: Timing diagram of the proposed oscillator [76].

comparator to work in subthreshold region. This reduces the comparator's transconductance gm which can worsen its input-referred noise. While it is possible to use a separated VDD for comparator, multiple supply generation requires additional power. Therefore, new RC block architecture is necessary for energy efficiency improvement.

3.4 The Proposed RC Relaxation Oscillator Architecture

In this chapter, a novel on-chip relaxation oscillator is proposed. The phase noise performance and energy efficiency are improved via the switch-capacitor swing boosting technique, while the frequency variation with supply and temperature is reduced by employing the inverter-based comparator with replica biasing and 1st order resistive temperature compensation technique.

To improve the performance of the classic design, a new RC relaxation

oscillator is proposed. The architecture of proposed RC relaxation oscillator and timing diagram are shown in Fig. 19 and Fig. 20, respectively. The proposed design consists of a novel energy efficient swing boosting RC circuit, an inverter-based comparator with replica bias, a SR latch and some logic buffers.

The basic operation of the proposed design is described as follows. Setting the initial state of $V_-=V_{DD}$ and $V_+=GND$, the inverter-based comparator and logic gates give $V_S=V_{DD}$ and $V_R=GND$, which triggers the SR latch to output $Q=V_{DD}$ and QB=GND. These two complimentary signals set the switch matrix of the RC charging/discharging block to that shown in Fig. 19. With this switch configuration, capacitor C_{11} and C_{12} are connected in parallel for charging, pushing V_+ to V_{DD}, while capacitor C_{21} and C_{22} are stacked together in series, pushing V_- to $2V_{DD}$ as C_{21} and C_{22} are both charged to V_{DD} before stacking. The stacked C_{21} and C_{22} are then discharged immediately via resistor R toward the ground, pulling V_- down from $2V_{DD}$.

When V_- drops to the comparator switching point V_{SW}, comparator output V_{o2} starts to increase. Therefore, V_R is set to V_{DD} while V_S is kept at GND as $V_+=V_{DD}$. As a result, the SR latch toggles its outputs Q and QB. The new states of Q and QB reconfigure the switch matrix in RC charging/discharging block, stacking C_{11} and C_{12} together while re-charging the paralleled C_{21} and C_{22} to V_{DD}. The waveforms of V_{m1} and V_{m2} are also shown in Fig. 20 to assist the calculation of capacitor voltage changes. The whole process iterates, resulting in a 50%-duty-cycle square wave outputs at Q and QB with a theoretical oscillation period of

$$T_{osc}=2RC\ln\left(\frac{2V_{DD}}{V_{SW}}\right)=2RC\ln(4) \quad (9)$$

where $C=(C_{11}C_{12})/(C_{11}+C_{12})=(C_{21}C_{22})/(C_{21}+C_{22})$. As the comparator is inverter-based, V_{SW} is designed to be $0.5V_{DD}$ by selecting proper aspect ratio for input transistors. Therefore, the period is theoretically independent of V_{DD}. However, since comparator delay, offset and logic stage delay are still supply-dependent, with the comparator delay being the dominant factor based on

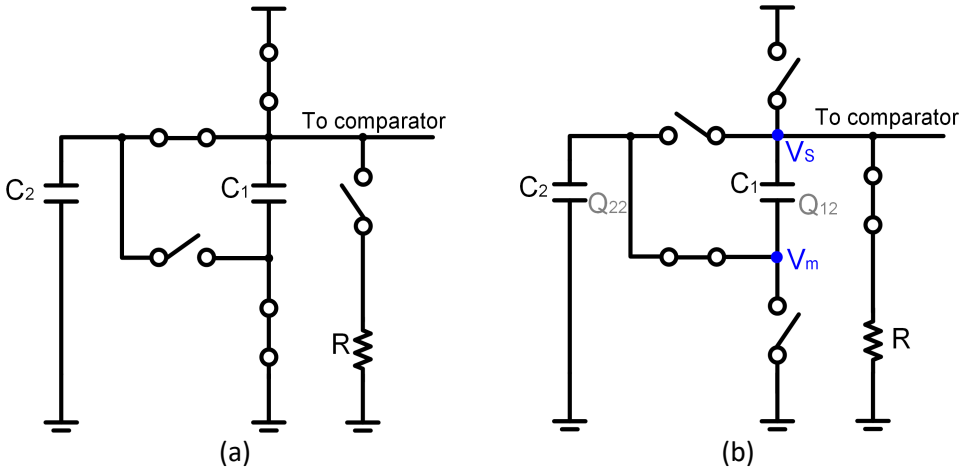

Fig. 21: The proposed switched capacitor RC network configuration during (a) charging and (b) discharging. [76]

simulation. To compensate this, relatively large comparator current is chosen for the comparator to minimize the delay effect on T_{osc}. Other than supply, temperature variation alters the resistance R, resulting in frequency inaccuracy too. This is compensated by adopting 1st order resistive temperature compensation. The proposed architecture has the following advantages. The stacked capacitors boost the voltage swing and increase the waveform slope at V_+ and V_- for a better phase noise performance, while at the same time increase the RC block energy efficiency by drawing less charges for each oscillation cycle. The inverter-based comparator with replica bias employing current reuse technique realizes large transconductance gm and thus smaller input-referred noise. The replica bias also enhances the frequency stability over supply variations by regulating the comparator switching threshold to always be $0.5V_{DD}$. More details will be provided in circuit implementation section.

3.5 Circuit Implementations

3.5.1 Energy Efficient Swing Boosting RC block

An energy efficient swing boosting RC network is proposed, and as shown in Fig. 19, with its simplified half circuit given in Fig. 21. During the charging phase (see Fig. 21(a)), both capacitors C_1 and C_2 are charged to V_{DD} and the total charging capacitance $C_P=C_1+C_2$. During the discharge phase shown in Fig. 21(b), the total capacitance $C_s=(C_1C_2)/(C_1+C_2)$. V_s is $2V_{DD}$ at the start of

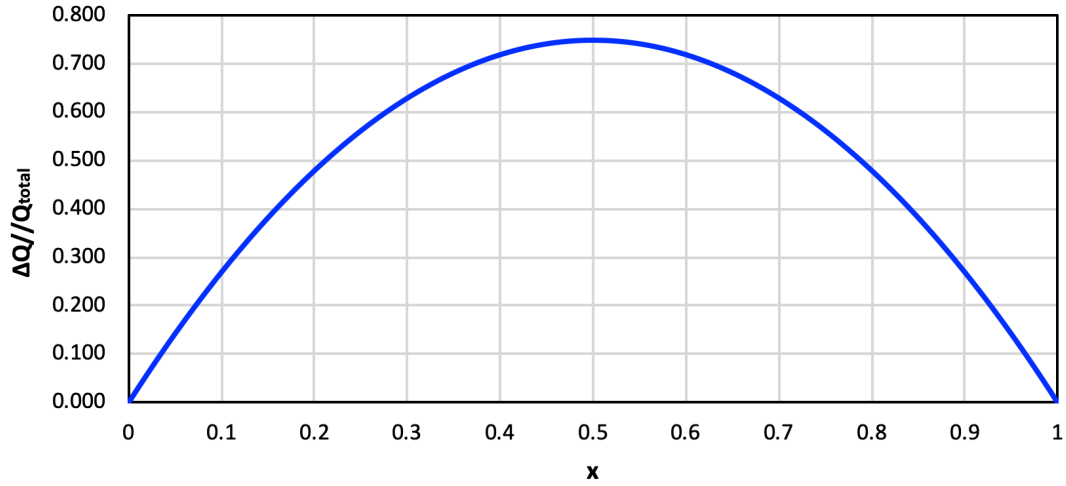

Fig. 22: The relation between capacitor ratio x and $\Delta Q/Q_{total}$. [76]

discharge phase because of the stacking capacitors. C_s discharges via resistor R pushing V_s down to comparator's switching threshold V_{SW} at the end of the discharging phase.

The charge stored in each capacitor at the start of a charge phase is written as

$$\begin{cases} Q_{22}=V_m C_2 \\ Q_{12}=(V_s-V_m)C_1 \end{cases} \quad (10)$$

where V_s and V_m are the capacitor terminal voltages at the end of the previous discharge phase shown in Fig. 21(b). Since discharging stops when V_s reaches comparator V_{SW}, $V_s=0.5V_{DD}$ is obtained at the end of discharging. Solving Eq. (10) for three possible scenarios where $C_2>C_1$, $C_1>C_2$ and $C_1=C_2$, a unified solution is obtained as

$$V_m=\frac{(C_2-C_1)V_{DD}+(C_1)V_s}{C_1+C_2}=(1.5x-0.5)V_{DD} \quad (11)$$

where $x=C_2/(C_1+C_2)$, which is the ratio of C_2 to the total charging capacitance (C_1+C_2).

Without considering the parasitic capacitance, the total amount of charges drawn by C_1 and C_2 after the completion of one charging event is therefore derived as

$$\begin{aligned}\Delta Q &= C_1[V_{DD}-(V_s-V_m)]+C_2(V_{DD}-V_m)\\ &=\left(3x-3x^2\right)CV_{DD}\\ &=\left(3x-3x^2\right)Q_{total}\end{aligned} \quad (12)$$

where $C=C_1+C_2$ and is the total capacitance in the charging cycle, and Q_{total} represents the maximum amount of charges that C can hold when fully charged to V_{DD}. Noted that Q_{total} is a constant once CV_{DD} is selected. Fig. 22 shows the plot of Eq. (12). The quadratic curve suggests that the lowest ΔQ, and thus the lowest energy per cycle, occurs when x value is at its two extreme points. However, these two cases are not practical for circuit implementation since when x=0 or 1, there is in fact only one capacitor and the corresponding energy per cycle will be the same as the conventional architecture in Fig. 17(b). Moreover, simulations show that when x approaches these two extreme points, the parasitic capacitance from the comparator input transistors and the passive resistor R becomes more significant, affecting the oscillation frequency. Therefore, x=0.9 is chosen in the proposed design as the result of energy efficiency optimization. The corresponding $\Delta Q=0.27CV_{DD}$.

Referring to the conventional RC relaxation oscillator shown in Fig. 17(b), with the waveform for half circuit during charging event highlighted in red, the charges drawn per charging event is $\Delta Q=0.5C_1V_{DD}$. Similarly, referring to previous swing boosted relaxation oscillator in Fig. 18 [42], it is derived that $\Delta Q=C_1V_{DD}$. By using Eq. (8), the E_{Cycle} of relaxation oscillators can be computed. Comparing to both, assuming the same capacitor for charging and same V_{DD}, the theoretical E_{Cycle} of the proposed design is only 27% and 54% of what the swing-boosted relaxation oscillator in [42] and the conventional RC relaxation oscillator consume, respectively. This demonstrates a significant improvement in energy efficiency.

On the other hand, the proposed RC block also contribute to lower output phase noise. Based on Eq. (4), a low $\sigma^2_{\Delta t}$, which translates to a low RMS jitter or low output phase noise, can be achieved by decreasing $\sigma^2_{\Delta V_C}$ and increasing dV_C/dt.

The $\sigma^2_{\Delta V_C}$ of the proposed oscillator can be derived as

$$\sigma^2_{\Delta V_C} = \int_{-\infty}^{\infty} S_{\Delta V_C}(f)\,df = \int_{-\infty}^{\infty} \frac{S_{v_n}}{1+(2\pi fRC)^2}\,df \quad (13)$$

where $S_{\Delta V_C}(f)$ is the power spectral density associated with error voltage ΔV_C, which is the product of discharging time constant RC, and the power spectral density S_{v_n} of noise sources appearing at terminals of discharging capacitor C. The result derived from Eq. (13) is similar to the that of conventional design shown in Fig. 17(b) since both designs employs the RC structure. Therefore, the proposed design does not sacrifice $\sigma^2_{\Delta V_C}$ for high energy efficiency.

However, the proposed design demonstrates a larger dV_C/dt as compared to the conventional. The expression of dV_C/dt for the propose design is derived as

$$\left|\frac{dV_C}{dt}\right| = V_{DD}\frac{\ln\left(\frac{2V_{DD}}{V_{SW}}\right)}{T_{osc}} = \frac{V_{DD}}{2RC} = V_{DD}\frac{\ln 4}{T_{osc}} \quad (14)$$

With the same V_{DD} and oscillation period T_{osc}, the conventional design can only achieve dV_C/dt of $V_{DD}(\ln 2/T_{osc})$, which is 2× less than Eq. (14). This is because dV_C/dt is proportional to the maximum capacitor voltage swing, which is $2V_{DD}$ in the proposed design but V_{DD} in the conventional design. This theoretically proves the ability of the proposed RC block in reducing the output phase noise.

The above discussion shows that comparing to the conventional RC oscillator or the reported swing boosted architectures, the proposed design consumes less energy per cycle, while at the same time, achieves better noise performance. These account for the higher energy efficiency and better FOM of the proposed design.

In addition, to compensate the output frequency inaccuracy due to temperature dependent timing resistor, both HR-poly and N+ diffusion resistors are used. Based on simulation, the resistance variation of HR-poly resistor and N+ diffusion resistor is -0.037%/°C and 0.123%/°C, respectively, for temperature range of –45°C to 125°C. The resistive temperature compensation is achieved by combining them in series to minimize the 1st order temperature dependent term in the combined resistor.

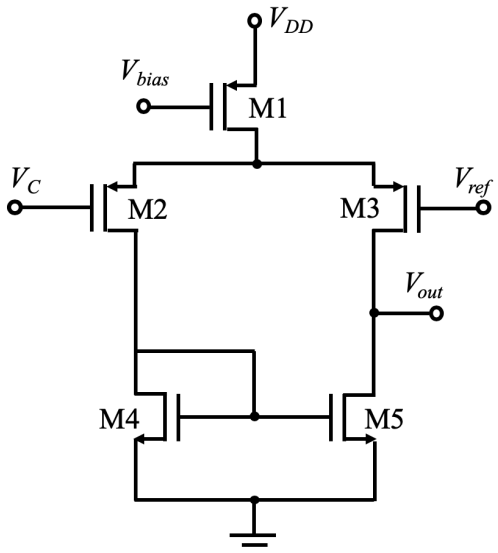

Fig. 23: Classic differential input single output comparator.

3.5.2 The Inverter-based Comparator with Replica Bias

Instead of employing the conventional differential-pair comparator, an inverter-based comparator with replica biasing, similar to [42], is adopted in this design as shown in Fig. 19. It consists of a replica biasing circuitry and an inverter-based comparator core.

The comparator core benefits from its inverter-based current reuse input pairs which increase the comparator transconductance gm_{comp} at switching point. Referring to Fig. 19, the comparator gm_{comp} is approximated to $gm_{PM5} + gm_{NM5} = gm_{PM6} + gm_{NM6}$, where gm_{PM5}, gm_{NM5}, gm_{PM6}, gm_{NM6} are the transconductance of PM5, NM5, PM6, NM6, respectively. Since the bias current is the same for all input transistors, assuming $V_{thp} = V_{thn}$ and NMOS-PMOS inverter pair is properly sized, the comparator gm_{comp} can be approximated to $2gm$, where $gm=gm_{PM5}=gm_{NM5}=gm_{PM6}=gm_{NM6}$. As compared to the classic differential comparator shown in Fig. 23, assuming the same bias current for input transistor and same input transistor size, i.e. M2 in Fig. 23 is identical to PM5 in Fig. 19, the inverter-based comparator gm_{comp} is twice as compared to the classic's. This larger gm suppressed the comparator input-referred noise floor, which translates to lower S_{v_n} in Eq. (13) and thus, lower phase noise.

In addition, as the comparator core is inverter-based, it only turns on when

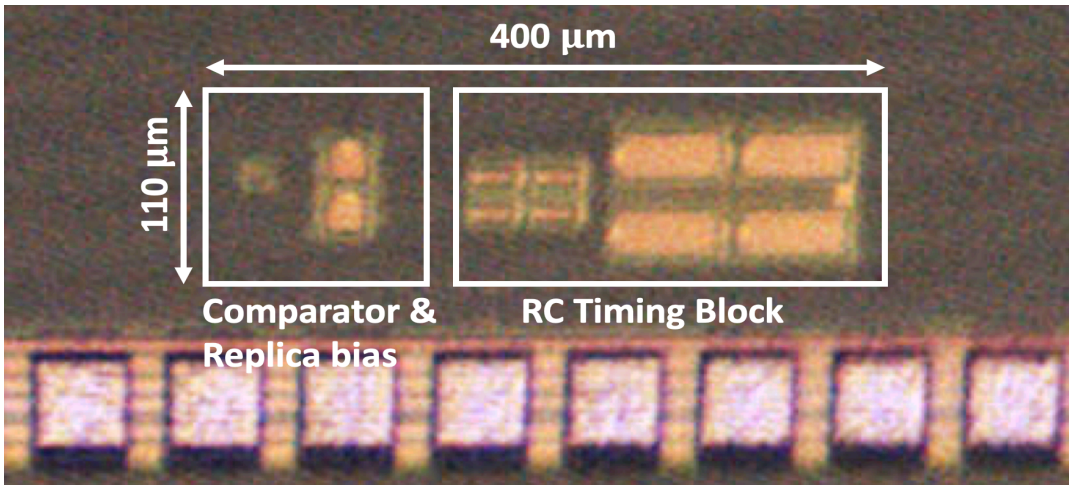

Fig. 24: Chip photo and circuit dimensions.

the input is near the comparator switching point. Therefore, the static power consumption is minimized which better supports the low power operation. The nominal comparator bias current is optimized to make comparator delay negligible as compared to the oscillation period. Under nominal conditions for this design, the simulated comparator delay is only 2% of the oscillation period, which ensures that the oscillation period mainly depends on RC constant and capacitor voltage swing.

The comparator core is biased by its replica circuit as shown in Fig. 19. The replica circuit formed by PM1-PM3 and NM1-NM3 provides a predicted comparator's switching threshold to the amplifier. The amplifier generates an output voltage which controls comparator biasing current and replica circuit current, such that the comparator switches at the designed switching threshold. Any deviation of predicted comparator switching threshold from V_{ref} will cause a change in amplifier output voltage, and thus both currents in replica circuit and comparator, until both voltages are equal. Based on Eq. (9), the oscillation period only depends on the ratio of $\frac{2V_{DD}}{V_{SW}}$. Therefore, V_{ref} is obtained from a resistor divider and is designed to be a ratio of V_{DD}, i.e. $0.5V_{DD}$.

3.6 Measurement Results and Analysis

The proposed design has been implemented in a standard 65-nm CMOS process. The chip photo is shown in Fig. 24, the total active chip area is 0.044

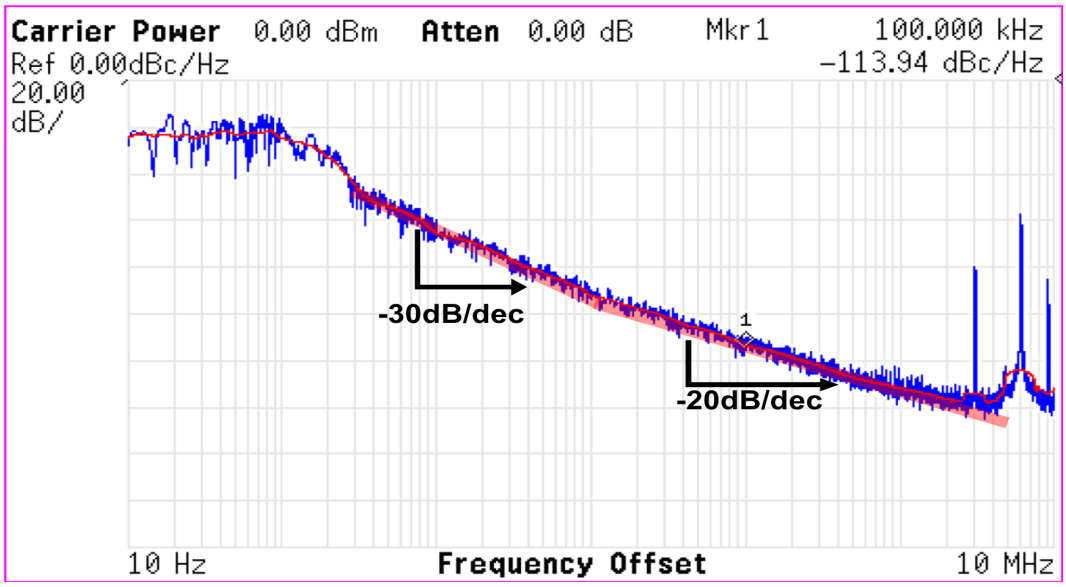

Fig. 25: Measured oscillator output phase noise.

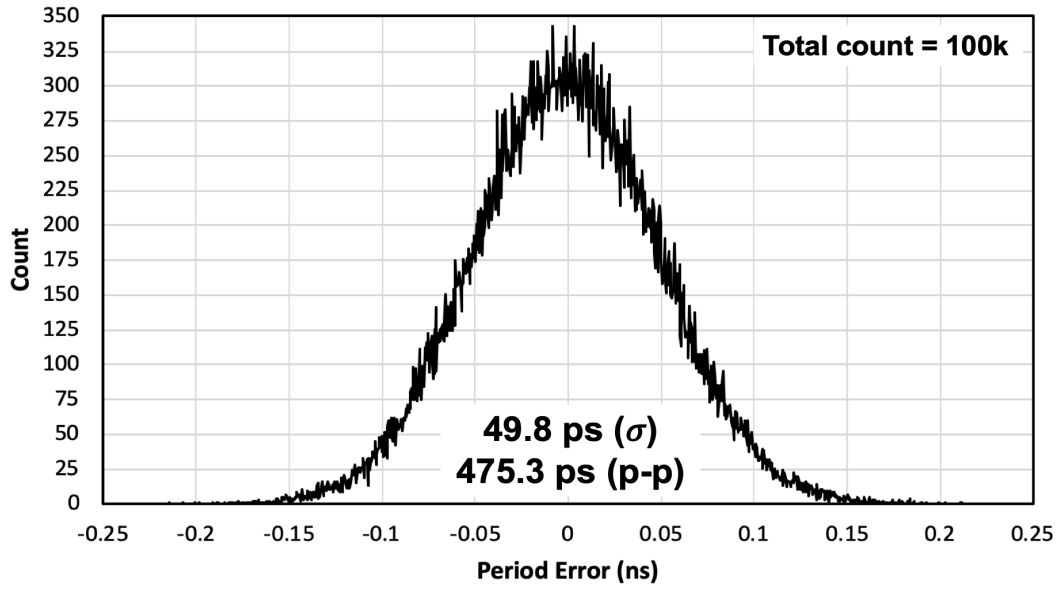

Fig. 26: Measured oscillator output period jitter.

mm^2. The measured oscillation frequency is 3.0 MHz with 17.3 μW power consumption under 1 V supply. The circuit power breakdown shows that the RC network consumed 49% of the total power, the compactor consumes 44% and the logics consumes 7%. The circuit energy efficiency is 5.7 pJ/cycle.

The oscillator startup time is approximately 3.8 μs, equivalent to 12 clock cycles. The oscillator phase noise plot is shown in Fig. 25. The measured phase noise is -113.94 dBc/Hz at 100 kHz frequency offset. The low phase noise is largely contributed by the proposed switch capacitor swing boosting circuit and the low noise inverter-based comparator. Fig. 26 shows the measured statistical

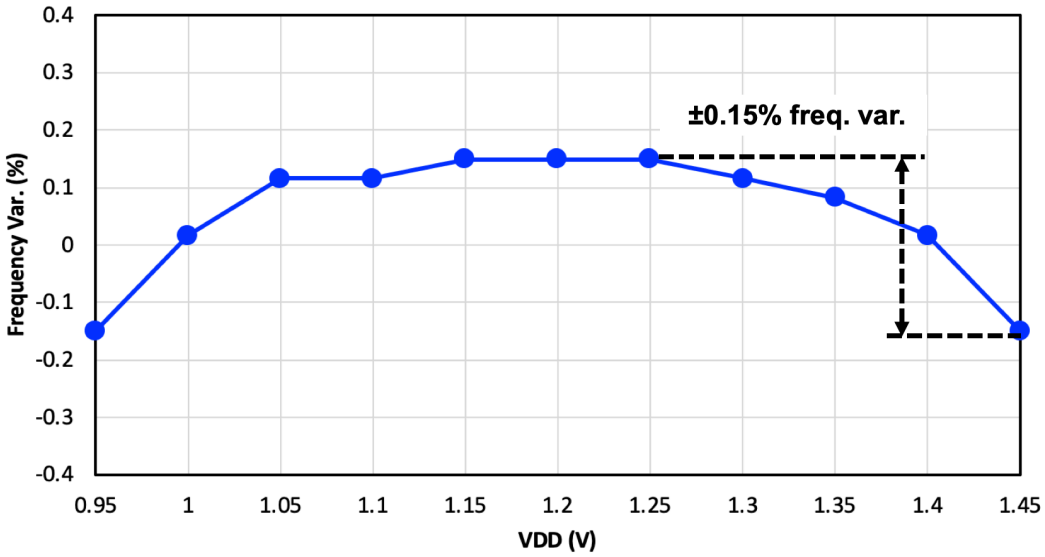

Fig. 27: Measured frequency variation over supply voltage.

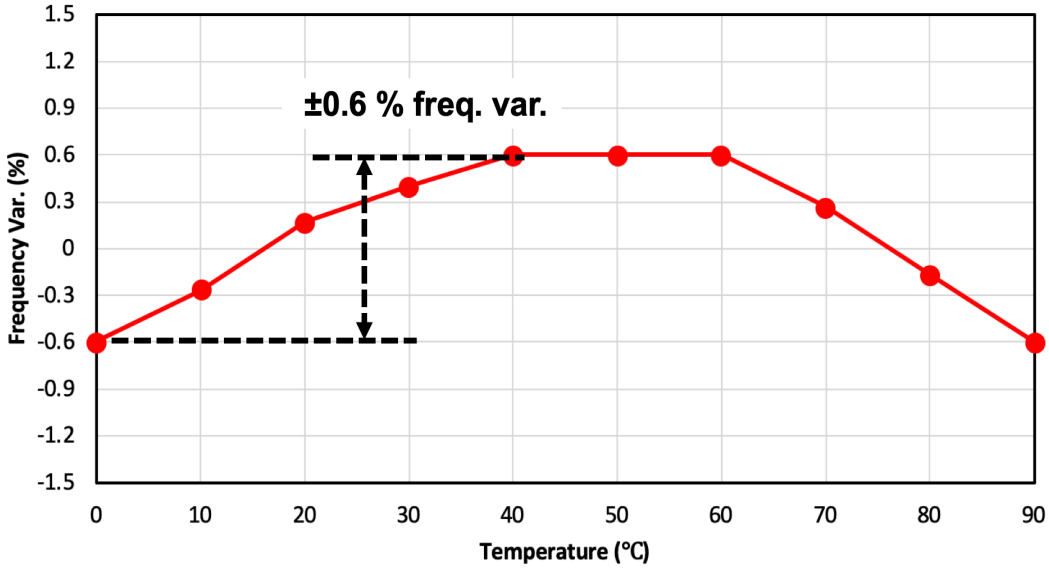

Fig. 28: Measured frequency variation over temperature.

distribution of the oscillation period over 100k counts. The RMS (1σ) period jitter is 49.8 ps, which translates to 0.015% relative period jitter. The peak-to-peak period variation is 475.3 ps. The measurement results also show that all counts fall within 3σ region, showing a centralized period distribution.

Fig. 27 and Fig. 28 show the measured frequency stability over supply and temperature variations. At room temperature of 25°C, the frequency variation with V_{DD} is ±0.15% over 0.95 V to 1.45 V, which corresponds to ±0.3%/V. At a nominal supply voltage of 1 V, the frequency variation with temperature is ±0.6% over 0°C to 90°C. The oscillator frequency is less sensitive to the supply

Table 1: Comparison Table for 1st Design

Year	Tech. (nm)	Freq. (MHz)	Power (µW)	E_{cycle} (pJ/cycle)	Supply (V)	Phase noise (dBc/Hz)	FOM (dBc/Hz)	Period jitter (%)	Freq. Var. with V_{DD} (%)	Freq. Var. with Temp. (%)	Start-up (cycles)
This work	**65**	**3**	**17.3**	**5.7**	**1**	**-114 @100kHz**	**161 @100kHz**	**0.015**	**±0.15 0.95 – 1.45V**	**± 0.6 0 – 90 °C**	**12**
2010 [47]	65	6	100	16.7	1.25	N.A.	137.6 @10kHz	0.05	± 0.26 1.15 - 1.35V	± 0.2 -40 – 125 °C	N.A.
2013 [51]	65	12.6	98.4	7.8	1.2	-100 @100kHz	152.6 @100kHz	N.A.	± 0.07 1.1 - 1.5V	± 0.82 0 – 80 °C	N.A.
2015 [65]	65	26	17.8	0.7	0.35	-104.1 @1MHz	149.9 @1MHz	N.A.	N.A.	N.A.	N.A.
2016 [42]	180	10.5	219.8	20.9	1.4	-115.1 @100kHz	162.1 @100kHz	0.01	± 0.264[e] 1.4 - 2V	± 1.13[a] -40 –125 °C	N.A.
2017 [66]	90	51.3	18	0.4	0.8	-83.3 @1MHz	N.A.	0.45	± 0.53 0.8 – 1.2 V	± 0.13[b] -20 – 100 °C	150
2017 [73]	180	0.4449	21.3	47.9	1.8	-103 @10kHz	152.7 @10kHz	0.047	± 0.038[f] 1.4 – 3.3V	± 1.01[c] -20 –100 °C	N.A.
2018 [44]	180	0.364	1.36	3.7	1.2	N.A.	156.4 @100kHz	0.025	N.A.	± 0.39[d] -20 – 90 °C	N.A.
2019 [72]	180	0.9431	5.2	5.5	0.9	-96.78 @100kHz	139.1 @100kHz	N.A.	± 1.53[g] 0.8 – 1.5V	± 0.516[h] -10 – 100 °C	N.A.
2019 [74]	350	1	160	160	3.3	-92 @10kHz	140 @10kHz	0.0235[i]	±0.12[l] 3 – 4.5V	± 0.26 -40 –125 °C	1
2019 [75]	180	13.4	157.8	11.78	1.2	-104.82 @100kHz	154.4 @100kHz	N.A.	N.A.	± 1.16[k] -20 –100 °C	N.A.
2019 [64]	65	1.05	69	65.7	1	N.A.	N.A.	0.016	±0.085[j] 0.98 – 1.02V	± 0.005[m] 0 –40 °C	8[p]

- Converted from reported data of [a]137 ppm/°C, [b]21.8 ppm/°C, [c]169 ppm/°C, [d]70 ppm/°C, [e]±0.44%/V, [f]±0.02%/V, [g]4.73%/V, [h]93.88 ppm/°C, [i]235 ppm, [j]±0.08%/V, [k]193.15 ppm/°C, [l]0.17% with LDO, [m]2.5 ppm/°C, and [p]8 us.

variation. This is because the comparator switching threshold is fixed at $0.5V_{DD}$ by the replica bias such that it tracks the variation of supply voltage automatically. However, a ±0.15% variation is still observed due to the supply-dependent circuit delay variation. On the other hand, the frequency is more sensitive to the temperature variation because the higher order temperature dependent terms still exist after the 1st order resistive temperature compensation. To improve the frequency stability over supply and temperature, feedback circuit in [47] and [51] can be adopted. To reduce the higher order temperature dependency of the timing resistor, resistor combination with different temperature coefficients such as in [63], and dynamic frequency error compensation in [64] can be considered.

The measurement results are summarized in Table I and compared with other state-of-the-art relaxation oscillators. The proposed design shows excellent FOM of 161 dBc/Hz, consuming only 5.7 pJ/cycle energy. The FOM is calculated using

$$\text{FOM (dBc/Hz)} = L(\Delta f) + 20\log\left(\frac{\Delta f}{f_{osc}}\right) + 10\log\left(\frac{P_{total}}{1mW}\right) \quad (15)$$

Compared to the reported energy efficient designs [65] [66] [44] [72], this oscillator achieves the highest FOM and the lowest phase noise and relative jitter, indicating a better trade-off between energy efficiency and noise performance. Comparing to [42] which has the highest FOM of 162.1 dBc/Hz, this design achieved 12.7× reduction in total power and 4× reduction in energy per cycle, demonstrating significant improvement in power efficiency. Comparing to [47] [51] [73] [74] [75], this design demonstrates the highest FOM and lowest energy per cycle. Overall, the proposed design realized both high energy efficiency and FOM, providing a good trade-off between the energy efficiency and noise performance.

3.7 Conclusion

In this chapter, a low jitter RC relaxation oscillator with power efficient swing boosting technique is proposed. The analysis of the new boosting circuit is also presented. The oscillator oscillates at 3.0 MHz and consumes 17.3 μW of power under 1 V. This design achieves a FOM of 161 dBc/Hz while consuming merely 5.7 pJ/cycle energy. The frequency variation is ±0.6% over a temperature range of 0 °C to 90°C, and ±0.15% over a supply range of 0.95 V to 1.45 V. The proposed relaxation oscillator demonstrates great potential for sensor interface applications or on-chip clock reference.

Chapter 4

Relaxation Oscillator with Voltage-to-Delay Feedback and Switch Capacitor Swing Boosting

Abstract

This chapter presents a new low-jitter low frequency inaccuracy RC relaxation oscillator for biomedical sensor interface application or on-chip clock reference. A novel relaxation oscillator with voltage-to-delay feedback (VDF) and switch-capacitor swing boosting (SCSB) RC network is proposed to effectively improve the oscillator phase noise and frequency accuracy over supply and temperature variations. The novel VDF keeps track of the circuit delay and regulate the comparator delay accordingly such that the overall circuit delay remains unchanged. The SCSB RC network enhances capacitor voltage swing for phase noise reduction. The first-order resistive temperature compensation is also employed in this design to reduce output frequency variation over temperature variations. The prototype relaxation oscillator circuit is designed and fabricated in a commercial 180-nm CMOS process. The measured output frequency is 1.6 MHz under nominal supply voltage of 1.3 V, consuming a total power of 51.4 μW. The measured output phase noise of -118.6 dBc/Hz at 100 kHz offset frequency. The measured relative period jitter is 0.01%. The frequency inaccuracy is $\pm 0.15\%$/V over a supply range of 1.24 V to 1.48 V, and 23.35 ppm/°C over a temperature range of 0°C to 90°C. The Figure-of-Merit (FOM) is computed to be 155.6 dBc/Hz.

Organization of Chapter

This chapter is organized as follows. Section 4.1 summarizes previous

works and indicates the new targets to achieve. Section 4.2 presents the proposed techniques and relaxation oscillator that meets the targets. Section 4.3 presents the circuit block designs. Section 4.4 reported the measurement results of the proposed relaxation oscillator with discussions. Lastly, section 4.5 summarizes the work done in this chapter.

4.1 Introduction

The fully integrated on-chip relaxation oscillator has attracted significant research interests in recent years. This is attributed to its great potentials as on-chip clock reference or sensor interface for IoT and wearable healthcare device. It is area and cost efficient compared to the bulky off-chip crystal oscillator. It is also preferred over the ring oscillator for its high frequency stability, control linearity and wide tuning range [42]. However, many issues remain to be addressed when designing high performance relaxation oscillator. In Section 3.1, the main challenges of designing a relaxation oscillator for sensor interface application or on-chip clock reference are identified. They are the low output phase noise, high energy efficiency and low frequency inaccuracy with supply and temperature variations. In chapter 3, a novel energy efficient low phase noise RC relaxation oscillator to address the first two challenges is presented. As no dedicated technique was proposed to reduce the frequency inaccuracy over supply and temperature variations, a RC relaxation oscillator with voltage-to-delay feedback (VDF) and switch-capacitor swing boosting (SCSB) is proposed to address this problem.

4.1.1 Frequency Variation due to Circuit Delay Variation

It is understood that the supply change alters the oscillator circuit delay. With a larger voltage headroom, the current flowing through each branch of the circuit increases, resulting in less circuit delay. Referring to Fig. 29, when taking the circuit delay into consideration, the oscillation period of design in Fig. 19 is expressed as

$$T_{osc,real}=T_{osc,ideal}+2t_d \quad (16)$$

where $T_{osc,ideal}$ is the ideal oscillation period as shown by Eq.(9) and t_d is the

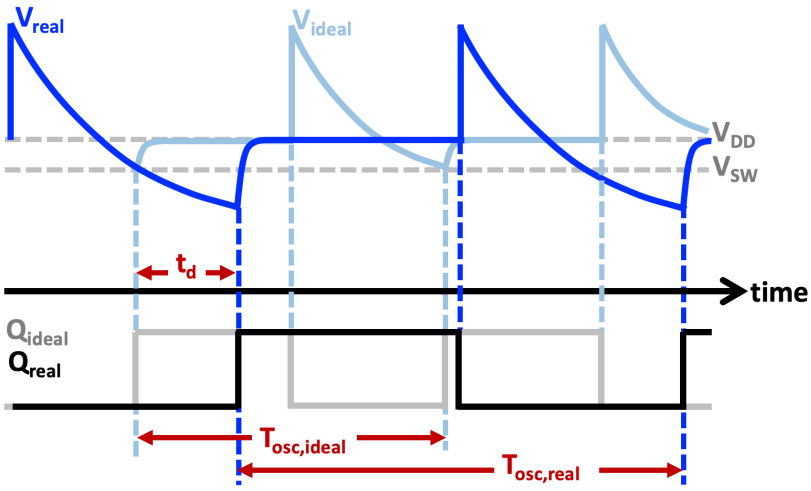

Fig. 29: Impact of circuit delay on oscillation period.

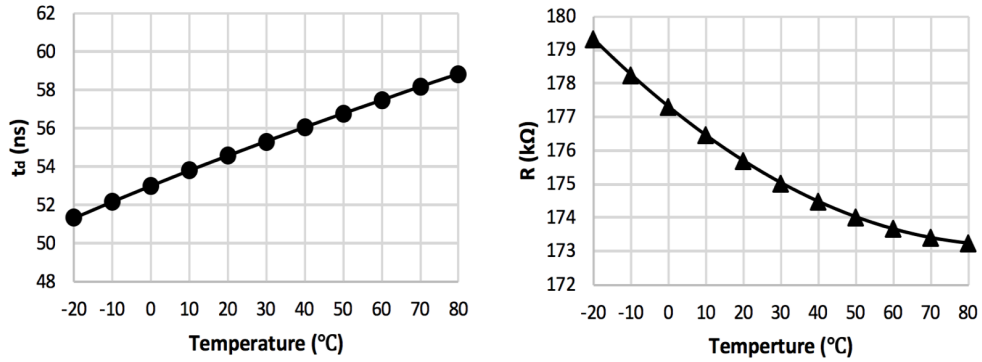

Fig. 30: Resistance versus temperature of (a) PTAT resistor (b) CTAT resistor.

circuit delay.

The circuit delay is inevitable and cannot be removed because all circuits need some time to generate outputs in response to input changes, i.e. the propagation delay always exists. Although circuit delay is a non-ideal factor in the oscillation period expression, it will have negligible impact on the oscillation frequency if it is a constant under all situations. However, in reality, the circuit delay varies with supply and temperature, resulting in oscillation frequency variation with supply and temperature too. Therefore, to compensate for the frequency variation, the circuit delay should be regulated carefully.

4.1.2 Frequency Variation due to Resistance Variation

One of the major impacts of temperature variation is the timing resistance variation, which in turn changes the RC constant and thus the oscillation period.

Referring to Fig. 30, resistors generally have proportional-to-absolute-temperature (PTAT) or complimentary-to-absolute-temperature (CTAT) temperature profiles. Therefore, when temperature changes, due to the change of resistance, the RC constant in relaxation oscillator varies too, which results in frequency variation with temperature. Therefore, resistance variation should be compensated for high frequency stability over temperatures.

4.1.3 Existing Designs

Many circuit design techniques have been reported to improve the frequency stability over supply and/or temperature variations such as [50] [51] [52] [53]. In [50], the voltage averaging feedback (VAF) technique is proposed. The capacitor voltage swing is integrated over half of the oscillation period. The integrator output voltage regulates the comparator switching threshold which compensate the circuit delay to achieve constant the oscillation period. In [51], the feedback mechanism called integrated error feedback (IEF) is proposed to integrate only the part of capacitor voltage swing due to circuit delay. The integrator output is also used as the comparator switching threshold. In [52], instead of employing analog integrator for integration and feedback, a digital compensation technique is proposed to adjust the delay of a delay cell implemented in the oscillator. In [53], instead of using digital compensation loop, Gm-C integrator is implemented to regulate the delay of the delay cell. Previous works have demonstrated the effectiveness of feedback mechanism in reducing the frequency inaccuracy over supply and temperature variations. Therefore, in this design, a new implementation of feedback is proposed which is the VDF. Meanwhile, for designs discussed previously, they demonstrate limited phase noise performance, which is not desirable for sensor interface application. Therefore, other than VDF, the switch-capacitor swing boosting (SCSB) technique is also employed in this design for phase noise reduction.

In this chapter, a novel on-chip RC relaxation oscillator with VDF and SCSB technique is proposed to reduce output phase noise and frequency inaccuracy due to circuit delay variation with supply and temperature. The proposed relaxation oscillator achieves low phase noise of -118.6 dBc/Hz which is at least 18 dBc/Hz less when compared to [51] [47] which are also of feedback topologies. Comparing with [42], which has the closest phase noise

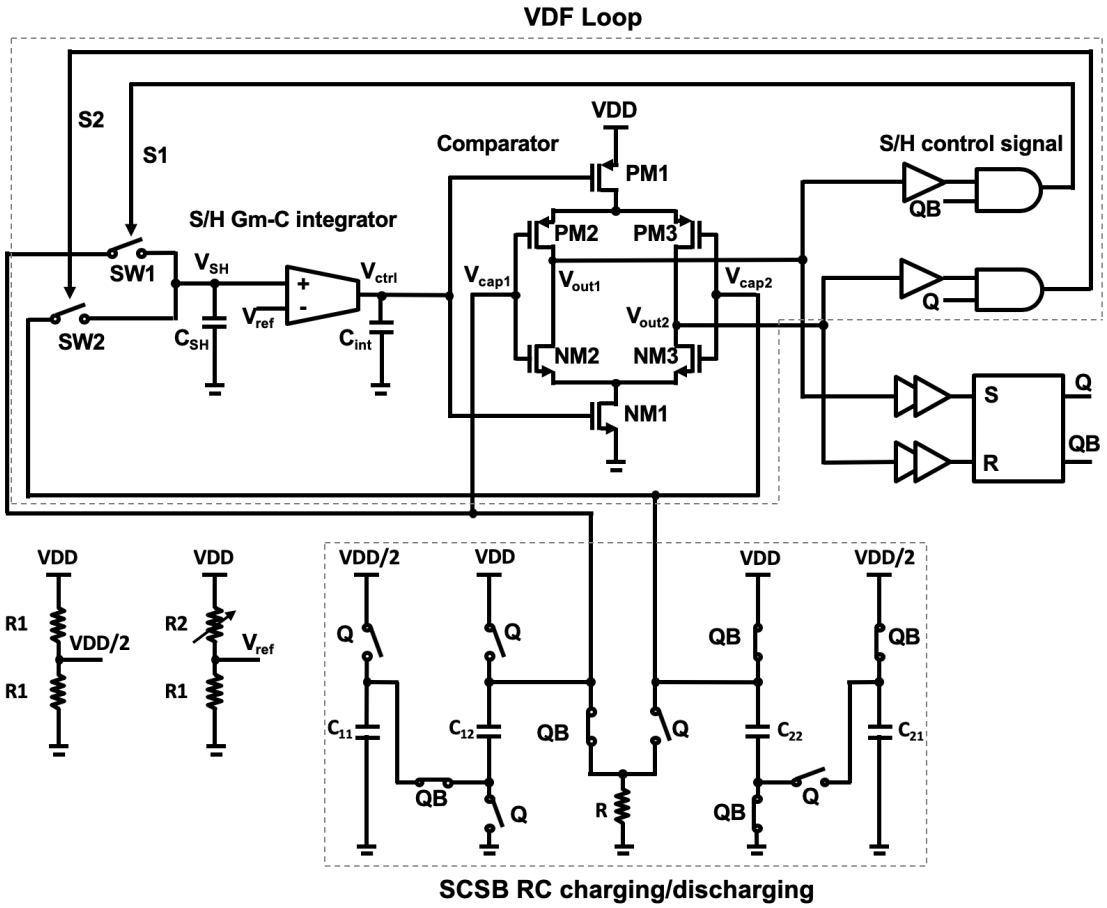

Fig. 31: Schematic of proposed relaxation oscillator.

performance, the proposed oscillator achieves a 5.9× as well as a 2.9× reduction in frequency inaccuracy over temperature and supply variations.

4.2 Proposed Relaxation Oscillator

4.2.1 Architecture of the Proposed Design

Fig. 31 shows the schematic of the proposed RC relaxation oscillator. It consists of three main building blocks: (1) a voltage-to-delay feedback (VDF) loop consisting of a sample and hold (S/H) Gm-C integrator and an inverter-based comparator, (2) a switch-capacitor swing boosting (SCSB) RC charging and discharging circuit, and (3) a SR latch.

Fig. 32 shows the timing diagram of the proposed oscillator. The first clock cycle represents the steady-state operation of the system. A new cycle starts with the state of Q = LOW and QB = HI. These two complimentary signals set the SCSB block in the configuration shown in Fig. 31. Capacitors C_{11} and C_{12}

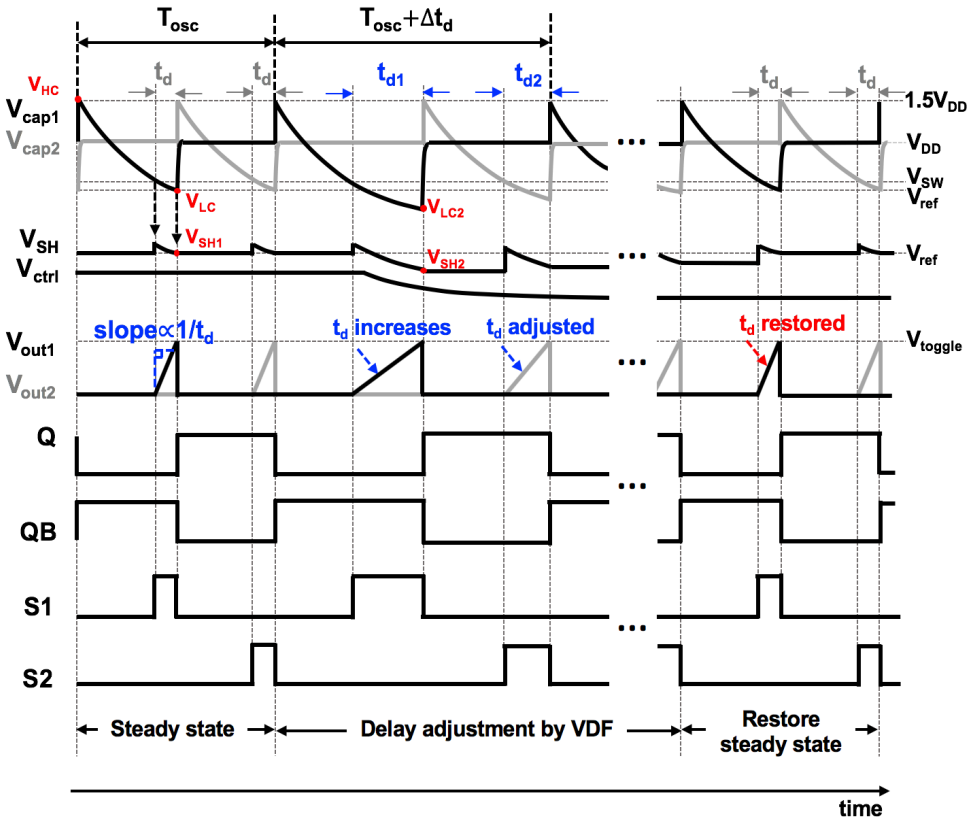

Fig. 32: Timing diagram of proposed oscillator with VDF loop.

are stacked in series and discharged via resistor R, while C_{21} and C_{22} are charged and held at V_{DD} and $V_{DD}/2$, setting $V_{cap1}=1.5V_{DD}$ and $V_{cap2}=V_{DD}$. When V_{cap1} decreases to the comparator switching point V_{SW}, comparator output V_{out1} starts to increase. V_{out2} is still at LOW since V_{cap2} is held at V_{DD}. As a result, the SR latch toggles its outputs Q and QB. C_{11} and C_{12} are reconfigured in parallel connection, charged and held at V_{DD} and $V_{DD}/2$, while C_{21} and C_{22} are stacked in series and discharged via resistor R. Meanwhile, the increase of V_{out1} also triggers the S/H control circuit to generate a sampling pulse S1, which closes the switch SW1 to cause voltage V_{cap1} to be sampled onto capacitor C_{SH}. Due to circuit delay, the sampled voltage V_{SH1} is lower than the comparator's V_{SW}. The Gm-C integrator compares V_{SH1} with a preset reference voltage V_{ref} and integrates the difference over half of the clock period. The integrator output V_{ctrl} controls the gate drive voltage of the comparator biasing transistor PM_1, which then controls the comparator current and delay. In this design, V_{SW} is of $V_{DD}/2$ and under steady state, $V_{LC}=V_{ref}=0.4V_{DD}$ and V_{LC} is the lowest peak of V_{cap1}. The nominal output period is represented as:

$$T_{osc}=2RC\ln\left(\frac{V_{HC}}{V_{LC}}\right)=2RC\ln\left(\frac{1.5V_{DD}}{0.4V_{DD}}\right)=2RC\ln(3.75) \quad (17)$$

where $C=(C_{11}C_{12})/(C_{11}+C_{12})=(C_{21}C_{22})/(C_{21}+C_{22})$ and all capacitors are on-chip temperature-insensitive MIM capacitors, and V_{HC} is the highest peak of V_{cap1}.

4.2.2 Operation of VDF Compensation Loop

Fig. 32 also illustrates the operation of the proposed VDF compensation loop when there is a change in circuit delay due to either a change in the supply or temperature. This changed delay is labelled as t_{d1} in the second clock cycle in Fig. 32. To illustrate the feedback operation, take for example, with lower supply, t_{d1} is longer than the nominal delay t_d. There is thus a longer discharging time for C_{11} and C_{12}, causing V_{cap1} to drop to beyond its lowest nominal voltage level V_{ref}. The discharging process continues until Q and QB toggle after a delay t_{d1} with corresponding $V_{cap1}=V_{LC2}$. The output period is thus increased from T_{osc} to $T_{osc} + \Delta t_d$, where Δt_d represents the change in delay. To recover the distorted period, the S/H circuit samples the voltage V_{LC2} onto C_{SH} as V_{SH2}, which is lower than the Gm-C integrator's reference voltage V_{ref}. The integrator output V_{ctrl} therefore decreases, resulting in an increase in comparator current since V_{ctrl} is the gate voltage of the current-controlling transistor PM_1. A higher comparator bias current leads to a reduction in comparator delay from t_{d1} to t_{d2} in the next half clock cycle. The VDF works continuously, adjusting the delay until the original t_d is restored.

It should be noted that the proposed VDF loop is different from the feedback systems reported in [51] and [52]. Instead of using multiple comparators and power consuming integrator as [51], the new S/H control signal generating circuit and the half-clock-cycle integration window designed in the proposed oscillator eliminate multiple comparators and relax the speed requirement on the integrator, thus achieving the low power operation for this design. The digital delay compensation is proposed in [52]. However, it is a one-time non-autonomous calibration, whereby the delay change cannot be compensated in real time.

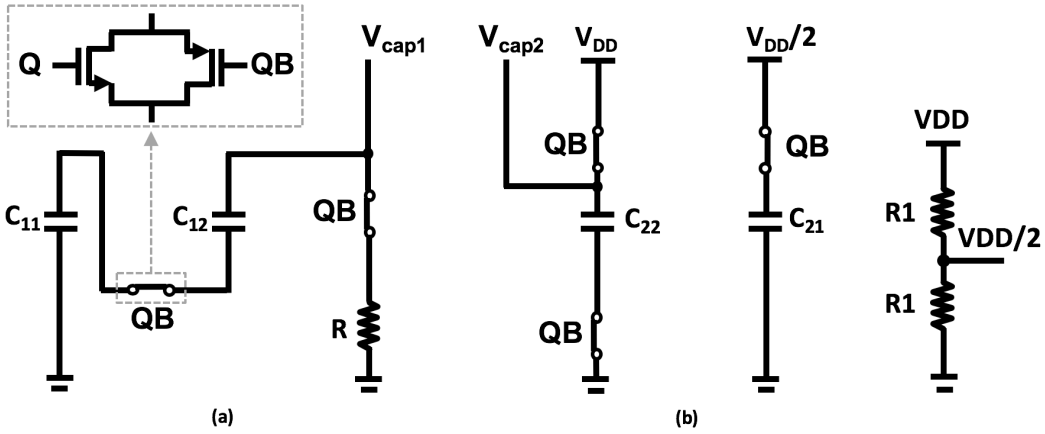

Fig. 33: RC network during: (a) discharging phase, and (b) charging phase.

4.3 Circuit Implementation

4.3.1 Switch-Capacitor Swing Boosting (SCSB)

Fig. 33 shows the capacitor configuration in charging and discharging phases [76]. The switch matrix controls the connection of capacitors. During the discharging phase, two capacitors are stacked in series as shown in Fig. 33(a) for instant swing boosting followed by discharging. During the charging phase, two capacitors are charged to V_{DD} and $V_{DD}/2$, respectively, and in parallel. Such switch-capacitor swing boosting (SCSB) circuit creates a capacitor discharging voltage swing of $1.1V_{DD}$, which is higher than the swing of V_{DD} in [42]. This further improves the phase noise of this design. Meanwhile, the SCSB circuit only boosts the capacitor voltage up to $1.5V_{DD}$, which is well within the allowed electrical stress range of the fabrication process.

4.3.2 The Voltage-to-Delay Feedback (VDF) Loop

The complete voltage-to-delay feedback (VDF) loop is shown in Fig. 31. The Gm-C integrator circuit is shown in Fig. 34. It consists of the differential inputs and a single-ended output. The two stages structure is adopted to deliver current to C_{int} for the integration of V_{ctrl}. The window left for the integration is half that of the clock cycle, alleviating the speed requirement for this integrator. Also, compared to [47] and [51] which require integrators with wide output voltage linear range for generating feedback voltages, the VDF loop makes use of the

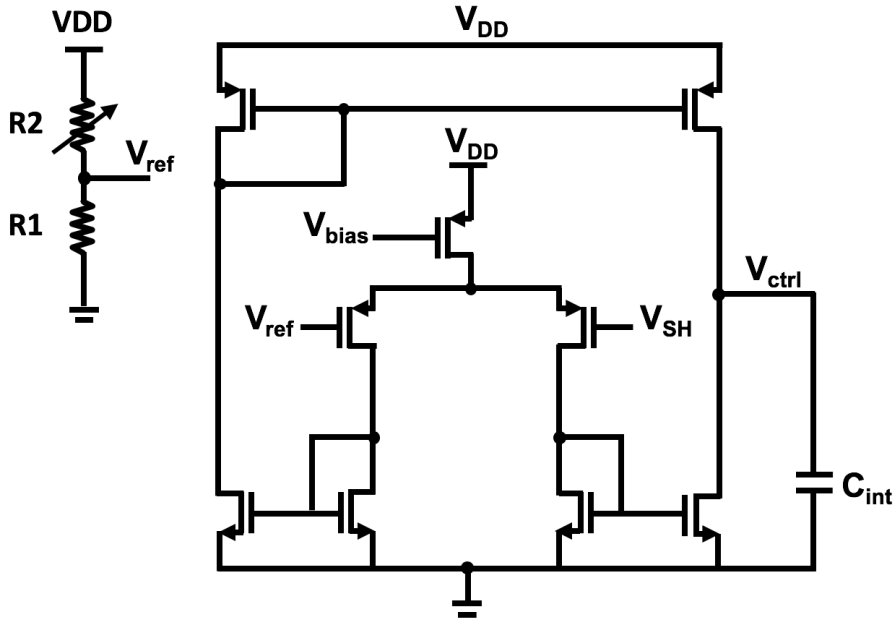

Fig. 34: Gm-C integrator.

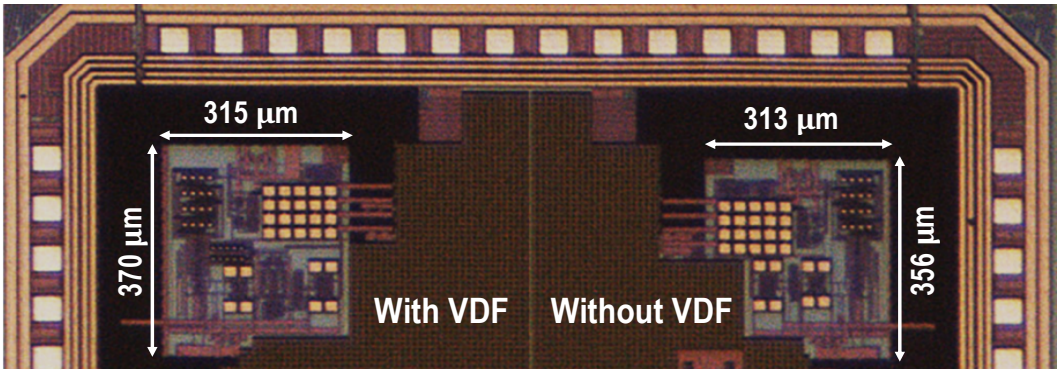

Fig. 35: Die photo of the proposed circuit.

square relationship between PM_1 drain current and its gate overdrive voltage. This relieves the integrator output linear range, reducing its power consumption. On the other hand, the integrator reference V_{ref} is designed to be CTAT to compensate the CTAT resistor R. This is achieved by selecting R2 to be more PTAT than R1.

The inverter-based comparator circuit is shown in Fig. 31. It contains current starving biasing transistors and inverter-based differential input pairs. Its current, and thus the delay, is controlled by the bias voltage V_{ctrl}. Due to the large transconductance g_m, the inverter-based comparator can have small input-referred noise to realize a reduction of phase noise. The dynamic nature of this comparator also helps to lower the power consumption.

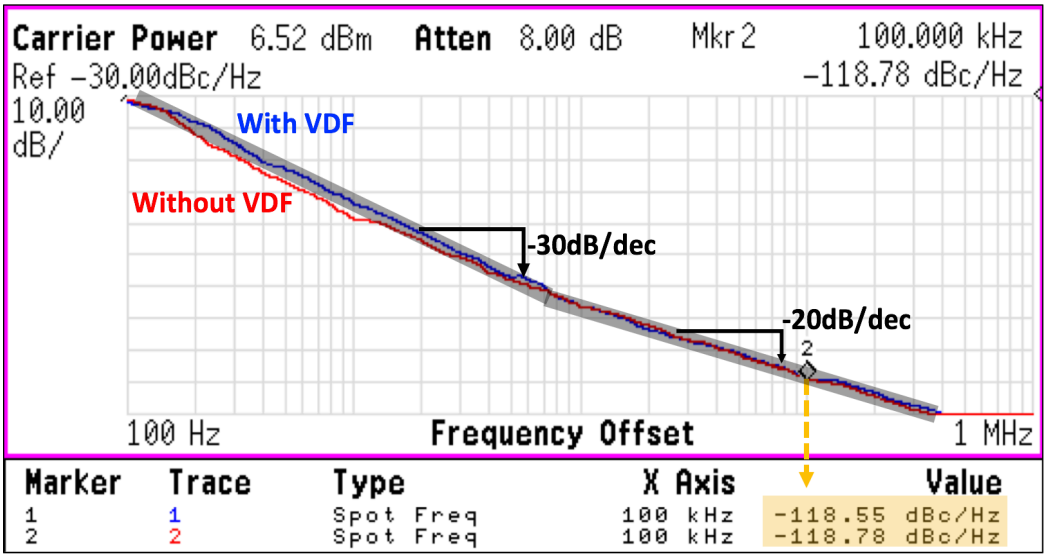

Fig. 36: Measured phase noise of oscillator with and without VDF.

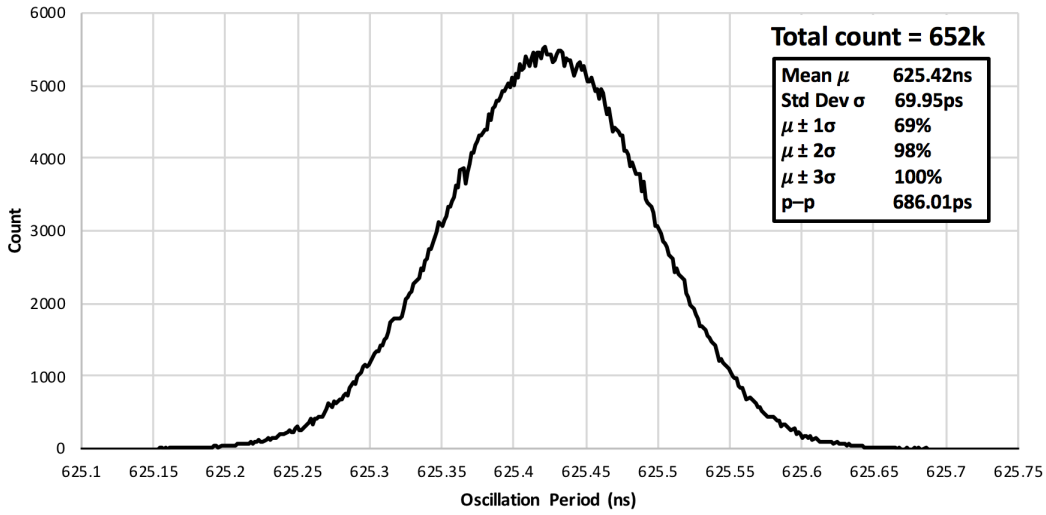

Fig. 37: Statistical distribution of period of the proposed oscillator.

4.4 Measurement Results

The proposed design has been fabricated in a standard 0.18-μm CMOS process. The chip die photo is shown in Fig. 35. To validate the efficacy of the proposed VDF, the same oscillator core without VDF loop is also fabricated. A replica bias introduced in [42] and [76] is used as a proper bias to the inverter-based comparator for fair performance comparison. The active chip area is 0.12mm^2. The measured oscillation frequency is 1.6 MHz with 51.4-μW power consumption under 1.3-V supply.

The measured output phase noise is shown in Fig. 36. It is observed that

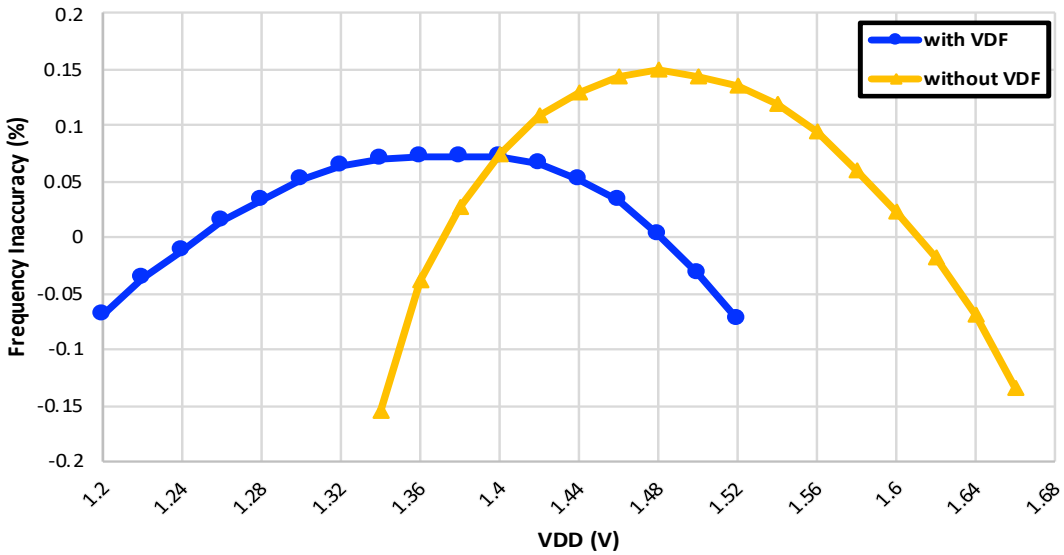

Fig. 38: Frequency variations with V_{DD}, both with and without VDF.

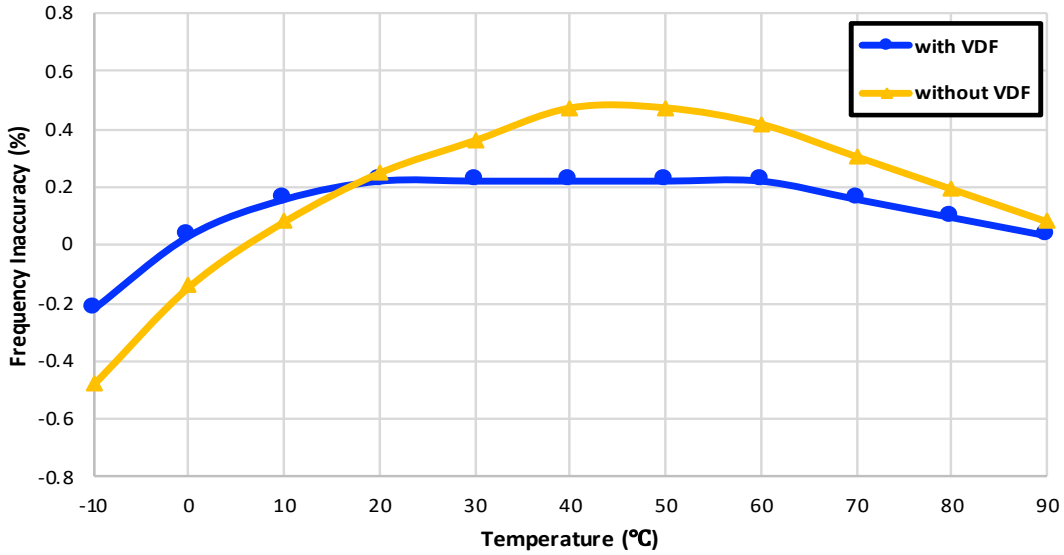

Fig. 39: Frequency variations with temperature, both with and without VDF.

oscillators, both with and without VDF, achieve similar phase noise performance at 100 kHz frequency offset, namely -118.6 dBc/Hz with VDF and -118.8 dBc/Hz without VDF. This shows that the VDF does not add significant noise to the oscillator output, thanks to the large g_m of the inverter-based comparator which reduces the VDF noise being referred back to the comparator inputs.

Fig. 37 shows the measured statistical distribution of the oscillation period. The total number of cycles measured is about 652k. The measured period mean μ for these cycles is 625.42 ns, which corresponds to 1.6 MHz in frequency. With measured standard deviation σ of 69.95 ps, the relative period jitter is as low as 0.01%. Statistically, 69% of the sample falls within 1σ offset from the mean, 98% falls within 2σ offset and 100% falls within 3σ offset. This shows that

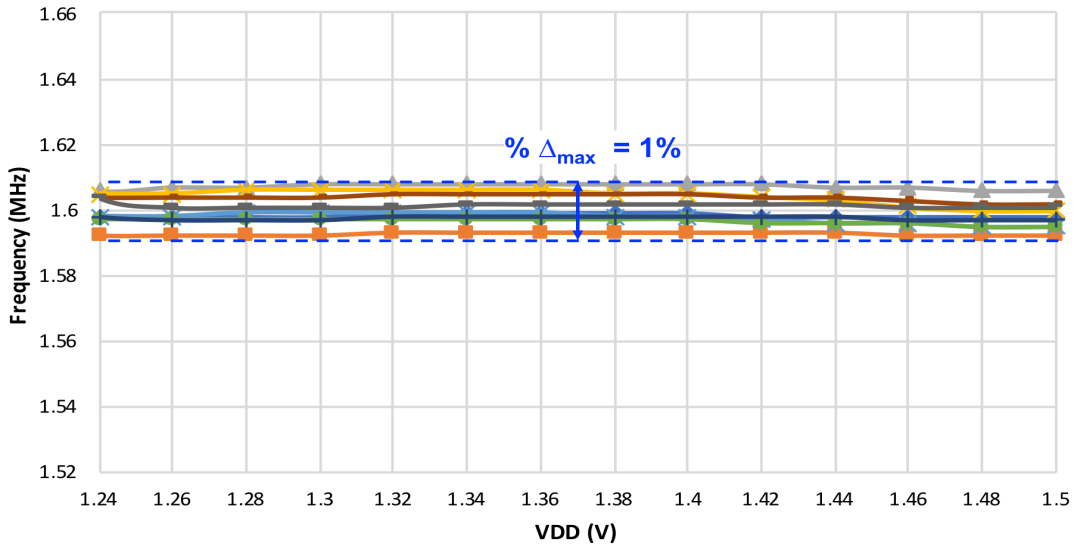

Fig. 40: Frequency versus V_{DD} for 9 samples of the proposed oscillator.

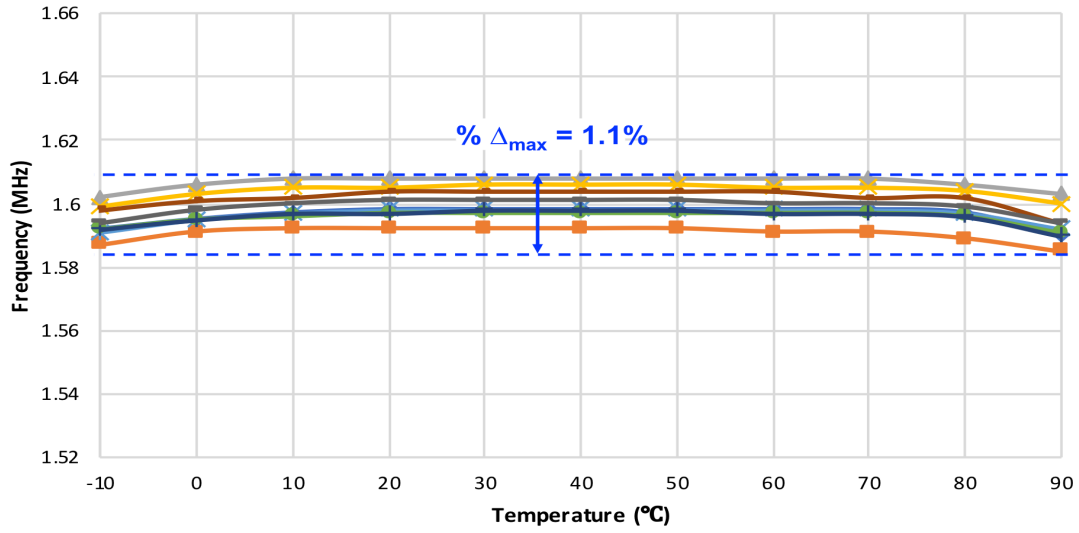

Fig. 41: Frequency versus temperature for 9 samples of the proposed oscillator.

the oscillation period is very centralized around the mean value and the deviation from the mean is rather small.

Fig. 38 and Fig. 39 show the measured frequency inaccuracy over supply and temperature variations, respectively. The oscillator without VDF requires higher typical voltage for its replica bias circuit. For oscillator with VDF, the frequency inaccuracy is ±0.19%/V and 23.4 ppm/°C across 1.2 V to 1.52 V and 0°C to 90°C, respectively. With a wider temperature range of -10°C to 90°C, the frequency inaccuracy is 41 ppm/°C. For oscillator without VDF, the frequency variation is ±0.48%/V and 68.5 ppm/°C across 1.34 V to 1.66 V and 0°C to 90°C, respectively. Compared to oscillator without VDF, the proposed oscillator with

Table 2: Performance Comparison for 2nd Design

Year	Tech. (nm)	Power (µW)	Freq. (MHz)	Supply (V)	Freq. Var. with VDD (%/V)		Freq. Var. with with Temp. (ppm/°C)		Phase noise (dBc/Hz)	FOM (dBc/Hz)
This work	**180**	**51.4**	**1.6**	**1.3**	**±0.19**	**1.2 - 1.52V**	**23.4** **41**	**0 – 90 °C** **-10 – 90 °C**	**-118.6 @100kHz**	**156 @100kHz**
2016 [42]	180	219.8	10.5	1.4	± 0.44	1.4 - 2V	137	-40 – 125 °C	-115.1 @100kHz	162.1 @100kHz
2015 [93]	180	12.8[a] / 56.2[b]	12.77	0.9	± 0.5	0.6 – 1.1V	53.3[c]	-30 – 120 °C	N.A.	N.A.
2014 [53]	180	16.6	32.8	1.5	± 0.13	1.5 – 3.6V	134	-40 – 85 °C	N.A.	N.A.
2013 [51]	65	98.4	12.6	1.2	± 0.18[d]	1.1 - 1.5V	205[e]	0 – 80 °C	-100 @100kHz	152.6 @100kHz
2010 [47]	65	100	6	1.25	± 0.26	1.15 - 1.35V	24	-40 – 125 °C	-70 @10kHz	137.6 @1kHz
2009 [94]	130	38	3.2	1.4	± 0.4	1.4 - 1.6V	125	20 – 60 °C	N.A.	132 @10kHz

[a]Oscillator core only; [b]With digital calibration; Converted from original reported data of [c]± 0.4%, [d]± 0.07%, [e]± 0.82%

VDF achieves 2.5× and 2.9× reduction in frequency inaccuracy over supply and temperature variations, respectively. The frequency variation over supply and temperature for 9 samples of circuit are illustrated in Fig. 40 and Fig. 41. Across VDD range of 1.2 V to 1.52 V and temperature range of -10°C to 90°C, the output frequency of these 9 samples concentrates around 1.6 MHz, with deviation of 1% and 1.1% from nominal 1.6 MHz, respectively. The cross-chip measurements show a constant trend of frequency variation over supply and temperature. The deviation from nominal frequency among 9 samples is thus mainly due to process variation and the parasitic added. Noted that there is no supply regulation circuit used in both oscillators.

The measured results are summarized in Table 2. Compare with other state-of-the-art relaxation oscillators, this design shows low frequency inaccuracy to both supply and temperature variation, while at the same time achieves low phase noise. The achieved FOM is 156 dBc/Hz, which is the highest among designs with feedback structures [47] [51].

4.5 Conclusion

In this work, a low phase noise RC relaxation oscillator with improved resilience to supply and temperature variations is presented. The oscillator oscillates at 1.6 MHz and consumes 51.4 µW of power under 1.3 V. The proposed design achieves frequency inaccuracy of 23.4 ppm/°C over 0°C to

90°C, and ±0.19%/V over 1.2 V to 1.52 V. The phase noise at 100 kHz frequency offset is -118.6 dBc/Hz and the corresponding FOM is 156 dBc/Hz. The proposed RC relaxation oscillator is therefore a good candidate for on-chip clock reference or high precision sensor interface applications.

As compared to the design in chapter 3, this design demonstrates outstanding frequency stability over supply and temperature variations while achieving low phase noise at the same time. However, the energy efficient swing boosting technique is not implemented in this design, and therefore, the energy efficiency of this design is lower than that of the previous design. As a result, another design with both VDF and energy efficient swing boosting is being fabricated and will be presented in our future publication.

Chapter 5

Wide Input Range Wide Bandwidth VCO-based CT-DSM Bio-Signal Recording Interface

Abstract

This chapter presents a wide input range wide bandwidth bio-potential recording circuit. An energy efficient voltage-controlled oscillator (VCO) based continuous time Delta Sigma Modulator (CT-DSM) which is able to handle 100-mV_{pp} 10-kHz bandwidth (BW) input signal is proposed. The current-reuse fully differential operational transconductance amplifier (OTA) provides high gain for both oscillator phase noise and quantization noise attenuation. The VCO converts time-domain input signals to frequency for quantization, alleviating the supply constraint on the quantization resolution while at the same time reducing design complexity with CMOS technology scaling. The digital counter-based phase quantizer realizes phase quantization of VCO outputs. The feedback structure increases the input linearity range to avoid frontend saturation under large input signal swing. The prototype circuit is designed and fabricated in a commercial 40-nm CMOS process. The simulated chip total power consumption is 19.5 μW under 1.2-V supply voltage for 1kHz-BW 100-mV_{pp} input signal, which corresponds to a low FOMw of 1.19 pJ/conv. The SNDR is 59 dB for 10-kHz BW input and 63 dB for a reduced BW of 2 kHz. The large input swing tolerance, wide signal BW and high energy efficiency make the proposed design suitable for applications such as wearable vital signs monitoring or closed-loop neural stimulation system.

Organization of Chapter

This chapter is organized as follows. Section 5.1 introduces related prior arts and the target system specifications. Section 5.2 presents the proposed system architecture and the circuit model. Section 5.3 presents the circuit block design in detail. Section 5.4 reports the simulation results of the proposed design with discussions. Section 5.5 summarizes the work done in this chapter.

5.1 Introduction

Different from the relaxation oscillator-based sensor interface circuits presented in Chapter 3 and 4, this chapter presents another type of interface circuit — the VCO-based Continuous-Time Delta-Sigma Modulator (CT-DSM). In this design CT-DSM is adopted as the bio-potential recording front-end of the closed-loop electrical stimulation system to attain high energy efficiency, wide input range and high resolution.

Electrical stimulation has been proven to be a safe and effective medical therapy for various central nerve system (CNS) disorders such as Parkinson's disease, essential tremor and dystonia [77]. Recently, there are increasing interests to extend the electrical stimulation to the peripheral nerve system (PNS). By modulating a specific PNS neural pathway with electrical signals, therapeutic outcomes can be achieved for symptoms such as chronic pain, hypertension and rheumatoid arthritis [78].

Compared to the conventional open-loop stimulator architecture, a closed-loop stimulator can adjust the stimulation parameters dynamically based on the feedback signal. This feedback mechanism is usually based on the recording of the evoked action potential (EAP) generated by the stimulation signal. This adaptive stimulation leads to personalized therapy with better treatment outcomes [79]. However, the EAP signal is generally much smaller compared to the interferences such as stimulation artifacts and electrode input DC offset. Fig. 42 illustrates the amplitude difference of the EAP signal and other interferences. The EAP signal usually has an amplitude ranging from a few μV to 1 mV. However, the stimulation artifacts or electrode offset can reach 100 mV. The large interferences will cause saturation of the recording analog frontend and

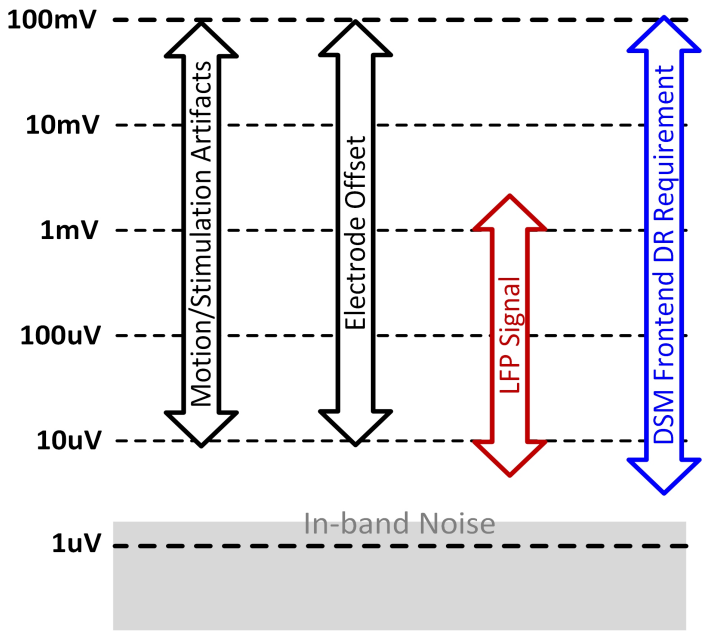

Fig. 42: Amplitude ranges of signals.

degrade or even disable the recording function. To achieve large input range, a traditional method is to implement a large input range frontend circuit, i.e. operational amplifier, which consumes significant amount of power, sacrificing the circuit energy efficiency. Therefore, in our design, a frontend circuit with large linear input range while having high energy efficiency is targeted for high fidelity closed-loop stimulation application.

The VCO-based CT-DSM has been used in various recording interface circuits [34] [80] [81] [32] [33]. It converts signals from voltage domain to phase domain for phase quantization. Compared to the traditional voltage integrator and quantizer, the major advantage of VCO-based CT-DSM is that the performance is not limited by the voltage headroom constraint, amplifier's finite DC gain or process scaling [32]. Many VCO-based CT-DSM designs for neuro-recording have been reported. In [32], an open-loop architecture with current control oscillator (CCO) front-end and phase quantizer has been proposed. The digital-intensive DSM achieved high area efficiency and low noise PSD. The shortcoming, however, is that its input range is limited by the narrow linear input range of the front-end. To extend the input signal range, various close-loop architectures have been proposed. In [80] [33], a capacitively-coupled DAC is employed as the feedback circuit. This effectively improves the input range as

compared to [32]. In [34], a digital nonlinearity correction (NLC) circuit is designed to compensate the nonlinear operation of the DSM under large input range. Up to 5^{th}-order of nonlinearity can be compensated by NLC. However, the NLC logic involves polynomial coefficients computation, which increases the design complexity and occupies a significant die area. In [81], a degeneration R-DAC feedback is introduced to mitigate the nonlinearity and increase input linear range. One trade-off of this method is the resistor noise which increases the noise floor.

In this chapter, a closed-loop VCO-based CT-DSM for bio-potential recording is proposed. A system feedback loop consisting of data weighted averaging circuit (DWA) and capacitive DAC is employed to boost the input linear range. A current-reused OTA frontend is proposed to suppress the overall input-referred noise. A current-starving ring oscillator as VCO is proposed to realize the voltage-to-phase conversion. Under a nominal supply voltage of 1.2V, it consumes 19.5 μW of power. It is able to maintain linear operation with input signal amplitude up to 100 mV_{pp}, achieving a SNDR of 59 dB over a wide frequency bandwidth of 10 kHz. As compared to [32], the proposed design improved the input amplitude range by 12.5$\times$ with 2$\times$ wider bandwidth while achieving the comparable SNDR. Comparing to [34], the proposed design achieves the same input range and reduces the feedback design complexity while achieving 50$\times$ wider bandwidth.

5.2 System Architecture and Circuit Model

5.2.1 System Architecture

The system architecture of the proposed VCO-based DSM circuit is given in Fig. 43. It consists of a current-reuse OTA, VCO-based voltage-to-phase converters, a counter-based 5-bit quantizer, a 5-to-32 DWA thermos-code generator, and the capacitively-coupled DAC feedback circuits. A fully differential OTA is used as the input G_m stage. The AC coupling capacitor C_{in}, DC bias resistor R_{bias}, and OTA input impedance R_{in} collectively forms the RC high pass filter (HPF) at the OTA input to reject input DC offset. Each HPF has a high pass corner frequency lower than 10 Hz to prevent undesirable neural

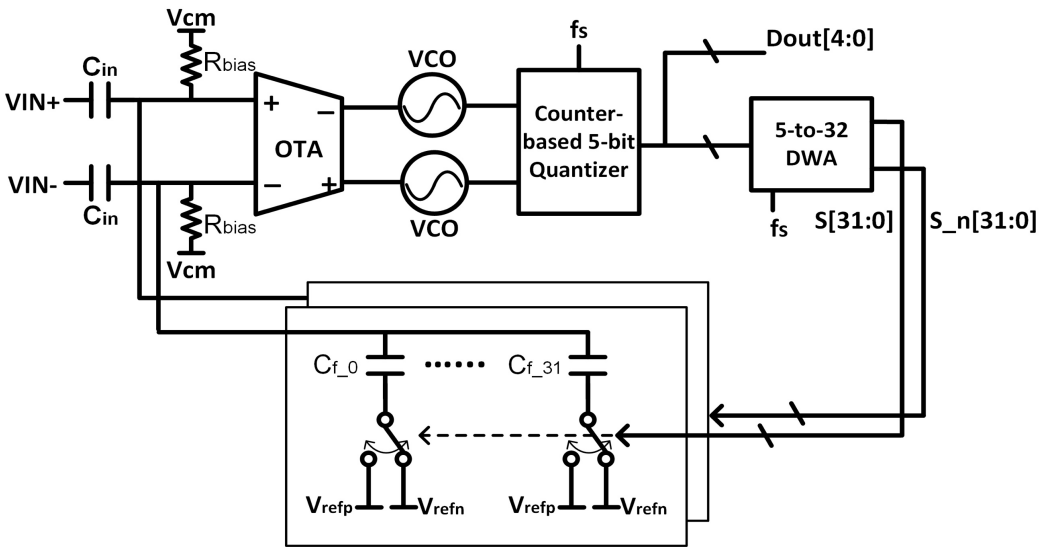

Fig. 43: Block diagram of proposed VCO-based CT-DSM.

signal loss and to minimize noise contribution from HPF to the inputs. Previous studies presented in [34] [82] have shown that

$$v_{n,HPF}^2 \propto \frac{f_c}{f_l} \quad (18)$$

where $v_{n,HPF}^2$ is the noise generated by HPF, f_c is the HPF corner frequency and f_l is the lower bound of signal band. In order to minimize additional noise from the HPF, the corner frequency f_c should be small as compared to f_l. This requires large RC constant which translates to large passive components. For example, with C_{in}=10 pF and f_l=10 Hz, the corresponding HPF resistor has to be at least 15.9 GΩ such that f_c/f_l = 0.1. Therefore, pseudo-resistor is employed for both high resistance and area efficiency. On the other hand, the input common-mode voltage of OTA is provided via R_{bias}. This sets the correct biasing region for OTA throughout the entire operation. It should be noted that although the maximum differential input is 100 mV_{pp}, the actual inputs to the OTA only vary within a small range, i.e. within the linear input range of the OTA, due to the negative feedback configuration of the system. This structure alleviates the linearity requirement to the OTA design.

5.2.2 Circuit Model

In this design, a 1st order DSM is implemented. For the analysis of signal transfer function (STF) and noise transfer function (NTF) of the proposed circuit,

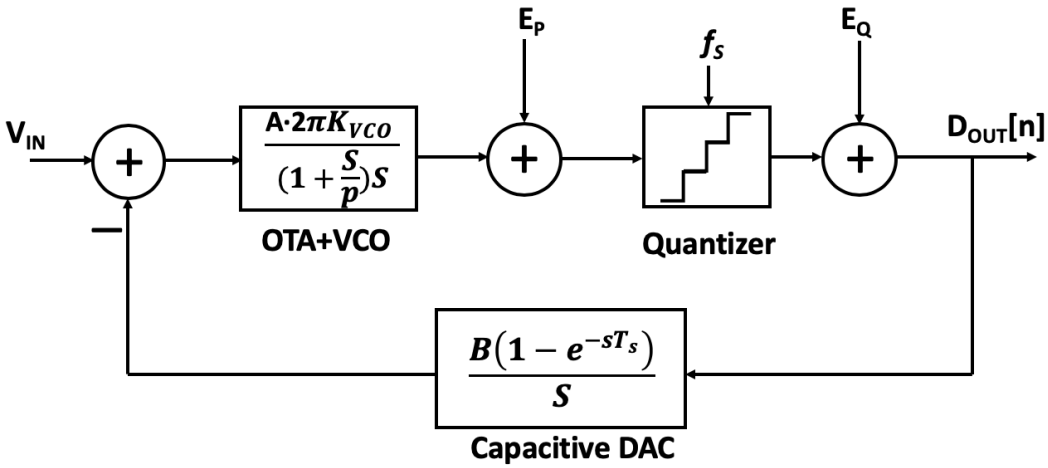

Fig. 44: Single-ended circuit model of the proposed design.

the single-ended circuit model is illustrated in Fig. 44. The OTA is modelled has a single pole LPF with a DC gain of A and pole p. The VCO, which generates output phase from input voltage, acts as an implicit integrator $\frac{2\pi K_{VCO}}{S}$ in the system because phase is the time integral of frequency in nature. Because both OTA and VCO operates in continuous-time (CT), their models are represented in s-domain as shown. Due to the non-ideality of VCO, distortion and noises from VCO itself will appear in its phase output as E_P. The phase quantization will also add another type of noise, namely quantization noise E_Q, to the final digital bit stream. The feedback capacitive DAC is modelled as a zero-order hold with a gain of B. Since the feedback circuit is merely capacitor deck, B is a constant denoting in volt/code.

The STF can be derived as

$$STF=\frac{2\pi AK_{VCO}}{\left(1+\frac{s}{p}\right)s+\frac{2\pi ABK_{VCO}(1-e^{-sT_s})}{s}} \quad (19)$$

The STF equation shows that the input signal is low-pass filtered before reaching the output. This equation also suggests that the signal bandwidth is defined by the OTA bandwidth. By designing OTA's bandwidth, the DSM's signal bandwidth is defined.

The NTF due to E_P is denoted as NTF1 and it is derived as

$$NTF1=\frac{1}{1+2\pi ABK_{VCO}\frac{(1-e^{-sT_s})}{s^2\left(1+\frac{s}{p}\right)}} \quad (20)$$

From equation (20), it is seen that the VCO noise and distortion E_P is be high pass filtered and 1st order shaped within the signal bandwidth.

Similarly, the NTF due to E_Q denoted as NTF2 is derived as

$$NTF2=\frac{1}{1+2\pi ABK_{VCO}\frac{(1-e^{-sT_s})}{s^2\left(1+\frac{s}{p}\right)}} \quad (21)$$

Equation (21) is identical to (20) because both noises are essentially appearing at the same node of the system. It shows that the quantization noise E_Q is also 1st order shaped within the signal band at the system output. Note that since the OTA and VCO blocks are CT in nature while the DAC is discrete-time (DT) in nature, the transfer function derivations involves CT-to-DT conversion [83].

The overall transfer function of the circuit model is therefore written as:

$$D_{out}[n]=V_{IN}\cdot STF+E_P\cdot NTF1+E_Q\cdot NTF2 \quad (22)$$

5.3 Circuit Block Implementation

5.3.1 Operational Transconductance Amplifier (OTA)

The schematic of the OTA is shown in Fig. 45. It consists of a replica bias circuit for the output common-mode regulation and a fully differential current-reused G_m-stage to provide large transconductance with low power consumption. The inverter-based differential input pair generates a large transconductance which approximates to $gm_{PM5,6}+gm_{NM5,6}$. Assuming that $gm_{PM5,6}=gm_{NM5,6}$ which can be achieved by adjusting the PMOS and NMOS sizing, this current-reused structure doubles the transconductance. With larger G_m transconductance, the noise contribution from the following stage can be effectively suppressed, leading to smaller input-referred noise.

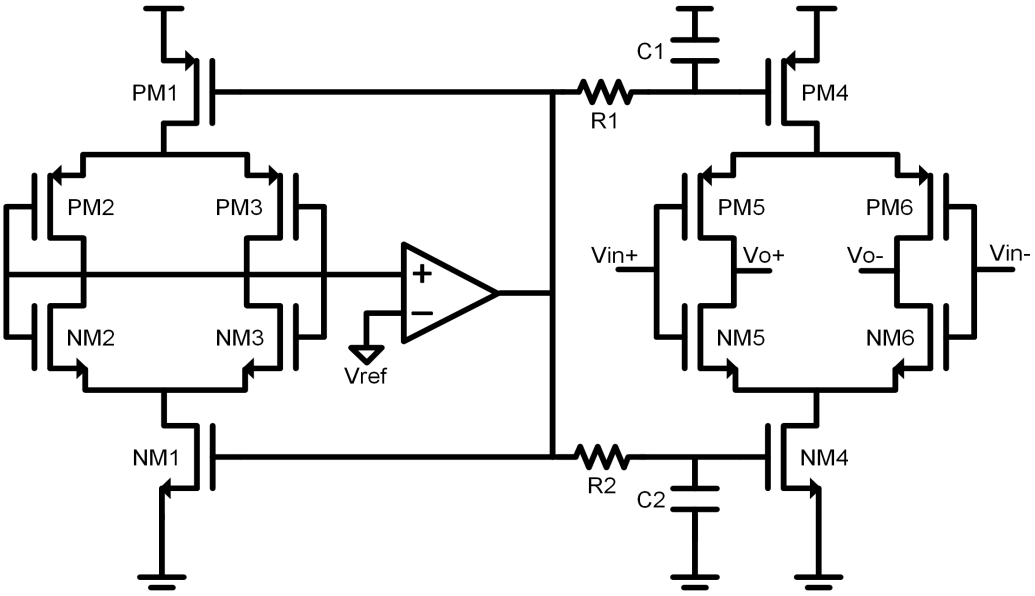

Fig. 45: Schematic of current-reused OTA.

5.3.2 Voltage-Controlled-Oscillator (VCO)

The differential outputs of the OTA function as differential control voltages V_{ctrl} of the next stage VCOs shown in Fig. 46. The VCO is implemented using current-starved ring oscillator structure. The current-starved structure is adopted for two reasons. Firstly, the current-starving transistor PM1 functions as a voltage-controlled-current-source, allowing it to control the ring oscillator's frequency by varying the current via adjusting the control voltage V_{ctrl}. Secondly, PM1 can also limit the current of the ring oscillator for power optimization. The VCO's free-running frequency is derived as

$$f_{VCO} = \frac{I_{VCO}}{NCV_{VCO}} \qquad (23)$$

where I_{VCO} is the oscillator current controlled by V_{ctrl}, N is the number of stages of ring oscillator, *C* is the load capacitance of each stage, and V_{VCO} is the local supply voltage of the ring oscillator. From (23), the K_{VCO} can be calculated as

$$K_{VCO} = \frac{\Delta f_{VCO}}{\Delta V_{ctrl}} = \frac{\Delta I_{VCO}}{NCV_{VCO}\Delta V_{ctrl}} = \frac{Gm_{VCO}}{NCV_{VCO}} \qquad (24)$$

where Gm_{VCO} is the transconductance of PM1 in Fig. 46. In this work, the VCO's free-running frequency and K_{VCO} are designed to be 1.5 MHz and 6.1 MHz/V

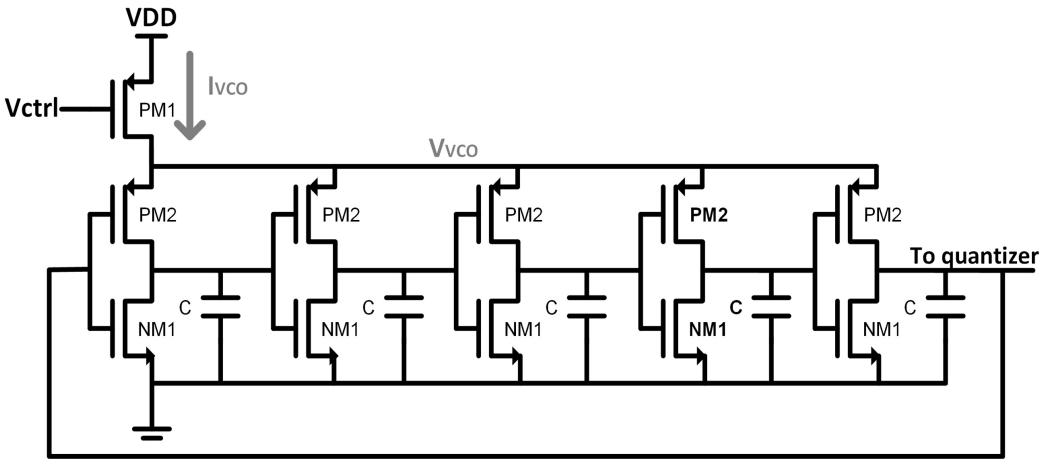

Fig. 46: Schematic of ring oscillator based VCO.

respectively. It should be noted that when the OTA voltage gain becomes excessively large, for a given input voltage change, the change in V_{ctrl} can be so large such that ΔI_{VCO} is no longer linearly proportional to $\Delta(V_{DD}-V_{ctrl})$, causing an adverse effect on the linearity of the system output. Therefore, the OTA voltage gain and the size of PM1 should be optimized carefully as a trade-off between the OTA input-referred noise and the circuit linearity. In this work, PM1 is sized to operate linearly within a range of $0.6V \le V_{ctrl} \le 0.8V$. The OTA's voltage gain is designed such that both outputs are well within the targeted V_{ctrl} range.

The VCO noise will add to the overall output noise. However, since the VCO used in this work produces rail-to-rail output, phase noise becomes the dominant noise generated by the VCO. The major contributors to phase noise is the VCO's 1/*f* noise and white noise. To suppress 1/*f* noise, bigger size inverter pairs is designed. A sufficiently high I_{VCO} is also chosen for noise suppression. The simulated phase noise plot of the VCO proposed is shown in Fig. 47. Within the -20 dB/dec region, at 100 kHz offset, the simulated phase noise is as low as -117 dBc/Hz. Within the -30 dB/dec region, at 1 kHz offset, the simulated phase noise is as low as -65 dBc/Hz.

To better examine the effect of VCO phase noise to the overall system noise performance, the VCO input-referred noise is computed from the phase noise shown in Fig. 47 using (25) derived in [32]:

$$S_{VIN}(f)=S_{\Phi}(f)\frac{f^2}{K_{VCO}^2} \qquad (25)$$

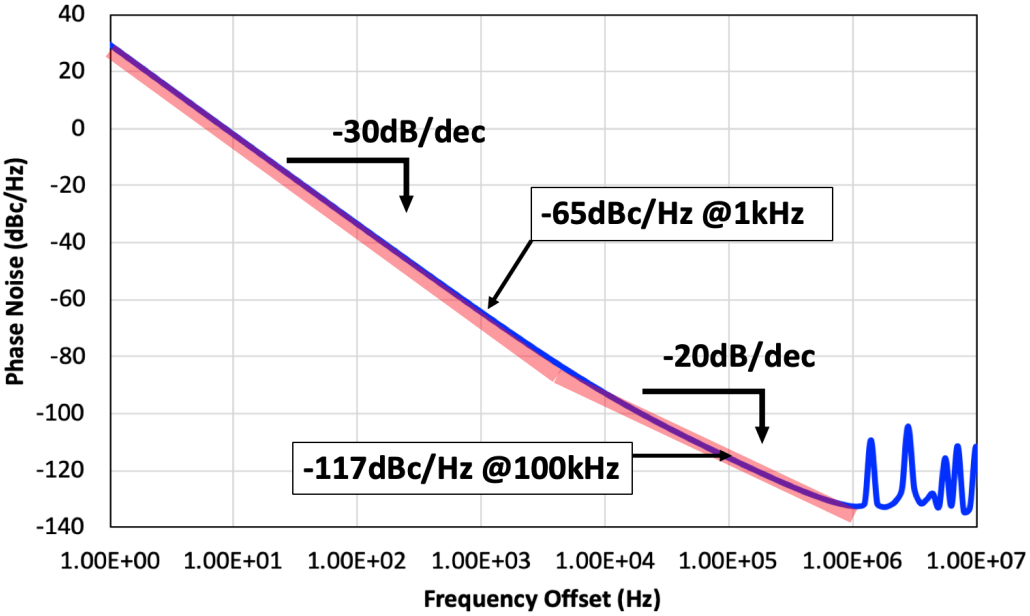

Fig. 47: Phase noise plot of VCO.

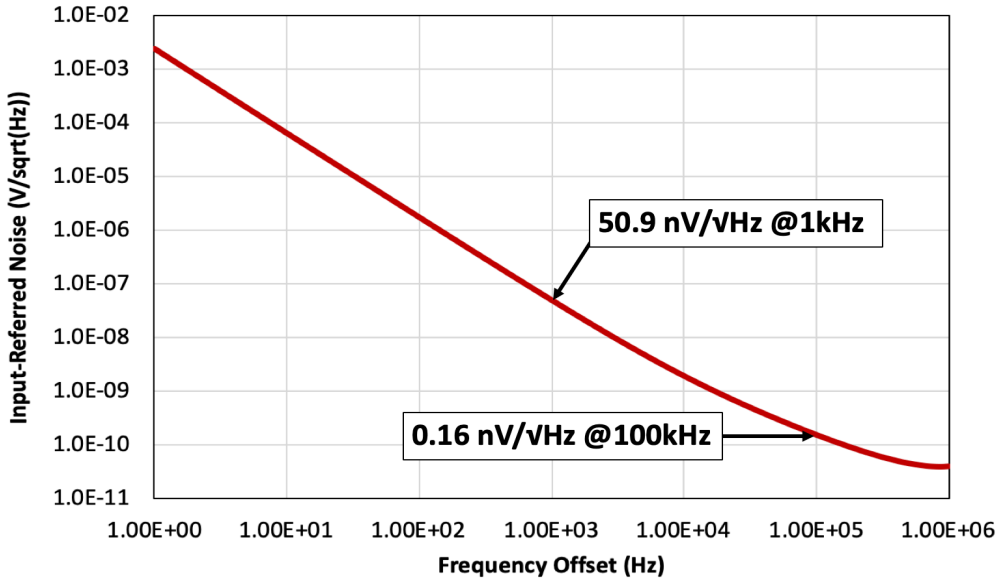

Fig. 48: Input-referred noise PSD of the VCO.

where $S_{VIN}(f)$ is the input-referred noise PSD of VCO, $S_{\Phi}(f)$ is the phase noise PSD. The $S_{VIN}(f)$ plot is given in Fig. 48. For an input signal of 1 kHz, the equivalent input-referred noise PSD of VCO is 50.9 nV/√Hz. As compared to the VCO in [32] with input-referred noise PSD of 64.7 nV/√Hz at 1 kHz, the proposed VCO achieves 13.8 nV/√Hz lower in the input-referred noise PSD. Together with the OTA, the VCO noise being referred back to the DSM input is further suppressed. This minimizes the effect of VCO phase noise on the overall noise performance.

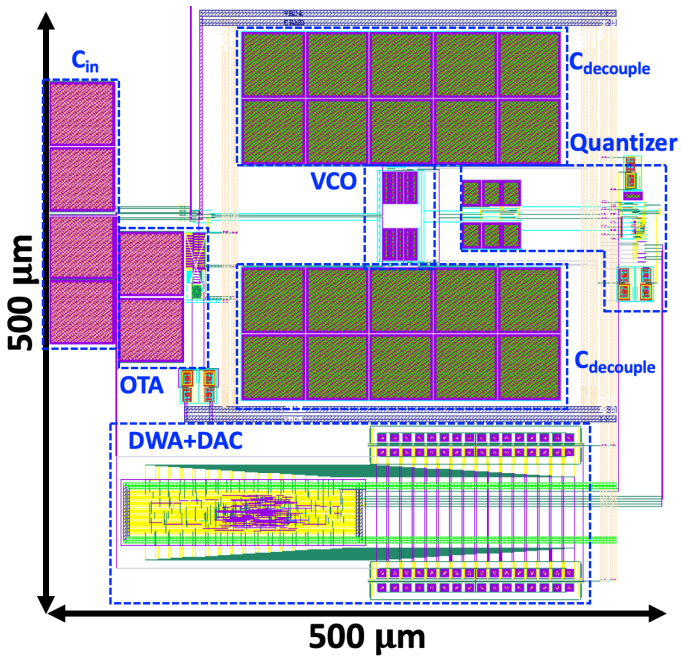

Fig. 49: Layout of CT-DSM.

The two VCOs convert the OTA's differential outputs into two phase-modulated (PM) square waveforms. These PM waveforms are integrated by the digital counters and their difference in phase is quantized into 5-bit digital output Dout [4:0]. Since the subtraction of input signals is purely performed in phase-domain, the DSM resolution is no longer limited by the supply voltage. A 5-bit quantizer is selected to boost the ENOB. Theoretically, quantizer with more bits improves the DAC feedback signal's resolution. However, in reality, the process mismatches among DAC capacitors form the fundamental limit to the feedback resolution. Therefore, a 5-bit counter is selected in this work. The 5-bit output is converted to two complimentary 32-bit thermo-codes, S[31:0] and S_n[31:0,] by the DWA logic with barrel-shifting. The thermo-code decides if DAC capacitors C_f[31:0] are connected to V_{refp} or V_{refn}. Barrel-shifting is employed to mitigate the mismatch from process variation among DAC capacitors.

5.4 Circuit Simulation Results

The proposed CT-DSM circuit has been designed and implemented in a commercial 40-nm CMOS process. Fig. 49 shows the chip layout; the chip active area is 0.25 mm^2. It draws a total current of 16.3 µA and a total power

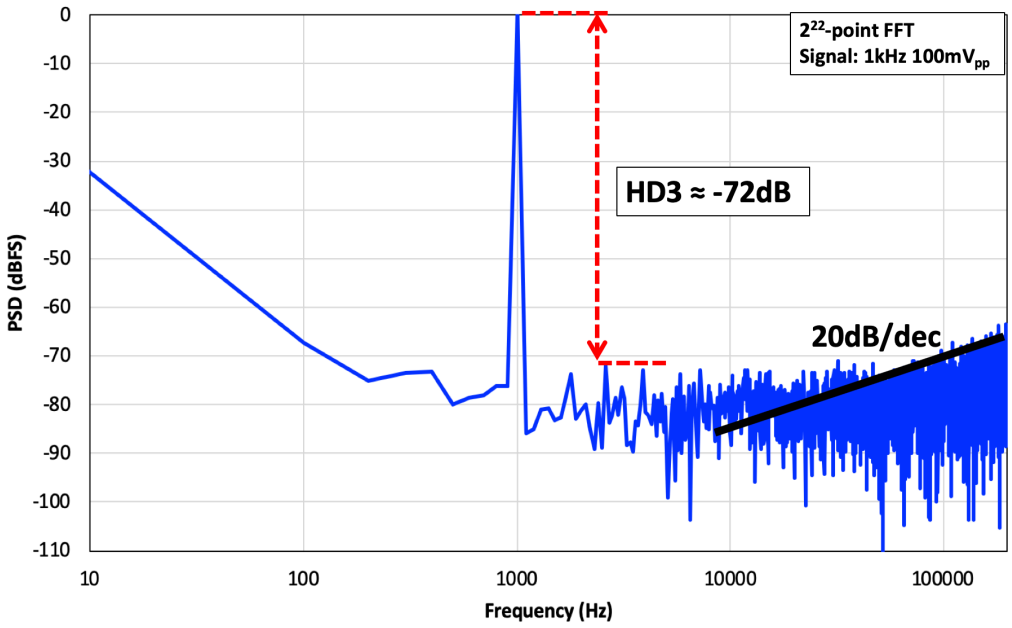

Fig. 50: Output PSD of DSM.

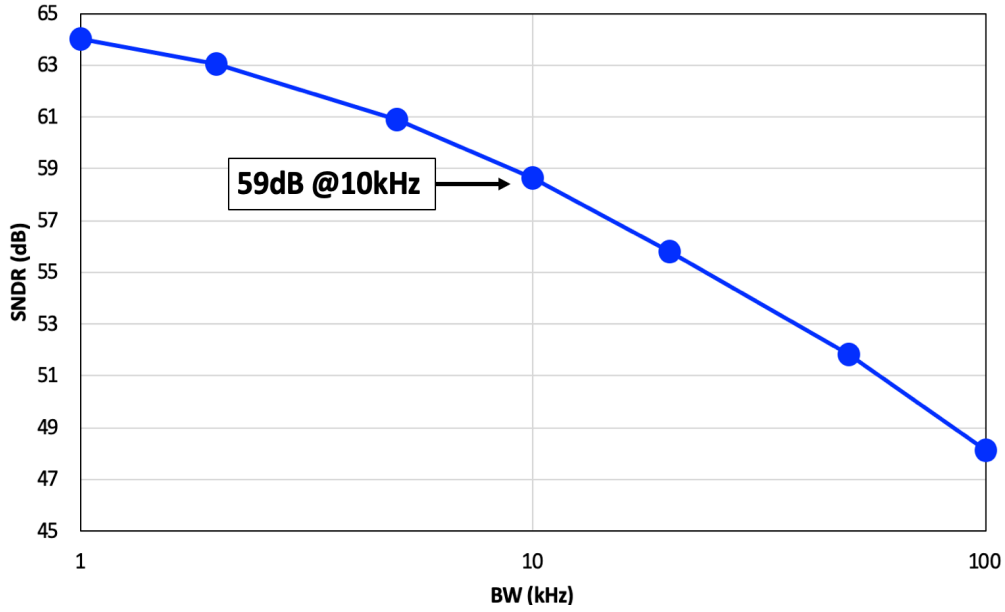

Fig. 51: SNDR versus bandwidth.

consumption of 19.5 μW under 1.2-V supply voltage.

Fig. 50 shows the spectrum of the CT-DSM output as a result of 2^{22}-point FFT with rectangular window. The circuit is simulated with following conditions. The common-mode voltage V_{cm} is 0.6 V and the fully differential sinusoidal input is of 1 kHz frequency with 100 mV_{pp} amplitude. The oversampling clock is chosen to be 6.2 MHz. It is observed that the quantization noise has been shaped away from the signal band to higher frequency as the result of first order

Table 3: Performance Comparison for 3rd Design

	This work	2017 [33]	2017 [34]	2017 [32]	2015 [85]	2014 [19]	2013 [84]	2012 [30]	2012 [18]
Technology (nm)	**40**	40	40	40	180	65	130	130	65
Topology	VCO-based DSM							IA+ADC	
Supply (V)	**1.2**	1.2	1.2	1.2	5/1.8	0.5	1	1.2	0.5
FSR (mV_{pp})	**100**	100	100	8	4μA	1	100	5	3.5
f_{sample}	**6.2 MHz**	1 MHz	3 kHz	4.2MHz	10 MHz	1 kHz	10 MHz	N.A.	20 kHz
BW	**10 kHz**	2 kHz	200	5 kHz	1.25	500	10 kHz	10 kHz	10 kHz
SNDR (dB)	**59**	74.9	74	61.85	73	N.A.	55.5	60.3	45
THD (dB)	**-70**	-82	-79	-70.8	N.A.	-52	N.A.	-80	-40
Power (μW)	**19.5**	21	7	17	340	2.3	125	68	5.04
FoMs (dB)	**147.1**	154.7	148.6	146.5	108.6	132.1	143.4	142	138
FoMw (pJ/conv)	**1.19**	1.16	4.27	1.68	37300	10.3	12.8	3.3	1.73

FoMs (dB) = SNDR + 10log(BW/Power)
FoMw (pJ/conv) = Power/(2BW×2^{ENOB})

noise shaping. The output PSD shows a distinct signal power at 1 kHz. The noise floor can be calculated by integrating the noise power over targeted bandwidth. Instead of the DSM output SNR, SNDR is used as a metric to evaluate the DSM performance because it includes both noise and distortion information, which is a more comprehensive performance evaluation. The SNDR over different bandwidth is computed and illustrated in Fig. 51. It is observed that SNDR improves with reduced bandwidth. Within 10 kHz bandwidth, the simulated SNDR of the proposed design is 59 dB. With a reduced bandwidth of 2 kHz, the SNDR improves to 63 dB.

The circuit overall performance is summarized in Table 3 and compared with other state-of-the-art VCO-based CT-DSM designs. As compared to traditional neural interface employing amplifier frontends [18] [30] whose maximum input range is 3.5mV and 5mV, respectively, the proposed design achieves much larger input signal range of 100mV, which reduces the chance of frontend being saturated under large input artifacts. Comparing to [34] [32] [33] [19] the proposed design obtained the highest BW with one of the highest input amplitudes and moderate SNDR. This demonstrates that the proposed design is able to operate with both high input range and high speed, while achieving good noise performance. The proposed design and work in [84] have similar

input range and bandwidth. However, the proposed design achieves 3.5-dB improvement in SNDR.

For multi-factor comparison, the general FoMs and FoMw equations are also adopted. The FoMs includes SNDR, BW and power information, which is used to evaluate system's in-band noise performance with corresponding power consumption. The FoMw includes power, BW and ENOB information, which is more often used to evaluate the system's energy efficiency. Comparing to [34], the proposed design attains about the same FoWs but 3 pJ/conv less FoMw, showing a higher energy efficiency while maintaining similar noise performance. Comparing to [32] [85] [19] [84], this design achieves the highest FoMs and the lowest FoMw, thanks to the careful noise consideration and highly-digital architecture.

5.5 Conclusion

In this chapter, a VCO-based delta-sigma modulator for bio-potential recording is presented. A system feedback loop consisting of DWA and capacitive DAC is employed to boost the input linear range. A current-reused OTA frontend is proposed to suppress the overall input-referred noise. A current-starving ring oscillator as VCO is proposed to realize the voltage-to-phase conversion. Under nominal supply voltage of 1.2 V, the proposed CT-DSM consumed 19.5 μW of power at a sampling frequency of 6.2 MHz. With 100-mV_{pp} input signal, it achieves SNDR of 59 dB within a wide bandwidth of 10 kHz. The corresponding FoMs is 147.1 dB and FoMw is 1.19 pJ/conv, demonstrating a good noise performance and energy efficiency comparing to prior arts.

The design has been sent out for fabrication in commercial CMOS foundry. The chip characterization results will be reported in our coming publications.

Chapter 6

Summary and Future Works

6.1 Summary

In this thesis, circuits for high-resolution sensor interface of wearable health monitoring are presented. The research focuses on two topics (1) relaxation oscillator frontends for time-domain sensor interface and (2) VCO-based DSM sensor interface. Three novel circuit structures have been presented. The novelty and advantages of each design are summarized as follows.

1) High FOM RC Relaxation Oscillator with Energy Efficient Swing Boosting

An RC oscillator with energy efficient swing boosting technique is proposed. Timing capacitors are stacked up during discharging phase to achieve high swing for low phase noise. Meanwhile, a novel energy efficient technique is proposed to largely improve the energy efficiency from the traditional swing boosting implementation. Implemented in 65-nm CMOS process, this 3.0 MHz oscillator consumes 17.3 μW under 1-V supply, achieving -112 dBc/Hz phase noise and 160.3 dBc/Hz FOM at 100-kHz offset frequency, which is very near to benchmark FOM of 162.1 dBc/Hz.

2) Delay-locked RC Oscillator with Voltage-to-Delay Feedback

A novel voltage-to-delay feedback (VDF) technique is proposed for frequency locking. This technique converts the frequency error due to circuit delay change into a counteracting comparator delay change, compensating the frequency error over cycles. Designed in 180-nm CMOS process. The frequency inaccuracy is as low as 23.4 ppm/°C over 0°C - 90°C and ±0.19%/V over 1.24 V – 1.5 V. This 1.6-MHz oscillator achieves -118.6 dBc/Hz phase noise at 100-kHz offset, which is the much lower than previous relaxation oscillators with

feedback circuit [47] [51].

3) Wide Input Range Wide Bandwidth VCO-based CT-DSM Bio-Signal Recording Interface

A VCO-based DSM is proposed for direct conversion of input bio-potential signal to output digital code without preceding amplifier stage. A feedback architecture is proposed to increase the input linear range of the system up to 100 mV_{pp}. The input bandwidth is also widened to 10 kHz by employ the OTA frontend. Implemented in 65-nm CMOS process. The reported SNDR is 59 dB (at BW=10 kHz) with FOMs of 147.1 dB and FOMw of 1.19 pJ/cycle. This topic is still being studied and will be further developed for performance improvement and integration with sensor.

6.2 Future Works

The current and future research focuses are described as below.

1) To integrate the relaxation oscillators with physical sensors to form a complete sensor system.

The first topic targets to complete the sensor interface system by integrating proposed current relaxation oscillator with real sensors and data-processing digital backend. Examples such as [16] [6] are the goal for this task. To achieve this goal, sensors will be chosen, and digital blocks will be added for output bitstream generation. At system level, innovation in new system architecture will be conducted. Notice that in [16], two identical relaxation oscillators are employed, with one generating the reference clock and the other converting sensor output into corresponding frequency. This almost doubles the power consumption as compared to if there is only one relaxation oscillator. This problem shall be addressed in future research.

2) To continue research on the VCO-based DSM for bio-signal recording.

This forms another important future research task since the VCO-based DSM has demonstrated high suitability for bio-signal recording interface applications and has generated promising results in many existing designs. The design proposed in this thesis shall continue to be improved so as to accommodate larger input range and to achieve better SNDR and power

performances. To further improve the input range, one direct approach is to optimize the current OTA block for higher linearity. As reported in [80], which adopts similar 1st-stage OTA block and 5-bit feedback circuit as the proposed design in chapter 5, the input range can be boosted to 360 mV_{pp}. This shows the potential of circuit optimization in improving the input range. Another approach is to utilize the bulk-driven architecture for OTA. Due to the lower bulk transconductance as compared to the gate transconductance, the bulk driven differential OTAs are able to handle larger input range while maintaining linearity. Such OTA designs [86] [87] [88] demonstrate potential to be implemented as the frontend of bio-signal recording interface. Meanwhile, there is no compensation or technique proposed to minimize the low frequency noises, such as flicker noise, in the current proposed design. This results in high noise floor at low frequency region which degrades the SNDR. To solve this problem, choppers will be implemented in the next version of the design. Also, a better common-mode feedback circuit will be employed to minimize the impact of possible bias drift which can contribute to the output distortion. Furthermore, the power consumption of the current design can be reduced by adopting low-voltage low-power amplifiers such as the one proposed in [89] which has excellent power performance. Moreover, innovations on the phase quantizer, such as the low-power phase extended quantizer in [90] and double noise shaping quantizer in [91], will be conducted to further improve the FoMs and FoMw performances. Other than making improvement on circuit block level, the system level innovation such as higher order VCO-based DSM for higher SNDR [92] will also be emphasized in our future research.

3) To further explore relaxation oscillator design for on-chip reference application.

It is natural to extend the application of relaxation oscillator from sensor interface to general on-chip clock reference due to its capability in generating stable frequency under noise, supply and temperature fluctuations. While many techniques have been proposed to reduce the impact of noise and supply on the output frequency, the higher order temperature dependence of passive resistor is still the major contributor to the frequency inaccuracy over temperature changes. Therefore, the future research focus will involve the

compensation of resistor's temperature dependence. This has been an emerging trend in the field of relaxation oscillator research and some recent works such as [63] [64] have already been reported with promising results. In [63], a voltage ratio adjusting technique is proposed to compensate up to 2nd order temperature dependence, while in [64], the digital compensation method is adopted to improve the overall frequency accuracy over temperature variations. Both works achieve benchmarked frequency accuracy over temperature variations, allowing them to operate within wide temperature range which is essential for on-chip clock reference. Our existing designs only employ 1st order temperature compensated timing resistors, whose resistances still vary with temperature due to higher order temperature dependent terms. Therefore, this problem shall also be addressed in the future work.

In conclusion, there are plenty of rooms to further improve the sensor interface circuit performance, from circuit block level to the system architecture level. The journey of research on various sensor interface circuits design shall be continued.

Author's Publications

(1) W. Zhou, W. L. Goh, J. H. Cheong and Y. Gao, "A 16.6 μW 3.12 MHz RC Relaxation Oscillator with 160.3 dBc/Hz FOM," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-5.

(2) W. Zhou, W. L. Goh and Y. Gao, "Integrated Temperature Sensor with CMOS Relaxation Oscillator Based Sensor Interface for Biomedical Sensing," *2019 Electron Devices Technology and Manufacturing Conference (EDTM)*, Singapore, Singapore, 2019, pp. 416-418.

(3) W. Zhou, W. L. Goh and Y. Gao, "A 1.6MHz Swing-Boosted Relaxation Oscillator with ±0.15%/V 23.4ppm/°C Frequency Inaccuracy using Voltage-to-Delay Feedback," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-4.

(4) W. Zhou, W. L. Goh and Y. Gao, "A 100-mV_{pp} Input Range 10-kHz BW VCO-based CT-DSM Neuro-Recording IC in 40-nm CMOS," *2019 32nd IEEE International System-on-Chip Conference (SOCC)*, Singapore, Accepted for conference on September 3-6, 2019.

(5) W. Zhou, W. L. Goh Y. Gao, "A 3-MHz 17.3-μW 0.015% Period Jitter Relaxation Oscillator with Energy Efficient Swing Boosting", *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, in minor revision.

(6) W. Zhou, W. L. Goh, and Y. Gao, "A 1.6 MHz Swing Boosted Relaxation Oscillator with Voltage-to-Delay Feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, to be submitted by Aug 2019.

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