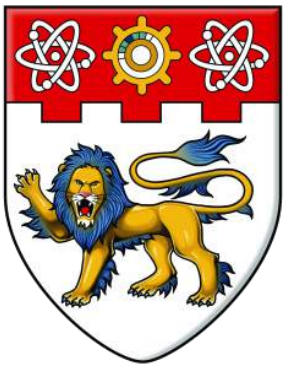

NANYANG TECHNOLOGICAL UNIVERSITY

# ELECTROMIGRATION STUDY OF COPPER INTERCONNECTS WITH SIDE RESERVOIR DESIGN

**HENDRO MARIO**

**School of Materials Science and Engineering**

**2016**

# ELECTROMIGRATION STUDY OF COPPER INTERCONNECTS WITH SIDE RESERVOIR DESIGN

School of Materials Science and Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Master of Engineering

**2016**

## Abstract

Reliability issues in copper interconnect/low-k dielectric system, namely electromigration and TDDB (Time Dependent Dielectric Breakdown), have become more crucial as the dimensions of the copper interconnect structures keep shrinking with the technology node. In this project, a new method to mitigate the effects of electromigration of copper interconnect is being proposed. Many researchers had tried to improve the lifetime of the copper interconnect when it undergoes electromigration test, such as introduction of end of line metal reservoir, or improving the capping layer of the copper interconnects. However, no matter how robust the fabrication process of the copper interconnects is, there is always a possibility of a defect or pre-existing void present in the metal interconnects. Fatal voids that are found near the end of cathode vias are the cause of electromigration failures, and recent *in-situ* electromigration tests have revealed that the voids can drift towards the end of cathode vias, instead of nucleating there.

The motivation of this project is to improve the lifetime of copper interconnects in the knowledge that pre-existing voids exist, and when subjected to electrical stressing, could lead to earlier failures due to electromigration. An unique design of a side metal reservoir is being introduced in the project, which is hypothesized to be capable of enhancing the lifetime of the copper interconnects under the proposed electromigration mechanism.

The modeling and simulation done in this study suggest that the distance from the cathode end of the interconnect, $L_{crit}$, is important when it comes to the location of where the pre-existing void was nucleated or pinned. When the pre-existing void is nucleated or pinned at the distance smaller than $L_{crit}$, there would not be any new void nucleation at the end of cathode via due to the change in the stress evolution along the metal interconnect.

The newly designed side metal reservoir was studied to check its impact towards the lifetime of the metal interconnect under electromigration test. The end of line metal reservoir was used as the reference in this study. It is observed that the side reservoir design is able to enhance the lifetime of the copper interconnect as hypothesized. The effectiveness of various length of the side metal reservoir was investigated as well. From the experiments, it was found that there is a limit on how far the side metal reservoir can extend before losing its effectiveness of trapping the pre-existing voids.

Finally, attempts on *in-situ* electromigration experiment on the side metal reservoir were done. However, it proved to be a challenge due to the lack of a high temperature heater to accelerate the stressing during the *in-situ* electromigration testing.

## Acknowledgements

First and foremost, I would like to thank God, Jesus Christ, for His kindness and faithfulness throughout the entire journey of the study. Without the help and strength from Him, it would be impossible to complete this thesis.

I would like to express my humble gratitude to my supervisor, Associate Professor Gan Chee Lip, for his patience and guidance so that I can complete this thesis. In time of difficulties and challenges, he will always keep his calmness and confront me with his knowledge and suggestion. I am truly grateful for having such a wonderful supervisor like him.

I would also like to thank the members of the Prof Gan's lab for the valuable time spent together throughout the entire study and the assistance provided along the way, especially to Wardhana, Riko, Wahyu, Eric Tan, Meng Keong, Liu Qing and Shu Rong, and for others whose name not mentioned here.

I am also thankful to GLOBALFOUNDARIES SINGAPORE for the financial support in term of scholarship, to the collaborator from A*Star SimTech for lending me the wafer dicing and gold wire bonder so I can complete my experiment.

Lastly, I want to express my heartfelt gratitude to my lovely wife, Imelda, my parents, and siblings for their continuous support and love, so that I can complete my degree.

# Table of Contents

# Table Captions

## Figure Captions

## Abbreviations

| | |
|---|---|
| Al | Aluminum |
| Cap | capping |
| CMP | Chemical Mechanical Polishing |
| Cu | Copper |
| cm | centimeter |
| FIB | Focus Ion Beam |
| hrs | hours |
| IC | Integrated Circuit |
| IMD | Inter Metal Dielectric |
| m | meter |
| M1 | metal one |
| M2 | metal two |
| M3 | metal three |
| nm | nanometer |
| Pt | Platinum |
| RC | Resistance Capacitance |
| RIE | Reactive Ion Etching |
| s | second |
| SEM | Scanning Electron Microscopy |
| SiCOH | Hydrogenated Silicon Oxycarbide |
| SiN | Silicon Nitride |
| SiCN | Silicon Carbon Nitride |
| Ta | Tantalum |
| TaN | Tantalum Nitride |
| TDDB | Time Dependent Dielectric Breakdown |
| TEM | Transmission Electron Microscopy |
| µm | micrometer |
| V1 | via one |
| V2 | via two |

# Chapter 1

# Introduction

*In this chapter, the background of the project will be elaborated; follow with the basic concept of electromigration and the problem associated with it. The objectives and scope of the project will be stated as well. In addition, a short dissertation overview of the project will be presented. Finally, it highlights the findings and novelty of the project.*

## 1.1 Background

The Moore's Law of doubling the device's speed every 18 months has resulted in the continuous miniaturization of the integrated circuits (ICs) and enabled multiple function integration. This has increased the density of interconnects needed as well as the power dissipation. Thus, an increase in the overall temperature in the ICs has been observed. The smallest technology node on today's integrated circuits (ICs) is 14 nm and below. The international technology roadmap for semiconductors (ITRS) projects that in the future years, the smallest technology node will be even smaller than 10 nm [1]. New materials have been introduced into the industry during the scaling of the technology node down to 90 nm. This is to cope with the performance requirements as part of scaling down the technology node. In the Back End of Line (BEOL) processes, the norm of the process stage starting from the lowest metal interconnect up to the last metal bond pad process, two main materials are being replaced, the aluminium metal interconnects are replaced by copper (for its lower resistivity), and the dielectric oxides by the so called low-*k* material (for its lower dielectric constant). Figure 1.1 [2] shows the cross section of the CMOS090 IC with the copper and low-*k* materials indicated. Despite all the advantages of copper and low-*k* material, the implementation of these materials has severe implications on the structural integrity of the ICs interconnects as well, namely reliability issues such as electromigration and TDDB (Time Dependent Dielectric Breakdown) [3, 4].

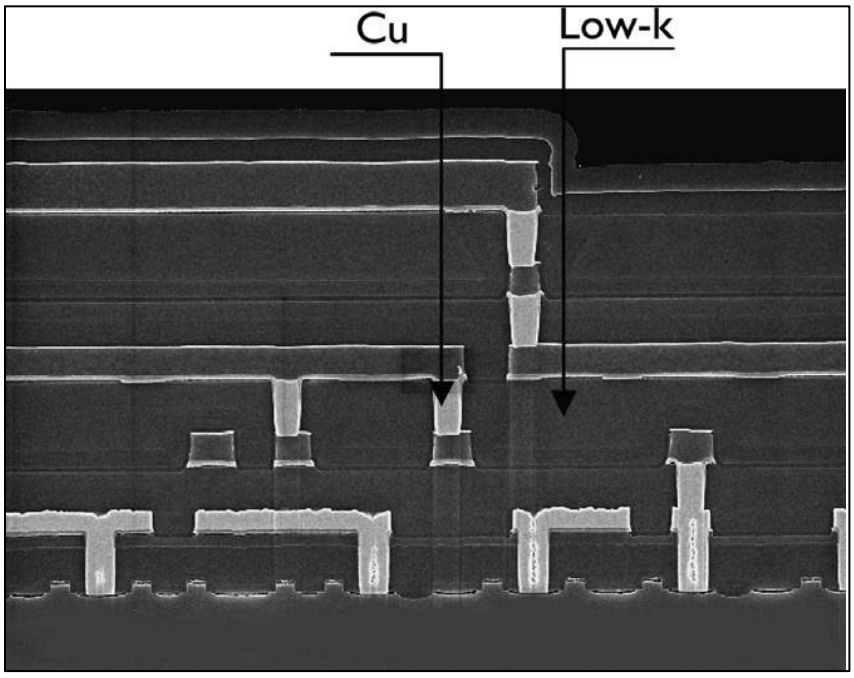


**Figure 1.1** Cross section view of the CMOS090 IC [2].

The electrical signal's speed in an IC is governed by both the switching time of a transistor (gate delay) and the signal propagation time through the interconnect lines (interconnects RC delay). The gate delay is being improved by shrinking the device gate lengths, implementing the strain technology and introducing new materials. On the other hand, the work on improving the interconnect delay (i.e. reducing the line resistance and parasitic capacitance) becomes a more challenging task due to the scaling of interconnect cross sectional area, which translates into increasing the line resistance and line-to-line capacitance, as well as increasing crosstalk noise between parallel lines. This is further illustrated in Figure 1.2, whereby the interconnect delay becomes the major dominant factor contributing to the circuit delay as the technology node goes to a smaller feature sizes [5]. In addition, the metal lines have to withstand electromigration issues since the current density is higher when the cross sectional area is scaled down. It has to withstand the stress migration issues as well due to the temperature stressing during the process fabrication. The integration of low-*k* materials with copper technology also leads to another reliability problem, TDDB. Therefore, the reliability issues on the interconnects system must be well understood in order to cope with the pace of technology scaling. In

this project, it will be focused on the electromigration reliability issue rather than stress migration or TDDB.

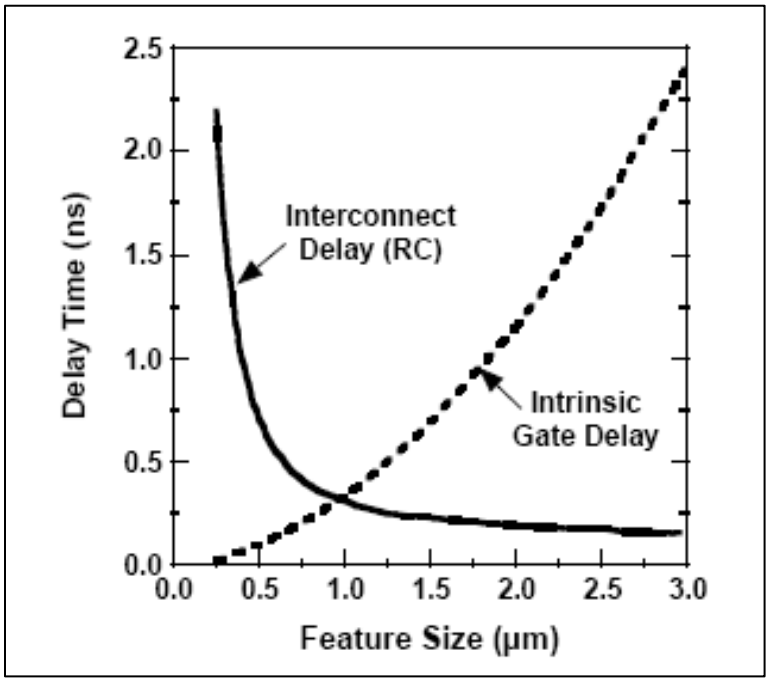


**Figure 1.2** Interconnect delay dominates over gate delay as the feature size decreases [5].

## 1.2 Electromigration

The term electromigration refers to the process of electric-current-induced self-diffusion in the interconnect line. Electromigration occurs when there is a momentum transfer from electrons to the metal atoms during scattering events when the electrons flow in the presence of an electric field (Figure 1.3).

This momentum transfer generates gradual movement of the metal atoms in the direction of electrons flow, that is, towards the end of the interconnect that has higher electric potential (anode). The vacancies, created out of the diffusion or displacement of the metal atoms, will move in the direction opposite to that of the metal atoms, that is, towards the end of the interconnect that has lower electric potential (cathode).

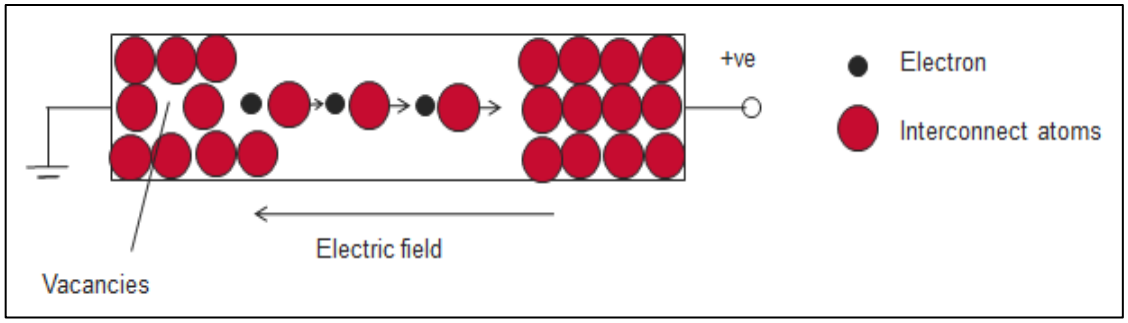


**Figure 1.3** Electromigration in the interconnect line.

At the cathode side, voids will form after some time when the vacancies coalesce with each other. On the other hand, at the anode side, hillocks will form as a resultant of metal accumulation. Figure 1.4, shows the hillock at the anode side, whereas voids at the cathode side. Electromigration failure happens when the void spans over the cross-section of the interconnect, which will cause an open circuit failure behavior, or when hillocks touches adjacent interconnect that causes electrical short-circuit failure behavior.

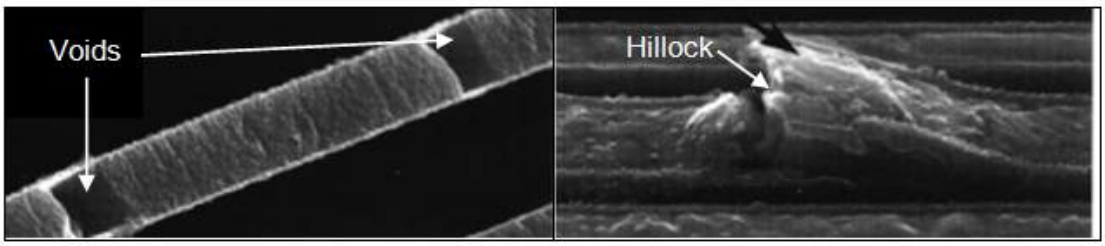


**Figure 1.4** SEM images of voids and hillock caused by electromigration [6].

There are various pathways for atomic diffusion to occur, which are surfaces of interconnect, grain boundaries, and vacancies in crystal grains. Generally, the diffusion along the surface is the fastest, followed by diffusion through grain boundaries, and lastly, diffusion through crystal grains. This is because, generally, the value of the activation energy for surface diffusion is the lowest comparing to the other pathways of diffusion. However, different materials will give different activation energies for the various modes of diffusion. Therefore for the case of aluminum, surface diffusion may not be the fastest diffusion pathway [7]. On the other hand, for copper the fastest diffusion pathway is still along the surface of the material.

In the overall mass transport in the interconnect, beside momentum transfer from electrons to metal atoms, stress gradient contributes as well to the mass transport, but in the opposite direction of the electron flow or electron wind force [7]. Electromigration will lead to a tensile stress on the cathode side and compressive stress on the anode side, which causes a stress gradient along the interconnect line [7, 8]. This stress gradient is commonly known as back-stress, since it will provide a force for migration of the metal atoms from the compressive stressed anode back to the tensile stressed cathode. Hence, the total net atomic flux ($J_a$) in an interconnect line when electromigration occurs is shown as follows [8, 9]

$$J_a = \frac{DC}{kT}\left(Z^* q\rho j - \Omega\frac{\partial\sigma}{\partial x}\right) \qquad (1.1)$$

where $D$ is atomic diffusivity, $C$ is concentration of atoms, $k$ is Boltzmann's constant, $T$ is temperature, $Z^*$ is effective charge number or effective valence, $q$ is elementary charge, $\rho$ is resistivity of interconnect, $J$ is current density applied to the interconnect, $\Omega$ is atomic volume, $\sigma$ is hydrostatic stress, $x$ is the length of the interconnect. Equation 1.1 can be simplified to give the atomic flux induced by electron wind force ($J_1$) and back-stress ($J_2$) as [8]

$$J_1 = \frac{DC}{kT}\cdot Z^* q\rho j \qquad (1.2)$$

$$J_2 = -\frac{DC}{kT}\cdot\Omega\frac{\partial\sigma}{\partial x} \qquad (1.3)$$

The negative sign in front of the atomic flux expression in equation 1.3 signifies that the direction of mass transport by back-stress is opposite to that of electron wind force (Figure 1.5).

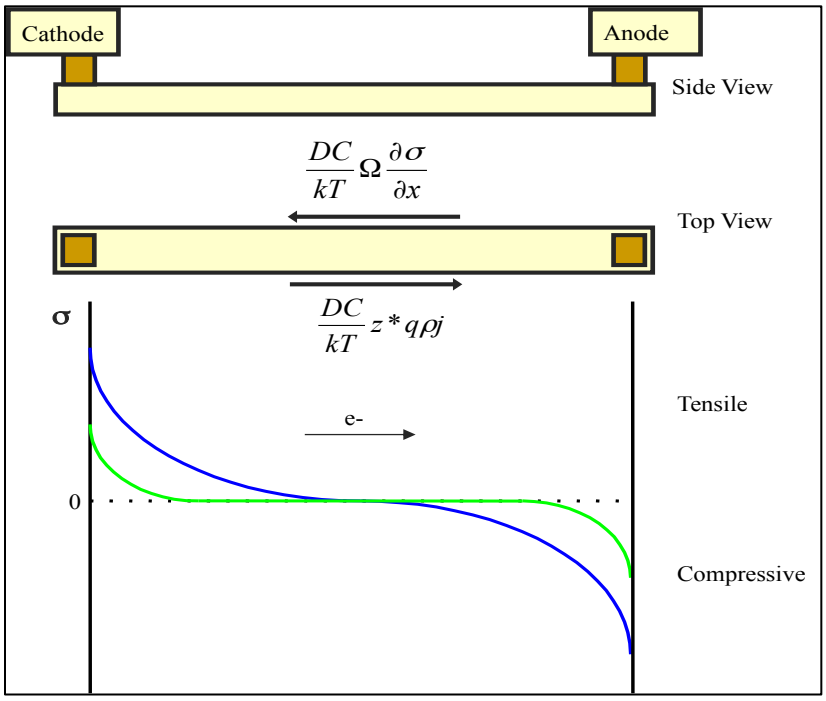


**Figure 1.5** Total atomic flux acting on the interconnect line.

Current density and temperature affect the electromigration behavior in the interconnect line. A larger current density will result in a larger atomic flux induced by the electron wind force ($J_1$). Higher temperatures will make the lifetime of the interconnect line lower since it increases the rate of atomic diffusion since D, atomic diffusivity, in equation 1.1 is a temperature dependent variable given by [8],

$$D = D_o \exp\left(-\frac{E_a}{kT}\right) \qquad (1.4)$$

where $D_0$ is a temperature independent constant, $E_a$ is the activation energy for diffusion, $k$ is Boltzmann's constant and $T$ is temperature.

An interconnect can be immortal (i.e. does not fail) even though it may be susceptible to a minor electromigration when the generated back-stress balances the electron wind force, resulting in a zero net atomic flux. Rearranging equation 1.1 in order to get the critical threshold condition for immortality condition,

$$\frac{DC}{kT}\left(Z^*q\rho j - \Omega\frac{\partial\sigma}{\partial x}\right) = 0$$

$$Z^* q\rho j = \Omega \cdot \frac{\Delta\sigma}{\Delta L}$$

$$(jL)_{crit} = \frac{\Omega \cdot \Delta\sigma}{Z^* q\rho} \qquad (1.5)$$

Where $(jL)_{crit}$ is the critical threshold product of current density, $j$, and interconnect length, L, for which the net atomic flux is zero, and $\Delta\sigma$ is the hydrostatic stress difference between anode and cathode.

Research done on the both aluminium and copper interconnect line have shown that the critical threshold product is dependent on temperature [9, 11, 12]. It was found that with increasing temperature, the numerical value of critical threshold product decreases. Thus, an interconnect can fail when the temperature is increasing, even though at low temperature it exhibits the immortal condition.

## 1.3 Problem Statement

The issue of electromigration on metal interconnects has been widely known and studied for many years. Many attempts and research had been done in trying to improve the lifetime of the metal interconnects under electromigration test. The improvements are mainly due to a change in the fabrication process, the material used, or the design of the metal interconnects.

To date, the issue of impact of pre-existing voids on electromigration, instead of void nucleation at the end of cathode vias, has become more crucial due to its severity of reducing the electromigration lifetime of the metal interconnects.

In this project, a new design of the side metal reservoir interconnect would be introduced, with the aim to improve the lifetime of the metal interconnects in view of the pre-existing voids issue. The commonly used end of line metal reservoir interconnect design would be used as a comparison.

## 1.4 Objectives and Scope

The objectives of this study is to develop and investigate a novel design of metal side reservoir interconnect test structure with the aim to enhance its lifetime under electromigration reliability test in view of the presence of pre-existing voids. Its design limitation with respect to its effectiveness on improving the lifetime of the copper metal interconnects will be studied as well.

The scope for the project would be on the electromigration study. The material of the metal interconnects would be copper. The samples were obtained from the industrial partner and fabricated according to the company's processes.

## 1.5 Dissertation Overview

The thesis reports the impact of the pre-existing void through modeling, simulation and experiments. The role of the side metal reservoir as a unique design in conjunction with pre-existing voids will be reported in detail.

Briefly, Chapter 1 introduces the topic of the project as well as introducing the basics on electromigration.

Chapter 2 focuses on a detailed literature review of relevant topics on copper interconnect, impacts of interconnect trees, end-of-line reservoir structure, copper/cap interface influence and pre-existing voids issue. This chapter provides the foundation and understanding leading to the methodology and strategies that are being used in the study.

Chapter 3 describes the experimental setup and methods carried out for this study.

Chapter 4 presents the results and discussion obtained from the experiments performed in this study. The first section of this chapter describes the modeling and simulation done on pre-existing void cases. Subsequently, studies on the effect of side metal reservoir

interconnect structure. And follows by the design constraint or limitation on how much the side metal reservoir interconnects can be extended. Lastly, attempts on *in-situ* electromigration on the side metal reservoirs will be discussed.

Finally, a conclusion of the studies and recommended future works are given in Chapter 5.

## 1.6 Findings and Outcomes/Originality

The introduction of the novel side metal reservoir structure has been studied and it is able to improve the lifetime of the copper metal interconnects by acting as a void trap for the pre-existing voids. Thus, it increases the reliability of the overall metal interconnects in the IC chip. The length effectiveness of side metal reservoir is also studied and should be taken into consideration for future designs.

**References:**

[1] International Technology Roadmap for Semiconductors (ITRS): Interconnect, Edition. **2013**, Available from: http://www.itrs.net/

[2] W. D. van Driel. *Microelectronics Reliability*. **2007**, 47(12), 1969-1974.

[3] E. T. Ogawa. *IEEE Transactions on Reliability*. **2003**, 51(4), 403-419.

[4] J. R. Lloyd, M. R. Lane, X. -H. Liu, E. Liniger, T. M. Shaw, C. -K. Hu, R. Rosenberg. *Microelectronics Reliability*. **2004,** 44(11), 1835-1841.

[5] A. L. S. Loke. *Ph.D. thesis, Stanford University.* **1999**.

[6] L. Arnaud, G. Tartavel, T. Berger, D. Mariolle, Y. Gobil, I. Touet. *Microelectronics Reliability.* **2000,** 40, 77-86.

[7] J. R. Lloyd. *Semicond. Sci. Technol.* **1997,** 2, 1177-1185.

[8] I. A. Blech and C. Herring. *Appl. Phys. Lett.* **1976,** 29, 131-133.

[9] A. G. Sabnis. *VLSI Reliability (VLSI Electronics Microstructure Science)*. **1990,** 22.

[10] P. C. Wang and R. G. Filippi. *Appl. Phys. Lett.* **2001,** 78 (23), 3598-3600.

[11] I. A. Blech. *J. Appl. Phys.* **1976,** 47, 1203-1208.

[12] R. Frankovic and G. H. Bernstein. *J. Appl. Phys.* **1997,** 81, 1604-1605.

# Chapter 2

# Literature Review

*Chapter 2 presents a literature review of the topics that are important to the build up of the foundation of this study, which are the introduction of copper as metal interconnect, electromigration on copper interconnect, impact of interconnect trees on electromigration in copper interconnect, the introduction of end-of-line reservoir, the influence of copper/cap interface and lastly, the pre-existing voids on copper electromigration.*

## 2.1 The Introduction of Copper as Metal Interconnect

Aluminium (Al) as the early generation of interconnect material has been replaced by copper (Cu), since the properties offer by copper are much superior as compared to aluminium. The comparisons of the properties for aluminum and copper are presented in the table 2.1. Since the value of the copper resistance is lower than aluminium, it is expected to give a better RC delay performance. The lower $D_0$ (temperature independent material constant) and $Q_d$ (Energy activation) value of copper also means that it is expected to resist against electromigration effects much better as compared to the aluminium interconnect, since a lower $D_0$ and higher $Q_d$ value implies a slower diffusion of the copper metal based on equation 1.4.

Note that the $D_0$ value shown in Table 2.1 represents the case of self-diffusion, although the actual diffusion path in the Al and Cu may be different during electromigration. For polycrystalline Al, atoms prefer to diffuse along the grain boundaries due to its lowest $E_a$ (0.6 – 0.7 eV) as compared to bulk (1.2 – 1.4 eV) [2]. Whereas for Cu, the surface or interface is preferred as the diffusion path as compared to grain boundary or bulk due to its lowest $E_a$ [13].

**Table 2.1** Electrical resistivity, $D_o$ and $Q_d$ of Aluminium and Copper [1].

| Material | Electrical Resistivity | $D_o$ | $Q_d$ |
|---|---|---|---|
| Aluminium | $2.65 \times 10^{-8}$ Ω-m | $2.3 \times 10^{-4}$ $m^2/s$ | 200 (kJ/mol) |
| Copper | $1.73 \times 10^{-8}$ Ω-m | $7.8 \times 10^{-5}$ $m^2/s$ | 144 (kJ/mol) |

The conventional technique of aluminium interconnect fabrication by subtractive metal reactive ion etch (RIE), which the deposited metal on top of a planar surface being patterned and removed by RIE, then followed with the gapfill intermetal dielectric (IMD) deposition and a planarization by chemical mechanical polishing (CMP), is not suitable for copper metal. This is due to its poor dry etching characteristics. Therefore, the damascene technique is being used for copper during the metal interconnect fabrication. The damascene technique, as being described in Figure 2.1, begins with the deposition of the IMD then followed by patterning by RIE, deposition of barrier and copper liner, then

copper plating. Lastly, the excess copper metal is being planarized by CMP and capped by another layer of IMD. For the damascene process, it can be either single or dual damascene. For dual damascene, it includes the fabrication of the metal line with the vias below, which is the connection path between two different metal layers.

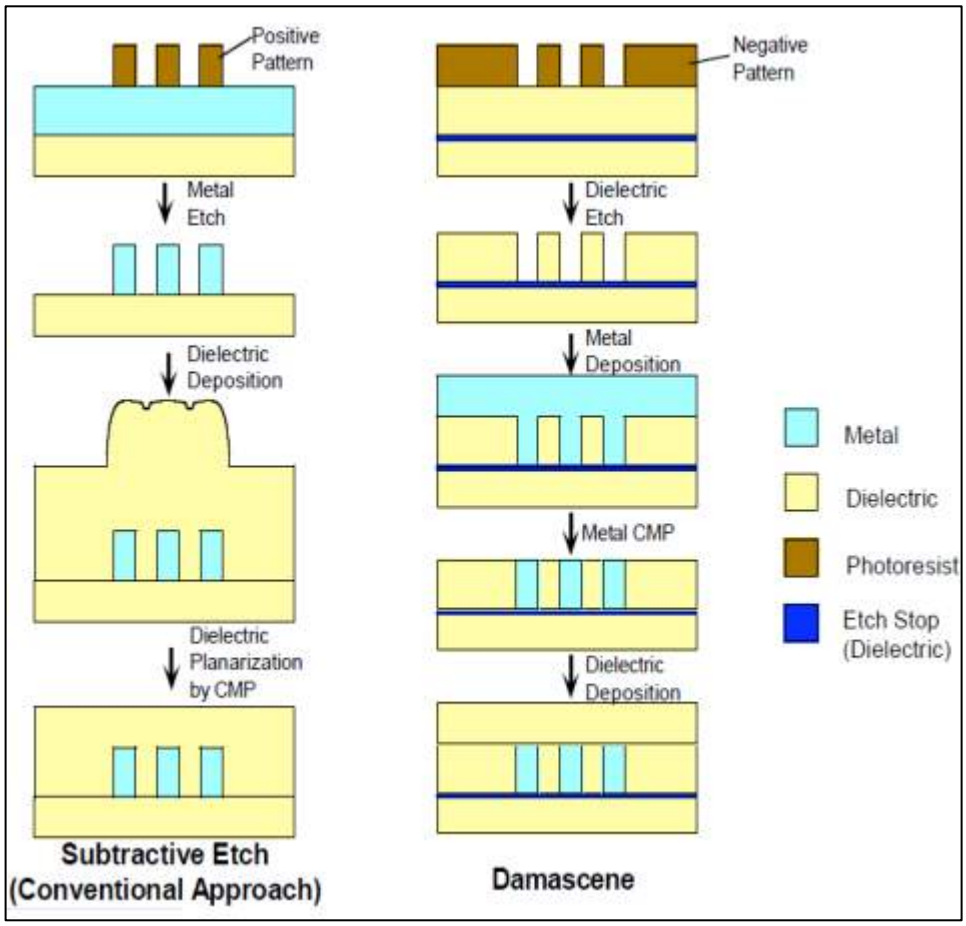


**Figure 2.1** Fabrication method of metal interconnect [3].

## 2.2 Electromigration in Copper Interconnects

As electromigration is an electric-current-induced atomic diffusion phenomenon, it thus depends on the diffusion path of the atoms. Research has been done extensively in order to investigate the dominant diffusion path in copper interconnects. Various studies have shown that unlike in aluminum-based interconnects, grain boundaries are not the fastest diffusion pathways in the copper interconnect [4, 5, 6]. Instead, the studies [5, 6] reported

that surface diffusion is the fastest diffusion pathway in copper electromigration, regardless whether the copper interconnect is poly-granular or has bamboo structure. In those studies as well, they showed that median-time-to-failure of copper interconnect is independent of line width. The value of the activation energies for surface and grain boundary diffusions in copper interconnect have been reported to be approximately 0.9 eV [5, 6] and 1.1 eV [5], respectively. Studies done by Usui *et al* showed that the value of the activation energy at 0.9 eV is independent to the line width of the copper interconnects [6]. Based on these values and results, it further supports the deduction that surface diffusion is the dominant diffusion mode in copper interconnects.

J.R. Black has derived the most widely used and accepted reliability model based on electromigration failure [7]. This model is widely known as Black's law. The equation 2.1 shows the model that was derived by Black.

$$t_{50} = \frac{A}{j^n} \exp\left(\frac{E_a}{kT}\right) \qquad (2.1)$$

where $t_{50}$ is the median-time-to-failure, $A$ is a constant dependent on the material and geometry, $j$ is the current density, $n$ is a constant that relates to the failure kinetics, $E_a$ is the activation energy for failure, $k$ is Boltzmann's constant and $T$ is temperature.

This model explains that the interconnect lifetime (i.e. median time to failure) is inversely proportional to the power-law of current densities ($j^{-n}$). The choice of the correct value for $n$ has been the focus of many works depending on the structure and testing condition [8, 9]. Clement *et al.* showed that when the value of $n = 1$, it means that void growth is the main mechanism during the electromigration testing [10]. Shatzkes *et al.* reported that when the value of $n = 2$, the dominating mechanism is void nucleation [11]. If the value of n rises above 2, the mechanism attributed to this failure is joule heating [8]. However, if the value of $n$ is between 1 and 2, the proposed mechanism to explain this value is nucleation followed by void growth [12].

By rearranging equation 2.1, the value of the activation energy for failure, $E_a$, in equation 2.1 can be determined in order to find out what is the dominant diffusion pathway for

mass transportation as mentioned earlier.

$$\ln(t_{50}) = \ln\left[\frac{A}{j^n}\exp\left(\frac{E_a}{kT}\right)\right]$$

$$\ln(t_{50}) = E_a\left(\frac{1}{kT}\right) + \ln\left(\frac{A}{j^n}\right) \qquad (2.2)$$

By plotting the a graph of $\ln(t_{50})$ against $1/kT$ , the activation energy for diffusion can be obtained. And from those values, the diffusion pathway such as surface transportation, grain boundary transportation or lattice transport, can then be determined as shown in Table 2.2.

**Table 2.2** Activation energy representing different diffusion path [13].

| Diffusion path | $E_a$ (eV) |
|---|---|
| Bulk Cu | 2.2 |
| Dislocations | 1.2–1.5 |
| Grain Boundaries | 0.88–0.95 |
| Surface | 0.8–0.9 |

Black's model was derived under the DC current stress condition. The model does not perfectly match when the type of current changes from DC to either pulse or AC current. Therefore, in the later years, various models were introduced to fit the experiments under pulse or AC current testing. Tao *et al.* has reported that the non-DC testing can either be fitted with the on time model or the average current model, depending on the *m* value in equation 2.4 below [14].

$$t_{50} = \frac{A}{j^n r^m}\exp\left(\frac{Q}{kT}\right) \qquad (2.3)$$

Where *r* is the duty ratio, and the rest of the notation follows the Black's law. When the value of $m$ = 1, this model assumes that the current-induced material transport is a function of the total on time current, which is widely known as the on time model. However, when the value of $m$ = 2, the model assumes that the full-direct current equivalence to the average magnitude of the current over the entire stressing period, which is known as average current model.

## 2.3 Impact of Interconnect Trees on Copper Interconnect

For the copper interconnect, the lifetime of an interconnect line may vary depending on the position of the metallization level of the interconnect line. This phenomenon was observed due to the location of void formation. Gan *et al.* reported that under similar test structure and condition, an interconnect in the second level of metallization (M2) will exhibit longer lifetime than a corresponding interconnect in the first level of metallization (M1) [15]. As shown in figure 2.2, the current flowing through the via situated above M1 interconnect can be blocked by the void formed at the $Cu/Si_3N_4$ interface. However, for the case of M2 interconnect, the void needs to grow across the full height and width of the interconnect before it can totally block the current flowing through the via situated below M2 interconnect (Figure 2.3). Therefore, the longer lifetime on the M2 interconnect is due to the longer time that is needed for a void to grow across the full height and width of the interconnect.

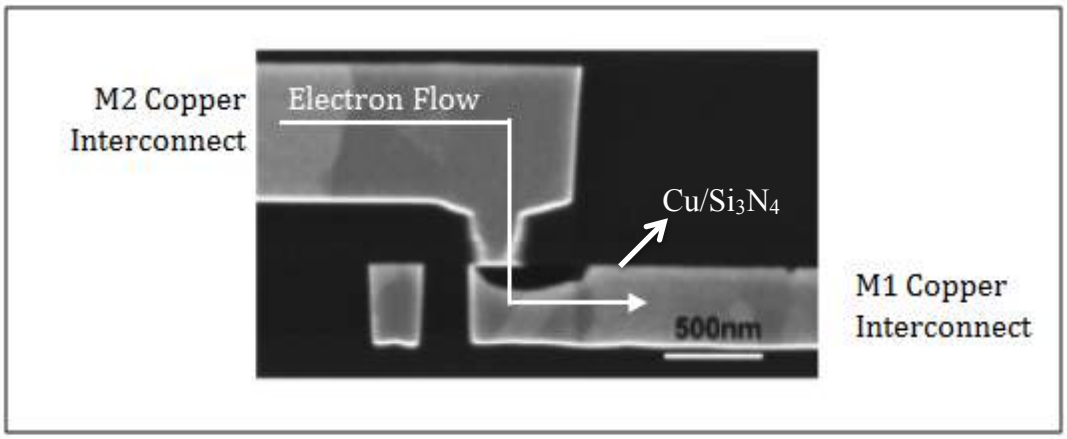


**Figure 2.2** FIB cross-section of a copper interconnect showing a void formed at M1 Copper/ $Si_3N_4$ interface [16].

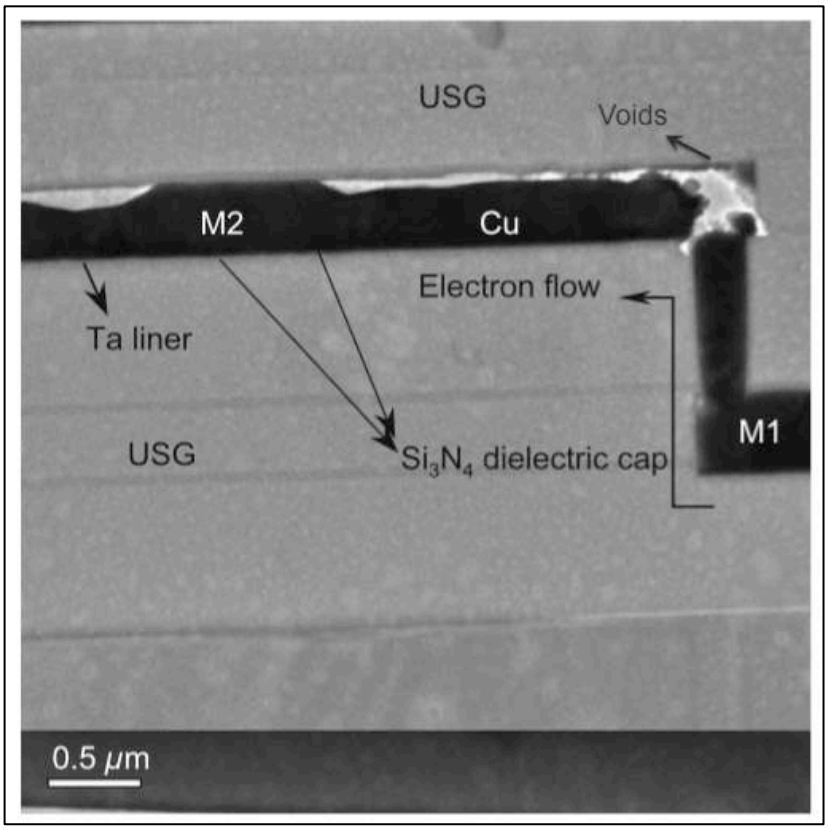


**Figure 2.3** FIB cross-section of a copper interconnect showing a void formed at M2 Copper/ $Si_3N_4$ interface [17].

The values of the critical threshold product are also different for the copper interconnects situated at different metallization levels. A value of 1500 A/cm was reported for the critical threshold product for M1 copper interconnect tested at 350°C [18, 19], whereas the value 3700 A/cm was reported for M2 copper interconnect tested between the temperature range of 340°C to 360°C [20].

In the integrated circuit, it is hard to find a simple single straight via-to-via metal line. Instead, interconnect trees (i.e. interconnects with bends, junctions or more than two vias) are easily found in integrated circuits. An interconnect tree is a term that refers to an unit of conductive metal line which has more than one segment of metal line connected at junction(s) within the same level of metallization. The ends of metal segments that are not connected at junction are terminated at diffusion barriers such as vias or contacts with refractory metal liners [21, 22, 23].

In the interconnect trees, there are several scenarios where the metal segment that is coupled with the other metal segment can either act as a passive or active reservoir, and thus can either improve or deteriorate the reliability of the overall interconnect trees. Passive reservoir means that the metal segment does not carry any electric current; whereas the active reservoir means that it carries an electric current [21, 24]. Active and passive reservoirs can be further categorized into atomic source or atomic sink. If metal atoms from this segment flows into the adjacent segment, it is called an atomic source. On the other hand, if metal atoms from adjacent segments flow into this passive or active segment, it is called an atomic sink [25]. Figures 2.4, 2.5 and 2.6 show the right segment of a Dotted-I-structure interconnect tree acting either as a passive atomic source or atomic sink, or an active atomic source or atomic sink. Due to the effects of these active and passive reservoirs, various authors have reported that a segment that is stressed with the highest current density may not exhibit the shortest time-to-failure as compared to other segment(s) in the same interconnect tree [24, 26, 27].

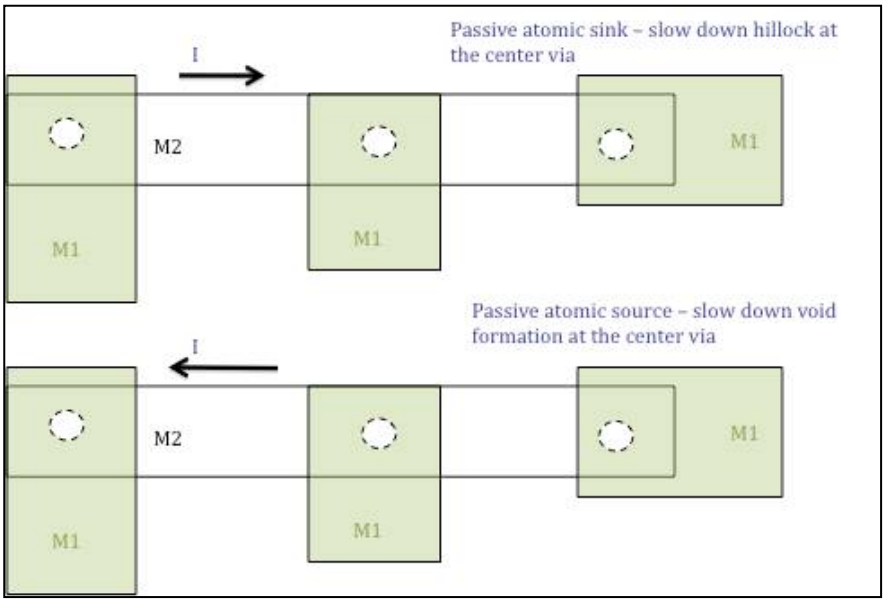


**Figure 2.4** Right segment of the dotted-I structure acting as passive atomic source or atomic sink, improving the reliability of the left segment.

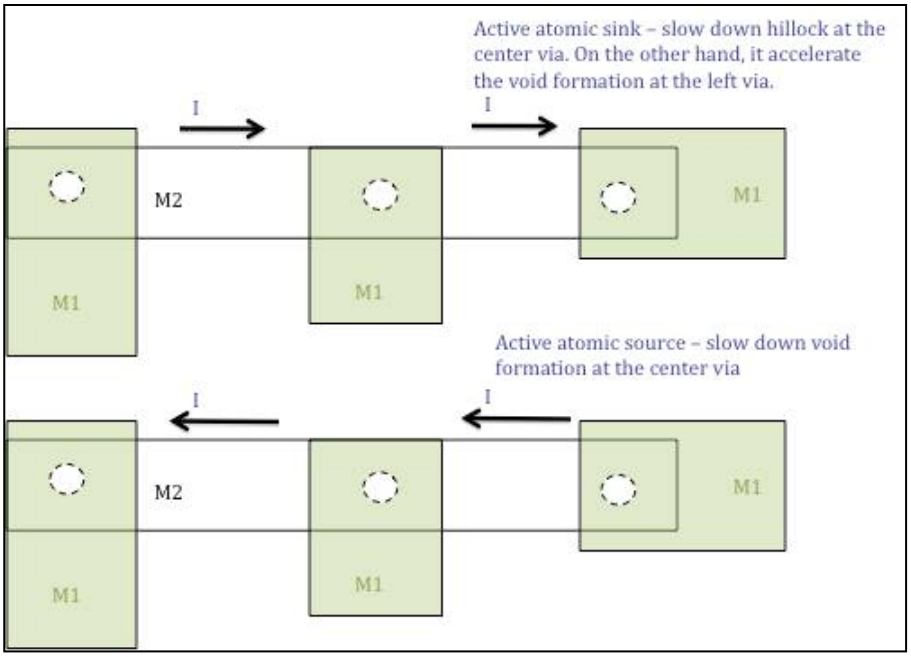


**Figure 2.5** Right segment of the dotted-I structure acting as active atomic source or atomic sink, improving the reliability at the center via.

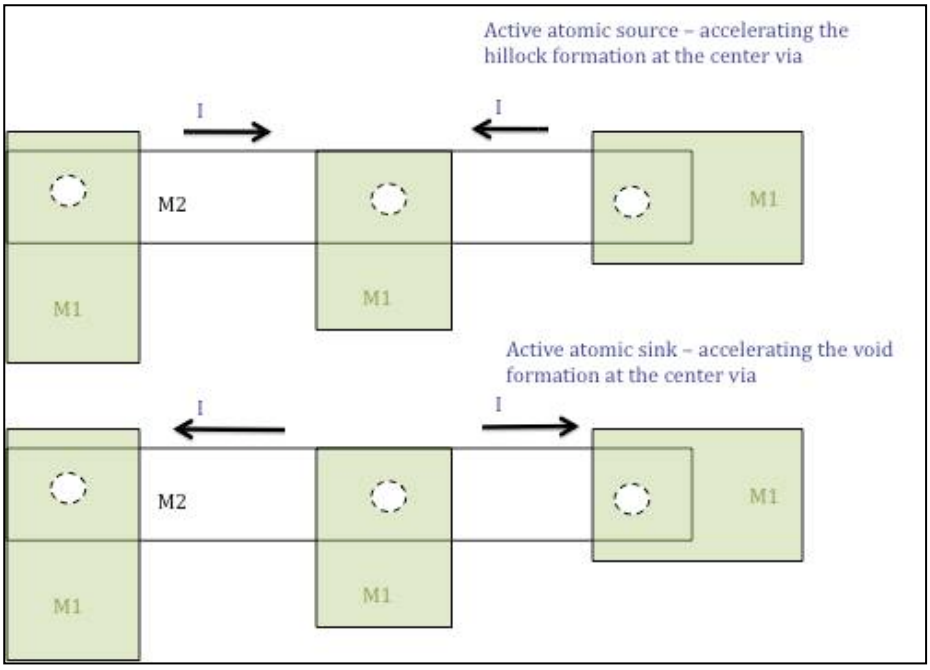


**Figure 2.6** Right segment of the dotted-I structure acting as active atomic source or atomic sink, deteriorating the reliability at the center via.

## 2.4 Introduction of End-of-line Metal Reservoir

The concept of an end-of-line metal reservoir or overhang was introduced in the interconnect structures in 1999 [28], whereby in the experiments for the Al interconnect system, it was found that the end-of-line metal reservoir is able to increase the lifetime of the interconnect as shown in Figure 2.7. K. N. Tu *et. al.* [29] proposed that the reason is due to the flux gradient of current density that exists between the stressed metal line and end-of-line metal reservoir. This flux gradient will push the vacancies toward the lower current density region in the end-of-line metal reservoir. Therefore, the void will nucleate there and due to the additional metal volume provided by the end-of-line reservoir, it will allow for a bigger void to grow and expand before it completely shuts off the current path in the metal line. The argument proposed led to a disagreement between several other researchers [29, 30]. J.R. Lloyd [30] argued that the current crowding plays a small if not insignificant role in electromigration and maintained that the electromigration induced stress model is able to explain why the void is formed at the end-of-line reservoir. Despite the arguments between the two proposed mechanisms, other studies found similar observations on the end-of-line metal reservoir [31, 32, 33] whereby the lifetime of the interconnect was greatly improved and the void was found in the end-of-line metal reservoir section.

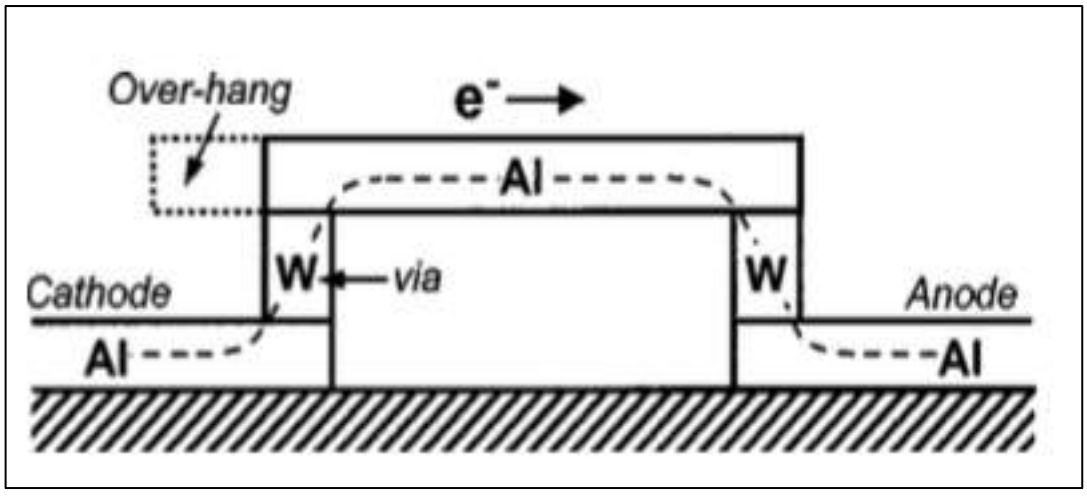


**Figure 2.7** Schematic diagram of a two-level Al interconnect connected by W vias. The broken line depicts the overhang as a reservoir for void growth. [29].

The concept of the end-of-line metal reservoir was extended to the Cu metal interconnect as well. S. Wei *et. al* [17] found that with increasing length of the end-of-line metal reservoir from 0 nm to 60 nm, it increased the lifetime $t_{50}$ of the interconnect by almost 3 times. However, she observed that by increasing the length of the end-of-line metal reservoir from 60 nm to 120 nm, it did not change much of its lifetime as shown in Figure 2.8. Z.H. Gan *et. al* [34] reported that the critical extension length for the end-of-line metal interconnect is a function of void size and electrical field gradient. In order for the void to keep moving inward of the end-of-line metal reservoir, the void size cannot be too big and the gradient of the electrical field in the *y*-direction must be less than four times of that in the *x*-direction. Tan *et. al.* [35] proposed the AFD (Atomic Flux Divergence) concept in explaining the effectiveness of the length end-of-line metal reservoir. In his simulation as shown in Figure 2.9, the $\overline{\overline{AFD_{total,\ V}}}$ decreases as the length of the end-of-line metal reservoir increases, which is indicating that the void growth rate decreases as length of end-of-line metal reservoir increases. The results also show that $\overline{\overline{AFD_{total,\ V}}}$ saturated at L = 0.08 μm, which indicates that the effectiveness of end-of-line metal reservoir ceases at L = 0.08 μm and beyond.

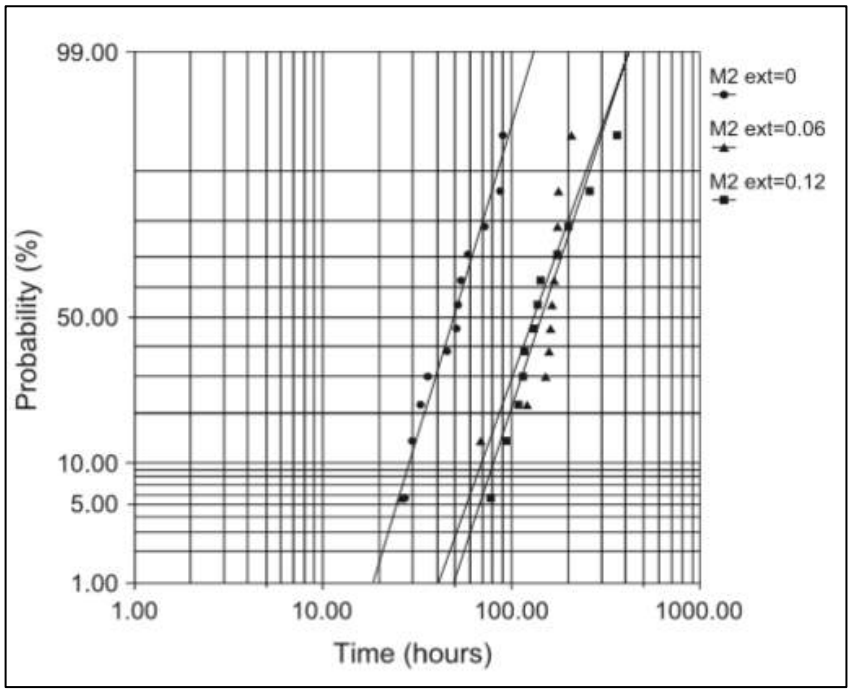


**Figure 2.8** EM failure time distribution for M2 structures with various reservoir lengths [17].

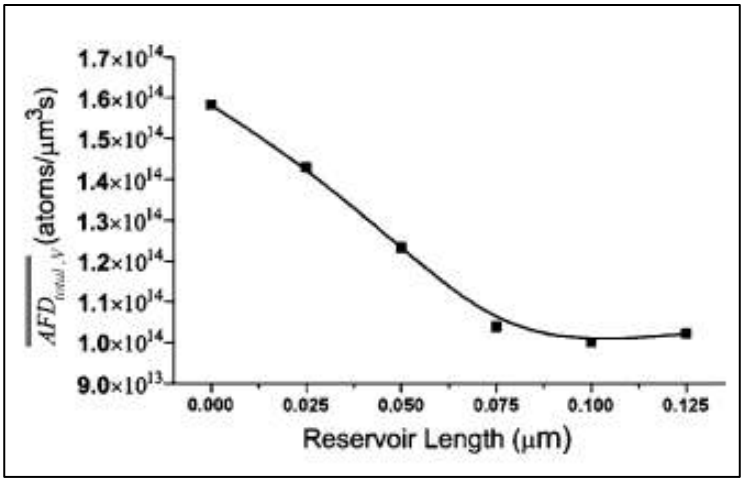


**Figure 2.9** Variation of the mean of the volume-averaged AFD, $\overline{\overline{AFD_{total,\ V}}}$ within the control volume with the reservoir length. $\overline{\overline{AFD_{total,\ V}}}$ decreases gradually with the reservoir length until a critical length of around 0.08 μm intervals [35].

The experiments conducted by A.V. Vairagar *et al.* [36, 37, 38] and D.J. Pete *et al*. [39], showed that for the Cu metal interconnect system, the mechanism on how the end-of-line metal reservoir is able to improve the lifetime is not due to the current density gradient as being shown in the Al electromigration, but is being explained by that the void, which was found at the Cu/$SiN_x$ interface at a distance away from the cathode, drifting towards the cathode due to the opposing electron wind force. It then reached the end of the cathode line and did not move into the end-of-line metal reservoir due to the absence of the opposing electron wind force there. When the other voids that were drifting reached the end of the cathode line, they would coalesce together and formed a bigger void. This void can then partially agglomerated into the end-of-line metal reservoir segment before further spanning towards the cathode via and completely shut off the current path. Because of this, the end-of-line metal reservoir acts as an additional volume for the void to grow and expand. A point to note is that the author did not observed any void nucleation or formation at the end-of-line metal reservoir, which is supposed to be the lowest current gradient location in the whole metal line. Therefore, it is suggested that the current crowding effect is negligible in the Cu interconnect system.

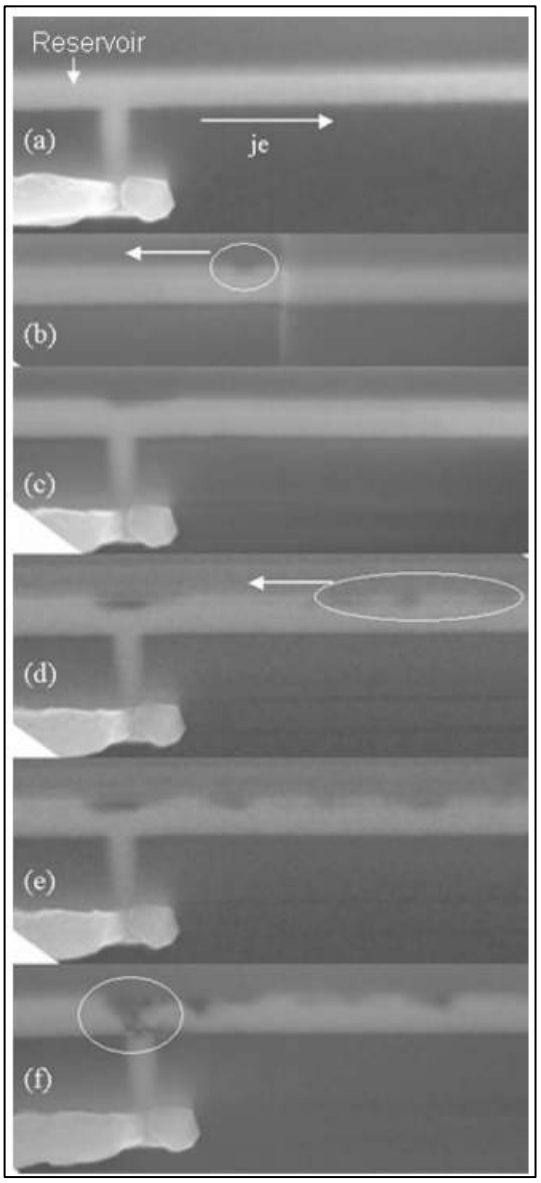


**Figure 2.10** SEM images of the middle via region at various time intervals [37].

K. Croes *et al*. [40] provided further evidence that current crowding and current density gradients play a negligible role in the void formation in dual damascene copper interconnects. In the experiment, the void was not found in the location of the lowest gradient current density (the $90^0$ corner angle) but instead it was found at a distance away from the $90^0$ corner angle location as shown in the Figure 2.11 and Figure 2.12.

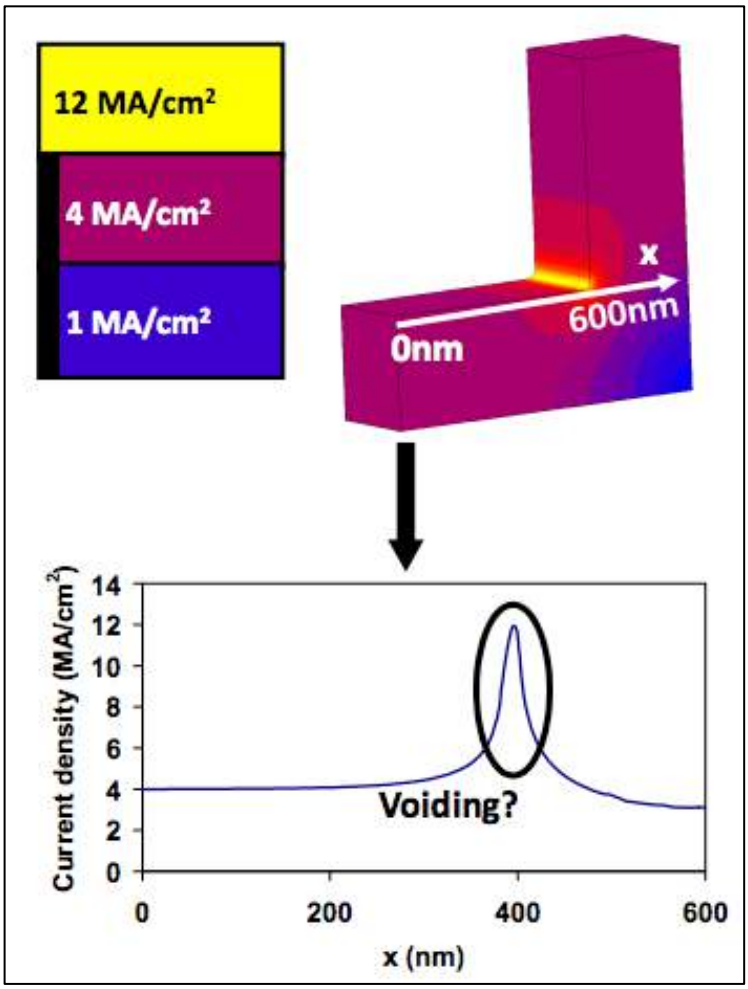


**Figure 2.11** Finite Element Model of current distribution in proposed angled structures. High current density at the angle should induce voids in case current crowding or current density gradients have an high impact [40].

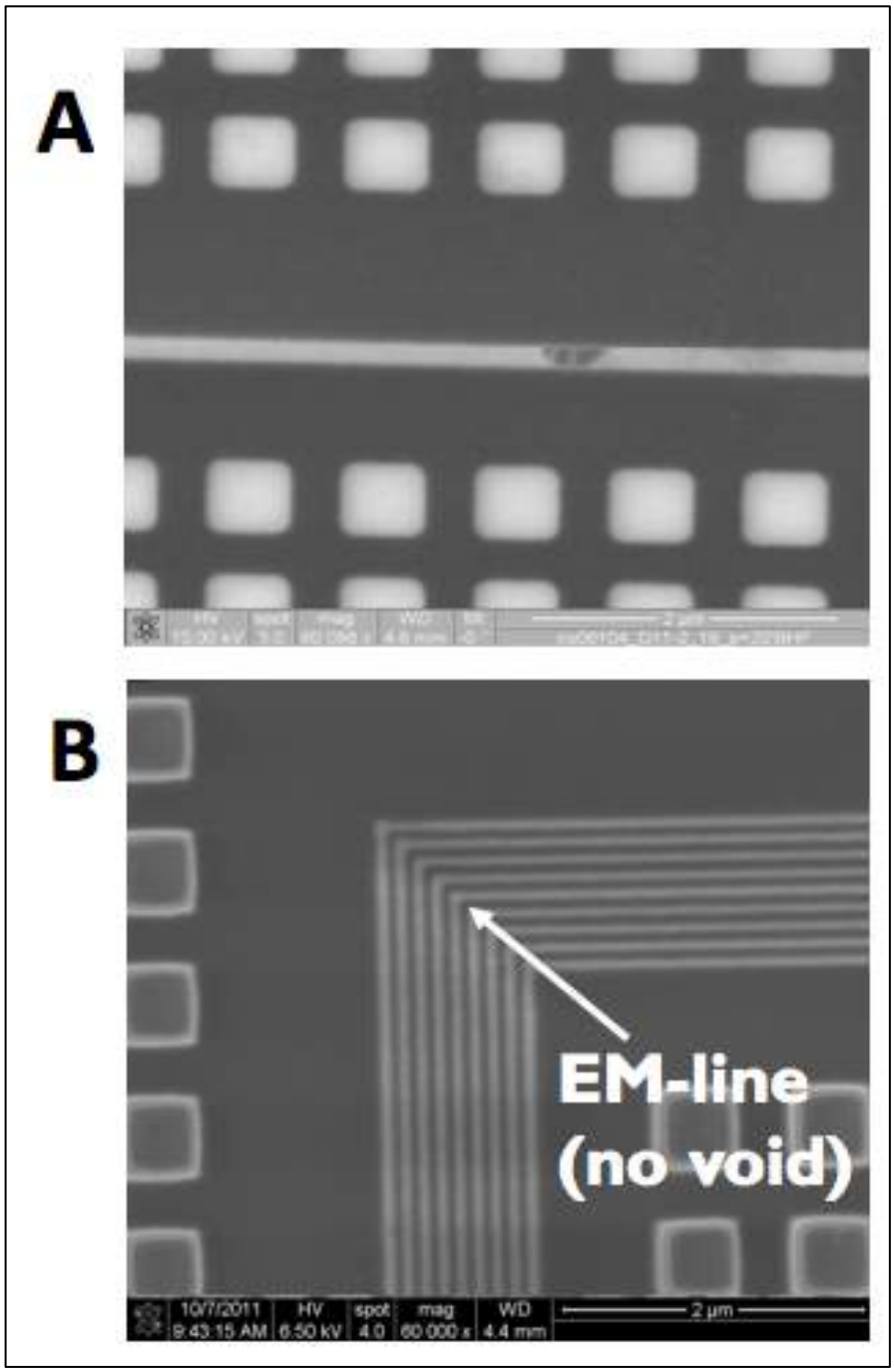


**Figure 2.12** Failure analysis. Top-down SEM image of an angled structure after void formation. A) void formed away from the angle (example of 120 nm wide line) and B) no void observed in the 30 nm wide line (example of 30 nm wide line) [40].

## 2.5 Copper/Cap Interface Influence on Electromigration

As mentioned in the earlier section that void was found at the interface of Cu/$SiN_x$, it can be assumed that the Cu/cap interface is regarded as the diffusion path during the electromigration. From the fabrication point of view, this Cu/cap interface is vulnerable in introducing a defect during the CMP process before being capped by the capping material. Therefore, many researches have tried to improve the electromigration lifetime by trying to improve the quality of the Cu interface before the capping process such as using sulfuric acid wet etching, thermal treatment in vacuum environment at 350$^{o}$C, He, $H_2$ or $NH_3$ plasma treatment [41, 42, 43, 44, 45] or changing the capping material such as SiN, BloK$^{TM}$, SiC, Ta, TaN, Pd, Ag, Co, CoWP and AlN [46, 47, 48, 49, 50, 51].

Lane *et al*. [46] conducted an experiment of electromigration by changing the capping materials of the copper interconnect. From the experiment, it was found that CoWP is the best capping material due to its slowest void growth rate when compared to the rest of the capping material such as SiN, BloK$^{TM}$ and SiC (Figure 2.13). This is being attributed to the highest adhesion energy of Cu/CoWP interface. Similar observation was made by Hu *et al.* [47], whereby they found that the CoWP has the highest activation energy for EM which is around 2.4 eV as compared to Ta/TaN 1.4 eV, $SiN_x$ 1.0 eV and $SiC_xN_yH_z$ 1.0 eV. Therefore, the electromigration lifetime of Cu/CoWP is the longest as shown in Figure 2.14.

Kang *et al.* [48] found that Ag capping layer is able to retard the formation of Cu oxide at post CMP process. The Ag capping layer was deposited via *in-situ* process. Yang *et al.* [49] reported that Co capping layer with the thickness of around 6 nm is able to extend the lifetime of electromigration much longer compared to control no-metal cap, Co cap thickness of 1.5 and 3 nm as shown in Figure 2.15.

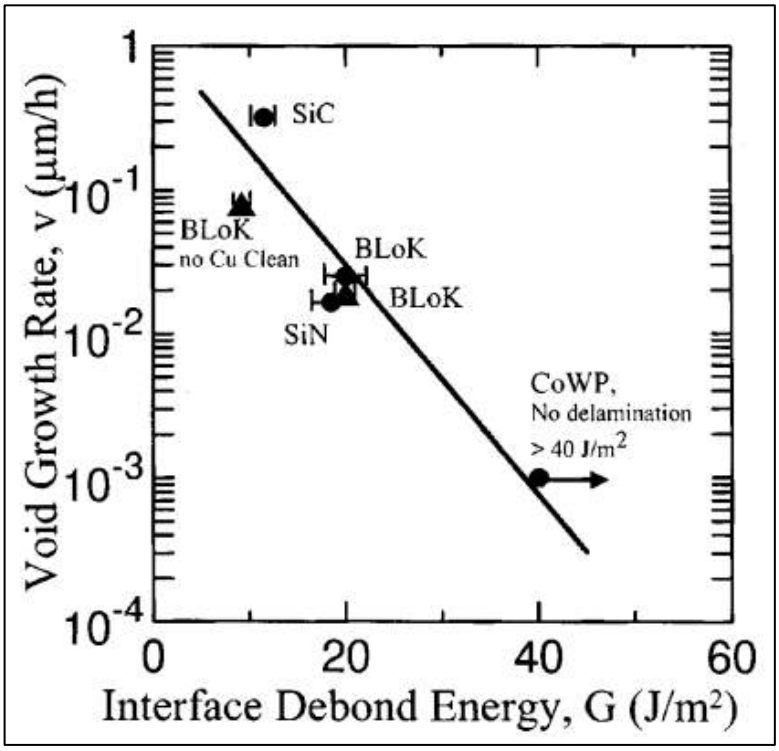


**Figure 2.13** Void growth rate at 310°C as a function of the interface debond energy. Note that there appears to be a linear relationship between the log of the growth rate and the debond energy but the lack of a definite value of the Cu/CoWP adhesion limits this conclusion [45].

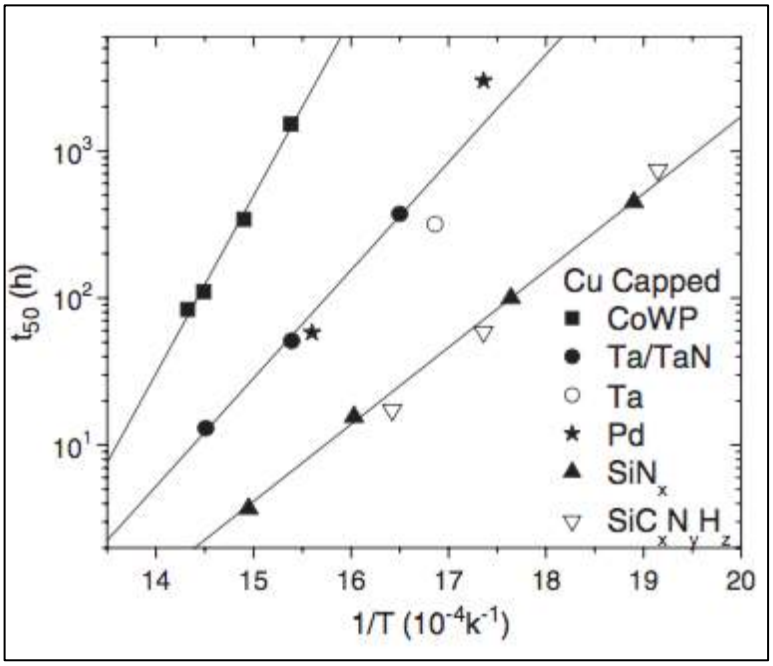


**Figure 2.14** $t_{50}$ vs. (1/T) for the Cu lines with various caps [46].

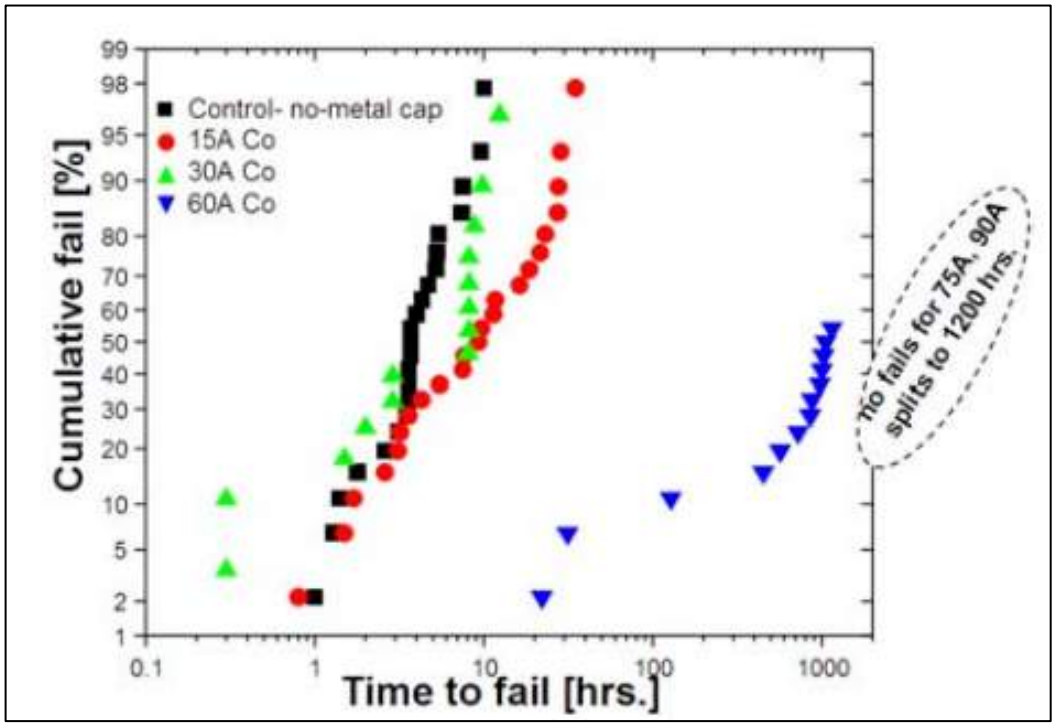


**Figure 2.15** Distribution of EM fails showing dependency on the deposited Co cap thickness [48].

D. Priyadarshini *et al.* [50] found that by having a full wrap around of Co cap/Co liner, it can greatly increase the lifetime of the electromigration up to 1000x higher when compared to SiN cap and up to 100x higher when compared to selective Co cap (Figure 2.16). The electromigration activation energy for the wrap around Co cap/Co liner was found to be around 1.7 eV, while the SiN cap around 1 eV. Thus, this makes the copper atoms or vacancies much harder to diffuse along the interface of Co cap/Co liner/copper as opposed to SiN/copper.

M. Zhou [51] investigated the AlN capping material as a means to enhance the adhesion between Cu and SiCN. AlN was deposited by using an atomic layer deposition (ALD) process and the thickness of the AlN ~8.5 nm. Reliability test VBD (Voltage Break-Down) and electromigration on control versus AlN capping samples shows that AlN capping is able to improve the VBD by around 24% and increase the lifetime of both upstream and downstream electromigration (Figure 2.17).

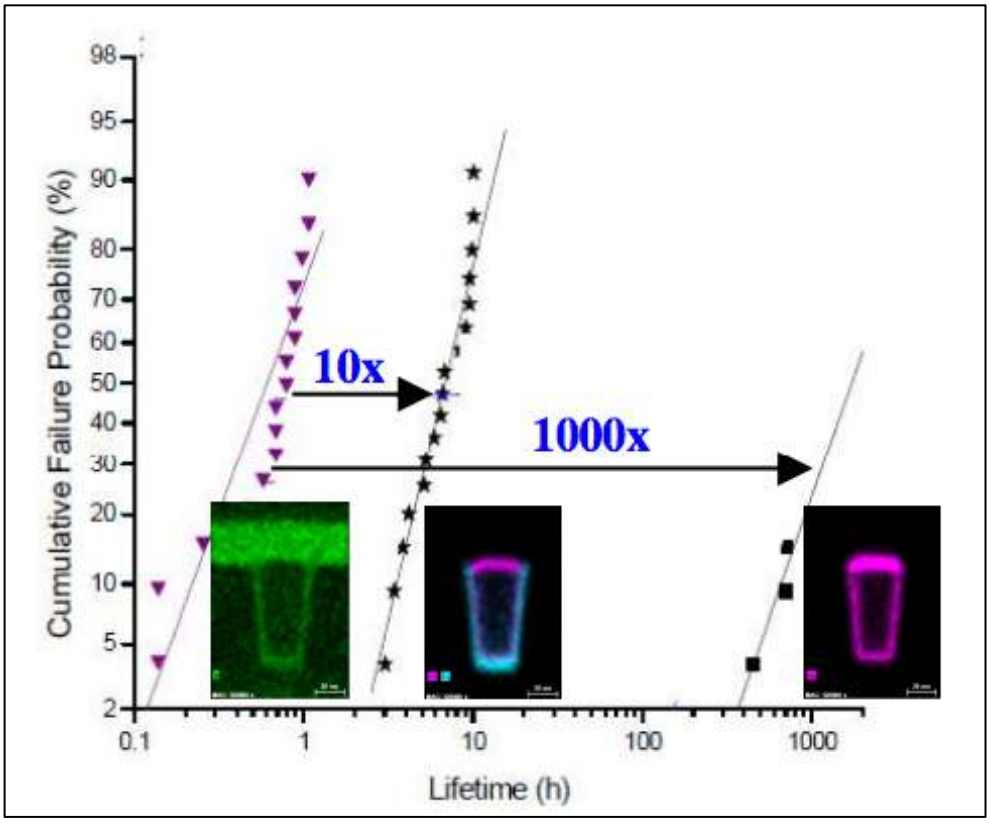


**Figure 2.16** Electromigration lifetime distribution- dielectric cap, selective Co cap (10X higher) and wrap around Co cap/Co liner structure (1000X higher) [49].

The change in the capping material does greatly improve the electromigration lifetime. However, in terms of the actual implementation in the mass production wafer fabrication, it still needs more time due to its complexity of process integration and the additional steps will incur additional cost and lower down the throughput as well when compared to the SiN cap process [52]. Therefore, most of the wafer fabrication companies are still using the SiN cap as their capping material post CMP process.

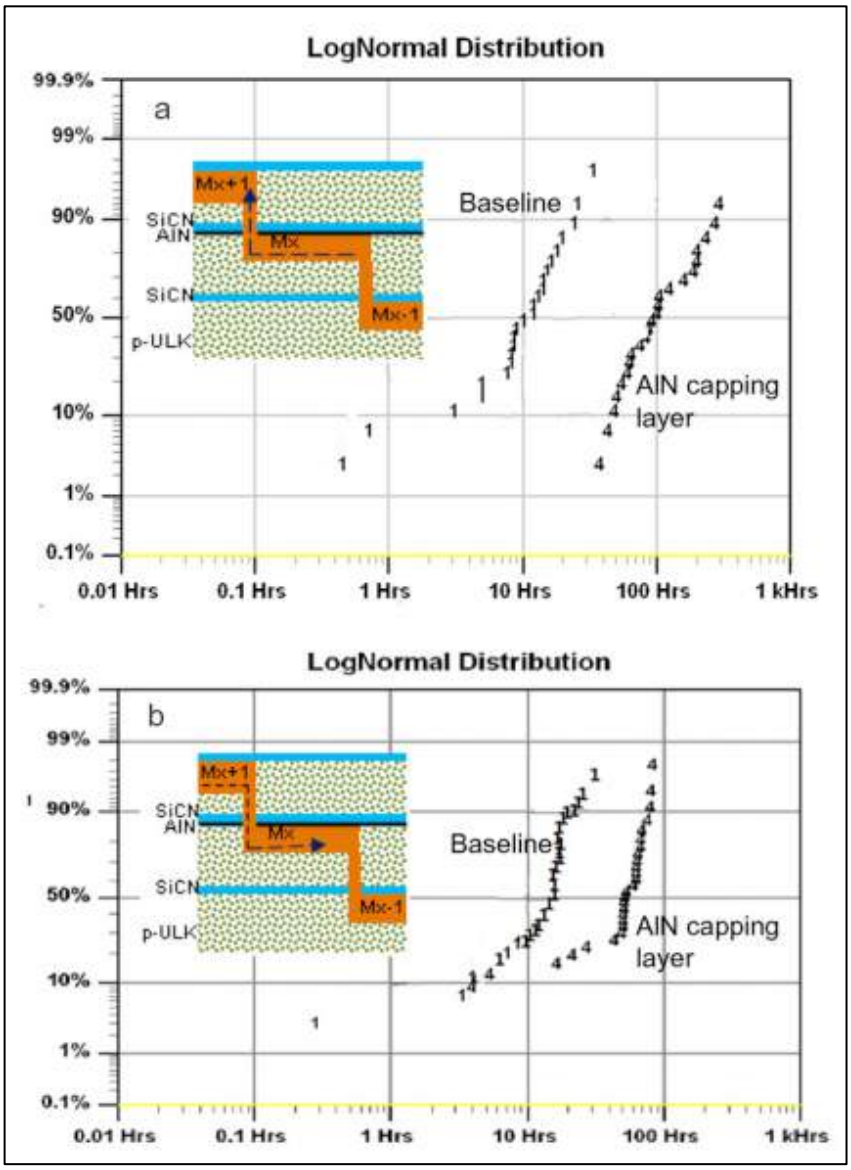


**Figure 2.17** The EM performance of upstream (a) and downstream (b) using the alone SiCN dielectric barrier layer and AlN capping layer combined with SiCN dielectric barrier layer [50].

## 2.6 Pre-existing Void on Copper Electromigration

Based on the Korhonen's model [53], the stress evolution during electromigration stressing will lead to a maximum tensile stress at the end of cathode vias due to copper atoms depletion. When this tensile stress exceeds the critical value, it will cause the void to nucleate there to relieve the stress. The void will continue to grow until it causes an open circuit failure. However, in the electromigration experiment conducted by S.P. Hau-Riege *et al.* [16] and M.H. Lin *et al.* [54], it was found from the post-mortem failure analysis on the copper interconnect that the voids were not always found at the end of the cathodes vias as shown in Figure 2.18. The location where the voids varies from line to line.

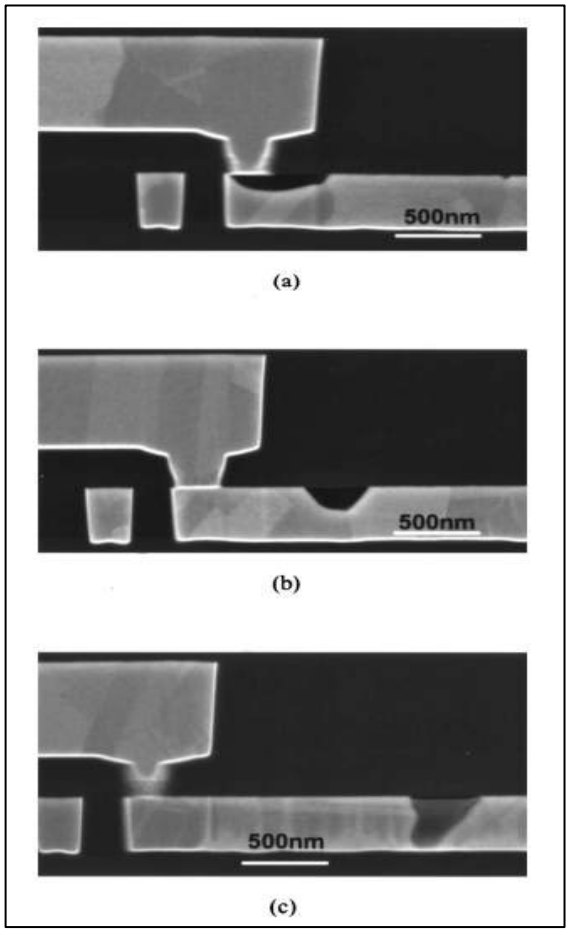


**Figure 2.18** Post-mortem physical failure analysis from electromigration in M1 Cu interconnects [16].

F. Bana *et al.* [55] have similar observations in their experiments, where multiple voids were found under the same copper interconnect line after the electromigration test as shown in Figure 2.19.

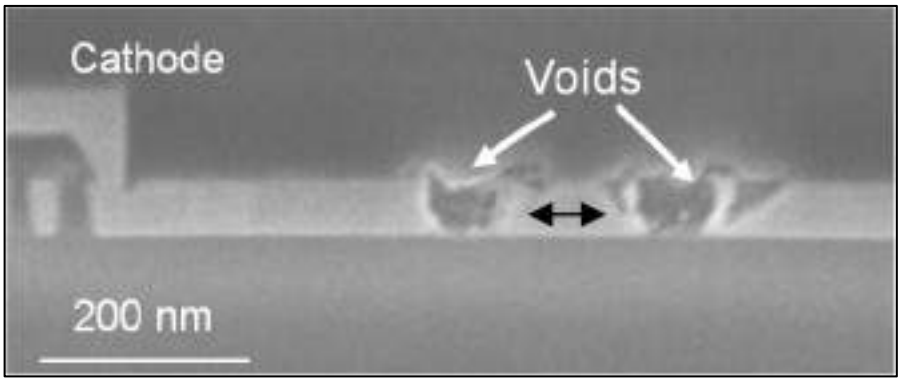


**Figure 2.19** SEM image where multiple voids were found in the copper interconnect [55].

Recent *in-situ* experiments done by M.A Meyer *et al.* [56], A.V. Vairagar *et al.* [36] and Z.S. Choi *et al.* [57] revealed that some of the voids were first seen not at the end of the cathode via, but instead a distance away from it. These voids drifted towards the end of cathode via when further electrically stressed and they merged with others voids. Subsequently, the void would continue to grow until it causes an open circuit failure, leading to an abrupt change in the resistance.

Therefore, it can be concluded that the origin of such voids can be due to electromigration flux divergence associated at grain boundaries, or are pre-existing due to differential thermal expansion between the Cu metallization and the dielectric layer [58, 59], or due to defects inherited from process fabrication. In Cu metallization, the Cu/dielectric cap interface is the fastest diffusion path as compared to grain boundaries in Al interconnects [60]. Thus, void formation due to a flux divergence at the cap/grain boundaries junction at a distance away from the cathode requires a large difference in diffusivity value between the adjacent grains, or having a long cluster of high-diffusivity grains, which both are very unlikely in Cu metallization [61].

**References:**


[1] W.D. Callister, Jr. *John Wiley & Sons, Inc: Materials Science and Engineering: An Introduction*, **2000**, 5th ed

[2] J. Lienig. *Proc. of the Int. Symposium on Physical Design (ISPD)* **2006,** 39–46.

[3] R. Doering and Y. Nishi, Eds. *CRC Press: Handbook of Semiconductor Manufacturing Technology.* **2007**, 2nd ed.

[4] C.S. Hau-Riege and C.V. Thompson. *Appl. Phys. Lett.* **2001,** 78, 3451-3453.

[5] C.K. Hu, R. Rosenberg, and K.Y. Lee. *Appl. Phys. Lett.* **1999,** 74, 2945-2947.

[6] T. Usui, H. Nasu, T. Watanabe, H. Shibata, T. Oki, and M. Hatano. *J. Appl. Phys.* **2005**, 98, 063509.

[7] J.R. Black. *Proc. 6th Int. Reliab. Phys. Symp.: Mass Transport of Aluminum by momentum exchange with conducting electrons.* **1967,** 148-153.

[8] J.J. Clement. *J. Appl. Phys.* **1997,** 82, 5991-6000.

[9] I.A. Blech, E. Kinsbron, and Y. Komen. *Thin Solid Films*. **1999,** 38, 3790-3799.

[10] J.J. Clement. *IEEE Transactions on Device and Materials Reliability*. **2001,** 1, 33-42.

[11] M. Shatzkes and J.R. Lloyd. *J. Appl. Phys.* **1986,** 59, 3890-3893.

[12] J.J. Clement and J.R. Lloyd. *J. Appl. Phys.* **1991,** 71, 1729-1731.

[13] C.S. Hau-Riege, *Microelectronics Reliability*. **2004**, 44 (2), 195-205.

[14] J. Tao, N.W. Cheung, and C. Hu. *IEEE Electron Device Letters*. **1995,** 16, 476-478.

[15] C.L. Gan, C.V. Thompson, K.L. Pey, W.K. Choi, H.L. Tay, B. Yu, and M.K. Radhakrishnan. *Appl. Phys. Lett.* **2001,** 79(27), 4592-4594.

[16] S.P. Hau-Riege. *J. Appl. Phys.* **2002,** 91, 2014-2022.

[17] S. Wei, A.V. Vairagar, C.H. Tung, Z.L. Xie, A. Krishnamoorthy, S.G. Mhaisalkar. *Surface and Coating Technology*, **2005**, 198, 257-261.

[18] C.S. Hau-Riege, A.P. Marathe, and V. Pham. *Proc. Advanced Metallization Conference*, **2002**, 169.

[19] C.S. Hau-Riege, A.P. Marathe, and V. Pham. *Reliability Physics Symp. Proc,* **2003,** 173.

[20] K.D. Lee, E.T. Ogawa, H. Matsuhashi, P.R. Justison, K.S. Ko, and P.S. Ho. *Appl. Phys. Lett.* **2001,** 79, 3236-3238.

[21] S.P. Hau-Riege and C.V. Thompson. *Mat. Res. Soc. Symp. Proc.* **2000,** 612, D8.7.1.

[22] S.P. Hau-Riege and C.V. Thompson. *J. Appl. Phys.* ***2000,*** 88, 2382-2385.

[23] S.P. Hau-Riege and C.V. Thompson. *J. Appl. Phys.* **2001,** 89, 601-609.

[24] C.L. Gan, C.V. Thompson, K.L. Pey, W.K. Choi, C.W. Chang, and Q. Guo. *Proceedings of the 2003 Int'l. Symposium on Reliability Physics: Effect of Current Distribution on the Reliability of Multi-Terminal Copper Dual-Damascene Interconnect Trees.* **2003**.

[25] J.R. Lloyd, *Microelectronics Reliability*. **2007**, 47, 1468-1472.

[26] C.L. Gan, C.V. Thompson, K.L. Pey, and W.K. Choi. *J. Appl. Phys.* **2003,** 94, 1222-1228.

[27] A.V. Vairagar, S.G. Mhaisalkar, M.A. Meyer, E. Zschech, A. Krishnamoorthy, K.N. Tu, and A.M. Gusak. *Appl. Phys. Lett.* **2005,** 87, 081909.

[28] K.S. Low, H. Poetzlberger, and A. O'neill. *Mater Res. Soc. Symp. Proc.* **1999,** 563, 133.

[29] K.N. Tu, C.C. Yeh, C.Y. Liu, and C. Chen. *Appl. Phys. Lett.* **2000,** 76, 988-990.

[30] J.R. Llyod. *Appl. Phys. Lett.* **2001,** 79, 1061-1063.

[31] S. Shingubara, T. Osaka, S. Abdeslam, H. Sakue, and T. Takahagi. *4th International Workshop on Stress-Induced Phenomena in Metallization, Tokyo, Japa*n, 1997 @AIP Conf. Proc. **1998,** 418, 159.

[32] Y.B. Park and I.S. Jeon. *Microelectronics Enginnering.* **2004,** 71, 76-89.

[33] I.S. Jeon and Y.B. Park. *Microelectronics Reliability.* **2004**. 44, 917-928.

[34] Z.H. Gan, A.M. Gusak, W. Shao, Z. Chen, S.G. Mhaisalkar, T. Zaporozhets, and K.N. Tu. *J. Material Research*. **2007,** 22, 152-156.

[35] C.M. Tan, Y. Hou, and W. Li, *J. Appl. Phys.* **2007,** 102, 033705.

[36] A.V. Vairagar, S.G. Mhaisalkar, A.Krishnamoorthy, K.N. Tu, A.M. Gusak, M.A. Meyer and E. Zschech. *Appl. Phys. Lett.* **2004,** 85, 2502-2504.

[37] A.V. Vairagar, S.G. Mhaisalkar, M.A. Meyer, E. Zschech, and A. Krishnamoorthy. *Microelectronic Engineering*. **2005,** 82, 675-679.

[38] A.V. Vairagar, S.G. Mhaisalkar, A. Meyer, E. Zschech, A. Krishnamoorthy, K.N. Tu, and A.M. Gusak, *Appl. Phys. Lett.* **2005,** 87, 081909.1-081909.3.

[39] D.J. Pete, J.B. Helonde, A.V. Vairagar, and S.G. Mhaisalkar. *J. Electronic Materials*. **2012,** 41, 568-572.

[40] K. Croes, Y. Li, M. Lofrano, C. J. Wilson and Zs. Tokei. *Reliability Physics Symposium (IRPS), 2013 IEEE International,* **2013,** 2C.3.1-2C.3.4.

[41] C.C. Chiang, M.C. Chen, L.J. Li, Z.C. Wu, S.M. Jang, and M.S. Liang. *J. Appl. Phys.* **2004,** 43, 7415-7418.

[42] G.P. Beyer, M. Baklanov, T. Conrad, and K. Maex. *Material Research Society Symposium Proccedings.* **2000,** 612, 9-17.

[43] R.C.J. Wang, D.S. Su, C.T. Yang, D.H. Chen, Y.Y. Doong, J.R. Shih, S.Y. Lee, C.C. Chiu, Y.K. Peng, and J.T. Yue. *Proceedings of Seventh International Symposium on Plasma and Process-Induced Damage, American Vacuum Society*, **2002,** 166–168.

[44] A.V. Vairagar, S.G. Mhaisalkar, and A. Krishnamoorthy. *Thin Solid Films,* **2004,** 325, 462-463.

[45] Y.M. Chang, J. Leu, B.H. Lin, Y.L. Wang, and Y.L. Cheng. *Advance Materials Science Engineering,* **2013,** 1-7.

[46] M.W. Lane, E.G. Linger, and J.R. Lloyd. *J. Appl. Phys.* **2003,** 93, 1417–1421.

[47] C.K. Hu, D. Canaperi, S.T. Chen, L.M. Gignac, S. Kaldor, M. Krishnan, S.G. Malhotra, E. Liniger, J.R. Llyod, D.L. Rath, D. Restaino, R. Rosenberg, J. Rubino, S.C. Seo, A. Simon, S. Smith and W.T. Tseng. *Thin Solid Films.* **2006,** 504, 274-278.

[48] M.C. Kang, Y.J. Kim and J.J. Kim. *Electrochemical and Solid State Letters.* **2009,** 12, 340–343.

[49] C. Yang, F. Baumann, P.C. Wang, S.Y. Lee, P. Ma, J. AuBuchon, D. Edelstein. *Interconnect Technology Conference and 2011 Materials for Advanced Metallization (IITC/MAM), 2011 IEEE International,* **2011,** 1–3.

[50] D. Priyadarshini, S. Nguyen, H. Shobha, S. Cohen, T. Shaw, E. Liniger, C.K. Hu, C. Parks, E. Adam, J. Burnham, A.H. Simon, G. Bonilla, A. Grill, D. Canaperi, D. Edelstein, D. Collins, M. Balseanu, M. Stolfi, J. Ren and K. Shah. *Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), 2014 IEEE International.* **2014,** 185-188.

[51] M. Zhou. *Microelectronics Reliability.* **2015,** 55, 2705-2711.

[52] C.M. Tan and A. Roy. *Materials Science and Engineering R.* **2007,** 1-75.

[53] M.A. Korhonen, P. Borgesen, K.N. Tu, and C.Y. Li. *J. Appl. Phys.* **1993,** 73, 3790-3799.

[54] M.H. Lin, Y.L. Lin, K.P. Chang, K.C. Su and T.H. Wang. *Microelectronics Reliability.* **2005,** 45, 1061-1078.

[55] F. Bana, L. Arnaud, D. Ney, and Y. Wouters. *Microelectronics Enginnering*. **2013,** 112, 130-132.

[56] M.A. Meyer, M. Herrmann, E. Langer and E. Zschech. *Microelectronic Engineering*. **2002,** 64, 375-382.

[57] Z.S. Choi, R. Moenig, and C.V. Thompson. *Journal of Materials Research*. **2008,** 23, 383-391.

[58] A. Sekiguchi, J. Koike, and K. Maruyama. *Applied Physics Letters.* **2003,** 83, 1962-1964.

[59] C.W. Chang, C.V. Thompson, C.L. Gan, K.L. Pey, W.K. Choi and Y.K. Lim. *Applied Physics Letters*. **2007,** 90, 193505.

[60] S.M. Alam, C.L. Gan, C.V. Thompson and D.E. Troxel. *Microelectronics Journal*. **2007,** 38, 463-473.

[61] Z.S Choi, J.H. Lee, M.K. Lim, C.L. Gan and C.V. Thompson. *Journal of Applied Physics*. **2011,** 110, 0335057.

# Chapter 3

# Experimental Methodology

*This chapter presents the experiment methodology used in the project, starting from an overview of the experimental setup, follows with the details of methodology used which includes the process fabrication, the design of the proposed test structures, the electromigration testing setup, the physical failure analysis, the in-situ electrical dual beam focused ion beam setup and lastly the simulation method.*

## 3.1 Overview of Experimental Methodology

The overview of the experimental methodology is shown in Figure 4.1 below.

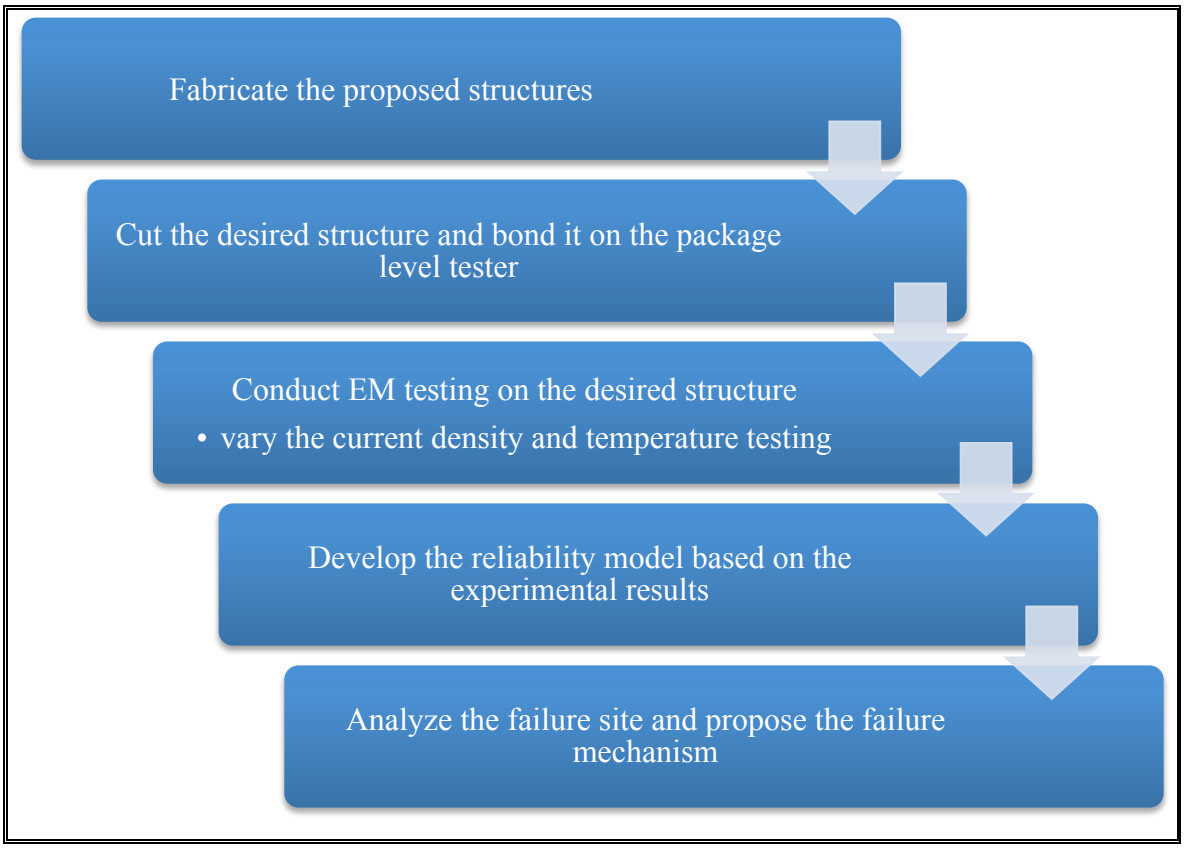


**Figure 3.1** The overview flow of the experimental method.

Firstly, the proposed test structures were fabricated according to the design of experiment. The wafer-dicing machine was used to cut out the chips with the desired test structures. After that, it was attached onto ceramic packages and wire-bonded using gold wires. The electromigration testing was done by using the Micro instrument SPC8010, Xpeqt or Qualitau electromigration system.

Failure analysis was done via FIB (Focused Ion Beam) cutting on the exact failure site for the SEM (Scanning Electron Microscopy) imaging. Based on the failure analysis, the failure mechanism was proposed in order to explain the failure that occurred during the experiment.

## 3.2 Design of the Proposed Test Structures

The unique design of side metal reservoir is introduced in these designs; with the aim to enhance the lifetime of the copper interconnect when it is subjected under electromigration testing in view of pre-existing void. The test structures that were proposed are shown in Figure 3.2.

The test line at M2 level has a metal width of 0.07 μm and the length of the test line is 200 μm. The length of the side metal reservoir, which is located just in front of the vias1 (V1)/ vias2 (V2) interface was varied from 0 μm, 0.03 μm, 0.07 μm and 140 μm. The extrusion monitoring surrounding the metal test line was placed with a spacing of 0.07 μm and width of 0.07 μm to act as a guard ring to monitor for extrusion failure in the metal line, and at the same time to act as a reference structure during the sample failure analysis by FIB/SEM system. The width of the short metal lead line at M1 is 0.3 μm, which is connected to a longer metal lead line at M2 with a wider width of 15 μm, which is much wider when compared with the width of the metal test line. Thus, it would not succumb an electromigration failure during the testing . The vias size was kept 0.07 μm for V1 and V2. Single via contact was used to simplify the analysis of the experiment.

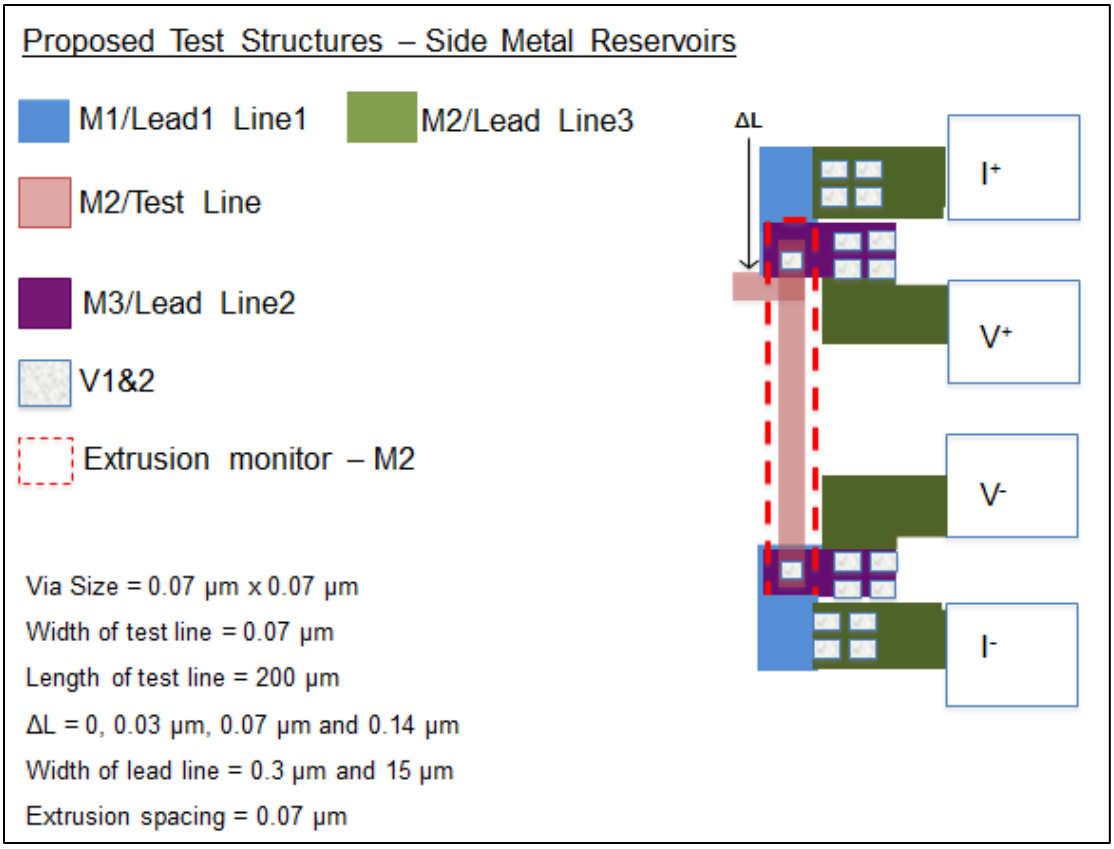


**Figure 3.2** Simplified top view image of test structure - side metal reservoirs**.**

Besides the side reservoir test structure that was proposed, the end of line reservoir test structures were also fabricated in this experiment to act as a reference point when analyzing the lifetime of electromigration as shown in Figure 3.3. The dimensions of the metal test line, metal lead line, metal extrusion monitoring and vias followed exactly as the side metal reservoir test structures.

Both of the test structures (side and end of line metal reservoir) have a stack vias of V1 and V2 at the end of the metal test line. The aim for such a design was to prevent any asymmetrical behavior due to structural design. The side view for both test structures is shown in Figure 3.4.

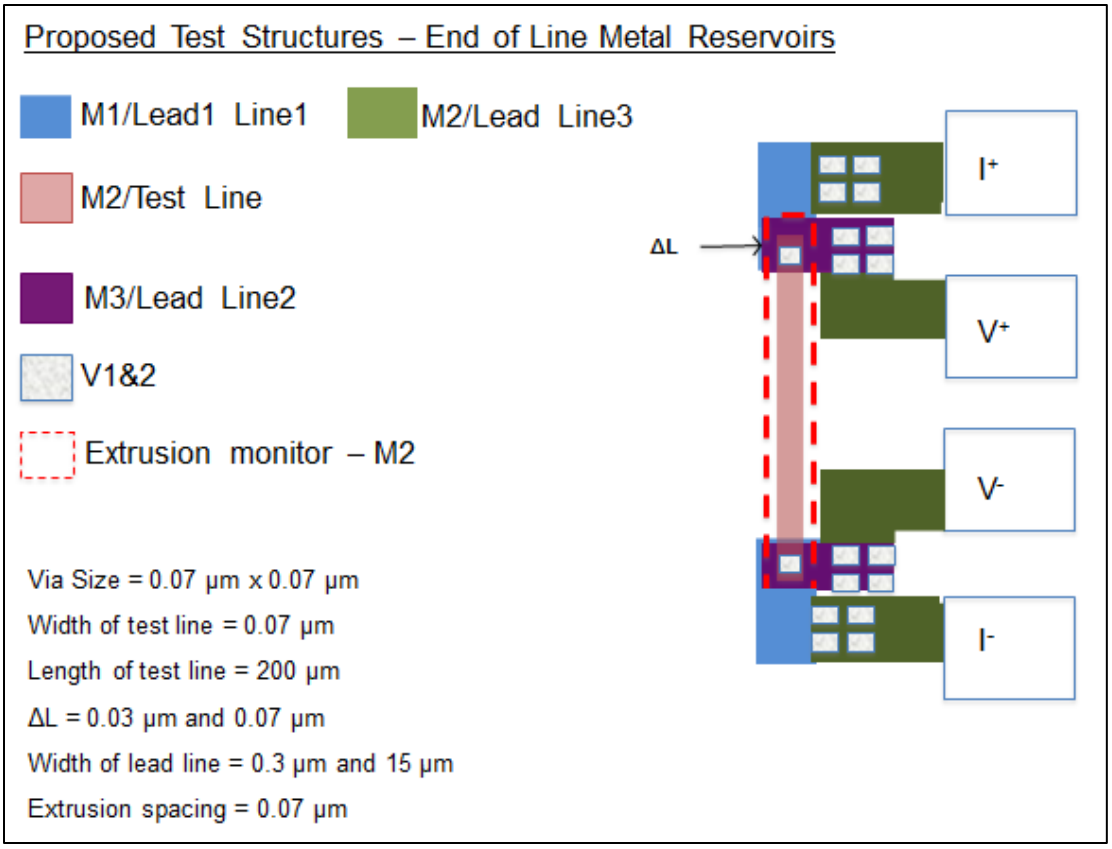


**Figure 3.3** Simplified top view image of test structure – end of line metal reservoirs**.**

The test line of both test structures is on the M2 level, whereas the M1 and M3 would act as lead lines. The current configuration would allow four points measurement setup where the voltage drop would be measured on the top vias (V2) and the current would flow from the bottom vias (V1). This design is to ensure the accuracy of the resistance measurement of the test line during the electromigration testing.

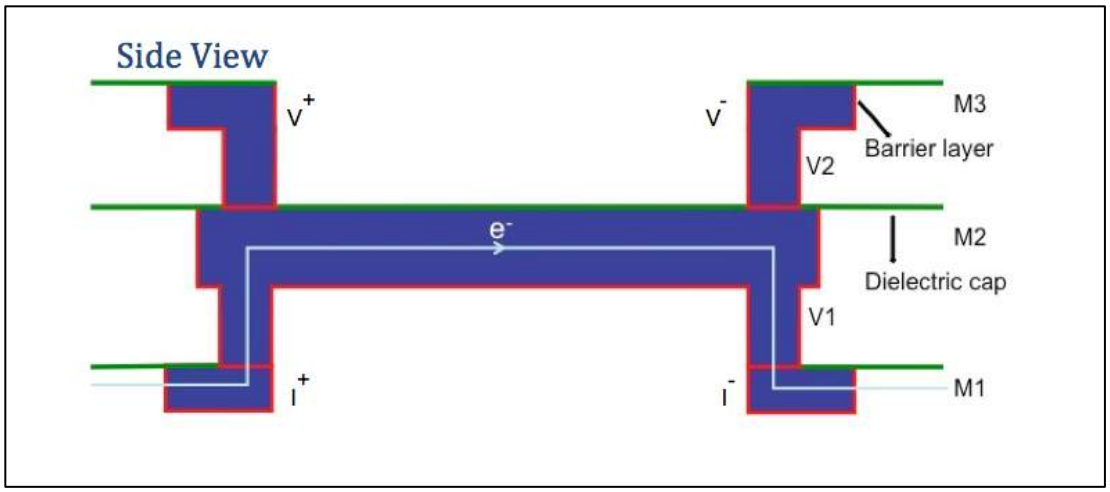


**Figure 3.4** Simplified side view image of both test structures – side and end of line metal reservoirs**.**

## 3.3 Fabrication of the Proposed Test Structures

The proposed test structures were fabricated by using 45nm Cu/low-*k* technology. The whole fabrication process of the test structures was done at Chartered Semiconductor Pte Ltd Singapore (now GlobalFoundries Singapore). The single damascene process was used at first level metallization (M1) and for the subsequent level metallization (M2 and M3), dual damascene process was used during the fabrication. The dielectric material was SiCOH-based and has a dielectric constant of 2.7. A Ta/TaN liner was used as the barrier layer. Lastly, the cap layer was SiN-SiCN-based.

## 3.4 Electromigration Testing Setup

A dicing machine, Disco DFD-651, was used to dice up the fabricated test structures. Then they were bonded onto a 24-pin ceramic package with gold wires using Kaijo wire bonder. The wire bonding was configured to match the four-point measurement configuration on the Micro Instrument SPC8010 (Figure 3.5), Xpeqt or Qualitau system. The Micro Instrument SPC8010, Xpeqt and Qualitau system was able to conduct electromigration and TDDB testing with a maximum temperature setting of 400°C.

During the electromigration testing, a current density of 1 MA/cm$^2$ was used and the stress temperature was 300°C. The lifetime measurement was based on the resistance evolution of the tested metal line. The failure criterion adopted was 10% increase of $R_0$ (initial resistance value at the start of the experiment, i.e. time = 0 s). The stress current passed from metal 1 (M1) lead line to the metal 2 (M2) test line, and back to M1. As for the voltage sensing, it was measured from anode end at metal 3 (M3) to the cathode end, which is located at M3 as well. These configurations of stressing mimic the four-point probe measurement that allows a very accurate measurement of resistance across the metal interconnect test line.


**Figure 3.5** Micro Instrument SPC8010.

## 3.5 Physical Failure Analysis by Dual Beam Focused Ion Beam

Dual beam Focused Ion Beam (FIB) system is mainly being used in the material characterization, semiconductor industry, and many other industries. In the dual beam system, both Scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB) co-exist. The primary function of the SEM is to collect the image. Meanwhile, the FIB is mainly used to remove and deposit some materials. SEM uses an electron to scan the object in order to produce the image. FIB uses ion to remove or deposit some material on the

object of interest. The main advantage of having the dual beam system is the ability to monitor the sample while removing or depositing some materials. Therefore, the accuracy and time efficiency are highly improved. Examples of the applications of the dual beam FIB are Transmission Electron Microscopy (TEM) sample preparation, circuit editing, selective etching, and generation of high resolution imaging under a lower current beam that is able to provide the grain orientation, etc. Here, we used the dual beam FIB, FEI Nova ™ Nanolab DualBeam™ 600i (Figure 3.6), primarily for post-mortem electromigration failure analysis in order to give a better understanding on the failure mechanism.

**Figure 3.6** FEI Nova™ Nanolab DualBeam™ 600i.

## 3.6 *In-situ* Electrical Dual Beam Focused Ion Beam Setup

The dual beam FIB, FEI Nova™ Nanolab DualBeam™ 600i, was enhanced with electrical measurement capability by combining it with a Keithley 6221a current source (Figure 3.7). Cable connection with a vacuum compatible property was crucial in this setup to prevent outgasing during the operation of the dual beam FIB. Not only the cable connection, the material used to solder all the electrical connection must be vacuum

compatible as well. The computer or laptop was used to control the electrical measurement activity and store all the measured data.

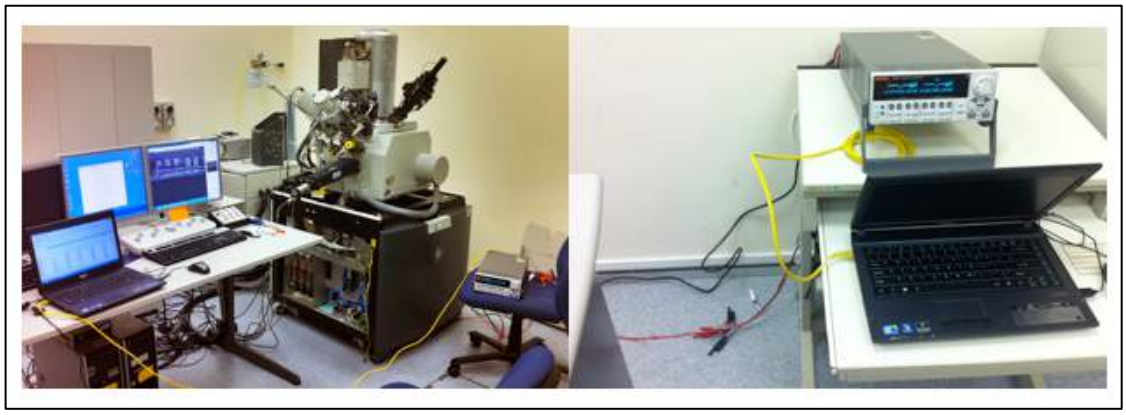

**Figure 3.7** In-situ electromigration dual beam FIB setup.

The introduction of electrical measurement capability into the dual beam FIB would enable the sample or test structure to be stressed electrically while performing a normal task of the dual beam FIB system. Hence, live monitoring on the sample during the electrical testing could be done. One of the very useful applications is to perform a circuitry check on the sample while doing circuit editing by FIB. The other application is to do a live reliability monitoring of the interconnect upon the long current stress, which is usually known as electromigration reliability.

There were few steps required in order to perform live electromigration testing. First, the surface of the sample was coated with platinum (Pt). This was done to prevent charging and drifting during the imaging or cutting of the sample by dual beam FIB. Second, the isolation of the bond pads was essential as shown in the Figure3.8. If this was not done properly, it would cause a short circuit between the sample and the dual beam FIB machine.

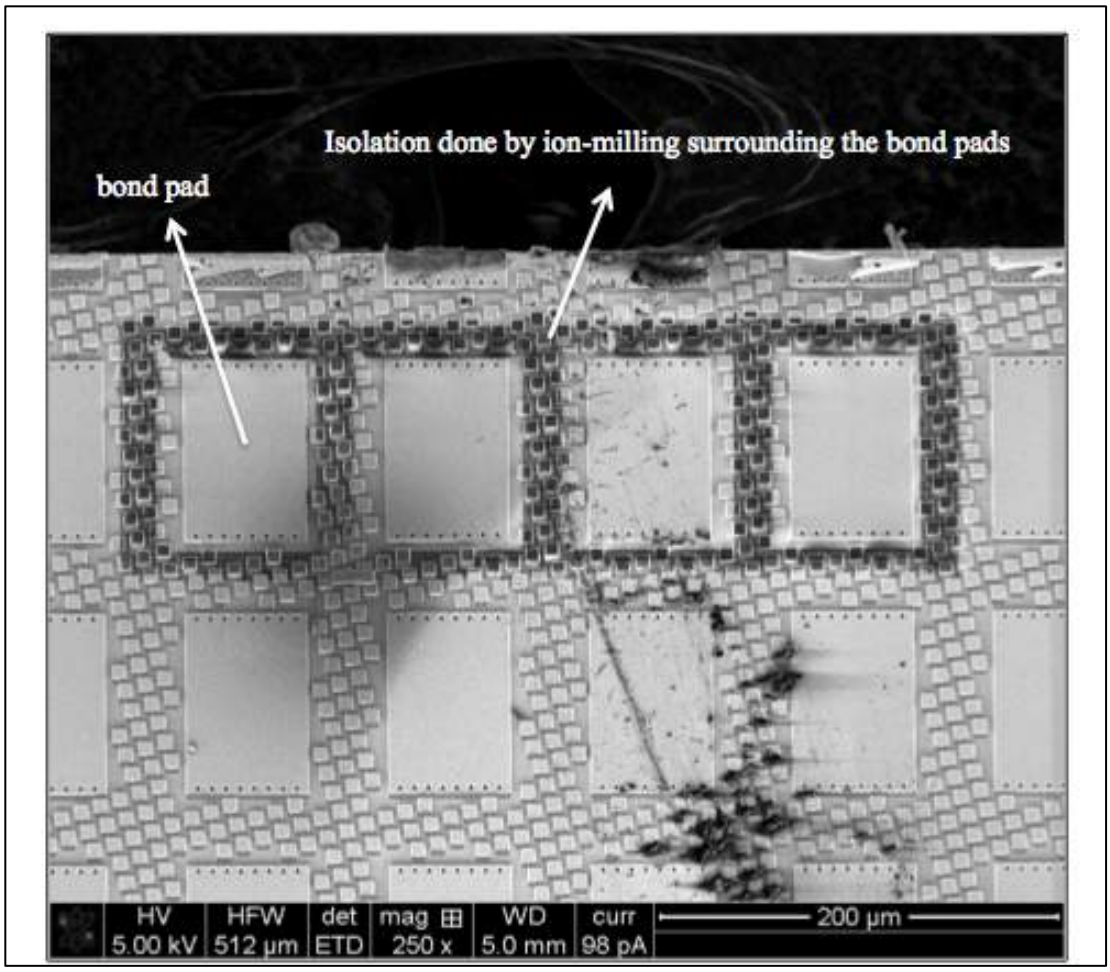


**Figure 3.8** Bond pad isolation by ion-miling FIB.

Third, the sample was bonded onto a 24-pin gold inlaid ceramic package, and the ceramic package was fully shielded by copper tape with good grounding (Figure 3.10). This was to prevent sample drifting or charging as well during the FIB operation. Fourth, during the cross section of the area of interest by FIB, there was a need to leave a thin low-*k* in front of the targeted metal interconnect test line so as to prevent oxidation of the metal interconnect. Fifth, the setup of the electrical connection with Keithley 6221a to the sample package must be properly grounded to minimize any noise interference during the electrical testing. Lastly, the laptop or computer was connected to the Keithley 6221a in order to conduct the electrical measurement and record its electrical history with respect to the live monitoring on the sample.

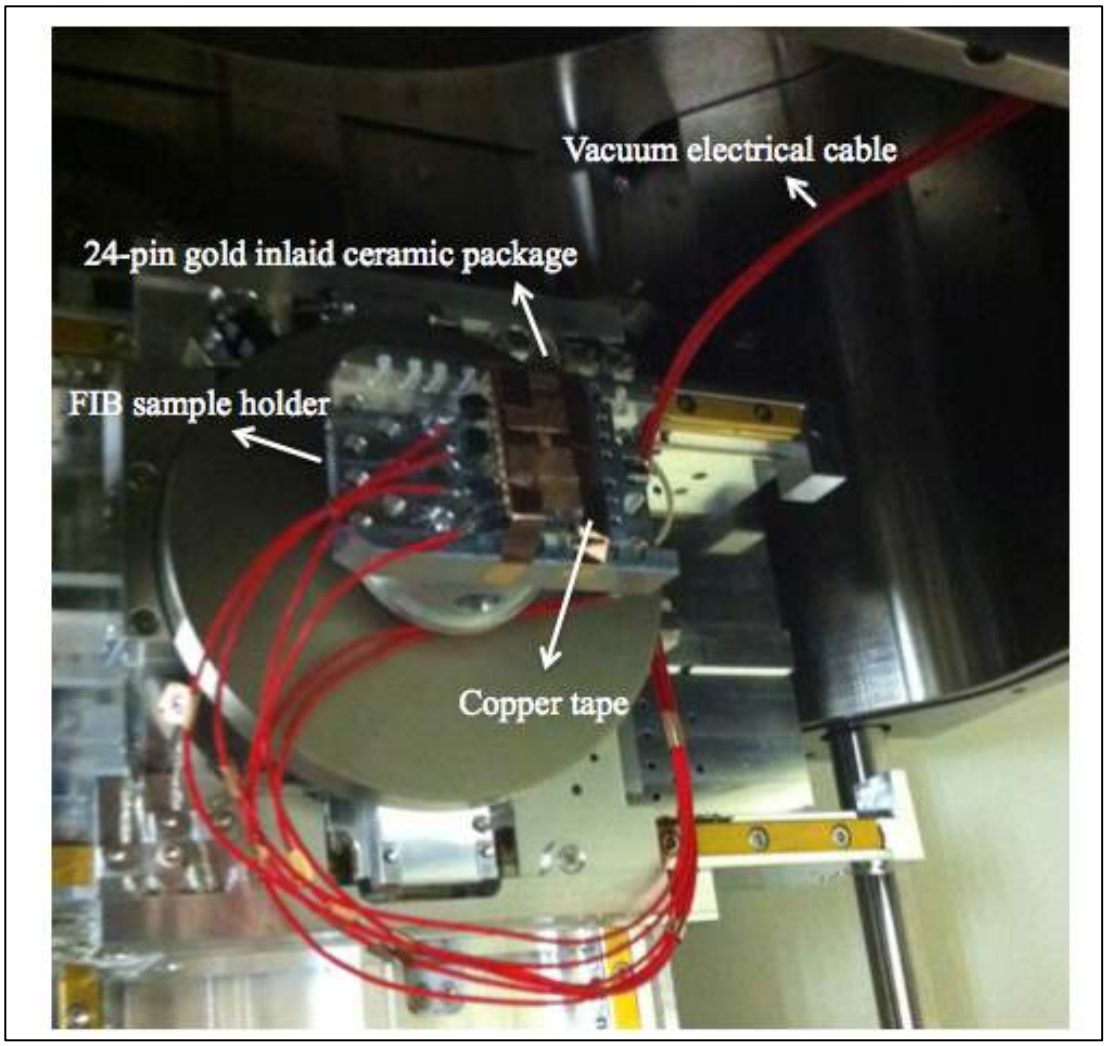


**Figure 3.9** *In-situ* electromigration test setup within a FIB system**,** 24-pin gold inlaid ceramic package, with electrical connection to Keithley 6221a.

## 3.7 Modeling and Simulation

A numerical solver based on the simple 1D model of Korhonen *et al.* [1] was used to simulate the stress evolution along a 200 μm long and 70 nm wide Cu interconnect. The hydrostatic stress σ at any position *x* along the length of an interconnect segment is given by

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB}{kT}\left(\Omega \frac{\partial \sigma}{\partial x} + z^{*} q\ \rho\ j\right)\right] \qquad (3.1)$$

Where $D$, $k$, $T$, $\Omega$, $q$, $z^*$, $\rho$ and $B$ were explained earlier in the chapter 1, electromigration section.

The details of the numerical solver are described elsewhere [2] and the parameters used in the simulations were shown in Table 3.1.

**Table 3.1** Parameters used in simulations.

| Parameter | Value |
|---|---|
| $\sigma_{nuc}$ | 25 MPa [3] |
| $z^*$ | 1 [4] |
| $B$ | 10 GPa [5] |
| $\Omega$ | $1.18 \times 10^{-29}$ $m^{-3}$ |
| $D_0$ | $1.232 \times 10^{-9}$ $m^2/s$ [6] |
| $\rho$ | 4.623 μΩ-cm (at 300°C) |
| $\Delta H_{eff}$ | 0.8 eV [7] |

**References:**

[1] M.A. Korhonen, P. Borgesen, K.N. Tu, and C.Y. Li. *J. Appl. Phys.* **1993,** 73, 3790-3799.

[2] Z. S. Choi. *Ph.D. thesis, Massachusetts Institute of Technology.* **2007**.

[3] C.S. Hau-Riege, S.P. Hau-Riege and A.P. Marathe. *J. Appl. Phys.* **2004,** 96, 5792-5796.

[4] C. K. Hu, R. Rosenberg, and K. Y. Lee. *Appl. Phys. Lett.* **1999,** 74, 2945-2947.

[5] F.L. Wei, C.S. Hau-Riege, A.P. Marathe, and C.V. Thompson. *J. Appl. Phys.* **2008,** 103, 084513-084513-11.

[6] C. L. Gan, C. V. Thompson, K. L. Pey, and W. K. Choi. *J. Appl. Phys.* **2003,** 94, 1222-1228.

[7] K. D. Lee, E. T. Ogawa, H. Matsuhashi, P. R. Justison, K.-S. Ko, and P. S. Ho. *Appl. Phys. Lett.* **2001,** 79, 3236-3238.

# Chapter 4

# Results and Discussion

*In this chapter, it is divided into 5 sub chapters, namely impact of pre-existing void to the electromigration lifetime, modeling and simulation, side metal reservoir versus end of line metal reservoir, side metal reservoirs with various lengths and lastly, in-situ electromigration on side metal reservoir. The details of the results and discussion from each sub chapter will be highlighted in this chapter.*

## 4.1 Impact of Pre-existing Void to the Electromigration Lifetime

Based on the Black's Law equation [1], $t_{50}$ is given by:

$$t_{50} = \left(\frac{A}{J^n}\right) \exp\left(\frac{E_a}{KT}\right) \qquad (4.1)$$

where $t_{50}$ is the median-time-to-failure, $A$ is a constant dependent on the material and geometry, $j$ is the current density, $n$ is a constant that relates to the failure kinetics, $E_a$ is the activation energy for failure, $k$ is Boltzmann's constant and $T$ is the temperature.

As discussed earlier in Chapter 2, the value $n$ can range from 1 to 3. When $n$ = 1, it means that void growth is the main mechanism in determining electromigration failure [2]; while with $n$ = 2, the dominating mechanism is void nucleation [3]. If $n$ rises above 2, the electromigration mechanism is attributed to joule heating [4]. In most cases, $n$ will lie between 1 and 2, which means both void nucleation and growth mechanisms are playing a role in the failure [5]. However, in the case of pre-existing void, it can be assumed that no void nucleation takes place and only void growth determines the failure time, giving a $n$ value of 1.

In order to predict how much $t_{50}$ will be impacted by the pre-existing void reasonably, the first assumption is that the location of the pre-existing void is at a distance away from the cathode but not greater than $L_{c.cr}$ [6] and the void is not large enough to cause an early failure. Thus, the pre-existing void will experience void growth without void nucleation before it causes failure in the copper interconnects.

Based on the $t_{50}$ equation above, for the case without pre-existing void, where both void nucleation and growth take place, $t_{50}$ can be represented as:

$$t_{50nor} = t_{nuc} + t_g = \left(\frac{A_1}{J} + \frac{B}{J^2}\right) \exp\left(\frac{E_{a1}}{KT}\right) \qquad (4.2)$$

While for the interconnect with pre-existing void, since only void growth takes place, it can be represented as:

$$t_{50pre} = t_g = \left(\frac{A_2}{J}\right) \exp\left(\frac{E_{a2}}{KT}\right) \qquad (4.3)$$

With the assumption that $A_1$ is equivalent to $A_2$, and $E_{a1}$ is equivalent to $E_{a2}$, $K$ and $T$ are the same for both cases. Therefore, the ratio of $t_{50nor}/t_{50pre}$ is given by:

$$\frac{t_{50nor}}{t_{50pre}} = 1 + \left(\frac{B/A_1}{J}\right) \qquad (4.4)$$

This shows that the $t_{50nor}$ will always be larger than $t_{50pre}$ because the second component of the equation will always be positive. Further estimation can be made here by assuming that the value of $A_1$ is equivalent to $B$, and for a current density $J$ of 2 MA/cm$^2$, $t_{50nor}$ will be 1.5 times longer than $t_{50pre}$.

In the studies done by G. Marti *et al.* [7] and L. Arnaud *et al.* [8], they conducted experiments and simulation with a specially designed test structure, which is able to detect an early void formation before a full spanning void is formed. With such a structure, they were able to decouple the contribution of void nucleation time (TN) from the $t_{50}$ (TTF or TF) as shown in both Figures 4.1 and 4.2 below.

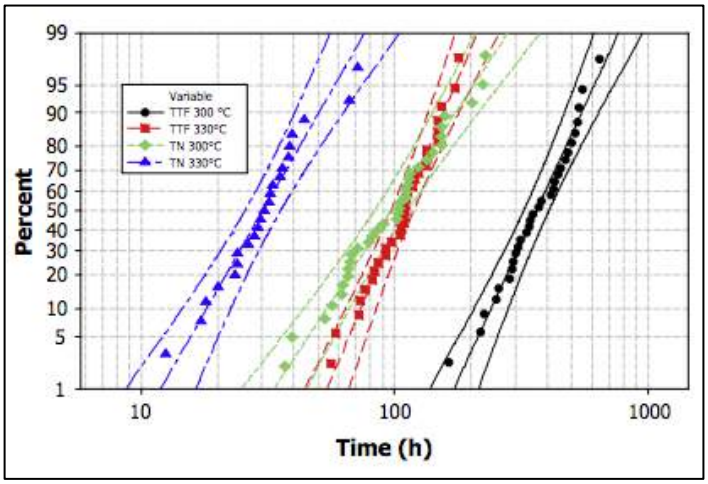


**Figure 4.1** Time to failure (TTF) and Time of Nucleation (TN) calculated respectively with the SSV and LSS at accelerated conditions of temperature accelerated conditions of temperature [7].

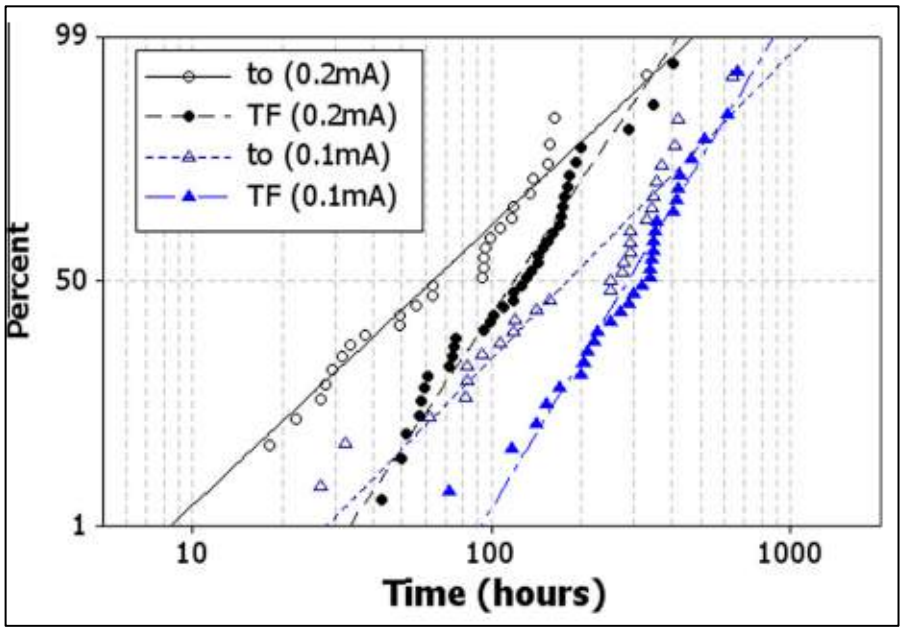


**Figure 4.2** Cumulative distributions of TF and $t_0$ for 2 currents for the sample with CuAl seed process [8].

Referring to their data which is under a current density stress between 2 – 3 MA/cm$^2$, the contribution of the void growth time to the overall $t_{50}$ can be calculated, which is around 70% [7] and 50% ~ 60% [8],. Thus it can be inferred that with any pre-existing void, there is at least 30% to 50% $t_{50}$ reduction when compared to the case where a void needs to be nucleated first before it undergoes the growth mechanism. This is consistent with the estimation made earlier using Black's Law.

However, it is to be noted that the actual impact of the pre-existing void to the overall lifetime of copper electromigration may vary depending on the condition of the experiments and samples. Nevertheless, from the discussion above, it clearly shows that with the pre-existing void, the interconnect will have a significantly shorter lifetime.

## 4.2 Modeling and Simulation

The impact of the pre-existing void has not been well studied yet especially in their roles during the electromigration. The stress model simulation was done to analyze the impact of pre-existing voids at different locations along the copper interconnect. In these simulation, first it is assumed that the pre-existing void has present in the copper interconnects. Second, the stress around the pre-existing void will be relaxed. It is assumed that the stress at the pre-existing void location is zero. Further assumptions were made in these simulations, the pre-existing void is partial spanning (i.e. does not span the thickness of the line), the pre-existing void is pinned at a fixed location (e.g. a grain boundary), the diffusivity is uniform in the interconnect, and that current crowding and Joule heating around the void are negligible.

There are two cases that were simulated in this study. First, when the pre-existing void was pinned at a considerable distance away from the cathode, for this simulation 10 μm was used (Figure 4.3 (a)), Second, when the pre-existing void was pinned close enough at the distance of 2 μm away from the cathode (Figure 4.3 (b)).

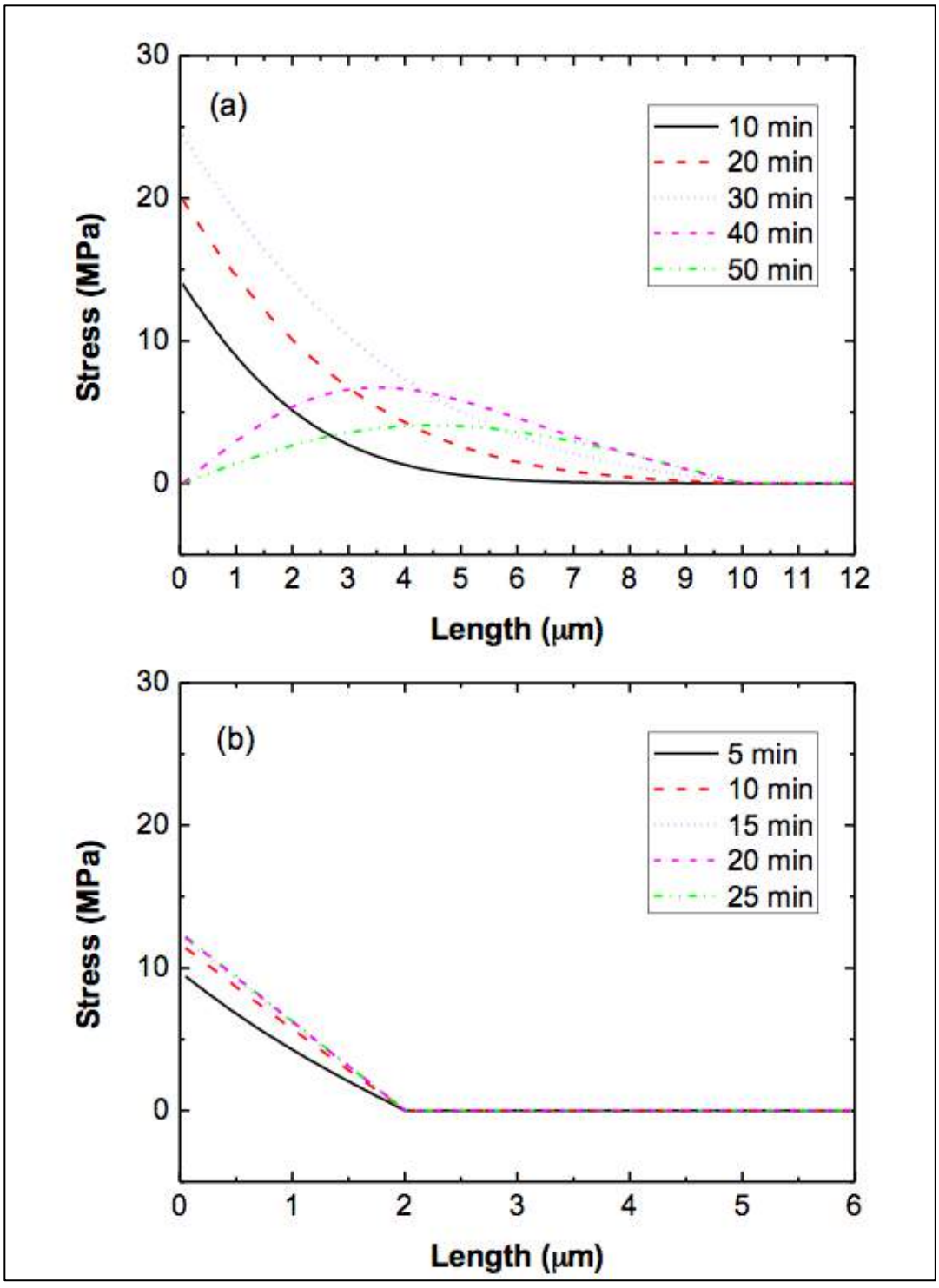


**Figure 4.3** Stress profile evolution at the cathode end of a 200 μm-long interconnect that has a pre-existing void at (a) 10 μm, and (b) 2 μm away from the cathode via ($j$ = 1.0 MA/cm2, $T$ = 300°C).

In the first case, it could be observed that the pre-existing void did not have any impact on the stress evolution in the copper interconnect. Thus, it leads to the well known stress impact behavior during the electromigration that resulting on the void nucleation at the cathode due to the maximum tensile stress build up there (i.e. same as without the pre-existing void).

In contrast on the second case, when the pre-existing void was pinned nearer to the cathode, it changes the stress profile at the cathode via, where the tensile stress build up at the cathode via quickly reached a steady-state condition. The steady-state condition is achieved due to the balance between the electron wind force in the direction toward the anode via with the back-stress from the void to the cathode in the opposing direction (Figure 4.3 (b)). Under this condition, if the maximum steady state tensile stress at the cathode via is lower than the critical stress for void nucleation, an additional new void beside the pre-existing void will not nucleate. This scenario is similar to the well-known Blech phenomenon [9], and an analogous critical distance between the cathode via and pre-existing void $L_{crit}$ can be determined as

$$L_{crit} = \frac{\Omega(\sigma_{nuc} - \sigma_0)}{jqz^* \rho} \qquad (4.6)$$

Where $\sigma_0$ is the initial stress, here taken to be zero. With the parameters in Table 3.1, $L_{crit}$ is determined to be 4.0 μm for $j$ = 1.0 MA/cm$^2$ and $T$ = 300°C. As seen from Eqn. (4.6), as $j$ is decreased, $L_{crit}$ increases, implying that the probability of void nucleation at a cathode via when pre-existing void is present in the copper interconnect is lower in actual used condition than under accelerated testing due to the lower used current density.

Under continued current stressing, the pre-existing void that is pinned within the critical distance $L_{crit}$ (for $L_{crit} \leq$ 4.0 μm) will continue to grow, even though it prevents an additional void to nucleate at the cathode via (Figure 4.4). This is because while there is a driving force for the flux of atoms out of the pre-existing void towards the anode, the force balance between the pre-existing void and the cathode via prevents flux of atoms into the pre-existing void. On the other hand, a pre-existing void that is pinned at a distance greater than $L_{crit}$ will grow initially and then saturate (for $L_{crit}$ > 4.0 μm). An

additional new void will nucleate eventually at the cathode via and relaxes the stress. This is due to the stress evolution behavior that was explained earlier where under continued current stressing, the tensile stress would continue to build up at the cathode via until it reaches the critical void nucleation stress. This means that the new void nucleated at the cathode via will continue to grow due to the electron wind force only (no back-stress presence here), while the pre-existing void experiences zero net atomic flux and thus its volume saturates.

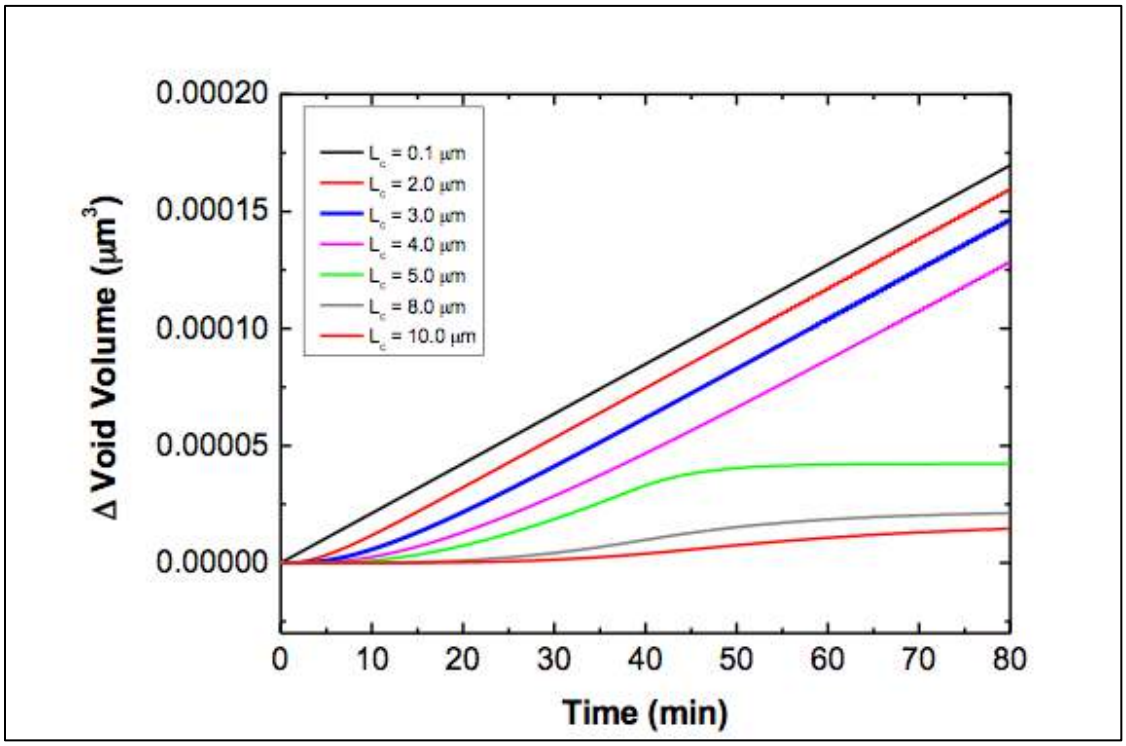


**Figure 4.4** Change in void volume as a function of time of pre-existing voids at different distances from the cathode via $L_c$ ($j$ = 1.0 MA/cm2, $T$ = 300°C).

In the preceding discussions, it has been assumed that the pre-existing void is pinned to a location (e.g. grain boundary) and diffusivity is uniform in the metal interconnect and. In the actual case, these two assumptions may not be true at all, which may lead to the different observations seen experimentally. First, if the pre-existing void is not pinned to a specific location; it will just drift towards the cathode via (opposing the electron wind force direction) without a volume change since there is no atomic flux divergence. Consequently, it means that a void observed at the cathode via from failure analysis post-

mortem after electromigration testing may not necessarily comes from a void nucleation event due to the stress evolution in the metal interconnect. Moreover, the pre-existing void may drift towards the cathode via before the steady-state stress is achieved between the pre-existing void and the cathode via. Second, if the diffusivity varies in the grain of the metal interconnect, a flux divergence can occur and the pre-existing void will grow or shrink, depending on the difference in grain diffusivity on the anode and cathode side of the pre-existing void as seen in the recent in-situ experiment [10]. However, if the pre-existing void lies within $L_{crit}$, it will still grow eventually based on the earlier discussion [12].

The simulation done revealed that the pre-existing void would definitely impact the stress evolution in the copper interconnects, depending on whether it is pinned on the specific location (greater or smaller than $L_{crit}$) or not. And if it is not pinned, it will drift towards the cathode via and induce a back-stress when the pre-existing void is close enough to the cathode via. From the prior discussions above and observations from recent in-situ experiment results, it is highly suggested that the event of pre-existing void drifting is more likely to happen rather than pinning at the specific location.

The side metal reservoir is designed with the purpose of acting as a void-trap toward the drifting of pre-existing void that in return will improve the overall lifetime of the metal interconnects.

## 4.3 Side Metal Reservoir Versus End of Line Metal Reservoir

The electromigration experiments were conducted for both side metal reservoir and end of line metal reservoir with the same methodology as being explained in the chapter 3. The purpose for such experiments is to compare the lifetime of both test structures in view of the presence of the pre-existing void that might occurs and drifts during the electrical stressing.

Figure 4.5 shows the plane view layout of the test structures. The total length and width of both interconnects are 200 µm and 70 nm, respectively. Figure 4.5(a) shows the typical end of line extension structure, with a 70 nm long end extension. Figure 4.5(b) shows the side reservoir test structure. Both the length and width of the side reservoir are 70 nm and it is placed just at the edge of the cathode via. The SEM image of both test structures at the end of cathode side is shown in the Figure 4.6 with the indication of the current direction during the experiment.

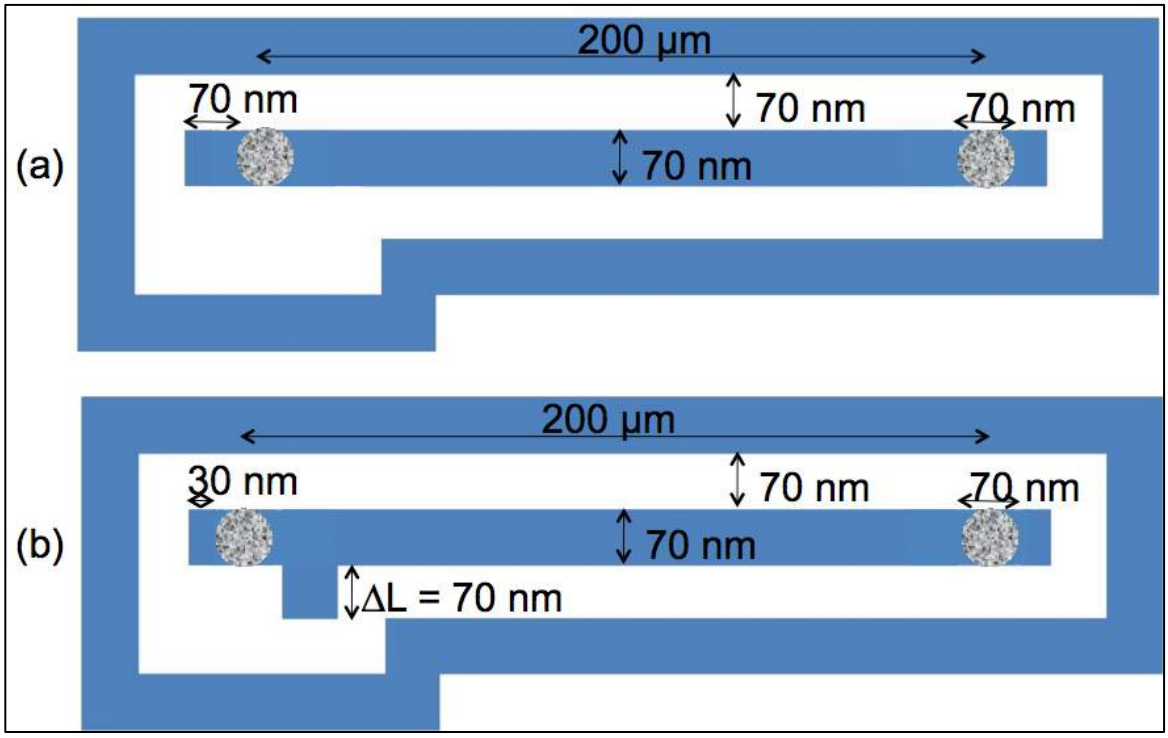


**Figure 4.5** Plane view of the samples. (a) End of line metal reservoir, (b) Side metal reservoir.

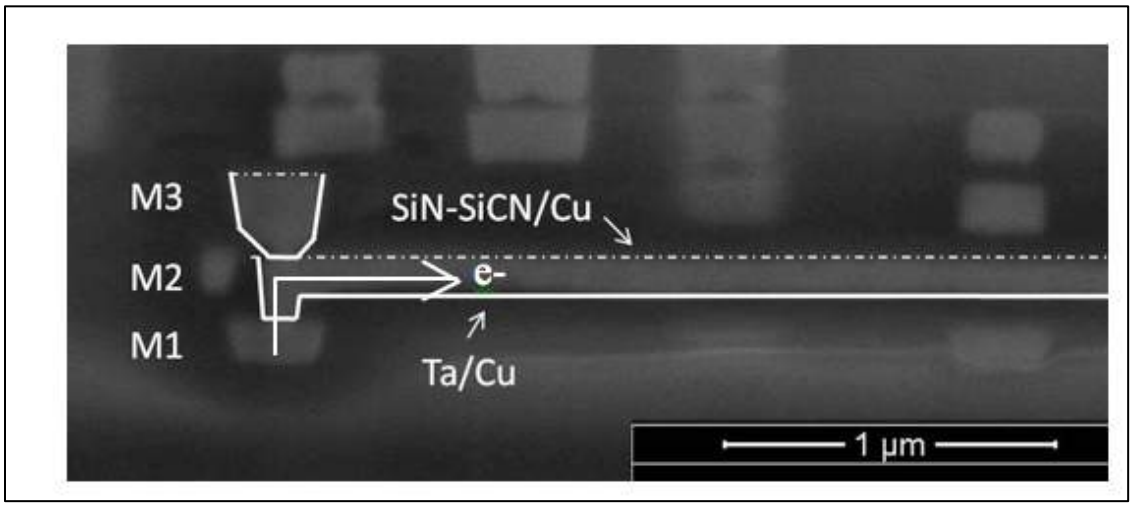


**Figure 4.6** Side view SEM image of both samples at the cathode end.

The results from the experiments are shown in Figure 4.7, table 4.1, Figure 4.8 and Figure 4.9. In the Figure 4.7, it shows the time to failure distribution for samples with side metal reservoirs and end of line metal reservoirs. The failure criterion as per defined in the chapter 3, experimental methodology.

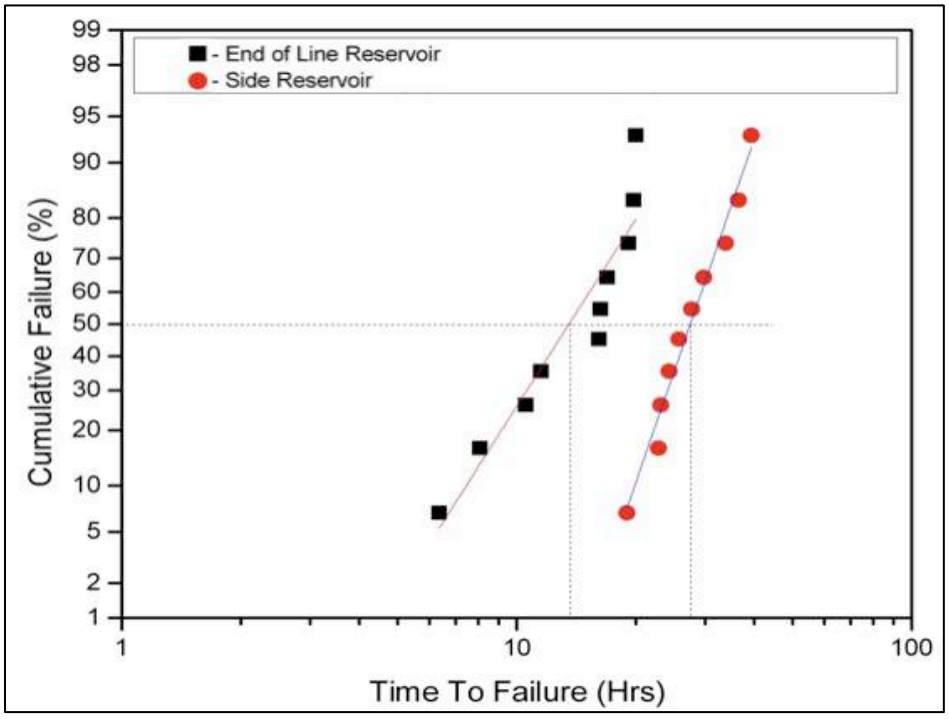


**Figure 4.7** The time to failure distribution for the end of line metal reservoir and side metal reservoir test structures.

The statistical analysis in Table 4.1 shows that the electromigration lifetime nearly doubled for the samples with side metal reservoirs as compared to those with end of line metal reservoirs, indicating that side metal reservoirs are more effective in enhancing the lifetime of metal interconnect than the end of line metal reservoirs.

**Table 4.1** $T_{50}$ of end of line metal reservoir and side metal reservoir test structures.

| Sample | $t_{50}$ (hrs) | % Change |
|---|---|---|
| End of Line Metal Reservoir | 13.57 | - |
| Side Metal Reservoir | 27.54 | 102.95% |

Figures 4.8(a) and (b) show resistance versus time evolution for a sample with an end of line metal reservoir and a sample with a side metal reservoir, respectively. For the end of line metal reservoir structure, the resistance remained fairly constant during current stressing before it rapidly increased to cause an open circuit failure. On the other hand, for the side metal reservoir structure, Figure 4.8(b) shows that the resistance profile actually decreased first before it gradually increased to a very high resistance value.

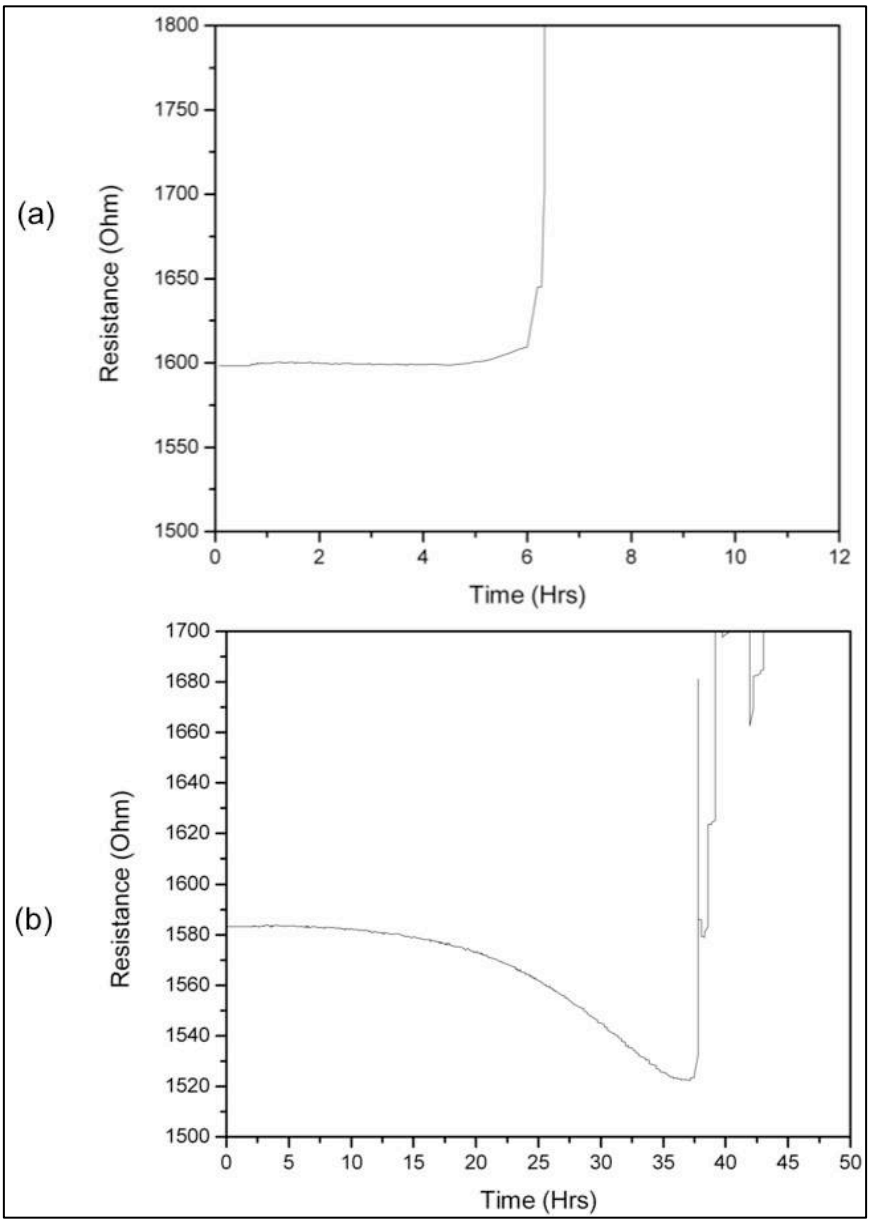


**Figure 4.8** Resistance profile for the samples. (a) End of line metal reservoir, (b) Side metal reservoir.

The resistance profile for the end of line metal reservoir structure is typical for cases where the pre-existing void, which has drifted to the end of cathode via [10, 11, 12], or the void, which nucleated due to critical tensile stress at cathode via, that grows to fully span the whole cross-section of the line, at which point the current shunts across the line and leads to the rapid increase in resistance. This may lead to a fast breakdown of the

liner due to joule heating. This is consistent with the images obtained from failure analysis as shown in Figure 4.9.

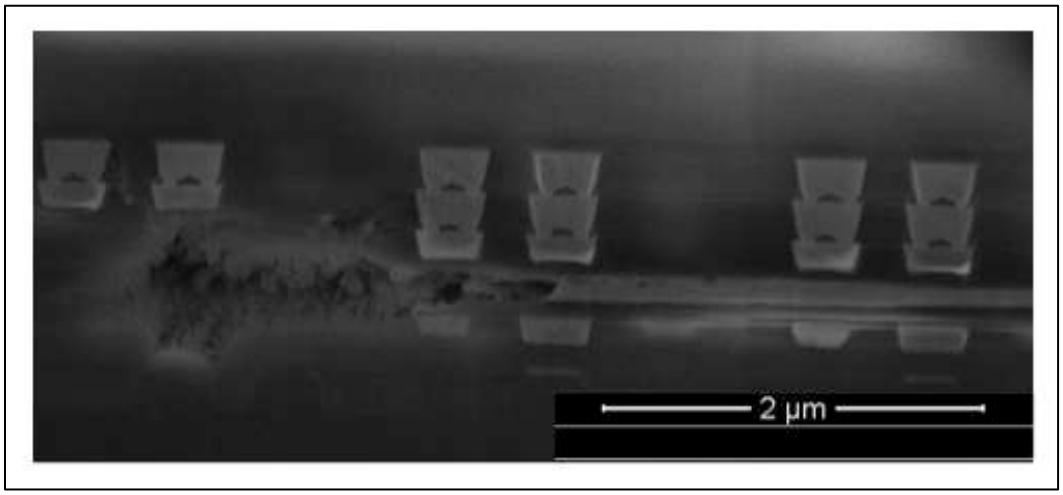


**Figure 4.9** Failure analysis cut by using focused ion beam at the cathode end of line.

In contrast, the gradual resistance decrease observed for the side reservoir structure is unusual. This may indicate that the interconnect has pre-existing voids initially, and when these pre-existing voids drift toward the cathode via, these pre-existing voids may move into the side reservoir and get "trapped". However, as the pre-existing void grows bigger over time under a continued current stressing, it eventually will cause an open circuit failure. It is also suggested that the event of typical void nucleation at the end of cathode via did not occurred during this experiment.

Based on the results so far, it is clearly seen that the side metal reservoir is more effective in enhancing the lifetime of the metal interconnect and its resistance profile over the stressing time clearly suggested that the side metal reservoir might able to trap the pre-existing void and prevents the void nucleation at the end of cathode via.

There are there factors that likely to lead to such observations and results on the side metal reservoir structure. First factor, the electromigration-induced stress evolution with pre-existing void in the metal inteconnect. As being discussed in the simulation part earlier, a stress gradient will develop between the pre-existing void and the cathode via,

with a tensile stress developing at the cathode via but zero stress at the pre-existing void edge [6, 13], when the pre-existing void drifted close enough to the end of cathode via. This gradient of back-stress opposes the electron wind force. On the other hand, there is no back stress in the side metal reservoir due to the absence or minimal current flow. Therefore, it leads to the pre-existing void to grow into the side metal reservoir rather than continue to migrate toward the cathode via. Eventually the side metal reservoir volume is consumed and the void continues to grow toward the cathode via and cause failure under a continued current stressing. And as discussed earlier in the simulation, the presence of the pre-existing void at the side metal reservoir that is close enough to the cathode via will leads to a lower probability of reaching a critical tensile stress at the end of cathode via. Thus, it prevents any new void nucleation there.

Second factor, the presence of Ta/Cu interface just at the end of cathode via. This is schematically illustrated in Figure 4.10. As being discussed earlier in the Chapter 2.5, the Cu or Cu/cap interface plays a significant role in term of altering the electromigration lifetime [14, 15, 16, 17, 18, 19, 20, 21, 22,]. In this experiment, initially the pre-existing voids drift along the SiN-SiCN/Cu interface towards the cathode via due to the electron wind force. As the pre-existing voids get nearer to the cathode via, they must move toward the Ta/Cu interface in order to reach the end of the cathode via line. However, it suggested that the pre-existing voids would prefer to stay on the SiN-SiCN/Cu interface and grow into the side metal reservoir, rather than move along the Ta/Cu interface. This is due to the stronger adhesion strength of the Cu atoms with the Ta liner as compared to that with the SiN-SiCN cap [14, 15]. Therefore, it is harder for the Cu atoms to debond from the Ta liner than from the SiN-SiCN cap. As a result, the pre-existing voids will drift and be trapped at the side metal reservoir. Under a continued current stress, the electromigration force will continue to drive the pre-existing voids and vacancies toward the cathode and eventually the void will grow and extend over the cathode via end of the interconnect and cause a failure.

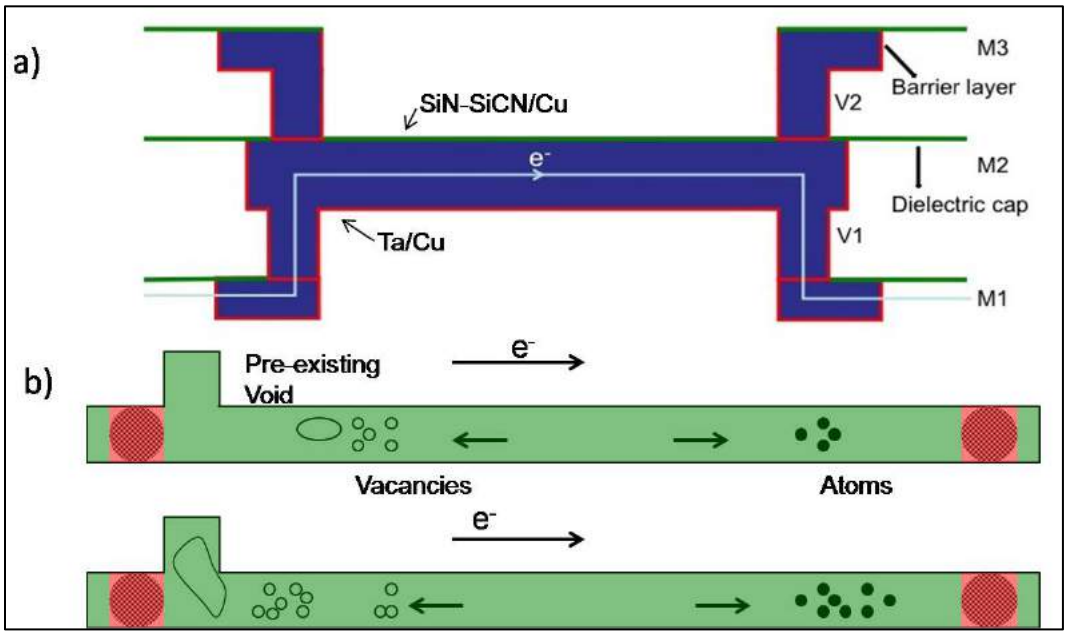


**Figure 4.10** The proposed mechanism on how the side metal reservoir works. (a) The side view, (b) The top view of the side metal reservoir structure.

The third factor is the current crowding or current density gradient effect that exists naturally due to the metal side reservoir configuration as shown in Figure 4.11, whereby COMSOL simulation was used to simulate the current density in the various length of side metal reservoir.

From the simulation, it clearly shows that the smallest current density is located at the side metal reservoir. Consequently, it will cause the pre-existing void to drift into the side metal reservoir when it is moving towards the end of cathode line. However, as being studied and observed by others, a void does not necessary nucleate at the location of the lowest current density [11, 12, 23]. In fact, voids were found drifting from the middle of cathode line and stopped right at the end of cathode line before it grew into the end-of-line metal reservoir [11, 12]. Similar observation was made on the bended $90^0$ angle test structure, whereby the void was not found at the lowest current density location [23]. Therefore, the effect of current crowding can be considered negligible as well in the side metal reservoir configuration.

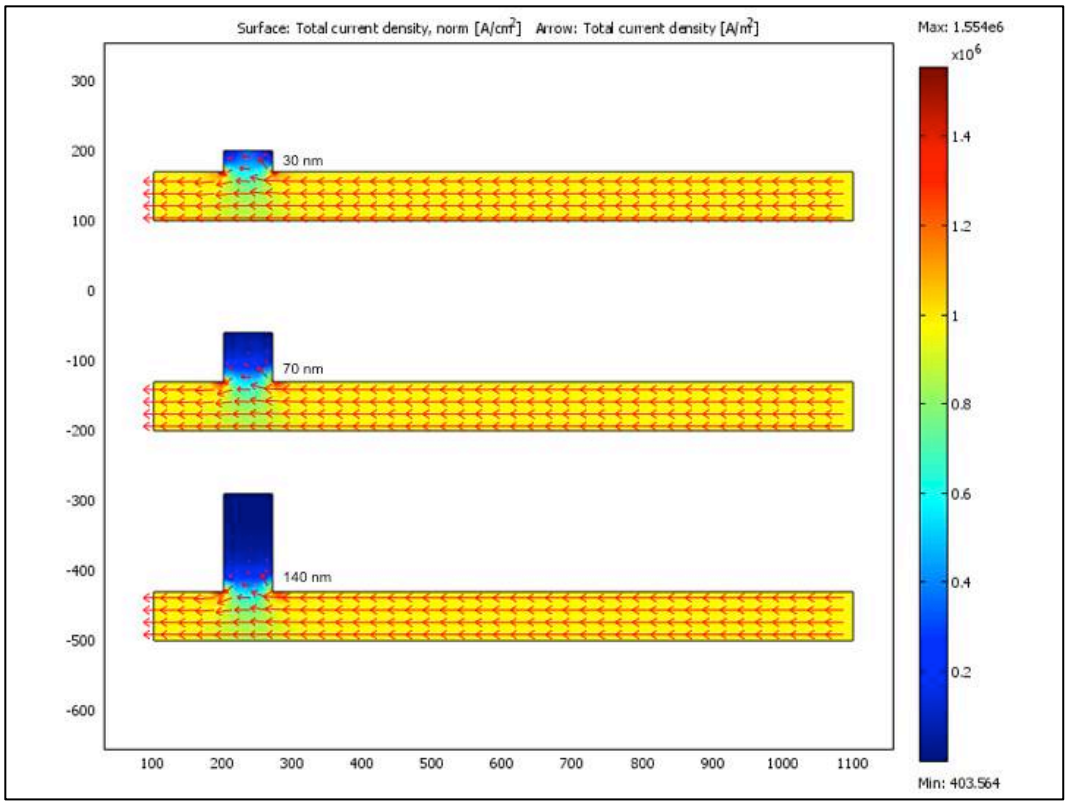


**Figure 4.11** Current crowding and gradient simulation on the various lengths of side metal reservoir structure (top view).

## 4.4 Side Metal Reservoir with Various Lengths

The effectiveness of the side metal reservoir in improving the lifetime of metal interconnect was further investigated. Figure 4.12 shows the plane view layout of the test structure for the next experiment. The total length and width of the interconnect were 200 µm and 70 nm, respectively. The width of the side reservoir was 70 nm and the length was 0 (i.e. no side reservoir), 30 nm, 70 nm and 140 nm. It was placed just at the edge of the cathode via. These test structures were subjected under the same electromigration testing as the earlier experiment.

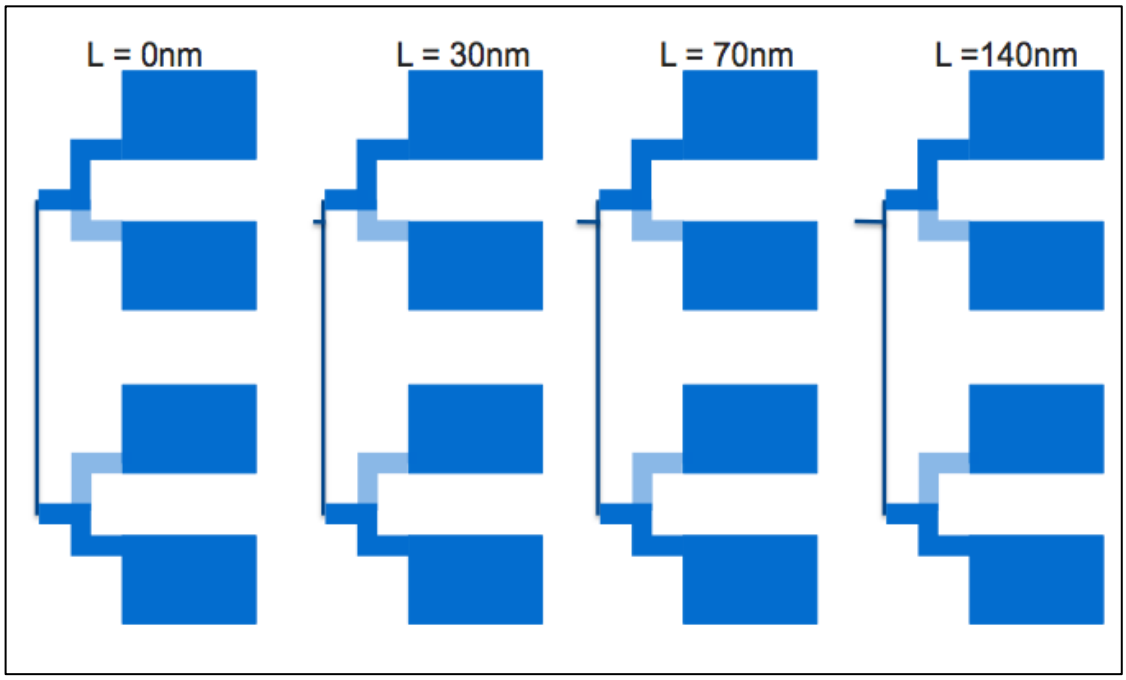


**Figure 4.12** The simplified top view images of the side metal reservoirs used in the experiments with length = 0, 30 nm, 70 nm and 140 nm.

The results from this experiment are shown in the Figure 4.13 and Figure 4.14. Figure 4.13 shows the lifetime distributions on the side metal reservoir test structures with different length of side metal reservoir. The failure criterion is defined in chapter 3, experimental methodology. The median-time-to-failure, $t_{50}$, obtained was 4.4 hrs, 15.7 hrs, 27.5 hrs and 24.9 hrs for the 0 nm, 30 nm, 70 nm and 140 nm side reservoir, respectively. It clearly shows that when the side reservoir is introduced, the lifetime of the interconnect line has improved. This further confirmed the results of the earlier experiment. However, the lifetime of the 70 nm and 140 nm side reservoir are comparable, which seemed to imply that there is a saturation length of the side reservoir for it to be further effective.

Another observation is that for the interconnect without the side reservoir (i.e. 0 nm), there are 2 samples which had failed much earlier. On the other hand, no early failures are recorded for the side reservoir test structures, which suggested that the presence of side metal reservoir is able to prevent such cases. This will be further explained on the subsequent discussion.

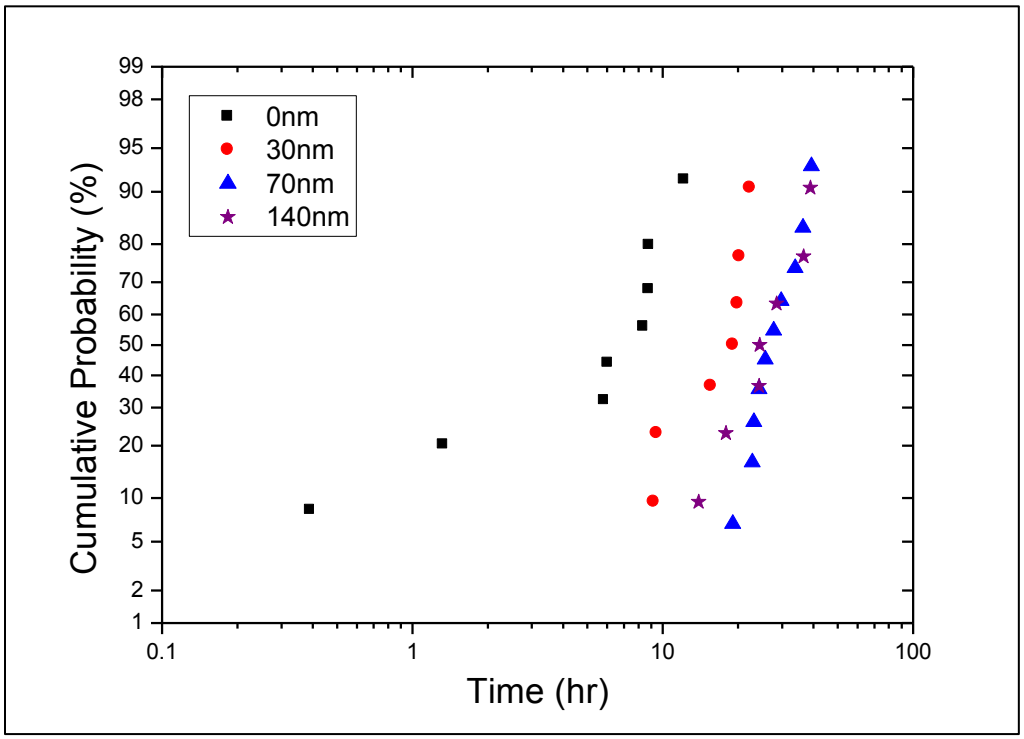


**Figure 4.13** Time to failure distributions for the different lengths of side metal reservoir test structures.

Figure 4.14 shows the SEM failure analysis images of the 140 nm side reservoir test structure through cross-sectioning cuts using the FIB system. The images were taken at different locations along the line as indicated, with the numbering indicating the sequence. The number one position was at the metal ring guard. Position number two was at the via of the test structure, where void was not observed in the line or via. Position number three was just at the edge of the side reservoir to the cathode via, and void could not be detected yet. At position number four, which is at the side reservoir position, a void could be found.

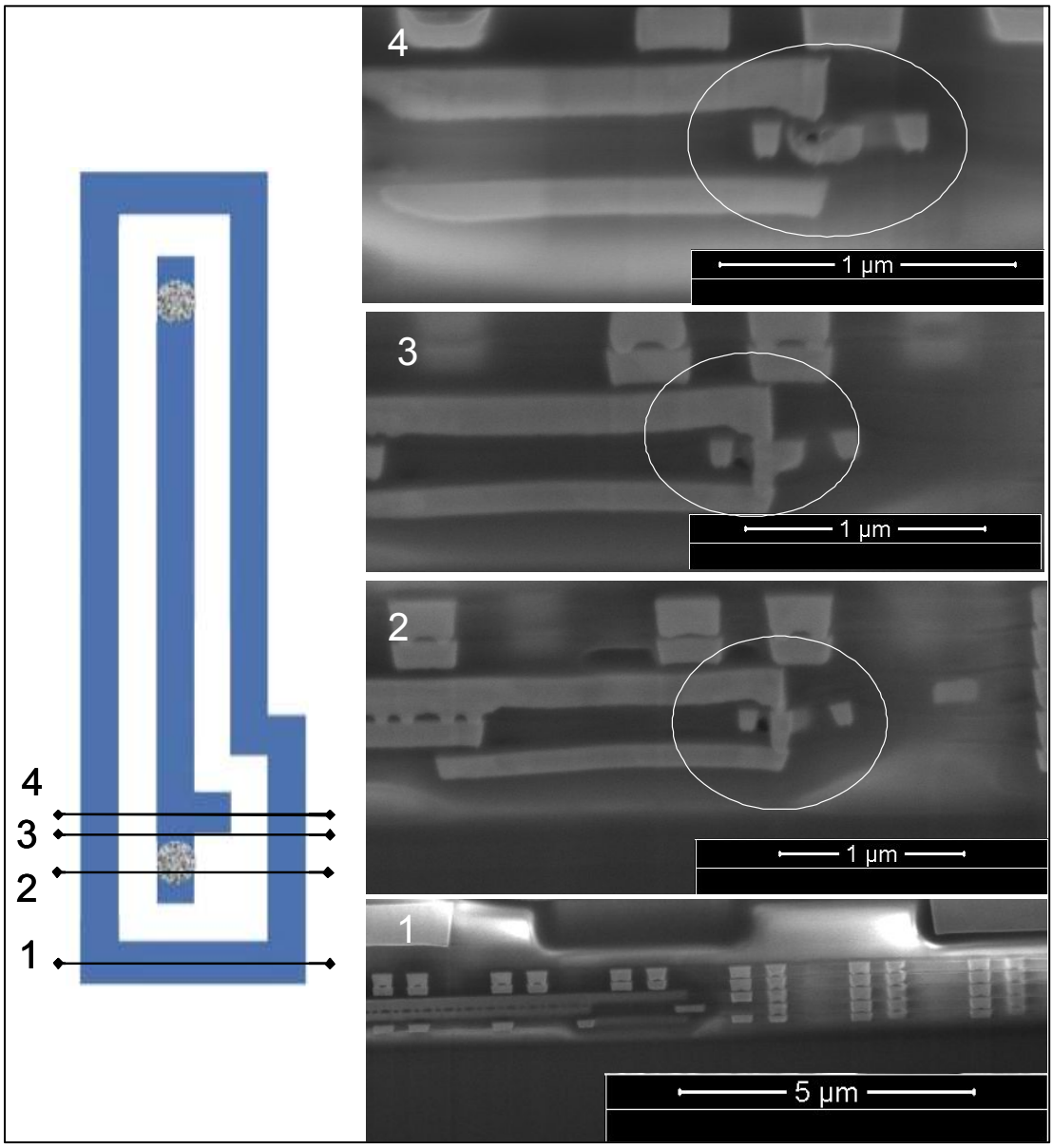


**Figure 4.14** Sequential FIB cut by at the cathode side of 140 nm side metal reservoir test structure.

Further failure analysis was performed on the 30 nm side reservoir test structure to compare with the 140 nm side reservoir structure as shown in Figure 4.15. Figure 4.15(a) shows that the void extended the whole length of the 30 nm side reservoir. On the other hand for the 140 nm structure (Figure 4.15(b)), it shows that the void has only partially

filled up the side reservoir, which is about 70 nm out of the 140 nm side reservoir. This explains the median-time-to-failure, $t_{50}$, of 70 nm and 140 nm side metal are comparable.

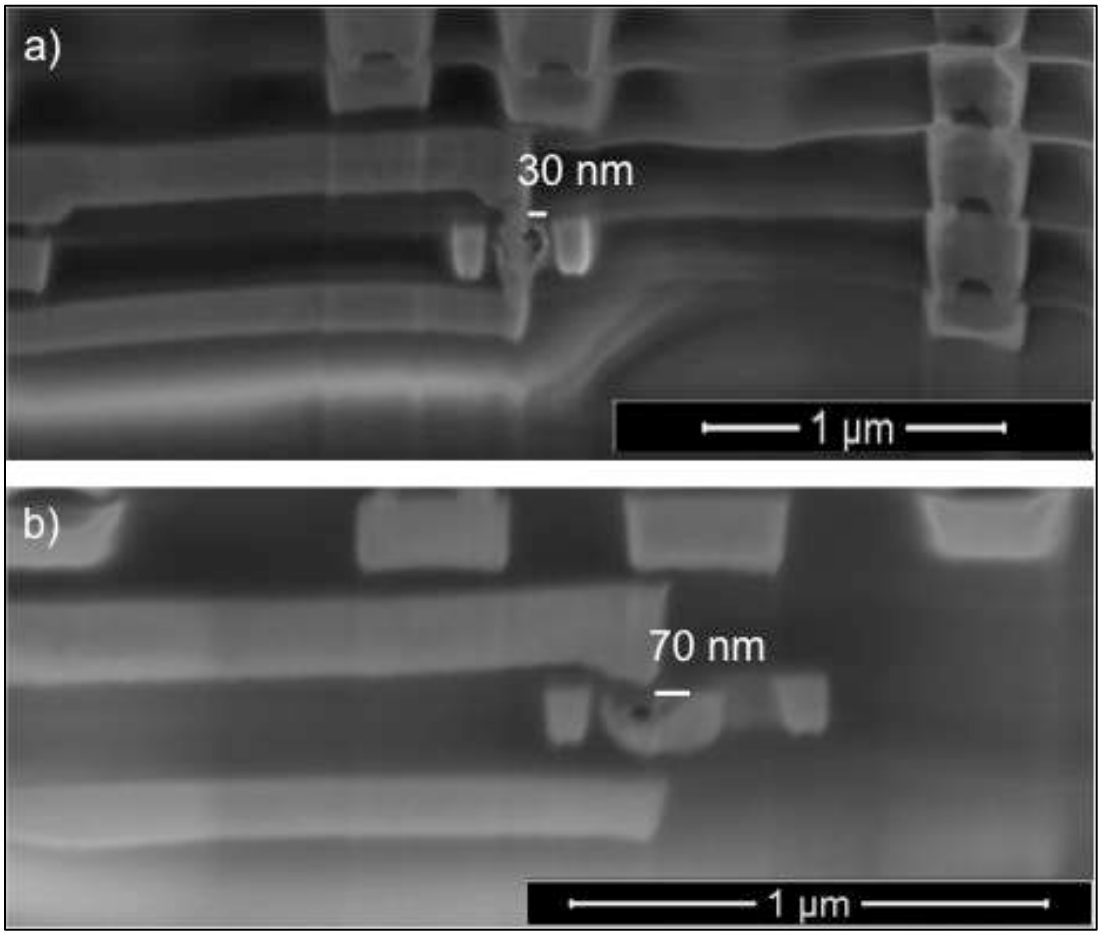


**Figure 4.15** Cross section SEM images of voids in (a) 30 nm and (b) 140 nm side metal reservoir test structures.

From the failure analysis in Figure 4.15, it seems to indicate that the void does not nucleate from the cathode via, but is from pre-existing voids that have drifted into the side metal reservoir. This is supported by the previous experiments results where a 70 nm length end of line metal reservoir has a shorter lifetime than a 70 nm side metal reservoir structure. Thus, a larger volume of void can be accommodated before a significant resistance increase has occurred and at the same time preventing new void nucleation at the end of cathode via due to electromigration-stress behavior explained earlier, resulting in the elimination of early failures from side metal reservoir structures.

From the lifetime distributions and failure analysis results of the side metal reservoir structures, the effectiveness of the side reservoir is demonstrated. It shows that further lengthening of the side metal reservoir beyond 70 nm does not seem to be effective in improving the electromigration lifetime as the void did not extend beyond that distance. The reasons for the pre-existing void to move into the side metal reservoir are explained earlier, namely back-stress gradient and the presence of Ta/Cu interface. However, back-stress gradient may likely the main factor of causing the pre-existing void does not move beyond 70 nm further inwards. This is because the amount of back-stress gradient that build up when the pre-existing void drifted close enough to the end of cathode via, is not high enough to push the pre-existing void all the way to the extend of 140 nm side metal reservoir. A similar length saturation effect for end of line metal reservoir structures has also been reported [24, 25].

A point to note is that in the both experiments, the pre-existing voids are likely not pinned along the interconnect, but are able to drift toward the cathode via. However, by designing the side reservoir further away from the cathode via, but still within $L_{crit}$, the pre-existing voids may be trapped by the side metal reservoir and prevent further void nucleation at the cathode via. Thus, the side metal reservoir structure can help to eliminate early failures and improve overall electromigration reliability in interconnects with pre-existing voids. However, note that there is a limit on how far the side metal reservoir can be extended.

## 4.5 *In- situ* Electromigration on Side Reservoir Metal

As mentioned in the experimental setup and method under *in-situ* electrical dual beam FIB, the side metal reservoir test structure with length 70 nm was chosen and carefully handled by following the all the procedure that had been outlined. Figure 4.16 shows the direction of the cross section that needs to be carried out during the experiment. Thin dielectric just in front of the side metal reservoir is needed to ensure the same interface surrounding the Cu interconnect during the electromigration lifetime stressing is

maintained during the in-situ testing, as well as to prevent any oxidation during the electromigration testing.

After all the sample preparation steps were executed, the test structure was subjected under electromigration testing with $J$ = 5 MA/cm$^2$ and temperature stressing of room temperature 27°C. The increase in the current density used here as compared to the previous experiment is to further accelerate the electromigration effect in term of void diffusion in the absence of high temperature stressing. These experiments might not necessarily leads to fatal failures due to high jump in the resistance of the metal interconnect.

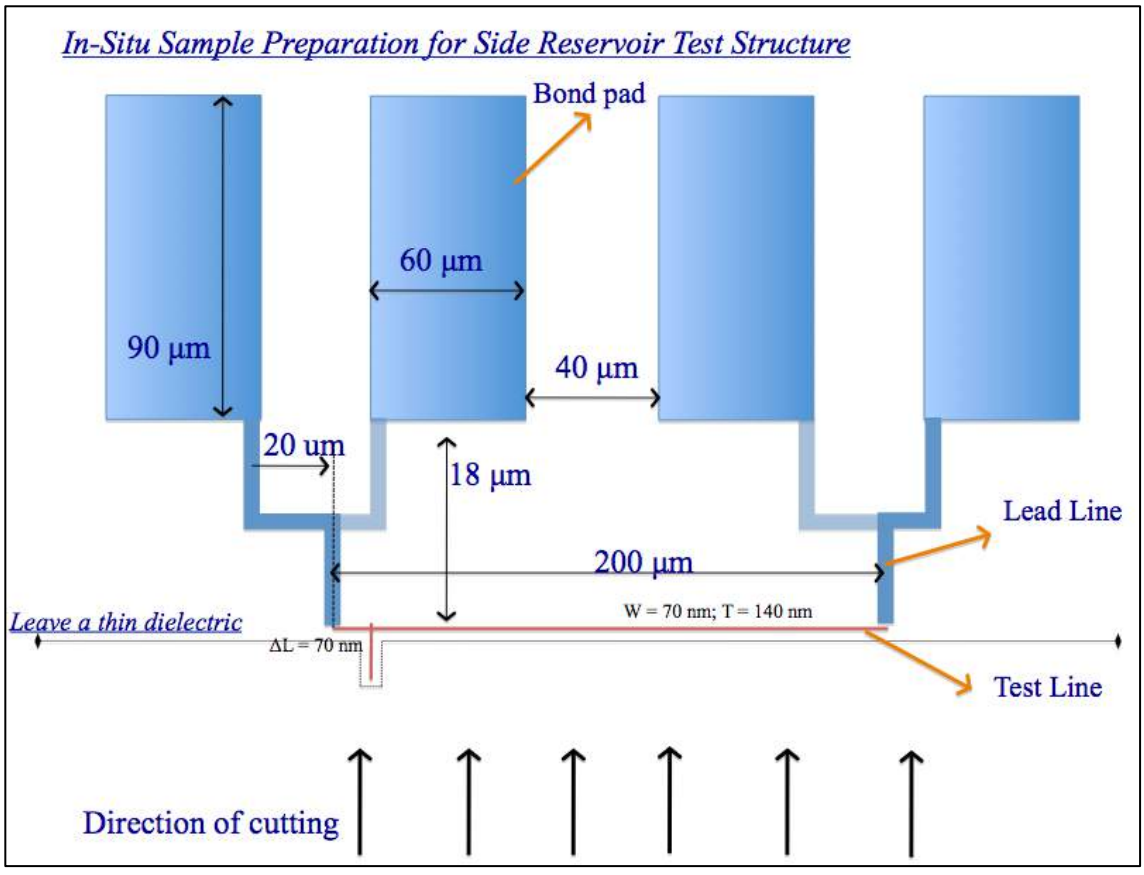


**Figure 4.16** Cross section direction on the sample preparation for *in-situ* electromigration testing.

Figure 4.17 shows the SEM image of the sample that undergo electromigration stressing at 0 hrs and 18 hrs. Unfortunately no visible change can be observed from the SEM image even though the sample has been subjected under electromigration test up to 18 hours. The resistance evolution in the metal line did not show much change as well. This might be due to the temperature stressing applied during the *in-situ* electromigration testing was too low (27°C), resulting in a much lower electromigration flux when compare at the high temperature stressing during the normal electromigration test (typically around 300°C). Further improvement is needed on the current setup to allow high temperature stressing.

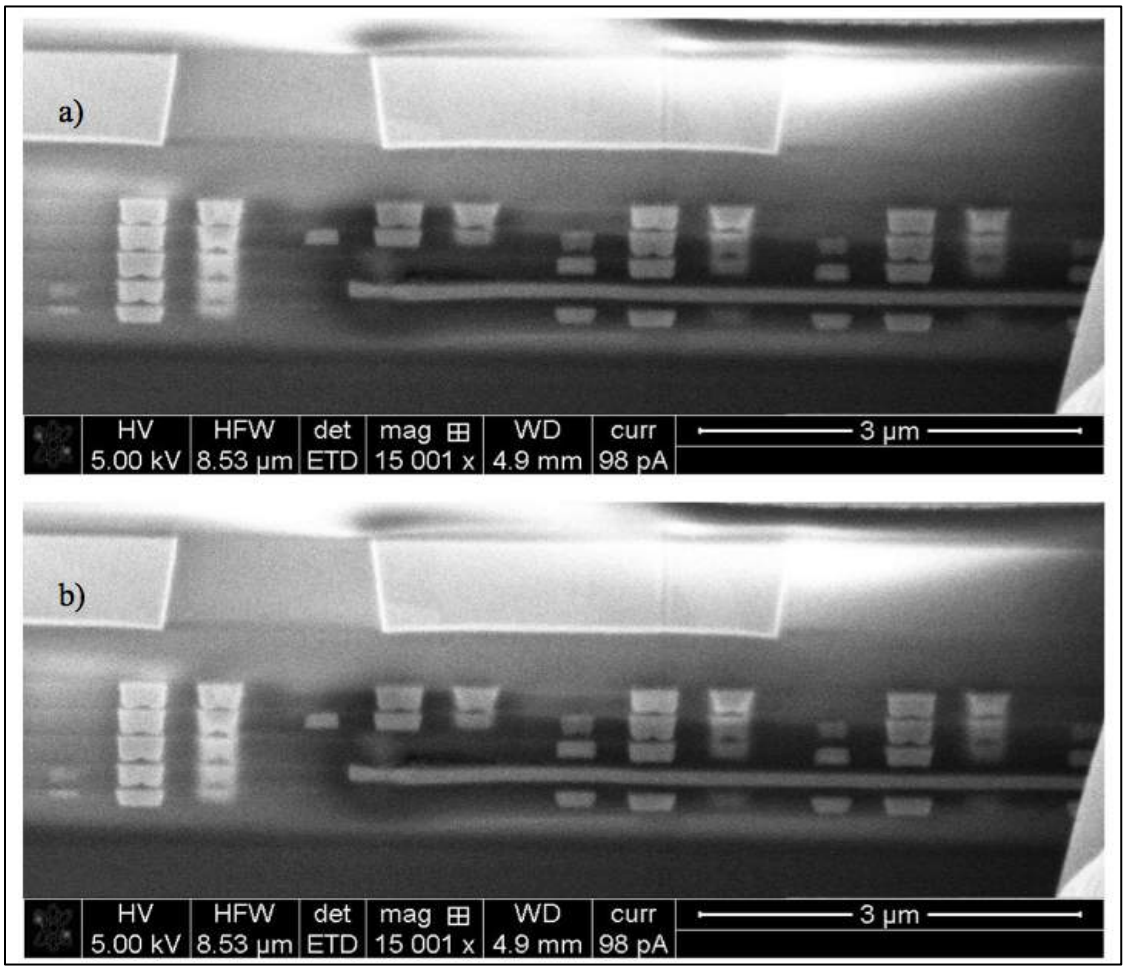


**Figure 4.17** SEM image of the sample that undergo electromigration stressing at a) 0 hrs and b) 18 hrs.

**References:**


[1] J.R. Black. *Proc. 6th Int. Reliab. Phys. Symp.: Mass Transport of Aluminum by momentum exchange with conducting electrons.* **1967,** 148-153.

[2] J.J. Clement. *IEEE Transactions on Device and Materials Reliability*. **2001,** 1, 33-42.

[3] M. Shatzkes and J.R. Lloyd. *J. Appl. Phys.* **1986,** 59, 3890-3893.

[4] J.J. Clement. *J. Appl. Phys.* **1997,** 82, 5991-6000.

[5] J.J. Clement and J.R. Lloyd. *J. Appl. Phys.* **1991,** 71, 1729-1731.

[6] Z.S. Choi, J. Lee, M.K. Lim, C.L. Gan and C.V. Thompson. *Journal of Applied Physics*. **2011,** 110, 033505-1-033505-9.

[7] G. Marti, L. Arnaud and Y. Wouters. *Microelectronics Reliability.* **2014,** 54, 1692-1696.

[8] L. Arnaud, P. Lamontagne, F. Bana, Y.L. Friec, and P. Waltz. *Microelectronics Engineering.* **2013,** 107, 145-150.

[9] I. A. Blech. *J. Appl. Phys.* **1976,** 47, 1203-1208.

[10] Z. S. Choi, R. Moenig, and C.V. Thompson. *Journal of Materials Research*. **2008,** 23, 383-391.

[11] A.V. Vairagar, S.G. Mhaisalkar, A.Krishnamoorthy, K.N. Tu, A.M. Gusak, M.A. Meyer and E. Zschech. *Appl. Phys. Lett.* **2004,** 85, 2502-2504.

[12] A.V. Vairagar, S.G. Mhaisalkar, M.A. Meyer, E. Zschech, and A. Krishnamoorthy. *Microelectronic Engineering*. **2005,** 82, 675-679.

[13] A.V. Vairagar, S.G. Mhaisalkar, A. Meyer, E. Zschech, A. Krishnamoorthy, K.N. Tu, and A.M. Gusak, *Appl. Phys. Lett.* **2005,** 87, 081909.1-081909.3.

[14] H. Mario, M. K Lim, C.L. Gan. *Proceedings of the 19$^{th}$ International Symposium on the Physical and Failure Analysis of Integrated Circuits*. **2012**, 1-5.

[15] C. K. Hu et. al. *Thin Soild Films*. **2006,** 504, 274-278.

[16] M. W. Lane, E. G. Liniger, and J. R. Llyod. *J. Appl. Phys.* **2003,** 93, 1417-1421.

[17] Y.M. Chang, J. Leu, B.H. Lin, Y.L. Wang, and Y.L. Cheng. *Advance Materials Science Engineering,* **2013,** 1-7.

[18] C.K. Hu, D. Canaperi, S.T. Chen, L.M. Gignac, S. Kaldor, M. Krishnan, S.G. Malhotra, E. Liniger, J.R. Llyod, D.L. Rath, D. Restaino, R. Rosenberg, J. Rubino,

S.C. Seo, A. Simon, S. Smith and W.T. Tseng. *Thin Solid Films.* **2006,** 504, 274-278.

[19] M.C. Kang, Y.J. Kim and J.J. Kim. *Electrochemical and Solid State Letters.* **2009,** 12, 340–343.

[20] C. Yang, F. Baumann, P.C. Wang, S.Y. Lee, P. Ma, J. AuBuchon, D. Edelstein. *Interconnect Technology Conference and 2011 Materials for Advanced Metallization (IITC/MAM), 2011 IEEE International,* **2011,** 1–3.

[21] D. Priyadarshini, S. Nguyen, H. Shobha, S. Cohen, T. Shaw, E. Liniger, C.K. Hu, C. Parks, E. Adam, J. Burnham, A.H. Simon, G. Bonilla, A. Grill, D. Canaperi, D. Edelstein, D. Collins, M. Balseanu, M. Stolfi, J. Ren and K. Shah. *Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), 2014 IEEE International.* **2014,** 185-188.

[22] M. Zhou. *Microelectronics Reliability.* **2015,** 55, 2705-2711.

[23] K. Croes, Y. Li, M. Lofrano, C. J. Wilson and Zs. Tokei. *Reliability Physics Symposium (IRPS), 2013 IEEE International,* **2013,** 2C.3.1-2C.3.4.

[24] S. Wei, A.V. Vairagar, C.H. Tung, Z.L. Xie, A. Krishnamoorthy, S.G. Mhaisalkar. *Surface and Coating Technology*, **2005**, 198, 257-261.

[25] Z.H. Gan, A.M. Gusak, W. Shao, Z. Chen, S.G. Mhaisalkar, T. Zaporozhets and K.N. Tu. *Journal of Materials Research*. **2007,** 22(1), 152-156.

# Chapter 5

# Conclusions and Future Recommendations

*In this final chapter, the conclusions of the study will be drawn and highlighted together with some future recommendations.*

## 5.1 Conclusions

This project started out with the objective of improving the lifetime of the copper metal interconnects. Based on the observation of pre-existing voids in Cu interconnects and their electromigration mechanism, an uniquely design side metal reservoir test structure was introduced in this project. Besides proving the effectiveness of the design, it is important to understand the limitation of the side metal reservoir in enhancing the lifetime of the copper interconnects.

From the simulation and modeling, it is well understood that the minimum and maximum electromigration flux will always be located at the two ends of the metal interconnect, anode and cathode, when it is under constant current stressing. With the presence of pre-existing void, the stress evolution in the metal interconnects changes accordingly, depending on where the pre-existing void exists or is pinned. If the pre-existing void is located at a distance greater than $L_{crit}$ (4.0 μm for metal interconnect with dimension of 200um length and width 0.07 μm, $J$ = 1.0 MA/cm$^2$ and T = 300°C), the impact to the stress evolution would be minimum and the maximum tensile stress at the cathode line would be achieved after some times of stressing until it reaches the nucleation stress limit. On the other hand, if the pre-existing void is nucleated or pinned at the distance smaller than $L_{crit}$, it could retard the tensile stress at the end of cathode line from reaching the nucleation stress limit. Thus, preventing nucleation of void at the end of cathode line. Under this condition, there will be a back-stress gradient build up as well between the electron wind force in the direction toward the anode with the back-stress from the void to the cathode in the opposing direction.

A newly designed side metal reservoir test structure is observed to be more effective in improving the electromigration lifetime than conventional end of line metal reservoir structures. It is suggested that the side metal reservoir is able to act as a void trap for the pre-existing void during the electromigration, thus delaying the onset of failure. The ability of the side metal reservoir to trap the drifting pre-existing void is due two factors, namely, the electromigration-induced stress evolution with pre-existing void in the metal

inteconnect and the presence of the Ta/Cu interface at the end of cathode via. The electromigration-induced stress evolution with pre-existing void in the metal interconnect has been discussed earlier in the section the simulation section.

Further results from the physical failure analysis done on side metal reservoir 30 nm and 140 nm suggested that the pre-existing void is indeed drifted towards the end of cathode via and being trapped in the side metal reservoir. The side metal reservoir structure is able to prevent an early failure during the electromigration as well. This is due to the larger allowance of volume void growth and prevention of void nucleation at the end of cathode via.

The effectiveness of side metal reservoir was studied as well in the project. From the experiments conducted, it is suggested that there is a limit on how far the side metal reservoir can be extended, for this project, it is found that 70 nm, is the limit before it reaches saturation in terms of the prolonging the lifetime of the metal interconnect. When designing the side metal reservoir in the actual circuitry, beside the length of side metal reservoir, it should also consider that the introduction of side metal reservoir will increase the total layout area of the metal interconnects.

The physical failure analysis done by FIB/SEM machine suggests the same observation where the void could only fill up to 70 nm out of the 140 nm of the side metal reservoir length. The reason is the back-stress gradient in side metal reservoir is not strong enough for the pre-existing void to move further inwards.

In the *in-situ* electromigration experiment, no visible change observed on both SEM imaging and resistance evolution. This might be due to a much lower electromigration flux. Therefore, it is suggested that further optimization can be done in the test structure for future works.

## 5.2 Future Recommendations

The outcomes of this Master research have led to the understanding on how the side metal reservoir is able to expand the lifetime of the copper metal interconnect under electromigration stressing. However, more things can be done in order to give a more and thorough understanding on the roles of the side metal reservoir in the stress evolution during the electromigration stressing. We would like to recommend developing at least a 2-D modeling and simulation which incorporate the side metal reservoir in to the simulation rather than just 1-D modeling and simulation shown in this project. We believe it will give a more complete understanding on how the interaction of the side reservoir towards the pre-existing void with the presence of back stress on both end cathode vias as well as end of side metal reservoir.

We will like to proposed some of the test structures as well for future studies which shown in the Figure 5.1, Figure 5.2 and Figure 5.3. The purposes of those test structures are described below:

1. For the first test structure: First, there is no longer Ta/Cu interface at the end of cathode via. Therefore, it will enable to decouple the effect of the Ta/Cu interface with the back-stress gradient effect during the experiment. And second, with the variation of the distance of the side metal reservoir to the end of cathode via, it will enable to quantify the back-stress gradient effect in improving the lifetime of the side metal reservoir.
2. For the second test structure: There is no side metal reservoir and it only has a single or multiple Ta/Cu interface. Therefore, it will enable to study the effect of the Ta/Cu liner toward the pre-existing void of impacting the electromigration lifetime.
3. For the third and last test structure: It is similar like the side metal reservoir structure studied earlier. However, on this structure, the position of both side metal reservoir and Ta/Cu liner will be varied together at the same time. This is to study the impact of the back-stress gradient portion during the electromigration

experiment when both back-stress and presence of Ta/Cu liner are needed for pre-existing void to drift toward the side metal reservoir.

And note that all the test structures are designed with a un-silicide polyheater underneath the test metal line. This is to enable the high temperature stressing that was missing during the *in-situ* electromigration experiment.

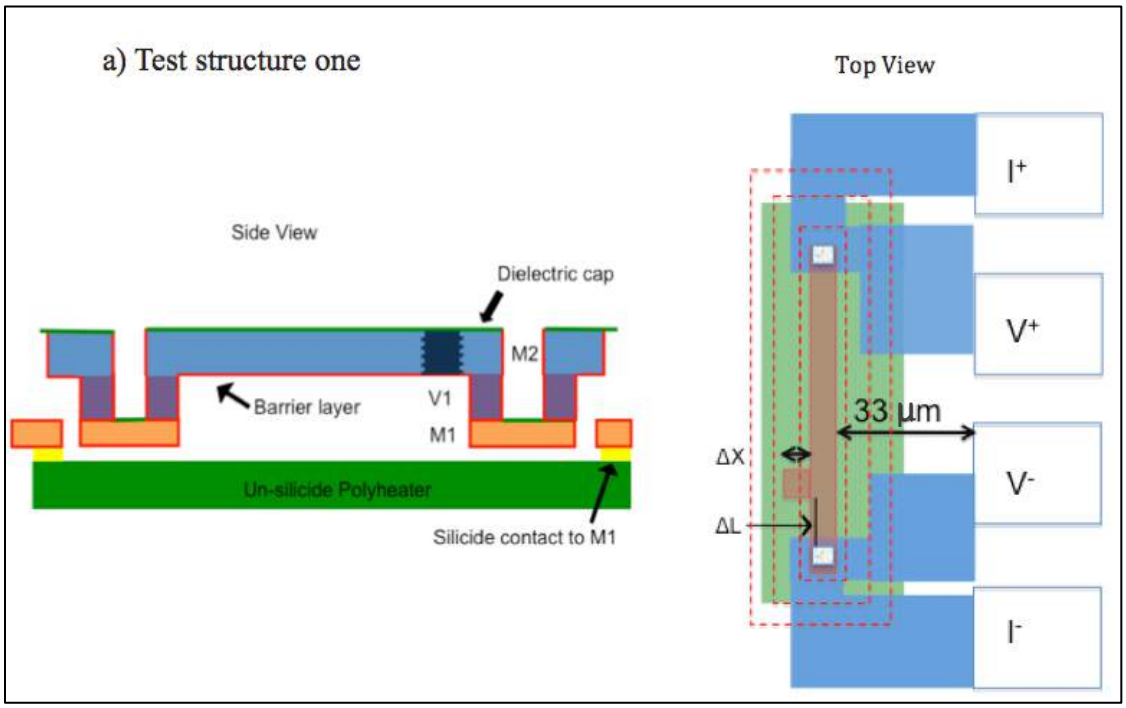


**Figure 5.1** Simplified side and top view image of the proposed test structure one.

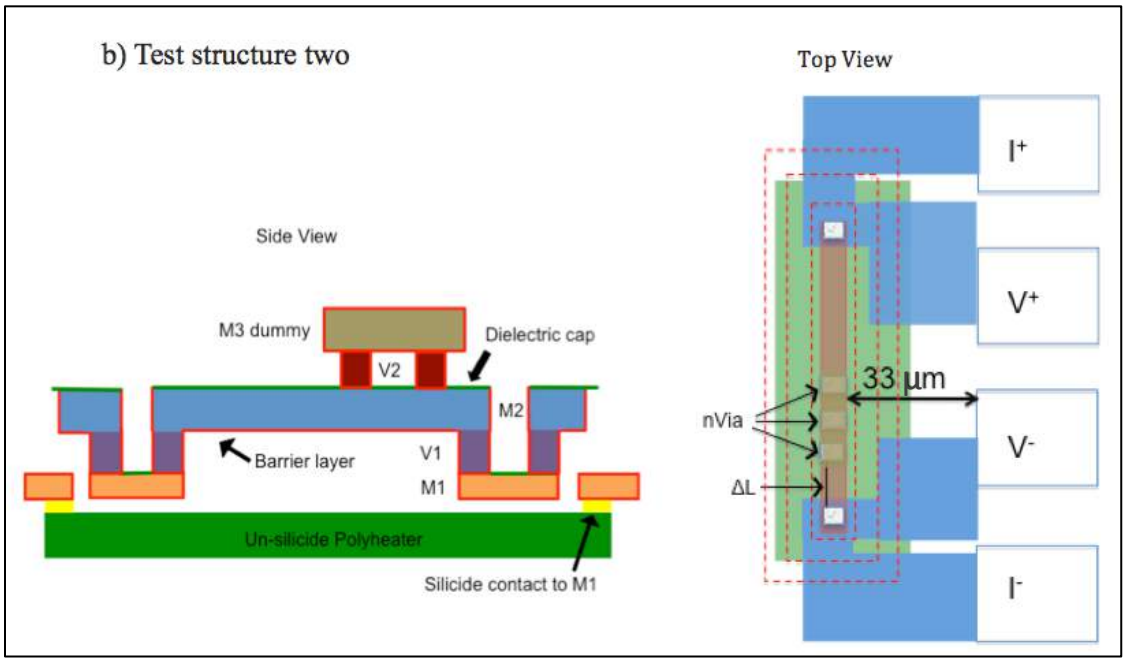


**Figure 5.2** Simplified side and top view image of the proposed test structure two.

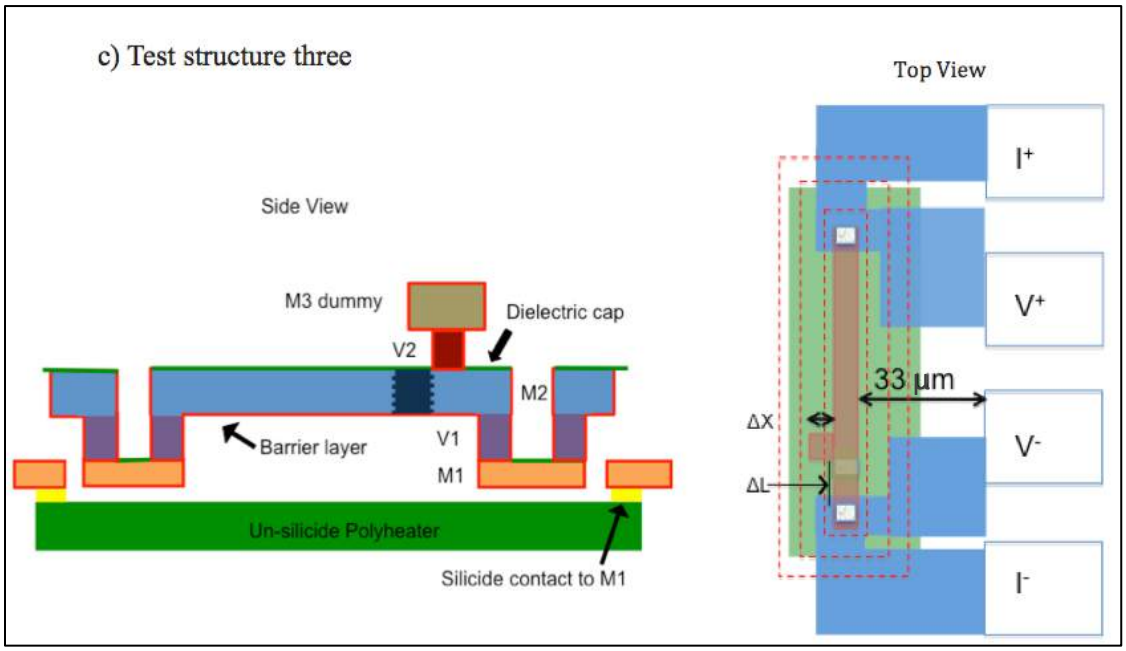


**Figure 5.3** Simplified side and top view image of the proposed test structure three.

# List of Publications

**Conferences Papers**

1) **H. Mario***, M.K. Lim, C.L. Gan. Impact of Pre-Existing Voids on Electromigration in Copper Interconnects, in Proceedings of the 19th International Symposium on the Physical and Failure Analysis of Integrated Circuits, p. 1-5, Singapore, July 2012.
2) **H. Mario***, C.L. Gan, Y.K. Lim, J.B. Tan, J. Wei, T. Chookajorn, C.V. Thompson. Effects of Side Reservoirs on the Electromigration Lifetime of Copper Interconnects, in Proceedings of the 18th International Symposium on the Physical and Failure Analysis of Integrated Circuits, p. 1-4, South Korea - Incheon, July 2011.

***Note***: Papers published in the first and second article are used in this thesis and necessary copyright permissions have been sought from the publisher. Please see the following pages for the copyright permissions.

Copyright Clearance Center RightsLink®

Home | Create Account | Help | Live Chat

IEEE Requesting permission to reuse content from an IEEE publication

**Title:** Effects of side reservoirs on the electromigration lifetime of copper interconnects

**Conference Proceedings:** Physical and Failure Analysis of Integrated Circuits (IPFA), 2011 18th IEEE International Symposium on the

**Author:** Mario, H.; Chee Lip Gan; Yeow Kheng Lim; Juan Boon Tan; Jun Wei; Chookajorn, T.; Thompson, Carl V.

**Publisher:** IEEE

**Date:** 4-7 July 2011

Copyright © 2011, IEEE

LOGIN

**If you're a copyright.com user,** you can login to RightsLink using your copyright.com credentials. Already **a RightsLink user** or want to learn more?

**Thesis / Dissertation Reuse**

**The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:**

*Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:*

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

*Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:*

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.