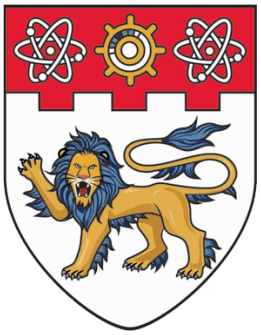

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

3D Interconnects and Multi-module Integrated Surface Electrode Ion Trap for Scalable Quantum Information Processing

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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3D Interconnects and Multi-module Integrated Surface Electrode Ion Trap for Scalable Quantum Information Processing

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

in partial fulfilment of the requirement for the degree of

Doctor of Philosophy

2022

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Zhao Peng

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Tan Chuan Seng

Authorship Attribution Statement

This thesis contains material from 5 papers published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as the first author.

Chapter 2 is published as: **Zhao, P.;** Lim, Y. D.; Li, H. Y.; Guidoni, L.; Tan, C. S. Advanced 3D Integration Technologies in Various Quantum Computing Devices. IEEE Open Journal of Nanotechnology 2021. 2, 101-110. The contributions of the co-authors are as follows:

- I worked on the literature review on the integration technologies in various quantum computing devices. I drafted the manuscript.
- Dr. Lim Yu Dian, Dr. Li Hong Yu and Dr. Guidoni Luca offered advices on the review scope. They also helped with manuscript revision.
- Professor Tan Chuan Seng provided the initial direction. He also helped to finalise the manuscript.

Chapter 3 is published as: **Zhao, P.;** Tao, J.; Li, H. Y.; Lim, Y. D.; Lin, Y.; Guidoni, L.; Tan, C. S. Performance Comparison of High Resistivity Silicon, Silicon with Grounding Plane and Glass as Substrate of Ion Trap for Quantum Information Processing. 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC), IEEE: 2020; pp 1-5. The contributions of the co-authors are as follows:

- I proposed the design and characterization work of surface electrode ion traps on various of substrates. I finished partial fabrication work. I also worked on the data analysis and manuscript drafting.
- Dr. Tao Jing helped with trap design and simulation.
- Dr. Li Hong Yu helped with the fabrication.
- Dr. Lim Yu Dian helped with data analysis and manuscript revision.
- Dr. Lin Ye helped with the electrical measurement setup.
- Dr. Guidoni Luca helped with the ion trapping test.
- Professor Tan Chuan Seng provided the initial direction and technical guidance for the study. He also edited the manuscript drafts.

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- I worked on the design, simulation, fabrication and characterization of TSV integrated ion trap. I also worked on the data analysis and manuscript drafting.
- Dr. Likforman Jean-Pierre helped with ion trapping test.
- Dr. Li Hong Yu helped with the fabrication.
- Dr. Tao Jing helped with trap design and simulation.
- Henner Theo helped with ion trapping test setup.
- Dr. Lim Yu Dian helped with data analysis and manuscript revision.
- Seit Wen Wei helped with assembling process between TSV die and glass interposer.
- Professor Tan Chuan Seng provided the initial direction and technical guidance for the study. He also edited the manuscript drafts.
- Dr. Guidoni Luca helped with the ion trapping test and data analysis on the trapping result.

Chapter 4 is also partially published as: **Zhao, P.;** Li, H. Y.; Tao, J.; Likforman, J.-P.; Lim, Y. D.; Seit, W. W.; Guidoni, L.; Tan, C. S. RF Performance Benchmarking of TSV Integrated Surface Electrode Ion Trap for Quantum Computing. IEEE Transactions on Components, Packaging and Manufacturing Technology 2021, 11 (11), 1856-1863.

- I worked on the design, simulation, fabrication and characterization (especially RF characterization) of TSV integrated ion trap. I also worked on the data analysis and manuscript drafting.
- Dr. Li Hong Yu helped with the fabrication.
- Dr. Tao Jing helped with trap design and simulation.
- Dr. Likforman Jean-Pierre helped with the ion trapping test.
- Dr. Lim Yu Dian helped with data analysis and manuscript revision.
- Seit Wen Wei helped with assembling process between TSV die and glass interposer.

- Dr. Guidoni Luca helped with the ion trapping test.
- Professor Tan Chuan Seng provided the initial direction and technical guidance for the study. He also edited the manuscript drafts.

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- I worked on the simulation, analysis and manuscript drafting.
- Bi Xin Wen helped with the simulation.
- Dr. Li Hong Yu, Dr. Lim Yu Dian and Seit Wen Wei provided advices on the simulation result analysis.
- Dr. Guidoni Luca helped to measure the temperature increase of TSV trap.
- Professor Tan Chuan Seng provided the initial direction and technical guidance for the study. He also edited the manuscript drafts.

25-12-21

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Date

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Zhao Peng

This thesis is dedicated to my parents and Ziqi.

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Throughout my PhD journey, I have kept imagining the moment when I could finish the thesis drafting and start typing in my acknowledgement. Here it comes, but I realize that I could not find words to express my thanks.

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Table of Content

Summary

Among the various physical systems for quantum bit (qubit) implementation, trapped ion has drawn significant attention due to its long coherence time (in the second range) and high gate fidelity (>99.99% for single qubit gate). After years of careful development, the ion trap, from mechanically assembled linear trap to lithography-defined surface electrode ion trap, is compatible with CMOS fabrication, which opens the door for the high-resolution, high-repeatability and large-scale ion trap manufacturing. To date, the number of fully connected ion qubits in state-of-the-art ion trapping devices is ~10. However, to scale close to or even beyond the noisy intermediate-scale quantum regime (NISQ, ~100 ions), some challenges remain. One such challenge is to maintain the delicate control of multiple components over individual ion with increasing ion number. In such context, this thesis is committed to boost the scalability of ion trap by integrating advanced 3D interconnects (e.g., through silicon via) and other functional modules (e.g., silicon photonics and multilayer metallization). 3D interconnects are integrated in the half space underneath surface electrode, to replace conventional wire bonding that extends out of the surface. Silicon photonics (grating coupler and waveguide) in place of bulk optics and lenses are used for on-chip light routing and emission. Multilayer metallization is used to maintain the overall RF performance and enable high-density interconnection where necessary.

Firstly, surface electrode ion traps on different substrates (namely high resistivity silicon, silicon with grounding plane and glass) are designed and fabricated. Standard CMOS back-end-of-line fabrication process on 12-inch wafer platform is employed. The electrical performances of different traps are compared in terms of leakage current (*I*-*V*), parasitic capacitance (*C*-*V*), on-chip RF loss (S-parameter) and post-packaging resonance. Though the leakage (at the order of 10^{-8} A) between neighboring electrodes is relatively high, ion trap on glass substrate demonstrates extremely small capacitance (<1 pF) and low RF loss (insertion loss of <0.05 dB at RF frequency of 50 MHz), as compared to the silicon counterparts. This is mainly due to excellent insulation property of glass. Following that, ion trapping test is performed on the glass trap and ions are successfully confined with an averaged lifetime of ~30 minutes (compatible with the 10^{-11} mbar vacuum level (10^{-13} Pa)).

To simultaneously leverage the dielectric property of glass and the microfabrication compatibility of silicon, the integration of silicon ion trap and glass interposer is performed, between which TSV is used to build the vertical interconnection. Due to the incorporation of

TSV, the original wire bonding pads as well as the connection circuits on the surface electrodes can be eliminated. As a result, the form factor of TSV integrated trap is reduced by ~10 times. Correspondingly, the parasitic capacitance between neighboring electrodes is reduced from >24 pF to 3 pF. Similarly, the insertion loss of TSV integrated trap drops to 0.11 dB, in sharp comparison to the previous traps on silicon substrates (up to 2.4 dB). Analytical models are built to respectively characterize the electrode capacitance and overall power loss, and a good agreement is achieved between the model and the measurement result. In addition, since TSV is located in the half space underneath the surface electrodes, the electrodes geometry design is enabled with high flexibility. Meanwhile, the laser obstruction issue due to the stick-out bonding wires has been resolved. In terms of the ion trapping performance, both the heating rate (17 quanta/ms for an axial frequency of 300 kHz) and the lifetime (~30 minutes) of TSV trap are comparable with non-cryogenic traps of similar dimensions. Moreover, a customized CPGA with patterned redistribution layer is used to locate TSV integrated trap directly in the absence of glass interposer, facilitating high-efficiency thermal management and upgrading the packaging flexibility.

At the next stage, the co-integration of other functional modules such as silicon photonics and multilayer metallization with TSV trap is investigated. In silicon photonics module, waveguide and grating coupler are on-chip introduced in place of bulk optics to achieve localized light routing and emission. In multilayer metallization module, as a first step, a grounding plane is incorporated into TSV trap to shield the silicon substrate from RF signal, in which specific windows are patterned onto the plane to accommodate TSV and allow the transmission of lights. The compatibility between TSV/multilayer metallization and waveguide/grating coupler for electrical and optical (E/O) signal routing is demonstrated. The preliminary test result based on wafer frontside shows that a ~40% capacitance reduction is achieved, and the insertion loss further drops to 0.06 dB, close to the performance of glass trap. In addition, the simulation results on photonics components indicate that an overall coupling efficiency of <30 dB is obtained from the input fiber to the ion through the photonics circuit. However, the measured power loss for light with wavelength of 1092 nm is as high as 50 dB. The deviation between the simulation and measurement is largely due to the fabrication imperfection and the resultant sloped grating coupler profile.

This thesis focuses on the scalability enhancement of ion trap by integrating TSV, silicon photonics and multilayer metallization into conventional ion trap. The results are promising and pave the way for the future large scale quantum computing based on trapped ion.

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List of Abbreviations

2D	two dimensional
3D	three dimensional
AC	alternating current
AFM	atomic force microscopy
ALD	atomic layer deposition
AOM	acousto-optic modulator
BARC	bottom anti-reflective coating
BEOL	back end of line
CMOS	complementary metal-oxide-semiconductor
CMP	chemical mechanical polishing
CPGA	ceramic pin grid array
CTE	coefficient of thermal expansion
CVD	chemical vapor deposition
DAC	digital-to-analog converter
DC	direct current
ECP	electroplating
EDX	energy-dispersive X-ray spectroscopy
ESR	equivalent series resistance
FDTD	finite-difference time-domain
FEM	finite element modelling
FEOL	front end of line
FET	field effect transistor

FLDW	femtosecond laser direct-write
FWHM	full width at half maximum
GND	ground
HR	high resistivity
IC	integrated circuit
IP	ion pump
JJ	josephson junction
MM	multilayer metallization
MOS	metal-oxide-semiconductor
PCB	printed circuit board
PECVD	plasma enhanced CVD
PRS	photoresist strip
PVD	physical vapor deposition
QCCD	quantum charge-coupled device
RDL	redistribution layer
RF	radio frequency
RLC	resistor-inductor-conductor
SEM	scanning electron microscope
SET	single electron transistor
SNSPD	superconducting nanowire single photon detector
SoC	system on a chip
SPAD	single photon avalanche diode
SiARC	Si containing anti-reflective coating
SiP	system in package

SOI	silicon on insulator
TEM	transmission electron microscope
TSP	titanium sublimator pump
TSV	through silicon via
UBM	under bump metallization
UHV	ultra-high vacuum
XPS	X-ray photoelectron spectroscopy

Chapter 1. Introduction

This chapter provides a brief introduction on the basics for the trapped ion-based quantum computing: the fundamentals of quantum computing, the ion trapping mechanism, the geometry evolution of ion trap, the choice of atomic specie and corresponding electronic states. Meanwhile, the essentials of three-dimensional (3D) integration technologies (especially, the through silicon via) in the semiconductor industry are introduced. Finally, the motivation, objective, and outline of this thesis are highlighted.

1.1 Fundamentals of Quantum Computing

Following the famous Moore's law, the length of transistor gate keeps shrinking from 1960s [1]. However, this scaling is expected to hit its fundamental limit. When the physical structure dimension of electron confinement is comparable with electron wavelength, the quantum effects of electron instead of the particle property will dominate its physical phenomena. To take advantage of this quantum effect, information processing based on quantum mechanics can be used as an alternative solution to continually boost the capability of computing, as proposed by Richard Feynman and Paul Benioff [2, 3].

1.1.1 Quantum Bit versus Classical Bit

The power or capability of a computer is determined by the physical nature of its most fundamental unit: the bit. The classical bit in classical computing always has a definite value (state) of 0 or 1 by switching the gate voltage of a transistor. However, in contrast to the classical bit, the quantum bit (qubit) in quantum computing is able to represent the states of $|0\rangle$ and $|1\rangle$ simultaneously. This is known as superposition. The general state of a qubit can be expressed as:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle, \quad (1)$$

in which α and β are complex numbers and fulfill the normalization requirement $|\alpha|^2 + |\beta|^2 = 1$. The Equation (1) can be rewritten as:

$$|\psi\rangle = cos\frac{\theta}{2}|0\rangle + e^{i\varphi}\sin\frac{\theta}{2}|1\rangle. \quad (2)$$

The state of a qubit is now defined as a point at a sphere (Bloch sphere), as shown in Figure 1. States $|0\rangle$ and $|1\rangle$ and angles θ and φ are marked accordingly. In fact, the parallel processing capability of quantum computer lies in the power of superposition. For example, for a 3-bit information, 8 possible states (000, 001, 010, 100, 011, 101, 110, 111) are required to be input in sequence into a classical computer. However, in quantum computer, due to the superposition, the 8 states can be input in a single attempt. Apparently, the parallel processing capability can be enhanced exponentially with the qubits number.

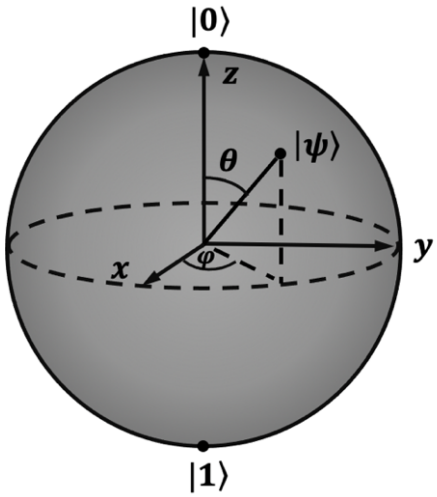


Figure 1. Bloch sphere. The general state of a qubit can be any point on the surface of this sphere.

Another amazingly unique phenomenon in quantum mechanics is called entanglement, which is refer to the instant correlation between qubits over any distance. An example is given to demonstrate the mystery of entanglement. A state of two qubits is given as $|\psi\rangle = \frac{1}{\sqrt{2}}|00\rangle + \frac{1}{\sqrt{2}}\beta|11\rangle$. It is easy to prove that this state cannot be factorized as two single qubit states $|a\rangle$ and $|b\rangle$ such that $|\psi\rangle = |a\rangle|b\rangle$. This is because the states of two single qubits are entangled. Also, another way to see entanglement is the measurement. For the state of two qubits given above, when the state of one qubit is measured, the state of the other qubit is defined. Specifically, if the first qubit is measured to be state $|0\rangle$ ($|1\rangle$), the second qubit will be state $|0\rangle$ ($|1\rangle$). Till now, the mechanism behind entanglement is not fully understood. However, entanglement plays a crucial role in quantum computing, quantum information and quantum teleportation [4].

1.1.2 Criteria to Build a Quantum Computer

To build a quantum computer, the physical implementations should fulfill the criteria outlined by David DiVincenzo [5]:

- Typical two-level quantum system can be realized, and this system is stable and well isolated from the environment.
- The ability to initiate the state of qubits to a simple fiducial state.
- The decoherence time is much longer than the gate time so that a successful error correction can be done in time.
- A set of universal quantum gates.
- State readout of the qubit should be accessible.

Considering the transmission of intact qubits from place to place (i.e., scalability), two more features are added:

- The ability to interconvert stationary and flying qubits.
- The ability to faithfully transmit flying qubits between specified locations.

A variety of physical systems of qubit have been proposed and demonstrated, including trapped ion, neutral atom, superconducting circuit, electron spin, photon, etc [6, 7]. These two-level systems can generally fulfill the criteria listed above. However, they barely share anything in common in terms of design, manufacturing, and manipulation. As Richard Feynman said in the famous talk given at American Physical Society meeting in 1959, 'when we get to very, very small world - say circuits of several atoms - we have a lot of new that would happen that represent completely new opportunities to design' [8].

The current demonstrations of quantum computing based on these physical systems are generally at the nascent stage. Most achieved progresses focus on some specific metrics that evaluate the quantum operations (e.g., qubit initiation fidelity, single qubit gate time and fidelity, two qubit gate time and fidelity, lifetime, qubit numbers, etc.). Though some platforms have been demonstrated with the qubits number of ~50 [9, 10], close to the noisy intermediate-scale quantum (NISQ) scheme [11], there is still a long way ahead to develop an actual large-scale quantum computing platform which can run the useful quantum algorithm and show the quantum supremacy. To develop some initial concepts about these qubit candidates, a brief

comparison of the obtained performance metrics is provided in Table I, but a more detailed description is allocated to Section 2.2.

Table I. Comparison of various physical systems of qubits.

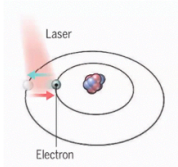
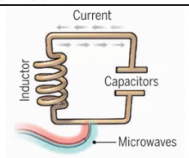
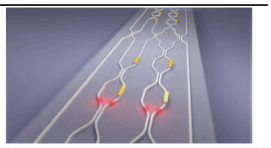
	ion trap	superconducting circuit	silicon spin	photons
schematic				
advantages	1.identical qubits 2.long coherence time	1.fast gates 2.solid state qubits	1.silicon platform 2.solid state qubits	1.silicon photonics platform 2.free of decoherence
challenges	many lasers required	poor uniformity	limited qubit number	heralded gate
lifetime (s)	>1000	0.00005	0.03	long
logic fidelity	99.9%	99.4%	99%	97% (non-deterministic)
commercialization	IonQ Honeywell	IBM Google	Intel	PsiQuantum Xanadum

Table I modified from Ref [7]. The schematic of photons is from https://www.extremetech.com/extreme/108573-worlds-first-programmable-quantum-photonic-chip.

1.2 Fundamentals of Ion Trap

The fundamentals of ion trap introduced in this section are all based on radio-frequency (RF) trap, which is also called Paul trap (invented by Wolfgang Paul).

1.2.1 How Trapped Ions Fulfill the Criteria

The criteria outlined by David DiVincenzo is discussed one by one in the scope of trapped ions [12]. First, the trapped ions in the RF null are well isolated with surrounding environment (ultra-high vacuum, in the range of 10^{-11} mbar) and the trapping lifetime can be up to several hours (with proper cooling). Second, using lasers with specific wavelengths, state initiation and readout (both $|0\rangle$ and $|1\rangle$) of trapped ions can be straightforwardly performed. For initiation (optical qubit), one can optically couple the long-lived state (say $|0\rangle$) to an auxiliary state $|e\rangle_{spontaneous}$, and $|e\rangle_{spontaneous}$ will rapidly decay to state $|1\rangle$. For readout, only the ions at state $|1\rangle$ ($|0\rangle$) can be repetitively excited into a transition cycle by lasers and emit the detectable photons during this cycle, whereas the ions at the other state $|0\rangle$ ($|1\rangle$) will remain dark. Both the initiation and readout operations have a reported fidelity as high as 99.9% [13,

14]. In addition, considering the universal quantum gate, the rotation between states $|0\rangle$ and $|1\rangle$ can be simply performed by focusing a laser beam (optical qubit) that resonant at the transition frequency (single qubit gate). The shared motional mode in a string of ions can be used as a quantum bus to transfer information. Along with certain single qubit gate rotations, the entangled two qubit gate can be performed [15]. Single qubit gate and two-qubit entangling gate are sufficient to construct a universal gate (e.g., Controlled NOT gate) [16, 17]. In the end, the ratio of coherence time (up to 600 s) to gate time (1 to 100 μs for typical two-qubit gate) is of $\sim 10^6$ of trapped ions, that is three orders of magnitude higher than the ratio of superconducting loops (~ 1000) [18, 19]. Meanwhile, the interaction between remote trapped ions can also be achieved by physically shuttle ions (flying qubits) or using mediums like photons, enabling the trapped ions with high scalability [20, 21]. In summary, it is concrete to conclude that all the criteria outlined by David DiVincenzo have been fulfilled by trapped ions.

1.2.2 Geometry Evolution of Ion Trap

The ion trap geometry evolution basically follows a route from mechanically assembled hyperbolic trap or quadruple trap to the microfabrication-compatible surface electrode ion trap. The hyperbolic trap was first developed for mass spectrometry by Wolfgang Paul in 1955 [22]. The hyperbolic trap has a rotationally symmetric geometry consists of a ring and two endcap electrodes. Since the ions are three-dimensionally trapped at the RF null (where RF field is zero), the hyperbolic trap is also called point trap. In contrast, the quadruple trap is able to form a linear RF null, where multiple ions can be trapped into a 1D crystal. A transformed approximation of hyperbolic trap is four-rod linear trap (Figure 2 (a)). Four rod electrodes are placed in parallel at the corners of a square. One pair of electrodes at the diagonal are applied with RF potentials, whereas the other two are set as ground. Axial confinement is provided by the endcap electrodes placed at the two ends of rods, or the two ground electrodes can be segmented and used as control electrodes. As compared to the quadruple trap, the four-rod linear trap features higher optical access. Due to the formed linear RF null, the ions can be moved along this line without excess micromotion, which is the essential component of the quantum charge-coupled device (QCCD) scheme for scalable quantum computing [20].

In 2005, the first surface electrode ion trap was developed by transforming the 3D rod electrodes into 2D planar electrodes located on the same substrate (Figure 2 (c)) [23]. This opens a door for the use of microfabrication techniques in ion trap manufacturing. In fact, before the introduction of planar ion trap, the microfabricated traps (e.g., laser-machined traps)

already appeared as an assembly of multiple electrode layers (multilayer ion trap, Figure 2 (b)) [24, 25]. However, those traps were still suffered from the complex alignment and assembling process (e.g., screw may be required). The electrodes of planar trap, in contrast, are co-located on the same plane, making planar trap inherently compatible with advanced lithography-based fabrication process. As a result, high design flexibility and fabrication repeatability are enabled. More importantly, with the adoption of integration technologies in advanced semiconductor chips, some previously bulk components for ion trapping can now be monolithically integrated (e.g., lasers, photodetectors, control electronics, etc.), which is an important step towards large-scale ion trap-based quantum computing.

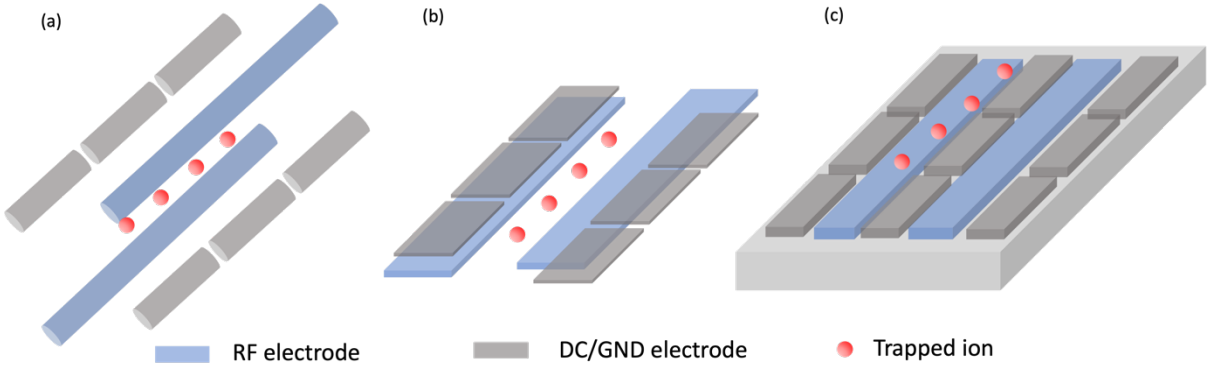


Figure 2. The geometry evolution of linear ion trap. (a) Four-rod ion trap. (b) Multilayer ion trap. (c) Surface electrode ion trap.

1.2.3 Ion Motion and Potential Model in an Ion Trap

The electrical potential in the ion trap can be expressed by equation [22, 26]:

$$\Phi = \frac{\Phi_0}{2R^2}(\alpha x^2 + \beta y^2 + \gamma z^2), \tag{3}$$

where $\Phi_0 = U + Vcos(\omega t)$, R is the distance from trap center to electrode surface, α, β, γ are factors determined by the electrode geometry. U is the DC voltage, V is the amplitude of RF voltage, and ω is the RF driving frequency. To satisfy the Laplace condition $\nabla^2\Phi = 0$, one can get:

$$\alpha + \beta + \gamma = 0. \tag{4}$$

One simplest set of the factors is $\alpha = -\gamma = 1$ and $\beta = 0$, which can be formed by the quadruple electrodes (Figure 3). Meanwhile, the motion of ion can be expressed by classical equation:

$$m\ddot{x}_i = F_{x_i}(t) = -Ze\frac{d\Phi}{dx_i}, \quad (5)$$

where m is the ion mass, F is the Coulomb force, and Z is the ion charge. After substitution, the ion motion in x and z direction can be expressed as:

$$\ddot{x} + \frac{Ze}{mR^2}(U + Vcos\omega t)x = 0, \quad (6)$$

$$\ddot{z} - \frac{Ze}{mR^2}(U + Vcos\omega t)z = 0, \quad (7)$$

which both can be further rewritten into a Mathieu equation form:

$$\frac{d^2x}{d\tau^2} + (a + 2qcos2\tau)x = 0, \quad (8)$$

$$\frac{d^2z}{d\tau^2} - (a + 2qcos2\tau)z = 0, \quad (9)$$

where $a = \frac{4ZeU}{mR^2\omega^2}$, $q = \frac{2ZeV}{mR^2\omega^2}$, and $\tau = \frac{\omega t}{2}$. Both a and q are stability factors that determine whether the ion motion is stable (i.e., with limited motional amplitude). In general, a trapped ion will remain stable in the *i* direction if $0 \leq \sqrt{a_i + q_i^2/2} \leq 1$.

The lowest-order approximation solution to the Mathieu equation describes the ion trajectory:

$$x(t) = x_0\cos(\omega_x t)(1 - \frac{q_x}{2}\cos(\omega_{RF}t)). \quad (10)$$

The trajectory consists of a secular motion at the secular frequency of $\omega_x = \frac{\omega_{RF}\sqrt{a_x + q_x^2/2}}{2} \ll \omega_{RF}$ and a micromotion at the RF frequency ω_{RF} with a small amplitude factor of $q_x/2$. Note the ion trajectory in *z* direction is similar with that in *x* direction (quadruple trap). Neglecting the effect from micromotion, the time-averaged pseudopotential describing the trapping depth of the confinement in the radial plane is expressed as:

$$\Phi_{eff}(x, z) = \frac{(Ze)^2}{4m{\omega_{RF}}^2}|\nabla\Phi(x, z)|^2. \quad (11)$$

This pseudopotential is sort of approximation that characterizes the energy required for ion to escape from the trap [27].

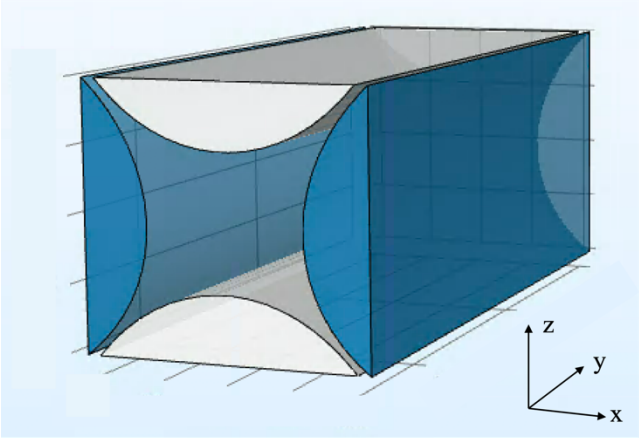


Figure 3. Electrode configuration of quadruple ion trap.

For surface electrode ion trap, the geometry design was largely dependent on the numerical modelling. However, these is an analytical approach for modeling the electric field and determining the ion trapping height, as proposed by M. House [28].

Two approximations are made in this approach. The first approximation is to use electrostatic field to represent RF field in the modelling process. This approximation is convincing since the RF field wavelength (in the range of 10^6 μm) is far larger than the electrode dimension (in the range of 10^3 μm). The second approximation is that the rectangular electrodes used in the modelling have infinite length and no gaps in between. In a typical design of surface electrode trap, the gap is normally far smaller than the electrode length. Therefore, the second approximation can also be fulfilled.

The electrostatic potential generated by a rectangular electrode is:

$$\Phi(x,y,z) = \frac{V}{2\pi}\left[\arctan\left(\frac{(x_2-x)(y_2-y)}{z\sqrt{z^2+(x_2-x)^2+(y_2-y)^2}}\right) - \arctan\left(\frac{(x_1-x)(y_2-y)}{z\sqrt{z^2+(x_1-x)^2+(y_2-y)^2}}\right) - \arctan\left(\frac{(x_2-x)(y_1-y)}{z\sqrt{z^2+(x_2-x)^2+(y_1-y)^2}}\right) + \arctan\left(\frac{(x_1-x)(y_1-y)}{z\sqrt{z^2+(x_1-x)^2+(y_1-y)^2}}\right)\right], \quad (12)$$

where $x_{1,2}$, $y_{1,2}$ are the coordinates of the electrode, and V is the applied voltage. For the long RF electrodes in surface trap ($y \to \pm\infty$), the electrostatic potential above can be rewritten as:

$$\Phi(x,z) = \frac{V}{\pi}\left[\arctan\left(\frac{x_2-x}{z}\right) - \arctan\left(\frac{x_1-x}{z}\right)\right]. \quad (13)$$

The voltage applied to the RF electrodes is:

$$\Phi(x,0,t)=\begin{cases}0, & x<-c\\ Vcos(\omega t), & -c<x<0\\ 0, & 0<x<a\\ Vcos(\omega t), & a<x<a+b\\ 0, & x>a+b\end{cases}. \qquad (14)$$

Here a, b and c are parameters that describe the electrodes dimensions, as shown in Figure 4. Substituting Equation (14) to Equation (13) and adding the potentials from two RF electrodes together, one can obtain:

$$\Phi(x,z,t)=\Phi_{RF1}(x_1,z,t)+\Phi_{RF2}(x_2,z,t)$$

$$=\frac{V}{\pi}\left[\arctan\left(\frac{a+b-x}{z}\right)-\arctan\left(\frac{a-x}{z}\right)-\arctan\left(\frac{x}{z}\right)+\arctan\left(\frac{c+x}{z}\right)\right]\cos(\omega t). \qquad (15)$$

The derivations of Equation (15) in x and z direction provide the corresponding coordinates of the ion trapping position:

$$x_0=\frac{ac}{b+c} \qquad z_0=\frac{\sqrt{abc(a+b+c)}}{b+c}. \qquad (16)$$

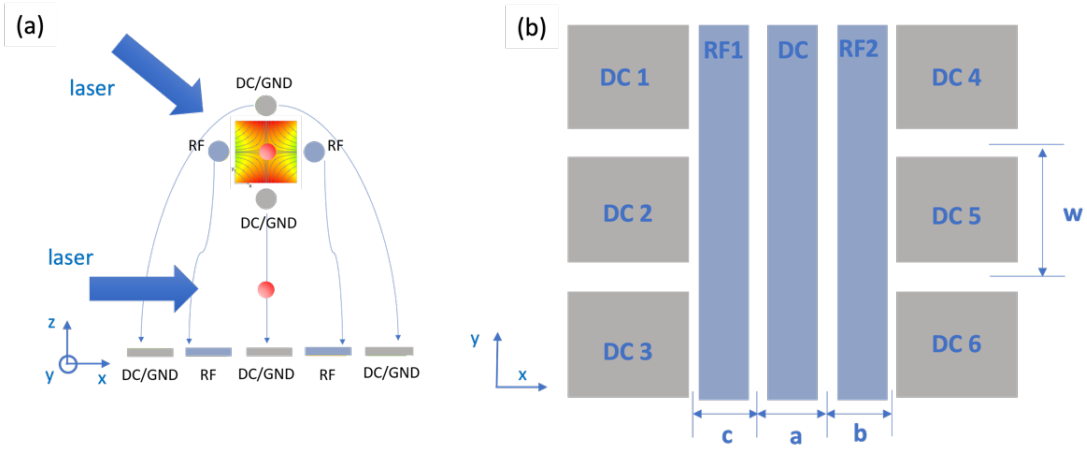


Figure 4. (a) The deformation from linear trap to surface electrode ion trap. (b) Configurations of surface electrodes in the x-y plane.

1.2.4 Strontium (Sr) Optical Qubit

Depending on the states that used for qubits encoding, qubits can be classified into three types that are Zeeman qubits, hyperfine qubits and optical qubits. Regarding Zeeman qubits, all the two states for qubits come from same ground state manifold. Due to the Zeeman shifts, one can encode the qubit with ground level splitting. The typical transition frequency of Zeeman qubit is at megahertz range. However, it is very sensitive to the magnetic field

fluctuations [29]. Special protection should be taken for Zeeman qubits manipulation. Hyperfine qubits also use ground state only for qubit states preparation. The transition frequency of hyperfine qubit is of several gigahertz since the ground state splitting is induced by nuclear spin that has a higher energy. Although the first-order sensitivity to magnetic field has been eliminated due to the different sign of two hyperfine manifolds [30], more lasers are required due to the large number of electronic levels. Different from Zeeman and hyperfine qubits, optical qubits use states not only from ground level but also a metastable *D* level. Due to the relatively large energy difference between these two states, the transition frequency is at terahertz regime.

Several constraints are applied to select a suitable ion specie [12]. A relatively simple energy level structure (with metastable level) is needed to build the two-level system and encode the qubit. Meanwhile, the energy difference between levels shall be covered by the technologically available lasers. Some other factors like ion mass and isotope may also be considered. As a result, the most widely used species are alkaline-earth (e.g., Be^+, Me^+, Ca^+, etc.) ions. The ion traps presented in this work are optically operated with $^{88}Sr^+$ ions. The energy level diagram of $^{88}Sr^+$ ion is illustrated in Figure 5. In general, level $5^2S_{1/2}$ (ground state) and $4^2D_{5/2}$ (metastable state) are used to encode $|0\rangle$ and $|1\rangle$ and the corresponding energy transition wavelength is 674 nm. Lasers with wavelength of 1092 and 1033 nm are used to repump the $4^2D_{3/2}$ and $4^2D_{5/2}$ states. Laser with wavelength of 422 nm is used for Doppler cooling and state detection. A more detailed description considering the lasers setup and operation during ion trapping test is provided in Section 3.4.1.

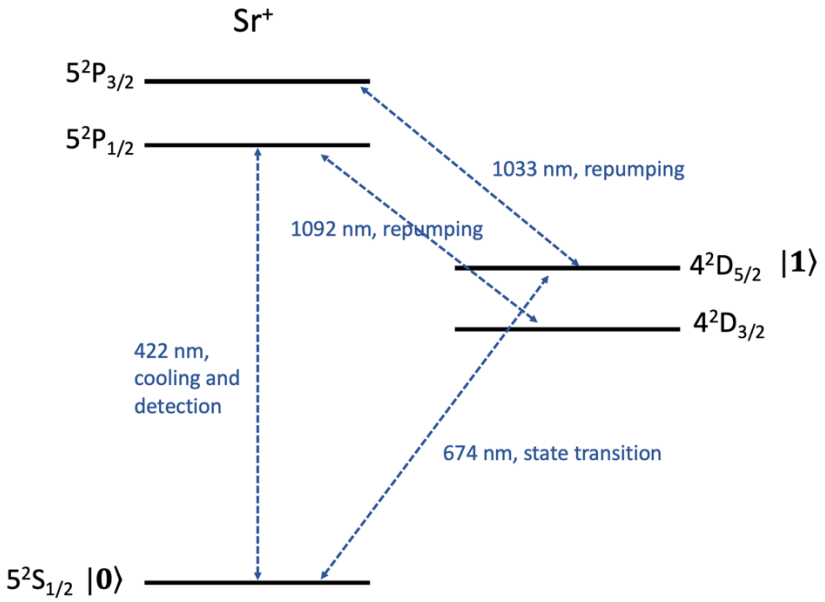


Figure 5. The energy diagram of $^{88}Sr^+$ ion.

1.3 Integration Technologies in Semiconductor Industry

1.3.1 Three-Dimensional Integration

The origin of three-dimensional (3D) integration can be traced back to the silicon on insulator (SOI) technology in 1978 [31]. Following that, the initial idea of active devices stacking in integrated chips was proposed in 1980's [32]. Until year 2006, the first CMOS sensor with 3D interconnect was developed by Toshiba, demonstrating the 3D integration application in the high-volume commercial product in semiconductor industry [33]. Interestingly, Richard Feynman who initiates the idea of quantum computing is also an important contributor in the propagation of the idea of 3D integration. In a talk named 'the computing machines in the future' given in Japan, 1985, he said 'another direction of improvement (computation performance) is to make physical machines three dimensional instead of all on a surface of a chip' [34].

With the slowdown of transistor node scaling in the past decade, advanced 3D integration technologies have been developed as an alternative approach for the continuity of Moore's law in the semiconductor industry, specifically in reducing form factor, cost, power and increasing functionality and performance [35, 36]. By extending the conventionally two-dimensional layout, assembling, or interconnections into the third dimension, 3D integration has progressively become the primary building block of advanced electronic devices. As shown in Figure 6, high performance computing devices are keeping benefited from the improved heterogeneity and reduced interconnect pitch [37].

In general, depending on the interconnect hierarchy, 3D integration technologies can be classified into three categories: 3D System-in-Package (SiP, package or system level), 3D System-on-Chip (SoC, device level) and 3D monolithic integration (transistor level) [38, 39]. The 3D SiP technology is based on the packaged die stacking, where multiple packages (for different chips) with independent wire bondings are vertically stacked. It is mature in high-volume production, but is limited by the low integration density. The post-packaging stacking is also volume-consuming. Note through silicon via (TSV) is not included in 3D SiP. The 3D SoC technology is to integrate various devices (e.g., analog, logic, memory, RF, etc.) instead of packages in a 3D approach. In this scheme, wafer thinning, bonding and TSV are extensively used to interconnect devices at different height. The 3D monolithic integration moves towards the full use of the third dimension at the transistor scale. Vertical layers of transistors are

fabricated on the same starting substrate using a build-up approach: each active layer is processed in sequence starting from the bottommost layer and nanoscale interlayer vias are needed. Correspondingly, in 3D monolithic scheme, the 3D interconnect pitch is required to be scaled down to <100 nm and the interconnect density is expected to be higher than $10^8/mm^2$ [40].

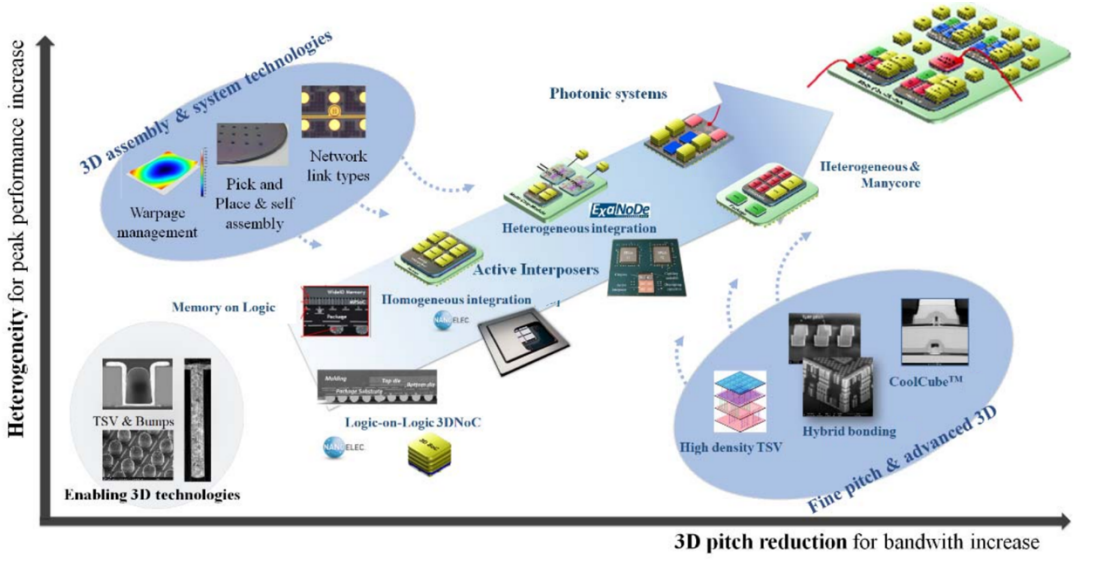


Figure 6. 3D integration roadmap for high performance computing. The figure is from Ref [37].

1.3.2 Through Silicon Via

Through silicon via, which provides the electrical connection between layers at different heights, is the key enabler of 3D IC integration [41, 42]. As compared to the wire bonding at the chip edges, TSV can be placed as a full-area array underneath the chip. Also, the typical TSV depth is ~10 - 100 µm, whereas wire bonding has a length of ~1- 5 mm. This allows TSV with smaller resistance, inductance and capacitance, reducing the latency and power consumption.

Depending on the timing or sequence of TSV introduction into the integrated chips, the fabrication of TSV can be divided into three approaches [43]:

- Via-first approach: TSV is formed before the active device fabrication (i.e., front end of line (FEOL) process).
- Via-middle approach: TSV is formed after the device FEOL fabrication process, but before the wiring metallization (i.e., back end of line (BEOL) process).
- Via-last approach: TSV is formed after the BEOL fabrication process.

The fabrication process of TSV mainly consists of four steps [43]:

- Via etching: Due to the large aspect ratio (i.e., via depth over diameter) of TSV, a high selectivity via etching process is needed. Currently the most widely used etching process is Bosch process, which uses alternate steps of via bottom etching and via sidewall passivation (protection). As a result, a scallop feature can be found on the via sidewall after etching (Figure 7).
- Via insulation: An insulation layer (i.e., TSV liner) is required to be formed between metal via and silicon substrate to avoid leakage and short-circuit. Plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD) can be used for the insulation layer formation. A good in-via deposition uniformity is the key challenge.
- Via filling: Currently, due to the smaller resistance, copper filled vias are more popular than the tungsten and polysilicon filled counterparts. Before the filling of copper, a barrier layer (e.g., titanium nitride, tantalum, etc.,) and a copper seed layer are required to be deposited onto the via sidewall. A good step coverage is required. During the electroplating (ECP) of copper, a 'bottom-up' approach (i.e., higher plating speed at via bottom) is normally used to enable a void-free via filling.
- Overburden removal: A step of chemical mechanical polishing (CMP) process is required to remove the copper overburden after the via filling process. The barrier and seed layers are simultaneously removed. The wafer is also planarized.

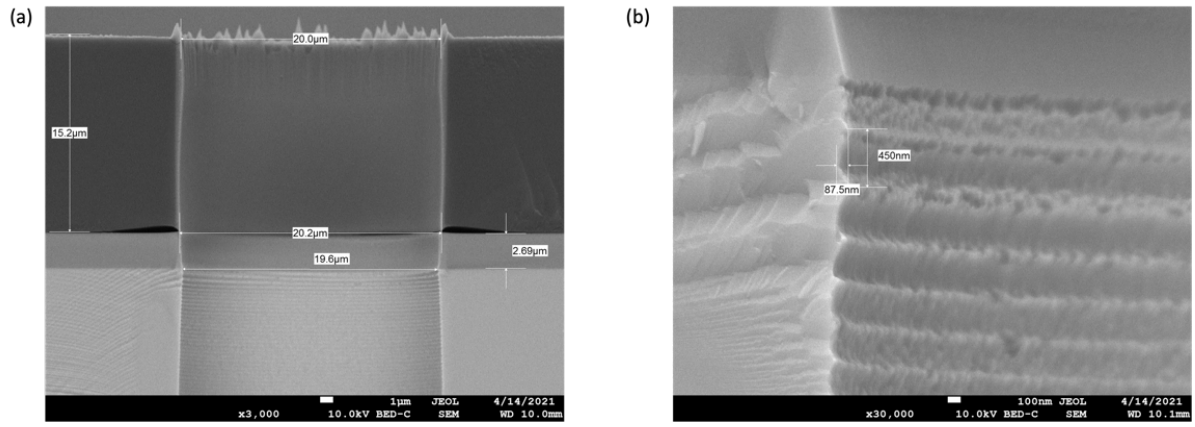


Figure 7. Cross-sectional SEM images of the etched via using Bosch process. (a) Overall view of the etched via (including photoresist, silicon oxide and silicon). (b) Zoom-in view of the etched scallop features on the via sidewall.

1.4 Thesis Outline and Original Contributions

As mentioned earlier, the development from macroscopic and mechanically assembled linear trap to microscopic and coplanar surface electrode trap has opened the door for the incorporation with advanced fabrication techniques. To make a step forward, in this thesis, the well-developed 3D integration technologies in semiconductor industry are adopted to the ion trapping devices to boost the scalability. In particular, 3D interconnects (i.e., TSV) and other function modules (e.g., silicon photonics and multilayer metallization) are integrated into the surface electrode ion trap step by step. The thesis is outlined with six chapters.

Chapter 1 gives a brief introduction on the quantum computing mechanics, the fundamentals of ion trap and the 3D integration technologies in semiconductor industry.

In Chapter 2, a comprehensive literature review is presented on the surface electrode ion trap development roadmap. Specifically, the ion trap substrate evolution, the interconnection technology evolution, and various integration attempts of conventionally bulk components are covered. Meanwhile, the use of advanced 3D integration technologies in other physical implementations of qubits is introduced.

In Chapter 3, surface electrode ion traps on various substrates (high resistivity silicon, silicon with grounding plane and glass) are designed, fabricated and tested. The obtained performance is compared. This chapter serves as an essential preparation for the next-step TSV integration into ion trap.

Chapter 4 presents a novel ion trap design in which TSV is incorporated in place of the conventional wire bonding. The geometry evolution, CMOS-compatible fabrication process, electrical testing results together with analytical and numerical analysis, and ion trapping test are given in detail. The imperfections and corresponding solutions of TSV integrated trap are also discussed.

In Chapter 5, based on the developed TSV integrated ion trap, functional modules including silicon photonics and multilayer metallization are further integrated. The delicate design process and intricate fabrication steps are elaborated.

Chapter 6 gives a summary of this thesis. In addition, some hints towards future research directions are provided.

Chapter 2. Review on Integration Technologies for Quantum Computing Devices

In this chapter, a literature review is presented on the advanced integration and packaging technologies in four different quantum computing devices (namely ion trap, superconducting circuit, silicon spin and photon). For the surface electrode trap (the key focus of this thesis), a more comprehensive roadmap is provided, from the evolution of substrate material and interconnection technologies to the various on-chip integrated electrical and optical components. In the case of other qubits candidates, an introduction in terms of basic quantum operations and specific scalability bottlenecks is first given. Subsequently, the current solutions particularly those using 3D integration technologies are reviewed. In the end of this chapter, there is a short discussion on the 3D integration technologies classification and thermal management after 3D integration.

2.1 The Integration Roadmap of Surface Electrode Ion Trap

2.1.1 Evolution in Substrate Materials and Interconnection Technologies

Two factors shall be considered to select a suitable ion trap substrate, which are respectively RF loss and manufacturability [44]. Initially, materials with good dielectric property were more favourable options. For example, the first surface electrode ion trap was on fused silica [23]. Similarly, substrates like printed circuit board (PCB), sapphire, quartz and glass were extensively used [45-49]. Due to the limited compatibility to the standard fabrication techniques (e.g., etching), the trap electrode geometries on these dielectric substrates were generally simple and poor at scalability. In contrast, silicon, as the backbone of semiconductor industry, is endowed with the most advanced fabrication process. The use of silicon as the ion trap substrate would certainly improve the manufacturability to an unprecedented level. However, to avoid sacrificing the RF performance, some modifications were required to be adopted on the silicon substrate. The first modification is to change the silicon resistivity by

tuning the dopant concentration. On the one extreme, when the resistance is sufficiently high, no current would flow through silicon. On the other extreme, when the resistance is sufficiently small, the voltage drop can be neglected. Early from 2006, highly doped silicon was used as the substrate of microchip trap to minimize the RF loss by reducing the resistance [50, 51]. Also, in a work reported in 2014, an intrinsic silicon substrate was used at cryogenic environment to freeze out the charge carriers [52]. As a result, silicon was converted into a good insulator and low RF loss was achieved. Another modification option is to introduce an additional grounding plane. By shielding the lossy silicon substrate from the RF signal penetration, the RF loss can be considerably reduced. Again, this option was first adopted in the multilayer ion trap and now widely used in surface electrode ion trap on silicon substrate. Similarly, people can increase the thickness of insulation layer between RF electrode and silicon substrate. In a trap demonstrated in 2009, a 10 μm SiO_2 is used [53]. However, the thick oxide layer formation and patterning are not compatible with standard fabrication. Besides, the thick oxide layer can induce high local stress and even wafer warpage, which shall be avoided.

The interconnection technology development basically follows a roadmap from above-surface overhung wire bonding to the on-chip integrated multilayer metallization and TSV. Previously, wire bonding was commonly used due to its cost-effective and simple-assembly characteristics. Wire bondings were laterally located at the chip edges and kept with a sufficient distance from the trap centre to avoid the possible optical path block (Figure 8 (a)) [23]. However, with the development of ion trap geometry, certain electrodes located at the geometry centre are inevitably surrounded by the peripheral electrodes, challenging the accessibility of wire bonding. Also, the increase of electrodes number will result in the interconnections overcrowding at the wafer edge, and the incorporation of other functional components that necessitate independent signal wires will worsen the case. In the past 15 years, the geometry of surface electrode ion traps has been progressively evolved from ~10 electrodes to hundreds of electrodes with complex layout, in order to trap more ions and facilitate operations like ion shuttling [47, 54]. As limited by the wire bonding number, the traps always feature a dumbbell shape to accommodate more bonding pads at two ends [10, 55]. To mitigate these issues, one needs to explore the third dimension of interconnections. The previous approach is to employ multilayer metallization, where patterned metal layers and dielectric materials are alternately overlapped beneath surface electrode (see Figure 8 (b)). Small vias through dielectric layers are required to build interconnections between different metal layers [56-58]. In a work reported in 2014, 8 interconnection layers were accommodated in a trap,

which was fabricated with 90-nm CMOS process on a 300 mm multi-project wafer [56]. The incorporation of routing leads underneath allows for the flexible design of surface electrodes geometry, particularly in the case where extremely small electrodes are required (e.g., junctions in multi-track traps). However, this approach also comes with issues. First, though multiple steps of CMP are used, the accumulated wafer thickness variations may hinder the on-chip integration of optical components. In addition, the multilayer metallization may increase the coupling parasitics, resulting in high RF losses and subsequent heating of the device.

Through substrate vias are another effective approach to ion trap integration. With relatively small form factor and large pitch, through substrate vias feature small parasitic and are more compatible with photonics integration. In a work reported in 2015, polysilicon filled vias of ~50 μm diameter were used for surface electrode connection (Figure 8 (c)) [59]. Similarly, in a ring trap design proposed in 2017, the circular electrodes were connected with 100 μm diameter electrical vias etched through a 70 μm glass substrate followed by 800 nm gold deposition [60]. Though the fundamental merits of via were already demonstrated, some challenges remain to be solved. For the polysilicon filled via, due to its poor conductivity, only DC electrodes were contacted with vias, and additional platinum silicide was required to create ohmic contacts between electrodes and polysilicon. In terms of the via adopted in the ring trap, the customized fabrication process limited the large-scale implementation. Meanwhile, the cointegration of TSV and multilayer metallization has not been demonstrated in the existing ion trapping devices. In summary, further advancement is required for the integration of TSV in the ion trap.

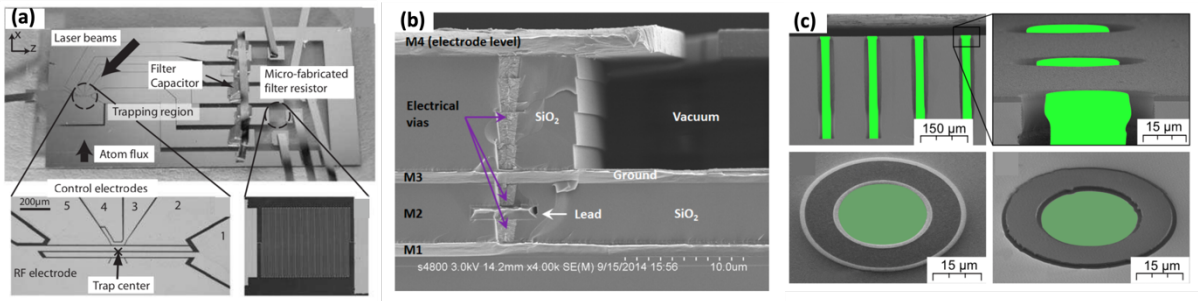


Figure 8. (a) First surface electrode ion trap that used leads as interconnections. (b) Ion trap integrated with multilayer metallization. (c) Ion trap integrated with polysilicon filled via. Panels used from [23] for (a), [57] for (b), and [59] for (c).

2.1.2 Photonics and Electronics Integrated Surface Electrode Ion Trap

Free-space optics (e.g., mirrors and lenses) are heavily used in the ion trapping setup, from which laser beams are routed through the vacuum chamber window and delivered onto the ions. Similarly, fluorescence from the ions is collected by photomultiplier tube located outside the chamber. However, with increasing number of trapped ions, the optical input and output interface for control and measurement of individual ions is significantly compressed. At the same time, the increased dimensions of ion trap itself may lead to undesired beam scattering. Therefore, the integration of photonics become necessary. In 2011, optical fibers for light delivery were embedded underneath ion trap through drilled holes on the substrate [61, 62]. Nevertheless, the large diameter of fibers, complex hole drilling process and exposed dielectric surface make direct fiber integration less compatible for large-scale application. Until year 2016, a waveguide and grating coupler integrated ion trap was demonstrated [63]. A 120 nm SiN layer was introduced underneath surface electrode as the core material for the photonics components, of which similar micro/nano fabrication process was adopted. Light with wavelength of 674 nm was routed by the waveguides and focused to the ions by the grating couplers at multiple locations (Figure 9 (b)). Recently, with similar techniques, waveguides and grating couplers were designed for all wavelengths of light (from 422 to 1092 nm) required for the quantum operations of Sr^+ ion, and were fully integrated into a single trap. This undoubtedly demonstrates a milestone for complete photonics integration of single ions [64]. However, the precise alignment of multiple beams at same location remained a challenge [64]. Meanwhile, in another work, the integrated photonics were used to implement the two-ion quantum logic gate with a fidelity as high as 0.993(2) [65]. Simultaneously, the integration of optical components that facilitate efficient fluorescence collection was also advancing in the past decade, with a similar roadmap as the light input integration. At the beginning, bulk optics (e.g., fibers) were mounted into the traps in relatively brute-force approaches (Figure 9 (a)) [66]. Following that, localized components like micromirrors and lenses were integrated and fabricated together with ion trap to improve the coupling efficiency [67-69]. In addition, traps directly fabricated onto high-reflectivity or transparent substrates were also demonstrated [70-72]. In recent years, the ion trapping communities were also exploring the monolithic integration of high-efficiency photodetectors into the ion trap [73, 74]. In a work reported in

2020, an average readout fidelity of 0.9991(1) was achieved for a trap-integrated superconducting nanowire single photon detector (Figure 9 (c)) [74].

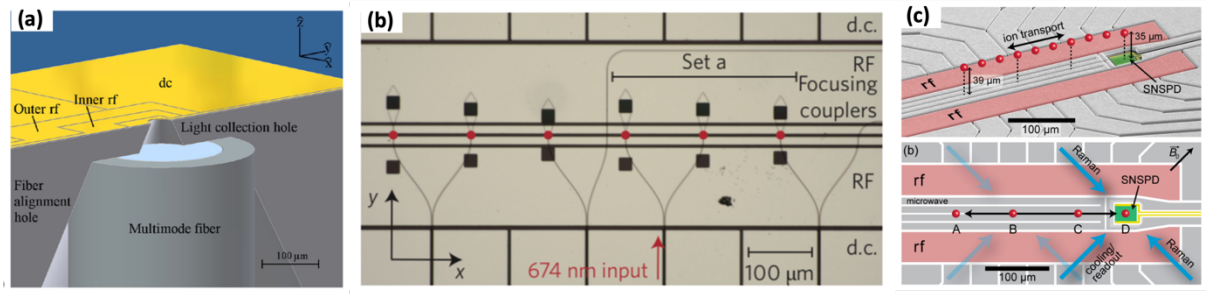


Figure 9. (a) Fiber inserted into an ion trap. (b) Waveguide and grating coupler integrated beneath surface electrode in an ion trap. (c) Superconducting nanowire single photon detector integrated in an ion trap. Panels used from [66] for (a), [63] for (b), and [74] for (c).

At the same time, passive electronic components like trench capacitors were integrated in ion trap to filter the RF pick up on the control electrodes [59], yet the full integration of RF resonators commonly used for voltage step-up is still not demonstrated, partially due to the power dissipation issue. In terms of active electronics integration, in 2019, voltages sources together with DACs (digital-to-analog converters) were integrated into trap to generate low-noise control potentials on the electrodes [75]. In fact, early in year 2012 and 2014, the attempts to place RF resonator and DACs inside the vacuum chamber were disclosed [76, 77]. However, neither works used on-chip integration strategy. Besides, it is necessary to mention that the 3D integration of magnetic components (e.g., microwave conductors) for qubits driven by microwave fields is also undergoing [78, 79].

2.2 Advanced Integration Technologies in Various Quantum Computing Devices

2.2.1 Superconducting Circuit Qubit

At sufficiently low temperature ($kT \ll \hbar\omega$), the potential of a resonant circuit consists of a capacitor and inductor becomes quantized with a constant energy difference ($\hbar\omega$) between neighboring levels (harmonic oscillator). By introducing a Josephson Junction (a thin insulated layer sandwiched by two superconducting thin films) into the circuit, the energy difference turns into anharmonic, enabling specific state addressing and thus the encoding of qubit.

Depending on the types of encoded qubit (e.g., flux, charge, etc.) [80, 81], different layouts are implemented for the fundamental circuits built from capacitors, inductors and Josephson Junctions (Figure 10 (a)). The most popular transmon qubit (charge qubit) is used as an example to demonstrate the quantum operations for superconducting qubit [82, 83]. The single qubit gate (x or y axis rotation) is predominately driven by coupling a microwave signal (5-10 GHz) via a coplanar waveguide line, whereas the z axis rotation is driven through a flux tunning line if needed. For two qubit gate, two neighboring transmon qubits are normally coupled through a capacitor in between (capacitive coupling). In addition, the qubit transition frequency can be dynamically tuned by incorporating a dc superconducting quantum interference device (dc SQUID, a superconducting loop interrupted by two Josephson Junctions), which is essential for both single and two qubit gates implementation [84-87]. For superconducting circuit readout, dispersive readout is typically used by coupling the qubit to a transmission line resonator [88]. In summary, all components that are required to define, manipulate and readout superconducting qubits are macroscopic circuits, which can be patterned on the superconducting films with lithography-based techniques (Figure 10 (b)). This makes it inherently compatible with advanced CMOS process and thus promising for large-scale realization. However, some challenges are remained. As differed from large array of classical bits in memory that can be parallel addressed using Word or Bit lines, every single superconducting qubit requires independent circuits designed for control, readout, and qubit-qubit coupling, resulting in huge footprint and interconnection overhead. Meanwhile, most of the circuit layouts are still in a 2D scheme, where interconnections for various signals can only access the qubits via chip perimeters. In the Sycamore processor demonstrated by Google in 2019, a rectangular array of 54 qubits took a surface area of ~10 × 10mm [9]. Therefore, to scale up the 2D scheme and maintain the qubit addressability, 3D integration technologies are essential.

The incorporation of superconducting multilayers to increase wiring density was started in 2005 [89]. In 2010, D-WAVE employed four superconducting Nb layers to supply 64 flux biases to flux qubits, where Josephson Junctions were located between the bottom two layers [90]. HYPRES also developed a technique to extend eight superconducting layers underneath conventional four-layer chip [91]. Similarly, MIT Lincoln Laboratory released a roadmap, envisaging the fabrication development for 4, 8 and 10 superconducting layers with minimized Josephson Junction diameter (from 1000 to 500nm) [92, 93] (Figure 10 (c)). Though superconducting multilayers is able to ease the interconnections crowding issue, the obtained

coherence time is generally shorter as compared to the qubits with single layer structure, which is limited by the fabrication complexity (CMP process is heavily used) and undesired interlayer coupling. Furthermore, the natural defeats exist in the interlayer amorphous dielectric materials (SiO_2 and Si_3N_4) can disturb the electric field and thus decrease the qubit lifetime [94].

To mitigate this challenge, a 3D integrated superconducting qubit scheme was proposed in 2017 [95]. This scheme consists of three bonded chips that are individually fabricated. The top chip is the qubit chip which contains qubit circuits, and the bottom chip is for readout and interconnection. To bridge these two chips, an interposer chip that incorporates superconducting TSV is bump-bonded in between as shown in Figure 10 (d). With this scheme, the capability for complex interconnection routing is maintained in the bottom chip, while the qubit performance in the top chip will not be degraded. The first step of this scheme was demonstrated in 2017, where the qubit chip was flip chip bonded to a chip underneath containing circuits specifically for qubit readout and control (Figure 10 (e)) [95]. As the second step, superconducting TSVs that transmit signals from chip backside to the front side were integrated into the interposer chip, controlling the qubits chip bonded on the top [96]. In addition, to demonstrate the full potential of this 3D scheme, qubit circuits were also directly fabricated onto superconducting TSVs integrated interposer (Figure 10 (f)). The resulting mean lifetime is ~10 μs, in favorable comparison with state-of-the-art planar devices. Recently, this 3D scheme has been widely adopted. For example, in the *Zuchongzhi* superconducting quantum processor, two sapphire chips which respectively carries qubits and readout circuits were aligned and bonded [97].

Indeed, as an important component in the abovementioned 3D scheme, superconducting TSVs have been independently investigated over past 5 years [98-101]. However, most of the work focused on the via fabrication process (e.g., via etching, sputtering or atomic layer deposition for via metallization), and did not move forward to the cointegration of superconducting TSVs with real qubits. Meanwhile, other structures like airbridges and sapphire balls with diameter of 200 μm were also explored to extend the control and measurement circuits into the third dimension [102, 103]. In addition to those using microfabrication techniques, mechanically assembled 3D packaging architectures were also proposed using either spring-mounted 3D microwires or multilayer PCB clamping [104, 105]. However, the alignment process and large form factor hinder them from large scale implementation.

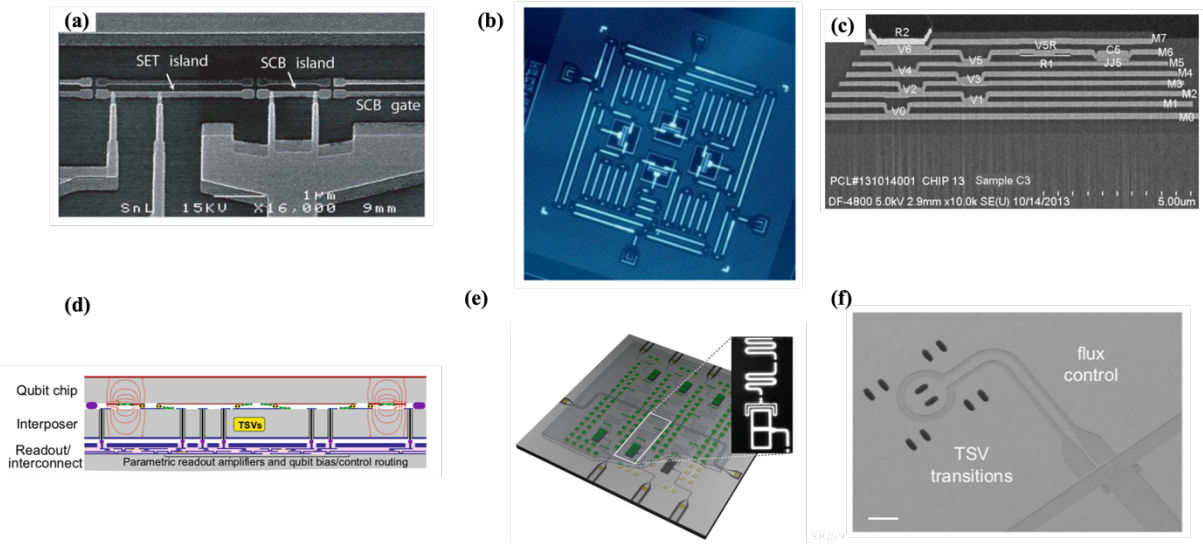


Figure 10. (a) SEM (scanning electron microscope) image of a charge qubit consists of Copper-pair box and single electron transistor. (b) Image of a device with 4 qubits, 4 quantum bus and 4 readout circuits. (c) Cross-sectional SEM image of 8 Nb layers, with Josephson junction (JJ), resistor (R) and vias (V). (d) The 3D integrated superconducting qubits scheme. Readout circuit and qubit circuit were separated and interconnected with interposer that contains TSVs. (e) Schematic of a qubit chip that was flip-chip bonded to the chip specifically designed for readout and control. (f) Superconducting circuit built directly on the TSV integrated substrate. Panels used from [81] for (a), [83] for (b), [93] for (c), [95] for (d) and (e), [96] for (f).

2.2.2 Silicon Spin Qubit

Different from qubits based on trapped ion or superconducting circuit that have a relatively long research history, the first single qubit gate and two qubit gate of silicon spin qubits were respectively demonstrated in 2012 and 2015 [106, 107]. To date, the number of entangled qubits reaches three in silicon and four in germanium [108, 109]. Silicon spin qubits are encoded on the spin of electrons, that either bound to the embedded dopants or quantum dots (MOS and SiGe material systems are commonly used to define quantum dots) [110, 111]. Unlike charge-based qubits that generally suffer from electric noise, spin qubits can only be interacted magnetically and therefore feature long coherence time. An in-plane large static magnetic field is required to create the Zeeman splitting. The single qubit gate is achieved using electron spin resonance technique, in which an AC current is sent into a transmission line close to the qubit and thus generate a localized AC magnetic field resonant with spin transition frequency. The two qubit gate is implemented via the exchange interaction [112]. To facilitate the entanglement beyond immediate neighbors, coherent transport of spin qubits across the chip can be used [113]. For the qubit readout (spin encoded by single electron), a process known as spin-to-charge conversion is used, where the qubit electron is coupled to a single

electron transistor (SET), and under specific conditions spin-up electron will tunnel to the electron reservoir and produce a detectable current pulse [114, 115]. It should be noted that all these basic operations are controlled and enabled by appropriate voltages tunning on the corresponding gate electrodes located on top of qubits (Figure 11 (a)) [116]. In addition to the abovementioned simplest spin qubit defined by single electron, singlet-triplet qubit and three-electron spin qubit (e.g., hybrid qubit) are also being investigated which can be controlled partially or fully electrically [117, 118].

The counted, deterministic implantation of single donors, as well as the novel methods for precise placement and alignment are key challenges that significantly limited the large-scale application of the spin qubit bound in donor system [119, 120]. On the other hand, taking advantage of the lithography-based fabrication, quantum dot-based silicon spin qubit has exhibited the favorable scalability. In terms of fabrication compatibility, quantum dot in MOS (metal-oxide-semiconductor) system is naturally more appealing than its counterparts in SiGe system, though the interface disorder between Si and amorphous SiO_2 may introduce undesired noise and degrade the fidelity [121]. In 2016, silicon spin qubit with a geometry derived from the field effect transistor (compact two gate FET) was developed as shown in Figure 11 (b), where two top gates were respectively used to control two quantum dots (in series) that defined in the silicon channel [122]. This work started from the standard CMOS process in transistor fabrication and adapted it to achieve the quantum functionality. Though auxiliary quantum dot was required for readout and two qubit gate was yet performed, this work indeed demonstrated the often-argued compatibility of silicon spin qubits with CMOS fabrication process.

Similar to the superconducting circuit qubits, even in a huge array of millions of qubits, the independent control from multiple gate electrodes is anticipated to be indispensable for every single silicon spin qubit. As a result, the gate electrodes number and corresponding classical circuit that control electrodes will boost with the increase of qubits number, posing significant challenges to the qubit architecture itself as well as the quantum-classical interface. To mitigate the first challenge, a 3D architecture was proposed in the qubit level [123, 124]. As shown earlier, two quantum dots in series were fabricated, of which one was encoded as a spin qubit whereas the other one was for qubit readout (sensing dot) [122]. In the new 3D architecture, the sensing dot was repositioned to the layer underneath the qubit dot layer (Figure 11 (c)). A controllable and addressable tunnel barrier was introduced to transmit electron in between the two layers. In addition, separate control layers that contain gate electrodes were required for both sensing and qubit dot layers. In this scheme, the footprint overhead due to the additional

sensing dot can be minimized and therefore the scalability is enhanced. In terms of the interface overcrowding, 3D integration scheme was also proposed for future quantum computer processor where the bottom layer and top layer of a silicon-on-insulator wafer were respectively used to accommodate qubits array and classical transistors for control (Figure 11 (d)) [125]. Vias through the insolation layer were required to connect the bottom and top layers, enabling a scalable quantum-classical interface. Although current CMOS manufacturing capabilities may not fulfill the stringent requirement in terms of qubits uniformity and reproducibility, this conceptual architecture makes an important step towards large-scale silicon spin qubits scenario. Recently, a 3D dielectric resonator was stacked on top of the qubits circuit with a sapphire spacer in between [126]. In place of conventional transmission lines that placed close to every single qubit, the dielectric resonator was used to generate a global magnetic field across the entire quantum circuits underneath and the ESR of single qubit with this field was successfully demonstrated. Again, this global field eases the concern of large AC current running into the quantum circuits and the control of millions of qubits appears to be practical.

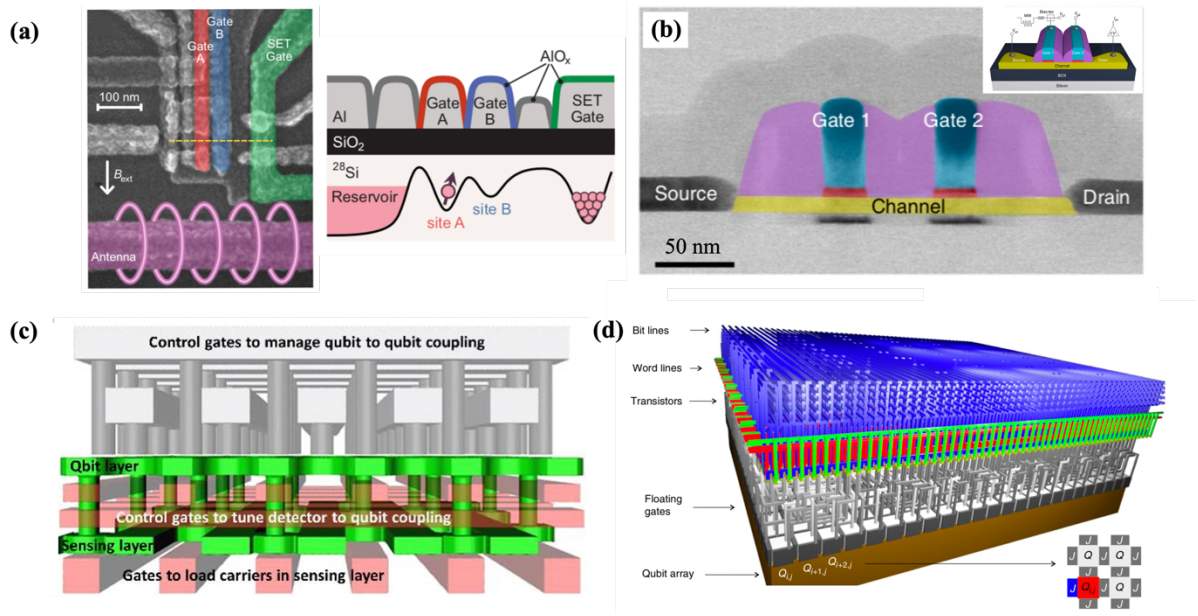


Figure 11. (a) False-colored SEM image of silicon spin qubit device consists of gate electrodes, microwave transmission line and SET. A corresponding schematic is shown on the right. (b) Colorized TEM (transmission electron microscopy) image of the CMOS qubit device, where two quantum dots were defined in series. (c) The 3D architecture of silicon spin qubit. Two layers of quantum dots that respectively used as qubit and for sensing were coupled through a vertical tunnel barrier. (d) The 3D architecture of classical-quantum interface of silicon spin qubits. Transistors on the top were used to control the qubits array underneath. Panels used from [113] for (a), [122] for (b), [123] for (c), and [125] for (d).

2.2.3 Photon Qubit in Silicon Photonics

Photons are appealing to be used as qubits since they are almost free of decoherence. With that, the stringent environmental conditions (e.g., millikelvin temperature and ultra-high vacuum) as required by other qubit candidates can be eliminated, enabling photon qubits with high scalability. The previous concern was the heavily used bulk optics (beam splitters and mirrors) that located on the large vibration-free table. However, with the incorporation of silicon photonics, photons can now be guided and routed by waveguides with high phase stability (Figure 12 (a)) [127, 128]. Meanwhile, photons generation, state manipulation, and photons detection can also be performed on-chip using corresponding photonics components together with delicate photonic circuit design [129, 130]. Though the photon qubit can be encoded in various degrees of freedom (polarization, path, etc.) and the single qubit rotation can be straightforwardly performed by using waveplates and beam splitters, the extremely strong nonlinearity required for a two-qubit gate (i.e., Controlled NOT gate) implementation has not been demonstrated [131]. In 2001, a landmark scheme was proposed to implement the universal quantum computing with linear optics only, in which the CNOT gate on control and target qubits is conditional on the single photon detection of two auxiliary photons [132]. Nevertheless, the unfavorable consequence is that the gate is non-deterministic and only a small fraction of the outputs is used. To achieve a near-deterministic gate, the overhead of auxiliary photons will become exceptionally huge. Different from the abovementioned qubit candidates that have demonstrated single and two qubit gates but lack scalability, photon in waveguide circuits is naturally scalable thanks to the silicon photonics advancement. However, the challenge is to make it quantum, or more particularly, to achieve the entangled logic gate efficiently, which requires further theoretical and experimental innovations. Currently, one of the key requirements is to develop high efficiency single photon sources and single photon detectors, which are integratable to the sophisticated photonics circuit [96].

Two types of single photon sources are commonly used which are respectively quantum dots single-photon source and parametric photon-pair source. The superior advantage of quantum dots is that the resonance fluorescence photons from them are deterministic. Nevertheless, it is challenging to fabricate quantum dots array with high uniformity and repeatability. Also, the alignment between quantum dots and waveguides-based quantum circuit is troublesome [133, 134]. In 2016, a pick-and-place technique was developed as shown in Figure 12 (b) in which preselected III-V quantum dots in nanowires were transferred and

integrated into SiN waveguides on silicon substrate using a micromanipulator [135]. This technique allows for the precise alignment and high coupling efficiency between quantum dots and waveguide circuits. On the other hand, parametric photon-pair source is normally generated by pumping nonlinear waveguides, which makes it inherently integratable. Using similar fabrication techniques as quantum circuits, identical but individually controllable single photon source array was achieved [136]. However, parametric photon-pair source is non-deterministic with a probability of 5-10%. Though time or spatial multiplexing techniques can be applied to increase the probability, the resultant source overhead will degrade the overall performance (computation speed and chip footprint).

Single photon avalanche diode (SPAD) and superconducting nanowire single photon detector (SNSPD) are particularly popular in the quantum photonics circuit for single photons detection. As compared to SNSPD, SPAD eliminates the stringent requirement of low operation temperature (several Kelvins). However, the poor performance (detection efficiency of <10%) and relatively complex fabrication process make it less applicable in the integrated system [137]. On the contrary, waveguide integrated SNSPDs have been demonstrated with >90% detection efficiency and extremely low dark counts [138-141]. The trade-off is that the required cryogenic apparatus (for SNSPDs only) introduces resources overhead. In a typical integrated SNSPD, patterned superconducting nanowires are used to absorb the photons incident from the waveguide underneath (Figure 12 (c)). To enhance the absorption process, as reported in [142], waveguide was etched with holes to define a microcavity for superconducting nanowire and thus achieving the near-unity quantum efficiency. However, due to the incorporation of various superconducting materials and additional tens of fabrication steps, the resultant yield of large-scale quantum circuit may be significantly degraded as the number of integrated SNSPDs grows. In 2015, a micrometer-scale flip chip method was demonstrated to transfer ten SNSPDs onto the same photonic circuits as shown in Figure 12 (d) [143]. Based on separate fabrication and individual pre-selection of SNSPDs and photonic circuits, a 100% device yield was achieved.

Though single photon sources and detectors can be integrated into the photonic circuits in an out-of-plane approach, the waveguide circuits themselves generally feature a 2D geometry. This is limited by the lithography and etching based fabrication process. However, the femtosecond laser direct-write (FLDW) technique is able to build a novel 3D integrated waveguide circuits by focusing the laser beams at different depth in the substrate (Figure 12 (e)) [144-147]. In terms of device level integration, single photon sources, detectors as well as

multiple waveguide circuits can be stacked vertically in a 3D fashion. Optical vias may be required to interconnect modules at different heights [148, 149].

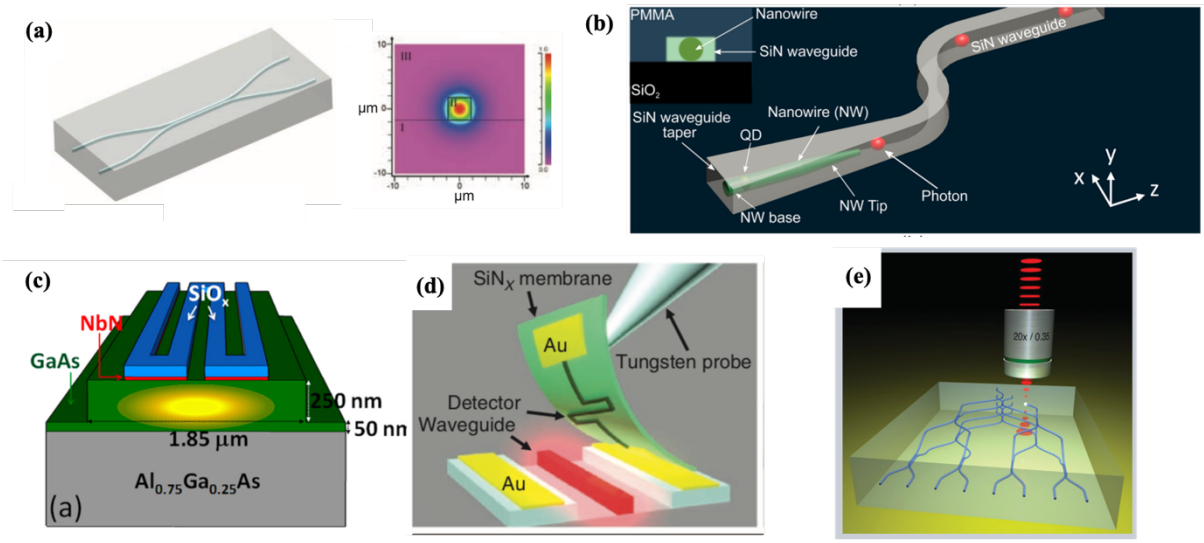


Figure 12. (a) Schematic of a waveguide circuit used to entangle photons, together with a modeled transverse intensity profile. (b) Schematic of a III-V quantum dot in a nanowire that was transferred into a SiN waveguide. (c) Schematic of a waveguide integrated superconducting nanowire single photon detector. Four NbN wires were directly patterned on top of the GaAs waveguide. (d) Schematic showing the process of transferring individually fabricated SNSPD onto a waveguide circuit. (e) Schematic of a laser writing process to build 3D waveguide circuits. Panels used from [127] for (a), [135] for (b), [138] for (c), [143] for (d), and [147] for (e).

2.3 Discussion

2.3.1 Classification for 3D Integration Technologies

Table II gives a comparison of the abovementioned four qubit candidates, in terms of the environment requirement, various control signal, qubit feature size and pitch, challenges to scale up as well as the current status of the investment from industry. Figure 13 summarizes the 3D integration technologies adopted in various quantum computing devices according to the integration hierarchy. The well-known concepts in electronics 3D integration are used as reference (see Section 1.3.1). The first hierarchy (3D SiP) is to integrate the bulk components into the quantum chip, such as the fibers in ion trap. The next hierarchy (3D SoC) is at the classical-quantum interface. The goal is to maintain the I/O accessibility of individual qubits with the boost of qubits number, such as the multilayer metallization integration in ion trap in place of wire bonding. The final hierarchy (3D monolithic integration) is at the device itself, aiming to transfer the 2D qubit architecture into a 3D fashion. Laser written 3D waveguide

circuits is a good example in this hierarchy. Meanwhile, quantum dots that aligned vertically was proposed but has not been demonstrated.

Table II. Scalability Comparison of Various Quantum Computing Devices.

Qubit type	Temperature and vacuum	Control signal	Feature size	Pitch between qubits	Challenges to scale up
Ion Trap	Ambient and ultra-high vacuum^	Lasers, RF and DC voltage	~5 μm (gap width between electrodes)	~10 μm	a. flexible interconnection b. electrode and photonics fabrication node difference c. off-chip light alignment with ions
Superconducting circuit	~10mK and high vacuum*	Microwave current, DC current, RF control[#]	~50 nm (Josephson Junction)	~1 mm	a. complex circuit layout b. cryo-electronics c. noise shielding and filtering d. entangle with neighboring qubits only
Silicon spin	1K and high vacuum*	DC magnetic field, AC magnetic field, DC voltages, RF control[#]	~50 nm (gate electrode)	10-100 nm	a. multiple quantum dots placement and alignment b. complex electrodes layout c. cryo-electronics d. noise shielding and filtering
Photons	Ambient and atmosphere	Lasers, DC voltage, RF control[#]	200 nm (waveguide)	~200 μm	a. high efficiency single photon source and detector b. the integration and alignment with waveguide circuit

^Cryogenic apparatus in ion trapping test also benefits for anomalous heating reduction; * The high vacuum (down to 0.1 mbar) is required by the dilution refrigerator; [#]RF control is required for the pulsed operations within qubit lifetime.

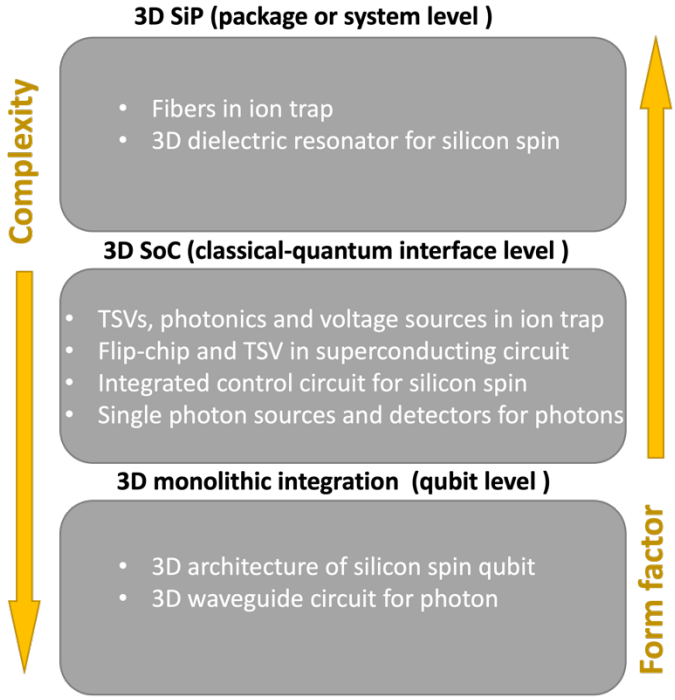


Figure 13. The hierarchy of 3D integration technologies used in various quantum computing devices.

2.3.2 Thermal Management for 3D Integrated Quantum Computing Devices

The heating issue of 3D integrated chips is one of the major constraints for its broad applications [150, 151]. In general, as more components and interconnections are incorporated, higher loss/heating will be generated. The compact architecture will aggravate the situation due to the lack of efficient heating dissipation path. Moreover, the commonly used organic substrates (e.g., printed circuit board) that located 3D integrated chips are not a good heat sink.

In the field of quantum computing, heating issue becomes more daunting as additional decoherence source is introduced. As a result, the qubit lifetime and gate operation fidelity may be reduced. In the voltage source integrated ion trap, the temperature of trap increased from 4 K (cryogenic apparatus) to 50 K due to the high power dissipation (500 mW) from integrated DACs, leading to a high heating rate of the trap [75]. The situation is more complex for qubit candidates working at ~10 mK. Conventionally, for superconducting circuit and silicon spin qubits, most of the classical control electronics are located outside the dilution refrigerator and connected to the qubits layer with long coaxial cables. However, the induced signal latency is even comparable with the two-qubit gate speed. Also, the arrangement of free-space cables for millions of qubits will become unmanageable. To mitigate these issues, the idea of placing the classical electronics closer to the qubit layer was proposed, triggering the recent developments of cryo-electronics working at 4 K [152-154]. Though a 3D architecture is required to integrate the cryo-electronics with qubits layer as envisioned in [155], a major concern is that the limited cooling power (thermal budget) at 4 K. Further systematic investigations are required to evaluate the possible impact of temperature increase both on the integrated classical electronics and the qubits performance.

Although the content above reviews the applications of 3D integration technologies in individual quantum computing device, 3D integration is foreseen to be essential in the future hybrid quantum system. By integrating two or more quantum systems, it is believed the strength of different systems can be amplified while the shortages can be avoided [156]. For example, the design to simultaneously leverage the high gate speed of superconducting circuit and the long lifetime of trapped ion has been proposed [157]. However, as mentioned earlier, quantum systems are generally fabricated with different nodes and processes, hindering the

direct combination. This is exactly where proper integration technologies can contribute, in particular at the system and interface level.

2.4 Summary

The scalability issues of quantum computing devices have been discussed for ion trap and other three popular qubit candidates (superconducting circuit, silicon spin and photon) that are compatible with CMOS fabrication process. Specifically, the role of 3D packaging in large-scale integration is highlighted. From the prior studies covered in this chapter, it can be concluded that 3D integration technologies exhibit promising potential in architecture scaling-up and device miniaturization to achieve the future large scale quantum computer.

Chapter 3. WB Traps on Different Substrates

In this chapter, surface electrode ion traps on different substrates are designed, fabricated, and tested. Conventional wire bonding is used as the interconnection. To be differentiated with the TSV integrated traps in Chapter 4, traps in this chapter are denoted as WB (wire bonding) traps. Three different substrates are explored (i.e., high-resistivity silicon, silicon with grounding plane and glass) for the ion trap implementation. For each type of trap, two size variations are included. The fabrication steps are first illustrated with details. Next, electrical characterization including *I-V*, *C-V*, on-chip S-parameter and post-package resonator tests are performed, and the obtained performances are compared and discussed. Following that, ion trapping test setup is introduced. Finally, the ion trapping result based on glass trap is demonstrated.

3.1 Design of WB Traps with Different Dimensions

A typical 5-wire geometry is adopted for the design of WB traps, in which DC, RF, DC, RF and DC electrodes are alternately located on the same horizontal (*x*-*y*) plane [23]. In addition to the core geometry that generates trapping field, extra wire bonding pads and connecting circuits are required. Two size variations of traps are designed, of which the RF electrode width is respectively 40 or 80 μm, as shown in Figure 14 (a) and (b). Note the overall dimension of the traps is basically proportional to the RF electrode width. The gaps between central three electrodes are kept with a constant width of 5 μm, whereas the gap width between peripheral DC electrodes and RF electrodes is 15 μm. The details of the dimensions are given in Table III.

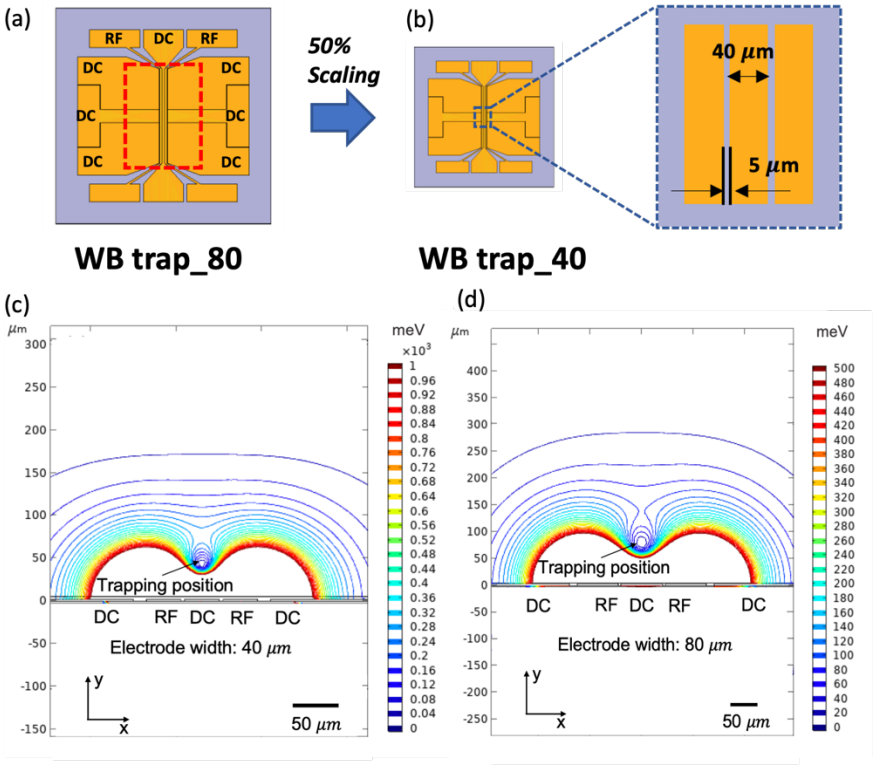


Figure 14. (a) Geometry of WB trap_80. The geometry outside the dotted rectangle is the connecting circuit and wire bonding pad. (b) Geometry of WB trap_40. The RF electrode width and gap width are marked in the inset. (c) and (d) Pseudopotential distribution of WB trap_40 and WB trap_80. Corresponding trapping positions of different traps are marked.

Table III. Design parameters of WB traps with two size variations.

Traps and dimensions	RF electrode width (μm)	RF electrode length (μm)	Gap width (μm)	Wire bonding pad (RF electrode) dimensions (μm²)	Overall dimensions (μm²)
WB Trap_40	40	1460	5	1150 × 400	4000 × 4000
WB Trap_80	80	2920		2300 × 800	8000 × 8000

Finite element modelling (FEM) is carried out to extract the produced electric field of different traps. All the FEM results presented in this thesis are from COMOL Multiphysics (see Appendix). Two '1 : 1' 3D models are built based on the actual dimensions. An air/vacuum entity with extremely small meshing size is introduced above the electrode surface to precisely visualize the field distribution. An RF signal with amplitude of 200 V and frequency of 60 MHz is applied on the two symmetric RF electrodes, whereas the other electrodes are set as ground. By searching the minimum potential point, the theoretical ion trapping positions can be pinpointed (Figure 14(c) and (d)). Likewise, the trapping depth (i.e., pseudopotential difference between saddle point and trap point) of different traps can be determined and compared. As shown in Figure 15, WB trap_80 has a trapping height of 75 μm and trapping depth of 78 meV, as compared to 41 μm and 251 meV of WB trap_40. The trapping heights

obtained from FEM are consistent with the analytical results calculated using Equation (16), which are respectively 40.4 and 75.0 μm for WB trap_40 and WB trap_80. The dimension parameters *a*, *b*, and *c* used in the calculation are shown in Table IV.

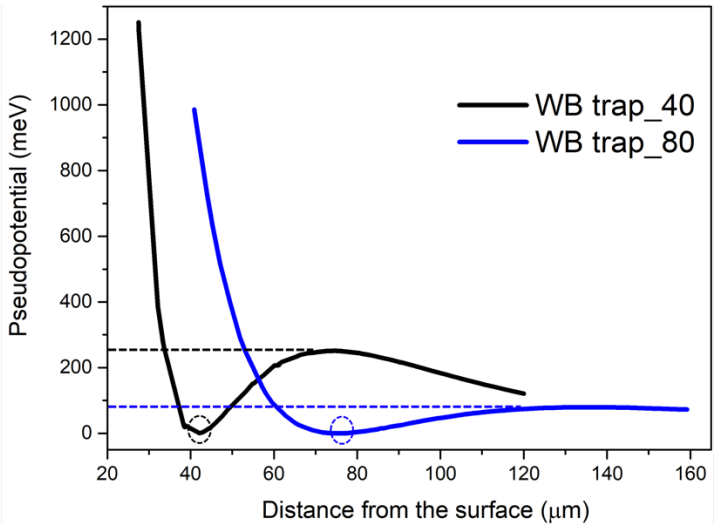


Figure 15. Pseudopotential distribution as a function of distance from the electrode surface. The trapping height and trapping depth are marked respectively.

Table IV. The comparison of calculated and simulated ion trapping height of different-dimension traps.

Traps and dimensions	**Parameter *a* (μm) ***	**Parameter *b* (μm) ***	**Parameter *c* (μm) ***	**Calculated trapping height (μm)**	**Simulated trapping height (μm)**	**Simulated trapping depth (meV)**
WB trap_40	45	50	50	40.4	41.0	251
WB trap_80	85	90	90	75.0	75.0	78

*a, b, c are electrode dimension parameters, as illustrated in Figure 4.

3.2 Fabrication Process of WB Traps

Both silicon and glass are selected as the substrate materials of WB traps. As the dominant building block material of semiconductor industry, silicon is compatible with the most advanced fabrication process. Ion trap on silicon substrate is therefore enabled with high fabrication resolution and design flexibility. However, the intrinsic high RF loss issue seriously limits the large-scale integration of ion trap on silicon. Two possible solutions are proposed to mitigate this issue. The first solution is to use high resistivity silicon (>750 $\Omega \cdot cm$) in place of normal silicon substrate (WB-HR trap). The second solution is to introduce additional

grounding plane to shield lossy silicon from RF signal penetration (WB-GND trap). On the other hand, with the development of glass fabrication technology in modern foundry, glass has become a popular substrate particularly for high frequency devices and back end applications. In this case, ion traps on glass substrate is also explored (WB-Glass trap). The detailed fabrication process of three types of traps are presented below. It should be highlighted that entire fabrication process illustrated in this thesis is performed at Institute of Microelectronics (IME, A*STAR), where standard back end of line CMOS process on 12-inch wafer platform is used.

3.2.1 Fabrication Process of WB-HR Trap

The fabrication process of WB-HR trap is illustrated in Figure 16. The Si substrate used for WB-HR trap has a resistivity that is larger than 750 $\Omega \cdot cm$. First, to insulate the electrical signal from substrate, a 3 μm SiO_2 layer is deposited on Si substrate by plasma enhanced chemical vapor deposition (PECVD). To avoid any stray field induced by the exposed dielectric, the insulation layer is patterned with lithography-defined etching, yielding exactly same geometry as the electrodes. Adhesion layer (0.1 μm Ti) and seed layer (0.1 μm Cu) are deposited in sequence using physical vapor deposition (PVD) onto the surface prior to the second lithography that defines the geometry of surface electrodes. Subsequent electroplating (ECP) of 3 μm Cu and 0.3 μm Au is conducted. Au is used to protect Cu from oxidization. No additional barrier layer is introduced between Cu and Au. First, the widely-used barrier layer Ni is ferromagnetic, making it unsuitable in the application of ion trap. Meanwhile, an X-ray photoelectron spectroscopy (XPS) depth profile is performed to characterize the layers composition of Au/Au-Cu interface/Cu [158]. As shown in Figure 17 (a) and (b), with the etching time (Ar^+ etching) increases, the main component detected is transferred from Au to Cu, which is consistent with the electrode composition. Assuming the etching speed is constant, the thickness of different layers can be extracted. Figure 17 (c) demonstrates that the formed Au-Cu interface is kept far from the Au surface, indicating that 0.3 μm Au is sufficient thick to prevent Cu diffusion onto the surface. After the photoresist strip (PRS), the adhesion and seed layers shall be completely etched, while the time of isotropic wet etching shall be closely controlled since any over etching could result in undesired undercut of electrodes. The front-view and cross sectional SEM images of fabricated WB-HR trap are shown in Figure 18.

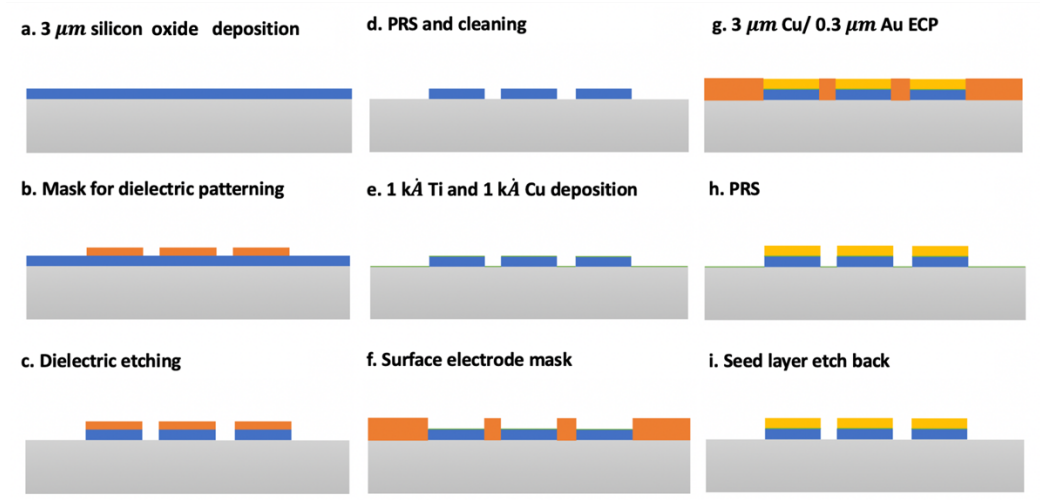


Figure 16. Fabrication process of WB-HR Trap.

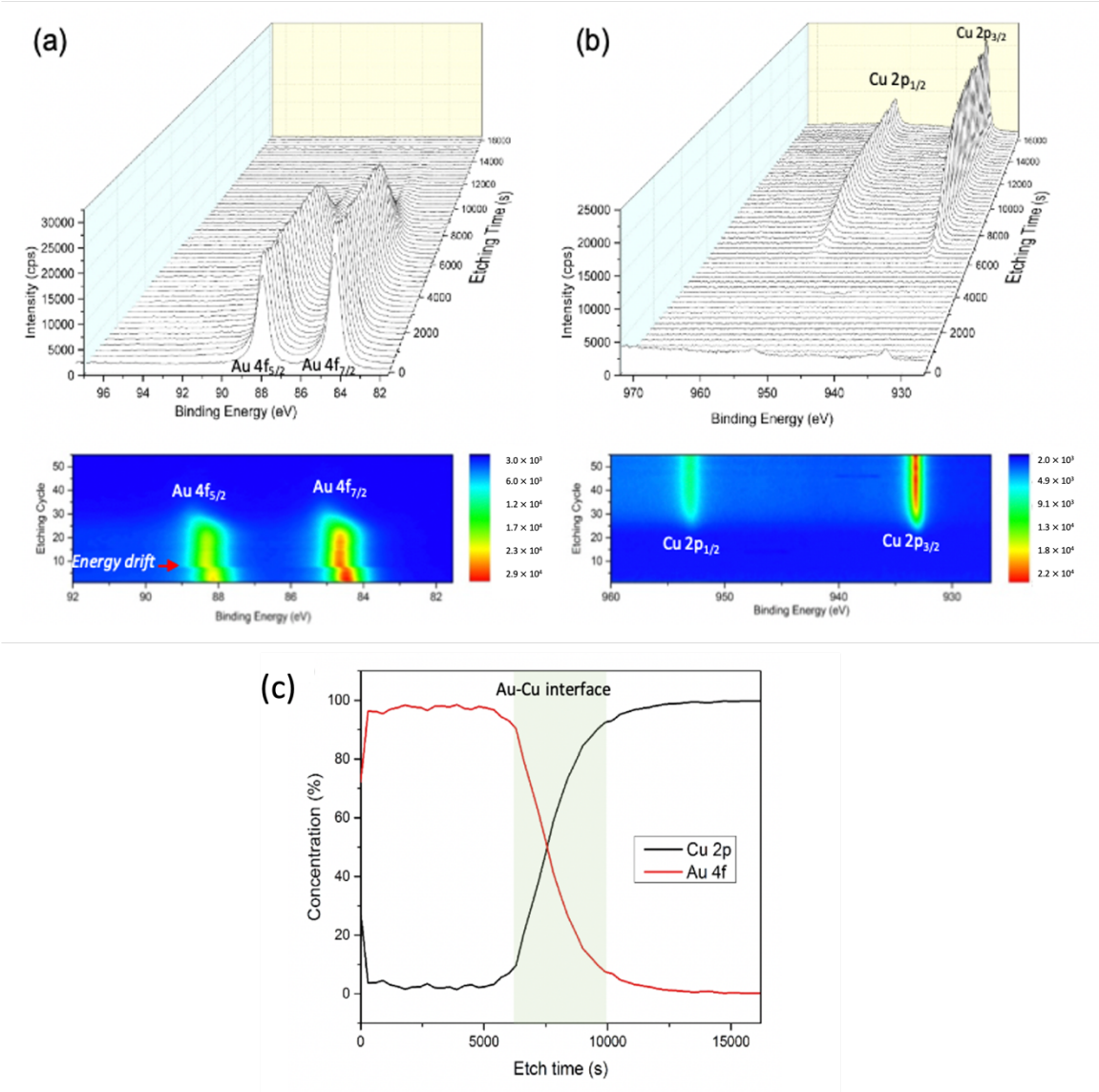


Figure 17. XPS depth profiling of Au/Cu layers for surface electrode. (a) Involution of Au 4*f* doublets in terms of etching time, (b) Involution of Cu 2*p* doublets in terms of etching time and (c) The concentration profiling of Cu 2*p* and Au 4*f* in terms of etching time and the Au-Cu interface with Cu 2*p* and Au 4*f* overlapping area is marked accordingly. Note the etching speed is assumed to be constant throughout the etching process.

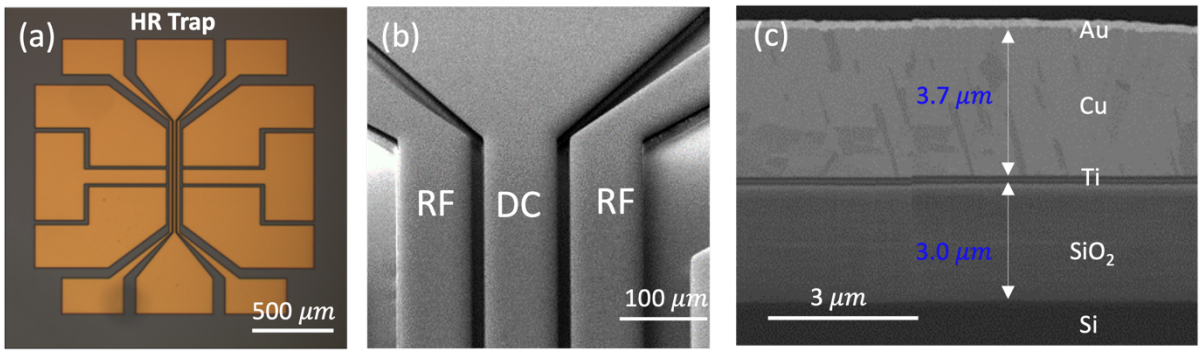


Figure 18. (a) Optical image of fabricated WB-HR trap. (b) Front-view SEM image of WB-HR trap_80. (c) Cross-sectional SEM image showing the layers composition of WB-HR trap.

3.2.2 Fabrication Process of WB-GND Trap

The grounding plane is inserted underneath surface electrodes but on the top of silicon substrate. Cu damascene process is performed in the SiO_2 layer to form the grounding plane (Figure 19). Due to the large coefficient of thermal expansion (CTE) mismatch between Cu (17×10^{-6}/K) and SiO_2 (0.75×10^{-6}/K), the grounding plane is designed with a meshed structure to release the possible thermal stress. The small windows made onto the grounding plane have a dimension of 15×15 μm^2. The lateral separation distance between neighbouring windows is 30 μm in both directions (see inset of Figure 20 (a)).

The fabrication of WB-GND trap also starts from the SiO_2 deposition (2 μm) onto Si substrate. Normal resistivity instead of high resistivity Si is used as the substrate. Following that, SiO_2 is etched by ~1 μm with lithography-defined patterns. ECP of the Cu is performed once Ti and Cu layers are deposited. After annealing in N_2 environment for 30 minutes, a chemical-mechanical polishing (CMP) is used to remove the Cu overburden and planarize the surface. A SiN capping layer of 0.2 μm is deposited onto the grounding plane to protect it from oxidization. The following process is similar to WB-HR trap. Another 3 μm SiO_2 is deposited as insulation layer. Second lithography is performed to define the geometry of SiO_2, while the third lithography is to define the ECP of surface electrodes. Note after the PRS of insulation layer patterning, the exposed SiN capping layer is completely etched. Finally, wet etching of adhesion and seed layers is conducted. The front-view and cross sectional SEM images of fabricated WB-GND trap are shown in Figure 20. Slight undercut into the grounding plane is observed in Figure 20 (c).

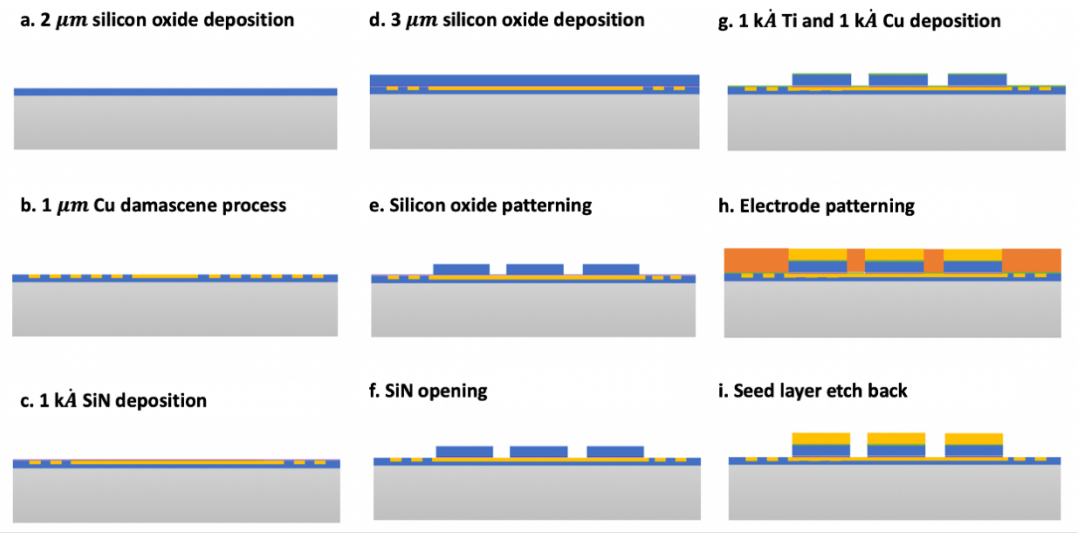


Figure 19. Fabrication process of WB-GND trap.

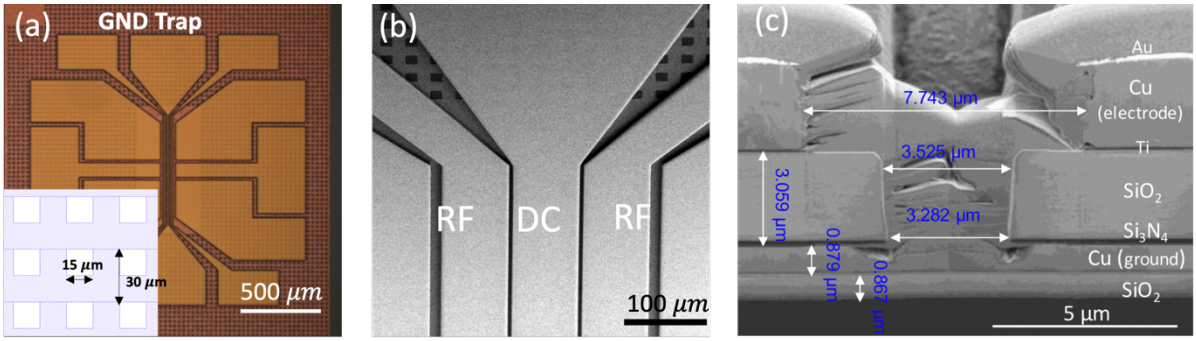


Figure 20. (a) Optical image of fabricated WB-GND trap. The inset shows the dimensions of the meshed structure. (b) Front-view SEM image of WB-GND trap_80. (c) Cross-sectional SEM image showing the layers composition of WB-GND trap. Undercut into the grounding plane can be observed.

3.2.3 Fabrication Process of WB-Glass Trap

The glass wafer used as ion trap substrate is SWG 8.5 from Corning®, which has a resistivity of $4.6 \times 10^{10}\ \Omega \cdot cm$, a loss tangent of 0.025 at 5 GHz and a dielectric constant of 7.2 at 5 GHz. Due to these superior insulation properties, the original insulation layer between electrodes and Si can be eliminated, simplifying the overall fabrication process (Figure 21). The adhesion and seed layers are directly deposited onto glass substrate. Following that, the single step of lithography is performed to define the subsequent ECP of electrodes. To achieve a smaller aspect ratio at the gap region between electrodes and ease the adhesion and seed layers etching process, the thickness of Cu layer is reduced to ~2 µm in WB-Glass trap. The front-view and cross sectional SEM images of fabricated WB-Glass trap are shown in Figure 22.

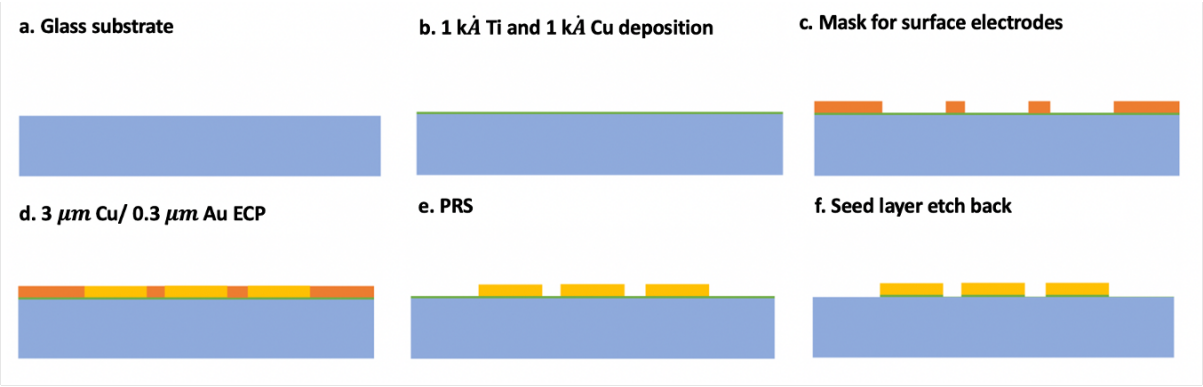


Figure 21. Fabrication process of WB-Glass trap.

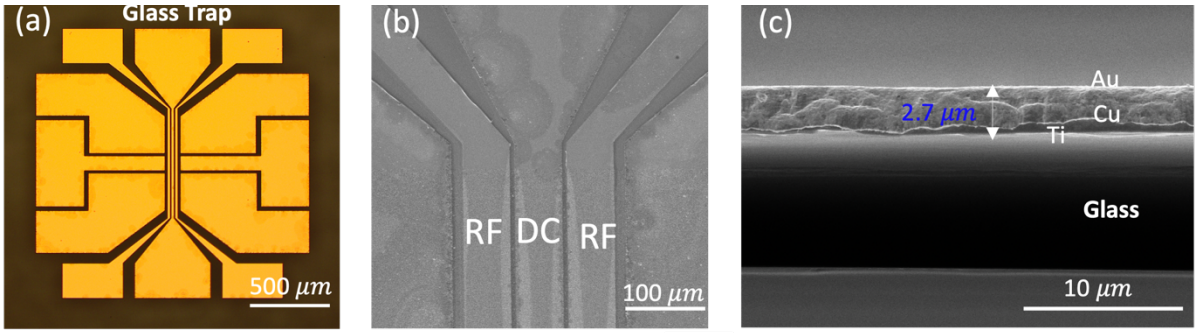


Figure 22. (a) Optical image of fabricated WB-Glass trap. (b) Front-view SEM image of WB-Glass trap_80. (c) Cross-sectional SEM image showing the layers composition of WB-Glass trap. Adhesion and seed layers are deposited onto glass surface directly.

3.3 Electrical Characterization and Performance Comparison of WB Traps

After wafer fabrication and individual dies singulation, various preliminary electrical tests are performed to evaluate the performance of different traps. Suitable candidates will be selected for the final ion trapping operation. Two DC tests are respectively used to characterize the leakage current between neighboring electrodes (*I*-*V* test) and the capacitance of electrodes (*C*-*V* test). At the same time, two RF tests are respectively used to characterize the on-chip loss (S-parameter measurement) and post-packaging loss (resonator test). The experimental setup, results discussion and performance benchmarking of each test are presented in detail in this section.

3.3.1 *I-V* Test

High leakage current (i.e., low resistance) between neighboring electrodes may lead to sparks or even short circuits when a high RF voltage is applied during ion trapping test. To avoid this issue, individual *I-V* test is required once traps fabrication is completed. Due to the large border length of RF electrodes as well as the small gaps (5 μm) in between, RF electrodes generally suffer from higher possibility of leakage issue. Therefore, the *I-V* test mainly focuses on the two RF electrodes and the neighboring central DC electrode.

Cascade Microtech 200 mm shielded probe system and a Keithley 4200-SCS parameter analyzer are used for the *I-V* test. One probe is connected to the central DC electrode, and the other probe is alternately connected to the two RF electrodes, as shown in Figure 23 (a). Traps with different substrates and dimensions are loaded in sequence. Applying a voltage sweep from 1 to 100 V with a 1 V step, the corresponding leakage current can be extracted and compared.

The result in Figure 23 (b) shows that WB_80 has a higher leakage current as compared to WB_40, on all investigated substrates. This is caused by the longer length of WB_80 electrodes, which will increase cross section area and therefore reduce the inter-electrode resistance (note the inter-electrode gap has a constant width of 5 μm). Besides, the metal seed is more difficult to be completely etched in the narrow gaps with longer length of WB 80, aggravating its high leakage issue. The *I-V* curves of WB-GND and WB-HR traps are basically overlapped, indicating that no additional leakage is introduced by the grounding plane. On the other hand, it is found that WB-Glass traps have a two-magnitude higher leakage current in comparison to WB-HR and WB-GND traps, suggesting more residues are left on WB-Glass trap after adhesion and seed layer etching process. Atomic force microscopy (AFM) scanning is carried out on different substrates. The results illustrate that glass substrate surface has a R_{ms} (root mean square roughness) of 8-10 nm, while silicon substrate has a R_{ms} that is smaller than 1 nm. It is thus speculated that the metal seed on WB-Glass traps is hard to be completely etched, and eventually leads to the high leakage current. High leakage current will limit the RF voltage can be applied. Determined by its asymmetric property, surface electrode ion trap normally features a lower trapping depth as compared to the linear Paul trap. The voltage amplitude limitation will worsen the situation, especially for ion transportation and multiple ions confinement.

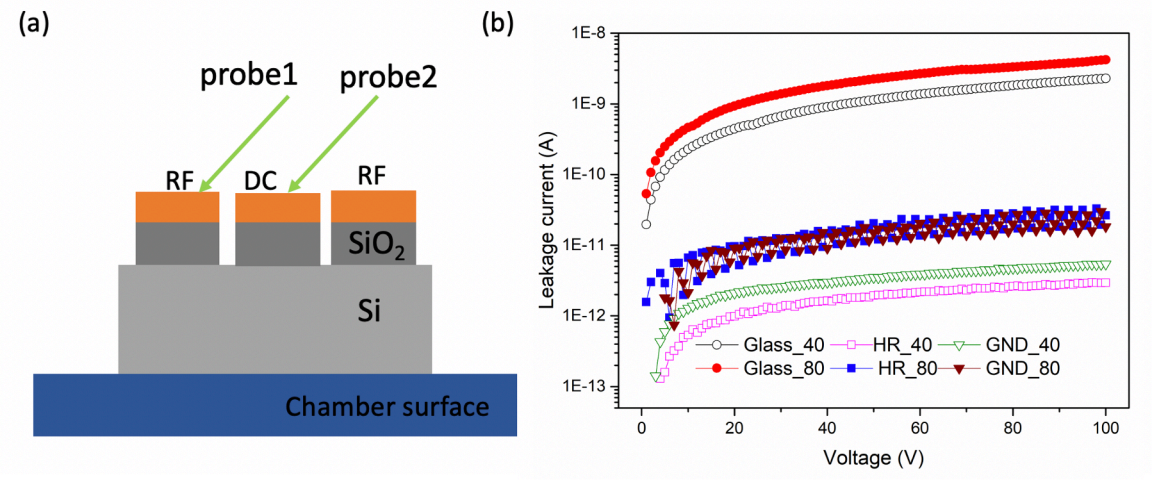


Figure 23. (a) Schematic of leakage current measurement setup. (b) Comparison of leakage current as a function of applied voltage of different traps with size variations.

3.3.2 *C-V* Test

The *C-V* test is also performed using the abovementioned probe system. The metal-oxide-semiconductor (MOS) capacitance of single electrodes (RF electrode) is first measured. A metal pad serving as grounding is inserted underneath the traps, in good contact with the backside of trap substrate (Figure 24 (a)). In this setup, one probe is connected to the RF electrode, while the other probe is connected to the metal pad. A DC voltage sweep from -30 to 30 V with a step of 0.6 V is used. The AC signal has an amplitude of 0.03V and its frequency is set as 100 kHz.

The obtained results are shown in Figure 24 (b). First, WB_80 shows larger capacitance compared to WB_40. This is due to larger surface area A of RF electrodes in WB_80, and capacitance C increases linearly with A ($C = \varepsilon \frac{A}{d}$). Also, it is found that WB-HR trap and WB-GND trap have similar capacitance values. However, the curves of WB-HR traps feature a bending shape, indicating the capacitance changes with the voltage, whereas WB-GND traps have a constant capacitance across the complete voltage range as shown in Figure 24 (c). Indeed, the capacitance from depletion layer in the silicon substrate plays a key role in the total MOS capacitance of WB-HR trap. In the accumulation regime (positive voltage for *n*-type substrate), the measured MOS capacitance is solely determined by the oxide capacitance. In the depletion regime (negative voltage for *n*-type substrate), however, the capacitance of depletion layer come into effect, in series connection with the original oxide capacitance, making the total MOS capacitance smaller (see circuit in Figure 24 (a)). Nevertheless, due to

the incorporation of grounding plane, the effect from silicon substrate is shielded. For WB-GND trap, the measured 'MOS' capacitance can be approximately seen as the pure oxide capacitance between RF electrode and the grounding plane, which cannot change with voltage. Meanwhile, as shown in Figure 24 (b), the curves of WB-GND trap are always slightly lower than the curves of WB-HR trap. This can be attributed to the constant but large capacitance between the grounding plane and silicon, which is also in series connected to the 'MOS' capacitance. Similarly, the capacitance of WB-glass trap is also constant. Due to the large thickness of glass substrate (~700 μm), the obtained capacitance of glass trap is two-magnitude smaller than the silicon counterparts.

In addition to the MOS capacitance of individual RF electrodes, the capacitance between RF and central electrodes is also measured (two-electrode capacitance). The setup is similar to the *I-V* test, where two probes are correspondingly connected to two parallel electrodes. Same conditions as the MOS capacitance measurement are used for the input electrical signal. The relation between two-electrode capacitance and MOS capacitance of single electrodes is illustrated in Figure 25 (a). A similar capacitance distribution pattern among different traps (WB-HR trap ≈ WB-GND trap ≫ WB-Glass trap) is observed in Figure 25 (b). Meanwhile, a ~50 % capacitance reduction is found, as compared to the MOS capacitance of same trap. This is because the measured capacitance between two electrodes is roughly equal to the total capacitance of two MOS capacitances that are connected in series (ignoring the capacitance of Si substrate, Figure 25 (a)).

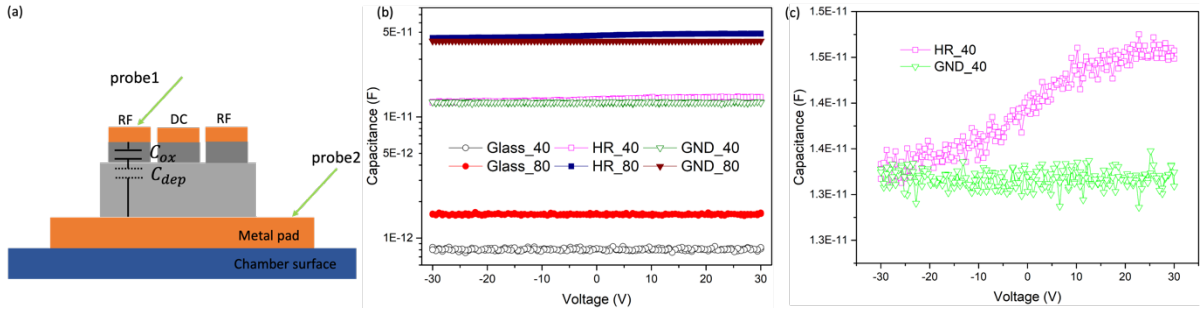


Figure 24. (a) Schematic of the MOS capacitance measurement setup. The capacitance circuit is also shown. (b) Comparison of MOS capacitance of different traps with size variations. (c) The curves of capacitance as a function of voltage from WB-HR trap_40 and WB-GND trap_40. Curve from WB-HR trap_40 has a bending shape.

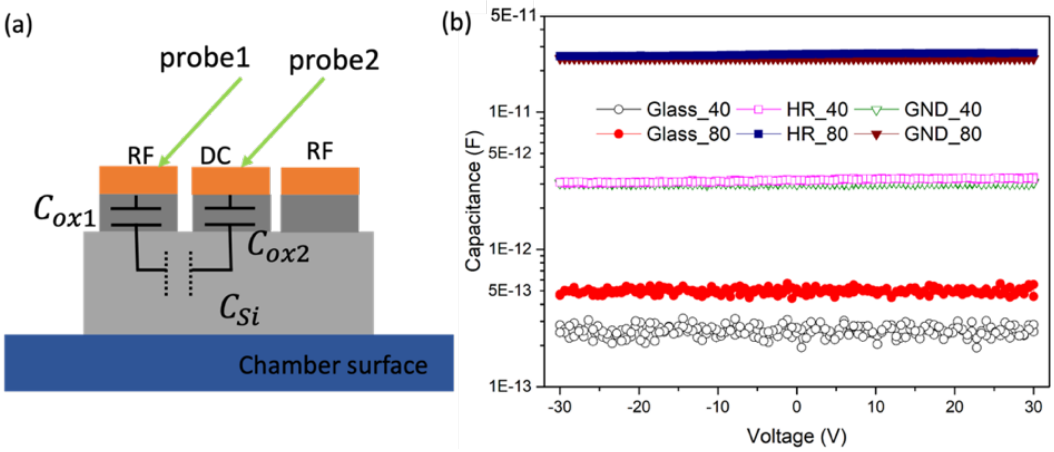


Figure 25. (a) Setup schematic of the measurement on capacitance between two electrodes. The corresponding capacitance circuit is also shown. (b) Comparison of capacitance between two electrodes of different traps with size variations.

3.3.3 S-parameter Measurement

The S-parameter measurement is conducted using Cascade Elite probe station and Agilent PNA network analyzer, to evaluate the on-chip RF performance of various ion traps. Since the operation frequency for surface electrode ion trap is normally in the range of several tens of megahertz, a frequency sweep from 10 to 110 MHz (step size of 1 MHz) is employed to completely cover the range. By probing the two ends of central RF-DC-RF electrodes (3-pin probe, with a pitch of 100 μm), a two-port circuit network is thus built.

The obtained insertion loss (S21) and reflection loss (S11) of different traps are shown in Figure 26. In general, for traps on same substrate, the one with smaller dimensions (WB_40) feature less loss. Intuitively, this can be due to the shorter signal transmission distance. The abovementioned smaller capacitance of WB_40 trap also benefits the power loss reduction. In addition, owing to the shielding effect of grounding plane, WB-GND trap has lower insertion loss and reflection loss as compared to those of WB-HR trap. Meanwhile, the smooth curve of WB-GND trap reflects the favorable stability of its circuit components across the entire frequency range. However, the overall performance of traps on silicon substrates is still inferior to that of WB-Glass trap. For both WB-Glass trap_40 and 80, the insertion losses at 50 MHz are smaller than 0.05 dB.

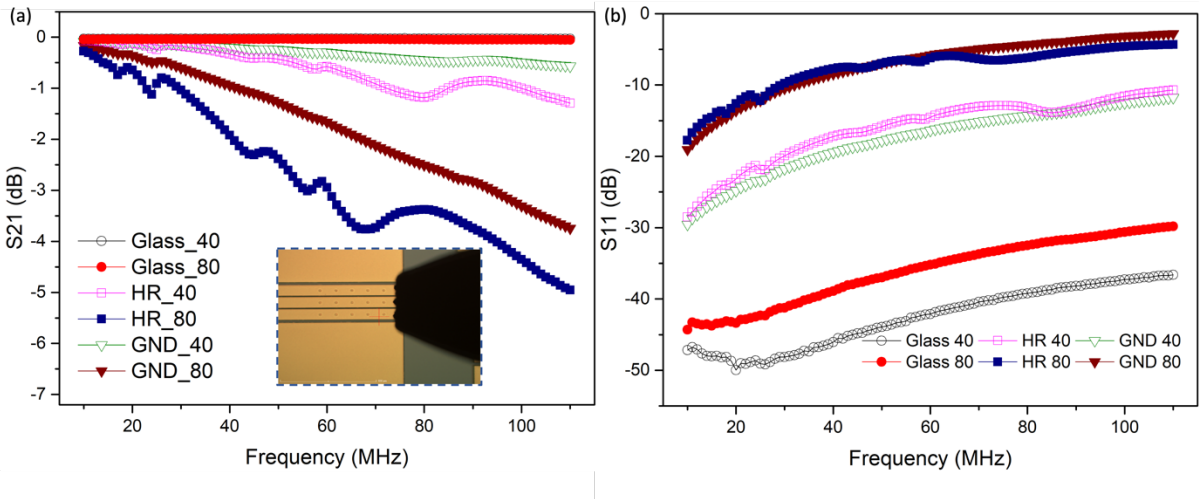


Figure 26. (a) Insertion loss (S21) and (b) reflection loss (S11) comparison of different traps with size variations. An inset showing the 3-pin probe in connection with the central three electrodes is included in (a).

3.3.4 Resonator Test

To facilitate flexible electrical signal feedthrough in the vacuum chamber, ion trap is required to be packaged into a 121-pin ceramic pin grid array (CPGA, Kyocera). A glass spacer of ~0.5 mm thick is used to raise the height of the trap above the CPGA surface for laser access. Ultra-high vacuum (UHV) compatible die attach paste (EPO-TEK 353ND) is used for the packaging process. The connections between surface electrodes and corresponding CPGA pins are built with bonding wires. For DC electrodes, additional single layer ceramic capacitors (~820 pF) shall be introduced in between to filter the possible RF pickup noise. The image of the packaged trap is shown in Figure 27 (a). To evaluate the post-packaging RF performance of ion trap, a resonator test is carried out.

In ion trapping test, the packaged ion trap is connected with an external resonant transformer to step up the input voltage to the required voltage for ion trapping (amplitude of ~100 V). This transformer together with the package ion trap can be schematized as a series resistor-inductor-capacitor (RLC) circuit, resonating at certain frequency determined by the RLC components. The capacitance component in this circuit largely comes from the ion trap. Appling a liner frequency sweep from 1 to 100 MHz with a step size of 1 MHz, the corresponding resonance curves of various traps can be generated (input power of -10 dBm). A reference curve from the transformer connected with a standard 3.3 pF capacitor (wire bonded into CPGA) is also included for comparison (Figure 27 (b)).

Due to the incorporation of grounding plane, the power peaks are improved by ~10 dBm in each size variation for WB-GND traps, with respect to the WB-HR traps (Figure 27 (b)). However, the performance is still not comparable with traps on glass substrates. The curves of WB-Glass traps almost overlap with the reference curve, suggesting its superior capacitor-like behavior. The higher resonance peaks indicate less power is dissipated through the circuit. Besides, smaller full width at half maximum (FWHM) can be observed for the WB-Glass traps. As a result, the corresponding quality (Q) factors of WB-glass traps are higher. The resonance frequency f distribution of various traps also agrees well with their corresponding capacitance C, since f is proportional to $C^{-\frac{1}{2}}$ ($f = \frac{1}{2\pi\sqrt{LC}}$). Similarly, as WB-HR and WB-GND traps have similar capacitance in each size variation, no significant deviation is found in their resonance frequencies.

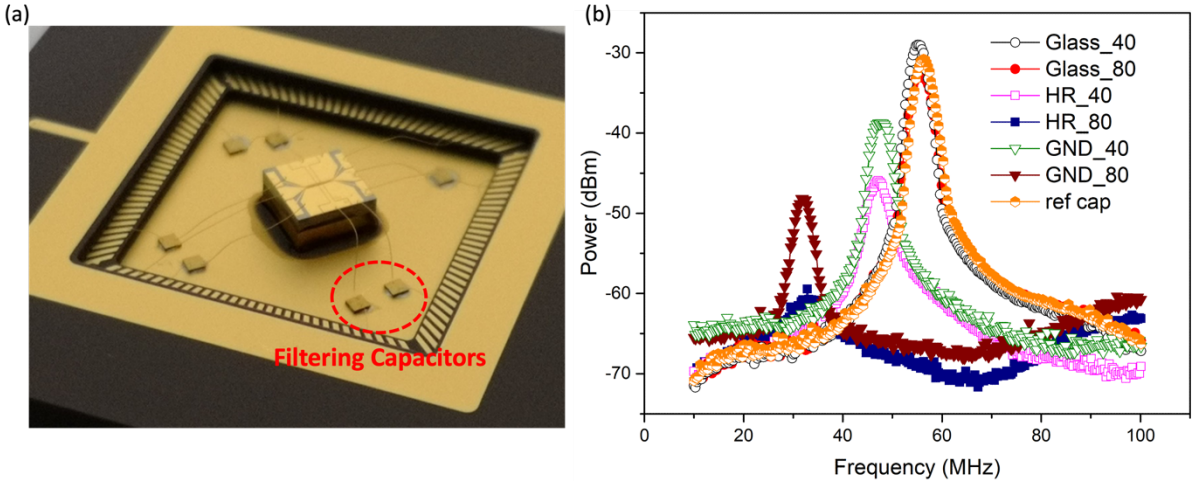


Figure 27.(a) Ion trap (WB-HR trap_40) packaged in a CPGA. The filtering capacitors for DC electrodes are marked. (b) Resonance curves comparison of different traps with size variations.

3.4 Ion Trapping Test on WB-Glass Trap

Due to the superior RF performance, ion trapping test is first carried out on the WB-Glass trap_80. The functionality is tested by loading the laser-cooled $^{88}Sr^{+}$ ions.

3.4.1 Ion Trapping Setup

The images in Figure 28 show parts of the ion trapping setup including laser system and vacuum chamber. The packaged trap is inserted in a stainless-steel ultra-high vacuum (UHV)

cylindrical chamber (K.J. Lesker). A CF63 viewport of the chamber is dedicated to photon detection, three CF40 viewports to laser input and output and a CF16 viewport for lateral imaging purposes. The other CF63 flange available is used for pumping, a CF40 for electrical feedthrough (both RF and DC voltages) and two CF16 flanges are used for a Sr oven and a cold cathode vacuum gauge (Pfeiffer IKR 270) respectively. During trap operation the chamber is pumped by an ion pump (IP) and a Titanium sublimator pump (TSP). The WB-Glass trap is baked during a week at 130 °C while pumping with a Turbo pump (Pfeiffer TC600). After the baking and the switching to IP+TSP pumping the residual pressure is in the 5×10^{-11} mbar range. This demonstrates the perfect UHV compatibility of the materials used for fabrication and packaging. Adjustable DC voltages are generated by a computer-controlled DAC card (Measurement Computing PCI-DAC6703), filtered by low-pass passive inductor-capacitor-resistor filters and then steered to CPGA via a Sub-D 9 feedthrough and shielded Kapton-insulated wires (Allectra 311-KAPM-060). RF voltage (frequency of 32.7 MHz) is supplied by a Rigol DG4162 generator, amplified in a 10 W, 50 Ohms amplifier (DeltaRF LA0005-10) and then adapted to the high impedance of the trap by a toroidal resonant transformer (step-up of 9). The resonator is directly plugged to two BNC feedthrough that are connected to the CPGA via 20 cm long Kapton-insulated coaxial cables (Allectra 311-KAP50). With this setup the maximum RF voltage amplitude at the trap is around 250 V.

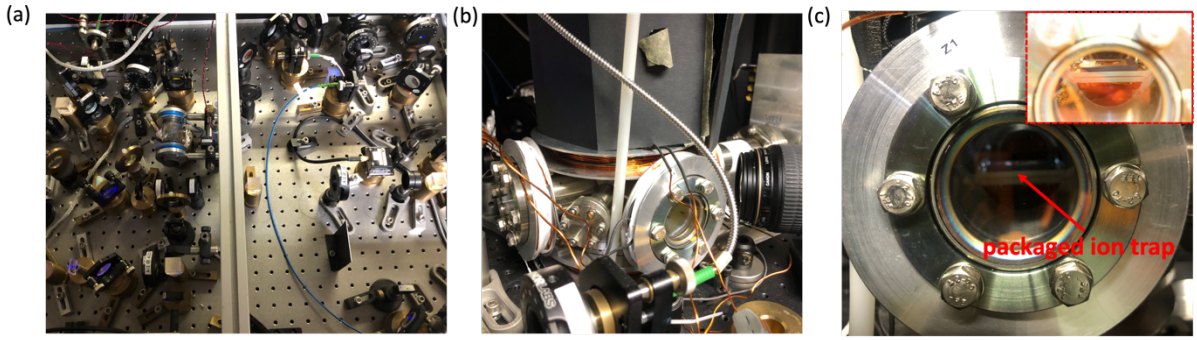


Figure 28. Ion trapping setup. (a) Part of lasers and optics system on the vibration isolation table used for ion trapping. (b) The stainless-steel ultra-high vacuum cylindrical chamber. (c) Ion trap (WB-Glass trap_80) in the vacuum chamber viewed from a CF40 viewport. A zoom-in image is attached on the top right corner.

An atomic beam of neutral Sr is generated by sublimation of a small Sr dendrite (Aldrich) inserted in an helicoidal tungsten filament. To create Sr^+ ions the atoms are photo-ionized using a two-color CW technique (Figure 29 (a)) [159, 160]. For this purpose, a 650 THz (461 nm) commercial extended cavity laser (Toptica DL Pro) is used to address the $5s^2\ ^1S_0 \rightarrow 5s5p\ ^1P_1$ transition and a free running 740 THz (405 nm) diode laser is used to address the $5s5p\ ^1P_1 \rightarrow$

($4d^2+5p^2$) $^1D_2$ transition that ends up in an auto-ionizing state. Both lasers are coupled in the same single mode optical fiber and then focused in the center of the trap (with a beam waist of approximately 40 μm). The power at the ion position is around 1 mW for the 650 THz and 80 μW for the 740 THz beam, respectively. In typical experimental conditions the loading-time for an ion is roughly 10 seconds. The precise frequency of the 650 THz laser is tuned with a lambda-meter (Coherent WaveMaster) to maximize the fluorescence of a neutral Sr beam. No active frequency stabilization is needed during several hours.

The energy level diagram of $^{88}Sr^+$ ion is shown in Figure 29 (b). The $^{88}Sr^+$ ions are Doppler-cooled addressing the $5^2S_{1/2} \rightarrow 5^2P_{1/2}$ transition (711 THz, 422 nm) with a laser beam (Toptica DL-100 laser diode). To avoid optical pumping into the metastable $4^2D_{3/2}$ state, two additional lasers ("repumpers") are used addressing the 299~THz $4^2D_{3/2} \rightarrow 5^2P_{3/2}$ transition (1003 nm, Toptica DL pro laser diode) and the 290 THz $4^2D_{5/2} \rightarrow 5^2P_{3/2}$ transition (1033 nm NKT Koheras Adjustik fiber laser). With this scheme [161], it is possible to eliminate coherent population trapping issues that may affect Doppler cooling using the repumping scheme based on the driving of the 275 THz $4^2D_{3/2} \rightarrow 5^2P_{1/2}$ transition [162]. Nevertheless, a 275 THz "readout" laser (1092 nm NKT Koheras Adjustik fiber laser) is used in order to measure the collection efficiency of the detection system. Frequency stabilization of the 711 THz cooling beam is obtained by a saturated absorption technique in a Rb cell, taking advantage of the near coincidence of the $5^2S_{1/2} \rightarrow 5^2P_{1/2}$ transition in $^{88}Sr^+$ with the $5^2S_{1/2} \rightarrow 6^2P_{1/2}$ transition of neutral ^{85}Rb [163]. Infrared lasers are stabilized with a transfer lock scheme [164]. The frequency gap is filled-up and fine tuning of the cooling beam frequency is obtained using a double-pass acousto-optic modulator (AOM). The beam is coupled in a single mode optical fiber and then focused (beam waist on the order of 30 μm) at the ion position with typical power in the 2 - 50 μW range. The AOM is also used to implement a closed loop stabilization of the beam intensity by measuring a portion of the beam transmitted by the fiber on a photodiode and feeding back the signal to the AOM RF source in AM mode. Repumper lasers are both coupled in a single mode, made collinear with the cooling beam and focused at the ion position (waist on the order of 60 μm) with a typical power of 1 mW per beam.

711 THz (422 nm) photons scattered by the ion are collected by a home-made objective with numerical aperture of 0.4, spatially filtered in a 150 μm diameter pinhole, spectrally filtered by an interference filter (Semrock FF01-420/10) and detected by a photomultiplier in photon-counting mode (Hamamatsu H7828). The overall collection efficiency is on the order of 10^{-3}. Alternatively, during the alignment process, it is possible to acquire images of the

trapped and cooled ions (no spatial filtering) with an electron-multiplier CCD camera (Andor Luca).

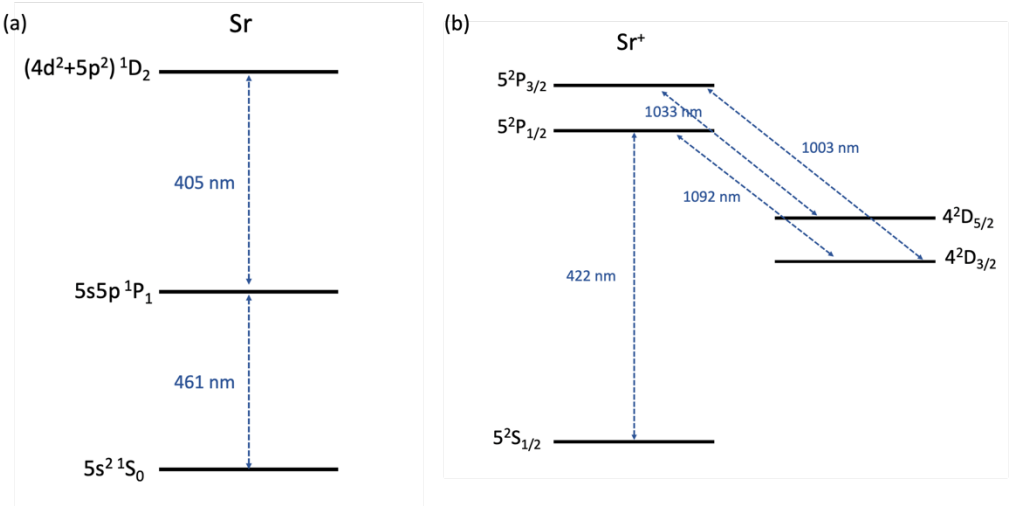


Figure 29. (a) Energy level diagram showing the two-step ionization pathway for neutral Sr. (b) Energy level diagram of the cooling, repumping and readout transitions for Sr^+ ion.

3.4.2 Ion Trapping Results on WB-Glass trap

Using the abovementioned setup, the ion trapping operation is performed on the WB-Glass trap_80. Stable trapping of ions for ~30 minutes with Doppler cooling is observed. Up to four ions are successfully confined. Figure 30 shows a typical spatially resolved florescence of two ions, where the inter-ion distance is measured to be 9.5 ± 0.5 μm.

The motional frequencies in the trap are measured using a "tickle" technique coupled to a sequential fluorescence acquisition [165]. In brief an acquisition sequence is made of thousands of cycles in which first Doppler cooling is applied during roughly 1 ms, then a short (typically 10 μs) pulse of sinusoidal excitation at frequency *f* is applied to a DC electrode, then the scattered fluorescence photons are acquired during 100 μs. During the excitation phase, the motional energy of the initially cold ion may increase in a resonant way such that the fluorescence signal acquired in the detection window is affected by Doppler shift. By scanning the frequency *f*, the motional frequencies of a single ion in the trap as a function of trapping parameters (i.e., RF amplitude and DC voltages) are measured with a precision up to 1 kHz.

In Figure 31 (a), the average radial frequency of trapped ion as a function of RF amplitude is plotted (with constant DC voltages). The theoretical average radial frequency calculated using an analytical model is also plotted together [28]. The discrepancies between

measurement and theoretical values may come from the approximations (e.g., absence of electrode gaps) used in the analytical model. At the same time, a finite element modelling is used to extract the motional frequencies (see Appendix). In brief, the ion motion tracing with the designed trap geometry is firstly obtained. With Fourier transformation of ion position with time, the radial frequencies are then extracted, which is given as red circles in the plot. An overall more favorable agreement is found between the measured and simulated frequencies. In addition, the measured axial frequency is plotted as a function of the nominal axial frequency (Figure 31 (b)). Similarly, a shift of roughly 100 kHz exists between measurement and analytical calculation, while the result from modelling shows a better agreement.

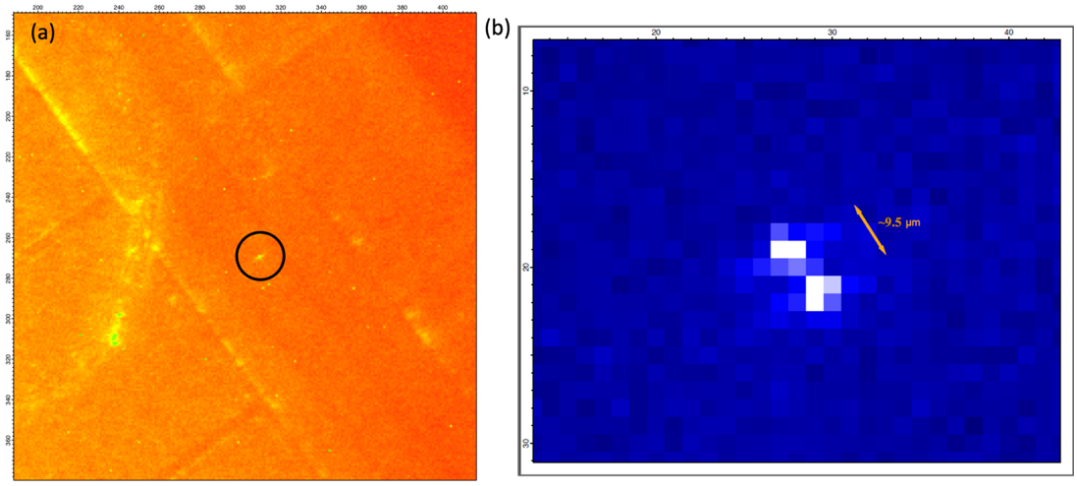


Figure 30. (a) Image of trapped ions on the WB-Glass trap_80. (b) Fluorescence images of two trapped ions (the inter-ion distance is ~9.5 μm). The image is acquired with an electron-multiplier CCD camera with background subtracted.

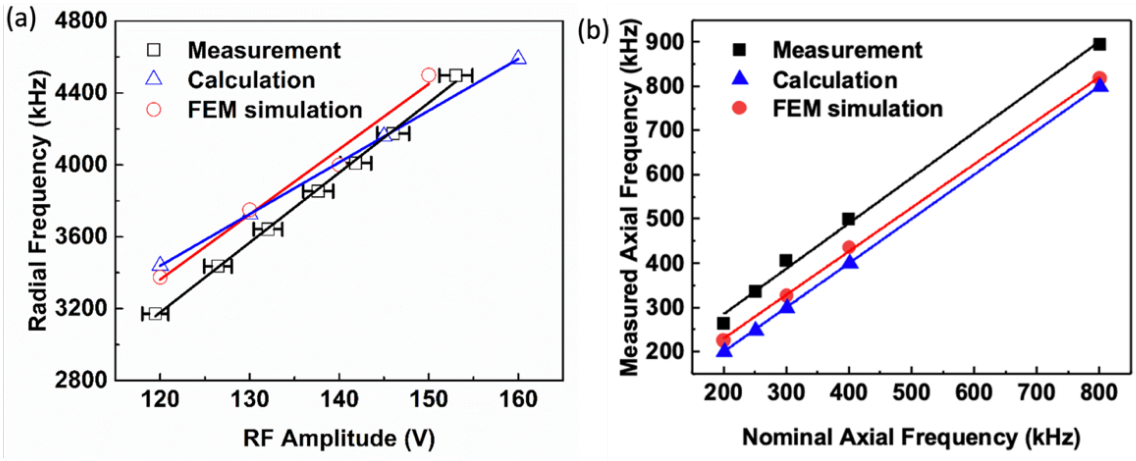


Figure 31. (a) Measured and simulated radial motion frequency as a function of RF amplitude. (b) Measured and simulated axial motion frequency as a function of the nominal axial frequency.

3.5 Summary

In this chapter, ion traps are designed with two size variations based on the different RF electrode widths. High resistivity silicon, silicon with grounding plane and glass are respectively used as the ion trap substrates. The corresponding fabrication process is presented in detail. The electrical performance is compared among various traps, in terms of leakage current between electrodes, parasitic capacitance (MOS capacitance as well as capacitance between electrodes), on-chip insertion loss (S21) and post-packaging power loss.

Table V gives an executive summary of the performance comparison of various planar traps. It is found that WB-Glass trap features smaller capacitance (<1 pF for two-electrode capacitance), lower RF power loss (insertion loss <0.05 dB at RF frequency of 50 MHz) and higher resonance peak (about -30 dBm), as compared to the counterparts on silicon substrates. Concerning the effect from the dimensions of traps, smaller traps (WB_40) generally have better performance in multiple electrical metrics. However, WB_80 trap has a higher trapping height (75 μm), which is more friendly to the laser focusing. Therefore, ion trapping test is first performed on the WB-Glass trap_80. Up to four ions are simultaneously confined. The obtained lifetime of single ions with laser cooling is ~30 minutes. An overall good (albeit not perfect) agreement exists between measured, calculated and simulated frequencies (both radial and axial frequencies).

Table V. Summary of electrical performance comparison of traps on different substrates with size variations.

	WB-HR trap		**WB-GND trap**		**WB-Glass trap**	
	WB_40	**WB_80**	**WB_40**	**WB_80**	**WB_40**	**WB_80**
Leakage current @ 100 V (A)	3.0E-12	2.6E-11	5.4E-12	1.8E-11	2.3E-9	4.2E-9
MOS capacitance @ 0 V (F)	1.4E-11	4.7E-11	1.3E-11	4.2E-11	8.2E-13	1.6E-12
Capacitance between two electrodes @ 0 V (F)	3.2E-12	2.6E-11	3.0E-12	2.4E-11	2.7E-13	5.2E-13
On-chip insertion loss @ 50 MHz (dB)	-0.43	-2.38	-0.24	-1.28	-0.02	-0.04
Resonance peak power (dBm), resonance frequency (MHz)	-45.9, 47.2	-60.8, 33.3	-38.7, 47.6	-48.3, 31.9	-29.0, 55.2	-32.9, 55.4

Chapter 4. TSV Integrated Surface Electrode Ion Trap

To simultaneously leverage the established fabrication technique of silicon and superior insulation property of glass, a novel ion trap is demonstrated in this chapter, where silicon and glass respectively used as ion trap and interposer substrate are heterogenous integrated. The vertical connection between the silicon ion trap and the glass interposer is achieved by TSV, instead of conventional wire bonding.

First, the geometry development (from WB trap to TSV integrated trap) and the fabrication process of this TSV integrated ion trap are presented. A 10 times form factor reduction is achieved due to the incorporation of TSV. Next, the electrical characteristics (namely leakage current, MOS capacitance, capacitance between two electrodes, on chip RF loss and post packaging RF loss) of TSV integrated ion trap are tested and evaluated. In each test, the results on TSV integrated trap are compared, with regard to those from WB-HR trap and WB-GND trap (Chapter 3) which also use silicon as the substrate. An analytical model is built to calculate the capacitance of various traps. A good albeit not perfect consistency is found between the model and the measurement result. Meanwhile, the obtained S-parameter and resonance curves from simulation are also compared with those from experiment. Furthermore, a quantitative analysis in terms of power loss of different traps is performed. Based on the promising electrical testing results, ion trapping test on the TSV integrated trap is performed. The measured heating rate is benchmarked with state of the art. Additionally, the thermal management of TSV integrated trap is discussed. Possible solutions to the undesired temperature increase issue are proposed from the perspectives of heat generation and heat dissipation enhancement, respectively. The solutions are further evaluated using finite element modelling. Finally, the idea of the direct bonding of trap onto customized CPGA with patterned RDL (i.e., in the absence of glass interposer) is presented and examined.

In this chapter, TSV integrated ion trap is denoted as TSV trap, which consists of bonded TSV integrated silicon die (TSV die) and glass interposer.

4.1 Design of TSV Integrated Ion Trap

The design of TSV trap starts from the geometry of WB trap (WB trap_80) in Chapter 3. As shown in Figure 32 (a), TSV die geometry only preserves the core region that generates trapping field, eliminating the wire bonding pads and the connecting circuits present in the WB trap. The original wire bonding pads are transferred to the interposer underneath, drastically reducing the surface of the electrodes. The overall dimension is reduced from 8000 × 8000 μm^2 of WB trap to 2000 × 3000 μm^2 of TSV die. Meanwhile, the obtained high optical access of TSV trap make it possible to keep a regular shape, instead of the 'bow tie' shape that is used in traps from Sandia National Laboratories [55] and Honeywell [10]. This simplifies the fabrication process and enables TSV trap high scalability. TSVs are designed with a diameter of 20 μm and a depth of 100 μm. The pitch between TSVs is 100 μm. Since standard Cu-filled TSV is used, all the electrodes (including RF) are connected with TSV. 10 TSVs are accommodated under RF electrodes (5 on each side), while 6 or 10 TSVs are accommodated under DC electrodes, depending on the electrode size. Micro bumps with a diameter of ~25 μm are located underneath every single TSV to allow for connection and assembling with the interposer. The interposer is designed with a redistribution layer (RDL), acting as a bridge between the CPGA and the TSV trap for electrical connection. The tested RDL geometry is a sort of extension of trap electrodes. Obviously, more complex routing can be implemented where necessary. As mentioned earlier, glass instead of silicon is used as the interposer substrate, due to its superior dielectric property.

To evaluate the possible effect from the wire bonding pad elimination to the ion trapping performance, a similar finite element modelling is conducted based on the geometry of TSV die. The obtained results are compared with that from WB trap. The overlapping curves in Figure 32 (b) indicate that the changes in terms of trapping height (~75 μm) and trapping depth (~78 meV with RF amplitude of 200V and frequency of 60 MHz) are negligible before and after the bonding pads elimination.

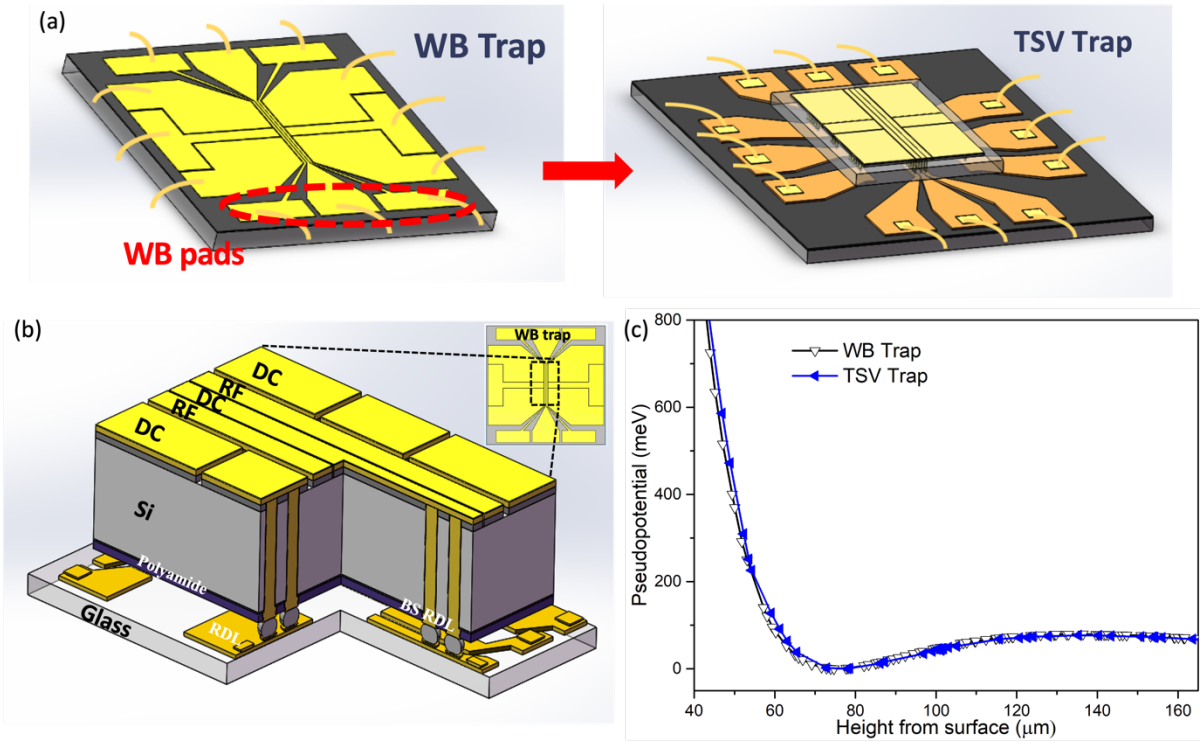


Figure 32. (a) Geometry development from WB trap to TSV trap. Only the core surface geometry of WB trap is maintained in TSV trap, whereas the wire bonding pads and connection circuits are transferred to the interposer underneath. (b) 3D schematic of TSV trap. (c) Pseudopotential distributions as a function of distance from the electrode surface for WB trap and TSV trap. The overlapping curves indicate that the elimination of wire bonding pads on the surface electrode has negligible effect to the trapping electric field distribution.

4.2 Fabrication Process of TSV Integrated Ion Trap

TSV trap fabrication mainly consists of three parts: the fabrication of TSV die on Si wafer, the fabrication of interposer on glass wafer, and the alignment and bonding of TSV die and interposer after wafer singulation. Similar with the fabrication process of WB trap, all the fabrications of TSV trap are performed on the 12-inch wafer processing platform.

4.2.1 Fabrication of TSV Die

In the fabrication of TSV die on Si substrate, a via-first approach is adopted, in which TSV is etched and filled before surface electrode patterning. First, a 2.4 μm SiO_2 layer is deposited onto Si wafer (normal resistivity) by PECVD as insulation layer (Figure 33 (a)). A photoresist with thickness of ~7 μm is used to define the 20 μm diameter via etching. To form 100 μm deep blind via in Si substrate (2.4 μm SiO_2 is first etched), ~400 cycles of Bosch etching process is required (Figure 33 (b)). Next, a 0.75 μm SiO_2 is deposited onto via sidewall as TSV liner to insulate the TSV core (Cu) from Si substrate. Before the ECP of TSV core, barrier (0.2 μm

Ta) and seed (0.8 µm Cu) layer are deposited by PVD. To accurately characterize the TSV dimensions especially in the vertical direction, cross-sectional SEM is used. As shown in Figure 34, a good diameter consistency is observed at via top, middle and bottom. The TSV liner is conformally deposited onto the via sidewall. After the ECP of TSV core, to completely release the stress due to the CTE mismatch between TSV core and Si substrate, wafer annealing of 30 minutes at 250 ℃ in N_2 environment is required. The CMP after annealing is adopted to remove the Cu overburden as well as the barrier and seed layers (Figure 33 (c)). An additional SiN layer (~0.1 µm) is deposited to protect the exposed Cu from oxidization. Subsequently, the ~3 µm (2.4 + 0.75 µm) SiO_2 insulation layer is patterned with the similar process as WB trap (Figure 33 (d)), where lithography defined etching is performed. After the PRS of SiO_2 etching, the SiN layer is completely etched away. Barrier (Ti) and seed (Cu) layers are then deposited before the ECP process of 3 µm Cu and 0.3 µm Au as surface electrodes. After the etching of barrier and seed layer, the wafer frontside is temporarily bonded with a handling wafer and the fabrication of wafer back side starts.

To maintain the bonded wafer thickness <800 µm, after the temporary bonding, the device wafer is grinded to a thickness of ~110 µm, whereas the handling wafer is grinded by ~100 µm. The thickness of interlayer (bonding glue) is ~50 µm.

The device wafer is first etched by ~10 µm to reveal the TSV (TSV liner). Note some over etching is required so that the subsequent SiO_2 deposition can cover the TSV sidewall. Once the 3 µm SiO_2 layer is deposited for back side insulation, both CMP and etching are required, to reveal the TSV (Cu) from this insulation layer once again (Figure 33 (e)). Afterwards, the first lithography on the wafer backside is performed to define the patterning of RDL (3 µm Cu). After the ECP of backside RDL, a polyimide layer (5 µm HD8930) is coated to protect the RDL from oxidization (Figure 33 (f, g)). Note lithography-defined openings are made on this polyimide layer, where micro bumps would be placed. Additional curing process (200 ℃, 30 minutes) is required to enable the polyimide with high stiffness and mechanical stability. Since the micro bump has a diameter of 25 µm (10 µm Cu and 15 µm SnAg), a thick photoresist (~30 µm) is required in the last lithography. After ECP and reflow of the micro bump, the device wafer is separated from the handling wafer (Figure 33 (h)). During the de-bonding process, some cracks on the chips at the wafer edge are observed. As a result, the achieved yield of the device wafer is ~80 %. However, with appropriate process optimization, this cracking issue can be solved in the future fabrication.

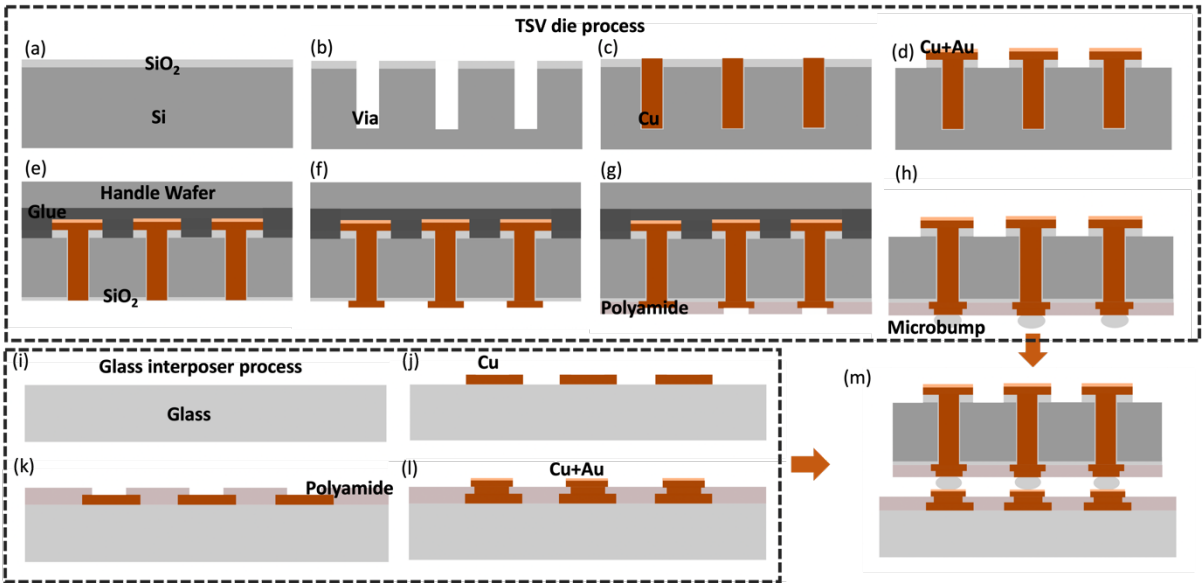


Figure 33. Fabrication process of TSV trap. (a-h) Fabrication process of TSV die. (i-l) Fabrication process of glass interposer. (m) Bonding of TSV die and glass interposer to form the final TSV trap.

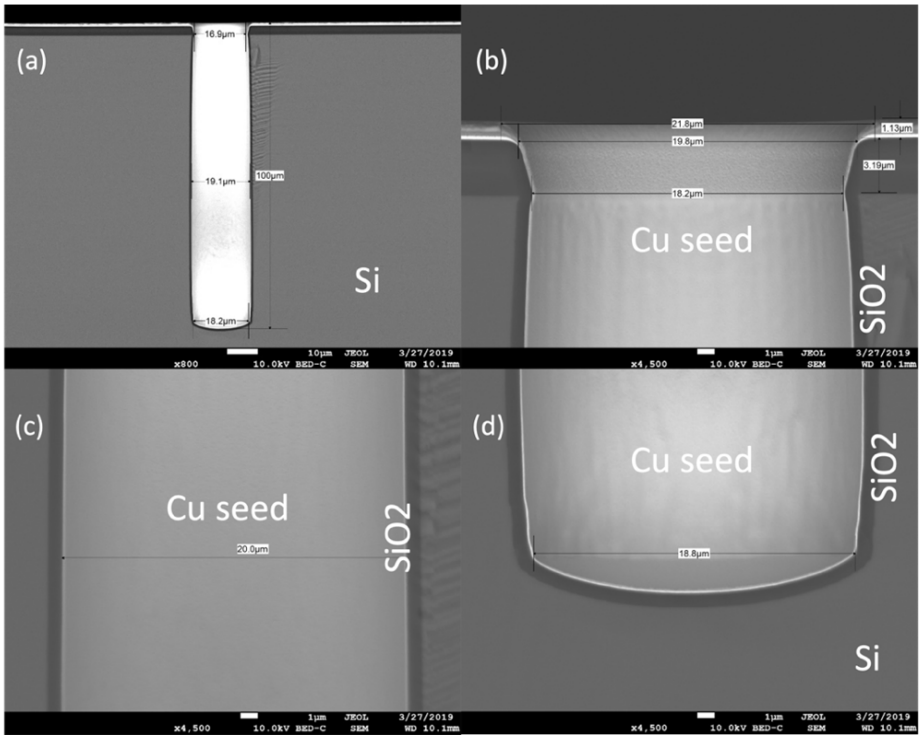


Figure 34. (a)The cross-sectional SEM image showing the etched blind via into Si substrate. (b), (c) and (d) The zoom-in images showing the top, middle and bottom part of the via. The via diameter has a good consistency along vertical direction.

4.2.2 Fabrication of Glass Interposer

Glass instead of Si is selected as the interposer substrate due to its high resistivity and low permittivity, which are beneficial for RF loss reduction. The fabrication of glass interposer also requires three steps of lithography (similar with the backside process of TSV die). The first lithography is to define the RDL (3 μm Cu). After the ECP of RDL, the adhesion and seed layers are carefully etched. In addition to the chemical wet etching process, H_2 plasma etching is used to physically remove the residue and minimize the leakage current. Following that, the 5 μm polyimide (HD8930) is coated on top of Cu RDL as passivation layer. The second lithography is then performed to define the passivation layer opening, followed by another step of adhesion and seed layers deposition. The third lithography is then carried out to define the ECP of under bump metallization (UBM) (Figure 33 (i-l). The final etching for the adhesion and seed layers of UBM is more straightforward as compared to that of RDL, as the UBM pattern is disperse and no small gaps exist. The obtained yield of interposer wafer is up to 99%. The fabricated TSV die and interposer on the Si and glass wafers (12-inch) are respectively shown in Figure 35 (a) and Figure 35 (b).

After diced into small chips, individual TSV die and glass interposer are aligned and bonded together (Figure 33 (m)). Three paired markers which are respectively located at the backside RDL of TSV die and frontside RDL of glass interposer are used for precise alignment (Figure 36). An in-situ reflow process with temperature of up to 220 ℃ is conducted to melt the micro bumps and form the solid connection. No underfill material is introduced between TSV die and glass interposer due to the limitation of ultra-high vacuum compatibility. After bonding, the TSV trap is packaged into a CPGA in a similar way to that illustrated in Section 3.3.4. The cross-sectional SEM images and post-package optical images of TSV trap are shown in Figure 37 (a) and (b). Note that the shape of micro bump has been slightly deformed after the reflow and bonding processes. Apparently, a vertical signal transmission path is built from the RDL on the interposer, through the TSV, to the surface electrode on the ion trap.

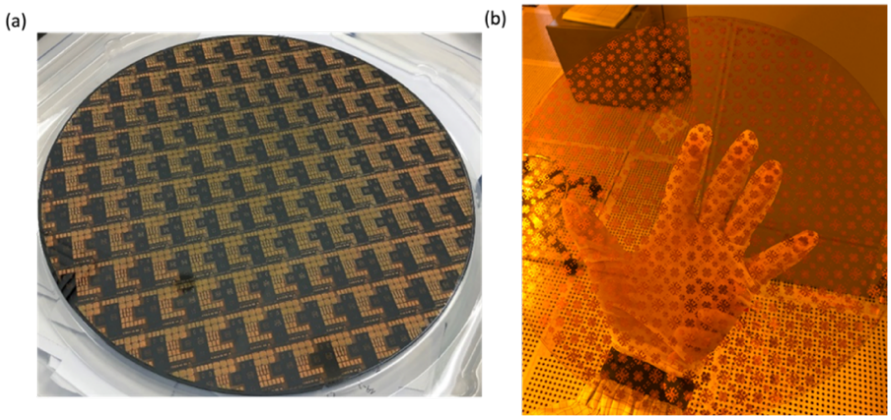


Figure 35. (a) Fabricated TSV die on a 12-inch silicon wafer. (b) Fabricated interposer on a 12-inch glass wafer.

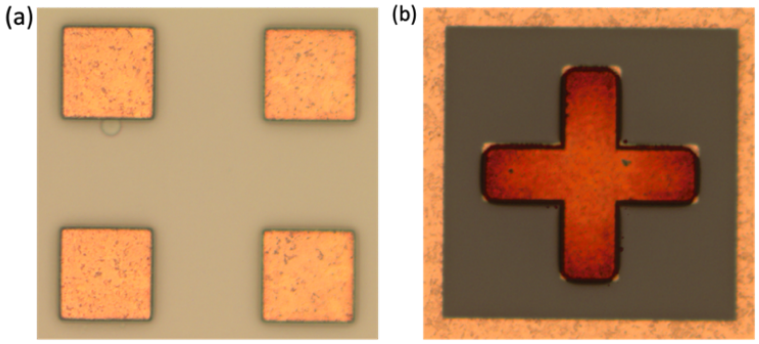


Figure 36. Paired markers for bonding alignment of TSV die and glass interposer. (a) Female marker on TSV die backside. (b) Male marker on glass interposer.

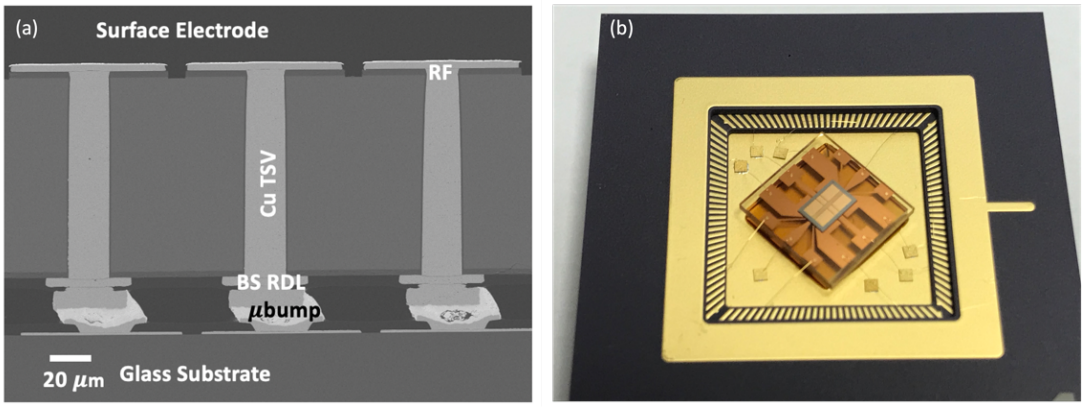


Figure 37. (a) Cross-sectional SEM image of TSV die bonded onto glass interposer. The bump shape is slightly deformed due to the thermal and mechanical stress. (b) TSV trap assembled into a CPGA.

4.3 Electrical Characterization and Analysis of TSV Integrated Ion Trap

4.3.1 Leakage Current Test of TSV

During ion trapping operation, RF signal with >100 V amplitude is transmitted from interposer to the RF electrodes through TSV, rising a challenge to the dielectric liner (0.75 μm

SiO_2). To assess the reliability of the TSV liner on withstanding the high voltage, a leakage current test is conducted.

As shown in Figure 38 (a), a standard TSV array for TSV leakage current test is designed within the TSV die. Before the fabrication of wafer backside (the backside routing interconnects of TSV array has not been built), leakage current measurement on single TSV can be carried out. The setup for TSV liner leakage measurement is illustrated in Figure 38 (b), in which a metal pad serving as grounding is placed underneath the TSV die. One probe is contacted with the surface electrode connecting with single TSV, whereas the other probe is contacted with the grounding pad. The voltage sweep applied ranges from -200 to 200 V with a 2 V step. As shown in Figure 38 (c), the measured maximum leakage current of single TSV is ~7×10^{-12} A at 200 V, indicating that the TSV liner is sufficiently thick and has a breakdown voltage larger than 200 V.

Also, a similar *I-V* measurement as that illustrated in Section 3.3.1 is performed between RF and central DC electrodes on both TSV die and glass interposer. The results show a minimum resistance of ~2×10^{8} Ω (TSV die), which is sufficiently large for voltage insulation. In addition, the connection between interposer RDLs and corresponding surface electrodes is checked. No open circuit is found, indicating a firm and stable signal transmission path.

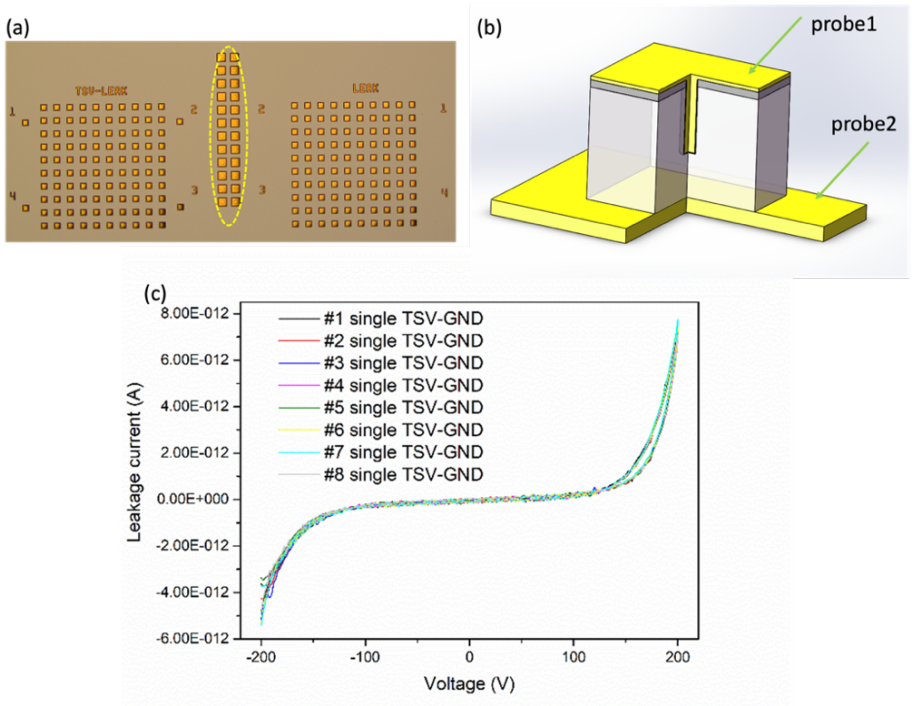


Figure 38. (a) Standard TSV array structure designed within TSV die. The pads containing single TSVs (the routing at wafer backside has not been built) are marked in the yellow circle. (b) Setup for TSV liner leakage current measurement. (c) Repetitive test results for leakage current of single TSVs.

4.3.2 *C-V* Test and Analysis

Using the similar setup as illustrated in Section 3.3.2, the MOS capacitance of individual RF electrodes (in connection with TSV) can be measured. Note this measurement is also performed before the wafer backside fabrication. At the same time, an analytical model is developed to calculate the MOS capacitance. The obtained results from measurement and calculation are compared and discussed.

As different from WB traps, for TSV die in TSV trap, both planar surface electrode and TSVs contribute to the total MOS capacitance (Figure 39 (a)). These two capacitors from corresponding oxide layers are in parallel as illustrated in the circuit model in Figure 39 (b) (accumulation regime). However, at the depletion regime, the capacitance of depletion layers will come into effect. Again, these depletion layers are formed not only under planar oxide layer but also around TSV oxide liner. Accordingly, the model should be modified where depletion layer capacitance are added in series with the original oxide capacitance (Figure 39(c)). The total MOS capacitance can now be expressed as:

$$C_{total} = \left(\frac{C'_{planar\_ox} \times C'_{planar\_dep}}{C'_{planar\_ox} + C'_{planar\_dep}}\right) + \left(\frac{C'_{TSV\_ox} \times C'_{TSV\_dep}}{C'_{TSV\_ox} + C'_{TSV\_dep}}\right), \quad (17)$$

where C'_{planar_ox} (C'_{planar_dep}) is equal to the oxide (depletion layer) capacitance per area C_{planar_ox} (C_{planar_dep}) times the electrode surface area *S,* and C'_{TSV_ox} (C'_{TSV_dep}) is equal to the oxide (depletion layer) capacitance of single TSV C_{TSV_ox} (C_{TSV_dep}) times the TSV number n. The C_{planar_ox} for planar surface electrode can be calculated using equation:

$$C_{planar\_ox} = {\varepsilon_{ox}}/{t_{ox}}, \quad (18)$$

where ε_{ox} is the dielectric constant ($4.2\varepsilon_0$) and t_{ox} (3 μm) is the thickness of planar oxide layer. For TSV, C_{TSV_ox} is expressed in equation given by [166]:

$$C_{TSV\_ox} = {2\pi\varepsilon_{ox} l_{TSV}}\Big/{\ln\left(\frac{R_{ox}}{R_{copper}}\right)}, \quad (19)$$

where l_{TSV} (100 μm) is the length of TSV, R_{ox} (10.75 μm) is the radius of TSV trench (as etched) and R_{copper} (10 μm) is the radius of Cu core. Similarly, at the depletion regime, the C_{planar_dep} can be expressed with equation:

$$C_{planar\_dep} = {\varepsilon_{Si}}/{t_{dep}}. \quad (20)$$

C_{TSV_dep} is expressed with equation:

$$C_{TSV\_dep} = {2\pi\varepsilon_{Si} l_{TSV}}/{\ln\left(\frac{R_{dep}}{R_{ox}}\right)}, \quad (21)$$

where $R_{dep} = R_{ox} + t_{dep}$. The t_{dep} is the maximum thickness of depletion layer, which can be expressed using the following equation:

$$t_{dep} = \sqrt{\frac{2\varepsilon_{Si} 2\varphi_B}{qN_d}}, \quad (22)$$

where ε_{Si} is the dielectric constant of silicon ($11.7\varepsilon_0$), q is elementary charge, φ_B is the bulk potential and N_d is donor concentration. To determine the value of N_d, a spreading resistance profile is carried out from the trap surface all the way down to 110 μm depth of Si substrate so that the whole TSV length has been covered (Solecon Laboratories). It is found that the doping concentration is quite consistent along the vertical direction and has a value of about 7×10^{13} cm^{-3}. Also, φ_B can be characterized with equation:

$$\varphi_B = \frac{kT}{q} ln \frac{N_d}{n_i}, \quad (23)$$

where k is Boltzmann constant, T (300K) is room temperature, and n_i (~1×10^{10} cm^{-3}) is the intrinsic carrier concentration.

Using the equations given above, the parameters φ_B, t_{dep}, C_{planar_ox}, C_{TSV_ox}, C_{planar_dep}, and C_{TSV_dep} are calculated and summarized in Table VI. Based on that, the total MOS capacitances of different traps are further analytically derived. The calculation process is demonstrated using the MOS capacitance at depletion regime of TSV die as an example:

$$C_{total} = \frac{1}{\frac{1}{1.24 \times 10^{-5} \times 233600 \times 10^{-12}} + \frac{1}{3.55 \times 10^{-5} \times 233600 \times 10^{-12}}} + \left(10 \times \frac{1}{\frac{1}{0.32 \times 10^{-12}} + \frac{1}{0.27 \times 10^{-12}}}\right) = 3.6 \times 10^{-12}\ (F). \quad (24)$$

The measured curves of MOS capacitance as a function of voltage of different traps are shown in Figure 40. In Table VII, the capacitance readings from Figure 40 are compared with the analytical results. An overall good agreement is achieved. Both the measurement and calculation show that the MOS capacitance of TSV die is reduced to ~10 % of WB traps. This significant reduction can be attributed to the elimination of wire bonding pad and the corresponding electrode size minimization. Indeed, the incorporation of TSV underneath electrode introduces additional parasitic capacitance from TSV itself. However, as shown in Table VI, the total MOS capacitance is dominated by the planar surface electrodes. Certainly, the capacitance can be further reduced if less TSVs are included in each electrode.

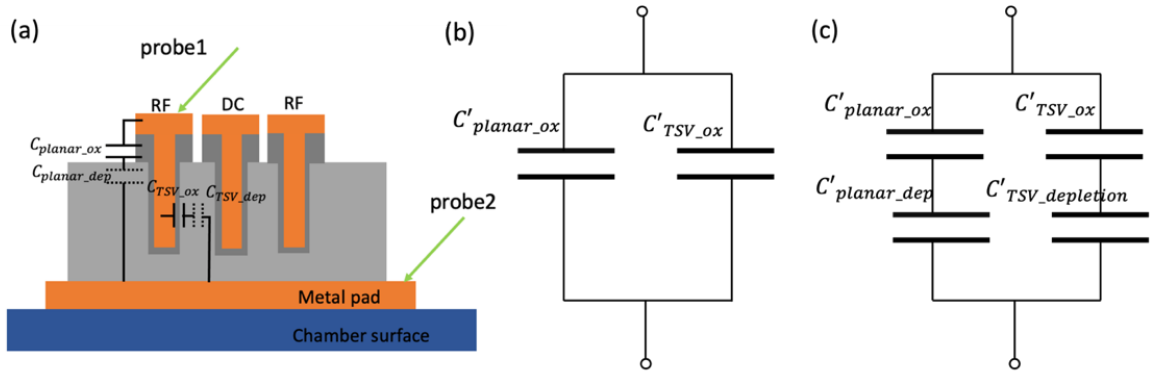


Figure 39. (a) Setup schematic of the TSV die MOS capacitance measurement. The corresponding circuit model on capacitance is plotted inside. Simplified capacitance circuit model at (b) accumulation and (c) depletion regime of TSV die.

Table VI. Calculated fundamental parameters for capacitance characterization.

Parameters	φ_B(V)	t_{dep}(μm)	C_{planar_ox} (F/m^2)	C_{TSV_ox} (pF)	C_{planar_dep} (F/m^2)	C_{TSV_dep} (pF)
TSV wafer	0.23	2.91	1.24E-5	0.32	3.55E-5	0.27
WB wafer*	0.28	1.11	1.24E-5	N.A.	9.35E-5	N.A.

*The doping concentration of WB wafer is 6×10^{14} cm^{-3}

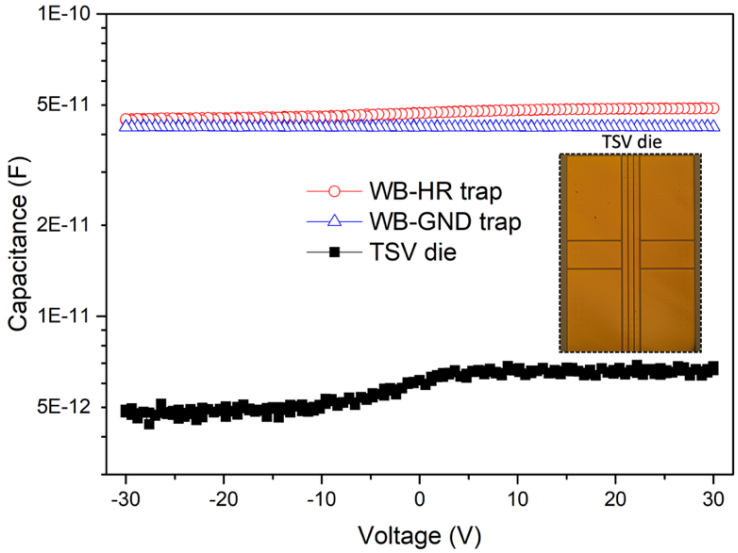


Figure 40. The comparison of MOS capacitance of TSV die, WB-HR trap and WB-GND trap. An optical image of TSV die is shown in the inset.

Table VII. Calculated capacitance and the comparison with measurement of various traps.

	RF electrode area (μm^2)	**TSV number**	**C_{total} (pF) from *calculation* (accumulation)**	**C_{total} (pF) from *measurement* (accumulation, 30V)**	**C_{total} (pF) from *calculation* (depletion)**	**C_{total} (pF) from *measurement* (depletion, -30V)**
WB-HR trap	4509600	0	55.9	48.9	49.4	44.8
WB-GND trap	4509600	0	55.9	42.4	49.4	42.4
TSV die	233600	10	6.1	6.6	3.6	4.8

In addition to the MOS capacitance, the capacitance between RF and central DC electrodes of TSV die (two-electrode capacitance) is measured. Note this measurement is performed after the fabrication of wafer backside. The obtained curve is compared with those from WB-HR and WB-GND traps in Figure 41. The two-electrode capacitance of TSV die is reduced to 1.2 pF from >24 pF of WB trap. After bonding the TSV die to the glass interposer, the final capacitance of TSV trap increases from 1.2 pF to 3 pF, as shown in Figure 41. It should be highlighted that though the overall size and corresponding parasitic components of ion trap are generally proportional to the electrode dimension, TSV trap is able to maintain a relatively large electrode dimension (80 μm) while a small capacitance (3 pF), due to the introduction of TSV. As a comparison, in a work reported by Duke University in year 2016, a trap with RF electrode of 60 μm has a capacitance of ~12 pF [72].

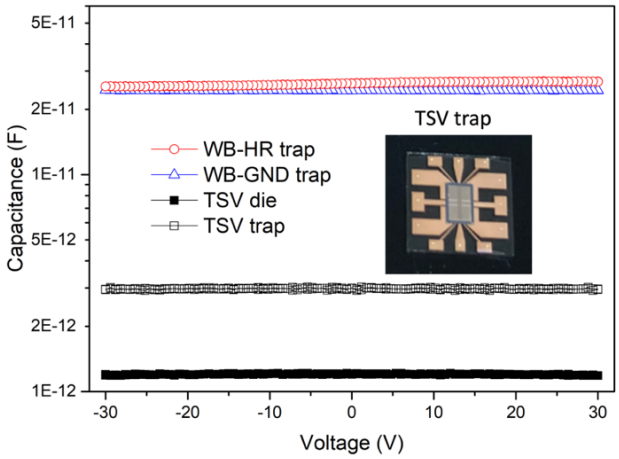


Figure 41. The comparison of capacitance between two central electrodes of TSV die, TSV trap, WB-HR trap and WB-GND trap. An optical image of TSV trap (TSV die bonded with glass interposer) is shown in the inset.

4.3.3 S-parameter Measurement

The on-chip RF loss of TSV trap (TSV die bonded with glass interposer) is measured with similar setup as illustrated in Section 3.3.3. As shown in Figure 42, the insertion loss of TSV trap have been reduced significantly (0.11 dB at 50MHz), as compared to those from WB counterparts (2.38 dB for WB-HR trap and 1.28 dB for WB-GND trap).

In addition to the measurement, the RF loss is also characterized using FEM. As different from the modelling used to visualize the electric field distribution, the modelling for S-parameter does not require to build a vacuum entity above the trap. Instead, the electric field distribution inside the trap is the focus. In the modelling, the frequency sweep is set from 10 to 110 MHz with a step of 10 MHz. A good consistency between measurement and modelling is established, as shown in Figure 42. In addition, from the modelling, it is also found that the thickness decrease of silicon substrate (from 700 to 100 μm) also benefits for the loss reduction.

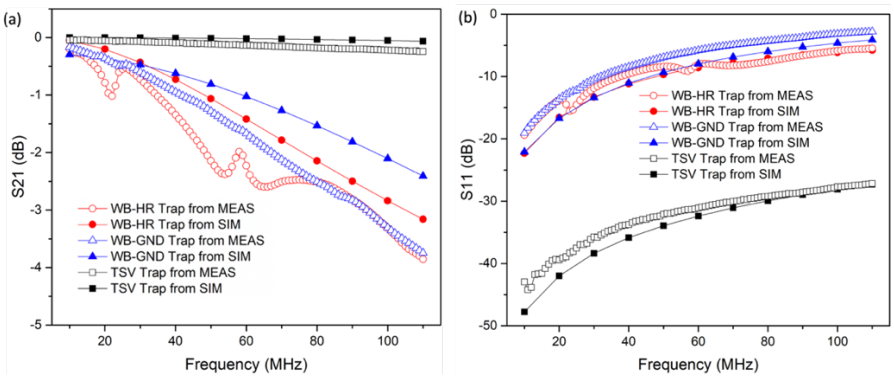


Figure 42. (a) Insertion loss and (b) reflection loss comparison of TSV trap, WB-HR and WB-GND trap. The curves obtained from FEM are plotted together, demonstrating a decent agreement between measurement and modelling for each trap variation.

4.3.4 Resonator Test and Analysis

After the TSV trap is assembled into the CPGA, a resonator test is performed with similar setup as given in Section 3.3.4. The resonance curve of TSV trap is obtained and compared with those from WB traps. To provide a quantitative insight of the power loss of different ion traps, the lumped circuit model of the trap connecting with the external transformer is built, as shown in Figure 43. The resonance curves are determined by the characteristics of two elements: 1) the resonant circuit + cabling + CPGA; 2) the trap itself. The ion trap is further modelled as a capacitor (C_{trap}) in series connection with an equivalent series resistance (ESR).

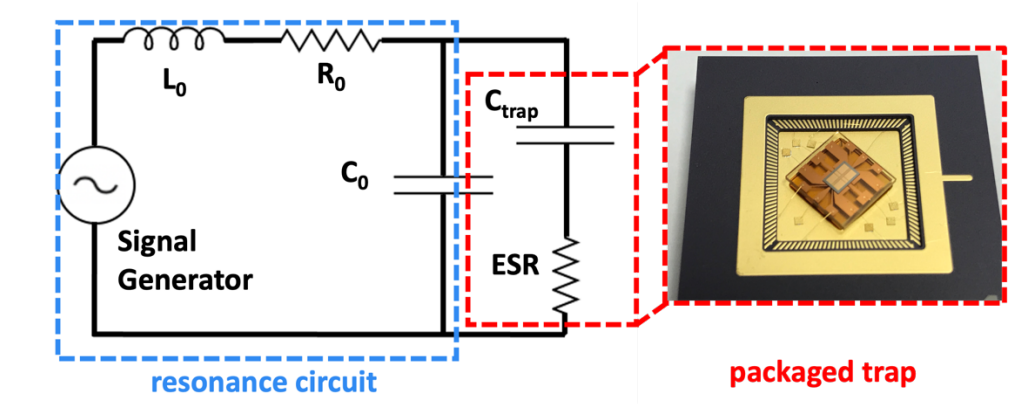


Figure 43. Lumped circuit model of the trap connecting with transformer in resonator test.

To determine the RLC circuit parameters (R_0, L_0, and C_0 in Figure 43) independently of the trap, separate resonator test is performed on the standard capacitors with negligible ESR (AVX SQ series capacitors, wire bonded into CPGA) as well as bare CPGA (Figure 44 (a)). The resonance frequency f_0 for circuit with bare CPGA can be calculated using the following equation:

$$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}}. \tag{25}$$

When a standard capacitor is connected, the resonance frequency changes accordingly due to the incorporation of external capacitance C_e:

$$f_e = \frac{1}{2\pi\sqrt{L_0(C_0+C_e)}}. \tag{26}$$

The inductance L_0 can thus be extracted using the following equation:

$$L_0 = \frac{(1/2\pi f_e)^2 - (1/2\pi f_0)^2}{C_e}. \quad (27)$$

Substituting L_0 into Equation (25), the capacitance C_0 is also determined. The resistance R_0 can be calculated with the Q factor equation in series RLC circuit after a simple transformation:

$$R_0 = \frac{1}{Q}\sqrt{\frac{L_0}{C_0}}. \quad (28)$$

At the same time, the Q factor can be extracted using the following equation:

$$Q_0 = \frac{f_0}{FWHM} \quad (29)$$

where $FWHM$ is the 3dB bandwidth which can be directly extracted from the reference resonance curves in Figure 44 (b). Table VIII shows the determined parameters (R_0, L_0, and C_0) using the equations listed above.

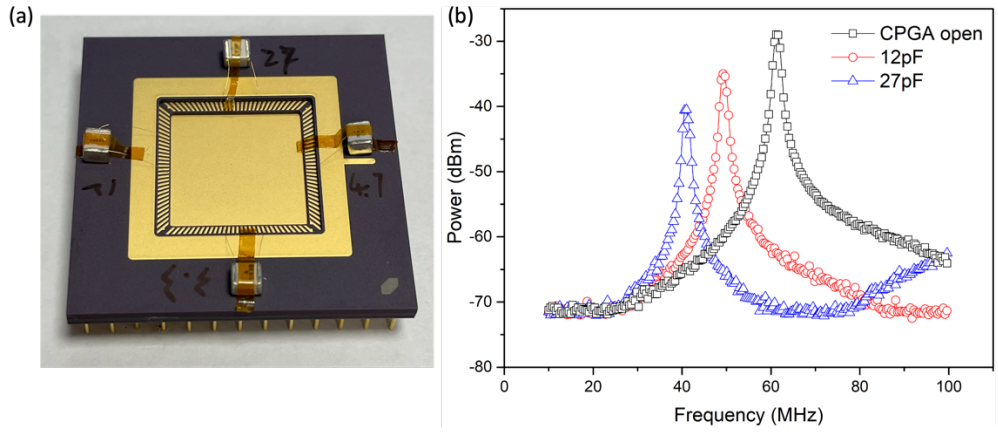


Figure 44. (a) Standard capacitors with different capacitance that wire bonded into CPGA. (b) Reference resonance curves from bare CPGA and standard capacitors that wire bonded into CPGA.

Table VIII. Extracted RLC circuit parameters.

	Capacitance (pF)	**Resonance frequency (MHz)***	**Calculated L_0 (μH)**	**Calculated C_0 (pF)**	**Calculated R_0 (Ω)**
Standard capacitor#1	12	49.25	0.310	21.67	3.70
Standard capacitor#2	27	41.00	0.309	21.73	3.69

*Circuit with bare CPGA has a resonance frequency of 61.4 MHz, and a 3dB bandwidth of 1.9 MHz.

Next, C_{trap} and ESR shall be determined. With the resonance frequencies of different traps read from Figure 45 (a), the C_{trap} can be respectively calculated using Equation (26). Meanwhile, fixing these obtained circuit parameters, the ESR associated to the traps can be retrieved from a fit of the trap resonance curves, in which ESR mainly affects the Q factor. The fit is performed by building the corresponding lumped circuit in COMSOL Multiphysics. The extracted C_{trap} and ESR are summarized in Table IX. Note the C_{trap} here is the total capacitance from RF electrode to the ground (including trap and CPGA surface), which is larger than the measured capacitance (between two neighbouring electrodes) in Section 4.3.2. With C_{trap} and ESR, the power loss (P_{loss}) of ion trap itself can be calculated with equation given by [23, 167]:

$$P_{loss} = \left(C_{trap}\Omega_{RF}V_{RMS}\right)^2(R_s + ESR), \tag{30}$$

where Ω_{RF} is the RF frequency, V_{RMS} is the root-mean-square RF voltage, and R_s is net series resistance of surface electrodes. Assuming R_s is much smaller than ESR, the P_{loss} of different traps can be determined. As shown in Table IX, the calculated power loss of WB-GND trap and TSV trap is ~100 times smaller than that of WB trap. The power loss reduction of WB-GND trap is dominated by its small ESR (0.3 Ω), owing to the complete elimination of the parasitic components in silicon substrate which is effectively shielded from RF signal by the grounding plane. In the TSV trap, however, both small capacitance (9.1 pF) and ESR (5 Ω) play an important role in power loss reduction, of which the ESR is minimized largely due to the smaller dimension and thickness of the silicon substrate itself.

Meanwhile, the RF power losses of different traps are also evaluated from the FEM (Figure 45 (b) and (c)). The Joule heating induced by the electric field inside the ion trap can be extracted. In the simulation, different resonance RF frequencies (but same V_{RMS} of 100 V) are applied to the corresponding ion traps. The simulated heating powers basically agree well with those from calculation (Table IX). The deviation between calculation and simulation for TSV and WB-GND traps may come from the negligence of R_s in calculation.

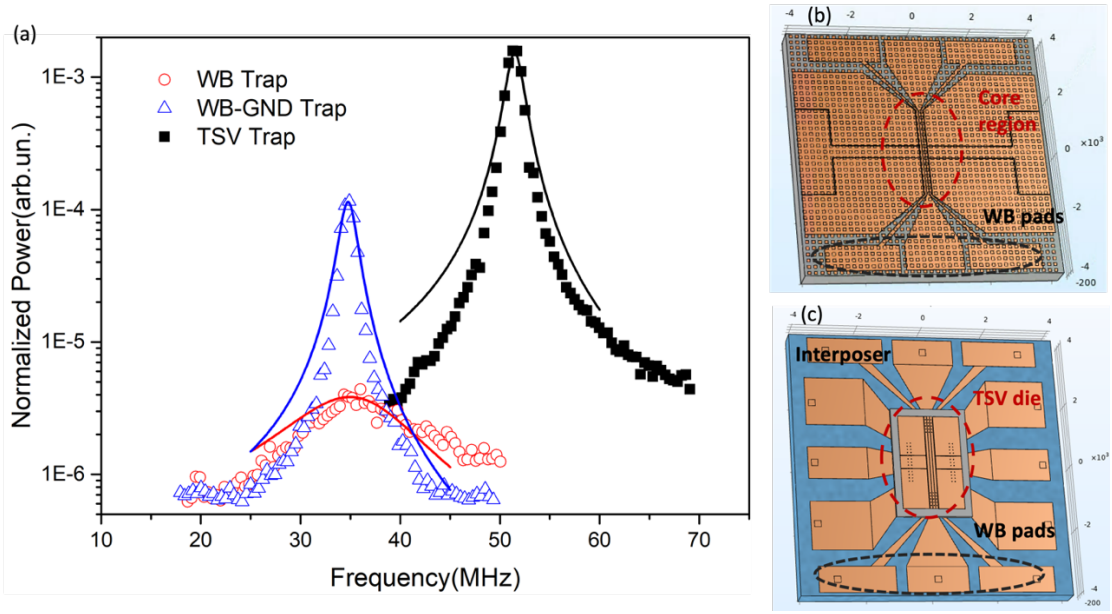


Figure 45. (a) Resonance curves of TSV trap, WB-HR trap and WB-GND trap (with normalized power). The fit from circuit modelling are plotted together. (b) WB-GND trap and (c) TSV trap built in FEM for power loss simulation.

Table IX. Extracted circuit parameters and power losses of different ion traps.

	Resonance frequency (MHz)	***Q* factor (MHz)**	**C_{trap} (pF)**	**ESR (Ω) from fit**	**Calculated power loss @100V (W)**	**Simulated power loss @ 100V (W)**
WB-HR trap	35.1	1.8	44.7	40	38.83	39.74
WB-GND trap	34.8	16.5	45.8	0.3	0.30	1.96
TSV trap	51.5	22.4	9.1	5	0.43	2.85

4.4 Ion Trapping Test on TSV Integrated Ion Trap

The TSV trap assembled into CPGA is inserted in the vacuum cell and then baked at 150°C for one week. The resulting base pressure is approximately 4×10^{-11} mbar, demonstrating the excellent ultra-high vacuum compatibility of the packaged ensemble (trap, interposer and micro-bumps). The RF lines are driven with an impedance-matching toroidal resonant transformer at a frequency $\Omega_{RF}/2\pi$ = 30 MHz. The trap is only tested with amplitudes V_{RF} below 120 V. For V_{RF} larger than 85 V, a slight increase of the base pressure (of the order of some 10^{-11} mbar) is observed, probably associated to residual heat dissipation in the trap.

The ionization, cooling, repumping, and detection procedures are similar with those described in Section 3.4.1. Image of the trapped ions on the TSV trap captured by an electron-multiplier CCD camera is shown in Figure 46 (a).

Excess of micromotion in the trap is minimized using a single photon time correlation method [168]. The compensation DC voltages are found to be stable in a week basis. The lifetime of a laser-cooled ion in the trap is of the order of 30 minutes, compatible with the vacuum level and similar with that of glass trap (Section 3.4.2).

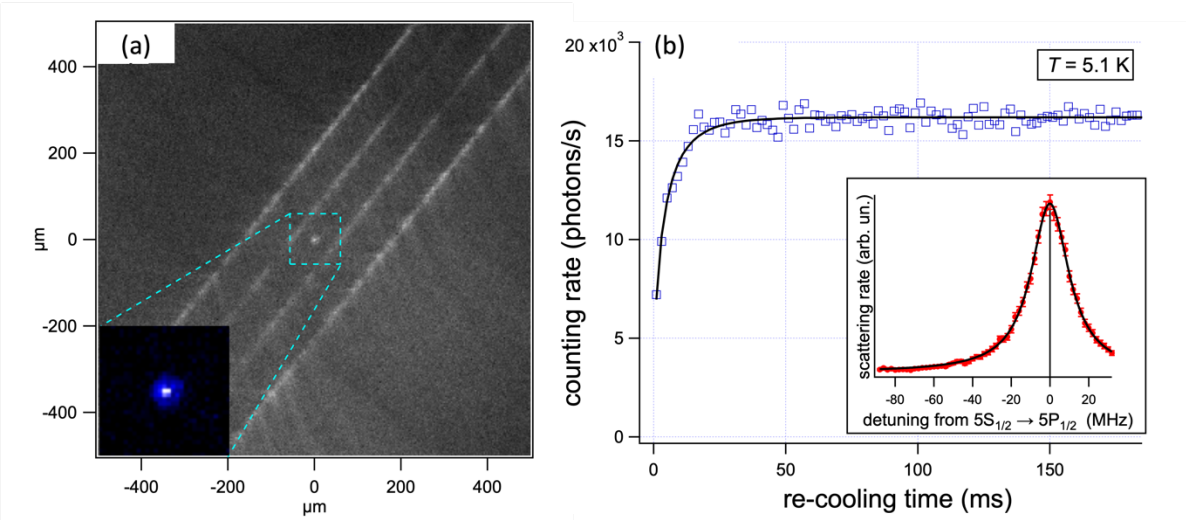


Figure 46. (a) Image of a single $^{88}Sr^{+}$ laser-cooled ion trapped above the surface of the TSV trap; the image field covers a 1 mm^2 area, the trap is illuminated by a light emitting diode. (b) Counting rate as a function of the re-cooling time averaged over 120 realisations for a heating time t_h = 20 seconds (blue squares). The continuous black curve is the best one-parameter fit that allows us to retrieve a temperature increase T=5.1 K. Inset: fluorescence spectrum of the ion as a function of the detuning of a probe beam that scans the cooling transition (red circles); the continuous black curve is a Lorentzian fit that shows that the incoherent repumping scheme leads to a very good two-level atom approximation.

The anomalous heating from electric-field noise above electrode surface represents limitations for various trapped-ion based applications. Though the sources of this heating are still not sufficiently clear, the heating rate indeed reflects the performance of a specific ion trap from the trap design, fabrication imperfections to the electrode surface contaminations. Therefore, the TSV trap performances are evaluated by measuring the heating rate with the technique of Doppler re-cooling [169]. For this purpose, the trap is operated with an axial frequency $\omega_y/2\pi$ = 300 kHz and radial frequencies around $\omega_r/2\pi$ = 2.6 MHz. In this situation, it is expected that the re-cooling dynamics will be dominated by the temperature of the low frequency axial mode, even though the cooling laser wavevector has a non-negligible projection along the radial direction [170]. A sequential acquisition first cools the ion during

500 ms, then switches off the cooling laser for a waiting (heating) time t_h, and then switches on again the cooling laser triggering the acquisition of single photons timestamped with arrival times. The two-level-atom approximation needed for the analysis of the acquired data [169, 170] is well fulfilled by the incoherent repumping approach. As shown in Figure 46 (b) inset, a single-ion fluorescence spectrum displays a Lorentzian line-shape. The single shot and average histograms of the scattered photons are recorded as a function of the emission time for different heating times t_h. An example of averaged histogram is plotted in Figure 46 (b) with the corresponding fit obtained with the hypothesis of a Maxwell-Boltzmann velocity distribution (T = 5.1 K for t_h = 20 s). From the analysis of all the experimental sets the heating rate of the trap is evaluated at 250 ± 15 mK/s that corresponds to 17 axial quanta per millisecond. The calculated figure of merit corresponding to the noise spectral density times the motional frequency [171] is $\omega_y * S_E(\omega_y)$ =1.5 × 10^{-4} $(V/m)^2$. Technical noise contribution to this figure is expected to be negligible, thanks to previous evaluations performed with the same setup. While it does not set a new record, this result favorably compares to non-decontaminated and non-cryogenics traps of similar dimensions [172].

4.5 Thermal Dissipation of TSV Trap

As mentioned earlier, in the ion trapping test, a slight vacuum level degradation is found (in the level of several 10^{-11} mbar) when the RF amplitude is higher than 85 V. This is attributed to the high temperature of TSV trap ($P = {nRT}/{V}$). Even though TSV trap has a low power loss (Section 4.3.4), the poor thermal dissipation may still result in its high temperature as similarly suffered by conventional 3D integrated circuits [173, 174].

Note the heat dissipation mechanism of ion trap is dominated by the thermal conduction, while the effect from thermal convection is negligible since ion trap is operated at an UHV environment. Currently, the produced Joule heat is transferred from TSV die to the CPGA surface (assuming it maintains a constant room temperature, 23 $°C$ or 296.15 K) through micro bump and glass interposer. Due to the small contact area of micro bump as well as the poor thermal conductivity of glass, it is speculated that heat is concentrated at the TSV die and cannot be dissipated efficiently, resulting in a high temperature of TSV die. To verify this speculation, first, the temperature of TSV trap electrode surface is measured (not in the vacuum chamber). As shown in Figure 47 (a), the temperature of TSV die increases by ~20 K at an RF amplitude of 50 V. Meanwhile, the temperatures of different traps (WB-HR, WB-GND and

TSV trap) as a function of applied RF amplitude are obtained from the finite element modelling (Figure 47(b)). It should be highlighted that the temperatures of TSV trap from simulation and measurement are in good agreement (Figure 47 (a)). The simulation result indicates that WB-HR trap has the highest temperature increase due to its high power loss. In contrast, WB-GND trap can basically maintain the initial temperature, whereas the temperature of TSV trap is intermediate between WB counterparts. The temperature distribution patterns of WB-GND trap and TSV trap are further extracted. As illustrated in Figure 48 (b), WB-GND trap has a low and uniform temperature distribution due to its low power loss and relatively large thermal conduction area. However, as speculated, the heat of TSV trap is concentrated at the TSV die, while the temperature increase of glass interposer is negligible (Figure 48 (a)).

To mitigate the heating issue of TSV trap, different solutions are proposed based on two fundamental mechanisms: heat generation reduction and heat dissipation enhancement. Concerning the heat generation reduction, the effect of the silicon substrate that dominates the power loss is largely investigated. Again, by increasing the wafer resistivity or introducing grounding plane, it is believed the conventionally-lossy silicon substrate can be more resistant to the RF signal and thus generate less power loss. On the other hand, in terms of heat dissipation enhancement, to build a high efficiency heat dissipation path between ion trap and CPGA, materials with different thermal conductivity are modelled as the interposer substrate and the performance is compared. In a more aggressive approach, the glass interposer can even be eliminated (see Section 4.6). All the proposals are validated with corresponding finite element modelling.

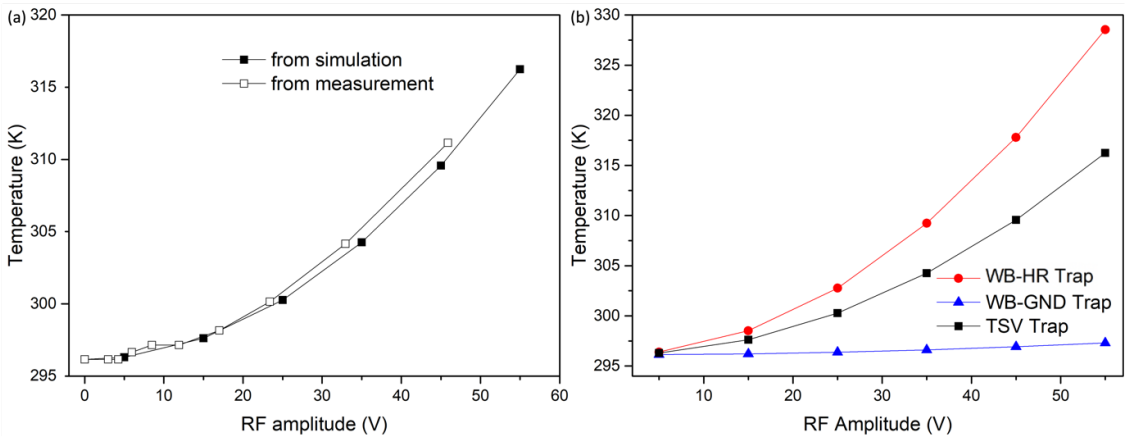


Figure 47. (a) The measured and simulated temperature of TSV trap surface as a function of applied RF amplitude. (b) Comparison of simulated temperature of TSV trap, WB-HR trap and WB-GND trap.

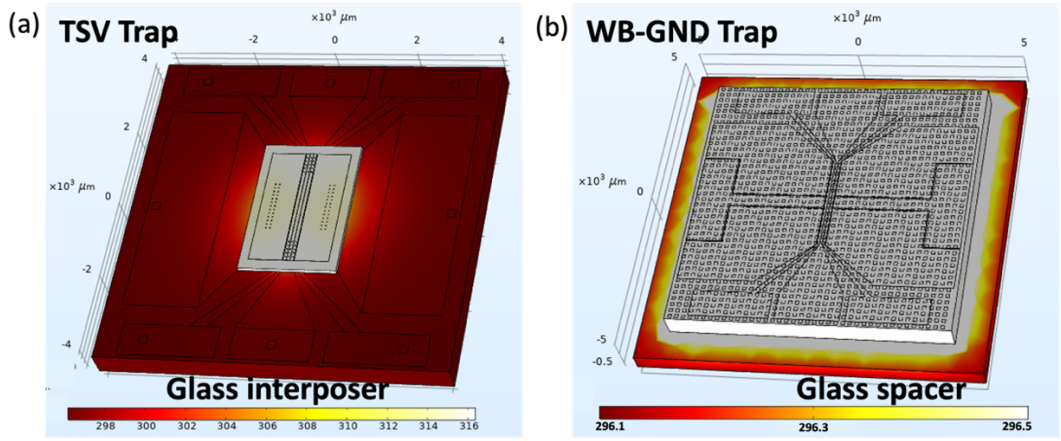


Figure 48. Simulated temperature distribution pattern of (a) TSV trap and (b) WB-GND trap.

4.5.1 Heat Generation Reduction of TSV Trap

Based on the result of the volume integration of heat power in different components of ion trap, it is found that the heat generated from the silicon substrate dominates (~0.1 W at 50V RF amplitude) the total heat, as compared to the metal electrodes and vias (5E-7 W), and glass interposer (3E-5 W). In this case, it is necessary to select a silicon substrate with suitable electrical conductivity to minimize the power loss from silicon substrate itself. Based on the simulation (Figure 49 (a)), it is found that the silicon substrate with conductivity of smaller than 0.01 or larger than 100 S/m is able to reduce the temperature significantly. As mentioned in Section 2.1.1, on the one extreme, when the resistance is sufficiently high, the silicon substrate behaves like an insulator and no current would flow through silicon (low capacitance). On the other extreme, when the resistance is sufficiently small, the silicon substrate can be seen as a conductor and the voltage drop over it can be neglected (low resistance). As a result, in both cases, the RF loss is very small, resulting in a low temperature. However, in the worst case, the silicon substrate has a mild resistance and capacitance simultaneously. This corresponds to the region close to the peak in Figure 49 (a) that has a silicon conductivity of 0.1-10 S/m. Since the resistance transition from insulator to conductor for silicon substrate is continuous, the resultant temperature (RF loss) has a up and down shape, as shown in Figure 49 (a). However, the wafers currently used to fabricate the TSV integrated ion trap have a conductivity in the high loss region, which can be replaced by high-resistivity wafers in future.

Additionally, grounding plane is commonly used in high-frequency devices to shield the lossy silicon substrate from the signal. Similar with the idea of incorporating grounding plane

into WB trap (Section 3.1), it is worthwhile to investigate the effect of grounding plane to the heat generation reduction in the case of TSV trap. In the simulation, a grounding plane (Cu, 2 μm in thickness) is introduced between surface electrode and silicon substrate. Note specific windows are made onto this plane to accommodate the TSVs. As shown in Figure 49 (b), the temperature drops notably for trap with this grounding plane, as compared to the current TSV trap. The temperature increase is able to be kept <1 K at an RF amplitude of 50 V. Meanwhile, the electric field distribution inside silicon substrate is extracted. As shown in Figure 50, after the incorporation of grounding plane, the electric field intensity (especially close to RF TSVs) is reduced by more than one order of magnitude. The actual implementation of grounding plane into TSV trap is discussed in Chapter 5.

As different from conventional traps that use bonding wires located on the surface, the TSVs in TSV trap goes vertically in the half space underneath electrode. As a result, the electric field can penetrate to the entire silicon substrate and generate more heat (Figure 50). In theory, the decrease in TSV number and increase in pitch between TSV will enable the heat reduction. However, considering the reliability during fabrication and assembling, the number of TSV cannot be reduced without limitation. Meanwhile, the pitch between TSV is normally fixed with the via diameter in a foundry due to the limitations from etching and via filling process.

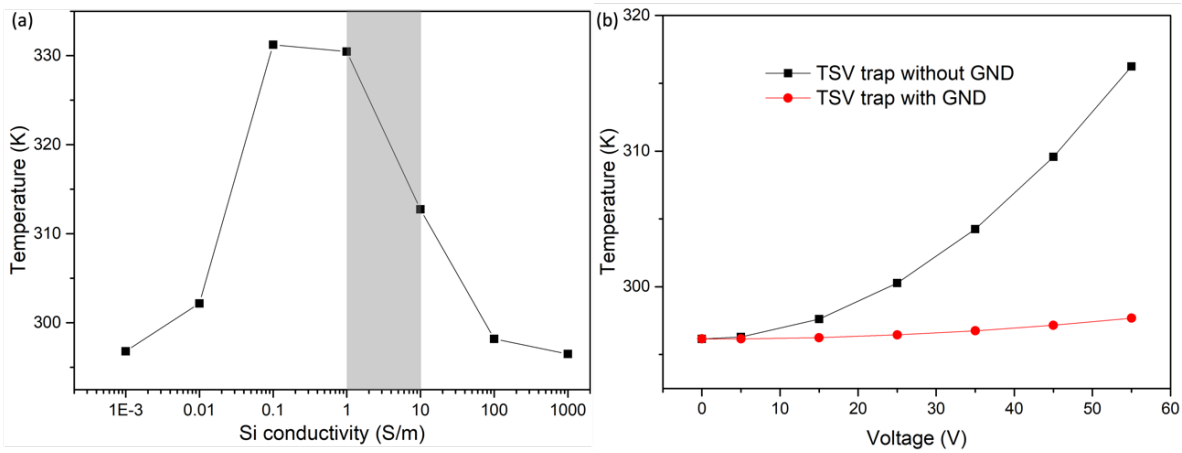


Figure 49. (a) The resultant temperature of TSV trap as a function of Si conductivity. The RF voltage has a constant amplitude of 50 V and frequency of 30 MHz. (b) The comparison of resultant temperature for TSV trap with or without grounding plane.

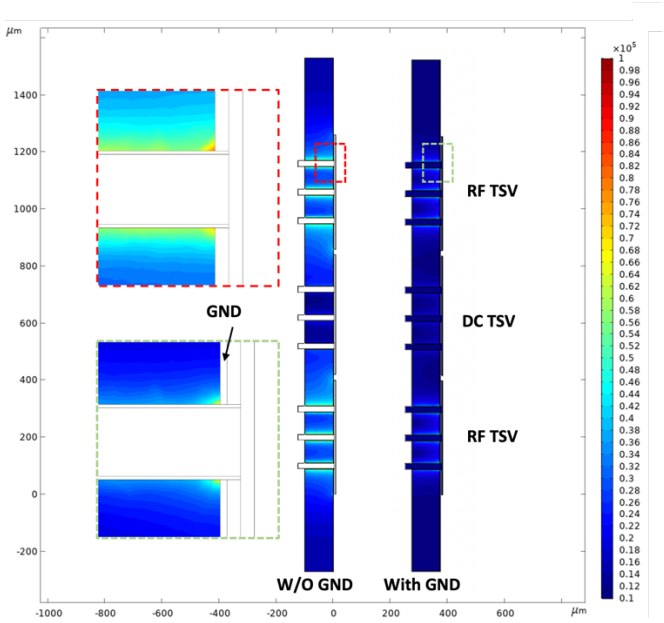


Figure 50. The electric field distribution in the silicon substrate before and after the incorporation of grounding plane. Two zoom-in image on the connection region of TSV and surface electrode for both cases are shown on the left. The grounding plane position is marked accordingly.

4.5.2 Heat Dissipation Enhancement of TSV Trap

According to the principle of one-dimensional Fourier's law of heat conduction:

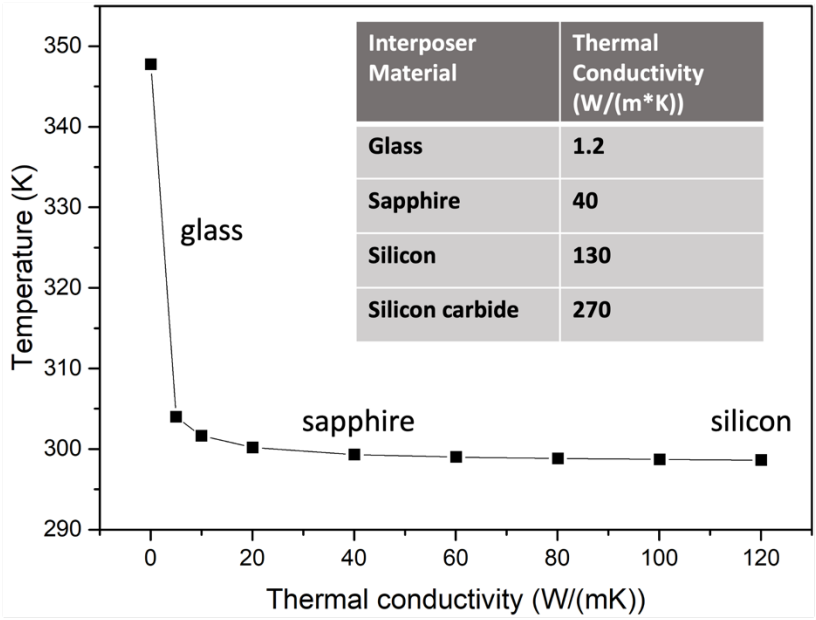
$$q = \frac{Q}{A} = -k\frac{\partial T}{\partial x}, \tag{31}$$

the heat flux density q is linear with the thermal conductivity of substance k and temperature gradient $\frac{\partial T}{\partial x}$. To enable high heat conduction flow, one can increase the contact area or the thermal conductivity.

As shown in Figure 48 (a), the temperature gradient between TSV trap and interposer is quite high due to the large temperature difference (TSV trap temperature increases by ~20 K, while glass interposer basically maintains the initial temperature). However, it is found that very small amount of heat is transferred from the TSV trap to the interposer. This is limited by the small contact area of micro bumps in between, though the SnAgCu micro bumps have favourable thermal conductivity. Therefore, to enhance the heat dissipation between TSV trap and glass interposer, additional thermal medium shall be introduced. In the modelling, an ideal thermal medium with thermal conductivity of 2000 W/(mK) but electrical conductivity of 0 S/m is introduced. In this case, no additional loss is generated from the medium itself and the embodied micro bumps are well isolated. The temperature reduction as the function of the area of this medium is obtained. Certainly, the trap with larger medium features larger temperature

reduction. However, for a thermal medium with maximum size (same dimension as TSV die), the temperature increase is merely reduced by ~5 K. The effect is not as obvious as that from grounding plane introduction. Also, it should be noted that for the fabricated ion trap, any additional underfilling or adhesion to be used as the thermal medium between TSV trap and interposer shall be compatible with the UHV working environment.

On the other hand, due to the poor thermal conductivity of interposer substrate, the heat cannot be dissipated to the CPGA surface which is seen as a heat sink. The resultant temperature as a function of the thermal conductivity of interposer substrate is thus investigated, as shown in Figure 51. It is found the temperature drops remarkably when the thermal conductivity increases to 20 W/(m · K). However, the further increase of the thermal conductivity may not play a significant role. The selection of interposer material with high thermal conductivity should not sacrifice the electrical performance. In general, a material with high thermal conductivity and dielectric property is preferred (for example, sapphire). However, a favourable manufacturability is always required.



Interposer Material	Thermal Conductivity (W/(m*K))
Glass	1.2
Sapphire	40
Silicon	130
Silicon carbide	270

Figure 51. The resultant temperature as a function of thermal conductivity of interposer material. The RF voltage has constant amplitude of 50 V and frequency of 30 MHz. The thermal conductivity of various possible materials is shown in the inset table.

4.6 Customized CPGA for Direct TSV Die Bonding

As discussed earlier, although glass interposer has superior insulation property, its poor thermal conductivity may result in the undesired temperature increase of the overall TSV trap. In this section, the possibility to eliminate the glass interposer is investigated. The idea is to bond the TSV die directly onto the CPGA surface where RDL is repositioned. In order to perform this operation, a customized CPGA with size modification, RDL patterning, internal CPGA and RDL connection is required.

4.6.1 Customized CPGA Design

The first concern about the customized CPGA is the overall size. The laser beams from fibers are Gaussian beams. Assuming the ion trapping height (~75 μm) is constant, the maximum allowable customized CPGA size can be calculated according to the beam size and wavelength of different laser lights. From calculation, the laser light with wavelength of 1092 nm (repumping for $^{88}Sr^{+}$) and beam waist of ~60 μm determines the maximum dimension (width and length, ~13 mm) of final CPGA. The embedded cavity of original CPGA is eliminated and all the surface of CPGA is raised to the same height, to protect light beam from scattering. Figure 52 (a) and (b) show the images of original and customized CPGA. Note the height difference (~120 μm, TSV + micro bump) from the trap surface to the CPGA surface is ignored in the calculation. As a result, the obtained 13 mm is sort of minification of the actual allowable dimension. An array of 25 pins (5 × 5) with an inter-pin pitch of 2.5 mm are accommodated at the backside in the customized CPGA.

The redistribution layer originally on the interposer is transferred onto the CPGA surface as Au trace. Note no additional under bump metallization is patterned. Based on the preliminary test result, the micro bump on the TSV die can be directly soldered onto the Au surface of CPGA. The patterned RDL geometry has an overall size of 5 × 5 mm^2.The peripheral area next to RDL is all covered by Au and grounded to specific CPGA pins. The RDL pad pattern designed for every single electrode of TSV die is shown in Figure 52 (c). The non-patterned region between RDL is exposed ceramic. Internal connections bridging RDL pad (circular tail at each pad) and CPGA pin are built through the ceramic substrate. In this approach, a more direct signal transmission path is established from CPGA pin to the surface electrode, through internal connection and TSV. In total, 11 pins of 25 pins are currently occupied for signal connection (i.e., RF, DC and GND), while the left 14 pins are floating. The tail of RDL pad

can also be connected with wire bonding where necessary (e.g., connect filtering capacitors for DC electrodes). Again, the patterned RDL geometry is sort of extension of surface electrode and can certainly be more complex if necessary. The leads on the peripheral of original CPGA have been completely eliminated due to the internal connection from RDL pad to the CPGA pin (Figure 52 (a) and (b)).

The fabrication of the customized CPGA is supported by Kyocera. The bonding procedure of TSV die and customized CPGA is similar with that illustrated in Section 4.2.2. Frist, TSV die is precisely placed onto the customized CPGA. Second, a reflow process is performed on the bonded chip. Due to the critical dimension limitation during customized CPGA fabrication process, the alignment marks on CPGA RDL are simplified to three empty squares. The optical image of the bonded chip is shown in Figure 53 (a). At the same time, X-ray is used to visualize the internal connections after bonding. A favorable alignment is observed in Figure 53 (b).

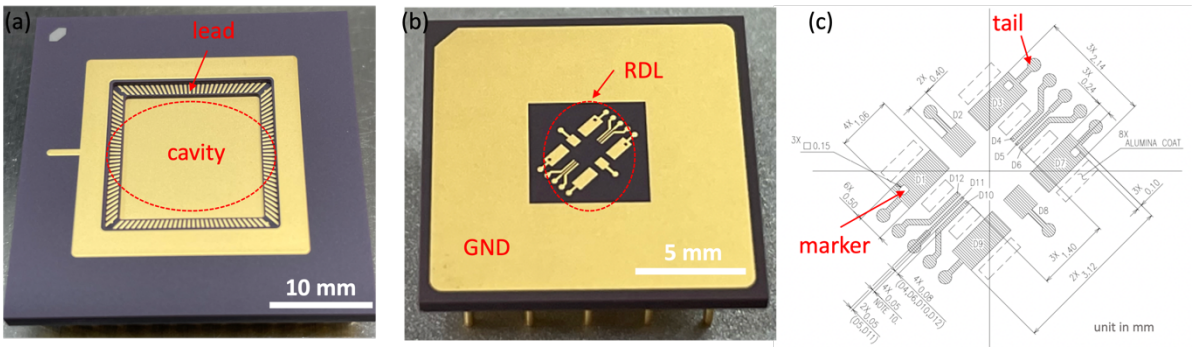


Figure 52. Front-view optical images of (a) original CPGA and (b) customized CPGA. (c) The geometry of RDL pattern of customized CPGA.

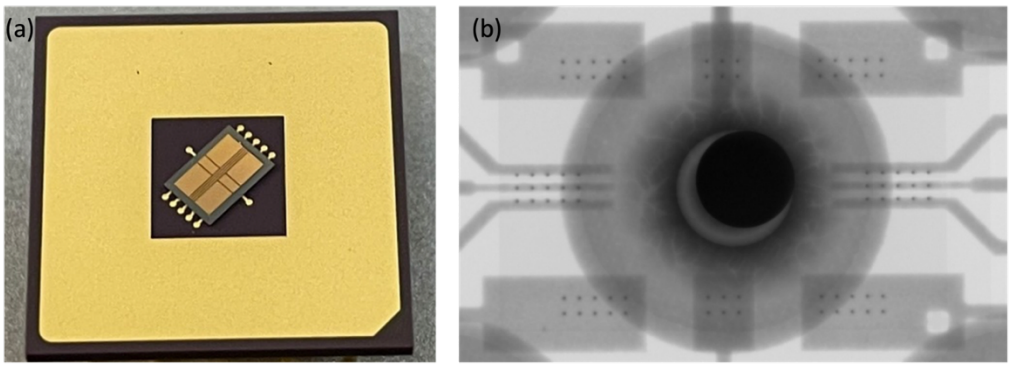


Figure 53. (a) Front-view optical image and (b) X-ray image of TSV die bonded onto customized CPGA.

4.6.2 Test of Customized CPGA Bonded with TSV Die

After the TSV die is bonded onto the customized CPGA, the first test is to check the connection from CPGA pin to the surface electrode. No open circuit is found, indicating a solid

signal transmission path. Next, the total resistance between neighboring RF and central electrodes (including the RDL pad on CPGA surface) is remeasured using *I-V* test. The result shows that the total resistance of bonded chip is basically equal to that of TSV die itself (at the order of 10^8 ohm, see Section 4.3.1), which means the resistance from RDL on CPGA is much higher. Indeed, based on the independent measurement, the resistance between neighboring RDL of customized CPGA is at the order of ~10^{14} ohm. Meanwhile, the total capacitance between neighboring RF and central electrodes of bonded chip is measured. The obtained total capacitance is ~5.4 pF, slightly higher than 3 pF of TSV trap (TSV die on glass interposer). However, it should be highlighted that the parasitic from CPGA has not been taken into account in the TSV trap capacitance measurement in Section 4.3.2.

To evaluate the RF performance of packaged TSV die on customized CPGA, a similar resonator test is performed. As expected, a higher power peak is observed as compared to that of TSV trap on original CPGA, suggesting that less power loss is generated from the whole device (Figure 54). Meanwhile, the higher resonance frequency indicates a smaller total capacitance.

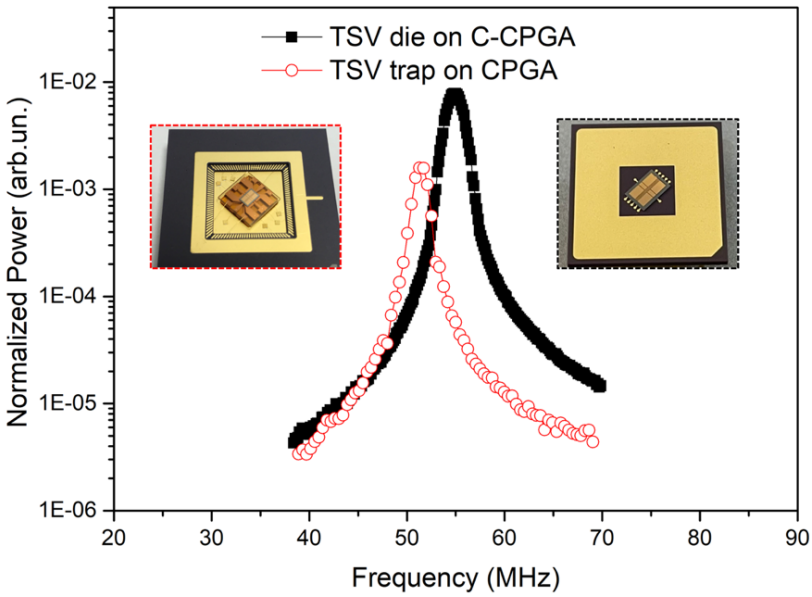


Figure 54. Resonance curves comparison between TSV die on customized CPGA (C-CPGA) and TSV trap on CPGA. Images of corresponding packaged chips are shown as insets.

Since TSV die is directly bonded to the CPGA surface, the thermal dissipation is enhanced significantly. A finite element modelling is performed based on the new physical model. It is found that the temperature increase of TSV die on the customized CPGA can be kept ~1 K at an RF amplitude of 50 V and frequency of 30 MHz. In addition to the good thermal

management, this customized CPGA together with the TSV die also open a broader path for advanced packaging of ion trap devices. The signal routing accessibility and flexibility for the trapping chip and the packaging assembly are simultaneously improved. The complete elimination of wire bonding that extends out the surface can be achieved (assuming capacitors are on-chip integrated). Meanwhile, once photonics components are integrated and lights are emitted from the chip itself, the CPGA size limitation will be released, allowing large scale implementation. Ion trapping test on this TSV trap with customized CPGA will be carried out once the CPGA socket modification in the vacuum chamber is completed.

4.7 Summary

In this chapter, the Cu-filled TSV integrated ion trap is introduced, in terms of trap design, fabrication process, electrical performance and analysis, ion trapping performance, and the thermal management. A novel silicon-glass integrated system is incorporated for the ion trap, where silicon die on the top maintains the compatibility with advanced fabrication process and glass interposer underneath guarantee the RF performance of the entire device. Due to the elimination of wire bonding pads on the silicon die, the final TSV trap capacitance (between two central electrodes) is reduced to 3 pF, as compared to the >24 pF of WB counterparts. The on-chip insertion loss is 0.11 dB at a frequency of 50 MHz. Meanwhile, TSV trap features the highest Q factor (22.4) and achieves ~100 times power loss reduction (from calculation) regarding to the WB-HR trap. Also, the finite element modelling is extensively used for the analysis of RF related tests (i.e., to characterize the S-parameter and the power loss of different traps). In addition, circuit modelling is performed to extract the equivalent circuit components of different traps in the resonator test. The results from measurement and modelling are generally in good agreement.

The functionality of the TSV trap is demonstrated by loading and laser-cooling single $^{88}Sr^{+}$ ions. It is found that both heating rate (17 quanta/ms for an axial frequency of 300 kHz) and lifetime (~30 minutes) are comparable with non-cryogenic traps of similar dimensions. The undesired heating issue of TSV trap during ion trapping operation is discussed and the corresponding thermal management solutions are proposed and evaluated. In the last section of this chapter, a customized CPGA design is presented where RDL is patterned and TSV die can be directly bonded, in the absence of a glass interposer. This design can further eliminate

the use of wire bonding and prompt efficient thermal management of ion trap due to its direct contact with CPGA surface (heat sink).

Chapter 5. Multi-module Integrated Surface Electrode Ion Trap

In this chapter, a multi-module integrated surface electrode ion trap is developed. 3D interconnects TSV module, multilayer metallization module as well as silicon photonics module are designed and co-integrated into the ion trap. TSV and multilayer metallization modules are respectively used for flexible electric feedthrough and RF signal shielding, whereas the silicon photonics module is used for on-chip optical addressing. The design of each module is presented first. Next, the fabrication process, especially the steps for photonics layer patterning are highlighted. The post-fabrication electrical (e.g., *I-V*, *C-V*, S-parameter) and optical characterization (e.g., coupling loss) are presented in detail. The deviation between measurement and simulation for photonics components is discussed and several possible causes are proposed.

5.1 Design of Multi-module Integrated Surface electrode Ion Trap

In general, multi-module integrated ion trap (MM trap) uses similar design idea of TSV trap in Chapter 4. Trap die on the top uses silicon as the substrate with more integrated functional components (TSV, multilayer metallization and silicon photonics), whereas a glass interposer with RDL is located underneath. The electrical and mechanical connection in between is built by the micro bumps. A cross-sectional schematic of MM trap is shown in Figure 55.

The electrode geometry of MM trap is identical with that of TSV trap. However, two specific windows (20×20 μm^2) are made onto the central DC electrodes to allow the passthrough of the light emitted from the grating couplers underneath (Figure 55). From the finite element modelling, it is found that these openings have negligible effect to the electric field distribution in the radial plane. The distribution along axial direction at the trapping height is slighted altered (in the range of 0.1 meV). However, this can be compensated by the DC voltages control.

For the interposer design, while the gaps between RDL circuit on the interposer are enlarged to further minimize the leakage, the overall RDL geometry is shrank and becomes more compact. As a result, the overall size of MM interposer is reduced from 8000 × 8000 μm^2 to 4400 × 5600 μm^2.

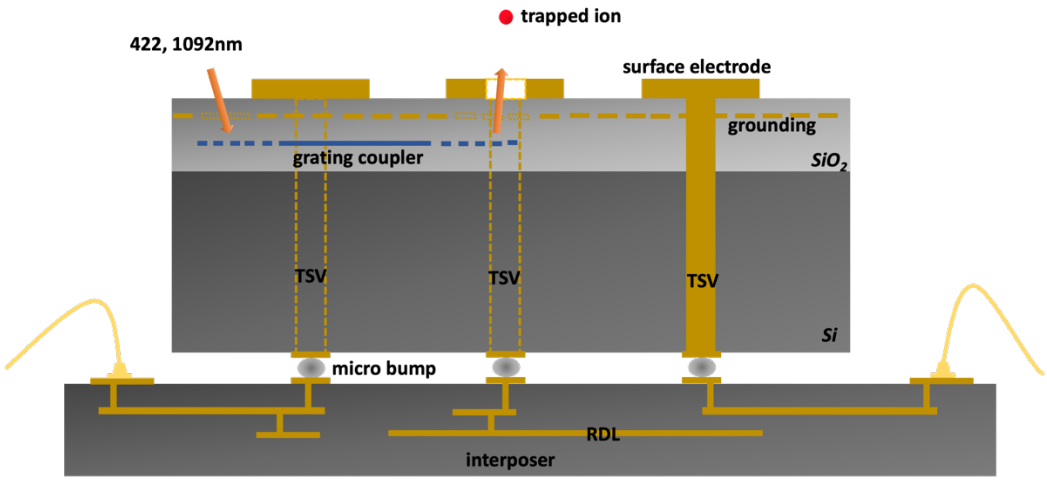


Figure 55. Schematic of the multi-module integrated ion trap. For glass interposer, single layer of RDL is used.

5.1.1 Silicon Photonics Module Design and Modelling

A grating-waveguide-grating structure is built in the photonics layer underneath surface electrode for localized optical addressing. The light is coupled from input fiber to the input grating coupler, routed by the waveguide circuit and finally emitted to the ions by the output grating coupler (Figure 56).

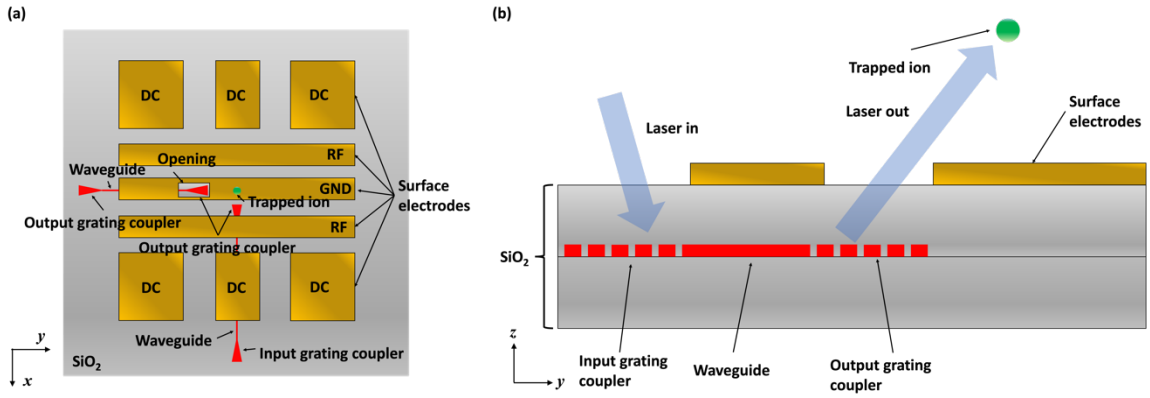


Figure 56. (a) Top view and (b) cross-sectional schematic of the grating-waveguide-grating structure integrated underneath surface electrode.

Before the integration of photonics layer into ion trap, independent photonics components are fabricated and tested [175]. The trial fabrication is carried out on 200 mm silicon on

insulator (SOI) wafer with 220 nm Si core layer and 2 µm buried oxide layer. Two key factors of the grating coupler design are investigated, which are respectively the radius of curvature and the taper shape. In terms of curvature radius, 4 variations are designed (12 µm, 15 µm, 25 µm and 30 µm) with a fixed liner side shape of taper. Meanwhile, three different taper shapes (linear side, inner and outer curved side) are designed with a fixed radius of curvature of 25 µm (Figure 57).

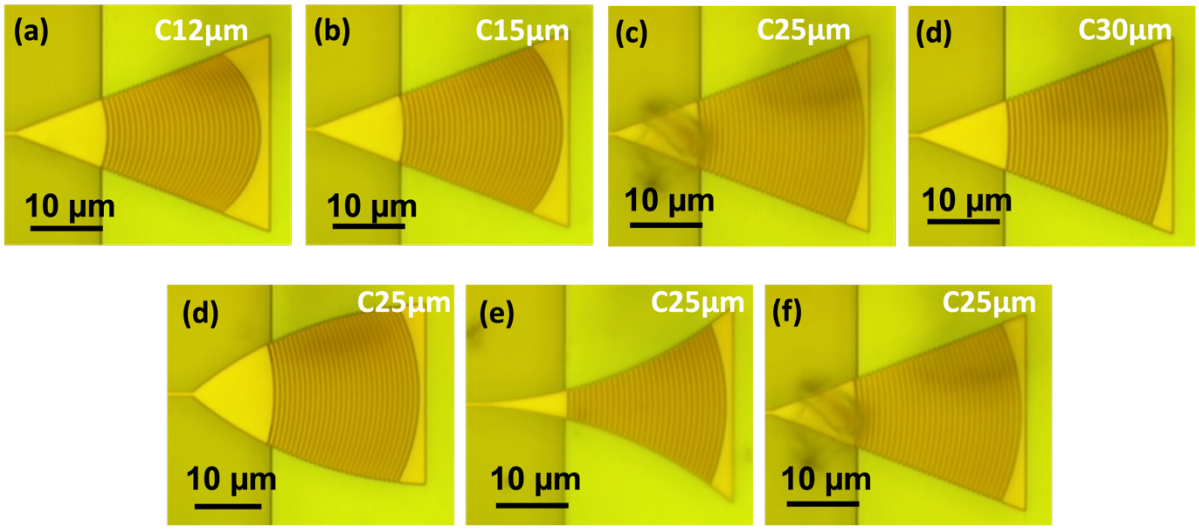


Figure 57. Grating coupler design variations (a-d) on the radius of curvature and (d-f) on the taper shape.

Measurement is performed to evaluate the performance (e.g., coupling efficiency and focused beam size) of various grating designs. First, it is found that the coupling efficiency increases with radius of curvature. The power loss for grating coupler with radius of curvature of 12 µm is 39 dB, which is reduced to 34 dB for coupler with radius of curvature of 30 µm. Meanwhile, the measured beam profile shows that the grating couplers with 25 and 30 µm radius curvature exhibit more focused beam profile (sharper and higher intensity peak) as compared to the 12 and 15 µm counterparts, facilitating the individual addressing of single ions in a long ion string (Figure 58 (a-d)). Simultaneously, the measurement result on the taper shape of grating coupler shows that the coupler with linear side is able to shape a more focused beam, which has a beam size of ~15 × 30 μm^2 at the nominated ion trapping height (~75 µm). In addition, the measurement also indicates that the effect from coupler shape to the coupling efficiency is negligible (<1 dB difference across different shapes).

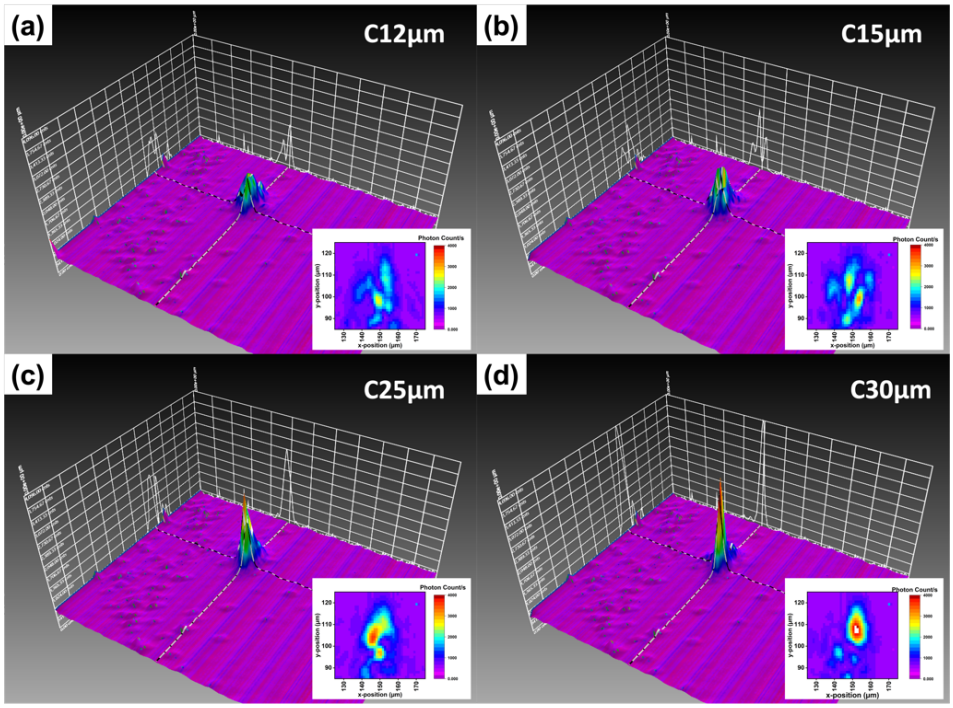


Figure 58. (a-d). Measured beam profile for grating couplers with various radius of curvatures (from 12 to 30 µm). The 2D insets are zoom-in beam profile viewed from the top.

Based on the testing outcomes from the trial fabrication, the design of grating couplers to be integrated into ion trap adopts the 25 µm radius curvature and a taper shape with linear side. Two wavelengths (1092 and 422 nm) are focused. As introduced in Section 1.2.4, the infrared light is used for repumping, whereas the blue light is used for cooling and readout. In addition to the fixed radius curvature and taper shape, two important parameters of grating structure shall be considered: pitch size and duty cycle. The duty cycle is fixed at 0.5 for all grating couplers deign, which means the grating ridge width is half to the pitch size. In terms of pitch size, the pitch is respectively 600 and 1200 nm of input and output grating coupler for light with wavelength of 1092 nm. While for light with wavelength of 422 nm, the corresponding grating pitch size is fixed at 300 nm. The width of waveguide is fixed at 500 nm. The path length of waveguide (from input to output grating coupler) is in the range of several millimetres. The height of all the photonics components is 300 nm (etch-through of SiN core layer). Table X gives a summary on the dimensions of various grating couplers.

At the initial stage, finite-difference time-domain (FDTD) modelling is employed to view the beam path and extract the coupling efficiency based on the abovementioned grating couplers design. The simulated results are also summarized in Table X. The windows position on the surface electrode are determined by the simulated angle of output beam and the

nominated ion trapping height. In addition, the focused beam size and shape are simulated by extending the 2D geometry into 3D in FDTD modelling (Figure 59 (a)). Using light with wavelength of 1092 nm as an example, the obtained beam size at ion trapping height (75 μm) is ~10 × 15 μm^2 (Figure 59 (b)).

Table X. Design parameters and modelled coupling efficiency of grating couplers for different wavelengths.

	Input grating coupler		Output grating coupler	
	Pitch (nm)	**Efficiency**	**Pitch (nm)**	**Efficiency**
1092 nm	600	0.0025	1200	0.5379
422 nm	300	0.0359	300	0.0884

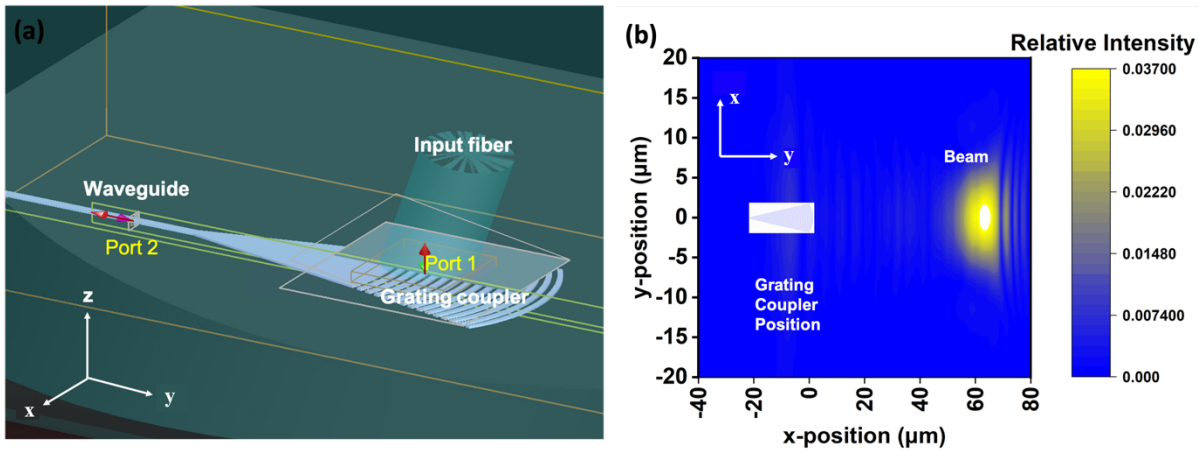


Figure 59. (a) 3D model of grating coupler and waveguide built in FDTD. (b) The beam size and shape for light with wavelength of 1092 nm at the nominated ion trapping height of 75 μm.

5.1.2 3D TSV and Multilayer Metallization Module Design

As mentioned in Chapter 2, both multilayer metallization and TSV have been individually used for flexible electrical feedthrough in ion trap. To simultaneously leverage the advantages (e.g., grounding plane in multilayer metallization, large aspect ratio of TSV) and avoid the drawbacks (e.g., alternated layers formation and planarization in multilayer metallization) of both techniques, the co-integration of TSV and multilayer metallization into ion trap is performed.

As different from TSV trap, for RF electrodes in MM trap, TSVs are only located at one side (5 for each RF electrode), while the TSVs on the other side are eliminated, further reducing the parasitic capacitance and resistance of MM trap (Figure 60). Similarly, for DC electrodes, the TSV number is reduced from 10 or 6 to 4. The TSV diameter, depth and pitch between neighboring TSVs are respectively kept as 20, 100 and 100 μm. Though total TSV number is reduced, more dummy micro bumps are added to facilitate high-efficiency thermal dissipation between the trap die and the interposer. In total, 175 micro bumps are introduced in each MM trap (Figure 60 (a)), as compared to 82 of TSV trap (Figure 60 (b)). Concerning the possible effect from TSV-induced stress onto the photonics performance, the lateral distance between TSV and nearby grating coupler is kept larger than 100 μm (keep-out zone).

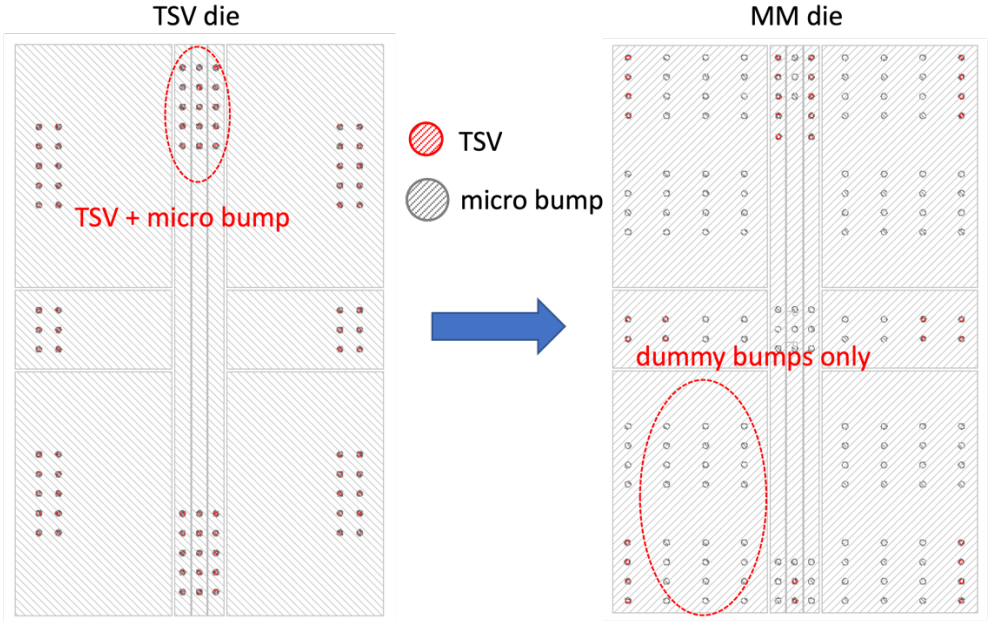


Figure 60. The development from TSV die to MM die. TSV number is reduced, whereas dummy bumps are added in MM die.

As mentioned in Section 2.1.1, for typical trap-integrated multilayer metallization, the bottommost layer is always a grounding plane for RF shielding. Therefore, in the multilayer metallization module, a grounding plane is incorporated into the MM trap as the first step. The grounding plane has a dimension of 2150 × 3150 μm^2, covering the entire surface electrode geometry (1880 × 2920 μm^2). Similar with the grounding plane used in the WB-GND trap (Chapter 3), this grounding plane also adopts a meshed structure to release the stress due to the CTE mismatch between Cu and SiO_2. Meanwhile, since TSV penetrates vertically, circular windows with a diameter of 40 μm are built onto this grounding plane to accommodate the TSV. Also, to allow the transmission of light beam from output grating coupler, square

windows (20×20 μm^2) identical to those on the surface electrodes are also built onto this plane.

5.2 Fabrication Process of Multi-module Integrated Ion Trap

Similarly, the fabrication process of MM trap consists of three parts: the MM die fabrication on Si wafer, the interposer fabrication on glass wafer, and the bonding and alignment of MM die and glass interposer after wafer singulation. The fabrication of MM die adopts a via-middle approach, in which TSV formation is after photonics layer and grounding plane but before surface electrode. The detailed fabrication process of different modules is given in sequence.

5.2.1 Fabrication Process of Photonics Layer

Since the photonics components are very sensitive to the fluctuation of wafer flatness, the photonics layer is located at the very bottom in the MM die (right next to the Si substrate). First, a 3 μm SiO_2 layer is deposited on the Si substrate at 400 ℃ with low stress. A CMP of ~0.1 μm SiO_2 is carried out to planarize the layer surface. This SiO_2 layer is used as the bottom cladding layer for the integrated photonics. Next, a 0.3 μm SiN layer is deposited onto the SiO_2 as the core layer. To pattern the photonics components with small feature size (~150 nm), a tri-layer lithography technique is used (Figure 61). Bottom anti-reflective coating (BARC) layer, Si containing anti-reflective coating (SiARC) layer and photoresist are coated onto the SiN layer in sequence. After the development of photoresist, SiARC layer (0.03 μm) is first etched. Once the complete exposure of the BARC layer underneath is confirmed with energy-dispersive X-ray spectroscopy (EDX), subsequent BARC layer etching is performed. The BARC layer is a 0.25 μm spin-on-carbon (SoC), as a hardmask for the subsequent SiN etching. Again, EDX is required to confirm the SiN layer is fully exposed. Finally, the 0.3 μm SiN core layer is etched through.

After the PRS and cleaning, the SEM images of the output grating couplers designed for different wavelengths (1092 and 422 nm) are captured. As shown in Figure 62, the grating ridges are well defined and have a good uniformity. Three-dimensional atomic force microscope (3D-AFM) is also used to characterize the planar surface and sidewall roughness (Figure 63). Measurements are performed at five different sites (four corners and one center)

across the whole wafer. The averaged roughness R_a of planar surface (exposed SiO_2) is 0.5 nm, whereas the sidewall roughness R_a is 1.7 nm (2.7 nm) for 1092 nm (422 nm) grating coupler. After these morphological characterizations, another 3 μm SiO_2 layer is deposited as the top cladding layer. A CMP (~0.3 μm SiO_2) is added to remove the mapped pattern and planarize the surface simultaneously.

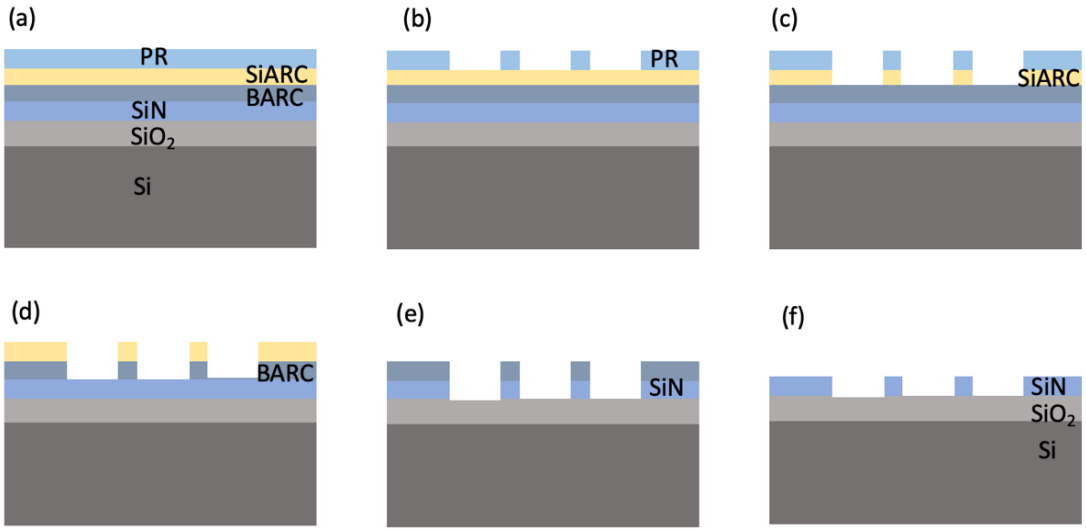


Figure 61. Tri-layer lithography process and the subsequent etching of SiN layer. (a) BARC layer, SiARC layer and PR layer are coated onto the SiN layer in sequence. (b) The pattern of PR after exposure and development. (c) The pattern of SiARC after the first etching defined by PR. (d) The pattern of BARC after the second etching defined by SiARC. (e) The pattern of SiN after the third etching defined by BARC. (f) PRS of the BARC layer.

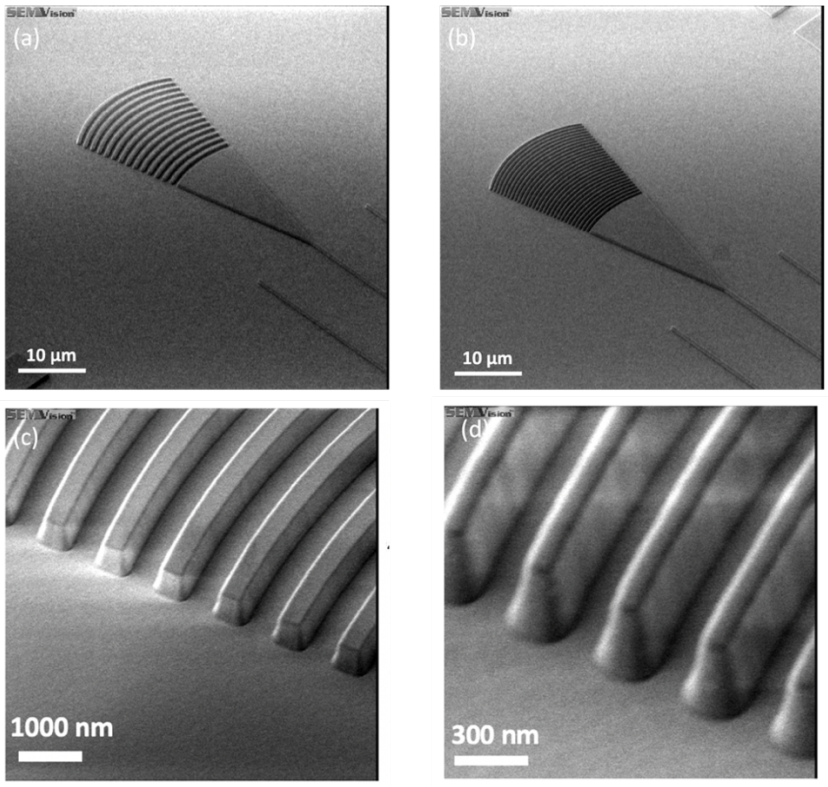


Figure 62. SEM images of the output grating couplers with wavelength of (a) 1092 nm and (b) 422 nm. Zoom-in SEM images for the output grating couplers with wavelength of (c) 1092 nm and (d) 422 nm.

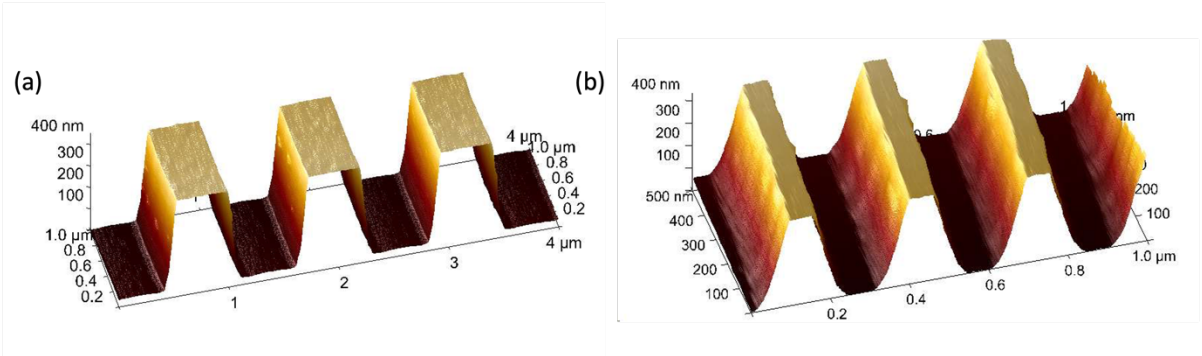


Figure 63. 3D AFM images of the output grating couplers with wavelength of (a) 1092 and (b) 422 nm.

5.2.2 Fabrication Process of Grounding Plane

As illustrated in Section 3.2.2, Cu damascene process is adopted to form the grounding plane in MM trap. The 2.7 µm SiO_2 (3 µm – 0.3 µm) is first etched by ~1 µm with lithography defined patterns. As mentioned earlier, a meshed structure together with specific windows for TSV penetration and light transmission are required for the grounding plane patterning (Figure 64 (a)). After that, adhesion (Ti) layer and seed (Cu) layer are deposited. ECP of Cu is performed with subsequent 30 minutes annealing in N_2 environment. CMP is then used to remove the Cu overburden (Figure 64 (b, c)) as well as the Ti and Cu layers. Figure 64 (a) and (b) show the excellent alignment between the grounding plane windows and the grating couplers underneath. Figure 64 (c) shows the windows (diameter of 40 µm) designed to accommodate the TSV. Finally, a capping layer (0.2 µm SiN) is deposited to protect grounding plane from oxidization.

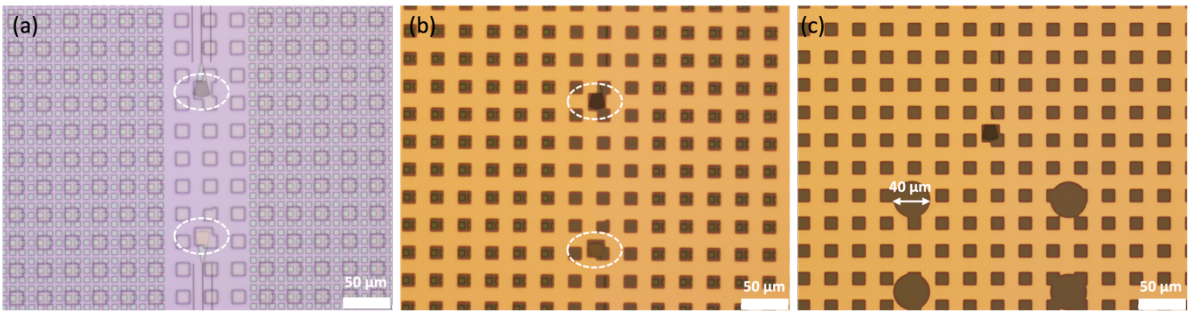


Figure 64. Optical images of the alignment between grounding plane windows and grating couplers (a) before and (b) after the ECP of Cu. (c) Windows on the grounding plane designed to accommodate the TSV.

5.2.3 Fabrication Process of TSV and Surface Electrode

Another 3 μm SiO_2 is deposited, which is used as the insulation layer between surface electrode and grounding plane. Again, to planarize the wafer, CMP of 0.2 μm SiO_2 is performed after the deposition. Next, the lithography for TSV (coating of PR, exposure and development) is carried out. Indeed, the entire fabrication process for TSV formation and surface electrode patterning is quite similar with that illustrated in Section 4.2.1. However, some new features shall be highlighted.

The first is related to the via etching process. Before the 100 μm blind via etching into the Si substrate, the etching of 2.8 μm SiO_2, 0.2 μm SiN and ~5 μm SiO_2 layer is conducted in sequence, from top to the bottom. At each step in between, EDX is required to confirm the bottom layer is fully exposed. Also, trial run on dummy wafers before critical steps is required for the MM trap fabrication due to the relatively intricate fabrication steps. For example, to confirm the feature size uniformity and avoid undesired issues related to the TSV etching process, a cross-sectional SEM is performed on the dummy wafer (i.e., no photonics layer and grounding plane) once the trial run of TSV etching completes. The image in Figure 65 (a) shows an ideal anisotropic etching profile and the diameter of the via is kept at 20 μm along the vertical direction. However, the resultant TSV depth is >100 μm. Therefore, the etching time for device wafers fabrication is adjusted accordingly. The optical image of formed TSV in the device wafer is shown in Figure 65 (b), from which a good alignment between TSV and grounding plane windows can be observed.

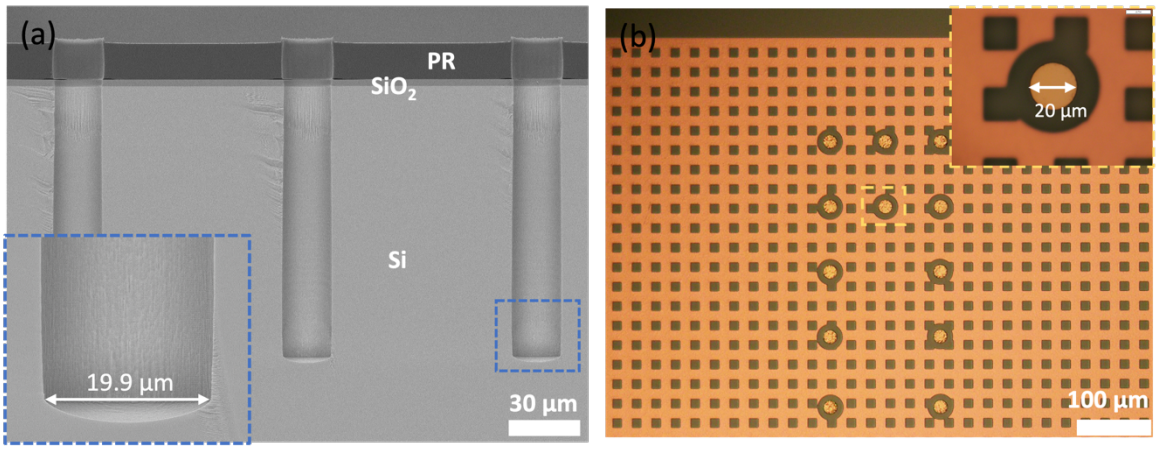


Figure 65. (a) Cross-sectional SEM image of etched blind via on the dummy wafer. The inset shows the diameter of via bottom. (b) Optical image of Cu-filled via and the alignment with grounding plane. The inset shows the diameter of via top after Cu filling.

The second feature is related to the SiN etching (capping layer) process. After the patterning of 2.8 µm SiO_2 insulation layer underneath surface electrode, an individual 0.2 µm SiN etching is performed. This is to simultaneously etch the SiN layer on top of the exposed grounding plane and the SiN layer covering the Cu via. The etching time shall be carefully controlled, since any dielectric residue may lead to electron charging during ion trapping operation or the open circuit between TSV and electrode. On the other hand, the over etch on the grounding plane surface may rough the Cu surface and make it susceptible to oxidization. Again, EDX is used to confirm that the Cu surface of both grounding plane and via core are fully exposed before the patterning of surface electrode. In addition, special attention shall be paid to the adhesion and seed layers etching process at the windows region (after both grounding plane and surface electrode ECP). Any metal residue can obstruct the optical path, which is not acceptable for ion addressing.

Eventually, the fabricated wafer frontside is shown in Figure 66 (a), from which the silicon photonics module, the grounding plane module underneath surface electrode can be viewed directly. Figure 66 (b) highlights the alignment between the windows on the surface electrode and the grating couplers underneath. Meanwhile, the cross-sectional SEM images in Figure 58 show the TSV connecting with surface electrodes and the good compatibility between TSV and grounding plane.

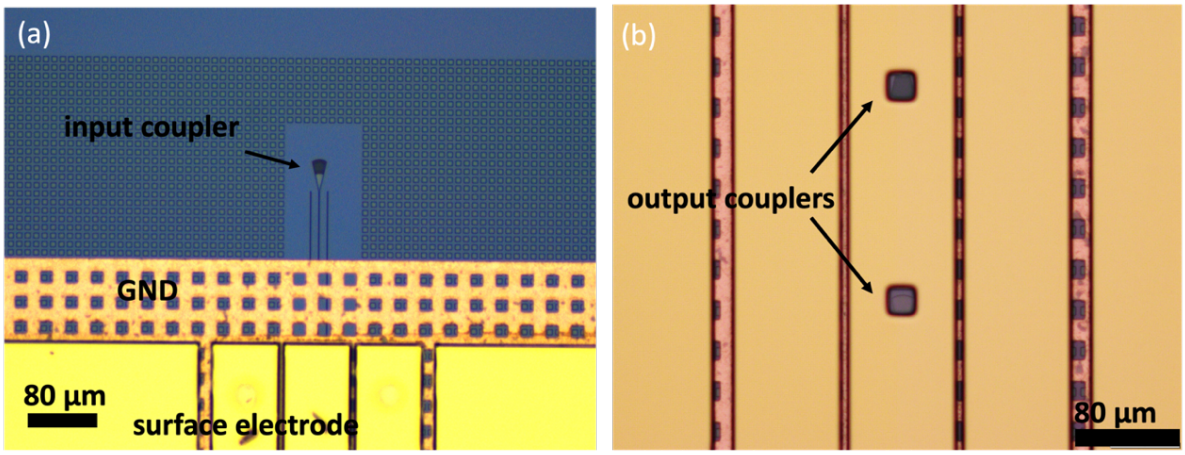


Figure 66. (a) Optical image of fabricated MM die frontside. The grounding plane and the silicon photonics modules are integrated underneath surface electrode. (b) Surface electrode (central DC electrode) with two windows on top of grating couplers for light transmission.

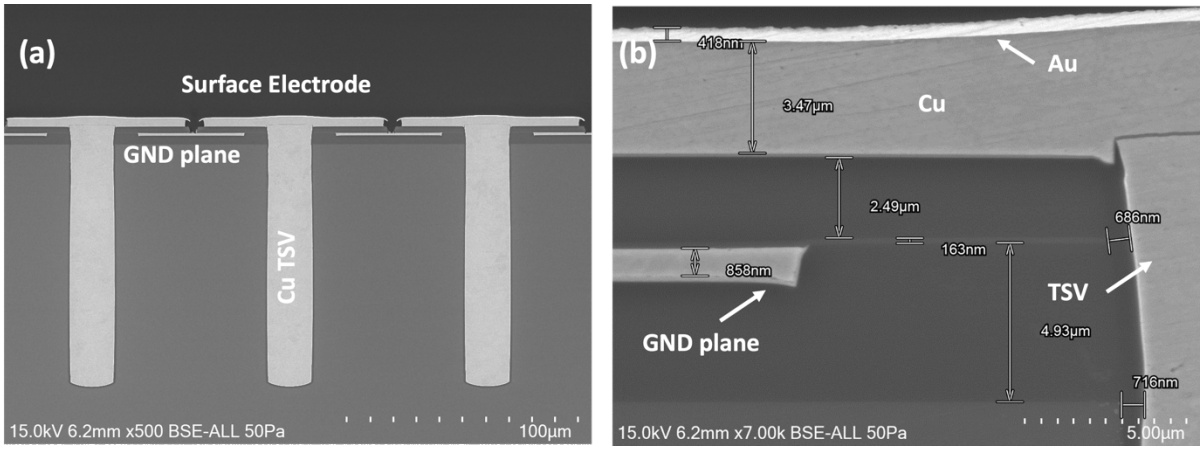


Figure 67. (a) The cross-sectional SEM image of overall structure that integrates TSV and grounding plane underneath surface electrodes in MM die. (b) The zoom-in cross-sectional SEM image illustrating the electrode dimensions and distances between modules. Note no photonics pattern exists at this cross-sectional region.

5.2.4 Fabrication Process of Wafer Backside and Glass Interposer

The fabrication process of wafer backside is identical with that illustrated in Section 4.2.1. In the beginning, two steps of TSV revealing are performed. The first is to reveal the TSV using Si etching, right after wafer grinding. In this step, some over etch on the Si substrate is required to confirm that TSV stretches out the backside surface. Multiple steps of etching and DRSEM verification are required. As shown in Figure 68 (a) and (b), the exposed TSV height is increased from ~0.5 µm to ~4.5 µm after repetitive Si etching. The second is to reveal TSV using CMP after backside insulation layer (3 µm SiO_2) deposition. The polishing time shall be moderately extended to completely planarize the Cu pillar. Subsequently, three steps of lithography are required, to respectively define the backside RDL plating, the passivation layer opening, and the micro bump plating. Since more dummy bumps are added as mentioned earlier, the backside RDL and passivation layer patterning shall be revised accordingly. Before and after the RDL and micro bump plating, two steps of adhesion and seed layers deposition and etching are performed.

The entire fabrication process of MM die on Si wafer is elaborated step by step in Figure 69. The fabrication process of glass interposer and the bonding between MM die and interposer are similar with the process described in Section 4.2.2.

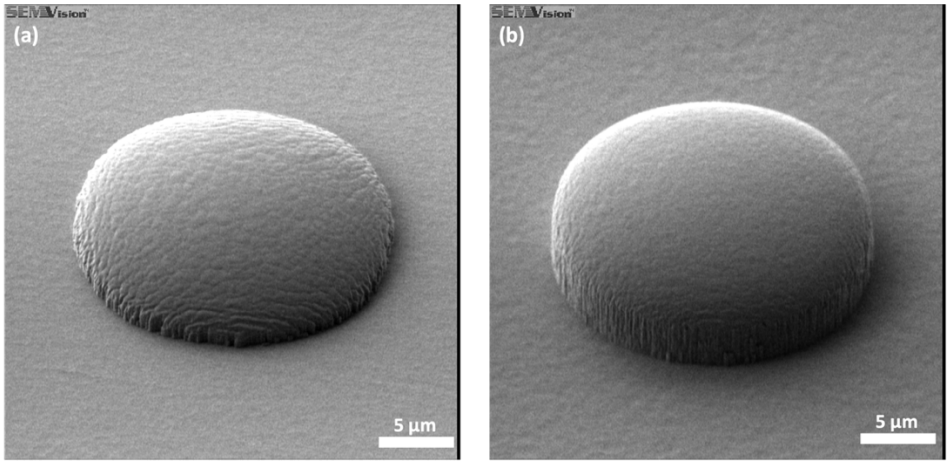


Figure 68. Backside TSV revealing by Si substrate etch. (a) Initial etch of Si substrate to reveal the TSV by ~0.5 µm. (b) Further etch of Si substrate to reveal the TSV by ~4.5 µm.

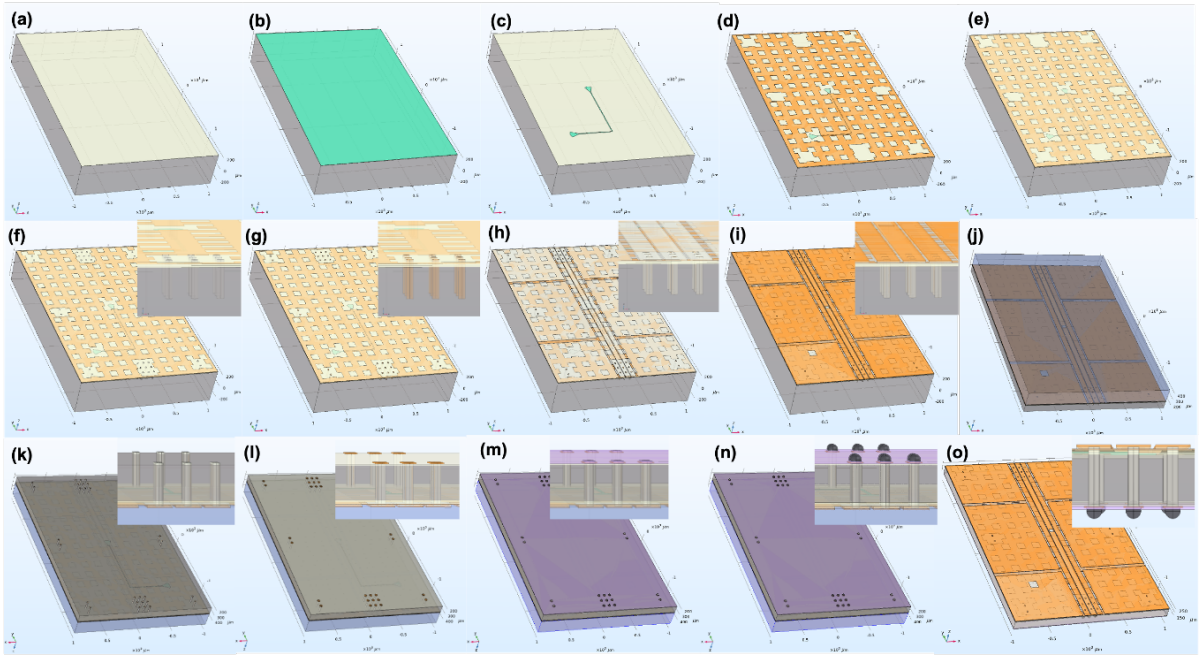


Figure 69. Fabrication process of MM die (trap chip in MM trap). (a) 3 µm SiO_2 deposited onto Si wafer as the bottom cladding layer for photonics components. (b) 0.3 µm SiN deposited onto SiO_2 as the core layer for photonics components. (c) Patterned photonics components on the SiN layer. (d) Formation of grounding plane on top of photonics layer after ECP and CMP. (e) 0.2 µm SiN layer (capping layer) and 3 µm SiO_2 deposited onto grounding plane. (f) Blind via etched into Si substrate. (g) Cu-filled TSV after barrier and seed layer deposition, ECP of Cu and CMP. (h) Patterning of insulation layer (SiO_2) between surface electrode and grounding plane. (i) Patterning of surface electrode. (j) Temporary bonding of the device wafer onto a handling wafer for wafer backside processing. (k) Revealed TSV after backside grinding and etching of Si substrate. (l) Backside RDL patterning after the SiO_2 insulation layer deposition and TSV revealing process. (m) Backside passivation layer (HD8930) patterning. (n) Plated micro bumps on the wafer backside. (o) De-bonded device wafer from handling wafer.

5.3 Electrical and Optical Characterization of Multi-module Integrated Ion Trap

The following electrical test results (*I-V*, *C-V* and S-parameter) are based on the wafer or die frontside (before the wafer grinding and backside fabrication process). The optical testing is performed right after the photonics layer fabrication.

5.3.1 DC Test

The first DC test is to measure the leakage current between neighboring electrodes. A wafer level *I-V* test is performed once the wafer frontside fabrication completes. As illustrated in Section 3.3.1, the leakage current is measured between RF electrode and central DC electrode. The applied voltage is from 0 to 100 V with a 1 V step. Every single die across the whole wafer is tested. In total, 67 individual tests are performed. The obtained wafer resistance map (Figure 70 (a)) demonstrates that a minimum resistance of the order of 10^{11} ohm is achieved, indicating the adhesion and seed layer in the narrow gaps between electrodes are completely etched. A good albeit not perfect uniformity across the whole wafer is observed.

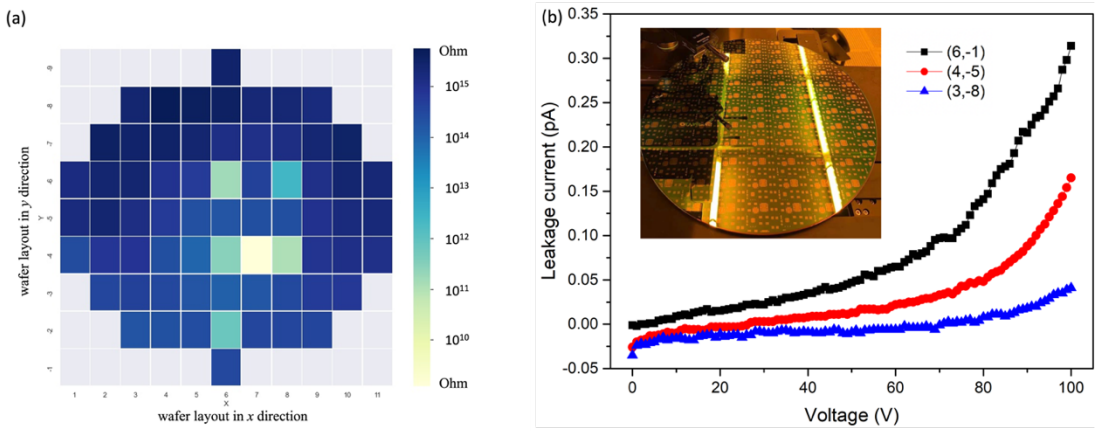


Figure 70. (a) Resistance map of dies across the whole wafer. Most samples have a resistance of the order of 10^{13} ohm. (b) *I-V* curves of three dies that are at different sites on the wafer. Numbers in brackets are wafer coordinates of dies. Inset: Fabricated MM die on a 12-inch silicon wafer (frontside completed).

In addition, the possible leakage between TSV and the grounding plane is investigated. In this test, one probe is contacted with the exposed grounding plane, and the other probe is contacted with neighbouring surface electrode in connection with TSV. It is found that the average resistance is at the order of 10^{12} ohm, indicating a good insulation between different

modules. To evaluate the reliability of TSV liner, the leakage of single TSV is also measured using the setup illustrated in Section 4.3.1. A similar result is obtained (the leakage current into Si substrate of single TSV is $<10^{-11}$ A), since the in-via SiO_2 deposition recipe and the formed TSV liner thickness (0.75 μm SiO_2) are basically maintained.

Another important DC metric of ion trap is the capacitance. Again, the MOS capacitance of single RF electrode is first measured. Based on the developed MOS capacitance model in Section 4.3.2, single TSV has a MOS capacitance of 0.32 pF at the accumulation regime. Due to the elimination of 5 TSVs, it is therefore speculated that the MOS capacitance of single RF electrode on MM die will correspondingly be reduced by ~1.6 pF, as compared to that on TSV die. As shown in Figure 71, the measurement result demonstrates a decent agreement with the speculation, especially at the accumulation regime. The small capacitance difference at the depletion regime is largely due to the capacitance reduction of TSV after the depletion layer formation (see Section 4.3.2).

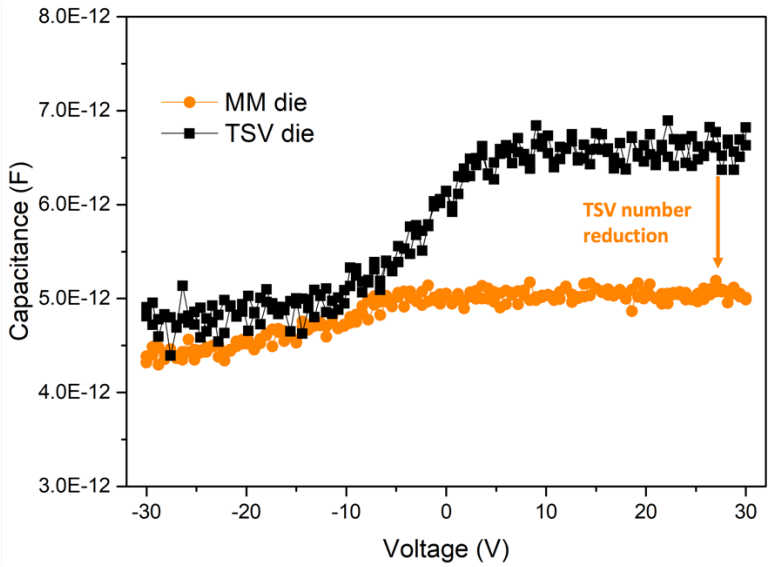


Figure 71. The MOS capacitance comparison of single RF electrode on MM die and TSV die.

Similarly, the capacitance between RF and central DC electrodes are also measured using the setup illustrated in Section 3.3.2. It is found that the capacitance of MM die is reduced to ~0.75 pF (Figure 72 (a)). Individual measurements are performed on 15 different MM dies, and a good repeatability is observed (Figure 72 (b)). Though the capacitance from wafer backside is not taken into account and the MM die has not been connected to the interposer, it can be anticipated that the capacitance of final MM trap can be further reduced. Again, this reduction is largely due to the elimination of TSVs at one side of central electrodes.

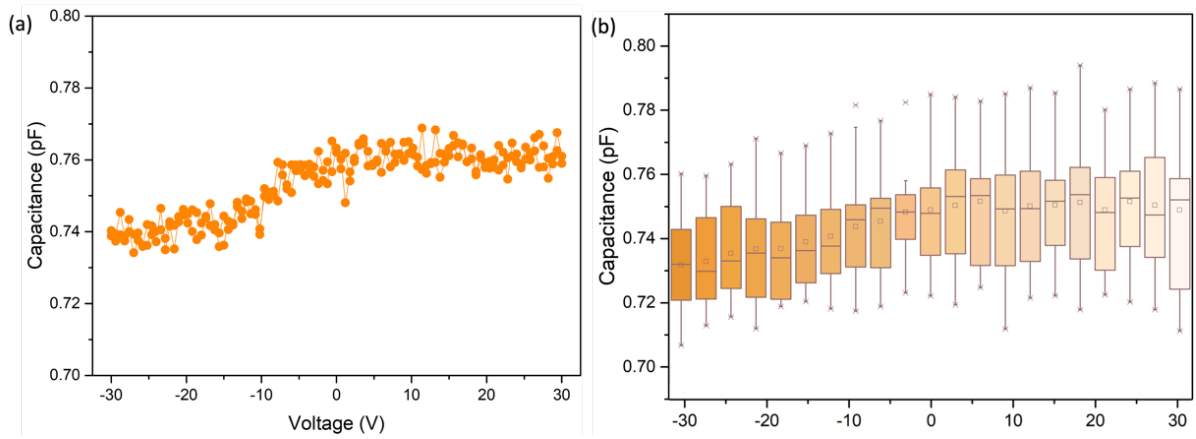


Figure 72. (a) The capacitance of MM die as a function of voltage. (b) The statistics capacitance distribution across 15 MM dies.

5.3.2 RF Test

The on-chip insertion (S21) and reflection loss (S11) of MM die are measured with the setup illustrated in Section 3.3.3. To provide a fair comparison, the S-parameter of TSV die frontside (before the wafer thinning and backside fabrication process) is also obtained. As shown in Figure 73 (a), the insertion (reflection) loss is further reduced to 0.06 dB (34.8 dB) of MM die, at a frequency of 50 MHz. This reduction can be attributed to the incorporation of grounding plane as well as the partial elimination of TSV connecting with RF electrodes. In addition, the insertion loss distribution across 5 different MM dies at different frequency is plotted in Figure 73 (b). While the discrepancy becomes significant when the frequency is higher than 120 MHz, it is maintained small in the normal ion trapping operation frequency range (tens of megahertz).

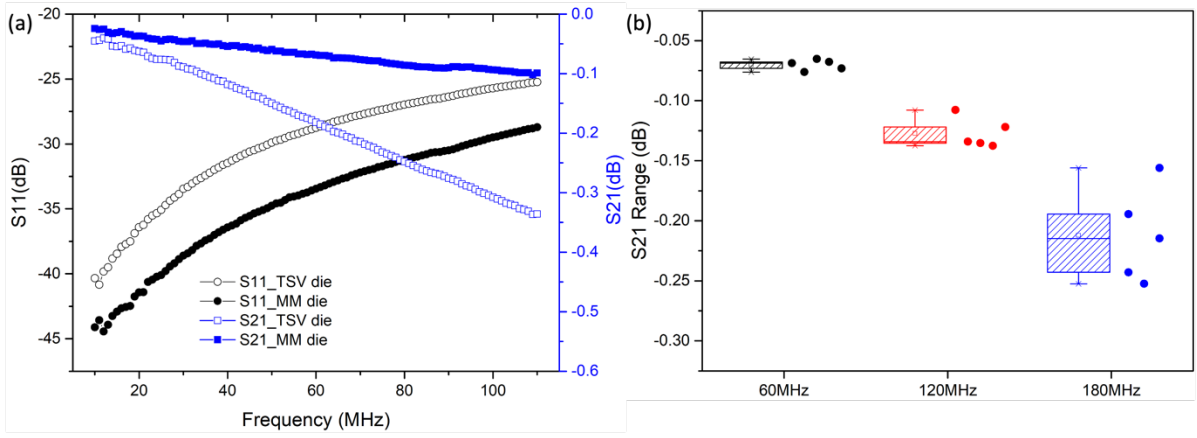


Figure 73. (a) S-parameter comparison of MM die and TSV die. (b) Statistics summary for the insertion loss of MM die across 5 different dies at different frequency (up to 180 MHz).

5.3.3 Optical Measurement

A. Setup

Optical measurement can be performed onto individual grating-waveguide-grating photonics structures, as mentioned in Section 5.1.1. The setup of measurement system is shown in Figure 74. Laser beam (10 dBm, 422 nm) from input fiber is coupled into the input grating coupler via the tip of a perpendicularly cleaved bare fiber. The coupled laser light is then propagating through waveguide, and emitted out from the output grating coupler, as illustrated in Figure 56, and coupled into the output fiber. The power of emitted beam from the output grating coupler is then measured by power meter via output fiber. To optimize the coupling efficiency, the position, and the vertical height of fiber tip to the sample can be adjusted. At the same time, a 3-panel polarizer is used to optimize polarization of the laser light to achieve minimized coupling loss. To capture the output beam profile, the output fiber will be moved away from the sample. Following that, the beam profiler will be placed on top of the sample to capture the profiles of the light beam emitted from the output grating coupler, as illustrated in Figure 74, where the beam profiles can be presented in both 2D and 3D form as shown in Figure 58. In a typical beam profile measurement as of Figure 58, a × 6.5 adjustable magnifying lens with × 5 optical adapter is used to fit the beam spot into the sensing area of the beam profiler. The height of the beam profiler is then adjusted to obtain a sharp beam spot, as shown in Figure 58.

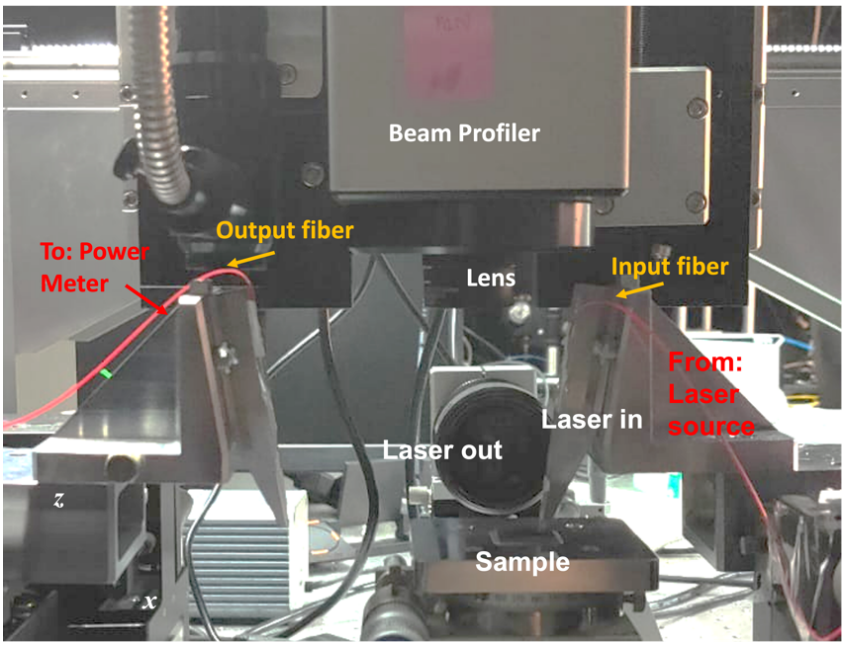


Figure 74. Setup of coupling efficiency and beam profile measurement system.

B. Results and Analysis

For power loss measurement, the inclination angle of input fiber to the normal of the sample chip is fixed at 10°. Meanwhile, the inclination angle of output fiber is adjusted from 8 – 11°. The loss from input to output grating couplers ranges between 35.27 – 39.67 dB, with optimal loss of 35.27 dB at 9.5°. The obtained losses are basically in line with the simulated outcomes (considering the fabrication imperfection and waveguide loss), where the coupling efficiencies of input and output gratings are 0.0359 and 0.0884, respectively, which corresponds to 25 dB loss in total (Table X). However, for 1092 nm laser, the measured power loss is ~50 dB, which is ~20 dB higher than that from simulation. The low coupling efficiency of 1092 nm can be attributed to several reasons. From the experimental point of view, the readily available 1092 nm laser has a low output power of ~1 dBm, which is much lower than 422 nm laser which can deliver 10 dBm power. Apart from that, there are also implicit factors in affecting the measured power loss, and the corresponding coupling efficiency of the grating.

Fundamentally, the coupling of light into grating structure requires fulfillment of Bragg condition, as indicated:

$$n_{eff} - n_c \cdot sin\,\theta = \frac{m\lambda}{\Lambda} \qquad (32)$$

For m_{th} order of diffraction, n_c, n_{eff}, θ, λ, and Λ denotes the effective index of the fibre mode, effective index of the grating, diffraction angle, wavelength, and pitch, respectively [176]. Thus, it is implied that the specific pitch size, Λ, is required to match with its corresponding wavelength, λ. However, in actual fabrication of grating coupler, the profile of the grating structure is not vertically straight, with slight trapezoidal profiles as shown in Figure 62 and Figure 63. As a result, the pitch varied with various etch depth levels within the grating, where Bragg's condition is not entirely fulfilled. At the same time, it has also been reported that trapezoidal profiles reduce output coupling efficiency of up to 96% on SOI platforms due to the abovementioned mismatch [177].

Besides trapezoidal profiles, other possible source of loss is the scattering of light from sidewall roughness. It has been reported that the main source of propagation loss in waveguide is the sidewall roughness, where similar loss mechanisms are also found in the coupling of light into grating structure. To reduce the dominance of propagation loss due to sidewall roughness scattering, the width of the waveguide can be enlarged, where in our case 0.5 μm waveguides are used for both 1092 and 422 nm measurements. Nevertheless, the sidewall

roughness obtained from Figure 63 range between 1.7 to 2.7 nm, which is acceptable in terms of minimizing scattering loss. The obtained 1.7 and 2.7 nm roughness can be benchmarked against a prior study reported by Grillot et al., where for a 150 × 150 nm waveguide cross section with roughness parameters $\sigma = 2$ nm, $L_c = 50$ nm, propagation loss of 0.5 dB/cm is expected [178]. Nevertheless, most studies on the effect of surface roughness on propagation loss is carried out on SOI platforms in telecommunication wavelengths, where studies on SiN platforms on 422 and 1092 nm are limited. Thus, further studies are needed.

Apart from that, some existing issues in measurements shall be resolved. First, the current inclination angles of measurement system are in the range of 10°, which may not match with the fabricated 1092 nm grating couplers. A larger range (~30°) for angle adjustment is required. Meanwhile, the beam profiles in *y-z* plane are needed. The beam profile measured in Figure 58 is based on focused beam produced by 3-mm focal length magnifying lens. By adjusting the focusing of the beam profiler, the corresponding height of the obtained beam can be estimated. However, to perform accurate optical addressing, on trapped ion, beam profiling in *y-z* plane is needed, as shown in Figure 56. To obtain this, an automated stage is needed to elevate the beam profiler in small steps, usually 1 μm, with corresponding beam profile captured in each step. By compiling the obtained beams, the *y-z* profiles can be obtained.

5.4 Summary

In this chapter, a novel surface electrode ion trap is presented, where TSV, multilayer metallization and silicon photonics are monolithically integrated, that are respectively used for flexible electric feedthrough, RF signal shielding, and on-chip ion addressing. In the module of silicon photonics, two sets of input grating-waveguide-output grating photonics circuit are designed for light with wavelength of 422 and 1092 nm. The intricate fabrication process on 12-inch wafer platform is presented in detail. The compatibility between TSV/multilayer metallization and waveguide/grating coupler for electrical and optical signal routing is demonstrated. The electrical and optical performances are characterized and benchmarked. As compared to the TSV die in Chapter 4, the capacitance of multi-module integrated (MM) die is further reduced to 0.75 pF, due to the partial elimination of TSV at one side of RF electrode. Meanwhile, with the shielding effect of grounding plane, the on-chip insertion (0.06 dB at frequency of 50 MHz) and reflection loss (34.8 dB) are both minimized. In addition, the wafer level *I-V* test indicates that good insulation between neighboring electrodes is achieved. In optical test, considering the fabrication imperfection and the loss from waveguide, the

measured power loss (35.27 dB) of light with wavelength of 422 nm is basically consistent with the simulation result (25 dB). However, for light with wavelength of 1092 nm, the measured power loss is as high as 50 dB. This can be attributed to the etched trapezoidal profiles of grating. The mismatch of inclination angles may also play a role. At the time of this thesis writing, the backside fabrication of MM die is ongoing. Once completed, the ion trapping test will be performed.

Chapter 6. Conclusion and Future Work

6.1 Conclusion

In this thesis, a comprehensive study is presented to boost the scalability of surface electrode ion trap, via integrating 3D interconnects TSV and other function modules (i.e., silicon photonics and multilayer metallization) into the trap.

In Chapter 3, the surface electrode ion traps on three different substrates (i.e., high resistivity silicon, silicon with grounding plane and glass) with two size variations are designed, fabricated, tested and compared. It is found that the ion trap on glass substrate demonstrates the best RF performance, including low insertion loss of <0.05 dB (RF frequency of 50 MHz) and high resonance peak of -30 dBm, though the leakage current between neighboring electrodes is relatively high (of the order of 10^{-10} A). The $^{88}Sr^{+}$ ions trapped by this glass trap has a lifetime of 30 minutes and up to four ions are simultaneously confined.

In Chapter 4, the idea to integrate 3D interconnects TSV into ion trap is discussed in detail. TSV is integrated underneath electrode surface, in place of wire bonding that extends out, enabling electrode geometry design with high flexibility. A glass interposer with redistribution layer is placed beneath TSV integrated trap. Standard CMOS back-end-of-line process with 12-inch wafer processing platform is used for the TSV trap fabrication. The electrical performance of TSV integrated ion trap is evaluated from multiple metrics. The results show that TSV integrated trap features smaller capacitance (3 pF), lower on-chip insertion loss (0.11 dB at 50MHz) and lower post-packaging power loss (0.3 W from simulation), with regard to those traps on silicon substrates (without TSV) developed in Chapter 3. Meanwhile, an analytical model is built to characterize the trap capacitance. The power losses calculated from the developed circuit model is in good agreement with those from numerical simulations. Ions are successfully confined by the TSV integrated ion trap with a similar lifetime of 30 minutes. The measured heating rate is 17 quanta/ms for an axial frequency of 300 kHz, which is in favorable comparison to the non-cryogenic traps with similar dimensions. In addition, various solutions to temperature increase control of TSV integrated ion trap are proposed and evaluated. Finally, a customized CPGA is designed and fabricated, where redistribution layer is patterned and TSV integrated trap can be directly bonded, eliminating the use of glass interposer.

In Chapter 5, to make a step forward, a multi-module integrated ion trap is demonstrated based on the promising results of TSV integrated trap. In addition to TSV, multilayer metallization and silicon photonics (waveguide and grating coupler circuits designed for lights with wavelength of 422 and 1092 nm) are integrated into ion trap, which are respectively used for silicon substrate shielding and on-chip optical addressing. Similar electrical tests are performed on the wafer frontside of this multi-module integrated ion trap. The capacitance and insertion loss are further reduced to ~0.75 pF and 0.06 dB (RF frequency of 50 MHz). In terms of optical test, the measured power loss for light with wavelength of 422 nm is 35.27 dB, slightly higher than the simulation result (25 dB). However, for light with wavelength of 1092 nm, the measured loss is up to 50 dB. This is partially due to the undesired trapezoidal profile of grating structure and the mismatch of inclination angles between measurement system and fabricated grating coupler.

On the one hand, this work enriches the flexible interconnection toolbox of ion trap device by integrating TSV in the half space underneath surface electrodes. The comparable ion trapping performance of TSV integrated trap indicates the excellent compatibility of TSV (including material, process, assemble and packaging) to the ion trapping test environment. On the other hand, due to the limitations of back end fabrication process, the obtained grating coupler profile (feature size of ~100 nm) is not ideal, leading to a poor coupling efficiency. A combination of front end (for silicon photonics) and back end process (for TSV and surface electrode) is required. In addition, to facilitate high-accuracy off-chip light alignment with ions, the thermal stability of TSV integrated trap should be improved in the future, where grounding plane or interposer with high thermal conductivity can be a favourable option.

6.2 Future Work

6.2.1 Design and Modelling of Ring Trap and Point Trap

The ion trap with concentric circular electrodes is able to confine a ring-shaped chain of ions due to the circularly symmetric RF pseudopotential (ring trap) [179]. As different from the liner trap, DC electrodes in the ring trap are exclusively used for electric field compensation, not for the axial confinement. This can minimize the undesired micromotion. Ring trap is attractive in quantum simulation due to the unique circular symmetry. Furthermore, the demonstrated translational invariance in ring trap opens a door towards many-body physics [60, 180]. In addition, in the field of quantum computing, ring trap is also suitable to be used as a

quantum memory due to its capability in terms of large-scale ion storage. In a work reported in 2015, a ring trap with a diameter of <2000 μm successfully confined an ion ring with ~400 Ca^+ ions (average separation of ~9 μm between ions) [57].

In addition to confine a ring-shaped ion chain, ring trap can also be used to trap single ions by simply modifying the potentials of concentric electrodes (point trap) [181]. The vertical ion-electrode distance can be even in-situ tuned (without excess micromotion). The applications of point trap include the investigation of anomalous heating as the function of ion-electrode distance, large array of single ions in independent traps for quantum processor and two-dimensional lattice of interacting ions for quantum simulation.

In this section, a simplest circular trap design consists of four concentric electrodes is provided. The two operation modes (ring trap or point trap) are respectively demonstrated. The radius of four concentric electrodes is respectively 60, 110, 200 and 600 μm. The gap width between electrodes is 6 or 15 μm. As a ring trap (Figure 75 (a)), the 1st and 3rd (from centre to periphery) electrodes are set as RF electrodes, while the others are kept as ground. Applying an RF signal with amplitude of 100 V and frequency of 60 MHz in the modelling, the generated electric field is extracted, as shown in Figure 75 (b, c). A ring-shaped RF null is formed above the trap surface. The diameter of formed ring-shaped ion chain is ~160 μm and the vertical ion-electrode distance is ~55 μm. The obtained circular trapping depth is ~400 meV, while the vertical trapping depth is ~50 meV (Figure 75 (d, e)). As a point trap (Figure 76 (a)), the 2nd electrode is set as RF electrode, while the else are kept as ground. In this case, a single RF null is formed right at the trap centre but above the trap surface with a height of ~50 μm (Figure 76 (b, c)). By applying a RF signal with same phase but different amplitude onto the 1st electrode, the height of RF null can be in-situ tuned. For example, when the RF amplitude of 1st electrode increases from -40 to 40 V (the RF signal of 2nd electrode is kept with 100 V amplitude and 60 MHz frequency), the trapping height is correspondingly reduced from >80 to 20 μm (Figure 76 (d)). It should be highlighted that the obtained ion-chain diameter and trapping height are determined by the demonstrated geometry parameters. However, there is large parameter space in terms of electrode radius, gap width between electrode, RF amplitude, frequency, etc. Therefore, a more systematic design procedure is in demand.

Previously, two challenges restricting the circular trap development are the interconnection and optical addressing. The concentric geometry means that inner electrodes are always encircled by outer electrodes, which cannot be accessed by the wire bondings from periphery.

Meanwhile, the beam width from free-space laser is often incompatible with the ring-shaped ion chain diameter, complexing the optical addressing. However, as mentioned earlier, with the integration of TSV and silicon photonics, the challenges can be fundamentally solved.

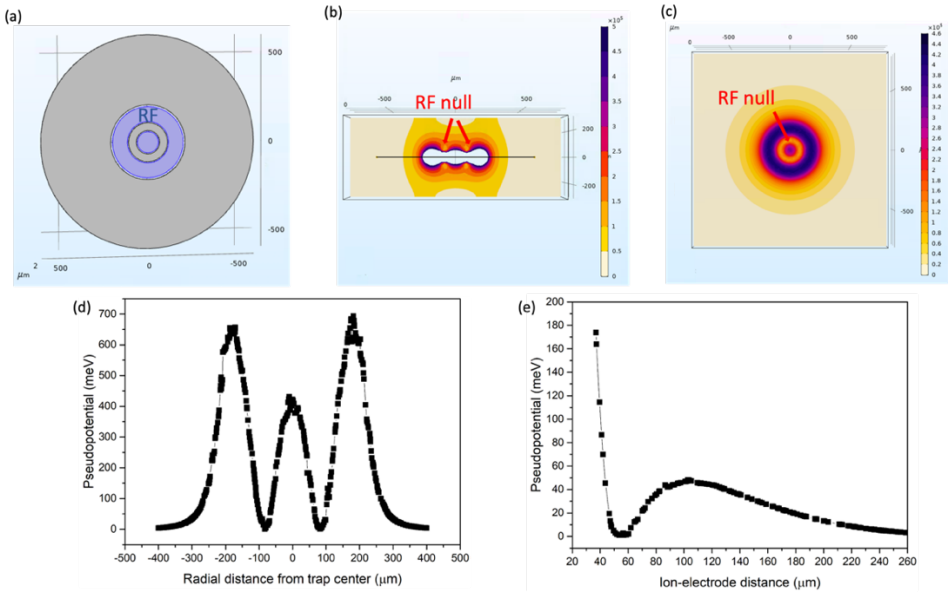


Figure 75. (a) Ring trap geometry and the corresponding RF voltage configuration. (b) Simulated electric field distribution in the vertical cut-plane at the trap centre. (c) Simulated electric field distribution in the planar cut-plane at the trapping height. The circular RF null is marked with red narrows. Pseudopotential distribution in the (d) radial direction and (e) vertical direction.

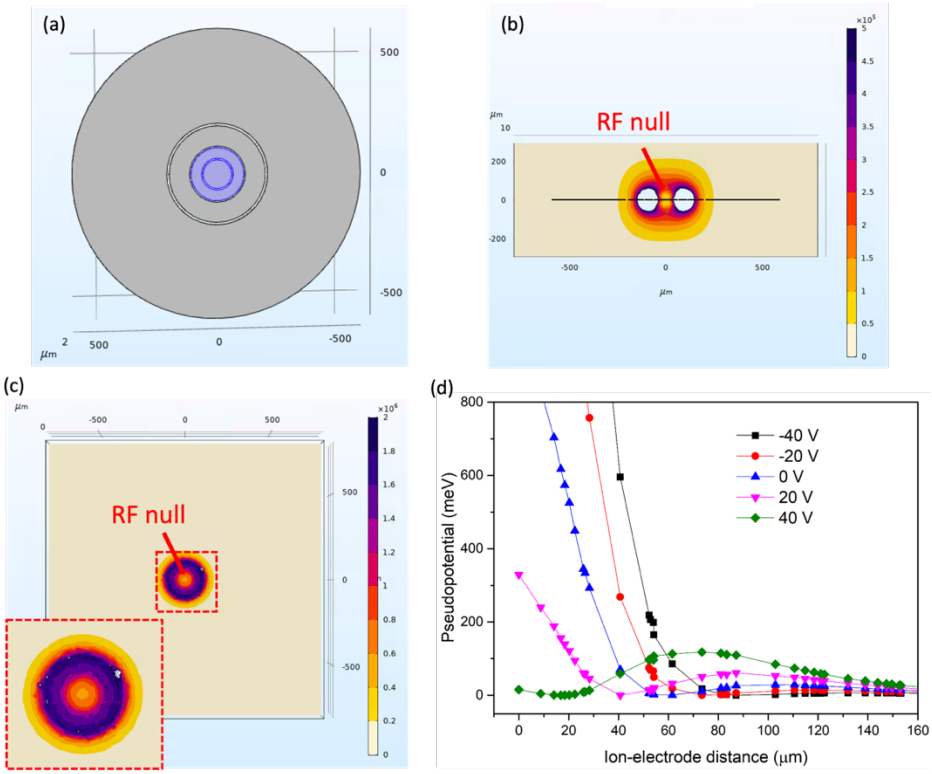


Figure 76. (a) Point trap geometry and the corresponding RF voltage configuration. (b) Simulated electric field distribution in the vertical cut-plane at the trap centre. (c) Simulated electric field distribution in the planar cut-plane at the trapping height. A zoom-in image of trapping field is shown in the inset. The single RF null is marked with red narrows. (d) Pseudopotential distribution at different RF amplitude of 1st electrode (the RF signal at the 2nd electrode is kept as constant).

6.2.2 Square Trap and the Integration with Linear Trap

Generally, ions are radially confined at the RF null of dynamic RF field in a surface electrode ion trap. Though the trapping height adjustment may be facilitated by DC potentials control [181], the offset between ions and RF null will result in the intensified micromotion. The existing in-situ approach (no excess micromotion) for trapping height adjustment is mainly dependent on the point trap which has a circular electrode geometry, as demonstrated in Section 6.2.1. However, the circular electrodes hamper its integration with linear trap that has a rectangular geometry, limiting its application in large-scale quantum computing. Also, people may employ multiple sets of RF electrodes in a single trap for height adjustment [66, 72, 182, 183]. Nevertheless, this kind of adjustment is always discrete and limited in a small range. To resolve the abovementioned issues, a point trap that has a square geometry is developed and further integrated with a linear trap. A two-dimensional ion shuttling path is thus built: the ion movement in axial direction is supported by linear trap with DC potentials tunning, whereas the trapping height can be in-situ adjusted by RF amplitudes in point trap. When the point trap is not in operation, the required electrodes of it can be seamlessly combined with neighboring electrodes and together work as an extended linear trap without performance degradation. Similarly, when the point trap is in operation, the other sections of linear trap will work as normal except for leaving a small buffer region that close to the point trap.

This design has immediate interests for mass ion addressing and heating rate reduction for certain ions in a large-scale ion trap. Meanwhile, a variety of experimental applications can be benefited. For example, the high-resolution trapping height adjustment can make the alignment between laser beams and ions more straightforward, especially in the case where grating couplers are on-chip integrated. Also, provided the ions at different point traps can be interconnected and entangled (e.g., through optical fibers), the scalability of this integrated point and liner trap can be further boosted.

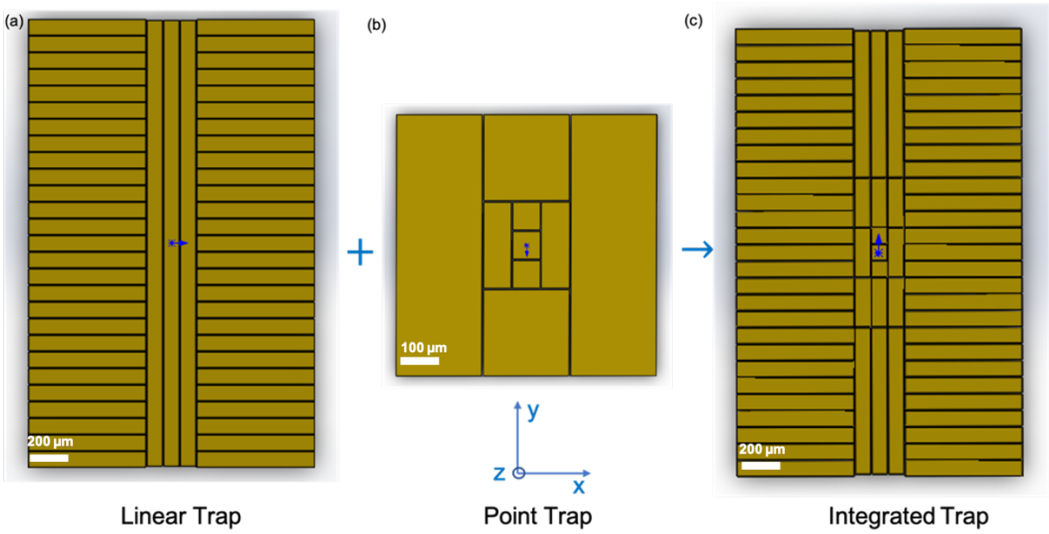


Figure 77. Geometry development of integrated ion trap. (a) Conventional linear trap, where ions can be shuttled along y direction by tunning DC potentials. (b) Point trap with a square geometry. Ions trapped by point trap can be shuttled along z direction. (c) The geometry after the integration of point and linear trap.

By configuring the electrodes potential accordingly, the integrated trap is able to perform the individual mode of linear trap, point trap, as well as the combination mode of these two.

The geometry development of integrated trap is shown in Figure 77. Different from conventional linear trap (Figure 77 (a)), the central three electrodes are incorporated with gaps and segmentations, where different electrical signals can be applied. In this demonstration, the electrode width of central three electrodes is set as 80 µm. The large segmentation has a length of ~700 µm, and the centre ones are further broke into three minor segmentations (~240 µm). The smallest segmentations is a square with a dimension of 80 × 80 μm^2, which are required for point trap implementation (Figure 77 (b)). All the gaps are designed with a width of 2 µm.

As shown in Figure 78 (a), the point trap mode is enabled by apply RF potentials (same phase but different amplitude) onto the central smallest (RF#2) and its surrounding neighbor segmentations (RF#1). The remaining electrodes are set as ground or DC. The encircled segmentations are used to produce trapping field with local minimum, whereas the central segmentation is used to adjust the potential minimum height. Figure 78 (b) and (c) show the modelled electric field distribution in two cut-planes (*x*-*z* and *x*-*y*), where a trapping point (RF null) can be seen above the ion trap surface (*x*-*z* cut-plane) and in the geometry center (*x*-*y* cut-plane). The relationship between ion-electrode distance and amplitude of RF#2 is shown in Figure 78 (d). The ion-electrode distance is ~55 µm when no RF#2 is applied and can be adjusted from 20 to 120 µm. Even larger adjustment range can be achieved if the trap is

working in a cryogenic environment in which only a lower trapping depth is needed. Note the trapping height adjustment in point trap is facilitated by in-situ moving RF null, instead of tunning DC potentials. This will minimize the excess micromotion induced by the position offset between ions and the RF null. An ion shuttling path perpendicular to the trap surface is thus built by continuous RF voltages tunning.

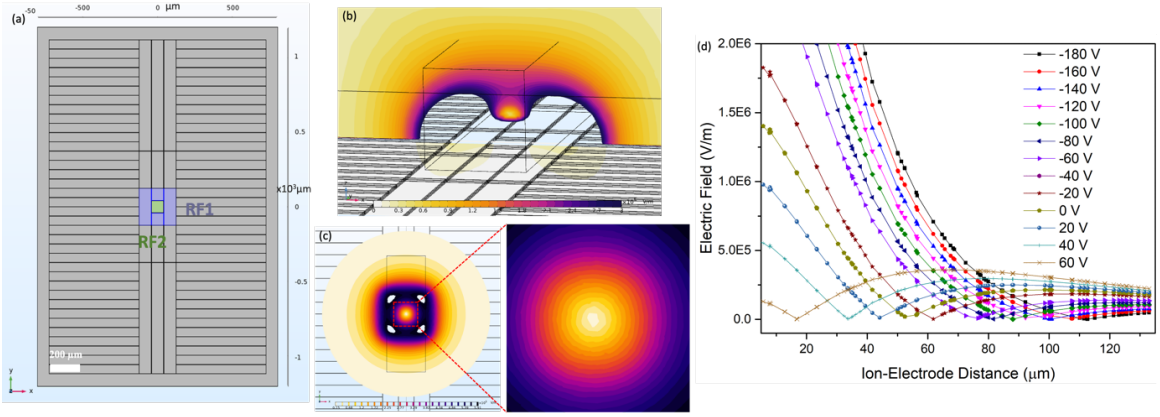


Figure 78. Integrated ion trap working in point trap mode. (a) Two RF signals with same phase but different amplitudes are applied onto the central electrode segmentation and the surrounding segmentations. The remaining electrodes are kept as DC or ground. (b) Electric field distribution in *x*-*z* cut-plane. A RF null can be observed above the electrode surface. (c) Electric field distribution across the RF null in *x*-*y* cut-plane, with a zoom-in image showing RF null in the center. (d) Ion-electrode distance as a function of the RF#2 amplitude (RF#1 has a constant amplitude of 100 V). Both signals have a frequency of 30 MHz.

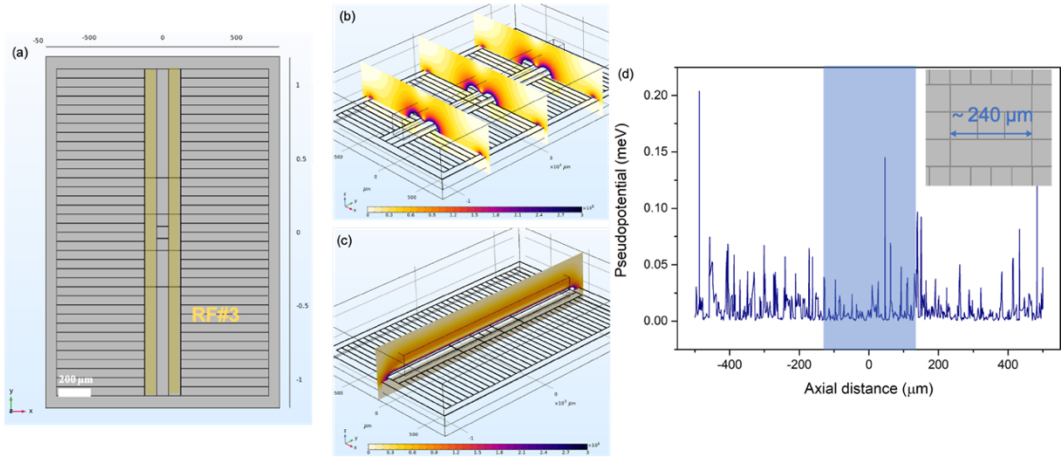


Figure 79. Integrated ion trap working in linear trap mode. (a) RF signal is applied onto two two symmetric electrodes. The remaining electrodes are kept as DC or ground. (b) Electric field distribution in three parallel *x*-*z* cut-planes, located respectively at y=0 and y=±700 μm. (c) Electric field distribution across the RF null in *y*-*z* cut-plane (x=0). (d) Pseudopotential distribution as a function of axial distance along the RF null line of linear trap above the trap surface. No excess fluctuation is observed in the region that has gaps.

By applying the RF potential onto two symmetric electrodes, the integrated trap will work in the linear mode (Figure 79 (a)). With the abovementioned electrode dimensions, the linear trap has a constant ion-electrode distance of ~75 μm. Since electrode segmentations have been incorporated for point trap implementation, it is necessary to evaluate the influence from these

gaps to the electric field distribution in axial direction (*y* axis in Figure 79 (b) and (c)). A uniform RF null line above trap surface is shown in Figure 79 (c). The pseudopotential distribution along this line is further extracted. It is found that the maximum fluctuation is less than 0.2 meV. In the region that accommodates three gaps (~240 μm in length), no excess fluctuation is observed. This indicates that a barrier-free ion shuttling path parallel to the trap surface has been built.

The integrated ion trap will simultaneously feature the functions of point trap and linear trap (the combination mode), when the RF signals are configured as shown in Figure 80 (a). The point trap and linear trap region are respectively located at the geometry centre and the remaining parts at two ends. Similarly, the distribution of electric field is modelled. As shown in Figure 80 (b), the electric field in the middle cut-plane (point trap region) is slightly different with those on the cut-planes of linear trap region. On the other hand, the regions can be clearly differentiated from the view of *y*-*z* cut-plane (Figure 80 (c)), where the linear trap region has a uniform RF null line while the point trap region has a single RF null point. The interference between two regions is also evaluated. As demonstrated in Figure 80 (d), though the pseudopotential in axial direction will decline rapidly from the point trap region to the linear trap region, a buffer region in between is needed to minimize the interference in between.

In a typical 2D shuttling process, certain ions can be first shuttled along axial direction to the position where point trap located by DC potentials setting in the linear trap mode. After that, the ion trapping height can be raised or dropped by the in-operation point trap. The remaining parts of integrated trap can still work as linear trap if needed.

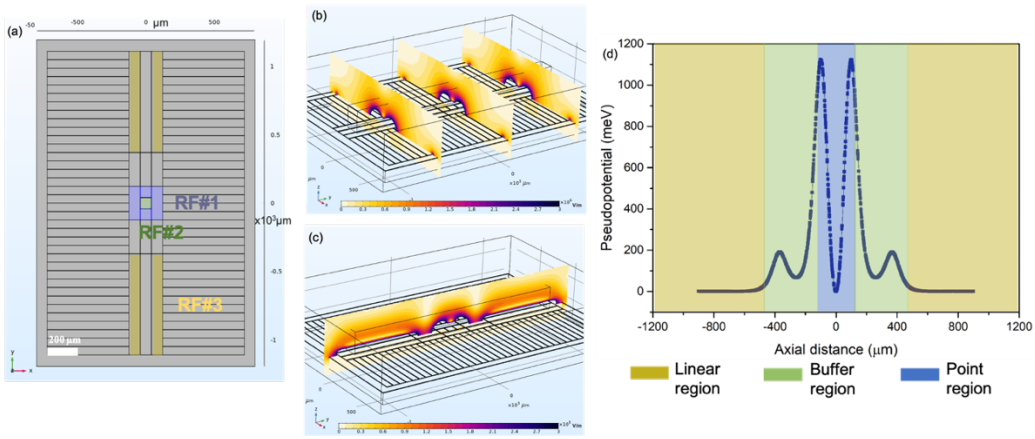


Figure 80. Integrated ion trap working in combination mode. (a) RF signals are applied onto the corresponding electrodes to operate point and linear trap simultaneously. The remaining electrodes are kept as DC or ground. (b) Electric field distribution in three parallel *x*-*z* cut-planes, located respectively at y=0 and y=±700 μm. The electric field in the middle *x*-*z* cut-plane is different from the other two. (c) Electric field distribution in *y*-*z* cut-plane (x=0). (d) Pseudopotential distribution as a function of axial distance along the RF null above the trap surface. A buffer region is introduced to minimize the interference between two regions.

6.2.3 Large-scale Ion Trap

To scale up the ion trap device, two basic schemes were proposed. The first scheme is to shuttle ions between different trapping zones with different functions (i.e., quantum memory region and interaction region). This scheme is so-called quantum charge-coupled device (QCCD) [20]. Another complementary scheme is to couple and entangle ions at different trapping potentials (different traps) without physically shuttling ions. In this scheme, communication mediums like propagating photons are required [21].

Obviously, the multi-module integrated ion trap can be an important building block in both schemes. To be concrete, the integrated photonics components can facilitate the intricate ion shuttling process in the first scheme and the communication qubits entanglement process in the second scheme. Meanwhile, as a complex electrode geometry is anticipated in both schemes (e.g., *T* and *X* junctions in QCCD scheme), TSV and multilayer metallization become indispensable for flexible interconnections.

Last but not least, the developed die-interposer hybrid architecture can further enable the large-scale ion trap implementation. Multiple multi-module integrated ion traps with different functions (e.g., linear trap and ring trap) can be co-located onto the same interposer and interconnected by the RDL on the interposer in a reconfigurable approach. Depending on the particular scaling up scheme, other functional components (e.g., DACs for qubit shuttling scheme and fibers for remote entanglement scheme) can be correspondingly added onto the interposer. In this case, high modularity is provided for the final large scale configuration. It should be noted that the further scaling up is not limited in a 2D fashion (i.e., all components are located on the same interposer). Indeed, multiple interposers designed for different components can be eventually bonded together using state-of-the-art die-to-wafer or even wafer-to-wafer bonding process (Figure 81). Meanwhile, since trap dies and interposers are independently fabricated, the testing and integration process can be largely simplified, promoting a high yield of the final device.

Certainly, the demonstrated architecture in Figure 81 is a conceptual idea for large-scale ion-trap-based quantum computing. Lots of practical challenges remain to be solved. For example, the threshold for bonding alignment of multiple traps on the interposer is foreseen to be extremely small. Also, the signal filtering and shielding between components are necessary. The noise to the qubit due to the diverse integration should also be investigated. However, the

exciting point is that no fundamental restriction is found, and the mentioned technical challenges can be finally solved. Therefore, it is concluded that the large-scale ion trap based on multi-module integrated trap and interposer architecture is promising and achievable.

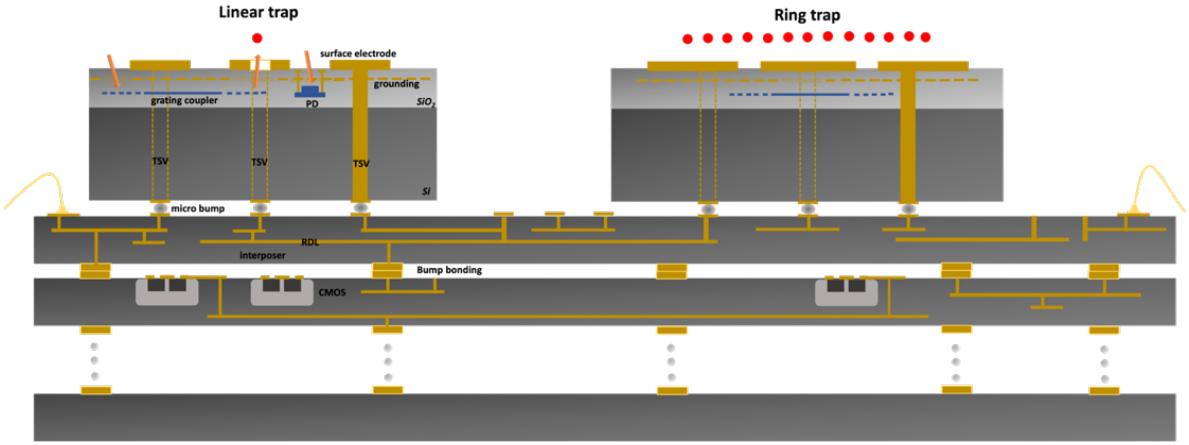


Figure 81. Schematic of large-scale ion trap device. Multi-module integrated ion traps are co-located onto multiple interposers. Multiple interposers integrated with particular functional components (DC sources, RF generation, DACs, microwave generation, etc.) are bonded together.

List of Publications

Journal Papers:

1. **Zhao, Peng.,** Likforman, Jean Pierre., Li, Hong Yu., Tao, Jing., Henner, Theo., Lim, Yu Dian., Seit, Wen Wei., Tan, Chuan Seng., & Guidoni, Luca. (2021). TSV-integrated surface electrode ion trap for scalable quantum information processing. *Applied Physics Letters*, *118*(12), 124003.

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3. **Zhao, Peng.,** Lim, Yu Dian., Li, Hong Yu., Guidoni, Luca., & Tan, Chuan Seng. (2021). Advanced 3D Integration Technologies in Various Quantum Computing Devices. *IEEE Open Journal of Nanotechnology, 2,* 101-110.

4. Lim, Yu Dian., Li, Hong Yu., **Zhao, Peng.,** Tao, Jing., Guidoni, Luca., & Tan, Chuan Seng. (2021). Design and Fabrication of Grating Couplers for the Optical Addressing of Trapped Ions. *IEEE Photonics Journal*, *13*(4), 1-6.

5. Tao, Jing., Likforman, Jean Pierre., **Zhao, Peng.,** Li, Hong Yu., Henner, Theo., Lim, Yu Dian., Seit, Wen Wei., Guidoni, Luca., & Tan, Chuan Seng. (2021). Large-Scale Fabrication of Surface Ion Traps on a 300 mm Glass Wafer. Physica status solidi (b), 2000589.

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1. **Zhao, Peng.,** Li, Hong Yu., Lim, Yu Dian., Seit, Wen Wei., Guidoni, Luca., & Tan, Chuan Seng. The Integration of Grounding Plane into TSV Integrated Ion Trap for Efficient Thermal Management in Large Scale Quantum Computing Device. *In 2022 72nd Electronic Components and Technology Conference (**ECTC**).* (accepted).

2. **Zhao, Peng.,** Bi, Xin Wen., Li, Hong Yu., Lim, Yu Dian., Seit, Wen Wei., Guidoni, Luca., & Tan, Chuan Seng. Heating Dissipation Discussion of TSV-integrated Ion Trap with Glass Interposer. *In 2021 IEEE 23rd Electronics Packaging Technology Conference (**EPTC**)* (pp. 628-632).

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4. **Zhao, Peng.,** Li, Hong Yu., Lim, Yu Dian., Tao, Jing., Seit, Wen Wei, Guidoni, Luca., & Tan, Chuan Seng (2020, December). Glass Substrate Interposer for TSV-integrated Surface Electrode Ion Trap. *In 2020 IEEE 22nd Electronics Packaging Technology Conference (**EPTC**)* (pp. 262-265).

5. **Zhao, Peng.,** Tao, Jing., Li, Hong Yu., Lim, Yu Dian., Lin, Ye., Guidoni, Luca., & Tan, Chuan Seng. (2020, September). Performance Comparison of High Resistivity Silicon, Silicon with Grounding Plane and Glass as Substrate of Ion Trap for Quantum Information Processing. *In 2020 IEEE 8th Electronics System-Integration Technology Conference (**ESTC**)* (pp. 1-5).

6. **Zhao, Peng.,** Tao, Jing., Li, Hong Yu., Lim, Yu. Dian., Guidoni, Luca., & Tan, Chuan Seng (2019, December). Design, Fabrication and Characterization of Surface Electrode Ion Trap Integrated with TSV. *In 2019 IEEE 21st Electronics Packaging Technology Conference (**EPTC**)* (pp. 13-17).

7. Lim, Yu Dian., Li, Hong Yu., **Zhao, Peng.,** Tao, Jing., Guidoni, Luca., & Tan, Chuan Seng. (2021, May). Design and Fabrication of Silicon Gratings for the Optical Addressing of Trapped Ion Qubits. *In **CLEO**: QELS_Fundamental Science* (pp. JF2G-3).

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Patent:

1. **Zhao, Peng.,** Li, Hong Yu., Lim, Yu Dian., & Tan, Chuan Seng. Square Point Trap and the Integration with Linear Trap for Large-Scale Quantum Computing. Filled as Singapore provisional patent and accorded with number 10202110905T. 2021.
2. Lim, Yu Dian., **Zhao Peng.,** & Tan, Chuan Seng. Wavelength Filtering And Photon Detection Methodology By Photonics Circuits With Multi-Layer Ring Resonator Filtering And Inter-Electrode Detector Placement. Filled as Singapore provisional patent and accorded with number 10202108328T. 2021.

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Appendix

COMSOL Multiphysics is a finite element modelling platform that provides fully coupled multiphysics and single-physics modelling capabilities. **COMSOL Multiphysics** is extensively used in this thesis for various simulations: from electric field distribution, ion trajectory visualization and RF loss extraction to thermal management verifications, for different ion traps. In the appendix, a typical modelling workflow using **COMSOL Multiphysics** is presented: from geometry definition, material properties setting, geometry meshing and applying physics that describe specific phenomena, to the postprocessing analysis.

In this section, two modelling examples are illustrated: the first modelling aims to obtain the trapped ions trajectory in trap WB_80 (Chapter 3); the second modelling focuses on the S-parameter extraction on trap WB_80 (Chapter 4).

First, a 3D model shall be built according to the geometry of WB_80 trap. Since ion trap features a 2D-like geometry (i.e., the vertical dimension is far smaller than the lateral dimensions), it is suitable to configure the electrodes geometry in a 2D **Work Plane** under the **Geometry** setting window. Following that, the work plane can be extruded to a specific thickness. The work plane geometry can be manually drawn using the toolset provided in **Plane Geometry** section. Also, it can be imported from CAD software (e.g., SolidWorks). The final electrode geometry is shown in Figure 82 (a). After electrode configuration, a block is created underneath and used as insulation layer (silicon oxide block). Another two air blocks are created: the big one is to embody all the entities, and the small one is located right above the electrode center for fine mesh implementation (Figure 82 (b)). This is to obtain high-resolution motion trajectory only at region near to trapping center. In addition, one point is created at the nominal trapping center (inside small air block), this point is used for ion release during ion trajectory simulation. Since this modelling focuses on the electric field generated by the surface electrode above the trap, the silicon substrate, adhesion layer and seed layers are eliminated in the model building for simplification.

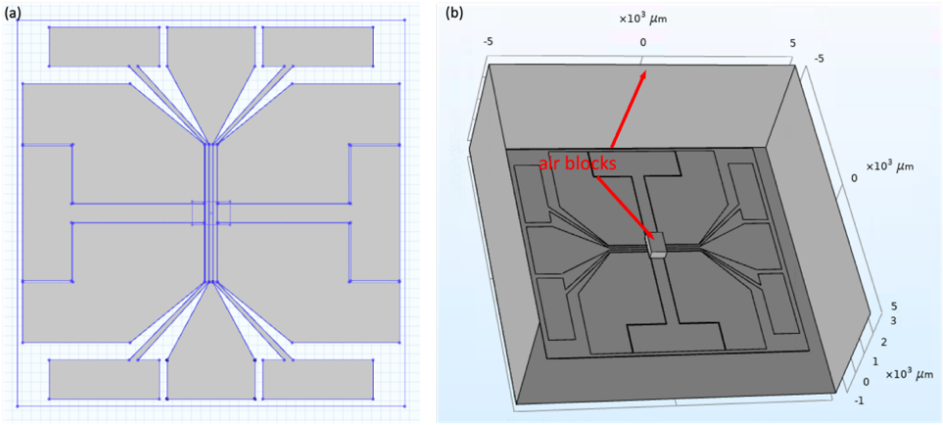

Figure 82. (a) 2D geometry built in the work plane. (b) Final 3D geometry for the ion trajectory simulation. Two boundaries of the big air block are hided for easy visualization.

After building the 3D model, the entities in the model are set with corresponding materials. In the setting window for **Material**, various materials can be selected from the database. Also, one can create a blank material and type in the properties accordingly (Table XI).

Table XI. Material properties used in the modelling.

Material Properties	Si	SiO_2	Cu
Conductivity (S/m)	10	0	6E7
Relative permittivity	11.7	4.2	–
Relative permeability	1	1	1
Thermal conductivity @ 300 K (W/(m·K))	150	1.2	380
Heat capacity @ 300K (J/(kg·K))	700	730	385

In finite element modelling, meshing the entire domain into small elements is an important step. To obtain high-fidelity result, a high-quality mesh is required. First, the meshing density shall be sufficiently high, in particular at the core regions (e.g., around the trapping center). Second, the meshing element type should match with the geometry. In the case of trap WB_80, two types of mesh are used based on the different geometry features. First, **Free Tetrahedral** node under **Mesh** window is adopted for the two air blocks. Particularly, for the small air block accommodating the ion, the elementary element size is set as 1 μm and the maximum is set as 10 μm. Again, this is to obtain a high-resolution ion trajectory. Second, for the extruded surface electrode, a 2D meshing is first created with a triangular element shape at the surface boundary using the **Free Triangular** node. A subsequent sweep is performed to map the boundary mesh into the entire entity. Considering the dimension of surface electrode, the element size of

triangular mesh is in the range of 10 – 100 µm. Only one mesh layer is created in the third dimension, since the electrode thickness is only 3 µm (ignoring the Au layer). Similarly, this '2D boundary mesh + sweep' process is used for the meshing of the silicon oxide block. The **Convert** node shall be used to convert the triangular prism mesh of electrode to the tetrahedral mesh of the air. The final meshed geometry is shown in Figure 83. In total, 2,958,240 mesh elements are created in the entire geometry.

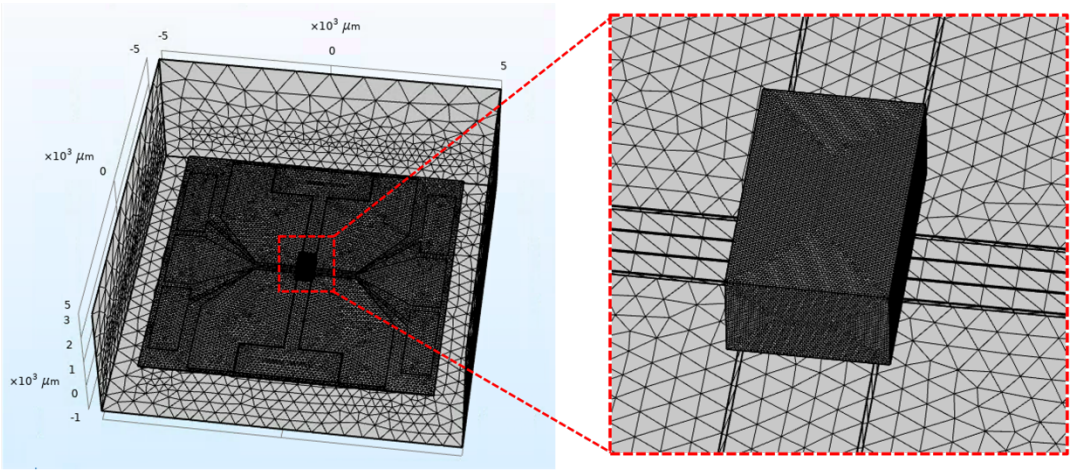

Figure 83. Meshed 3D geometry. A zoom-in image of fine-meshed air block above the electrode centre is included. Two boundaries of the big air block are hided for easy visualization.

100 V potential is applied onto two RF electrodes via the **Electric Potential** node under the **Electric Current** module in **Physics** setting window. The remaining electrodes are set as ground. This is to build the required RF field for ion trapping. Next, under the **Charged Particle** module, the ion mass and charge are set accordingly in the **Particle Properties** node. The **Release from Point** node is then enabled. Ions will be released from the point built above the surface as mentioned earlier. Meanwhile, under the same module, **Electric Force** node is enabled. This is to apply the electric force generated by the RF potential in the **Electric Current** module onto the ions. In other words, the electric force and ion motion are coupled.

Two studies are added in the **Study** setting window. The first is at frequency domain to oscillate the applied potential on the RF electrodes with a specific frequency (30 MHz). The second is a time dependent study (i.e., time domain), which is to calculate the ion motion as a function of the time. Note the time step in the second study should be significantly smaller than the period of RF signal ($\frac{1}{30 \times 10^6}$ s).

After the calculation, the first thing to do is to add specific data sets to the corresponding study in the **Data Sets** setting window. For example, one **Cut Plane** data set is created under

Study 1/Solution 1 (electric field study). This plane will be used to view the electric field distribution. Similarly, a **Particle** data set is automatically created under the **Study 2/Solution 2** (ion trajectory study). In the **Results** setting window, the **3D Plot Group** node is enabled, where a **Contour** plot of electric field can be created with the cut plane data set (Figure 84 (a)). Meanwhile, the ion motion can be viewed in the **Particle Trajectories** node. Selecting the Particle data set and setting a suitable time period, the ion trajectory can be viewed (Figure 84 (b)). The raw data of ion position (coordinates) as a function of time can be exported. With Fourier transform, the secular motional frequency in different directions can be extracted. Certainly, the simulation result can be further analyzed with various toolsets embedded in the **Result** window. For example, the pseudopotential distribution can be plotted using **1D Plot Group**. The power loss in a substrate can be calculated by **Volume Integration**.

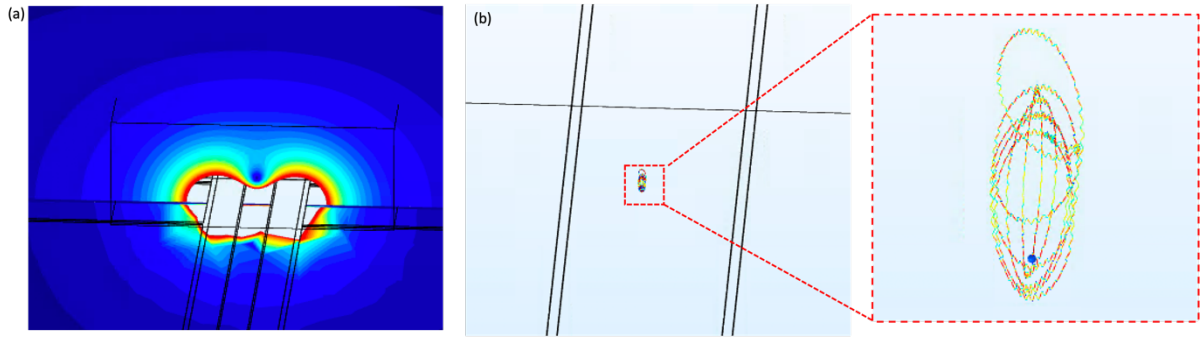

Figure 84. (a) Electric field distribution in a cut plane perpendicular to the trap surface. (b) Ion trajectory above the electrode. A zoom-in inset of the trajectory is included. The colour difference indicates the velocity change.

Next, S-parameter modelling based on trap WB 80 is introduced.

A similar 3D model is inherited from the ion trajectory modelling. However, in the 3D model for S-parameter modelling, the small air block above trap surface can be eliminated and four work planes are added, which will be used as the 'Lump Port' in the subsequent settings (Figure 85 (a)). The material properties are same with those listed in Table XI. The meshing method is also similar, except that the fine mesh region is moved to the added work planes. Due to the elimination of small air block, 533,768 mesh elements are now created.

Electromagnetic Waves, Frequency Domain module in **Physics** setting window is activated. Two **Lump Ports** are created by selecting the work planes mentioned earlier, but only one port has wave excitation (Figure 85 (b)). The excitation has a unit voltage and initial phase of 0 degree. In the **Study** setting window, only study in frequency domain is enabled. The frequency ranges from 10 to 110 MHz with a step of 2 MHz.

After calculation, in the **S-parameter** node under **Results** setting window, the expressions of S21 and S11 can be selected and the S-parameter as a function of RF frequency is plotted. Similarly, this raw data can be exported and replotted where necessary.

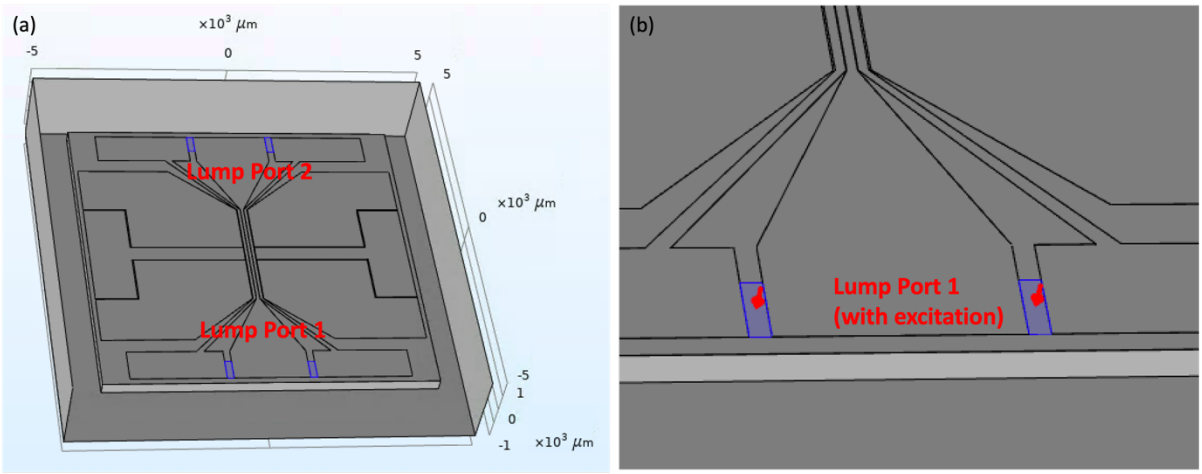

Figure 85. (a) Trap WB 80 with four added work plane, which are selected as two lump ports in S-parameter modelling. (b) A zoom-in image showing lump port #1, where wave excitation is enabled.