



**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DEVELOPMENT OF A FLIP-CHIP COMPOSITE
INTERCONNECTION SYSTEM**

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SCHOOL OF MECHANICAL AND AEROSPACE ENGINEERING

2012

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ENGINEERING**

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the
Degree of Doctor of Philosophy

2012



*To my beloved wife, Gek Noi,
for her unceasing love and devotion
To my lovely daughters, Jane, Sarah, Joann & Rayna,
for their joy and laughter*



Acknowledgements

I would like to express my heartfelt gratitude to Prof. John Pang for his guidance, mentorship and invaluable discussions throughout my research.

I would like to acknowledge the Singapore Institute of Manufacturing Technology (SIMTech), A*STAR, for sponsoring this research and my special thanks Dr Lim Ser Yong for his constant encouragement.

Throughout this research, I received great support from my colleagues from JTG, MMP, MTG and PMG. In particular, I would like to extend my greatest appreciation to Mr Fan Wei for assisting in the test instrumentation, Ms Lu Haijing in the plating evaluations, Dr Yi Ming in the FEM, Mr Cheng Chek Kweng in the assembly setup, Mr Paramasivam in sample preparations and Ms Ng Fern Lan in the SEM.

This thesis is dedicated to my beloved wife, Gek Noi, for her unceasing love and devotion to me throughout my academic pursuit, and to my four lovely daughters, Jane, Sarah, Joann and Rayna, for constantly surrounding me with their joy and laughter.

Abstract

The objective of this research is to develop a novel flip-chip composite interconnect structure to overcome the inherent weaknesses of the conventional solder bump interconnection. In the conventional flip-chip, 3-D stacking of chips is often not feasible due to the inherent solder bump collapse during reflow. The under-bump-metallization (UBM) compatibility with Pb-free solder is a concern, especially with the miniaturization trend. The thin UBM is susceptible to electromigration and metal diffusion.

The proposed flip-chip composite structure comprises a Cu pillar with a pinhead on its end which serves as an extended pad for solder bump attachment. The concern of UBM failure on a chip is mitigated as the pinhead which replaces the pad metallization on the chip is extended on a Cu pillar. The chip is no longer exposed to solder reaction during the reflow process.

An electrolytic Ni-Au UBM scheme is selected for the Cu pinhead (CPH) pillar bump as the UBM deposition can be carried out in the same plating process for CPH pillars fabrication. Sn-Ag-Cu (SAC) solder and Ni-Au UBM interfacial reaction was investigated. EDX analyses identified a $(\text{Ni,Cu})_3\text{Sn}_4$ IMC on the Ni UBM interface and a second layer of $(\text{Cu,Ni})_6\text{Sn}_5$ was formed on top of the $(\text{Ni,Cu})_3\text{Sn}_4$ IMC. The Ni UBM dissolution after reflow and isothermal aging is approximately 1 μm . A UBM thickness of 2.0 -2.5 μm is recommended for the CPH pillar bump solder attachment.

The flip-chip composite interconnect concept, comprising a CPH pillar attached with a SAC solder bump, is found to be more reliable than the conventional Cu pillar and flip-chip solder interconnections. A parametric study was carried out to benchmark the performance of the CPH pillar solder interconnection with the conventional Cu pillar solder bump and flip-chip solder bump interconnection respectively. A temperature

cycling condition of 0 – 100 °C was simulated. The FEA results show that the conventional flip-chip solder joint has a predicted life of 203 cycles and the solder joint on the conventional Cu pillar, with a diameter of 110 μm and height of 160 μm , can survive 297 cycles. The solder joint on the CPH pillar, with a diameter of 80 μm , height of 160 μm and pinhead diameter of 110 μm , has a predicted life of 443. Hence, the performance of the CPH pillar solder joint is 2.2 times more reliable than the conventional flip-chip solder joint and 1.5 times more reliable than the conventional Cu pillar solder joint.

A CPH pillar fabrication process is developed using a through-mask electroplating. To maintain good repeatability and plating yield in CPH pillars fabrication, plating mask openings of at least 80 μm in diameter in a 45 μm thick positive photoresist is recommended. A 4-step plating process is developed to fabricate CPH pillars on silicon wafer. The electroplating studies were carried out in a fountain-flow plating cell using an optimized plating current of 300 mA. The CPH pillar uniformity across a 4-inch wafer is 5% and the Cu deposition rate is 1.3 $\mu\text{m}/\text{min}$. CPH pillar structures of 80 μm pillar diameter, 165 μm overall pillar height and 110 μm pinhead diameter are successfully fabricated.

The compliance of the electroplated CPH pillars is further enhanced using elevated temperature annealing in nitrogen environment. The CPH pillar annealing is carried out before the solder bumping process. CPH pillars annealed for 30 minutes at three different temperatures (250, 325 and 400 °C) were evaluated. The temperature range was selected to simulate the processing temperatures of most electronics and MEMs devices. Microstructural changes in the CPH pillars due to recrystallization and grain growth induced by annealing were observed. The nanoindentation results show that the elastic modulus of CPH pillars is reduced by 24-28 % and the hardness decreased by 9-16

%. It could be deduced that the compliance of the Cu pillars has increased with annealing. The mechanical properties of the pillars are found to be uniform along their entire length. This shows that a constant DC plating current can produce homogeneous Cu properties in CPH pillars. XRD analyses indicate that the preferred crystallographic orientation in the CPH pillars is [111]. Previous studies have found that Cu in the [111] orientation has good mechanical strength and electromigration resistance.

The experimental reliability results show that the CPH pillar solder joint (without underfill) can survive 1.7 -1.8 times longer than the conventional flip-chip solder joint when they are subjected to accelerated temperature cycling at 0-100 °C. In the electromigration test where flip-chip and CPH solder joints were stressed at 1.6×10^4 A/cm² and 100 °C, five out of nine CPH pillar chips survived 596 hours of EM testing, whereas all the nine conventional flip-chips failed within 191 hours. Using 10% and 20% resistance changes as the EM failure criteria, the CPH pillar solder interconnection is found to survive 2.5 to 2.7 times longer than the conventional flip-chip solder joint.

The novel flip-chip composite interconnect structure comprising a Cu pinhead (CPH) pillar with an attached solder bump has demonstrated significantly better solder joint fatigue life and EM resistance, compared to the conventional flip-chip solder joint. The CPH pillar structure also has the design flexibility for the interconnect compliance to be adjusted without changing the substrate soldering pad. The CPH pillar interconnection concept can be easily implemented using the existing backend semiconductor fabrication and assembly infrastructure.

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List of Symbols

D	Diffusion coefficient
E	Elastic modulus
F	Faraday's constant
G	Shear modulus
H	Hardness
$I_{(hkl)}$	Measured relative peak intensity
$I_{o(hkl)}$	Relative peak intensity of standard powder of copper sample
N_f	Number of cycles to failure
Q	Activation energy
$T_{(hkl)}$	Texture coefficient
W_c	Plastic strain energy
W_{in}	Inelastic strain energy
W_p	Plastic strain energy
ΔW	Accumulated strain energy density
i or j	Current density
i_o	Exchange current density
i_L	Limiting current density
j_{em}	Atom flux
k	Boltzmann's constant
α	Current efficiency
δ	Diffusion layer thickness
ε	Strain
ε_c	Creep strain
ε_{in}	Inelastic strain
ε_p	Plastic strain
$\dot{\varepsilon}_c$	Creep strain rate
$\Delta \varepsilon$	Accumulated plastic strain
σ	Stress
σ_y	Yield stress

List of Abbreviations

3D	3-Dimensional
Ag	Silver
Al	Aluminium
APS	Advanpack Solutions
AR	Aspect ratio
ASE	Advanced Semiconductor Engineering
ATC	Accelerated temperature cycling
Au	Gold
BCB	Benzocyclobutene
BLM	Ball-limiting-metal
C4	Controlled collapse chip connection
CCGA	Ceramic column grid array
CPH	Copper pinhead
Cu	Copper
CuCGA	Copper ceramic grid array
CTE	Coefficient of thermal expansion
DNP	Distance from neutral point
EBSD	Electron backscatter diffraction
EDX	Energy-dispersive X-ray spectroscopy
ENIG	Electroless nickel with immersion gold
EPC	Elastic Plastic Creep model
FCB	Conventional flip-chip solder bump
FEA	Finite element analysis
FEM	Finite element method
HCl	Hydrochloric acid
IC	Integrated circuit
IMC	Intermetallic compound
iNEMI	International Electronics Manufacturing Initiative
I/O	Input / Output on an integrated circuit
ITRS	International Technology Roadmap for Semiconductors
Low-k	Low-constant

MCP	Multichip package
MEMS	Micro-electro-mechanical systems
m.p.	Melting point
Ni	Nickel
Ni-Au	Nickel-Gold
Ni(P)	Nickel-Phosphorous
PI	Polyimide
Pb	Lead
Pb/Sn	Lead-Tin
PCB	Printed circuit board
RTC	Rapid temperature cycling
SED	Strain energy density
Sn	Tin
Sn-Bi	Tin-Bismuth
Sn-Ag	Tin-Silver
Sn/Pb	Tin-Lead
SAC	Tin-Silver-Copper
SEM	Scanning electron microscopy
SiP	System-in-package
SOC	System-on-chip
SSC	Stretched solder column
TE	Thermal electric
Ti	Titanium
Ti-W	Titanium-Tungsten
UBM	Under-bump-metallization
V/A	Volume / Area ratio
WIT	Wire interconnect technology
WLCSP	Wafer-level chip scale packaging
WLP	Wafer-level packaging
XRD	X-ray diffraction

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List of Publications

The following patents and publications are based on the research work carried out in this thesis.

US Patent

- Wong C.K.S., Pang J.H.L., Fan W., Lu H.J. and Lok B.K., “Interconnect structure and a method of fabrication of the same,” *United States Patent Application US2010/0246150A1*, Sep 30, 2010

Singapore Patent

- Wong C.K.S., Pang J.H.L., Fan W., Lu H.J. and Lok B.K., “Interconnect structure and a method of fabrication of the same,” *Register of Patents, Singapore, SG Publication No. 152101*, Nov 06, 2007

Journal

- Wong C.K., Pang J.H.L., Tew J.W., Lok B.K., Lu H.J., Ng F.L., Sun Y.F. (2008), “The influence of solder volume and pad area on Sn–3.8Ag–0.7Cu and Ni UBM reaction in reflow soldering and isothermal aging,” *Microelectronics Reliability*, vol. 48, pp. 611-621

Conference

- Wong C.K., Pang J.H.L., Sun Y.F., Ng F.L., Tew J.W. and Fan W. (2005), “Influence of Solder Volume on Interfacial Reaction between Sn-Ag-Cu Solder and TiW/Cu/Ni UBM,” *Proceedings of Electronic Packaging Technology Conference (EPTC 2005)*, pp.492 – 496
- Pang J.H.L.; Wong C.K.; Neo S.K. and Tan K.E. (2008), “Thermal cycling fatigue analysis of copper pillar-to-solder joint reliability,” *Proceedings of Electronics System-Integration Technology Conference (ESTC 2008)*, pp. 743-748

Chapter 1 Introduction

1.1. Background

The trends towards miniaturization, resistance reduction and improved thermal performance are the main drivers for semiconductor devices development. As the functionality and portability of electronic products increase, the current semiconductor interconnection technology needs to be more reliable and flexible in design to keep pace with the short product life cycle. Constant I/O density increase and the use of 3-D packaging for multiple chips integration are posing new challenges for packaging and assembly. While the flip-chip solder bump has proven to be reliable and efficient for area array interconnection (Neugebauer et al, 1987, Bartlett et al, 1987, Heinen et al, 1989, Tummala 2001), several limitations become apparent when it is applied on emerging packages (Totta, 1971, Chao et al, 1988, Lee, 2009). An increase in I/O density will drive a decrease in the size of solder bumps. On the other hand, 3-D integration demands higher aspect ratio interconnecting structures with good thermal properties. The traditional flip-chip interconnection will not be adequate to meet the manufacturing and reliability requirements of emerging high density and multi-chip packages. A new interconnection system with good mechanical compliance, flexibility in design and ease in soldering will be needed to drive the electronic packaging industry forward.

Copper (Cu) is an excellent candidate material for the next generation of chip-package interconnections because of its high electrical and thermal conductivities, good mechanical properties at assembly and operating temperatures. There is also a well established manufacturing infrastructure to integrate the back-end processes with the Cu electroplating process. Cu pillar bump technology is currently considered a viable

alternative for direct-chip-attach interconnection (Tummala et al, 2006, Yeoh et al, 2006, Ebersberger et al, 2008, Lee, 2009, Orii et al, 2009). Cu pillar bumps can provide a superior thermal conduction path from the chip, and the standoff between the chip and substrate is controlled by the bumps. Since solder is not in direct contact with the silicon chip, the concern of metal diffusion and UBM dissolution on the chip is eliminated (Heinen et al, 1989, Tummala et al, 2006). In addition, Cu pillars can be manufactured in various shapes and sizes to further increase the current and heat capacities. As only solder is reflowed to create the joint, a consistent standoff can be maintained by the Cu pillar, which further enables the downstream processes of flip chip packaging. A novel approach proposed in this study is electroplating compliant Cu pinhead pillars capped with Pb-free solder bumps to provide reflow bonding in subsequent electronics assembly and packaging process.

1.2. Packaging interconnection limitations

Flip-chip technology, first introduced by IBM in the early 1960s (Tummala, 2001), is an important development for the microelectronic industry. Aided by the self-aligning characteristic of solder, flip-chip packaging using solder bump has an excellent yield. However, a few concerns arise in flip-chip solder bump interconnection when the transistor gate lengths decrease on silicon. An increase in I/O density on the silicon chip will lead to a decrease in solder bump diameter and effective area for current flow. Current density is not evenly distributed in a solder bump, instead it tends to crowd at the entrance and exit of its flow path. This leads to an increase in current density, joule heating and early failure. As illustrated in Figure 1.1, the reduction in solder bump size increases the volume ratio of intermetallic compound (IMC) to bulk solder in a solder joint. A high percentage of IMC in a solder joint is undesirable as IMC is brittle and the fatigue life of the solder joint will be reduced.

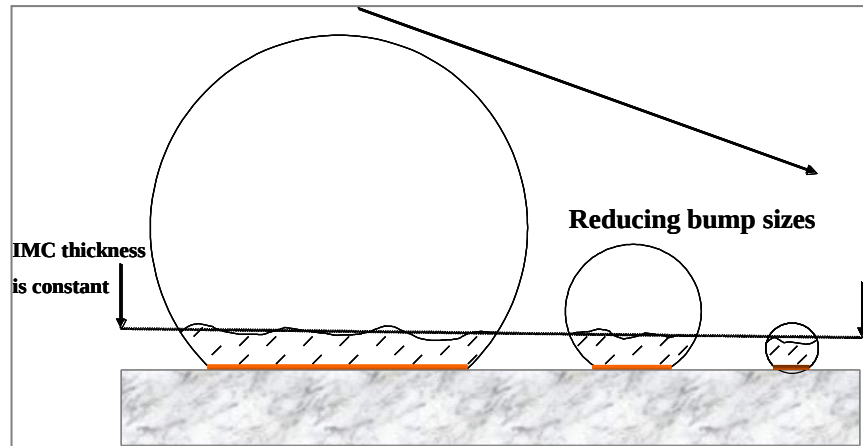


Figure 1.1 Volume ratio of IMC to bulk solder increases as bump size decreases

A typical solder bump interconnection comprises an under-bump-metallization (UBM), a solder bump and a matching substrate bond pad. Such an interconnection scheme has several inherent weaknesses. During reflow, the solder bump will collapse and attain a barrel-shaped profile upon solidification, as illustrated in Figure 1.2.

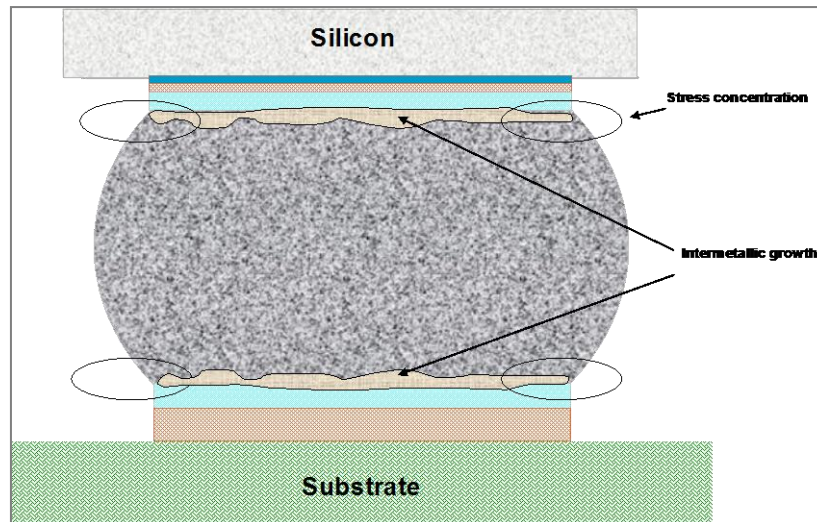


Figure 1.2 Stress concentration at solder bump interfaces and intermetallic growth

This limits the height and pitch of the solder joint and the application of solder bump interconnection in high-density miniaturized packages. The truncated spherical ends of the solder bump are the main load bearing points. High stress concentration occurs at these end points. Embrittlement at the IMC-solder interfaces and mismatch in coefficients of thermal expansion (CTE) in these areas, create sites for crack initiation and propagation.

Unlike solder bump, copper (Cu) pillar does not collapse during reflow soldering. Cu pillars can be packed closer together, increasing the interconnection density. There is no need for UBM at the chip-side in the Cu pillar bumping process. If the Cu pillar plating is carried out directly on the chip metal pads, IMC formation is on the Cu pillar side instead of on the chip. The concern of solder diffusion and interaction with the thin films on the chip is eliminated. In addition, given that the Cu mechanical properties are much better than those of conventional solder, failure is not likely to happen on the chip side. However, the stiff copper pillar can cause reliability problem. Thermal stress from the Cu pillars can cause cracks on the brittle silicon nitride or silicon oxide passivation and low-k dielectric layers. Further improvement is recommended in this study, so that the Cu pillar

structure can be engineered to reduce stress concentration and shear strain on the solder joint.

1.3. Objective

In this thesis, a novel composite Cu pinhead and solder bump interconnection structure will be developed to overcome the inherent weaknesses of the conventional solder bump interconnection. The proposed structure comprises a solid Cu pillar with a pinhead on its end serving as an extended pad for lead-free solder bump attachment (see Figure 1.3). The preliminary FEM results show that the Cu pinhead (CPH) pillar bump assembly performs significantly better than the conventional flip-chip and Cu pillar solder bump assemblies.

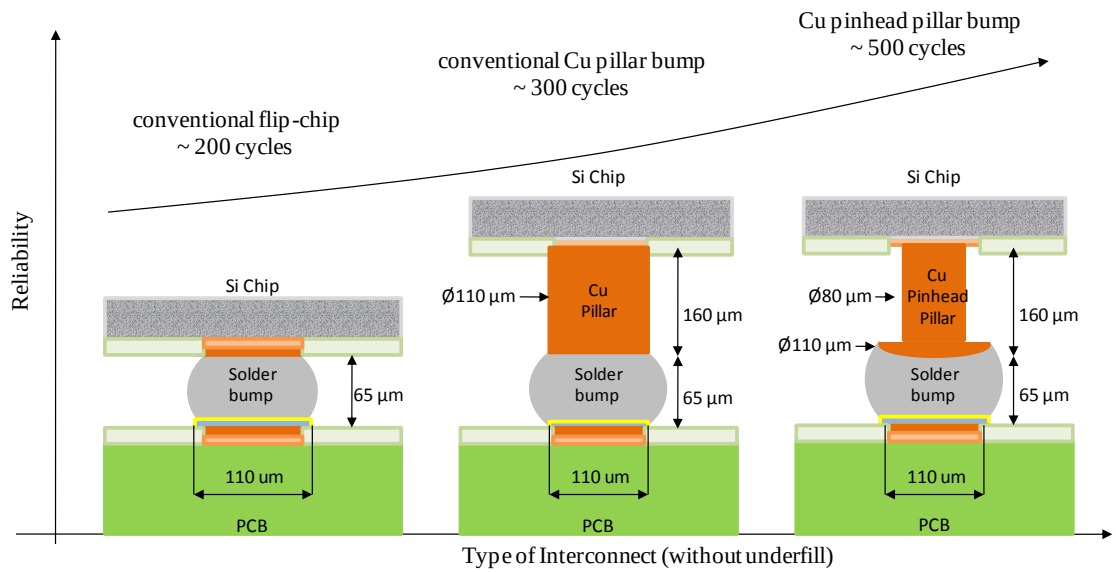


Figure 1.3 Concept of a Cu pinhead (CPH) pillar bump assembly and its predicted reliability

The specific objectives are as follows:

- i. Investigate the influence of Sn-Ag-Cu (SAC) solder bump volume and flip-chip UBM surface area on interfacial reaction and IMC growth
- ii. Conceptual design, CPH pillar solder bumping and assembly, FEM modelling, and reliability prediction of CPH pillar interconnection system.
- iii. Develop an electroplating process to fabricate CPH pillars, with an aspect ratio of up to two, on silicon wafers.
- iv. Characterize the shear strength, hardness, elastic modulus, crystallographic texture and microstructural properties of as-plated and annealed CPH pillars.
- v. Reliability assessment of CPH pillar solder assemblies in rapid temperature cycling (RTC), accelerated temperature cycling (ATC), electromigration tests and failure analyses.

1.4. Scope

The proposed Cu pinhead (CPH) pillar will be fabricated and its performance benchmarked against conventional flip-chip and Cu pillar interconnections. The novel CPH pillar designs and metallization schemes will be evaluated to establish a high performance interconnection scheme. The structures will incorporate features that can overcome or circumvent weaknesses observed in the solder bump interconnect. FEM modelling will be used to aid structural analyses and for designing test vehicles to assess the performance and reliability of the new interconnect structures. The reliability of CPH pillars assembled with SAC solder will be evaluated using RTC and ATC tests. Microstructures and electromigration behaviour of the CPH pillar and SAC solder bump assemblies will be investigated.

The five key areas of this research can be summarized as follows:

1.4.1 Investigation of SAC-Ni-Au UBM interaction in CPH pillar bumping process

Selecting a compatible UBM layer for SAC solder bumping is critical in the CPH pillar interconnection. In this study, various factors of SAC and Ni-Au interactions that may impact the solder interconnection reliability of CPH pillar will be investigated. The UBM is designed to tolerate multiple solder reflow and isothermal aging. The effect of pad area to solder volume ratio on interfacial reaction between Ni-Au UBM and SAC solder will be characterized. This understanding will enable us to determine an optimal UBM layer for the CPH solder bumping process.

1.4.2 Conceptual design and finite element analyses

The novel Cu pinhead (CPH) structure is designed to circumvent the weaknesses observed in the conventional flip-chip solder bump interconnect. A pinhead is incorporated onto the Cu pillar as a floating pad structure to improve interconnection compliance, high aspect ratio standoff height and soldering without direct contact with the silicon chip. Finite element method (FEM) modelling is used in the analysis of CPH pillar mechanical reliability. FEM simulation of CPH pillars with SAC solder bumps will be carried out to provide indicative reliability data and life expectation of CPH pillar structures with different aspect ratios.

1.4.3 Fabrication of Cu pinhead pillar structures

A wafer-level electroplating process for CPH pillars with an aspect ratio of 2 will be developed. A multi-step plating process to produce CPH pillars up to 160 μm in height using thick positive resist and DC current plating in a fountain plating cell will be evaluated.

1.4.4 Characterization of non-annealed and annealed CPH pillars

Electroplated CPH pillars will be heat treated at elevated temperatures to investigate the effect of annealing on Cu pillar compliance. The as-plated and annealed CPH pillars mechanical properties will be characterized by shear test and nanoindentation. The microstructures and crystallographic textures of the CPH pillars will be analysed by optical microscopy and x-ray diffraction.

1.4.5 CPH pillar bump assemblies accelerated reliability assessments and failure analyses

CPH pillar bumps assembled on FR4 substrates without underfill will be evaluated using 6 x 6 mm silicon test chips (with 36 CPH pillar bumps laid out in area array). The evaluation matrix includes as-plated pillars, annealed pillars and conventional flip-chips. SAC solder bumps will be used to form the solder joints. Rapid temperature cycling at 0-100 °C will be used for preliminary screening, followed by accelerated temperature cycling at 0-100 °C for standard benchmark reliability studies. Electromigration tests will be conducted to compare the performance of CPH pillar bump with conventional flip-chip bump.

The solder interconnection microstructures of the CPH pillar bumps, intermetallic compounds (IMC) and their growth kinetics will be characterized after temperature cycling and electromigration tests. The failure mechanisms of CPH pillar bumps assembled without underfill will be determined.

1.5. Structure of report

This thesis is organized into eight chapters:

- Chapter 1: Introduction, background, motivation, objectives and scope of research

- Chapter 2: Literature review, technology review summary and re-affirmation of objectives
- Chapter 3: Cu pinhead pillar bump conceptual design, FEM analyses and life prediction
- Chapter 4: Investigation of Sn-Ag-Cu solder and Ni-Au UBM interfacial reaction in CPH pillar bumping process
- Chapter 5: Electroplating process characterization and fabrication of Cu pinhead pillars
- Chapter 6: Non-annealed and annealed Cu pinhead pillars shear test, nanoindentation, microstructural analyses and x-ray diffraction crystallographic characterization
- Chapter 7: Rapid temperature cycling screening, accelerated temperature cycling and electromigration testing of CPH pillar and conventional flip-chip solder assemblies
- Chapter 8: Conclusions and further work recommendations
- References

Chapter 2 Literature Review

2.1. Introduction

The semiconductor technology roadmap can be traced back to the early 1970s where Moore's Law predicted that the number of transistors per IC would double every eighteen months. Today, the semiconductor industry is re-defining the trend with "More Moore Miniaturization" where a density increase on the device must come with improved performance. In addition, "More-than-Moore" aptly describes the migration of non-digital functionalities from PCB level into SiP and onto SOC levels (Arden et al, 2010). The dual trend of digital functions miniaturization and functional diversification as translated by The International Technology Roadmap for Semiconductors (ITRS) is shown in Figure 2.1.

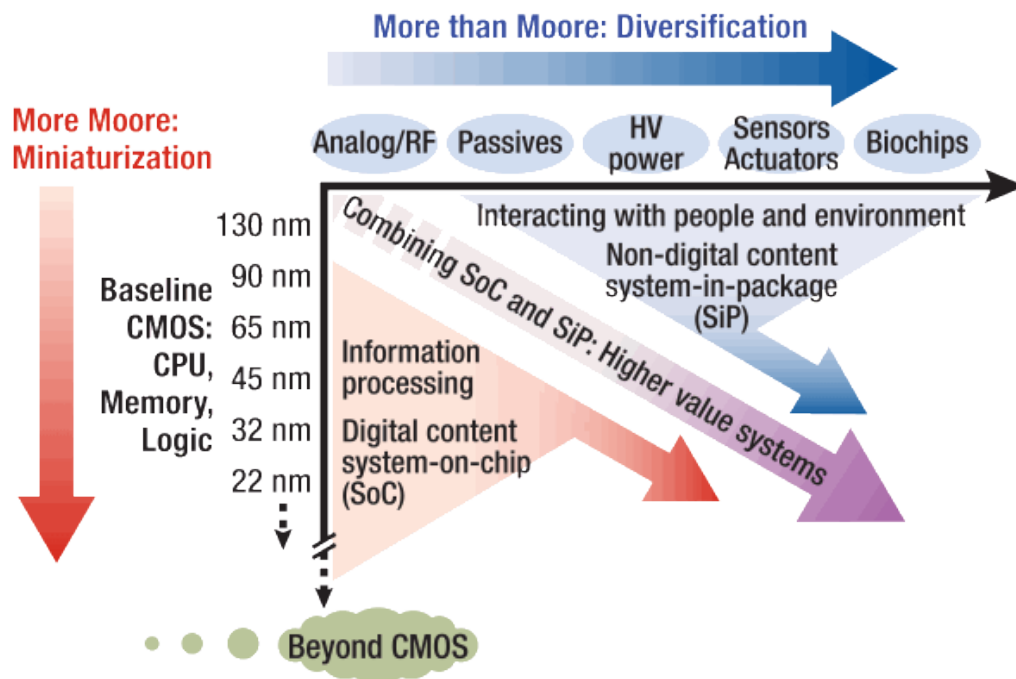


Figure 2.1 ITRS dual trend of miniaturization of digital functions in an integrated system (Arden et al, 2010)

2.2. Packaging Trend and Challenges

System-in-package (SiP) is an effective way to integrate small form factor systems that are often used in high density portable electronics. The variety of SiPs has expanded from simple stacked packages and multichip packages (MCPs) to more complex solutions as shown in Figure 2.2. With ultrafine pitches in the scale of 30 microns and less (ITRS, 2009) in some emerging SiPs, conventional solder bump interconnections may not meet the expected thermal, mechanical and electromigration reliability requirements.

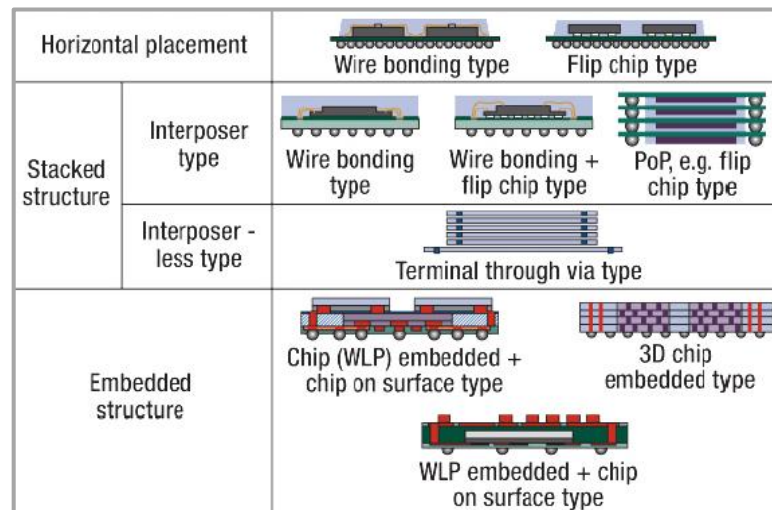


Figure 2.2 Major packaging and assembly formats for SiPs (*iNEMI 2009*)

As more functionalities and higher performance are packed into less silicon space, the interconnection density on the chip and board level will have to increase significantly. The interconnection layout will need to migrate from peripheral to area array layout for higher density packaging (ITRS, 2009). To reduce package form factors, the packaging industry have started to thin wafers and stack dies vertically in SiP assemblies (Kröninger et al, 2001, Takyu et al, 2008, Orii et al, 2009). A diverse set of structures and configurations in planar and 3-dimension are now being developed. Silicon ICs of different functionality and technology are being integrated

with passives, MEMS and optical devices into a single SiP (Swinnen, 2009, Arden et al, 2010, Johnson, 2011). As the pitch and height of an interconnection decrease, the present packaging technology has to overcome new challenges in chip-to-chip and chip-to-substrate interconnections. When solder bump size decreases, bump uniformity become more critical and yield will be affected due to bump non planarity. Underfilling IC chip with low standoff and highly populated interconnects will be difficult (Orii et al, 2009). IMC to solder volume ratio will increase as solder bump diameter shrinks, and brittle failure at solder interface is a concern (Salam et al, 2001, Huang et al, 2005, Park et al, 2011). Electromigration of solder interconnections is an issue when current density increases with decreasing bump size and pad geometry (Korhonen et al, 1993, Ye et al, 2003, Tu, 2007, Lin et al, 2008, Chang et al, 2010). Using brittle low-K dielectric materials to reduce on-chip interconnect parasitic capacitance in SiPs can pose serious thermomechanical reliability concerns (Heinen et al, 1989, Yeoh et al, 2006, Cheng et al, 2010), if a large CTE mismatch exist between the silicon chip (2.6 ppm/°C) and organic substrate (17 ppm/°C). Despite the adaptability of Cu pillar bump technology for high density interconnection, the high stiffness of Cu pillar remains a concern when used in low-k chip interconnection. In addition, the mechanical properties and reliability performance of electroplated Cu pillars are not widely reported (Tummala et al, 2006, Liu et al, 2009). These package integration challenges have provided the motivation to develop a compliant interconnection that can minimize mechanical stress on the chip and is adaptable for a wide range of packaging formats.

2.3. Review of compliant array interconnect structures

In this review, stacked and stretched solder bumps, novel compliant structures, and Cu pillar-solder interconnections will be discussed. The wire-bond interconnect

will not be reviewed as it is limited to peripheral bonding. Taking total costs and performance into consideration, array interconnection will be the dominant technology for future system and package integration.

2.3.1. Solder bump

The solder bump interconnection was developed by IBM in the early 1960s for flip chip assembly. Solder bump alloy has evolved from high lead and tin (Pb95/Sn5 %) to eutectic tin-lead (Sn63/Pb37 %). The solder bump has an inherent self-aligning behaviour during reflow solder which gives the solder bump assembly an excellent yield. However, after reflow the solder ball assumed a truncated sphere or barrel-shaped structure with a relatively low height and large circumference. This low aspect ratio creates high stiffness and non-uniform strain concentration at the interconnect interfaces. Cracks and fractures can occur at the interfaces of the bump interconnection when there is a mismatch in CTE between the chip and substrate leading to creep and fatigue in the solder joints.

To relief the stress concentration at the neck of the bump, Flip Chip International (FCI) introduces a polymer collar that wraps around the solder bump (Elenius et al., 2000). Figure 2.3 shows a conventional flip-chip solder bump with and without a polymer collar. The FCI test data shows that, with a polymer collar reinforcement, Sn-Pb solder bumps on a 10 x10 array CSP with 0.5 mm pitch and a distance of 3.2 mm from the neutral point (DNP) can survive over 1000 temperature cycles at -40 to 125°C without underfill. However, underfill is recommended for bigger chips.

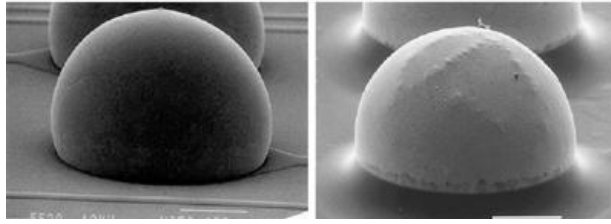


Figure 2.3 (a) Typical solder bump (b) FCI solder bump with polymer collar

2.3.2. Stacked solder bumps

The shape of a solder joint is controlled by the solder surface tension forces acting on the molten solder ball and the interconnecting pads. The truncated solder sphere typically has a ratio height / maximum diameter of 0.7 or less. Since strain is inversely proportional to the height of a solder joint and fatigue life is inversely proportional to the square of strain, a relatively small increase in the solder joint height or its diameter would extend its life in operation significantly. To increase the solder height, two solder balls of different melting temperatures can be stacked vertically.

Nippon Telegraph and Telephone (NTT) Electrical Communications Laboratories have developed a technique using a polyimide sheet deposited with solder bumps as an additional bump layer to be stacked and reflowed on a bumped substrate (Matsui et al., 1987). Copper (Cu) is used as the wetting layer and Ti as the diffusion barrier in the polyimide substrate pads. The Cu-Ti-Cu layer serves as the bump-limiting metal (BLM) to support the bumps through multiple reflows, see Figure 2.4. This technique allows multiple solder bumps with the same melting point to be stacked and reflowed simultaneously in the assembly process.

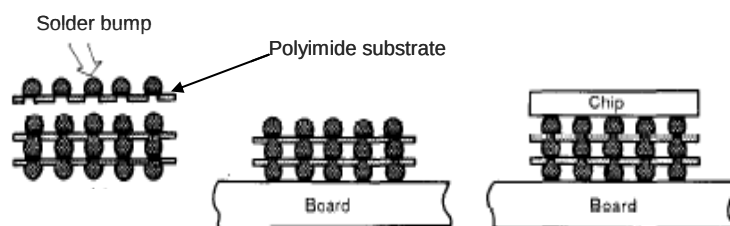


Figure 2.4 NTT stacked solder bump interconnections (Matsui et al., 1987)

IBM disclosed a method where an elongated solder structure can be formed on a pad and capped by solid metal or encapsulated at the side to retain its height (Agarwala et al., 1992). Further elongated solder mass can be deposited on the first solder structure. The bump stacking can be produced by an electroplating process, stencil printing or ball placement on the wafer. However, each bump stack will need an additional BLM to prevent inter-diffusion among adjacent bumps. The thin film and masking processes to produce the ball limiting metal (BLM) can be costly.

The Institute of Microelectronics and Reliability (IZM-Berlin) has developed a WLP process to produce double-bump structures on a wafer as shown in Figure 2.5. The process begins with a benzocyclobutene (BCB) or polyimide (PI) coating with patterned metallization pads for re-routing, followed by under bump metallization (UBM) deposition by electroless or electrolytic plating and finally solder bumping by stencil printing (Topper et al., 2000). To improve the package reliability, Motorola and IZM have jointly developed a double-bump wafer-level chip scale packaging (WLCSP) process. A stress compliant layer of polymer is added over the bumped surface. A planarization step follows to flatten and expose the first set of bumps for a second bumping process to take place. As the 2-bump structure is partially reinforced by a compliant polymer layer, the reliability life time can be significantly improved.

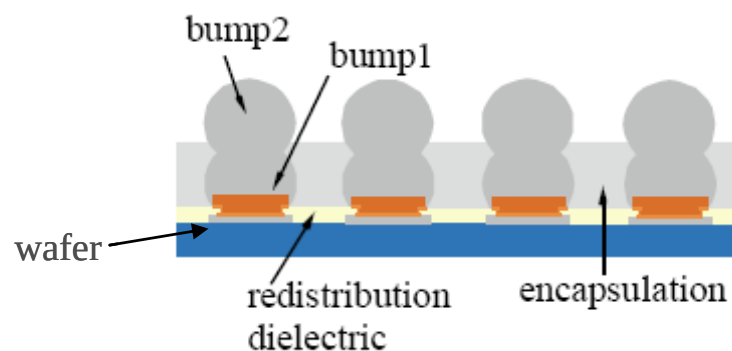


Figure 2.5 IZM and Motorola double-bump interconnect (Topper et al., 2000)

2.3.3. Stretched Solder Column (SSC)

The techniques to generate stretched solder columns or bumps, as shown in Figure 2.6, when mounting electronic devices on substrates, were reported separately by AT&T and Motorola (Schmidt et al., 1992). The Institute of Microelectronics (IME) has disclosed a novel way of producing stretched solder columns at wafer level which is much more productive than the preceding techniques (Wong et al., 2005). This is accomplished by using two wafers; a standard (functional) wafer that contains the ICs and a master (dummy) wafer that has an array of solder bumps that is a mirror image of those on the functional wafer. After alignment, both sets of solder bumps are melted and then slowly brought together until they are in contact. Then, as the solder bumps cool down, they are slowly pulled apart thereby stretching the merged solder columns. Once the latter have fully solidified, they are separated from the master wafer.

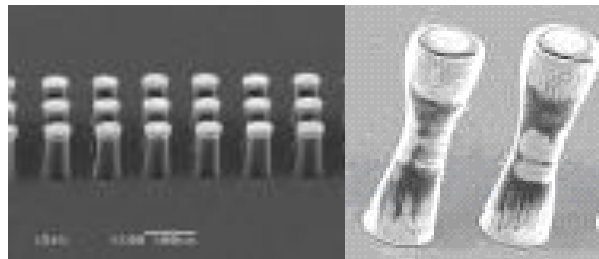


Figure 2.6 AT&T and Motorola stretched solder column (SSC) interconnect (LoVasco et al., 1989)

Experimental and simulation results have shown that crack initiation and propagation is found away from the chip interfaces and near the throat of the SSC (Satoh et al., 1991, Lau and Pao, 1997). The fatigue life of SSC was reported to be between 1500 and 3000 cycles on an organic substrate assembly. The SSC is an innovative way to re-structure solder bump to give a better mechanical performance. The new structure is able to transfer the inherent weakness at the interconnect

interfaces to the bulk material in the column. If the column can be made of a high fatigue resistance material, the SSC interconnect will be an excellent joint. The SSC is typically made of high Pb solder (Pb-Sn10%). The joint is normally made with eutectic Sn-Pb solder which has good reliability and manufacturability.

2.3.4. Copper Pillar Bump

Various Pb-based pillar structures in the Ceramic Column Grid Array (CCGA) format have been used for many years to increase the solder joint height as a way of overcoming the strain from CTE mismatch between alumina ceramic chip carrier and epoxy glass PCB (Ray et al., 1999, Master et al., 1995, Ray et al., 1997). In preparation for the Pb-free implementation, the Cu Column Grid Array (CuCGA) module was introduced (Interrantte et al., 2003) – see Figure 2.7. Sn-Ag which has a slightly higher melting temperature is used as the first-level solder and Sn-Ag-Cu as the second-level solder. This combination of Pb-free alloys is feasible because copper columns, with m.p. of 1083°C, remain rigid and the package standoff is maintained even as the Pb-free solder alloys soften during the second reflow. Experimental data (Interrantte et al., 2003) has shown that CuCGA can survive over 1400 temperature cycles at 0 to 100°C. The CuCGA evaluated is a large ceramic package, 42.5 x 42.5 mm, used in IBM high performance workstations. The tin plated copper columns used in CuCGA have a diameter of 0.25 mm and length 1.5 mm. The Cu columns could be soldered or casted on the ceramic chip carrier and subsequently attached to the PCB by soldering (Ray et al., 1997). Considering the CTE of IBM ceramic substrate is typically 3 ppm/°C and epoxy glass PCB 17 ppm/°C, the reliability of CuCGA is excellent using a Cu column interconnection. However, attaching sub-100 µm copper pillars in high density on a wafer or bare chip by soldering or casting is not feasible.

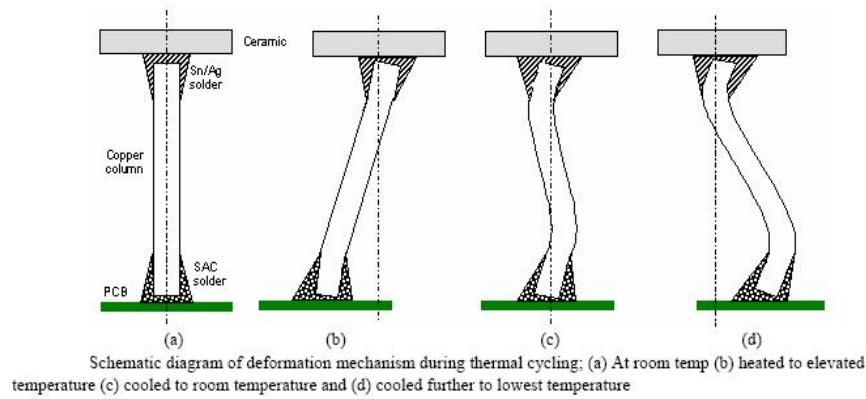


Figure 2.7 IBM Copper Column Grid Array (CuCGA) (Interrante et al., 2003)

To address the high reliability and fine-pitch interconnect challenge for the new generation microprocessors, Fujitsu developed the Wire Interconnect Technology (WIT). WIT is essentially high density copper pillars of 10-15 μm in diameter and 50 μm in height plated on silicon (Love et al., 1994, Lau and Pao, 1997). WIT with a pad pitch of 40 μm has been demonstrated and tested for reliability. This pitch allows up to 62,500 I/O per cm^2 . Figure 2.8 shows WIT fabricated on a wafer with a 40 μm pitch for bonding on 25 μm pads using solder.

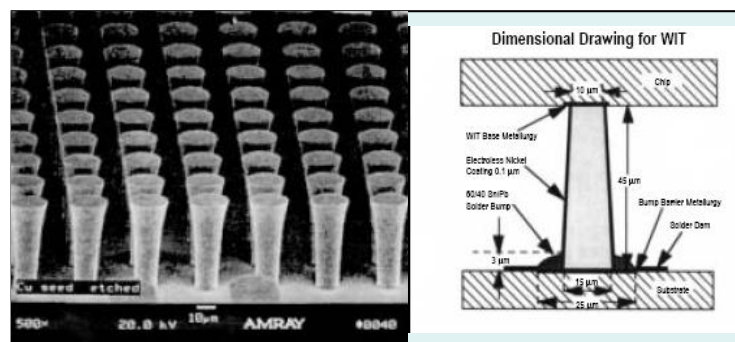


Figure 2.8 Fujitsu Wire Interconnect Technology (WIT) (Love et al., 1996)

The small bond pad greatly reduces the bond pad capacitance. The short path helps to reduce parasitic inductance and resistance, and reduce the demand for routing interconnects on the chip surface. Initial studies in a power cycling test between 70 and

150 °C have shown that WIT without underfill could be 10 times more reliable than a controlled collapse chip connection (C4) flip-chip assembly (Love et al., 1996). All the failures occurred in the Sn-Pb solder joints in the evaluation. The reason for the improvement in reliability is attributed to the high aspect ratio of the Cu pillars. While the C4 joint is almost entirely in shear stress, most of the WIT joint is in bending, imposing a very small amount of shear on the solder portion of the WIT. This technology has great potential as the high aspect ratio (≈ 3.0) pillars can be structured and designed to straddle across chips in 3D chip stacking.

The Cu pillar has the advantage of increasing the height without increasing the diameter. This is not the case for solder bump; any solder bump height increase is accompanied by a diameter increase. The aspect ratio of height over diameter is 0.7 or less. So far this has limited the use of flip-chip to planar high density interconnection. Long loop wire bonding is still used for multi-stack interconnections.

A Cu pillar technology has also been developed by NEC (Tsukamoto et al., 1997), Megic (Lee et al., 2002), Advanpack Solutions (APS) (Tung et al., 2003) and Aptos (Lei et al., 2006). NEC suggested that a sufficient solder volume should be used to attach the Cu pillar to the next level, thereby forming a solid core within an hour-glass shaped solder joint – see Figure 2.9. It claimed that the maximum stress on the interconnection was half of that in a typical barrel-shaped solder joint.

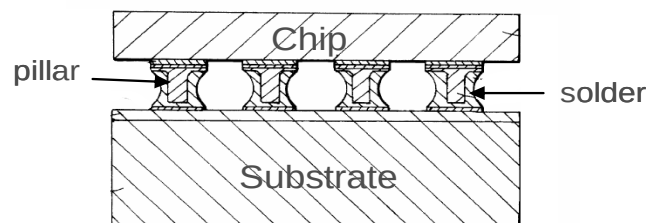


Figure 2.9 NEC solid core hour-glass shaped solder interconnect

Megic and APS proposed a very similar process where the Cu pillar is pre-deposited with a layer of solder to be used for assembly to the next level. APS has reported that their Cu pillar interconnection passed 1000 temperature cycles in the reliability test (Wang et al., 2001). The Cu pillars have an aspect ratio of 1.0 and the die size is 10 x 10 mm. The Cu pillar bump manufacturing process of APS is shown in Figure 2.10.

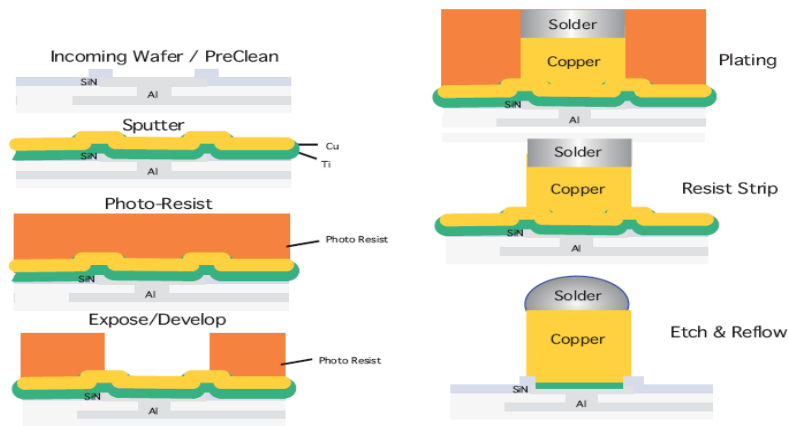


Figure 2.10 APS Cu Pillar Bump (www.advanpack.com)

2.3.5. Novel compliant interconnects

S-shaped Micro-spring Interconnect (Garrou, 2000): An “S” shaped micro spring is formed on the bond pad using gold wire bonding and then plated with electroless nickel and gold as shown in Figure 2.11.



Figure 2.11 S-shaped micro-spring interconnects by Form Factor (Garrou, 2000)

Notwithstanding the unique shape of the spring interconnection, a conventional wire bonder with some modification and standard plating process can be used to fabricate it. However, the springs are formed sequentially, thus this process may not be adopted for high I/O and area array packaging.

Micromachined Flexible Interconnect (Joung and Allen, 2001), see Figure 2.12. Step, bridge or semi-spiral structures can be fabricated by three masking steps using conventional lithography and wet processes. The compliance of these structures can normally go up to 50 μm to the wafer surface.

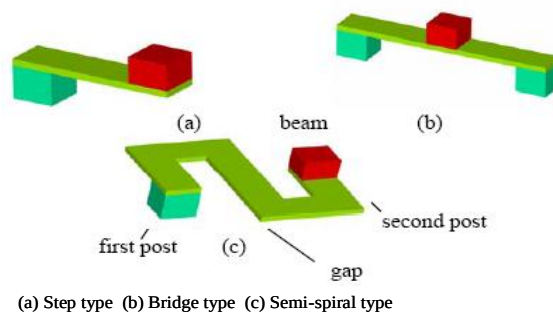


Figure 2.12 Micromachined flexible interconnects (Joung and Allen, 2001)

Sea-of-Leads (SoLs) (Bakir et al., 2003): SoL, as shown in Figure 2.13, is a metallic lead deposited over a polymer air cushion. The lead is made of copper or gold. Except for the portion exposed for soldering, the rest of the lead is covered by a non-wettable metal which can be titanium (Ti) or chromium (Cr). An interconnection density of more than 10,000 per square cm has been demonstrated. The SoL structures are fabricated using a MEMS-based micro fabrication process involving four masking steps. The process steps are very involved. Repeatability and maintaining good bump yield may be a concern, particularly in the fabrication of the polymer air cushion.

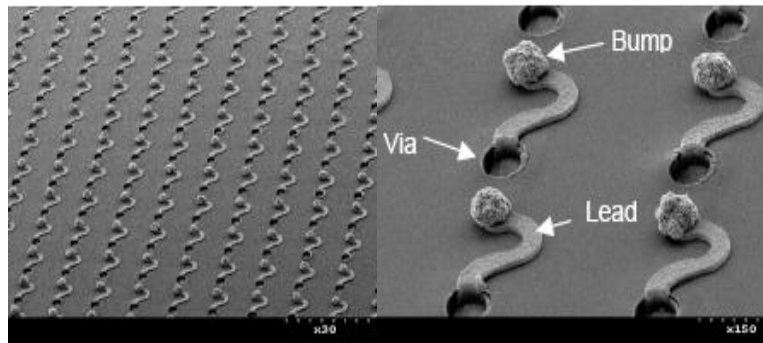


Figure 2.13 Sea-of-Leads interconnect (Bakir et al., 2003)

One-Turn Helix (OTH) (Zhu et al., 2002): The interconnect structure has good mechanical compliance in three dimensions. The structure, as shown in Figure 2.14, can be fabricated using a series of lithography, etching and electroplating processes. It was found that a thin and narrow beam with large radius and tall post had an excellent mechanical compliance but did not have good electrical performance. A certain trade-off is needed in the mechanical and electrical design to optimize the OTH structures and research in this area is still on-going.

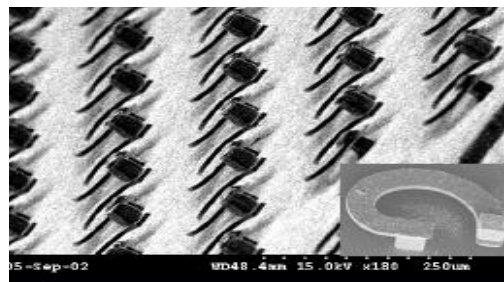


Figure 2.14 One-Turn Helix interconnect (Zhu et al., 2002)

J-Springs (Ma et al., 2002): The micro-springs are made by layering plated nickel with different stresses on a spring metal to give the desired gradient. The final structures are then plated with hard gold to enhance electrical and mechanical contact.

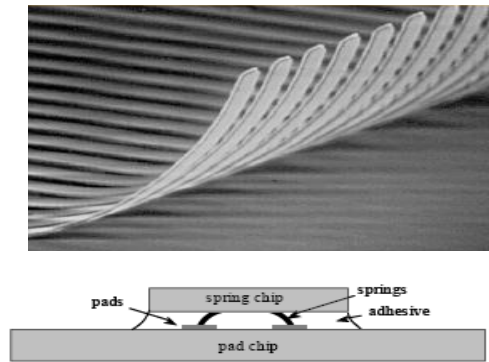


Figure 2.15 J-Spring interconnect (Ma et al., 2002)

The fabrication flow follows a typical MEMS process where Ti is used as an adhesion layer to silicon and Au as a seed layer where spring metal is deposited. Flip-chip with J-springs can be assembled without using solder (Chow et al., 2005). As shown in Figure 2.15, the contact between the chip and substrate can be sustained by compression using a UV curable underfill. Stiction of spring structure and its peel strength are issues that require further investigation.

The compliant interconnect concepts discussed in this section give a new perspective to future packaging. However, the major drawback of these novel structures is that their fabrication processes is complex and manufacturability is questionable. There is also a lack of performance data to verify their reliability. The prospect of industry adopting any of these concepts is unlikely in the short-term.

2.4. Discussion

Thirteen different compliant interconnect structures were analysed in this review. They can be broadly categorized as stacked solder bumps, stretched solder column, Cu pillar and novel spring-type interconnects.

The stacked solder structure is comprised of a solder material in the form of a bump or stud. The solder is stacked consecutively to achieve its desired height and compliance. There are several key issues in such an approach. A solder material with a

lower melting temperature will be needed for each subsequent stack in order for the stacked structure to retain its integrity and intended geometry. Alternatively, a polymer film such as polyimide is needed at the base and intermediate layer, in order to hold the solder bumps in place for subsequent stacking. The probability of a misalignment yield loss to occur will increase with each consecutive stack.

The stretched solder column (SSC) involves two levels of soldering to join two columns together for a subsequent stretching process. However, the lead-free implementation for electronics manufacturing (IPC, 2006) has created a lot of uncertainties in the reliability of solder interconnections, particularly for the SSC which requires two solder alloys that have a wide reflow temperature difference to effect first- and second-level soldering. If Pb-free solder alloys are used for the SSC, their feasibility and reliability have to be re-evaluated. A possible two-solder combination for a Pb-free SSC is to use a Sn-Ag-Cu or Sn-Ag solder that has a higher melting point (m.p.) solder and a Tin-Bismuth (Sn-Bi) solder which has a lower melting temperature for attaching the SSC during assembly. Sn-Bi50% solder, with a melting point of 139°C, is a good second-level solder if the SSC is made of Sn-Ag-Cu (m.p. 217°C) or Sn-Ag (m.p. 221°C) solder. However, the m.p. of Sn-Bi solder is too low for many electronics applications. Furthermore, if Sn-Bi alloys were contaminated by Pb, which could come from the pre-tinned layer on components and pads, these alloys may form a ternary eutectic that has a m.p. of 95°C (Moon et al., 2001). Such a low m.p. ternary eutectic will degrade the functional properties of a solder joint.

The novel spring-type structures offer some very interesting approaches for designing compliant interconnections. Most of these structures require two to four lithography steps and the complicated structures pose significant manufacturing challenges. One can imagine that a die shrink or pad layout change will trigger major

efforts to re-model and re-design a spring-type compliant structure. Maintaining structural uniformity on the cross-sections, curves and release angles of these spring structures are critical for the compliant structures to function with predictable reliability. Hence, the scalability in manufacturing for such novel designs is questionable.

The Cu pillar structure holds the greatest potential to provide flexible and compliant interconnections for fine-pitched devices and 3D integration of heterogeneous digital and analogue devices. The appeal of a Cu pillar is its simplicity in design, manufacturability and compatibility with Pb-free solders. The Cu pillar is especially attractive as interconnection density increases because Cu pillar bumps can be fabricated at wafer-level. Major semiconductor manufacturers like Intel, Texas Instruments, Amkor and Advanced Semiconductor Engineering (ASE) have indicated that they are already qualifying or implementing Cu pillar bump technology into their packages (Baliga, 2006, Cheng et al, 2010 and Gerber et al, 2011).

In spite of the inherent advantages of a Cu pillar interconnection, concerns on thermomechanical reliability have been reported when Cu pillar bumps are used in ultra low-k chip packaging. This is due to the much higher stiffness of Cu (Cu elastic modulus is approximately 110-128 GPa) compared to that of SAC solder (SAC solder elastic modulus is 46-54 GPa). Mechanical failures in low-k interlayer dielectric beneath Cu pillars, and delamination between Cu bumps and Al bond pads have been observed (Heinen et al, 1989, Yeoh et al, 2006, Wang et al, 2010 and Cheng et al, 2010). Hence, further improvement on the compliance of the Cu pillar bump structure is necessary for high density interconnection on chips with low-k interlayer dielectric.

With a CPH pillar interconnection, a higher density interconnection can be accomplished on chip-to-chip and chip-to-board packages. Displacement due to CTE

mismatch on a CPH pillar structure is taken up by bending the pillar, and hence greatly reduces the shear strain on the chip interfaces. With an inherently higher thermal conductivity (386W/mK) for Cu as compared to that of SAC solder (59W/mK), this means that CPH pillar solder interconnection can provide a ten-fold improvement in thermal transport over a SAC solder bump interconnection. Strategic sizing and positioning of CPH pillar bumps at hot spots on the silicon chip can significantly improve the thermal management of the device. As a result, lower stress will be transmitted to the low-k dielectric material which is prone to stress delamination.

It can be seen in Figure 2.16 that a conventional flip-chip interconnect is not well suited for 3D IC stacking. The inherent weakness of solder bump collapse after reflow is a severe limitation for fine pitch integration. The conventional Cu pillar is better suited for 3D IC integration, barring some of the limitations discussed in the preceding section. With a CPH pillar compliant structure, the interconnect reliability at the fragile low-k chip interface can be enhanced, even without underfill.

To assess the cost implications in adopting the CPH pillar interconnection without underfill, the costs of wafer bumping, underfill material, equipment and fixed manufacturing overheads were considered. The cost for solder bumping a 6-inch wafer is approximately US\$50. Each wafer can yield 320 (6x6 mm) chips. The solder bumping cost per chip is US\$0.16. The cost of CPH pillar bumping is estimated at \$65 per wafer, which is higher than conventional bumping, due to the high aspect ratio requirement of CPH pillar bumps. The cost of each 6x6 mm CPH chip is US\$0.23. A typical underfill material is US\$60 per 20 gm and each chip is assumed to consume \$0.08 of the underfill material. While each CPH pillar chip costs US\$0.07 more than a conventional solder bump flip-chip, there is still a net saving of US\$0.01 without using underfill. In a conventional flip-chip assembly line, there are five stations which

comprise of (i) flux dispensing, (ii) chip placement, (iii) reflow, (iv) underfill and (v) oven curing. The cost of an underfilling station is approximately US\$150,000 and a curing oven is US\$50,000. Hence, there is a total capital equipment cost of US\$200,000 for the underfilling process. The total floor space for the underfilling process is about 7 m². The monthly overhead per m² of clean-room space is approximately US\$65 (Ralf et al, 2000). The manpower cost for operating the underfill stations can be assumed to be US\$3000 per month. The combined space and manpower overhead annually to operate the underfill process would be \$41460. Finally, the underfilling process, including curing time, could be 15 to 150 minutes, depending on the underfill material used. The marginal increase in CPH wafer bumping cost can be easily offset by the substantial saving in capital costs, process time and manpower, if the underfilling process is eliminated. Hence, there will be significant cost benefits if a reliable CPH pillar interconnection can be implemented without using underfill.

2.5. Summary

In this literature review, stacked solder bump, stretched bump, Cu pillar and spring-type interconnects were analysed. The stacked solder bump approach has the inherent weaknesses of solder bump collapse, IMC interfacial reaction with the UBM on the chip and stress concentration. Pb-free solder implementation has rendered the performance of the stretched solder column unpredictable as this structure was initially developed and tested using high-Pb and eutectic Sn-Pb solders.

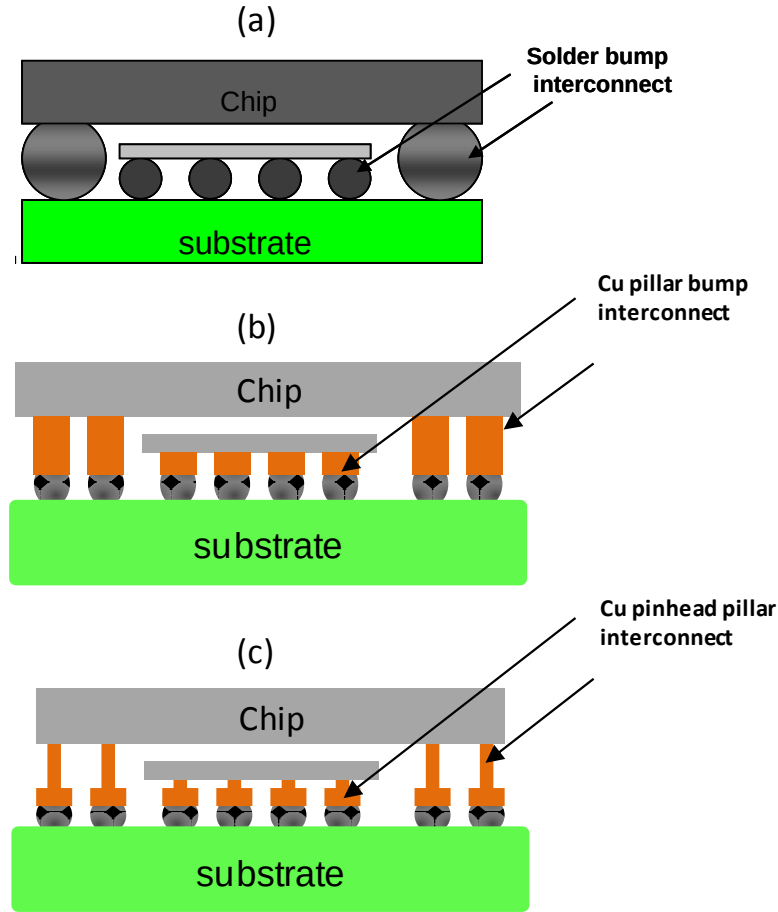


Figure 2.16 3D silicon chips stacking with (a) conventional flip-chip solder bump interconnections, (b) conventional Cu pillar bump interconnections and (c) Cu pinhead pillar bump interconnections

The novel spring-type interconnections reviewed require complex fabrication processes which will be costly to implement. The limitation of conventional the Cu pillar is that its structural compliance cannot be adjusted without affecting the interconnecting pad or its height.

The proposed CPH pillar offers a good structural compliance, design flexibility, superior thermal conductivity and the potential to assemble without underfill. A patent has been granted to the author for the invention of the novel CPH pillar structure and its related fabrication methods. A CPH pillar interconnection can be implemented easily

using the existing packaging infrastructure and process flow. Figure 2.17 illustrates a 3D packaging method using two levels of CPH pillars.

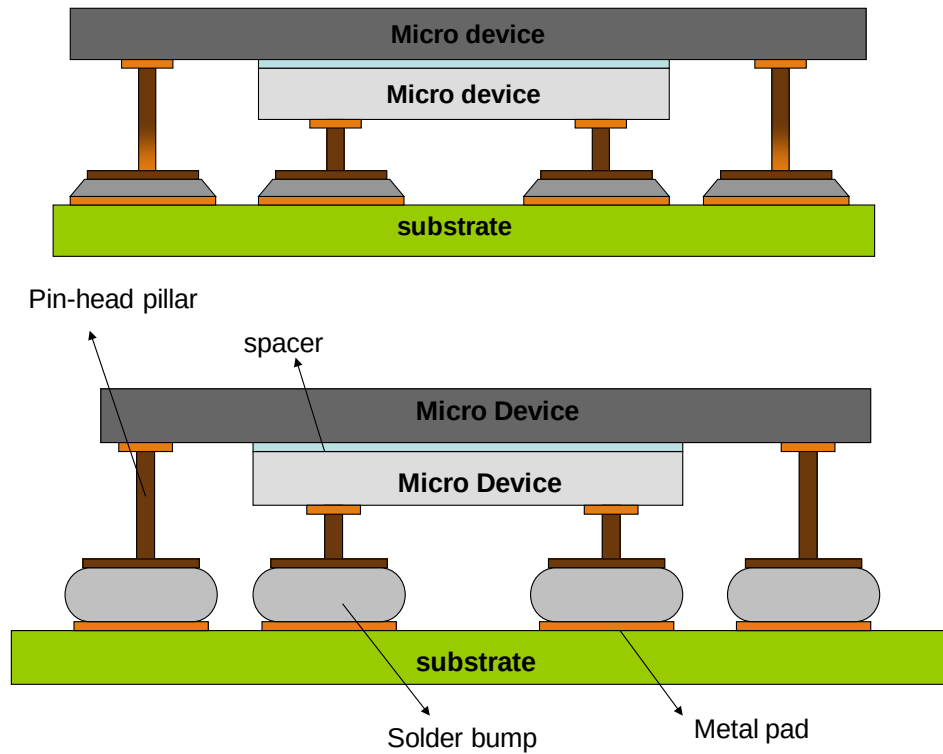


Figure 2.17 3D IC integration using two levels of CPH pillar interconnects

With major packaging manufacturers like Amkor and ASE already implementing the conventional Cu pillar bump technology in their production, and with Intel using Cu pillars in its high-end microprocessors, the additional benefits that the CPH pillar solder interconnection can offer are likely to pave the way for the CPH pillar solder interconnection adoption by the industry in the near future.

Chapter 3 Investigation of Sn-Ag-Cu Solder and Ni-Au UBM Interfacial Reaction in Flip-Chip Solder Bumping Process

3.1 Introduction

The under-bump-metallization (UBM) serves as a barrier and wetting layer on the CPH pillar. In this study, various aspects of the SAC solder and Ni-Au interactions that may affect the solder joint reliability of a CPH pillar will be investigated. The effect of pad area to solder volume ratio on the interfacial reaction between the Ni-Au UBM and SAC solder will be characterized. This understanding will enable us to determine an optimal UBM layer for the CPH solder bump attachment.

The SAC solder with a melting temperature of 217°C is the main Pb-free solder alloy that is recommended to replace Sn-Pb solder in reflow soldering of microelectronics (IPC, 2006, iNEMI, 2006). The SAC solder is short-listed because of its superior mechanical properties and its good wettability with copper and nickel surfaces. An in-depth review on Sn-Ag, Sn-Cu and SAC solder alloys can be found in (Kang et al., 2005, Puttlitz et al., 2004, Zeng and Tu, 2002, Anderson et al., 2001, Plumbridge et al., 2001).

With the projection that interconnection pitches will decrease from 150 μm today to 50 μm in 2020 (ITRS, 2009), the surface area of pad metallizations and solder materials used in interconnect structures will reduce in tandem. Understanding the volume effect of the SAC solder on IMC growth, UBM degradation and shear strength of solder bump interconnect structures will be crucial in the design and development of the next generation packages.

3.2 Sn-Ag-Cu solder interaction with Cu and Ni-Au UBM

The formation and growth of IMC in Pb-free solders have been investigated extensively (Bader et al., 1995, Korhonen et al., 2000, Zribi et al., 2001, Zeng and Tu, 2002, Ho et al., 2002, Kang et al., 2002, Jurenka et al., 2005). In general, the findings show that substrate or UBM with Cu have a high dissolution rate in molten Pb-free solders. Ni metallization with immersion Au is found to be a better wetting and barrier layer to interface with Pb-free solder. In the soldering process, IMC is formed as an interfacial layer between solder and pad metallization. The rate of IMC growth in the wetting stage is very fast. IMC continues to grow during the solid state aging process but at a much slower rate. One way to compare IMC growth rate in wetting reaction and solid state aging is to compare the time taken to form the same amount of IMC. K.N. Tu (Tu et al., 2000) reported that it took a few minutes in wetting reaction at 200° C to form an IMC layer between SnPb and Cu,. But in solid state aging at 170° C, it took 1000 hours. This means in SnPb solder-copper substrate reaction, the IMC growth during wetting reaction can be three to four orders of magnitude faster than IMC formation in solid state thermal aging.

In previous studies, the volume to area (V/A) ratio of copper metallization and SAC solder has been investigated (Salam et al., 2001, Islam et al., 2005). The investigations were carried out on relatively large copper pads of 0.5 mm to 3.6 mm. It was found that V/A ratio had an influence on IMC thickness formed in the wetting reaction. Thicker IMC layers were observed for lower V/A values. Salam et al reported that the IMC thicknesses formed between SAC and Cu pads under different V/A ratios levelled up after 100 hours of solid state thermal aging at 120°C. It was concluded, after 300 hours of solid state aging, that solder volume did not have a significant effect on IMC growth in solid state aging. Islam et al reported that lower

V/A ratio produced a thicker IMC layer on the Cu pad in SnAg reflow soldering. Similar work was carried out by Choi W.K. and his co-researchers (Choi et al., 2002) using 0.9 mm diameter Cu balls coated with Sn or NiSn. It was observed that the V/A ratio of solder volume and metal pad area could influence metal dissolution and diffusion. They explained that as the distance for metal diffusion was longer in larger volumes of solder, the time to saturate molten Sn with Cu would be longer. Therefore IMC growth in a larger volume of solder was slower.

In our study, the objective is to determine SAC solder and Cu-Ni UBM interaction and IMC growth in various solder bump sizes. The specifications of the test samples are given in Table 3.1. The V/A ratio was not held constant as B250 scaled down to B80. When B80 was scaled down to B40, the V/A ratio was constant.

3.3 Experimental Procedure

Test coupons were prepared using 6-inch silicon wafers. An adhesion layer of TiW (0.1 μm) and a seed layer Cu (0.5 μm) were sputtered on a 6-inch silicon wafer. The sputtered wafer was subsequently electroplated with Cu and Ni. An immersion Au layer was added over Ni to complete the TiW/Cu/Ni/Au UBM structure. The TiW/Cu/Ni/Au UBM scheme is preferred to TiW/Cu/electroless Ni/Au and TiW/Cu schemes because Ni has a much slower reaction rate with high tin content Pb-free solders and is shown to be more stable than electroless Ni (Korhonen et al., 2000, Kang et al., 2002, Zeng and Tu, 2002). . A BCB passivation layer was spun on the metallized layer and patterned with the desired openings for solder bumping. The test coupon structure is shown in Figure 3.1

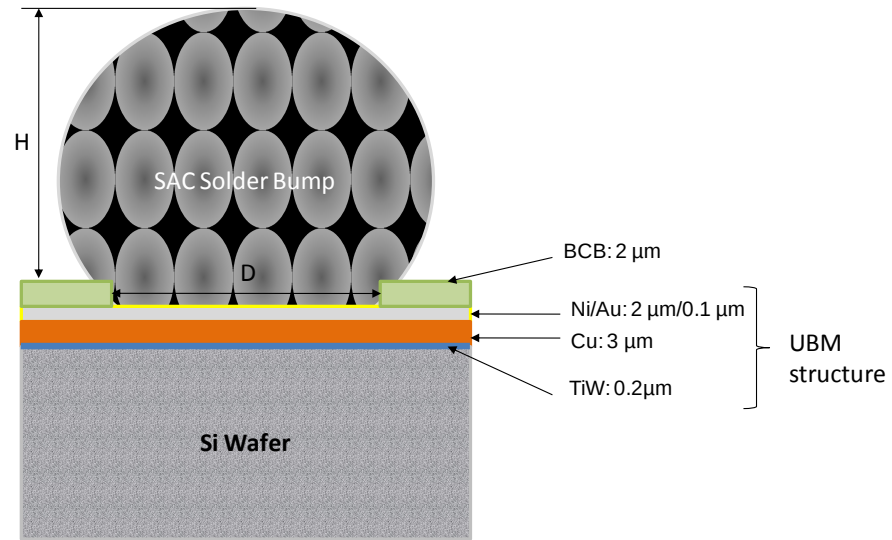


Figure 3.1 UBM structure on silicon test coupon

3.3.1 Stencil printing

Three types of test silicon wafers with pad sizes of 250, 80 and 40 μm respectively were prepared for solder ball size effect and IMC-UBM interaction studies. A Sn-Ag3.5%-0.5%Cu solder paste with 15-25 μm solder particles sizes (type 6) and 90% metal loading was used. The paste was deposited on test wafers by a fine-pitch Micro-Tec printer, using a polyurethane squeegee and polyester stencil. Solder bump reflow was carried out in a nitrogen-purged hot plate with 3-stage (preheat-reflow-cooling) heating. The peak reflow temperature was 245° C with a dwell time of 90 seconds.

3.3.2 Paste Shrinkage Factor

Theoretically, when uniform spherical solder particles are pushed into an aperture in a stencil, they assume a face-centred cubic (FCC) lattice packing arrangement. The packing factor (PF) is defined as:

$$PF = (\text{Volume of spheres in a unit cells}) / (\text{Total unit cell volume}) \quad (3.1)$$

The packing factor of FCC is 0.74. However, solder powders are suspended by flux with a metal loading of 89 -90 %. Hence, the PF is computed to be 0.65. Taking particle size variation and void into consideration, the industry rule-of-thumb states that the shrinkage factor (SF) of solder paste after reflow is 0.5, which is slightly lower than the theoretical PF.

3.3.3 Paste Transfer Rate

In the case of stencil printing, besides SF, there will be a further reduction of solder volume due to solder particles adhering to the stencil wall during stencil lift-off at the end of the printing process. The transfer rate (TR) is dependent on paste viscosity, aspect ratio of stencil aperture diameter to thickness (AR1), area ratio of aperture area to aperture wall and printing parameters (AR2). Establishing the TR of stencil printing is important as this is a determining factor for solder bump uniformity on the wafer. In order to determine the TR rate of the printing process in this study, a sample of five reflowed solder bumps of 250, 80 and 40 μm diameter were x-sectioned and measured - see Table 3.1. The truncated sphere volume formula (Li, 1998) for calculating the reflowed solder bump volume (V_{actual}) is based on the metal pad diameter (D) and bump height (H) measured after reflow, as shown in Figure 3.1.

$$V_{actual} = (\pi / 6) H (H^2 + 3 [D/2]^2) \quad (3.2)$$

Table 3.1 Bump Dimensions

Geometries of Sn-3.5%Ag-0.5%Cu Solder Bumps after reflow (Average of 5 samples)			
Size Parameters	Large (μm)	Medium (μm)	Small (μm)
Max. Bump Diameter	260	100	60
Pad Diameter: D	250	80	40
Bump Height: H	150	70	48

The volume of solder paste printed into the stencil aperture is a cylindrical volume given by V_{paste} , Eq. (3.3). The actual amount of solder paste that is transferred to the wafer is lesser as the transfer rate (TF) is not 100% efficient due to solder particles adhering to the stencil wall. The final solder after reflow is affected by SF and TF.

$$V_{paste} = \pi r^2 h \quad (3.3)$$

$$V_{actual} = V_{paste} \times SF \times TR \quad (3.4)$$

$$TR = (V_{actual}) / (V_{paste} \times SF) \quad (3.5)$$

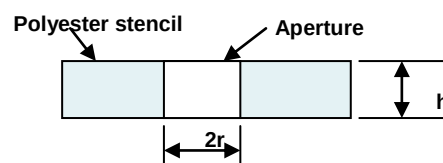
Table 3.2 Polyester Stencil Bumping Transfer Rate (TR)

D (μm)	V_{paste} (μm^3)	SF	V_{actual} (μm^3) (Calculated from x-sect measurements)	TR
40	510000	0.5	88000	0.35
80	1149000	0.5	356000	0.62
250	11662000	0.5	5449000	0.93

Since V_{actual} can be determined by Eq. (3.2), TR can be found using Eq. (3.5). The values of SF and TR for polyester stencil solder bumping are summarized in Table 3.2. The aspect ratio of stencil aperture diameter to thickness (AR1), area ratio of aperture area to aperture wall (AR2) and printing parameters are major factors affecting TR. AR1 and AR2 are determined by the stencil thickness and punch diameter, see Table 3.3.

Table 3.3 Stencil Dimensions

Pad diameter (μm)	250	80	40
Stencil thickness: h (μm)	100	65	65
Punch diameter: 2r (μm)	460	150	100



Solder bump reflow was carried out in a nitrogen-purged hot plate with 3-stage (preheat-reflow-cooling) heating process. The preheat was set at at 180° C, peak reflow temperature at 245° C, cooling at 180° C and unload to cool at 24° C ambient for further processing. The dwell time in each stage was 90 seconds. Three solder bump sizes (B40, B80 and B250) were prepared for characterization, see Table 3.4. The V/A ratios of B40 and B80 are 70 and 71 respectively. The V/A ratio of B250 is 111.

Table 3.4 V/A values of various solder bump sizes (*average of 5 samples*)

Sample S/N	D (μm)	H (μm)	Area (μm ²)	Volume (μm ³)	V/A
B40	40	48	1260	88000	70
B80	80	70	5000	356000	71
B250	250	150	49000	5449000	111

The test dies were thermally aged at 150°C for 500 hours after one reflow exposure to accelerate the interfacial reaction and IMC growth. The solder bumps were cross-sectioned, polished and etched with 5 parts of HCl in 95 parts methanol for 15 to 30 seconds. IMC layers were observed by a scanning electron microscope (SEM). The average IMC thickness was determined by image analysis software. Solder bump shear tests were carried out on the three types of test dies after thermal aging for 100, 250 and 500 hours. The shear test parameters were 100 μms⁻¹ shear rate and shear tip set at 0.1H from die surface (Huang et al., 2001).

3.4 Results

3.4.1 SEM and EDX analyses

After reflow soldering, the solder bumps were subjected to 500 hours of isothermal aging at 150° C. SEM micrographs were prepared at 0 (after reflow), 100, 250 and 500 hours for IMC elemental analyses and morphology studies. As-reflowed IMCs are observed in Figure 3.2 (a). In general, the IMC morphology seen on B40 and

B80 were quite similar. The surface topography comprised discontinuous clusters of needle-like microstructures and some blocky features. A thin layer of IMC formed a continuous interface with the B40 and B80 UBM pads. The IMC on B250 has more blocky and faceted features than needle-like microstructures. The IMC formation on B250 appears to be more fragmented and some discontinuity on the underlying IMC layer can be seen.

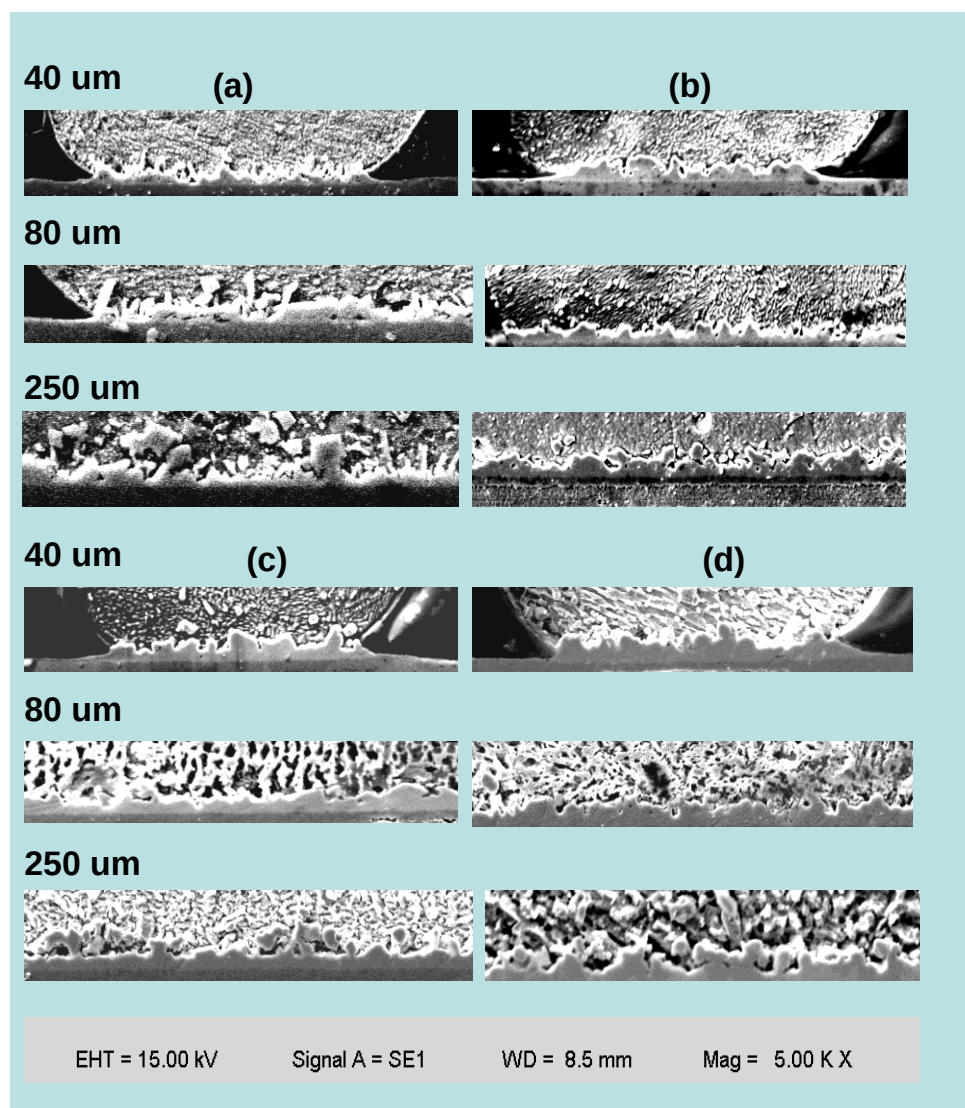


Figure 3.2 IMC morphologies of B40, B80 and B250 UBM diameters after isothermal aging at (a) after reflow, (b) 100 hours, (c) 250 hours, (d) 500 hours

After 100 hours of thermal aging, as observed in Figure 3.2 (b), the underlying IMCs on all the three UBM pads have formed planar continuous layers with irregular top surfaces consisting of blocky features. The clusters of needle-like microstructures have disappeared. IMC on B80 has a less irregular top surface. It comprises bulky and faceted features. After 250 hours of aging and beyond, as observed in Figures 3.2 (c) and (d), the IMC morphologies of all the pad sizes appear to be similar. The IMCs have blocky and faceted features and a thickened continuous planar layer that interfaces with the UBM.

A small number of IMC particles were observed near the IMC solder interface on all the samples. These detached IMC particles were more apparent on the B250 samples, as shown in the micrographs in Figure 3.2. The detached IMC particles could be IMC formed in the solder matrix or could have spalled off from the top IMC layers. However no severe spalling phenomenon was observed in any of the samples throughout the aging process. The IMC average thickness of different bump sizes during isothermal aging was determined by image analyses of the IMC SEM. The results are shown in Figure 3.3. IMC growth $h_t = x_t - x_o$ μm , where h_t is the increase in IMC thickness at time t , x_t is the average IMC thickness at “ t ” aging hours and x_o is the average IMC thickness after reflow. The range of IMC growth is between 1.8 and 1.9 μm on the three different UBM pad sizes after 500 hours of thermal aging.

EDX analyses were carried out on the samples of the three different UBM pad sizes. The EDX results of the samples after 100 and 500 hours of isothermal aging at 150°C are shown in Figures 3.4 (a) to (c). The EDX spectra revealed that there are at least two different IMC phases in the samples analysed. The planar continuous IMC that interfaces with the UBM is a ternary compound made up of Ni-Cu-Sn, where the atomic percentage of Ni is higher than Cu. The IMC with blocky and faceted features

that interfaced with the solder is found to be a ternary compound comprising Cu-Ni-Sn, where the atomic percentage of Cu is higher than Ni. At the IMC/solder interface, some of the Cu-Ni-Sn compounds are spotted together with Au and Ag elements.

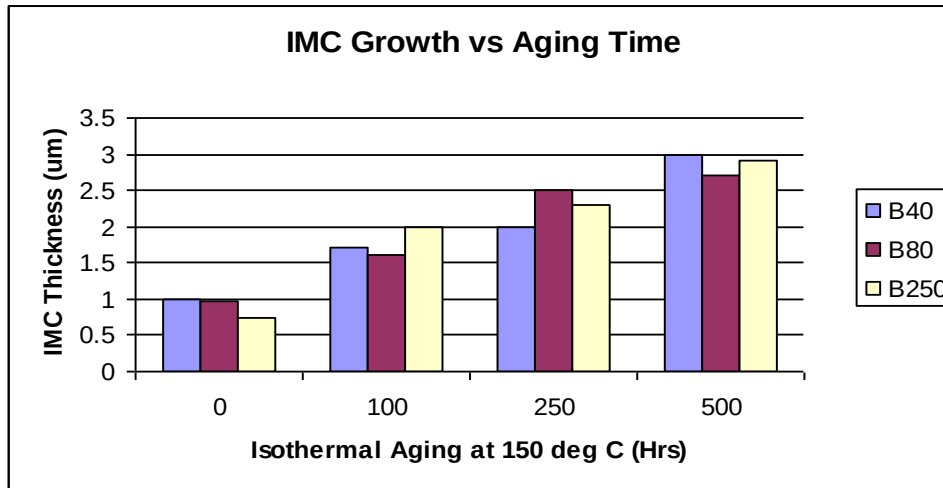


Figure 3.3 IMC growth during isothermal aging

The atomic percentage analyses show that the planar and blocky IMC elemental compositions of during 500 hours of aging do not vary significantly. The atomic percentage of the two types of IMCs spotted on B40, B80 and B250 exhibit a similar range and trend. The EDX results of the two main IMC compounds are summarized in Table 3.5. The results taken at 100, 250 and 500 hours are organized and grouped under IMC I and II. IMC I denotes the IMC that interfaces with the SAC solder. IMC II denotes the IMC that interfaces with the UMB pad. B40, B80 and B250 denote their respective UBM pad diameter sizes.

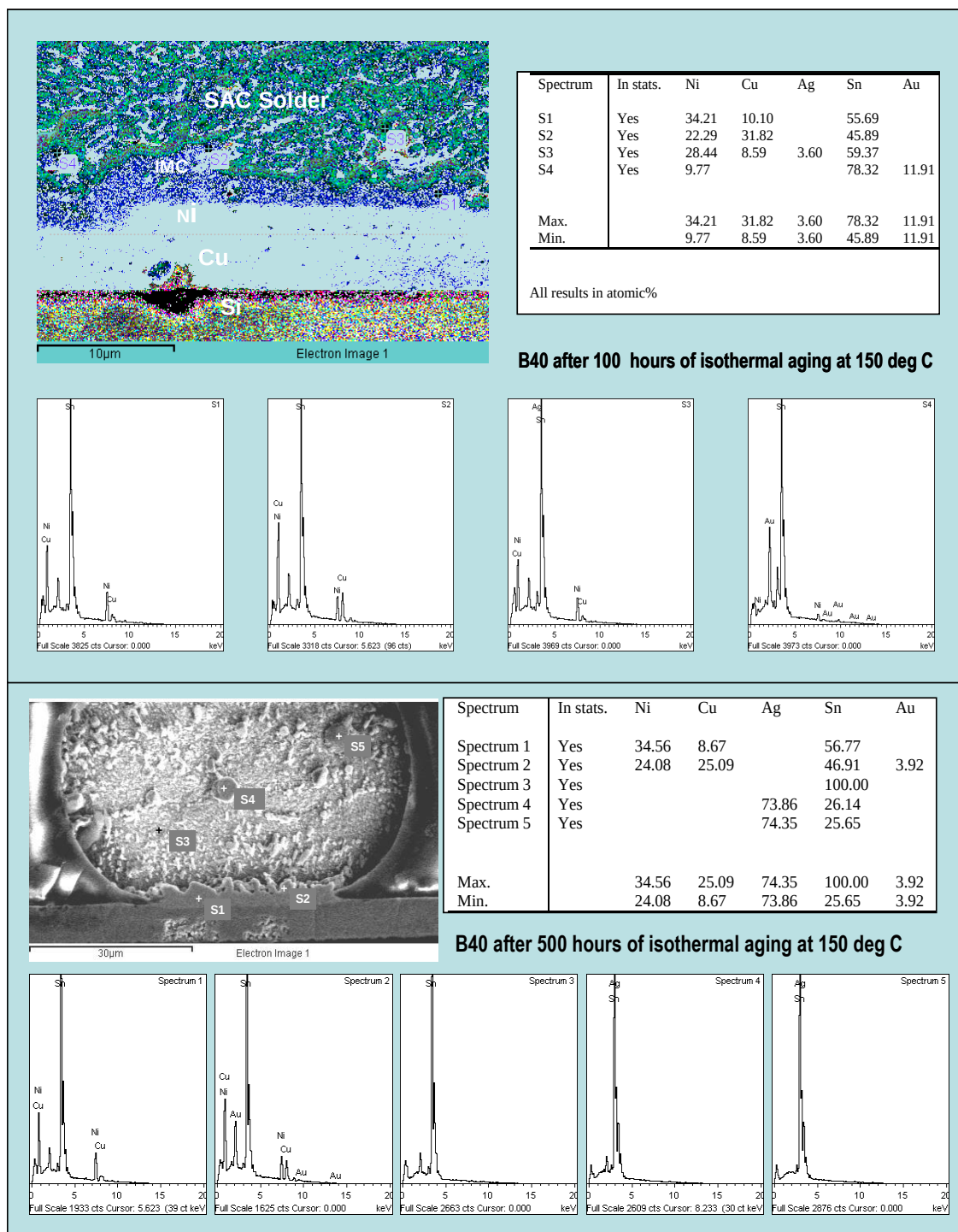


Figure 3.4 (a) EDX spectra of B40 after 100 and 500 aging.

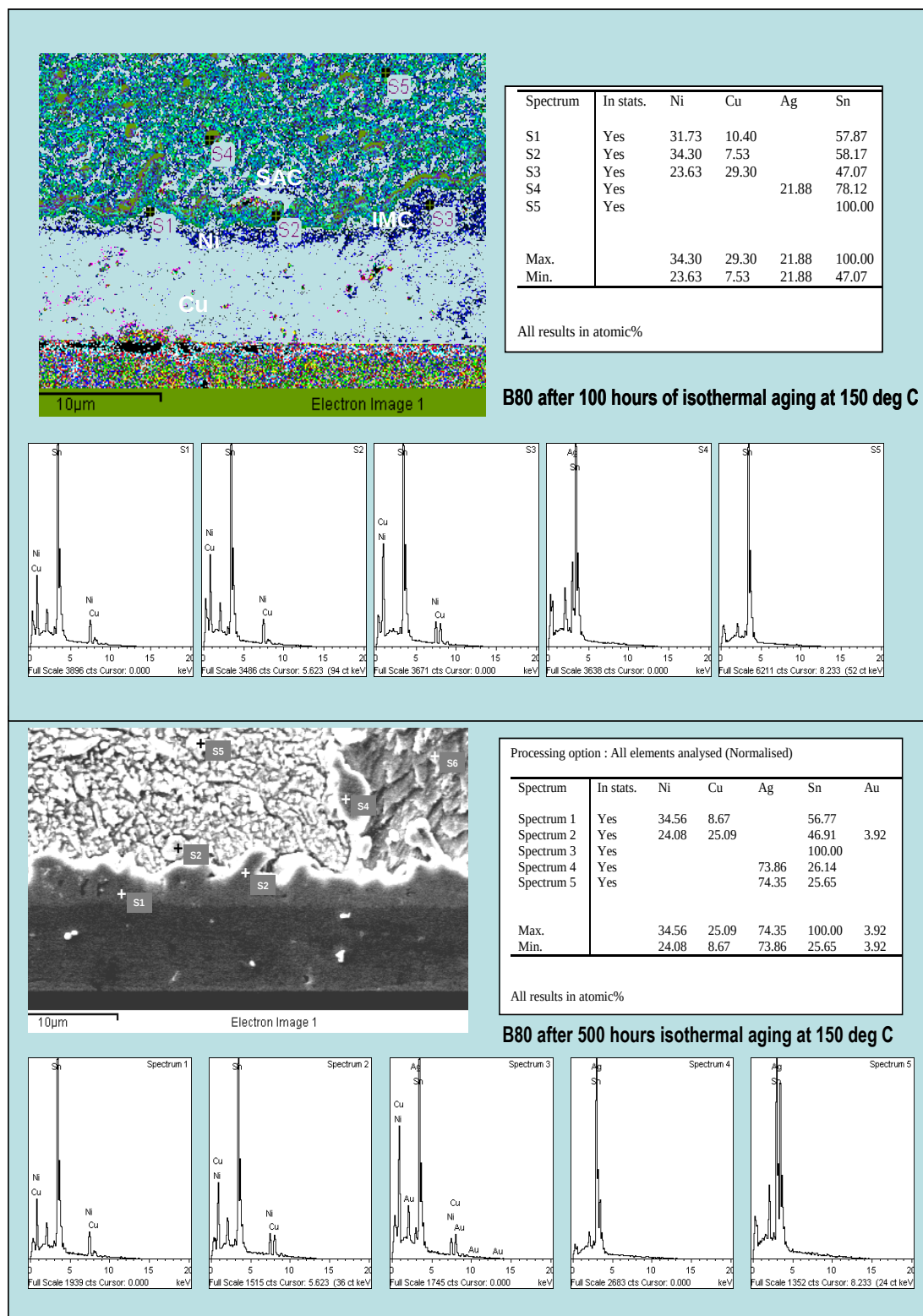


Figure 3.4(b) EDX spectra of B80 after 100 and 500 aging

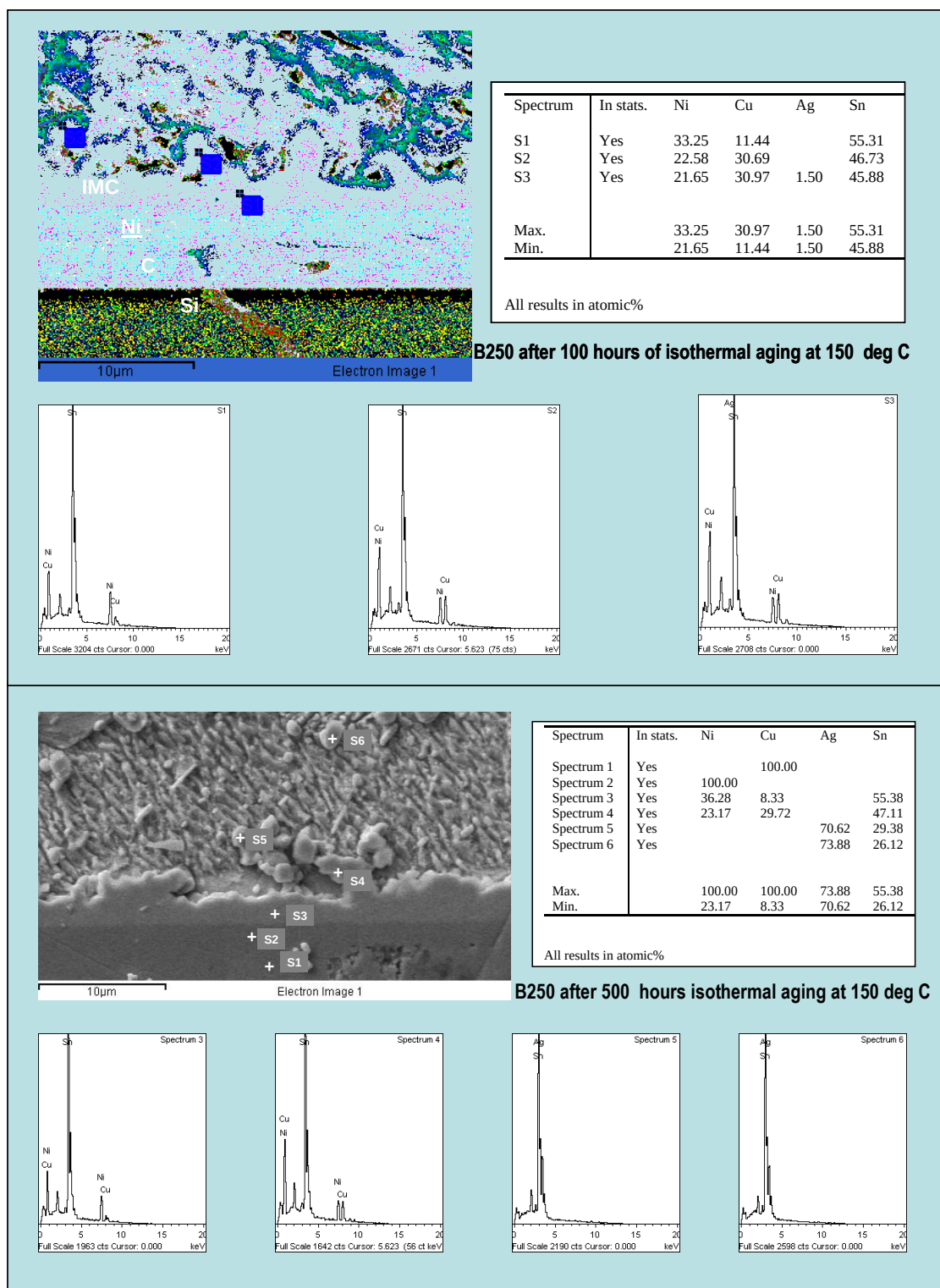


Figure 3.4(c) EDS spectra of B250 after 100 and 500 aging.

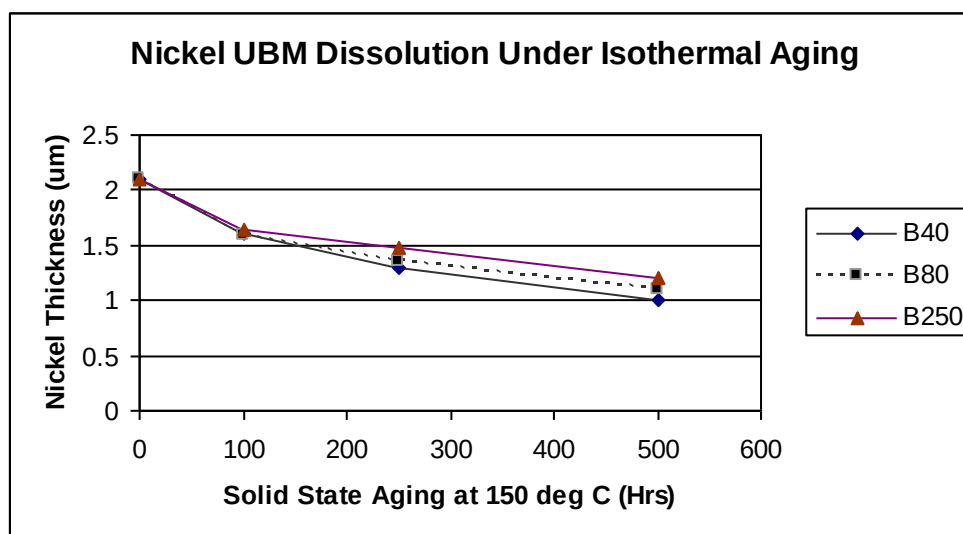
Table 3.5 Atomic Concentration of Spots on or close to IMC (+/- 0.5 atomic %)

Location	Cu	Ni	Sn	*Ag	*Au
IMC I _{B40}	25 – 32	18 – 24	46 – 51	1 – 3	3 – 4
IMC I _{B80}	27 – 31	19 – 25	45 – 48	3	1
IMC I _{B250}	29 – 30	21 – 23	45 – 48	1	2
IMC II _{B40}	8 – 10	34 – 35	56 – 57	---	---
IMC II _{B80}	9 – 14	30 – 33	54 – 58	---	---
IMC II _{B250}	8 – 11	33 – 36	55 – 58	---	---

** Ag and Au elements spotted together with detached IMC particles in the Sn matrix were close to the IMC I / SAC solder interface*

3.4.2 Nickel metallization dissolution

The dissolution rate of Ni metallization was measured during solid state aging. The results are shown in Figure 3.5. To further determine the resilience of Ni UBM in reflow soldering, a separate batch of samples was put through six reflow exposures. The IMC morphologies of the samples B40, B80 and B250 were found to be similar to those with one reflow and 100 of hours aging and approximately 1 μm of Ni UBM was observed.

**Figure 3.5** Nickel UBM dissolution during solid state aging

3.5 Discussion

3.5.1 The effect of V/A ratio on interfacial reaction and solid state diffusion

The SEM micrographs in Figure 3.2 (a) show that the IMC morphologies of B40 and B80 are similar in IMC thickness and topography after reflow. The average IMC thickness for both samples is 1 μm . The SEM micrograph of B250 in Figure 3.2 (a) shows that its surface topography is different from those on B40 and B80. The underlying IMC in B250 is thinner with more discontinuities and the surface topography is more blocky. The average IMC thickness is 0.75 μm . It was noted earlier that the V/A values of B40 and B80 were the same but lower than B250 V/A value. The IMC morphology indicated samples with lower V/A values had thicker and more continuous IMC growth after reflow. This finding concurs with reports by other researchers (Salam et al., 2001, Choi et al., 2002 and Islam et al., 2005). The differences in the IMC morphologies could be explained by the effect of constituents concentration in the molten solder. It will take a shorter time for the samples with lower V/A value to be saturated with Ni. During the solder wetting reaction, Ni will dissolve into the molten solder and react with Cu and Sn. Following this reaction, IMC nucleations will start on the Ni UBM surface. In saturated solder, a higher atomic flux of the constituents accelerates the IMC growth rate. In addition, saturated solder would not dissolve away the IMC at the UBM interface while unsaturated solder would tend to dissolve the IMC. Thus, B250 which has higher V/A ratio, displays a thinner and more fragmented IMC morphology after reflow reaction. Whereas B40 and B80 have better defined and thicker IMC layers.

In addition, our results show that if V/A ratio is held constant when B80 scales down to B40, the morphology and IMC growth are not influenced by the scaling.

Hence, for a specific solder volume, if the V/A ratio is known, a matching UBM pad size can be determined. Such information is useful for interconnection design.

During solid state diffusion, B250 which started with a thinner IMC layer than B40 and B80, ended up with a thicker IMC layer after 100 hours of solid state aging. This could be explained by the fact that the thin and fragmented IMC layer on B250 was exposing more Ni directly to the SAC solder. Direct interdiffusion of Sn, Cu and Ni among the fragmented IMC channels resulted in rapid IMC growth in B250. A thinner IMC layer also means shorter diffusion path. In high V/A samples, larger amounts of Sn and Cu could be diffused through the IMC barrier to feed the growth of IMC on B250. The better defined continuous IMC layers in B40 and B80 acted as barriers between Ni UBM and SAC. The IMC barrier reduced the atomic flux of Sn, Cu and Ni elements, slowing down their reaction. This means that diffusion of metals is slowed down by an increase in diffusion path length created by the IMC barriers and a reduction in concentration gradient of metals in the system.

It was observed that the test samples had IMC of between 0.75 to 1 μm in thickness after 6 minutes of reflow reaction. Figure 3.3 shows that after 100 hours of solid state aging, the IMC of the B40 and B80 samples grew between 0.6 to 0.7 μm and B250 grew by 1.2 μm . This indicates that the rate of IMC formation between Ni and SAC solder during reflow is two orders of magnitude greater than Ni-SAC solder IMC growth in solid state aging. The IMC growth rates in the samples show a parabolic growth trend rather than a linear trend during aging. This implies that the IMC formation on B40, B80 and B250 are diffusion controlled. If the growth process was controlled by volume diffusion or stationary grain boundary diffusion, the increase of the IMC layer after aging should follow the square root time law, where IMC thickness; $h \approx (Dt)^{1/2}$ (Guan et al., 2000). D is the diffusion coefficient and t is the aging time.

3.5.2 IMC Composition on Ni UBM

The EDX results show that there are two different compositions of IMC on the Ni UBM after reaction with SAC solder. Figures 3.4 (a), (b) and (c) show that IMC I which interfaces with SAC solder has a higher Cu atomic percentage. IMC II which is located between IMC I and the Ni UBM has a higher Ni atomic percentage. Based on the IMC locations, one could deduce that IMC I is the first compound to be formed as it has a direct interfacial reaction with SAC solder. Even though there was plenty of Ni and Sn at the interface, an IMC compound with richer Cu was formed. It was reported that when Ni reacted with Sn-Ag3.9%-Cu0.5% (or Cu concentration between 0.5-0.8 wt.%), a layer of $(\text{Ni}_{1-x}\text{Cu}_x)_3\text{Sn}_4$ would form beneath $(\text{Cu}_{1-y}\text{Ni}_y)_6\text{Sn}_5$ (Ho et al., 2002). The compositions of IMC I and II in B40, B80 and B250 samples which were produced from the Ni reaction with Sn-Ag3.8%-Cu0.7% were similar to the results reported by Ho and his co-researchers (Ho et al., 2002). The atomic percentage composition of IMC I and IMC II also corresponded with the phases and figures reported by Paik and his co-researchers (Paik et al., 2004) who investigated Sn-Ag4.0%-Cu0.5% reacting with electroless Ni with 11-13% phosphorous. But instead of the needle-like $(\text{Ni}_{1-x}\text{Cu}_x)_3\text{Sn}_4$ observed by Paik, the IMC II layer in this study which involved electrolytic Ni reacting with Sn-Ag3.8%-Cu0.7% produced planar $(\text{Ni}_{1-x}\text{Cu}_x)_3\text{Sn}_4$ – see Figures 3.4 (a) to (c). In a previous study on IMC growth on SAC/Cu metallization and SAC/Ni metallization (Zribi et al., 2001), it was found that the growth rates of Cu_6Sn_5 and $(\text{Cu,Ni})_6\text{Sn}_5$ were similar and distinctly higher than Ni_3Sn_4 growth rate in a Ni/Sn diffusion couple. As kinetics generally dominate phase selection, faster growing phases will grow first. Hence, it is suggested that $(\text{Cu,Ni})_6\text{Sn}_5$ will form first at the SAC solder / Ni interface. If a significant amount of Sn continues to diffuse across the $(\text{Cu,Ni})_6\text{Sn}_5$ IMC, Sn will interact with the Ni UBM and transform the $(\text{Cu,Ni})_6\text{Sn}_5$ IMC

close to the Ni UBM interface into $(\text{Ni,Cu})_3\text{Sn}_4$. In the presence of limited Cu content, $(\text{Ni,Cu})_3\text{Sn}_4$ could be the more stable phase.

Au was spotted with $(\text{Cu,Ni})_6\text{Sn}_5$ IMC at the vicinity of the IMC I and solder interface. It is expected that during reflow, the thin layer of immersion Au on the Ni UBM dissolves very rapidly and exposes the Ni to react with the solder. In a previous study (Bader, 1969), it was found that the dissolution rate of Au exceeded that of Ni by almost three orders of magnitude, and the solubility of Au to that of Ni by five orders of magnitude. While $(\text{Cu,Ni})_6\text{Sn}_5$ IMC started to form during reflow soldering, Au would remain in the Sn-rich phase. At lower temperatures, the solubility of Au started to decrease and precipitate out. However, as the temperature decreased, the Au atoms mobility in Sn would also decrease. It is suggested that if Au exists at the solder IMC I interface, it may react with the $(\text{Cu,Ni})_6\text{Sn}_5$ IMC to form a quaternary IMC of Cu-Ni-Sn-Au. Due to the low mobility of Au in solid state, it is presumed that there is limited Au at the interface. Hence, the quaternary IMC was only spotted occasionally in the samples. The presence of Ag in the IMCs was likely the Ag_3Sn IMC particles located close to the IMC I layer.

From the analyses of the SEM micrographs in Figures 3.2(a) to (c), IMC growth rates in Figure 3.3 and EDX results in Figure 3.4, it is evident that varying V/A ratio can influence reflow soldering interfacial reaction, resulting in different IMC morphologies and thicknesses. However, after 250 hours of aging, the thickness differences level off. The IMC surface topography of the samples with a higher V/A value continued to display more blocky features than the samples with a lower V/A value. The blocky features were spotted by EDX as $(\text{Cu,Ni})_6\text{Sn}_5$ IMC. This means that there is more Cu available to support IMC I formation in a higher V/A ratio. The higher incidence of fragmented or detached $(\text{Cu,Ni})_6\text{Sn}_5$ IMC could be due to weak

adhesions between IMC I and II grain boundaries along the IMC I and II interface leading to IMC I breaking away.

3.5.3 Ni UBM dissolution rate

The original thickness of all the test samples before reflow is approximately 2.1 μm . At the end of 500 hours of aging, the average Ni thickness on B40, B80 and B250 is between 1.0 to 1.2 μm . Figure 3.5 shows that the Ni dissolution gradient is decreasing over time. Ni UBM with 2 μm will suffice for most applications. The dissolution rate of Ni on the samples after reflow and 100 hours aging is similar. Figure 3.5 shows that as the aging time increases, the Ni dissolution rate of B40 > B80 > B250. It seems that the geometrical distance and thickness of solder play a role in Ni dissolution rate. For simplicity, if the reaction space is defined by the vertical column of solder above the UBM pad as shown in Figure 3.6, one could see that constituents in a larger bump will have to cover a longer diffusion distance and consequently a longer time to reach saturation. Even with the same V/A ratio, a smaller solder bump could be saturated faster. A more saturated environment leads to faster IMC formation and thus a higher Ni consumption. The longer column of solder above the UBM could generate a stronger flux of Cu atoms to react with Ni to form $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC I. If Cu atoms were depleted in a shorter column of solder in a small bump, Ni will be consumed in the transformation into $(\text{Ni},\text{Cu})_3\text{Sn}_4$ IMC II.

3.5.4. Shear Test Results

As shown in Figure 3.7, the shear strength of the isothermally aged B40, B80 and B250 solder bumps did not show any significant variation over 500 hours. Despite the IMC thickening, there is no apparent degradation of the bump shear strength. Further investigations have to be carried out to characterize the performance of the

different bump sizes to better understand the implication of these shear results on solder joint reliability.

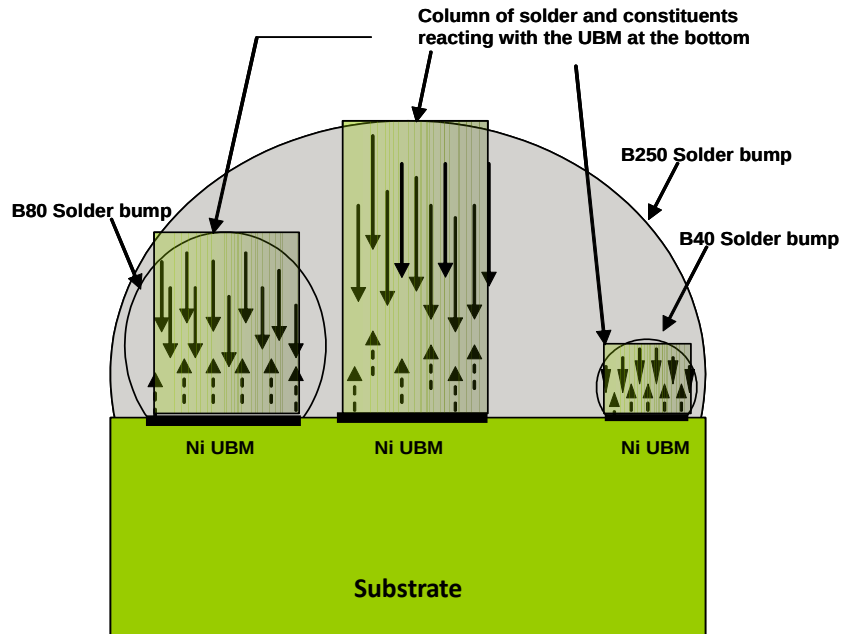


Figure 3.6 Size effect of solder bump on Ni dissolution

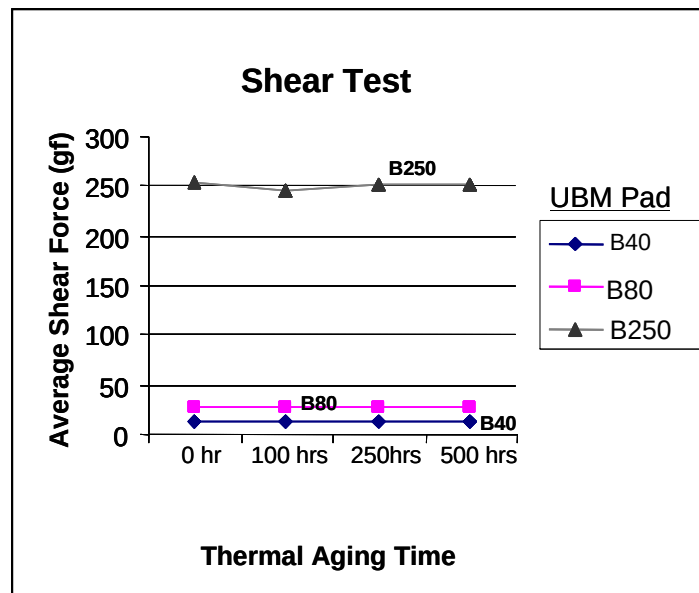


Figure 3.7 Shear test data of SAC solder bumps on 250, 80 and 40 μm pads

3.6 Summary

The morphology of the IMC at the interfaces of SAC solder and Ni UBM is found to be similar if the solder volume/Ni metallization area (V/A) ratio is constant. The IMC formation is found to be sensitive to V/A ratio changes, with a higher V/A ratio resulting in thinner and more fragmented IMC and a lower V/A ratio having a more defined and continuous IMC layer. The results from this study also suggest that if the V/A values differ by 30%, as in the case of B250, compared with the V/A values of B80 and B40, a perceivable difference in the IMC morphology can be observed. It could be deduced that a solder joint with higher V/A ratio is not saturated with Ni during reflow and hence, resulting in a slower IMC formation. In a lower V/A ratio solder joint, the molten solder could be saturated with or have a higher content of Ni, leading to a faster IMC formation.

The IMC phases are similar at the solder/Ni interface for samples B40, B80 and B250. The top layer, IMC I, which interacts directly with solder is $(\text{Cu,Ni})_6\text{Sn}_5$ and the layer below, IMC II, is found to be $(\text{Ni,Cu})_3\text{Sn}_4$. The IMC II is formed when Sn diffused into IMC I, and at the proximity of the Ni UBM when the Cu content would be limited, $(\text{Cu,Ni})_6\text{Sn}_5$ is transformed into $(\text{Ni,Cu})_3\text{Sn}_4$ which could be a more stable phase.

The Ni UBM dissolution rate is observed as follows: $\text{B40} > \text{B80} > \text{B250}$. The Ni dissolution rate has a decreasing gradient over aging time. From the results of this study, it is determined that an initial Ni UBM thickness of 2.0 μm should suffice for most applications as 1.0 to 1.2 μm of Ni UBM has remained after 500 hours of aging.

There is no significant variation in shear force for the different UBM sizes over 500 hours aging. Further investigations have to be done to characterize the

performance of the different bump sizes to better understand the implication of these shear results on solder joint reliability.

Chapter 4 Conceptual Design of a Copper Pinhead Pillar Bump Structure

This chapter examines the design and application of the Cu pinhead (CPH) pillar for interconnecting flip-chip-on-board. ANSYS finite element analysis software is used in the simulation studies to evaluate the reliability of CPH pillar solder bump interconnections and the data is benchmarked with conventional Cu pillar and flip-chip solder bump interconnections.

4.1 Conceptual design of Cu pinhead pillar bump interconnection

The flip-chip process, which flips and attaches a bare die to a substrate using a solder bump, is a significant development for the microelectronic industry. An optimized flip-chip device provides improvement in cost, reliability and performance over a wire-bonded device. Aided by the self-aligning characteristic of solder, flip-chip packaging using solder bumps has an excellent assembly yield. An area array interconnection format on flip-chip allows a large number of I/Os to be distributed across the chip surface. This improves pitch spacing and power distribution. With no additional packaging material over the bare chip, the flip-chip has the smallest possible size. Figure 4.1 shows a typical solder bump interconnection.

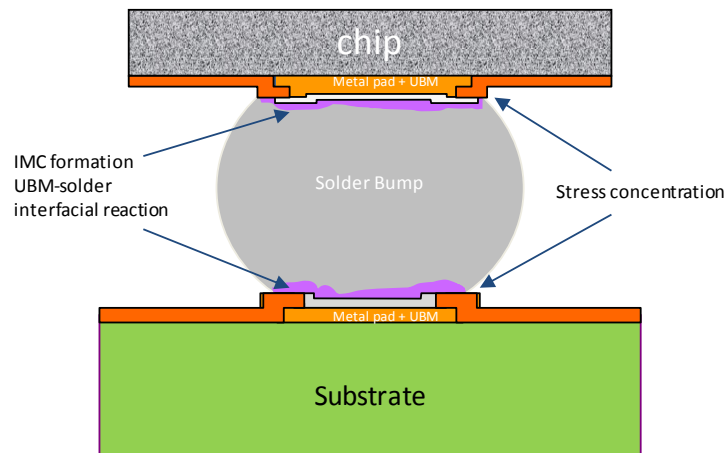


Figure 4.1 Conventional solder bump flip-chip interconnection

The solder bump interconnection comprises an under-bump-metallization (UBM), a solder bump and a matching substrate bond pad. However, the typical solder bump interconnection has several inherent weaknesses. During reflow, the solder bump will collapse and become barrel-shaped upon solidification. This limits the height and pitch of solder joints. The applications of the solder bump interconnection in high-density miniaturized packages are limited. The truncated spherical ends of the solder bump are the main load bearing points and high stress concentration occur at these ends. The UBM interacts with the solder bump to form a layer of brittle intermetallic compound (IMC). The coefficient of thermal expansion (CTE) mismatch in these IMC-solder interfaces creates nodes for crack initiation and propagation.

Unlike the solder bump, the copper pillar does not collapse during reflow soldering. If plating is carried out directly on the chip metal pads, IMC formation on the chip interface is avoided. Solder diffusion and interaction with the thin films on the chip is eliminated. Compliant pillar structures can be designed and fabricated to reduce stress concentration and shear strain on the solder. Figures 4.2(a) and 4.2(b) show a conventional Cu pillar interconnect design with a larger and a smaller pillar diameter respectively. A key issue with the conventional pillar interconnect design is that the

solder volume and its wetting surface vary as the diameter of the pillar changes. The pillar with a smaller diameter, as shown in Figure 4.2(b), is more compliant compared to the pillar with a larger diameter, as shown in Figure 4.2(a). However, the wetting surface decreases when the diameter of the pillar becomes smaller. A decrease in the wetting surface affects joint reliability.

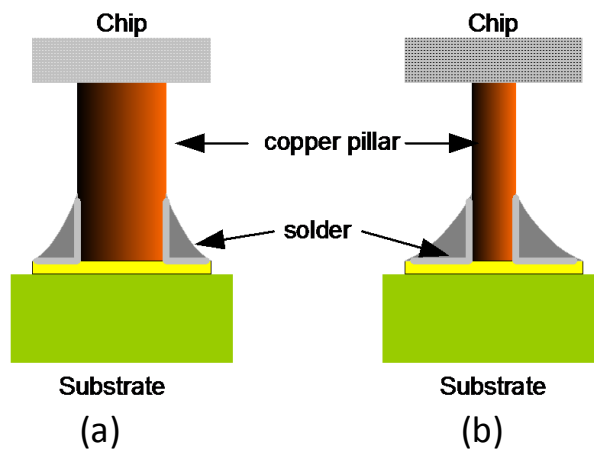


Figure 4.2 Conventional Cu pillar bump interconnection - solder volume and joining surface area vary with pillar diameters

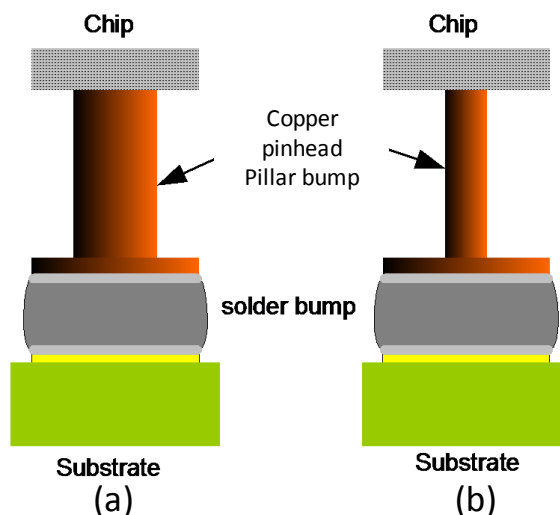


Figure 4.3 Cu pinhead (CPH) pillar bump interconnection – solder volume and joining surface area can be kept constant when pillar diameter changes

In this study, a pinhead pillar configuration is introduced as an improvement over the conventional Cu pillar. The pinhead on the pillar acts as a floating metal pad for the solder bump, see Figure 4.3. The pinhead can be designed to match the metal pad of the substrate and optimize joint reliability. In addition, the Cu pinhead (CPH) pillar extending from the pinhead can be varied in height and diameter to enhance joint compliance. The pinhead structure renders the CPH pillar greater design flexibility compared to the conventional Cu pillar. With the pinhead serving as the interconnecting pad, the pillar height and diameter can be changed freely without affecting the layout of the interconnecting pads. The advantages of a CPH pillar interconnection over conventional Cu pillar are illustrated in Figures 4.4. To illustrate the compliance of a CPH pillar interconnection, Figure 4.5 compares the displacement sustained by a conventional flip-chip solder bump and a CPH pillar bump respectively.

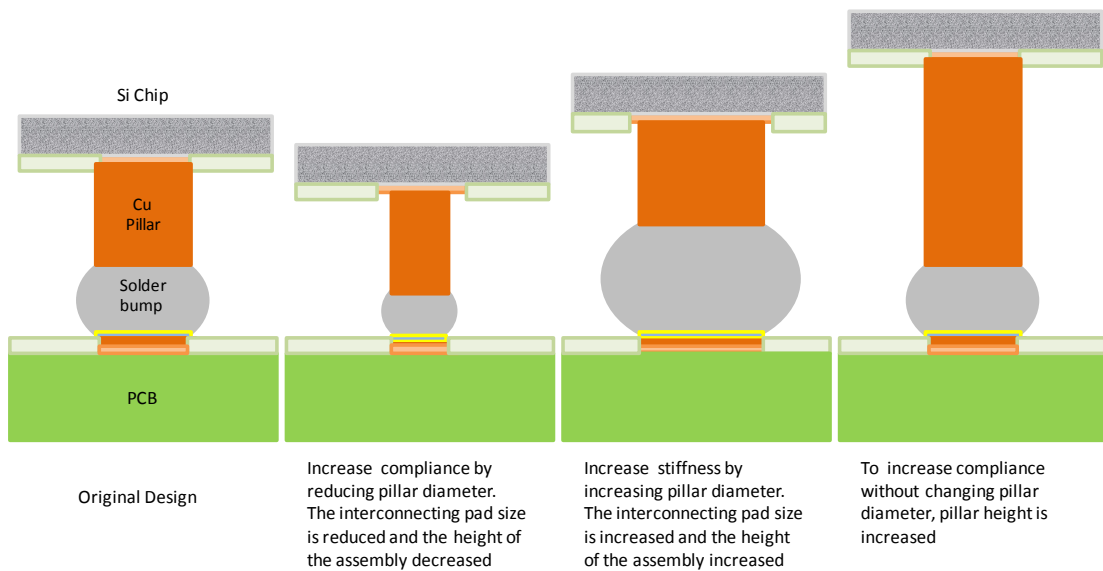


Figure 4.4(a) Conventional Cu pillar design: adjusting the interconnect compliance will change the pad size and overall assembly height

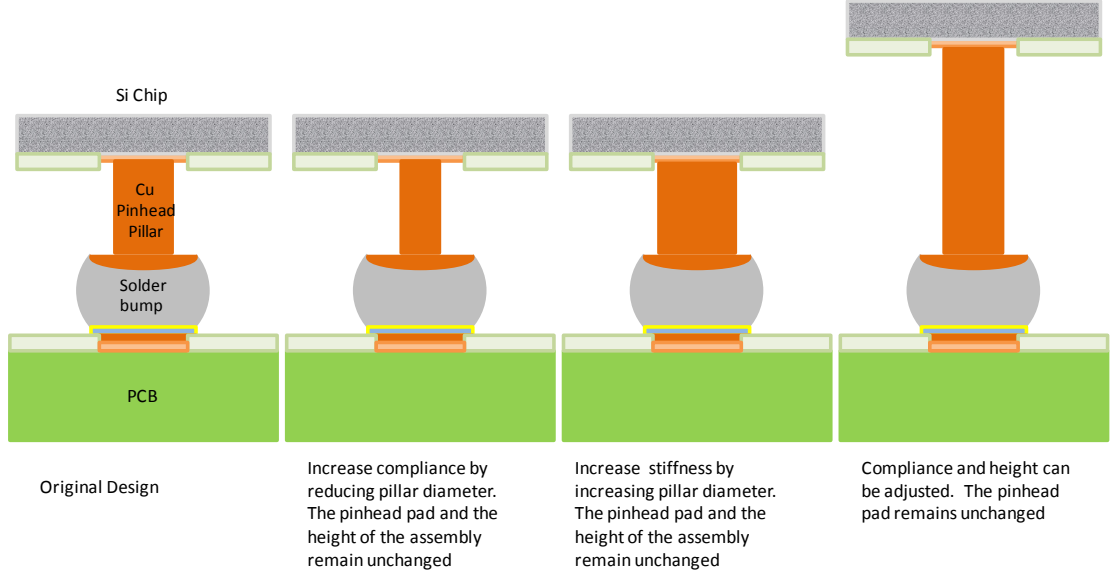


Figure 4.4(b) Cu pinhead (CPH) pillar design: interconnect structure compliance can be adjusted without changing the solder volume, interconnecting pad size and height

If the thermal expansion coefficients of the silicon chip and substrate are such that $CTE_{chip} > CTE_{substrate}$ for the assembly shown in Figure 4.5, heating and cooling will essentially fatigue the solder joint through shear strain reversals. The shear strain, γ_{FC} , of the solder on the conventional flip-chip solder bump joint can be expressed as follows:

$$\gamma_{FC} = (\Delta_{FC}) / (h) \quad (4.1)$$

Similarly, the shear strain of the CPH pillar bump joint is as follows:

$$\gamma_{CPH} = (\Delta_{CPH}) / (h) \quad (4.2)$$

The displacement arising from CTE difference of chip and substrate on the CPH pillar bump assembly is largely taken up by the bending of the CPH pillar, as seen from Figure 4.5. As a result, the shear strain in the CPH pillar solder joint, γ_{CPH} , is significantly smaller than the shear strain in the conventional flip-chip solder joint, γ_{FC} . A detailed reliability analysis of conventional flip-chip and CPH pillar solder joints is discussed in Section 4.3.

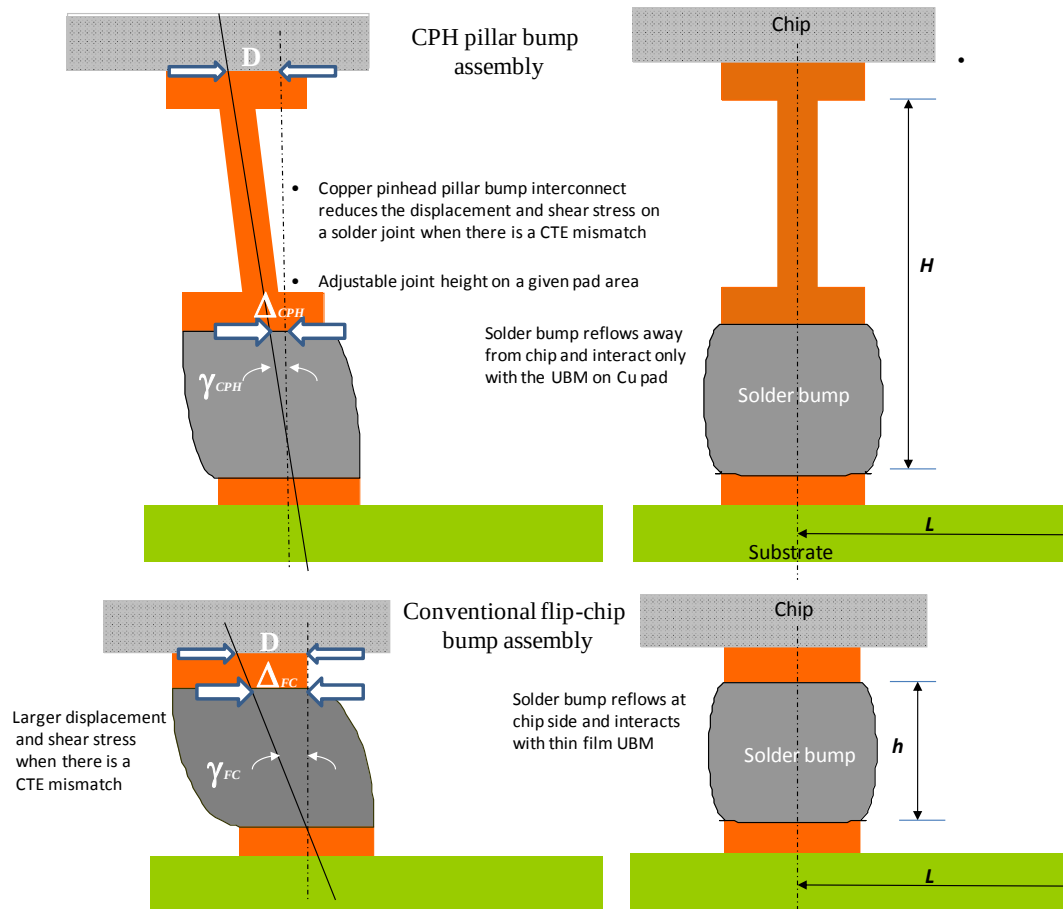


Figure 4.5 The CPH pillar bump interconnection is more compliant compared to the conventional flip-chip solder bump interconnection

4.2 Bumping and assembly of Cu pinhead pillar bump interconnection

In the conventional wafer bumping process, a UBM layer is deposited on the metalized pad of the wafer or over a re-distributed metal layer. Subsequently, solder bumps are deposited on the UBM layer to complete the process. The UBM solder layer serves as a wetting surface for solder bump attachment to the chip, as well as a barrier layer to prevent metal diffusion from the solder into the chip side that can degrade the electrical and mechanical performance of the device.

A simplified solder bumping and assembly sequence is illustrated in Figure 4.6. The UBM is usually deposited by physical vapour deposition, followed by electroplating process, and solder bumps can be printed, electroplated or picked-and-placed. The detailed fabrication process of the CPH pillars is covered in Chapter 5 of this report. A simplified CPH pillar bumping and assembly sequence is illustrated in Figure 4.7. The UBM layer comprising nickel and gold is electroplated on the pinhead structure in the same CPH fabrication process. The solder bumps can be electroplated or picked-and-placed.

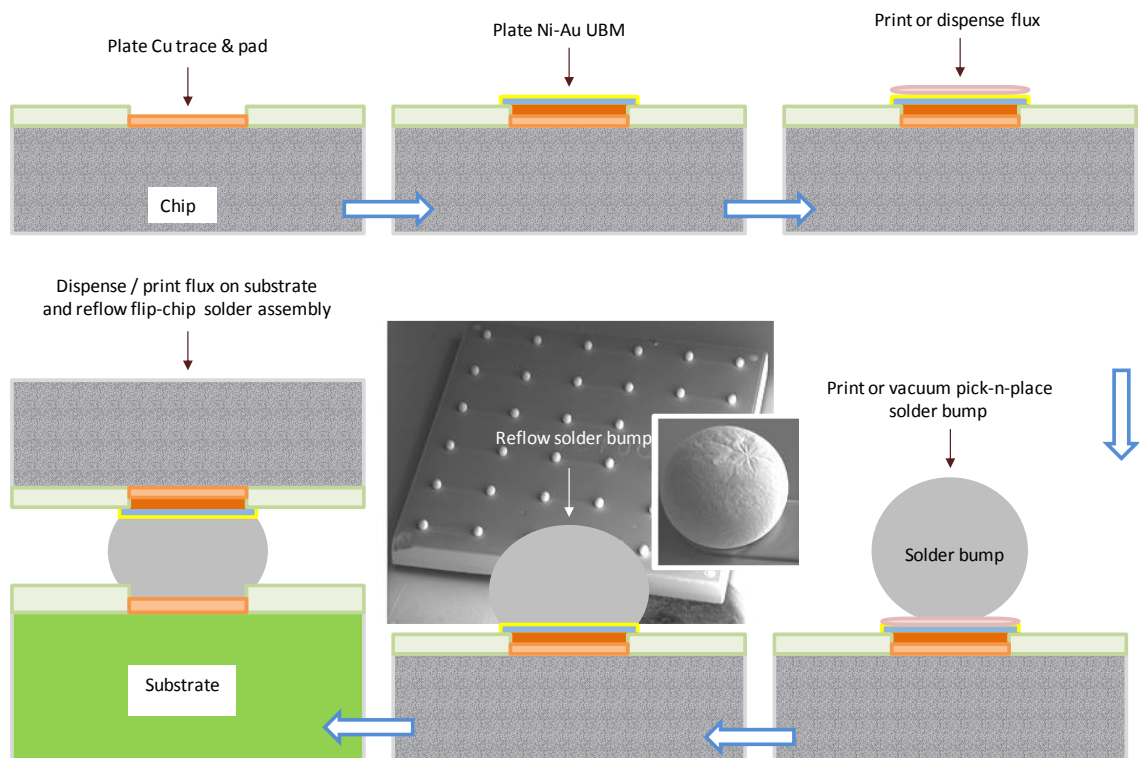


Figure 4.6 Conventional flip-chip solder bumping and assembly process flow

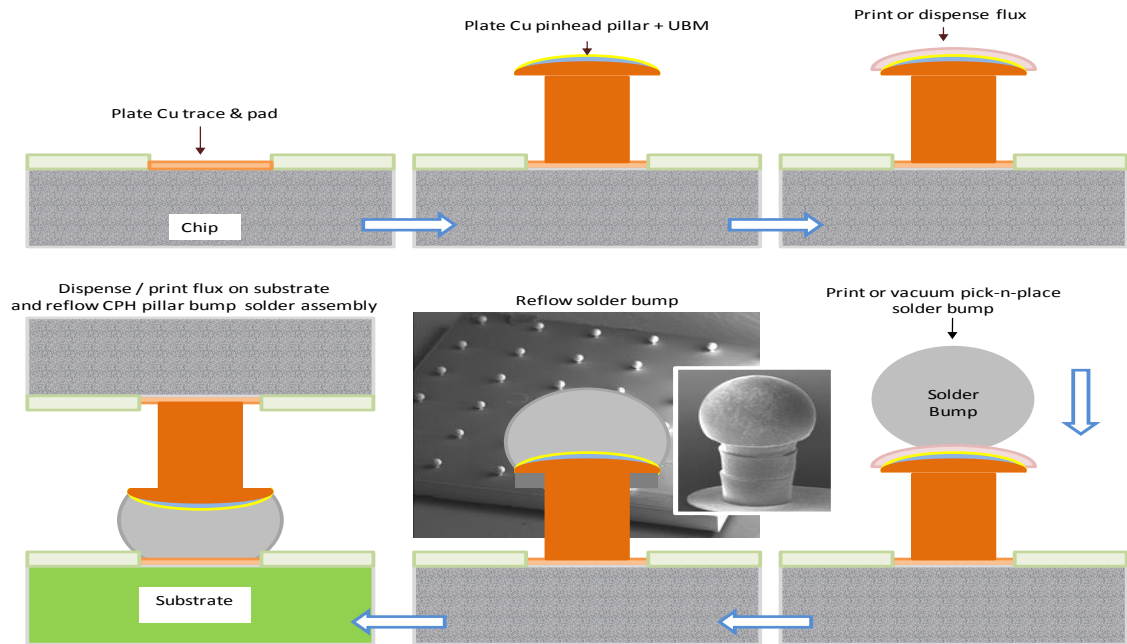


Figure 4.7 CPH pillar solder bumping and assembly process flow

In this study, 120 μm SAC solder bumps were picked and placed on 6x6 mm silicon test chips that were populated with thirty-six CPH pillars of 160 μm in height. The test chip layout is illustrated in Figure 4.8. The completed assembly without underfill is shown in Figure 4.9. It is clear that with the CPH pillar bump floating pads, the solder bumps are shifted away from the chip. This has resulted in greater compliance and better reliability in a chip or module assembly.

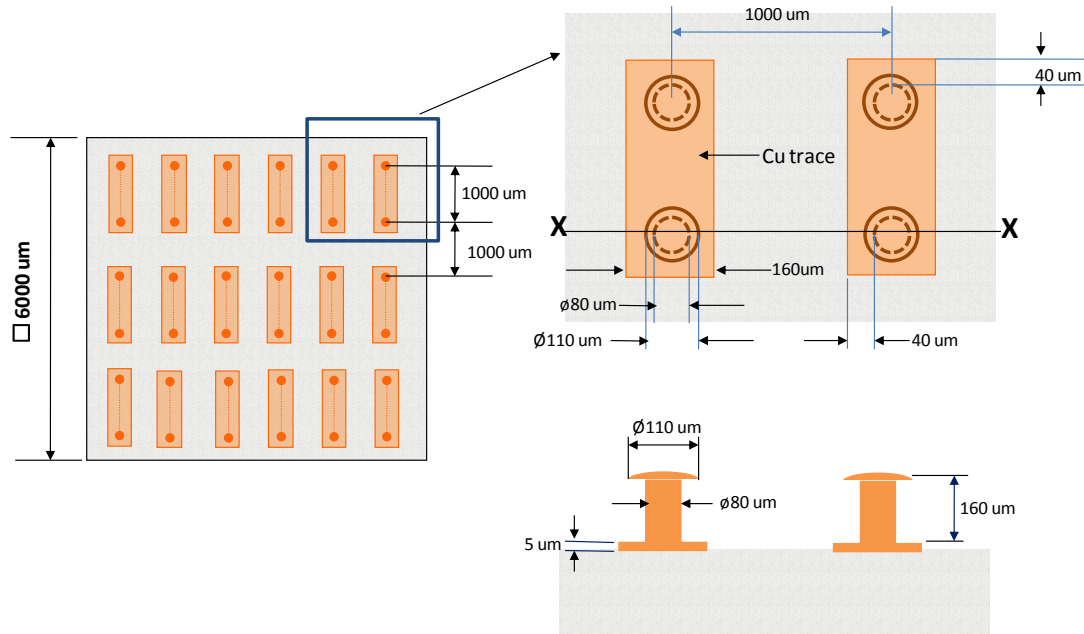


Figure 4.8 Layout of 6x6mm silicon test chip with 36 CPH pillars

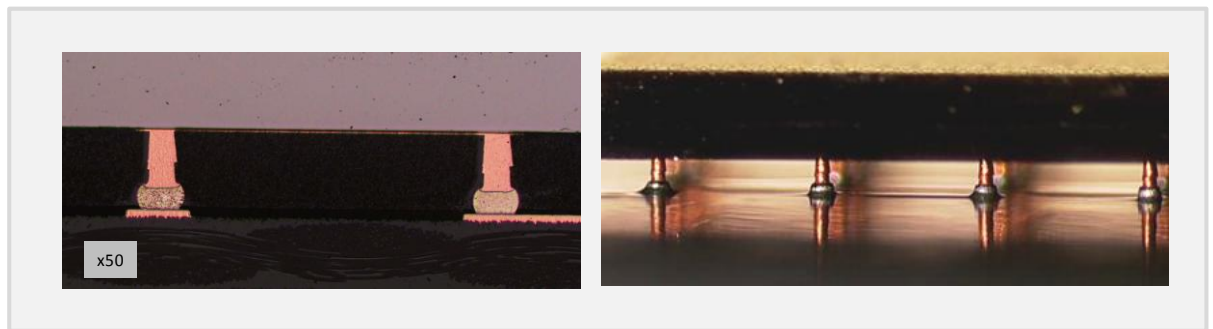


Figure 4.9 160 μm height / 80 μm diameter CPH pillars, attached with 120 μm SAC solder bumps, assembled on PCB

4.3 FEM modelling of Cu pinhead pillar bump interconnection

FEM modelling is used extensively in electronic packaging design as a tool for virtual design and reliability assessment. ANSYS finite element analysis software is used in this simulation study to model the reliability of different CPH pillar structures and the data is benchmarked with SAC solder bump interconnect.

FEM modelling is used as a screening tool to pre-determine an interconnect design for subsequent experimental evaluations.

Creep behaviours of SAC solder are important properties and these are typically characterized through experiments such as lap shear tests and tensile tests. Creep strain rates are obtained as a function of temperature and non-linear multiple regressions are subsequently carried out to curve fit the data to a general constitutive material model to obtain material constants.

Strain-based fatigue models and energy-based fatigue models are widely used to determine the fatigue life of solder joints. Prior to fatigue life prediction, the damage parameter has to be obtained. The damage parameter is either inelastic strain or strain energy density. The inelastic strain or the strain energy density is obtained through thermal cycling simulation and from experimental thermal cycling reliability data. Linear regression is carried out to obtain fatigue life model constants.

4.3.1 Constitutive models for SAC solder

The time- and temperature-dependent deformation behaviours of solder material can be simulated by FEM. These models include single creep equations with power-law or hyperbolic sine functions (Syed, A., 2004), elastic-plastic and elastic-plastic-creep models (Pang J.H.L. et al, 2001) and viscoplastic Anand's model (Cheng Z.N. et al, 2000).

In this study, the elastic-plastic-creep (EPC) model is used to simulate SAC solder as an elastic-plastic-creep material with temperature dependent Young's modulus and yield stress. The solder is assumed to exhibit elastic, bilinear kinematic hardening plastic behavior after yield. The creep behavior of solder is modeled using the hyperbolic sine creep equation:

$$\dot{\epsilon}_c = C_1 \frac{G}{T} \left[\sinh \left(\alpha \frac{\sigma}{G} \right) \right]^n \exp \left[\frac{-Q}{kT} \right] \quad (4.3)$$

where C_1 is a constant, G is the shear modulus, α is the stress level at which power law dependence breaks down, σ is the equivalent von Mises stress, n stress exponent, Q activation energy, k Boltzmann's constant, T is the absolute temperature.

Fatigue damage parameters such as inelastic strain or inelastic strain energy density can be expressed as follows:

$$\varepsilon_{in} = \varepsilon_c + \varepsilon_p \quad (4.4)$$

$$W_{in} = W_c + W_p \quad (4.5)$$

where subscripts in , p and c represent inelastic, plastic and creep respectively.

4.3.2 Fatigue life prediction model

Coffin-Manson's strain-based model and Morrow's energy-based model have been reported (Pang J.H.L. et al, 2004):

$$N_f^m \Delta \varepsilon_{in} = C \quad (4.6)$$

$$N_f^n \Delta W_{in} = A \quad (4.7)$$

The fatigue exponents, m and n and fatigue ductility coefficients, C and A , for Sn-3.8Ag-0.7Cu are 0.853, 0.897, and 9.2, 311.7MPa (at 125°C with 0.001Hz) respectively (Pang J.H.L et al, 2004).

4.3.3 Parametric study of conventional flip-chip, Cu pillar and CPH pillar bump assemblies

A parametric study was carried out to assess the CPH pillar bump solder joint reliability and the results were benchmarked with the reliability performance of a conventional flip-chip bump and a Cu pillar bump joint. The study matrix is given in Table 4.1. A schematic of a CPH pillar bump assembly, a conventional copper pillar bump assembly and a flip-chip solder bump assembly are shown in Figures 4.10(a), (b)

and (c). In the FEM study, a 6 x 6 mm silicon chip with thirty-six interconnects as shown in Figure 4.11 was used.

Table 4.1 FEM parametric study matrix

Parametric Study	Conventional flip-chip interconnect	Cu pillar interconnect		CPH pillar interconnect	
		Pillar	Pillar	Pillar	Pillar
		Height	Diameter	Height	Diameter
		75 μm	80 μm	75 μm	80 μm
		160 μm	80 μm	160 μm	80 μm
	120 μm SAC solder bumps were used in all the cases				

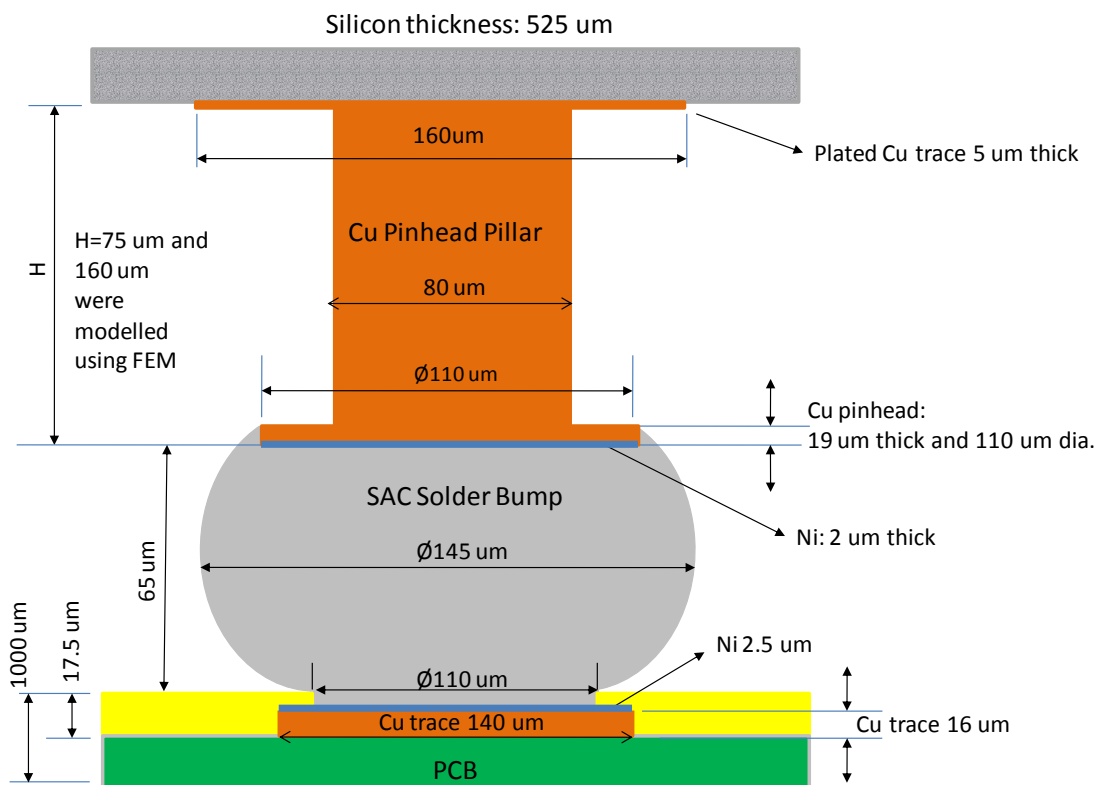


Figure 4.10(a) CPH pillar bump assembly

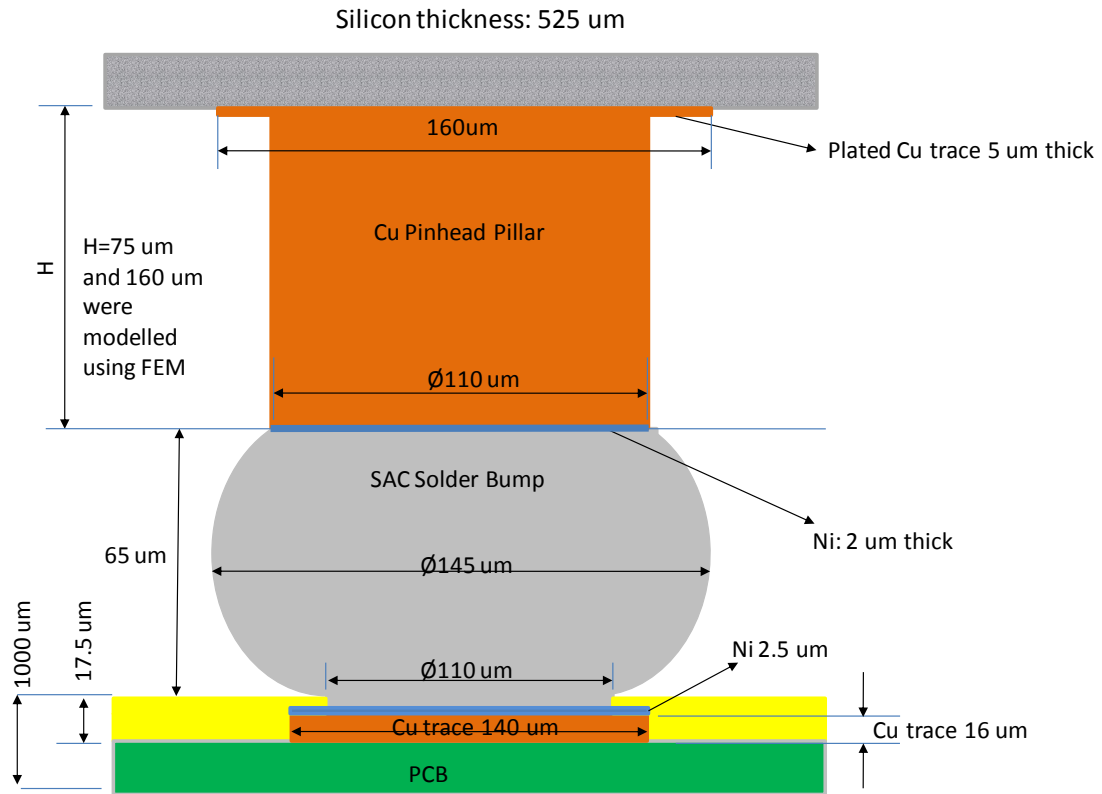


Figure 4.10(b) Conventional copper pillar bump assembly

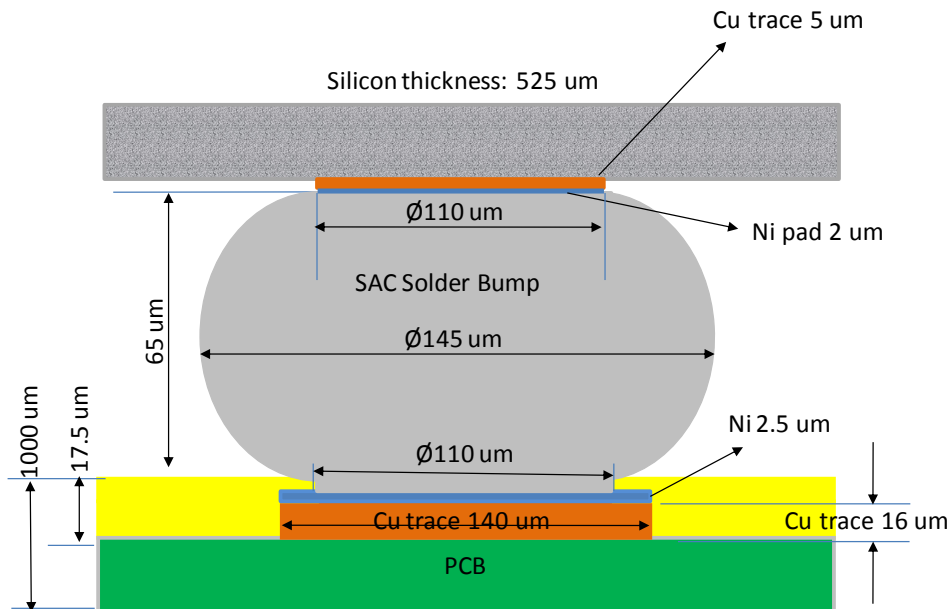


Figure 4.10(c) Flip-chip solder bump assembly

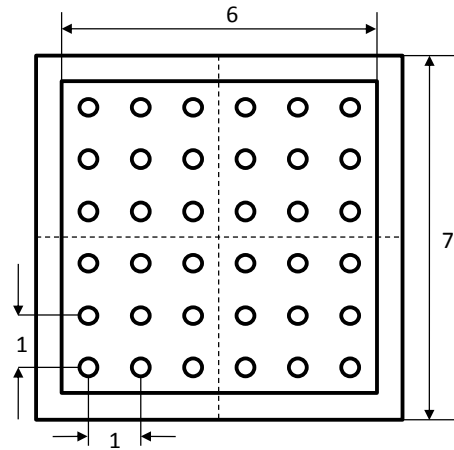


Figure 4.11 6x6 mm silicon chip with 36 I/Os

A quarter model of the assembly is generated based on dimensions shown in Figure 4.12. The interconnect structure located at the edge of the four corners of the silicon die is taken to simulate the worst case solder joint life as the CTE mismatch was the greatest at that region. The FEM representations are shown in Figures 4.13 and 4.14

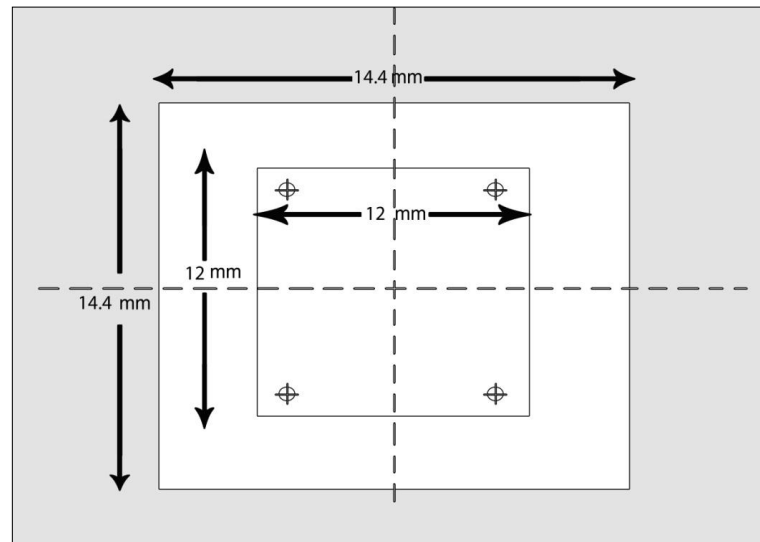


Figure 4.12 Chip and assembly layout geometry for FEM

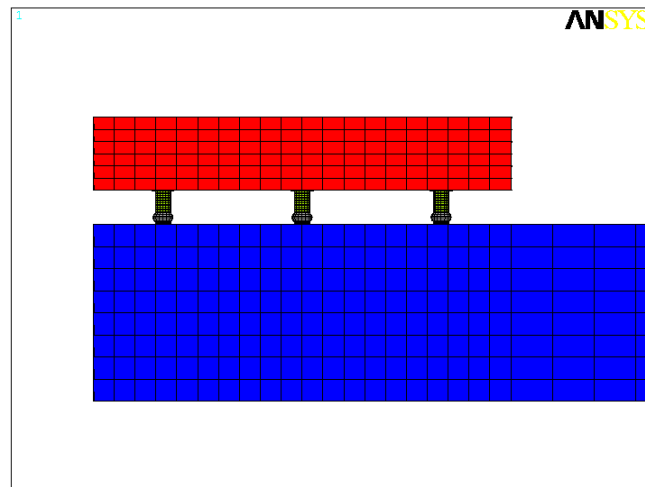


Figure 4.13 Chip assembly FEM side view

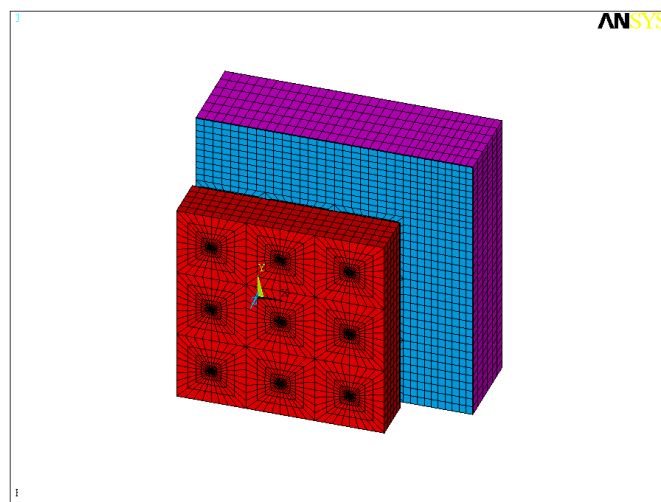


Figure 4.14 FEM meshing of a quarter model

The meshing details of the CPH pillar, Cu pillar and conventional flip-chip solder bump assemblies are shown in Figures 4.15 – 4.17

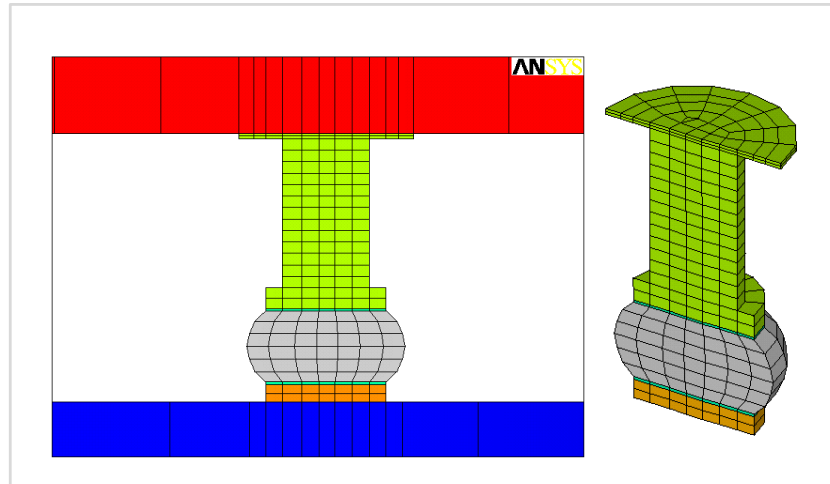


Figure 4.15 CPH pillar and solder joint meshing

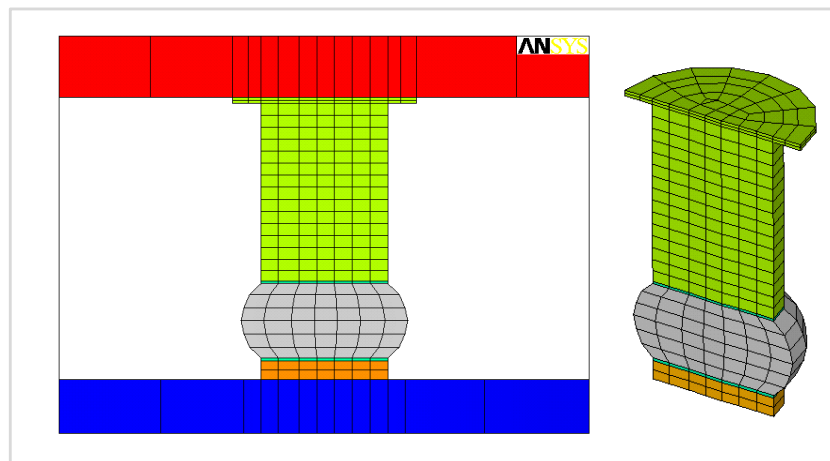


Figure 4.16 Cu Pillar and solder joint meshing

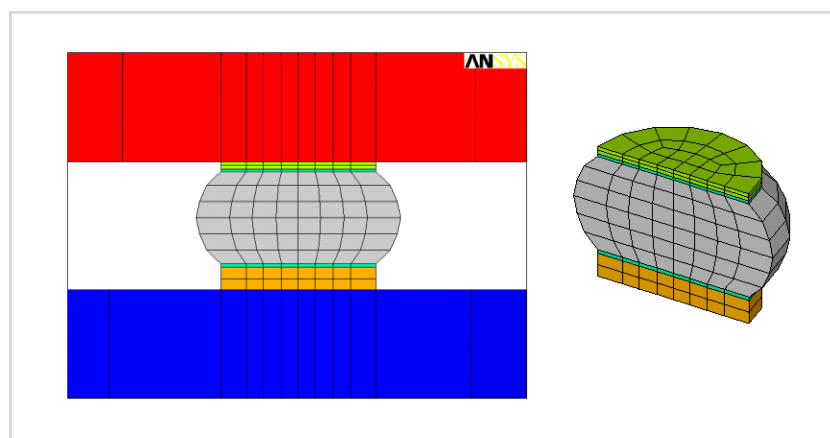


Figure 4.17 Conventional flip-chip solder joint meshing

4.3.4 Materials properties for FEM Modelling

Five materials, namely silicon chip, copper, nickel, SAC solder and PCB substrate are used in CPH pillar, Cu pillar and flip-chip interconnect assemblies. Material properties are obtained from published literature. These material properties are given in Table 4.2. Some temperature dependent material properties are presented separately in Table 4.3.

Table 4.2 Material Properties

Materials	Young's modulus (GPa)	Possion's ratio	CTE (ppm/°C)	Shear modulus (GPa)
Plated Cu	115	0.34	Table 4.3	
FR-4 PCB	in plane (x, z): 20 out-of-plane(y): 9.8	x, z: 0.28 y: 0.11	x, z: 18 y: 50	x, z: 3.5 y: 2.5
Ni	213	0.3	12.9	
Silicon Die	Table 4.3	0.278	Table 4.3	
Solder	Table 4.3	0.35	24.5	

Table 4.3 Temperature dependent material properties

Temperature	−40°C	25°C	50°C	125°C
Solder modulus	54.43	41.73	36.84	22.19
Copper CTE	15.3	16.4	16.7	17.3
Die modulus	192.1	191	190.6	190
Die CTE	1.5	2.6	2.8	3.1

4.3.5 Elastic Plastic Creep (EPC) model

In the EPC model, solder is modelled as an elastic-plastic-creep material with temperature dependent Young's modulus and yield stress. The solder is assumed to exhibit elastic, bilinear kinematic hardening plastic behavior after yield. The temperature dependent yield stress of SAC solder is given as (Schubert A. Et al, 2003):

$$\sigma_y = 7 \times 10^{-6}T^3 + 0.0023T^2 - 0.3122T + 29.142 \text{ (MPa)} \quad (4.8)$$

The creep behaviour of solder is modelled using the hyperbolic sine creep equation, Eq.

$$(4.3). \quad \dot{\epsilon}_c = C_1 \frac{G}{T} \left[\sinh \left(\alpha \frac{\sigma}{G} \right) \right]^n \exp \left[\frac{-Q}{kT} \right]$$

This equation is then re-written into Eq. (4.9) in the required format for implicit creep model (ANSYS, 2002). Table 4.4 lists the constants C_1 , C_2 , C_3 and C_4 for SAC solder. The EPC model can be realized in ANSYS by combining bilinear kinematic hardening plasticity with implicit creep

$$\dot{\epsilon}_c = C_1 [\sinh(C_2 \sigma)]^{C_3} \exp^{-C_4/T} \quad (4.9)$$

Table 4.4 Material constants of creep model for Sn-Ag-Cu solder

Solder Type	C_1	C_2	C_3	C_4
Sn-3.8Ag-0.7Cu	3200	0.037	51	6524.7

The plasticity behaviour of Cu can be represented by the stress-strain relation shown in Figure 4.18, (Yong et al., 2002).

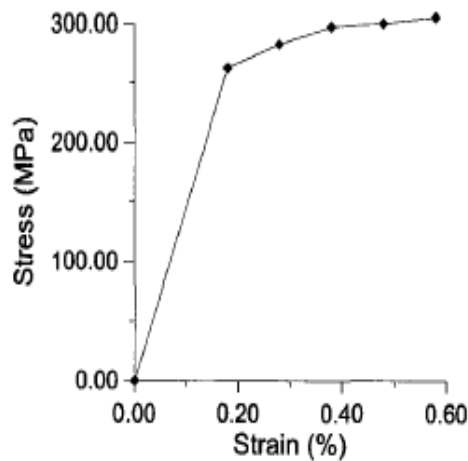


Figure 4.18 Stress-Strain Curve for thin film copper

4.3.6 Loading Condition

The IPC recommended thermal cycling parameters (IPC 9701, 2002) as shown in Figure 4.19 were used in the FEM simulations. The cycling temperatures were between 0°C and 100°C, with a ramp time up / down of 10 minutes and a dwell time of 10 minutes at 0°C and 100°C. The TC profile has a cycle time of 40 minutes.

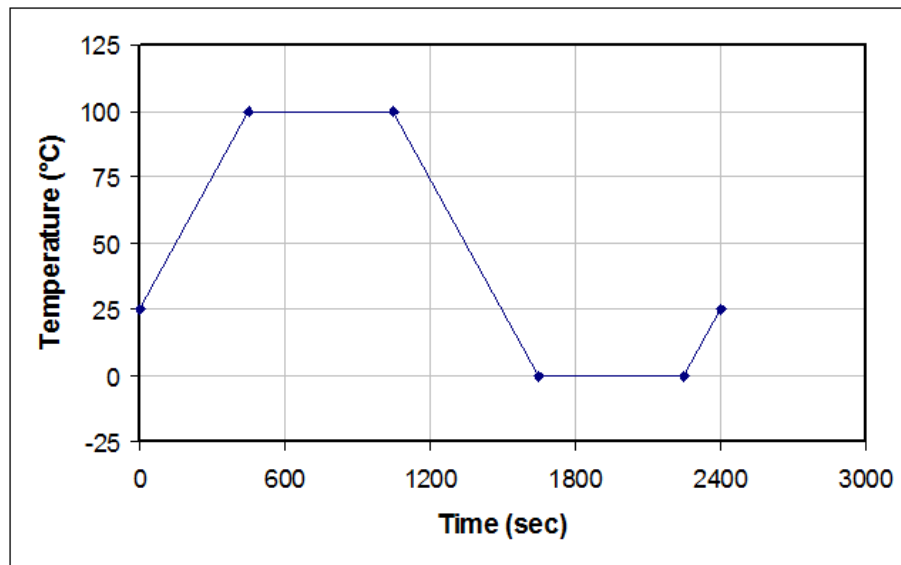


Figure 4.19 Temperature cycling profile FEM simulation

To determine the appropriate number of thermal cycles for simulation, the damage parameters for the conventional solder joint and CPH solder joint are extracted from a three cycle simulation as shown in Figures 4.20 and 4.21 respectively. It is observed that there are only small differences in the damage parameters between the second and third cycle. Hence, a two-cycle simulation approach is used for this study.

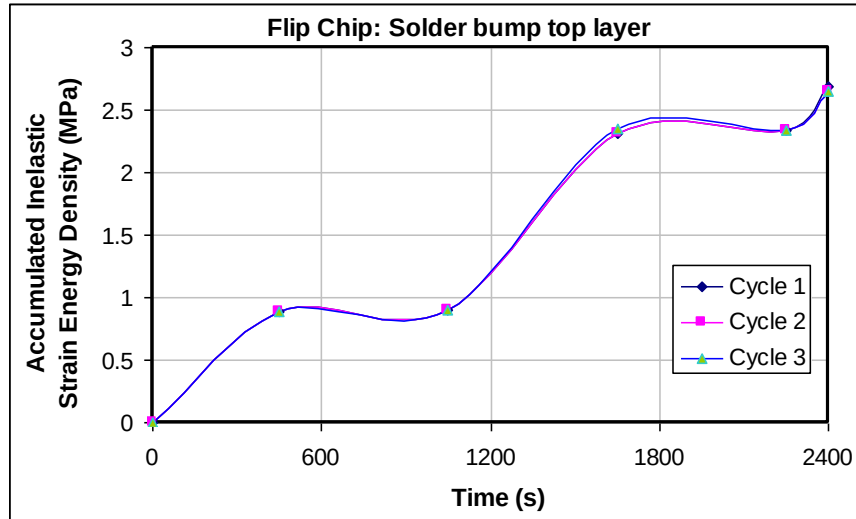


Figure 4.20 Accumulated SED convergence of the flip-chip solder joint

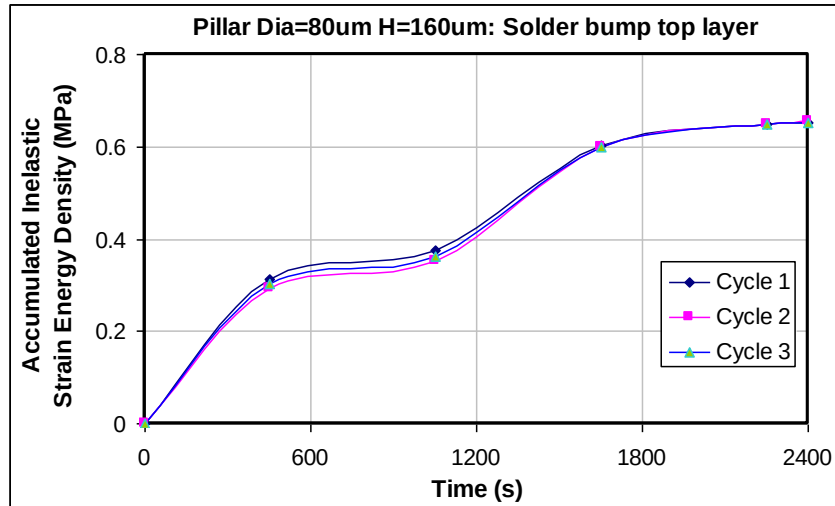


Figure 4.21 Accumulated SED convergence of the CPH solder joint

4.3.7 Volume Averaging

Fatigue life prediction using Strain-based and Energy-based fatigue models highly depends on volume averaging at the interface where a failure initiates and propagates. The critical value of a damage parameter is located at this interface. Failure of a solder joint typically occurs on the top and bottom layer of the solder near the chip interface and the substrate interface.

The accumulated strain energy density is the difference between strain energy density in temperature cycle 1 and cycle 2. Volume averaging is employed to obtain the accumulated creep strain energy density. The volume averaging expression is given as follows:

$$\Delta W_{in} = \frac{\sum_i^n W_{in2}^i \cdot V_2^i}{\sum_i^n V_2^i} - \frac{\sum_i^n W_{in1}^i \cdot V_1^i}{\sum_i^n V_1^i} \quad (4.10)$$

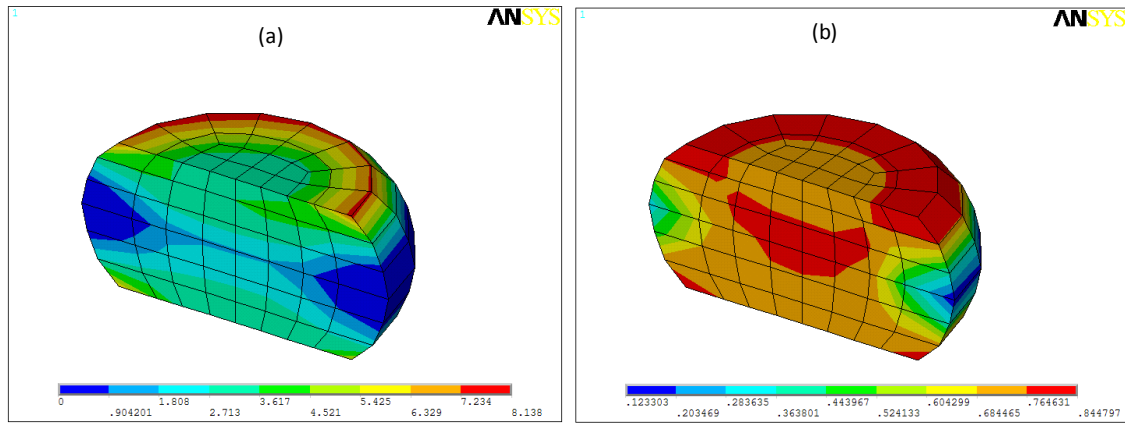
where W_{in2}^i , W_{in1}^i are accumulated strain energy density in temperature cycle 2 and cycle 1. The highest accumulated strain energy density denotes the critical solder joint.

4.3.8 Finite element analysis (FEA) results and discussions

The ultimate goal in the implementation of the CPH pillar bump assembly is to improve the solder joint reliability without the need for an underfill. To verify this potential, FEA modelling and simulation was carried out. Three types of assembly, namely: i) CPH pillar, ii) Cu pillar and iii) conventional flip-chip solder joints were modelled and finite element analyses were carried out to benchmark their reliability performance.

- **FEA results of conventional flip-chip solder joint**

Taking the accumulated inelastic strain energy at the second cycle as shown in Figures 4.22 and 4.23, the FEA results for flip-chip solder joint shows that the corner bump on the die has the highest accumulated plastic work at the solder-chip interface. Hence the solder joint failure is likely to occur at the chip side.



Conventional flip-chip solder bump

Figure 4.22 (a) Creep strain energy plot (b) Plastic strain energy plot

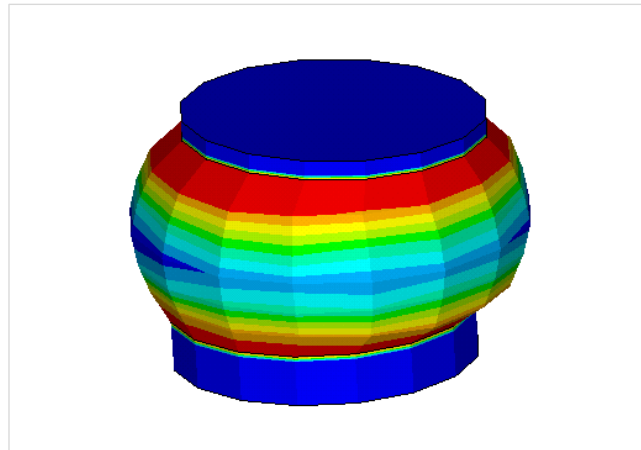
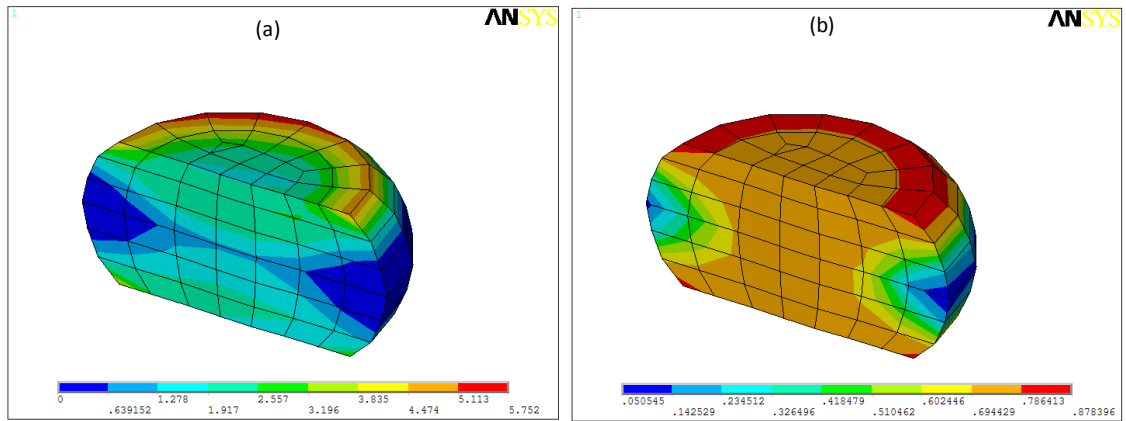


Figure 4.23 Flip-chip solder joint deformation profile

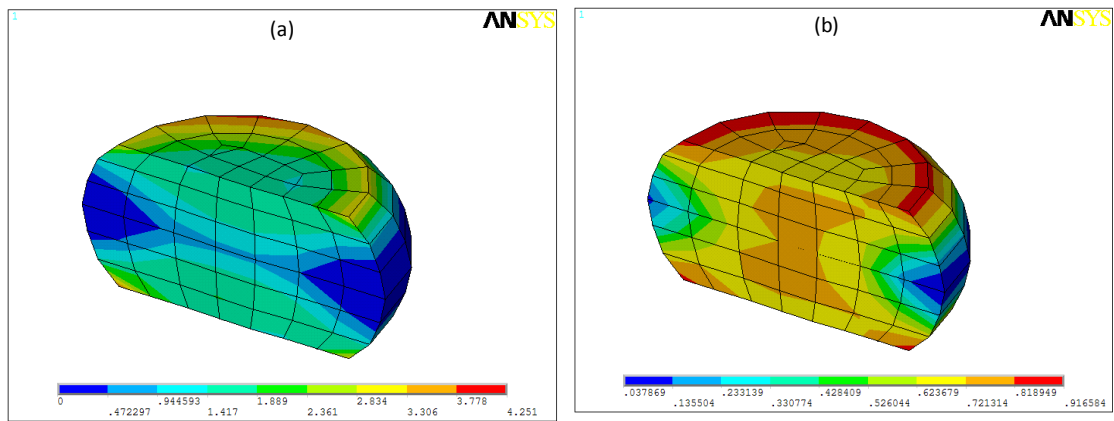
- ***FEA results of Cu pillar solder joint***

With the addition of a Cu pillar structure which is 75 μm in height, there is a small reduction in accumulated strain energy density at the critical joint solder-chip interface. When the Cu pillar height is increased to 160 μm , the accumulated strain energy density in the solder joint is reduced significantly and the maximum strain energy is shifted to the solder-substrate interface.



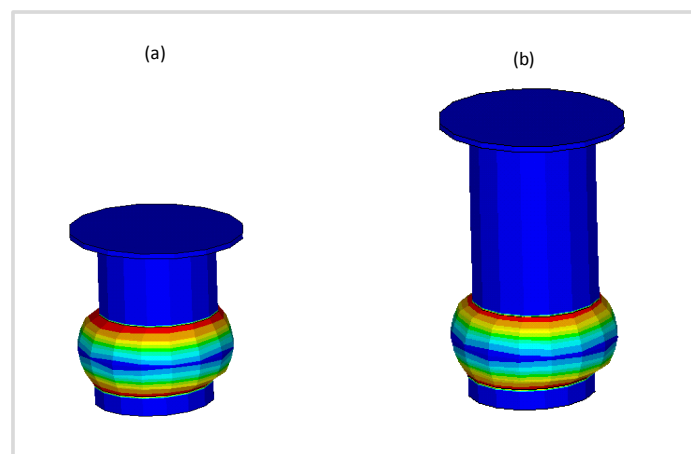
Solder bump connected to a conventional Cu pillar of 75 μm height

Figure 4.24 (a) Creep strain energy plot (b) Plastic strain energy plot



Solder bump connected to a conventional Cu pillar of 160 μm height

Figure 4.25 (a) Creep strain energy plot (b) Plastic strain energy plot



Solder joint deformation profile

Figure 4.26 (a) Cu pillar of 75 μm height , (b) Cu pillar of 160 μm height

- **FEA results of CPH pillar solder joint**

When a 75 μm tall CPH pillar is attached to the solder joint, a further reduction in accumulated strain energy is observed in the solder joint as compared to a Cu pillar solder of similar height. With a 160 μm tall CPH pillar, the strain energy reduction in the solder is even more significant. The maximum strain energy density in the solder joint attached to 75 and 160 μm CPH pillar is found at the solder-substrate interface.

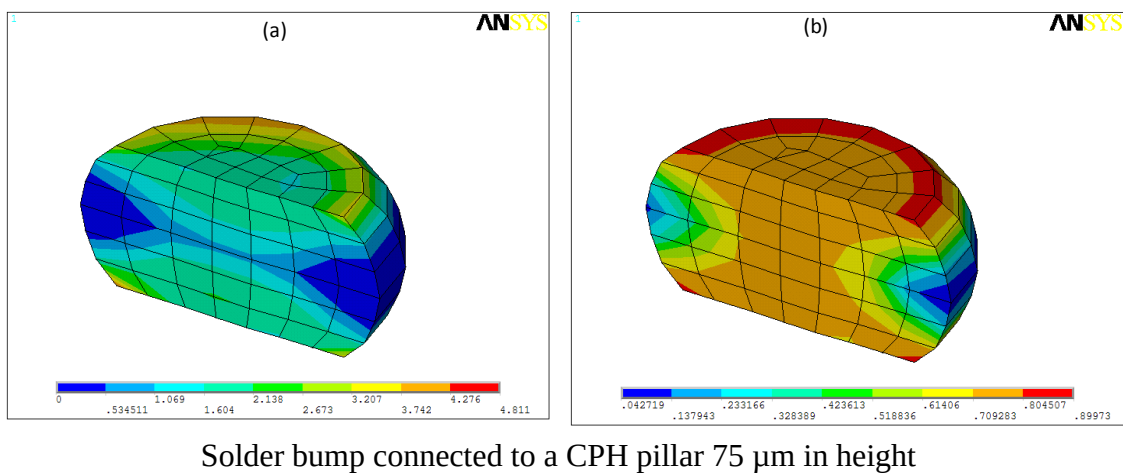


Figure 4.27 (a) Creep strain energy plot (b) Plastic strain energy plot

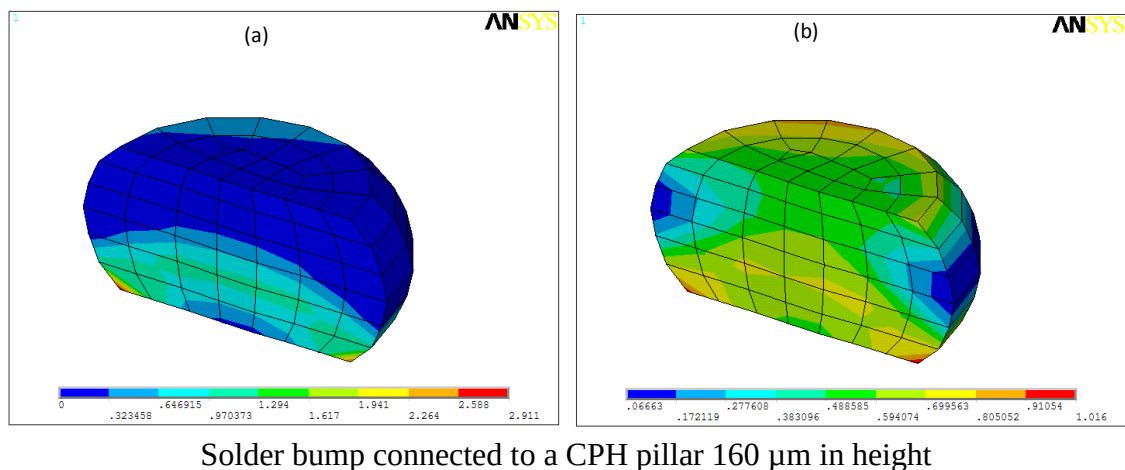


Figure 4.28 (a) Creep strain energy plot (b) Plastic strain energy plot

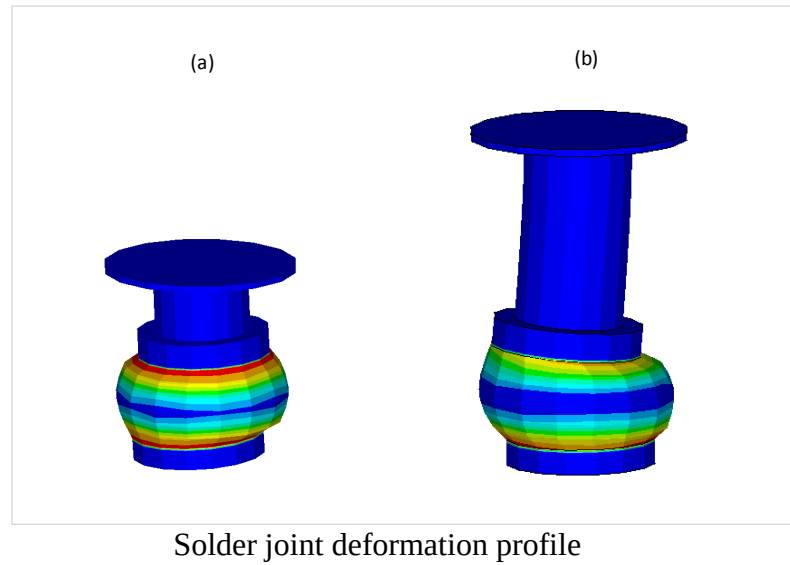


Figure 4.29 (a) CPH pillar of 75 μm height, (b) CPH pillar of 160 μm height

- ***FEA results of Cu and CPH pillars***

The von Mises strain range is used as a damage parameter for the evaluation of fatigue life of the Cu and CPH pillars. The von Mises strain contour plots for both structures are extracted and presented in Figures 4.30 and 4.31.

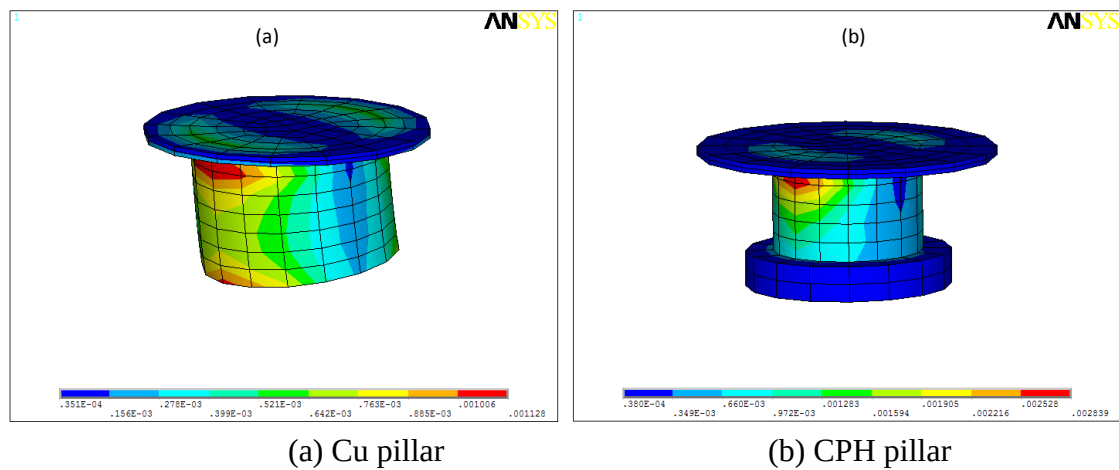


Figure 4.30 von Mises strain and deformation plots of pillars 75 μm in height

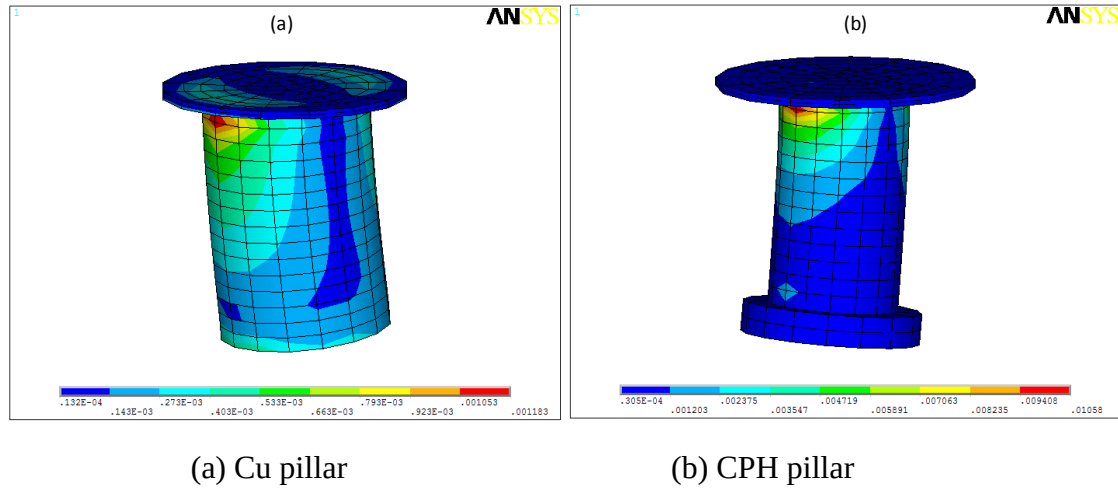


Figure 4.31 von Mises strain and deformation plots for pillars 160 μm in height

The location of the maximum equivalent plastic strain, which is the region of likely failure, is at the top side of the pillar (chip side), for both Cu and CPH pillars of heights 75 and 160 μm .

- ***Fatigue life prediction of CPH pillar, Cu pillar and conventional flip-chip assemblies***

It is assumed that the worst-case exposure for consumer electronics is 0 $^{\circ}\text{C}$ ($T_{\min}$), 60 $^{\circ}\text{C}$ ($T_{\max}$) and 365 cycles per year; where $T_{\min}$ and $T_{\max}$ are the operational minimum and maximum temperatures (IPC9701, 2002). Major electronic packaging manufacturers are evaluating package-on-package (PoP) using a non-filler underfill with a temperature cycling test with 500 cycles as one of the requirements (Lee et al, 2007). Hence, the reliability criterion for CPH pillar assembly is set at 0 – 100 $^{\circ}\text{C}$ temperature range and 500 cycles.

The solder joint fatigue results for the conventional flip-chip, Cu pillar and CPH pillar assemblies are given in Tables 4.5 – 4.7. From Table 4.6, it can be observed that increasing the height of the Cu pillar will result in an increase in fatigue life for the solder joint compared to the flip-chip solder assembly in Figure 4.5. The increase in

solder joint life is due to the increase in compliance in the Cu pillar interconnection between the chip and substrate. The deformation is taken partly by the bending of the Cu pillar. With the introduction of a pinhead on the CPH pillar, the diameter of the Cu pillar can be reduced while the solder joint geometry is maintained. This contributes to better flexibility in the CPH pillar-to-solder joint interconnection system.

Table 4.5 Flip-chip solder joint fatigue life prediction (assembly without underfill)

Interconnect type	Flip-chip solder joint	
Solder Joint Location	Chip-side	Substrate -side
ΔW (creep) (MPa)	0.3851	0.3755
ΔW (plastic) (MPa)	2.2598	1.8470
ΔW (overall) (MPa)	2.6449	2.2225
Fatigue Life	203	247

Table 4.6 Cu pillar solder joint fatigue life prediction (assembly without underfill)

Interconnect Type	Cu pillar solder joint			
Cu pillar Dia. (um)	110			
Cu pillar Height (um)	75		160	
Solder Joint Location	Chip-side	Substrate -side	Chip-side	Substrate -side
ΔW (creep) (MPa)	0.3927	0.3816	0.3858	0.3859
ΔW (plastic) (MPa)	1.9688	1.6566	1.4369	1.4985
ΔW (overall) (MPa)	2.3615	2.0382	1.8227	1.8844
Fatigue Life	231	272	308	297

Table 4.7 CPH pillar solder joint fatigue life prediction (assembly without underfill)

Interconnect Type	CPH pillar solder joint			
Cu pillar Dia. (um)	80			
Cu pinhead Dia. (um)	110			
Cu pillar Height (um)	75		160	
Solder Joint Location	Chip-side	Substrate -side	Chip-side	Substrate -side
ΔW (creep) (MPa)	0.3933	0.3864	0.3234	0.3764
ΔW (plastic) (MPa)	1.5407	1.6490	0.3317	0.9399
ΔW (overall) (MPa)	1.9340	2.0355	0.6551	1.3163
Fatigue Life	288	272	965	443

From Table 4.7, it can be seen that increasing the height of the CPH pillar will result in an increase in fatigue life of its solder joint. The FEA fatigue lives of the conventional flip-chip, Cu pillar and CPH pillar solder joints are shown in Figure 4.32. The CPH pillar solder joint fatigue life is 443 cycles after temperature cycling between 0-100 °C. Conceptually, this is close to the expected 500 cycles in a temperature cycling reliability test for most consumer electronics. The Cu pillar with the same height survived 297 cycles under the same temperature cycling condition and the conventional flip-chip solder joint survived only 203 cycles.

From Table 4.8, a different trend can be observed for the fatigue life of the Cu pillar. The fatigue lives of the two Cu pillars, with 110 μm diameter / 75 μm height and 110 μm diameter / 160 μm height, are in the range of 180,000 – 160,000 cycles respectively. To survive such high fatigue cycles, the Cu pillars have to be stressed mainly within the elastic range and accumulated very little plastic strain. The results also indicate that an increase in the height of the Cu pillar leads to a decrease in the fatigue life.

A similar trend is observed in the two CPH pillars. The CPH pillar with 80 μm diameter / 75 μm height has a fatigue life of 19,048 cycles, and the CPH pillar with 80 μm diameter / 160 μm height has a fatigue life of 775 cycles. The FEA results show that the 75 μm tall CPH pillar has an accumulated plastic strain of 0.284% and the 160 μm tall CPH pillar has an accumulated plastic strain of 1.058. The significant reduction in fatigue lives of the CPH pillars is an indication that the CPH pillars have yielded and the accumulated plastic strains have contributed to a decrease in their fatigue lives.

Table 4.8 CPH and Cu pillars fatigue life predictions

Interconnect type	CPH Pillar		Cu Pillar	
Cu pillar Dia (μm)	80		110	
Cu pinhead Dia (μm)	110		N.A.	
Cu pillar Height (μm)	75	160	75	160
$\Delta\epsilon$ (%)	0.284	1.058	0.113	0.118
Fatigue Life	19048	775	179961	160607

From the FEA and fatigue analysis results, it can be seen that the fatigue lives of the Cu pillars and CPH pillars are higher than those of the solder joint fatigue lives underneath them. Therefore, fatigue failure is expected to lie in the solder material and not in the Cu or CPH pillar structures. It is clear that the solder joint on the CPH pillar with diameter 80 μm /160 μm height has the highest fatigue life. As FEA life prediction might be conservative, it is decided that conventional flip-chip and CPH pillar bumps as shown in Figure 4.23 should be fabricated for experimental testing to verify their actual reliability performance.

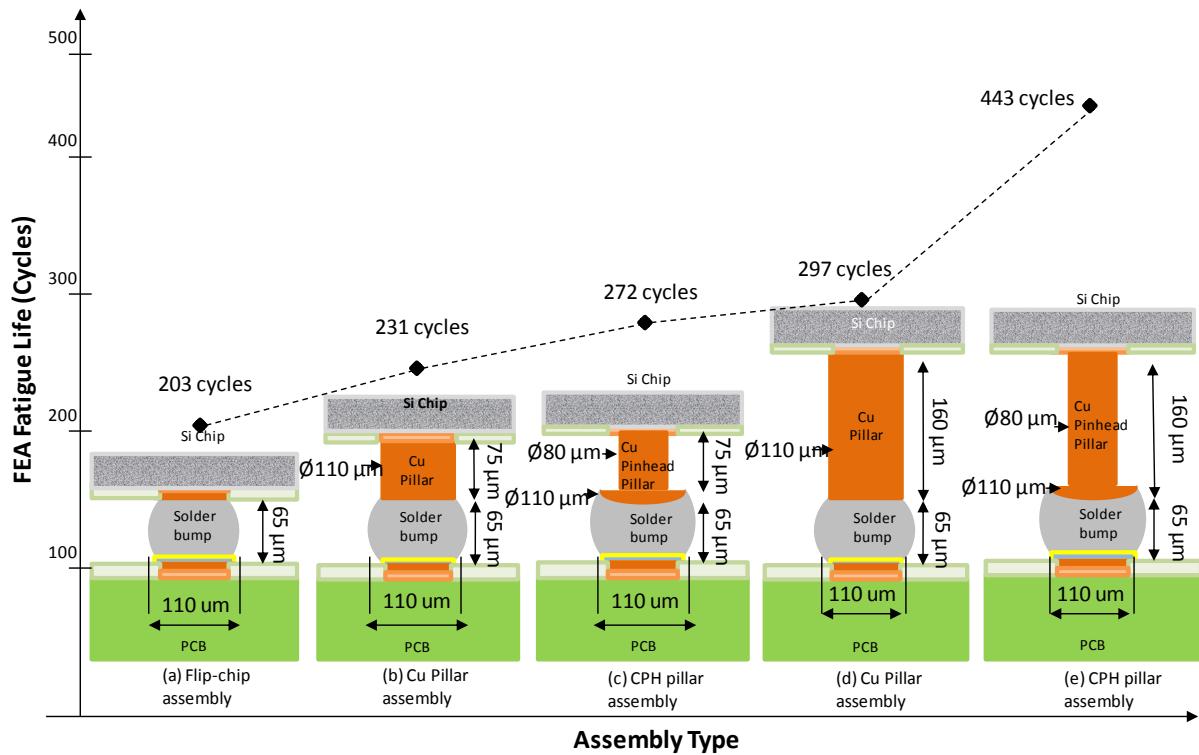


Figure 4.32 FEA fatigue lives of the conventional flip-chip, Cu pillar and CPH pillar solder joints

4.4 Summary

A new copper pinhead (CPH) pillar-to-solder joint structure is designed for flip-chip assembly. The FEA results show that the CPH pillar interconnection provide sufficient compliance to the solder joint to eliminate the need for an underfill.

Solder joint fatigue analyses were conducted to benchmark the CPH pillar solder joint with Cu pillar and conventional flip-chip solder joints. It is observed that the strain levels in the CPH pillar structure are much lower, confirming the effectiveness of the compliant feature in the proposed CPH pillar-to-solder joint interconnection. The failure location of the flip-chip model with only solder joint is at the silicon die-side as expected. The failure location of the 75 μm tall Cu pillar interconnection is at the silicon die-side and the 160 μm tall Cu pillar interconnection fails at the substrate side. For the CPH pillar interconnections, all the failures are

observed at the substrate side. The increase in compliance brought about by the implementation of the Cu pillar and CPH pillar structures has a strain relieving effect on the solder joint due to the bending of the compliant copper pillars. Hence, the accumulation of inelastic strain in the solder joint is reduced, resulting in a better solder fatigue performance. The Cu pinhead design, in particular, has allowed the Cu pillar diameter to be reduced without reducing the solder joint volume and pad area.

In the parametric studies, it is observed that for both the Cu pillar and CPH pillar interconnection, an increase in the height of the copper structure gives an increase in solder joint fatigue lives. The CPH structure is preferred over the Cu pillar structure as the former is more compliant and has a longer solder fatigue life.

For a solder joint reliability requirement of 500 cycles at 0 to 100 °C, the recommended CPH pillar geometry is a pillar diameter of 80 μm , at least a 160 μm height and 110 μm pinhead diameter. As the FEA fatigue life prediction may be conservative, experimental testing will be carried out to verify the actual reliability of the CPH pillar solder interconnection.

Chapter 5 Fabrication of Copper Pinhead Pillar Bumps for Flip-chip Interconnection

5.1 Introduction

Cu pillars on silicon wafers can be produced by a series of photolithography, electroplating and etching processes. Damascene plating and through-mask plating are two options considered for the Cu pillar fabrication. The through-mask plating process is a bottom-up approach where the metal is deposited at the bottom seed layer and gradually built up within the confines of the thick photoresist template openings. Through-mask process is ideal for plating free-standing structures as it is a simpler and lower cost process when compared to damascene plating. Damascene plating is better suited for embedded structures and when there is a need for the barrier layer to be retained between conductor and insulator layers.

The Cu pinhead (CPH) pillar damascene plating involves two photolithography masks and six process steps. The process flow is illustrated in Figure 5.1(a) and the process steps are as follows:

- (i) spin-coat and UV pattern photoresist-PR1
- (ii) sputter TiW adhesion layer followed by Cu seed layer
- (iii) electroplate Cu in and over via
- (iv) spin-coat and UV pattern photoresist-PR2
- (v) etch down to form pin-head over Cu pillar
- (vi) strip PR1 & PR2 to reveal pin-head Cu pillar.

The through-mask plating, in contrast, applies only one photolithography mask and has five process steps. The pinhead on the Cu pillar is formed when isotropic

deposition of copper ions on the pillar continues above the patterned photoresist. The process flow is illustrated in Figure 5.1(b).

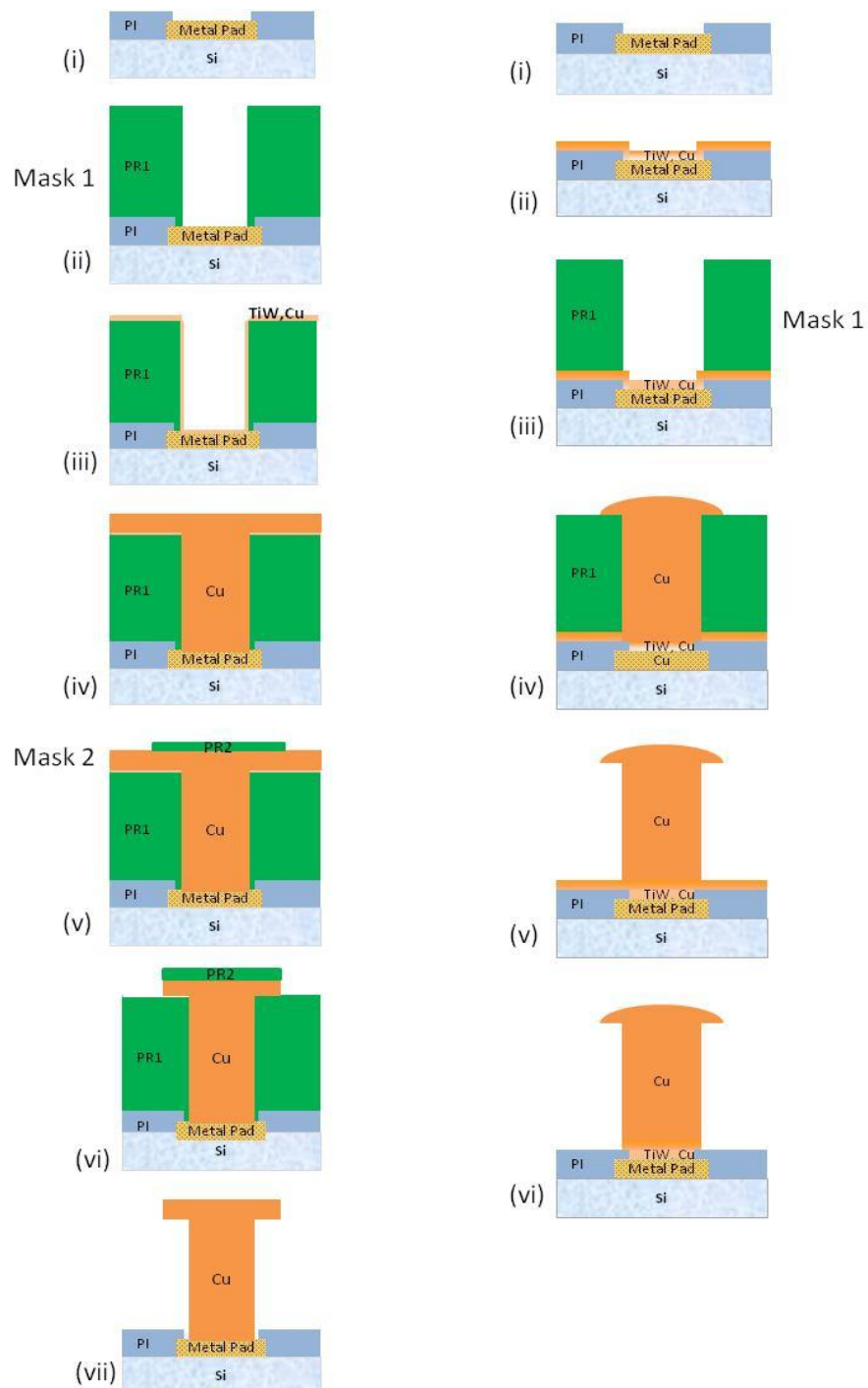


Figure 5.1 (a) Damascene Plating

(b) Through-Mask Plating

The through-mask process steps are as follows:

- (i) sputter TiW adhesion layer followed by Cu seed layer
- (ii) spin-coat and UV pattern photoresist-PR1
- (iii) electroplate Cu in and over via to form a pin-head over Cu pillar
- (iv) strip PR1 to reveal pin-head Cu pillar
- (v) etch off seed and adhesion layers to complete the process.

5.2 Kinetics of electrodeposition

Electrodeposition of metals is performed by immersing a conductive surface in a solution containing ions of the metal to be deposited. The surface is electrically connected to an external power supply and a current is passed through the surface into the solution. This causes a reaction between the metal ions M^{z-} and the electrons e^- to form metal M : $M^{z-} + ze^- = M$.

To electroplate Cu on a silicon wafer, the wafer has to be coated with a thin conductive seed layer of Cu and immersed in a solution containing cupric ions. Electrical contact is made with the seed layer and a current is supplied to activate the $Cu^{2+} + 2e^- = Cu$ reaction at the wafer surface. The equilibrium electrode potential E between the metal and its ions in the electrolyte can be established using the Nernst Equation (Schlesinger, 2000):

$$E = E^0 + \frac{RT}{nF} \ln a \quad (5.1)$$

where E = equilibrium electrode potential (V)

E^0 = standard electrode potential (V)

R = gas constant

T = absolute temperature ($^{\circ}K$)

a = concentration of metal ions

$F = \text{Faraday's constant}$

$n = \text{charge of deposited ions}$

When the electrode is a part of the electroplating cell where current is flowing through, its potential will differ from the equilibrium potential. If the equilibrium potential of the electrode is E and the potential of the same electrode as a result of the current flowing is $E(I)$, then the difference η between these two potentials is called overpotential.

$$\eta = E(I) - E \quad (5.2)$$

The wafer is electrically connected at the cathode so that the metal ions deposited on its surface are reduced to metal atoms. Another electrically active surface, known as the anode, is present in the conductive solution to complete the electrical circuit. At the anode, an oxidation reaction occurs to balance the current flow at the cathode, thus maintaining electrical neutrality in the solution.

In the absence of any secondary reaction, the current delivered to a conductive surface during electroplating is directly proportional to the quantity of metal deposited approximated by the Faraday's Law (W. Ruythooren et al., 2000). The plated mass can be found using Equation (5.3) or alternatively the plating rate can be expressed as Equation (5.4).

$$m = \alpha \frac{ItM}{nF} \quad (5.3)$$

$$\frac{h}{t} = \alpha \frac{IM}{nFA\rho} = \alpha \frac{iM}{nF\rho} \quad (5.4)$$

where m is the mass of deposited material, α the current efficiency and I the plating current, t the plating duration, n (copper $n = 2$) the charge of the deposited ions, F Faraday's constant (96500 coulombs), h and A the thickness and area of the plated

surface, ρ the density of the deposit, M the molar mass and i the current density. Using this relationship, the mass deposited can be readily controlled through variations of plating current and time.

5.2.1 Current-Potential relationship in electroplating

With no applied potential, no current flow across the interface between the metal and solution, and an equilibrium potential exists between the two. Once the potential is shifted by an external power source away from the equilibrium potential, a current will be driven across the interface. Under conditions typical of most plating processes, the cathodic current density can be derived from the Tafel equation (Zoski, 2007, Schlesinger, 2000):

$$\eta = \frac{RT}{\alpha F n} \ln \left[\frac{i_0}{i} \right] \quad (5.5)$$

where i_0 is the exchange current density, i is the cathodic current density, α the transfer coefficient and η , n , R , T and F have their usual meaning. Figure 5.2 shows a current-potential curve typical of a typical deposition process. As the potential shifts away from the equilibrium potential to the right, the current increases in an exponential manner (Tafel region) and the overall deposition rate is determined largely by the reaction rate at the cathode.

As the potential continues to increase, mass transfer effects become predominant, and a limiting current plateau is reached. This results as the species reacting at the cathode (Cu^{2+}) no longer reach the interface at a rate sufficient to sustain the high rate of reaction. The limiting or maximum current density is given by (Bard, 1980):

$$i_L = \frac{nFD}{\delta} C_b \quad (5.6)$$

where D is the diffusion coefficient of the depositing species Cu^{2+} , c_b is the bulk concentration of Cu^{2+} ions in the solution, δ is the diffusion layer thickness, n the number of electrons involved in the reaction, and F is the Faraday constant.

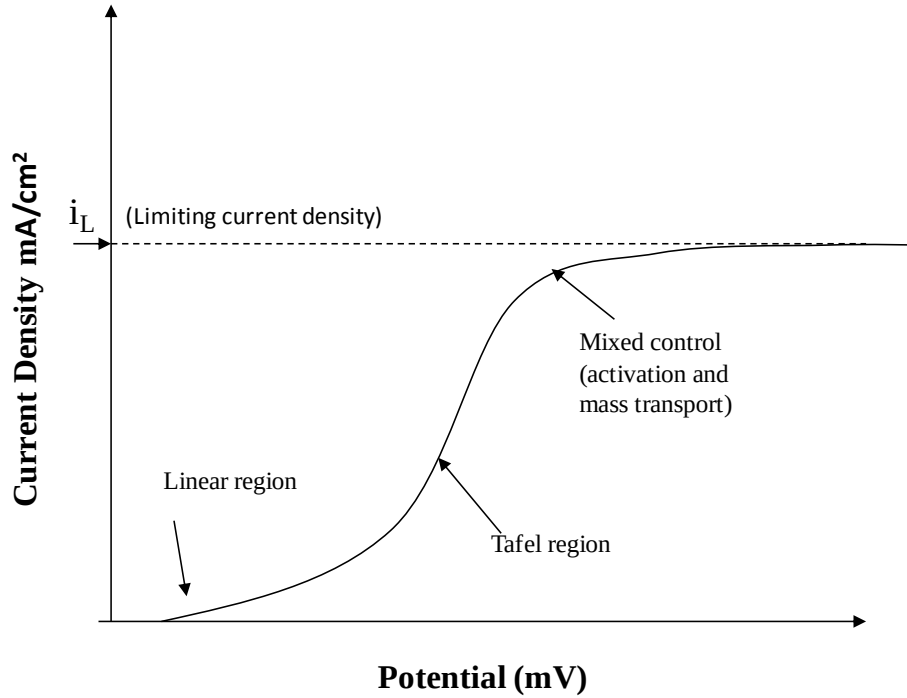


Figure 5.2 Plating current density and potential relationship

The diffusion layer thickness δ is defined by the Nernst diffusion-layer model shown in Figure 5.3 (Schlesinger, 2000). This model assumes that the concentration of Cu^{2+} ions has a bulk concentration of c_b up to a distance δ from the electrode surface and then falls off linearly to $c_{x=0}$ at the electrode surface. It is assumed that the liquid layer within δ is quiescent. Cu^{2+} ions must diffuse through δ to reach the electrode surface. At the limiting current density i_L the species Cu^{2+} are reduced as soon as they reach the electrode. If the current density is greater than i_L , some other reactions and plating defects may occur.

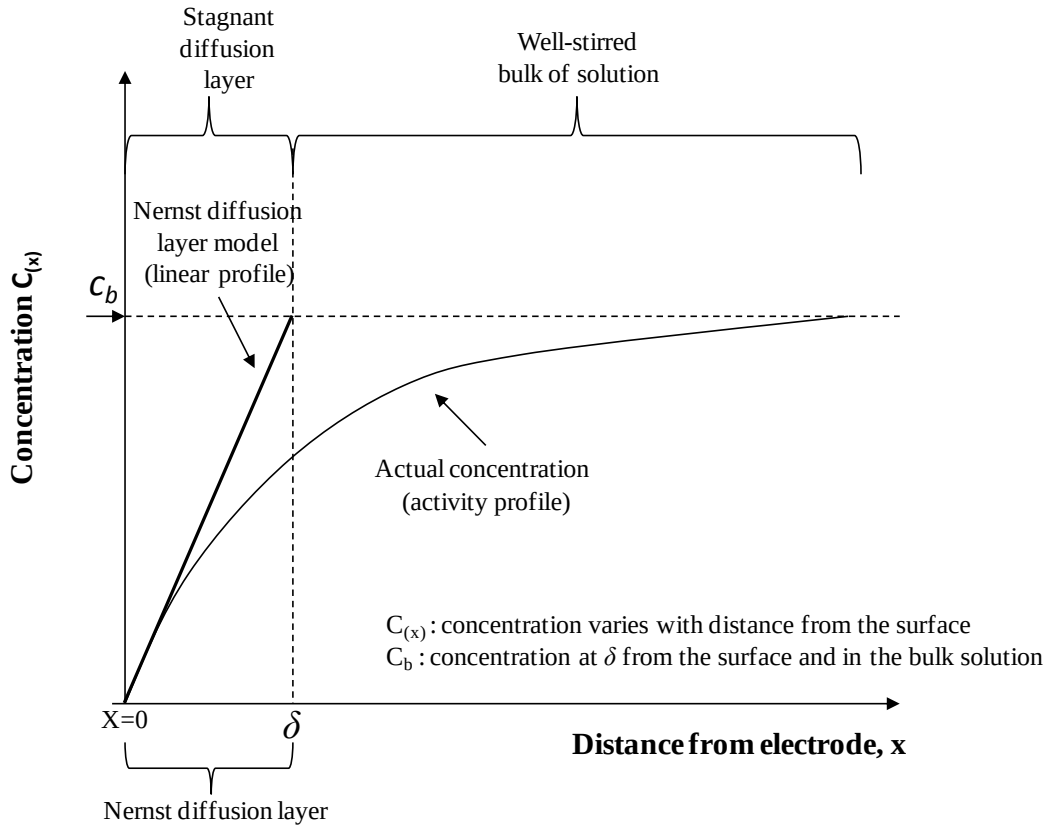


Figure 5.3 Variation of the reactants concentration within the Nernst diffusion layer

To ensure that the rate of mass transfer of electroactive species to the interface is large compared to the reaction rate and uniform across the wafer surface, the rates of diffusion and convection must be understood and controlled. Convection is the most important mode of mass transfer and it can vary from stagnant to laminar or turbulent flow as a result of impinging flow caused by solution pumping, flows that are due to substrate movement and flows resulting from density variations. Electroplating can be carried out using a constant current, a constant voltage, or variable waveforms of current or voltage. If a constant current is used, the mass of deposited metal can be controlled more accurately. Plating with a constant voltage or variable waveforms requires more complex equipment and control. However, this can be useful when tailoring specific thickness distributions and film properties.

5.2.2 Cu pinhead pillar electroplating

The CPH pillar electroplating is carried out using an optimized commercial plating solution with sulfuric acid, copper sulphate and chloride as its main ingredients. Various proprietary additives are added in the plating solution to enhance the via filling and deposition rate. The additives mix typically contains i) relatively large, slow diffusing additives (e.g. polyethylene glycol) which act as plating suppressors at the top and rim of the cavities and ii) smaller fast diffusing enhancers (e.g. organic sulfur compound) which are preferentially adsorbed within the cavities (U. Landau, 2000) to accelerate the deposition of Cu atoms as illustrated in Figure 5.4.

Cu deposition takes place under kinetics control and in this regime the deposition rate is sensitive to the Cu concentration and plating additives at the boundary layer across the wafer. As metal ions are depleted in the electrodeposition process, their replenishment of metal ions and additives are mass transported to the convection zone by a regulated flow of electrolyte directed towards the wafer.

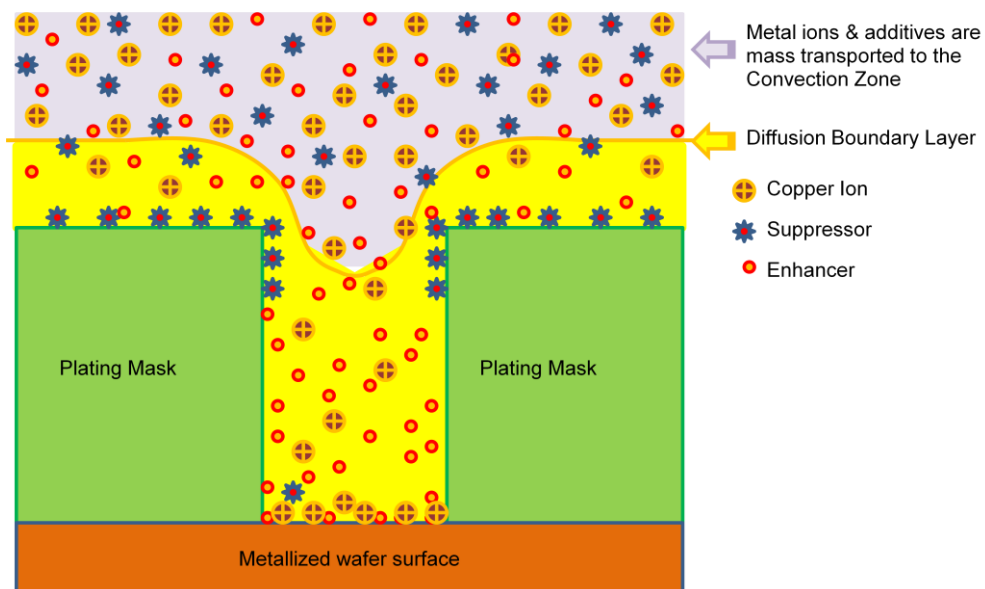


Figure 5.4 A cross-section of a plating site on a wafer showing the electrodeposition activities

5.3 Experimental setup

The wafers were processed according to the process steps and parameters as shown in Tables 5.1 (a) and (b).

Table 5.1(a) Lithography process flow and parameters for CPH pillar electroplating

S/N	Process Sequence	Parameters and Procedures
1.	Wafer Preparation	O ₂ at 200 sccm, + Ar at 10 sccm, 30 sec DI water rinse, 60 sec Dehydration bake, 100°C, 5 mins, N ₂ inert chamber
2.	Spin Coat #1	Karl Suss RC8 Spin Coater Clariant AZ 4620, positive photoresist (resist exposure with UV light will be removed the developer solution)Place wafer on vacuum chuck of coater Photoresist is dispensed at the centre of the wafer Spin at 300-800 rpm for 60 seconds Spin speed determines the final thickness of the coating Edge Bead Removal (EBR) to remove excess resist build up at the edge of the wafer after spin coating Spin at 300 rpm, 2 mins, dispense acetone
3.	Soft Bake #1	Place wafer on hotplate. Bake wafer, 90°C, 90 sec, on contact mode (Soft baking evaporates most of the solvents in the photoresist) Cool down to room temperature, 5 mins
4.	Spin Coat #2	Place wafer on vacuum chuck of coater Photoresist is dispensed at the centre of the wafer Spin at 300-800 rpm for 60 seconds Spin speed determines the final thickness of the coating Edge Bead Removal (EBR) to remove excess resist build up at the edge of the wafer after spin coating Spin at 300 rpm, 2 mins, dispense acetone
5.	Soft Bake #2	Place wafer on hotplate Bake wafer, 90°C, 180 sec, on contact mode (Soft baking evaporates most of the solvents in the photoresist) Cool down to room temperature, 5 mins
6.	UV Exposure	Karl Suss Aligner (Broadband 365 – 405 nm UV spectrum at 2.1 mW/cm ² and 4.5 mW/cm ² respectively)
7.	Development	Place resist coated wafer in a beak (resist exposure in UV light will be removed by the developer solution) Soak in potassium-based AZ-400K developer 1:2 part DI water Agitate for 6 minutes at room temperature Rinse thoroughly with DI water and blow dry with nitrogen
8.	Hard Bake	Place developed wafer on hotplate Bake wafer at 100°C for 180 sec on contact mode

Table 5.1(b) Electroplating and etching process flow and parameters for CPH pillars

S/ N	Process Sequence	Parameters and Procedures
1.	Plasma Ashing	Place wafer in AP-1000 March Plasma Chamber To clean and ensure complete removal of resist residues within openings. Set at 400W, 120 sec, O ₂ 200 sccm, Ar 50 sccm
2.	Electroplating	Place wafer with patterned resist openings in EEJA Manual Cup-Plater Plate Cu traces and pillars using Enthone Copper Bath SC Cu plating current is set at constant DC 300mA, 24°C. Plate Ni UBM using Technic Nickel S Nickel plating current is set at constant DC 50mA, 45°C Plate Au over Ni UBM using Gold Technic 434 Au plating current is set at constant DC 50mA, 45°C
3.	Photoresist Stripping	Acetone or AZ100 at ~70°C DI water rinse
4.	Cu Seed Layer Etch-off	98% H ₂ SO ₄ 82ml CircuitprepTH 2040 (from OMI) 40ml 35% H ₂ O ₂ 86ml Water 790ml Temp: 40°C
5.	TiW Adhesion Layer Etch-off	H ₂ O ₂ 30% and DI water 1:3 Temp: 24°C
6.	Finish	DI water rinse and N ₂ dry

5.3.1 Photolithography Patterning for CPH Pillars Electroplating

In this fabrication process, thick photoresist coatings in the range of 40 to 150 μm are required to produce plating masks for Cu pillar electroplating. A Novolak-based Clariant AZ4620 positive photoresist was used to produce various photoresist thicknesses in a multi-step spin coating process. The UV exposure of the photoresist was conducted on a Karl Suss broadband aligner with a UV spectrum of 365 – 405 nm at 2.1 mW/cm² and 4.5mW/cm². Under UV exposure, the development inhibitor in the positive photoresist decomposed and the developer solution dissolved the photoresist in

the exposed areas. The relationship between the film thickness and the spin coating speed is given in Eq. (5.7), (Emslie et al, 1958).

$$h = \frac{1}{2\omega} \sqrt{\frac{3\eta}{\rho t}} = \frac{h_0}{\sqrt{1 + 4\rho\omega^2 h_0^2 \frac{2t}{3\eta}}} \quad (5.7)$$

where: h = film thickness, h_0 = initial film thickness, ρ = resist density, ω = rotation speed, t = coating time, η = viscosity

Table 5.1 shows the process steps involved in the plating mask preparation. Incoming 4-inch silicon wafers were baked in a nitrogen-filled oven at 100°C for 5 minutes. The first layer of AZ4620 photoresist was spin-coated on the wafer. A relatively slow 2-stage rotation coating speed was used to achieve a thick photoresist layer. The resist layer was thicker at the edge of the wafer when a high viscosity resist was used. This is due to an increase in resist viscosity as a result of resist solvent evaporation at the edge of the wafer. An edge bead removal process was required to remove the excess resist build-up. This was followed by a soft bake and cooling to room temperature before subsequent resist coating steps were repeated to build a thicker layer.

5.3.2 CPH pillar fountain plating

A Cup-Plater manual plating system from Electroplating Engineers of Japan Ltd (EEJA) was used for electroplating CPH pillars on silicon wafers. The plating system and setup is shown in Figure 5.5. The wafer was held face down over the impinging flow of electrolyte within a cylindrical plating cell. The flow pattern was manipulated to provide a uniform current distribution across the wafer to ensure good thickness uniformity.

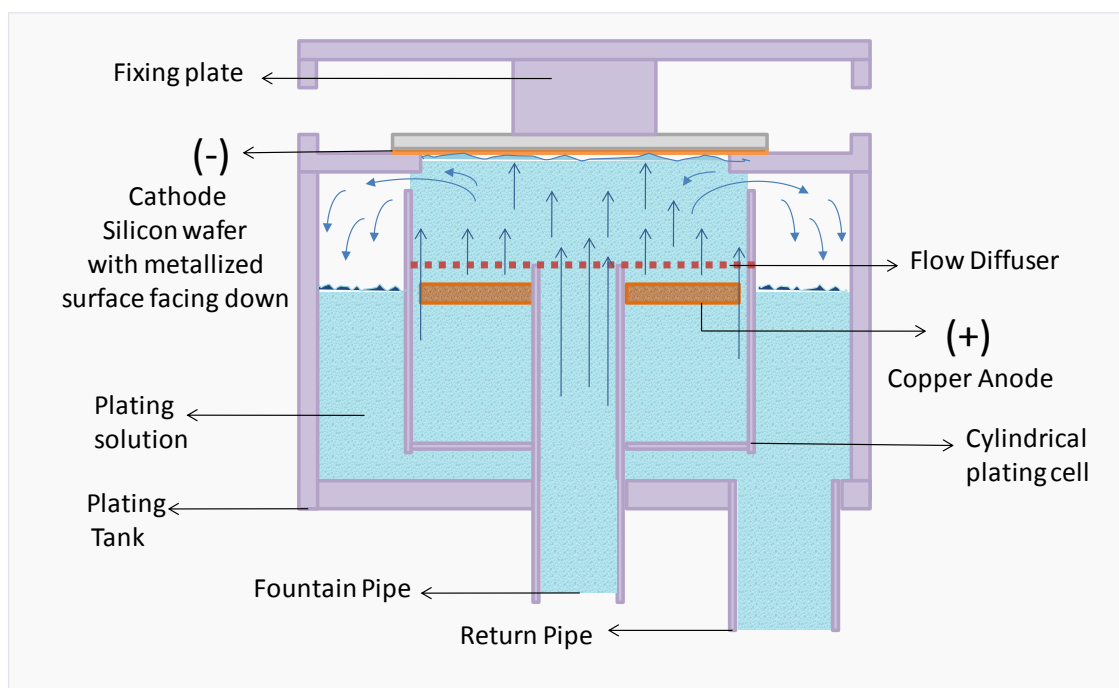


Figure 5.5 Fountain plating system

The plating rate and uniformity on the wafer are largely influenced by the plating cell design, composition of the electrolyte, applied voltage and plating current. In this study, the plating hardware and chemicals were kept constant as they were established specialist products for wafer copper plating.

5.4 Results and discussion

5.4.1 Photoresist Uniformity

Three 4-inch wafers were processed following the flow as shown in Table 5.1. The photoresist thicknesses on twenty-seven points across three 4-inch wafers were measured using a surface profiler. The photoresist thickness uniformity can be calculated using Equation (5.8). The thickness variation plot is shown in Figure 5.6. The average thickness of the photoresist was $46 \pm 1.2 \mu\text{m}$.

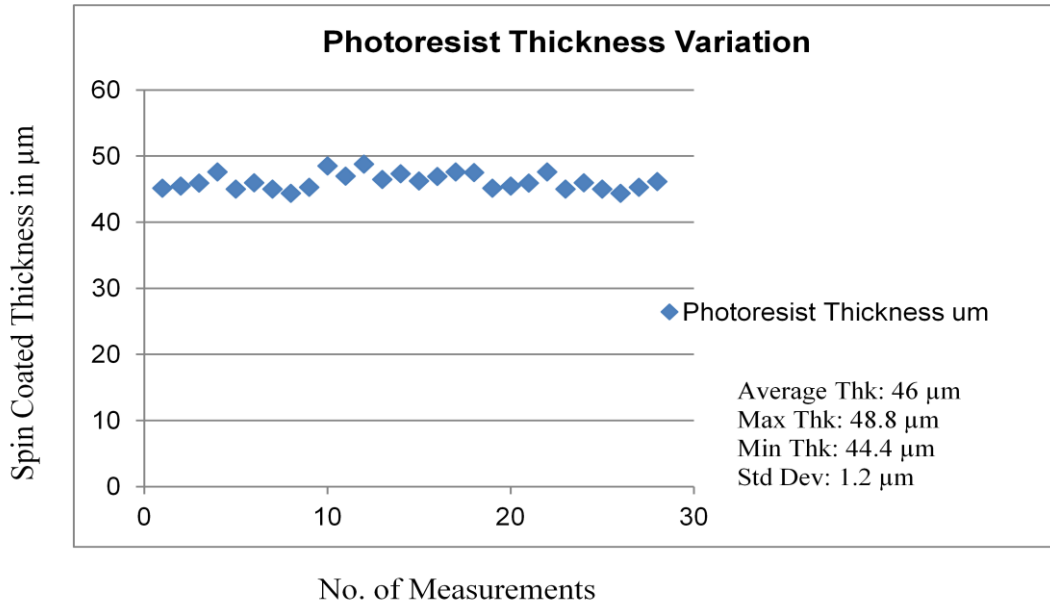


Figure 5.6 Photoresist thickness variation measurements after UV exposure and development

$$\frac{(Thickness_{max} - Thickness_{min})}{(Thickness_{max} + Thickness_{min})} \% = 5\% \quad (5.8)$$

The uniformity of photoresist after exposure and development was found to be 5%. After the exposed resist was developed, a plasma ashing step was introduced to ensure complete removal of residual photoresist at the base within the resist openings. Obtaining a residue-free opening with an aspect ratio of 2 (H: height / D: diameter) is necessary for the subsequent plating process to produce compliant CPH pillar bumps.

5.4.2 CPH pillar plating uniformity

In the CPH pillar plating process, maintaining a good height uniformity of 5% among the CPH pillars across the wafer and within each individual die is desired. As the plated features on the wafer are uniform in size and spacing, the influence of size effect due to variation of feature geometries is not an issue. An evaluation was conducted on plating current settings to optimize the pillar structure geometry specific to the pinhead design. Three plating current settings on constant direct current (DC):

i) 200 mA, ii) 300 mA and iii) 400 mA were selected to evaluate their influence on the deposition rate of Cu and uniformity in 100 μm openings with a 500 μm pitch in a layer of 45 μm thick plating mask.

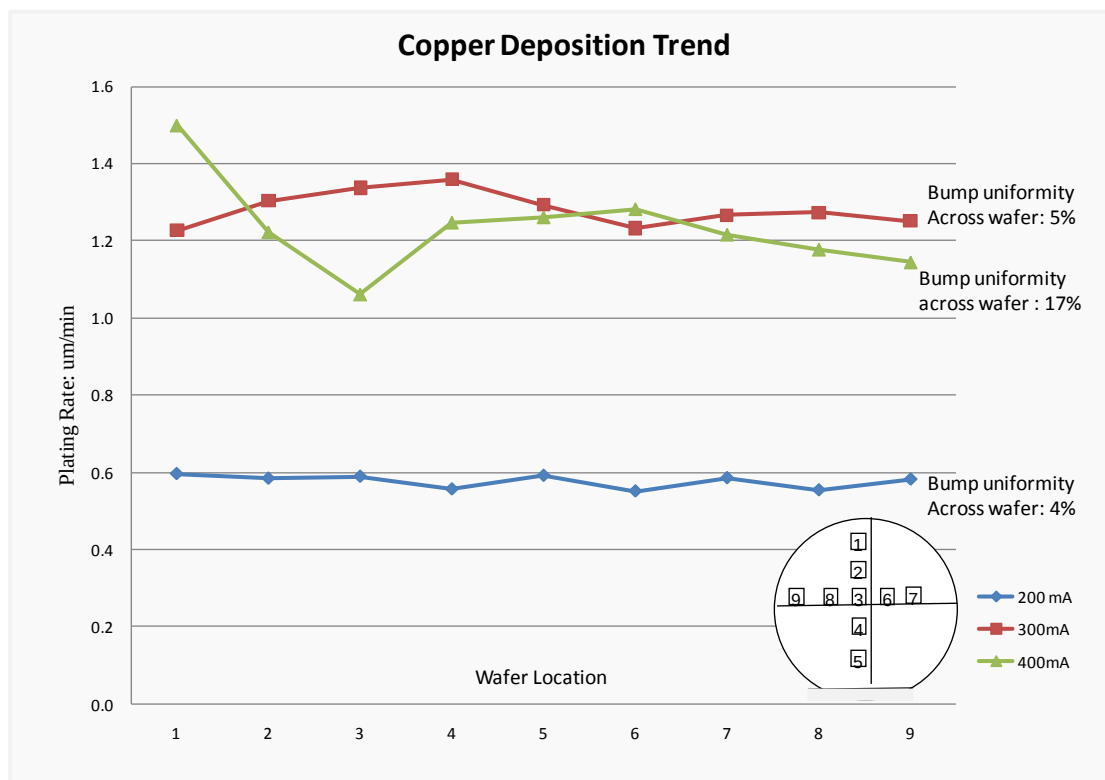


Figure 5.7 Cu deposition trends of various plating current settings

The Cu deposition trends of the three current settings are shown in Figure 5.7. The average deposition rates of 200 mA, 300 mA and 400 mA are 0.6 $\mu\text{m}/\text{min}$, 1.3 $\mu\text{m}/\text{min}$ and 1.2 $\mu\text{m}/\text{min}$ respectively. It was observed that with a 300 mA plating current, a pillar uniformity of 5% across wafer was achieved and this satisfies most industry requirements. Applying 200 mA plating current yielded a slightly better pillar uniformity but the deposition rate was only 46% that of 300 mA. At 400 mA, plating nodules and poor uniformity occurred, and the deposition rate did not increase further.

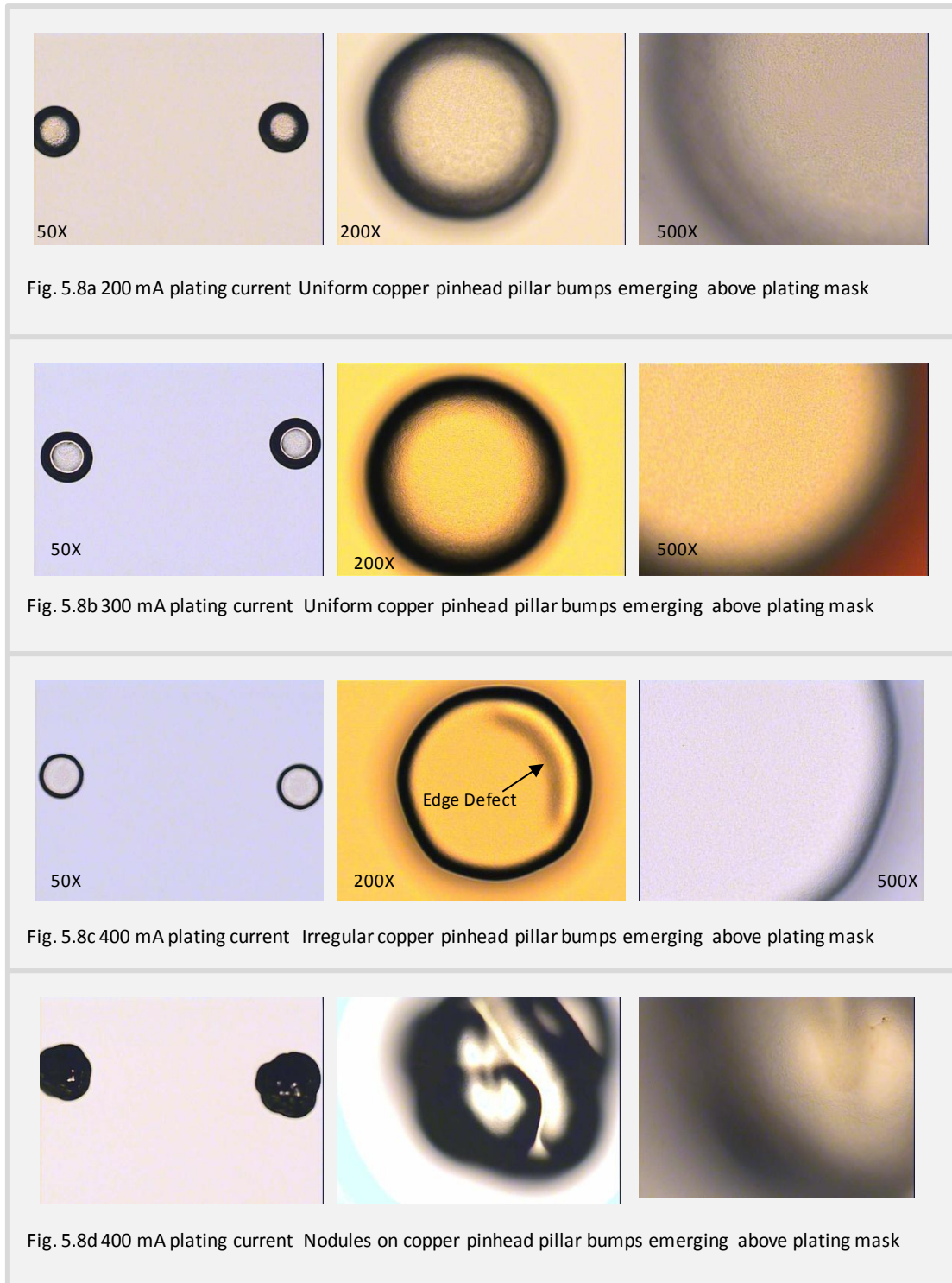


Figure 5.8 CPH pillar profiles using plating current of 200 mA, 300 mA and 400 mA

When plating is carried out at a limiting current, the metal ions are plated as fast as they arrived at the wafer plating sites. Plating beyond the limiting current reduces energy efficiency and the deposition defects increase. It can be deduced that the limiting current for this wafer plating setup is between 300 – 400 mA as the deposition rate started to plateau and plating defects increased beyond this. Figure 5.8 shows the various CPH pillar bump surface profiles and finishing above the plating mask. AFM was carried out on the pillars plated with 300mA to further analyse the surface morphology across the wafer. Figure 5.9 shows the morphology and surface roughness of the pillar top.

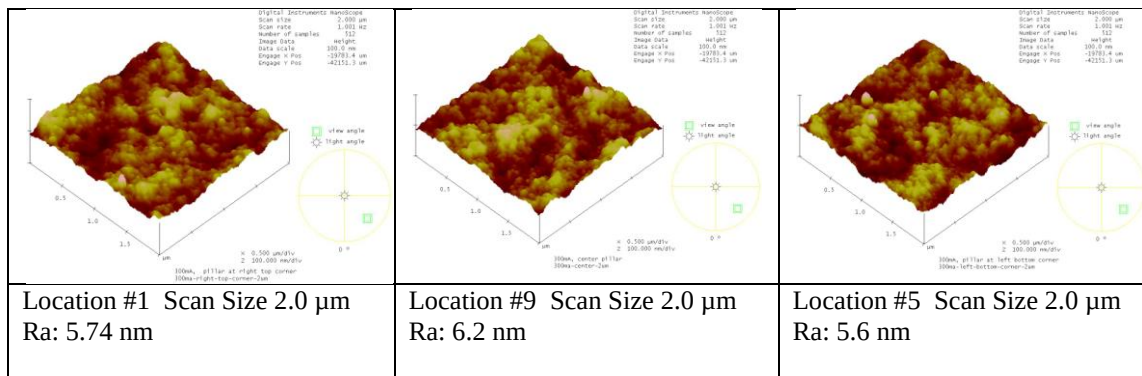


Figure 5.9 Morphology of the top of a copper pinhead pillar bump plated with 300 mA DC

5.4.3 CPH pillar fabrication process development

A series of daisy-chain test chips were fabricated using the optimized plating current of 300 mA deduced in the preceding evaluation. The process flow is shown in Figure 5.10 for a dual-coat 45 μm thick positive resist, AZ4620. The initial plating trial was carried out on 4-inch silicon wafers with a 0.1 μm Ti-0.5 Cu seed layer. The patterned photoresist mask effectively defined the aspect ratio and pitch density of the

metal features to be fabricated. The CPH pillars and additional layers of UBM comprised of nickel and gold could be plated sequentially in different plating tanks.

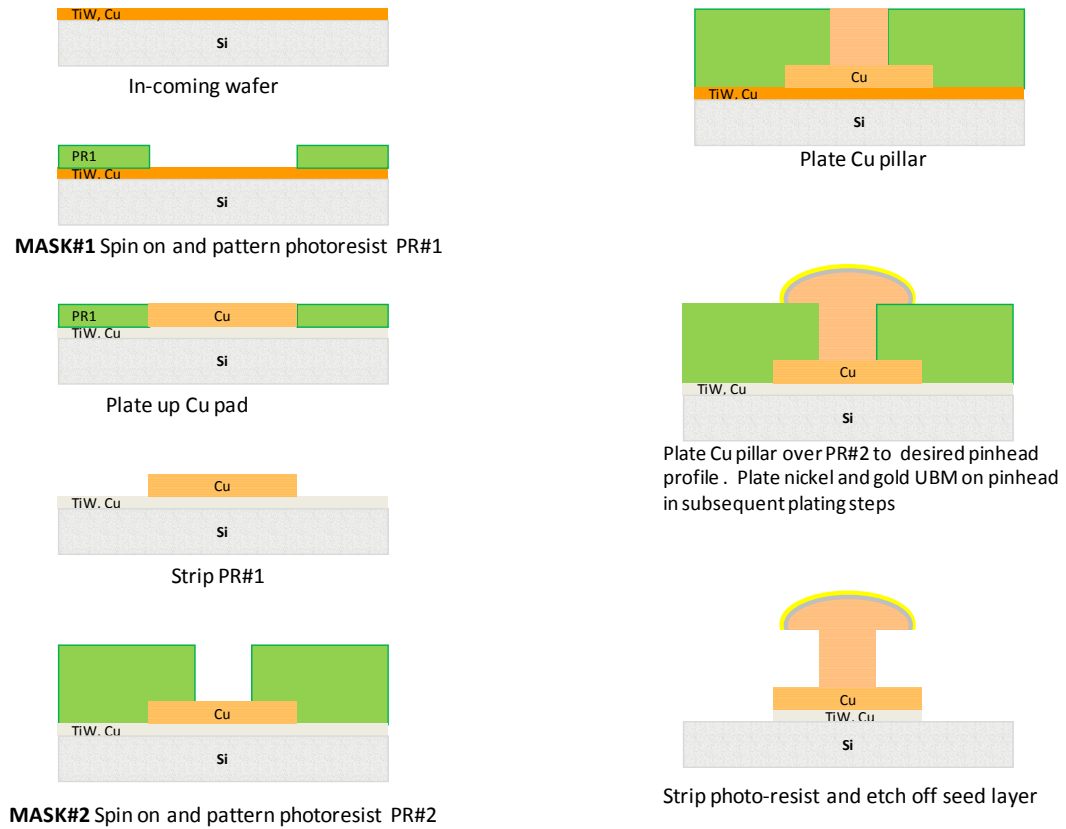


Figure 5.10 Electroplating of CPH pillar bump and Ni-Au UBM

The plating was conducted in a fountain cup plating system as shown in Figure 5.5. As the fountain flow of electrolyte, containing copper ions and plating additives, impinged the wafer surface, the relatively larger and slow diffusing suppressors settled on the top and the rim of the cavities and the fast diffusing enhancers were preferentially adsorbed into the cavities and promoted rapid copper deposition. The fast deposition rate within the cavities did not slow down immediately when the plated Cu pillars reached the top surface of the plating resist. It is most likely that the pillar surface was free of suppressing additives (U. Landau, 2000). Redistribution of enhancing and suppressing additives will take some time. Consequently, a convex

pinhead was formed on the top of the pillar even as isotropic Cu deposition takes place when the pillar emerged from the plating resist. Taking advantage of this plating behaviour, a Cu pillar with a pinhead can be fabricated. The successfully plated Cu pinhead pillar (CPH) bumps of the initial trial are shown in Figure 5.11. The pinheads on top of the Cu posts were well-defined for subsequent solder bump attachment.

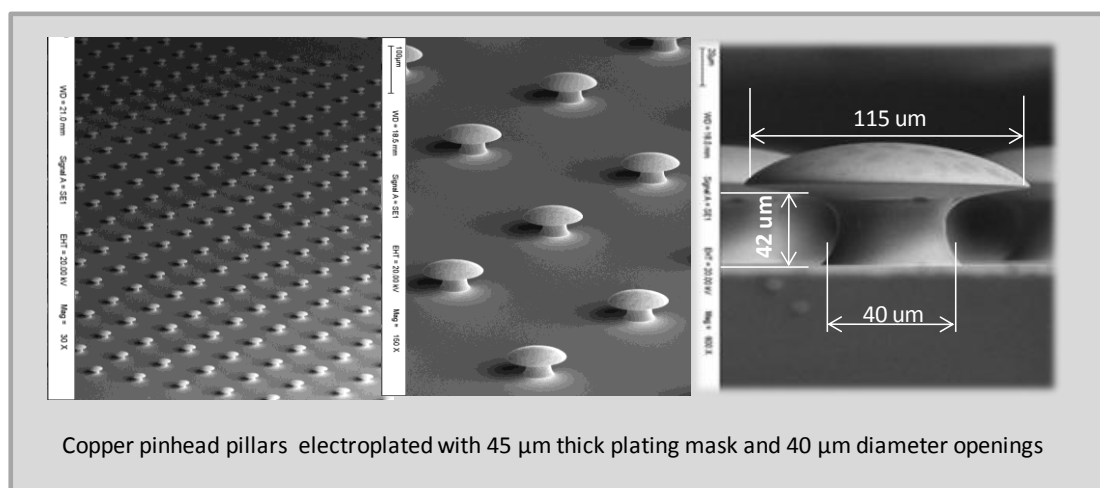


Figure 5.11 CPH pillar bumps from plating trial on 4-inch silicon wafer

5.4.4 Fabrication of CPH pillars with various aspect ratio

Electroplating of CPH pillars with an aspect ratio of up to 2 were investigated. The test chip layout is shown in Figure 5.12. The first batch of test chips was fabricated with a 2-step plating process. The first plating was carried out with a 25 μm patterned plating mask. The second plating step was carried out with a 45 μm plating mask on top of the first plating mask. The process flow is shown in Figure 5.13. The 2-step plating process was necessary as the available UV aligner and developer had limitations in exposing and developing cavities beyond an aspect ratio of 2. The results of the 2-step plated bumps are shown in Figure 5.14 (a). Within 60 minutes, using a 300 mA plating current, CPH pillar bumps with a diameter of 39 μm , overall bump

height of $79\text{ }\mu\text{m}$ and pinhead diameter of $86\text{ }\mu\text{m}$ were produced with about 70% yield. However, there were random non-plated cavities. These defects were most likely due to residues of partially developed photoresist or air entrapment in the plating cavities.

To increase the aspect ratio of the pillar bumps, a 3-step plating process was investigated. Maintaining a 3-stack alignment and proper photoresist exposure was a challenge. The gross misalignment between a pillar stack could be $6 - 8\text{ }\mu\text{m}$ as shown in Figure 5.14 (b). Some of the 3-step plated pillars had very weak plated interfaces between stacks when plated to an average diameter of $40\text{ }\mu\text{m}$ and height of $102\text{ }\mu\text{m}$. This aspect ratio is not attainable with an acceptable yield.

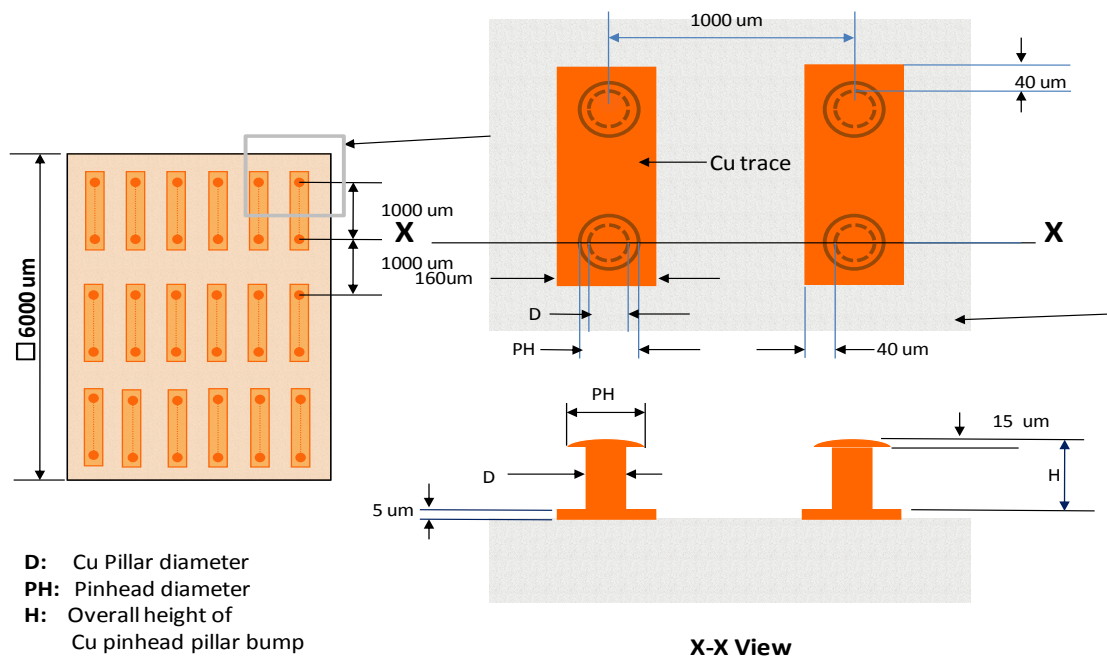


Figure 5.12 36 CPH pillar bumps layout on 6 mm square silicon chip

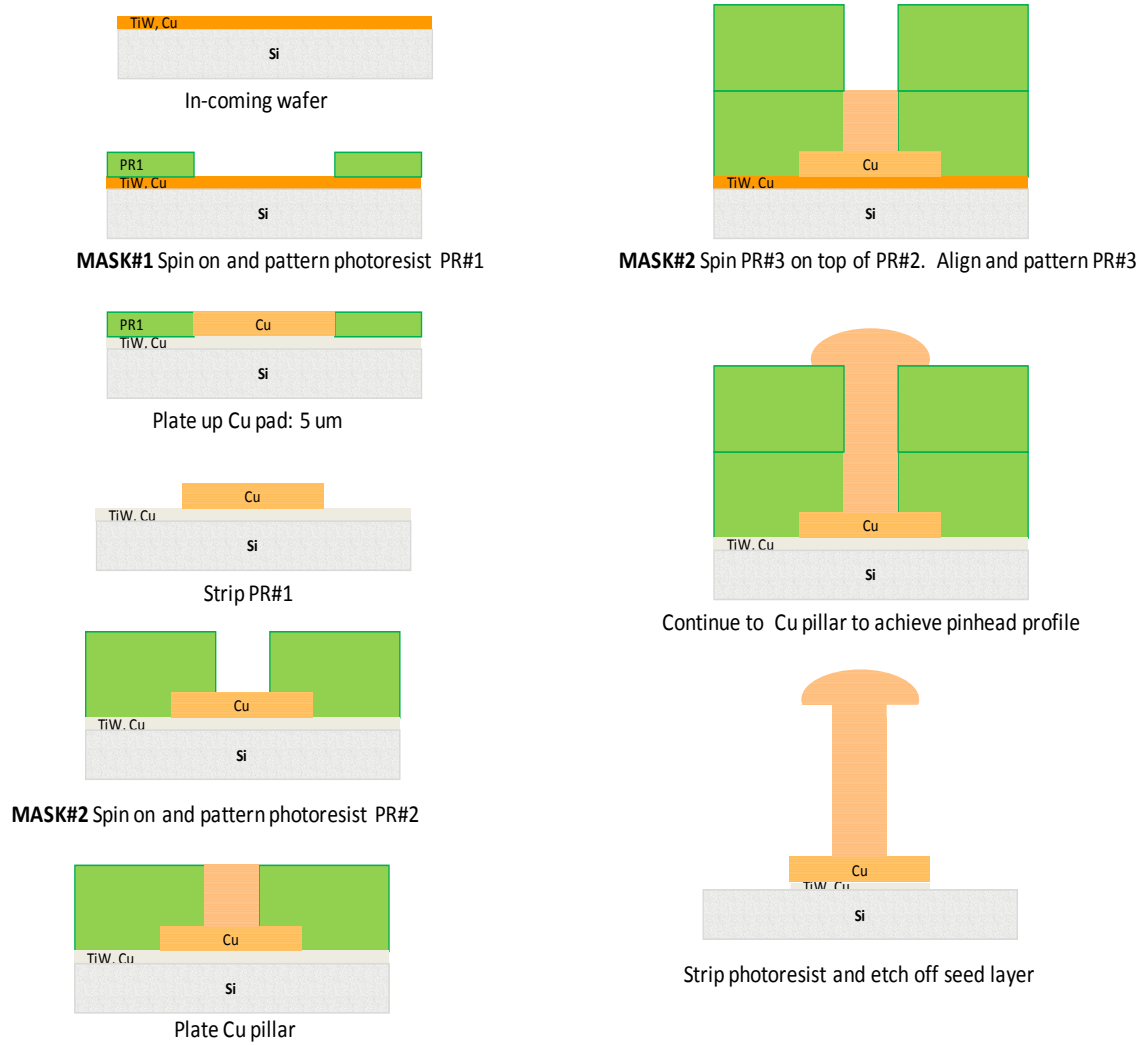


Figure 5.13 Two-step electroplating for high aspect ratio CPH pillar bumps

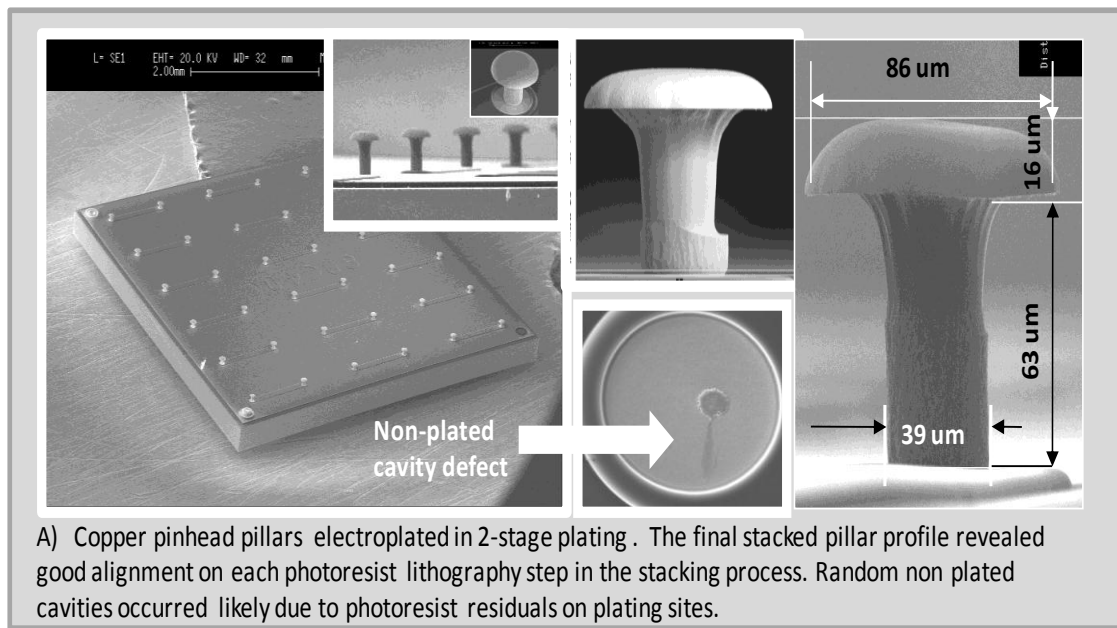


Figure 5.14 (a) 2-step plated CPH pillars with aspect ratio of 2

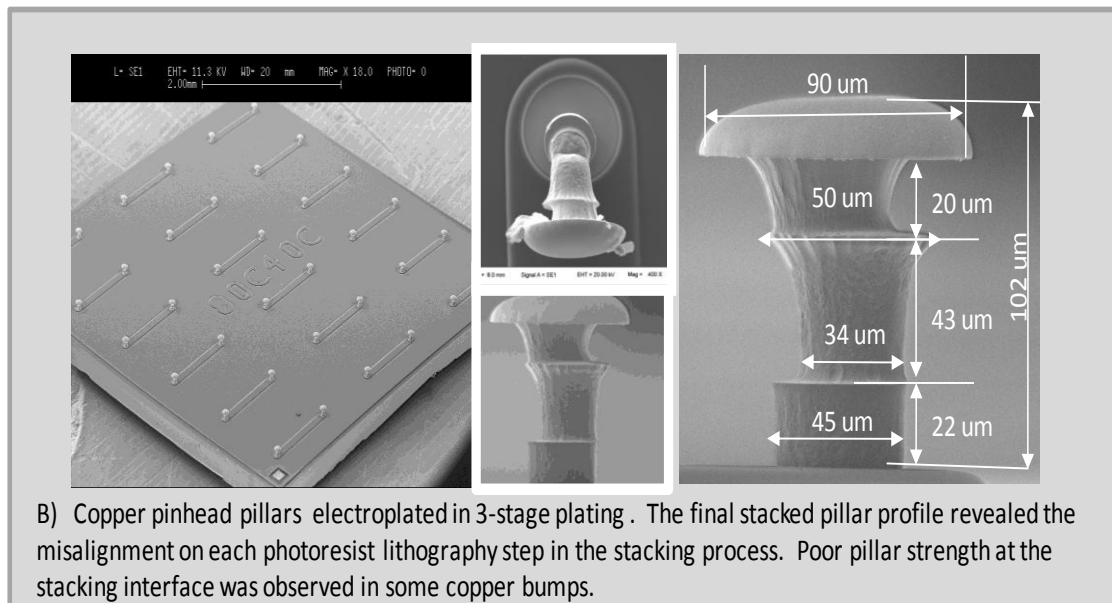


Figure 5.14 (b) 3-step plated CPH pillars with aspect ratio of 2.5

Further process investigations were carried out to fabricate CPH pillars in 80 μm via openings using a multi-step plating process. The initial evaluation was conducted on a 1-step plating process with 45 μm thick photoresist with 80 μm via openings. The photolithography process, from UV exposure to resist development, was more repeatable for 80 μm vias. The plating yield was over 90% and the pillars adhesion to silicon was very firm using a manual twister push test. Figure 5.15 shows the 1-step plated CPH pillars. The CPH pillar structure has a 80 μm diameter pillar with a height of 45 μm and a 110 μm diameter pinhead which is 10 μm thick. The overall CPH pillar height is 55 μm .

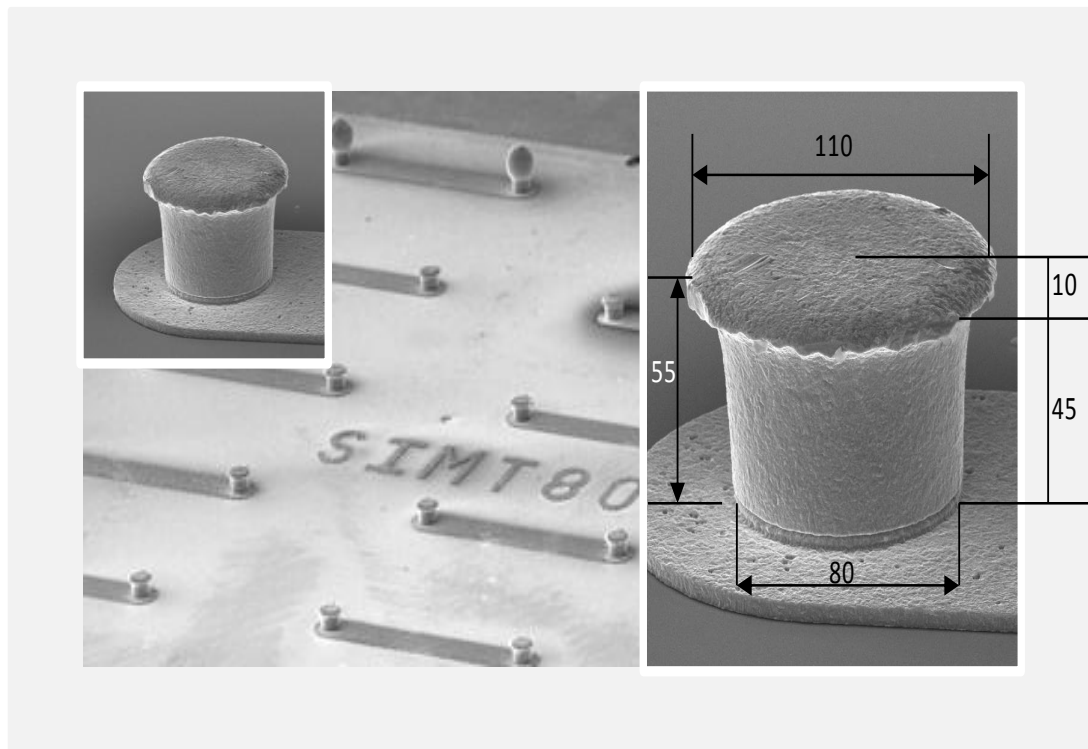


Figure 5.15 CPH pillar structures plated with a 1-step process

Finally, a 4-step plating process was attempted to produce robust and compliant Cu pinhead pillar bumps. CPH pillars with 80 μm diameter and 165 μm in height were fabricated with good repeatability. The detailed structure dimensions are illustrated in Figure 5.16.

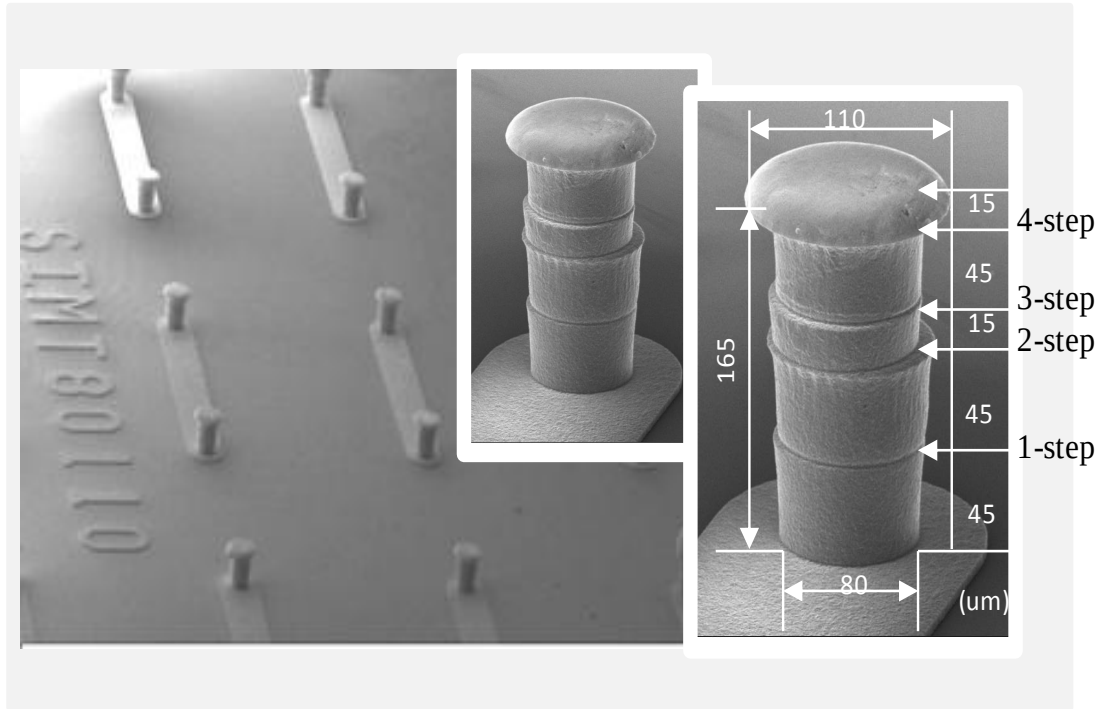


Figure 5.16 CPH pillars: 80 μm pillar diameter, 110 μm pinhead diameter and 165 μm overall height, fabricated with a 4-step plating process.

5.5 Summary

A through-mask plating process is evaluated for CPH pillar bump fabrication. Developing 80 μm diameter vias in 45 μm thick AZ4620 positive photoresist is found to be the limit for the available process setup. A multi-coat photoresist and multi-step plating process is developed to fabricate high aspect ratio CPH pillar structures (pillar height/pillar diameter ≥ 2). The optimized electroplating current is found to be 300 mA. The copper deposition rate is 1.3 $\mu\text{m}/\text{min}$ and the plated copper bump uniformity

across a 4-inch wafer is 5%. Compliant CPH pillar structures of 80 μm pillar diameter, 165 μm overall pillar height and 110 μm pinhead diameter are successfully fabricated with a 4-step plating process.

Chapter 6 Characterization of Annealed and Non-Annealed Copper Pinhead Pillar Bumps

Various studies have reported that electroplated Cu film undergoes microstructural changes in terms of grain growth and texture. In a study on electroplated Cu (Stangl et al, 2005), it was observed that electroplated Cu exhibited changes in microstructure widely known as self-annealing. The microstructure evolution was divided into two periods. The first period of inhibited grain growth showed a diffusion of impurities out of the metallization layer combined with a significant stress relaxation. In the following second period a grain growth evolution formed a coarse grain microstructure within 10 hours of plating. In the subsequent 30 hours, there was significant grain evolution in the as-plated Cu grains which were typically smaller than 100 nm and grew into grains of a few micrometers in size. In a paper on electroplated Cu columns (Liu et al, 2009), it was found that recrystallization could occur during plating and spontaneous post-plating self-annealing was observed. In another study, a 2-step grain growth mechanism (Brongersma et al, 1999) was proposed based on experimental observations made on a focus ion beam (FIB) cross-sectional microstructure of plated Cu. It observed that rapid recrystallization occurred from the top surface just after Cu deposition followed by a slower lateral recrystallization resulting in large grain growth. Recently, a paper (Zhang et al, 2010) reported that self-annealing of electrodeposited Cu stabilized after 96 days. If Cu is subjected to elevated temperature annealing, further recrystallization and grain growth can occur.

In this study, the effect of elevated temperature annealing on the microstructure and mechanical properties of annealed and non-annealed CPH pillars are characterized.

Annealing of the CPH pillars is carried out before the solder bumping process. The aim is to induce recrystallization and grain growth in the CPH pillars in a controlled environment so as to increase the ductility and compliance of the CPH pillars.

6.1. Microstructure characterization of CPH pillars before and after annealing

In the previous chapter, a high aspect ratio CPH pillar fabrication using a multi-step plating process was discussed. It was not known if fault lines or defects existed in the multi-step plating interfaces. In this study, CPH pillars before and after annealing are cross-sectioned and ion-etched for detailed microstructural analysis. It is important to determine if the multi-step plating process creates any defect which can affect Cu pillar compliance and facilitate crack propagation that can lead to early failure. In addition, the effect of elevated temperature annealing on grain growth in CPH pillars was investigated.

An array of thirty-six CPH pillars electroplated on 6 x 6mm silicon chips as shown in Figure 6.1 were prepared as test samples. Non-annealed samples and samples subjected to three different sets of annealing parameters, as listed in Table 6.1, were evaluated. The annealing parameters are chosen to be compatible with the temperature tolerances of most electronics materials used in SAC Pb-free soldering at 250-260°C, Au-Sn soldering at 320-330°C and Cu-Cu bonding at 400°C. The annealing time of 30 minutes is tolerated by most electronics materials used in the respective categories.

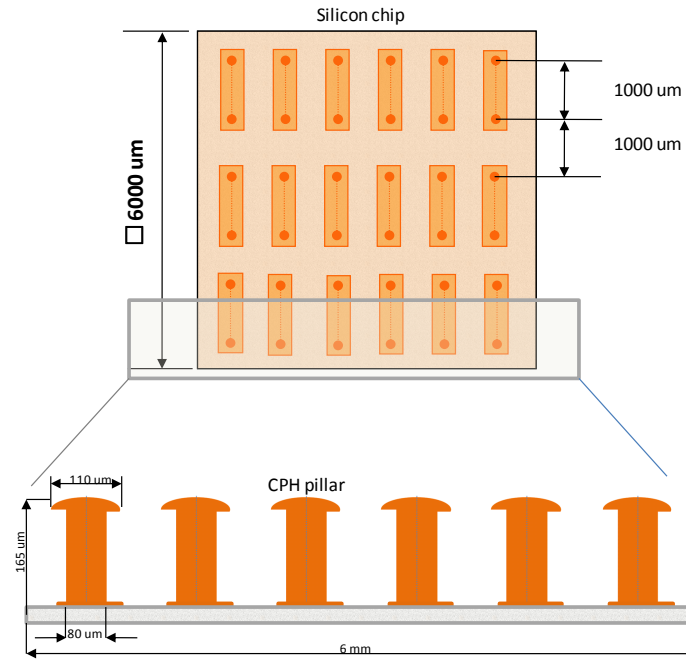


Figure 6.1 6 mm square silicon test chips with an array of 36 CPH pillars

Table 6.1 Cu Pinhead Pillars Annealing Process Parameters

Annealing Temperature & Dwell Time	250° C, 30 mins.	325° C, 30 mins	400° C, 30 mins
Heating Time	30 minutes from ambient to annealing temperature		
Cooling Time	40 minutes from annealing temperature to ambient		
Furnace Environment	Continuous nitrogen gas flow: 10 litres/min during heating and holding; 40 litres/min during cooling.		
Equipment	Horizontal tube furnace (Model 1725-12HT, CM Furnaces Inc)		

6.1.1 Cross-sectional analyses of CPH pillars

As-plated CPH pillar samples and samples annealed as per Table 6.1 parameters were cross-sectioned and etched by a Gatan 682 ion beam etching system to produce defined microstructures as shown in Figure 6.2. The micrograph in Figure 6.2(a) shows a relative smooth surface morphology and some evidence of grain growth in a fine-grained matrix. With thirty minutes annealing at 250°C, grain boundaries and individual grains in contact with adjacent grains become more prominent. A cluster of

finer grains which were originally deposited on the seed layer is perceivable at the base of the pillar. When the CPH pillars were annealed for thirty minutes at 325°C, significant grain growth seems to take place along the entire length of the CPH pillars, with many larger grains packing closer together and grain boundaries meeting at a line or point juncture. The copper microstructure annealed at 400°C, Figure 6.2(d), is similar to that of Figure 6.2(c). This is likely due to the fact that a similar grain growth has occurred between 325-400 °C. The large grains in the microstructure become more stable and grain growth is slowed down.

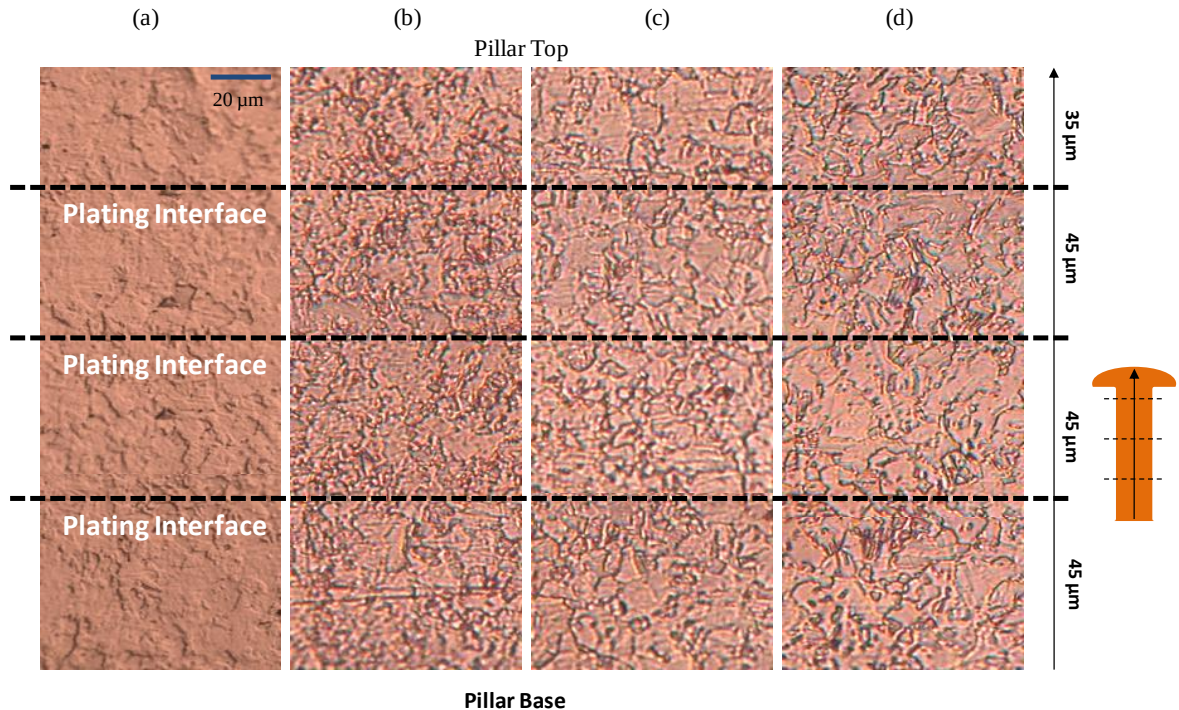


Figure 6.2 Optical micrographs of plated CPH pillars: (a) non-annealed, (b) annealed for 250°C, 30 mins, (c) annealed for 325°C, 30 mins and (d) annealed for 400°C, 30 mins,

Although the CPH pillars were fabricated using a 4-step plating process, no plating interface or fault line was observed in any of the samples. This could be attributed to the self-annealing and recrystallization process that occurred at the plating

interfaces during or after electroplating at room temperature, which eventually homogenized the microstructure of the entire Cu pillar.

The micrographs in Figure 6.3 illustrate the successive changes in microstructure during the annealing process. Annealing twins can be observed in samples annealed for 30 minutes at 325-400°C.

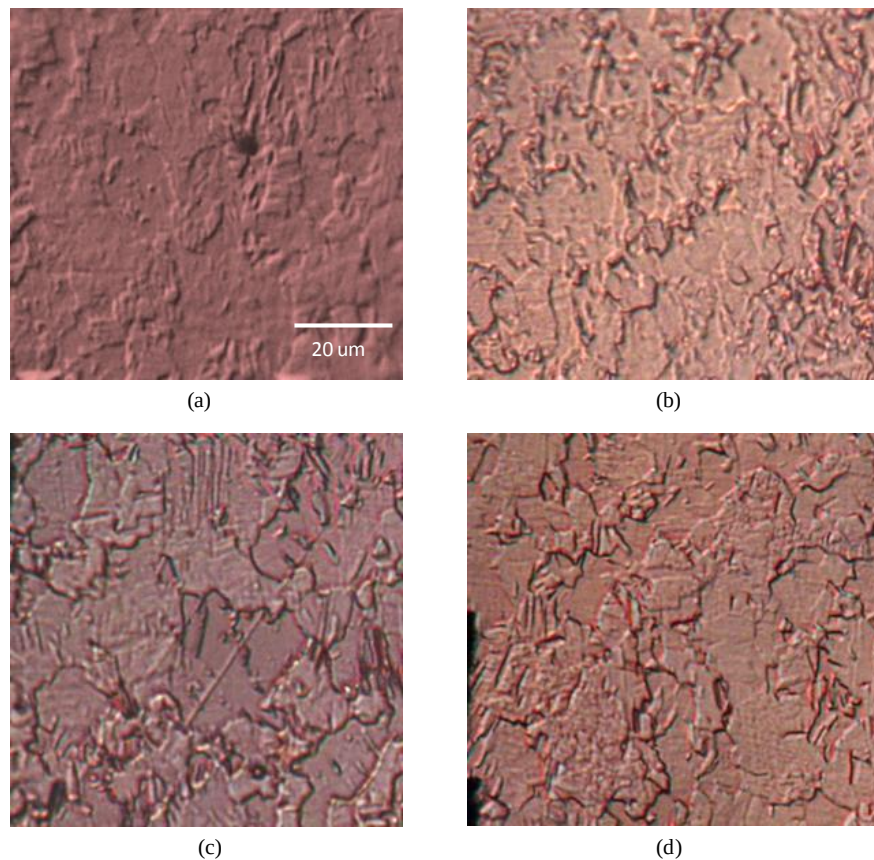


Figure 6.3 Microstructural evolution of electroplated CPH pillars: (a) non-annealed, (b) annealed for 250°C, 30 mins, (c) annealed for 325°C, 30 mins, and (d) annealed for 400°C, 30 mins

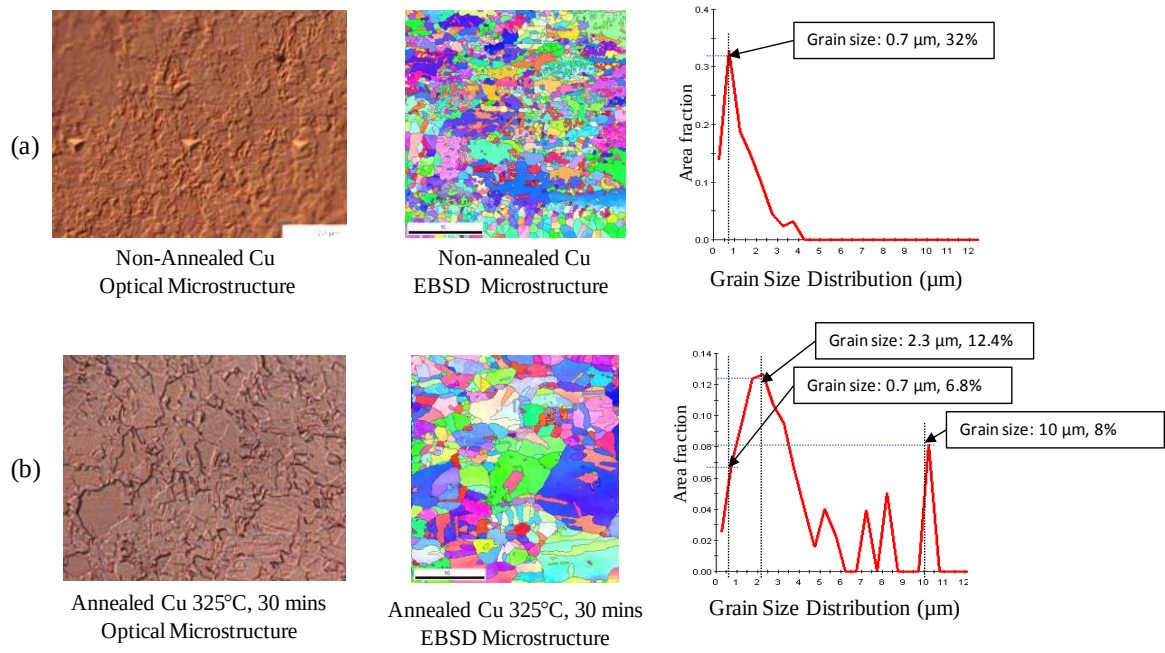


Figure 6.4 Optical and EBSD microstructure characterization of non-annealed and annealed CPH pillar samples

The Cu recrystallization behaviour was characterized using electroplated CPH pillars that were non-annealed and annealed at 325°C for 30 mins. The samples for optical microscopy were cross-sectioned, polished and etched by ion beam. The samples for electron backscatter diffraction (EBSD) were cross-sectioned and an area 30 x 40 μm along the Cu pillar was etched by a focused ion beam (FIB).

The grain growth in the annealed CPH pillar sample in Figure 6.4(b) is obvious when compared with the optical and EBSD images of the non-annealed CPH pillar in Figure 6.4(a). The grain sizes distribution of the CPH pillar samples as observed by EBSD are computed as area fraction over the scanned area. In the non-annealed sample, the area fraction of small grains in the range of 0.7 μm is 32%. After elevated temperature annealing, the area fraction of grain sizes above 2 μm is approximately 12% and large grain above 10 μm is 8%. The area fractions of the annealed microstructures are dominated by grain sizes ranging from 2-10 μm. It is clear from

the optical and EBSD microstructures analyses that the annealing process can drive significant grain growth in electroplated CPH pillars.

6.2. Shear test of Cu pinhead pillars

Shear Test is a well accepted method to evaluate the attachment strength of Cu pillar bump on silicon devices (Lee and Huang, 2002, Wang et al, 2001, Kim et al, 2006, JESD22-B117A, 2006). In this study, the shear strengths of CPH pillars with and without annealing are characterized.

CPH pillars of diameter 80 μm and height 170 μm , electroplated on 160 μm copper traces routed on 6x6 mm silicon test chips, were used in the tests. Three batches of eight test chips, subjected to 250° C, 325° C and 400° C annealing conditions as defined in Table 6.1, and a control batch without annealing were prepared. The shear tests were carried out on a Dage 4000 Shear Tester as shown in Figure 6.5.

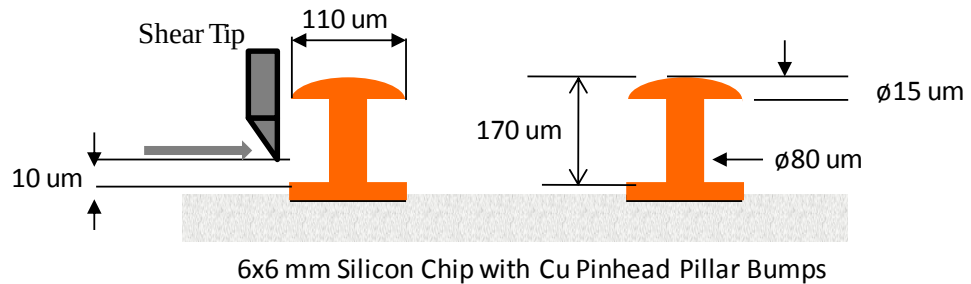


Figure 6.5 Shear Test Setup for CPH Pillar Bumps

6.2.1 Shear test analyses of CPH pillars

The shear test results are shown in Figure 6.6. The shear force decreases as the anneal temperature increases. The shear force reduced by 12.7% after annealing at 400°C for 30 minutes and 5% at 325°C. The shear strength reduction after annealing at 250°C is 2% which is insignificant.

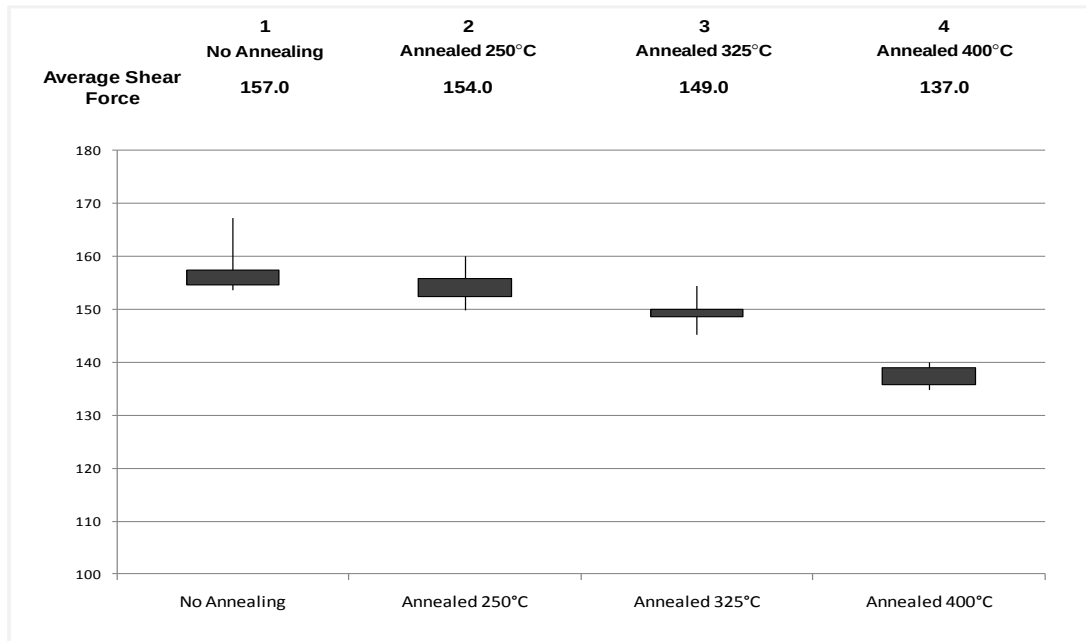


Figure 6.6 Shear Strength of non-annealed and annealed CPH pillars

The fractographs and shear plots in Figure 6.7 show that all the samples have ductile fracture surfaces and some tearing occurred at the edges where pillars were sheared off the pads. A characteristic kink was observed at the initial displacement in each of the Cu pillar shear test. This is because the CPH pillar was bending at the beginning of the shear test in the elastic strain region as the shear tip pushed against it. It is observed in Figure 6.7(a), 40 gf was applied on the non-annealed Cu pillar to attain a deflection of 30 μm before the Cu pillar experienced plastic strain. For the Cu pillar annealed at 250°C, approximately 30 gf was applied to attain a deflection of 20 μm . For the Cu pillars annealed at 325°C and 400°C, approximately 25 gf and 20 gf were required respectively, to attain a deflection of 20 μm . It is observed that the shear forces required for deflecting the annealed CPH pillars elastically decrease as annealing temperatures increase.

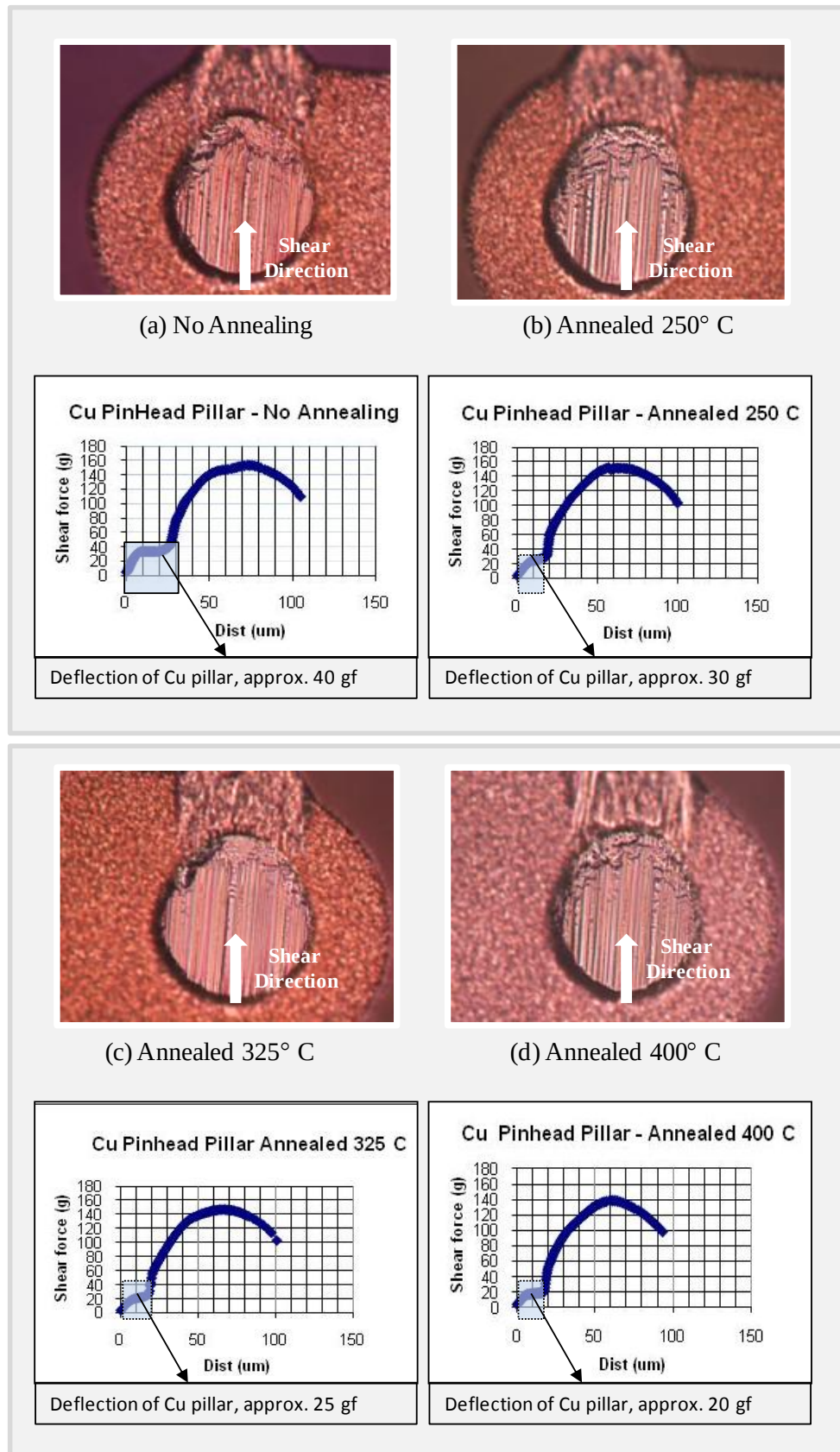


Figure 6.7 Fractographs and shear test plots of non-annealed and annealed CPH pillars

The results indicate that the annealing process, which drives recrystallization and grain growth, increases the ductility of the CPH pillars. Subsequent temperature cycling tests will be carried out to determine if the annealing process on CPH pillars translates to better interconnection compliance and reliability.

6.3. Nanoindentation of Cu pinhead pillars

A nanoindenter can produce material deformation in nanometer depth and in sub-micrometer spatial resolution. By analysing the nanoindentation load-depth curve, the hardness and elastic modulus can be determined (Oliver and Pharr, 1992, Erinc et al, 2004). Nanoindentation is particularly suitable for determining mechanical properties of micro structures like the CPH pillars.

6.3.1 Hardness and elastic modulus measurements of CPH Pillars

Nanoindentation on CPH pillars was conducted on a NanoTest from MicroMaterials. The indenter is a Berkovich diamond tip, with a nominal radius of 150nm. The diamond indenter area function can be approximated to $A = 20.68 h_c^2 + 2617.43 h_c$ (ISO 14577, 2002). Nanoindentations for CPH pillars were carried out under displacement control, with a 60-second dwell at maximum load to minimize the creep effect. The loading and unloading rate was maintained at 0.3mN/s. In this study, a 400 nm indentation depth was used. The Young's modulus (E) and hardness (H) values for a given indentation were established from the average value over a specimen depth where E and H were independent of depth, which is typically 200 – 500 nm into the specimen (Deng et al, 2004).

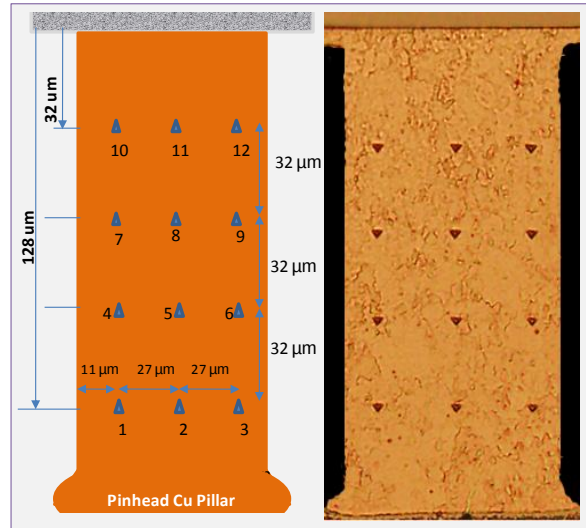


Figure 6.8 Nanoindentation locations on each CPH pillar tested

A typical maximum load-dwell curve and load-displacement nanoindentation curve of the CPH pillar are shown in Figure 6.9.

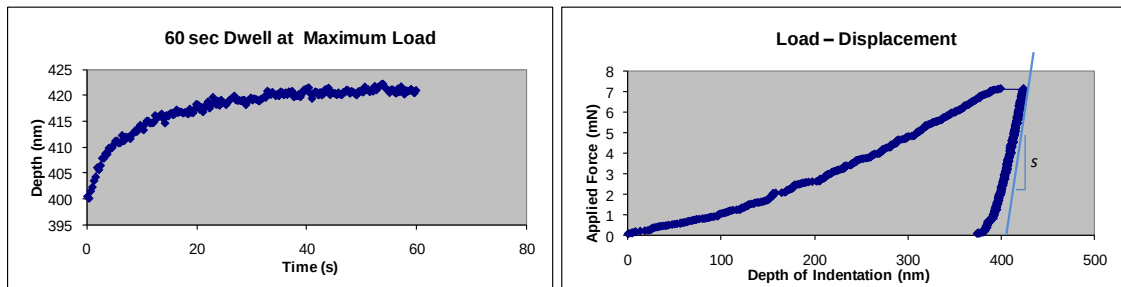


Figure 6.9 Typical maximum load-dwell and load-displacement curves obtained from the CPH pillar nanoindentation tests

The Young's modulus, E , of CPH pillar can be determined from the initial slope, S , of the unloading curve (King, 1987), which is the stiffness of the CPH pillar using the relation given by Equations (6.1) and (6.2):

$$S = \beta \frac{2}{\sqrt{\pi}} E_r \sqrt{A} \quad (6.1)$$

$$\frac{1}{E_r} = \frac{1-\nu_i^2}{E_i} + \frac{1-\nu^2}{E} \quad (6.2)$$

Here, β is a numerical factor relating to the geometry of the indenter, E_r is the reduced modulus, A is the projected contact area of the indentation, E_i and ν_i are the elastic modulus and Poisson's ratio of the indenter. In this study, E_i was taken to be 1141 GPa, ν_i to be 0.07 (ISO 14577, 2002) and ν to be 0.34 for electroplated copper.

For non-annealed CPH pillars, a series of twelve indentations across the whole pillar were made, see Figure 6.8. This was carried on three CPH pillars in order to map the values of H and E along the length of the pillar. The results are shown in Figures 6.10 and 6.11. Bulk copper H is commonly reported as 1.0-1.2 GPa and E as 110-128 GPa. The overall average of H and E measured across the length of the CPH pillars are 1.64 GPa and 115.6 GPa respectively. There is a deviation of 3% in H and 6% in E values along the length of the pillars which can be attributed to microstructural variation of the plated copper. The data variation is not significant and this indicates that the material properties along the length of the pillars are quite homogeneous. The H and E values established in this study correlate well with a related paper that reported on the mechanical properties of Cu pillars fabricated by pulse plating with increasing current density (Dixit et al, 2007). In Dixit's study, the H values were found to be highest at the base of the pillar and lowest at the top. The H values were reported to range from 1.6 GPa at the top to 2.4 GPa at the bottom of the Cu pillar. The lower H at the top is likely due to the large grains produced by a larger plating current. In the current work, relatively uniform H and E were maintained across the pillar length. A constant DC current used in the multi-step CPH pillar plating process has resulted in a more homogeneous microstructure.

Subsequently, three sets of annealed CPH pillar samples and one set of non-annealed pillars were prepared for nanoindentation. Nanoindentation was carried out on five equally spaced points on two pillars per sample as shown in Figure 6.12. The

results of the E and H measurements are given in Table 6.2. It is found that the H and E of the CPH pillars decreased by 9% and 24% respectively, after annealing at 250°C for thirty minutes. The CPH pillars annealed at 325°C and 400°C for thirty minutes show a 15 – 16% reduction in hardness. In comparison with the CPH pillar annealed at 250°C, there is only a further 6-8% decrease in H and E of the CPH pillar when the annealing temperatures were increased to 325°C and 400°C.

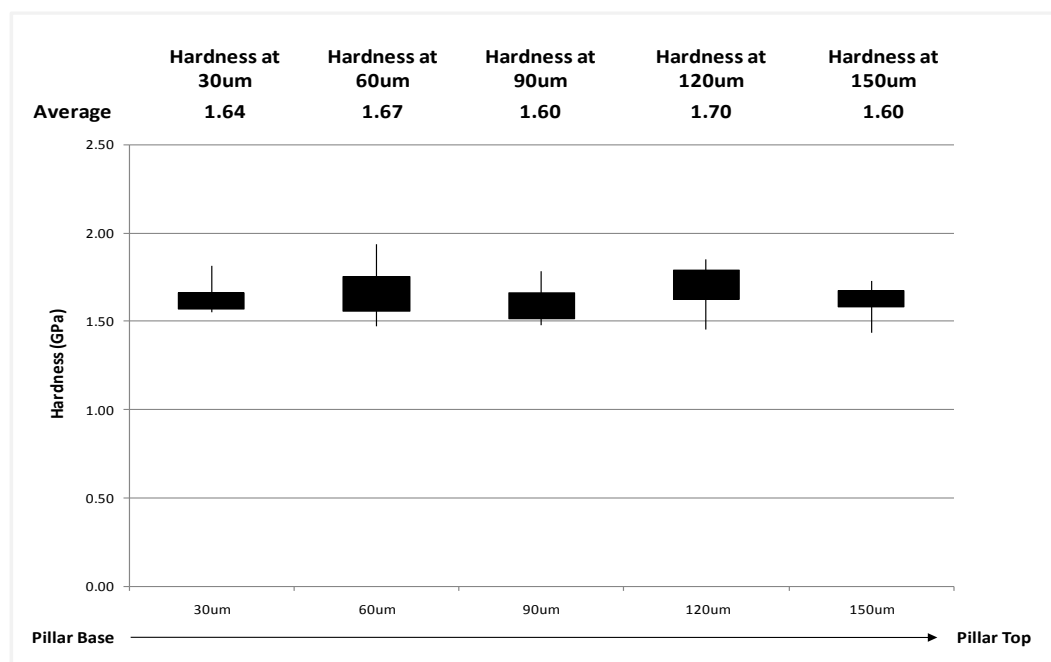


Figure 6.10 Hardness measurements of non-annealed CPH pillars

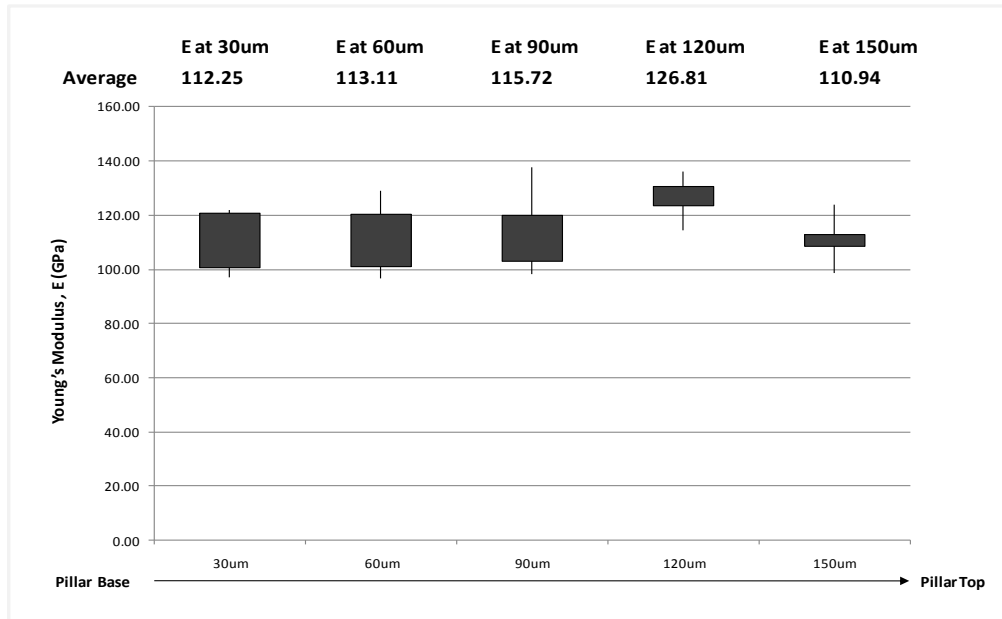


Figure 6.11 Young's modulus measurements of non-annealed CPH pillars

A reduction in the elastic modulus of the CPH pillar after annealing indicates that the tendency for plastic deformation has increased. Hardness measurement is more qualitative and often correlated to the tensile strength of the material. A reducing trend in hardness and elastic modulus is evident that ductility of CPH pillars has increased after annealing at elevated temperature. This correlates with the grain growth observed in the annealed CPH pillar microstructures shown in Figures 6.2-6.4. Larger grain sizes in the microstructure can accommodate larger dislocation movements and hence become more ductile and compliant.

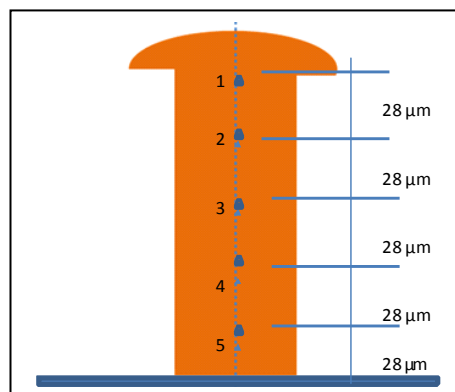


Figure 6.12 Nanoindentation locations on each CPH pillar

Table 6.1 Young's modulus and hardness results of non-annealed and annealed CPH pillar bumps (average of 10 measurements per sample)

Sample Measurement	Non- Annealed	Annealed 250° C 30 mins.	Annealed 325° C 30 mins.	Annealed 400° C 30 mins.
Young's Modulus (GPa)	115.77	88.27	90.53	83.51
Hardness (GPa)	1.64	1.49	1.40	1.37

6.4. X-ray Diffraction Characterization (XRD) of CPH Pillars

Studies have shown that crystal orientation and texture in electrodeposited Cu microstructure have a significant influence on its mechanical and electrical properties (Ryu et al, 1999, Chong et al, 2005) and the texture component (111) is recognized as one which increases electrical conductivity and electromigration resistance (Mane et al, 2005). It is of interest in this study to characterize the crystallographic texture and investigate the effect of elevated temperature annealing on crystal orientation of electroplated CPH pillars. Electroplated CPH pillars as shown in Figure 6.1 were prepared for XRD analysis. Annealed samples were prepared according to Table 6.1 heating parameters. The XRD experiments were performed on a Bruker D8 X-ray diffractometer at 40 kV, 40mA, with a beam size of 0.1mm. The scan range was from 30° to 150°, with a step size of 0.02°.

6.4.1 Crystallographic analyses of CPH pillars before and after annealing

The diffraction patterns of non-annealed and annealed CPH pillars are shown in Figure 6.13. The four main diffraction peaks for all the CPH pillar samples were found at $2\theta = 43.3^\circ$, Cu (111); 50.4° , Cu (200); 74.1° , Cu (220) and 89.9° , Cu (311). Table 6.3 gives a summary of the XRD diffraction peaks and intensities, and relative peak intensities (RPI) data obtained from the samples. The preferred crystal orientations or

textures of the CPH pillars can be determined by analysing the texture coefficients, $T_{(hkl)}$ (Dixit et al, 2007), as defined in Equation (6.3). The highest $T_{(hkl)}$ corresponds to the most dominant preferred orientation of the sample. $T_{(hkl)}$ can be calculated by comparing the relative peak intensities of the CPH pillars with the relative peak intensities of the standard polycrystalline copper powder sample (JCPDS 04-0836).

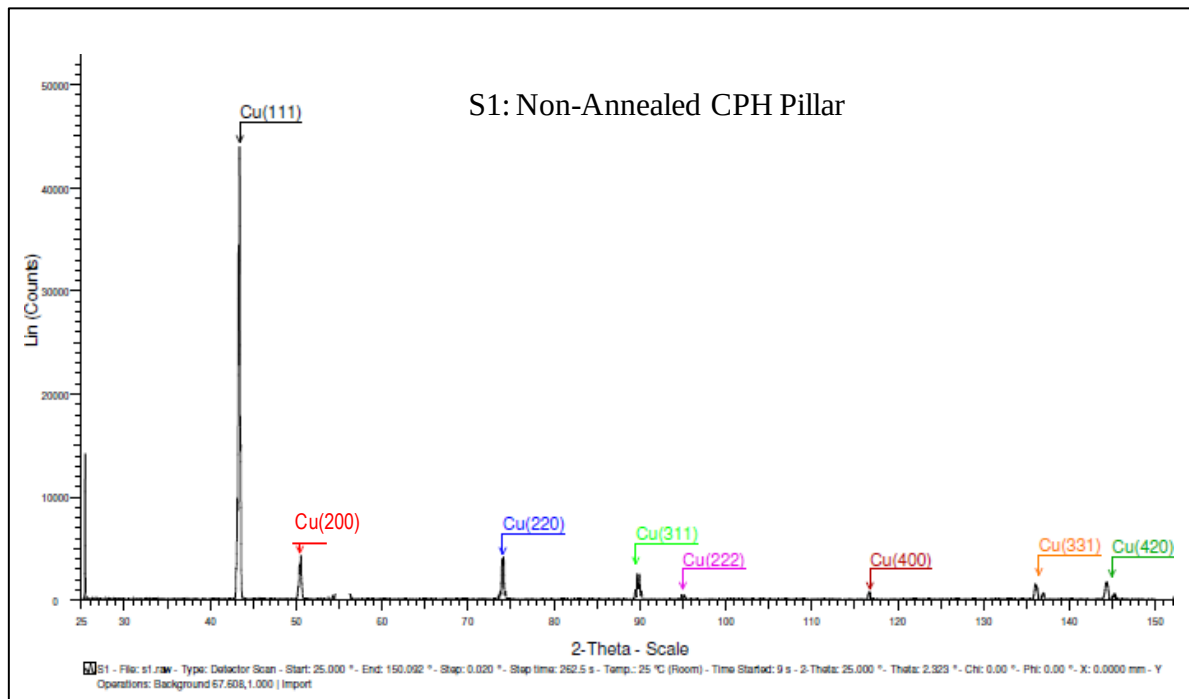


Figure 6.13 (a) XRD profile of non-annealed CPH pillar

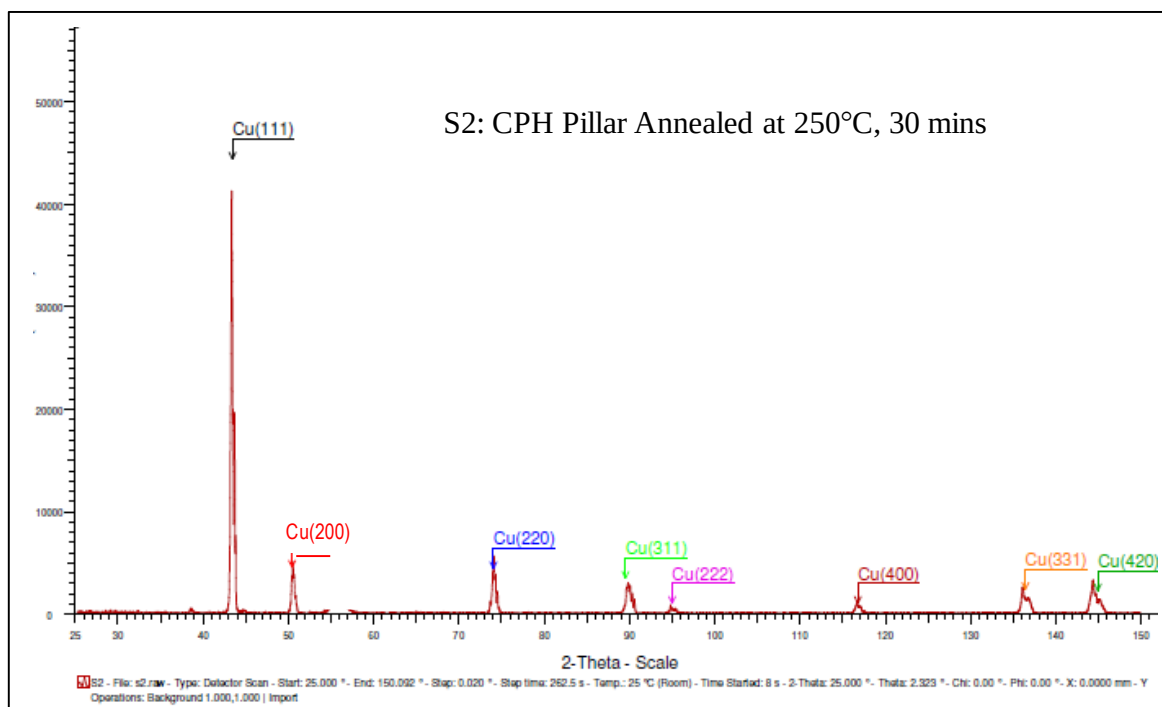


Figure 6.13(b) XRD profile of CPH pillar annealed at 250°C, 30 minutes

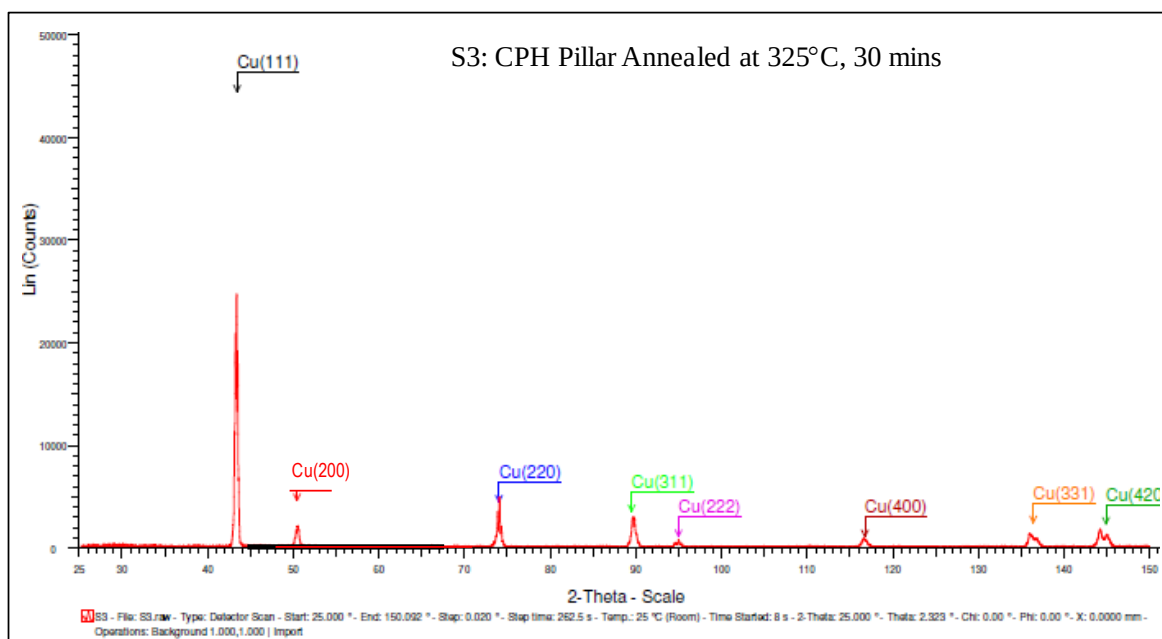


Figure 6.13(c) XRD profile of CPH pillar annealed at 325°C, 30 minutes

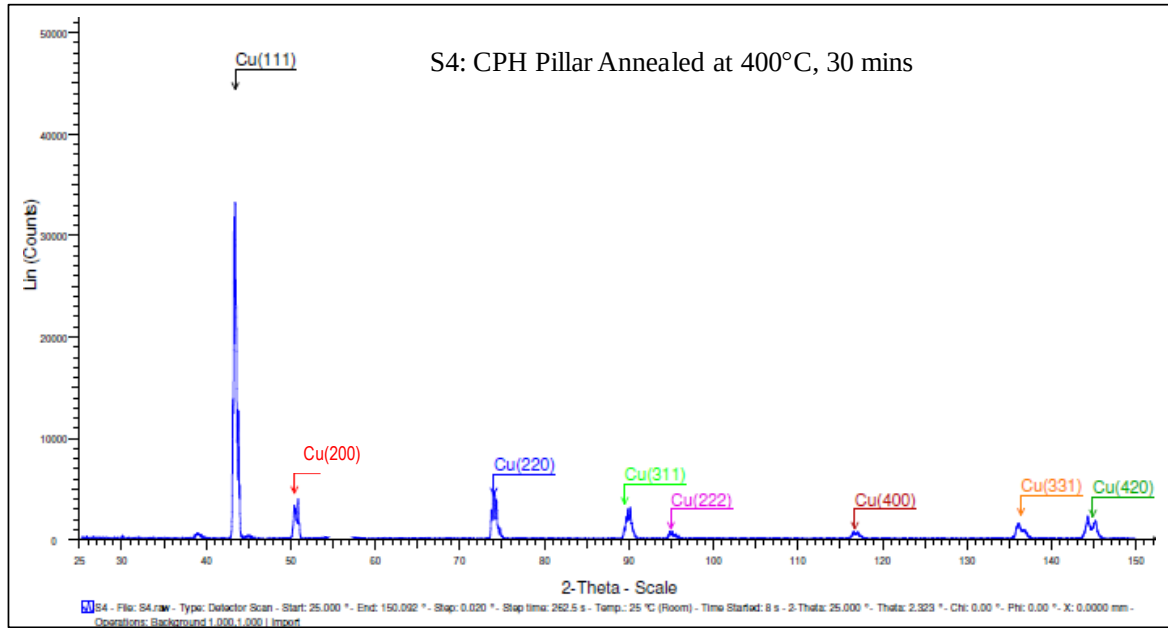


Figure 6.13(d) XRD profile of CPH pillar annealed at 400°C, 30 minutes

Table 6.3 XRD data of CPH pillars obtained from scan 30-150°

Angle 2θ	Crystal Plane	S1: Non-annealed		S2: Annealed at 250°C, 30 mins		S3: Annealed at 325°C, 30 mins		S4: Annealed at 400°C, 30 mins		Standard Data. JCPDS 04-0836
		Intensity	RPI	Intensity	RPI	Intensity	RPI	Intensity	RPI	
43.30	111	44198	100%	40601	100%	24118	100%	32560	100%	100%
50.43	200	4254	10%	4468	11%	1698	7%	3358	10%	46%
74.13	220	4254	10%	4818	12%	4416	18%	4497	14%	20%
89.93	311	2595	6%	1927	5%	2335	10%	2219	7%	17%
95.14	222	505	1%	613	2%	510	2%	420	1%	5%
116.92	400	793	2%	526	1%	467	2%	300	1%	3%
136.51	331	1514	3%	1664	4%	679	3%	899	3%	9%
144.72	420	1802	4%	2278	6%	1019	4%	1319	4%	8%

In this study, the texture coefficients of the four predominant ($h k l$) peaks observed in the x-ray diffraction spectra were calculated. The $T_{(hkl)}$ of each reflection ($h k l$) is defined by Equation (6.3):

$$T_{(hkl)} = \frac{I_{(hkl)}}{I_0(hkl)} \left[\frac{1}{n} \sum \frac{I_{(hkl)}}{I_0(hkl)} \right]^{-1} \quad (6.3)$$

Table 6.4 Coefficients of texture of non-annealed and annealed CPH pillars

Crystal Orientation	Coefficient of Texture, $T_{(hkl)}$			
	S1: Non-annealed	S2: Annealed at 250°C, 30 mins	S3: Annealed at 325°C, 30 mins	S4: Annealed at 400°C, 30 mins
(111)	1.96	1.89	1.52	1.73
(200)	0.41	0.45	0.23	0.39
(220)	0.95	1.12	1.39	1.19
(311)	0.68	0.53	0.86	0.69

The value of $I_{(hkl)}$ is the measured relative peak intensity of $(h\ k\ l)$ reflection, $I_{0(hkl)}$ is the relative peak intensity of a standard powder of copper sample, n is the number of reflections used in the calculation. The results of the $T_{(hkl)}$ calculation are shown in Table 6.4 and plotted in Figure 6.14. It can be seen that the texture of all the CPH pillar samples is dominated by [111] orientation which corresponds to the highest $T_{(hkl)}$ value. The second most dominant orientation is [220]. When CPH pillars were annealed, the strength of $T_{(hkl)}$ changed with the evolution of crystal orientation. It was observed that there was a decrease in the [111] preferred orientation and a sustained increase in the [220] orientation over 250 – 325 °C temperature range. However, [111] remained as the most preferred orientation for the crystals in the CPH pillars. Thus, (111) should be the crystallographic plane with the lowest energy. As (111) is the slip plane of a copper face-centred cubic (FCC) structure (Chong et al, 2005), having (111) planes aligned on the length of the CPH pillar will enhance its yield strength. It is also known that (111) textured microstructure suppresses grain boundary and interfacial diffusion of metal atoms and improves the electromigration lifetime significantly (Ryu et al, 1999).

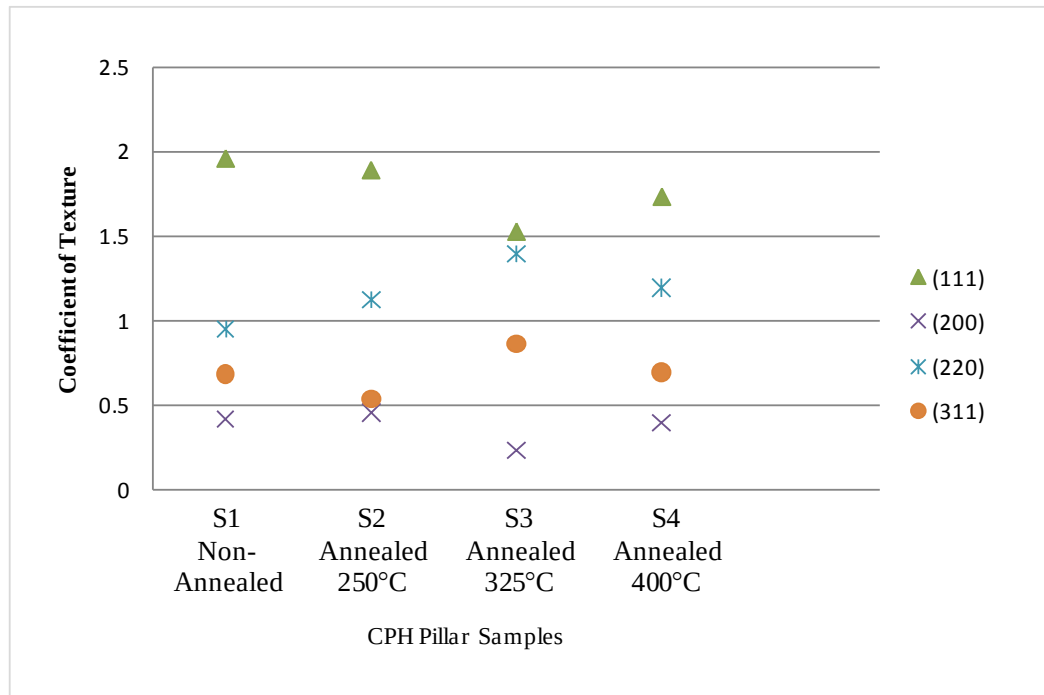


Figure 6.14 Texture coefficients of non-annealed and annealed CPH pillars

6.5. Summary

A detailed characterization study is conducted to establish the shear strength, ductility, hardness, elastic modulus, crystal orientation and texture of non-annealed and annealed CPH pillars. The cross-sectioned samples were polished and ion-etched to enhance the surface resolution of the microstructures.

The shear test results of the CPH pillars annealed in elevated temperatures show a decreasing trend in shear strength. There is a decrease of 5-13% in shear strength when CPH pillars were annealed at 325 - 400°C for 30 minutes, and there is no significant change in CPH pillars annealed at 250°C. All the sheared samples have ductile fracture surfaces.

Microstructural evolution and grain growth are observed when CPH pillars were annealed at elevated temperatures. The microstructural analyses on CPH pillars did not reveal any plating fault lines or defects at the plating interfaces. This verifies

that the multi-step plating process is capable of fabricating high aspect ratio CPH pillars.

Nanoindentation tests indicate that multi-step plated CPH pillars have homogeneous hardness and elastic modulus and this could be attributed to the constant plating current applied throughout the plating process. There is a reduction of 9-16% in hardness and 24-28% in elastic modulus when CPH pillars were annealed at elevated temperatures. This indicates that the compliance of a CPH pillar can be increased by heat treatment.

XRD indicates that the most preferred crystallographic orientation in CPH pillars is [111] and it is observed that the texture is not altered by the elevated temperature annealing process. As the [111] texture in Cu has good resistance to electromigration and stress migration, the reliability of CPH pillars is enhanced.

CHAPTER 7 Reliability Assessment of Copper Pinhead Pillar Bump and Flip-Chip Solder Bump Assemblies

In this chapter, the solder joint reliability of non-annealed and annealed CPH pillar solder joints, as well as conventional flip-chip solder joints were evaluated. The CPH pillar and flip-chip solder joint reliability performances in rapid temperature cycling (RTC), accelerated temperature cycling (ATC) and electromigration tests were assessed. Post-test failure distributions and mechanisms of failures were discussed.

The preliminary reliability evaluation was carried out using CPH-40 chips which have a pillar height of 75 μm , pillar diameter of 40 μm and pinhead diameter of 80 μm . The results did not meet the reliability expectation. Hence, the CPH pillar structure is improved for subsequent reliability evaluation using CPH-80 chips which have a pillar height of 165 μm , pillar diameter of 80 μm and pinhead diameter of 110 μm .

7.1. Rapid temperature cycling (RTC) test

RTC is introduced to enable various CPH pillar designs fabricated by different processes to be evaluated within a short time frame. The RTC reliability results provide some benchmarks for the new interconnects development and are useful indicators for process optimization. The RTC tests in this study were conducted using a thermal electric (TE) module which could heat up and cool down the devices-under-test rapidly. The TE module operates as a solid state heat pump based on the Peltier effect (Rittner, 1959, Riffat et al, 2003) which causes a temperature differential when DC current is applied across a pair of P-N junction. Heat is absorbed at one junction and

discharged at the other when electric current flows through the system. With this setup, rapid ramp rate and short dwell time at the upper and lower temperature limits can be achieved. A 0 – 100 °C cycle can be run within 2 minutes and 720 cycles could be completed in a day versus 24 cycles by a regular temperature cycling chamber. Devices with a small thermal mass are well suited for RTC, as there is minimal latency in the entire package to be heated or cooled rapidly. However, it is noted that due to a much higher frequency of cycling in the RTC test, the solder joint will experience higher stress and less creep within the short dwell time. Hence, RTC results will differ from the traditional accelerated temperature cycling test results. Nonetheless, it is an effective and fast screening method to compare the performance of different interconnects structures, especially at the conceptual stage.

7.1.1. RTC experimental procedure

A preliminary RTC screening was conducted to establish a baseline reliability performance for conventional flip-chip and CPH pillar bump assemblies. The test vehicle was comprised of a 6x6 mm silicon chip with a 36 bump array layout and a matching daisy-chain FR4 PCB as shown in Figures 7.1(a) and (b). The pad metallization on the FR4 was copper with electroless nickel-gold finish (ENIG) and all the test chips had electroplate nickel and gold UBM. The configuration of the bumped test chips are shown in Figure 7.1(c). All the assemblies were without underfill.

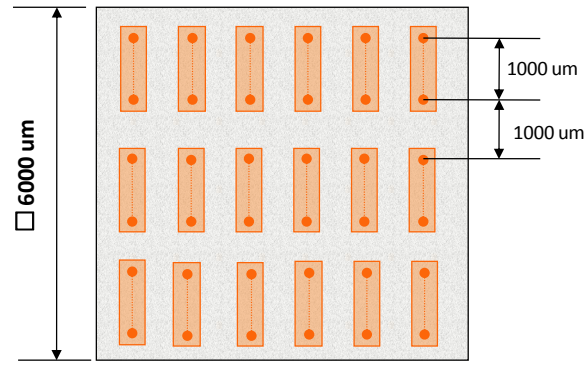


Figure 7.1 (a) 6x6 mm silicon chip for conventional flip-chip and CPH pillar bump assembly

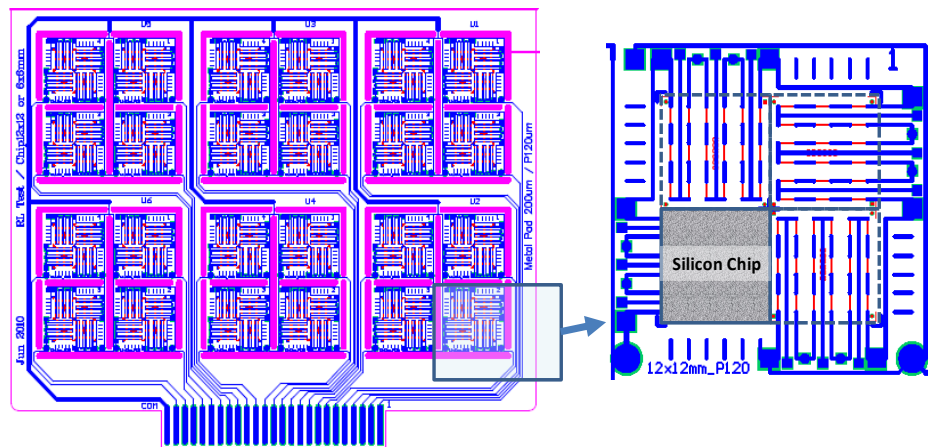


Figure 7.1(b) Daisy-chain FR4 PCB for CPH pillar & Flip-chip solder bump assembly

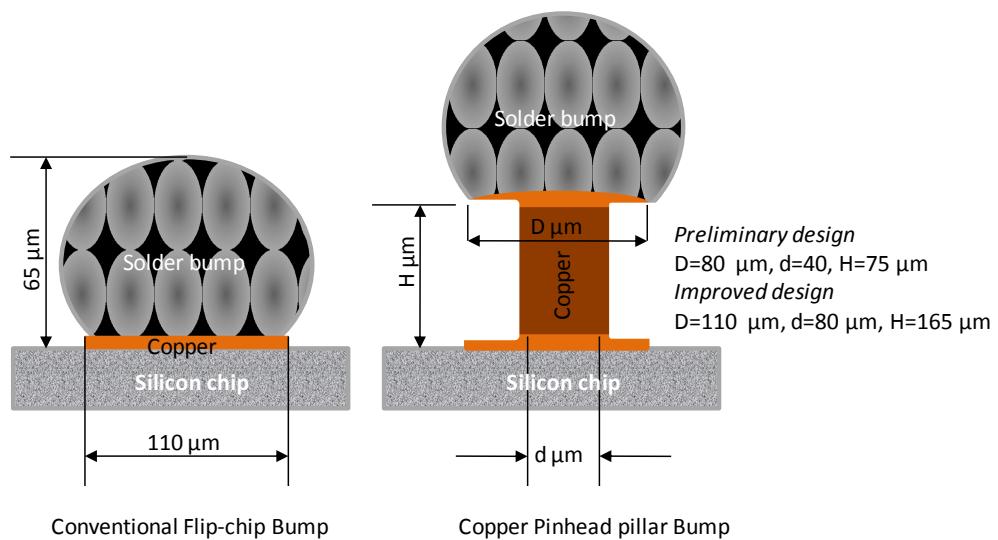


Figure 7.1(c) Configuration of bumped test chips used in preliminary RTC screening

The RTC setup is illustrated in Figure 7.2. The device-under-test (DUT) was placed on top of the thermal electric (TE) module which provided the rapid heating and cooling cycles. A layer of thermal grease was applied between the substrate and Al_2O_3 plate of the TE module to ensure a good thermal transfer during RTC testing. A full-open circuit was used as the failure criterion and monitoring was carried out with a HP 34970A data acquisition unit. The details of the test chips are shown in Table 7.1 and RTC profile is shown in Figure 7.3.

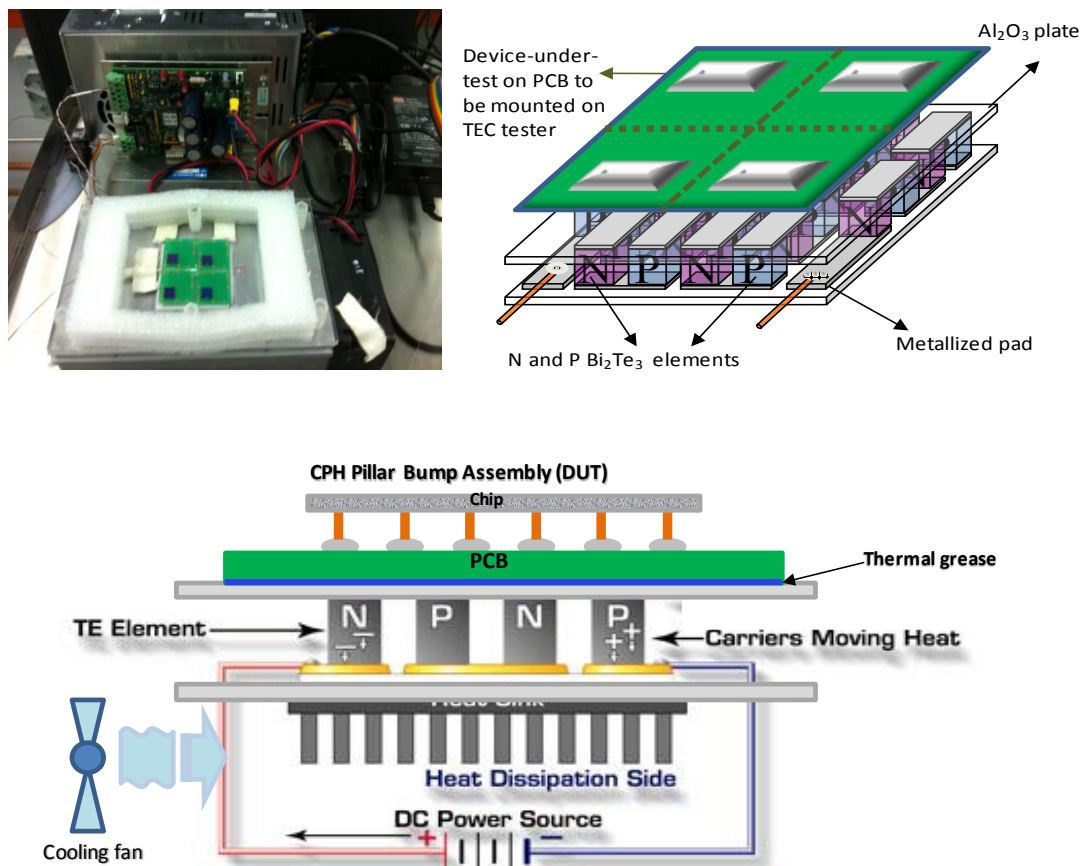


Figure 7.2 Thermal electric module rapid temperature cycling testing for CPH pillar bump and flip-chip solder bump assemblies

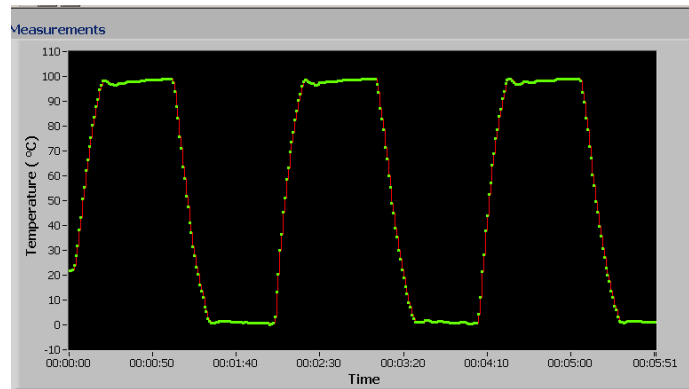


Figure 7.3 RTC temperature profile: 0 – 100°C, 6.7°/sec ramp-up and 45 sec dwell 100°C, and 5°/sec ramp-down and 40 sec dwell at 0°C

7.1.2. RTC test sample preparation

In the preliminary evaluation, a small sample of three test chips in each category was prepared for rapid screening using RTC test. The results provided key information for process and pillar structure improvement at the early stage of the development.

Table 7.1 Types of test chips assembled for RTC benchmarking evaluation

S/N	Type of Test Chip	Sample Size
1	FC-B10: flip-chip with 110 μm diameter soldering pads, 100 μm diameter SAC bumps	3
2	FC-B12: flip-chip with 110 μm diameter soldering pads, 120 μm diameter SAC bumps	3
3	CPH-40-B10: CPH pillars, 75 μm height, 40 μm pillar diameter, 80 μm pinhead diameter, with 100 μm diameter SAC bumps	3
4	CPH-40-B12: CPH pillars, 75 μm height, 40 μm pillar diameter, 80 μm pinhead diameter, with 120 μm diameter SAC bumps	3

7.1.3. RTC preliminary screening results

A summary of the RTC screening test results is given in Table 7.2. The results reveal that FC-B12 solder joints survived the longest, followed by FC-B10. The

reliability of CPH-40-B12 and –B10 are significantly worse, compared to FC-B12 and FC–B10.

Table 7.2 RTC Screening Test Results

S/N	Types of Test Chips	RTC Life (No. Of Cycles)			Average RTC Life (No. Of Cycles)
1	FC-B10	224	258	298	260
2	FC-B12	357	410	249	339
3	CPH-40-B10	92	142	76	103
4	CPH-40-B12	102	149	113	121

All the failures of the FC test chips occur on the substrate side, with cracks propagating through the bulk solder materials near the IMC region as shown in Figure 7.4(a). The cross-sectional failure analyses reveal that the failures of the CPH-40 joints are all at the copper pillar structures. The failures were traced to the copper plating interfaces. These CPH pillars were plated in two steps. In the fabrication process, it was difficult to ensure a completely clean photoresist 40 μm via openings for step-plating of the CPH pillars. It is deduced that this has caused poor surface adhesion on the copper pillars, particularly at the plating interfaces. Crack propagations in the CPH pillar plating interfaces can be seen in Figure 7.4(b).

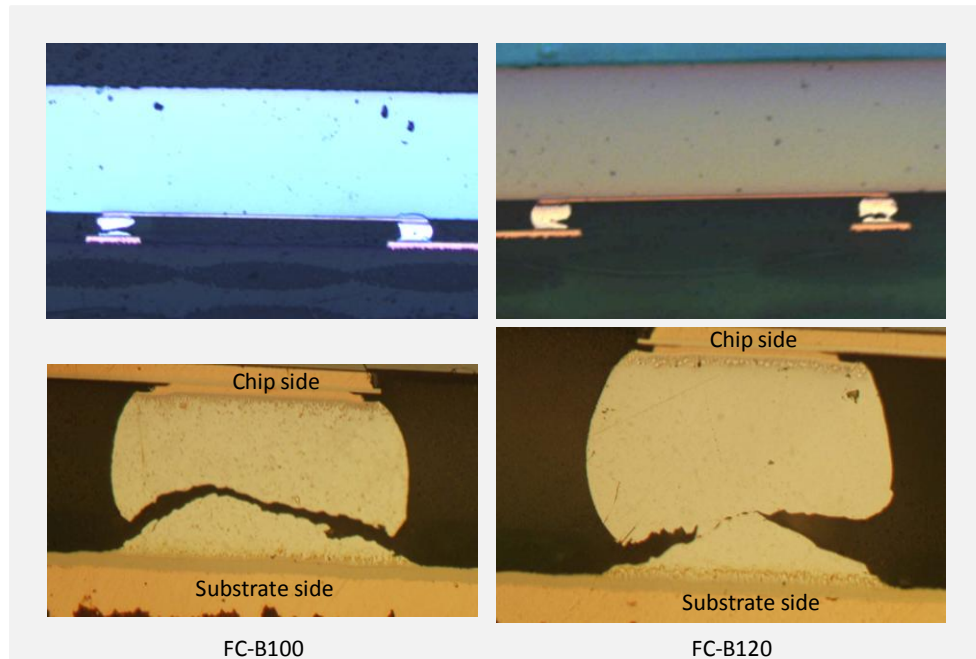


Figure 7.4 (a) FC-B10 and FC-B12 solder joint cracking through the bulk solder near the substrate

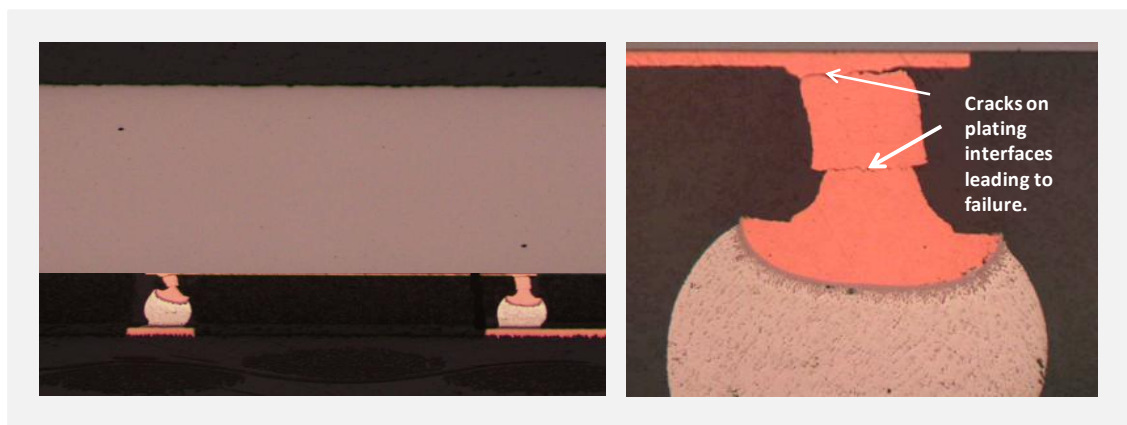


Figure 7.4(b) CPH-40 interconnect failures occurred at the plating interfaces of the copper columns instead of the solder material

7.1.4. Improved CPH pillar structure

The preliminary evaluation reveals that the photolithography process is not consistent in producing 40 μm via openings with a 25 μm thick photoresist. After further process trials (the fabrication process is presented in chapter 5 of this report) consistent yield is established with 80 μm via openings on 25 – 50 μm thick AZ4620

photoresist. Hence, the diameter of CPH pillars of the test chips was increased to 80 μm to ensure complete development and clean removal of photoresist before copper electroplating. Based on the FEA results, the overall height of the CPH pillars has to be increased to 160 μm or more to provide sufficient compliance to the interconnect structure. To fabricate the tall pillar structures, a 4-step plating process was used to attain an acceptable yield and plating quality. The electroplating started at step “1” finished at step “4”, with over-plating at the top to form a pinhead of diameter 110 μm . The overall height of the CPH pillar is 165 μm and the diameter of the pillar is 80 μm . The 4-step CPH pillar with an attached SAC solder bump is shown in Figure 7.5.

To further improve the compliance of the CPH pillars, some test chips were annealed at various elevated temperatures in a nitrogen environment prior to solder bump attachment. The annealed CPH pillar bump assemblies, together with a batch of non-annealed CPH pillar and flip-chip bump assemblies were subjected to an RTC test, with a rapid cycling regime of 0 – 100 $^{\circ}\text{C}$, ramp rate of 5 $^{\circ}\text{C}/\text{sec}$ and dwell time of 40 seconds. The test chips for RTC testing are summarized in Table 7.3. Due to yield loss during assembly, the sample sizes of test chips were different.

Table 7.3 Types of test chips prepared for RTC evaluation

S/N	Type of Test Chip	Sample Size
1	FCB: flip-chip with 110 µm diameter soldering pads, 120 µm diameter SAC bumps	8
2	CPH-165-NA: Non-annealed CPH pillars, height 165 µm, pillar diameter 80 µm, pinhead diameter 110 µm, with 120 µm diameter SAC bumps	11
3	CPH-165-250: CPH pillars annealed at 250 °C for 30 mins, height 165 µm, pillar diameter 80 µm, pinhead diameter 110 µm, with 120 µm diameter SAC bumps	10
4	CPH-165-325: CPH pillars annealed at 325 °C for 30 mins, height 165 µm, pillar diameter 80 µm, pinhead diameter 110 µm, with 120 µm diameter SAC bumps	8
5	CPH-165-400: CPH pillars annealed at 400 °C for 30 mins, height 165 µm, pillar diameter 80 µm, pinhead diameter 110 µm, with 120 µm diameter SAC bumps	12

7.1.5. RTC reliability results and analyses of improved CPH pillar bump assemblies

Two-parameter Weibull plots are used to analyse the probability of failure for each type of test chip. The slope or shape parameter of the Weibull plot, β , describes the failure distribution that best fits the data. $\beta < 1$ indicates infant mortality failures, $\beta = 1$ is random failures and $\beta > 1$ indicates wearout failures. The characteristic life, η , is the number of cycles to failure at 63.2%. The number of cycles or time to failure is denoted by t . The reliability function, $R(t)$, and probability of failure, $F(t)$, are given by the following equations (Ohring, 1998):

$$R(t) = e^{-(t/\eta)^\beta} \quad (7.1)$$

$$F(t) = 1 - e^{-(t/\eta)^\beta} \quad (7.2)$$

The RTC evaluation results of each test chip given in Table 7.3 are shown in the 2-parameter Weibull plots in Figures 7.5(a) – (e) respectively.

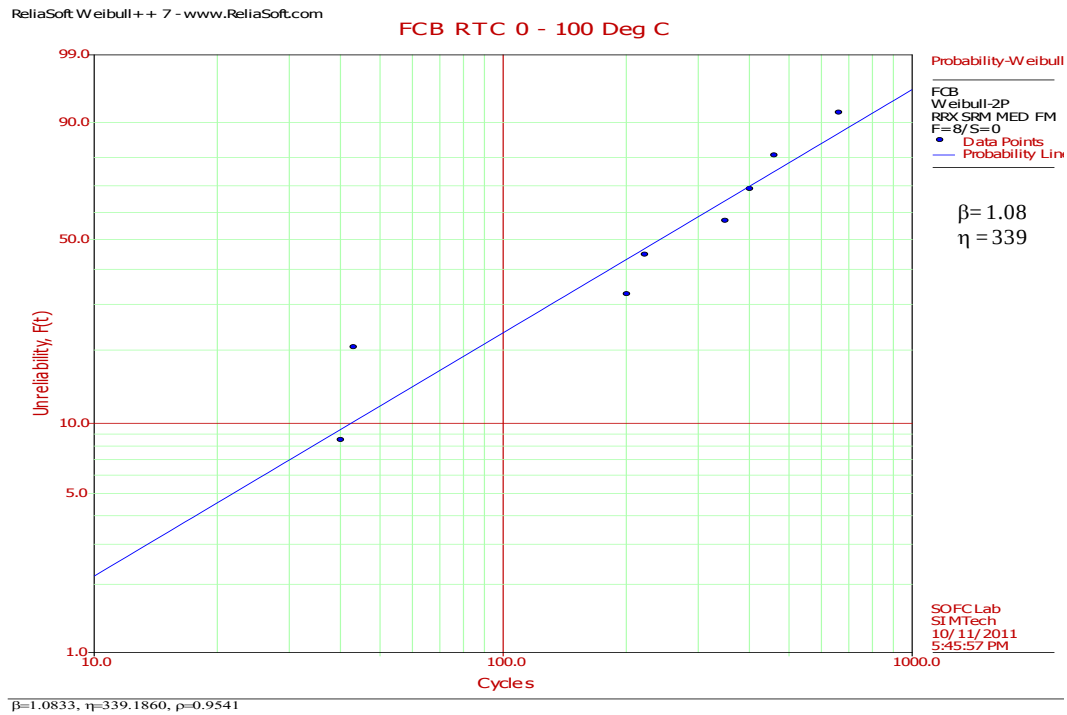


Figure 7.5(a) RTC solder joint reliability of FCB. Conventional flip-chip assembly

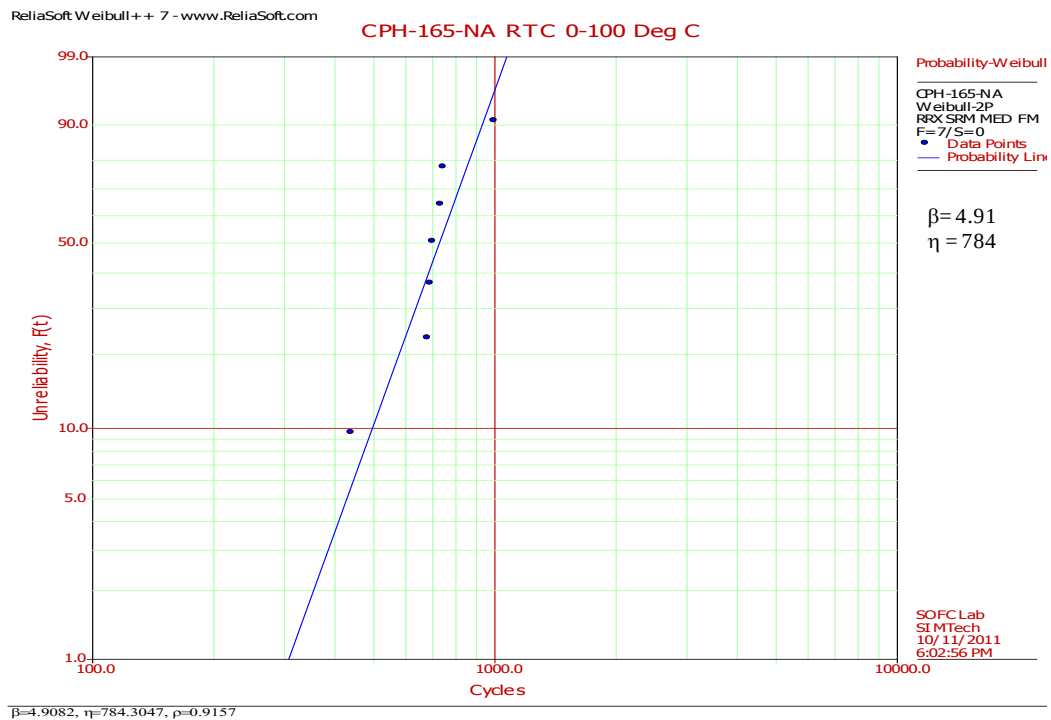


Figure 7.5(b) RTC solder joint reliability of CPH-165-NA. Non-Annealed CPH pillar assembly

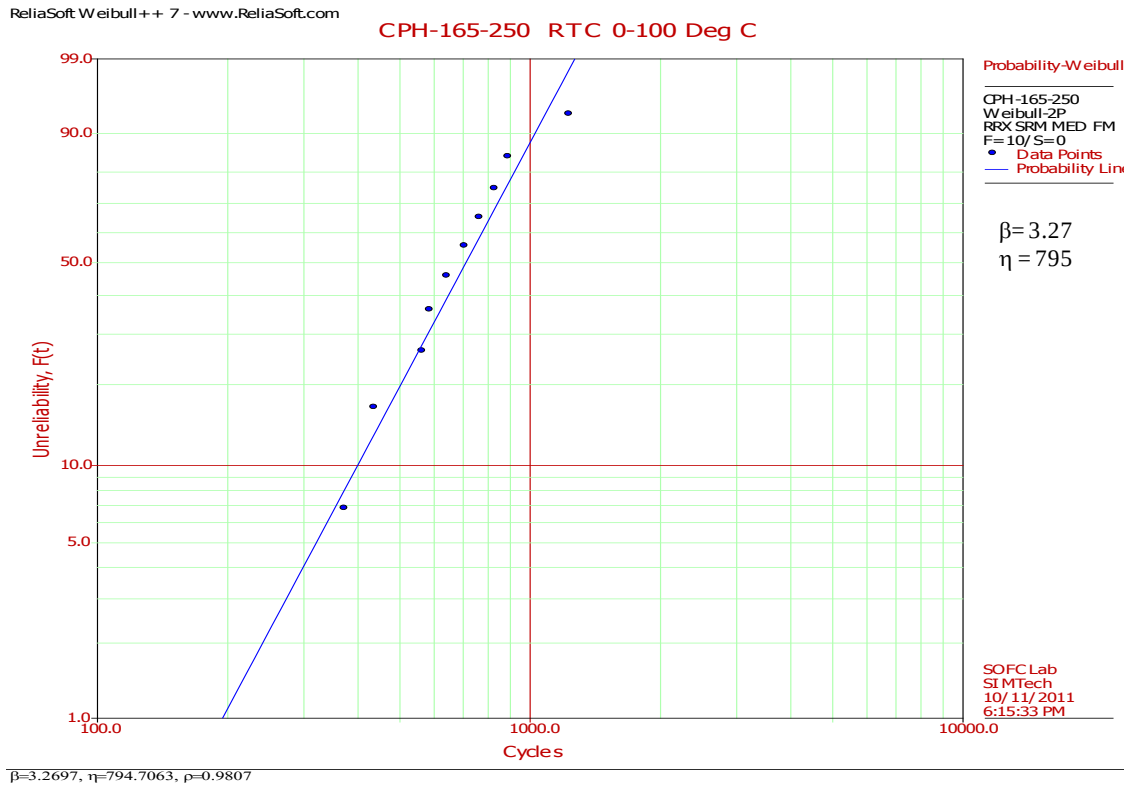


Figure 7.5(c) RTC solder joint reliability of CPH-165-250. Annealed CPH pillar assembly (CPH pillars annealed at 250°C for 30 mins)

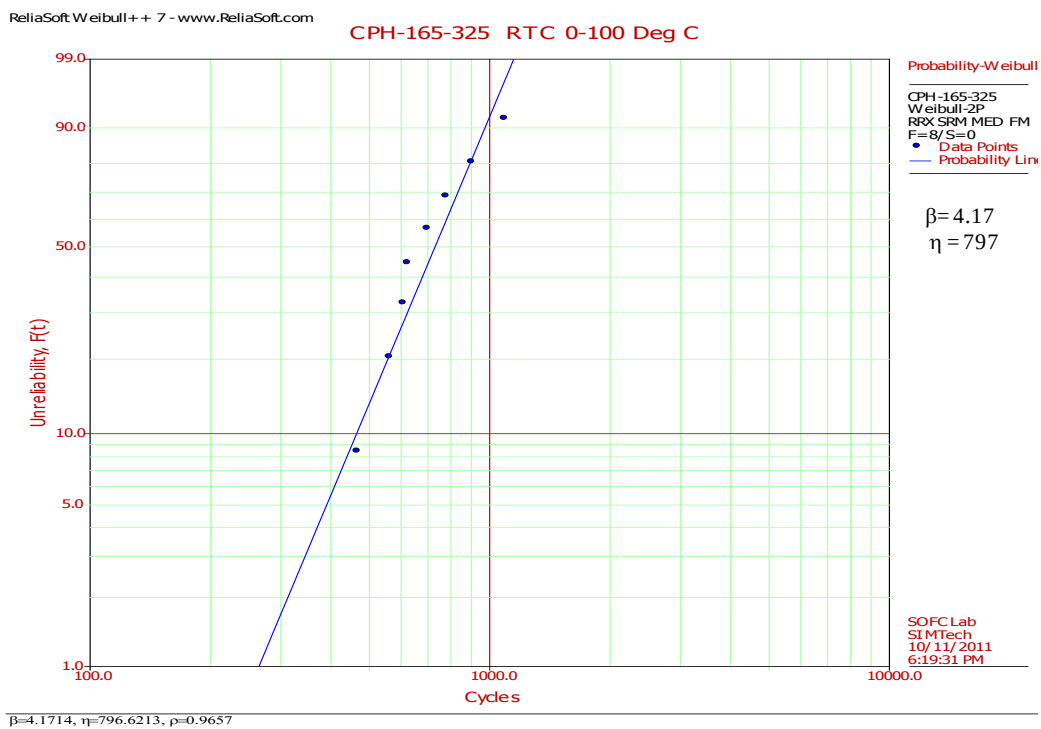


Figure 7.5(d) RTC solder joint reliability of CPH-165-325. Annealed CPH pillar assembly (CPH pillars annealed at 325°C for 30 mins)

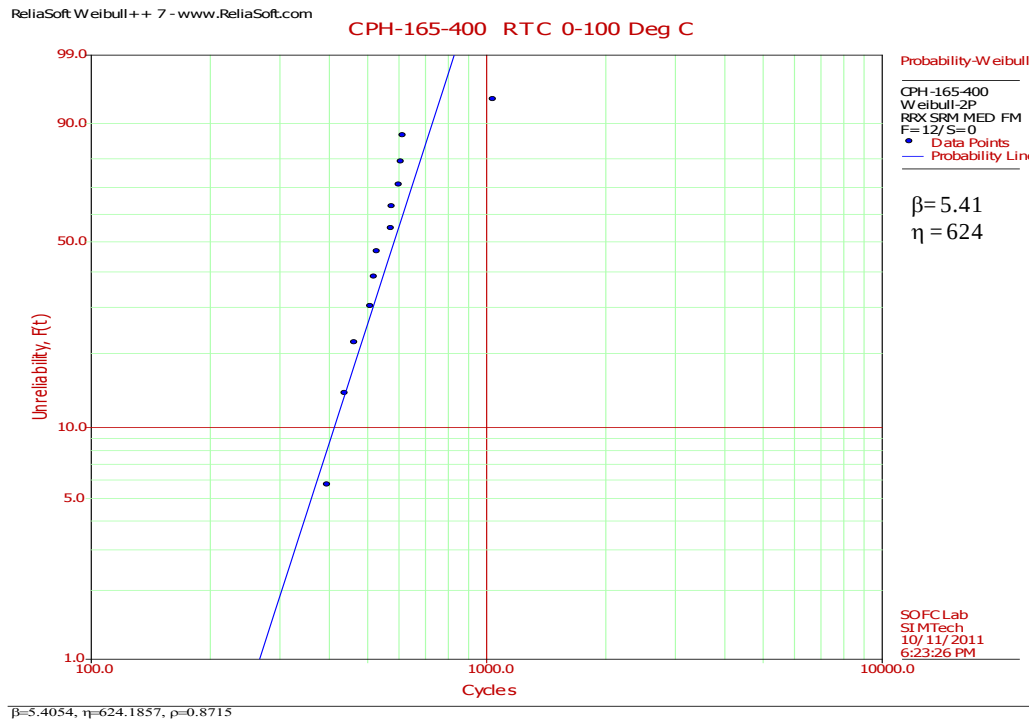


Figure 7.5(e) RTC solder joint reliability of CPH-165-400. Annealed CPH pillar assembly (CPH pillars annealed at 400°C for 30 mins)

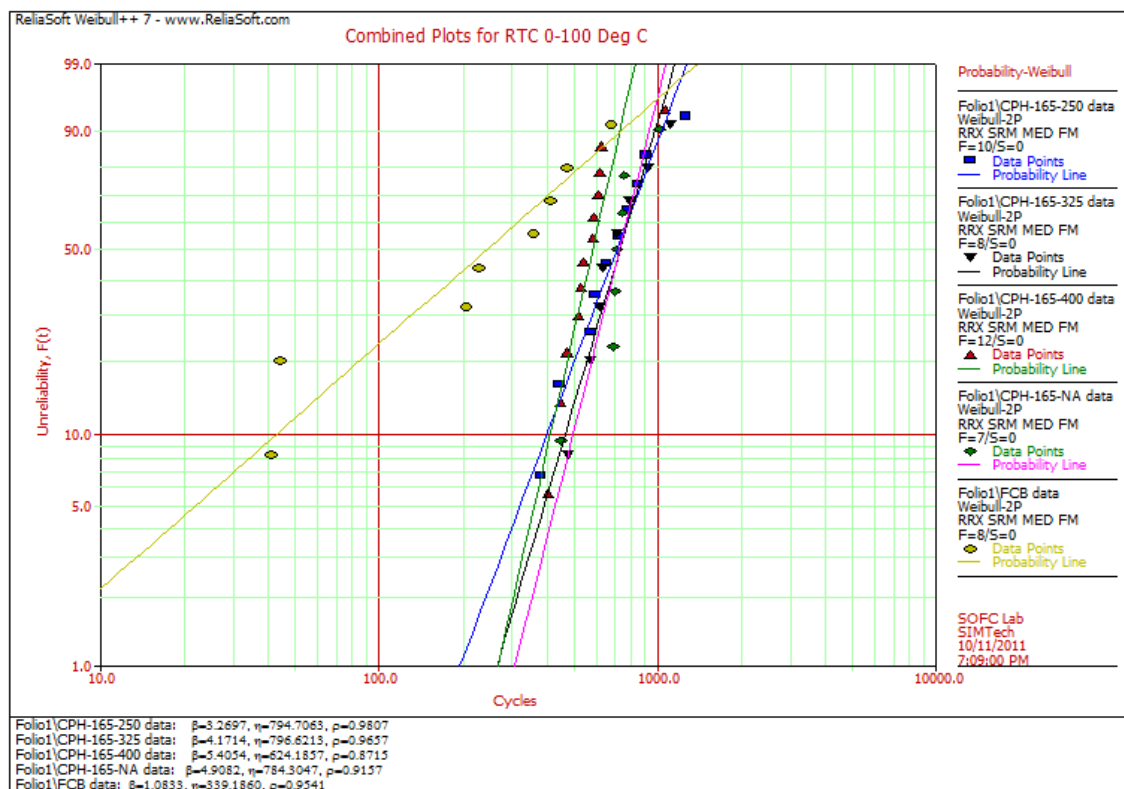


Figure 7.5(f) RTC solder joint reliability of conventional flip-chip, non-annealed and annealed CPH pillar bump assemblies

Table 7.4 Summary of the RTC reliability performance of the conventional flip-chip and CPH pillar bump assemblies

S/N	Test chip	β	η	$R(t) = e^{-(t/\eta)^\beta}$ RTC Reliability at 500 cycles
1	FCB	1.08	339	22%
2	CPH-165-NA: CPH pillars without annealing	4.91	784	90%
3	CPH-165-250: CPH pillars annealed at 250 °C for 30 mins	3.27	795	80%
4	CPH-165-325: CPH pillars annealed at 325 °C for 30 mins	4.17	797	87%
5	CPH-165-400: CPH pillars annealed at 400 °C for 30 mins	5.41	624	74%

Note: CPH pillars were annealed before soldering

A combined Weibull plot showing all the RTC results is shown in Figure 7.5 (f). A summary of the RTC reliability performance of the conventional flip-chip and CPH pillar bump assemblies is given in Table 7.4. As shown in Figure 7.5 (a), FCB has a β value of 1.08, which indicates that the conventional flip-chip assembly without underfill has infant mortality failures or random failures. FCB has a characteristic life of only 339 cycles as shown in Figure 7.5 (a). This is not surprising as it is well established that flip-chip-on-board is not reliable without underfill. As shown in Figures (b) – (e), the β values of all the CPH pillar assemblies tested are in the range of 3.27 to 5.41, which indicate wear-out failures due to fatigue. The annealed Cu pillars, CPH-165-250 and CPH-165-325, have marginally higher characteristic lives (η) than the non-annealed Cu pillars, CPH-165-NA. The CPH-165-250 and CPH-165-325 Cu pillar bump assemblies characteristic lives at 63.2% failures are 795 and 797 cycles respectively. The annealing process is expected to improve the ductility of the CPH pillars, thereby giving better compliance and fatigue resistance during RTC. However, the elevated temperature annealing at 400 °C seems to have degraded the solderability

of the pillars, leading to a poorer solder bump interconnection and reliability, and a lower characteristic life of 624 cycles.

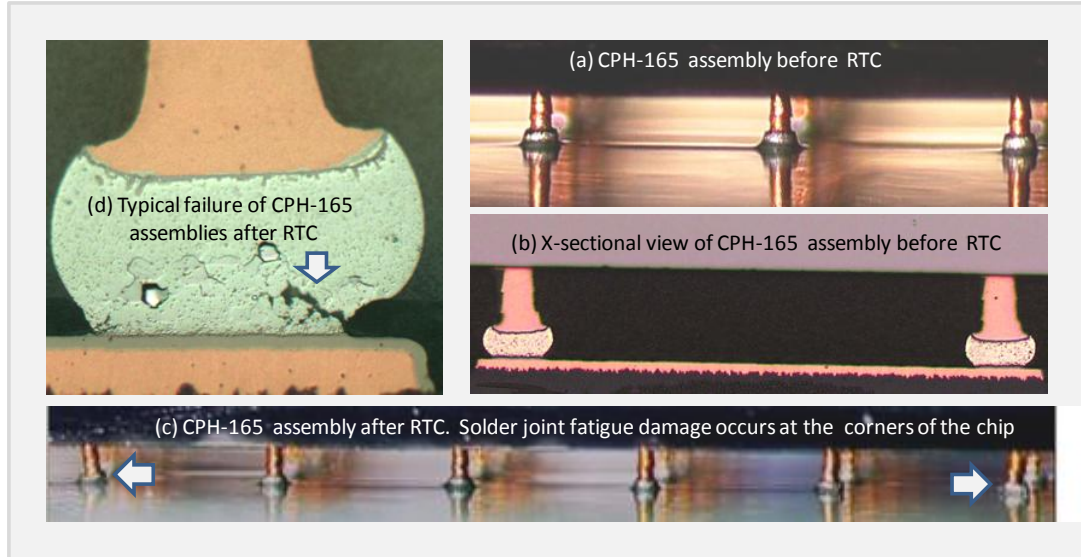


Figure 7.6 A typical CPH-165 type assembly: (a) & (b) before RTC, (c) & (d) after RTC test

Using Eq. 7.1, the reliability, $R(500)$, of the assemblies to survive 500 cycles in the RTC test at 0 – 100 °C can be computed. The reliability data in Table 7.4 indicates that CPH-165-250 and CPH-165-325 are able to achieve a $R(500)$ reliability of 80% and 87% respectively. CPH-165-NA is able to reach a reliability $R(500)$ of 90% and FCB only 22%. It is clear that CPH-165 type interconnection is superior to FCB type interconnection. A typical CPH-165 solder joint before and after RTC is shown in Figure 7.6.

The results in the RTC test show that increasing the pillar diameter from 40 μm to 80 μm and overall pillar height to 165 μm has enhanced the solder joint reliability of CPH pillar bump assemblies. Both the non-annealed and annealed CPH pillar solder joints performed better in comparison with standard flip-chip solder joints. The influence of elevated temperature annealing on the compliance of a CPH pillar is only

marginally better. Further investigation using accelerated temperature cycling (ATC) test would be necessary.

7.2. Accelerated temperature cycling test

Accelerated temperature cycling (ATC) test is widely adopted for assessing solder joint reliability. According to IPC (IPC-SM-785, 1992) guidelines for accelerated reliability testing for consumer electronic products, the worst-case operating environment is between 0°C and +60°C with a total of 365 service cycles per year. Further reference to IPC (IPC-9701, 2002) performance test methods for surface mount devices, temperature cycling conditions of 0-100°C and 500 cycles duration were selected for ATC test in this study. The reliability results derived should be applicable to both consumer electronics and computer products. A dwell time of 10 minutes as recommended by IPC-9701 is chosen to allow build-up stresses to relax. This is important, particularly in evaluating Pb-free solders which has a 10 – 100 times lower creep rate than Sn-Pb solder (Grossman et al, 2002). The test vehicles were assembled without underfill.

7.2.1. ATC experimental procedure and sample preparation

The ATC test was carried out in a Temptronic MobileTemp chamber. It was set to a ramp rate of 10 °C per minute and a dwell time of 10 minutes for the upper and lower temperature limits. A temperature cycle could be completed in 40 minutes. The defined temperature cycling profile is shown in Figure 7.7.

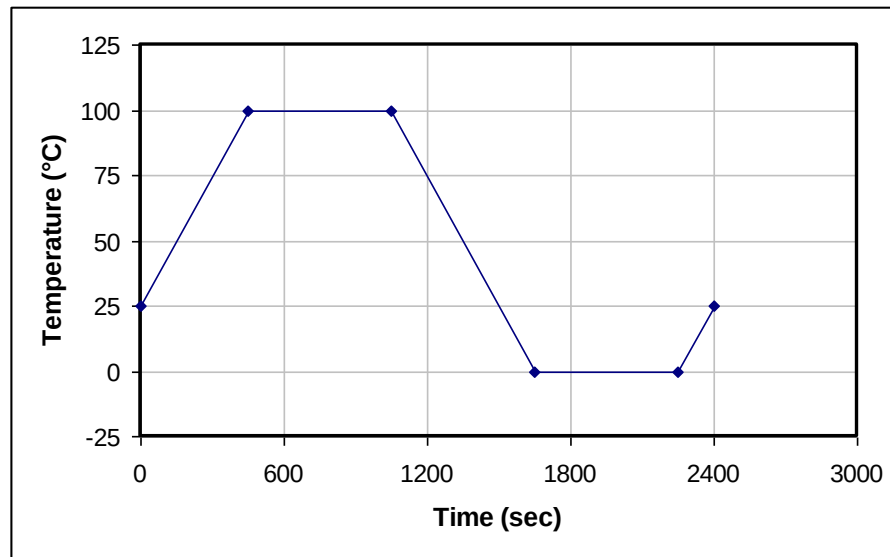


Figure 7.7 Accelerated temperature cycling (ATC) test profile

Three types of test chips were used in the ATC test, a conventional flip-chip and two different types of CHP pillar chip. One type of CPH chip has a pillar height of 135 μm and the other a pillar height of 165 μm . One batch of CPH pillar chips with a pillar height of 165 μm was annealed at 250 $^{\circ}\text{C}$ for 30 minutes (before solder bumping) to investigate the influence of annealing on CPH pillar compliance.

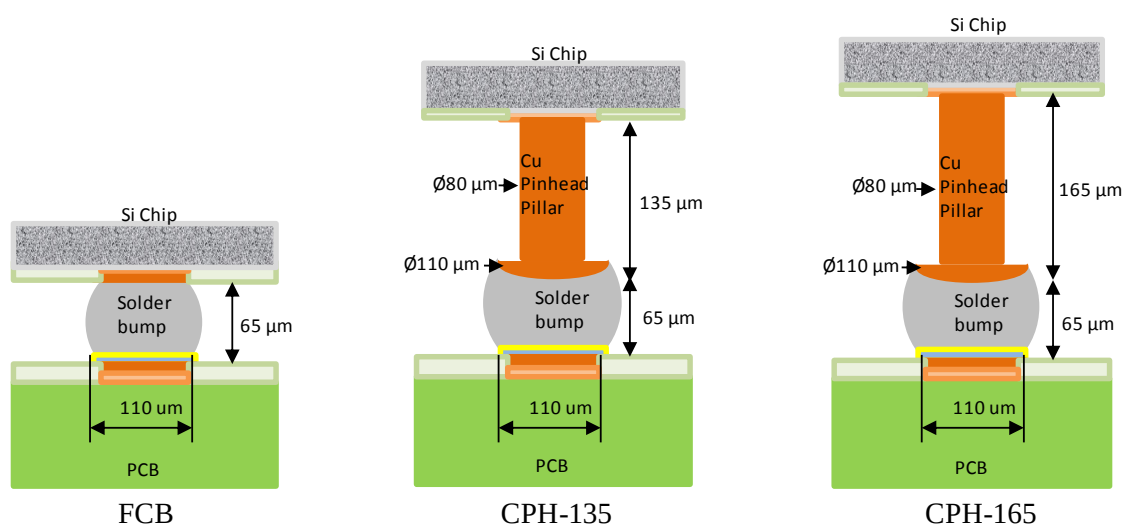


Figure 7.8 Three types of test chips were assembled for ATC reliability test

All the test chips were attached with 120 μm SAC solder bumps. Figure 7.8 provides a schematic of the test vehicles assemblies. The description of the test chips is given in Table 7.5. The layout of the test vehicle and substrate was similar to that of Figure 7.1.

Table 7.5 Types of test chips prepared for ATC reliability test

S/N	Type of Test Chip	Sample Size
1	FCB: flip-chip attached with 110 μm soldering pads attached with 120 μm diameter SAC bumps	12
2	CPH-135: Non-annealed CPH pillars, height 135 μm , pillar diameter 80 μm , pinhead diameter 110 μm , attached with 120 μm diameter SAC bumps	12
3	CPH-165-NA: Non-annealed CPH pillars, height 165 μm , pillar diameter 80 μm , pinhead diameter 110 μm , attached with 120 μm diameter SAC bumps	11
4	CPH-165-250: CPH pillars annealed at 250 $^{\circ}\text{C}$ for 30 mins, pillar height 165 μm , pillar diameter 80 μm , pinhead diameter 110 μm , attached with 120 μm diameter SAC bumps	11

Note: Due to assembly defect, CPH-165-NA and CPH-165-250 samples have 11 chips each

7.2.2. ATC reliability results and analyses of conventional flip-chip, CPH-135 and CPH-165 pillar bump assemblies

The ATC evaluation results of each test chip given in Table 7.5 are shown in the two-parameter Weibull plots in Figures 7.9(a) – (d) respectively.

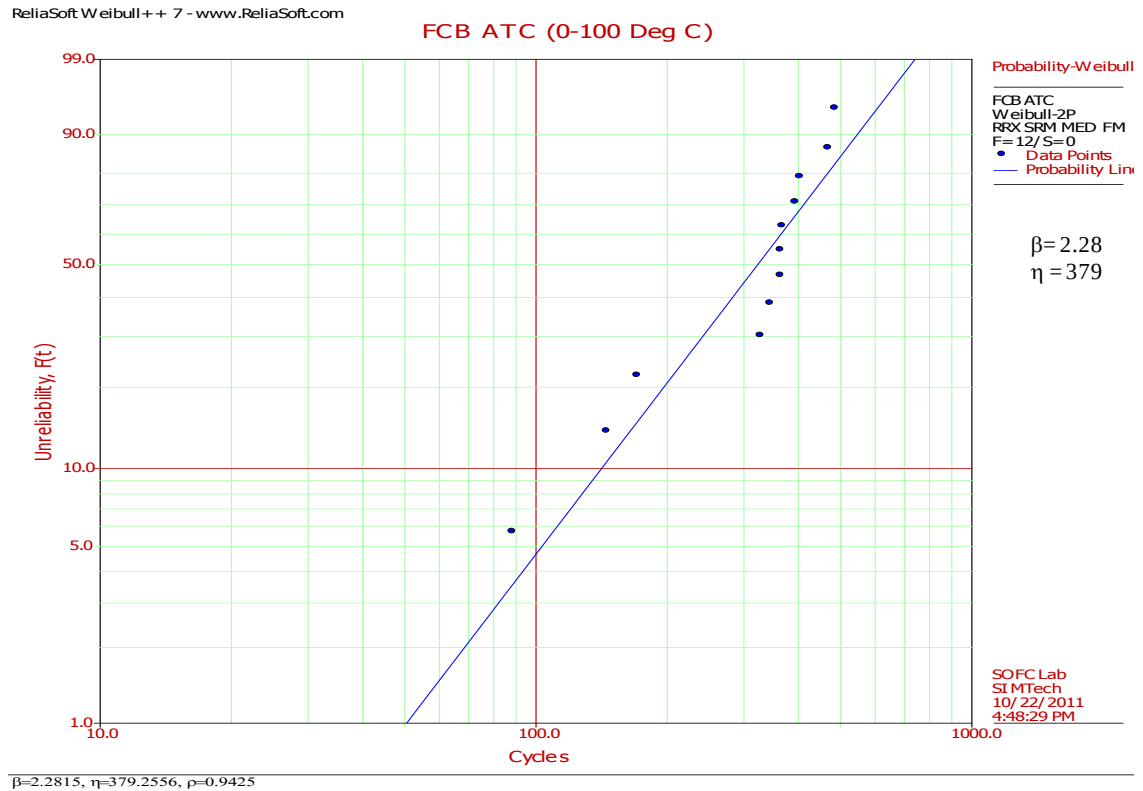


Figure 7.9(a) ATC solder joint reliability of FCB

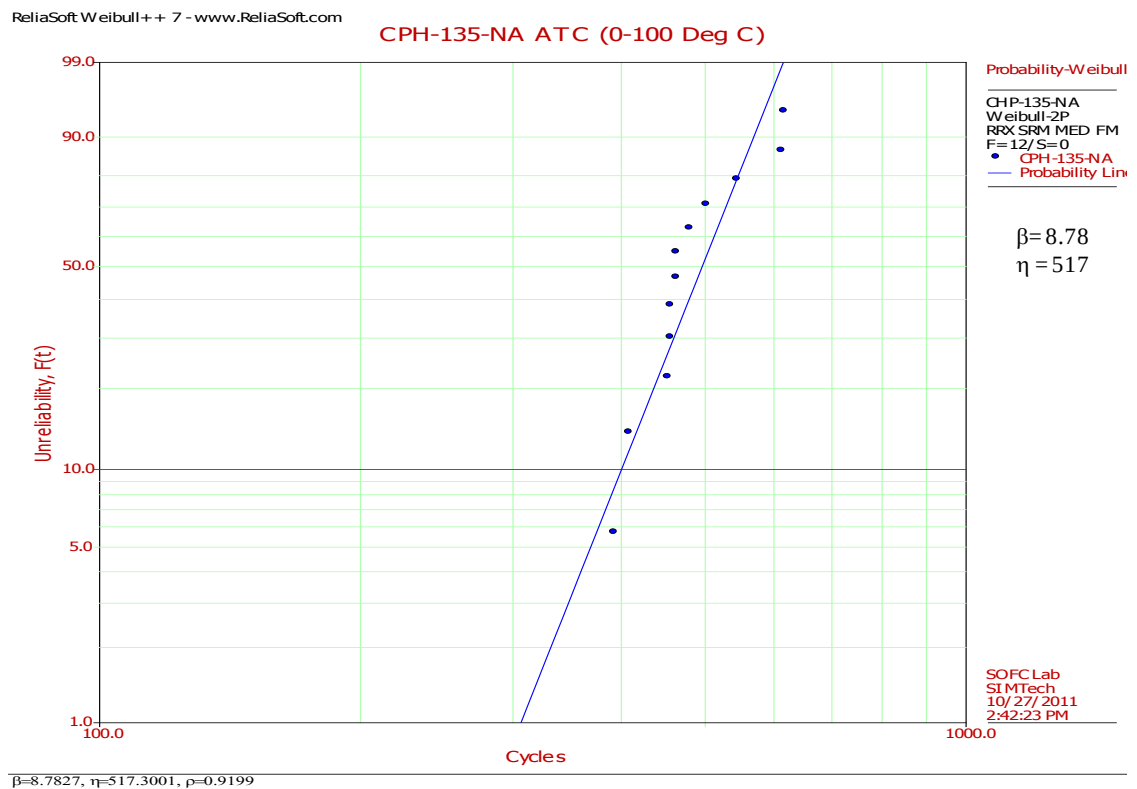


Figure 7.9(b) ATC solder joint reliability of CPH-135-NA

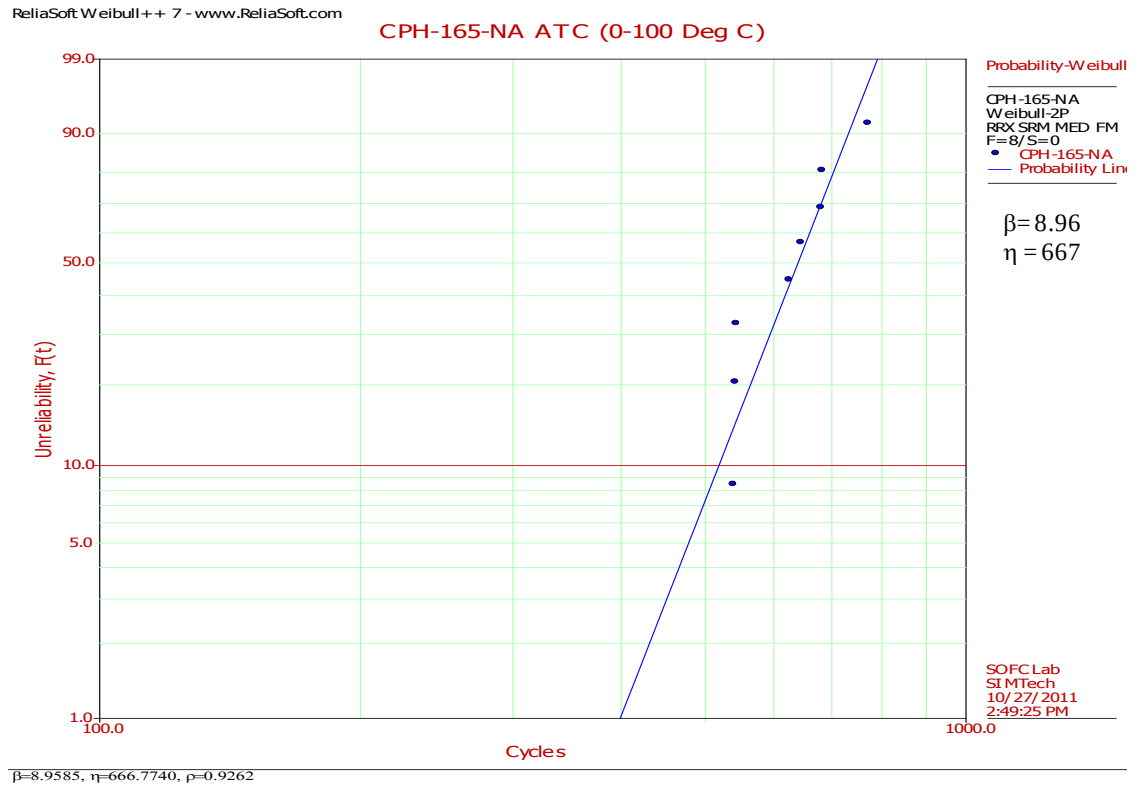


Figure 7.9(c)

ATC solder joint reliability of CPH-165-NA

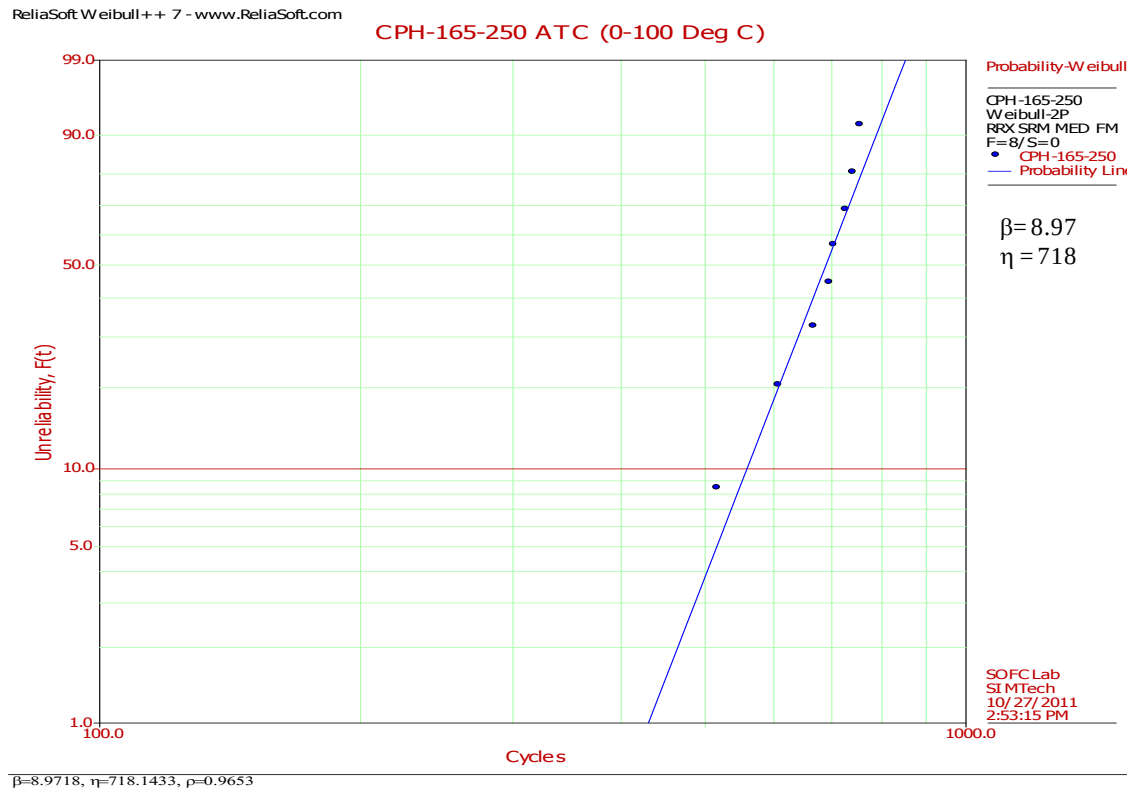


Figure 7.9(d)

ATC solder joint reliability of CPH-165-250

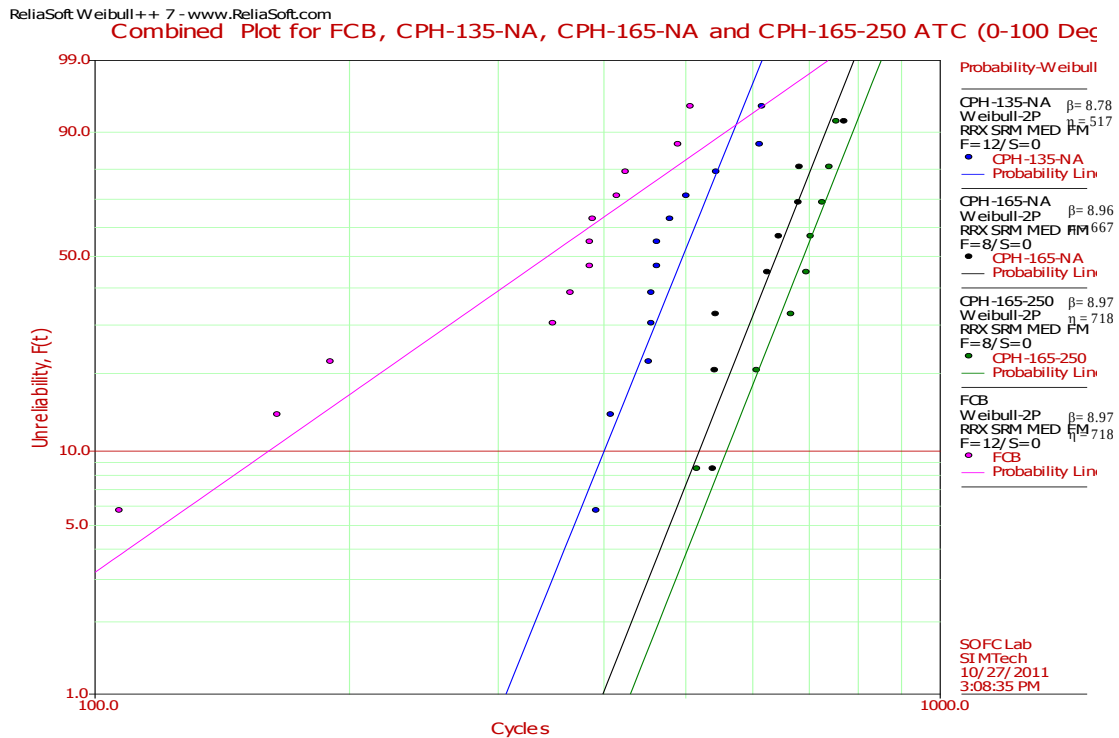


Figure 7.9(e) ATC solder joint reliability of FCB, CPH-135-NA, CPH-165-NA and CPH-165-250

Table 7.6 Summary of the ATC reliability performance of the conventional flip-chip and CPH pillar bump assemblies

S/N	Test chip	β	η	$R(t) = e^{-(t/\eta)^\beta}$ ATC Reliability at 500 cycles
1	FCB	2.28	379	15%
2	CPH-135-NA: CPH pillars without annealing	8.46	499	36%
3	CPH-165-NA: CPH pillars without annealed	8.09	650	89%
4	CPH-165-250: CPH pillars annealed at 250 °C for 30 mins	8.72	700	95%

A combined Weibull plot with all the ATC results is shown in Figure 7.9(e). A summary of the ATC reliability performance of the FCB conventional flip-chip and CPH pillar bump assemblies is given in Table 7.6. In the Weibull plot shown in Figure

7.9(a), FCB has a β value of 2.28 which indicates that the conventional flip-chip assembly without underfill has early wear-out failures. The characteristic life of FCB at 63.2% failures is 379 cycles. As shown in the Weibull plots in Figures 7.9(b) - (d), the β values of all the CPH pillar assemblies after ATC test are in the range of 8.78 to 8.97, which indicate wear-out failures due to fatigue. CPH-135-NA, which has a pillar height of 135 μm , has a characteristic life of 517 cycles. CPH-165-NA and CPH-165-250 have characteristic lives of 667 and 718 cycles respectively.

The ATC reliability data indicates that annealing CPH pillars at 250 °C for 30 minutes has improved the characteristic life of CPH-165 pillar solder joints. Using Eq. 7.2, it can be determined that CPH pillar assemblies can achieve a R(500) reliability of 96%. The better ATC reliability results of the annealed CPH-165-250 solder joints compared to that of non-annealed CPH-165-NA solder joints corroborates the findings in the previous chapter which indicate that annealing CPH pillars at 250 – 400 °C for 30 minutes can improve their ductility and compliance.

7.3. Microstructures and failure mechanisms of CPH pillar and FCB SAC solder joints

During the soldering process, the reaction of Sn in the solder with the metallized layers on the chip and substrate will result in the formation of an intermetallic compound (IMC) which is an essential joining layer for the solder joints. Uncontrolled reaction between Sn and metallized layers, on the other hand, can lead to excessive metal dissolution at the joining interfaces and formation of thick and brittle IMC which is detrimental to the long-term reliability of the solder joints. Studying the IMC formation and microstructural evolution of the SAC solder joint in FCB and CPH

solder joints can provide a better understanding on their reliability and failure mechanism.

The phase diagrams (Moon, 2000, NIST, 2011) as shown in Figure 7.10 illustrate the formation of different IMCs in the Sn-Ag-Cu system. Two diagrams are needed to show the metallurgical transformations that occur in the SAC alloy. In the ternary phase diagram, the percentage weight of Ag and Cu determines the percentage content of Sn. The temperature lines (isotherms) indicate the interactions at that specific temperature.

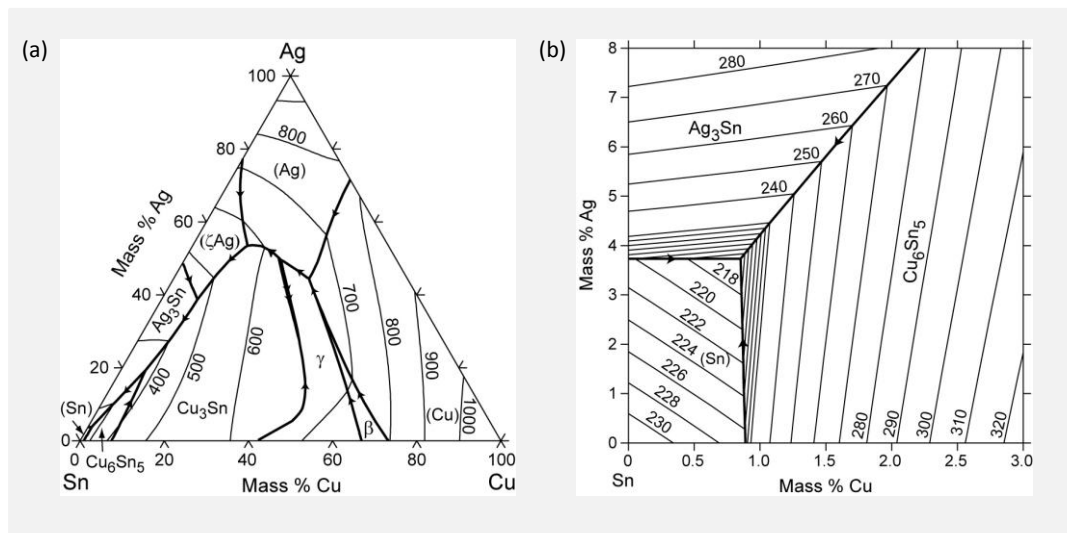


Figure 7.10 Sn-Ag-Cu ternary system temperature composition phase diagram (NIST, 2011)

The points of intersection of the isotherms on the composition axis determine the composition of the alloy at which the IMC formation takes place. The isotherms are drawn increasing from 218 °C as that is the melting point of SAC solder alloy and IMC formation is initiated in molten state. Figure 7.10(a) shows the 3D phase diagram of a SAC system. It can be seen that the Ag and Cu phases are very stable and do not interact even at temperatures above 700 °C. Hence, any interaction in the system is

either in the Sn-Ag phase or in the Sn-Cu phase. Figure 7.10(b) shows the Sn-rich region which is commonly observed in the SAC solder alloy.

The formation and growth of IMC in Pb-free solders have been investigated extensively (Bader, 1995, Korhonen, 2000, Zribi, 2001, Ho, 2002, Kang, 2002, Tu, 2007). In general, the findings show that substrate or chip pad metallization of Cu has a high dissolution rate in molten Pb-free solders. Electrolytic Ni-Au and electroless Ni with immersion Au (ENIG) are found to be better wetting and barrier layers to interface with Pb-free solder. In this study, the IMCs and microstructures of SAC solder on CPH pillar and FCB UBM were characterized.

7.3.1. Experimental samples for FCB and CPH interconnection microstructural studies

The schematic of FCB and CPH solder interconnections are shown in Figure 7.11. Electrolytic Ni-Au on Cu served as the UBM layer on the FCB chip side and on the CPH pinhead surface. The substrate soldering pads were Cu and ENIG served as the wetting and barrier layer. SAC 305 (Sn-3.0% Ag-0.5% Cu at. wt.) solder bumps of 120 μm diameter were used in the solder assembly. The solder interfaces on the FCB chip side and CPH pinhead experienced two reflow exposures; one in solder bumping process and the other during assembly process. The maximum reflow temperature on the solder joints was 245 °C and the dwell above 217 °C was approximately 60 seconds. As-reflowed samples and samples subjected to temperature cycling tests were characterized by optical microscopy, SEM and EDX.

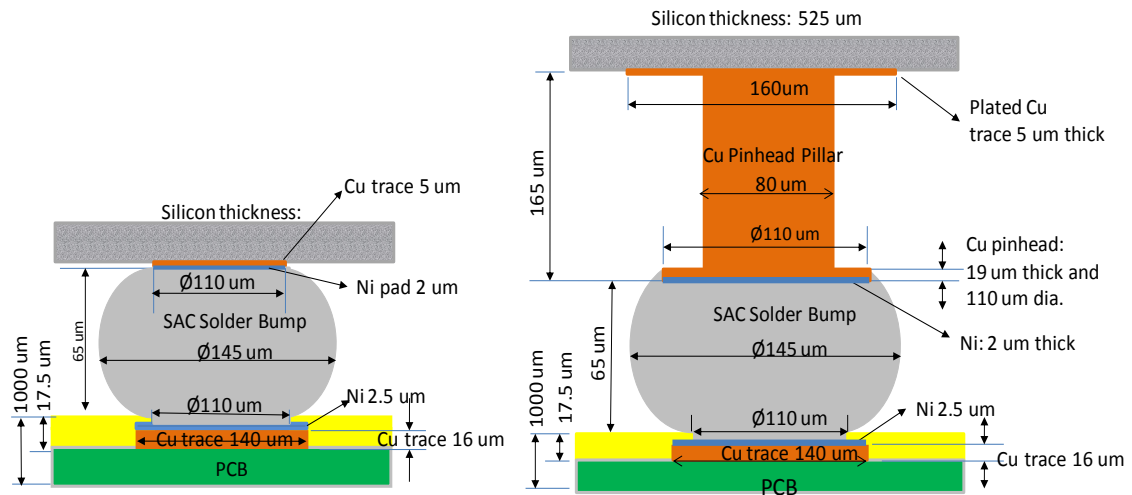


Figure 7.11 Schematics of FCB and CPH solder interconnections

7.3.2. Microstructure characterization of FCB and CPH solder joints

The UBM on the FCB chip-side is electrolytic Ni (2.0 µm) and Au (0.1 µm). Figure 7.12 (a) shows the cross-sectional view of a FCB solder joint after reflow soldering and Figure 7.12 (b) is the corresponding EDX spectra. The IMC layer has a continuous layer of Ni_3Sn_4 growing from the Ni UBM interface to the surface, where needle-like microstructures extend into the bulk solder. The needle-like microstructures near the base have a Ni_3Sn_4 whilst the extended microstructures are found to be $(\text{Ni,Cu})_3\text{Sn}_4$. As the Ni_3Sn_4 is formed, the Ni atoms available for reaction are reduced and the kinetics of the reaction support the formation of $(\text{Ni,Cu})_3\text{Sn}_4$. Some larger and blocky $(\text{Ni,Cu})_3\text{Sn}_4$ and $(\text{Cu,Ni})_6\text{Sn}_5$ are found to have spalled from the IMC layer. At the vicinity of the IMC, Ag_3Sn and AuSn_4 are spotted.

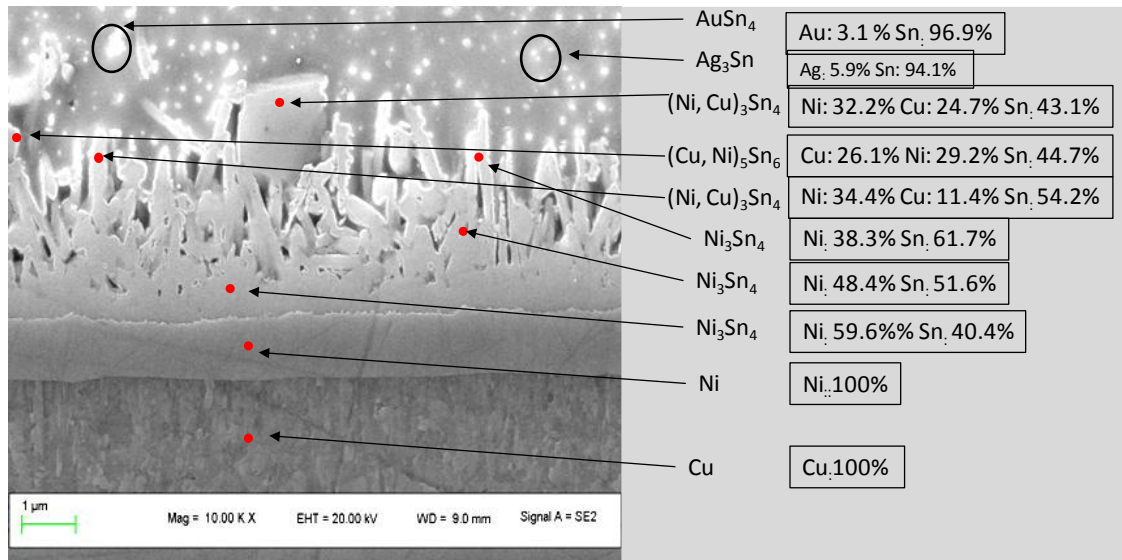


Figure 7.12(a) SEM image of a FCB solder joint at the chip-side after reflow. The EDX elemental analyses are in atom%

At the substrate side, ENIG (2.5 μ m) is the metallization over the Cu soldering pad. The UBM layer after reflow has approximately 89% Ni and 11% P. A distinct layer of NiSnP could be seen above the Ni(P) UBM and some voids are found. Needle-like structures identified as (Ni,Cu)₃Sn₄ with EDX are found on top of the NiSnP layer and Ag₃Sn and AuSn₄ are spotted within the bulk solder matrix. The IMC is illustrated in Figure 7.13(a) and its corresponding EDX spectra are shown in Figure 7.13(b).

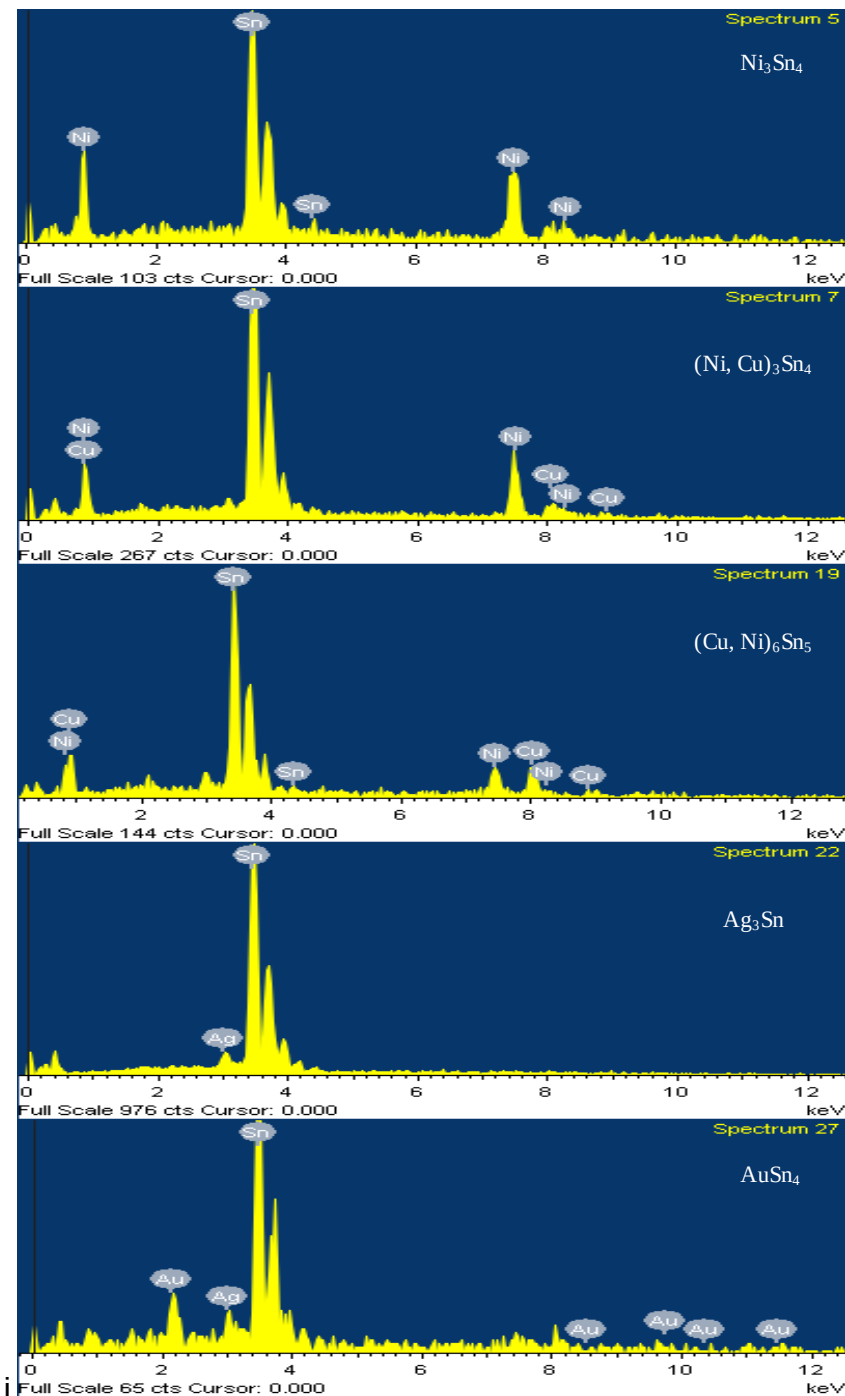


Figure 7.12(b) EDX spectra of the IMC in the FCB solder joint at the chip-side

The SEM observations and EDX analyses on the FCB solder joint microstructure suggest that when there is a strong presence of Ni as in electrolytic Ni UBM, the formation of Ni_3Sn_4 is not suppressed by the presence of Cu in Sn-3.0%-0.5%Cu solder and the Cu layer beneath the Ni UBM which cannot diffuse out fast

enough to influence the reaction. Subsequently, $(\text{Ni,Cu})_3\text{Sn}_4$ IMC may be formed by reacting with a lower content of Ni and Cu from the SAC solder present above the Ni_3Sn_4 layer. In contrast to the chip-side, where a Ni_3Sn_4 continuous IMC layer is formed at the electroplated Ni UBM, the IMC at the ENIG interface on the substrate-side comprises a dense cluster of needle-like $(\text{Ni,Cu})_3\text{Sn}_4$. No Ni_3Sn_4 compound is observed on the substrate-side. The results suggest that there is enough Cu content during the reflow reaction to support the formation of $(\text{Ni,Cu})_3\text{Sn}_4$ instead of Ni_3Sn_4 . The supply of Cu atoms could have come from the Cu pad beneath the UBM by diffusion through the amorphous Ni(P) layer and through some of the voids in the NiSnP layer.

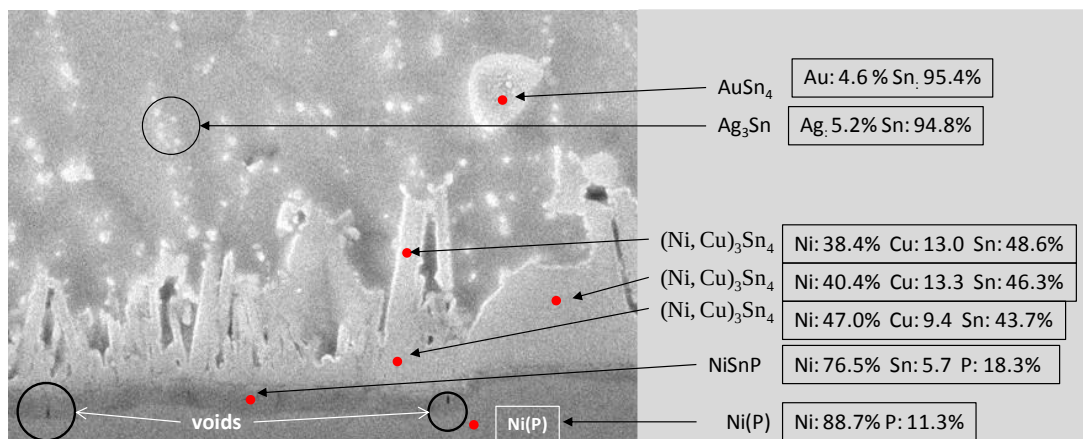


Figure 7.13(a) SEM image of a FCB solder joint at the substrate-side after reflow. The EDX elemental analyses are in atom%

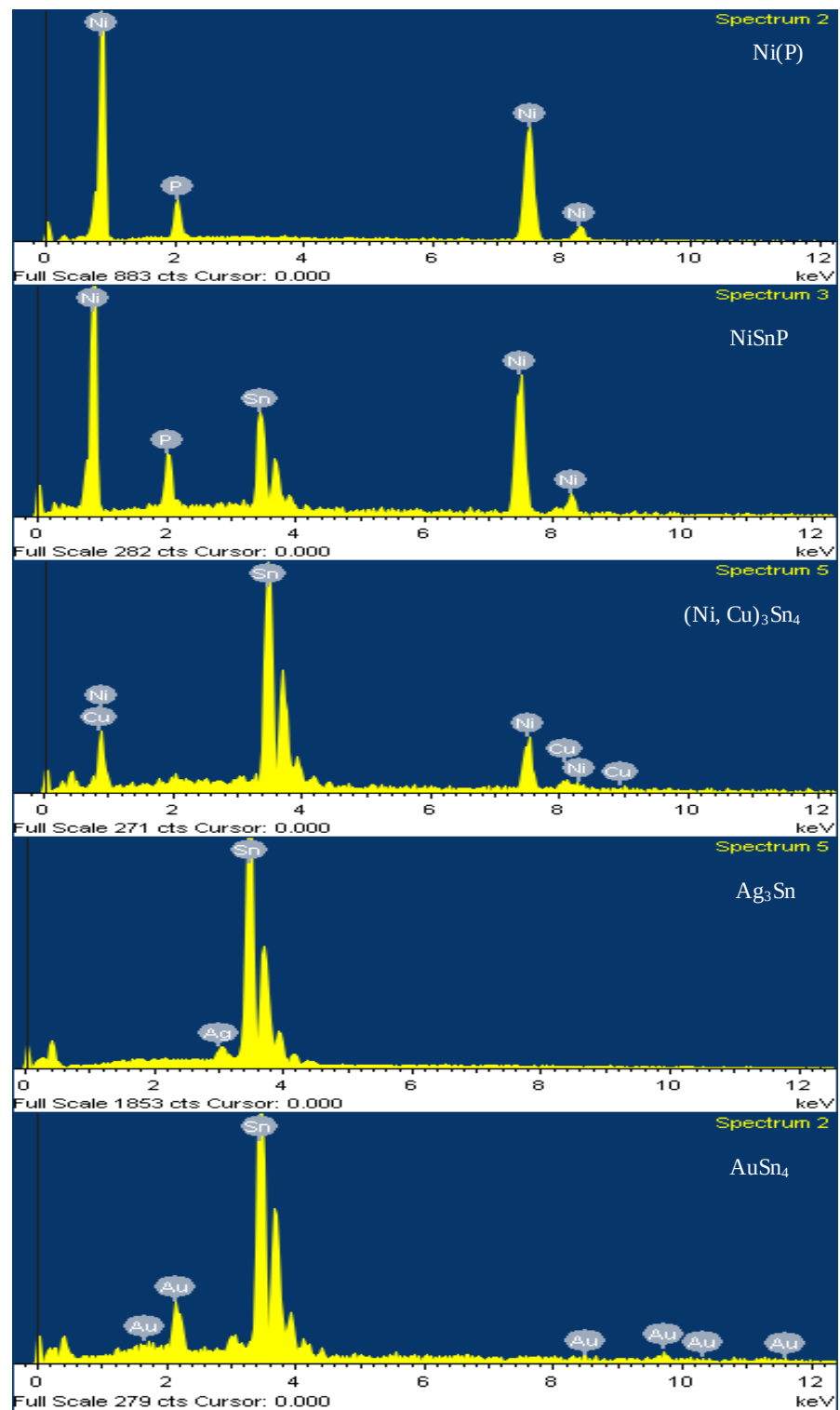


Figure 7.13(b) EDX spectra of the IMC in the FCB solder joint at the substrate-side

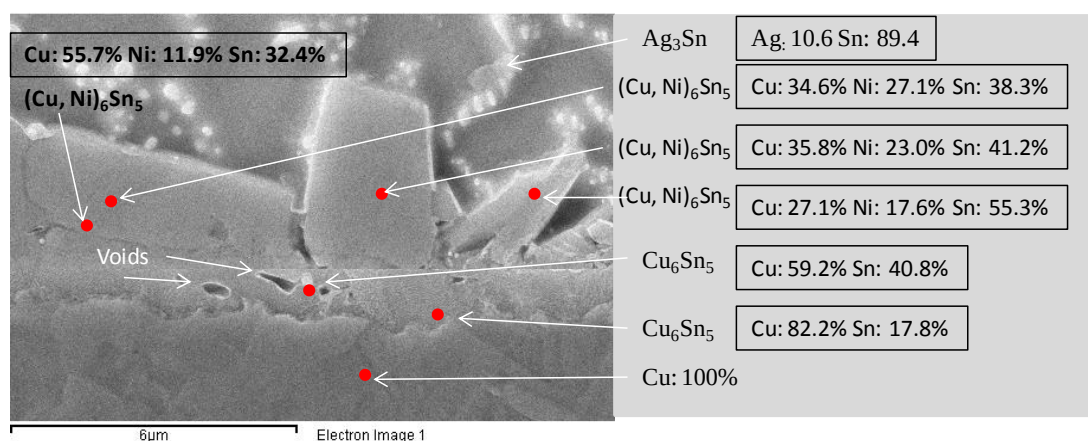


Figure 7.14(a) SEM image of a CPH solder joint at the chip-side after reflow. The EDX elemental analyses are in atom%

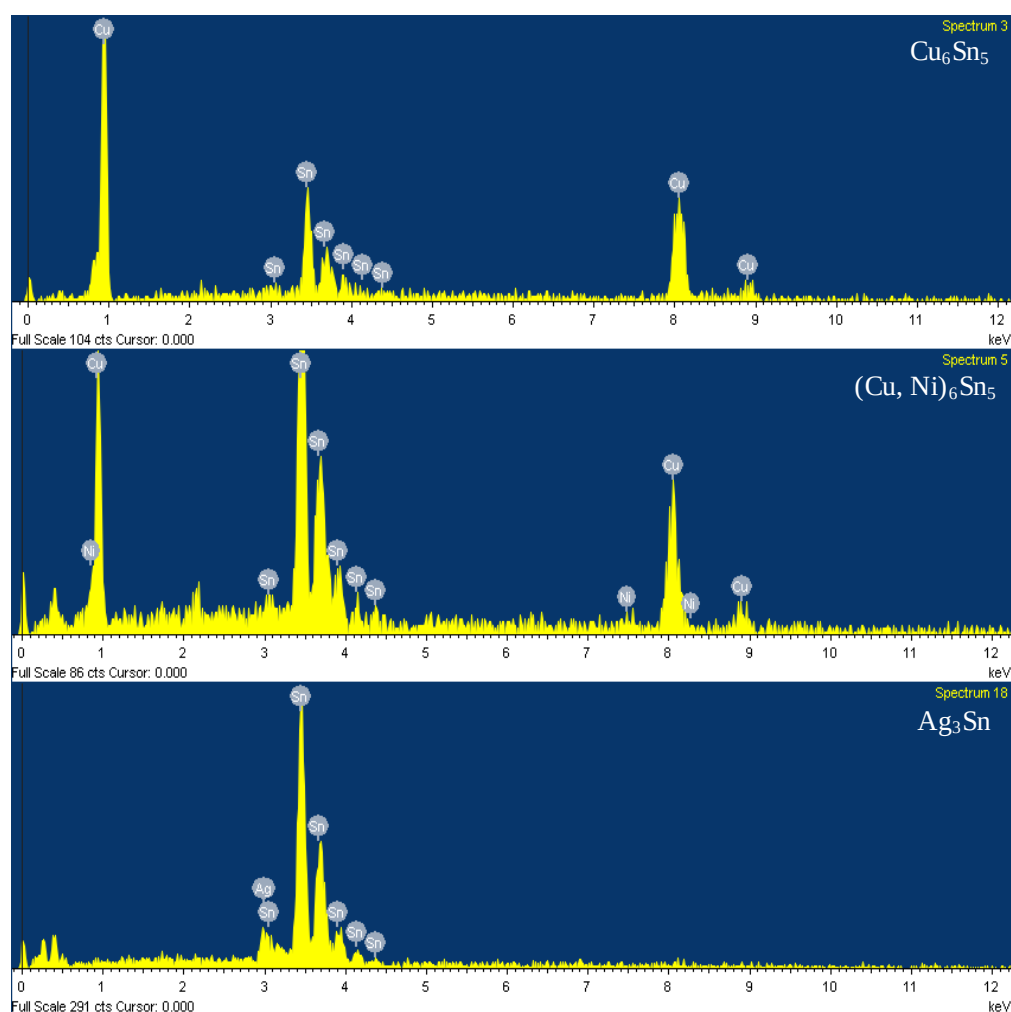


Figure 7.14(b) EDX spectra of the IMC in the CPH solder joint at the chip-side

The UBM on the CPH chip-side is electrolytic Ni (0.4 μm) and Au (0.1 μm). The intended Ni UBM thickness was 2 μm but due to process variation only 0.4 μm was deposited. As a result of the thin Ni UBM, the entire Ni UBM is converted to IMC after 2 reflow exposures (bumping + assembly), as shown in Figures 7.14(a) and (b). It is observed that the IMC layer directly at the interface with the Cu pillar is Cu_6Sn_5 . On top of the Cu_6Sn_5 layer, a layer of $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC is found. Some blocky and needle-like $(\text{Cu},\text{Ni})_6\text{Sn}_5$ appear to be partially detached and spalling from the layered IMC.

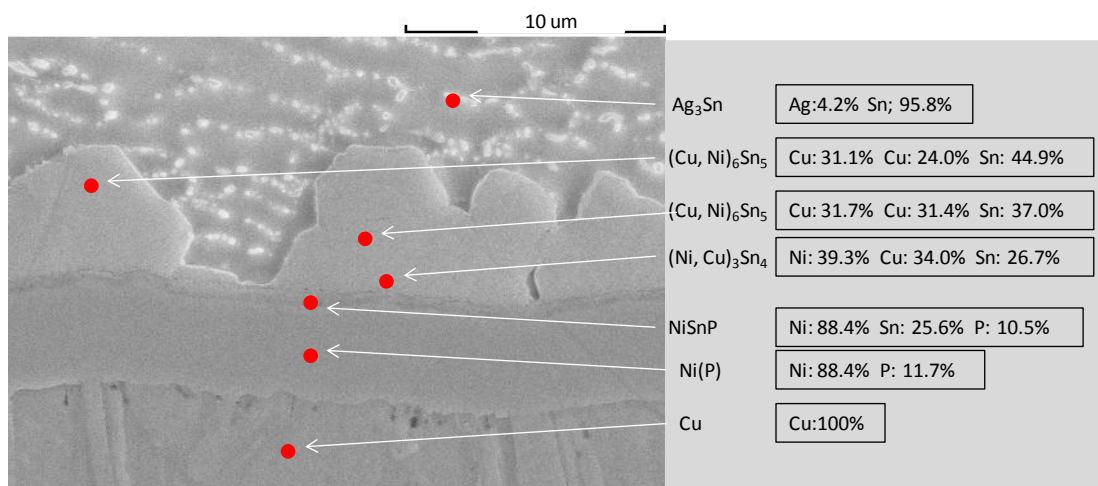


Figure 7.15(a) SEM image of a CPH solder joint at the substrate-side after reflow. The EDX elemental analyses are in atom%

At the substrate side, ENIG (2.5 μm) is the metallization over the Cu soldering pad. Figure 7.15(a) shows that the UBM layer after reflow has approximately 89% Ni and 11% P. The corresponding EDX spectra is shown in Figure 7.15(b). A distinct layer of NiSnP could be seen above the Ni(P) UBM and some Kirkendall voids are detected at the interface. Blocky and discontinuous $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC are formed on the NiSnP layer. No needle-like $(\text{Cu},\text{Ni})_6\text{Sn}_5$ is observed. $(\text{Ni},\text{Cu})_3\text{Sn}_4$ IMC is identified between $(\text{Cu},\text{Ni})_6\text{Sn}_5$ and the NiSnP layer.

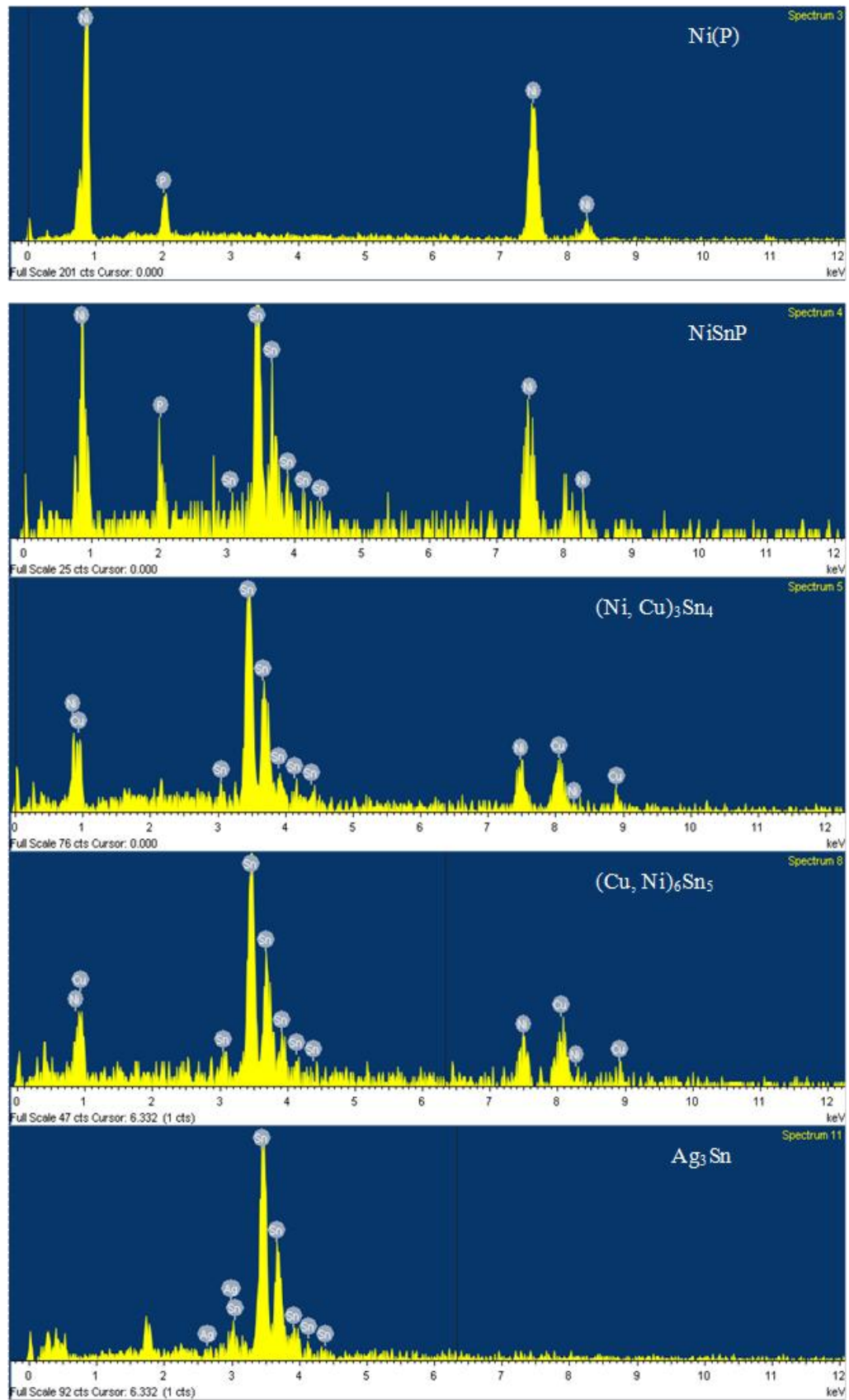


Figure 7.15(b) EDX spectra of the IMC in the CPH solder joint at the substrate-side

The EDX analyses and SEM results (see Figures 7.12, 7.13, 7.14 and 7.15) suggest that Cu diffusion from Cu pillar has contributed to the reactions to form Cu_6Sn_5 and suppressed the formation of Ni_3Sn_4 at the chip-side interface. In the presence of Ni UBM, some of the Cu_6Sn_5 IMC is transformed to $(\text{Cu},\text{Ni})_6\text{Sn}_5$ as Ni diffuses into the Cu_6Sn_5 . At the substrate-side interface, the actual sequence of $(\text{Ni},\text{Cu})_3\text{Sn}_4$ and $(\text{Cu},\text{Ni})_6\text{Sn}_5$ IMC formation is not clear. During reflow, the N(P) UBM could have first reacted with Sn and Cu in the SCA alloy to form $(\text{Ni},\text{Cu})_3\text{Sn}_4$. As $(\text{Cu},\text{Ni})_6\text{Sn}_5$ is thought to be more stable than $(\text{Ni},\text{Cu})_3\text{Sn}_4$ (Tu, 2007), the former could be formed as the Ni atoms in the latter are displaced by Cu atoms diffused across from the Cu pillar.

The particles among the β -Sn matrix are identified by EDX as mainly Ag_3Sn and a small number of AuSn_4 particles. No Cu_6Sn_5 particles are detected in the matrix as most of the Cu in the SAC alloy could be involved in the IMC reaction.

7.3.3. Failure Analysis of FCB and CPH solder joints after RTC

At the time this report was written, the ATC test was just completed and the samples were not ready for failure analysis. In this section, the solder failures in FCB and CPH assemblies (without underfill) arising from rapid temperature cycling (RTC) test were characterized. The microstructural evolution and the damage mechanism induced by thermal fatigue in the solder joints were investigated.

At the macro-level, the solder joints experienced bending and shear stresses induced by CTE mismatch between the silicon chip and the FR4 substrate during temperature cycling. Several cross-sections of the failed solder joints in the FCB and CPH-165 assemblies were prepared after RTC. The failure modes of FCB and CPH-165 solder joints were similar. The point of crack initiation was usually near the solder and pad interface at the substrate-side. However, the failure damage at microstructural-level is quite different. The FCB solder joints suffer large deformation due to the large

strain sustained by the solder joints without underfill support. The CPH solder joints display relatively smaller deformation as the Cu pillars would have taken part of the plastic strain. After temperature cycles, some recrystallized grains in the FCB solder joints can be seen in Figures 7.16 and 7.17. The damage mechanism is a combination of cracking through the recrystallized grain boundaries and fatigue bending and tearing of the bulk solder material which ultimately fracture the solder joint.

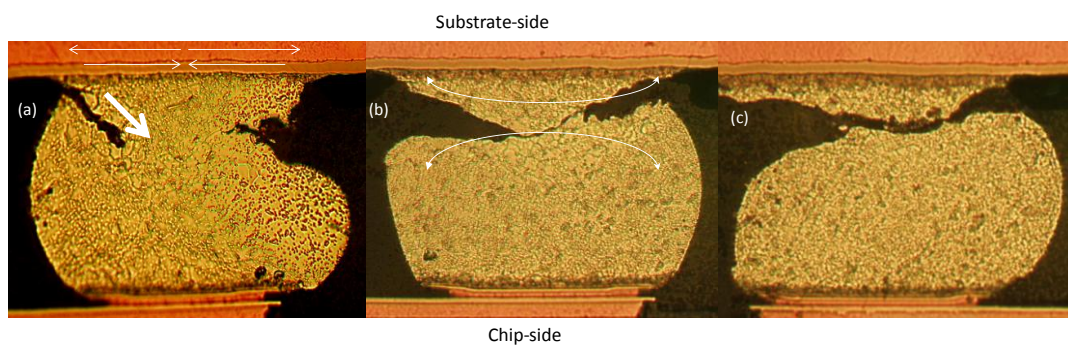


Figure 7.16 Typical FCB solder joint failures found (a) near the centre of chip, (b) & (c) inner rows and corners of the chip

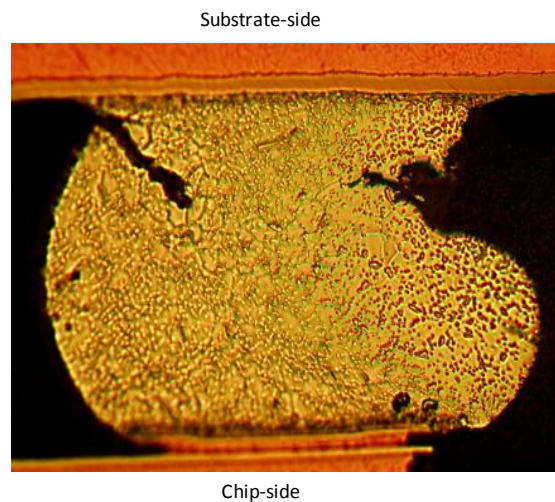


Figure 7.17 A deformed FCB solder joint. Grain recrystallization can be seen ahead of the macro crack path

On the other hand, Figure 7.18 shows that significant recrystallization have occurred in the CPH solder joints which have been subjected to over 650 temperature cycles, that is more than twice the duration of FCB joints.

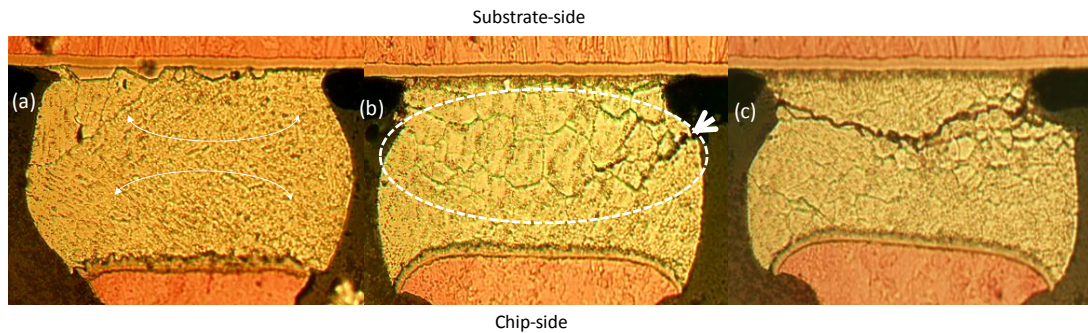


Figure 7.18 Typical CPH-165 solder joint failures found (a) near the centre of chip, (b) & (c) inner rows and corners of the chip. Two large grains can be seen at the top left-hand corner of the solder joint in (a)

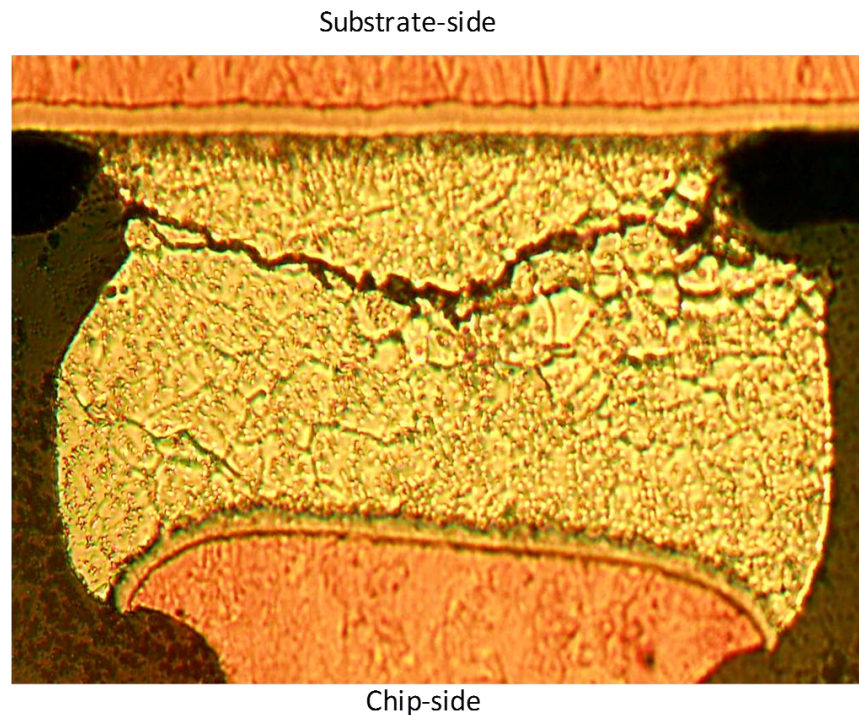


Figure 7.19 A CPH-165 solder joint with significant recrystallization. A transverse crack propagated through the grain boundaries of the recrystallized grains

In Figure 7.18(a), the crack is initiated at the base of the solder joint which is a stress concentrator. The crack grows along the grain boundaries and subsequently travelled through the small-angle grain boundaries that are formed during the recrystallization process until the transverse crack propagates across the solder joint, as shown in Figure 7.19.

The failure observations on FCB and CPH joints indicate that RTC thermal and mechanical loadings in the solder joints can lead to recrystallization and microstructure coarsening in the solder joints. Similar observations were made on Pb-free solder joints subjected to ATC in previous studies (Dunford, 2004). Stress concentration is a source for crack initiation and the recrystallized grain boundaries provide the paths for crack propagation. The recrystallization process produces a number of equiaxed Sn-rich grains which have lesser particle precipitations. It is likely that the Sn-rich grains are softer and the grain boundaries without precipitate strengthening are more prone to crack propagation.

7.4. Electromigration testing of CPH pillar and conventional flip-chip solder joints

7.4.1 Fundamentals of electromigration

Electromigration is characterized by the migration of metal atoms in a conductor in the presence of large current density flow. The atomic displacement and mass transport are in the same direction as the electron flow and this phenomenon requires electrical and thermal energies to provide a driving force and sustain atomic diffusion. The atomic flux is driven towards the anode and a flux of vacancies goes to the cathode in the opposite direction. Below a certain critical length, electromigration will not occur in a conductor (Korhonen, 1993, Lin, 2008). This is due to the gradients

of opposing fluxes from the atoms and vacancies balanced and there will be no depletion at the cathode and pile-up at the anode.

Flip-chip electromigration has been investigated by many researchers (Yeh et al, 2002, Tu, 2003, Xu et al, 2009, Su et al, 2009, Syed et al, 2010). Electromigration failure in solder joints is a growing concern as solder bump diameter reduces in size. It is common for a solder joint in a flip-chip to carry a current of 0.2 A and this may double in the near future. When 0.2 A is supplied to a 120 μm diameter solder bump, the current density is about $2 \times 10^3 \text{ A/cm}^2$. If the solder bump were reduced to 50 μm , the current density would be $1 \times 10^4 \text{ A/cm}^2$. This is found to be the threshold for electromigration to occur in the flip-chip solder joint. The electromigration threshold of solder is two orders of magnitude smaller than that of Cu and Al interconnects. Furthermore, it is found that current crowding at the conducting trace leading into the solder bump could increase the current density at the trace and bump intersection by one order of magnitude (Tu, 2007).

As electromigration is an interaction between the current carrier and the migrating atoms, the atomic flux J_{em} in the solder joint, electron wind force and the mechanical force can affect the motion of the atoms. This relationship can be defined by (Herring, 1950, Tu, 2007):

$$J_{em} = C \frac{D}{kT} Z^* e \check{E} - C \frac{D}{kT} \frac{d\sigma \Omega}{dx} \quad (7.3)$$

where J_{em} is the atomic flux in atoms / $\text{cm}^2 \text{ sec}$, C the concentration of atoms per unit volume, D/kT the atomic mobility, σ the hydrostatic stress in the metal and $d\sigma/dx$ the stress gradient along the direction of the electron flux, Ω the atomic volume, Z^* the effective charge number of electromigration, e the electron charge, $\check{E}$ the electric field and $\check{E} = \rho j$, where ρ is the electrical resistivity and j the current density. The first part

of Eq. 7.3 represents the flux due to electromigration, whereas the second part represents the opposite flux due to back stress.

To analyse electromigration failures of solder, the Black' equation (Black, 1969) for mean-time-to-failure (MTTF) can be adapted:

$$MTTF = A \frac{1}{j^n} \exp \left(\frac{Q}{kT} \right) \quad (7.4)$$

where A is a constant, j the current density of solder joint, n the model parameter of j , Q the activation energy for electromigration, k the Boltzmann constant and T the solder joint temperature. If current crowding and joules heating are considered, Eq. (7.4) can be modified (Tu, 2007):

$$MTTF = A \frac{1}{(cj)^n} \exp \left[\frac{Q}{k(T+\Delta T)} \right] \quad (7.5)$$

where c is due to current crowding and has a typical value of 10 and ΔT is due to joule heating. Adding these two parameters to Black's equation will result in a faster solder joint failure. Since ΔT is influenced by j , Eq. (7.5) will be more sensitive to the change in current density.

7.4.2 Electromigration experimental procedure

The FCB and CPH-135 chips were assembled with underfill for the electromigration (EM) test and their EM reliability performances were investigated. The layout of the daisy-chain test board is shown in Figure 7.20(a). Five chips were tested simultaneously. A DC current of 1.5 A was passed through a single row of 6 solder bumps on each chip. The solder pad was 110 μm in diameter. Hence each solder bump would experience approximately $1.6 \times 10^4 \text{ A/cm}^2$ at the entrance and exit interfaces of the solder joint if current crowding was ignored. The DC current was drawn from a Texio PW16-2ATP power supply and the data monitoring was carried

out with a HP 34970A data acquisition unit. Figures 7.20(b) and (c) show the electron flow path through six daisy-chained solder bumps on the FCB and CPH-135 test chips respectively. Ten FCB chips and ten CPH-135 chips were assembled for EM testing. The assembled boards were loaded into a Memmert Convection Oven where the EM test could be conducted in a controlled ambient environment. A thermocouple was attached to the surface of one chip on each test board to monitor the chip temperature when a 1.5 A DC current was passed through the chips. It was found that the FCB chip surface temperature was approximately 159 °C and the CPH-135 chip surface was 149 °C when the temperature of the convection oven was set at 100 °C. The temperature plots of the oven and test chip temperatures are shown in Figure 7.21. The test parameters of the test chips are summarized in Table 7.7.

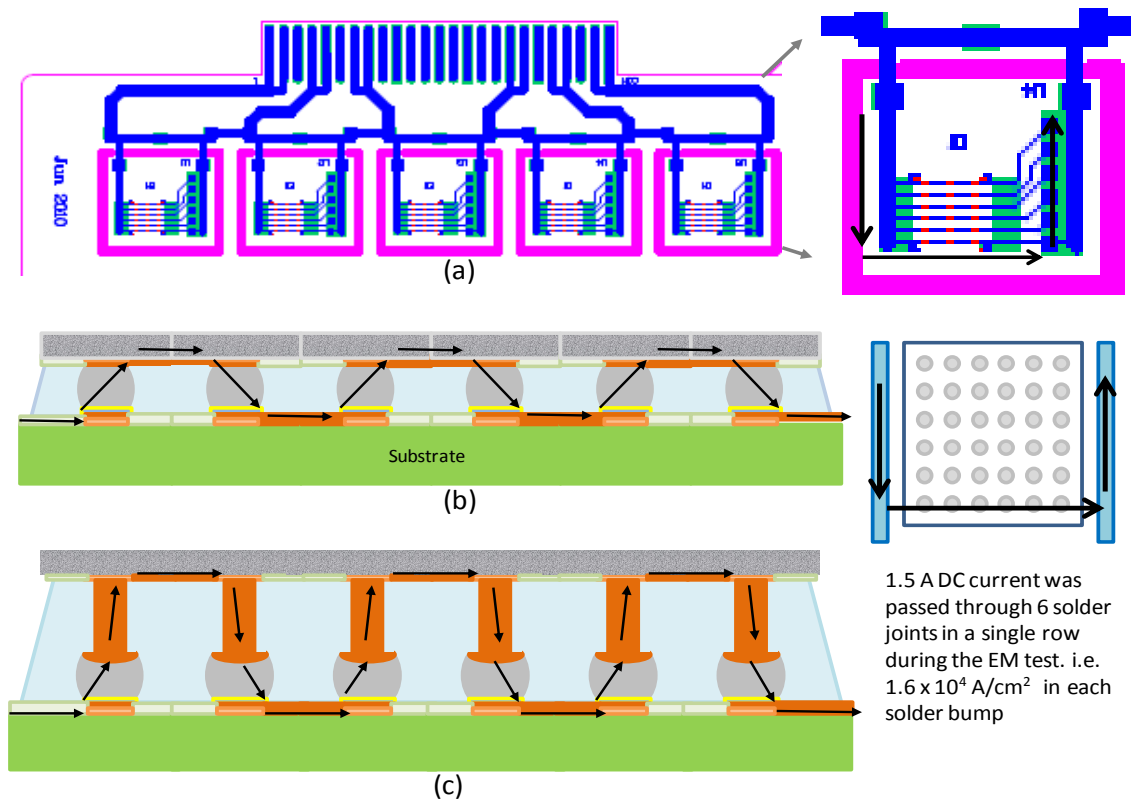


Figure 7.20 (a) A daisy-chain EM test board layout, (b) & (c) show the direction of electron flow through a single row of six daisy-chained solder bumps of a FCB and CPH-135 chip assembly respectively.

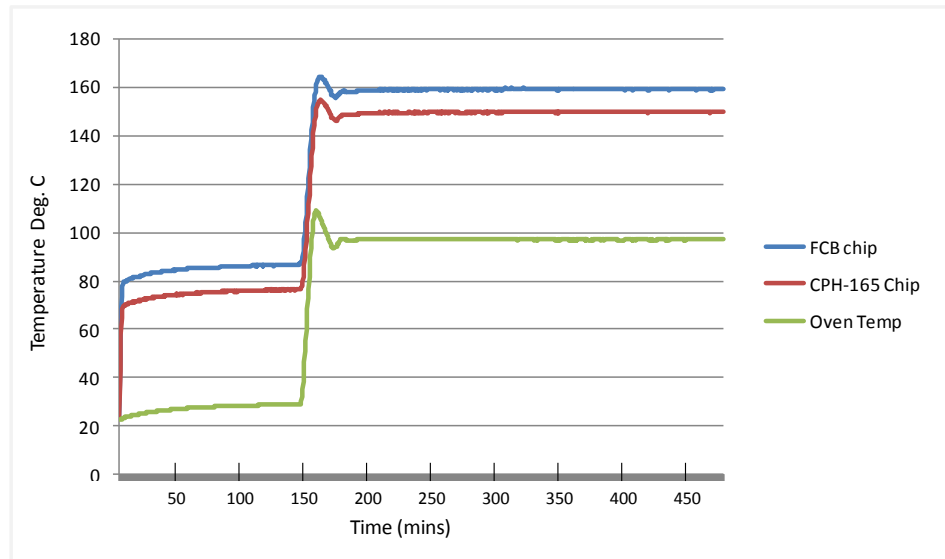


Figure 7.21 Temperature profiles of test chips with 1.5A stress current applied and oven temperature at 100°C

The EM test boards were loading into the oven at 24°C. A 1.5A DC current was applied and the surface temperature on a FCB chip and a CPH chip was monitored for 150 minutes. As shown in Figure 7.21, it is observed that the chip surface temperature of the FCB assembly and CPH assembly rose to 79°C and 89°C respectively, due to Joule heating. When the oven temperature was adjusted to 100°C, the chip surface temperature of the FCB assembly and FCB assembly corresponding increased to 149°C and 159°C respectively.

Table 7.7 Types of test chips assembled for EM test

S/N	Type of Test Chip	Stress Current (DC Amp)	Oven Temp (°C)	Chip surface temperature	Sample Size (chips)
1	FCB: flip-chip attached with 110 μm soldering pads attached with 120 μm diameter SAC bumps	1.5	100	159	10
2	CPH-135: CPH pillars, height 135 μm , pillar diameter 80 μm , pinhead diameter 110 μm , attached with 120 μm diameter SAC bumps	1.5	100	149	10

During the EM test, the first chip to record a 20% resistance change in each batch was removed for analysis. Hence, only 9 chips in each batch would complete the full test. The maximum test duration was set at 500 hours.

7.4.3 Electromigration test results and discussion

Due to the lengthy EM test duration, only one set of test parameters was evaluated in this study. In this EM test, the solder bumps were subjected to a stress current of 1.6×10^4 A/cm² in an ambient temperature of 100 °C maintained within a convection oven. With Joule heating in the chip, the FCB chip surface temperature was elevated to 159 °C, whilst the CPH-135 chip surface was 149 °C. It is apparent that the Cu pillar structures, which have a better thermal conductivity than the solder and triple the stand-off height of a conventional flip-chip interconnect, is able to keep the chips cooler.

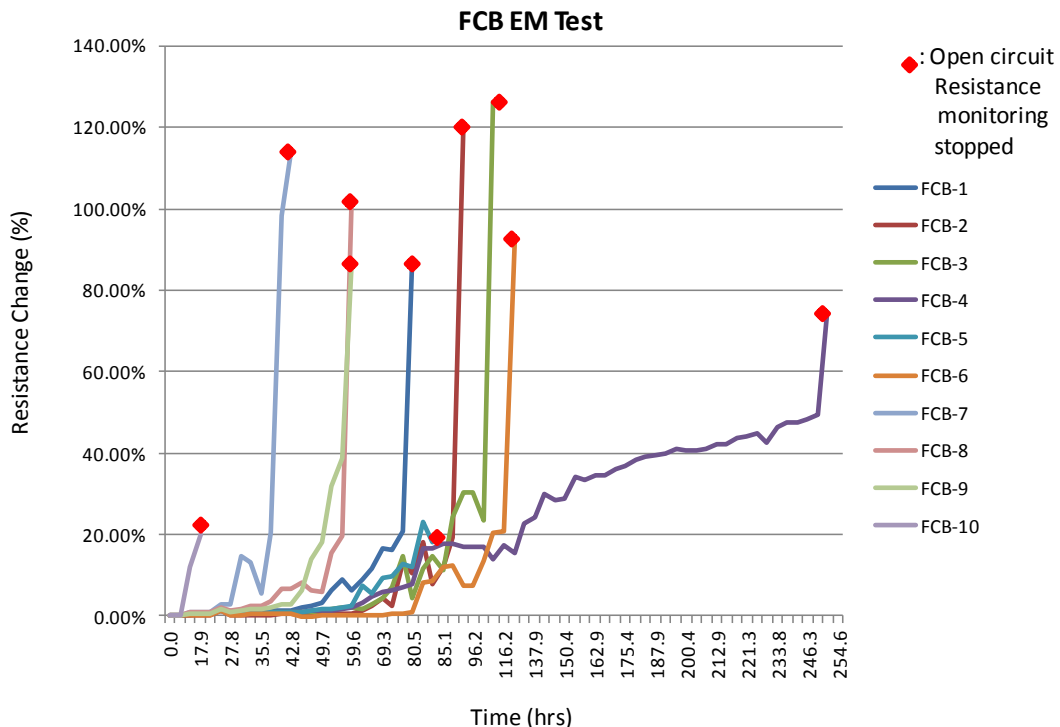


Figure 7.22 The resistance change in the FCB daisy-chained solder joints during EM testing over time leading to open-circuits. (The 1st “open-circuit” was a sample removed for observation when its resistance change reached 20%)

The trend in Figure 7.22 indicates that the FCB solder joints failed very rapidly by open-circuit after they had experienced a resistance change of 10 - 20 %. The failure behaviour of the CPH-135 chips during EM test was found to be different from the FCB chips. There were only 5 open-circuit failures during the entire test duration of 597 hours. It is observed that the solder joints started to fluctuate widely after recording a resistance change of 5 - 10%, as shown in Figure 7.23.

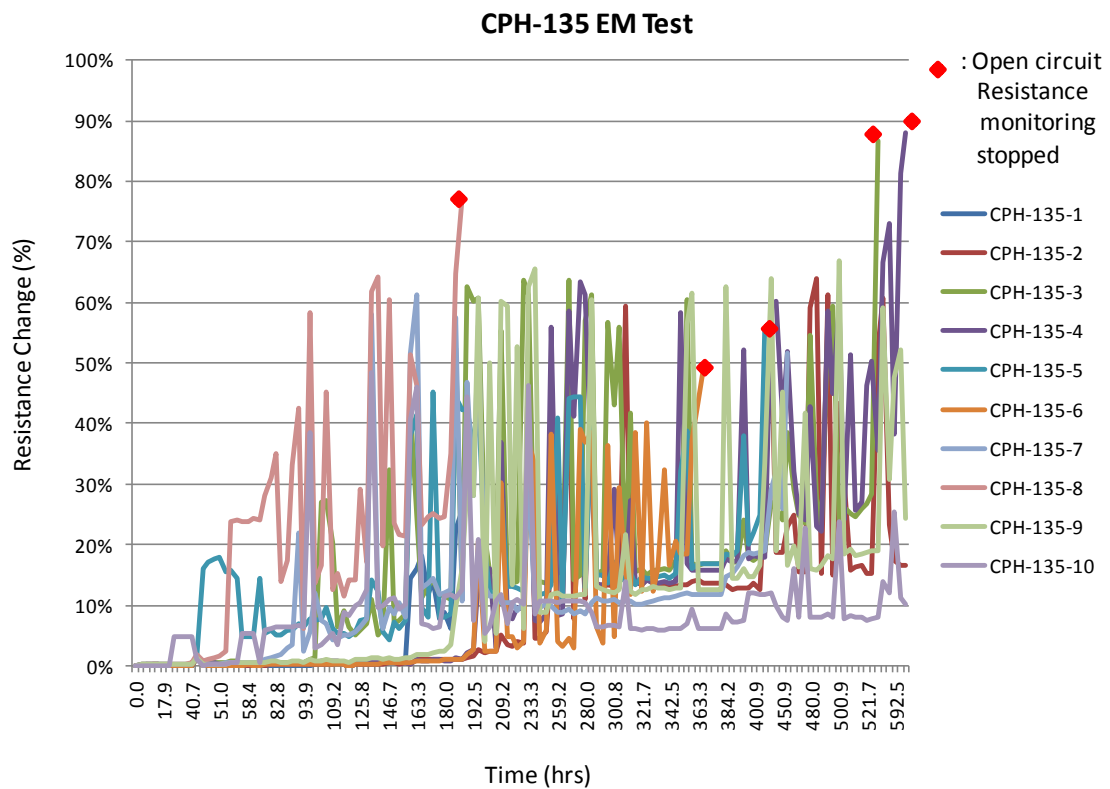


Figure 7.23 The resistance fluctuation in the CPH-135 daisy-chained solder joints after 5-10% resistance change occurred during EM test. 5 solder joints ended with open-circuits. (The 1st “open-circuit” was a sample removed for observation when its resistance change reached 20%)

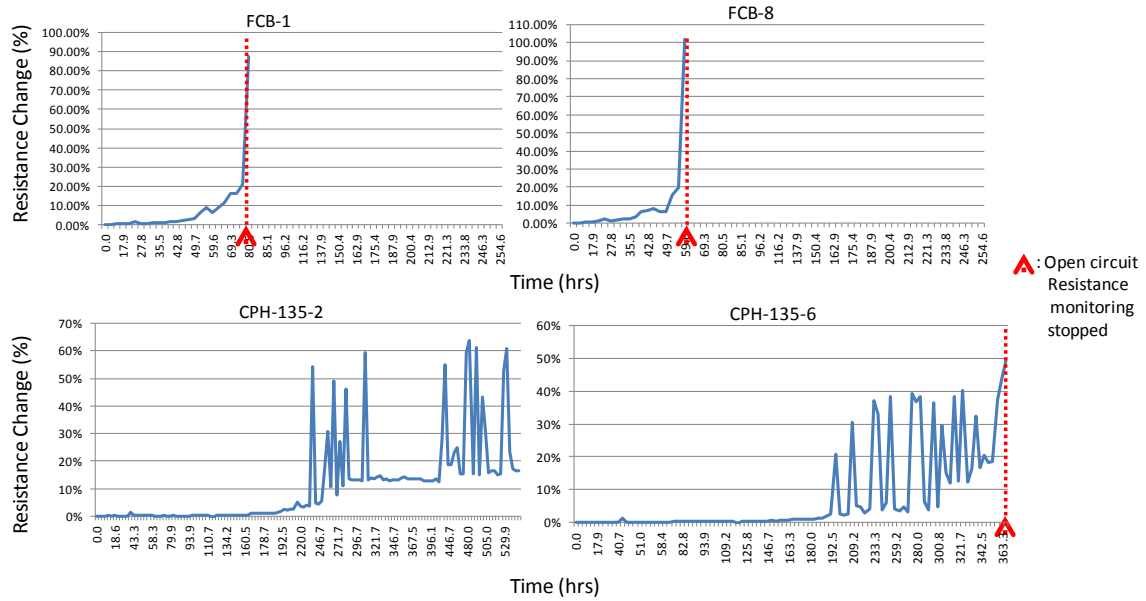


Figure 7.24 Typical FCB solder joints have rapid open-circuit failures after recording a 10-20% resistance change. Typical CPH-135 solder joints have sustained resistance fluctuation after recording a 5-10% resistance change

The failure behaviour is further illustrated by Figure 7.24(a) and (b), where two FCB test chips had open-circuit failures within 10 hours after recording a 20% resistance change. From the EM failure analysis of FCB interconnection in Section 7.4.5, Figure 7.27, it is clear that all the EM failures occur at the chip sides. This could be attributed to the severe current crowding and as the electrons flow from the cathode from the chip side to the anode on the substrate side, the thin layer of UBM would be consumed gradually. As the contact area on the chip side become smaller due to the depletion of the UBM pad, contact resistance increase and current crowding is further aggravated and the rate of UBM diffusion would increase leading to an open-circuit failure in a relatively short time. All the nine FCB chips have open-circuit failures within 255 hours of EM testing.

The resistance of the CPH test chips is typically stable for a longer period before showing changes. After recording 5 - 10 % resistance change, subsequent resistance changes could fluctuate between 50 - 60%. However, the CPH-135 pillar

solder joints did not go into failure rapidly as in FCB solder joints. From the EM failure analysis of the CPH interconnection in Figure 7.28, it is clear that all the EM failures occurred at the substrate side. In the CPH pillar interconnection, the Cu pillar is a robust structure which reduces current crowding at the chip UBM interface and provides better thermal conductivity to the chip. In comparison, the solder interface on the substrate cathode side is weaker and prolonged substrate metallization diffusion would ultimate lead to an open-circuit failure. As the Cu pad on the substrate side is approximately 15 μm thick and 110 μm in diameter, there could be multiple micro sites causing open and short circuitries as the Cu pad diffuses in the EM process. The large resistance fluctuation before failure, observed in CPH interconnect EM test, could be due to the gradual diffusion of the Cu pad and trace in the electromigration process. Five out of nine chips survived the EM test without going into open-circuit failure after 596 hours.

7.4.4 Weibull analysis of electromigration test results

Further analyses on the probability of failure of FCB and CPH-135 chips were carried out using the 2-parameter Weibull plots as shown in Figures 7.25 (a) and (b). Resistance changes at 10% and 20% are used as EM criteria to compare the performances of FCB and CPH-135 solder joints. The reason is that most of the EM failures are observed between these two levels of resistance change. β describes the failure distribution that best fits the data and the characteristic life, η , is the number of cycles to failure at 63.2%.

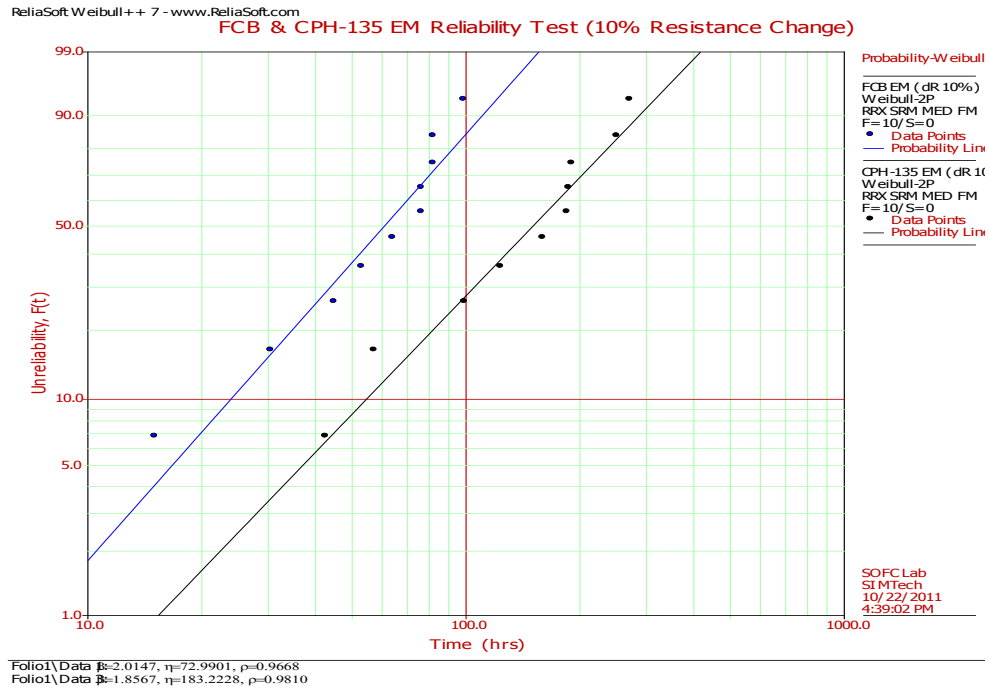


Figure 7.25(a) EM test: 10% Resistance change in FCB and CPH-135 solder joints

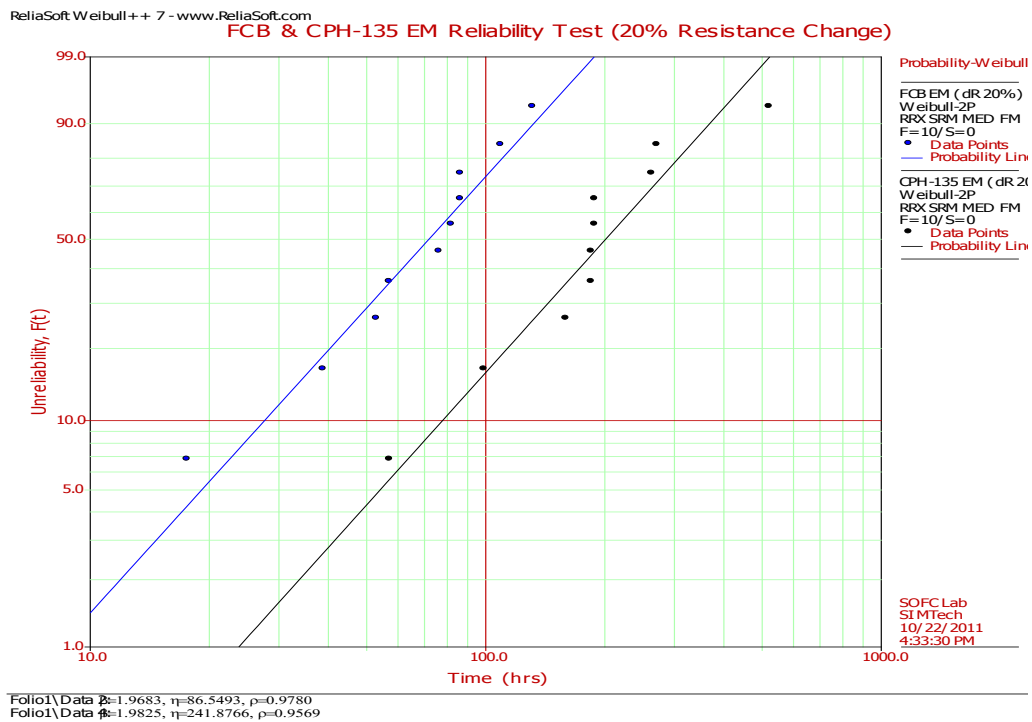


Figure 7.25(b) EM test: 20% Resistance change in FCB and CPH-135 solder joints

The EM test data of the FCB and CPH solder joint EM failures are shown in the Weibull plots in Figures 7.25(a) and (b) and the results are summarized in Table 7.8.

It can be seen that at the point of 63.2% failures, the characteristic lives of the CPH-135 solder joints at 10% and 20% resistance changes were 2.5 to 2.8 times longer than the FCB solder joints. The results support earlier discussion in Chapter 4 that CPH pillar interconnect structure can reduce current crowding at the pillar-solder joint interface and thus, improve solder joint reliability.

Table 7.8 Summary of FCB and CPH solder joint reliability in EM test

S/N	Type of Test Chip	β	η (hrs)
Failure Criterion: 10% resistance change			
1	FCB	2.01	73.0
2	CPH-135	1.86	183.2
Failure Criterion: 20% resistance change			
3	FCB	1.97	86.5
4	CPH-135	1.98	241.9

7.4.5 Microstructural characterization and failure analyses of FCB and CPH solder joints after EM test

The test parameter of 1.6×10^4 A/cm² under 100°C ambient temperature is used to accelerate EM failures in the solder joints (Tu, 2007). The test chips layout is shown in Table 7.6 and Figure 7.20. In this study, microstructural characterization and failure analyses were carried out on the samples which had with open-circuit failures.

- ***EM failure characterization and analyses of FCB solder joints***

Figure 7.26 indicates the electron flow path going from right to left, passing through six FCB solder joints connected in a series daisy-chain. The chip surface temperature was found to be 159°C within a controlled ambient temperature of 100°C. With the Joules

heating in the chip, the solder joints could be experiencing 170°C, assuming the temperature difference between the solder joint and chip surface to be 10°C. The open-circuit failure in this sample occurred within 40 hours. The microstructures of the solder joints show a distinct electromigration pattern where significant metal dissolution took place at the cathode side and IMC piled up at the anode side. This pattern is consistent throughout the three pairs of solder joints, regardless whether the cathode is on the chip side or substrate side. It is observed that the IMC pileup at the chip-side is typically thicker than the substrate side. This is likely due to its IMC made up of $(\text{Ni,Cu})_3\text{Sn}_4$ which is known to be less stable and has a tendency to spall (Zribi et al, 2001).

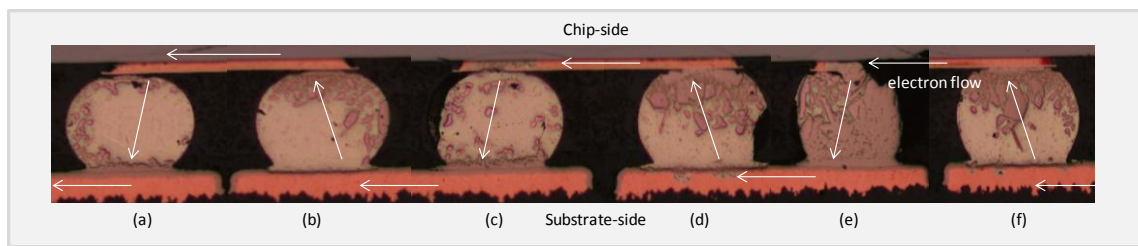


Figure 7.26 Cross-sectional view of FCB solder joints after 40 hours of EM testing at $1.6 \times 10^4 \text{ A/cm}^2$, 100°C ambient temperature

Figure 7.26(e) is an exception where the IMC pileup at the substrate-side is so huge that the entire solder joint is converted to IMC. With further examination, it is found that the trace leading into the chip-side is consumed. It is likely that the electrolytic Ni UBM on the chip has a crack or opening, creating a path for rapid diffusion and consumption of the Cu trace. Under normal circumstances, the Ni UBM would be consumed first and an open-circuit occurs when the solder joint is detached from the Ti-W adhesion layer beneath the UBM layer. Figure 7.27 further illustrates the EM failure mechanism in the FCB solder joints. On the right-hand-side, it can be seen that

the $(\text{Ni,Cu})_3\text{Sn}_4$ IMC and Ni(P) UBM are depleted. The EDX elemental analysis did not show the presence of $(\text{Ni,Cu})_3\text{Sn}_4$ IMC. Only NiSnP and traces of $(\text{Ni,Cu})\text{SnP}$ are detected.

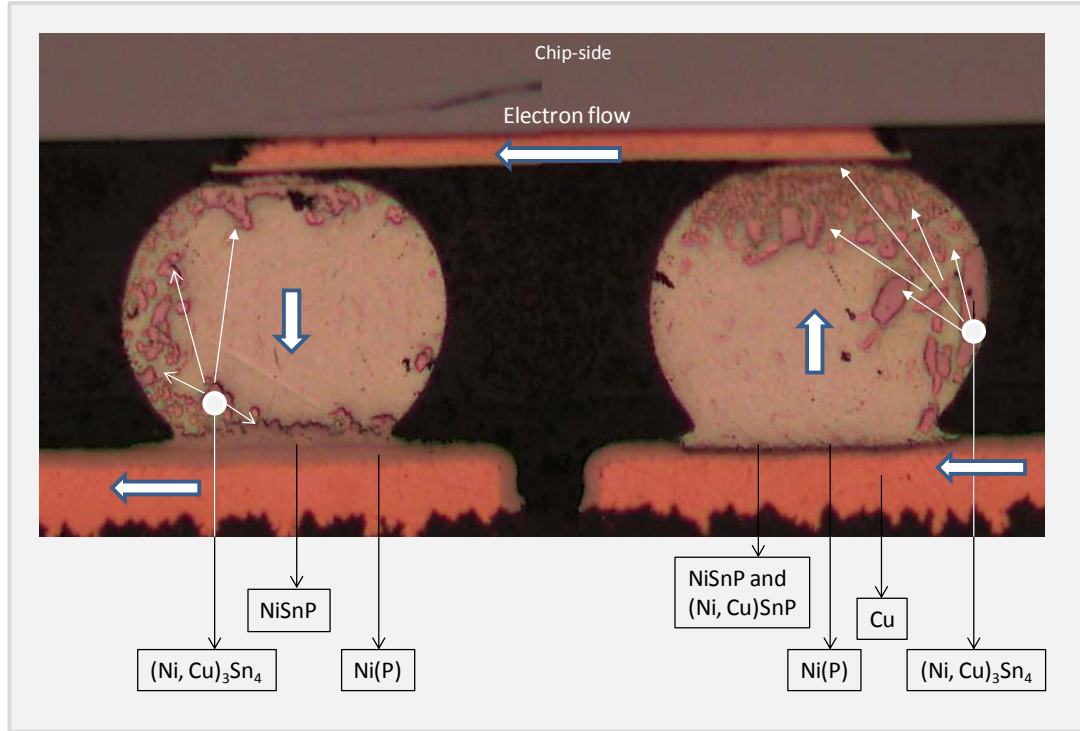


Figure 7.27 Microstructure of a pair of FCB solder joints after 40 hours of EM testing at $1.6 \times 10^4 \text{ A/cm}^2$, 100°C ambient temperature

In our earlier EDX analysis on as-reflowed FCB sample in Figure 7.13(a), a layer $(\text{Ni,Cu})_3\text{Sn}_4$ IMC was clearly present on top of the NiSnP layer. It is obvious most of the $(\text{Ni,Cu})_3\text{Sn}_4$ IMC has spalled off and diffused to the anode. $(\text{Ni,Cu})\text{SnP}$ was not observed before EM testing. The electron flux flowing through the cathode could have pushed some of the Cu atoms to displace some Ni atoms in NiSnP , thus forming $(\text{Ni,Cu})\text{SnP}$. On the left-hand-side of Figure 7.27, the chip-side is the cathode. With current crowding and Joules heating, the rate of Ni dissolution into the solder would increase. It can be seen that the Ni UBM is partially consumed and detached from the chip. The energy from the electron flux moving towards the anode has accelerated the

diffusion rate of Ni and other solute metals to the anode, forming a thick $(\text{Ni,Cu})_3\text{Sn}_4$ IMC.

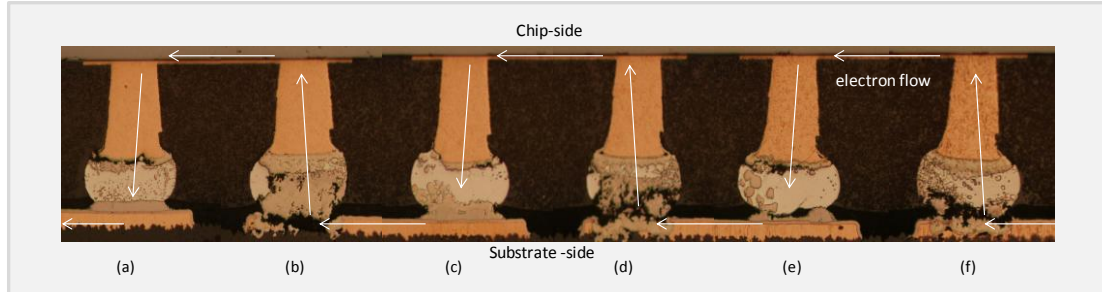


Figure 7.28 Cross-sectional view of CPH-135 solder joints after 162 hours of EM testing at $1.6 \times 10^4 \text{ A/cm}^2$, 100°C ambient temperature

In the CPH solder joints, the mass transport of diffused metals from cathode to anode is similar to that of FCB during EM testing. However, the CPH solder joints sustained a much longer period of current stressing and heating before failure. This is mainly attributed to the Cu pillar structure which reduces the current crowding effect in the solder joint and provides better thermal conductivity to the chip.

Figure 7.28(f) shows evidences that the UBM and IMC layers at the cathodes (substrate-side) are completely depleted, exposing the Cu pad beneath them. Apparently, the amorphous Ni(P) UBM and $(\text{Ni,Cu})_3\text{Sn}_4$ IMC have disintegrated and diffused into the solder matrix under EM stressing. Consequently, the Cu beneath the Ni(P) UBM and $(\text{Ni,Cu})_3\text{Sn}_4$ IMC diffused into the Sn matrix and was transported to the anodes at the chip-side. In some of the solder joints, the Cu pads were almost depleted and large pileups of $(\text{Cu,Ni})_6\text{Sn}_5$ IMCs were formed at the chip-side anodes. Figure 7.29 further illustrates the failure mechanism of the CPH solder joint in EM test. It is likely that the failure of CPH solder joint occurs at the substrate side where the electrons enter the solder joint. This is the point where the dissolution of the IMC,

UBM and Cu pad is most severe. The depletion of the Cu pad would have resulted in an open-circuit. On the other hand, when the electrons flow into the chip side, the solid Cu pillar is much more resilient to EM. The current crowding effect, which probably increases the current density by one order of magnitude at the point of entry, does not cause any significant electromigration in the Cu pillar.

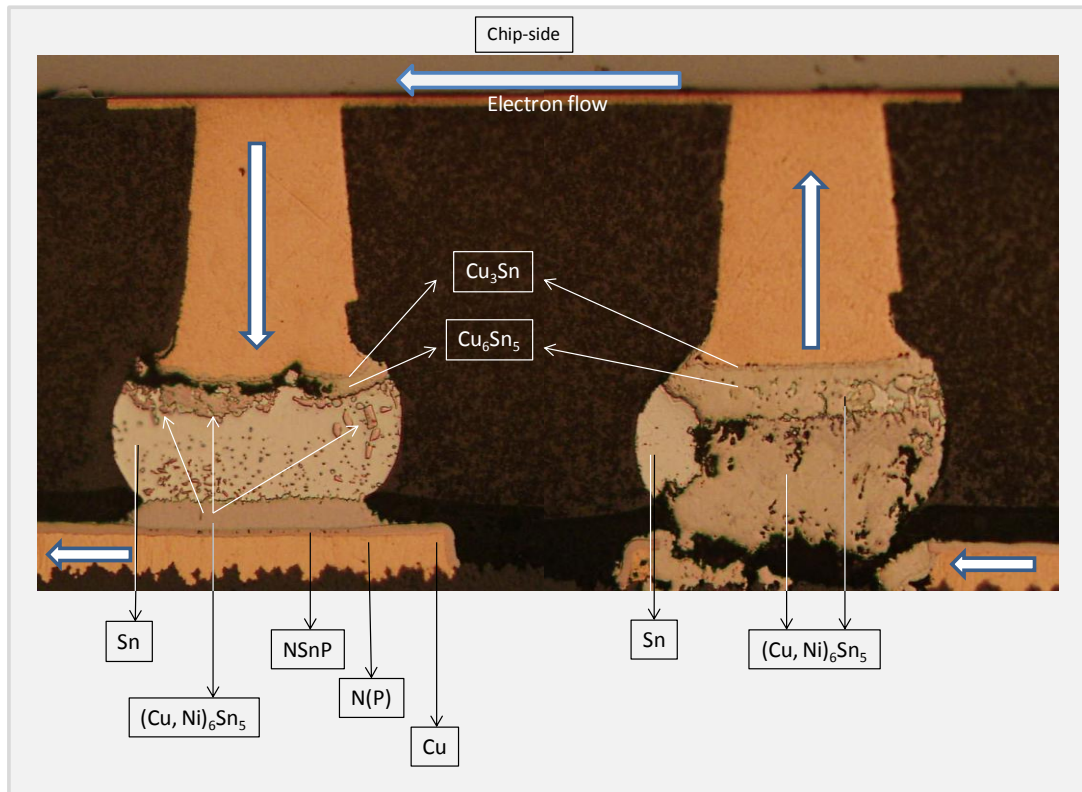


Figure 7.29 Microstructure of a pair of CPH-135 solder joints after 162 hours of EM testing at $1.6 \times 10^4 \text{ A/cm}^2$, 100°C ambient temperature

Subsequently, the electron flow entered the solder joint via the Cu pinhead, the dissolution rates of the UBM and IMC would occur. However, the current crowding effect at the Cu pinhead-solder interface is not as severe as the conventional solder joint-Cu pad interface where the current has to make a right-angle turn at the point of entry. Nonetheless, voids and a macro crack could be seen at the Cu pinhead-solder interface. The composition of the IMC is Cu_6Sn_5 and $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ and the Ni UBM is

completely depleted. A thin layer of Cu_3Sn is detected between the Cu pinhead and the Cu_6Sn_5 layer. The formation of Cu_3Sn has also created voids at the interface with Cu pinhead. As Cu_6Sn_5 decomposes into Cu_3Sn , the two extra Sn atoms have to react with Cu atoms on the Cu pinhead to form more Cu_3Sn . As Cu is consumed, voids would gradually appear in the vicinity. Another observation is that a layer of $(\text{Cu},\text{Ni})_6\text{Sn}_5$ has remained at the chip-side despite the electrons flow toward the anode. This is an evident that $(\text{Cu},\text{Ni})_6\text{Sn}_5$ does not spall off from the interface as easily as $(\text{Ni},\text{Cu})_3\text{Sn}_4$. A thick and compact $(\text{Cu},\text{Ni})_6\text{Sn}_5$ is formed at the anode as a result of Cu and Ni atoms migration from the cathode. Since only $(\text{Cu},\text{Ni})_6\text{Sn}_5$ and no $(\text{Ni},\text{Cu})_3\text{Sn}_4$ IMC is detected, the high Cu content supplied by the CPH pillar might have suppressed the formation of $(\text{Ni},\text{Cu})_3\text{Sn}_4$ IMC.

With the current understanding of the failure mechanisms of FCB and CPH solder joints, the rapid failure trend of FCB solder joints and the wide fluctuation in resistance of the CPH solder joints, see Figure 7.24, can be explained. First, it can be estimated that a solder cube of 100 μm , which is the approximate volume of the solder joint in this study, is about 1 milliohm (Tu, 2007) and the resistance of a Cu line is several ohms. Hence, any damage in the solder joint cannot be detected until it is completely open. This is usually the case in the FCB solder joint during EM testing. The failure mechanism is the gradual dissolution of the UBM until the solder joint is completely detached from the chip. Conversely, in the CPH solder joint, the Cu pad and trace on the substrate are gradually consumed. The Cu atoms diffusion would have caused partial disconnections and re-connections intermittently before the Cu pad was completely disconnected from the solder joint.

7.5. SUMMARY

In this chapter, rapid temperature cycling (RTC) is used successfully to screen the reliability performance of conventional flip-chip (FCB) and Cu pinhead (CPH) pillar solder interconnections. An overall CPH pillar height of 165 μm has significantly enhanced solder joint compliance for the chip assembly without underfill. From the Weibull reliability analysis, the CPH-165-NA solder joints can survive 500 cycles at 0 – 100 °C with 90% probability. Annealing CPH pillars for 30 minutes at 250°C or 325°C marginally improves the characteristic life of the CPH solder joint.

In the ATC test, CPH-165-NA and CPH-165-250 solder joints characteristic lives are 650 and 700 cycles. These are 17% and 12% lower than the same solder joints tested in RTC. The lower characteristic lives in ATC is likely due to the increased creep damage in the solder joints as there is a dwell time of 10 minutes in the ATC test, compared to a 40 second dwell time in RTC test.

In the ATC test, annealed CPH-165-250 pillar solder joints achieve a R(500) reliability of 95% compared to a R(500) reliability of 89% for non-annealed CPH-165-NA solder joints. The results corroborate similar observations made in RTC that annealing can improve CPH pillar compliance.

The main IMC compositions of the FCB solder joint are Ni_3Sn_4 and $(\text{Ni,Cu})_3\text{Sn}_4$ on the chip-side. NiSnP and $(\text{Ni,Cu})_3\text{Sn}_4$ are the main IMC on the substrate-side. CPH solder joints have Cu_6Sn_5 and $(\text{Cu,Ni})_6\text{Sn}_5$ on the chip-side and NiSnP , $(\text{Ni,Cu})_3\text{Sn}_4$ and $(\text{Cu,Ni})_6\text{Sn}_5$ on the substrate-side. The chip UBM is electrolytic Ni and substrate pad metallization is Ni(P) .

The damage in the FCB and CPH solder joints were initiated from recrystallization and microstructure coarsening, which led to voiding and micro-cracking. Crack propagation is aggravated by the bending and shear stresses induced

by CTE mismatch between the silicon chip and FR4 substrate. In the CPH solder joint failure, a transverse crack propagates along the grain boundaries of the recrystallized grains in the solder joint. The solder joint failures in FCB assembly is a combination of cracking along recrystallized grain boundaries and solder tearing.

When subjected to current density loading of $1.6 \times 10^4 \text{ A/cm}^2$ and heating at 100°C ambient temperature, the FCB test chip and CPH test chip surface temperatures were 159°C and 149°C respectively. The higher chip surface temperatures were due to Joules heating within the test chips. FCB solder joints have rapid open-circuit failures, with the first failure recorded after 40 hours of EM test and all the nine test chips failed within 255 hours. The failure mode is determined to be Ni UBM and IMC dissolution and depletion, and finally solder joint detachment from the chip. CPH solder joints can survive much longer in the EM test. The first solder failure occurred after 191 hours and five out of nine test chips did not have open-circuit failure at the end of test after 596 hours. The failure mode of CPH solder joint is determined to be on the substrate-side. The failures occur after complete dissolution of the UBM and IMC layers, followed by the depletion of the Cu pad which lead to an open-circuit. The EM test reveals that the geometries of the chip UBM and substrate pad metallization have significant influence on EM reliability.

CHAPTER 8 Conclusions and Recommendations for Future Works

8.1 Conclusions

8.1.1 Literature review of compliant interconnection systems

In the literature review, thirteen different interconnect structures were analyzed. They are broadly categorized as stacked or stretched solder bump, spring-type and Cu pillar bump interconnects. For the solder bump category, the high homologous temperature that the solder interconnect structure experiences when exposed to the typical operating environment for electronic products would be a reliability concern. Compliant solder bump interconnections have high stress concentration areas and UBM dissolution is a concern as in the conventional solder interconnection. The spring-type interconnect structures could potentially be designed with excellent compliance. However, manufacturing scalability is uncertain due to their complex manufacturing steps. The conventional Cu pillar bump has the greatest potential to meet the requirements for high performance electronic interconnection. The appeal of Cu pillar is its simplicity in design, manufacturability and compatibility with Pb-free solder. Despite its inherent advantages, there were reported concerns on low-k dielectric interlayer delamination caused by high stresses induced by the rigid Cu pillar at the chip interface. The underfilling process continues to be an essential step to ensure solder joint reliability in all the proposed interconnection systems today. In this thesis, a Cu pinhead pillar (CPH) structure with enhanced compliance is proposed. Flip-chip assembly using CPH pillars can be accomplished without underfill.

8.1.2 Investigation of Sn-Ag-Cu solder and Ni-Au UBM interfacial reaction

The integrity and compatibility of the silicon chip UBM layer with the Sn-Ag-Cu solder is critical in any interconnection. The UBM is a barrier layer to protect the chip from any metal diffusion from the solder and also serves as a soldering interface. In this study, the influence of volume-to-area (V/A) ratio of solder and pad metallization on IMC formation and UBM dissolution was investigated. The results show that a thinner and more fragmented IMC is formed during SAC solder –NiAu UBM interfacial reaction when the V/A ratio of solder volume to pad area is 111. With a lower V/A ratio of 70, a thicker and better defined IMC is formed. The EDX analyses indicate that two IMC layers are formed. IMC I, $(\text{Cu,Ni})_6\text{Sn}_5$, interfaced with the solder, and IMC II $(\text{Ni,Cu})_3\text{Sn}_4$ interfaced with the Ni UBM. The UBM dissolution rate is found to increase when V/A ratio increases. The solder interfacial reaction results of 40, 80 and 250 μm diameter solder bumps indicate that an initial Ni UBM thickness of 2 μm should be sufficient to meet the demand of Pb-free solder bumping and up to six reflow exposures. At least 1 μm thick of Ni UBM remained after 500 hours of isothermal aging and the dissolution rate of Ni is found to decrease over time.

8.1.3 Conceptual design of a Cu pinhead pillar bump structure

A novel Cu pinhead (CPH) pillar-to-solder interconnection system is developed for flip-chip assembly. The CPH pillar structure is configured as a Cu pillar with pinhead serving as an extended pad away from the chip. The CPH pillar interconnection is developed as an improvement over the conventional Cu pillar interconnection. The compliance of the CPH pillar can be tuned independently by changing the diameter or height of the Cu pillar without affecting the geometry of the pinhead pad. The CPH pillar could provide sufficient compliance to the solder joint to eliminate the need for underfill. The CPH pillar is suitable for interconnecting first and

second level electronics components, and multi-stack components on a substrate. The UBM is deposited on the pinhead and bumping can be carried out without direct contact with the chip.

A parametric study was conducted using FEM to benchmark the reliability of the CPH pillar-solder joint reliability with those of conventional flip-chip and Cu pillar-solder joints. The results indicate that the strain levels in the CPH pillar solder joints are much lower, confirming the enhanced compliant feature is effective. The strain relieving effect on the solder joint is due to the bending and deformation of the Cu pillar. The FEM results reveal that the CPH pillar fatigue life is longer than that of the solder joint. Thus, the solder joint would fail before the CPH pillar. The predicted fatigue life of the CPH pillar-solder joint is 443 cycles after temperature cycling between 0 – 100 °C. This is close to the expected 500 cycles required of most consumer electronics. Under the same condition, the conventional flip-chip and Cu pillar solder joints can survive 203 and 293 cycles respectively.

8.1.4 Fabrication of Cu pinhead pillars

CPH pillars on silicon wafers were fabricated successfully using a through-mask process which was ideal for plating free-standing structures. In the fabrication process, thick resist coatings in the range of 40 to 150 μm were required as plating masks for Cu pillar electroplating. Novolak-based positive photoresist was used to produce plating masks of 15 to 45 μm thickness using multi-step spin coating. The aspect ratio (AR) of plating mask opening is determined by the thickness of the photoresist thickness and the diameter of the desired via opening. In this study, for a 40 μm diameter via opening, an AR of 1.0 is achievable with good plating yield. An AR of 2.0 would require at least 2 plating masks and a 2-step plating process. An AR of 2.5 would need 3 plating masks and a 3-step plating process. However, the plating

yields were not acceptable in the processes developed for AR 2.0 and 2.5. The plating defects were mainly caused by photoresist residues in the cavities of the vias. With further process evaluations, plating masks with 80 μm openings on 45 μm thick photoresist could be produced with good repeatability. CPH pillars with overall height of 55 μm could be fabricated with 90% yield in a 1-step plating process. Subsequent 2-, 3- and 4-step plating using 80 μm openings on 45 μm thick plating mask could fabricate CPH pillars with good repeatability. Each plating step plate could plate between 15 to 45 μm of the Cu pillars, depending on the thickness of the plating mask. The optimized electroplating current is found to be 300 mA, with a Cu deposition rate of 1.3 $\mu\text{m}/\text{min}$. CPH pillar structures with 80 μm pillar diameter, 165 μm overall height and 110 μm pinhead diameter are successfully fabricated with a 4-step plating process.

8.1.5 Characterization of annealed and non-annealed Cu pinhead pillar bumps

CPH pillars annealing was carried out before solder bumping, with the aim to increase their ductility and compliance. Shear test results show that the shear strength of CPH pillars decrease 5 to 13% when annealed at 325 to 400 $^{\circ}\text{C}$ for 30 minutes. The CPH pillars show insignificant shear strength change at 250 $^{\circ}\text{C}$. Progressive microstructural changes and grain growth were observed. There is a reduction of 9 to 16 % in hardness and 24 to 28 % in elastic modulus after the CPH pillars were annealed.

Nanoindentation tests indicate that the multi-step electroplated CPH pillars have homogeneous hardness and elastic modulus. No cracks or fault lines are observed at the plating interfaces in the samples cross-sectioned by FIB, thus confirming that the plating process is robust and repeatable. XRD determines that the most preferred crystallographic orientation in the CPH pillars is [111].

8.1.6 Reliability assessment of Cu pinhead pillar and flip-chip solder bump assemblies

The CPH pillar, with a diameter of 80 μm and a height of 165 μm , is found to have significantly better solder joint reliability than the conventional flip-chip solder joint. From the Weibull reliability analysis, the CPH solder joints could survive 500 cycles at 0 – 100 °C with 90% reliability. And under similar conditions, conventional flip-chip solder joints could only 500 cycles with 22% reliability. RTC and ATC results show that annealing CPH pillars for 30 minutes at 250 to 325 °C could improve the characteristic life of the CPH solder joints. The damage in the FCB and CPH solder joints during RTC are initiated from grain recrystallization and microstructure coarsening, which lead to voiding and micro-cracking.

When stressed by a current density of $1.6 \times 10^4 \text{ A/cm}^2$ in 100°C ambient temperature, CPH pillar solder interconnection performed significantly better than FCB solder joints. Using resistance changes of 10% and 20% as the failure criteria, the CPH-135 pillar solder interconnect characteristic lives are found to be 2.5 to 2.8 times better than that of the FCB solder interconnection.

8.2 Major contributions of this research work

- The flip-chip composite interconnection system comprising of CPH pillars and solder bumps enables flip-chip assemblies to be carried out without underfill. The reliability performance of flip-chip assemblies with compliant CPH pillar interconnects can satisfy the consumer electronics qualifying criterion of 500 cycles in the 0 to 100 °C temperature cycling test.
- The pinhead structure on the CPH pillar has an extended pad configuration which eliminates several reliability concerns in conventional flip-chip and Cu pillar interconnection. With the pinhead positioned away from the silicon chip,

any metal diffusion into the chip is avoided. The role of UBM on the pinhead is less critical as the Cu pinhead can be a wetting surface. Depletion of UBM on the pinhead will not lead to solder joint failure.

- The CPH pillar height and diameter can be changed and its compliance adjusted, without changing the soldering pad footprint on the substrate as only the Cu pinhead serves as a soldering interface. The ability to maintain a constant solder interface while the CPH pillar structure can be changed will render tremendous design flexibility to packaging engineers.
- The multi-step electroplating process allows Cu structures with an aspect ratio of two to be fabricated. The plated structures have homogenous mechanical properties and are proven to be robust and reliable, with no voids, cracks or fault lines at the plating interfaces.
- The elevated temperature annealing process has been used to improve the CPH pillar compliance. CPH pillar annealing at 250°C for 30 minutes is recommended for most applications as most electronic devices designed for Pb-free solder reflow will be able to tolerate this temperature exposure. This novel approach of improving Cu pillars before solder bumping has not been reported previously.
- The CPH pillar interconnection system has demonstrated significantly better EM reliability as compared to the conventional flip-chip interconnection. The EM findings have highlighted that catastrophic failures may not necessarily be due to UBM depletion and solder material migration which finally lead to voiding and transverse cracking of solder joints. The EM failures in CPH interconnections are linked to pad metallization and Cu trace depletion, and finally open-circuit failures.

8.3 Recommendations for future research

- A more comprehensive study on the pillar height/pillar diameter aspect ratio is needed to correlate the fatigue life of solder joints with CPH pillar aspect ratio changes. With the current state-of-the-art plating capability in the industry, a CPH pillar aspect ratio of 3.0 – 4.0 is feasible. If higher aspect ratio CPH pillars were used as compliant interconnects for flip-chip assembly without underfill, the process can potentially meet a more stringent industry temperature cycling qualifying test criterion of 1000 cycles in -40 to 125 °C.
- More extensive temperature cycling testing and failure analyses for assembly with and without underfill are necessary for the failure mechanisms to be better understood. Additional testing under high temperature storage, high temperature and humidity are needed to characterize the behaviour of the CPH pillar-solder interconnection system.
- The present annealing study at 250 °C shows that the reliability of CPH pillar-solder interconnection, at 500 cycles in 0-100 °C temperature cycling, can improve from 89% to 95%. Further research on CPH pillar annealing will significantly enhance the present knowledge on how Cu pillar recrystallization and grain growth can influence the interconnection reliability performance.
- It is observed that all the CPH pillar interconnection failures during temperature cycling test are within the solder joints. If this weak link can be circumvented using direct Cu to Cu bonding, the reliability of the CPH interconnection will be enhanced significantly. Alternatively, CPH pillars with Ni-Au UBM can be bonded with Au-Sn eutectic solder at approximately 320 °C to form (Au,Ni)Sn IMC. In these alternative bonding processes, a flat-top pinhead will be desirable and this can be fabricated with an additional plating step or by planarization.

- The application of Black's Equation on EM time-to-failure needs to be re-considered as the equation assumes metal migration, voiding and cracking as the failure mode. From the EM failure observations in the CPH pillar interconnections, the evidences indicate that the failures are not due to a single failure mechanism but a series of failure mechanisms that are linked to UBM, solder, Cu pad and Cu traces. New design rules for traces and pads will be needed to complement the robust EM performance of CPH pillar-solder interconnection.

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