Design and Analysis of Amplitude and Phase Tunable VCO for ISM Band Application

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Abstract

Oscillators are an integral part of many electronic systems. With rapid development in the area of Radio Frequency (RF) and wireless communication, the interest in oscillator which generates Local Oscillator (LO) signal has grown rapidly in the last few years. The LO signal is required to down-convert the RF signal to a lower Intermediate Frequency (IF) signal, or vice versa. For typical RF application, LC Voltage-Controlled Oscillator (VCO) is used. It is essential to tune the VCO for an optimized performance due to two reasons. Firstly, the phase noise of the VCO has great effect on the selectivity of the receiver. Secondly, VCO is one of the most power hungry blocks of the transceiver. Hence the power consumption of the transceiver can be reduced significantly by optimizing that of the VCO. Moreover, for transceivers that implement quadrature modulation/demodulation scheme, the phase error and amplitude error of the LO signal can affect the function of the overall performance significantly. With the development and popularity of Wireless Local Area Network (WLAN) and Personal Area Networks (PANs) which operates in the Industrial, Scientific and Medical (ISM) band, it is essential to design VCO with optimized performance for ISM band application.

In this thesis, the aim is to explore the VCO's tuning method, both differential and quadrature, to optimize the overall performance. Firstly, a fully integrated hybrid type Automatic Amplitude Calibration (AAC) VCO has been designed and fabricated in 0.18 μm CMOS technology. The operation of the whole loop and the state-dependent nature is analyzed followed by the analysis of important blocks. Based on these analyses, a quantitative transient analysis

for the whole loop is performed. A systematic design procedure is proposed according to the relationship explored in the quantitative transient analysis. Secondly, in order to satisfy the need for quadratuer signal generation with good phase noise and phase error performance, a novel in-phase coupling scheme is proposed. The principle of this in-phase coupling scheme is analyzed first, followed by the analysis for possible sources of phase error. Based on this analysis, two novel schemes for phase error tuning are proposed.

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Table of Acronyms

AAC	automatic amplitude calibration
BGC	back gate coupled
CMRR	common mode rejection ratio
CP	charge pump
CPLL	charge- pump phase-locked loop
DAC	digital-to-analog convertor
DSP	digital signal processing
ESD	electrostatic discharge
E-TSPC	extended true-single-phase-clock
FoM	figure of merit
FSM	finite state machine
IF	intermediate frequency
ILFD	injection-locked frequency divider
IPC	in-phase coupled
IRR	image rejection ratio
ISF	impulse sensitivity function
ISM	industrial, scientific and medical
LO	local oscillator
LTI	linear time invariant
LTV	linear time variant
PAN	personal area network
PD	peak detector
PLL	phase-locked loop

PQVCO	parallel quadrature voltage-controlled oscillator
QVCO	quadrature voltage-controlled oscillator
RF	radio frequency
SHC	super-harmonic-coupled
SNR	signal-to-noise ratio
SQVCO	series quadrature voltage-controlled oscillator
TSPC	true-single-phase-clock
VCO	voltage-controlled oscillator
WLAN	wireless local area network

List of Symbols

ω	angular velocity
f	frequency
G_m:	transconductance
k:	Boltzman's constant, or a variable
$\mathcal{L}\{\Delta\omega\}$:	phase noise at an offset frequency $\Delta\omega$
m:	coupling factor
T:	absolute temperature
Q:	quality factor
θ:	instantaneous phase;
$\emptyset_B$:	the built-in potential of the *pn* junction
γ:	the noise factor of a single FET
Γ:	Impulse sensitivity function
α:	angle which is equal to half of the conduction angle
φ:	phase error

CHAPTER 1

Introduction

1.1 Motivation

An oscillator generates a periodic output with a certain frequency and is found in many test and measurement equipments, as well as in communication equipments. In most RF application, the frequency of the oscillator's output should be adjustable. Normally this output frequency is controlled by voltage and such oscillator is called VCO.

In a transceiver design, there is a clear trend towards full integration of the RF front-end on a single die for low cost and low power consumption. The design of RF building blocks in a CMOS technology is now an important research topic in order to replace the more expensive bipolar technology. Although CMOS technology suffers from inferior device physics, continued investment on a large scale has increased its suitability for high frequency applications [1]. Another noteworthy advantage is the large number of interconnect layers now commonly available in CMOS RF/analog/logic processes and this leads to more compact designs. Therefore, a deep sub-micrometer CMOS technology can be used to incorporate the RF circuits with the baseband circuits on the same chip. Fully integrated CMOS RF building blocks are crucial and have been widely explored [2][3].

Over the last decade, the tremendous growth of the WLAN and PAN application markets has created an increasing demand for high-performance RF circuits for ISM band application in low-cost technologies, including smaller

size, lower power consumption hence longer battery life. As the "on the move with anyone, anytime, and anywhere" era becomes a reality, portability becomes an essential feature of the electronic systems that emphasize the efficient use of energy as a major design objective. Hence it is desirable to design tunable circuits to optimize the overall performance for ISM band application.

Currently, VCO's design is still one of the most challenging tasks in RF systems design as it must meet very stringent requirement such as phase noise, power consumption and tuning range simultaneously. During design process, trade-off is always required between these parameters. Thus to summarize the overall performance of the VCO, Figure of Merit (FoM) that is introduced in Chapter 2 is often used. The performance of the VCO is essential for the RF system for the following reasons. Firstly, the phase noise of the VCO has great effect on the selectivity of the receiver. Secondly, VCO is one of the most power hungry blocks of the transceiver and hence the power consumption of the transceiver can be reduced significantly by having a low power VCO. Moreover, for transceivers that implement quadrature modulation/demodulation scheme, the phase error and amplitude error of the LO signal can affect the function of the overall performance significantly. Hence it is essential to tune the VCO to achieve an optimized performance.

1.2 Objectives

In this thesis, the aim is to explore the tuning method for VCO, both differential and quadrature, to optimize the overall performance. To start with,

the relationship between the amplitude and the performance of the differential VCO is studied, followed by the principle of quadrature signal generation. It is notable that besides phase noise, phase error accuracy performance is also critical to quadrature VCO (QVCO) as mentioned above. In addition, it is also notable that coupling schemes for QVCO affect the phase noise and phase accuracy performance. Hence for differential VCO the research is focused on tuning the output amplitude to an optimized level while for QVCO the research is focused on topology with good performance in term of phase noise and phase error as well as phase error tuning scheme.

Amplitude calibration scheme of differential LC VCO has been proposed in different manners, such as analog approach [4] and digital approach [5]. However, while enjoying their own advantages, amplitude calibration schemes proposed so far have introduced different problems, such as high power consumption of the calibration circuitry, extra noise and stability. The goal of the research in this thesis on amplitude calibration is to proposed an automatic amplitude calibration scheme with low power consumption, low extra noise introduced and high stability.

Phase error tuning schemes for QVCO have been proposed in [6] and [7]. However, source of phase error and their mechanism varies between different QVCO topologies. Hence the phase error tuning scheme proposed in [6] and [7] is only suitable for their specified QVCO topology. In this thesis, research works starts with exploring QVCO topology that can achieve low phase noise and low phase error. Based on this novel QVCO topology, research is then focused on achieving phase error tuning scheme with low power, small extra area and number of components with wide phase error tuning range.

1.3 Major Contributions of the Thesis

In this thesis, the aim is to explore the tuning method for VCO, both differential and quadrature, to optimize the overall performance.

Firstly, a fully integrated hybrid type AAC VCO targeted for ISM application has been designed and fabricated in 0.18 μm CMOS technology. The operation of the whole loop and the state-dependent nature is analyzed, followed by the analysis of important blocks. Based on these analyses, a quantitative transient analysis for the whole loop is performed. A systematic design procedure is proposed according to the relationship explored in the quantitative transient analysis. Measurement results for this AAC VCO are shown in Table 1.1 below.

Table 1.1: The performance of the proposed AAC VCO

Tech (μm)	f_0 (GHz)	TR (%)	V_{dd} (V)	Power (mW)	Phase noise (dBc/Hz)	FoM (dBc)
0.18	2.4	13	1.8	4.5*	-97@10 kHz	189

$$\text{FoM} = -\mathcal{L}\{\Delta\omega\} + 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log(Power_{mW})$$

*0.8 mW consumed by the calibration circuit.

Secondly, an in-phase coupling scheme for quadrature signal generation is proposed. The principle of the in-phase coupling scheme is analyzed first, followed by the analysis for possible sources of phase error. The proposed coupling circuitry consumes less than 2% of the total power consumed by the QVCO. The proposed In-Phase Coupled (IPC) QVCO (Design A) is fabricated in 0.18 μm CMOS technology. Based on the analysis for possible sources of

phase error mentioned above, two novel schemes for phase error tuning are proposed. The first one is based on conventional differential Complementary VCO (Design B) and the second one is based on Class-C type LC VCO (Design C). Both have been designed in 0.18 μm CMOS technology. Measurement and post-layout simulation results of Design A, B and C are shown in Table 1.2

Table 1.2: The performance of the proposed QVCOs

	Design A	Design B*	Design C
Tech (μm)	0.18	0.18	0.18
f_0 (GHz)	2.7	2.7	2.7
Turning Range (%)	13.3	13.3	15.6
V_{dd} (V)	1.8	1.8	1.2
Power (mW)	4.3	4.1	3.6
Phase noise (dBc /Hz)	122@1 MHz	123@1 MHz	127@1 MHz
Phase Error (°)	0.1	0.6	0.5
Phase Error Tuning Range (°)	N.A.	11	17
FoM (dBc)	184	185	190

* : Post-layout simulation result

1.4 Organization of the Thesis

This thesis is organized into six chapters. In Chapter 1, the motivation, objective and contributions of the thesis are introduced, followed by an outline of the thesis. Chapter 2 provides an overview of basic concepts of VCO. Both the principle and the topology of LC VCO are studied. The performances of the LC VCO, such as phase noise and amplitude variation, are then discussed. Subsequently, several approaches to improve the performance of the LC VCO

are reviewed. AAC loop that calibrates the VCO's output amplitude automatically are then introduced. The two major conventional AAC types, namely the analog type AAC and the digital type AAC, are discussed. Both their advantages and disadvantages are reviewed. In Chapter 3, the fundamental of the quadrature signal is introduced. Advantages and disadvantages of different quadrature signal generation methods are studied and then two approaches are focused on, namely the polyphase filter and QVCO. A novel derivation for the transfer function of the 1st order and higher order polyphase filter based on basic Kirchhoff's law is presented. Based on this transfer function, condition for quadrature signal generation by polyphase filter is thus determined. Furthermore, phase/amplitude error due to mismatch between elements are analyzed according to the transfer function derived and then verified through simulation. Furthermore, QVCO circuit for quadrature signal generation is also studied in detail. Different coupling methods for QVCO are reviewed with their advantages and disadvantages. Based on these analyses, phase tuning schemes for different I/Q signal generation methods are discussed

In Chapter 4 a fully integrated hybrid type AAC VCO targeted for ISM application has been designed and fabricated in 0.18 μm CMOS technology. The operation of the whole loop and the state-dependent nature is analyzed, followed by the analysis of important blocks. Based on this analysis, a quantitative transient analysis for the whole loop is performed. A systematic design procedure is proposed according to the relationship explored in the quantitative transient analysis. The proposed AAC VCO is implemented and the measurement results are shown.

In Chapter 5, a novel in-phase coupling scheme for quadrature signal

generation is proposed. The principle of the in-phase coupling scheme is analyzed first, followed by the analysis for possible sources of phase error. Based on this analysis, two novel schemes for phase error tuning are proposed. All the circuits proposed are implemented in 0.18 μm CMOS technology and post-layout simulation/measurement results are shown.

Finally, the thesis conclusions are given in Chapter 6, followed by some interesting future work.

CHAPTER 2

Overview of Differential VCO

In a typical wireless transceiver, oscillator plays an essential role in generating LO signal. The LO signal is required to down-convert RF signal to a lower IF signal, or to up-convert IF signal to the RF signal [8]. In most cases, the frequency of the LO signal must be tunable for different carrier frequencies. For most RF system, the output frequency of the oscillator is usually tuned by varying a control voltage and such oscillator is called voltage-controlled oscillator. Although current-controlled oscillator designs are also reported, they are not widely used in RF system because of difficulties in varying the value of high-*Q* storage elements by means of a current [8].

For typical RF application, LC VCO is used. The design of a VCO is still one of the most challenging tasks in RF systems. A well-designed VCO must meet very stringent requirements, such as phase noise, power consumption and tuning range since it significantly affects the quality of the LO signal.

2.1 General Concept of Oscillator

An oscillator generates a periodic output. As such, the circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. Most RF oscillators can be viewed as feedback circuit [8]. Consider the general feedback system shown in Figure 2.1, where *H(s)* and *G(s)* are the gains of the feedforward and the feedback network respectively and $s = j\omega$. The overall transfer function can be expressed as:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+G(s)\cdot H(s)} \tag{2.1}$$

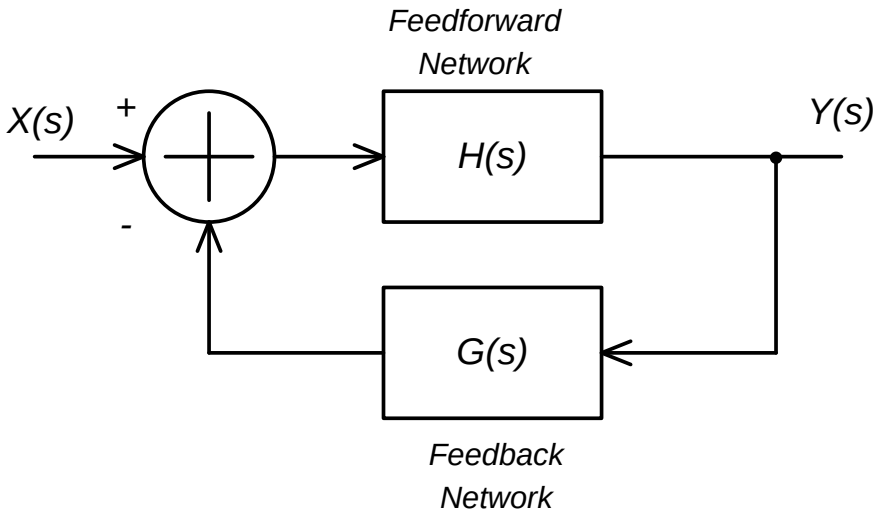


Figure 2. 1 Diagram of general feedback system

According to Barkhausen's Criteria, the system will oscillate at frequency ω_0 if and only if $G(j\omega_0)\cdot H(j\omega_0) = -1$. In other words, the open-loop gain of the feedback system is equal to unity, i.e. $Re\,[G(j\omega_0)\cdot H(j\omega_0)] = -1$ and the total phase shift of the loop is $2\pi n$, where n is an integer or $Im\,[G(j\omega_0)\cdot H(j\omega_0)] = 0$. Under this condition, the circuit amplifies its own noise components at ω_0 and the oscillation can be sustained without input.

To stabilize the oscillation frequency, a frequency-selective network is included in the loop, as shown in Figure 2.2. For LC-oscillator, the LC tank performs as the frequency-selective network.

In practice, the loop gain $H(j\omega_0)$ is typically chosen to be 2~3 times of the required value to counter the temperature and process variations [9]. On the other hand, to achieve stable amplitude, the "average" loop gain must return to unity [8].

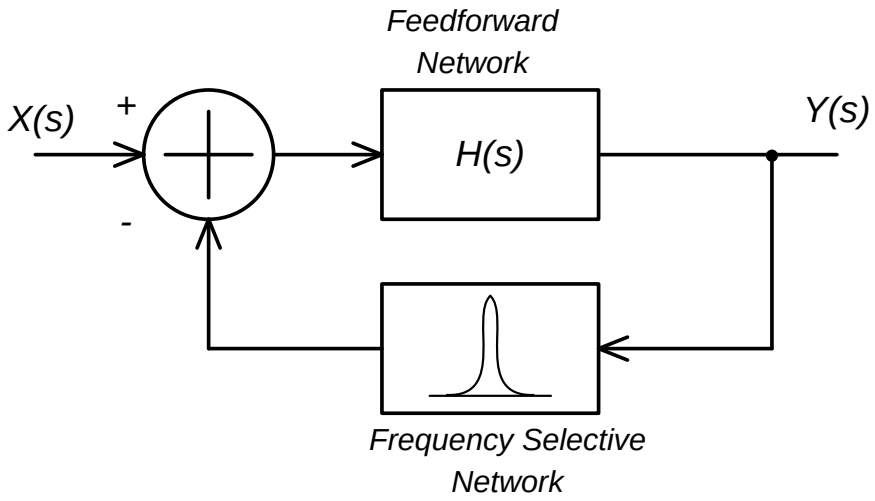


Figure 2. 2 Feedback oscillatory system with frequency-selective network

2.2 Mathematical Model of VCO

For an ideal VCO, the output frequency is a linear function of its control voltage. It can be expressed as:

$$\omega_{out} = \omega_0 + K_{VCO} \cdot V_{cont} \tag{2.2}$$

where ω_0 is the "free-running" frequency and K_{VCO} is the "gain" of the VCO with unit as rad/s/V.

Radian frequency $\omega = 2\pi f$ can also be expressed as the derivative of the phase with respect to time:

$$\omega_{out} = \frac{d\theta}{dt} \tag{2.3}$$

where θ is the instantaneous phase of the VCO's output waveform. Hence the instantaneous phase can be calculated as:

$$\theta = \int \omega_{out} dt + \theta_0 \tag{2.4}$$

with θ_0 is the initial phase of the VCO's output

Substitute equation (2.4) into equation (2.2), θ can be expressed as:

$$\theta = \int \omega_{out} dt + \theta_0 = \omega_0 \cdot t + K_{VCO} \cdot \int V_{cont}\, dt + \theta_0 \quad (2.5)$$

Thus VCO's instantaneous output voltage can be expressed as:

$$V_{VCO}(t) = V_A \cdot \sin(\omega_0 \cdot t + K_{VCO} \cdot \int V_{cont}\, dt + \theta_0) \quad (2.6)$$

where $V_{VCO}(t)$ is instantaneous output voltage of the VCO and V_A is its amplitude.

Equation (2.6) is the mathematic expression for ideal VCO. However, in practice, VCO exhibits non-linear characteristics. For example, the gain of the VCO, K_{VCO} , is not constant over the tuning range. Actual oscillator characteristics typically have a high gain region in the middle and a low gain at the two extremes [10], as shown in Figure 2.3:

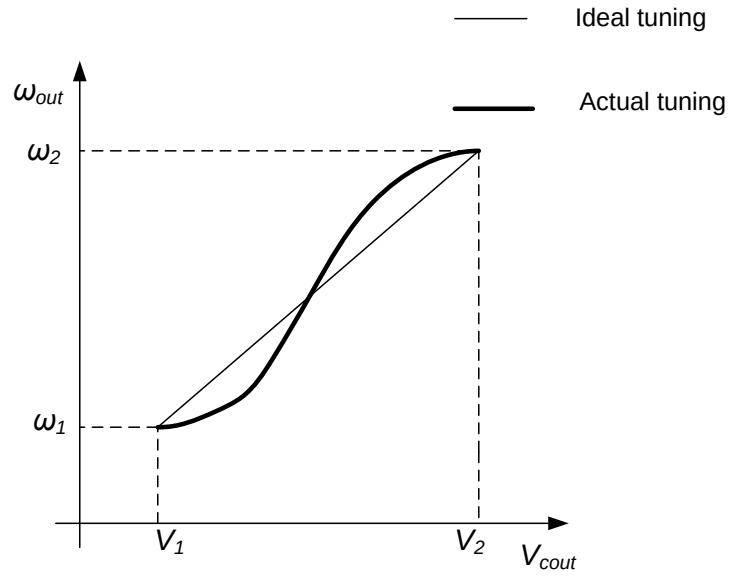


Figure 2. 3 Tuning characteristics for ideal and actual VCO

Such nonlinearity degrades the settling behavior of Phase-Locked Loops (PLL). For this reason, it is desirable to minimize the variation of K_{VCO} across the tuning range.

Other non-ideal characteristics of VCO include amplitude variation across

the tuning range and output signal impurity, or commonly quantified as “jitter” and “phase noise”. Detail discussion of these non-ideal characteristics will be given in Section 2.4.

2.3 LC VCO

As mentioned earlier, LC VCO is more commonly used in typical RF application. So it is important to analyze this type of VCO in detail. Analysis starts with LC oscillator.

2.3.1 General structure of LC oscillator

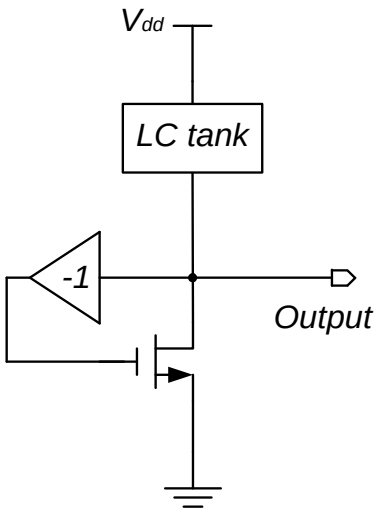


Figure 2. 4 General topology of an LC oscillator

Figure 2.4 shows a general topology of an LC oscillator. The LC tank works as a frequency-selective network and determines the output frequency of the oscillator. The MOSFET and the negative gain buffer provide the necessary gain and phase shift to sustain the oscillation. In addition, they also provide

power to compensate the loss of the LC tank.

2.3.2 LC tank

An ideal LC tank is shown in Figure 2.5(a). A capacitor C_1 is connected to inductor L_1 in parallel. Ideally, both of them have no loss. The total impedance of the tank can be calculated as:

$$Z_{eq}(s) = L_1 \cdot s // \frac{1}{s \cdot C_1} \tag{2.7}$$

The magnitude of this total impedance is:

$$\left|Z_{eq}(s = j\omega)\right| = \frac{\frac{L_1}{C_1}}{\left|L_1 \cdot \omega - \frac{1}{C_1 \cdot \omega}\right|} \tag{2.8}$$

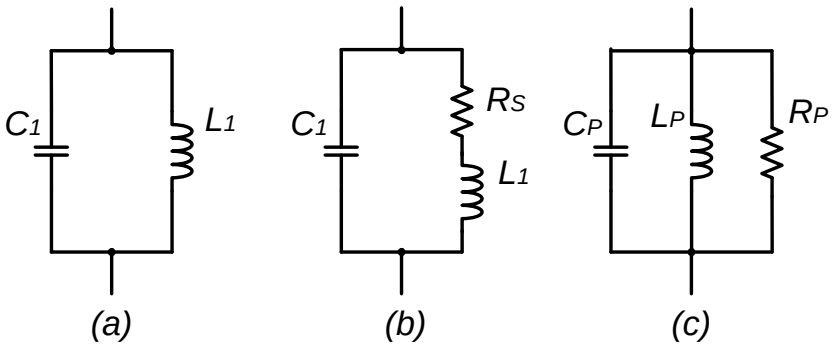


Figure 2. 5 General topology of an LC oscillator

From equation (2.8), it is clear that at frequency $\omega_0 = 1/\sqrt{L_1 \cdot C_1}$, the impendence of L_1 and C_1 has equal value but opposite sign. This means the total impedance of the LC tank is infinite.

However, in practice, both the inductor and capacitor suffer from resistive components. Considering these parasitic resistive components, the actual LC tank can be modeled as Figure 2.5(b) or Figure 2.5(c). For a given LC tank, relationship of different components' value can be calculated as:

$$L_P = L_1 \cdot \left(1 + \frac{R_S^2}{L_1^2 \cdot \omega^2}\right) \tag{2.9}$$

$$R_P = \frac{L_1^2 \cdot (\omega^2 + R_S^2/L_1^2)}{R_S} \tag{2.10}$$

$$C_P = C_1 \tag{2.11}$$

The quality factor of Figure 2.5(b) is defined as $Q = \frac{\omega \cdot L_1}{R_S}$. When converted to Figure 2.5(c), the same Q value can be calculated as $Q = \frac{R_P}{\omega \cdot L_P}$. It is worth to note this Q factor is an important factor to decide the phase noise of the LC oscillator [11].

From Figure 2.5(c), one can conclude that the maximum impedance of the tank is just R_P. This happens when and only when:

$$\omega_1 = 1/\sqrt{L_P \cdot C_P} = 1/\sqrt{L_1 \cdot \left(1 + \frac{R_S^2}{L_1^2 \cdot \omega^2}\right) \cdot C_1}$$

$$= 1/\sqrt{L_1 \cdot (1 + Q^{-2}) \cdot C_1} \tag{2.12}$$

Equation (2.12) shows the magnitude of the LC tank's impedance reaches a peak at a frequency slightly drifted from $\omega_0 = 1/\sqrt{L_1 \cdot C_1}$ and the variation depends on the quality factor Q. However, this variation can be ignored if Q is large enough.

Since the LC tank works as a frequency-selective network, the oscillation frequency of the LC oscillator is the one at which the total tank impedance reaches its maximum, which is ω_1. For simplicity, it is assumed the Q is large enough so ω_0 is approximately equal to ω_1 and the oscillation frequency is $\omega_0 = 1/\sqrt{L_1 \cdot C_1}$.

It is also worth noting that at the frequency where the magnitude of LC tank's impedance reaches the peak, the total phase shift introduced by the tank is 0. Furthermore, the LC tank is inductive and the phase of the total impedance

is positive when $\omega < \omega_1$. On the other hand, the LC tank is capacitive and the phase of the total impedance is negative when $\omega > \omega_1$.

2.3.3 Tuning of LC VCO

Since the oscillation frequency of the LC oscillator is equal to $f_{osc} = 1/(2\pi \cdot \sqrt{L_1 \cdot C_1})$, the frequency of the LC VCO can be tuned by varying the value of the inductor or capacitor. In practice, it is common to vary the value of the tank capacitance since it is difficult to vary the value of monolithic inductors. Such variable capacitor is usually implemented by varactor. Note that VCO with tunable active inductor has been reported recent years [12~14].

A reverse-biased *p-n* junction can serve as a varactor. The voltage dependence is expressed as [10]:

$$C_{var} = \frac{C_0}{(1+\frac{V_R}{\emptyset_B})^m} \tag{2.13}$$

where C_0 is the capacitance at zero-bias condition, V_R is the reverse-bias voltage, $\emptyset_B$ is the built-in potential of the *pn* junction, and m is an empirical constant typically between 0.3 to 0.4. It is clear that the relationship between C_{var} and V_R is not linear. Furthermore, substituting equation (2.13) into $\omega_0 = 1/\sqrt{L_1 \cdot C_1}$ to replace C_1, ignoring all parasitic capacitance and perform a differentiation with respect to V_R, it can be concluded that K_{VCO} is not linear even in theory.

To enhance the tuning range of the LC VCO, digital-controlled switched-capacitor banks are introduced to perform coarse tuning while varactor performs fine tuning. This strategy is commonly employed in wideband LC VCO design [15~17].

2.3.4 Types of LC VCO

The LC VCO can be either single-ended or differential. Compare with single-ended design, the differential LC VCO has higher common mode rejection ratio (CMRR), stronger attenuation of even-order harmonics and lower phase noise [18]. On the other hand, the differential LC VCO requires more components, larger area and higher power consumption. In most applications nowadays, the differential type is commonly required. The differential oscillators can be integrated on-chip according to different topologies, each having its own advantages and disadvantages in connection to power dissipation, frequency tuning range, phase noise and voltage swing [19].

In an LC VCO, the cross-coupled transistor pair can be used to provide the $-G_m$ to compensate the loss of the LC resonant tank. In CMOS technology, depending on the transistor type used to build the cross-coupled pair, the LC VCO can be classified into NMOS-only, PMOS-only and Complementary oscillator, as shown in Figure 2.6(a), (b) and (c) respectively. In an NMOS-only LC VCO topology, the cross-coupled pair is formed by NMOS transistor only. The advantages of this topology are its simplicity and low phase noise. For the same supply voltage, the maximum output amplitude is larger compare with the Complementary topology. In a PMOS-only LC VCO topology, only PMOS transistor is used to form the cross-coupled pair. However, at room temperature the electron mobility for Si is typically about 3 times of the hole mobility. As a result PMOS transistor pair requires 3 times area than that for NMOS transistor pair in order to generate the same $-G_m$ value with the same power consumption. Hence the PMOS-only topology is not a favorable choice mainly due to the operation frequency, tuning range and cost consideration. The Complementary

topology shown in Figure 2.6(c) employs both NMOS and PMOS transistor to form the cross-coupled pair. Major advantage of this topology is its lower current consumption than the other two types to generate the same negative conductance value. However, compare with NMOS-only topology, the headroom for the output voltage swing is limited.

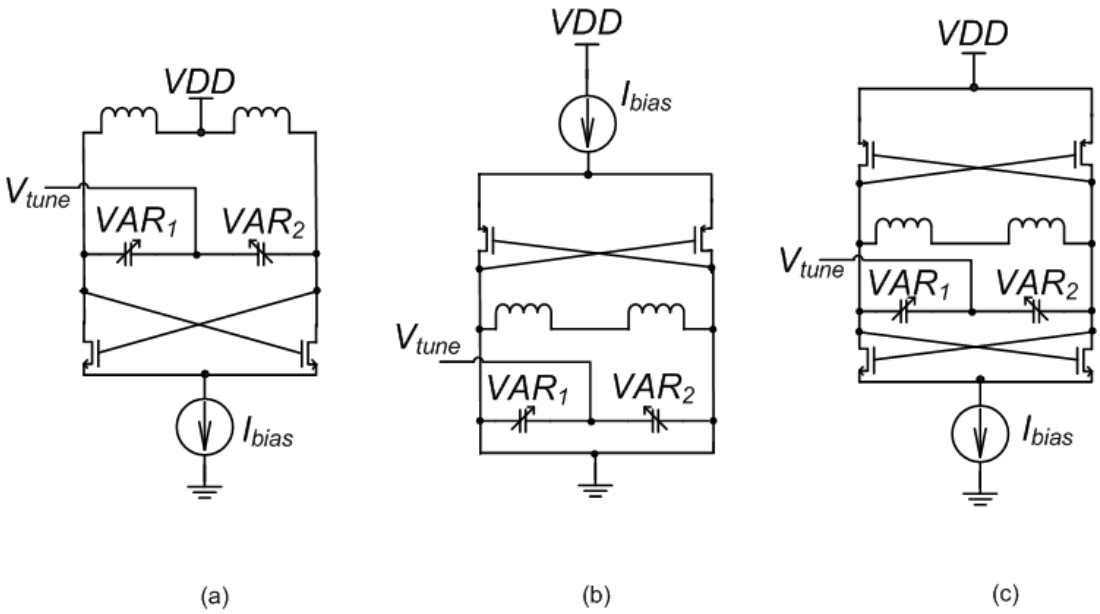


Figure 2. 6 NMOS only (a), PMOS only (b) and Complementary (c) LC oscillators

2.4 Phase noise

As mentioned above, an important non-ideal characteristic of VCO is the output signal impurity. Even with a constant control voltage, the output waveform of a VCO is not perfectly periodic. The output signal can be modeled as:

$$V_{out}(t) = V_{VCO}(t) \cdot sin[\omega_0 t + \theta(t)] \quad (2.14)$$

where $V_{VCO}(t)$ and $\omega_0 t + \theta(t)$ are the amplitude and phase from the output signal, respectively.

The electronic noise of the devices in the oscillator and supply noise lead to noise in the output phase and frequency [10]. Such effects are quantified as "phase noise".

Phase noise is often characterized in the frequency domain for RF applications. For an ideal sinusoidal oscillator operating at ω_c, the spectrum should be an impulse. However, for an actual oscillator, the spectrum exhibits "skirts" around the center frequency. Phase noise $\mathcal{L}\{\Delta\omega\}$ is defined as the ratio of the noise power in a bandwidth of 1 Hz at an offset frequency $\Delta\omega$ to the carrier power $P_{carrier}$. The result is a single-sided spectral noise density in the unit of dBc/Hz, where dBc indicates a measurement in dB relative to the carrier power.

$$\mathcal{L}\{\Delta\omega\} = 10log\left(\frac{P_{noise}}{P_{carrier}}\right) \tag{2.15}$$

In practice, during mixing process interferer at adjacent channel may be mixed with the tail of the skirt shape LO spectrum thus produces noise at the output. Hence each application has its own phase noise requirement to meet certain Signal-to-Noise Ratio (SNR).

Nonlinearity effects and periodic variation of the circuit parameters make the analysis of phase noise quite difficult. Nonetheless, for simple LC oscillators linear approximations have been used judiciously, yielding reasonable errors in the prediction of phase noise [8]. Relationship between the phase noise $\mathcal{L}\{\Delta\omega\}$ and the offset frequency $\Delta\omega$ is usually illustrated as Figure 2.7, where the angular frequency of the corner between the $1/f^3$ region and $1/f^2$ region is named as $\Delta\omega_{1/f^3}$. A lot of research has been done in describing the upconversion of low frequency noise sources into close-in phase noise [20]. In [21], a detailed explanation of why phase noise can be regarded as the

fluctuation of the zero crossing locations of a signal is presented. However, currently more rigorous analysis of oscillators is still a topic of active research.

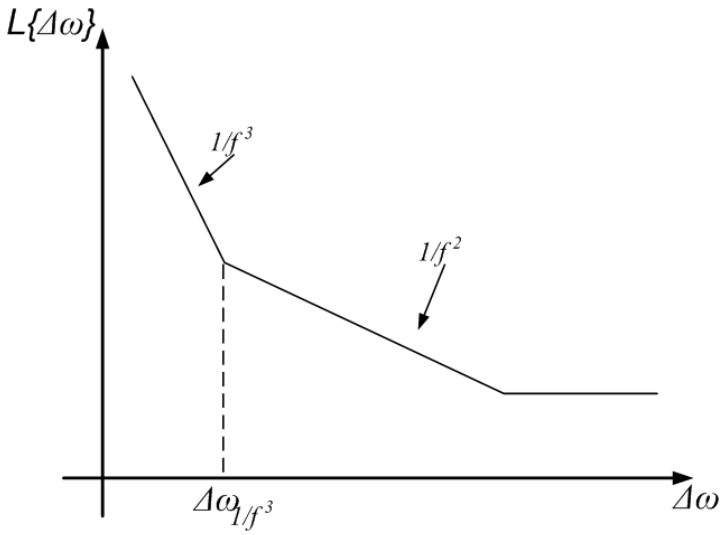


Figure 2. 7 Ideal Spectrum of the oscillator's phase noise

To describe the phase noise performance of a VCO, the following FoM is used. Both power consumption and oscillator's center frequency ω_0 are weighted in the FoM:

$$\text{FoM} = 10log\left(\frac{\left(\frac{\omega_0}{\Delta\omega}\right)^2}{P_{VCO}\cdot\mathcal{L}\{\Delta\omega\}}\right) \tag{2.16}$$

where P_{vco} is the VCO's total power consumption in mW.

2.4.1 The Leeson-Cutler phase noise model

As early as 1966, a semi-empirical model was proposed in [22] and [23], which is known as the Leeson-Cutler phase noise model. Based on a Linear Time Invariant (LTI) system assumption, it predicts the phase noise behavior can be expressed as:

$$\mathcal{L}\{\Delta\omega\} = 10log\left[\frac{2\cdot F\cdot k\cdot T\cdot R}{V_{VCO}^2}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{2.17}$$

where F is an empirical parameter, k is Boltzman's constant, T is the absolute temperature, R is the parallel resistance of the LC tank, V_{VCO} is the output amplitude of the oscillator and $\Delta\omega$ is the offset frequency from the carrier.

The Leeson-Cutler phase noise model suggests that the phase noise is proportional to the noise-to-carrier ratio and inversely to the square of resonator's quality factor. A major drawback of this model is that in general it is difficult to calculate *F a priori* [20]. As mentioned in [22], F and $\Delta\omega_{1/f^3}$ are usually used as *a posteriori* fitting parameters. One important reason is that much of the noise in a practical oscillator arises from periodically varying processes and is therefore cyclostationary [20]. By identifying the individual noise source in the LC VCO, an extended form is suggested in [24]. However it still requires an empirical parameter.

In [21], Rael and Abidi used a simple model of the switching differential pair to calculate the phase noise of differential LC oscillators. Considering all thermal noise source including noise from the resonator, the tail current source and the differential pair, the calculated phase noise matched the Leeson-Cutler phase noise model with F given by:

$$F = 2 + \frac{8 \cdot \gamma \cdot R \cdot I_T}{\pi \cdot V_0} + \gamma \cdot \frac{8}{9} \cdot g_{mbias} \cdot R \tag{2.18}$$

where γ is the noise factor of a single FET, which is 2/3 classically. I_T is the tail current of the oscillator and g_{mbias} is the transconductance of the tail current transistor. However, the uperconverted flicker noise is not included in the derivation.

2.4.2 The Hajimiri's phase noise model

This model is suggest in [23] in 1997. In contrary to the Leeson-Cutler phase noise model, oscillator is assumed as a linear time variant (LTV) system in this model. This model explains the exact mechanism by which spurious sources, random or deterministic, are converted into phase and amplitude variations. By introducing the impulse sensitivity function (ISF), which is a dimensionless, frequency-independent and amplitude-independent periodic function with a period of 2π, the influence of total phase noises from both active and passive elements is studied. This model considers an impulse charge introduced into the capacitance seen from the output node of the oscillator which operates in steady state, in which case both amplitude and phase error would be generated. Due to the amplitude limiting mechanism, the amplitude error generated can be corrected. However, the phase error is a function of the time τ. The unit impulse response for the excess phase hence can be expressed as:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} \cdot u(t-\tau) \tag{2.19}$$

where q_{max} is the maximum charge displacement across the capacitor on the node and $u(t-\tau)$ is the unit step. $\Gamma(\omega_0\tau)$ is the ISF, which is a function of the waveform or the shape of the limit cycle governed by the nonlinearity and the topology of the oscillator. The total sideband power of the phase noise caused by the charge injection hence can be calculated as

$$S_n(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \tag{2.20}$$

where Γ_{rms}^2 is the rms value of the ISF and $\overline{i_n^2}/\Delta f$ is the input noise source power spectral density.

Though equation (2.20) looks quite different from the Leeson-Cutler phase

noise model, it is in fact the same equation as explained below. [23] shows with the following assumptions: (1) all noise sources are stationary, (2) only the noise in the vicinity of the resonant frequency is important and (3) the noise-free waveform is a perfect sinusoid, total phase noise can be calculated based on this model as:

$$\mathcal{L}\{\Delta\omega\} = 10log\left[\frac{1}{2}\cdot\frac{kT}{V_{max}^2}\cdot\frac{1}{R_p\cdot(C\omega_0)^2}\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \quad (2.21)$$

where R_p is the parallel resistor, C is the tank capacitor and V_{max} is the maximum voltage swing across the tank. Recall that $Q = \frac{R_P}{\omega\cdot L_P}$ in Section 2.3.2 and with the approximation $L_P \approx L_1$, equation (2.21) is actually the same as equation (2.18).

Although the ISF cannot be accurately predicted, the Hajimiri's phase noise model has suggested ways to improve the phase noise performance of the LC oscillator, which will be mentioned in Section 2.5. On the other hand, methods for fast and accurate estimation of a certain VCO's ISF has been proposed in [25][26].

2.5 Methods to improve phase noise performance of LC Oscillator

A lot of research has been done to improve the phase noise performance of LC oscillator. Generally, these methods either tried to reduce the noise power of individual noise source or to reduce the noise contribution of individual noise source. For instance, since flicker noise upconversion is an important source of phase noise and noise power of flicker noise is inversely proportional to the

transistor's size, using larger transistor's size with the same *gm* can significantly improve the phase noise performance. However, larger transistor's size also introduces larger parasitic capacitance and limits the tuning range of the VCO.

The flicker noise is also known for its long correlation time and an associated physical process which has a "long-term memory" [27], [28]. A switched transistor will make it memory-less, hence reducing the power of flicker noise. Based on this idea, an LC VCO with memory reduction tail transistor is proposed in [29]. Outputs of the LC VCO are used to bias and switch the tail current source transistor, as shown in Figure 2.8. Simulation results presented in the paper show that with the introduction of memory reduction tail transistor, phase noise at close-in offset frequency can be significantly improved with same power consumption.

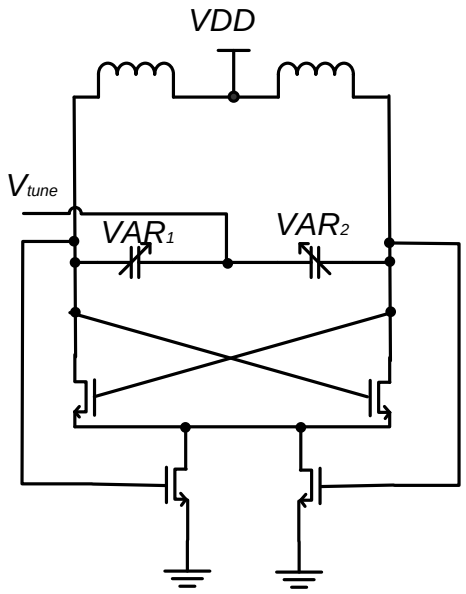


Figure 2. 8 Memory-reduced tail transistor VCO [29]

In [30], E. Hegazi *et al* examined each term in equation (2.16) and focused

on removing the noise contribution of the tail current source. Two important observations are made after studying the role of the tail current source: (1) only the thermal noise in the current-source transistor around the second harmonic of the oscillation causes phase noise, and (2) a high impedance at the tail is only required at the second harmonic to stop the differential-pair FET in triode from loading the resonator [30]. Based on the two observations above, it is suggested to introduce a filter to suppress the troublesome noise frequencies in the current source and to provide high impedance in the oscillation frequencies in parallel to the signal path. This is done by putting a large capacitor in parallel with the current source to short the noise frequencies at the second harmonic to ground, and to inserts an inductor between the current source and the virtual ground of the oscillator to form a high impedance at the 2nd harmonic of the oscillation frequency, as shown in Figure 2.9. The inserted inductor and the large capacitor comprise the "noise filter" [30].

A significant drawback of this noise filtering technique is the large area required by the additional inductor and capacitor. In [31], A. Hajimiri and T. H. Lee examined the effect of putting a capacitor in parallel with the tail current transistor. They confirmed that this tail capacitor can improved the phase-noise behavior of the differential LC oscillator. By applying the Hajimiri's phase noise model, the mechanism of this improvement is that as the tail capacitor makes the waveform of the oscillator's output more symmetrical and the harmonic distortion smaller, thus the Γ_{rms}^2 is reduced. However, it is pointed out in [31] that the tail capacitor reduces the output impedance of the tail-current source at high frequencies, which leads to higher sensitivity to supply voltage variation.

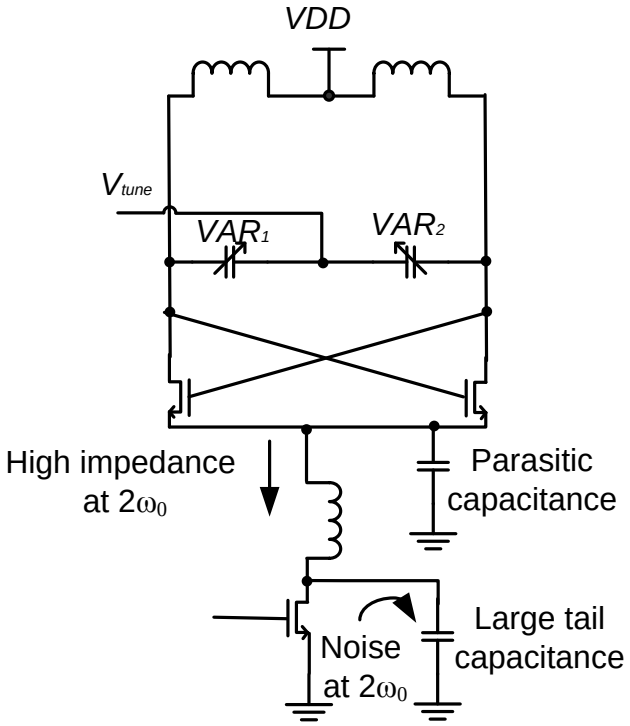


Figure 2. 9 Tail-biased NMOS VCO with noise filter [30]

To compare the methods mentioned above, a Complementary VCO is designed in 0.18 μm CMOS technology. The Complementary VCO is then modified to apply the noise filter and the memory reduction tail transistors while keeping the LC tank, cross-coupling pair and the power consumption the same as the original Complementary VCO. The simulated phase noise is shown in Figure 2.10. It is clear that phase noise at close-in offset frequency improved significantly by both the noise filter and the memory reduction tail transistors. However the improvement of phase noise at high offset frequency is marginal. On the other hand, difference between the noise filter approach and the memory reduction tail transistors approach is less than 0.5 dB and hence can be neglected. This is expected as both methods aim to reduce the flick noise introduced by the current source, which is up converted into close-in phase

noise.

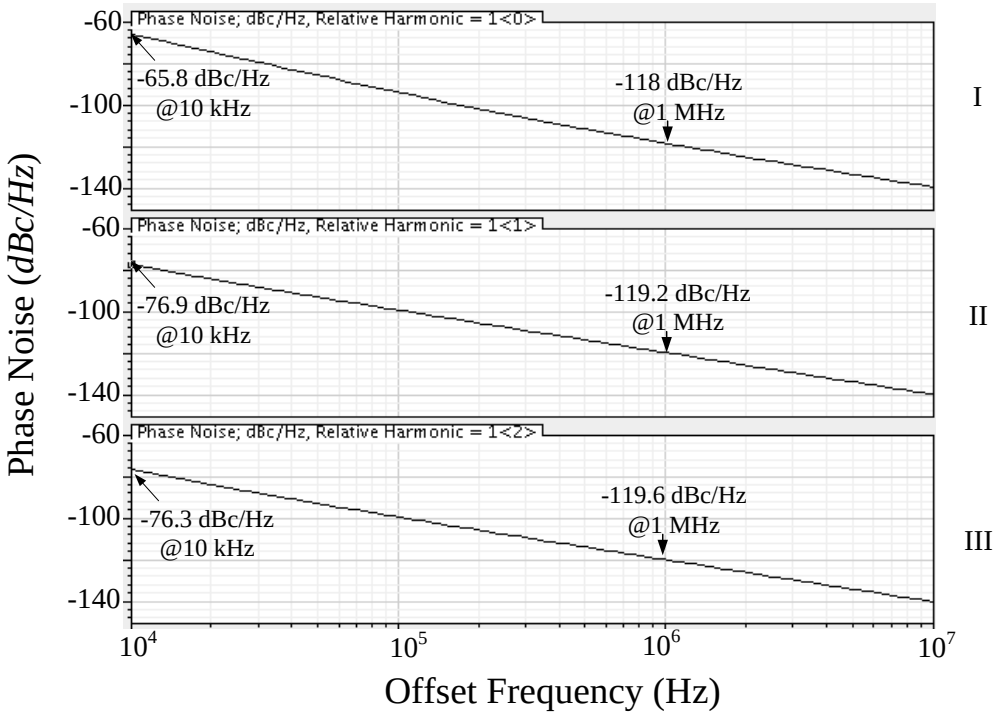


Figure 2. 10 Phase noise performance of Complementary VCO (I), Complementary VCO with noise filter (II) and Complementary VCO with memory reduction tail transistor (III)

The role of the tail capacitor shows an important observation: a more symmetrical output waveform means a smaller Γ_{rms}^2 value, hence reduces the total noise power. In [32], it is suggested a more symmetrical output waveform can be achieved by proper sizing and layout the PMOS and NMOS cross-couple pair in Complementary VCO design. Simulation result presented in the paper shows by making both the transconductance and size of the and NMOS cross-coupled pair match, phase noise at close-in offset frequency can be significantly improved.

Both equation (2.16) and equation (2.19) shows phase noise is inversely proportional to the square of the output amplitude. So it is straight forward to conclude that phase noise performance can be improved by increasing the

output voltage amplitude. Relationship between the tail current I_T and the amplitude V_{VCO} is given by:

$$V_{VCO} = \frac{4}{\pi} \cdot I_T \cdot R_{eq} \tag{2.22}$$

where R_{eq} is the equivalent parallel resistance of the tank. According to equation (2.20), the output amplitude can be increased by increasing the tail current. However, there exists a limit for the output amplitude.

Take the Complementary LC VCO for example, when V_{VCO} approaches the supply voltage, both the NMOS and PMOS pairs will enter the triode region at the peak of the output voltage. Besides the tail current transistor may spend a large portion of the operation cycle in the triode region. In this case, V_{VCO} is clipped at V_{DD} by the PMOS pairs and at ground by the NMOS pairs [31] and no longer proportional to I_T. In [31] this operation region is named as "voltage-limited region" and when V_{VCO} is proportional to I_T, the oscillator is in the "current-limited region".

Based on this concept and the Hajimiri's phase noise model, a systematical design and optimization method for LC VCOs is proposed in [33]. It suggests keeping V_{VCO} in an optimal value in the current-limited region obtained through a systematical graphical method. At this V_{VCO} value, both the phase noise performance and power consumption are optimized.

2.6 Class-C VCO

Recently, a new differential LC VCO topology, namely the Class-C VCO is proposed. It is first introduced in [34]. The schematic of this Class-C harmonic VCO is shown in Figure 2.11. The structure is very similar to conventional LC

VCO and the cross-coupled NMOS pair is biased by an external voltage, V_{bias2}, though an RC network. By properly biasing the cross-coupled NMOS pair, this NMOS pair is kept at the active region. The drain current waveform of each NMOS transistor has a small conduction angle that resembles of narrow pulses. As a result, the relationship between the output amplitude and the bias current is given by [34]:

$$V_{VCO} = 2 \cdot I_T \cdot R_{eq} \tag{2.23}$$

obviously, compare with the conventional LC VCO, the Class-C LC VCO requires smaller I_T to achieve the same V_{VCO}.

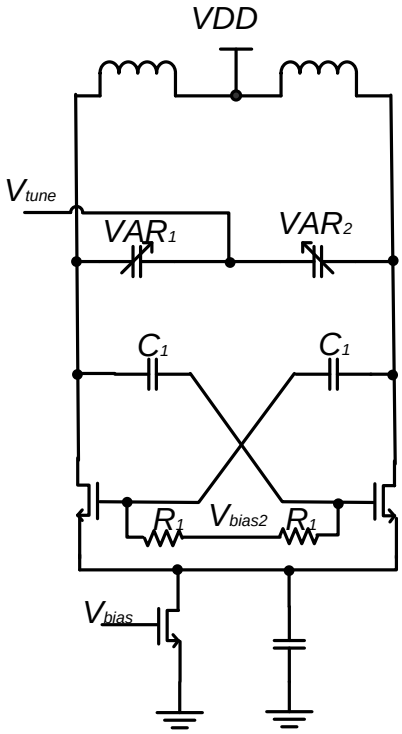


Figure 2. 11 Class-C VCO [34]

The noise performance of the Class-C VCO is also examined in [34]. It concludes that the Class-C operation may not provide any advantage in terms of effective transistor or tank noise power compare with conventional LC VCO.

However, for the same current consumption, the higher amplitude of Class-C VCO already shows advantage in improving phase noise performance and the FoM mentioned before. In [34], it is declared that compare with conventional NMOS only type LC differential VCO, Class-C VCO improves phase noise by 10 dB. Similar to other LC VCO topology, the design of the Class-C VCO requires special attention on the stability of the oscillation.

Though not mentioned in [34], the role of capacitor C_1 is also important. To understand this, a novel analysis is presented here. The half circuit of the Class-C VCO shown in Figure 2.11 is simplified as Figure 2.12.

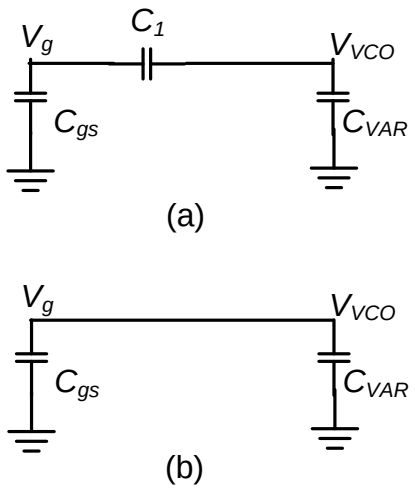


Figure 2. 12 Simplified half circuit of Class-C VCO (a) and conventional NMOS type VCO (b)

In this circuit, C_{VAR} is the capacitance of the varactor VAR_1, C_{gs} is the gate-source parasitic capacitance of each transistor of the cross-coupled pair. V_g is the AC signal at the gate of the cross-coupled transistor pair. For the simplified half circuit of the conventional NMOS type VCO topology, following relationships are straight forward:

$$V_g = V_{VCO}$$

$$C_{total} = C_{VAR} + C_{gs} \tag{2.24}$$

where C_{total} is the total capacitance looking into the output terminal of the VCO.

However, for Class-C VCO, the relationships are expressed as:

$$V_g = V_{VCO} \cdot \frac{C_1}{C_{gs}+C_1}$$

$$C_{total} = C_{VAR} + \frac{C_{gs} \cdot C_1}{C_{gs}+C_1} \tag{2.25}$$

Obviously, for Class-C VCO $V_g < V_{VCO}$. To sustain oscillation, V_g should not be too small, otherwise the cross-coupled transistors cannot be turned on/off periodically and proper oscillation cannot sustain. As a result, C_1 cannot be arbitrarily small. On the other hand, since $\frac{C_{gs} \cdot C_1}{C_{gs}+C_1} < C_{gs}$, total capacitance looking into the output terminal for Class-C VCO is smaller compare with conventional NMOS-only VCO topology. In other words, tuning range of the Class-C VCO is higher. Note for the same C_{gs}, a smaller C_1 leads to smaller $\frac{C_{gs} \cdot C_1}{C_{gs}+C_1}$. Hence to maximize the frequency tuning range, a smaller C_1 is desired. Thus there exists a tradeoff for the value of C_1 between proper oscillation and wide tuning range.

In practice, both the value of C_1 and R_1 should be carefully selected. A larger R_1 can help to reduce the value of C_1. In addition, a larger conduction angle of the cross-coupled pair is desired during start-up, thus V_{bias2} should be properly selected to ensure a reliable start-up.

2.7 Amplitude variation of LC VCO

Though seldom mentioned, practical LC VCO suffers from amplitude variation across the tuning range. Recall equation (2.13), the amplitude of the practical LC VCO, $V_{VCO}(t)$, is a function of time. Fortunately, as analyzed in [23], due to the amplitude limiting mechanism, the amplitude error generated can be corrected. On the other hand, as mentioned earlier, the output amplitude of a practical LC VCO varies across the tuning range. This effect is more significant for wideband VCO. For the wideband LC VCO proposed in [35] whose frequency range is from 3.5 GHz to 5.3 GHz, the amplitude variation over the tuning range is about 40%. In another example shown in [5], the amplitude variation over the tuning range is about 200mV, or about 22% of the standard amplitude. Such amplitude may affect the performance of the transceiver.

In a typical wireless transceiver, VCO is an essential block of the frequency synthesizer. The output of the VCO is connected to a series of frequency divider for frequency calibration. Generally, an optimum and constant input amplitude for the divider, which is the VCO's output, helps the frequency divider to achieve better performance. As introduced in [36], this property is important for wideband frequency synthesizer. Previous research has shown performance of different kinds of frequency divider is related to V_{VCO}.

For Injection-Locked Frequency Divider (ILFD), the relationship between the locking range ω_L and the injected current I_{inj} is shown in [37] as:

$$\omega_L \approx \frac{\omega_0}{2 \cdot Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{2.26}$$

where ω_0 and I_{osc} are the free-running frequency and current of the ILFD. A

more detailed analysis can be found in [38]. For an ILFD in the frequency synthesizer, the injected signal into the ILFD is likely the output of the VCO, so the VCO's output amplitude directly affects I_{inj}. [39] and [40] also reported that there exists an optimum input DC level and AC amplitude which come from the VCO's output for the typical D Flip-Flop frequency divider, namely the True-Single-Phase-Clock (TSPC) and extended-TSPC (E-TSPC).

2.8 Automatic Amplitude Calibration (AAC) Loop for LC VCO

The analysis in Section 2.6 and 2.7 above shows that it is attractive to achieve an optimized V_{VCO} value over the tuning range. This can be achieved through an AAC loop. In addition to the benefits mentioned above for constant and optimized amplitude, an AAC loop can also enable the VCO to achieve an optimum value of excess loop gain and reliable start-up. This property is especially important for the class-C VCO, as discussed in [5] and [41].

The basic block diagram of the AAC loop is shown in Figure 2.13 and it operates as follows: The output amplitude of the VCO, V_{VCO}, is measured by a Peak Detector (PD). The output of the PD, V_{PD}, should be a DC signal that indicates V_{VCO}. V_{PD} is then compared with an externally set reference voltage V_{REF} through comparator or amplifier. The gain control block generates a control signal V_{ADJ} according to the comparison result to tune the V_{VCO}.

Recall equation (2.22) and equation (2.23), it is obvious for both conventional and class-C LC VCO, the output amplitude V_{VCO} is proportional to the bias current I_T and the parallel resistance of the resonator, R_{eq}. Since tuning

R_{eq} will affect the Q of the resonator and it is difficult to tune R_{eq} in practice, it is more common to tune V_{VCO} by adjusting I_T.

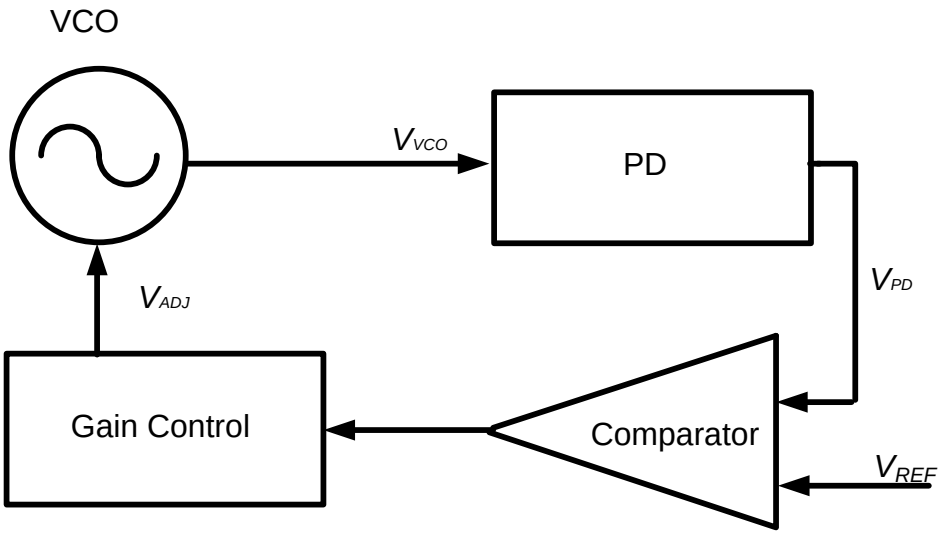
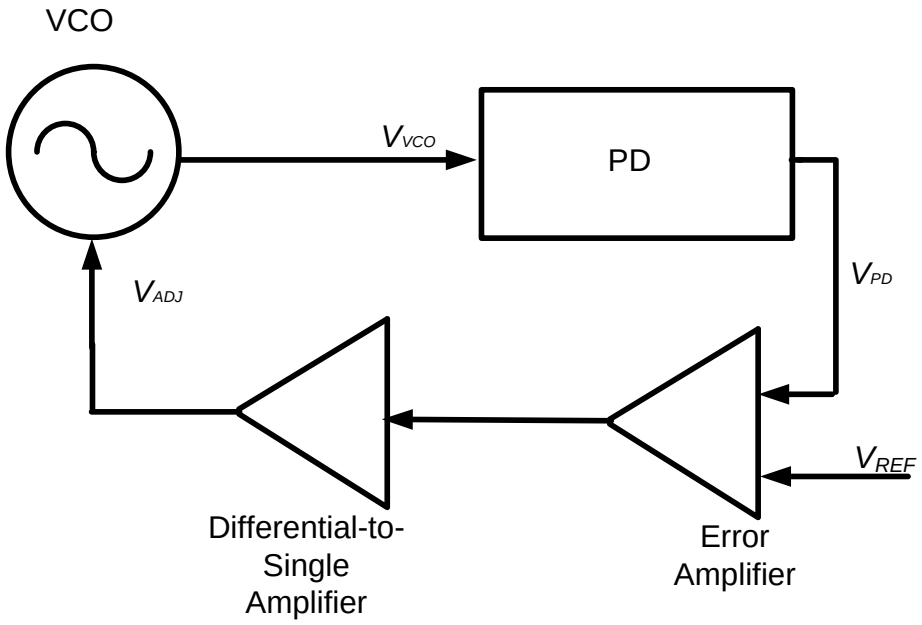


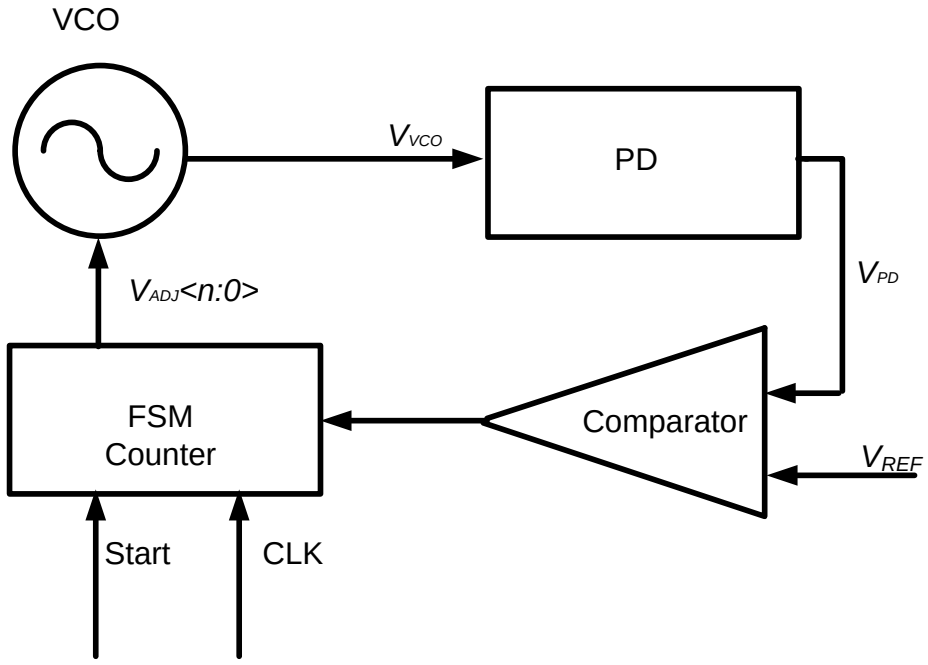
Figure 2. 13 General block diagram of the AAC loop

Depending on the mechanism of comparison between V_{PD} and V_{REF}, as well as structure of the gain control block, reported AAC VCO can be generally divided into two major types: analog type AAC VCO and digital type AAC VCO. Typical block diagram of these two types of AAC VCO are shown in Figure 2.14. Both types have their own advantages and disadvantages.

Block diagram of a classical analog type AAC is shown in Figure 2.14(a). Such architecture is applied in [4], [42] and [43]. In an analog AAC VCO, V_{PD} is compared with V_{REF} by an error amplifier. The "differential" amplified signal produced by the error amplifier is then converted to V_{ADJ} by the differential-to-single ended amplifier. V_{ADJ} acts as the bias voltage for the tail current source transistor of the VCO core and adjusts the bias current of the VCO continuously.



（a）



（b）

Figure 2. 14 Block diagram of typical analog AAC VCO (a) and digital AAC VCO (b)

Although the structure is simple, analog type AAC introduced extra noise to the VCO core. The PD's role is extensively studied in [4]. It concludes that the

PD acts as a major noise source and introduces extra noise. These noises are amplified by the following blocks and causing V_{ADJ} to fluctuate. Since V_{ADJ} is used to bias the tail current source transistor, these noises produces random fluctuations of the biasing current which are up-converted to phase noise by the mixing mechanism. To minimize the extra noise introduced, not only the PD itself but also the circuit driven by the PD should be properly designed, as suggested in [4].

Besides introducing extra noise, analog AAC VCO also faces stability problem since it always works as a negative feedback loop. For a typical analog AAC VCO shown in Figure 2.15(a), the PD and the differential-to-single amplifier each contributes a pole as $R_P \cdot C_P$ and $R_L \cdot C_L$. If not designed properly, for instance the frequency of the dominant pole is not low enough, the loop will not be stable. In this case V_{VCO} will vary periodically, which phenomenon is called "squegging". The analog AAC VCO illustrated in Figure 2.15(a) is designed in GlobeFoundary 0.18 μm CMOS technology and simulated. Proper oscillation sustains for the standard value of C_L, however if C_L is reduced to 1/10 of the standard value for instance, V_{OUT} exhibits amplitude modulation, as shown in Figure 2.15(b). In [44], J.W.M. Rogers *et al* suggests how to make the analog AAC VCO to be more stable in detail.

On the other hand, for the digital type AAC VCO whose block diagram is shown in Figure 2.14(b), V_{PD} is compared with V_{REF} by the comparator. The digitalized comparison result is used as a control signal for the Finite State Machine (FSM) counter, whose output is an multi-bit digital signal $V_{ADJ} < n:0 >$. This $V_{ADJ} < n:0 >$ controls the states of switches for the bias current array. As a result, the bias current of the VCO core is adjusted discretely.

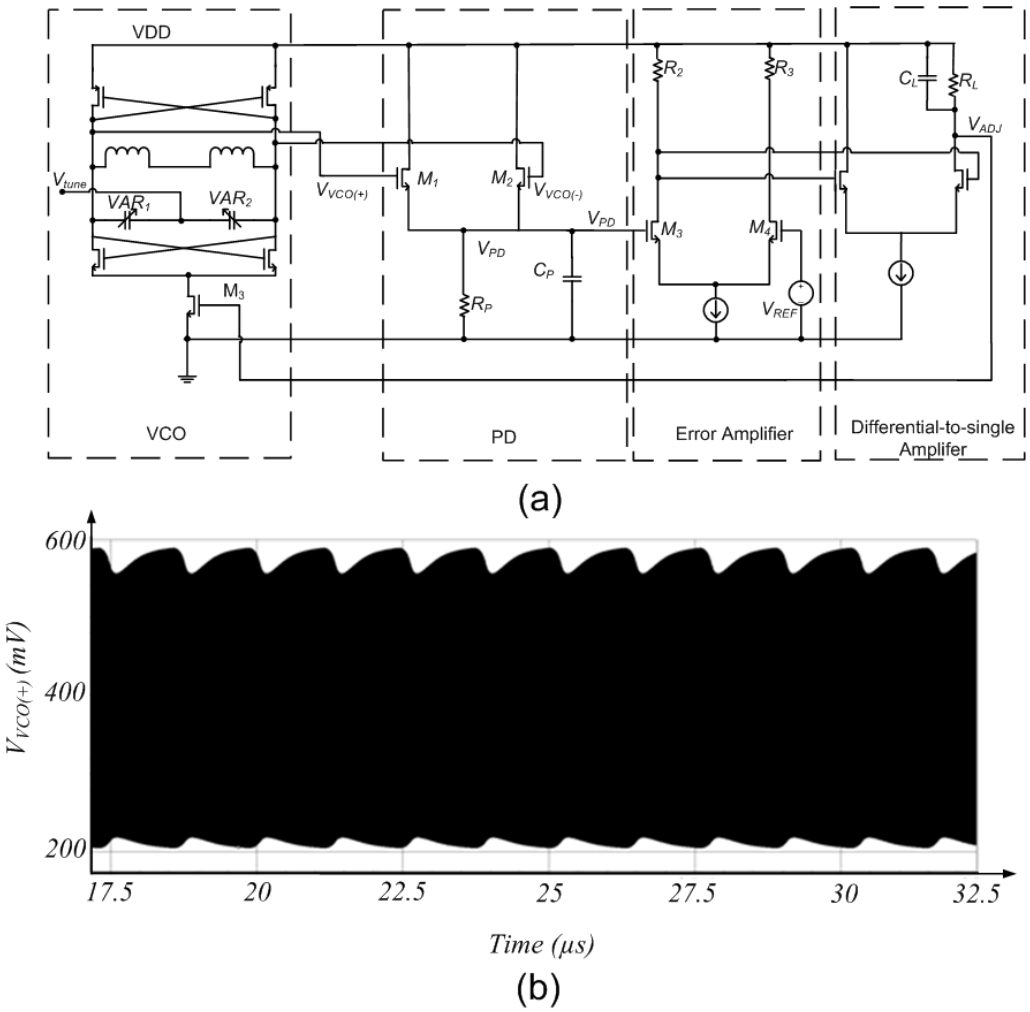


Figure 2. 15 Schematic of typical analog type AAC VCO (a) and squegging (b)

Since $V_{ADJ} < n: 0 >$ is an n-bit control signal and only determine the states of switches for the bias current array, the bias current is generally not affected by the noise in $V_{ADJ} < n: 0 >$. The near open nature of the loop [5] makes the digital type AAC VCO free of the stability problem that is common for analog type AAC VCO. However in some cases, such as [44], V_{PD} is compared with a pair of reference voltage, V_{HIGH} and V_{LOW} which defines a desired range for V_{VCO}. In these cases, if the resolution is so big that the voltage range defined by two adjacent $V_{ADJ} < n: 0 >$ counts is even wider than that defined by V_{HIGH} and

V_{LOW}, or in other words there is no solution of $V_{ADJ} < n: 0 >$ that V_{VCO} falls into the voltage region defined by V_{HIGH} and V_{LOW}, the loop will "hunts" between the two adjacent counts continuously [44], which also results in squegging.

Although in general the digital type AAC is more stable and less noisy compare with the analog type AAC VCO, the introduction of blocks such as the FSM counter, clock signal generator and current source arrays greatly increases the circuit complexity. These blocks may also increase the total area and power consumption of the AAC VCO. For instance, in [44], the power consumption of the digital type is twice that of the analog type. Besides, in this paper the area of one type is about 60% larger than that of the other type, though it is not indicated which type occupies smaller area.

Though seldom mentioned, both types of AAC loop can be applied to the quadrature VCO. One such example is shown in [45] and [46]. However, the circuitry is more complex than that of a differential VCO.

2.9 Summary

In this chapter, the fundamental of oscillator is introduced, then the operation principle and the topology of LC VCO is studied. Moreover, the performances of the LC VCO, such as phase noise and amplitude variation, are discussed. Finally, several approaches to improve the performance of the LC VCO are reviewed.

In Section 2.4, several important models to predict the VCO's noise performance are studied. The Leeson-Cutler phase noise model and the

Hajimiri's phase noise model are introduced separately. Based on these two phase noise models, approaches to improve the performance of LC VCO namely memory reduction tail transistors and noise filter are reviewed in Section 2.5. Simulation result shows both approaches show significant 11 dB phase noise improvement at 10 kHz offset frequency but only show marginal 1.5 dB improvement at 1 MHz offset frequency. In conclusion, both approaches improve phase noise at close-in offset frequency more significantly. It is expected as both of them try to reduce the flicker noise, whose contribution is significant at close-in offset frequency. It is noted that in addition to optimize the structure of LC VCO, maintaining optimal output amplitude is also important. For the VCO core of the AAC VCO proposed in Chapter 4, the memory reduction tail transistors approach is not applicable. This because the DC biasing point of the tail transistor will be affected by this technique. In addition, this technique cannot help to improve the flicker noise contribution of the auxiliary current source transistor. However, a simplified version of the noise filter approach, which is to put a capacitor in parallel with the tail current source is adopted to improve the performance of the VCO core. Class-C VCO which improves the overall performance by producing larger amplitude with the same power consumption is analyzed in Section 2.6. Some publications have declared a 10 dB improvement in measured phase noise has been achieved by Class-C VCO compared with the conventional NMOS only type LC differential VCO. Due to the advantage provided by Class-C VCO, this topology will be used in the proposed QVCO design in Chapter 5.

In Section 2.7, the amplitude variation of the LC VCO over the tuning range is studied. Since the performance of the frequency divider is closely related to

the amplitude of VCO in frequency synthesizer, it is also necessary to maintain optimal VCO output amplitude.

In Section 2.8, an AAC loop that calibrates the VCO's output amplitude automatically is introduced. The two major conventional AAC types, namely the analog type AAC and the digital type AAC, are discussed. Both their advantages and disadvantages are reviewed.

CHAPTER 3

Quadrature Signal Generation

The rapidly evolving wireless communication market demands low cost, low power, highly integrated RF transceiver designs. Low intermediate-frequency (low-IF) and direct conversion (zero-IF) architectures are potential candidates for such transceivers since they obviate the need for off-chip image and channel select filtering that degrade the level of integration, reduce design flexibility, and increase power consumption [47][48].

In modern RF transceiver designs, the in-phase and quadrature phase (I/Q) fully integrated signal generators has become ubiquitous blocks for these transceiver architectures. For 2.4 GHz ISM band application, the most widespread systems are IEEE 802.11 and Bluetooth nowadays. Besides, ZigBee and IEEE 802.15.4 are two upcoming standards for short range wireless networks [49]. According to these standards, quadrature modulation schemes such as DQPSK, QPSK, 16-QAM, 64-QAM and OFDM are adopted [50]. In addition, quadrature signals are required for up/down conversion in zero-IF architectures, which is a suitable solution for full integration of wireless transceivers on a single chip [51]. Besides parameters such as frequency tuning range, phase noise performance and power consumption, mismatch between I/Q signal is also an important parameter for judging the quality of signal generation. The synthesis of accurate quadrature I/Q signals are not only a prerequisite for the successful implementation of image-reject and direct conversion architectures [6], but are also directly related to the transceiver's performance. For most RF applications, the overall image suppression is around

60 to 70 dB [8]. Though this suppression can be partially provided by the front-end filter, image rejection mixer is preferred to perform image rejection due to its advantage of simplicity, small area and wide bandwidth [52]. The Image Rejection Ratio (IRR) for a typical commercial image rejection mixer is around 25 dB. Suppose a Hartley architecture is used and if this 25 dB IRR is purely due to the phase mismatch of the LO I/Q signal, according to the equation shown in [8], it can be calculated that the maximum phase error of the LO signal is 3.6 º. Note in practice, both the phase and amplitude mismatch between the I/Q signal affects the IRR.

Nowadays, accurate I/Q signal generation still remains a major challenge in modern RF design. There are several methods for generating quadrature signal. One popular method is to use a differential VCO that oscillates at twice of the desired frequency and then obtain the quadrature signal with frequency divider [52]. However, higher oscillation frequency and frequency divider result in higher power consumption. On the other hand, RC-CR phase shift network [53] or gm-C network [54] consumes low power, but the bandwidth is limited. Furthermore, matching between the I/Q signal is not so satisfactory. Currently, RC polyphase network and QVCO are still the most popular approaches for quadrature signal generation. This chapter will focus on these two approaches.

3.1 Polyphase filter

The mechanism of quadrature signal generation by polyphase filter has been derived in [55] and [56]. However, both analyses are complicated and not intuitive as the concept of complex signal and circulant matrix properties or

phase decomposition and matrix analysis are adopted. The analysis in [57] is based on superposition principle and thus is much simpler; however the necessary condition for quadrature signal generation is not fully explored. Furthermore, mismatch under these conditions are not discussed.

In this section, a novel analysis based on basic Kirchhoff's current law for the 1st order polyphase filter will be presented first. Based on this analysis, necessary condition for quadrature signal generation is then derived mathematically. High order polyphase filter will be analyzed based on this analysis.

3.1.1 1st order Polyphase filter

Phase shifter can be realized using an RC-CR network also known as a polyphase filter. The polyphase filter can be either passive or active and it can be a single stage or in multiple stages. In this section a novel analysis for quadrature signal generation based on intuitive Kirchhoff's current law is discussed.

The basic building block of the classical RC polyphase filter is shown in Figure 3.1. With the help of Figure 3.1, it is obvious that each output voltage is determined by the two nearest input signal, e.g. voltage output I_{out+} is determined by I_{in+} and Q_{in-}. Applying Kirchhoff's current law, it is obviously that:

$$\frac{I_{out+}-Q_{in-}}{sC^{-1}} = \frac{I_{in\pm}-I_{out+}}{R} \tag{3.1}$$

Thus I_{out+} can be expressed by I_{in+} and Q_{in-}. Following the same approach, the transfer function of all the four outputs in frequency domain can be derived as:

$$I_{out+} = H_A(s) \cdot I_{in+} + H_B(s) \cdot Q_{in-}$$

$$Q_{out+} = H_A(s) \cdot Q_{in+} + H_B(s) \cdot I_{in+}$$

$$I_{out-} = H_A(s) \cdot I_{in-} + H_B(s) \cdot Q_{in+}$$

$$Q_{out-} = H_A(s) \cdot Q_{in-} + H_B(s) \cdot I_{in-} \quad (3.2)$$

where:

$$H_A(s) = \frac{1}{1+s \cdot R \cdot C}$$

$$H_B(s) = \frac{s \cdot R \cdot C}{1+s \cdot R \cdot C}$$

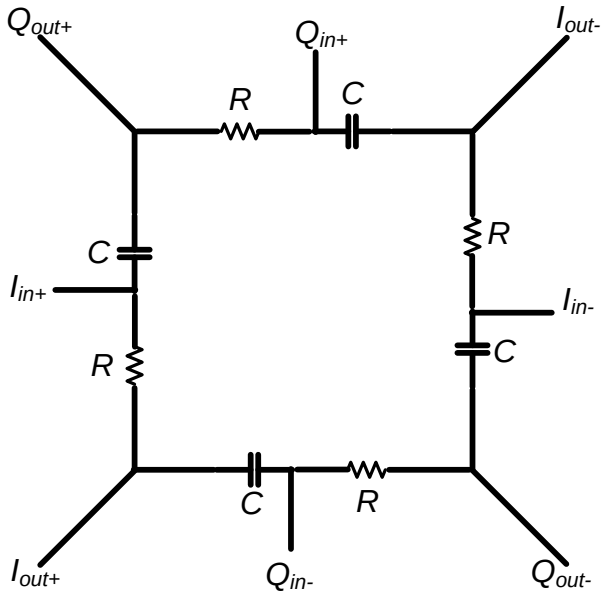


Figure 3. 1 Basic block of RC polyphase filter

So the relationship between the I/Q output is:

$$\frac{Q_{out}}{I_{out}} = \frac{Q_{out+}-Q_{out-}}{I_{out+}-I_{out-}}$$

$$= \frac{H_A(s)\cdot(Q_{in+}-Q_{in-})+H_B(s)\cdot(I_{in+}-I_{in-})}{H_A(s)\cdot(I_{in+}-I_{in-})-H_B(s)\cdot(Q_{in+}-Q_{in-})} = \frac{(Q_{in+}-Q_{in-})+s\cdot R\cdot C\cdot(I_{in+}-I_{in-})}{(I_{in+}-I_{in-})-s\cdot R\cdot C\cdot(Q_{in+}-Q_{in-})}$$

$$= \frac{(Q_{in+}-Q_{in-})+j\cdot\omega\cdot R\cdot C\cdot(I_{in+}-I_{in-})}{(I_{in+}-I_{in-})-j\cdot\omega\cdot R\cdot C\cdot(Q_{in+}-Q_{in-})} \quad (3.3)$$

Suppose $(Q_{in+} - Q_{in-}) = a \cdot (I_{in+} - I_{in-})$ where a is a complex number,

equation (3.3) can be rewritten as:

$$\frac{Q_{out}}{I_{out}} = \frac{a + j \cdot \omega \cdot R \cdot C}{1 - j \cdot \omega \cdot R \cdot C \cdot a} \tag{3.4}$$

Equation (3.4) indicates that for a given RC polyphase filter, the phase difference between I_{out} and Q_{out} is frequency dependent. Obviously in case $\omega \cdot R \cdot C = 1$, equation (3.4) is always equal to j no matter the value of a. This indicates at this frequency I_{out} and Q_{out} have the same amplitude and perfect quadrature phase relationship is established. For arbitrary frequency, two special cases are considered here:

(A): $a = 0$

In this case, equation (3.4) can be simplified as:

$$\frac{Q_{out}}{I_{out}} = j \cdot \omega \cdot R \cdot C \tag{3.5}$$

which indicates the phase difference between I_{out} and Q_{out} is 90 º. Thus quadrature signal I_{out} and Q_{out} are generated from the differential signal pair I_{in+} and I_{in-} while both Q_{in+} and Q_{in-} are grounded.

(B): $a = b \cdot j$ where b is a real number. In other words, this means a is a pure imaginary number.

In this case, equation (3.4) can be simplified as :

$$\frac{Q_{out}}{I_{out}} = \frac{j \cdot (b + \omega \cdot R \cdot C)}{1 - \omega \cdot R \cdot C \cdot b} \tag{3.6}$$

which indicates that the phase difference between I_{out} and Q_{out} is 90 º. Note this phase difference is independent of the value of b, which is the amplitude ratio of the input signal.

Mathematically it can be proved that for any other case, phase difference between I_{out} and Q_{out} is not 90 º.

Note that the magnitude of equation (3.5) and equation (3.6) are not fixed.

For equation (3.5), magnitude is equal to unity only when $\omega = (R \cdot C)^{-1}$. In this case, substitute $I_{in-} = -I_{in+}$ and $Q_{in+} = Q_{in-} = 0$ into equation (3.2), magnitude of the output signals are:

$$|I_{out+}| = |I_{out-}| = |Q_{out+}| = |Q_{out-}| = \frac{|I_{in+}|}{\sqrt{2}} \tag{3.7}$$

which means the output amplitude is always attenuated. Similarly, it can be shown that the magnitude of equation (3.6) is equal to 1 only when $b = \frac{1-\omega \cdot R \cdot C}{\omega \cdot R \cdot C+1}$ or $b = \frac{1+\omega \cdot R \cdot C}{\omega \cdot R \cdot C-1}$.

Since all elements are identical, the input impedance of each terminal is equal. On the other hand, all the output terminals have the same output impedance value. These can be expressed as:

$$Z_{in} = (R + \frac{1}{s \cdot C})//(R + \frac{1}{s \cdot C}) = \frac{1}{2} \cdot (R + \frac{1}{s \cdot C}) \tag{3.8}$$

$$Z_{out} = R//\frac{1}{s \cdot C} = \frac{R}{1+s \cdot R \cdot C} \tag{3.9}$$

Note although the logic flow is similar to that of [77], analysis above is simpler as Kirchhoff's current law is used instead of superposition principle. On the other hand, analysis above also discussed the conditions at which quadrature output is established and the amplitude error under these conditions.

3.1.2 Higher order Polyphase filter

Analysis above shows for an ideal basic building block of the classical polyphase filter, the phase difference between I_{out} and Q_{out} is always 90 º as long the phase difference between I_{in} and Q_{in} is 90 º. This indicates the polyphase filter can also be built by cascading several basic building blocks. For high order RC polyphase filter, the connection between the two adjacent

basic blocks is illustrated in Figure 3.2. Only the Q_{in+} and Q_{in-} terminal of the first block are grounded.

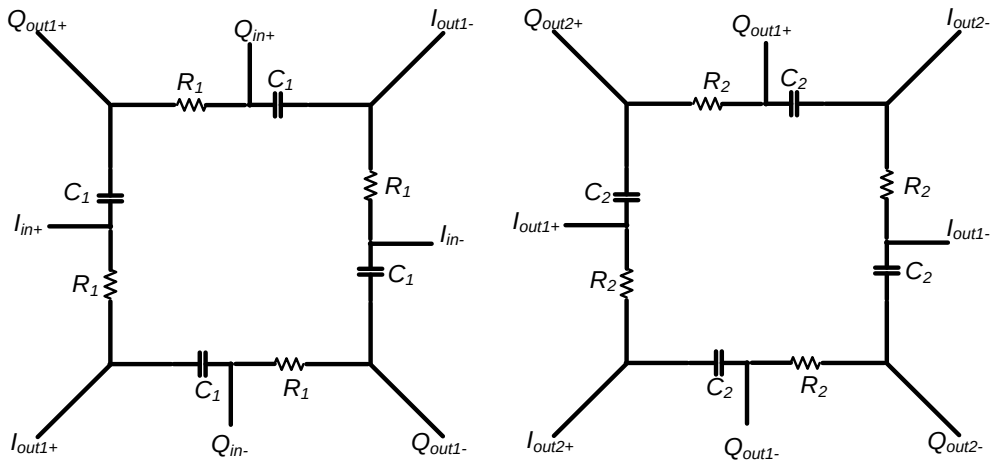


Figure 3. 2 Connection between the two basic block of high order RC polyphase filter

Generally, when two blocks are connected in series as shown in Figure 3.3, the overall transfer function can be derived as:

$$\frac{Y(s)}{X(s)} = H_1(s) \cdot \frac{Z_{in2}}{Z_{out1}+Z_{in2}} \cdot H_2(s) \tag{3.10}$$

where $H_1(s)$ and Z_{out1} are the transfer function and output impendence of the first block, $H_2(s)$ and Z_{in2} are the transfer function and input impendence of the second block.

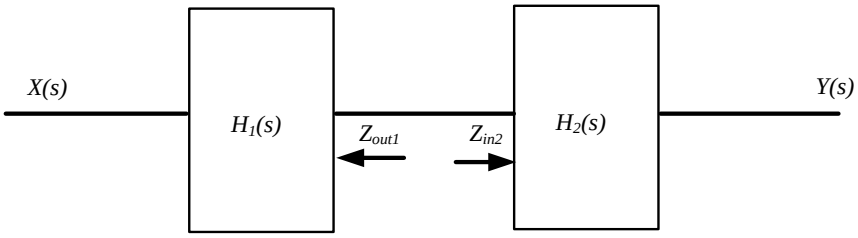


Figure 3. 3 Two blocks in cascade

For the two basic blocks of the polyphase filter connected in series, their individual transfer function and I/O impedance can be calculated according to equation (3.2), (3.8) and (3.9). So the overall transfer function can be calculated according to equation (3.10) as:

$$
\begin{aligned}
&I_{out2+} = H_{2A}(s)\cdot I_{out1+} + H_{2B}(s)\cdot Q_{out1-}\\
&= H_{2A}(s)\cdot p\cdot H_{1A}(s)\cdot I_{in+} + H_{2A}(s)\cdot p\cdot H_{1B}(s)\cdot Q_{in-}\\
&+H_{2B}(s)\cdot p\cdot H_{1A}(s)\cdot Q_{in-} + H_{2B}(s)\cdot p\cdot H_{1B}(s)\cdot I_{in-}\\
&Q_{out2+} = H_{2A}(s)\cdot Q_{out1+} + H_{2B}(s)\cdot I_{out1+}\\
&= H_{2A}(s)\cdot p\cdot H_{1A}(s)\cdot Q_{in+} + H_{2A}(s)\cdot p\cdot H_{1B}(s)\cdot I_{in+}\\
&+H_{2B}(s)\cdot p\cdot H_{1A}(s)\cdot I_{in+} + H_{2B}(s)\cdot p\cdot H_{1B}(s)\cdot Q_{in-}\\
&I_{out2-} = H_{2A}(s)\cdot I_{out1-} + H_{2B}(s)\cdot Q_{out1+}\\
&= H_{2A}(s)\cdot p\cdot H_{1A}(s)\cdot I_{in-} + H_{2A}(s)\cdot p\cdot H_{1B}(s)\cdot Q_{in+}\\
&+H_{2B}(s)\cdot p\cdot H_{1A}(s)\cdot Q_{in+} + H_{2B}(s)\cdot p\cdot H_{1B}(s)\cdot I_{in+}\\
&Q_{out2-} = H_{2A}(s)\cdot Q_{out1-} + H_{2B}(s)\cdot I_{out1-}\\
&= H_{2A}(s)\cdot p\cdot H_{1A}(s)\cdot Q_{in-} + H_{2A}(s)\cdot p\cdot H_{1B}(s)\cdot I_{in+}\\
&+H_{2B}(s)\cdot p\cdot H_{1A}(s)\cdot I_{in-} + H_{2B}(s)\cdot p\cdot H_{1B}(s)\cdot Q_{in+}
\end{aligned}
\tag{3.11}
$$

where

$$H_{1A} = \frac{1}{1+s\cdot R_1\cdot C_1}$$

$$H_{1B} = \frac{s\cdot R_1\cdot C_1}{1+s\cdot R_1\cdot C_1}$$

$$H_{2A} = \frac{1}{1+s\cdot R_2\cdot C_2}$$

$$H_{2B} = \frac{s\cdot R_2\cdot C_2}{1+s\cdot R_2\cdot C_2}$$

$$p = \frac{Z_{in2}}{Z_{out1}+Z_{in2}} = \frac{\frac{1}{2}\cdot(R_2+\frac{1}{s\cdot C_2})}{\frac{R_1}{1+s\cdot R_1\cdot C_1}+\frac{1}{2}\cdot(R_2+\frac{1}{s\cdot C_2})}$$

According to equation (3.11), relationship between the I/Q output can be

derived as:

$$\frac{Q_{out2}}{I_{out2}} = \frac{Q_{out2+}-Q_{out2-}}{I_{out2+}-I_{out2-}} = \frac{F_{12}\cdot(Q_{in+}-Q_{in-})+G_{12}\cdot(I_{in+}-I_{in-})}{F_{12}\cdot(I_{in+}-I_{in-})+G_{12}\cdot(Q_{in+}-Q_{in-})} \quad (3.12)$$

where

$$F_{12} = H_{2A}(s)\cdot p\cdot H_{1A}(s) - H_{2B}(s)\cdot p\cdot H_{1B}(s)$$

$$G_{12} = H_{2A}(s)\cdot p\cdot H_{1B}(s) + H_{2B}(s)\cdot p\cdot H_{1A}(s)$$

Note relationship between F_{12} and G_{12} is:

$$\frac{G_{12}}{F_{12}} = \frac{H_{2A}(s)\cdot p\cdot H_{1B}(s)+H_{2B}(s)\cdot p\cdot H_{1A}(s)}{H_{2A}(s)\cdot p\cdot H_{1A}(s)-H_{2B}(s)\cdot p\cdot H_{1B}(s)} = \frac{H_{2A}(s)\cdot H_{1B}(s)+H_{2B}(s)\cdot H_{1A}(s)}{H_{2A}(s)\cdot H_{1A}(s)-H_{2B}(s)\cdot H_{1B}(s)}$$

$$= \frac{s\cdot R_1\cdot C_1+s\cdot R_2\cdot C_2}{1-s^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2} = \frac{j\cdot\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2} \quad (3.13)$$

which is a pure imaginary number. Simplify $\frac{G_{12}}{F_{12}} = d\cdot j$ where $d = \frac{\omega\cdot(R_1\cdot C_1-R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}$ and is a real number, then equation (3.12) can be reduced to:

$$\frac{Q_{out2}}{I_{out2}} = \frac{Q_{out2+}-Q_{out2-}}{I_{out2+}-I_{out2-}} = \frac{(Q_{in+}-Q_{in-})+d\cdot j\cdot(I_{in+}-I_{in-})}{(I_{in+}-I_{in-})+d\cdot j\cdot(Q_{in+}-Q_{in-})} \quad (3.14)$$

Obviously, equation (3. 14) has the same form as equation (3.3) and similar conclusions can be drawn for $(Q_{in+} - Q_{in-}) = a\cdot(I_{in+} - I_{in-})$:

(A): $a = 0$

In this case, equation (3.14) can be simplified as:

$$\frac{Q_{out2}}{I_{out2}} = d\cdot j = \frac{j\cdot\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2} \quad (3.15)$$

which indicates the phase difference between I_{out2} and Q_{out2} is 90 º. In practice, this means the two basic blocks form a 2nd order polyphase filter and it generates quadrature output signal I_{out2} and Q_{out2} from the differential signal pair I_{in+} and I_{in-} while both Q_{in+} and Q_{in-} are grounded.

(B): $a = b\cdot j$ where b is a real number. In other words, this means a is a pure imaginary number.

In this case, equation (3.14) can be simplified as :

$$\frac{Q_{out2}}{I_{out2}} = \frac{j\cdot(b+d)}{1-b\cdot d} \tag{3.16}$$

which indicates the phase difference between I_{out} and Q_{out} is also 90º. This phase difference is independent of the input signal's magnitude.

Note that the magnitude of equation (3.15) and (3.16) are not constant. For equation (3.15), magnitude is equal to unity only when $\omega = (R_1 \cdot C_1)^{-1}$ or $\omega = (R_2 \cdot C_2)^{-1}$. Let $\omega_1 = (R_1 \cdot C_1)^{-1}$ and $\omega_2 = (R_2 \cdot C_2)^{-1}$. At these two frequencies, substitute $I_{in-} = -I_{in+}$ and $Q_{in+} = Q_{in-} = 0$ into equation (3.11), magnitude of the output signals are:

$$|I_{out+}| = |I_{out-}| = |Q_{out+}| = |Q_{out-}| = |p| \cdot |I_{in+}| \tag{3.17}$$

If R_1 is close to R_2 while C_1 is close to C_2, the magnitude of p is approximately equal to 0.5 (it is equal to 0.5 if $R_1 = R_2$ and $C_1 = C_2$). As a result, in this case the output amplitude is further attenuated compare with the 1st order polyphase filter. For the 2nd order polyphase filter, frequency range between ω_1 and ω_2 is usually called the operating band. Note within this band, the magnitude of equation (3.15) is close to unity. Furthermore, as $\left|\frac{Q_{out2}}{I_{out2}}\right| = \left|\frac{j\cdot\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}\right| = \left|\frac{(R_1\cdot C_1+R_2\cdot C_2)}{\frac{1}{\omega}+\omega\cdot R_1\cdot R_2\cdot C_1\cdot C_2}\right|$. Based on inequality of arithmetic and geometric means, it is obvious that the maximum value occurs at $\omega = \frac{1}{\sqrt{R_1\cdot R_2\cdot C_1\cdot C_2}}$ and at this frequency $\left|\frac{Q_{out2}}{I_{out2}}\right| = \left|\frac{(R_1\cdot C_1+R_2\cdot C_2)}{2\cdot\sqrt{R_1\cdot R_2\cdot C_1\cdot C_2}}\right|$. It can be rewritten as:

$$\left|\frac{Q_{out2}}{I_{out2}}\right| = \left|\frac{(R_1\cdot C_1+R_2\cdot C_2)}{2\cdot\sqrt{R_1\cdot R_2\cdot C_1\cdot C_2}}\right| = \left|\frac{\omega_1+\omega_2}{2\sqrt{\omega_1\cdot\omega_2}}\right| \tag{3.18}$$

For 2.4 GHz ISM band application the frequency range is 2.4 GHz to 2.4835 GHz. If the operating band of a 2nd order polyphase filter is chosen based on this frequency range, it is expected that the maximum amplitude mismatch within this frequency range is only 0.02% . This can be verified by simulation

with circuit designed using ideal elements, as shown in Figure 3.4. Note beyond the operating band, magnitude of $\left|\frac{Q_{out2}}{I_{out2}}\right|$ drops dramatically.

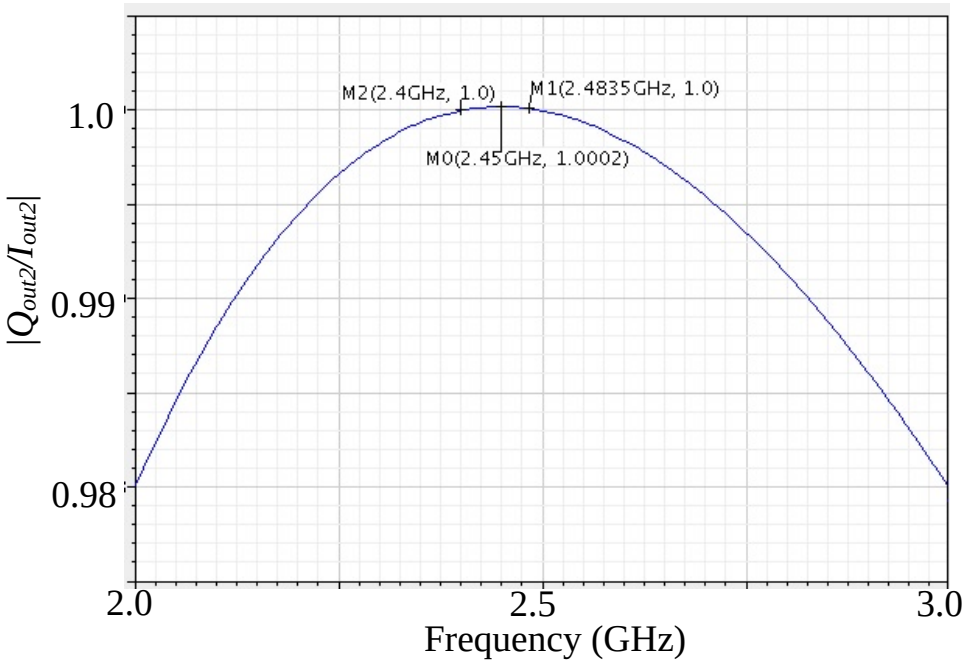


Figure 3. 4 Amplitude mismatch between I/Q signal for poloyphase filter built with ideal elements.

For equation (3.16), magnitude is equal to unity only when $b = \frac{1-d}{1+d}$ or $b = \frac{d+1}{d-1}$. The exact expression is too complicated and will be shown in Appendix.

For the 3rd and higher order polyphase filter, the analysis above is still applicable. However, the expression will be even more complicated than equation (3.11) and (3.12) and will not be mentioned here.

3.1.3 Impact of mismatch between elements

The analysis above assumed each basic block is ideal, e.g. all the resistors and capacitors in one basic block are identical. However this may not be the

case in practice. This section will focus on the impact of these mismatches.

Suppose a pair of capacitor has a variation ΔC, as shown in Figure 3.5.Similar to the analysis shown above, the output signal can be calculated as:

$$I_{out+} = H_A(s) \cdot I_{in+} + H_B(s) \cdot Q_{in-}$$

$$Q_{out+} = H'_A(s) \cdot Q_{in+} + H'_B(s) \cdot I_{in+}$$

$$I_{out-} = H_A(s) \cdot I_{in-} + H_B(s) \cdot Q_{in+}$$

$$Q_{out-} = H'_A(s) \cdot Q_{in-} + H'_B(s) \cdot I_{in-} \quad (3.19)$$

where:

$$H'_A(s) = \frac{1}{1+s \cdot R \cdot (C+\Delta C)}$$

$$H'_B(s) = \frac{s \cdot R \cdot (C+\Delta C)}{1+s \cdot R \cdot (C+\Delta C)}$$

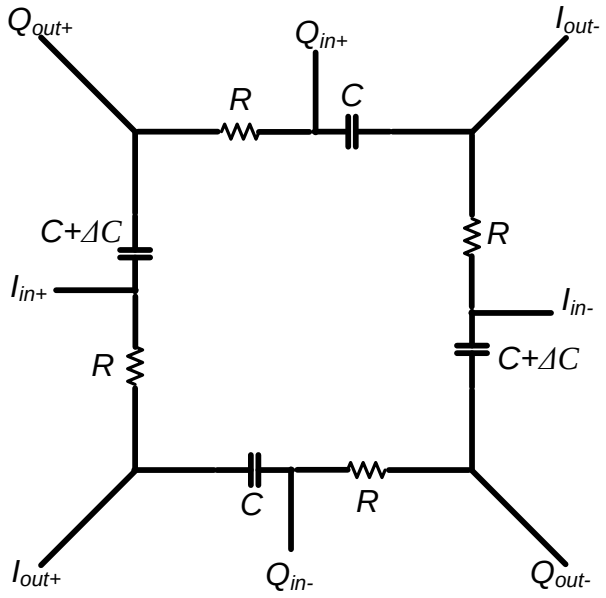


Figure 3. 5 Basic block of RC polyphase filter with variation

So the relationship between the I/Q output is:

$$\frac{Q_{out}}{I_{out}} = \frac{Q_{out+} - Q_{out-}}{I_{out+} - I_{out-}}$$

$$= \frac{H'_A(s) \cdot (Q_{in+} - Q_{in-}) + H'_B(s) \cdot (I_{in+} - I_{in-})}{H_A(s) \cdot (I_{in+} - I_{in-}) - H_B(s) \cdot (Q_{in+} - Q_{in-})}$$

$$= \frac{\frac{1+s\cdot R\cdot C}{1+s\cdot R\cdot (C+\Delta C)}\cdot (Q_{in+}-Q_{in-})+\frac{1+s\cdot R\cdot C}{1+s\cdot R\cdot (C+\Delta C)}\cdot s\cdot R\cdot (C+\Delta C)\cdot (I_{in+}-I_{in-})}{(I_{in+}-I_{in-})-s\cdot R\cdot C\cdot (Q_{in+}-Q_{in-})} \quad (3.20)$$

For equation (3.20), even if $(Q_{in+} - Q_{in-}) = b \cdot j \cdot (I_{in+} - I_{in-})$ where b is a real number, the value is still a complex number. This indicates that the phase difference between I_{out} and Q_{out} is not 90°. In other words, phase error has arisen.

For the case $I_{in-} = -I_{in+}$, $Q_{in+} = Q_{in-} = 0$, equation (3.20) can be simplified as:

$$\frac{Q_{out}}{I_{out}} = \frac{1+s\cdot R\cdot C}{1+s\cdot R\cdot (C+\Delta C)} \cdot s \cdot R \cdot (C + \Delta C) \quad (3.21)$$

Hence the phase of equation (3.21) at $\omega = (R \cdot C)^{-1}$ can be derived as:

$$arg\left(\frac{Q_{out}}{I_{out}}\right) = -\arctan\left(\frac{\Delta C}{2C+\Delta C}\right) + \frac{\pi}{2} \quad (3.22)$$

As $\arctan(\alpha) \approx \alpha$ when α is small, equation (3.22) shows if $\Delta C \ll C$, the phase of equation (3.21) can be estimated as $\frac{\pi}{2} - \frac{\Delta C}{2C}$. Two observations can be made as shown below:

(1): Q_{out} leads I_{out} by more than 90° if $\Delta C < 0$ and by less than 90° if $\Delta C > 0$;

(2): Phase error between I_{out} and Q_{out} (which is defined as $arg\left(\frac{Q_{out}}{I_{out}}\right) - \frac{\pi}{2}$) is proportional to $\frac{\Delta C}{C}$.

On the other hand, at $\omega = (R \cdot C)^{-1}$, the output signal magnitude can be calculated as:

$$|I_{out+}| = |I_{out-}| = \frac{|I_{in+}|}{\sqrt{2}}$$

$$|Q_{out+}| = |Q_{out-}| = |I_{in+}| \cdot \left|\frac{j\cdot R\cdot (C+\Delta C)}{R\cdot C + j\cdot R\cdot (C+\Delta C)}\right| \quad (3.23)$$

and the amplitude ratio between I/Q outputs is:

$$\frac{|Q_{out}|}{|I_{out}|} = \sqrt{2} \cdot \left| \frac{j \cdot R \cdot (C+\Delta C)}{R \cdot C + j \cdot R \cdot (C+\Delta C)} \right| \tag{3.24}$$

which is not equal to 1 and indicates an amplitude error has arisen. Note it can be derived that $\frac{|Q_{out}|}{|I_{out}|}$ increases with $\frac{\Delta C}{C}$.

Polyphase filter with an operation frequency of 2.4 GHz is designed. The simulated phase error and amplitude error between Q_{out} and I_{out} at 2.4 GHz versus $\Delta C/C$ is shown in Figure 3.6. As analyzed above, ΔC introduces both the phase error and the amplitude mismatch. As predicted by equation (3.22), phase error is proportional to $\frac{\Delta C}{C}$. Phase error is positive when $\frac{\Delta C}{C} < 0$ and vice versa. On the other hand $\frac{|Q_{out}|}{|I_{out}|}$ increases with $\frac{\Delta C}{C}$, as predict by (3.24).

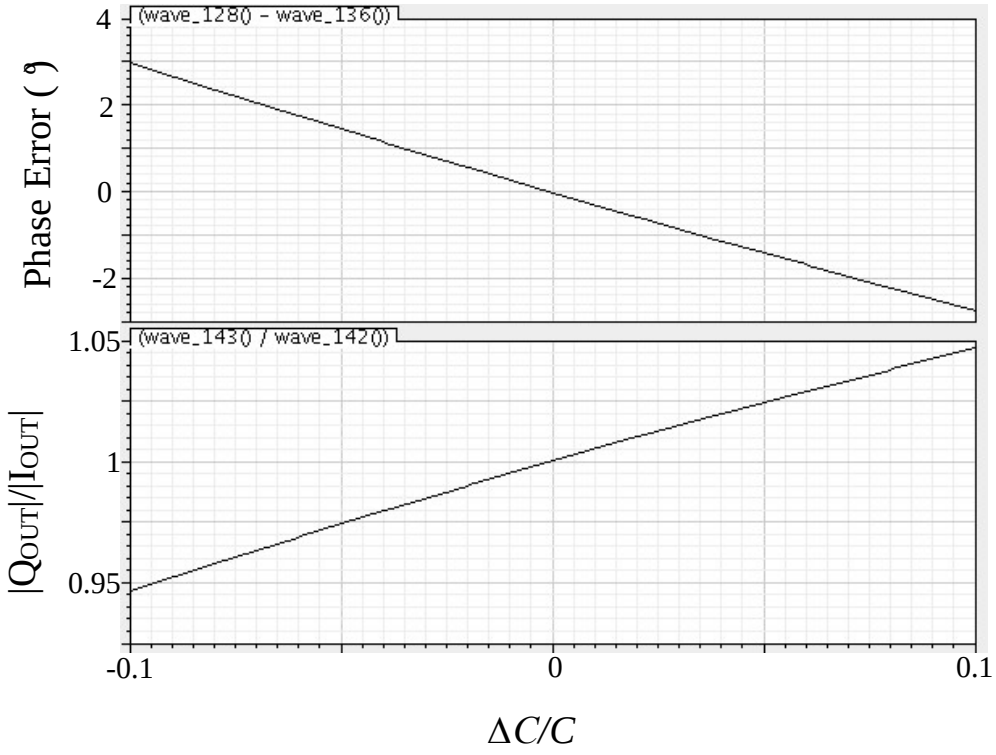


Figure 3. 6 Phase Error and Amplitude Error between $Q_{out}$and I_{out} of RC polyphase filter with variation versus $\Delta C/C$

The analysis above considered the variation of capacitors in a simple and

symmetrical manner only. However, in practice variation is much more complicated and can be in both the resistors and capacitors. Detailed analysis is too complicate and will not be shown here. Generally, these variations can introduce both phase error and amplitude mismatch. Tuning of all elements to reduce these non-ideal effects may require extra digital processing blocks, as shown in [58].

In general, the passive polyphase filter can generate quadrature output from differential input with low power consumption. Regardless of the number of stages, the phase accuracy of polyphase filter's output is perfect in ideal case. As the number of cascaded stages increases, the bandwidth of the operating band becomes wider. However, amplitude attenuation also increases with the number of stages. To compensate the signal loss, an amplifier is usually inserted, which causes extra power consumption. Besides, since the I/O impedance of the passive polyphase filter which are shown by equation (3.8) and (3.9) are normally low, I/O buffers are usually required. These buffers introduce parasitic effects which may deteriorate the phase accuracy [57]. It is worth noting that even in the ideal case, amplitude mismatch may still occur as analyzed previously. In addition, the passive polyphase filter usually has a narrow operating band [59][60]. On the other hand, active polyphase filter is suitable for wideband application and can provide gain to the signal at the price of higher power consumption. The operation of the active polyphase filter is similar to that of the passive polyphase filter where the active filters are replaced with the RC only filter in the passive design[60][61].

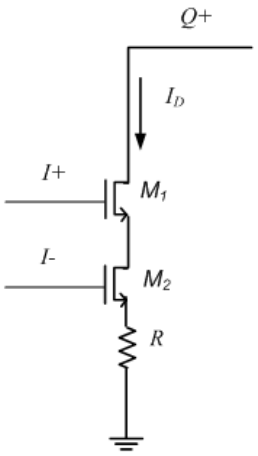
3.2 Quadrature VCO

The idea of cross-coupled quadrature VCO was first proposed by Rofougaran *et al* in 1996 [62]. Subsequently, this topology has motivated many researchers to devise the modified structures for better performance. Therefore, many variations of the cross-coupled quadrature VCO with low phase noise and small phase error has been proposed so far. Most of these circuits commonly adopt auxiliary active devices such as NMOS or PMOS transistor to realize the cross-coupling [63]. The coupling between the two VCOs can be accomplished in parallel [parallel quadrature VCO (PQVCO)] [64] or in series [series quadrature VCO (SQVCO)] with the core $-G_m$ transistor pair [65]. In [6], the principle of quadrature signal generation is analyzed in detail. Besides, the super-harmonic-coupled (SHC) QVCO [66~68] uses the 2^{nd} harmonic of the VCO's output to realize coupling. Each topology has its own advantages and disadvantages. The SQVCO topology reduced the contribution of the coupling transistor's channel noise through degeneration at the expense of reduced tuning range, transconductance and oscillation frequency while the coupling transistors does not require additional bias current. On the other hand, the PQVCO couples the signal more efficiently, but suffers from a critical trade-off between phase noise and I/Q phase accuracy while consumes more power [6]. Both the SQVCO and PQVCO operate away from the resonant frequency to create the required phase shift and this penalizes their FoM. Although this problem does not exist in SHC QVCO, but this topology is not particularly effective in reducing phase noise [57]. In [69] and [70], the tank signal is coupled through the back-gates of the core transistors using non-conventional CMOS technology. Such QVCO topology is called back-gate coupled (BGC) QVCO.

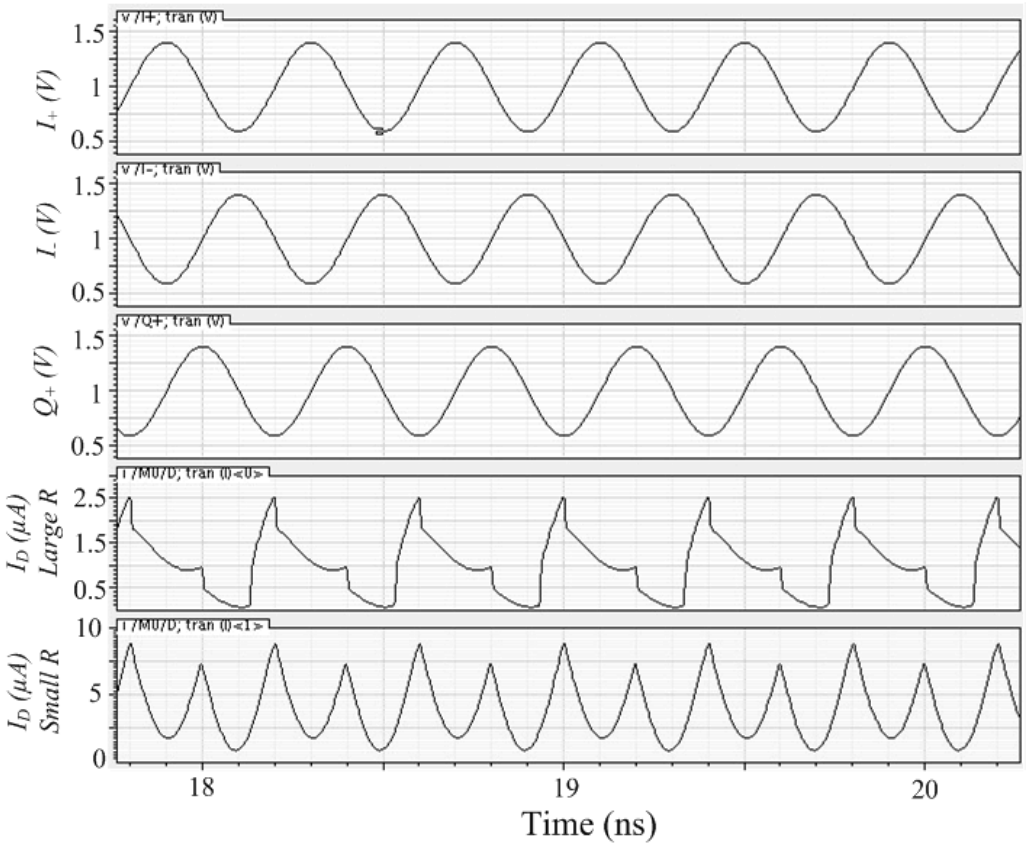
Recently, a few IPC QVCO are proposed. The effect of introducing a large phase shift on the coupling signal of the conventional PQVCO is first analyzed in [71]. It shows phase noise is significantly improved as the upconversion of the flicker noise is eliminated. It is also shown that the phase accuracy is improved by this phase shift. Theoretically the performance in terms of phase noise and phase error is fully optimized when the phase shift is 90°. Based on this conclusion, the idea of in-phase coupling has been developed.

The key feature of IPC QVCO is to generate in-phase signal for coupling purpose. The most straight forward approach is using the RC-CR phase shifter, the mechanism of which has been discussed intensively in previous section. This approach is adopted in [71]. An obvious drawback of this approach is that the actual phase shift of the coupling signal is frequency dependent. In addition, for the topology proposed in [71], the RC network is in parallel with the LC tank and reduces the parallel resistance R_P of the resonator. This results in a lower Q and degrades the phase noise performance. To alleviate this Q degradation, a large resistor should be chosen for the RC network.

On the other hand, it is noteworthy that the zero-crossing point of the I signal and the peak/valley of the Q signal happens simultaneously and vice versa. This property indicates for the circuits shows in Figure 3.7(a), component of I_D at the fundamental frequency is in antiphase with the voltage Q_+, as shown in Figure 3.7(b). For the cross-coupled VCO, phase of current that flows through the Q_+ is in antiphase with the voltage waveform of Q_+, hence this circuit can be used to generate in-phase signal.



(a)



(b)

Figure 3. 7 In phase coupling signal generation circuit (a) and transient simulation result (b).

However the degeneration resistor R should be large enough to force transistor M_2 to enter the triode region when Q_+ is high, otherwise I_D will

exhibit peaks at both the maximum and the minimum of Q_+, as shown in Figure 3.7(b). Such approach has been suggested in [72]. However the coupling circuitry proposed in [72] consumes considerable DC power.

In modern transistor technology, the carrier drift velocity saturates when V_{DS} is larger than the saturation drain voltage $V_{DS,sat}$, which is usually smaller than the threshold voltage. According to [73], in this condition the drain current changes proportionally to V_{GS}. On the other hand, for voltage I_+, I_- and Q_+ mathematically $(I_+ - Q_+) + (I_- - Q_+)$ if I_+ and I_- are precisely differential and the DC offset is ignored. Thus it is possible to design proper current model circuit to utilize equation above to generate in-phase coupling signal. One such example is proposed in [74]. However all the approaches above cannot perform phase error tuning, the role of which is analyzed below.

3.3 Tuning of the I/Q signal

As mentioned on Page 41, I/Q mismatch degrades the IRR thus affects the performance of the receivers. Digital Signal Processing (DSP) is commonly used to overcome the I/Q mismatch, as illustrated in [75~77]. However, an analog approach to achieve I/Q balance is still desirable. Such analog tuning reduces the DSP computation requirements and could reduce the overall power consumption of an integrated RF receiver [78].

In [78], a tunable polyphase filter is proposed. By tuning the value of the series output capacitance of the polyphase filter, the overall transfer function is tuned thus the phase of each output signal is adjusted. The structure is simple and requires virtually no current consumption. However, each output node

needs to be tuned individually and the tuning process is iterative. Furthermore, the proposed tuning method focuses on the phase error while the amplitude error cannot be guaranteed.

On the other hand, based on the analysis for PQVCO in [6], phase error and amplitude mismatch can be tuned separately while not affecting each other. Analysis in [6] shows the phase error can be corrected by deliberately introducing a mismatch between the conductances of the core transistor pair. It is also shown that the amplitude mismatch will not be affected by this operation. The deliberately introduced mismatch between the conductances of the core transistor pair can be controlled by adjusting the bias current of this transistor pair. However this phase tuning scheme is valid for conventional PQVCO only. Besides, the phase tuning range is directly related to the coupling factor of the PQVCO, which parameter is chosen based on the trade-off between the phase accuracy and the phase noise performance. As a result, the phase tuning range is limited. Furthermore, the impact of parasitic elements is ignored in the analysis.

Phase tuning scheme for a SHC QVCO topology has been proposed in [7]. Similar to [6], the source of phase error for the SHC QVCO is analyzed first and the idea of phase tuning is developed based on this analysis. An LC network consisting of an inductor and a varactor is inserted between the common ground point and the current source of each VCO core. Phase tuning is realized by tuning this LC network. Major drawback of this phase tuning scheme is that it requires an additional inductor and a varactor which occupy large area. Furthermore, as there are various methods to realize super harmonic coupling for QVCO, this approach may not be applicable for other SHC QVCO

topology.

As the principle of quadrature signal generation for QVCO varies between different QVCO topologies, the source of phase error and their impact should be studied case by case. Hence phase tuning scheme for a particular QVCO topology should be based on the analysis of phase error for this topology. Thus it is still challenging to design a QVCO with good performance and tunable phase error.

3.4 Summary

In this chapter, the fundamental of the quadrature signal is introduced, followed by the advantages and the necessity of employing the quadrature signal in modern transceiver topology and design. Advantages and disadvantages of different quadrature signal generation methods are studied and then two approaches are focused on, the polyphase filter and QVCO.

In Section 3.1, the transfer function of the 1st order polyphase filter is derived first based on basic Kirchhoff's law. Based on this transfer function, condition for quadrature signal generation is determined. Secondly, based on the analysis for the 1st order polyphase filter, the 2nd order polyphase filter is studied in terms of the transfer function and condition for quadrature signal generation. Furthermore, phase/amplitude error due to mismatch between elements are analyzed. In addition, QVCO circuit for quadrature signal generation is studied in Section 3.2. Different coupling methods for QVCO are reviewed with their advantages and disadvantages.

Based on these analyses, phase tuning schemes for different I/Q signal

generation methods are discussed in Section 3.3. It is noteworthy that a specific phase error tuning scheme should be developed for a particular QVCO topology.

CHAPTER 4

A 2.4 GHz VCO with Novel Hybrid Type Automatic Amplitude Calibration Loop

As discussed in Chapter 2, AAC loop contributes many attractive features in optimizing the performance of the VCO. However, both the two conventional types of AAC loop, namely analog type AAC and digital type AAC, have their own drawbacks.

In this chapter, a novel hybrid type AAC loop is proposed and implemented with a 2.4 GHz VCO. The proposed hybrid type AAC loop maintains advantages of both the conventional analog type AAC and digital type AAC while overcoming their individual disadvantages. This work is implemented using GlobalFoundries CMOS 0.18 μm CMOS technology.

4.1 Introduction of the proposed hybrid AAC VCO

In Section 2.7, basic idea of AAC loop is introduced. Based on this idea, two major conventional AAC topologies are developed. Both their advantages and disadvantages are analyzed and will not be repeated here.

As discussed in [2], the near open nature of the loop makes the digital type AAC VCO free of the stability problem. This is because the intermediate signal is digitalized by the comparator and all the following blocks processes with the digitalized signal. In addition, the near open nature of the loop also prevents noise generated by the blocks before the comparator propagating to the following blocks. As a result, the total noise introduced by the loop is reduced

and the design requirement of the PD is relaxed. In summary, the benefits of the digital type AAC based on the digitization of the intermediate signal.

A digital type AAC tunes the bias current of the VCO core discretely. This is because the digital control signal only decides the on/off state of each current source in the bias current array of the VCO core. Hence fine tuning of the VCO's amplitude will require a large current source array. On the contrary, analog type AAC tunes the bias voltage of the tail current source transistor of the VCO core directly, so the bias current I_T of the VCO core is tuned continuously.

To maintain the advantages of both conventional AAC types, analysis above shows that the intermediate signal should first be digitalized by the comparator. After some processing, the digital intermediate signal should be converted back into analog signal by the Digital-to-Analog Convertor (DAC) to tune the bias voltage of the tail current source transistor directly. The data flow diagram is shown in Figure 4.1, in which signal V_{VCO}, V_{PD}, V_{REF} and V_{ADJ} are all analog signal. Only signal between the comparator and the DAC are digitalized.

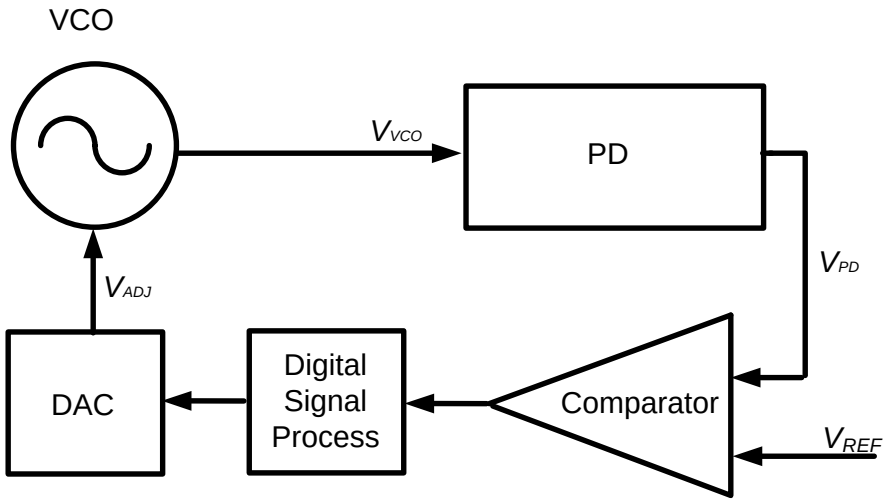


Figure 4. 1 Block diagram of the proposed hybrid type AAC VCO

4.2 Operation and analysis of the proposed hybrid AAC VCO

As discussed above, the digitalized intermediate signal generated by the comparator goes through some digital signal processing first. For the proposed AAC VCO, the digital signal processor includes a state machine that decides the direction the amplitude should be tuned. A DAC block is necessary to convert the state output of the state-machine to analog signal V_{ADJ} which tunes the bias current of the VCO core directly. In this design, a Charge Pump (CP) works as a state machine whose logical combination will be shown in Section 4.2.1. With proper load, CP can also works as a DAC.

4.2.1 Overall schematic and operation

Schematic of the proposed AAC VCO is shown in Figure 4.2. The operation of the AAC circuit is explained as follows.

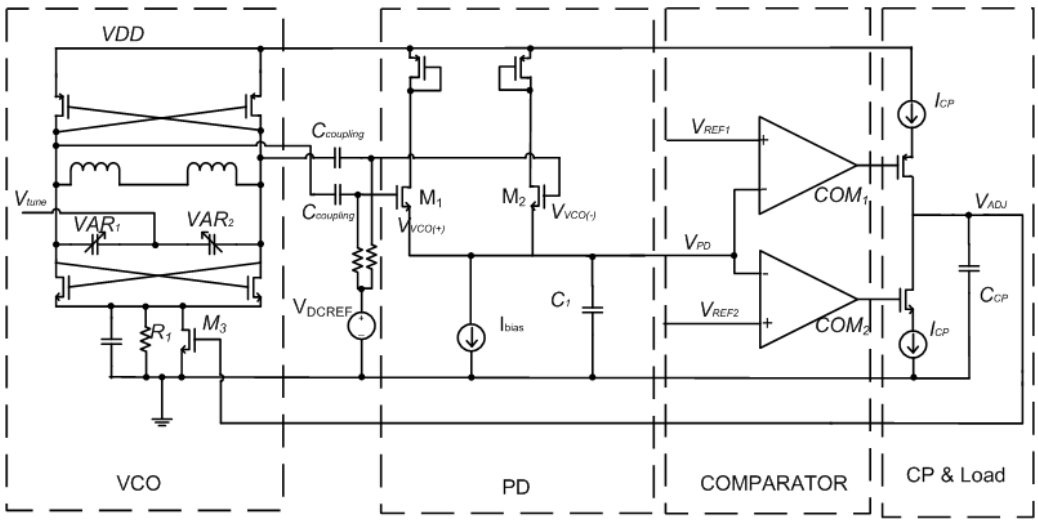


Figure 4. 2 Schematic of the proposed hybrid type AAC VCO

The schematic of the proposed AAC VCO can be mainly divided into four major blocks, namely VCO, PD, Comparator and CP with load.

Before feeding into the PD, the DC level of the VCO's output is first set to a fixed level V_{DCREF} by a pair of AC coupling structure. This ensures the output of the PD, V_{PD}, varies only according to the VCO's output amplitude, V_{VCO} and insensitive to DC variation of the VCO's output. As mentioned above, the role of the PD is to generate a DC signal V_{PD} that is proportional to V_{VCO}. Relationship between V_{PD} and V_{VCO} can be expressed as:

$$V_{PD} = V_{VCO} \cdot K_{PD} + V_{OFFSET} \tag{4.1}$$

where K_{PD} is defined as "gain of PD" and V_{OFFSET} is the offset output voltage of the PD.

V_{PD} is then compared with a pair of externally set voltage reference, namely V_{REF1} and V_{REF2} ($V_{REF1} < V_{REF2}$), through a pair of identical comparators. For each comparator, if voltage at the positive input terminal is higher than that at the negative input terminal, the output is "low" or "0". Otherwise the output is "high" or "1". As shown in Figure 4.1, COM_1 and COM_2 are outputs of the two comparators. Both of the outputs are state variable. In steady state, the value of V_{PD} should remain at a constant level between V_{REF1} and V_{REF2}, in other words $V_{REF1} < V_{PD} \leq V_{REF2}$, results into $COM_1 =$ "1" and $COM_2 =$ "0". Truth table of COM_1 and COM_2 is shown in Table 4.1:

Table 4.1: Truth table for COM_1 and COM_2

	COM_1	COM_2
$V_{PD} \leq V_{REF1}$	0	0

$V_{REF1} < V_{PD} \leq V_{REF2}$	1	0
$V_{REF2} < V_{PD}$	1	1

Since V_{REF2} is higher than V_{REF1}, logically COM_2 cannot be equal to "1" while COM_1 is equal to "0".

The voltage region defined by V_{REF1} and V_{REF2} is called "$V_{PDrange}$". It is converted from a pre-determined desired voltage amplitude range $V_{VCOrange}$, whose lower boundary is V_{VCO1} and higher boundary is V_{VCO2}. According to equation (4.1), following relationship can be obtained:

$$V_{REF1} = V_{VCO1} \cdot K_{PD} + V_{OFFSET}$$

and

$$V_{REF2} = V_{VCO2} \cdot K_{PD} + V_{OFFSET} \quad (4.2)$$

COM_1 and COM_2 are then used to control the state of CP. As indicated in Figure 4.1, CP provides a charging current whose value is I_{CP} when $COM_1 =$ "0" and provides a discharging current whose value is also I_{CP} when $COM_2 =$ "1". Since COM_2 cannot be equal to "1" while COM_1 is equal to "0", CP will never provide charging current and discharging current simultaneously. On the other hand, as mentioned above, logic combination of $COM_1 =$ "1" and $COM_2 =$ "0" indicates $V_{REF1} < V_{PD} \leq V_{REF2}$ or V_{PD} is within $V_{PDrange}$. In this case, CP is totally turned off and provides no current. Since the output current of CP is state-depended, it can be treated as a FSM.

Current provided by CP is converted to V_{ADJ} through the load capacitor C_{CP}. A simple capacitor is adequate for this design. For simplicity, in the quantitative analysis below, only the charging case is considered (for the discharging case quantitative analysis is similar with an opposite I_{CP} polarity).

The increment of V_{ADJ} according to charging time t can be derived as:

$$\Delta V_{ADJ} = \frac{1}{C_{CP}} \cdot I_{CP} \cdot t \tag{4.3}$$

Suppose the transconductance of transistor M_3 in Figure 4.2 is g_{m3}, then increment of VCO core's bias current I_T is:

$$\Delta I_T = \Delta V_{ADJ} \cdot g_{m3} = \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot t \tag{4.4}$$

Refer to equation (2.20), in steady state V_{VCO} is proportional to I_T . So the increment of V_{VCO} is:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \Delta I_T \cdot R_{eq} = \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \cdot t \tag{4.5}$$

where R_{eq} is the equivalent parallel resistance of the tank.

The increment of V_{PD} can be calculated according to equation (4.1) as:

$$\Delta V_{PD} = \Delta V_{VCO} \cdot K_{PD} = \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \cdot K_{PD} \cdot t \tag{4.6}$$

The term $\frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq}$ in equation (4.5) and (4.6) determines the rate of change for both V_{VCO} and V_{PD}. In the following section, this term will be referred to as CR.

For the derivation of equation (4.3) to equation (4.6), it is assumed that the CP is always in charging state or both COM_1 and COM_2 are equal to "0". If the states of COM_1 and $COM_2$are considered, equation (4.5) can be rewritten as:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \Delta I_T \cdot R_{eq}$$

$$= \frac{4}{\pi} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \cdot [t_1 \cdot (\overline{COM_1} \cap \overline{COM_2}) - t_2 \cdot (COM_1 \cap COM_2) \tag{4.7}$$

in which t_1 is the duration for both COM_1 and COM_2 are equal to "0" and t_2 the duration for both COM_1 and COM_2 are equal to "1" .

It is clear that equation (4.7) is a state-dependent equation and cannot be

transferred from time domain to frequency domain. In addition, the loop is closed only when V_{VCO} is out of the desired range defined by $V_{VCOrange}$. Otherwise both switches of CP are open hence the whole loop works as an open loop. Thus although the proposed hybrid type AAC looks similar to the Charge-Pump Phase-Locked Loop (CPLL), the close loop frequency domain analysis which is common for CPLL is not applicable for this AAC loop. A transient analysis will be given in the Section 4.2.4.

Another assumption made during the derivation above is an ideal case that all voltage/current change simultaneously, e.g. when there is a step increment of ΔV_{VCO} at the VCO's output amplitude, a corresponding step increment ΔV_{PD} appears at PD's output node immediately. However, in practice V_{PD} is changed by charging the load capacitor, C_1, of the PD. This charging process requires some time to complete and a delay is thus introduced. Although this delay may seems trivial, but its effect is critical particularly when V_{VCO} crosses the boundary of $V_{VCOrange}$. In ideal case, at the moment when V_{VCO} has just reached V_{VCO1}, V_{PD} will change to V_{REF1} instantly and hence CP is turned off immediately, thus the V_{ADJ} signal remains unchanged. In practice, due to the delay introduced by the charging process mentioned above, after V_{VCO} has reached V_{VCO1}, V_{PD} still needs a certain time t_{delay} to reach V_{REF1}. During this duration V_{PD} is still lower than V_{REF1} hence CP continues to provide a charging current to increase V_{ADJ}. As a result, V_{VCO} keeps on increasing until V_{PD} reaches V_{REF1} and shuts down CP. If V_{VCO} changes too drastically, it may exceed V_{VCO2} before V_{PD} reaches V_{REF1}. This will start another amplitude calibration process and may further leads to instability called "squegging" as mentioned previously. To the author's knowledge, this critical delay effect was never examined in

previous AAC VCO.

To prevent the squegging phenomenon, both the value of C_1 and CR should be selected properly and there is a trade-off between the calibration speed (which is determined by CR) and stability. Furthermore, the desired voltage range, $V_{VCOrange}$ and $V_{PDrange}$ which determines the calibration accuracy, cannot be arbitrarily small. These will be discussed in detail in Sections 4.2.4.

4.2.2 Operation of the VCO core

Schematic of the VCO core is shown in Figure 4.3 which is basically a conventional CMOS LC VCO. Resistor R_1 works as the main current source to reduce total flicker noise power that upconverted to phase noise. Transistor M_3 acts as the auxiliary current source which can be tuned by V_{ADJ}. A capacitor is placed in parallel with the tail current source to further improve the noise performance as discussed in [31]. It is pointed out in [41] that the output impedance of the tail-current source at high frequencies is reduced by this capacitor, which made the VCO sensitive to the variation of the supply voltage. However, this is not a problem for AAC VCO since the supply voltage variation will be compensated by the AAC loop itself.

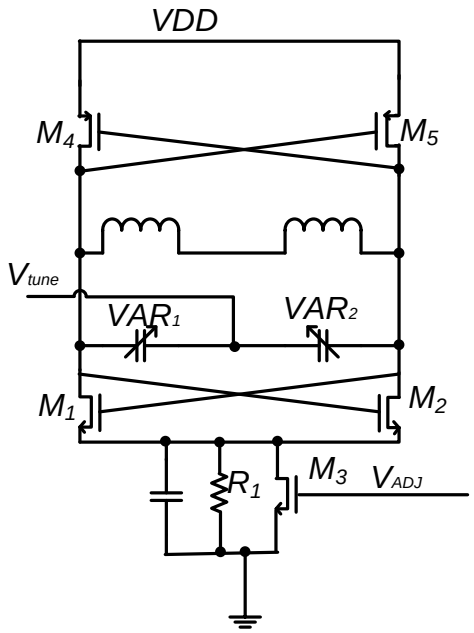


Figure 4. 3 The Schematic of the VCO core

Performance of the VCO is optimized according to the design and optimization method for LC VCOs proposed in [33]. Size of both PMOS and NMOS cross-coupled pair is carefully selected to provide a symmetrical output waveform. Dimensions of all devices are shown in Table 4.2.

Table 4.2: Components in the VCO core

Inductor	2 nH
Varactor	Tunable from 0.6 pF to 0.85 pF
Capacitor	15 pF
R_1	400 Ω
M_1 & M_2	24 µm/0.18 µm
M_3	80 µm/1 µm
M_4 & M_5	60 µm/0.18 µm

The VCO core is simulated with Cadence SpectreRF. Tuning range of the VCO core is 2.3 GHz to 2.7 GHz. Optimized phase noise is -95 dBc/Hz at 100

kHz offset. As shown in Figure 4.4, the tail capacitor helps to improve the phase noise performance of the VCO core, and more significantly at close-in offset frequency. The phase noise improvement is 5 dBc/Hz at 100 kHz offset frequency and reduces to 3 dBc/Hz at 1 MHz offset frequency. Optimized output peak amplitude is selected as 200 mV (at the output of buffer which is not shown in Figure 4.3). Note this optimized output peak amplitude is achieved when M_3 is turned on and current consumption of the VCO is 2.2 mA from 1.8 V voltage supply. Amplitude variation across the tuning range when V_{ADJ} is kept at 0 V is shown in Figure 4.5. Maximum variation is about 40 mV.

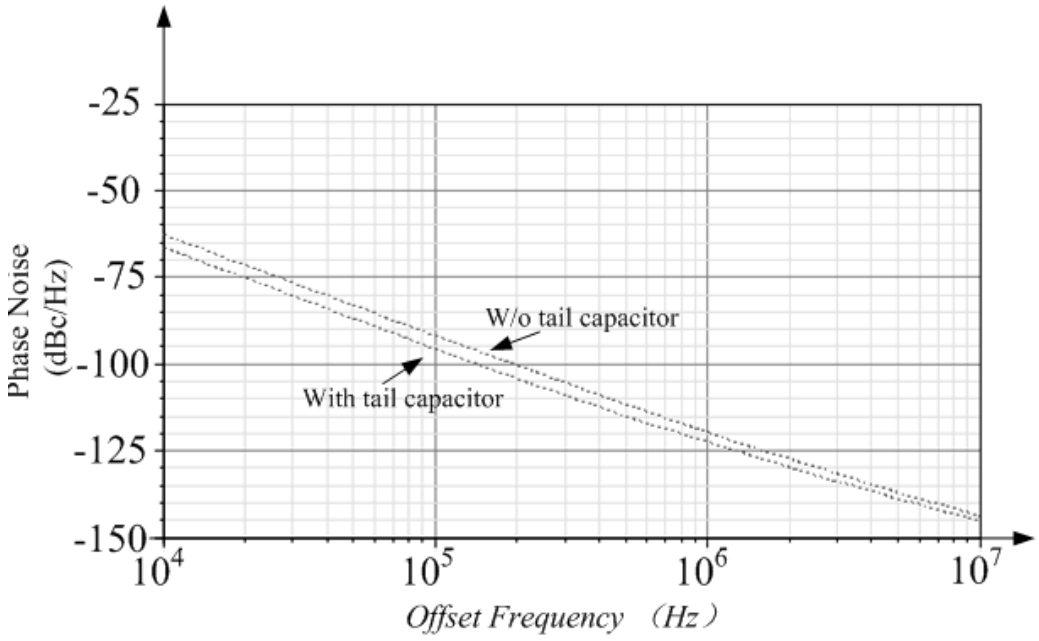


Figure 4. 4 Optimized phase noise performance of the VCO core

As mentioned in earlier section, due to the digitization of the intermediate signal by the comparator pair, noise generated by PD cannot propagate to the following blocks (feed forward), as shown in Figure 4.6. This can be verified by simulation. The circuit shown in Figure 4.7 is for comparison purposes. For fair comparison, circuit is opened between the VCO core and CP. A dummy VCO

is used as the load of CP. The gate of the auxiliary current source transistor is connected to an ideal DC source, whose voltage is the same as the V_{ADJ} in Figure 4.6.

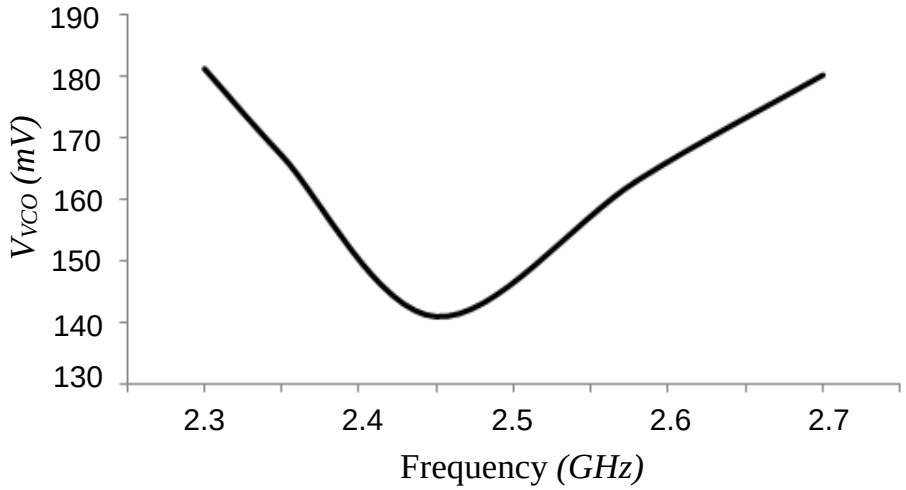


Figure 4. 5 V_{VCO} versus Frequency of the VCO core with $V_{ADJ} = 0V$

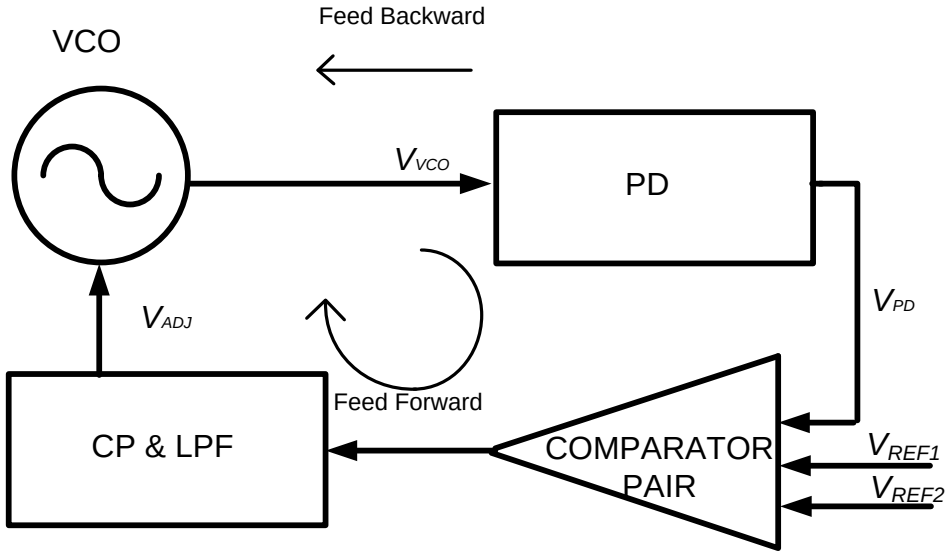


Figure 4. 6 Noise propagation direction within AAC VCO

Compare with simulation result of Figure 4.6, oscillation frequency of Figure 4.7 varies by 0.01% and total noise power at 1 MHz offset frequency increases

by 0.3%, which means phase noise at this offset frequency degrades by 0.013 dB. Both values are very small and can be neglected.

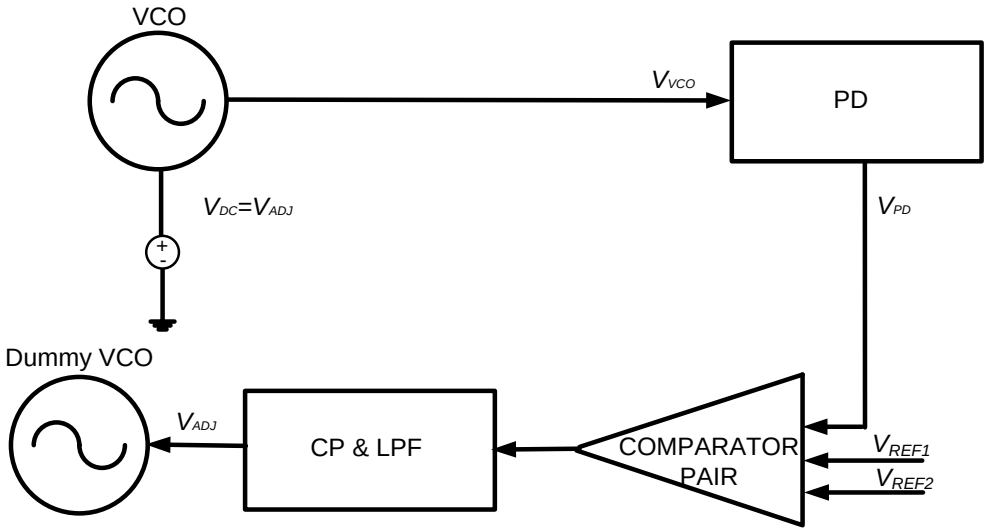


Figure 4. 7 Circuit set-up with no forward noise propagation

However, noise generated by PD can still affect the VCO core in another way. Since the VCO core and PD are connected directly, noise from PD can feed backward to the VCO core. This can be explained with the help of Figure 4.8.

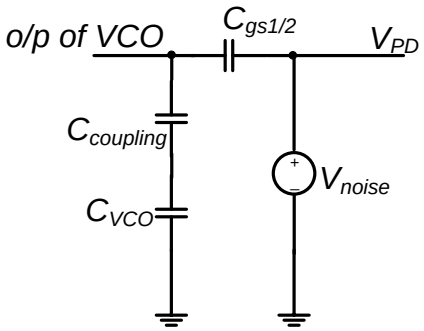


Figure 4. 8 Simplified schematic showing the noise propagation from PD to the VCO core

According to Figure 4.8, noise voltage at the output terminal of the VCO core can be calculated as:

$$V_{op\_noise} = V_{noise} \cdot \frac{\frac{1}{C_{coupling}}+\frac{1}{C_{VCO}}}{\frac{1}{C_{coupling}}+\frac{1}{C_{VCO}}+\frac{1}{C_{gs1/2}}} \tag{4.8}$$

where V_{noise} is the noise voltage at the output terminal of PD, $C_{coupling}$ is the capacitance of the AC coupling structure between the VCO core and PD, C_{VCO} is the total capacitance looking into the VCO's output terminal and $C_{gs1/2}$ is the parasitic gate-source capacitance of transistor M_1 and M_2. Both the high frequency and low frequency noise components are fed backward. The high frequency components whose frequencies are at the 2nd harmonic of the VCO's output frequency are down-converted to phase noise by the cross-coupled transistor pair. On the other hand, due to the non-linear effect of the varactors and transistors of the VCO, low frequency components are upconverted into phase noise. Mechanism of such upconversion process is explained in detail in [21] and [79].

Fortunately, since $C_{gs1/2}$ is usually much smaller than both $C_{coupling}$ and C_{VCO}, so the ratio of V_{op_noise}/V_{noise} is usually small. Hence the noise contribution of this feedback noise is not very significant. With the help of "noise summary" function in SpectRF, noise contribution of each source can be identified through simulation. It shows total noise contribution from PD is about 10%, or equivalent to 0.4 dB of total phase noise degradation. Since the low frequency components of V_{noise} is dominated by flicker noise, it can be reduced by using resistor as PD's current source and by properly sizing the PD's transistors.

4.2.3 Operation of PD

The role of PD in the AAC loop is to generate a DC signal V_{PD} that is

proportional to VCO's output amplitude V_{VCO}. As mentioned in previous section, the DC level of V_{VCO} is fixed to V_{DCREF} by AC coupling structure before feeding to PD, thus DC level variation of V_{VCO} will not affect V_{PD}. In addition, the gain of PD, K_{PD} should be designed to be a constant over the tuning range of the VCO core.

The simplified schematic of PD used in the proposed AAC VCO is shown in Figure 4.9. The resistor pair R_1 shown is just for biasing purpose. Analysis of PD's operation is shown below.

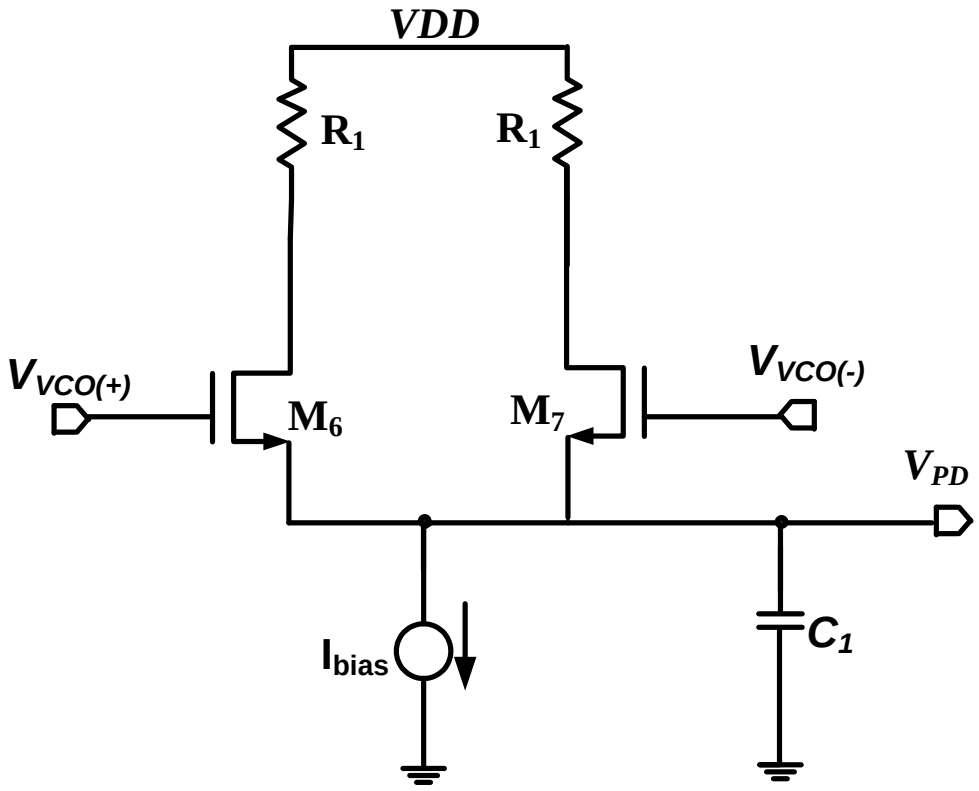


Figure 4. 9 Simplified schematic of PD used in the proposed AAC VCO

Let the value of V_{PD} when V_{VCO} is 0 to be $V_{PD}(0)$. When V_{VCO} increases, V_{PD} will deviate from $V_{PD}(0)$. In the analysis below, four assumptions are made for simplicity:

(A1): The tail current source is ideal. In other words, the resistance of this current source is infinite;

(A2): PD is properly biased so that during one cycle of V_{VCO}, both transistor M_6 and M_7 are "on" for half cycle;

(A3): There is no overlap between the "on" state of M_6 and M_7;

(A4): V_{PD} changes only at the end of each input signal cycle, such that V_{PD} changes discretely in a small step each time. It is still acceptable if the total number of input signal cycles required for V_{PD} to reach the final stable value is large enough. Based on this assumption, the value of V_{PD} at the end of *n*-th cycle is labeled as $V_{PD}(n)$.

With the assumptions made above, total charge injected into the load capacitor C_1 during the *n+1*th input cycle can be calculated as:

$$Q = 2 \cdot g_{m6/7} \cdot \int_0^{\frac{1}{2f}} \{V_{VCO} \cdot \sin(2\pi f t) - [V_{PD}(n) - V_{PD}(0)]\} dt \tag{4.9}$$

where $g_{m6/7}$ is the transconductance of transistor M_6 and M_7, f is the frequency of V_{VCO}. So the voltage difference between $V_{PD}(n+1)$ and $V_{PD}(n)$ can be expressed as:

$$V_{PD}(n+1) - V_{PD}(n) = \frac{Q}{C_1}$$

$$= \frac{2}{C_1} \cdot g_{m6/7} \cdot \int_0^{\frac{1}{2f}} \{V_{VCO} \cdot \sin(2\pi f t) - [V_{PD}(n) - V_{PD}(0)]\} dt \tag{4.10}$$

It can be simplified as:

$$V_{PD}(n+1) - V_{PD}(n) = \frac{g_{m6/7}}{C_1 \cdot f} \cdot [V_{PD}(0) - V_{PD}(n) + \frac{2}{\pi} \cdot V_{VCO}] \tag{4.11}$$

By using iteration method $V_{PD}(n)$ can be solved as:

$$V_{PD}(n) = -\frac{2}{\pi} \cdot (1 - \frac{g_{m6/7}}{C_1 \cdot f})^n \cdot V_{VCO} + \frac{2}{\pi} \cdot V_{VCO} + V_{PD}(0) \tag{4.12}$$

and total voltage increment of V_{PD} at the end of *n*-th input signal cycle compare

with $V_{PD}(0)$ is:

$$V_{PD-1step}(n) = V_{PD}(n) - V_{PD}(0)$$

$$= -\frac{2}{\pi} \cdot (1 - \frac{g_{m6/7}}{C_1 \cdot f})^n \cdot V_{VCO} + \frac{2}{\pi} \cdot V_{VCO} \quad (4.13)$$

It can be seen that equation (4.12) and (4.13) converge only when:

$$\left|1 - \frac{g_{m6/7}}{C_1 \cdot f}\right| \leq 1 \quad (4.14)$$

Throughout the analysis below, this convergence condition is assumed to be valid. Under this condition, when *n* is large enough, $V_{PD}(n)$ converges at:

$$V_{PD}(n) = \frac{2}{\pi} \cdot V_{VCO} + V_{PD}(0) \quad (4.15)$$

Note that it takes several input signal cycles to make the value of $(1 - \frac{g_{m6/7}}{C_1 \cdot f})^n$ to be negligible, e.g. less than 0.01. This is the mathematical representation of the delay effect mentioned in Section 4.2.1. The exact number of input signal cycles required depends on the value of $\frac{g_{m6/7}}{C_1 \cdot f}$ and the accuracy requirement. Generally, the value of $\frac{g_{m6/7}}{C_1 \cdot f}$ should be chosen to be close to 1 to achieve fast settling of V_{PD}.

$V_{PD}(n)$ can also be calculated in another way. In steady state, the total charge injected into the load capacitor C_1 during each input signal cycle should be 0. This means the right hand side of equation (4.11) is 0. It is clear that this is equivalent to equation (4.15).

Compare equation (4.15) with equation (4.1), parameter K_{PD} and V_{offset} can be derived as:

$$K_{PD} = \frac{dV_{PD}}{dV_{VCO}} = \frac{2}{\pi} \quad (4.16)$$

and

$$V_{offset} = V_{PD} - K_{PD} \cdot V_{VCO} = V_{PD}(0) \quad (4.17)$$

Equation (4.16) shows K_{PD} is independent of the frequency variation.

In practice, assumption (A1) and (A2) may not be valid. The tail current source has a finite resistance *R* (recall that in Section 4.2.1 it is suggested a resistor to be used as the current source of PD to reduce flicker noise contribution) and the "on" period of transistor M_6 and M_7 during each input signal cycle is shorter than one half cycle. However, it is still possible to derive V_{PD} even with these limitations.

As discussed above, the total charge injected into the load capacitor C_1 during each input signal cycle should be 0 when PD is stabilized. This means during steady state, the total charge that flows through transistor M_6 and M_7 during each input signal cycle should be equal to the total charge that flows through the tail current resistance R.

Similar as equation (4.9), the total extra charge in the form of AC current introduced by V_{VCO} and flows through transistor M_6 and M_7 during each input cycle can be calculated as:

$$Q = 2 \cdot g_{m6/7} \cdot \int_{\alpha_1}^{\alpha_2} \{V_{VCO} \cdot \sin(2\pi f t) - [V_{PD}(n) - V_{PD}(0)]\} dt$$

$$= 2 \cdot g_{m6/7} \cdot k \cdot \int_{0}^{\frac{1}{2f}} \{V_{VCO} \cdot \sin(2\pi f t) - [V_{PD}(n) - V_{PD}(0)]\} dt \qquad (4.18)$$

where α_1 and α_2 indicates the conduction angle of transistor M_6 and M_7. k is a coefficient which is always positive but less than 1 and is determined by this conduction angle.

On the other hand, at steady state, extra current required for tail current resistance R in order to maintain the output of PD at $V_{PD}(n)$ is:

$$i = \frac{V_{PD}(n) - V_{PD}(0)}{R} \qquad (4.19)$$

So the total charge required for tail current resistance R in each input signal

cycle is:

$$Q = i \cdot t = \frac{V_{PD}(n) - V_{PD}(0)}{R} \cdot \frac{1}{f} \tag{4.20}$$

Equalizing the right hand side of equation (4.18) and (4.20):

$$2 \cdot g_{m6/7} \cdot k \cdot \int_0^{\frac{1}{2f}} \{V_{VCO} \cdot \sin(2\pi f t) - [V_{PD}(n) - V_{PD}(0)]\} dt$$

$$= \frac{V_{PD}(n) - V_{PD}(0)}{R} \cdot \frac{1}{f} \tag{4.21}$$

Solving equation (4.21), $V_{PD}(n)$ can be calculated as:

$$V_{PD}(n) = \frac{2 \cdot g_{m6/7}}{\pi \cdot (g_{g_{m6/7}} + \frac{1}{k \cdot R})} \cdot V_{VCO} + V_{PD}(0) \tag{4.22}$$

So K_{PD} is

$$K_{PD} = \frac{dV_{PD}}{dV_{VCO}} = \frac{2 \cdot g_{m6/7}}{\pi \cdot (g_{m6/7} + \frac{1}{k \cdot R})} \tag{4.23}$$

The actual PD shown in Figure 4.10 is designed and simulated according to the topology analyzed above. Dimensions of all devices are shown in Table 4.3. Simulation result is shown in Figure 4.11 and compared with theoretical value of K_{PD} calculated with equation (4.16) under ideal condition.

Table 4.3: Dimension and values of components in the VCO core

M_6 & M_7	60 μm/1 μm
M_8 & M_9	20 μm/1 μm
R_2	4 kΩ
C_1	6.5 pF

Though equation (4.23) looks much more complicated compare with equation (4.16), K_{PD} is still insensitive to frequency if $g_{m6/7}$ is large enough (in which case K_{PD} can be simplified as $2/\pi$, same as equation (4.16)) or insensitive to frequency itself. However, a large $g_{m6/7}$ value leads to high

power consumption. Note that the differential coefficient of K_{PD} with respect to k is always positive within the value range of k. This means although k is positive correlates to V_{VCO} and K_{PD} may deviate at high V_{VCO}, both K_{PD} and V_{PD} are monotonous increasing functions of V_{VCO}, which still fulfill the principle operation requirement of PD.

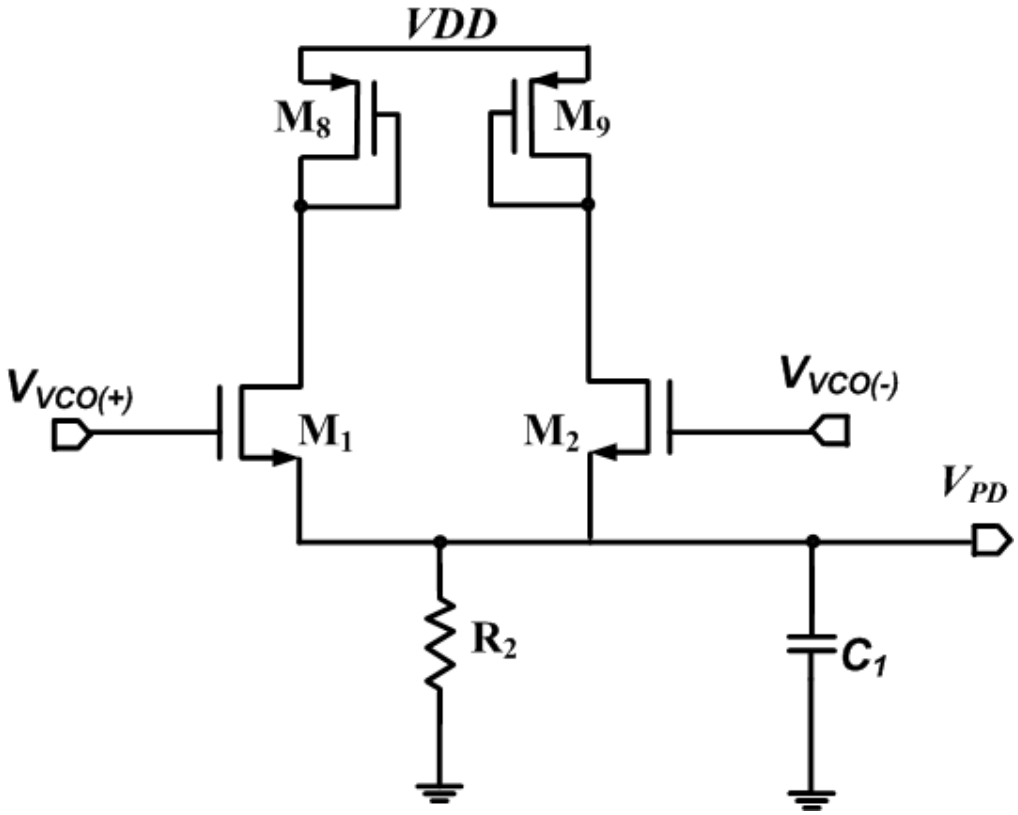


Figure 4. 10 Schematic of actual PD used in the proposed AAC VCO

Two important observations can be made from Figure 4.11: (1) simulated K_{PD} is smaller for lower V_{VCO} and it increases with V_{VCO}, which matches the conclusion draw from equation (4.23); (2) for high V_{VCO}, e.g. larger than 0.5 V, simulation plot and calculation plot are in parallel, this indicates that equation (4.16) is accurate for quick estimation. So it will be used in further analysis. The proposed PD is simulated at different frequencies and the results indicate

K_{PD} is insensitive to the frequency of V_{VCO}, which fulfils the design target as discussed previously.

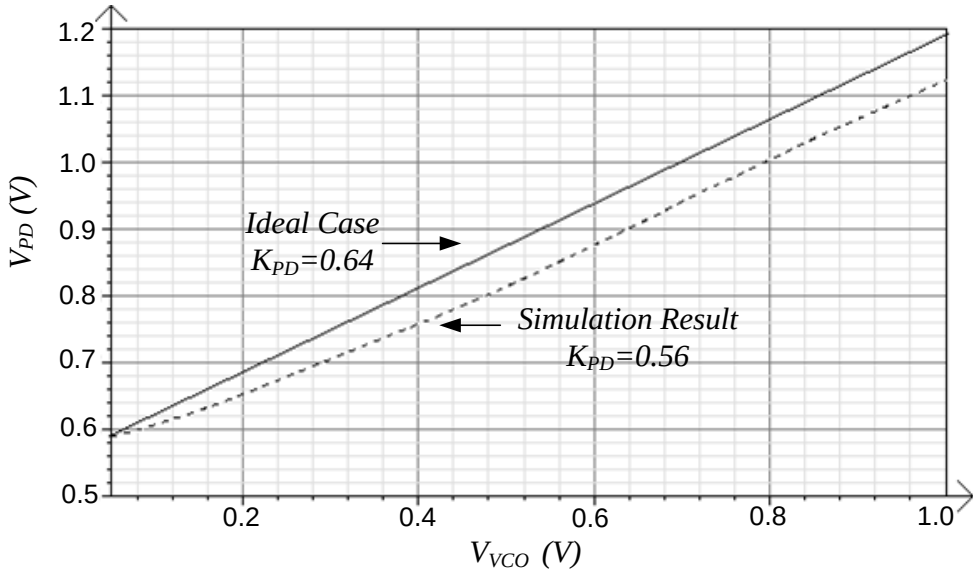


Figure 4. 11 Calculated and simulated result of K_{PD}

4.2.4 Transient analysis of the whole AAC loop

Due to the transient response of the PD, the transient analysis of the whole AAC loops is complicated. For simplicity, following assumptions are made:

(B1): Initially V_{VCO} is far below V_{VCO1}, which is the lower boundary of the desired amplitude range pre-defined as $V_{VCOrange}$. Consequently, the initial value of V_{PD} is also well below V_{REF1}, which is the lower boundary of the desired range $V_{PDrange}$.

(B2): During the calibration process, the CP's charging current I_{CP} and g_{m3} which is the transconductance of transistor M_3 are constant. Recall equation (4.3) ~ (4.5), this means both the increment of V_{ADJ} and V_{VCO} during each cycle of V_{VCO} are constant as long as the CP is at "on" state.

(B3): V_{VCO} changes only at the end of each cycle of V_{VCO} and it changes

instantaneously.

(B4): The settling time required for amplitude calibration process is long enough, or in other words it takes many cycles, e.g. several thousand cycles, of V_{VCO} for the calibration. Assumption (B3) and (B4) ensure the assumption of (A4) made in Section 4.2.3 to be valid. In other words, the analysis for PD is applicable for the transient analysis of the whole AAC loop.

According to equation (4.5), increment of V_{VCO} during each cycle can be calculated as:

$$\Delta V_{VCO} = \frac{4}{\pi} \cdot \frac{1}{f} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \tag{4.24}$$

This increment will be referred to as V_{step} in the following parts of analysis since it is constant for each cycle. So after p cycles, the total increment of V_{VCO} is:

$$p \cdot V_{step} = p \cdot \frac{4}{\pi} \cdot \frac{1}{f} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \tag{4.25}$$

Substitute into equation (4.17), the corresponding increment of V_{PD} is:

$$\Delta V_{PD} = \frac{2}{\pi} \cdot p \cdot V_{step} = \frac{8}{\pi^2} \cdot \frac{1}{f} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} \tag{4.26}$$

Due to the delay effect discussed in Section 4.2.3, V_{PD} cannot increase by this ΔV_{PD} immediately after the change of $p \cdot \Delta V_{VCO}$. The actual response of V_{PD} is complicated and will be illustrated below. Note that as long as V_{PD} is below V_{REF1}, the output of the comparator pair, COM_1 and COM_2 will not change since they are state function. Hence the state of CP will not change either and the assumptions (B2) to (B4) still hold.

According to equation (4.9), the total charge injected into C_1, which is the load capacitor of PD, is linearly related to $V_{PD}(\mathrm{n})$. Thus when several increments occur at V_{VCO} in succession, superposition principle can be applied

to calculate the response of V_{PD}. In other words, actual increment of V_{PD} at the end of the p-th cycle can be calculated by summing responses of each V_{step} occurs at different cycles. Response of V_{PD} at the end of the p-th cycle for certain V_{step} will be calculated first.

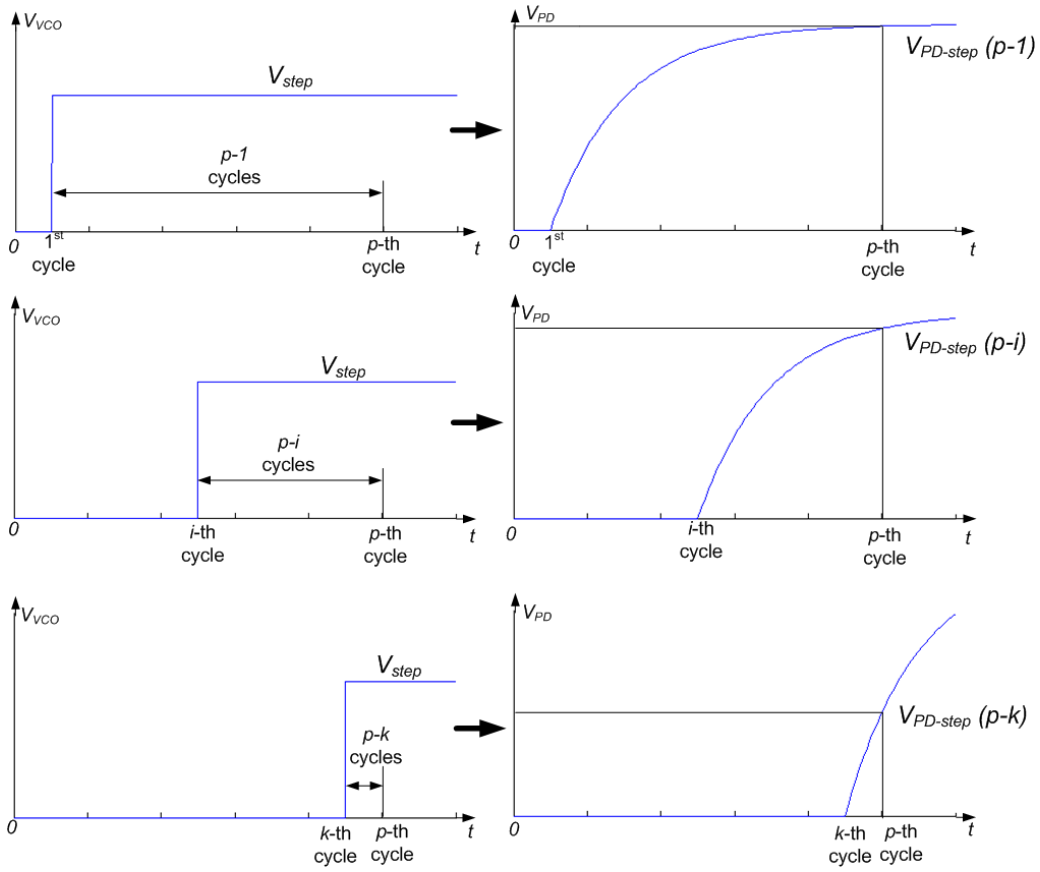


Figure 4. 12 Individual steps change for V_{VCO} (left column) and their response at V_{PD} (right column)

As shown in Figure 4.12, for V_{step} occurs at i-th (i<p) cycle, the duration between this V_{step} occur and the end of the p-th cycle is obviously (p-i) cycles. This means that when calculating the response of V_{PD} due to this V_{step} at the end of the p-th cycle by applying equation (4.13), the power n in this equation should be substituted by p-i.

By applying superposition principle, response of V_{PD} at the end of the p-th

cycle can be calculated by adding response of all individual V_{step} as:

$$\Delta V_{PD} = \sum_{m=0}^{p} V_{PD-1step}(m)$$

$$= \sum_{m=0}^{p} [-\frac{2}{\pi} \cdot \left(1 - \frac{g_{m6/7}}{C_1 \cdot f}\right)^m \cdot V_{step} + \frac{2}{\pi} \cdot V_{step}]$$

$$= -\frac{2}{\pi} \cdot [1 - (1 - \frac{g_{m6/7}}{C_1 \cdot f})^{p+1}] \cdot \frac{C_1 \cdot f}{g_{m6/7}} \cdot V_{step} + \frac{2}{\pi} \cdot p \cdot V_{step} \quad (4.27)$$

Compare equation (4.26) with equation (4.27), voltage difference between the actual value and ideal value is:

$$V_{delay} = \frac{2}{\pi} \cdot [1 - (1 - \frac{g_{m6/7}}{C_1 \cdot f})^{p+1}] \cdot \frac{C_1 \cdot f}{g_{m6/7}} \cdot V_{step} \quad (4.28)$$

For amplitude calibration purpose, total number of cycles required is very large according to assumption (B4). Under this condition, V_{delay} can be simplified as:

$$V_{delay} = \frac{2}{\pi} \cdot \frac{C_1 \cdot f}{g_{m6/7}} \cdot V_{step} \quad (4.29)$$

This indicates when V_{VCO} has just reached V_{VCO1}, which is the lower boundary of the desired amplitude range $V_{VCOrange}$, V_{PD} is still below V_{REF1} by V_{delay}. Thus the output state of the comparator pair does not change and the CP continues to provide the constant charging current I_{CP} to increase V_{ADJ}, which consequently makes V_{VCO} keep on increasing. This process stops only when V_{PD} has increased to V_{REF1} thus the output state of the comparator pair is changed and CP is turned off. Transition of V_{VCO} and V_{PD} during the whole amplitude calibration process is shown in Figure 4.13.

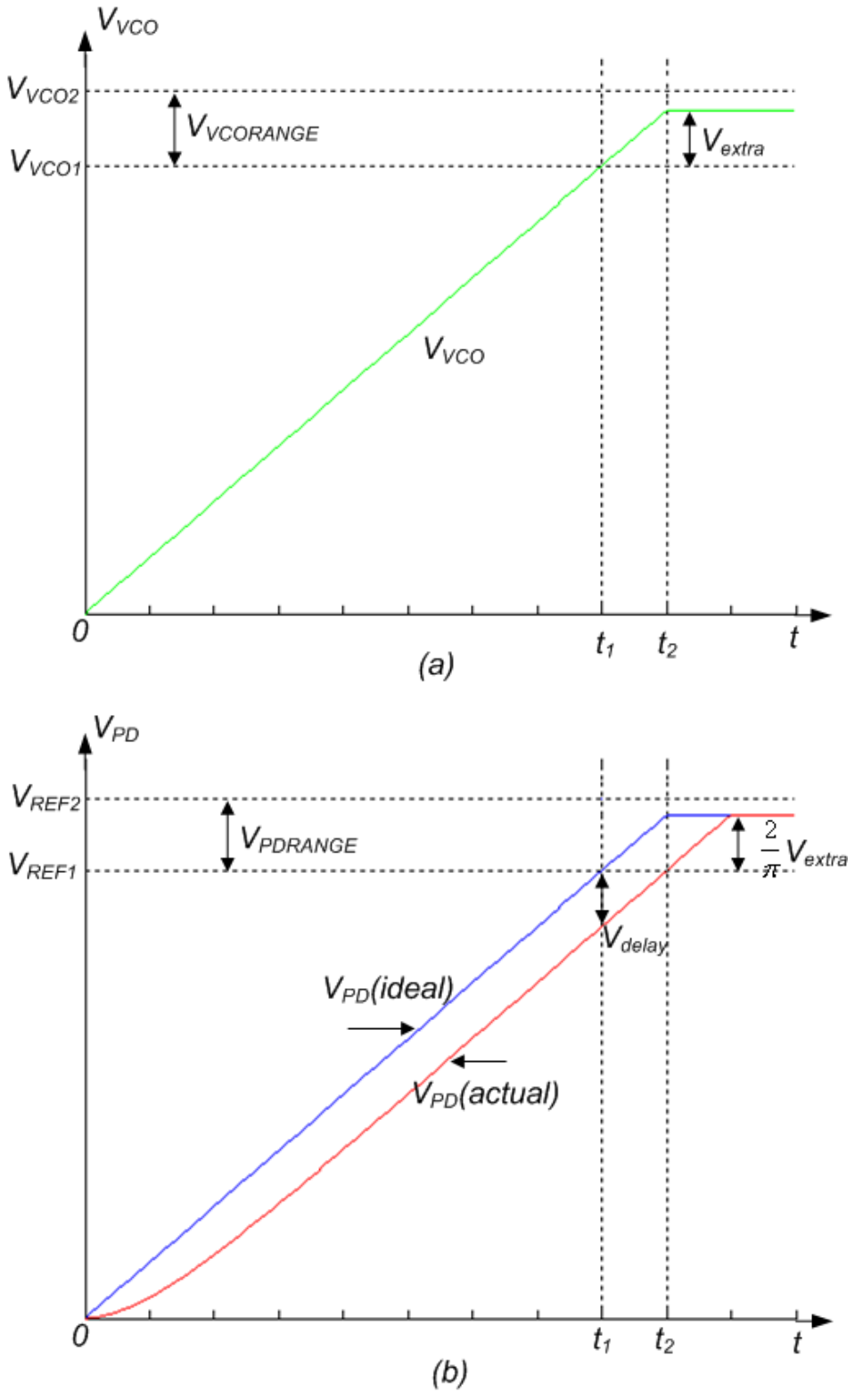


Figure 4. 13 Change of V_{VCO} (a) and V_{PD} (b) during the whole amplitude calibration process

Let the voltage difference between the final value of V_{VCO} and V_{VCO1} to be

V_{extra}. Note that the number of cycles required for V_{VCO} to accumulate this V_{extra} by each V_{step} is the same as that required by V_{PD} to increase by V_{delay}.

Since when total number of cycles spent for amplitude calibration process is large enough, the actual value of V_{PD} is always lower than the ideal value by this V_{delay} as long as the actual value of V_{PD} is lower than V_{REF1}. So when the actual value of V_{PD} is equal to V_{REF1}, the ideal value of V_{PD} should be higher than V_{REF1} by V_{delay} and at this moment CP is turned off thus there is no further increment for V_{VCO}. According to equation (4.16), the final value of V_{VCO} should be higher than V_{VCO1} by:

$$V_{extra} = \frac{\pi}{2} \cdot V_{delay} = \frac{C_1 \cdot f}{g_{m6/7}} \cdot V_{step} \tag{4.30}$$

Thus the total number of cycles, a required for V_{VCO} accumulating this V_{extra} by each V_{step} and for V_{PD} to increase by V_{delay} is:

$$a = \left[\frac{C_1 \cdot f}{g_{m6/7}}\right] \tag{4.31}$$

where the square bracket indicates the cell function.

Note that when the whole amplitude calibration is completed and the whole loop is in steady state, V_{PD} should be higher than V_{REF1} by V_{delay} as shown in Figure 4.13. To prevent squegging, voltage difference between V_{REF1} and V_{REF2} should be at least V_{delay}. This explained why neither $V_{VCOrange}$ nor $V_{PDrange}$ which determines the calibration accuracy can be arbitrarily small. Considering the convergence requirement for PD mentioned in Section 4.2.3, the following approximation can be used for quick estimation during AAC design process. :

$$V_{delay} = \frac{2}{\pi} \cdot \frac{C_1 \cdot f}{g_{m6/7}} \cdot V_{step} \approx \frac{2}{\pi} \cdot V_{step} \tag{4.32}$$

V_{delay} can be further expanded according to equation (4.24) as:

$$V_{delay} \approx \frac{2}{\pi} \cdot V_{step} = \frac{8}{\pi^2} \cdot \frac{1}{f} \cdot \frac{1}{C_{CP}} \cdot I_{CP} \cdot g_{m3} \cdot R_{eq} = \frac{8}{\pi^2} \cdot \frac{1}{f} \cdot CR \quad (4.33)$$

in which CR is defined in Section 4.2.1. For a certain $V_{PDrange}$ pre-determined during the optimization of the VCO core, the maximum value of CR can be derived using equation (4.32) and the value of V_{delay}. Larger CR will lead to squegging.

As mentioned previously, the quantitative analysis is the same for discharging case except for discharging case the sign of I_{CP} is negative. Hence for the discharging case, the final value of V_{PD} in steady state should be lower than V_{REF2}. For the discharging current has the same magnitude but opposite sign compares to charging current I_{CP}, the final value of V_{PD} should be lower than V_{REF2} by V_{delay}.

It is recommended to set the voltage difference between V_{REF1} and V_{REF2} to be $2 \cdot V_{delay}$. The advantages are:

(1) Under this condition, the final value of V_{PD} will be around the centre of $V_{PDrange}$ instead of the edge for both the charging and discharging case.

(2) Charge leakage effect may change the value of V_{ADJ} and thus changes V_{VCO} and consequently V_{PD}. Designing V_{PD} at the centre of $V_{PDrange}$ will provide some margin to tolerate the variation of V_{PD} due to charge leakage and this margin makes the AAC more stable. Note the charge leakage effect may change the value of V_{ADJ} and thus changes V_{VCO} and consequently V_{PD} so squegging may occur.

Relationship between ΔV_{PD} and ΔV_{ADJ} can be derived from equation (4.3), (4.6) and (4.16) as:

$$\Delta V_{PD} = \frac{8}{\pi^2} \cdot \Delta V_{ADJ} \cdot g_{m3} \cdot R_{eq} \quad (4.34)$$

Substitute into equation (4.32), maximum variation of V_{PD} that can be tolerated by V_{delay} region is:

$$\Delta V_{PD.max} = \frac{\pi}{4 \cdot g_{m3} \cdot R_{eq}} \cdot V_{step} \tag{4.35}$$

4.3 Design procedure of the proposed AAC VCO

According to the analysis of individual blocks and the overall transient response of the whole AAC loop, a systematic design procedure is proposed as followed:

(1): Design and optimize the VCO core. Determine the VCO's frequency range and the desired amplitude range ($V_{VCOrange}$);

(2): Design and optimize the PD. Choose the optimum value of $g_{m6/7}$ by considering both the power consumption of PD and K_{PD}. Based on this $g_{m6/7}$ value and the frequency range of the VCO core, choose a proper capacitor value for C_1. Ensure the combination of $g_{m6/7}$, C_1 and the frequency range of the VCO core fulfill the convergence requirement as shown in equation (4.14).;

(3): Based on $V_{VCOrange}$, K_{PD} and $V_{PD}(0)$, calculate both V_{REF1} and V_{REF2} by equation (3.2). Thus $V_{PDrange}$ is determined;

(4): Based on V_{REF1} and V_{REF2}, determine V_{delay} so that $2 \cdot V_{delay} \leq V_{REF2} - V_{REF1}$;

(5): Determine the maximum value of CR by considering the frequency range of the VCO core, value of V_{delay} and equation (4.33);

(6): According to the definition and maximum value of CR, determine the value of C_{CP}, I_{CP} and g_{m3} by taking in account of the trade-off with the area

and power consumption.

4.4 Simulation and Measurement Results of the Proposed AAC VCO

The proposed hybrid type AAC VCO was designed and fabricated in GlobalFoundries 0.18 μm CMOS technology. The die microphotograph is shown in Figure 4.14. The size of the proposed circuit is 1mm × 1 mm including PADs. In this thesis, all measurements have been conducted on wafer, using a probe station with DC connection and RF probes. The testing platform is placed inside a metal cage providing a common ground potential for all measurement equipment and wafer chuck to remove any potential electrostatic discharge (ESD) problem.

In all measurement, V_{REF2} is set to 5 mV higher than V_{REF1}. According to equation (4.2), it can be derived that $V_{REF2} - V_{REF1} = K_{PD} \cdot (V_{VCO2} - V_{VCO1})$. Considering value of K_{PD} according to equation (4.16), maximum amplitude variation should be 7.85 mV.

Measured tuning range of the proposed AAC VCO is from 2.25 GHz to 2.54 GHz. Measured and simulated amplitude versus oscillation frequency is shown in Figure 4.15 As show in Figure 4.15, amplitude increase with V_{REF1} as expected. When $V_{REF1} = 0$, the VCO core is free-running and there is no amplitude calibration. In this case amplitude variation over the tuning range is 40mV for both measurement and simulation. For all other measurements, the maximum amplitude variation according to each $V_{REF1}$is 9 mV. Considering the error between the actual K_{PD} and the value used for prediction, this is

acceptable and indicates the proposed hybrid type AAC functions as expected.

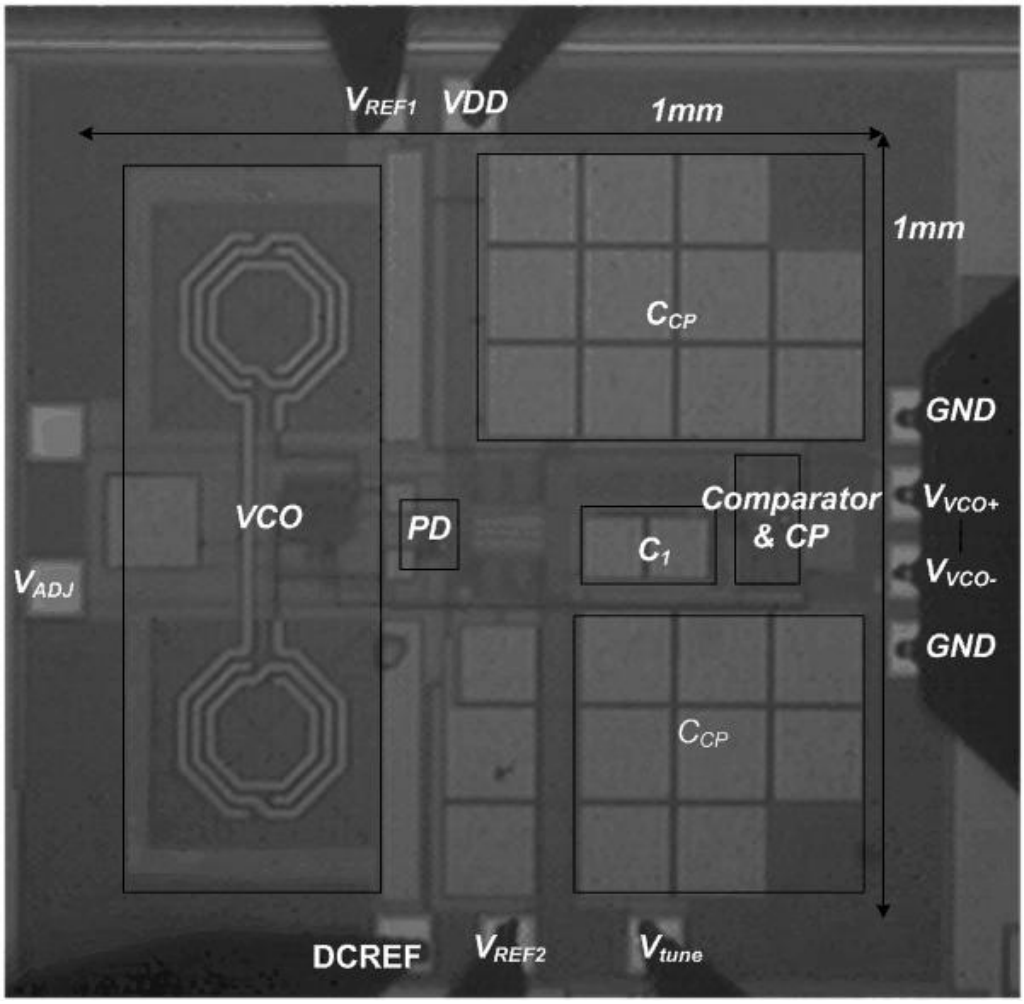


Figure 4. 14 Die microphotograph of the proposed hybrid type AAC VCO

Measured oscillation frequency and total current consumption of the proposed hybrid type AAC VCO (I_{AACVCO}) versus V_{REF1} is shown in Figure 4.16. The current consumption of the output buffer is 3.5 mA and is excluded in I_{AACVCO} . Total current consumption increases with V_{REF1} as expected. Frequency variation due to the change of V_{REF1} is less than 5 MHz. Compare with the oscillation frequency which is around 2.4 GHz, this frequency variation is less than 1% and can be easily tracked by the PLL loop.

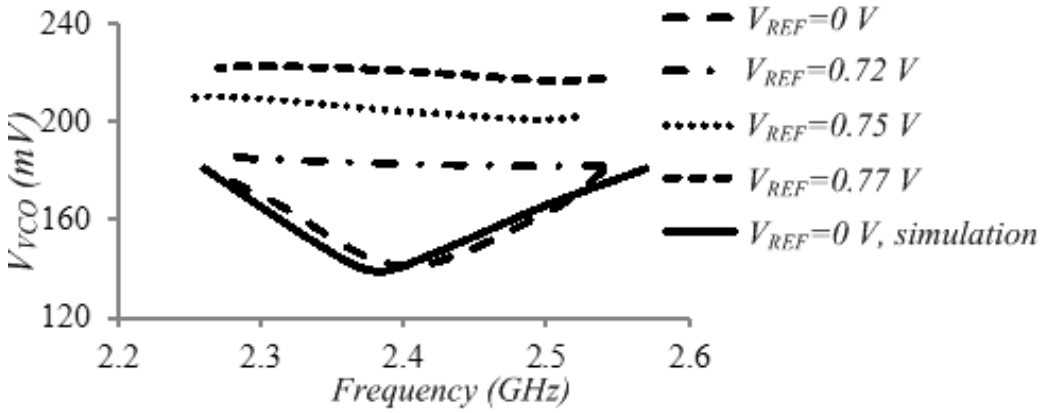


Figure 4. 15 Measured and simulated amplitude versus oscillation frequency for various values of V_{REF1}

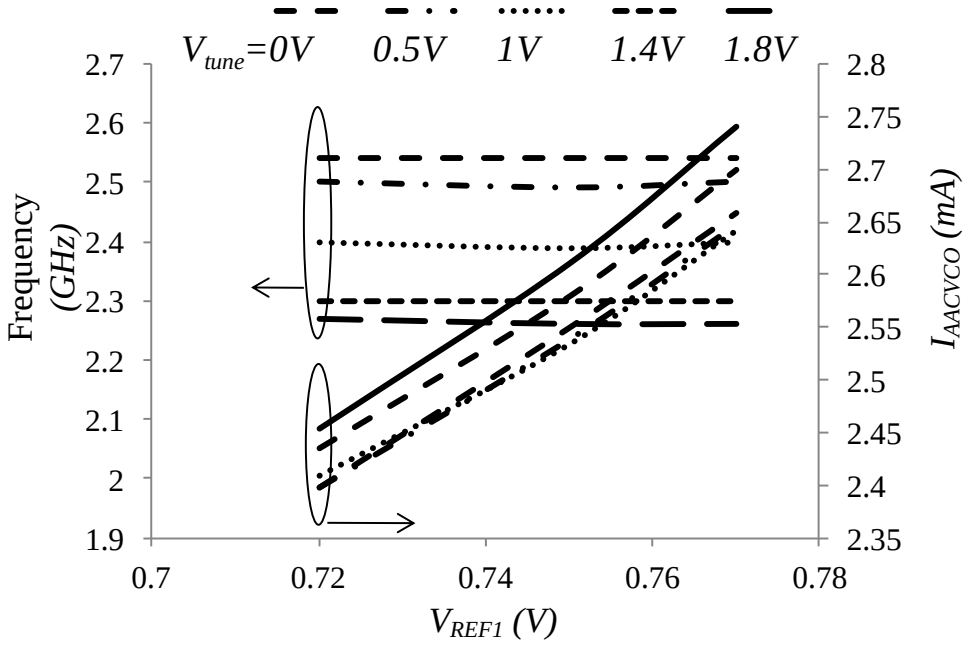


Figure 4. 16 Measured oscillation frequency total current consumption of the proposed hybrid type AAC VCO versus V_{REF1}

Measured phase noise for 2.54 GHz oscillation frequency is shown in Figure 4.17. With $V_{REF1} = 0.75\ V$, phase noise at 10 kHz offset is -97 dBc/Hz.

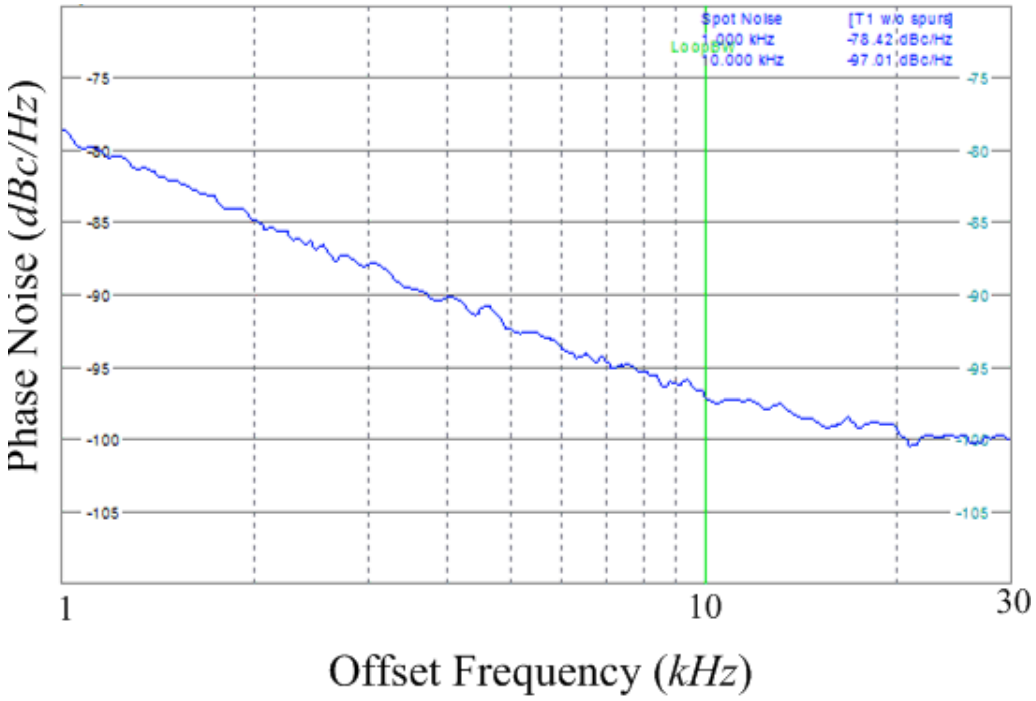


Figure 4. 17 Phase noise of the proposed hybrid type AAC VCO with $V_{REF1} = 0.75$ V

Since the duration for calibration of the proposed AAC VCO cannot be measured, simulation result is shown here instead. Larger value of C_{CP} reduces the value of V_{step} thus increases the total cycles required for calibration. On the other hand, as shown in Section 4.2.4, if the value of C_{CP} is too small, V_{step} could be so large that V_{delay} is larger than $V_{REF2} - V_{REF1}$, leading to squegging. Figure 4.18 shows the transient response of V_{ADJ} for different C_{CP}. Calibration process is completed when V_{ADJ} stopped changing.

As shown in Figure 4.18, for worst case the calibration process takes 10.5 μs for standard value of C_{CP}. When C_{CP} increased by 15%, it takes about 12 μs to complete the calibration process. Squegging occurs when C_{CP} is reduced to 60% of the standard value.

Besides, transient response of I_{CP}, V_{ADJ} and V_{PD} are shown in Figure 4.19,

which matches the analysis in Section 4.2.4 well.

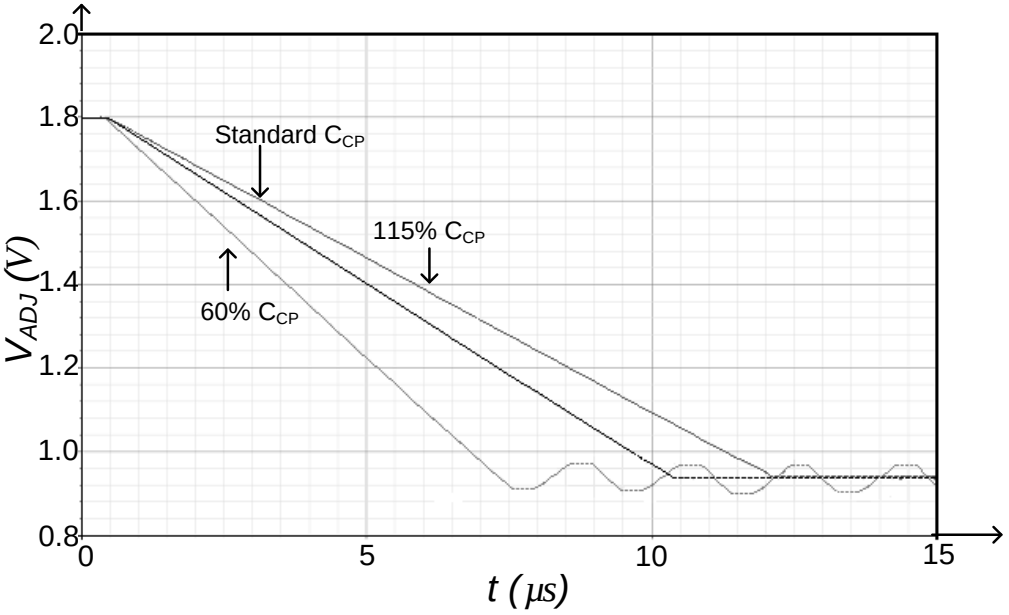


Figure 4. 18 Worst case calibration time for different C_{CP}

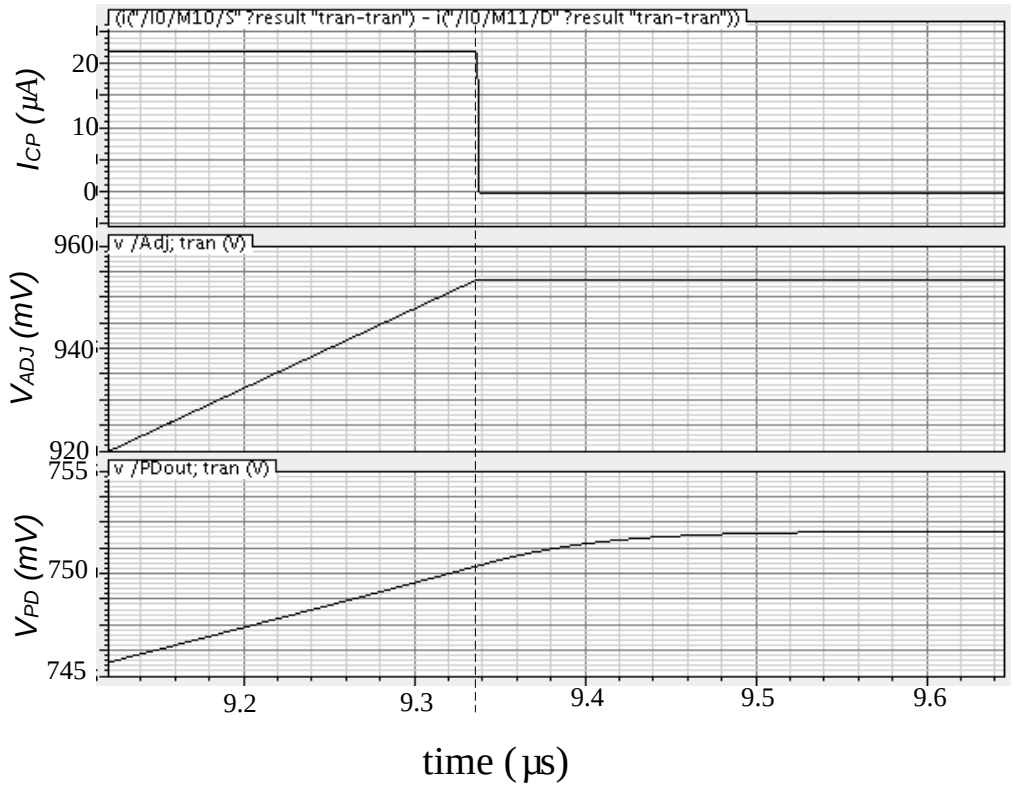


Figure 4. 19 Transient response of I_{CP}, V_{ADJ} and V_{PD}

4.5 Summary

In this chapter, a novel hybrid type AAC VCO is presented after reviewing the advantages and disadvantages of the conventional types AAC VCO. The operation of the whole loop and the state-dependent nature is analyzed first, followed by the analysis of important blocks. Based on these analyses, a quantitative transient analysis for the whole loop is performed. A systematic design procedure is proposed according to the relationship explored in the quantitative transient analysis.

A fully integrated hybrid type AAC VCO targeted for ISM band application has been designed and fabricated in 0.18 μm CMOS technology. Measured results show that the tuning range of the proposed VCO is from 2.25 GHz to 2.54 GHz. Measured maximum amplitude variation over this tuning range is 9 mV. Phase noise at 10 kHz offset is -97 dBc/Hz. Power consumption of the whole proposed AAC VCO is 4.5 mW (10.8 mW if buffer is included) while the power consumed by the calibration circuitry is about 0.8 mV.

The proposed hybrid type AAC VCO is compared with other published works in Table 4.4. The proposed hybrid AAC VCO achieves a comparable FoM. The AAC VCO proposed in [5] has a better FoM mainly due to the advantage brought by the Class-C type VCO core. On the other hand, [80] has a better FoM mainly due to its triode region biased current source in the VCO core. On the other hand, extra LDO voltage regulator is required for this design hence the circuit is much more complex. Besides, it should be carefully designed in order to prevent stability problem.

Table 4.4: The performance comparison of the AAC VCOs

	[5]	[42]	[80]	[81]	This work
Tech (μm)	0.18	0.18	0.18	0.18	0.18
Centre Frequency (GHz)	3.1	7.2	5	1.8	2.4
Tuning Range (%)	20	6	6.7	73	13
V_{dd} (V)	1.0	1.8	1.8	1.5	1.8
Total Power(mW)	1.57	4.32	7.56	7.2	4.5
Phase noise (dBc/Hz)	-102	-82	-104.8	-104.7	-97
Offest Frequency (Hz)	100k	100k	100k	100k	10k
FoM (dBc)	189.9	172.8	190	181.2	189

* $\text{FoM} = -\mathcal{L}\{\Delta\omega\} + 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log(Power_{mW})$

CHAPTER 5

Novel In-Phase Coupling Scheme and Phase Error Tuning Scheme for QVCO

As mentioned in Chapter 3, quadrature modulation is widely supported among the ISM band applications. Hence generating high performance quadrature signal is also essential for ISM band application. After first introduced in 1996, QVCO has become a popular choice for quadrature signal generation and attracts interests of many researchers. Many QVCO topologies with different coupling scheme have been proposed and their advantages and disadvantages are analyzed in Chapter 3. However, the coupling schemes reported so far are mostly for conventional VCO structure and there is yet any Class-C QVCO been reported. Furthermore, as the phase accuracy is an important parameter for the QVCO's performance, it is attractive to introduce phase error tuning to minimize the phase error.

The idea of in-phase coupling was first suggested in [71] to obtain both good phase noise and phase accuracy performance in a QVCO. Several topologies for in-phase coupling have been reported so far, as shown in [71, 72, 74]. [71] achieves the phase shifting for coupling purpose by an RC phase shifter. However, such approach is frequency dependent hence the frequency range is limited. The coupling structure proposed in [72] consumes considerable power. Furthermore, the phase shifting mechanism is not fully explained. It is worthwhile to note that the in-phase coupling schemes proposed in [71, 72, 74] do not have the function of phase error tuning. On the other hand, the phase

error tuning scheme proposed in [6] is only suitable for conventional parallel QVCO topology and the phase error tuning range is limited by the coupling factor while the phase error tuning scheme proposed in [7] requires additional inductor and varactor that occupies large area.

In this chapter, a novel in-phase coupling scheme is presented. The proposed in-phase coupling circuitry consumes less than 2% of the total power consumption of the QVCO and is frequency-independent. Based on this scheme, a 2.4 GHz QVCO with conventional LC VCO topology is implemented. After that, the proposed coupling circuitry is modified to realize phase error tuning. Furthermore, a Class-C IPC QVCO with tuneable phase error is proposed. All the work are implemented using GlobalFoundries CMOS 0.18 μm CMOS technology.

5.1 Novel IPC QVCO

The schematic of the proposed IPC QVCO (which will be referred to as "Design A") is shown in Figure 5.1. The two VCO cores are identical thus the frequency, amplitude and DC offset of the four output branches *I*+, *I*-, *Q*+ and *Q*- are equal.

The coupling circuitry consists of 8 identical transistors M_{C1}~M_{C8} whose drain terminals are all connected to *VDD*. The source and gate terminals of these coupling transistors are connected to the output branches of the VCO cores which have the same DC offset voltage. As a result, these coupling transistors work either in off or saturation region during operation. Detailed analysis of operation is shown below.

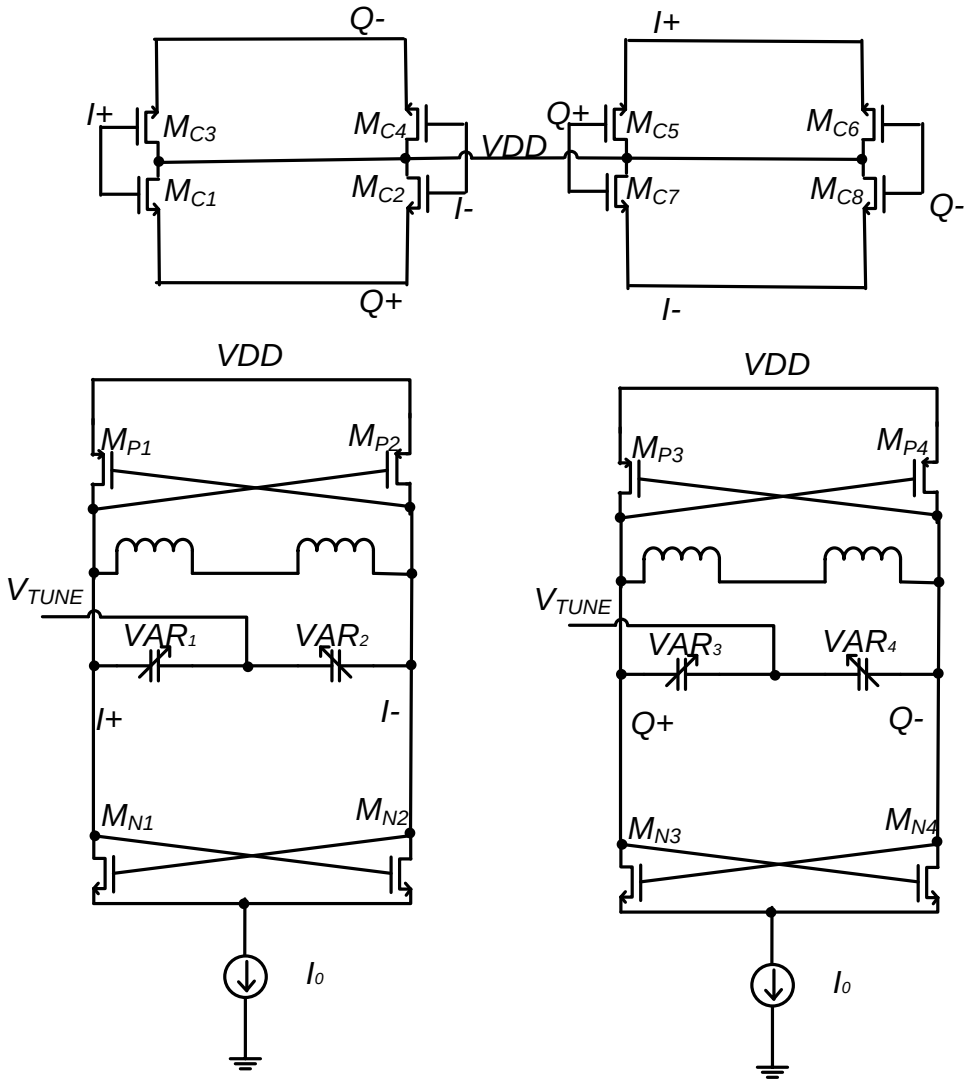


Figure 5. 1 Schematic of Design A

5.1.1 Drain current of the coupling transistors

In modern transistor technology, the carrier drift velocity saturates when V_{DS} is larger than the saturation drain voltage $V_{DS,sat}$, which is usually smaller than the threshold voltage. In this case, the drain current can be expressed as:

$$I_d = P \cdot (V_{GS} - V_{th}) \tag{5.1}$$

where $P = K \cdot v_{sat} \cdot C_{ox} \cdot W$. In this expression of P, K is the short channel effect modeling parameter, v_{sat} is the saturation velocity of the transistor while C_{ox} and W are both physical parameters of the transistor.

For the proposed coupling circuitry, the drain terminals of each coupling transistors are all connected to *VDD* which is higher than the gate voltage, thus the velocity saturation condition is fulfilled. Hence equation (5.1) is applied below to calculate the drain current of the coupling transistors.

As mentioned earlier, for each coupling transistor V_G and V_S have the same frequency, amplitude and DC offset but different phase. Thus V_{GS} is a sine wave with 0 volt DC offset. For general case, it is assumed that $V_{GS} = A \cdot sin\,\omega t$ where A is the amplitude and ω is the angular frequency. Obviously, in this case there exists a conduction angle 2α for the transistor and it can be calculated as:

$$2\alpha = 2arcsin(\frac{V_{th}}{A\cdot}) \tag{5.2}$$

In other words, when $\alpha + 2k\pi < \omega t < -\alpha + (2k+1)\pi$ where k is a positive integer, the transistor works in saturation region. Hence the drain current is:

$$I_d(t) = P \cdot (A \cdot sin\,\omega t - V_{th}) \quad \text{(transistor is on)}$$

$$I_d = 0 \quad \text{(transistor is off)} \tag{5.3}$$

The *Q* value of the resonator is supposed to be high enough and only current at the fundamental frequency is considered. In this case, when expanding I_d in the Fourier series, the fundamental terms of I_d can be calculated as:

$$i_d(t) = B \cdot sin\,\omega t + C \cdot cos\,\omega t \tag{5.4}$$

where

$$B = \frac{\omega}{\pi} \cdot \int_{\frac{\alpha}{\omega}}^{\frac{\pi-\alpha}{\omega}} P \cdot (A \cdot sin\,\omega t - V_{th}) sin\omega t dt$$

$$= \frac{P}{\pi}[\frac{A}{2}(\pi - 2\alpha + sin2\alpha) - 2V_{th} \cdot cos\alpha]$$

$$C = \frac{\omega}{\pi} \cdot \int_{\frac{\alpha}{\omega}}^{\frac{\pi-\alpha}{\omega}} P \cdot (A \cdot sin\,\omega t - V_{th}) cos\omega t dt = 0 \quad (5.5)$$

On the other hand, the Taylor expansion of the inverse trigonometric functions is:

$$\arcsin(x) = \sum_{n=0}^{\infty} \frac{(2n)!}{4^n \cdot (n!)^2 \cdot (2n+1)} x^{2n+1}$$

Substituting this expansion into equation (5.5), equation (5.4) can be simplified as:

$$i_d(t) = P \cdot (\frac{A}{2} - \frac{2}{\pi} V_{th}) \cdot sin\,\omega t \quad (5.6)$$

Equation (5.6) shows that the amplitude of the fundamental component of the coupling transistor's drain current is proportional to the amplitude of V_{GS} while the phase of this current is the same as the V_{GS}. As the *Q* value of the resonator is supposed to be high enough and only this fundamental component is of interest in analysis below, this fundamental component will be referred to as "drain current" for simplicity.

5.1.2 In-phase Coupling Current and Quadrature Signal Generation

Suppose the voltage of the four output branches *I*+, *I*-, *Q*+ and *Q*- are:

$$V_{I+}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1)$$

$$V_{Q+}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$V_{I-}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi)$$

$$V_{Q-}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_2 + \pi) \quad (5.7)$$

where V_A is the amplitude of Design A's output, ω_0 is the oscillation frequency and $0 \leq \theta_2 \leq \theta_1 < 2\pi$. DC offset of each branch is ignored as they are equal

and does not affect the drain current of the coupling transistors. For case $\theta_2 \leq \theta_1 \leq \theta_2 + \pi$, V_{GS} of each coupling transistor can be expressed as:

$$V_{GS1}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{\pi}{2})$$

$$V_{GS2}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi)$$

$$V_{GS3}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2})$$

$$V_{GS4}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} - \frac{\pi}{2})$$

$$V_{GS5}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} - \frac{\pi}{2})$$

$$V_{GS6}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi)$$

$$V_{GS7}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2})$$

$$V_{GS8}(t) = 2V_A \cdot sin(\frac{\theta_1-\theta_2}{2}) \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{\pi}{2}) \quad (5.8)$$

According to the assumption of the phase relationship mentioned earlier, the amplitude of these V_{GS} are expressed in the term of either $2V_A \cdot sin(\frac{\theta_1-\theta_2}{2})$ or $2V_A \cdot sin(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2})$ which are defined as positive for calculation purposes. Substituting into equation (5.6), the drain current of each coupling transistor can be calculated as:

$$I_{C1}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{\pi}{2})$$

$$I_{C2}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi)$$

$$I_{C3}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2})$$

$$I_{C4}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} - \frac{\pi}{2})$$

$$I_{C5}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} - \frac{\pi}{2})$$

$$I_{C6}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2} + \frac{\pi}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi)$$

$$I_{C7}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2}+\frac{\pi}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2})$$

$$I_{C8}(t) = P \cdot [V_A \cdot sin\left(\frac{\theta_1-\theta_2}{2}\right) - \frac{2}{\pi}V_{th}] \cdot sin(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2}+\frac{\pi}{2}) \quad (5.9)$$

Note for conventional LC VCO, the relationship between the amplitude of the oscillation current, I_{osc} that flows through each branch of the QVCO and the tail bias current I_0 can be derived from equation (2.22) as $I_{osc} = \frac{2}{\pi} \cdot I_0$. Thus according to the generalized equation for multiple injections introduced in [71], frequencies of the $I+$ and $Q+$ branches can be calculated as:

$$f_{I+} = \omega_0 + \frac{\omega_0}{2Q} \cdot \frac{|I_{C5}| \cdot sin(\frac{\theta_2-\theta_1}{2}-\frac{\pi}{2}) + |I_{C6}| \cdot sin(\frac{\theta_2-\theta_1}{2}+\pi)}{\frac{2}{\pi} \cdot I_0 + |I_{C5}| \cdot cos(\frac{\theta_2-\theta_1}{2}-\frac{\pi}{2}) + |I_{C6}| \cdot cos(\frac{\theta_2-\theta_1}{2}+\pi)}$$

$$= \omega_0 + \frac{\omega_0}{2Q} \cdot \frac{-\frac{2}{\pi} \cdot P \cdot V_{th} \cdot [sin\left(\frac{\theta_1-\theta_2}{2}\right) - cos\left(\frac{\theta_1-\theta_2}{2}\right)]}{\frac{2}{\pi} I_0 + P \cdot V_A - P \cdot \frac{2}{\pi} V_{th} \cdot [sin\left(\frac{\theta_1-\theta_2}{2}\right) + cos\left(\frac{\theta_1-\theta_2}{2}\right)]}$$

$$f_{Q+} = \omega_0 + \frac{\omega_0}{2Q} \cdot \frac{|I_{C1}| \cdot sin(\frac{\theta_1-\theta_2}{2}+\frac{\pi}{2}) + |I_{C2}| \cdot sin(\frac{\theta_1-\theta_2}{2}+\pi)}{\frac{2}{\pi} \cdot I_0 + |I_{C1}| \cdot cos(\frac{\theta_1-\theta_2}{2}+\frac{\pi}{2}) + |I_{C2}| \cdot cos(\frac{\theta_1-\theta_2}{2}+\pi)}$$

$$= \omega_0 + \frac{\omega_0}{2Q} \cdot \frac{-\frac{2}{\pi} \cdot P \cdot V_{th} \cdot [cos\left(\frac{\theta_1-\theta_2}{2}\right) - sin\left(\frac{\theta_1-\theta_2}{2}\right)]}{\frac{2}{\pi} I_0 - P \cdot V_A + P \cdot \frac{2}{\pi} V_{th} \cdot [cos\left(\frac{\theta_1-\theta_2}{2}\right) + sin\left(\frac{\theta_1-\theta_2}{2}\right)]} \quad (5.10)$$

For proper oscillation, the phase difference $\beta = \theta_1 - \theta_2$ must fulfill the equation $f_{I+} = f_{Q+}$. Mathematically, there should be three solutions for $f_{I+} = f_{Q+}$ as:

$$\beta = \frac{\pi}{2}$$

or

$$\beta = 2\arccos(\frac{-b+\sqrt{b^2-4ac}}{2a})$$

or

$$\beta = 2\arccos(\frac{-b-\sqrt{b^2-4ac}}{2a}) \quad (5.11)$$

where $a = 2 \cdot P \cdot V_A$, $b = -\frac{2}{\pi} \cdot P \cdot V_{th}$ and $c = \frac{2}{\pi} \cdot I_0 - P \cdot V_A$. According to the

domain of the arccosine function, the last two solutions may not be valid while $\beta = \frac{\pi}{2}$ is always a valid solution.

For case $\theta_1 \geq \theta_2 + \pi$, the solution is similar. However, since $\beta = \frac{\pi}{2}$ doesn't fulfill the assumption $\theta_1 \geq \theta_2 + \pi$, it is not valid. In simulation, only $\beta = \frac{\pi}{2}$ is observed. In the following section, only $\beta = \frac{\pi}{2}$ is considered and this indicates that quadrature phase relationship is established.

Furthermore, the coupling current of each branch can be calculated as:

$$I_{I+,inj}(t) = I_{C5}(t) + I_{C6}(t)$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1)$$

$$+ \frac{2}{\pi} \cdot P \cdot V_{th} \cdot [sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2}\right) + cos\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2}\right)]$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1)$$

$$+ \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{\pi}{4}\right)$$

$$I_{I-,inj}(t) = I_{C7}(t) + I_{C8}(t)$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi)$$

$$+ \frac{2}{\pi} \cdot P \cdot V_{th} \cdot [sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi\right) + cos\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi\right)]$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi)$$

$$+ \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{3\pi}{4}\right)$$

$$I_{Q+,inj}(t) = I_{C1}(t) + I_{C2}(t)$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$+ \frac{2}{\pi} \cdot P \cdot V_{th} \cdot [-sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2}\right) + cos\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2}\right)]$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$- \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{\pi}{4}\right)$$

$$I_{Q-,inj}(t) = I_{C3}(t) + I_{C4}(t)$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2 + \pi)$$

$$+ \frac{2}{\pi} \cdot P \cdot V_{th} \cdot [-sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi\right) + cos\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \pi\right)]$$

$$= -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2 + \pi)$$

$$- \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\left(\omega_0 \cdot t + \frac{\theta_1+\theta_2}{2} + \frac{3\pi}{4}\right) \quad (5.12)$$

Equation set (5.12) shows that each coupling current contains two terms. The first term is in phase with the coupled current while the phase of the second is complicated. However, for condition $\beta = \frac{\pi}{2}$, equation (5.12) can be simplified as:

$$I_{I+,inj}(t) = -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1) + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin(\omega_0 \cdot t + \theta_1)$$

$$I_{I-,inj}(t) = -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi) + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin(\omega_0 \cdot t + \theta_1 + \pi)$$

$$I_{Q+,inj}(t) = -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2) + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$I_{I-,inj}(t) = -P \cdot V_A \cdot sin(\omega_0 \cdot t + \theta_2 + \pi) + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin(\omega_0 \cdot t + \theta_2 + \pi) \quad (5.13)$$

which indicates that the two terms of each coupling current have the same phase as that of the coupled current. In other words, in this case the coupling current is in phase with the coupled current and in-phase coupling is thus established. Note that the amplitude of the coupling current for condition $\beta = \frac{\pi}{2}$ is $P \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th}$, which is proportional to the parameter P. Furthermore, this amplitude is usually smaller than I_{osc}. Thus if the coupling factor m is defined as $m = I_{inj}/I_{osc}$, it is obvious that for Design A, $m < 1$ and it is

proportional to P. As analyzed in [6], for conventional parallel QVCO there exists a trade-off on m between the phase accuracy and the phase error performance. A smaller m is essential for good phase noise performance but it will increase the phase error and vice versa. However, for Design A the coupling current of each branch is in phase with the injected current, hence the above mentioned trade-off does not exist and the *Q* value of the VCO core does not degrade.

In the analysis above it is assumed that the amplitude of the Design A's four outputs are equal. Below, the phase of V_{GS} of the coupling transistor will be considered in a much general case. Suppose the voltage of the four output branches *I*+, *I*-, *Q*+ and *Q*- are:

$$V_{I+}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1)$$

$$V_{Q+}(t) = V_B \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$V_{I-}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi)$$

$$V_{Q-}(t) = V_B \cdot sin(\omega_0 \cdot t + \theta_2 + \pi) \quad (5.14)$$

where V_A and V_B are the amplitude of Design A's output and other denotations are same as before. DC offset of each branch is ignored as they are equal and does not affect the drain current of the coupling transistors. In this case, V_{GS1} can be expressed as:

$$V_{GS1}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1) - V_B \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$= \sqrt{V_A^2 + V_B^2 - 2 \cdot V_A \cdot V_B \cdot cos(\theta_1 - \theta_2)} \cdot sin(\omega_0 \cdot t + \theta_{GS1}) \quad (5.15)$$

where

$$\tan\theta_{GS1} = \frac{V_A \cdot sin\theta_1 - V_B \cdot sin\theta_2}{V_A \cdot cos\theta_1 - V_B \cdot cos\theta_2}$$

and

$$sin\theta_{GS1} = \frac{V_A \cdot sin\theta_1 - V_B \cdot sin\theta_2}{\sqrt{V_A^2 + V_B^2 - 2 \cdot V_A \cdot V_B \cdot cos(\theta_1 - \theta_2)}} \tag{5.16}$$

Hence when $V_A = V_B$, equation (5.16) can be simplified as:

$$\tan\theta_{GS1} = \frac{sin\theta_1 - sin\theta_2}{cos\theta_1 - cos\theta_2} = -\frac{cos\frac{\theta_1+\theta_2}{2}}{sin\frac{\theta_1+\theta_2}{2}} = \tan(\frac{\theta_1+\theta_2}{2} + \frac{\pi}{2})$$

and

$$sin\theta_{GS1} = \frac{sin\theta_1 - in\theta_2}{\sqrt{2-2\cdot\cos(\theta_1-\theta_2)}} = \frac{2sin\frac{\theta_1-\theta_2}{2}cos\frac{\theta_1+\theta_2}{2}}{2sin\frac{\theta_1-\theta_2}{2}}$$

$$= cos\frac{\theta_1+\theta_2}{2} = \sin(\frac{\theta_1+\theta_2}{2} + \frac{\pi}{2}) \tag{5.17}$$

Thus it can be concluded that $\theta_{GS1} = \frac{\theta_1+\theta_2}{2} + \frac{\pi}{2}$, which is exactly the result shown in equation (5.8). However, if $V_A \neq V_B$, the solution of θ_{GS1} determined by equation (5.16) is very complicated. Besides θ_1 and θ_2, the ratio of V_A/V_B also matters. In this case equation (5.8) is not valid. However, it is worth noting as long as $\theta_1 - \theta_2 = \frac{\pi}{2}$, in-phase coupling signal can still be generated. This can be shown as below:

With $\theta_1 - \theta_2 = \frac{\pi}{2}$, V_{GS1} and V_{GS2} can be expressed as:

$$V_{GS1}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1) - V_B \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$= \sqrt{V_A^2 + V_B^2} \cdot sin(\omega_0 \cdot t + \theta_{GS1})$$

$$V_{GS2}(t) = V_A \cdot sin(\omega_0 \cdot t + \theta_1 + \pi) - V_B \cdot sin(\omega_0 \cdot t + \theta_2)$$

$$= \sqrt{V_A^2 + V_B^2} \cdot sin(\omega_0 \cdot t + \theta_{GS2}) \tag{5.18}$$

where

$$\tan\theta_{GS1} = \frac{V_A \cdot sin\theta_1 - V_B \cdot sin\theta_2}{V_A \cdot cos\theta_1 - V_B \cdot cos\theta_2} = \frac{V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{-V_A \cdot sin\theta_2 - V_B \cdot cos\theta_2} = -\frac{\frac{V_A}{V_B} - tan\theta_2}{1 + \frac{V_A}{V_B} \cdot tan\theta_2}$$

$$sin\theta_{GS1} = \frac{V_A \cdot sin\theta_1 - V_B \cdot sin\theta_2}{\sqrt{V_A^2 + V_B^2 - 2 \cdot V_A \cdot V_B \cdot cos(\theta_1 - \theta_2)}} = \frac{V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{\sqrt{V_A^2 + V_B^2}}$$

$$\tan\theta_{GS2} = \frac{V_A \cdot sin(\theta_1+\pi) - V_B \cdot sin\theta_2}{V_A \cdot cos(\theta_1+\pi) - V_B \cdot cos\theta_2} = \frac{-V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{V_A \cdot sin\theta_2 - V_B \cdot cos\theta_2} = -\frac{\frac{V_A}{V_B}+tan\theta_2}{1-\frac{V_A}{V_B} \cdot tan\theta_2}$$

$$sin\theta_{GS2} = \frac{V_A \cdot sin(\theta_1+\pi) - V_B \cdot sin\theta_2}{\sqrt{V_A^2+V_B^2-2 \cdot V_A \cdot V_B \cdot cos(\theta_1+\pi-\theta_2)}} = \frac{-V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{\sqrt{V_A^2+V_B^2}} \quad (5.19)$$

Suppose $\gamma = arctan\frac{V_A}{V_B}$, it is obvious that $sin\gamma = \frac{V_A}{\sqrt{V_A^2+V_B^2}}$ and $cos\gamma = \frac{V_B}{\sqrt{V_A^2+V_B^2}}$. Hence equation (5.19) can be simplified as:

$$\tan\theta_{GS1} = -\frac{\frac{V_A}{V_B}-tan\theta_2}{1+\frac{V_A}{V_B} \cdot tan\theta_2} = \tan(\pi + \theta_2 - \gamma)$$

$$sin\theta_{GS1} = \frac{V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{\sqrt{V_A^2+V_B^2}} = sin(\pi + \theta_2 - \gamma)$$

$$\tan\theta_{GS2} = -\frac{\frac{V_A}{V_B}+tan\theta_2}{1-\frac{V_A}{V_B} \cdot tan\theta_2} = \tan(\pi + \theta_2 + \gamma)$$

$$sin\theta_{GS2} = \frac{-V_A \cdot cos\theta_2 - V_B \cdot sin\theta_2}{\sqrt{V_A^2+V_B^2}} = sin(\pi + \theta_2 + \gamma) \quad (5.20)$$

Equation (5.18) indicates the amplitude of V_{GS1} and V_{GS2} are equal while equation (5.20) shows the phase of V_{GS1} and V_{GS2} are $\pi + \theta_2 - \gamma$ and $\pi + \theta_2 + \gamma$ respectively, which are symmetrical to $\pi + \theta_2$. Hence the drain current I_{C1} and I_{C2} have the same amplitude and their phase are $\pi + \theta_2 - \gamma$ and $\pi + \theta_2 + \gamma$ respectively, which are symmetrical to $\pi + \theta_2$. As the coupling current of the $Q+$ branch is equal to $I_{C1}(t) + I_{C2}(t)$, the phase of this coupling current is $\pi + \theta_2$ and is in phase with the current of the $Q+$ branch. As a result, in-phase coupling is achieved.

As mentioned above, for general case if $V_A \neq V_B$ then the phase of V_{GS} of the coupling transistor is too complicated to be analyzed. Hence here for a theoretical study, it is assumed that the amplitude of Design A's outputs are

equal as a simplified model to gain more insight of the mechanism.

5.1.3 Source of Phase Error

As mentioned in Chapter 3, the source of phase error and their impact varies between different QVCO topologies. Thus it is necessary to analyze the source of phase error for Design A. According to equation (5.10), the solution of β can be affected by variation of some parameters and phase error thus arises. These parameters include the free-running frequency, the Q value and the bias current of the two VCO cores, as well as the size and the threshold voltage of the coupling transistors. The effects of the variation of these parameters on the phase error are analyzed below.

(A) Mismatch between free-running frequencies

Suppose the free-running frequencies of the two VCO cores are ω_1 and ω_2 respectively. Substituting ω_1 and ω_2 into equation (5.10) accordingly, frequencies of the $I+$ and $Q+$ branches can be simplified as:

$$f_{I+} = \omega_1 + \frac{\omega_1}{2Q} \cdot \frac{-\frac{2}{\pi} \cdot P \cdot V_{th} \cdot [sin\frac{\beta}{2} - cos\frac{\beta}{2}]}{\frac{2}{\pi} \cdot I_0 + P \cdot V_A - P \cdot \frac{2}{\pi} V_{th} \cdot [sin\frac{\beta}{2} + cos\frac{\beta}{2}]}$$

$$= \omega_1 + \frac{\omega_1}{2Q} \cdot \frac{-\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot [sin(\frac{\beta}{2} - \frac{\pi}{4})]}{\frac{2}{\pi} \cdot I_0 + P \cdot V_A - P \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot [sin(\frac{\beta}{2} + \frac{\pi}{4})]}$$

$$f_{Q+} = \omega_2 + \frac{\omega_2}{2Q} \cdot \frac{-\frac{2}{\pi} \cdot P \cdot V_{th} \cdot [cos\frac{\beta}{2} - sin\frac{\beta}{2}]}{\frac{2}{\pi} \cdot I_0 - P \cdot V_A + P \cdot \frac{2}{\pi} V_{th} \cdot [sin\frac{\beta}{2} + cos\frac{\beta}{2}]}$$

$$= \omega_2 + \frac{\omega_2}{2Q} \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot [sin(\frac{\beta}{2} - \frac{\pi}{4})]}{\frac{2}{\pi} \cdot I_0 - P \cdot V_A + P \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot [sin(\frac{\beta}{2} + \frac{\pi}{4})]} \quad (5.21)$$

Suppose $\beta = \frac{\pi}{2} + \varphi$ when φ is the phase error, then equation (5.21) can be modified as:

$$f_{I+} = \omega_1 + \frac{\omega_1}{2Q} \cdot \frac{-\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\frac{\varphi}{2}}{\frac{2}{\pi} \cdot I_0 + P \cdot V_A - P \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot cos\frac{\varphi}{2}}$$

$$f_{Q+} = \omega_2 + \frac{\omega_2}{2Q} \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot sin\frac{\varphi}{2}}{\frac{2}{\pi} \cdot I_0 - P \cdot V_A + P \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot cos\frac{\varphi}{2}} \tag{5.22}$$

The exact solution of φ for $f_{I+} = f_{Q+}$ is complicated. However, for quick estimation, it is supposed that $\frac{\varphi}{2} < 0.1\ rad$ thus $sin\frac{\varphi}{2} \approx \frac{\varphi}{2}$ and $cos\frac{\varphi}{2} \approx 1$, hence $f_{I+} = f_{Q+}$ can be simplified as:

$$\omega_1 + \frac{\omega_1}{2Q} \cdot \frac{-\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot \frac{\varphi}{2}}{\frac{2}{\pi} \cdot I_0 + P \cdot V_A - P \cdot \frac{2\sqrt{2}}{\pi} V_{th}} = \omega_2 + \frac{\omega_2}{2Q} \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \frac{\varphi}{2}}{\frac{2}{\pi} I_0 - P \cdot V_A + P \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot} \tag{5.23}$$

and φ can be solved as:

$$\varphi = \frac{\sqrt{2} \cdot \pi \cdot Q}{P \cdot V_{th}} \cdot \frac{(\frac{2}{\pi} \cdot I_0)^2 - (P \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th})^2}{\frac{2}{\pi} \cdot I_0 \cdot (\omega_1 + \omega_2) + (P \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th}) \cdot (\omega_2 - \omega_1)} \cdot (\omega_1 - \omega_2) \tag{5.24}$$

As mentioned above, $|I_{osc}| > |I_{inj}|$. On the other hand, generally $\omega_1 + \omega_2 \gg \omega_2 - \omega_1$. Thus $\frac{2}{\pi} \cdot I_0 \cdot (\omega_1 + \omega_2) + (P \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th}) \cdot (\omega_2 - \omega_1)$ can be replaced by $\frac{2}{\pi} \cdot I_0 \cdot (\omega_1 + \omega_2)$ as approximation. As a result, equation (5.24) can be simplified as:

$$\varphi = \frac{\sqrt{2} \cdot \pi \cdot Q}{P \cdot V_{th}} \cdot \frac{(\frac{2}{\pi} \cdot I_0)^2 - (P \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th})^2}{\frac{2}{\pi} \cdot I_0 \cdot (\omega_1 + \omega_2)} \cdot (\omega_1 - \omega_2) \tag{5.25}$$

Equation (5.25) shows two important observations: (1) $|\varphi|$ is proportional to $|(\omega_1 - \omega_2)/(\omega_1 + \omega_2)|$; (2) for a fixed $|(\omega_1 - \omega_2)/(\omega_1 + \omega_2)|$, a smaller P leads to larger $|\varphi|$. It is also worth noting that if the difference between $\omega_1$and ω_2 is too big, there would be no valid solution for $f_{I+} = f_{Q+}$. In this case, proper oscillation cannot be sustained.

(B) Mismatch between the Q value of the two resonators

Suppose the Q values of the two resonators are Q_1 and Q_2 accordingly and

are substituted into equation (5.10). As the free-running frequencies of the two VCO cores are equal, β must fulfill the following equation

$$\frac{\omega_0}{2Q_1}\cdot\frac{-\frac{2}{\pi}\cdot P\cdot V_{th}\cdot\left[sin\left(\frac{\theta_1-\theta_2}{2}\right)-cos\left(\frac{\theta_1-\theta_2}{2}\right)\right]}{\frac{2}{\pi}\cdot I_0+P\cdot V_A-P\cdot\frac{2}{\pi}V_{th}\cdot\left[sin\left(\frac{\theta_1-\theta_2}{2}\right)+cos\left(\frac{\theta_1-\theta_2}{2}\right)\right]}$$

$$=\frac{\omega_0}{2Q_2}\cdot\frac{-\frac{2}{\pi}\cdot P\cdot V_{th}\cdot\left[cos\left(\frac{\theta_1-\theta_2}{2}\right)-sin\left(\frac{\theta_1-\theta_2}{2}\right)\right]}{\frac{2}{\pi}\cdot I_0-P\cdot V_A+P\cdot\frac{2}{\pi}V_{th}\cdot\left[cos\left(\frac{\theta_1-\theta_2}{2}\right)+sin\left(\frac{\theta_1-\theta_2}{2}\right)\right]} \quad (5.26)$$

It is obvious when $\beta=\frac{\pi}{2}$, the second terms for each side of equation (5.26) are both 0. In other words, in this case $\beta=\frac{\pi}{2}$ is always a valid solution and the phase error is 0 no matter the value of Q_1 and Q_2. Thus it is concluded that Q value alone does not affect the phase error for Design A if all other parameters are perfectly matched. However, it is worth to note when combine with mismatch of other parameters, the mismatch between Q value may affect the solution of β and causes phase error. An example of phase error caused by mismatches between multiple parameters will be illustrated in the later part of this section on Page 114~115.

(C): Mismatch between the parameter *P*

Since it is too complicated to treat the *P* parameter of each individual coupling transistor as an independent variable, only two general cases are considered here.

(C1) M_{C1}, M_{C4}, M_{C5} and M_{C8} have the same *P* value P_1 while M_{C2}, M_{C3}, M_{C6} and M_{C7} have the same *P* value P_2. Substituting P_1 and P_2 into equation (5.10), in this case β must fulfill the following equation:

$$V_A\cdot(P_1-P_2)\cdot sin\frac{\beta}{2}\cdot cos\frac{\beta}{2}=\frac{2}{\pi}\cdot V_{th}\cdot(P_1\cdot cos\frac{\beta}{2}-P_2\cdot sin\frac{\beta}{2}) \quad (5.27)$$

Similar to case (A), the exact solution for equation (5.27) is complicated and not intuitive. However, with the assumption that $\frac{\varphi}{2}<0.1\,rad$, $sin\frac{\varphi}{2}\approx\frac{\varphi}{2}$ and

$cos\frac{\varphi}{2} \approx 1$. Thus equation (5.27) can be simplified as:

$$\frac{1}{2}\cdot V_A\cdot(P_1-P_2)\cdot\left(1-\frac{\varphi^2}{4}\right)=\frac{\sqrt{2}}{\pi}\cdot V_{th}\cdot[P_1-P_2+(P_1+P_2)\cdot\frac{\varphi}{2}] \tag{5.28}$$

φ can then be solved as:

$$\varphi_{\,1}=2\cdot\frac{-\frac{2\sqrt{2}}{\pi}\cdot V_{th}\cdot(P_1+P_2)+\sqrt{\frac{8}{\pi^2}\cdot V_{th}^2\cdot(P_1+P_2)^2+(V_A^2-V_A\cdot\frac{\sqrt{2}}{\pi}\cdot V_{th})(P_1-P_2)^2}}{V_A\cdot(P_2-P_1)}$$

$$\varphi_{\,2}=2\cdot\frac{-\frac{2\sqrt{2}}{\pi}\cdot V_{th}\cdot(P_1+P_2)-\sqrt{\frac{8}{\pi^2}\cdot V_{th}^2\cdot(P_1+P_2)^2+(V_A^2-V_A\cdot\frac{\sqrt{2}}{\pi}\cdot V_{th})(P_1-P_2)^2}}{V_A\cdot(P_2-P_1)} \tag{5.29}$$

Suppose $P_1+P_2 \gg |P_2-P_1|$ and $\frac{2}{\pi^2}\cdot V_{th}^2\cdot(P_1+P_2)^2 \gg (V_A^2-V_A\cdot\frac{\sqrt{2}}{\pi}\cdot V_{th})(P_1-P_2)^2$, thus $\sqrt{\frac{8}{\pi^2}\cdot V_{th}^2\cdot(P_1+P_2)^2+(V_A^2-V_A\cdot\frac{\sqrt{2}}{\pi}\cdot V_{th})(P_1-P_2)^2}$ can be simplified as $\frac{2\sqrt{2}}{\pi}\cdot V_{th}\cdot(P_1+P_2)\cdot(1+\frac{(V_A^2-V_A\cdot\frac{\sqrt{2}}{\pi}\cdot V_{th})(P_1-P_2)^2}{\frac{4\sqrt{2}}{\pi}\cdot V_{th}\cdot(P_1+P_2)})$. In this case $\varphi_{\,2}$ is not a valid solution according to $\frac{\varphi}{2}<0.1\ rad$ and $\varphi_{\,1}$ is the only solution. As a result, $\varphi_{\,1}$ can be simplified as:

$$\varphi=\frac{(V_A-\frac{\sqrt{2}}{\pi}\cdot V_{th})\cdot(P_2-P_1)}{\frac{4\sqrt{2}}{\pi}\cdot V_{th}\cdot(P_1+P_2)} \tag{5.30}$$

Obviously, equation (5.30) shows $|\varphi|$ is proportional to $|(P_1-P_2)/(P_1+P_2)|$. In other words, in this case $|\varphi|$ is determined by the ratio between P_1 and P_2.

(C2) M_{C1}, M_{C2}, M_{C3} and M_{C4} have the same P value P_1 while M_{C5}, M_{C6}, M_{C7} and M_{C8} have the same P value P_2. Substituting P_1 and P_2 into equation (5.10) accordingly, similar to (B) it can be found that $\beta=\frac{\pi}{2}$ is always a valid solution and phase error is 0 regardless the value of P_1 and P_2 for this case.

(D): Mismatch of the threshold voltages between the coupling transistors;

Similar to (C), since it is too complicated to treat V_{th} of each individual

coupling transistor as an independent variable, only two general cases are considered here.

(D1) M_{C1}, M_{C4}, M_{C5} and M_{C8} have the same threshold voltage V_{th1} while M_{C2}, M_{C3}, M_{C6} and M_{C7} have the same threshold voltage V_{th2}. Substituting V_{th1} and V_{th2} into equation (5.10) accordingly, in this case β must fulfill the following equation:

$$V_{th2} \cdot sin\frac{\beta}{2} - V_{th1} \cdot cos\frac{\beta}{2} = 0 \tag{5.31}$$

and the solution is:

$$\beta = 2arctan\frac{V_{th1}}{V_{th2}} \tag{5.32}$$

Thus $|\varphi| = \left|\frac{\pi}{2} - 2arctan\frac{V_{th1}}{V_{th2}}\right|$. For case $\left|\frac{V_{th1}}{V_{th2}}\right| = 1.05$, the phase error is 2.8º.

(D2) M_{C1}, M_{C2}, M_{C3} and M_{C4} have the same threshold voltage V_{th1} while M_{C5}, M_{C6}, M_{C7} and M_{C8} have the same threshold voltage V_{th2}. Substituting V_{th1} and V_{th2} into equation (5.10) accordingly, it can be found $\beta = \frac{\pi}{2}$ is always a valid solution and the phase error is 0 no matter the value of V_{th1} and V_{th2} for this case.

(E): Mismatch between the bias current of the two VCO cores

Suppose the bias current of the two VCO cores are I_1 and I_2 accordingly and are substituted into equation (5.10). Similar to (B), it can be found that $\beta = \frac{\pi}{2}$ is always a valid solution and the phase error is 0 regardless the value of are I_1 and I_2 for this case. Thus it is concluded that the bias current alone does not affect the phase error if all other parameters are perfectly matched.

To verify the analysis above, Design A is first designed with ideal elements whose parasitic capacitance is eliminated. It is simulated while the parameters

mentioned above are varied accordingly. The free-running frequency is 2.25 GHz and the current consumption is 2.7 mA. As shown in Figures 5.2 and 5.3, the simulated phase error matches the calculated result based on analysis above.

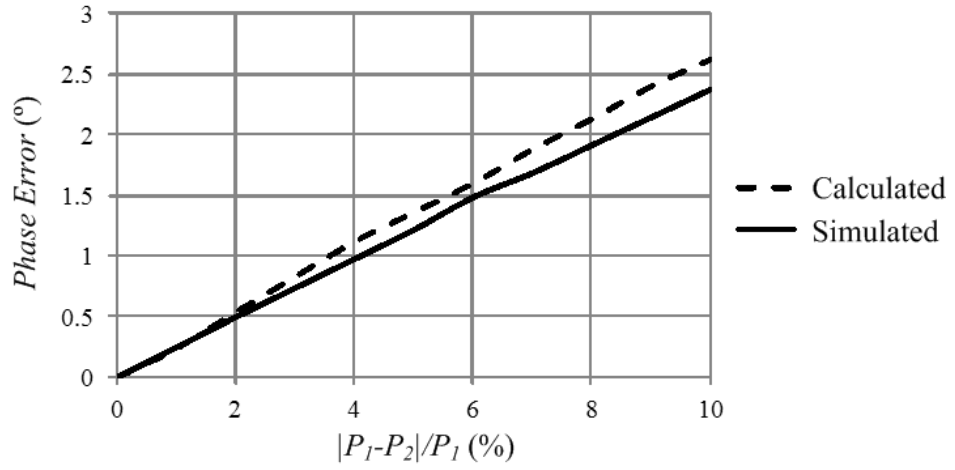


Figure 5. 2 Phase error due to mismatch of parameter P

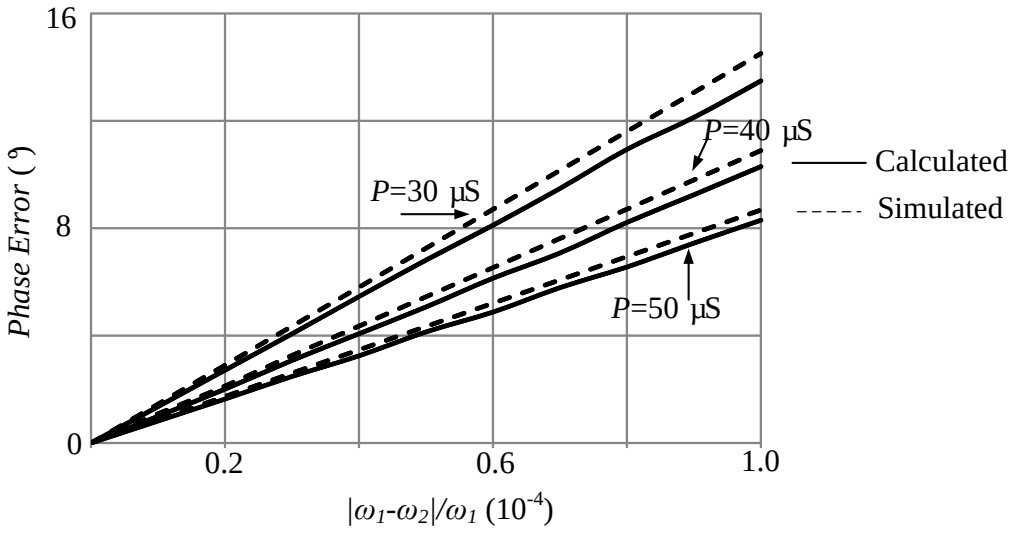


Figure 5. 3 Phase error due to mismatch of free-running frequency at different value of *P* parameters

Note in Figure 5.2, the mismatches of parameter *P* are based on the case (C1) mentioned above. As in the analysis for case (C1), the three assumptions below

are made: (1) $\frac{\varphi}{2} < 0.1\,rad$; (2) $P_1 + P_2 \gg |P_2 - P_1|$ and (3) $\frac{2}{\pi^2} \cdot V_{th}^2 \cdot (P_1 + P_2)^2 \gg (V_A^2 - V_A \cdot \frac{\sqrt{2}}{\pi} \cdot V_{th})(P_1 - P_2)^2$.

In the analysis above, the sources of phase error are treated as independent to each other and occur solely, however this may not be valid in practice. For instance, P is proportional to the width of the coupling transistors since $P = K \cdot v_{sat} \cdot C_{ox} \cdot W$. Suppose the width of the coupling transistors M_{C1}, M_{C2}, M_{C3} and M_{C4} are W_1 while the width of M_{C5}, M_{C6}, M_{C7} and M_{C8} are W_2, then M_{C1}, M_{C2}, M_{C3} and M_{C4} have the same P value P_1 while M_{C5}, M_{C6}, M_{C7} and M_{C8} have the same P value P_2. According to analysis for case (C2), in this case the phase error should be 0. However, since the size of the coupling transistors are not identical, the parasitic capacitances introduced to the two VCO cores are different thus the free-running frequencies of the two VCO cores are ω_1 and ω_2 respectively. Substitute these parameters into equation (5.22), frequencies of the $I+$ and $Q+$ branches can be simplified as:

$$f_{I+} = \omega_1 + \frac{\omega_1}{2Q} \cdot \frac{-\frac{2\sqrt{2}}{\pi} \cdot P_2 \cdot V_{th} \cdot sin\frac{\varphi}{2}}{\frac{2}{\pi} I_0 + P_2 \cdot V_A - P_2 \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot cos\frac{\varphi}{2}}$$

$$f_{Q+} = \omega_2 + \frac{\omega_2}{2Q} \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot P_1 \cdot V_{th} \cdot sin\frac{\varphi}{2}}{\frac{2}{\pi} \cdot I_0 - P_1 \cdot V_A + P_1 \cdot \frac{2\sqrt{2}}{\pi} V_{th} \cdot cos\frac{\varphi}{2}} \tag{5.33}$$

Thus φ can be solved as:

$$\varphi = 4 \cdot Q \cdot (\omega_1 - \omega_2) \cdot \frac{\left(\frac{2}{\pi} \cdot I_0 - P_1 \cdot V_A + \frac{2\sqrt{2}}{\pi} \cdot P_1 \cdot V_{th}\right) \cdot \left(\frac{2}{\pi} \cdot I_0 + P_2 \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P_2 \cdot V_{th}\right)}{\omega_1 \cdot \frac{2\sqrt{2}}{\pi} \cdot P_2 \cdot V_{th} \cdot \left(\frac{2}{\pi} \cdot I_0 - P_1 \cdot V_A + \frac{2\sqrt{2}}{\pi} \cdot P_1 \cdot V_{th}\right) + \omega_2 \cdot \frac{2\sqrt{2}}{\pi} \cdot P_1 \cdot V_{th} \cdot \left(\frac{2}{\pi} \cdot I_0 + P_2 \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P_2 \cdot V_{th}\right)} \tag{5.34}$$

Though complicated, equation (5.34) shows that in this case φ varies not only with the ratio between P_1 and P_2 but also with the absolute value of P_1 and P_2. If the ratio of P_1/P_2 is fixed, a smaller value of P_1 leads to larger $|\varphi|$, which

is similar as the case (A).

Analysis above also shows that when considering the overall phase error due to combination of various sources, the effect should be studied case-by-case. However, this sometimes made the analysis very complicated and not intuitive. Hence here only a simplified but intuitive discussion on such combination is provided as an illustration.

According to the phase error analysis above, it is essential to minimize the mismatch between the free-running frequency, size of the coupling transistor as well as the parasitic capacitance of the signal path. Thus central symmetrical layout style should be adopted. Layout arrangement of the transistor of the two VCO cores as well as the varactors is shown in Figure 5.4(a). Since the 8 coupling transistors are identical in size and each output of the VCO cores are connected to two coupling transistor's gate and source, it is convenient to apply central symmetrical layout style for the coupling circuitry, as shown in Figure 5.4(b). Theoretically, a perfectly matched layout can achieve 0° phase error in post-layout simulation. Unfortunately, due to inevitable asymmetry of parasitic elements introduced in the layout, in practice it is very difficult to achieve 0° phase error. By proper symmetrical layout design and compensation method, phase error can be optimized to a certain level. However, further improvement requires many iterations of check and compensation for each element hence too time consuming considering the unavoidable process, voltage and temperature variation.

The phase error analysis above also indicates the possible approaches for phase error tuning. Generally, phase error tuning can be achieved by introducing mismatch between free-running frequencies or the parameter *P*

intentionally. Although theoretically phase error tuning can also be achieved by varying the threshold voltage of the coupling transistor, equation (5.32) shows the phase error introduced by varying the threshold voltage is only determined by the ration of V_{th1} and V_{th2}, hence the degree of freedom to choose proper value V_{th1} and V_{th2} for a certain phase error is limited.

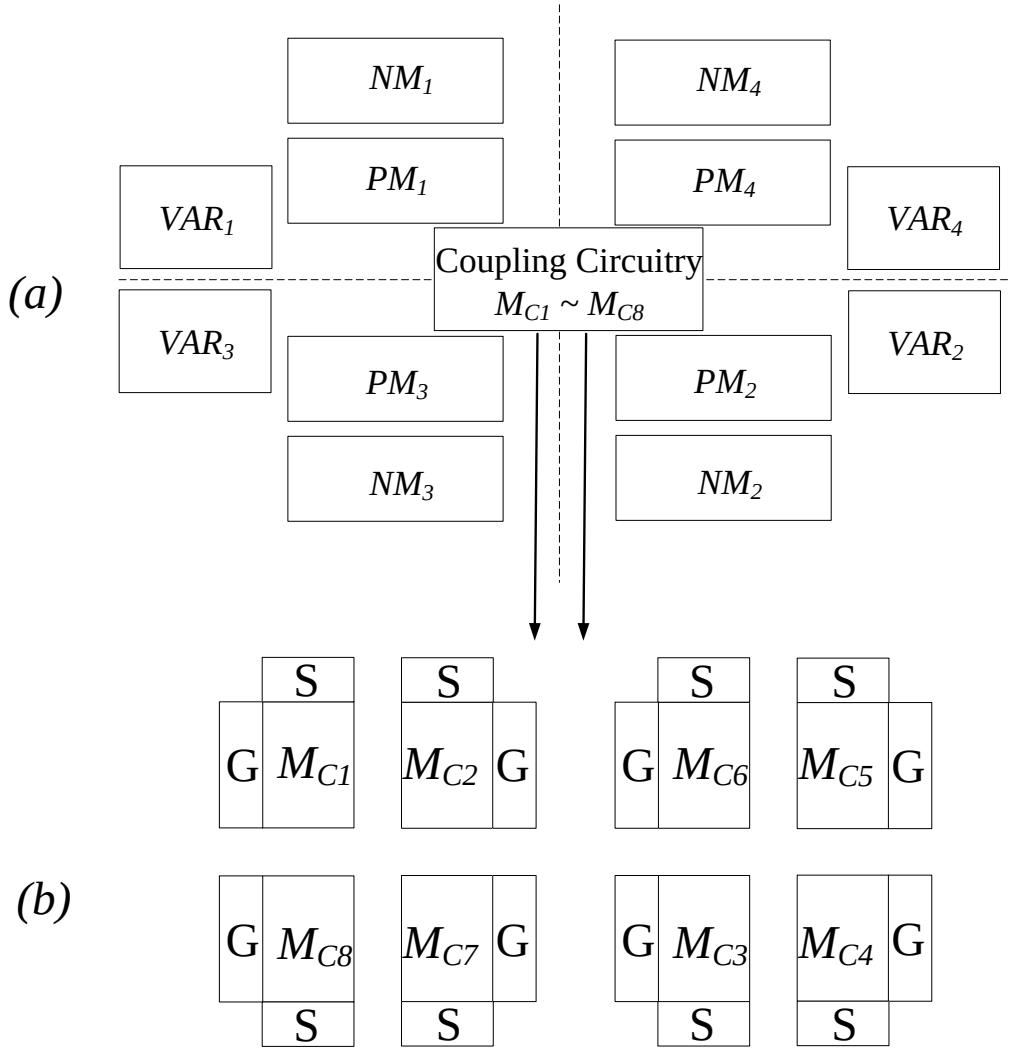


Figure 5. 4 Layout arrangement for transistors and varactors of the VCO core (a) and Layout of the coupling transistors (b). Note the drain terminals of coupling transistors are all connected to VDD.

Analysis above also shows a larger parameter *P* can help to reduce the phase error. On the other hand, as the coupling current is in phase with the coupled

current for Design A, the VCO core oscillate at frequency that the Q value of the VCO core does not degrade. As the coupling factor m is proportional to the parameter P, it can be concluded that the trade-off between the phase noise and phase error due to the coupling factor m for conventional parallel QVCO does not exists for Design A.

5.1.4 Simulation and Measurement Results

Design A is fabricated in GlobalFoundries CMOS 0.18 μm technology. The die photograph is shown in Figure 5.5.

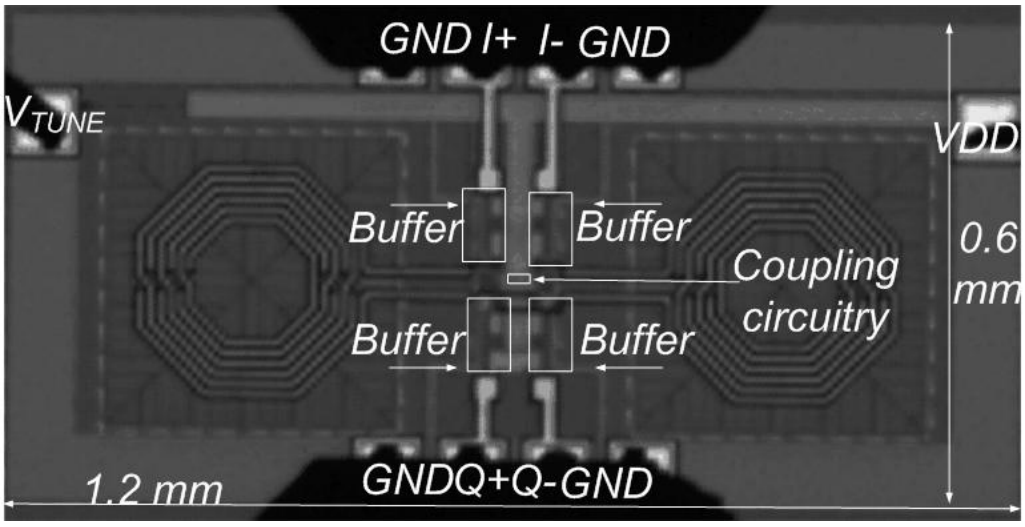


Figure 5. 5 Die photograph of Design A

The tuning range of Design A is from 2.55 GHz to 2.91 GHz and the power consumption is 4.3 mW with a 1.8 V power supply. The measurement setup for phase error is shown in Figure 5.6 where Design A is labelled as DUT. The DC voltage supply and DC signals are provided by the HP 4141 Modular DC source/monitor unit. The waveform of the output signal is observed with RF probe connecting to Lecroy WaveMaster 8600A oscilloscope whose sampling

rate is 20 GSa/sec and the phase error is calculated. Same setup for phase error measurement is applied to other QVCO proposed in this chapter.

Figures 5.7 and 5.8 show the measured spectrum and waveform of Design A at 2.582 GHz respectively. The phase error is 0.1 ºand the amplitude error is 2%. The distortion on the waveform is due to the output buffer.

The measured phase noise of Design A at 2.55 GHz is shown in Figure 5.9. The measured phase noise at 1 MHz offset frequency is -122.13 dBc/Hz. Figure 5.10 shows the post-layout simulated phase noise versus frequency within the tuning range.

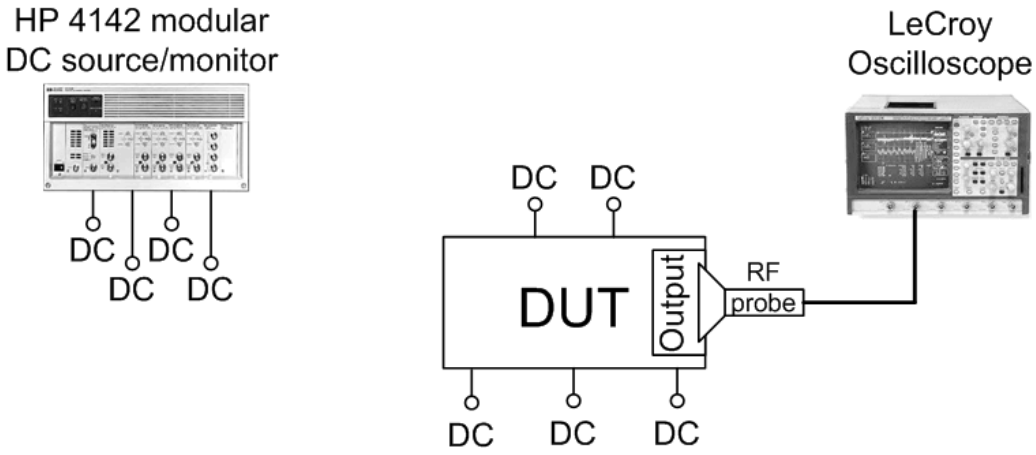


Figure 5. 6 Phase error measurement setup for Design A

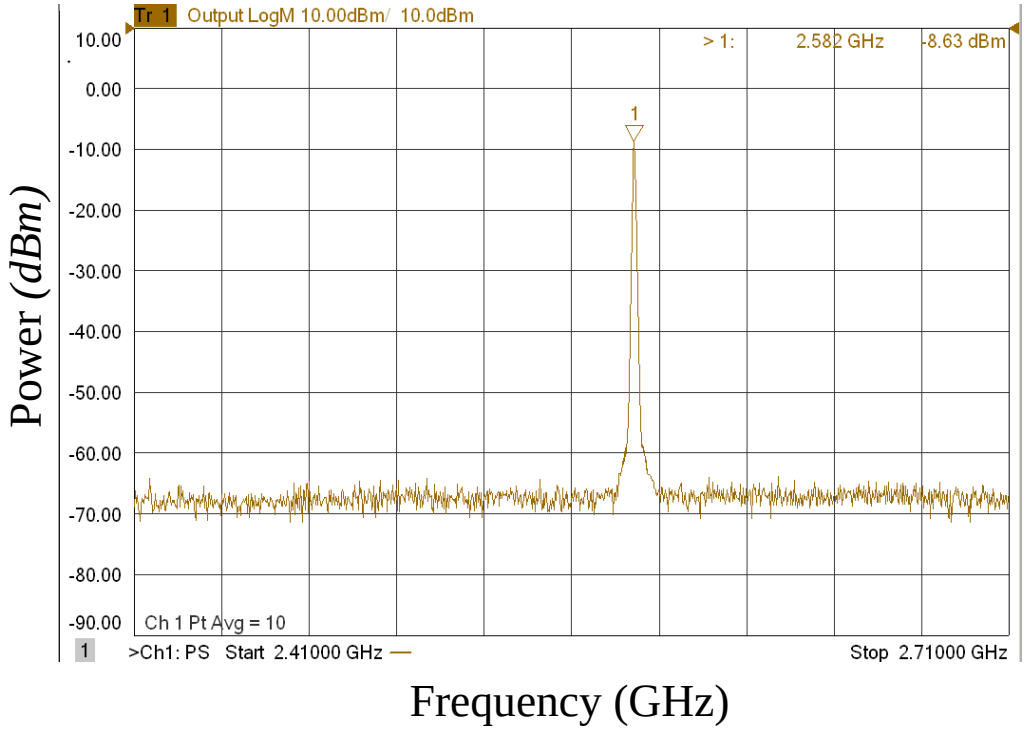


Figure 5. 7 Measured spectrum of Design A at 2.582 GHz

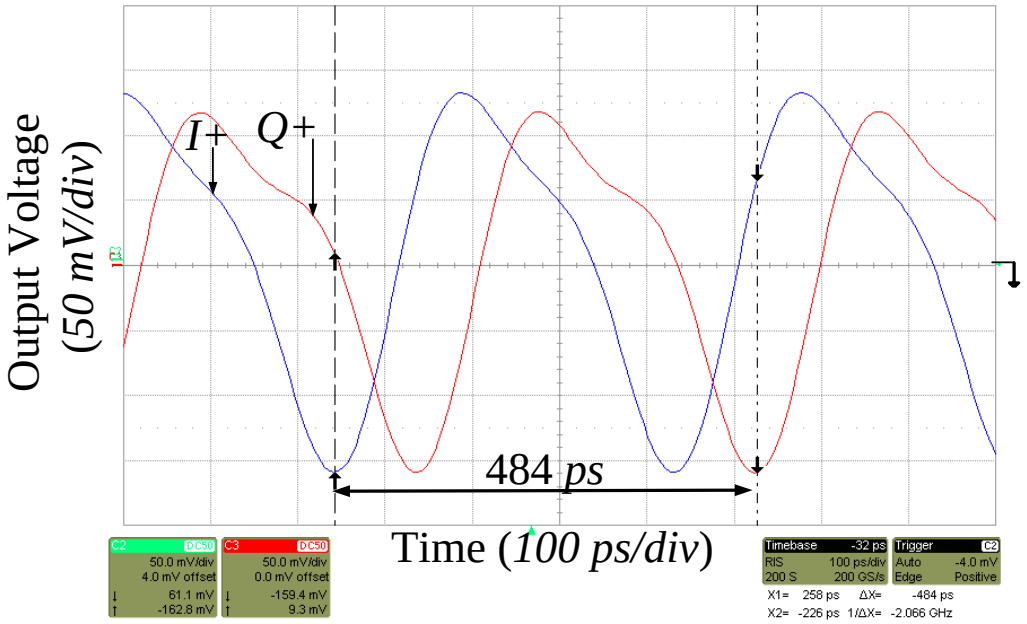


Figure 5. 8 Measured waveform of Design A at 2.582 GHz

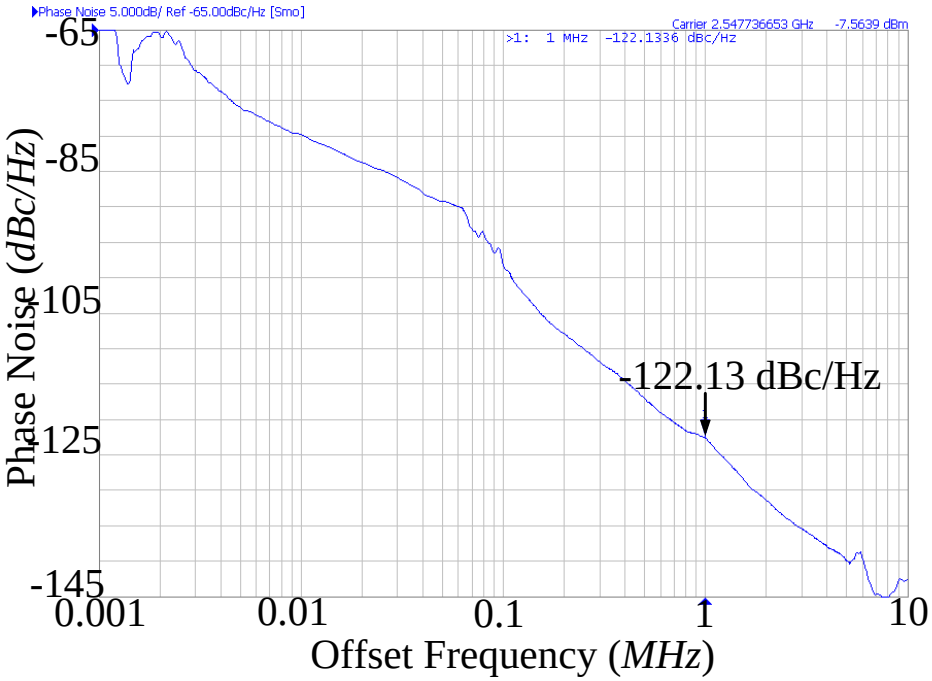


Figure 5. 9 Measured phase noise of Design A at 2.55 GHz

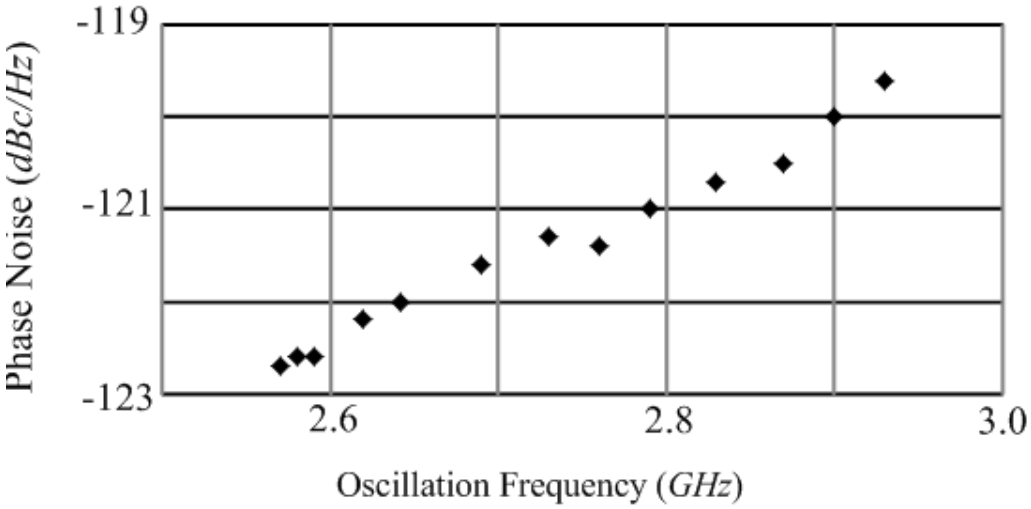


Figure 5. 10 Post-layout simulated phase noise versus different frequency for Design A

The transient waveform for V_{GS} and drain current of the coupling transistor M_{C1} are simulated and shown in Figure 5.11. As predicted in the analysis above, the phase of the current is the same as V_{GS} while M_{C1} is on for less than half a

cycle and works in either off or saturation region. The rms value of I_{C1} is only about 10 μA. Note the current consumption of each VCO core is about 1.2 mA \from a 1.8 V power supply. Hence it can be calculated that power consumed by the 8 coupling transistors is less than 2% of the total power consumption of Design A.

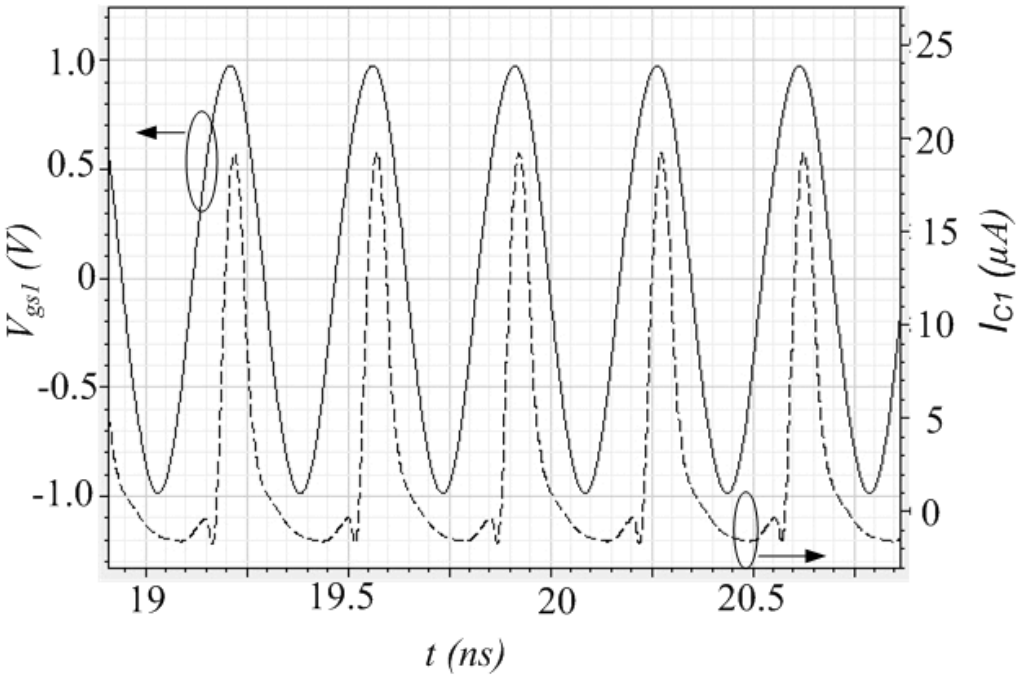


Figure 5. 11 Simulated V_{GS} and I_{C1} of M_{C1}

5.2 Novel IPC QVCO with Tuneable Phase Error

5.2.1 Schematic and Analysis

As analyzed in Section 5.1.3, there are several parameters that lead to phase error for Design A. On the other hand, it also indicates phase error can be tuned by adjusting these parameters knowingly. According to the analysis, there are at least two possible approaches to realize phase error tuning, namely introducing imbalance between the free-running frequencies of the VCO cores or between the coupling transistors. Thus a novel phase error tuning scheme is proposed,

which will be referred to as Design B below.

The schematic of Design B is shown in Figure 5.12. Compare with Design A proposed in Section 5.1, the drain terminals of the coupling transistor are no longer connected to VDD but to a pair of externally set voltage V_{bias2} and V_{bias3}. In Section 5.1, the drain terminals of the coupling transistors are connected to VDD to ensure that they work in either off or saturation region. Theoretically, as long as $V_{bias2,3} \geq V_{DC} + V_A - V_{th}$ where V_{DC} is the DC offset of the four output branches, these coupling transistors work in either off or saturation region. Furthermore, even if $V_{bias2,3}$ is so low that the coupling transistors is working in linear region, for the case $V_{bias2} = V_{bias3}$, the symmetrical nature of the proposed circuit ensures that $\beta = \frac{\pi}{2}$ is still a valid solution for a stable oscillation. The analysis below will focus on the case $V_{bias2} \geq V_{DC} + A - V_{th} > V_{bias3}$.

In practice, the parasitic capacitance of M_{C1}~M_{C4} are different from that of M_{C5}~M_{C8} when $V_{bias2} \neq V_{bias3}$. This introduces some difference between the free-running frequencies of the two VCO cores and phase error thus arises.

On the other hand, as $V_{DC} + V_A - V_{th} > V_{bias3}$, it is expected that M_{C5}~M_{C8} will enter into the linear region during operation. The actual drain current when transistor works in linear region is complicated thus for simplicity it is assumed the following relationship is valid:

$$I_{D,linear} = (1 - k_1) \cdot P \cdot (V_{GS} - V_{th}) = (1 - k_1) \cdot I_{D,sat} \tag{5.35}$$

where $I_{D,sat}$ is the drain current for a certain V_{GS} when the transistor works in saturation while $I_{D,linear}$ is the drain current for the same V_{GS} and a certain V_{DS}. k_1 is a coefficient whose value is between 0 and 1 which is determined by the

value of V_{DS}. Obviously, smaller V_{bias3} leads to smaller V_{DS} thus larger k_1.

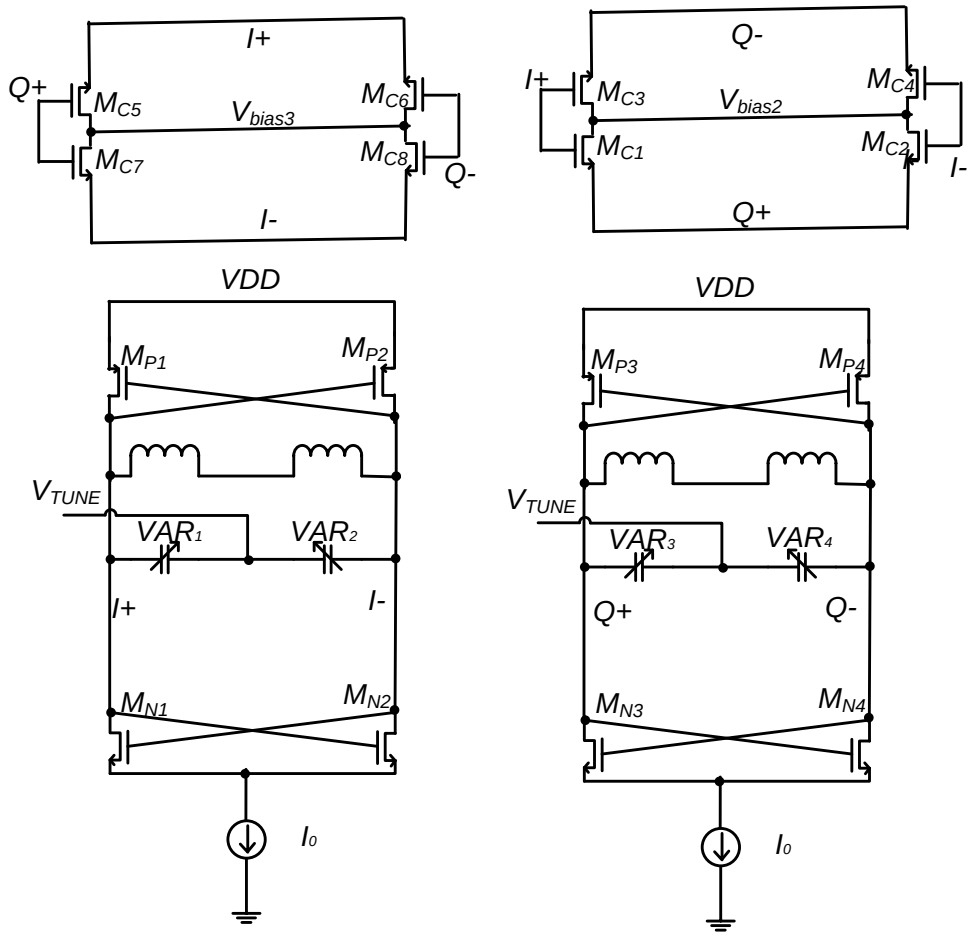


Figure 5. 12 Schematic of the Design B

With the help of equation (5.6) and following the same procedure presented in Section 5.1.1 the fundamental terms of i_d can be calculated as:

$$i_d = P \cdot \left[\frac{A}{2} - \frac{2}{\pi}V_{th} - k_1 \cdot \frac{A}{2} \cdot (sin2\theta_2 - sin2\theta_1)\right] = P' \cdot (\frac{A}{2} - \frac{2}{\pi}V_{th}) \qquad (5.36)$$

where θ_1 and θ_2 is the angle that transistor enters and leaves the linear region. It is obvious that for the same A, i_d calculated by equation (5.36) is smaller than that calculated by equation (5.6). Hence it can be treated as the $P' < P$. Note larger k_1 leads to smaller P' thus smaller V_{bias3} leads to smaller V_{DS} hence smaller P'.

With the help of equation (5.36), phase error for this case can be derived

from equation (5.34) as:

$$\varphi = 4 \cdot Q \cdot (\omega_1 - \omega_2) \cdot \frac{\left(\frac{2}{\pi} \cdot I_0 - P \cdot V_A + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th}\right) \cdot \left(\frac{2}{\pi} \cdot I_0 + P' \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P' \cdot V_{th}\right)}{\omega_1 \cdot \frac{2\sqrt{2}}{\pi} \cdot P' \cdot V_{th} \cdot \left(\frac{2}{\pi} \cdot I_0 - P \cdot V_A + \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th}\right) + \omega_2 \cdot \frac{2\sqrt{2}}{\pi} \cdot P \cdot V_{th} \cdot \left(\frac{2}{\pi} \cdot I_0 + P' \cdot V_A - \frac{2\sqrt{2}}{\pi} \cdot P' \cdot V_{th}\right)} \quad (5.37)$$

It can be observed from equation (5.37) that for the same $|\omega_1 - \omega_2|$ and the same P'/P, a smaller P leads to larger $|\varphi|$. Hence smaller P theoretically leads to larger phase error and hence the phase error tuning range increases. Note as defined in equation (5.1), P is proportional to the width of the coupling transistors. Thus a smaller P can be achieved with smaller transistors. In that case, the parasitic capacitance is smaller thus $|\omega_1 - \omega_2|$ is smaller for the same $|V_{bias2} - V_{bias3}|$ and the phase error tuning range is hence limited. This trade-off means P should be properly selected for the maximum phase error tuning range.

According to the case (C1) discussed in Section 5.1.3 and the fact that the parameter P can be varied by making the coupling transistor to spend a portion of each cycle working in the linear region, it can be concluded that phase error tuning can also be realized by the connection of coupling transistors as shown in Figure 5.13.

However, in this case the parasitic capacitance of the two VCO cores are still balanced thus the free-running frequencies of the two VCO cores are still equal. Hence the mechanism of the phase error tuning is only based on the mismatch between the parameter P, which is analyzed in case (C1). According to equation (5.29), in this case $|\varphi|$ is only determined by the ratio between $P'$and P. Compare with the coupling scheme shown in Figure 5.12, the later introduces one more degree of freedom on the value of P, thus the phase error

tuning range can be designed to be larger than that of shown in Figure 5.13.

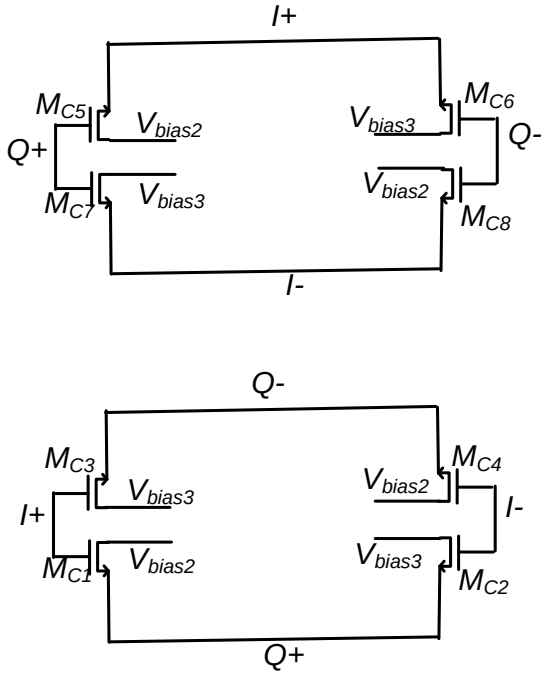


Figure 5. 13 Schematic of the coupling structure for phase error tuning based on case (C1)

Compare with the phase error tuning scheme proposed in [7], the proposed phase error tuning scheme does not require extra inductor and varactor which occupy large area. On the other hand, as shown in [6], for conventional PQVCO a smaller coupling factor is essential for good phase noise performance but it will increase the phase error. This trade-off limits the range of the coupling factor which determines the phase error tuning range given a limited tuning voltage. As shown in the analysis above, the proposed In-Phase Coupling scheme is free from such trade-off. Thus the parameter *P* can be properly selected for the maximum phase error tuning range. In addition, analysis above also considered the parasitic elements that are inevitable in practice. Note the impacts of these elements are ignored in the analysis of [6]. Furthermore, for the proposed phase error tuning scheme, both the free-running

frequency difference and mismatch of the parameter *P* which are the key parameters for phase error tuning are introduced by the coupling circuitry but not the VCO cores, hence the proposed phase error tuning scheme can also be applied to different VCO cores.

5.2.2 Simulation Results

Design B is designed in GlobalFoundries CMOS 0.18 μm technology. The layout is shown in Figure 5.14. Although it was sent for fabrication, but the chip is not ready for measurement. Hence post-layout simulation result is shown below.

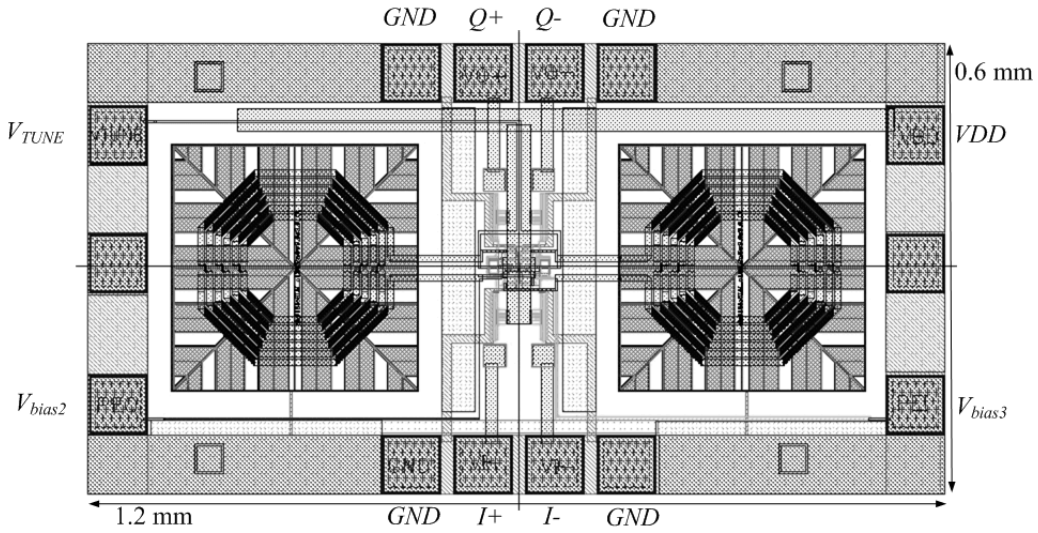


Figure 5. 14 Layout of Design B

The tuning range of Design B is from 2.56 GHz to 2.92 GHz and the power consumption is 4.1 mW with a 1.8 V power supply. The simulated phase error before phase error tuning is 0.6 ° at 2.56 GHz. The maximum phase shift happens when $V_{bias2} = 1.1$ V and $V_{bias3} = 0.6$ V a corresponding phase error

of 10.5 º. Simulated phase error versus $|V_{bias2} - V_{bias3}|$ at 2.56 GHz is shown in Figure 5.15.

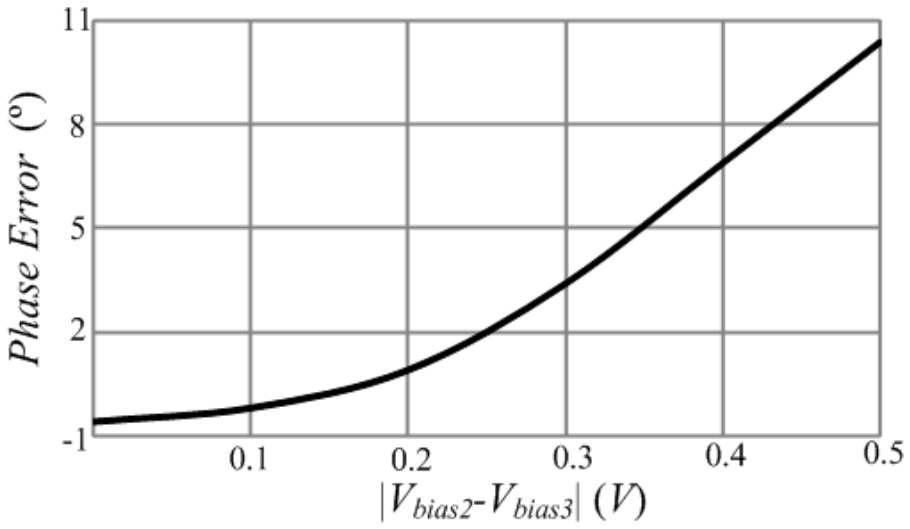


Figure 5. 15 Simulated phase error versus $|V_{bias2}-V_{bias3}|$

In addition, simulated phase error shift versus oscillation frequency for different $|V_{bias2}-V_{bias3}|$ is shown in Figure 5.16. It can be observed that for the same $|V_{bias2}-V_{bias3}|$, the phase error shift varies with frequency. The maximum variation is 3 degree. On the other hand, phase error shift versus $|V_{bias2}-V_{bias3}|$ is monotone-increasing. For the same frequency, phase error shift increases with $|V_{bias2}-V_{bias3}|$.

For the maximum phase error shift, oscillation frequency changes by about 300 kHz while the amplitude shifts by 8 mV. The relative amplitude error before and after phase error tuning is 1% and -1% respectively.

The simulated phase noise of Design B at 2.56 GHz is shown in Figure 5.17. The simulated phase noise at 1 MHz offset frequency is -123.0 dBc/Hz. On the other hand, phase noise difference before and after phase error tuning is less

than 0.2 dB, which is considered negligible. Figure 5.18 shows the post-layout simulated phase noise versus frequency within the tuning range.

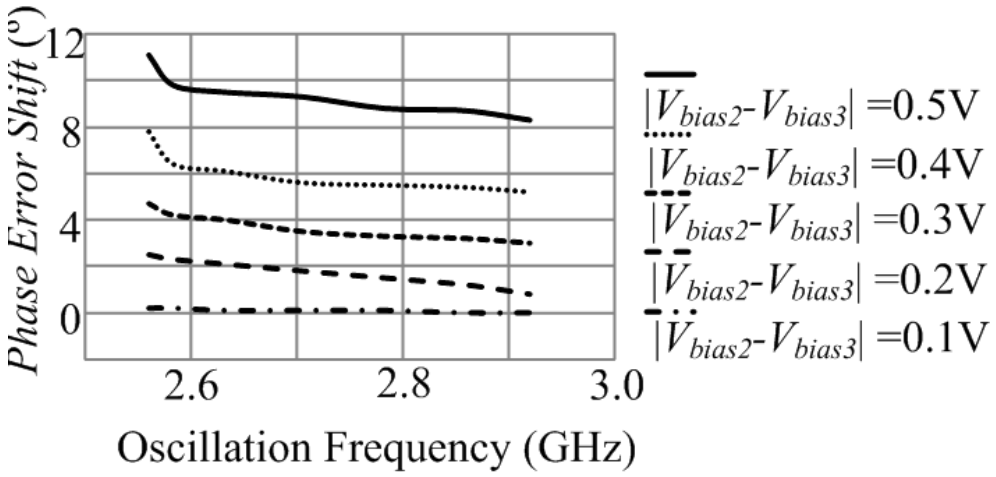


Figure 5. 16 Simulated phase error shift versus oscillation frequency for different $|V_{bias2}-V_{bias3}|$ for Design B

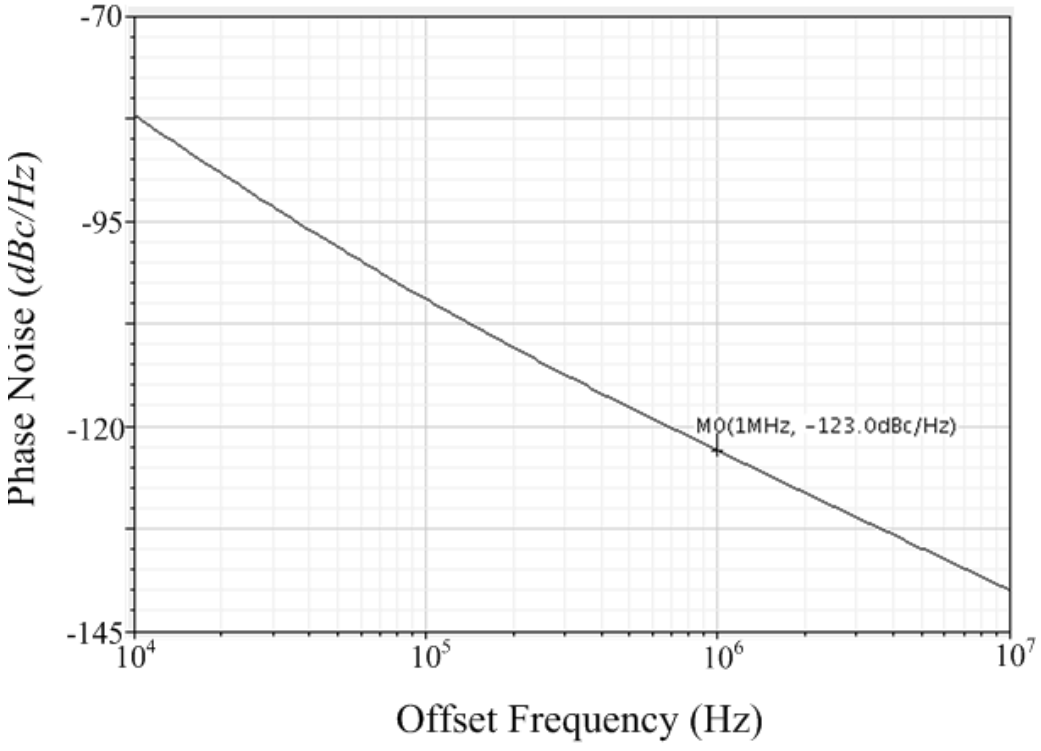


Figure 5. 17 Simulated phase noise of Design B at 2.56 GHz

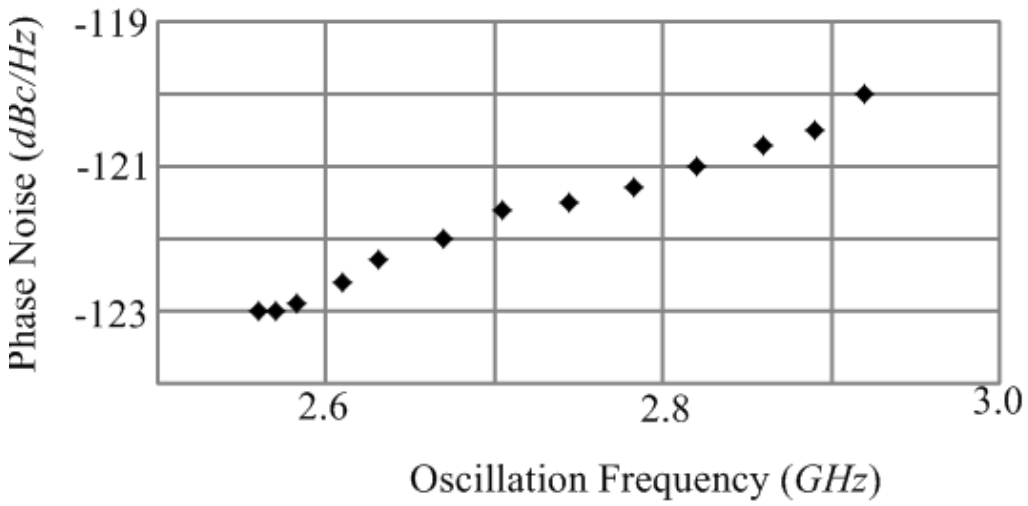


Figure 5. 18 Post-layout simulated phase noise versus different frequency for Design B.

5.3 Novel Class-C IPC QVCO with Tuneable Phase Error

5.3.1 Schematic and Analysis

As mentioned in Chapter 2, compared with the conventional LC VCO, Class-C VCO produces higher amplitude with the same current consumption. This property provides an advantage on phase noise performance per power consumption. Thus, it is attractive to design QVCO with Class-C VCO topology. However, the Class-C VCO topology limits the possible coupling scheme for quadrature signal generation.

For the IPC scheme proposed in this chapter, the coupling circuitry consumes less than 2% of the total power consumption of the QVCO and does not require extra component on the VCO core. Thus it is suitable to be employed in the Class-C QVCO. Besides, the free-running frequency of a Class-C VCO can be adjusted by tuning the parasitic capacitance of the VCO

core itself. Hence smaller value of the *P* parameter can be chosen and as a result the phase error tuning range is expected to be wider compare to the phase error tuning scheme proposed in Section 5.2. Detail will be discussed in the later part of this section on Page 132.

The schematic of the proposed IPC Class-C QVCO (which will be referred to as Design C below) is shown in Figure 5.19 Resistor R_2 is inserted between VDD and the VCO core to make the DC offset of VCO's output to be lower than VDD. By proper choice of R_2 this DC offset will be low enough to ensure the coupling transistors work in off or saturation region and the analysis shown in Section 5.1 can be applied directly.

Analysis for the in-phase coupling scheme and quadrature signal generation as well as the source of phase error is similar to that of the Design A with conventional LC VCO topology in Section 5.1 and thus will not be repeated here. One major difference is that the topology of Class-C QVCO introduces a degree of freedom to adjust the parasitic capacitance by varying V_{bias2} and V_{bias3}. Variation of the parasitic capacitance leads to variation of the free-running frequency of the individual VCO core. As analyzed in Section 5.1.3, this will cause phase error. In other words, phase error can now be tuned. Relationship between the phase error and the difference of the free-running frequencies of the two VCO cores can be derived following the same procedure shown in Section 5.1.3 as:

$$\varphi = \frac{\sqrt{2}\cdot\pi\cdot Q}{P\cdot V_{th}} \cdot \frac{I_0^2 - (P\cdot V_A - \frac{2\sqrt{2}}{\pi}\cdot P\cdot V_{th})^2}{I_0\cdot(\omega_1+\omega_2) + (P\cdot V_A - \frac{2\sqrt{2}}{\pi}\cdot P\cdot V_{th})\cdot(\omega_2-\omega_1)} \cdot (\omega_1 - \omega_2) \qquad (5.38)$$

Note the difference between equation (5.24) and equation (5.38) is due to the different I_{osc} of the two VCO topologies. According to equation (2.23), for

Class-C VCO $I_{osc} = I_0$.

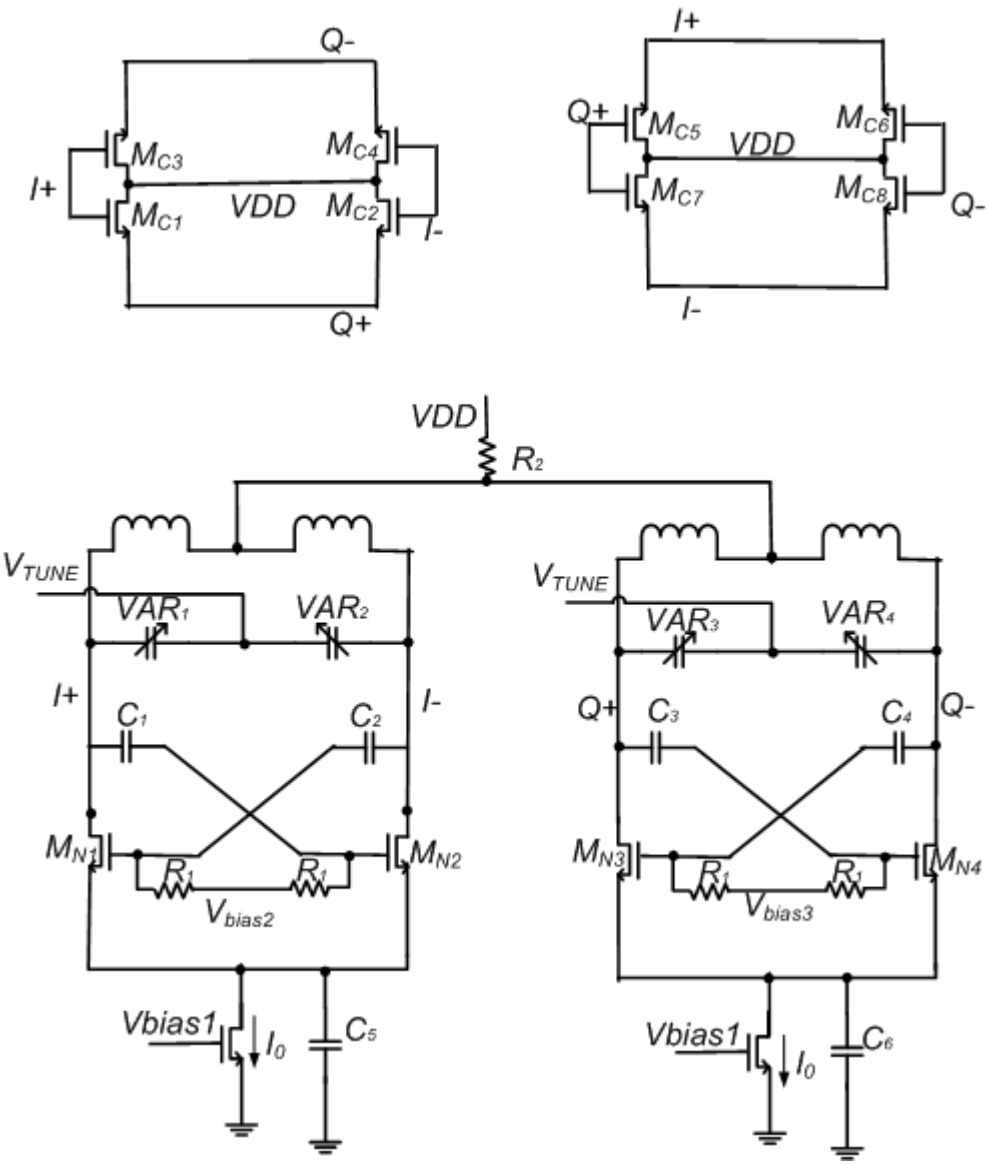


Figure 5. 19 Schematic of Design C

For Design C, variation of the parasitic capacitance can be realized by introducing voltage difference between V_{bias2} and V_{bias3}. As analyzed in Section 5.1.3, $|\varphi|$ is proportional to $|(\omega_1 - \omega_2)/(\omega_1 + \omega_2)|$. Thus it is expected that larger $|V_{bias2} - V_{bias3}|$ leads to larger $|\varphi|$. On the other hand, $|\varphi|$ is inversely proportional to P, thus for the same $|V_{bias2} - V_{bias3}|$, a smaller P will lead to larger $|\varphi|$, which leads to wider phase error tuning range. Simulated

$|\varphi|$ versus $|V_{bias2} - V_{bias3}|$ for different P parameters is shown in Figure 5.20.

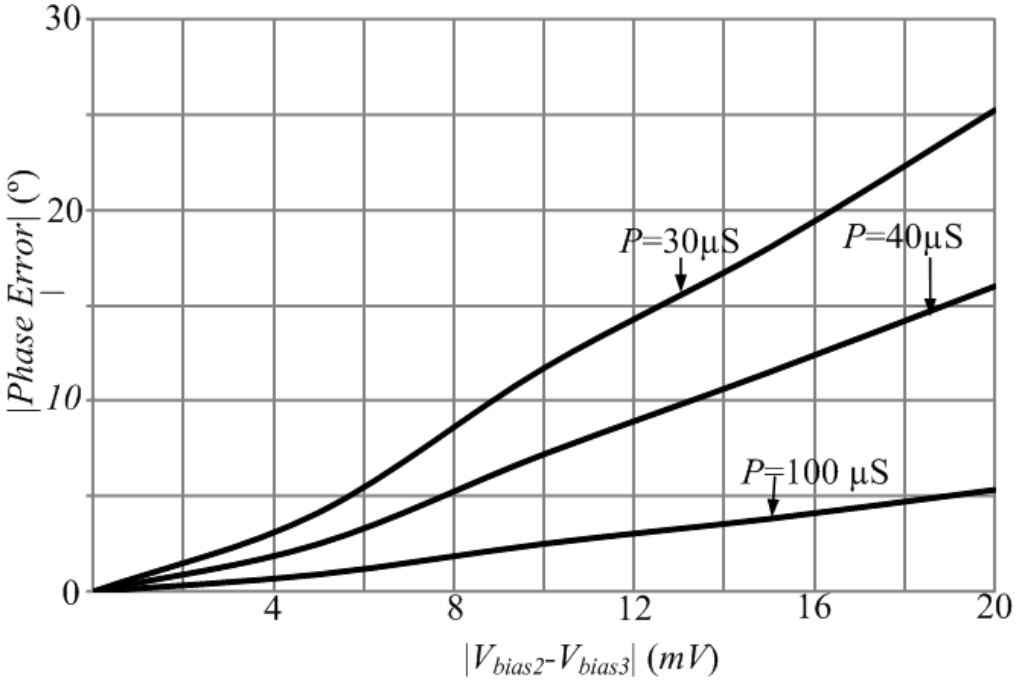


Figure 5. 20 Simulated absolute value of phase error versus $|V_{bias2} - V_{bias3}|$ for different P

As the P parameter is not a major contributor of the free-running frequency difference, the phase error tuning range can be expanded by shrinking the value of the P parameter. Theoretically, the phase error tuning range can be very wide if the P parameter is small enough. However in practice, the voltage accuracy of V_{bias2} and V_{bias3} is limited. Hence the phase error tuning accuracy is restricted by this limitation. As a result, there exists a trade-off between the phase error tuning range and phase accuracy for the P parameter.

Similar as the phase error tuning scheme proposed in Section 5.2, Design C is free from the trade-off on the coupling factor for the conventional parallel QVCO and does not require extra inductor and varator which occupy large area. Furthermore, as the free-running frequency of the VCO core is not tuned by the coupling circuitry, the size of the coupling transistor does not make a major

contribution on the variation range of this free-running frequency. As a result theoretically the phase error tuning range can be much wider compared with that proposed in Section 5.2. However as mentioned above, in practice the phase error tuning range is restricted by the voltage accuracy of V_{bias2} and V_{bias3}.

5.3.2 Measurement results

Design C is fabricated in GlobalFoundries CMOS 0.18 μm technology. The die photograph is shown in Figure 5.21.

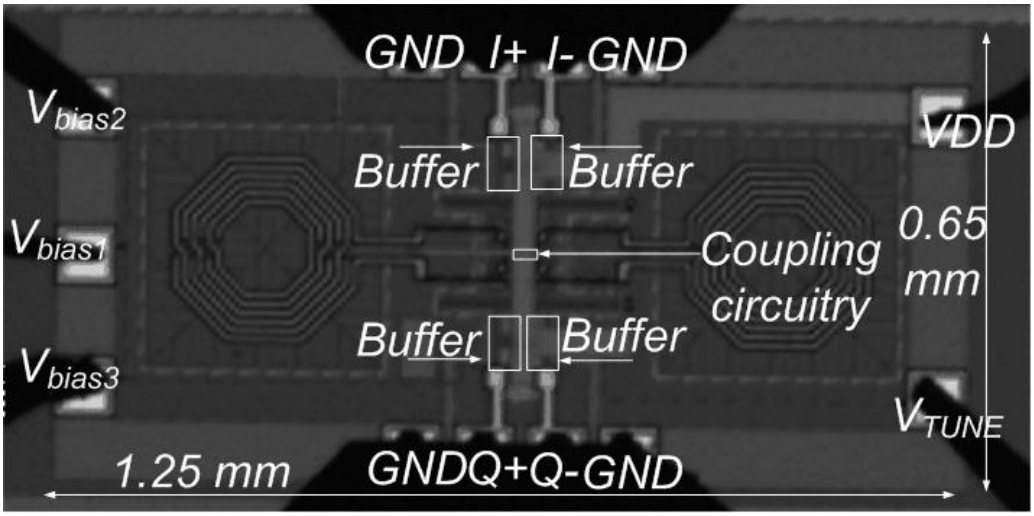


Figure 5. 21 Die photograph of Design C

The tuning range of Design C is from 2.5 GHz to 2.97 GHz and the power consumption is 3.6 mW with a 1.2 V power supply. Figures 5.22 and 5.23 show the measured spectrum and waveform of Design C at 2.623 GHz frequency with $V_{bias2} = V_{bias3}$. The phase error is 0.5°. After introducing voltage difference between V_{bias2} and V_{bias3} manually for measurement, phase error changes. Perfect quadrature generation may not be achieved in measurement

due to the accuracy limitation of externally set DC voltage V_{bias2} and V_{bias3} as well as the accuracy of the oscilloscope.

The maximum phase shift happens when V_{bias2} is larger than V_{bias3} by 20 mV with a corresponding phase error of 17 º. The shift in oscillation frequency is less than 1MHz while the amplitude shifts by 8 mV. Measured spectrum and waveform of Design C after phase error tuning are shown in Figures 5.24 and 5.25. Note the amplitude error before and after phase error tuning is 6% and -6% respectively. In addition, simulated phase error shift versus oscillation frequency for different $|V_{bias2}-V_{bias3}|$ is shown in Figure 5.26. It can be observed that for the same $|V_{bias2}-V_{bias3}|$, the phase error shift varies with frequency. The maximum variation is 4 degree. On the other hand, phase error shift versus $|V_{bias2}-V_{bias3}|$ is monotone-increasing. For the same frequency, phase error shift increases with $|V_{bias2}-V_{bias3}|$.

The measured and simulated phase noise at 2.5 GHz of Design C is shown in Figure 5.27 The measured phase noise at 1 MHz offset frequency is -126.8 dBc/Hz. In addition, Figure 5.28 shows the post-layout simulated phase noise versus frequency within the tuning range.

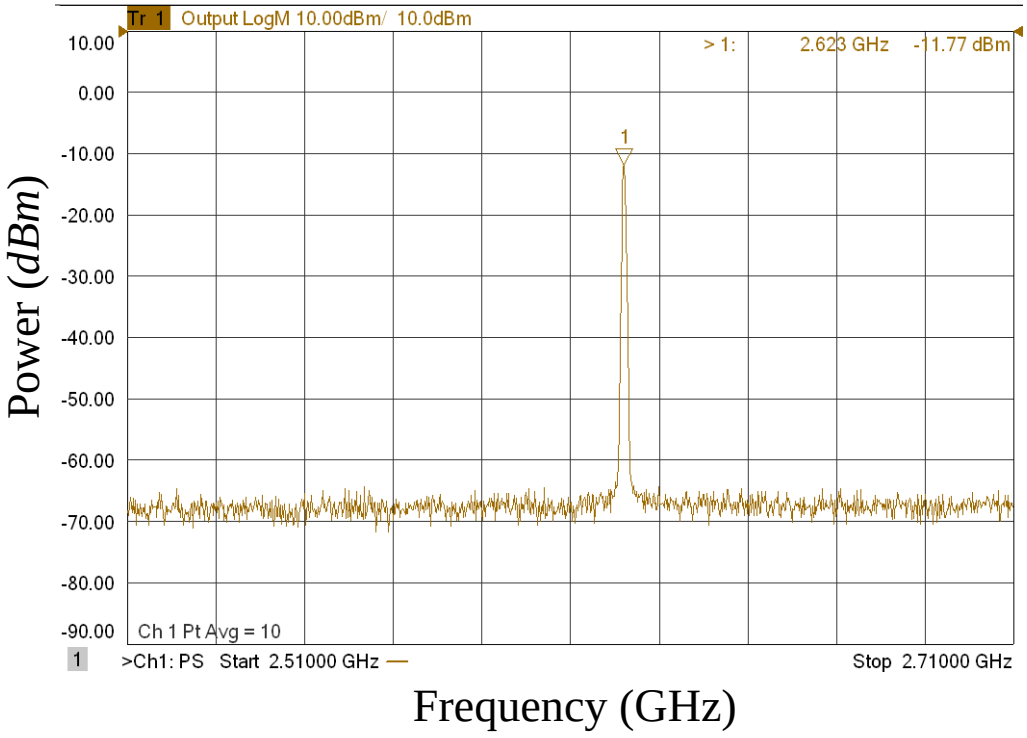


Figure 5. 22 Measured spectrum of Design C at 2.623 GHz before phase error tuning.

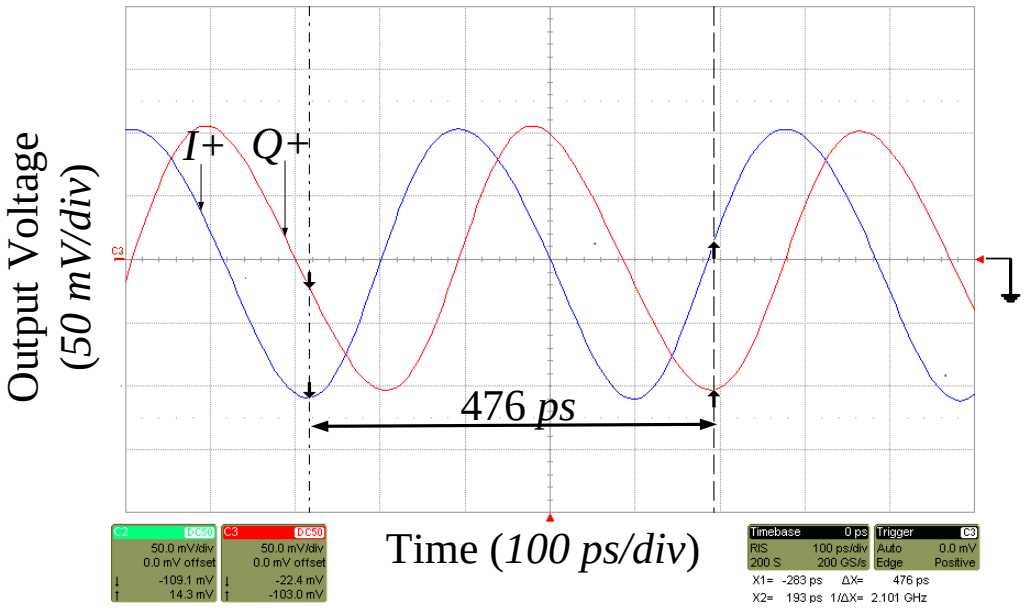


Figure 5. 23 Measured waveform of Design C at 2.623 GHz before phase error tuning.

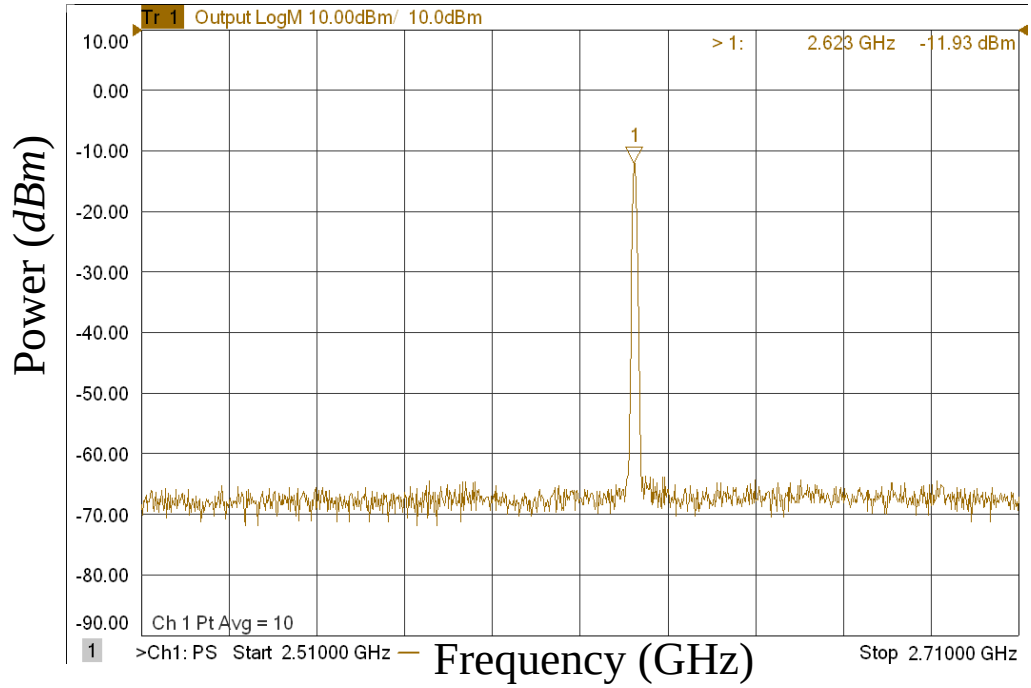


Figure 5. 24 Measured spectrum of Design C at 2.623 GHz after phase error tuning.

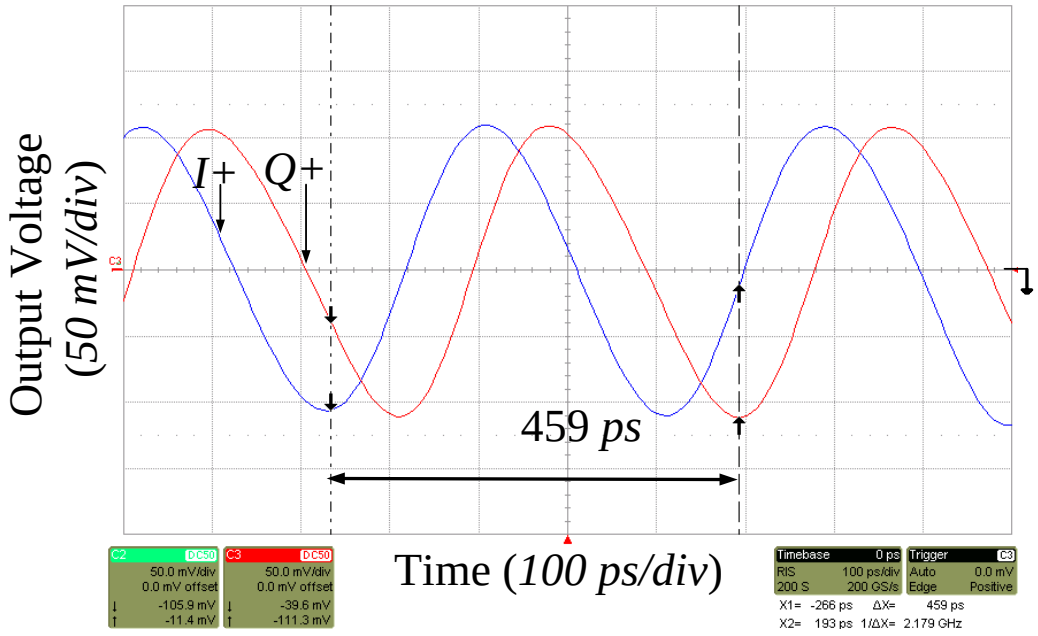


Figure 5. 25 Measured waveform (b) of Design C at 2.623 GHz after phase error tuning.

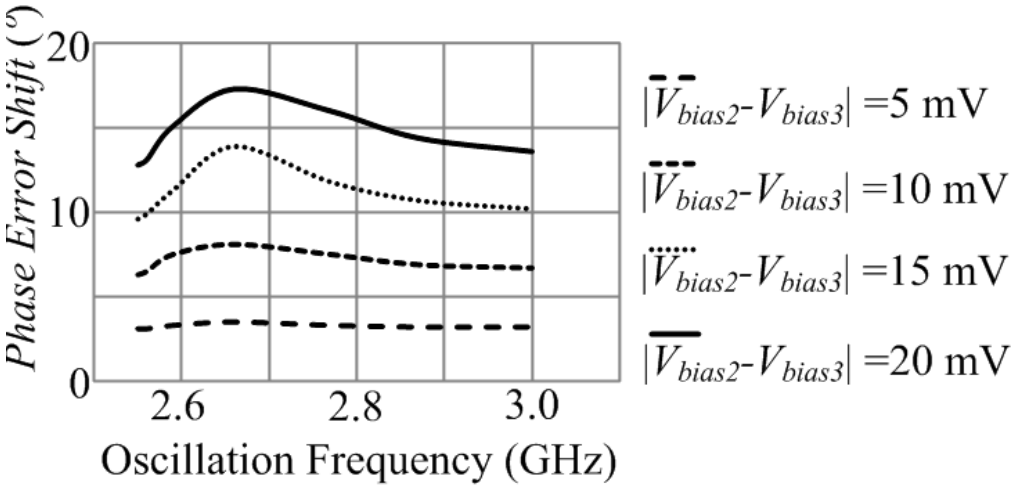


Figure 5. 26 Simulated phase error shift versus oscillation frequency for different $|V_{bias2}-V_{bias3}|$for Design C

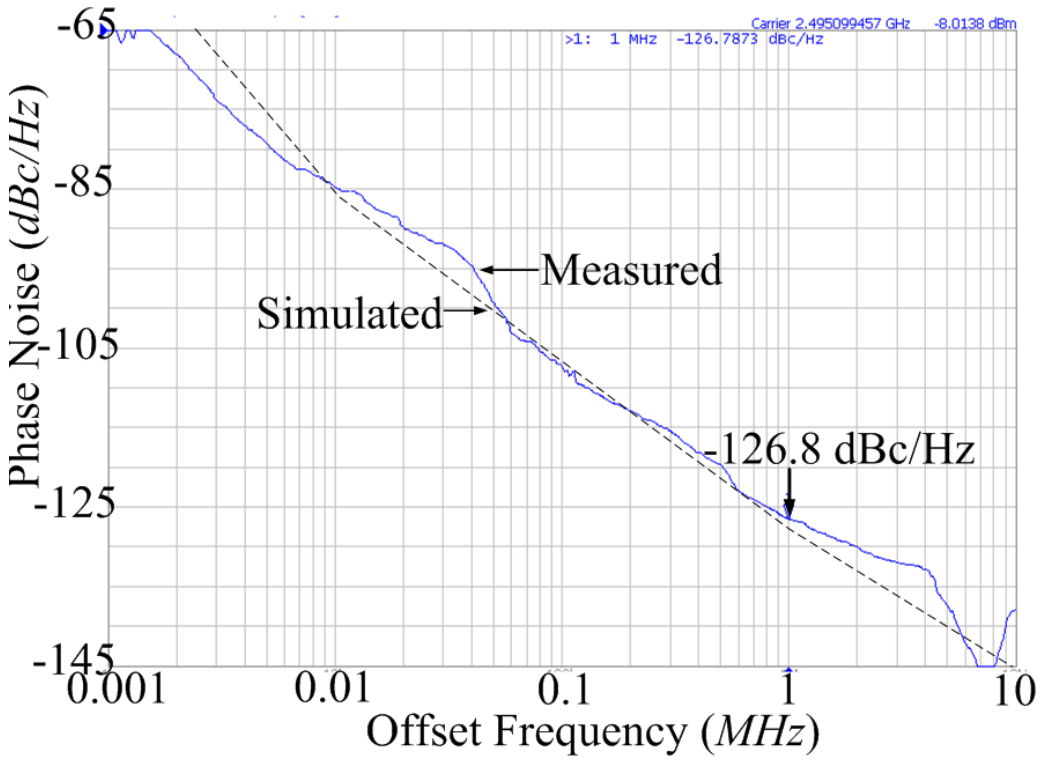


Figure 5. 27 Simulated and measured phase noise of Design C at 2.5 GHz

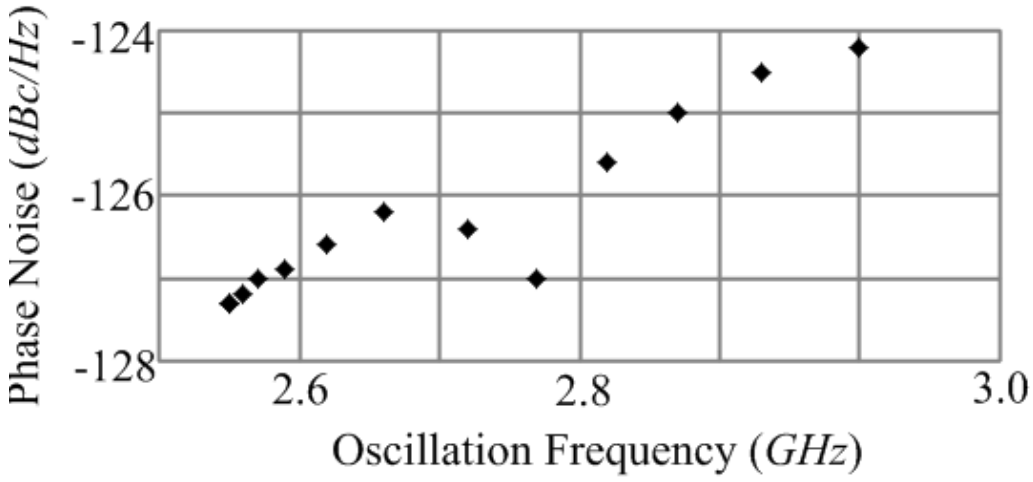


Figure 5. 28 Post-layout simulated phase noise of Design C versus different frequency.

5.4 Summary

In this chapter, a novel in-phase coupling scheme for quadrature signal generation is proposed. The principle of the proposed in-phase coupling scheme is analyzed first based on the drain current of the modern transistor and the generalized equation for multiple injections introduced in [71]. Based on this analysis, impacts of various types of mismatch are discussed individually and quantitative analysis for phase error is performed. A novel IPC QVCO (Design A) has been designed in 0.18 μm CMOS technology. The tuning range of Design A is from 2.55 GHz to 2.91 GHz and the power consumption is 4.3 mW with a 1.8 V power supply. At 2.55 GHz, measured phase noise at 1 MHz offset frequency is -122.13 dBc/Hz with a phase error of 0.1°. FoM is calculated to be 184 dBc.

On the other hand, according to the quantitative analysis for phase error performed, two novel schemes for phase error tuning are proposed. The first one is based on conventional differential Complementary VCO (Design B) and

the second one is based on Class-C type LC VCO (Design C). Both have been designed in 0.18 μm CMOS technology.

Post-layout simulation result shows the tuning range of Design B is from 2.56 GHz to 2.92 GHz and the power consumption is 4.1 mW with a 1.8 V power supply. At 2.56 GHz, simulated phase noise at 1 MHz offset frequency is -123.0 dBc/Hz. Simulated phase error is 0.6° and the phase error tuning range is ±11 º. FoM is calculated to be 185 dBc.

Measured result for Design C shows the tuning range is from 2.5 GHz to 2.97 GHz. At 2.623 GHz, with 3.6 mW power consumption from a 1.2 V power supply, the phase noise at 1 MHz offset achieves -126.8 dBc/Hz. Measured phase error is 0.5 º and the phase error tuning range is ± 17 º. It is noteworthy that the phase error tuning range of Design C is larger than that of Design B, as explained in Section 5.3.1. FoM is calculated to be 190 dBc.

The IPC QVCOs proposed in this chapter (Design A, B and C) are compared with other published works in Table 5.1. In Table 5.1 “Type” stands for coupling scheme where SHC stands for Super-Harmonic-Coupled and BGC stands for back-gate-coupled. On the other hand, TR stands for Tuning Range. In addition, as most papers report only the maximum phase error at one frequency for a few samples, the same approach is also adopted here for comparison purpose unless otherwise stated. Design A and Design B are both based on conventional Complementary LC VCO while Design C is based on Class-C VCO. As mentioned in Chapter 2, Class-C VCO topology produces higher amplitude with the same current consumption, hence Design C is expected to have a better FoM while Design A and B have a similar FoM, as shown in the table. On the other hand, phase error of Design A, B and C are

among the lowest. Note that the simulated phase error is not equal to that of measurement result. For instance, post-layout simulation result of Design A shows a phase error of 0.5 ºwhile the measured phase error is only 0.1 º. This is due to unaccountable parameter variation during fabrication that compensates part of parasitic mismatches between I/Q branch predicted by the post-layout simulation.

Table 5.1: The performance comparison of the QVCOs

	Tech (μm)	Type	f_0 (GHz)	TR (%)	V_{dd} (V)	Power (mW)	Phase noise (dBc /Hz)	Phase Error (°)	FoM (dBc)
[7]	0.18	SHC	9.3	6.5	1.8	9	-121@ 3 MHz	8***	182
[70]	0.18	BGC	5	17.5	1	2.5	-114@ 1 MHz	5	185
[72]	0.13	IPC	5	14	1	4.2	-121@ 1 MHz	<0.6	189
[74]	0.065	IPC	63	16.6	1.2	11.4	-95@ 1 MHz	<0.7	180
[82]	0.18	SQVCO	0.49	19	1.5	0.75	-118@ 1 MHz	0.3	173
[83]	0.18*	BGC	6.4	3.8	1	3.2	-114@ 1 MHz	N/A	185
Design A	0.18	IPC	2.7	13.3	1.8	4.3	-122@ 1 MHz	0.1	184
Design B**	0.18	IPC	2.7	13.3	1.8	4.1	-123@ 1 MHz	0.6	185
Design C	0.18	IPC	2.7	15.6	1.2	3.6	-127@ 1 MHz	0.5	190

$$\text{FoM} = -\mathcal{L}\{\Delta\omega\} + 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log(Power_{mW})$$

*: BiCMOS

**: Post-layout simulation result

***: Average value over the tuning range

It also worth noting that among the various QVCO compared here, only [7]

realized phase error tuning and the measured phase error tuning range is $\pm 11^{o}$ with 3 V tuning voltage while the frequency shift data is not available.

CHAPTER 6

Conclusions and Future Works

6.1 Conclusions

This thesis describes some tuning methods for differential and quadrature VCO to optimize the overall performance for LO signal generation. The investigation covers mainly amplitude calibration and phase error tuning scheme. The proposed phase error tuning scheme is based on the novel IPC QVCO proposed in this thesis.

In Chapter 2, an overview of basic concepts of VCO is provided. Both the principle and the topology of LC VCO are studied. The performances of the LC VCO, such as phase noise and amplitude variation, are then discussed. Subsequently, several approaches to improve the performance of the LC VCO are reviewed. AAC loop that calibrates the VCO's output amplitude automatically are introduced. The two major conventional AAC types, namely the analog type AAC and the digital type AAC, are discussed. Both their advantages and disadvantages are reviewed.

In Chapter 3, the fundamental of the quadrature signal is introduced. Advantages and disadvantages of different quadrature signal generation methods are studied and then two approaches are focused on, namely the polyphase filter and QVCO. A novel derivation for the transfer function of the 1^{st} order and higher order polyphase filter based on basic Kirchhoff's law is presented. Based on this transfer function, condition for quadrature signal generation is thus determined. Furthermore, phase/amplitude error due to

mismatch between elements are analyzed according to the transfer function derived and verified by simulation. On the other hand, QVCO circuit for quadrature signal generation is also studied in detail. Different coupling methods for QVCO are reviewed with their advantages and disadvantages. Based on these analyses, phase tuning schemes for different I/Q signal generation methods are discussed.

In Chapter 4, a fully integrated hybrid type AAC VCO targeted for ISM band application has been designed and fabricated in 0.18 μm CMOS technology. The operation of the whole loop and the state-dependent nature is analyzed, followed by the analysis of important blocks. Based on this analysis, a quantitative transient analysis for the whole loop is performed. A systematic design procedure is proposed according to the relationship explored in the quantitative transient analysis. The proposed AAC VCO is implemented and the measurement results are shown in Table 6.1.

Table 6.1: The performance of the proposed AAC VCO

Tech (μm)	f_0 (GHz)	TR (%)	V_{dd} (V)	Power (mW)	Phase noise (dBc/Hz)	FoM (dBc)
0.18	2.4	13	1.8	4.5	-97@10 kHz	189

$$\text{FoM} = -\mathcal{L}\{\Delta\omega\} + 20 \cdot \log\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log(Power_{mW})$$

*0.8 mW consumed by the calibration circuit.

In Chapter 5, a novel In-Phase Coupling scheme for quadrature signal generation is proposed. The principle of the in-phase coupling scheme is analyzed first, followed by the analysis for possible sources of phase error. The proposed coupling circuitry consumes less than 2% of the total power consumed by the QVCO. The proposed IPC QVCO (Design A) is fabricated in

0.18 μm CMOS technology. Based on the analysis for possible sources of phase error mentioned above, two novel schemes for phase error tuning are proposed. The first one is based on conventional differential Complementary VCO (Design B) and the second one is based on Class-C type LC VCO (Design C). Both have been designed in 0.18 μm CMOS technology. Measurement and post-layout simulation results of Design A, B and C are shown in Table 6.2

Table 6.2: The performance of the proposed QVCOs

	Design A	Design B*	Design C
Tech (μm)	0.18	0.18	0.18
f_0 (GHz)	2.7	2.7	2.7
Turning Range (%)	13.3	13.3	15.6
V_{dd} (V)	1.8	1.8	1.2
Power (mW)	4.3	4.1	3.6
Phase noise (dBc /Hz)	122@1 MHz	123@1 MHz	127@1 MHz
Phase Error (°)	0.1	0.6	0.5
Phase Error Tuning Range (°)	N.A.	11	17
FoM (dBc)	184	185	190

* : Post-layout simulation result

6.2 Future Works

Based on previous works, there are three considerations for the amplitude and phase tunable VCO in my future works, namely high performance VCO, automatic phase error calibrated QVCO and PLL with automatic calibrated VCO. They will be described separately below.

Firstly, high performance VCO is still challenging in modern RF design. In the transceiver for high data rate application, the more complex modulation requires higher VCO's phase noise requirement. Hence it is necessary to design VCO/QVCO with low phase noise. On the other hand, portability becomes an essential feature of the electronic systems that emphasize the efficient use of energy as a major design objective. This requires new VCO topology. For differential VCO, one possible solution is to adopt Class-D technique [84]. With Class-D operation, power efficiency is further improved compare with Class-C VCO, thus power consumption for a desired phase noise level can be reduced. For QVCO, in addition to new VCO core topology, new coupling scheme is another possible approach to improve the performance, in terms of power consumption, phase noise and phase error. It is worth noting such new VCO topology/coupling scheme may require new tuning scheme to optimize the VCO's performance over the operation frequency.

Secondly, automatic phase error calibrated QVCO is the next target needed to be achieved. As discussed in Chapter 3, phase error tuning schemes proposed so far are all valid for manually tuning only. In modern transceiver design, the more complex modulation schemes require higher phase accuracy. On the other hand, there is a clear trend towards full integration of the RF front-end on a single die for low cost and low power consumption. As a result, automatic phase error tuning scheme is a potential area to be explored. Compared with the manually phase error tuning scheme proposed so far, an indispensable block required by the automatic phase error tuning scheme is the Phase Error Detector (PED), whose function is to sense the phase error and convert it into some form of signal that can be processed by the following blocks. Theoretically, suppose

the I/Q signal can be expressed as $V_I = A \cdot sin(\omega t)$ and $V_Q = A \cdot cos(\omega t + \varphi)$ respectively where A is the amplitude, ω is the angular frequency and φ is the phase error, then the amplitude of $V_I + V_Q$ is equal to $A \cdot \sqrt{2 - 2sin\varphi}$. As a result, phase error can be sensed by the amplitude. However, such approach has two limitations. Firstly, for small value of φ, variation of $\sqrt{2 - 2sin\varphi}$ is also small, hence it requires a Peak Detector with high and constant gain (as defined in Chapter 4), which is difficult for GHz operation. Secondly, it is very sensitive to amplitude mismatch between I/Q signal. When there is amplitude mismatch, the result amplitude of $V_I + V_Q$ is complicated and depends on the phase error and both amplitude of the I/Q signal. Hence it is difficult to derive phase error information from the amplitude of $V_I + V_Q$. On the other hand, phase detector commonly used in circuits such as PLL, clock-and-data recovery, delay-locked loops can be employed as the PED. For such phase detector the output is proportional to the phase different of the two inputs, which is $\frac{\pi}{2} + \varphi$. However, for the phase detector used in circuits such as phase-locked loops, clock-and-data recovery and delay-locked loops, the input frequency is usually at MHz frequency range, which is much lower than the GHz frequency range required by the PED discussed here. In general, such PED works at high frequency is still a major challenge in automatic phase error calibrated QVCO design.

Finally, automatically calibrated VCO should be integrated in the PLL. This requires proper arrangement between frequency calibration and amplitude (for differential VCO) or phase error calibration (for QVCO) hence the two calibration processes do not interfere with each other. A simple approach is to

separate the two calibration processes and to run one calibration at a time. This requires proper design for indication of successful calibration and switch between the calibration processes. In addition, to ensure the PLL can achieve locked state, it is essential the frequency shift introduced by amplitude or phase error calibration should be properly designed such that it can be tracked by the PLL.

Appendix

Condition for the Magnitude of Equation (3.16) To Be Unity

According to equation (3.16), $\left|\frac{Q_{out2}}{I_{out2}}\right| = \left|\frac{(b+d)}{1-b\cdot d}\right|$. Hence if $\left|\frac{Q_{out2}}{I_{out2}}\right| = 1$, then $\left|\frac{(b+d)}{1-b\cdot d}\right| = 1$. As both b and d are real numbers, this means $\frac{(b+d)}{1-b\cdot d} = \pm 1$.

For $\frac{(b+d)}{1-b\cdot d} = 1$, it can be deduced as:

$$b + d = 1 - b \cdot d \tag{A1}$$

Hence

$$b = \frac{1-d}{1+d} \tag{A2}$$

It is worth noting equation (A2) indicates when $b = \pm 1$, $d = 0$ or not valid. As $d = \frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}$, it can be equal to 0 only when $\omega = 0$. Hence it can be concluded for $\frac{(b+d)}{1-b\cdot d} = 1$, b cannot be equal to ± 1.

As $d = \frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}$, equation (A2) can be rewritten as :

$$b = \frac{1-d}{1+d} = \frac{1-\frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}}{1+\frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}}$$

$$= \frac{1-\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2+\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2+\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)} \tag{A3}$$

Equation (A3) can be re-arranged as:

$$(b+1)\cdot\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2 + (b-1)\cdot\omega\cdot(R_1\cdot C_1 + R_2\cdot C_2)$$

$$+(b-1) = 0 \tag{A4}$$

The solution of equation (A4) is:

$$\omega_{1,2} = \frac{(1-b)\cdot(R_1\cdot C_1+R_2\cdot C_2)\pm\sqrt{\Delta}}{2(b+1)\cdot R_1\cdot R_2\cdot C_1\cdot C_2} \quad \text{(A5)}$$

Where $\Delta = b^2\cdot R_1^2\cdot C_1^2 - 2b^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2 + b^2\cdot R_2^2\cdot C_2^2$

$$-2b\cdot R_1^2\cdot C_1^2 - 4b\cdot R_1\cdot R_2\cdot C_1\cdot C_2 - 2b\cdot R_2^2\cdot C_2^2$$

$$+R_1^2\cdot C_1^2 - 6R_1\cdot R_2\cdot C_1\cdot C_2 + R_2^2\cdot C_2^2 \quad \text{(A6)}$$

However, Δ can be negative under certain condition. For instance, if $R_1\cdot C_1 = R_2\cdot C_2 = D$, it can be shown Δ can be simplified as:

$$\Delta = 4\cdot(b-1)^2\cdot D^2 - 4(b^2-1)\cdot D^2 \quad \text{(A7)}$$

Hence in this case Δ is negative when $(b-1)^2 < b^2 - 1$, which is equivalent to $b > 0.5$. When Δ is negative there is no real solution for ω in case $\frac{(b+d)}{1-b\cdot d} = 1$.

Furthermore, even $\Delta \geq 0$, both solutions of ω are negative when $b > 1$ or $b < -1$. When $-1 < b < 1$ one of the solutions for ω is negative. It is noteworthy a negative solution for ω is not valid.

For $\frac{(b+d)}{1-b\cdot d} = -1$, it can be deduced as:

$$b + d = b\cdot d - 1 \quad \text{(A8)}$$

Hence

$$b = \frac{d+1}{d-1} \quad \text{(A9)}$$

It is worth noting equation (A9) indicates when $b = \pm 1$, $d = 0$ or not valid. As $d = \frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}$, it can be equal to 0 only when $\omega = 0$. Hence it can be concluded for $\frac{(b+d)}{1-b\cdot d} = -1$, b cannot be equal to ± 1.

As $d = \frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}$, equation (A9) can be rewritten as :

$$b = \frac{d+1}{d-1} = \frac{\frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}+1}{\frac{\omega\cdot(R_1\cdot C_1+R_2\cdot C_2)}{1+\omega^2\cdot R_1\cdot R_2\cdot C_1\cdot C_2}-1}$$

$$= \frac{1+\omega^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + \omega \cdot (R_1 \cdot C_1 + R_2 \cdot C_2)}{\omega \cdot (R_1 \cdot C_1 + R_2 \cdot C_2) - 1 - \cdot \omega^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2} \quad \text{(A10)}$$

Equation (A10) can be re-arranged as:

$$(b+1) \cdot \omega^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + (1-b) \cdot \omega \cdot (R_1 \cdot C_1 + R_2 \cdot C_2)$$

$$+(b+1) = 0 \quad \text{(A11)}$$

The solution of equation (A11) is:

$$\omega_{3,4} = \frac{(b-1) \cdot (R_1 \cdot C_1 + R_2 \cdot C_2) \pm \sqrt{\Delta'}}{2(b+1) \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2} \quad \text{(A12)}$$

Where $\Delta' = b^2 \cdot R_1^2 \cdot C_1^2 - 2b^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + b^2 \cdot R_2^2 \cdot C_2^2$

$$-2b \cdot R_1^2 \cdot C_1^2 - 12b \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 - 2b \cdot R_2^2 \cdot C_2^2$$

$$+R_1^2 \cdot C_1^2 - 2R_1 \cdot R_2 \cdot C_1 \cdot C_2 + R_2^2 \cdot C_2^2 \quad \text{(A13)}$$

However, Δ' can be negative under certain condition. For instance, if $R_1 \cdot C_1 = R_2 \cdot C_2 = D$, it can be shown Δ' can be simplified as:

$$\Delta' = 4 \cdot (b-1)^2 \cdot D^2 - 4 \cdot (b+1)^2 \cdot D^2 \quad \text{(A14)}$$

Hence in this case Δ' is negative when $(b-1)^2 < (b+1)^2$, which is equivalent to $b > 0$. When Δ is negative there is no real solution for ω in case $\frac{(b+d)}{1-b \cdot d} = -1$.

Furthermore, even $\Delta \geq 0$, both solutions of ω are negative when $-1 < b < 1$. It is worth noting a negative solution for ω is not valid.

Author's Publications

Journal publications:

J1. **Y. X. Zhang** and C. C. Boon, "An In-Phase-Coupled Class-C Quadrature VCO with Tuneable Phase Error," *IEEE Microwave and Wireless Components Letters.* vol.24, pp. 796-798, Nov. 2014.

J2. **Y. X. Zhang**, C. C. Boon, K. S. Yeo, "Design And Analysis Of A 2.4 GHz Hybrid Type Automatic Amplitude Control VCO With Forward Noise Reduction," *Journal of Circuits, Systems and Computers* v. 23, no. 4, Apr. 2014.

J3. Y. N. Miao, C. C. Boon, M. A. Do, K. S. Yeo and **Y. X. Zhang**, "Low-power 2.4/5.15 GHz Dual-band Voltage-Controlled Oscillator," *Microwave and Optical Technology Letters*, v. 53, no. 11, p 2495-7, Nov. 2011

J4. Y. N. Miao, C. C. Boon, M. A. Do, K. S. Yeo and **Y. X. Zhang**, "High-Frequency Low-Power LC Divide-by-2/3 Injection-locked Frequency Divider," *Microwave and Optical Technology Letters,* v. 53, no. 2, pp. 337-340, Feb. 2011.

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C1. **Y. X. Zhang**, C. C. Boon, Y. N. Miao, K. S. Yeo and M. A. Do, "Novel Hybrid Type Automatic Amplitude Control Loop VCO," IEEE ICECC2011, Sept. 2011.

C2. Y. N. Miao, C. C. Boon, M. A. Do, K. S. Yeo and **Y. X. Zhang**, "A Low-Power 24-GHz Frequency Synthesizer for Automotive Radar Application," IEEE the 3rd ICIME, May. 2011.

C3. Y. N. Miao, C. C. Boon, K. S. Yeo, M. A. Do and **Y. X. Zhang**, "A Stacking Voltage-Controlled Oscillator and Injection-Locked Frequency Divider for Low-Power and 12-GHz Operation," IEEE ICECC2011, Sept. 2011..

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