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**STUDIES OF TRAPS IN AlGaN/GaN HIGH ELECTRON
MOBILITY TRANSISTORS ON SILICON**

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**STUDIES OF TRAPS IN AlGa_N/Ga_N HIGH ELECTRON
MOBILITY TRANSISTORS ON SILICON**

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To
My parents
M. Jesudas
N.C. Rosaline Mary

My wife
Subikshaa

My uncle
P. A. George

My good friend
Zubair Ahmed

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ABSTRACT

AlGaN/GaN-based high-electron-mobility transistors (HEMTs) are promising for high-voltage, high-frequency and high-power applications such as DC-DC convertors, cellular base stations, radar and wireless communication systems. The impressive intrinsic material parameters such as large bandgap, high saturation velocity and high critical electric field favours their operation under extreme conditions. Also, the ability to form a 2-dimensional electron gas channel at the AlGaN/GaN heterojunction interface leads to a remarkably high carrier mobility making GaN HEMTs a very fast and versatile device. In spite of these advantages, GaN HEMT technology still faces various reliability issues. One such major reliability issue that is detrimental to the device operation is the electron trapping phenomenon. Trapping of electrons in these devices leads to current dispersion or current collapse or increase of dynamic ON-resistance ($R_{DS[ON]}$) when the devices are operating at high voltages. These traps are found on the surface of the HEMT structure or distributed within AlGaN barrier or GaN buffer regions. Though significant progress has been achieved in the growth and fabrication technology, the occurrence of traps in GaN HEMTs still persist. Various reports suggest that traps could also be created when the devices are operated at high temperature and high voltage conditions over a long period of time. For realizing a reliable AlGaN/GaN HEMT technology, it is necessary to have a systematic understanding of trapping effects in GaN HEMTs.

In this thesis, a comprehensive trap analysis pertaining to the trapping mechanisms present in the AlGa_N barrier and Ga_N buffer of an AlGa_N/Ga_N HEMT on Si substrate has been carried out. Using pulsed I_D - V_D characterization under different pulse-widths and quiescent bias conditions, we have investigated the current collapse caused by the electron capture/emission phenomena. By treating the current dispersion in the linear and the saturation regions of the pulsed I_D - V_D characteristics as two distinct events, we have succeeded in explaining the electric field influence on $\text{dyn-}R_{DS[\text{ON}]}$ and V_{th} by electron trapping analysis.

Using different ON-state and OFF-state stress conditions as filling pulses, we have also investigated the trapping phenomenon in the AlGa_N barrier and Ga_N buffer layers of the AlGa_N/Ga_N HEMTs. The OFF-state stress condition that favours the tunnelling of gate electrons into the AlGa_N barrier was used to study the trapping phenomenon in the barrier layer of AlGa_N/Ga_N HEMTs. The actual location of the electron trapping was also identified by varying the electric field in the gate-drain region of AlGa_N/Ga_N HEMTs. Through the ON-state stress based studies, we have realized the presence of a distribution of trap energy levels in the Ga_N buffer layer. Moreover, the linear dependency of effective trap activation energies with applied stress voltage has also been identified. The trap properties such as activation energies, emission time constants and the capture cross-sections have been obtained by temperature dependent transient measurements. With the help of applied stress conditions and the obtained trap information, we have succeeded in identifying the actual location of the traps in AlGa_N/Ga_N HEMTs. By incorporating all the experimentally obtained trap information

into 2D numerical simulations, we have also validated our experimental findings. A multi-trap energy level model was adopted to account for the study of the distribution of trap energy levels in the GaN buffer layer.

In order to further improve the GaN HEMT device reliability, we have introduced a dielectric gate stack under the gate of AlGaN HEMTs and device encapsulation with benzo-cyclobutane (BCB). Using a bilayer gate dielectric insulation, we have suppressed the current collapse by $\sim 55\%$ and also reduced the gate leakage currents by at least an order of magnitude. Surface leakage current that prevailed due to the surface passivation layer was reduced by at least two orders of magnitude by the BCB encapsulation. Subsequently, we have enhanced the device breakdown voltage by at least two times as compared to the non BCB encapsulated HEMTs.

In summary, trapping related reliability issue still remains as a major obstacle for AlGaN/GaN HEMTs on silicon substrates, thus preventing them from being more widely adopted in applications particularly under more extreme operating conditions such as high-voltage and high-temperature. In this thesis, detailed experimental and theoretical studies of the origins and trapping mechanisms of traps in AlGaN/GaN HEMTs on silicon substrates are reported. The findings in this work provide new insight of traps in AlGaN/GaN HEMTs and will facilitate the optimisation of growth and fabrication process to enhance the device performance and reliability.

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Chapter 1

Introduction

1.1 GaN HEMT Technology – An Overview

In order to meet the commercial and military demand for robust and efficient power and communication systems that can operate at high-power, high-frequency and high-temperature, device engineers and researchers have proposed various competing device technologies. Semiconductor technologies such as Silicon (Si) transistors, Gallium Arsenide (GaAs) based high-electron-mobility transistors (HEMT), heterostructure bipolar transistors (HBT), Silicon Germanium (SiGe) HBTs and Silicon Carbide (SiC) based metal semiconductor field effect transistors (MESFETs) have been firmly established in these areas. Particularly, in the area of power electronics, Si based metal-oxide-semiconductor field effect transistors (MOSFET), gate turn-off thyristors (GTO) and insulated gate bipolar transistors (IGBT) have been dominant.

However, silicon technology is fast approaching its theoretical limits imposed by the intrinsic material properties such as low saturation velocity, low breakdown voltage, low inversion layer mobility and high device resistance [1]. GaAs suffers disadvantages such as high substrate costs, low thermal conductivity, lower critical electric field and scalability. Though GaAs is an ideal choice for ultra-high frequency applications owing to its high carrier mobility, its lower thermal conductivity and low critical electric

field makes it unsuitable for high-power applications. On the contrary, wide bandgap semiconductors such as SiC and GaN have material properties inherently superior to Si and GaAs making **them** more suitable for high-frequency and high-power switching applications. The important material properties of Si, GaAs, 4H-SiC and GaN are given in Table 1.1. The high critical field of both GaN and SiC is a property which allows these devices to operate at higher voltages and lower leakage currents. The electron mobility of GaN is higher than SiC, ultimately defining GaN as a good choice for very high-frequency and high-power switching device applications.

Table 1.1 *Important material properties of selected semiconductors at 300 K*

Properties	Si	GaAs	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.42	3.25	3.40
Dielectric Constant ϵ_r	11.8	12.8	9.7	9.0
Breakdown field E_{Br} (MV/cm)	0.25	0.4	3.0	3.3
Maximum saturation velocity v_{sat} ($\times 10^7$ cm/s)	1.0	2.0	2.0	3
Electron mobility μ (cm² /V.s)	1350	6000	800	1200 (Bulk) 2000 (2DEG)
Thermal conductivity χ (W/cm.K)	1.5	0.5	4.9	1.3
Melting Point K	1415	1238	2827	2791

Since the demonstration of the world's first GaN-based light emitting diode (LED) by H. Amano et al [2] in 1989, and the subsequent demonstration of high-efficiency high-brightness blue GaN based LED by S. Nakamura et al [3]

in 1991, the III-Nitride semiconductors have gained more importance, establishing itself as a vital component in the semiconductor device technology. Subsequently, in 1992, the presence of a 2-dimensional electron gas (DEG) in a metal-organic chemical-vapour deposition (MOCVD) grown AlGa_N/Ga_N heterojunction with excellent electronic properties was reported by M. Asif Khan et al [4], which formed the very basis of AlGa_N/Ga_N HEMTs. Since then, the AlGa_N/Ga_N based HEMTs have gained popularity in high-frequency and high-power electronic systems, commensurate with the huge demand for wireless telecommunication and high-power switching applications (e.g. base stations, satellite communication systems, high-voltage power switching systems for automobile applications, DC/DC converters etc.).

As shown in Fig. 1.1, the Ga_N-based devices show five superior performance attributes compared to Si- and GaAs-based devices, such as: high dielectric strength, high current density, high operating temperature, high-speed switching and low ON-resistance, thus making these devices suitable for applications that require high-speed, high-temperature and high-power handling capabilities. For example, it is now common to find Ga_N power amplifiers (PAs) that operate at a voltage much higher than a typical GaAs PA with better efficiency and delivering higher RF power density [1-5]. High-frequency Ga_N HEMT is an essential component for PAs for transmission of wireless communication systems and radar systems, which need high-output-power and high-efficiency performance. For instance, mobile base stations require high-output PA of >200 W with high-efficiency. To achieve power in the range of 200 W, a parallel configuration of multiple devices

with large device periphery is needed if conventional GaAs MESFET or Si LD-MOSFET is used. Overall, the base-station with GaAs MMIC technology will be in bigger size and heavier than the compact GaN-based MMIC technology PAs [6].

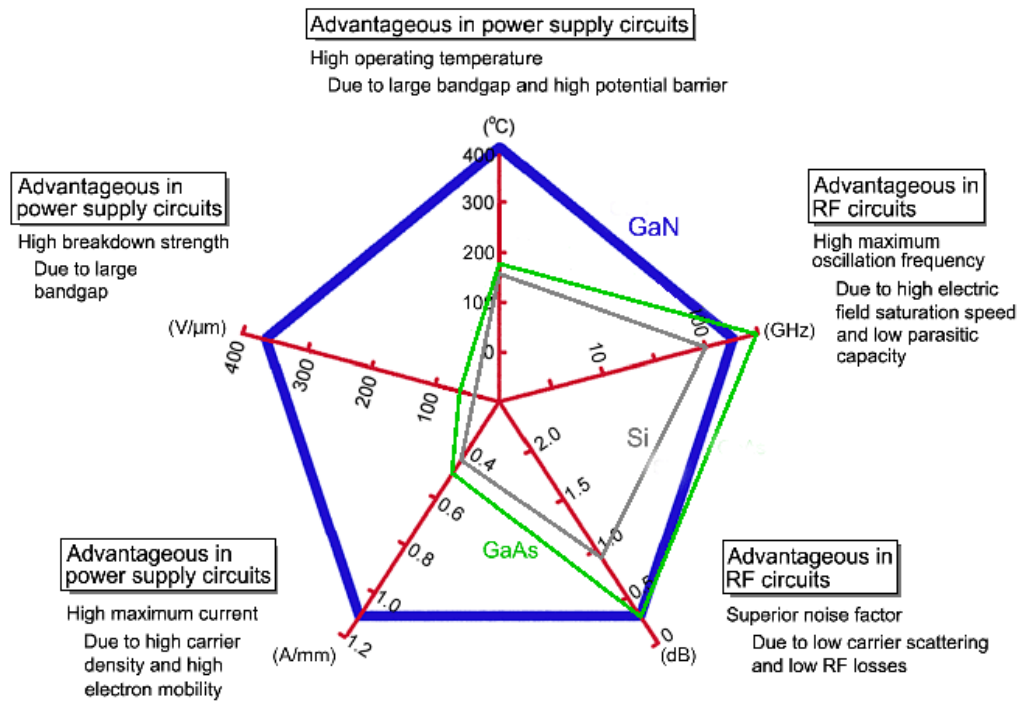


Figure 1.1 Merits of GaN material system over Si and GaAs [1]

In contrast, thanks to its high output-power performance, GaN HEMT can achieve >200W with just a single device, making high-efficiency and power-saving amplification possible.

The operation window of GaN technology with respect to power and frequency is shown in Fig. 1.2. It can be observed that the GaN based devices cover almost the whole spectrum for high-frequency and high-power technology and thus can become a good alternative to the majority of other semiconductor technologies (Si, GaAs and SiC). GaN based HEMTs have shown impressive performance in the high-power microwave regime, which

can be defined by the Johnsons figure-of-merit [$J\text{-FoM} = \text{breakdown voltage } (B V_{GD}) \times \text{cut-off frequency } (f_T)$]. The high breakdown strength of GaN leads to high $B V_{GD}$ capacity, whereas improvement of f_T could be achieved through device scaling.

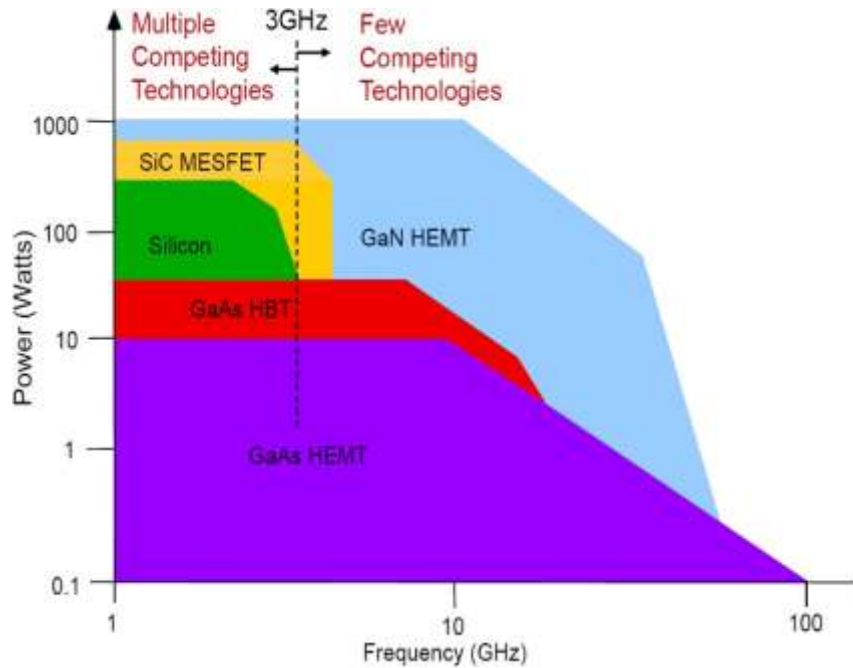


Figure 1.2 Five semiconductor technologies compete for RF power-amplifier sockets. (Graphic: courtesy RFMD) [5].

National Institute of Information and Communication Technology (NICT), Japan along with Fujitsu [7] demonstrated GaN-on-SiC HEMTs with a record high $J\text{-FoM}$ of $12.9 \text{ THz}\cdot\text{V}$ in 2009. They achieved $f_T > 118 \text{ GHz}$ and a $B V_{GD}$ of 110 V with a 60-nm gate technology. Very recently Y. Tang et al [8] with a 20-nm gated GaN-on-SiC technology achieved a $J\text{-FoM}$ of $4.5 \text{ THz}\cdot\text{V}$ with a record high f_T of 454 GHz ever to be achieved on GaN HEMTs and a $B V_{GD}$ of 10 V . With a f_T of 54 GHz and a $B V_{GD}$ of 119 V , S. Huang et al [9] in 2014 achieved $6.43 \text{ THz}\cdot\text{V}$ GaN-on-Si HEMT with a 200-nm gate technology. By reducing the gate length to 150-nm , K. Ranjan et al [10] achieved a $J\text{-FoM}$ of

8.32 THz·V for GaN-on-Si HEMT with a f_r of 63 GHz and a $B V_{GD}$ of 132 V in 2014, which still remains the state-of-the-art result for GaN-on-Si technology.

In the case of power switching applications, it is desirable to have a switching device that shows negligible resistance in the ON-state and an infinite resistance in the OFF-state condition. With regard to high-power switching applications, the two most important requirements are high $B V_{GD}$ with low specific ON-resistance ($R_{DS[ON]}$). Figure 1.3 shows the state-of-the-art $B V_{GD}$ vs $R_{DS[ON]}$ results for GaN based HEMTs, Si transistors and SiC power MOSFETs, achieved by various groups and the corresponding information is tabulated in Table 1.2.

During electric power conversion, it is required to handle high voltages, at the same time, minimizing the power losses as much as possible. With device structures such as the double-diffused metal-oxide-semiconductor (DMOS) and the U-grooved MOS, silicon based technology has long been a preferred choice for high-voltage switching applications [11].

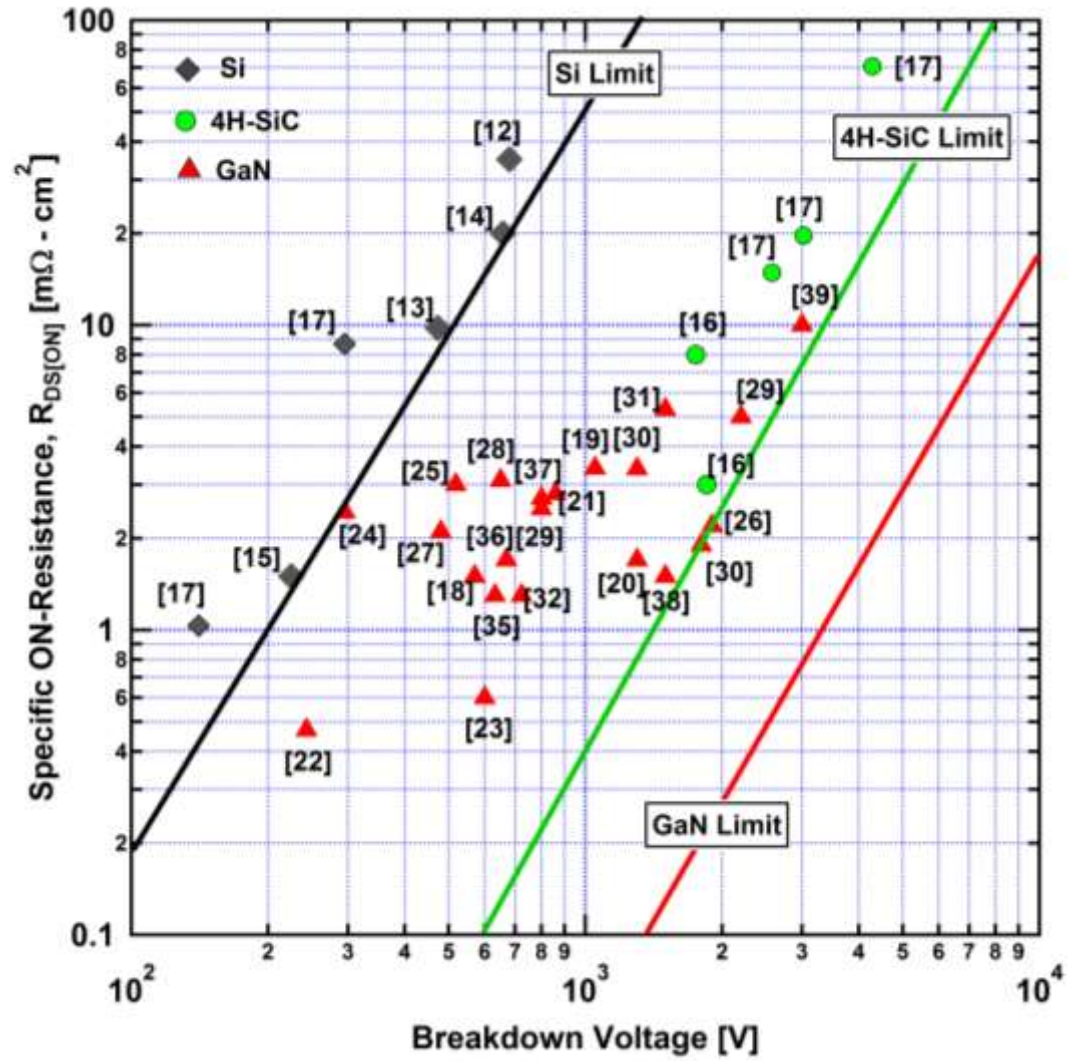


Figure 1.3 Specific on-resistance ($R_{DS(on)}$) vs breakdown voltage (BV_{GD}) of GaN based HEMTs and Si and SiC power MOSFETs.

Table 1.2 Specific ON-resistance ($R_{DS[ON]}$) and OFF-state device breakdown voltage ($B V_{GD}$) for GaN-on-Si, Si and 4H-SiC technologies.

Group	Year	Technology	$R_{DS[ON]}$ [m Ω -cm ²]	$B V_{GD}$ [V]
Infineon CoolMOS™ [12]	2000	Si MOSFET	35	680
Philips RESERF MOSFET [13]	2005	Si MOSFET	9.8	473
Fuji SJ-MOSFET [14]	2006	Si MOSFET	20	658
Denso/ToyotaSJ-MOSFET [15]	2006	Si MOSFET	1.5	225
Cree MOSFET [16]	2008	SiC MOSFET	8	1750
Semisouth VJFET [16]	2008	SiC VJFET	3	1850
Power Electronics report [17]	2008	Si, SiC and GaN – Range		
UCSB [18]	2000	GaN HEMT	1.5	570
UCSB [19]	2001	GaN HEMT	3.4	1050
UCSB [20]	2002	GaN HEMT	1.7	1300
UCSB [21]	2004	GaN HEMT	2.8	860
NTU [22]	2005	GaN HEMT	0.4	243
Toshiba [23]	2005	GaN HEMT	0.6	600
Cornell [24]	2006	GaN HEMT	2.4	295
Furukawa [25]	2006	GaN HEMT	3	518
USCB [26]	2006	GaN HEMT	2.2	1900
Toshiba [27]	2007	GaN HEMT	2.1	480
Panasonic [28]	2007	GaN HEMT	3.1	650
Sanken [29]	2007	GaN HEMT	2.5	800
Furukawa [30]	2009	GaN HEMT	3.38	1300
MIT [31]	2010	GaN HEMT	5.3	1500
NTU [32]	2011	GaN HEMT	1.3	723
IMEC [33]	2011	GaN HEMT	5	2200
MIT [34]	2012	GaN HEMT	1.9	1800
HKU [35]	2013	GaN HEMT	1.3	632
NTU [36]	2013	GaN HEMT	1.7	670
TSMC [37]	2014	GaN HEMT	1.7	800
ON Semiconductor [38]	2014	GaN HEMT	1.5	1500
IEMN [39]	2015	GaN HEMT	10	3000

However, the silicon power device performance has already reached its theoretical limits, due to the inherent material properties of Si as shown in Fig. 1.3 together with the performance limits of Si, 4H-SiC and GaN based devices. The theoretical limit of GaN is capable of delivering a higher $B V_{GD}$ with lower $R_{DS[ON]}$ beyond the material limits of Si and SiC semiconductors [17].

In 2009, Furukawa Electric co. [30] demonstrated high-power GaN HEMTs on 4-in Si substrate, with an OFF-state $B V_{GD}$ of 1.3 kV at a $R_{DS[ON]}$ of 3.38 m Ω -cm². In 2010, Bin Lu et al [31] of MIT demonstrated GaN HEMTs with an OFF-state $B V_{GD}$ of 1.5 kV and $R_{DS[ON]}$ of 5.3 m Ω -cm² using substrate-transfer technology. In 2011, S. Arulkumaran et al [32] of NTU demonstrated GaN HEMTs on 4-in high-resistive (HR) Si (111) with a $B V_{GD}$ of 723 V and $R_{DS[ON]}$ of 1.3 m Ω -cm². In 2011, IMEC [33] demonstrated GaN double-heterostructure FETs on Si (111) with an OFF-state $B V_{GD}$ of 2.2 kV and $R_{DS[ON]}$ of 5 m Ω -cm² achieved by localized substrate removal. In 2014, ON Semiconductor [38] reported an industrial process for GaN-on-Si power devices with an OFF-state $B V_{GD}$ of 1.5 kV and $R_{DS[ON]}$ of 1.5 m Ω -cm² achieved through gate insulation using in-situ Si₃N₄. Very recently, IEMN [39] demonstrated GaN-on-Si HEMTs with a record high OFF-state $B V_{GD}$ of 3.0 kV and $R_{DS[ON]}$ of 10 m Ω -cm² by applying a localized substrate removal process. As shown in Table 1.2 it is evident that the GaN based devices are capable of outperforming Si and SiC based device technology as its own theoretical limit is yet to be reached.

According to the report by Yole Développement [40], the most promising applications for the nitride semiconductors are in the information technology (IT), consumer, automotive and other industries for photovoltaic (PV) inverters, un-interrupted power supply (UPS) and motor control. Since about 67 % of the power electronics market is looking at the 0 – 900 V range devices, mostly made of cost-driven consumer and IT applications, GaN-on-Si appears as the most cost effective solution. Transphorm [41] in 2013 announced the “*Total GaN™*” family of GaN-on-Si transistors and diodes, presenting it as the world’s first JEDEC-qualified 600 V GaN device platform. GaN-based power electronics will thus be capable of being adopted in power supplies and adapters, PV inverters for solar panels, motor drives, as well as power conversion for electric vehicles [41]. Based on recent report by the Information Handling Services (IHS), the market for GaN-on-Si based power semiconductors is expected to attain a compound annual growth rate (CAGR) more than 50%, thus leading to a volume expansion for US\$15 million in 2014 to US\$800 million by 2023 [42].

1.2 Motivation of this Thesis

Given the attention and popularity of the GaN technology in the high-power applications market segment, it is imperative that it delivers **consistently** reliable performance over its complete operation lifetime. However, despite the ongoing technological advancements in the growth and fabrication of AlGaN/GaN HEMTs, various trapping based parasitic effects still exist [43]. It is only ideal to grow these III-Nitride semiconductors on native substrates. However, due to the lack of large native GaN substrates and their high costs

and other synthesis difficulties, GaN HEMTs are typically grown on foreign substrates such as sapphire (Al_2O_3), 6H-SiC and Si (111). The key properties and costs of the selected substrates for the growth of GaN are listed in the Table 1.3. The lattice-mismatch and thermal-mismatch for different substrates is calculated with respect to the GaN material.

Table 1.3 Comparison of substrate properties (thermal and lattice mismatch with respect to GaN).

<u>Substrate Properties</u>	<u>Si (111)</u>	<u>Al_2O_3 (100)</u>	<u>6H-SiC</u>	<u>GaN (0001)</u>
Lattice constant ($\text{\AA}$)	3.846	4.758	3.081	3.189
Lattice mismatch (%)	-17	-33	3.5	-
Thermal expansion coefficient (10^{-6}K^{-1})	2.6	7.3	4.5	5.6
Thermal mismatch (%)	116	-23	24	-
Thermal conductivity ($\text{W cm}^{-1} \text{K}^{-1}$)	1.5	0.5	4.5	1.3
Wafer size	2"→12"	2"→8"	2"→6"	2"
Price	Low	Medium	Very high	Extremely high

Even though sapphire and SiC substrates are already being employed for specific applications, GaN-on-Si is a very desirable choice taking into account the cost effectiveness, wafer size up to 200-mm diameter [44] and the maturity of the CMOS process line [36, 37]. However, the large lattice- and thermal-mismatch between GaN and Si leads to a large number of defects

which could affect the device performance giving rise to various reliability issues [45].

Lattice-mismatch also leads to a high-density of dislocations in the GaN epitaxial layers which lead to charge trapping and Coulomb scattering [46]. A very recent report from the Technology Qualification unit of the Boeing Network and space systems [43] shows the various degradation mechanisms in the GaN HEMT devices that jeopardizes its lifetime operation. Figure 1.4 shows three dominant degradation mechanisms such as surface pitting, hot-electron effects and electron trapping and the rate at which it degrades the performance of GaN based HEMTs over time [43].

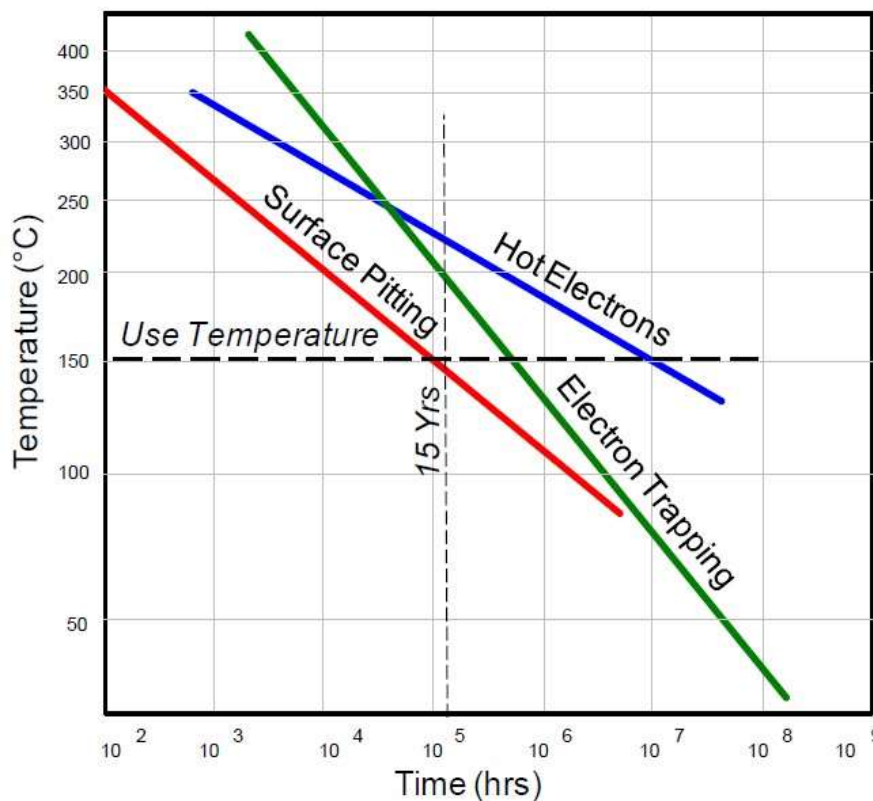


Figure 1.4 Arrhenius plots for the various degradation mechanisms in GaN HEMTs [43].

When the transistor operates as a power amplifier or as a switch, a high drain-to-source voltage is applied simultaneously with the gate bias pushing the device into the sub-threshold regime. As a result, the device characteristics become drastically different from the static characteristics for a period of time ranging from microseconds to hours. Changes in the surface morphology of electrically stressed AlGaIn/GaN HEMTs due to inverse piezoelectric effects, leading to surface pitting in the vicinity of the gate terminal has been reported by M. D. Hodge et al [47] and P. Makaram et al [48]. The hot-electron based effects which limit the output-power-density at microwave frequencies of GaN HEMTs has been reported by X. D. Wang et al [49]. A detailed analysis method for the hot-electron based effects and electron trapping effects has been given by M. Meneghini et al [50].

As shown in Fig. 1.4, device performance degradation due to electron trapping poses a major hindrance to the proposed performance range of GaN HEMTs over the complete operation lifetime. Various trapping based mechanisms have been proposed to explain the device degradation due to electron trapping. In particular, the trapping effects have been reported to exist in the GaN buffer, AlGaIn barrier and the device surface [51, 52, 53, 54, 55] as shown in Fig. 1.5.

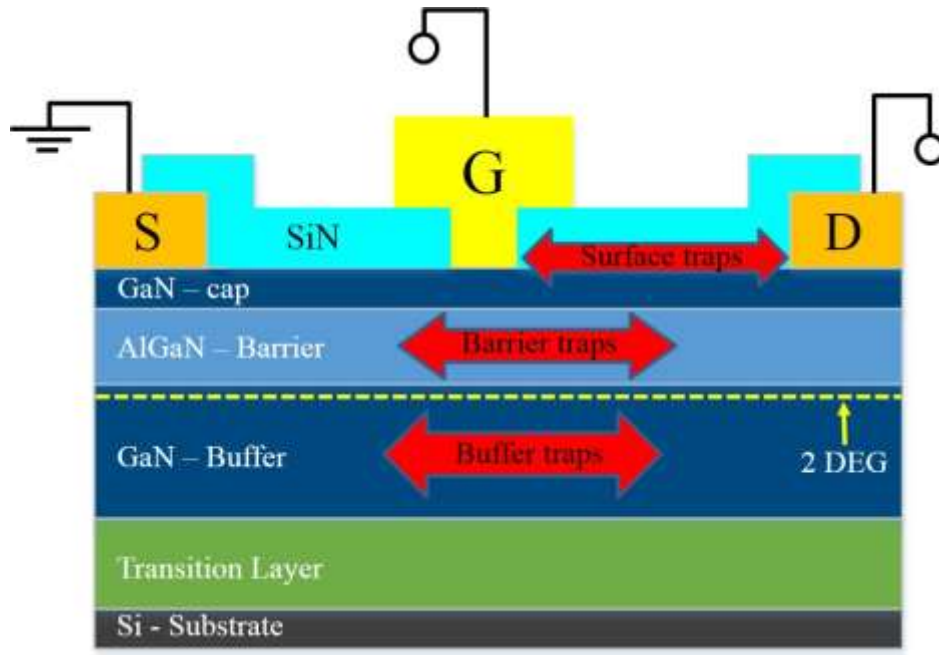


Figure 1.5 Traps in the AlGaN/GaN heterostructure.

The source of such traps are found to be either due to crystalline imperfections as a result of epitaxial growth, or due to various device fabrications processes. The trap centres can also be activated when the devices are operated at high voltages [56]. The existence of traps in the devices lead to drain current dispersion followed by the reduction of output-power at high-frequency operation [52, 53]. Similarly, electron trapping leads to the increase of dynamic- $R_{DS[ON]}$ (dyn- $R_{DS[ON]}$) under high-voltage operating conditions [55]. In the conventional planar structures, under high-voltage operations, the drain-side gate-edge experiences unprecedentedly high electric fields. Consequently, charge carriers can reach very high energies, thus triggering hot-carrier degradation phenomena such as charge trapping, defects, and/or deep-level generation. Moreover, high-voltage bias leads to increased power dissipation and thermal degradation or failure mechanisms related to the difference in thermal coefficients of the different

layers or strain due to piezoelectric effects [47, 48, 51]. Various reports on the high electric field reliability are already available in the literature [47, 48, 51, 52, 57], but a thorough conception of the underlying physical mechanisms, effect of the electric field on the different layers of the HEMT heterostructure and the critical voltage levels leading to permanent inverse piezo electric effects are still lacking [52, 57].

For the mitigation of the surface and the bulk traps which cause various trapping related issues during the operation of AlGa_N/Ga_N HEMTs, development of advanced material growth techniques, development of novel device structures and device fabrication processes have become the key research areas of the Ga_N HEMT technology. Even though remarkable improvements in growth/device fabrication technologies have been realized, the complete removal of trapping effects from the Ga_N transistors still remains a challenge. Various trap characterization techniques are currently employed for garnering a comprehensive understanding of the effects of trapping on the device performance [57]. By observing the various anomalies exhibited in the device current-voltage characteristics, the location of the traps can be determined [54, 55, 57]. Various methods such as deep-level transient spectroscopy (DLTS), gate-lag measurement, low-frequency noise measurement, and frequency-dependent transconductance (g_m) dispersion and conductance analysis, have been used in Ga_N HEMTs to study their trapping behaviour [58]. In spite of all these, a detailed understanding of the characteristics of the traps is still lacking until today.

In this thesis, we present an extensive investigation of electron trapping effects in AlGa_N/Ga_N HEMTs on Si. The influence of electric field on the location of trapping is presented for the first time [55]. Using OFF-state [55] and ON-state [54] conditions, we present a methodology of segregating the trapping effects for a more relevant analysis of trap location. We also show that during the current-transient technique of trap analysis, the obtained trap information is by virtue of the applied stress voltage, and thus the calculated activation energies are **the effective values** corresponding to the applied stress. This **has** also led to the conceptualization of the distribution of trap energy levels in the Ga_N buffer [54].

2-D numerical simulation based on Technology Computer Aided Designing (TCAD) was used for verifying the experimental observations [58]. The simulation environment was calibrated for AlGa_N/Ga_N based HEMT structure. Optimization was performed by matching the simulated and measured electrical parameters. To study the OFF-state and ON-state trapping mechanisms, Single-Trap Energy (STE) [54, 55] and Multi-Trap Energy (MTE) **models** [55] were used, respectively. A close match with the experimentally obtained trend was obtained by tuning the trapping parameters in the TCAD simulator and the results were thus verified.

We further extended our study on the gate leakage currents that prevails in Schottky gated AlGa_N/Ga_N HEMTs. By employing a bilayer gate dielectric stack consisting of Si₃N₄ (5-nm)/Al₂O₃ (5-nm), we reduced the gate leakage currents by at least one order of magnitude and also suppressed the current collapse by $\approx 60\%$. Furthermore, we show that the final device

encapsulation using benzocyclobutane (BCB) improves the device breakdown characteristics by effectively reducing the surface leakage currents.

1.3 Organization of Thesis

In **Chapter 2**, we present the background of GaN based HEMTs and MISHEMTs based on an extensive literature survey. The material properties and the merits of GaN material system which make it a front runner for high-power and high-frequency application are discussed. This chapter also covers details on the basic device operation principles and the various factors that lead to device performance degradation. We have also given an account of the different techniques that are used for studying the degradation modes.

In **Chapter 3**, we give an elaborate account on the device fabrication methods for both long ($L_G \geq 1 \mu\text{m}$) and sub-micron ($L_G < 1 \mu\text{m}$) gate-length AlGaIn/GaN HEMTs. Fabrication process flow for both conventional AlGaIn/GaN HEMTs and AlGaIn/GaN MISHEMTs are also presented.

In **Chapter 4**, we present a systematic study on the trapping effects in AlGaIn/GaN HEMTs under OFF-state stress conditions. We discuss on the influence of electric field on the location of trapping in the various layers of the heterostructure. Using pulsed current voltage characteristics performed at different pulse conditions and carefully chosen quiescent bias conditions, we have distinguished current collapse in the regions under the gate and the gate-drain access regions of GaN HEMTs. We have used temperature-

dependent current-transient technique to identify and investigate the trap properties in GaN HEMTs. Furthermore, we have also proposed a theory based on the two dimensional numerical simulations to support our experimental observations and hypothesis.

In **Chapter 5**, we have proposed a model that explains the presence of a distribution of trap energy levels in the GaN buffer layer of AlGaIn/GaN HEMTs. We have used fully ON-state stress conditions to intentionally fill the traps in the GaN buffer. Subsequently, using the temperature-dependent current-transient technique, we have studied the properties of the traps in the GaN buffer. By incorporating the obtained trap parameters into two dimensional numerical simulations, we have verified the experimental observations. In contrast to the literature that provides mostly discrete quantum energy states detected using the current-transient method, we have claimed that the obtained effective trap activation energy represents the presence of a distribution of trap energy levels in the GaN buffer.

In **Chapter 6**, we have presented the reduction of trapping effects and gate-leakage current issues by introducing dielectric layers under the gate terminal. A bilayer gate dielectric stack consisting of SiN (5 nm)/Al₂O₃ (5 nm) was used to form the MISHEMT which resulted in improved device performance by the reduction of interface states as compared to the conventional Schottky gate HEMTs.

In **Chapter 7**, a detailed investigation on the influence of a BCB encapsulation layer on the OFF-state $B V_{GD}$ characteristics is presented. The devices after BCB encapsulation exhibited enhanced $B V_{GD}$ characteristics.

We have shown that through BCB encapsulation, the surface leakage components were suppressed, thus leading to an enhancement in the device $B V_{GD}$ characteristics.

Finally in **Chapter 8**, we draw the conclusions by outlining the essential contributions of this work and also provide some recommendations for future work.

Chapter 2

AlGaN/GaN HEMTs and MISHEMTs: Operation principles and theory of trap mechanisms

Owing to the impressive intrinsic material properties of the GaN material system, the AlGaN/GaN based HEMTs and MISHEMTs have become highly sought after candidates for high-power switching and high-frequency applications. In this chapter, we elaborate on these basic material properties and the advantages of the III-Nitride material system that make them attractive for such applications. At the same time, as this technology is far from reaching its maturity, we also provide an outline on the trapping effects that limit this technology from reaching their full potential in terms of performance and reliability. Different types of trapping mechanisms that typically exist in GaN-based HEMTs and the various trap characterization methods are discussed. Finally, a brief account of the theory and understanding behind the TCAD-based 2-dimensional transient simulations used for validating the experimentally obtained results has been provided.

2.1 Advantages of III-Nitride material system

The group III-Nitrides such as GaN, aluminium nitride (AlN), aluminium gallium nitride (AlGaN), indium gallium nitride (InGaN), indium aluminium nitride (InAlN) etc., which are basically categorized as wide bandgap materials have attracted large attention from the semiconductor industry because of their potential to be used in optoelectronic devices and high-power/high-temperature and high-frequency electronic devices. Their major advantages arise from the basic physical properties of the materials such as:

- Direct bandgap → most suitable for optoelectronic applications
- Wide bandgap → most suitable for high voltage applications.

The unique combination of wide bandgap, high breakdown field and high saturated electron velocity gives GaN based material system a tremendous potential [59]. Some of the most important material properties of Si, 4H-SiC, GaAs and GaN are given in Table 1.1 of chapter 1. Since the saturated electron drift velocity of GaN is higher than that of Si, SiC and GaAs, device operations with high saturation current and high-frequency can be achieved with the GaN based devices. The relatively higher thermal conductivity of GaN compared to GaAs system makes it suitable for high-power operations. Furthermore, the radiation hardness of GaN is higher than GaAs and comparable to SiC [60] making it an attractive choice for space applications.

The GaN and its related ternary alloys come in three different crystal structures [61, 62]: (i) Wurtzite, (ii) Zinc blende and (iii) Rock salt.

Out of the three crystal structures, the wurtzite happens to be the most thermodynamically stable structure. Most of AlGaN/GaN based semiconductor technology is based on growth in the wurtzite phase. The III-Nitride compounds are covalently bonded, so each atom is tetrahedrally bonded to four atoms of the other type. The differences in the electronegativity of the Ga- and N-atoms results in an electrostatic attraction that in turn further stabilizes the crystal structure. The wurtzite structures with Gallium (Ga)-face corresponding to (0001) crystalline face and Nitrogen (N)-face corresponding to (000 $\bar{1}$) crystalline face are shown in Fig. 2.1 (a) and (b), respectively. It comprises of a hexagonal unit cell with two intercepting Hexagonal Closed Packed (HCP) sub-lattice. As shown in the Fig. 2.1, the two lattice parameters that define the Wurtzite structure are ' a_0 ', which is the edge length of the base hexagon (basal plane parameter) and ' c_0 ', which corresponds to the height of the hexagonal lattice cell (axial parameter) along the [0001] or the [000 $\bar{1}$] direction, perpendicular to the basal plane.

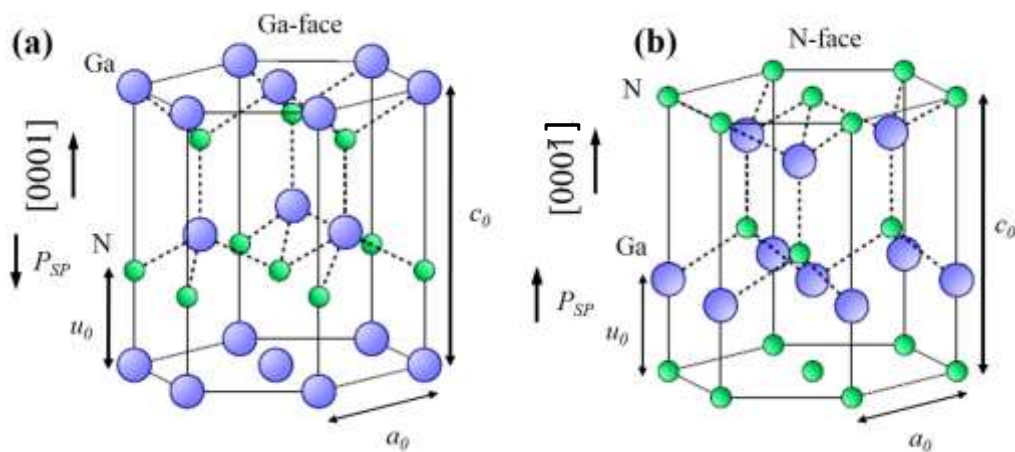


Figure 2.1 Wurtzite GaN lattice structure (a) Ga-face, and (b) N-face [63].

The interatomic distance between Ga and N located on the sites of the two HCP sub-lattices is defined by the internal parameter ' u_0 '. For an ideal wurtzite structure the ratio of the lattice parameters are $c_0/a_0 = (8/3)^{1/2} \approx 1.633$, with the internal parameter $u_0 = 3/8 = 0.375$. However, with increasing lattice non-ideality, the c_0/a_0 ratio moves away from 1.633 [63].

Additionally, there is a large difference in electronegativity between nitrogen and the Group-III elements resulting in electron charge transfer from the Group-III atom to the N atom. Thus, the bonding shows partly covalent and partly ionic characteristics. In the case of GaN, the electronegativity difference is about 1.4, which means that the ionicity of the bonding is $\approx 40\%$ [64]. This distinct ionicity leads to a microscopic polarization. In combination with the above mentioned lack of inversion symmetry, the microscopic electric dipoles result in a strong macroscopic polarization (P) of the crystal along the $[0001]$ axis. This kind of polarization, in the absence of any external influence such as strain or an applied electric field, is known as spontaneous polarization (P_{sp}). If the crystal lattice is deformed by external fields or internal forces and stresses, both lattice parameters c_0 and a_0 and the polarization strength will be changed [65]. This additional polarization is called piezoelectric polarisation (P_{pe}). Both types of polarization dramatically affect the optical and electrical properties of multi-layered Group III-Nitride heterostructures and devices.

2.2 AlGaN/GaN Heterostructure and 2DEG formation

The Group III-Nitride based heterostructure consists of two different materials, an un-intentionally doped GaN buffer layer with a narrower bandgap, above which a ternary alloy, called a barrier layer with a wider bandgap is grown. This thin $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is grown on a GaN buffer layer and is therefore under tensile strain. In this special case, both the piezoelectric and the spontaneous polarizations point in the same direction and the value of the total polarization is $P = P_{\text{PE}} + P_{\text{SP}}$. Since the values of the piezoelectric constants and spontaneous polarization increase from GaN to AlN, the total polarization of a strained (or even unstrained) $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is larger than that of a relaxed GaN buffer layer and therefore a positive polarization charge (σ^+) is present at the lower AlGaN/GaN interface for Ga-face structure [see Fig. 2.2 (a)] and at the upper GaN/AlGaN interface for the N-face structure [see Fig. 2.2 (b)].

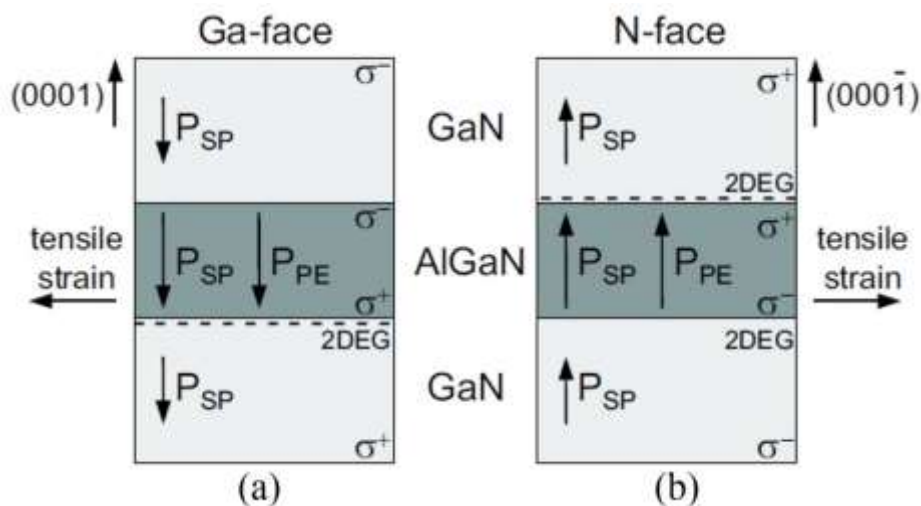


Figure 2.2 Directions of spontaneous- and piezoelectric-polarization and the polarization induced sheet charge (2DEG) in AlGaN/GaN heterostructures with (a) Ga-face and (b) N-face.

Growing AlGa_N over Ga_N results in an interface with high levels of polarization. This induces a sheet charge with a density σ in the AlGa_N material. If the sheet charge density is positive (σ^+), an accumulation of free mobile carriers (electrons in this case) occurs in order to compensate the positive charges. The accumulated charges are confined in a triangular quantum well at the AlGa_N/Ga_N interface where the conduction bands of AlGa_N and Ga_N drop below the Fermi level (E_F) due to band bending. This forms the basis for the formation of the 2DEG along the AlGa_N/Ga_N interface. These confined electrons exhibit enhanced mobility provided the interface roughness is low [66].

In analogy, a negative polarization sheet charge (σ^-) density can cause an accumulation of holes at the interface if the valence band edge of the AlGa_N/Ga_N heterostructure crosses the E_F . In fact, the spontaneous and piezoelectric polarization are large enough to produce 2DEG with high sheet electron concentration even without intentionally doping the barrier, in contrast to almost all other material (heterostructure) systems (e.g: AlGaAs/GaAs system). Since the formed 2DEG channel is well separated from the top supply layer, parasitic effects such as Coulomb scattering can be mitigated, thus resulting in a significant enhancement of mobility. In addition, since the quantum well is located in the un-intentionally doped material, impurity scattering can also be strongly reduced leading to an enhancement in the carrier mobility. The enhanced electron mobility in the 2DEG channel is the key feature of HEMTs.

2.3 Principles of HEMTs

The main operation principle of AlGaN/GaN HEMT is by the modulation of the 2DEG formed at the heterostructure junction. The AlGaN/GaN HEMT was first demonstrated by M. Asif Khan et al [67] in 1993. The cross-sectional schematic of an AlGaN/GaN HEMT and its corresponding energy band diagram under the gate electrode is shown in Fig. 2.3. A GaN-based HEMT transistor is a three terminal device consisting of the source, gate and the drain electrodes. As discussed in the previous sections, the spontaneous and the piezoelectric polarization effects give rise to a high sheet-carrier density at the AlGaN/GaN hetero-interface. The source and the drain contacts are ohmic contacts and they are electrically connected to the highly conductive 2DEG channel which is formed by majority carriers, in this case electrons. Electrons are supplied from the source contact and flow to drain contact when a positive voltage is applied to drain contact with respect to the source contact (V_{DS}).

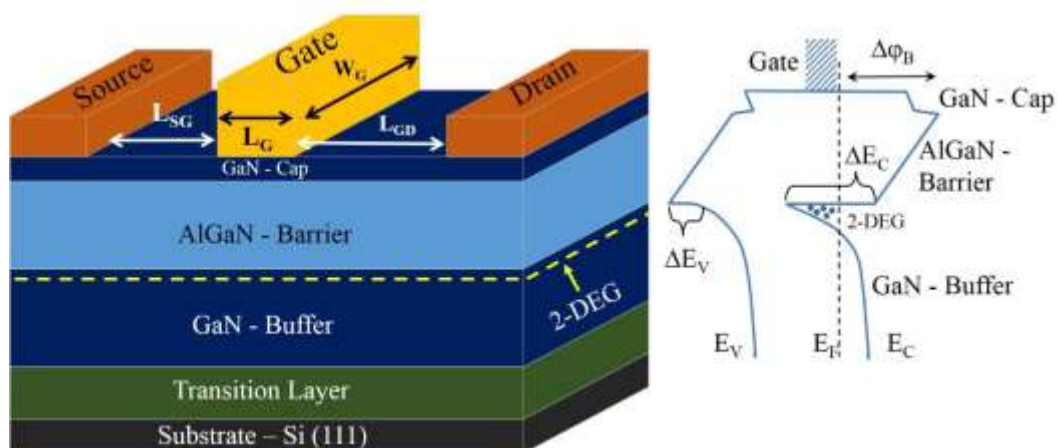


Figure 2.3 The schematic cross-section and the corresponding energy band diagram of a typical AlGaN/GaN HEMT.

The gate electrode is separated from the 2DEG channel by the AlGa_N barrier, thus forming a Schottky contact. The gate to source voltage (V_{GS}) affects the energetic position of the conduction band under the gate relative to the Fermi level. Thus, the V_{GS} controls the amount of the electrons flowing in the 2DEG channel. The AlGa_N/Ga_N HEMTs used for this study are in the depletion mode (D-mode), also known as normally-ON transistors. Thus, the 2DEG channel is present even under zero gate bias. By reverse biasing the gate electrode, the position of the conduction band is shifted relative to the Fermi Level; and when the gate voltage is lowered below the threshold voltage, the bottom of the conduction band at the AlGa_N interface does not coincide with the Fermi level any longer. Thus, the 2DEG channel will be fully depleted of carriers switching OFF the device.

2.4 AlGa_N/Ga_N Metal-Insulator-Semiconductor HEMTs (MISHEMTs)

Despite AlGa_N/Ga_N HEMTs being a strong contender in the area of high-power radio-frequency applications owing to its enhanced mobility and saturation velocity, one of the key problems degrading its performance and reliability is its relatively high Schottky-gate leakage currents [68]. High gate-leakage currents results in the device BV_{GD} reduction, power-added efficiency reduction and also increases the noise figure [68]. Various gate-leakage mechanisms have been proposed such as thermionic emission [69, 70], thermionic field emission [71, 72], trap assisted tunnelling [70, 73], dislocation assisted tunnelling [74, 75], defect hopping [73, 76], Fowler-

Nordheim tunnelling [77], Frenkel–Poole emission [78, 79] and space charged limited current [80, 81].

Under forward bias, high forward gate current attributed to thermionic emission, thermionic field emission and other trap induced mechanisms can affect the gate-channel capacitance causing an alternate leakage path for the channel electrons, thus limiting the maximum drain current. The leakage currents during the negative gate bias which is mostly a defect-state based mechanism, takes place through trap assisted tunnelling or emission. High reverse leakage currents result in a voltage drop across the gate and the drain electrodes causing a premature breakdown, thus impeding the reliability of the device.

One of the most efficient ways to suppress the Schottky-contact leakage currents which is predominantly caused by the tunnelling and the emission mechanisms is to create an additional barrier for the leakage processes. This can be achieved by introducing a gate dielectric layer at the metal-semiconductor interface. It is preferred to have a gate dielectric with a large conduction band offset in order to suppress the gate-leakage currents and also a high-dielectric constant to improve the device transconductance [82]. Schematic cross-sectional view of a typical AlGaN/GaN MISHEMT and the corresponding energy band diagram is shown in Fig 2.4. Some of the prevalently used gate dielectric materials are SiO₂ [83, 84], SiN_x [84, 85], HfO₂ [86, 87], Al₂O₃ [88, 89], AlN [90] and ZrO₂ [91]. C. J. Kirkpatrick et al [83] and T. Huang et al [85] reported a 3 to 4 orders magnitude reduction in gate-leakage currents using a 7 nm-thick SiO₂ and Al₂O₃ gate dielectric

respectively, compared to that of conventional Schottky gated GaN HEMTs. ON-semiconductor [38] has demonstrated GaN-on-Si power devices with a high BV_{GD} of 650 V achieved by gate insulation using in-situ grown Si_3N_4 dielectric layer. The devices exhibited a very low gate-leakage current of $\approx 20 \text{ nA/mm}$ even at 1.0 kV.

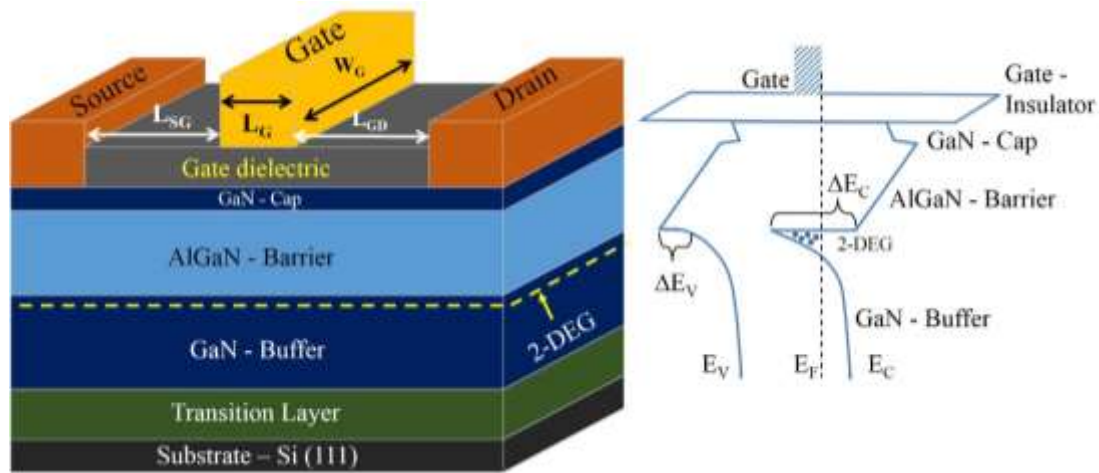


Figure 2.4 Schematic cross-section of AlGaN/GaN MISHEMT and its corresponding energy band diagram.

Researchers have also employed double or bilayer gate dielectric schemes in order to take advantage of the favourable material properties of different dielectric materials simultaneously [92, 93, 94, 95]. N.-Q. Zhang et al [92] demonstrated a high switching-speed kilo-volt GaN-on-SiC MISHEMTs using a SiO_2 (10 nm)/ Si_3N_4 (15 nm) bilayer gate dielectric scheme. Their devices exhibited an OFF-state BV_{GD} of 1.3 kV at a very low $R_{DS[ON]}$ of $1.7 \text{ m}\Omega\text{-cm}^2$. They claim that the Si_3N_4 layer deposited directly over the AlGaN barrier layer mitigated the shallow surface traps resulting in high switching speeds, whereas the SiO_2 layer deposited over the Si_3N_4 reduced gate leakage currents thus improving the breakdown characteristics of the device. N.

Maeda et al [93] demonstrated excellent radio frequency characteristics with very low gate-leakage currents using $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ bilayer gate insulated AlGaIn/GaN MISHEMTs. K. Balachandar et al [94], realized low current collapse in AlGaIn/GaN MISHEMTs with bilayer Si_3N_4 (5 nm)/ SiO_2 (10 nm) gate stack [94]. S. Yagi et al [95] employed a $\text{TiO}_2/\text{Si}_3\text{N}_4$ bilayer dielectric layer and fabricated GaN MISHEMTs that exhibited an OFF-state $B V_{\text{GD}}$ of 1.1 kV at a $R_{\text{DS[ON]}}$ of $15 \text{ m}\Omega\text{-cm}^2$. IMEC [82] demonstrated a CMOS compatible low leakage GaN-on-Si MISHEMT with a $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ bilayer gate dielectric which exhibited a $B V_{\text{GD}}$ of 750 V at a $R_{\text{DS[ON]}}$ of $2.9 \text{ m}\Omega\text{-cm}^2$. We have reported $\approx 60\%$ current collapse reduction and one order of magnitude reduction in gate-leakage currents by employing a $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ bilayer gate dielectric in our GaN MISHEMTs compared to conventional Schottky-gated HEMTs [96].

2.5 Effects of traps on HEMT performance

Though the GaN HEMT technology has achieved significant progress, various material related issues are yet to be addressed in order to prove it to be a viable and a competent technology. The actual device performance of AlGaIn/GaN HEMTs is yet to reach the proposed theoretical expectations. One of the major obstacles causing performance degradation is the trapping effects in AlGaIn/GaN HEMTs during operation, causing current dispersion between DC to RF or otherwise, DC to pulsed $I_D - V_D$ characteristics. Various kinds of trapping effects such as transconductance frequency-dispersion, light sensitivity, gate- and drain-lag transients, and restricted microwave power output have been reported [97]. Figure 2.5 illustrates the presence of traps in the surface, barrier and buffer regions of the AlGaIn/GaN

heterostructure. The different trapping mechanisms commonly encountered in AlGaN/GaN HEMTs as depicted in the Fig. 2.5 are:

- gate electron injection into the surface and barrier traps under high negative V_{GS} ,
- hot-electron injection into the barrier/buffer traps under high ON-state V_{DS} and,
- Capturing of electrons by deep levels introduced during material growth.

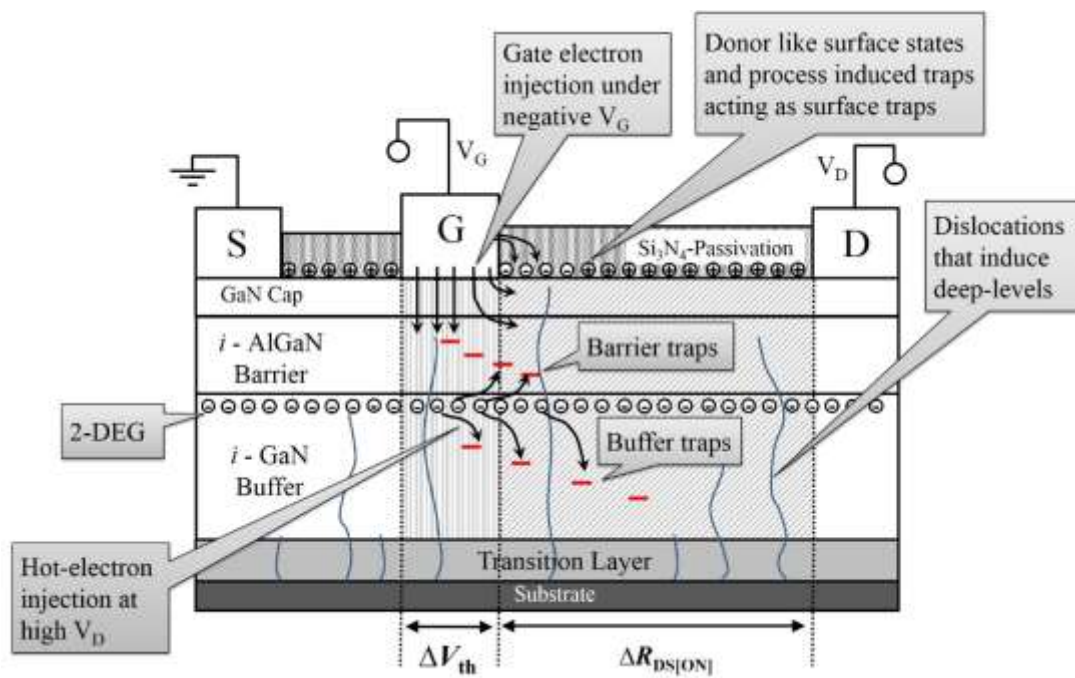


Figure 2.5 Schematic of the AlGaN/GaN heterostructure showing various trapping mechanisms and their effect on the device performance.

Trapping of electrons results in the reduction of the sheet-carrier density in the 2DEG channel in order to conserve charge neutrality and thus leads to a reduction in the drain current density. In general, this reduction in the drain current is termed as “*current collapse*”. The first paper on current collapse

in AlGaIn/GaN HFET was published by M. A. Khan et al. [98] in 1994. Current collapse is a persistent yet a recoverable phenomenon [97]. Current collapse is best characterized and analysed through pulsed $I_D - V_D$ measurements. The major parameters used in characterizing the current collapse phenomenon is the “*gate-lag*” and the “*drain-lag*” quiescent bias (Q-bias) conditions [97].

The transient response of the drain current to a gate voltage is referred to as gate-lag, and to a drain voltage is referred to as the drain-lag, while the corresponding gate or drain voltage remains constant. The $I_D - V_D$ characteristics showing the effect of current collapse on the output power of HEMT is illustrated in Fig. 2.6. The device $I_D - V_D$ characteristics before and after the current collapse phenomenon are represented by the solid and dotted lines respectively.

It can be observed that the current collapse results in the increase of the knee voltage (V_{knee}) and a decrease in the maximum current (I_{Dmax}). This in turn decreases the achievable maximum output power (P_{max}), which is given by the following expression:

$$P_{max} = \frac{(\Delta V_D \times \Delta I_D)}{8}$$

Where, ΔV_D is the maximum voltage swing which is the difference between the breakdown voltage (BV_{GD}) and the V_{knee} . ΔI_D is the maximum current swing given by I_{Dmax} . The shaded region in the Fig. 2.6 represents P_{max} , and this operation window is reduced by the current collapse phenomenon.

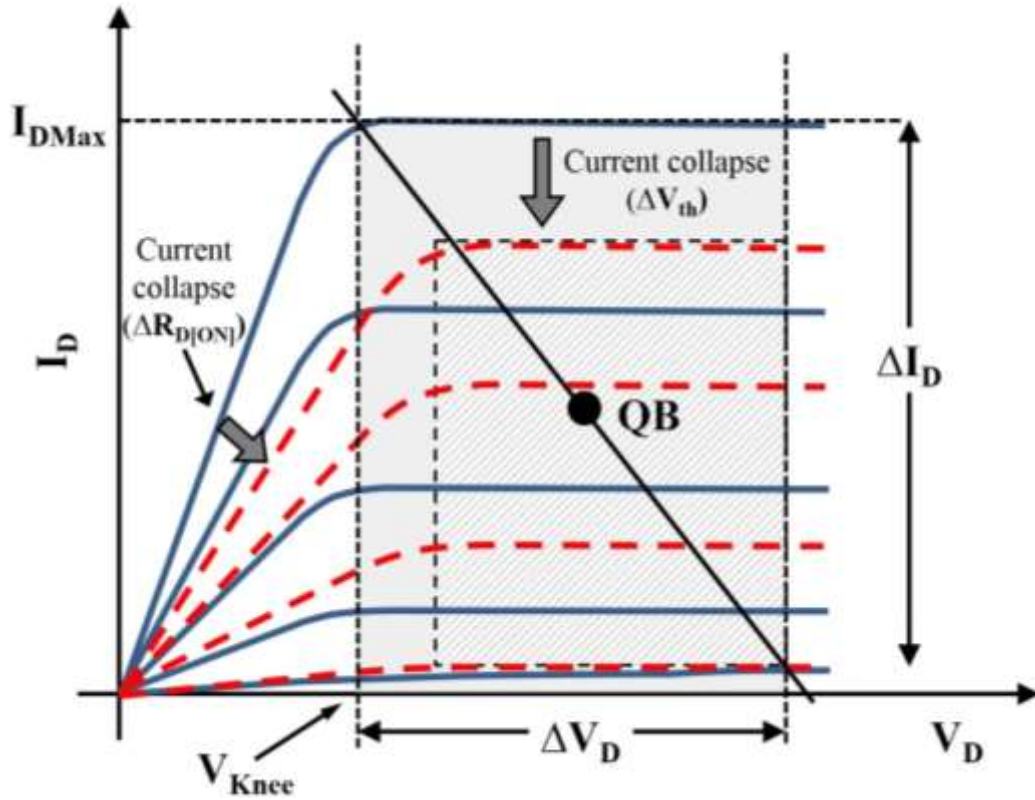


Figure 2.6 A sketch of I_D - V_D characteristics for HEMT before (solid lines) and after (graded lines) current collapse. The maximum attainable device output-power is approximately proportional to the area of the shaded and broken rectangles, before and after current collapse, respectively [93].

The removal of polarization induced positive charges from the surface or otherwise called the surface states (also see Fig. 2.5) of the heterojunction transistor, accompanied by the removal of equal number of electrons in the 2DEG is considered to be a major cause for current collapse [99]. Buffer and barrier related traps also play a significant role in current reduction at RF frequencies [98]. Electron trapping by the surface, barrier or buffer traps present in the gate drain access region (see Fig. 2.5) leads to current collapse characterized by $\text{dyn-}R_{DS[ON]}$ as shown in Fig. 2.6. Likewise, electron trapping in the regions under the gate (see Fig. 2.5) leads to current collapse

characterized by a threshold voltage shift (ΔV_{th}), resulting in a decrease of drain current in the saturation region of the device pulsed I_D-V_D characteristics as shown in Fig. 2.6. Even though the AlGaN/GaN HEMTs exhibit drain current dispersion during operation, the actual origins of the trapping mechanisms are yet to be understood. The following sections elaborate on the various trapping mechanisms that are present in AlGaN/GaN HEMTs.

2.6 Trapping Mechanism

Various studies suggest that the trapping effects in AlGaN/GaN HEMTs lead to a considerable degradation of the device performance during operation. Electrically active traps have been reported in various locations of the AlGaN/GaN heterostructure as shown in Fig. 2.5. A broad classification has been given as:

- *Surface traps* [92, 100, 101, 102] → Present on the surface of the device heterostructure
- *Bulk traps* [55], [97]–[100], [102] → present within the heterostructure, which could be in the AlGaN barrier, AlGaN/GaN interface or the GaN buffer.

The dislocations that occur by virtue of the lattice-mismatch between GaN and the substrate (non-native) are also responsible for introducing deep levels. Regardless of the location of the traps, the trapping effects have been a very intriguing field of study. Until now, mitigating the trapping effects in GaN HEMTs have been rather a challenging ordeal. In the following sections we discuss on the trapping effects in GaN HEMTs based on their location.

2.6.1 Surface Trapping Effects

The trapping of electrons on the surface of the AlGa_N barrier in GaN HEMTs is widely characterized as surface trapping effects. The presence of traps on the surface have been explained through various theories. One of the major causes for surface trapping effects is considered to be the “*surface states*”. The mechanism of the formation of charged surface states and the resulting origin of electrons in the 2DEG at the AlGa_N/GaN interface was first proposed by J. P. Ibbetson et al. [103].

The “*surface donor model*” as proposed by J. P. Ibbetson et al. is based on the following facts. Firstly, the sum of the various space charges is zero, since under the absence of any externally applied field, the structure as a whole must be charge neutral. Secondly, the polarization-induced charges constitute a dipole whose net contribution to the total space charge is exactly zero. Thirdly, the fixed buffer charges must be negative or the 2DEG will not be confined at the AlGa_N/GaN interface. Thus, the 2DEG cannot be due to electrons generated thermally in the buffer, which have to leave behind a positive space charge. This means that a positive sheet charge must exist on the heterostructure surface in order for the 2DEG to be present in the AlGa_N/GaN interface.

The effects of surface related traps were first reported by R. Vetury et al [100] using un-passivated AlGa_N/GaN HEMTs. As discussed in the earlier sections, conventional AlGa_N/GaN HEMTs are fabricated in D-mode or otherwise called as normally-ON transistors. Thus, the 2DEG channel is present even under zero bias conditions. At a certain negative V_{gs} below the

V_{th} , drain current ideally becomes zero over any drain voltage. This is because the negative bias on gate ($< V_{th}$) fully depletes the 2DEG channel under the gate. After the removal of the negative bias at the gate terminal, while the drain voltage is maintained constant, the measured drain current shows a transient effect [97]. However, the conventional principle cannot explain this current dispersion. This is because electron trapping in the region below the Schottky gate results in a V_{th} shift, but the drain current in pulsed $I_D - V_D$ under a sub-threshold Q-bias is still lower at a higher V_{GS} to compensate V_{th} shift than that in DC $I_D - V_D$. R. Vetry et al [100] used the “*virtual gate*” concept to explain the current dispersion due to surface trapping on the ungated surface between the gate and drain contact under a positive drain bias and negative V_{GS} . According to the model, the donor like surface states which exist by virtue of the 2DEG will act as electron traps. These surface states when filled by electrons that are injected from the gate metal at negative potential will compensate the 2DEG electrons in the channel in order to conserve charge neutrality. This will result in the extension of the depletion region beyond the influence of the gate terminal as shown in Fig. 2.7(a). Even when the gate bias is removed, the electrons trapped by the surface states still remain which correspond to their emission time. Hence, now it seems that there is yet another gate in between the actual gate and the drain terminal as shown in Fig. 2.7(b).

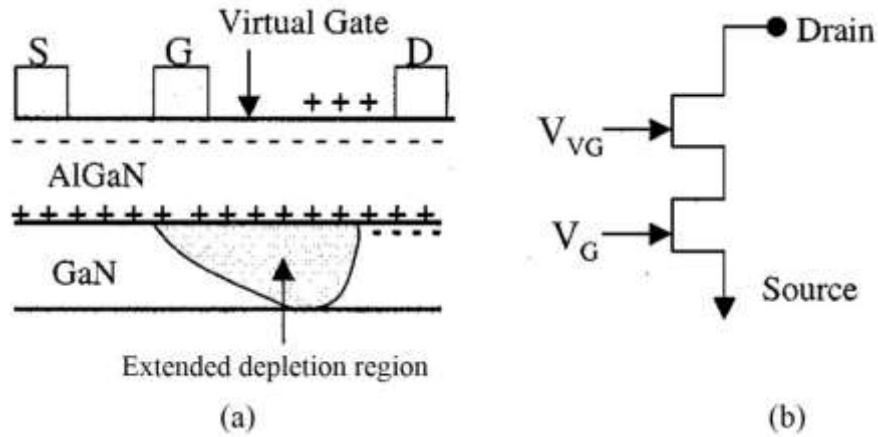


Figure 2.7 Model of the device showing (a) the location of the virtual gate and (b) the schematic representation of the device including the virtual gate [100].

This virtual gate is totally controlled by the trapping and detrapping of electrons by the surface states. Thus, the presence of the virtual gate results in a delayed response of the device.

This delayed response of the drain current to V_G variation from OFF-state to ON-state is also called the *gate-lag* effect [97]. The presence of the trapped charge on the surface was confirmed by scanning Kelvin probe microscopy [104]. In addition to the surface states, various process induced anomalies can also give rise to electronically active traps on the AlGaN/GaN HEMT surface, leading to gate-lag effects [see Fig. 2.5]. These traps originate from surface point-defects, dangling-bonds or impurities at the surface, formed during crystal growth or in subsequent device fabrication processes/surface preparation methods such as metal evaporation and plasma damage during etching.

2.6.2 Bulk Trapping Effects

As illustrated in the Fig. 2.5, the electron traps that are also present in the AlGaN barrier or GaN buffer or anywhere within the device heterostructure are collectively termed as bulk traps. Under high electric field conditions, due to the high drain-source voltage (V_{ds}), electrons from the 2DEG channel may get injected into the traps within the heterostructure. Although the trapping at the surface or inside the AlGaN barrier layer is believed to be an important cause for current collapse, electron trapping in the GaN buffer can also lead to severe drain current dispersion [53]. The trapped electrons again produce a negative charge, which depletes the 2DEG, and therefore result in a drain current dispersion. This current collapse induced by bulk traps is characterized as “*drain-lag*”. The source of these bulk traps are mostly due to material growth conditions of the AlGaN/GaN heterostructure. These traps are also related to threading dislocations in the GaN layer due to the large lattice-mismatch between the GaN and the non-native substrates. The threading dislocations in the GaN epitaxial layers give rise to a multitude of deep level states distributed across the GaN energy bandgap. Another major source of buffer traps are the compensation charges present even in the un-intentionally doped GaN buffer which occurs due to the background doping effects which have been observed in MOCVD growth. These deep acceptors act as traps causing drain current collapse under high voltage operations. This type of current collapse at high drain voltage is attributed to injection and trapping of hot-electrons or hot electron effects (HEE) in the GaN buffer [97]. The injection of hot-electrons

into the bulk traps can lead to the “*kink effect*” in the DC characteristic, as shown in Fig. 2.8.

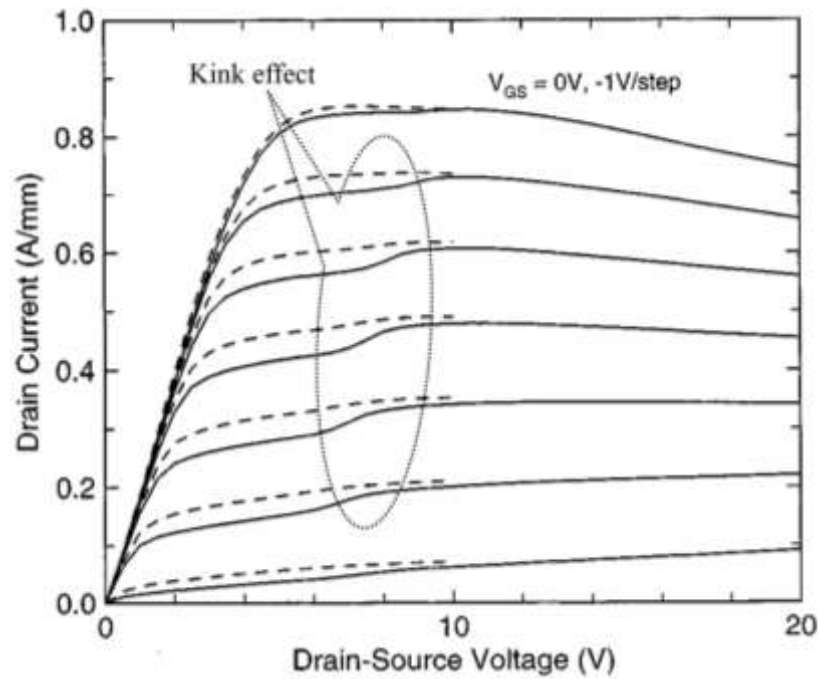


Figure 2.8 DC I_D - V_D characteristics of AlGaIn/GaN HEMTs showing a pronounced kink effect when measured until $V_{DS} = 20$ V (solid lines), and the absence of kink effect when measured only until $V_{DS} = 10$ V (graded lines) [97].

Once the hot-electrons are captured by trapping centres in the buffer, the channel is depleted and the drain current is reduced. However, the collapsed current is recovered at a higher drain voltage. Bulk trapping can also occur due to charge tunnelling from the gate into the semiconductor [101]. The tunnelling is assisted by a strong transverse electric-field across the gate-to-channel barrier layer. The electron injection from the gate into the bulk traps has also been observed by J. Joh et al [105]. Figure 2.9 shows, the bulk

trapping effects by AlGaN barrier traps (TP1) and GaN buffer traps under ON and OFF state conditions and their corresponding energy band diagrams.

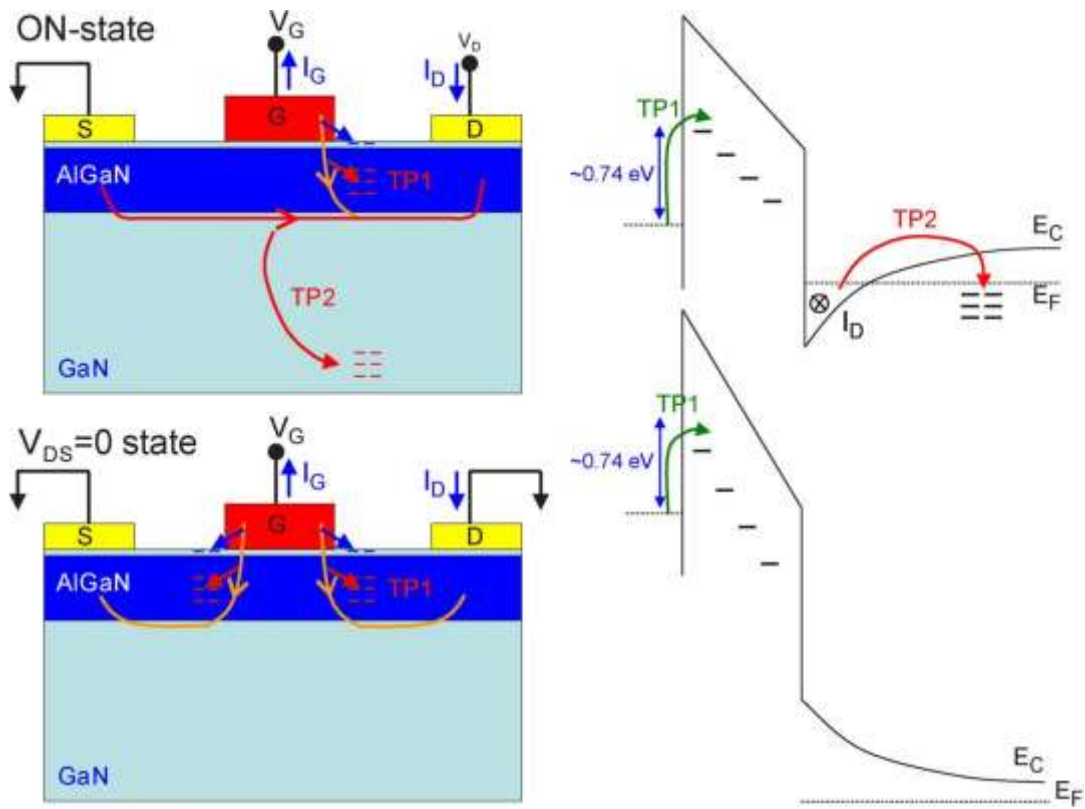


Figure 2.9 Schematic cross-sectional diagrams of the trapping behaviour in the ON-state and OFF-state. Corresponding band diagrams are also shown. Arrows indicate the direction of electron flow [105].

Under ON-state condition, electrons are injected from the gate into the AlGaN/GaN heterostructure and get trapped in the traps present in the AlGaN barrier (TP1). The hot electrons generated at the 2DEG channel gain enough energy to spread into the GaN buffer region get trapped in traps present in the GaN buffer (TP2). Under the OFF-state conditions, trapping in the AlGaN barrier due to the injection of gate electrons is observed. Measurements of drain-lag as a delayed response of drain current to V_{DS} change is one method to analyse current collapse due to bulk trapping

effects. Current collapse in AlGaIn/GaN HEMTs characterized by means of pulsed measurements based on drain-lag turn-ON technique was used by Tirado et al [106] to differentiate between surface and bulk traps. The obtained drain current suggested that the surface related traps exhibited faster emission rate whereas the bulk related traps exhibited a relatively slower emission rate.

Various researchers have attributed the current collapse phenomenon observed in AlGaIn/GaN HEMTs to different types of traps present in the buffer layer. L. Zhang et al. [54] observed a significant DC drain current reduction after applying a high drain-bias to GaN HEMT devices. They attribute this drain current collapse to charge injection and trapping of electrons in the GaN buffer region due to the prevailing high electric fields at high drain-bias. G. Meneghesso et al. [107] were able to draw a correlation between drain current collapse and the threshold voltage shift in GaN HEMTs. Through photo-transient measurements, they attribute the observed current collapse to electron trapping in the regions under the gate and the gate-to-drain access region. Furthermore, they were able to identify the presence of traps in the unintentionally-doped GaN buffer region or at the GaN buffer/channel interface using photoionization spectroscopy measurements.

S. C. Binari et al. [108] have also reported on the trapping effects in GaN HEMTs. The effect of current collapse in GaN HEMTs under dark (dotted line) and illuminated (solid line) conditions is shown in Fig. 2.10 (a). A significant reduction in the drain current with a clear knee walk-out can be

observed due to the current collapse phenomenon. They report that, under elevated temperature (up to 155°C), the GaN HEMTs exhibited little or no drain current collapse. This reduction in the current collapse at higher measurement temperatures is attributed to the thermal emission of trapped electrons from deep traps. However, they observed a time dependence for the drain current recovery, which suggested a multiple-component response relating to the involvement of multiple traps that caused the current collapse.

Figure 2.10 (b) shows the recovery of collapsed drain-current when illuminated with light of different wavelengths. The drain-current recovery pattern showed a clear dependency on the incident wavelength. This wavelength-dependency was attributed to a broad trap related absorption below the GaN energy bandgap. These deep level traps originated due to the compensation of shallow donors in order to achieve high-resistive GaN buffer layer while grown by MOCVD growth process. Using drain-lag measurements X. Dang et al. [109] were able to identify traps with different emission time constants in GaN HEMTs. Three different traps corresponding to three different emission times were identified:

- 1) Traps with an intermediate time (10 s), which were attributed to deep levels in the AlGaN;
- 2) Fast traps (1 s), attributed to the surface, and
- 3) Slow traps (100 s), which were associated with the channel.

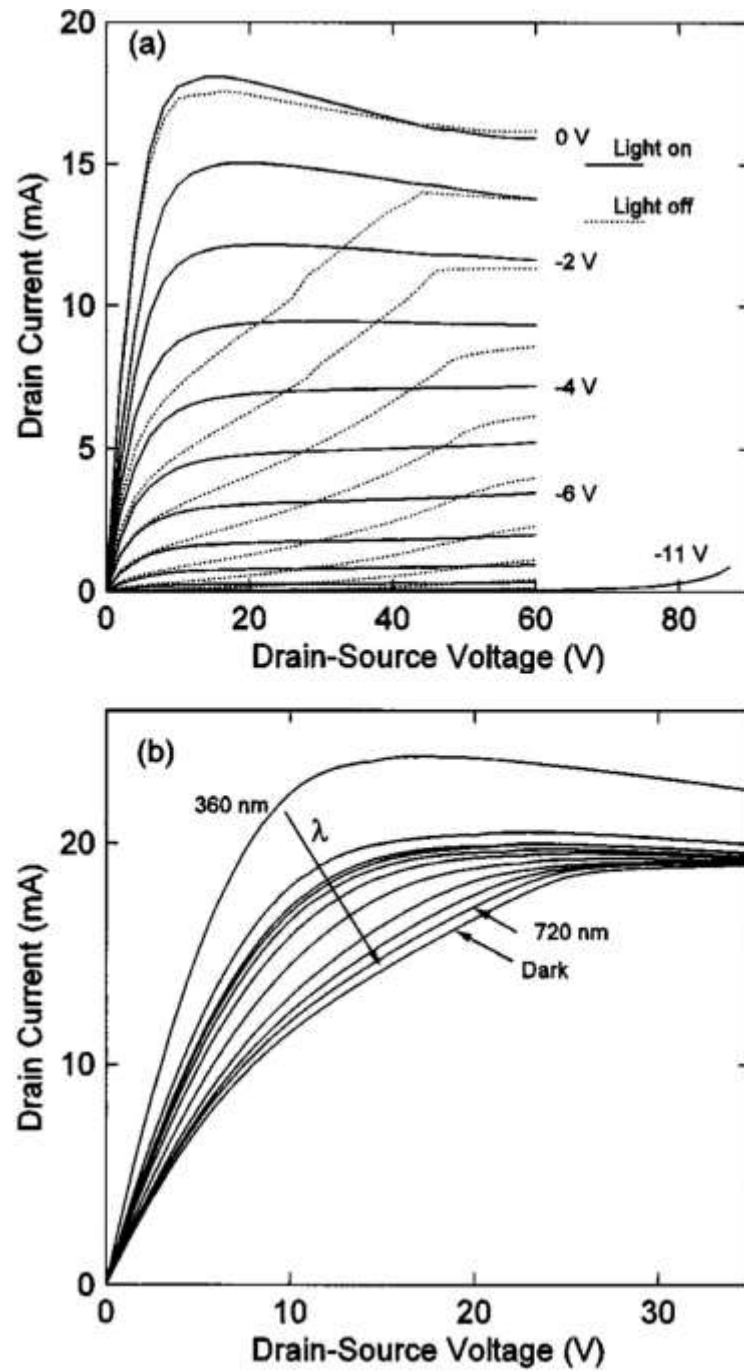


Figure 2.10 (a) Current collapse phenomenon observed in GaN HEMTs, under dark (dotted) and illuminated (solid) conditions, (b) Recovery of collapsed drain-current under light illumination with different wavelengths [108].

We analysed the drain current-transients obtained after fully ON-state stress conditions and observed the presence of a distribution of trap energy (DTE) levels in the energy band gap of buffer GaN of AlGaN/GaN HEMTs [58].

2.7 Trap Characterization methods

There are various methods that are used for investigating the trapping behaviour in semiconductor structures. A quick and reliable characterization of the current collapse can be obtained through the execution of pulsed drain-current versus drain (or gate) voltage measurements (pulsed I_D - V_D or I_D - V_G characterization) [59], which helps to investigate the changes in drain current, ON-resistance, and threshold voltage induced by the capture of electrons within the AlGaN/GaN heterostructure. Other methods including deep-level transient spectroscopy (DLTS), constant capacitance deep-level transient spectroscopy (CC-DLTS), deep-level optical spectroscopy (DLOS), gate-lag measurement, low-frequency noise measurement, and frequency-dependent g_m dispersion and conductance analysis, are used to study the trapping behaviour in GaN HEMTs [52][53][110][111]. A more accurate description of the properties of the traps relevant for GaN-based transistors operation can be obtained by studying the current-transients (in the ON-state) induced by exposure to a trapping voltage in the OFF-state (typically a negative gate bias, or a high drain-gate voltage), through drain-current DLTS (I-DLTS) [92] or multi exponential transient measurements [55][57][104][112]. However, for the

trap characterization in AlGaN/GaN HEMT devices, pulsed I_D - V_D and multi-exponential current-transient techniques are found to be more effective.

2.7.1 Pulsed I_D - V_D characterization

The DC (static) I_D - V_D measurements of GaN HEMTs are greatly influenced by self-heating and trapping effects, which renders it ineffective for trap characterization. Thus, in order to capture the nonlinear dispersion that occurs in GaN HEMTs due to trapping effects, a more relevant technique is necessary. The conventional trap analysis techniques such as DLTS require large gate area devices (e.g., diodes) for precise data acquisition [105]. In highly scaled devices, the DLTS signals can be affected [105] by the fringing capacitances of the adjacent electrodes. Furthermore, with a pulse width and separation of 200 ns and 1 ms, respectively, the pulsed I_D - V_D measurement technique resembles radio-frequency and micro-wave conditions which is basically the operation conditions of the device [113]. The pulsed (dynamic) I_D - V_D characterization technique is considered to be the most suitable technique to characterize traps in AlGaN/GaN HEMTs [113][114].

This technique has two distinct advantages over DC I_D - V_D characterization when used to examine these devices. Firstly, by limiting the amount of time that high currents are flowing through the device, thermal heating effects are minimized that may cause higher channel resistance. Secondly, by conducting measurements on a time scale that is shorter than the time constants of the surface states that cause RF dispersion, pulsed I_D - V_D can

effectively obtain a snapshot of the degraded performance that would be seen during RF operation.

A schematic of the Accent Diva D265 pulsed I_D - V_D measurement setup is shown in Fig. 2.11. It consists of power supplies and input/output measurement units which are embedded in the same hardware. It also consists of two probe heads for the gate and drain access. The purpose of these probe heads is to provide short pulses (down to 200 ns) and also to improve the quality of the pulse shape even in the presence of strong drain current variation. For pulsed I_D - V_D measurements, voltage signals of square pulse are applied from a static Q-bias point to obtain currents at the end of the pulse duration and, then, devices under test returns to and stay at the Q-bias point until the next voltage pulse is applied.

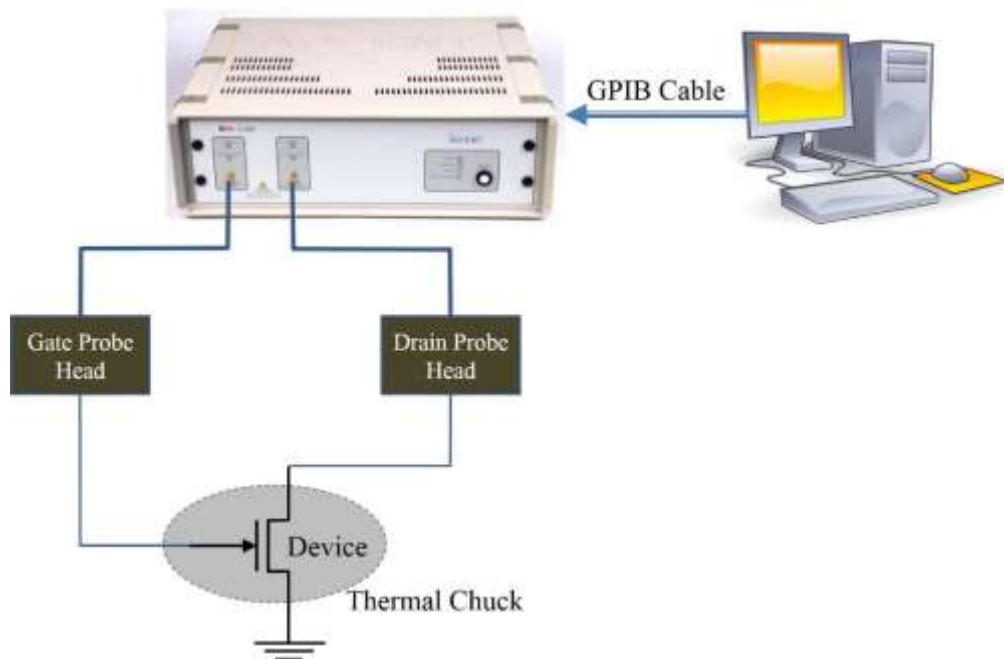


Figure 2.11 Pulsed I_D - V_D setup for GaN HEMT characterization with Accent Diva D265 analyser.

If the pulse duration is short enough compared with the separation time between consecutive voltage pulses, both temperature and trapping effects are dependent mainly on the Q-bias point. In case of a very short pulse duration, thermal effects are considered to be invariant and trapping effects are frozen when emission/capture time constants is smaller than the pulse duration. Figure 2.12 shows the pulse pattern of a pulsed I_D - V_D measurement under the gate- lag and the drain- lag condition. The pulse width is 200 ns and the pulse separation is 1 ms.

Gate-Lag Condition ($V_{GQ} = < V_{th}$, $V_{DQ} = 0$): In this case of Q-bias condition, the gate pulse is in the sub-threshold regime and the drain pulses is usually 0 V. The negative voltage applied to the gate terminal will cause tunnelling of gate electrons into the AlGa_N barrier. The tunnelled gate electrons get trapped in the various traps present in the AlGa_N barrier region directly under the gate, thus resulting in a shift in the V_{th} [57].

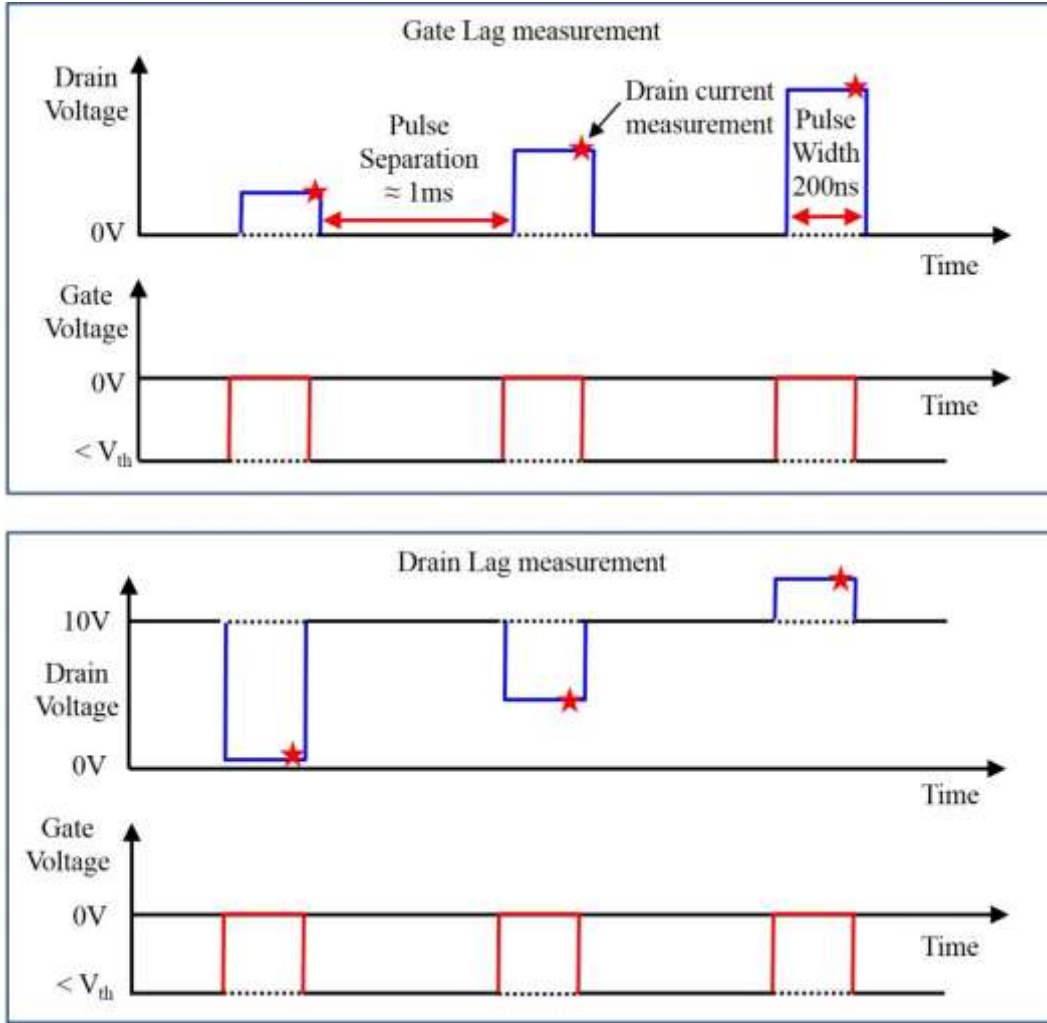


Figure 2.12 Generation of pulsed I_D-V_D for gate lag condition and drain lag condition.

Drain-Lag Condition ($V_{GQ} = < V_{th}$, $V_{DQ} = V_{DD}$) : In this case of Q-bias condition, gate pulse is in the sub-threshold regime as in the previous step, while a drain pulse equivalent to the value of V_{DD} is applied. In this case, due to the high voltage bias applied to the drain terminal, a huge spike in the electric field is created in the drain-side gate-edge leading to trapping of the tunnelled gate electrons in the access regions and surface of the AlGaIn/GaN barrier. This results in the increase of the dyn- $R_{DS[ON]}$ of the device [57].

It should be noted that the above stated conditions have the same thermal conditions, which means almost no power dissipation. Thus, these characterizations only involve trap related dispersion. Hence, by comparing the measurement results in the gate-lag Q-bias conditions and the drain-lag Q-bias conditions with that of a cold Q-bias condition of $[(V_{GQ}, V_{DQ}) = (0, 0) V]$, one can assess and quantify effects of trapping in the corresponding regions of prominence. Since a very short pulse width is applied, the pulsed I_D - V_D characteristics can be treated as quasi-static based on the following assumptions:

- 1) the number of traps with a capture time constant less than the pulse width applied is negligible, meaning that when such a short pulse is applied, electron trapping within the applied pulse width for each measurement is neglected at Q-bias of $(V_{GSQ}, V_{DSQ}) = (0, 0) V$, that is, there is no trapped charge;
- 2) The number of traps with an emission time constant less than pulse width applied is negligible, meaning that if a short pulse is applied, the trapped charge at a Q-bias of sufficiently high reverse gate bias is frozen during pulsed I_D - V_D measurements. That is, there is no emission of the trapped charge. Based on the above assumptions, change in V_{th} of a short pulse I_D - V_D characteristics between Q-bias of $(V_{GSQ}, V_{DSQ}) = (0, 0) V$ and any Q-bias conditions under which electrons are trapped (i.e. pinch-off Q-bias) corresponds to the V_{th} shift due to the density of trapped electrons.

In this thesis, the pulsed $I_D - V_D$ measurements were carried out using Accent DIVA 265 dynamic $I_D - V_D$ analysers (see Fig 2.11) with a pulse width of 200 ns and a pulse separation of 1 ms (see Fig 2.12). This pulse condition ensures that the emission/capture processes of electrons by trap centres are not affected by each measurement point, but by the applied Q-bias condition. We have limited to these minimum pulse signal condition due to the equipment limitations. In Chapter 4, we have extensively used the pulsed $I_D - V_D$ conditions to characterize the emission time constants of the traps.

2.7.2 Drain Current-Transients

The drain-current obtained from GaN HEMT after a high-voltage event has a transient nature due to the current-collapse caused by trapping effects. By analysing the measured drain current-transient signature, it is possible to characterize the properties of the traps involved in the trapping phenomena. This method is considered as a very reliable method for the study of trapping phenomenon in GaN HEMT devices [105]. The methodology consists of initially filling the traps using a “filling pulse”, which is a chosen bias stress condition, and later monitoring the recovery transient of the current over a period of time. The transient data that emerges from these experiments are analysed through mathematical calculations that extract the dominant time constants. The current-transient signal consists of the information of electrons that are being emitted by the traps that were previously filled during the filling pulse. The filling pulse is carefully chosen in order to activate the traps at different locations of the AlGaIn/GaN heterostructure. The calculation of the time constants of the current transients is a necessary

step toward the extrapolation of the Arrhenius plot of the trap levels. Drain current-transients are first fitted using a polynomial function $I_d(x) = a_0 + \dots + a_{n-1}x^{n-1}$ ($n = 10$; $x = \log(\text{time})$), and then $dI_d(x)/dx$ was de-convoluted using Gaussian functions. M. Tapajna et al [112] have reported that four Gaussian functions were adequate to fit $dI_d(x)/dx$ with mean, variance, and amplitude as fitting parameters.

For proper analysis of the trapping effects, D. Bisi et al [57] have clearly reported on the choice of bias points for the drain current-transient measurements. Using a semi-ON bias condition and a fully-OFF bias condition, the location of the traps were determined as buffer and surface/barrier related traps, respectively. Figure 2.13 gives the schematic representation of the location of trapping based on the applied bias conditions.

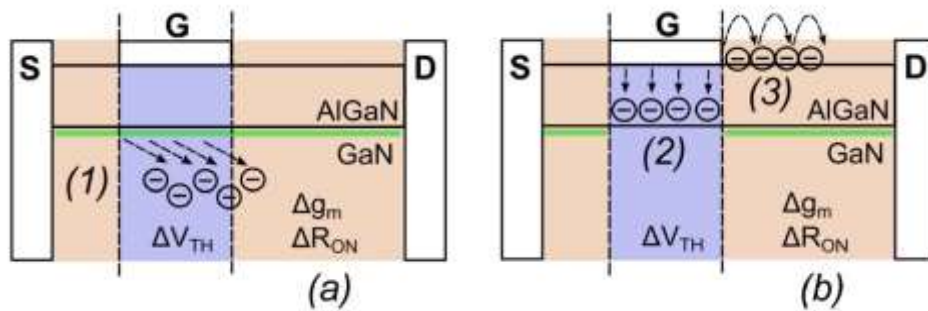


Figure 2.13 Possible trapping mechanisms and their influence on electrical parameters in (a) semi-ON-state and (b) OFF-state bias operating points [57].

They used three different biasing conditions in order to investigate the location of the traps. This result was obtained by carrying out a set of

transient measurements, starting from three different filling bias conditions:

- 1) $(V_{GQ}; V_{DQ}) = (-6; 27)$ V, in the OFF-state with both high-negative V_{GS} and high- V_{DS} , which promotes both gate- and drain-dependent trapping;
- 2) $(V_{GQ}; V_{DQ}) = (-1; 27)$ V, in the semi-ON state with high- V_{DS} level, which promotes only the drain-dependent trapping mechanisms; and
- 3) $(V_{GQ}; V_{DQ}) = (-6; 8)$ V, in the OFF-state, with high-negative V_{GS} and lower V_{DS} , promotes predominantly the gate-dependent trapping mechanisms.

Three different de-trapping behaviours corresponding to the three different biasing conditions were obtained as shown in Fig. 2.14 (a). The corresponding derivative is shown in Fig 2.14 (b). The amplitude of the transient labelled as “T1” is enhanced by filling pulses with high-drain voltage, and experiences its maximum amplitude under semi-ON-state trapping conditions $(V_{GQ}; V_{DF}) = (-1; 27)$ V

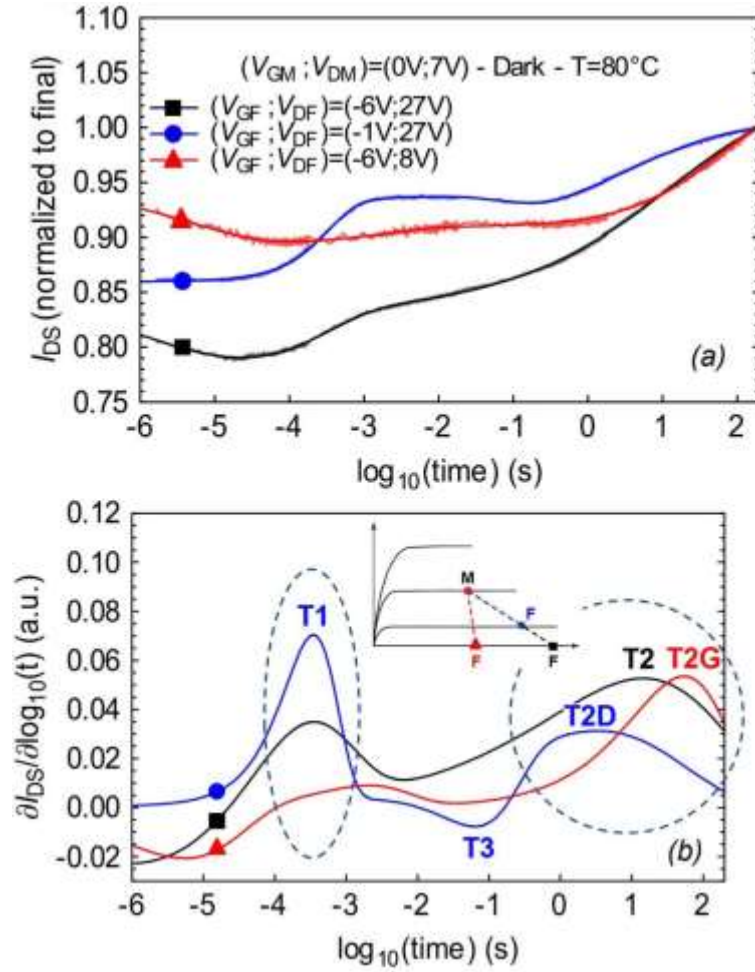


Figure 2.14 (a) Drain current transients recorded after different trapping conditions and (b) related differential signals [57].

On the contrary, the broad spectrum of transient “T2” is constituted by two components: one drain-influenced (labelled as T2D) which is enhanced during semi-ON-state condition, and one gate-influenced (labelled as T2G) which is enhanced during OFF-state trapping with moderate V_{DS} and high-negative V_{GS} ($V_{GQ}; V_{DF}$) = (−6, 8) V. Furthermore, during semi-ON-state trapping condition, an additional weak electron-capture or hole-emission process (labelled as T3) is detected.

The results described in Fig. 2.14 therefore indicate that by choosing proper filling voltages, it is possible to distinguish between drain- and gate-

dependent trapping processes: the peaks T1 and T2D, which amplitude are maximized by the combination of high- V_{DS} and relatively high-drain current levels can be ascribed to the trapping of negative charge which is likely due to hot-electrons injection into the buffer region. On the other hand, trap T2G supposed to be located in the region under the gate where charge trapping could be caused by high-reverse V_{GS} and the subsequent high-gate leakage current levels.

2.8 TCAD Simulations on the trapping effects in AlGaIn/GaN HEMTs

TCAD simulation and modelling is a versatile tool for predicting the device performance based on basic scientific understanding and to translate the results towards expediting the device development and optimization process for new technology. The TCAD tools are widely being used today in the semiconductor industry and academia. Even before the devices are ready for measurements, such simulators can give a thorough understanding of the mechanisms that govern the device performance and the various failure modes that are associated with it. A beforehand understanding of the device electrical characteristics based on simulations will help us in creating a meaningful design of experiment and also a clear direction for data analytics. In this thesis we have used a TCAD tool called ATLAS, a PISCES based two-dimensional numerical device simulator from Silvaco [58].

A simplified flow chart of the TCAD simulation work performed for this thesis is shown in Fig. 2.15. The basic steps followed are:

- Use the device editor to virtually fabricate the device
- Create an appropriate mesh for device simulation
- Define simulation parameters and models
- Perform numerical simulations and get device performance
- Generate output plots

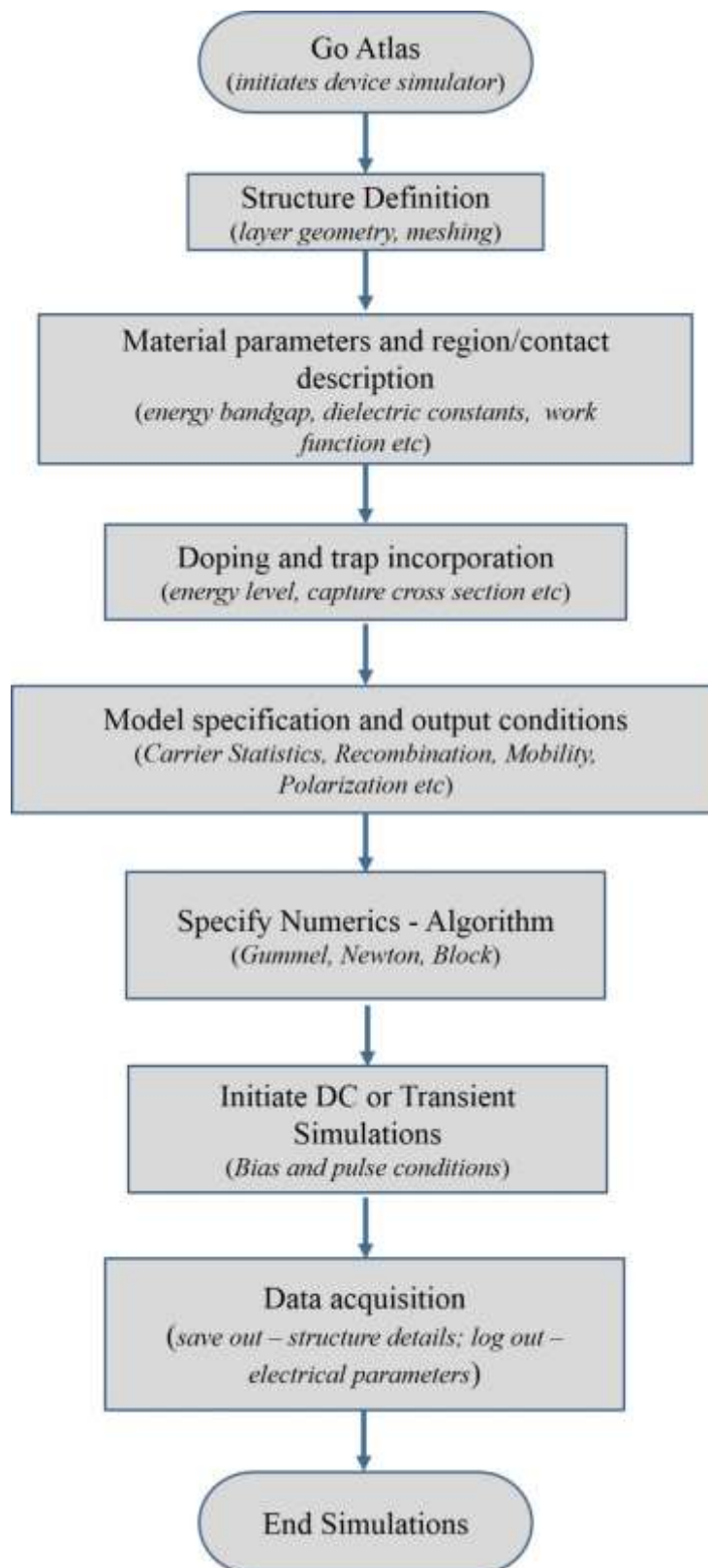


Figure 2.15 Simplified flow chart representation of TCAD simulations.

A set of fundamental semiconductor physics equations are solved for every grid point of the defined mesh. The numerical method used in the calculations is the Newton method. The temperature is 300 K by default. The current-voltage relationship for each electrode can be calculated, as well as the carrier density, electric-field and electric potential profiles in the device.

The basic equations to be solved are: the Poisson's equation including the contribution of mobile and fixed charges and ionized traps, carrier continuity equations for electrons and holes, and transport equations using the drift-diffusion model. Poisson's equation relates the variations of electrostatic potential and electric-field to the electrostatic charges including the contribution of mobile and fixed charges and ionized traps [58]. Dynamic traps are modelled by a Shockley-Read-Hall recombination term, included in the continuity equations. The Universal Schottky Tunnelling (UST) model is enabled in order to capture the tunnelling of the gate electrons under negative gate bias. An additional differential rate equation is solved to account for emission and capture processes in transient trap simulations. The emission time constant of the incorporated traps are controlled by the capture cross sections.

Since our focus is to understand and simulate the effects of trapping on the electrical characteristics of AlGa_N/Ga_N HEMTs, we have incorporated the experimentally obtained trap parameters into the heterostructure and simulated the transients under different bias conditions. By incorporating the traps in the AlGa_N barrier and Ga_N buffer of the AlGa_N/Ga_N heterostructure, we were able to verify the effects of trapping OFF-state and

ON-state voltage stresses. We have used both single trap energy (STE) model [55] and the multiple trap energy (MTE) models [54][55] to validate our experimental observations in this work.

Chapter 3

Fabrication of GaN HEMTs and MISHEMTs

The fabrication process flow for the AlGa_N/Ga_N HEMTs and MISHEMTs used for this thesis is furnished in this chapter. The first part of this chapter describes the device structure and the process flow for the fabrication of conventional Schottky gated Ga_N HEMTs with different gate lengths. The second part of the chapter deals with the process flow for the Ga_N MISHEMTs.

3.1 Device Structure

For our studies, we have used conventional AlGa_N/Ga_N heterostructures grown by metal organic chemical vapour deposition (MOCVD) method. The substrate used was high resistivity (HR) Si (111). The AlGa_N/Ga_N heterostructure consists of the following layers (from top to bottom):

- 1) Ga_N Cap Layer
- 2) AlGa_N barrier layer
- 3) Ga_N buffer
- 4) Transition or nucleation layer and
- 5) Si Substrate

The typical Ga_N heterostructure is shown in Fig. 3.1. The cap, barrier and *i*-Ga_N layers are unintentionally doped. Figures 3.1 (a) and (b) show the two

types of AlGaN/GaN heterostructures used for fabricating devices that were used for this thesis. The first device structure shown in Fig. 3.1 (a) corresponds to: i -GaN (2 nm)/ i -Al_{0.26}Ga_{0.74}N (18 nm)/ i -GaN (800 nm)/transition layer (1400 nm)/HR-Si (111) substrate. The resistivity of the Si substrate is $>6,000 \Omega\text{-cm}$ [55]. The grown structures exhibited a room-temperature 2DEG mobility of $1500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and room-temperature sheet-carrier density of $1 \times 10^{13} \text{ cm}^{-2}$ as determined through Hall measurements.

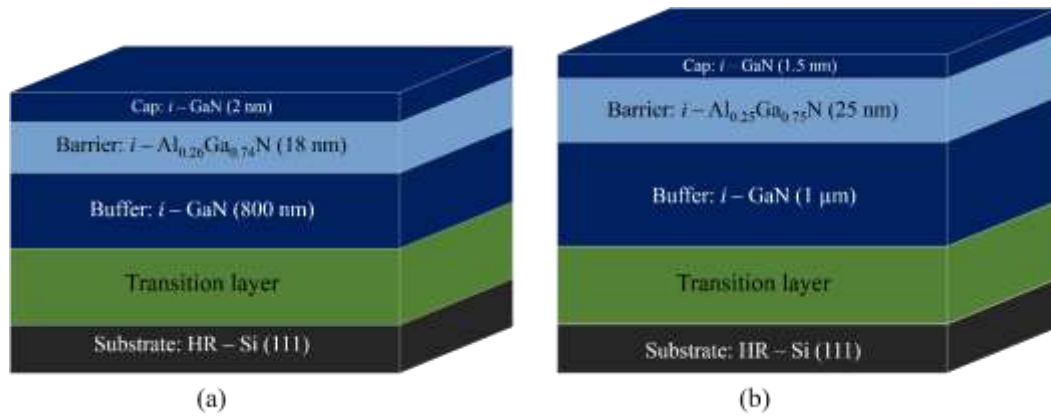


Figure 3.1 Schematic cross-section of a conventional AlGaN/GaN heterostructure with two different buffer and barrier thicknesses used for this study.

The sequence of the AlGaN/GaN heterostructure shown in Fig. 3.1 (b) corresponds to: i -GaN (1.5 nm)/ i -Al_{0.25}Ga_{0.75}N (25 nm)/ i -GaN (1 μm)/transition layer/ HR-Si (111) substrate. The resistivity of the Si substrate is $>6,000 \Omega\text{-cm}$. The AlGaN/GaN heterostructure exhibited a 2DEG sheet-carrier density, sheet resistance, and a mobility of $0.8 \times 10^{13} \text{ cm}^{-2}$, $450 \Omega/\square$, and $1456 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively at 300 K [115]. The epilayer

thicknesses were confirmed by cross-sectional transmission electron microscopy (TEM).

3.2 Fabrication of AlGa_N/Ga_N HEMTs

For this study, we fabricated AlGa_N/Ga_N HEMTs with different gate-lengths. For high-voltage stress studies, we used long gate-length ($L_g \geq 1 \mu\text{m}$) Ga_N HEMTs. For high-frequency based studies, we used sub-micron gated ($L_g \leq 1 \mu\text{m}$) Ga_N HEMTs. The fabrication process consists of four main steps.

- i) Mesa Isolation
- ii) Ohmic contact formation (source and drain terminals)
- iii) Schottky contact formation (gate metallization), and
- iv) Surface passivation.

i. Mesa Isolation:

Proper electrical isolation between adjacent devices is necessary to prevent leakage currents and possible short circuiting. Thus, it is vital to isolate the devices by realizing a very high-resistive region (buffer Ga_N) between the adjacent devices. The device isolation is achieved by mesa isolation. In this study, mesa isolation has been achieved through dry etching process. Reactive Ion Etching (RIE) or Inductive Coupled Plasma (ICP) are the most commonly used dry etching methods for mesa isolation of Ga_N based heterostructures. However, ICP etching offers low damage etch compared to the RIE.

For the devices used in this thesis, the mesa structures were realized using the ICP etching method. ICP system has the advantages of high plasma

density, low ion and electron energy (and thus low damage) while maintaining fast etch rates. The ICP etching recipe developed in this work was optimized for low surface damage while keeping an acceptable etch rate. For the devices used in this study, the mesa isolation was achieved through patterning using conventional lithography followed by ICP etch with BCl_3/Cl_2 gas chemistry. In order to attain effective electrical isolation, the etch depth is optimized to be larger than the 2DEG depth. The successful mesa isolation was ensured by etching down below the 2DEG channel into the GaN buffer to a depth of ~ 200 nm.

ii. Ohmic Contact Formation

An ohmic contact is necessary to establish a good electrical connection between the channel and the heterostructure surface. Thus, the quality and the behaviour of the metal semiconductor contact is an important issue in device design and transistor performance. For realizing high maximum drain current densities, the ohmic contact resistance (R_c) has to be as low as possible. Furthermore, low R_c also leads to higher extrinsic transconductance, which helps to achieve high frequency operation.

In order to achieve very low R_c , the work-function of the contact material has to be smaller than the electron affinity of GaN to provide a low resistance path for the channel electrons. Secondly, the ohmic contacts must have a smooth surface morphology with good edge quality in order to prevent alignment problems during further lithography steps. Also, the contacts must have a sufficient mechanical stability, especially for testing with measurement probes.

To achieve a low R_c and conformal adhesion between the metal and the semiconductor, proper surface preparation is necessary before the metallization process. Any residual photoresist from the previous process steps are removed by a short-time oxygen plasma by RIE. Subsequently, the ohmic metal stack is formed using the electron beam (E-beam) evaporator.

iii. Schottky Gate formation

GaN HEMTs being a field effect transistor, the formation of a Schottky contact which is the gate is very vital. The energy barrier height that forms in between the contact metal and the semiconductor surface is a crucial parameter in order to achieve the desired device electrical characteristics. Thus, in order to realize devices with low gate leakage currents and high breakdown voltages, a gate contact with high Schottky barrier height is necessary. This is achieved by using metals with high work function. Furthermore, since the GaN HEMTs exhibit high channel currents resulting in high channel temperatures, the gate metal should have high thermal stability. Also, for conformal and a stable gate structure, the gate metal should have a good adhesion with the semiconductor surface. The gate metal contact is formed by E-beam evaporation.

iv. Surface Passivation

One major challenge in the transistors under operation conditions is the performance degradation under high-frequency and high-voltage stress. Thus, the measured maximum power density is lower than that predicted from the static DC current-voltage characteristics. This RF to DC dispersion, commonly termed as current collapse is mostly due to the presence of a

large amount of surface states at the surface of the III-Nitride semiconductor. Furthermore, surface contamination and plasma related damages due to various fabrication processes can also bring about surface related trapping resulting in current collapse. These surface states which arise due to the dangling bonds/dislocations/defects at the surface as grown or by process induced surface damages or contaminations act as a source of electron traps. By trapping the electrons that are injected from the gate or the hot electrons from the 2DEG channel, a charge imbalance is created which depletes the channel electrons by forming a virtual gate. Thus it is important to mitigate the surface states through an appropriate process.

It has been found that passivation of the III-Nitride heterostructure surface using dielectrics such as Si_3N_4 [116][117], SiO_2 [118][119], Al_2O_3 [120], etc. dramatically improves the RF performance of the devices by effectively suppressing the surface related trapping effects. The devices used in this study were passivated using a 120 nm-thick Si_3N_4 layer deposited by PECVD at 300°C.

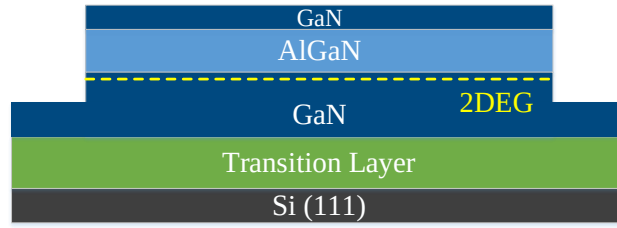
3.2.1 Long Gate-Length ($L_g \geq 1 \mu\text{m}$) GaN HEMTs

The AlGaN/GaN heterostructure used for fabricating HEMT devices with long L_g ($\geq 1 \mu\text{m}$) is shown in Fig. 3.1 (a). The fabrication process flow for the long L_g GaN HEMT devices used for this work is shown in Fig. 3.2. For the mesa isolation, patterning was done through conventional lithography followed by ICP etch using BCl_3/Cl_2 gas chemistry. After the mesa isolation, the samples went through ammonium sulphide $[(\text{NH}_4)_2\text{S}_x]$ surface treatment [121]. Subsequently a 120 nm-thick Si_3N_4 was deposited by

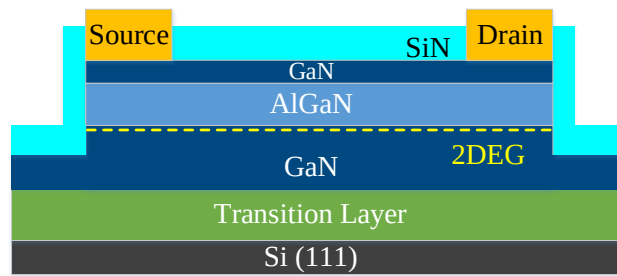
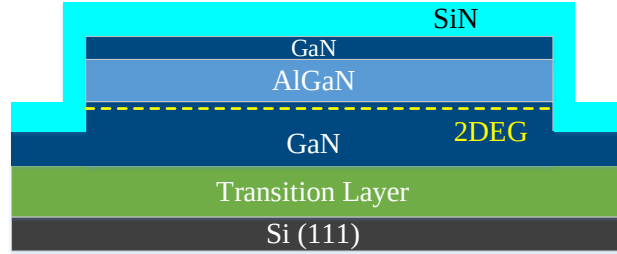
PECVD at 300°C. The source and the drain regions were then opened by lithography and the Si₃N₄ was dry etched using CF₄/O₂ plasma. A non-gold metal stack of Ta/Si/Ti/Al/Ni/Ta (8/2/15/140/30/25-nm) was then deposited as ohmic contacts and annealed at 800°C for 30 s [36][55]. This metal scheme exhibited a low R_c of 0.24 Ω -mm. Subsequently, for forming the gate electrode, a contact mask aligner was used for patterning the gate foot print for $L_g \geq 1 \mu\text{m}$. The non-gold gate electrode was formed using Ni/Al/Ta (50/400/50-nm) metal stack after etching Si₃N₄ by CF₄/O₂ plasma. Finally, the devices were passivated with 120 nm-thick PECVD grown Si₃N₄.

Fabrication Process Flow for HEMTs with $L_g \geq 1 \mu\text{m}$

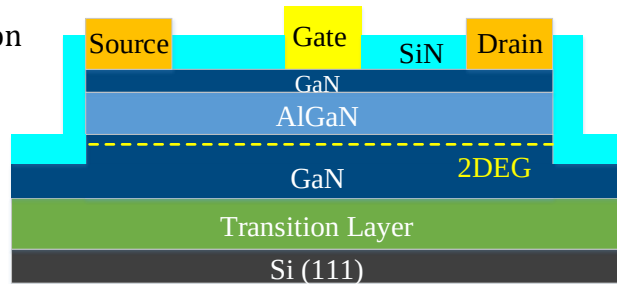
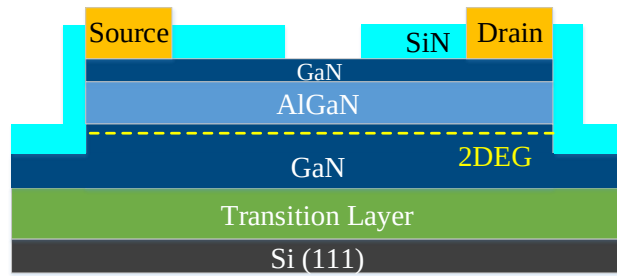
1) Mesa Isolation



2) Ohmic contact formation



3) Schottky contact formation



4) Final Passivation

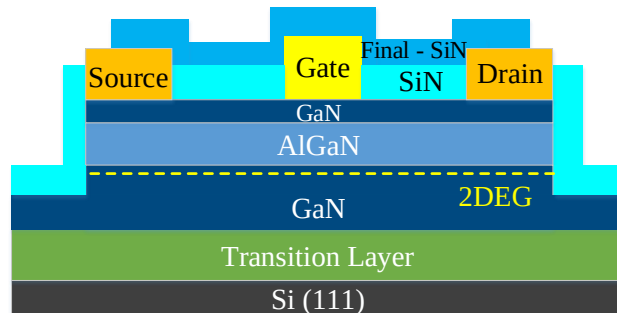


Figure 3.2 Main processing steps for $L_g \geq 1 \mu\text{m}$ AlGaN/GaN HEMTs.

For trap studies presented in Chapters 4 and 5, we have used devices fabricated with a non-gold CMOS compatible non-gold metal schemes with an L_g of 2 μm [54][55].

3.2.2 Sub-Micron Gate GaN HEMTs

The AlGaN/GaN heterostructure used for fabricating sub-micron gated devices is shown in Fig. 3.1 (b). The fabrication process started with mesa isolation, patterned using conventional lithography followed by ICP etch using BCl_3/Cl_2 gas chemistry. Subsequently the ohmic contacts were formed with a metal stack of Ti/Al/Ni/Au (20/120/40/50-nm) by E-beam evaporation, followed by rapid thermal annealing at 800°C for 30 s in N_2 atmosphere. The R_c and the specific contact resistivity (ρ_c) of the ohmic contact were 0.2 $\Omega\cdot\text{mm}$ and $8.06 \times 10^{-7} \Omega\cdot\text{cm}^2$, respectively [115]. Thereafter, the samples went through ammonium sulfide $[(\text{NH}_4)_2\text{S}_x]$ treatment [121] followed by 120 nm-thick Si_3N_4 layer [1st Si_3N_4] deposition by PECVD at 300°C. Subsequently a 0.15 μm gate foot-print and 0.5 μm gate-head was formed using electron beam lithography followed by Ni/Au (100/400-nm) gate metallization by E-beam evaporation. The samples then went through final passivation with 120 nm-thick Si_3N_4 (2nd Si_3N_4) by PECVD followed by air-bridge formation with 5 μm -thick gold plating process. The fabrication process flow for the sub-micron gated GaN HEMT devices used for this work is shown in Fig. 3.3. A cross-sectional high-resolution transmission electron microscopy (HR-TEM) image of the fabricated 0.15 μm T-gate is shown in Fig. 3.4.

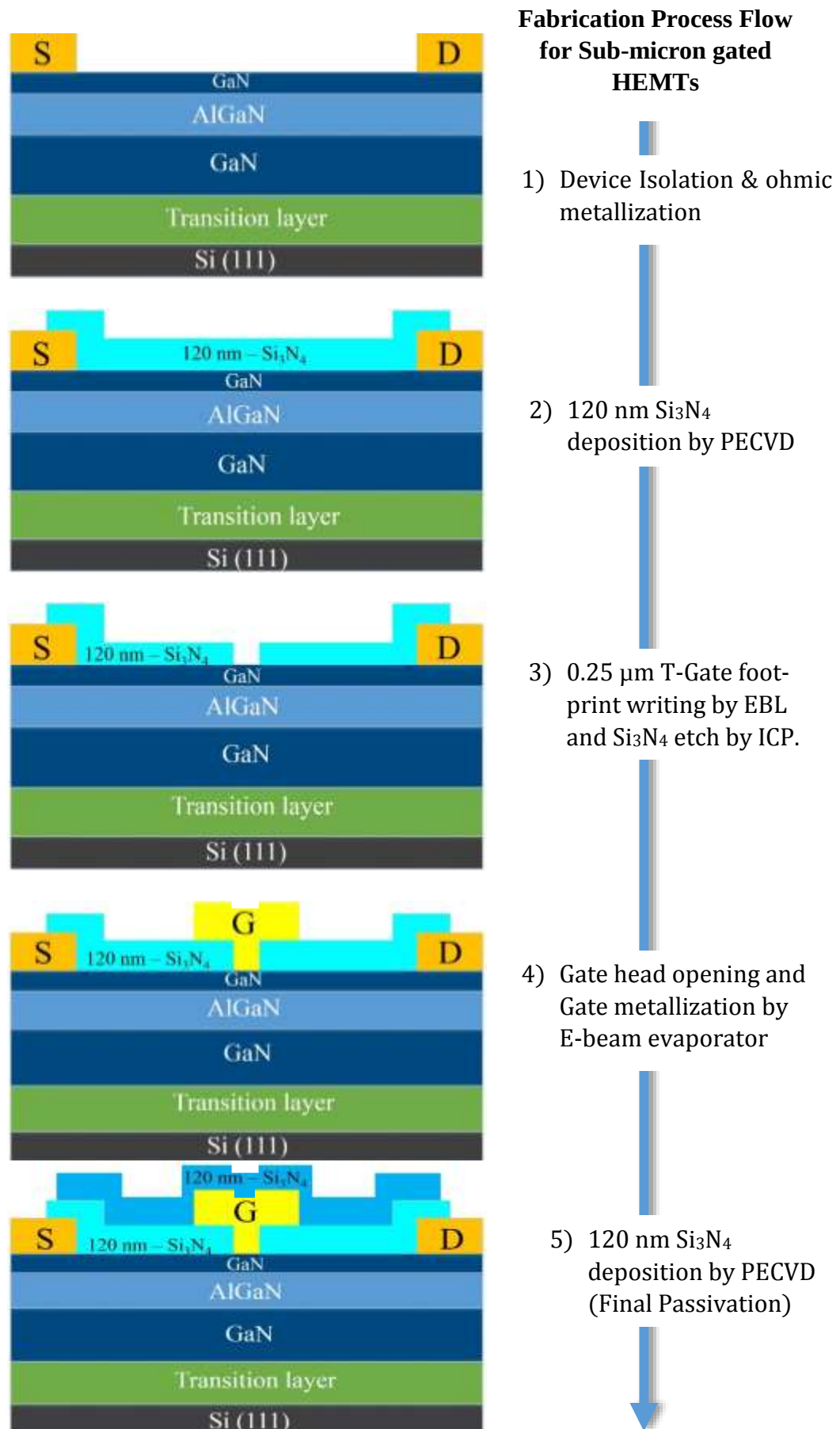


Figure 3.3 Process flow for fabrication of GaN HEMTs with submicron T gate.

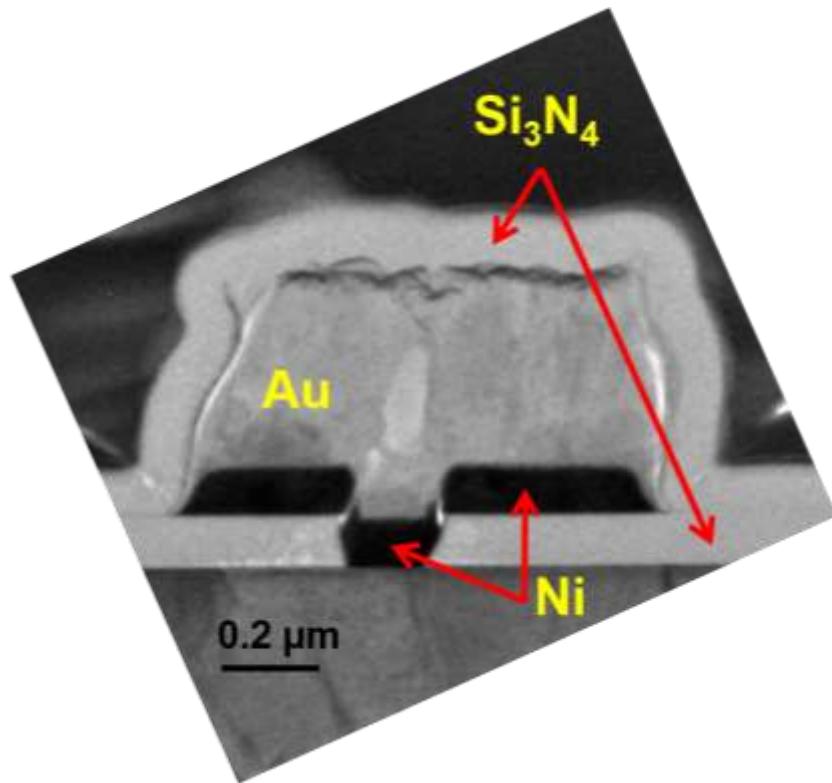


Figure 3.4 Cross-sectional view of the HR-TEM image of 0.15 μm T-gate.

3.3 Fabrication of AlGaN/GaN MISHEMTs

The AlGaN/GaN heterostructure used for fabricating the sub-micron gated AlGaN/GaN MISHEMT devices is shown in Fig. 3.1 (a). The cross-sectional schematic of the fabricated AlGaN/GaN MISHEMT is shown in Fig. 3.5. The fabrication processes started with mesa isolation, patterned using conventional lithography followed by ICP mesa etch using BCl_3/Cl_2 gas chemistry. Subsequently, the ohmic contacts were formed with the four layer metal scheme of Ti/Al/Ni/Au (20/120/40/50-nm) followed by rapid thermal annealing at 850°C for 30 s in N_2 atmosphere. A low R_c value of 0.16 $\Omega\text{-mm}$ was achieved.

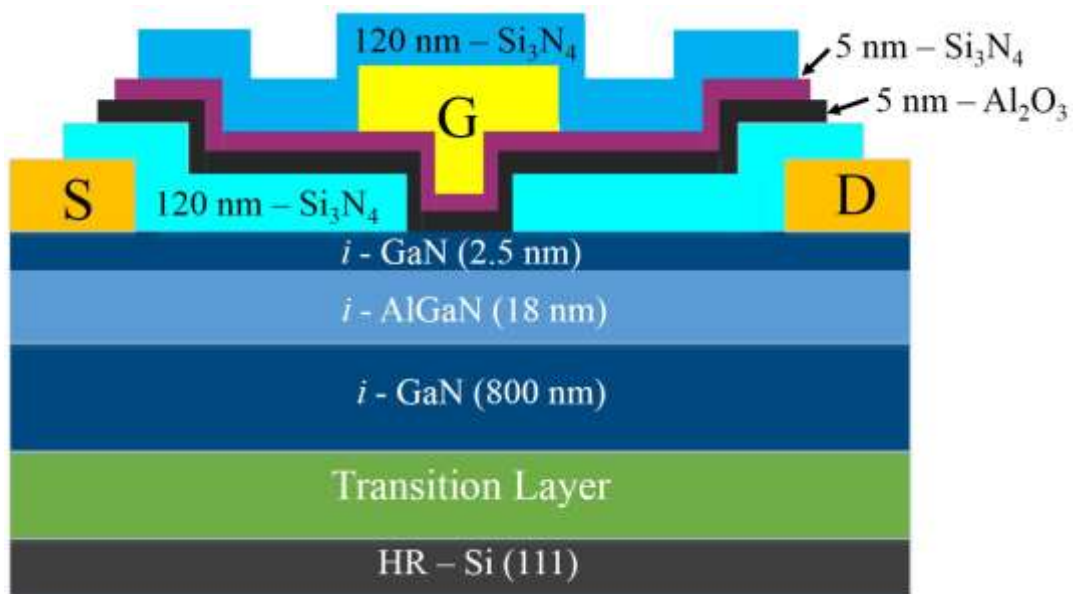


Figure 3.5 Schematic diagram of AlGaN/GaN MISHEMT with bi-layer $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ (5/5 – nm) gate dielectric layers.

Subsequently, a 5 nm-thick Al_2O_3 film was deposited at 300°C using an Oxford Instrument OpAL ALD system with TMA and H_2O precursors followed by deposition of a 5 nm-thick Si_3N_4 film by PECVD. Subsequently a

0.3 μm gate foot-print was formed using electron beam lithography followed by Ni/Au (50/400-nm) gate metallization by E-beam evaporation [96]. Finally, the devices were passivated with a 120 nm-thick PECVD grown Si_3N_4 . The cross-sectional HR-TEM image of the fabricated MISHEMT is shown in Fig. 3.6 and the inset shows the zoomed-in image of the 5/5 nm-thick $\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ dielectric gate stack. The measured dielectric layer thicknesses are in good agreement with the designed thicknesses.

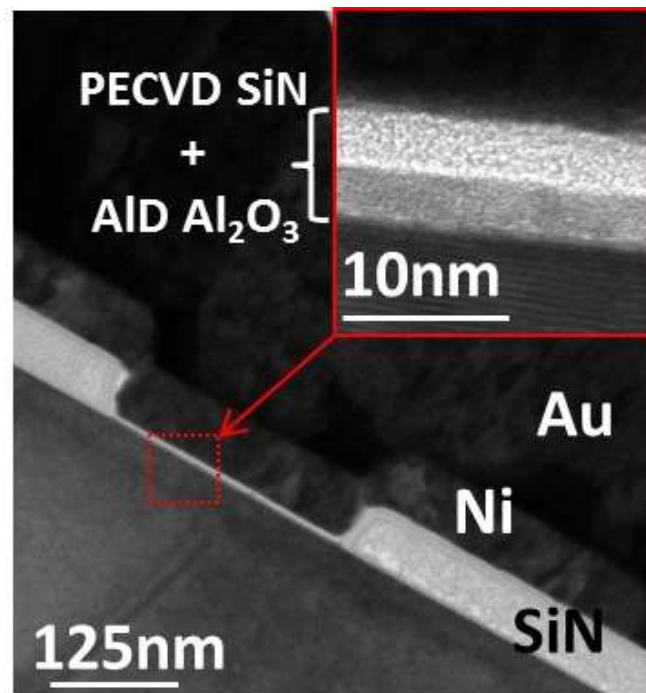


Figure 3.6 Cross-sectional HR-TEM image showing the gate region of AlGaIn/GaN MISHEMT. Inset: Zoomed-in HR-TEM of dielectric stack thickness.

Chapter 4

OFF-state stress in AlGa_N/Ga_N HEMTs

Dynamic ON-resistance ($\text{dyn-}R_{\text{DS[ON]}}$) degradation is one of the most crucial issues that affects the performance of high-power AlGa_N/Ga_N HEMTs. In this work, we focus on the influence of high-peak electric field on the $\text{dyn-}R_{\text{DS[ON]}}$ of AlGa_N/Ga_N HEMTs on Si through pulsed current-voltage ($I_{\text{D}}-V_{\text{D}}$) and transconductance (g_{m}) dispersion measurements, current-transient measurements and two-dimensional transient numerical analysis simulations. We present a unique approach towards the analysis of current collapse by treating the dispersion in the linear and the saturation region of pulsed $I_{\text{D}}-V_{\text{D}}$ output characteristics as two separate events. The device gate to drain spacing (L_{gd}) has been used as a measure to control the peak electric field under OFF-state stress conditions in this study. We show that the high-peak electric fields promote trapping in the extrinsic gate-drain access region causing $\text{dyn-}R_{\text{DS[ON]}}$ degradation whereas a threshold voltage (V_{th}) shift is observed under similar bias conditions but with lower peak electric fields. The traps responsible for current collapse have been detected through the temperature-dependent current-transient measurements. Finally the 2-D numerical simulations have been performed to analyse and support our claim.

4.1 Introduction

Though various research groups have demonstrated excellent performances of AlGa_N/Ga_N HEMTs on Si [122][123], reliability issues such as current collapse [53][124] and dyn- $R_{DS[ON]}$ degradation [53][125] still persist. For high-voltage switching operations, it is very important to have control over dyn- $R_{DS[ON]}$ of the device [126]. By employing multiple field-plates, R. Chu et al [127] demonstrated a low dyn- $R_{DS[ON]}$ /stat- $R_{DS[ON]}$ ratio (1.6 at 600 V) in normally-off AlGa_N/Ga_N MISHEMTs on Si. S. Huang et al [128] reported a reduction in dyn- $R_{DS[ON]}$ degradation in AlGa_N/Ga_N HEMTs by AlN passivation. We have reported low dyn- $R_{DS[ON]}$ (0.58 m Ω -cm²) in AlGa_N/Ga_N HEMTs by ammonium-sulphide [(NH₄)₂S_x] treatment followed by Si₃N₄ passivation [36].

Even though a steady improvement in the device performances have been reported, problems such as current collapse, especially under high-voltage operations still persist. The optimization of the gate to drain access region which is subject to high electric fields is very vital. High electric field stress to the device induces both temporary and permanent current collapse due to electron trapping and mechanical strain in Ga_N HEMTs [129]. Under OFF-state bias conditions, strong reverse electric fields prevail between the gate and the drain terminals. The large concentration of electric fields in the drain-side gate-edge results in the injection of electrons which get trapped at the passivation/AlGa_N interface and within the heterostructure. G. Meneghesso et al [130] investigated the high electric field reliability and the role of surface/bulk traps by analysing the threshold-voltage shift (ΔV_{th}) and increase of access-resistance in un-passivated AlGa_N/Ga_N HEMTs on SiC.

Both surface and bulk traps are found to be contributing to the current degradation due to high electric field.

4.2 Device DC and Breakdown Characteristics

The device heterostructure and fabrication details are given in Chapter 3. For DC characterization, breakdown measurements and high voltage stress studies, we used devices with dimensions of $W_g/L_{sg}/L_g/L_{gd} = 80/2/2/(2, 4, 6, 8, 10) \mu\text{m}$. The DC characterization was performed on a Keithley 4200 source meter. Figure 4.1 shows (a) $I_D - V_D$ and (b) transfer characteristics of AlGaIn/GaN HEMTs with device L_{gd} of 2, 6 and 10 μm . The devices exhibited a consistent maximum drain current density ($I_{D\text{max}}$), maximum extrinsic transconductance ($g_{m,\text{max}}$) and threshold voltage (V_{th}) values of $\approx 450 \text{ mA/mm}$, $\approx 158 \text{ mS/mm}$, and $\approx -2.3 \text{ V}$, respectively.

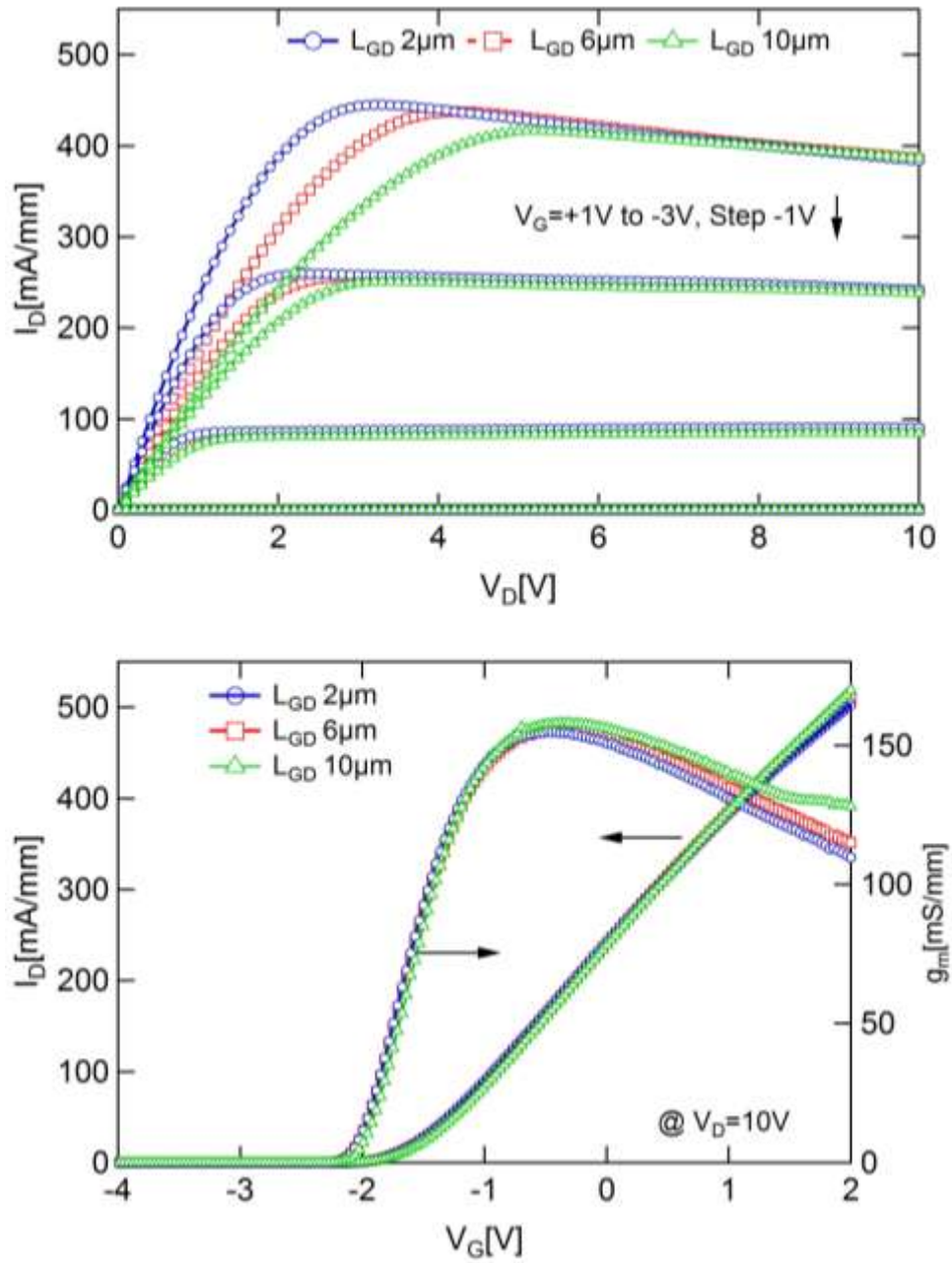


Figure 4.1 (a) I_D - V_D and (b) transfer characteristics of AlGaIn/GaN HEMTs on Si. Device Dimensions: $L_{sg}/L_g/W_g = 2/2/80\text{ }\mu\text{m}$; $L_{gd} = (2, 6, 10)\text{ }\mu\text{m}$.

Three terminal OFF-state BV_{GD} characteristics of AlGaN/GaN HEMTs was measured as a function of device L_{gd} . For the measurements, the V_G was maintained at a sub-threshold voltage of -5 V. The source terminal was grounded all through the measurements. During the BV_{GD} measurements, the samples were immersed in Fluorinert™ (FC-40) to avoid any atmospheric surface flashover at the gate-drain access region.

Figure 4.2 shows (a) three-terminal OFF-state BV_{GD} and (b) substrate-leakage current-voltage characteristics of AlGaN/GaN HEMTs for different L_{gd} . The BV_{GD} of the devices with L_{gd} 2, 4, 6, 8 and 10 μm were 138 V, 285 V, 451 V, 642 V and 672 V, with an $R_{DS[ON]}$ of 0.34, 0.5, 0.69, 0.92 and 1.17 $\text{m}\Omega\cdot\text{cm}^2$ respectively.

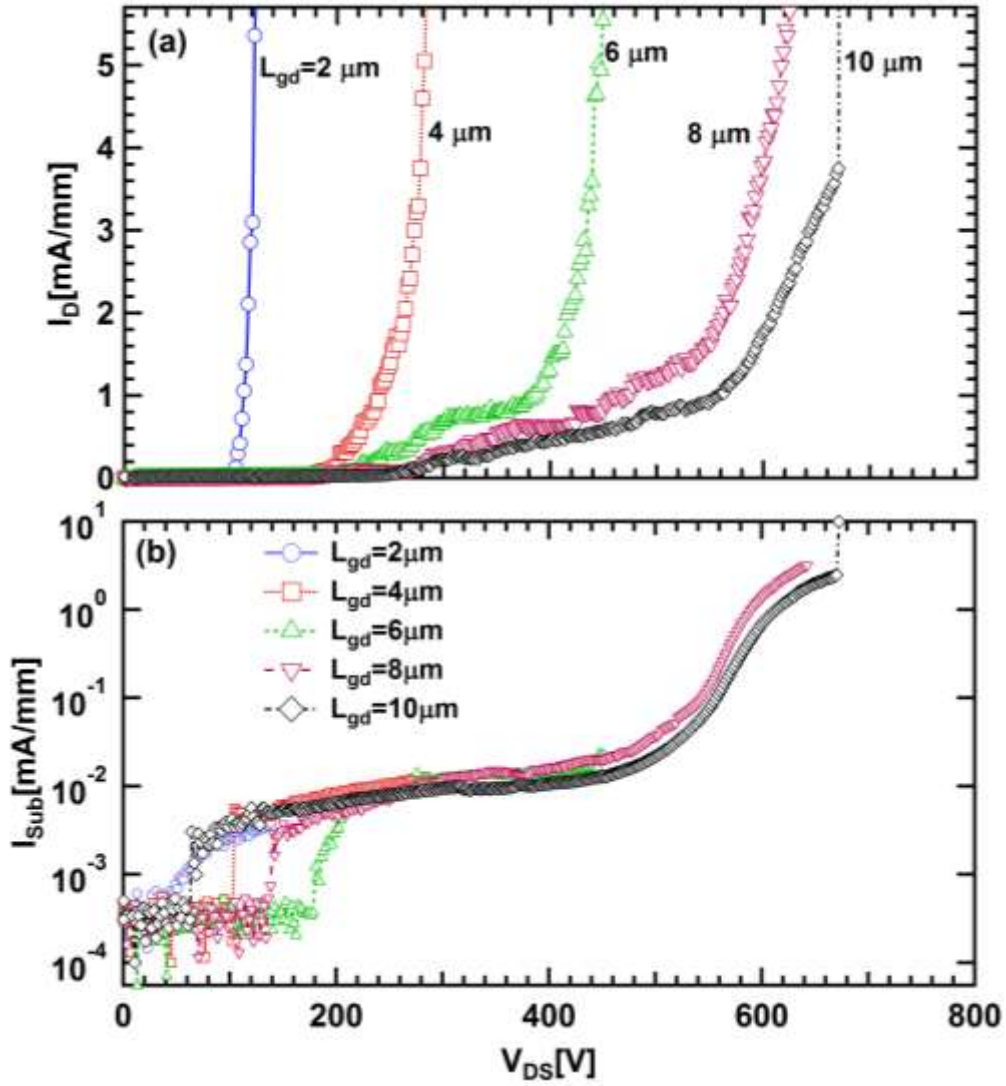


Figure 4.2 (a) Three terminal OFF-state BV_{GD} (b) substrate leakage characteristics ($@V_g = -5V$) of AlGaIn/GaN HEMTs on Si. Device Dimensions: $L_{sg}/L_g/W_g = 2/2/80 \mu\text{m}$; $L_{gd} = (2, 4, 6, 8 \text{ \& } 10) \mu\text{m}$.

Figure 4.3 (a) shows the I_{Dmax} , g_{mmax} and BV_{GD} of AlGaIn/GaN HEMTs with different L_{gd} . The BV_{gd} increased linearly for devices with L_{gd} up to $8 \mu\text{m}$. Figure 4.3 (b) shows $R_{DS[ON]}$ and the power device figure-of-merit (FOM) as a function of the device L_{gd} . The GaN HEMTs with $L_{gd} = 8 \mu\text{m}$ and $10 \mu\text{m}$ exhibited a BV_{GD} of 640 and 670 V with $R_{DS[ON]} = 0.92$ and $1.17 \text{ m}\Omega\cdot\text{cm}^2$, respectively. The FOM ($BV_{GD}^2/R_{DS[ON]}$) is as high as $4.45 \times 10^8 \text{ V}^2\Omega^{-1}\text{cm}^{-2}$.

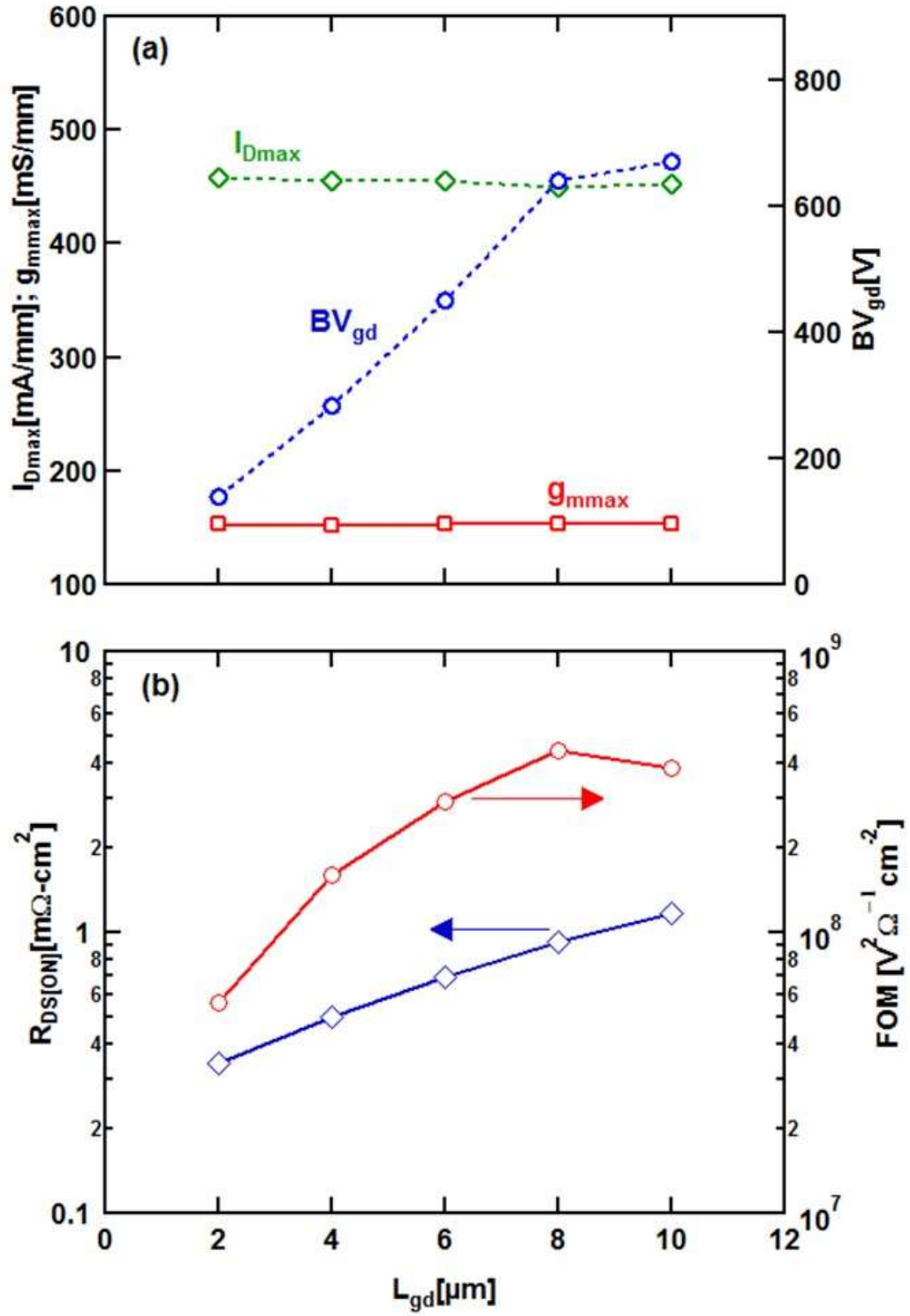


Figure 4.3 (a) I_{Dmax} , g_{mmax} and BV_{GD} for different L_{gd} , (b) $R_{DS(on)}$ and power FOM of AlGaIn/GaN HEMTs on Si. Device dimensions for static- $R_{DS(on)}$: $L_{sg}/L_g/W_g = 2/2/80 \mu m$; $L_{gd} = (2, 4, 6, 8 \text{ \& } 10) \mu m$.

However, for the device with $L_{gd} = 10 \text{ }\mu\text{m}$, the $B V_{gd}$ tends to saturate as the buffer/substrate leakage current begins to dominate as shown in Fig 4.2 (b). The obtained breakdown strength of AlGaIn/GaN HEMTs from the slope is $\sim 0.8 \text{ MV/cm}$ [see Fig. 4.3 (a)]. The $B V_{GD}$ is limited due to the thin GaN buffer layer ($2.2 \text{ }\mu\text{m}$). Enhanced $B V_{GD}$, even beyond 1.4 kV can be achieved without affecting the $R_{DS[ON]}$ by optimizing the buffer GaN thickness from $2.2 \text{ }\mu\text{m}$ to $6 \text{ }\mu\text{m}$ [53][127][129]. In the case of GaN HEMTs and other field effect devices, under high gate to drain reverse bias condition, the breakdown is initiated by electron current underneath the depletion region through the insulating GaN-buffer layer. This process is known by various terms such as space charge injection of electrons into the GaN buffer layer [131], carrier spill-over [132] or buffer layer punch-through effect [133][134]. Due to the punch-through of electrons into the buffer layer, there is a sharp increase of sub-threshold drain leakage current which subsequently leads to device breakdown.

4.3 Pulsed I_D - V_D characteristics

The pulsed I_D - V_D characterization was performed on an Accent Diva D260 dynamic I – V analyser. For pulsed I_D - V_D measurements, we used devices with dimensions of $W_g/L_{sg}/L_g/L_{gd} = (2 \times 100)/1/2/2 \text{ } \mu\text{m}$. Pulsed I_D - V_D measurements were performed on the device to study the current collapse characteristics under OFF-state stress conditions. A gate-lag Q-bias condition of $(V_{Gso}, V_{Dso}) = (-5, 0) \text{ V}$ and gate- and drain-lag Q-bias condition of $(V_{Gso}, V_{Dso}) = (-5, 30) \text{ V}$ were used for this study. The pulse width and pulse separation were 200 ns and 1 ms, respectively. The pulsed I_D - V_D characteristics measured under $(-5, 0) \text{ V}$ and $(-5, 40) \text{ V}$ Q-bias conditions are shown in Fig. 4.4 (a) and (b) for devices with $L_{gd}=2$ and $5 \text{ } \mu\text{m}$, respectively and compared with the corresponding cold Q-bias condition of $(0, 0) \text{ V}$. Under the gate-lag condition $(-5, 0) \text{ V}$, both devices exhibited $\sim 3\%$ current collapse as measured at the saturation region ($V_D = 8 \text{ V}$). The $\text{dyn-}R_{DS[ON]}$ degradation was also minimal for both the devices.

Since the samples were subjected to $(\text{NH}_4)_2\text{S}_x$ treatment followed by Si_3N_4 passivation [121], the surface states in the gate drain access region were well mitigated and the devices exhibited negligible virtual gate effect [100]. However, under the gate- and drain-lag condition, the current collapse and the $\text{dyn-}R_{DS[ON]}$ degradation was different for both the devices. The device with $L_{gd} = 5 \text{ } \mu\text{m}$ exhibited a higher percentage (16%) current collapse in the saturation region ($V_D = 8 \text{ V}$) compared to that of the device with $L_{gd} = 2 \text{ } \mu\text{m}$ which suffered a current collapse of only 8%. The presence of large current

collapse only under the gate- and drain-Q-bias condition is attributed to trapping of electrons in the AlGaIn barrier layer or GaN buffer layer.

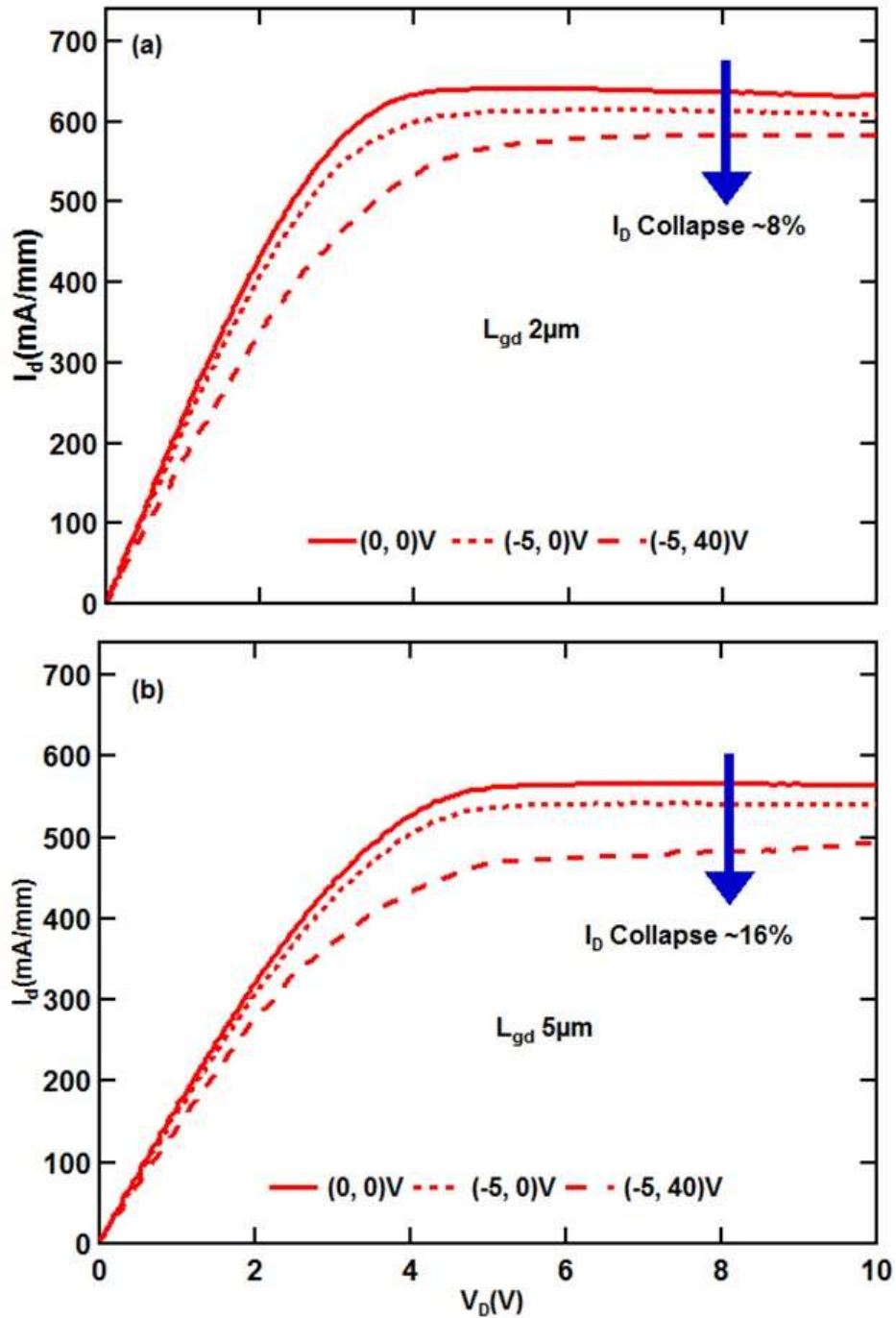


Figure 4.4 Pulsed I_d - V_d characteristics measured at Q-bias conditions $(-5, 0)V$ and $(-5, 40)V$ for HEMTs with (a) $L_{gd} = 2 \mu m$, and (b) $L_{gd} = 5 \mu m$. Device Dimensions: $L_{sg}/L_g/W_g = 1/2/(2 \times 100) \mu m$.

Furthermore, the pulsed transfer (g_m - V_G) characteristics were measured to study the location of the trapping of electrons. Figures 4.5 (a) and (b) show the pulsed (pulse-width/pulse-separation = 200 ns /1 ms) g_m - V_G characteristics at (-5, 40) V Q-bias condition for HEMTs with L_{gd} =2 and 5 μ m, measured at V_D = 3 V and 8 V which correspond to the linear and saturation regions, respectively, with reference to the pulsed I_D - V_D characteristics. The HEMTs with L_{gd} = 2 μ m exhibited a higher g_m -dispersion of ~15% for V_D = 3 V, whereas the g_m -dispersion for V_D = 8 V was negligible. However, an overall ΔV_{th} of ~120 mV was observed. The HEMTs with L_{gd} = 5 μ m, exhibited a much lower g_m -dispersion (~5%) under both the V_D conditions, but a large ΔV_{th} of ~380 mV was observed.

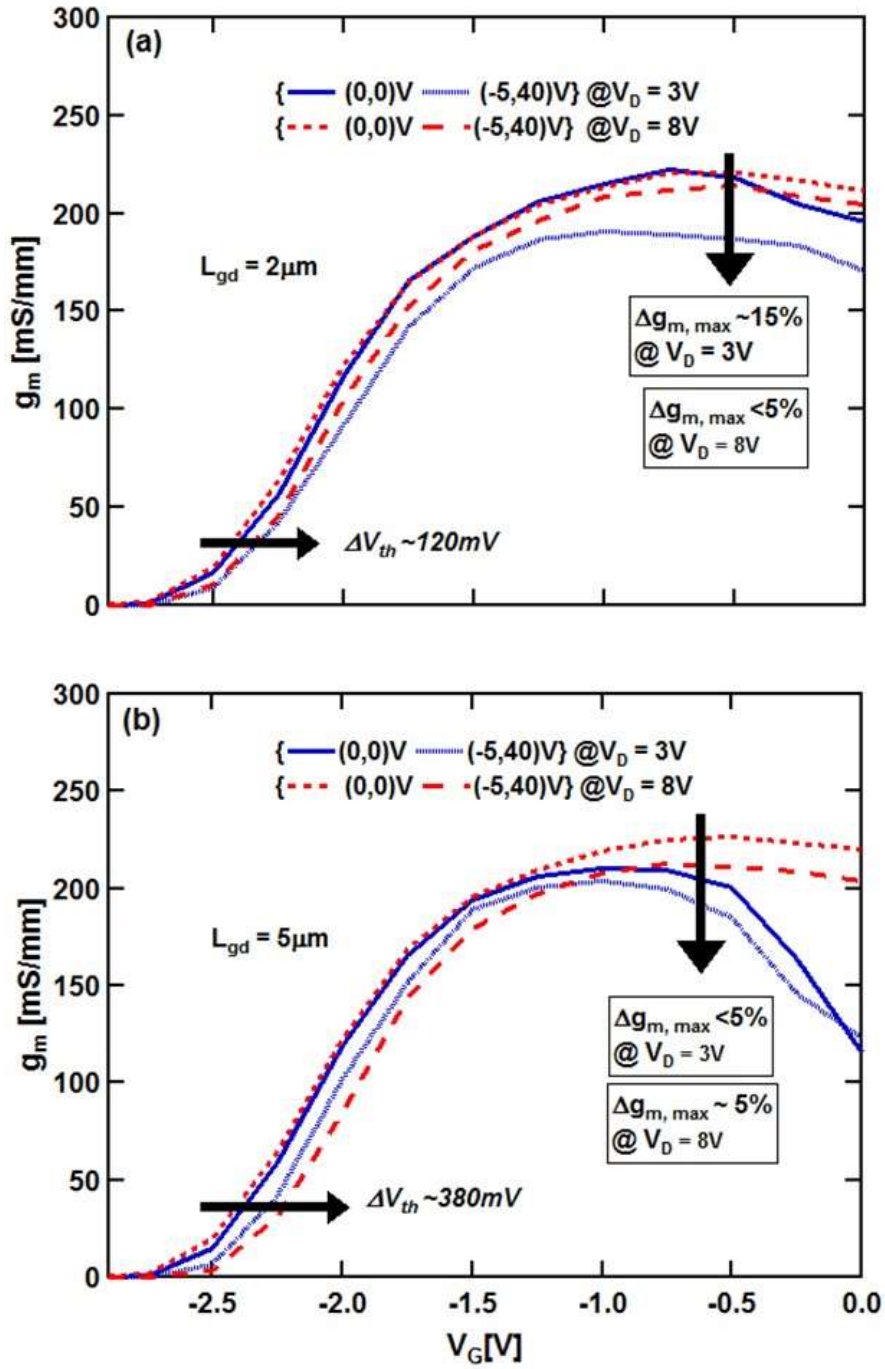


Figure 4.5 Pulsed g_m - V_g characteristics at $(0, 0)$ V and $(-5, 40)$ V for HEMTs with (a) $L_{gd} = 2 \mu\text{m}$, (b) $L_{gd} = 5 \mu\text{m}$; measured at $V_D = 3$ V and 8 V respectively. Device Dimensions: $L_{sg}/L_g/W_g = 1/2/(2 \times 100) \mu\text{m}$.

4.4. Influence of Electric-Field on the location of trapping

To understand the trap dynamics, pulsed I_D-V_D measurements were performed at different pulse-widths and fixed pulse-separation. Figure 4.6 (a) shows the current collapse (ΔV_{th}) and the $\text{dyn-}R_{DS[ON]}/\text{stat-}R_{DS[ON]}$ ratio of HEMTs as a function of device L_{gd} under (-5, 40) V Q-bias for pulse-widths: 0.2 μs and 10 μs . The current collapse (ΔV_{th}) increased with increasing L_{gd} . Under 0.2 μs pulse-width range, devices with $L_{gd} = 2$ and 5 μm exhibited a current collapse of 8% and 16%, respectively in the saturation region ($V_D = 8$ V). Increase of current collapse with increasing L_{gd} was attributed to L_{gd} dependent trapping effects by Lee et al [135]. However, the $\text{dyn-}R_{DS[ON]}$ degradation exhibited an opposite trend with increasing L_{gd} .

Figure 4.6 (b) shows the $\text{dyn-}R_{DS[ON]}/\text{stat-}R_{DS[ON]}$ ratio of HEMTs with $L_{gd} = 2, 3, 4$ and 5 μm under (-5, 40) V Q-bias for pulse-widths: 0.2 μs to 10 μs . All devices exhibited smaller $\text{dyn-}R_{DS[ON]}$ degradation ($\text{dyn-}R_{DS[ON]}/\text{stat-}R_{DS[ON]} \sim 1.04$) in the longer pulse-width (≥ 2 μs) range. However, in the shorter pulse-width (< 2 μs) range, the HEMTs with $L_{gd} = 2$ and 3 μm exhibited larger $\text{dyn-}R_{DS[ON]}$ degradation ($\text{dyn-}R_{DS[ON]}/\text{stat-}R_{DS[ON]} \sim 1.27$).

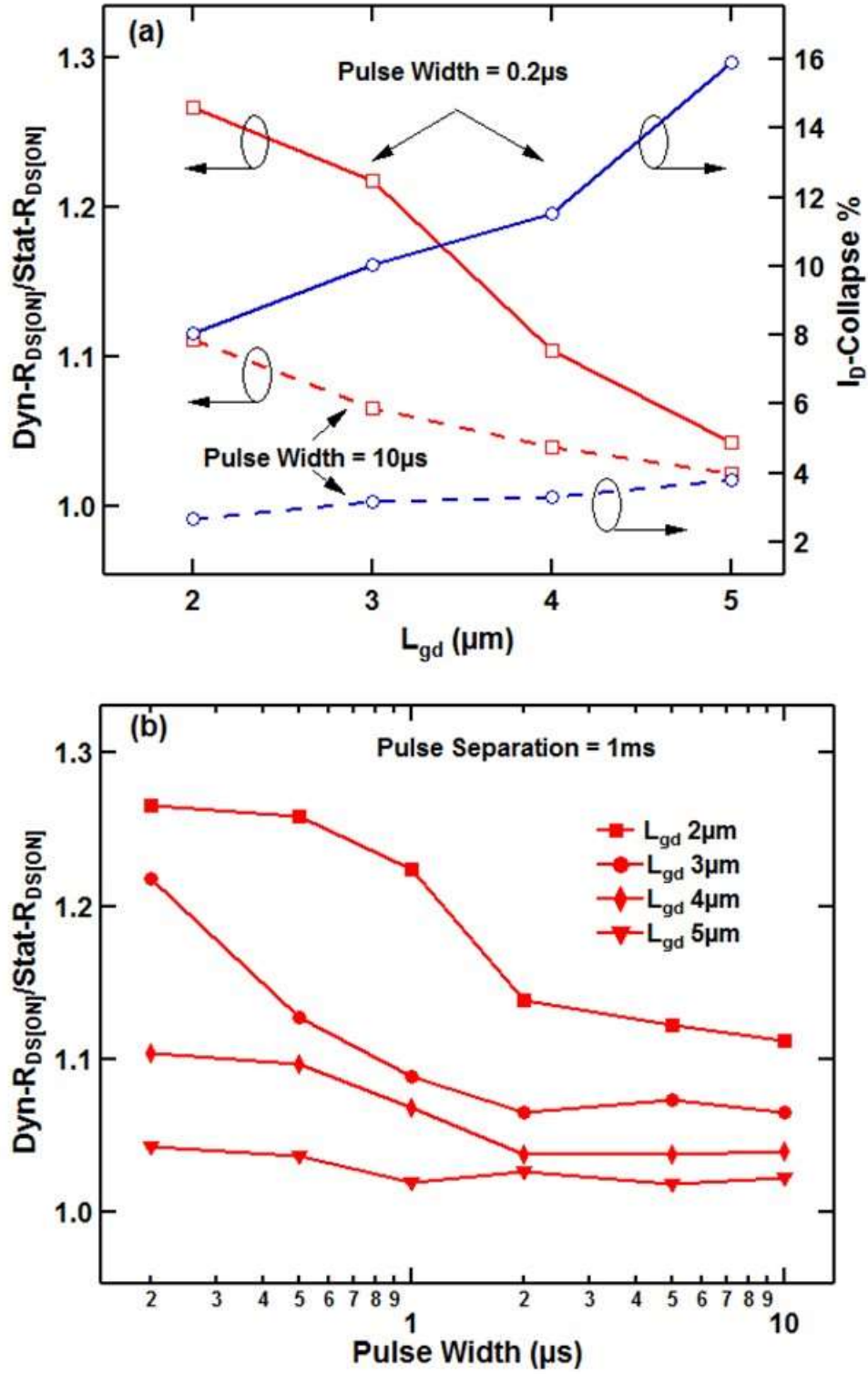


Figure 4.6 (a) $\text{Dyn-}R_{\text{DS[ON]}}/\text{Stat-}R_{\text{DS[ON]}}$ ratio for devices of $L_{\text{gd}} = 2$ to $5 \mu\text{m}$ measured at different pulse-widths, (b) $\text{Dyn-}R_{\text{DS[ON]}}/\text{Stat-}R_{\text{DS[ON]}}$ ratio and current collapse as a function of device L_{gd} under $(-5, 40) \text{ V}$ Q-bias for pulse-widths $0.2 \mu\text{s}$ and $10 \mu\text{s}$. Device Dimensions: $L_{\text{sg}}/L_{\text{g}}/W_{\text{g}} = 1/2/(2 \times 100) \mu\text{m}$.

This increase of dyn- $R_{DS[ON]}$ degradation for smaller L_{gd} devices can be attributed to increased trapping due to activation of additional trapping centres caused by high electric field in the gate-drain region [56]. This behaviour follows the Poole-Frenkel field-dependent emission process where the rate of electron detrapping from the traps experiencing high electric field substantially increase due to potential barrier lowering given by:

$$\Delta\phi_{PF} = \left(\frac{q^3}{\pi\epsilon}\right)^{1/2} \sqrt{EF} \quad (1)$$

where q is the electronic charge and ϵ is the dielectric constant of AlGaN. Also, the rate-of-change of the dyn- $R_{DS[ON]}$ /stat- $R_{DS[ON]}$ ratio with pulse-width is very high for devices with smaller L_{gd} [Fig. 4.6(b)]. This corresponds to the exponential increase in electron emission rate $[e(EF)]$ from the traps with the square-root of electric field (EF) given by:

$$e(EF) = e(0)\exp\left(\frac{\Delta\phi_{PF}}{kT}\right) \quad (2)$$

To further investigate the source and the mechanism of trapping of electrons, temperature-dependent current-transient measurements have been performed on devices with $L_{gd} = 2$ and $6 \mu\text{m}$.

4.5 Temperature-dependent current-transients

Using the detrapping drain current-transient measurement technique, we performed trap characterization of the GaN HEMTs with $L_{gd} = 2$ and $6 \mu\text{m}$. The devices were stressed with a filling pulse of $V_G = -5 \text{ V}$ and $V_D = 40 \text{ V}$ for 1000 ms . After the OFF-state stress, the detrapping signals were measured by fully turning ON the 2DEG channel with a gate bias of $V_G = 0 \text{ V}$ and the drain voltage to $V_D = 1.5 \text{ V}$. The detrapping signals were recorded from a time of $100 \mu\text{s}$ onwards. The $V_D = 1.5 \text{ V}$ was chosen to eliminate the influence of self-heating effects during measurements.

The opposite trend in the current collapse for the devices with smaller and longer L_{gd} in the linear and the saturation region [as shown in Fig. 4.6 (a)] was also validated using the current-transient measurements. For this purpose, after the OFF-state stress of $(V_G, V_D) = (-5, 40) \text{ V}$ for 1000 ms , the detrapping current-transients were measured at a $V_G = 0 \text{ V}$ and $V_D = 1.5 \text{ V}$, corresponding to the linear region, and $V_D = 4 \text{ V}$, corresponding to the saturation region for HEMTs with $L_{gd} = 2$ and $6 \mu\text{m}$. The transient response measured after the OFF-state stress is shown in Fig. 4.7 (a) and (b) measured at $(V_G, V_D) = (0, 1.5) \text{ V}$ corresponding to the linear region; (c) and (d) measured at $(V_G, V_D) = (0, 4) \text{ V}$ corresponding to the saturation region for HEMTs with $L_{gd} = 2$ and $6 \mu\text{m}$, respectively. It can be seen that the HEMT with $L_{gd} = 2 \mu\text{m}$ suffers larger current collapse when measured at $(V_G, V_D) = (0, 1.5) \text{ V}$, whereas the HEMT with $L_{gd} = 6 \mu\text{m}$ suffers larger current collapse when measured at $(V_G, V_D) = (0, 4) \text{ V}$.

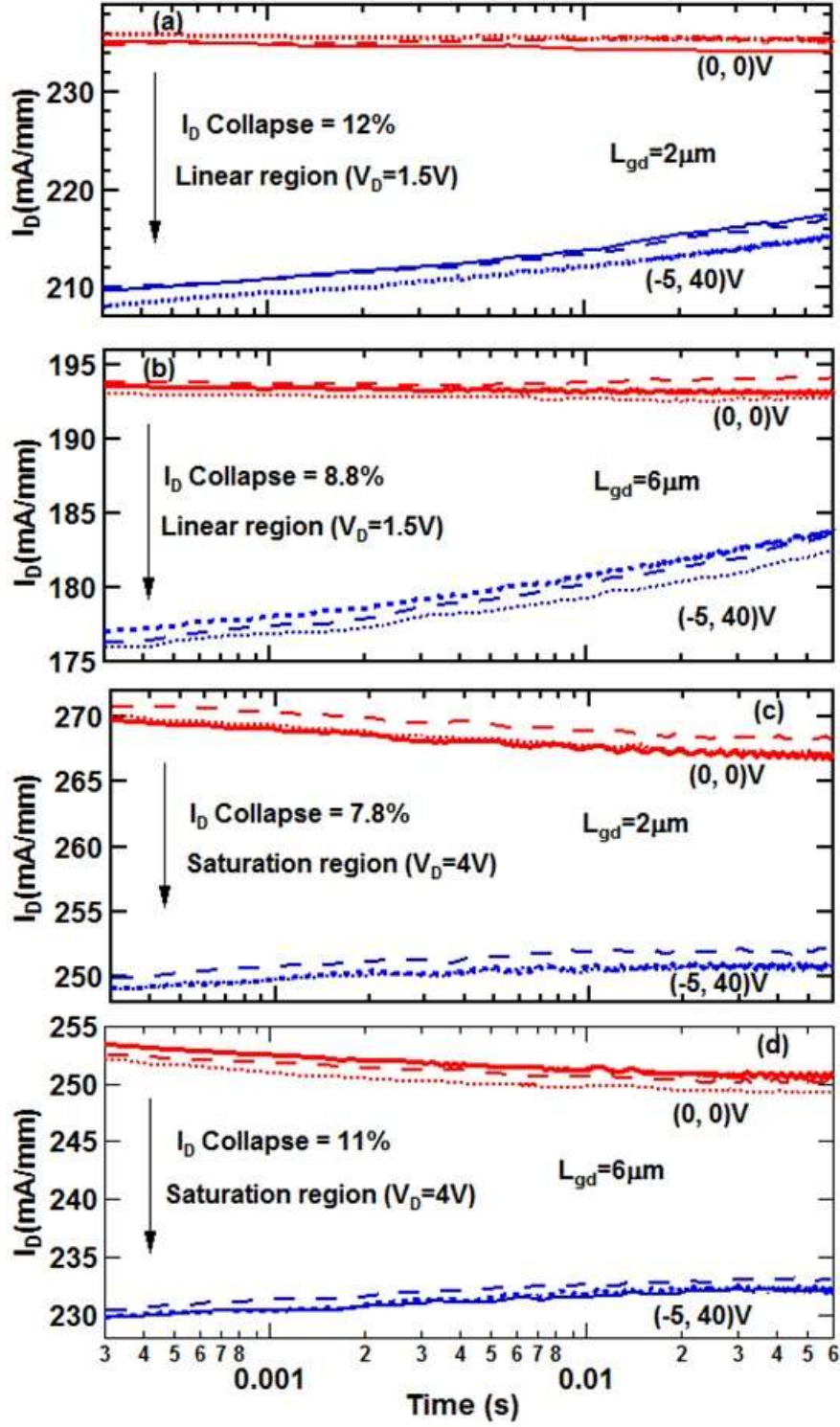


Figure 4.7 Current-transients obtained after a 1000 ms OFF-state stress of $(V_G, V_D) = (-5, 40)$ V for HEMTs with (a) $L_{gd} = 2 \mu\text{m}$, (b) $L_{gd} = 6 \mu\text{m}$, measured at $(V_G, V_D) = (0, 1.5)$ V, and (c) $L_{gd} = 2 \mu\text{m}$, (d) $L_{gd} = 6 \mu\text{m}$, measured at $(V_G, V_D) = (0, 4)$ V.

This is analogous to that shown in Fig. 4.6 (a) and (b). However further measurements were carried out at $(V_G, V_D) = (0, 1.5)$ V in order to mitigate the influence of self-heating on the transient response [136]. The I_D -transients response (normalized to final steady-state value) measured at room temperature for devices with $L_{gd} = 2$ and $6 \mu\text{m}$ are shown in Fig. 4.8 (a). The transient response of both the devices shows a similar pattern signifying a detrapping process from the same trap energy level. Figure 4.8 (b) shows the current-transients of AlGaIn/GaN HEMTs with $L_{gd} = 6 \mu\text{m}$ at different measurement temperatures. A clear increase in the current collapse and as well a decrease in the emission time signature is observed with the increase in temperature.

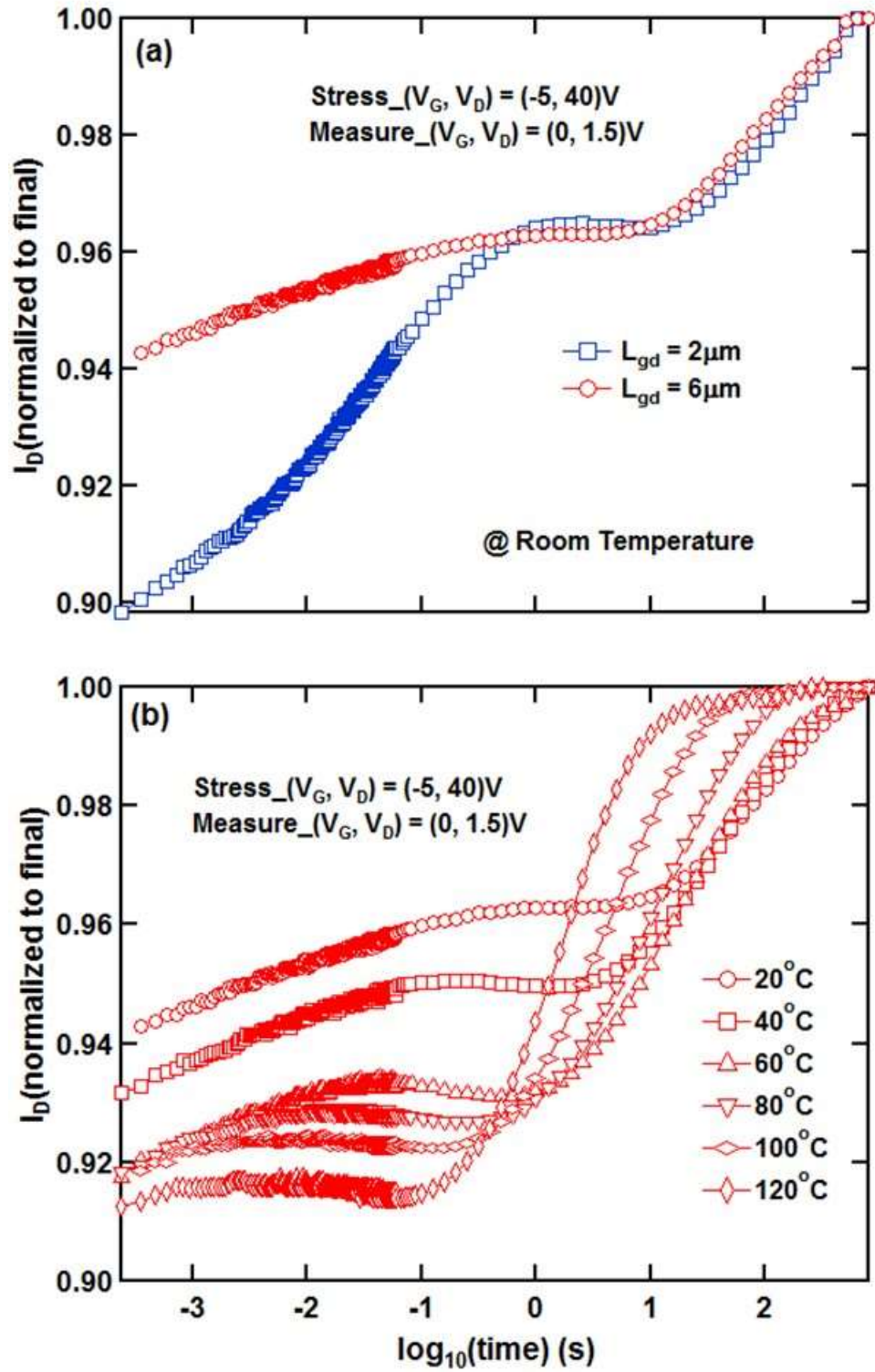


Figure 4.8 Current-transients (normalized) after an OFF-state stress of $(V_G, V_D) = (-5, 40) \text{V}$ for HEMTs with (a) $L_{gd} = 2$ and $6 \mu\text{m}$, (b) Temperature-dependent current-transients for HEMTs with $L_{gd} = 6 \mu\text{m}$.

Figure 4.9 (a) and (b) shows the corresponding differentials of the current-transient signals for devices with $L_{gd} = 2$ and $6 \mu\text{m}$, respectively. Both devices exhibited a thermally activated detrapping time constant. Using the Arrhenius analysis, an activation energy (E_a) of 0.33 ± 0.05 eV with a capture cross-section of $1.2 \times 10^{-20} \text{cm}^2$ was obtained. Figure 4.9 (c) shows the Arrhenius plot for both the devices. The observed trap with $E_a = 0.33$ eV is commonly accepted to be located in AlGaIn barrier [137][138]. The obtained trap information was used for further analysis through TCAD numerical simulations.

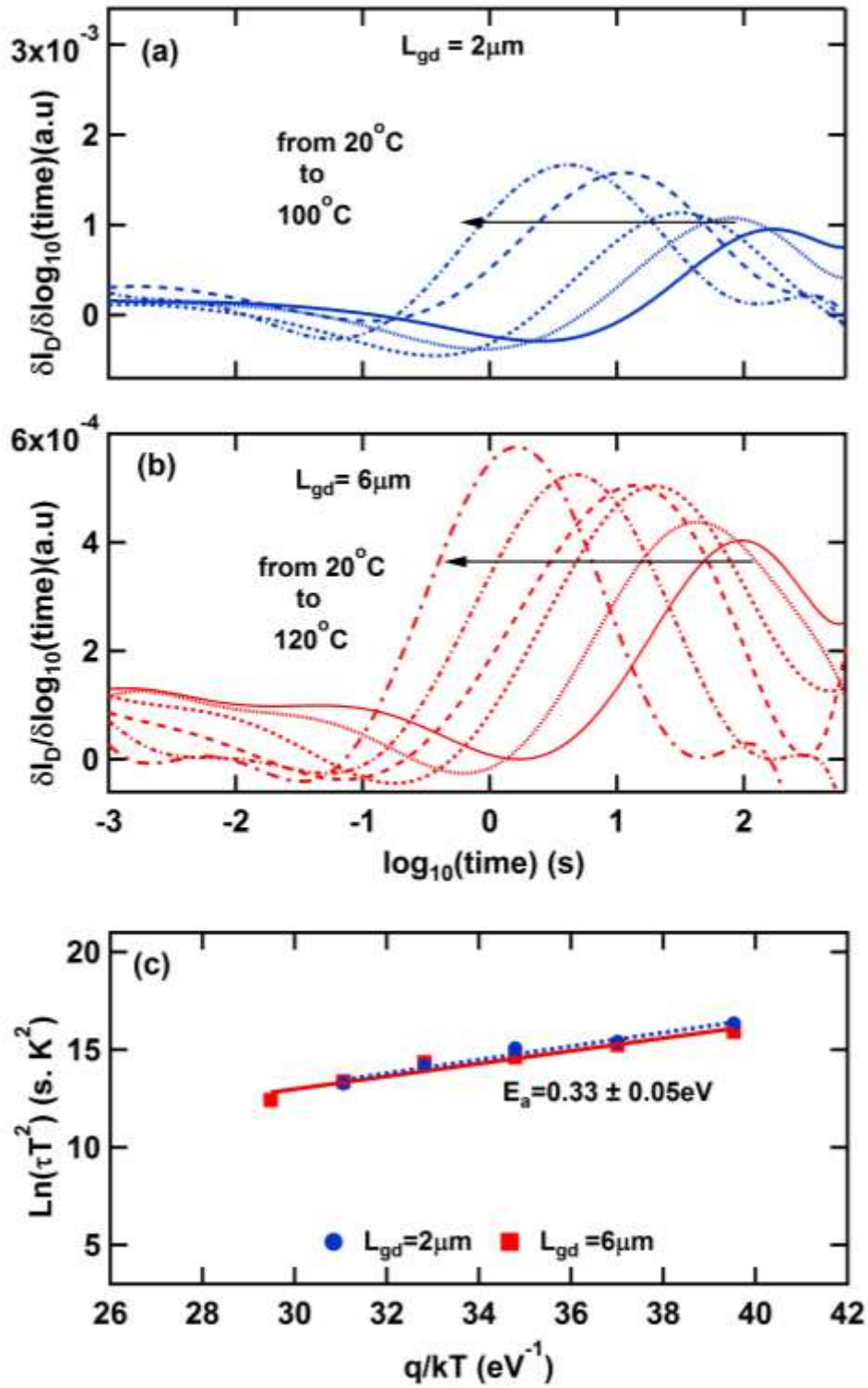


Figure 4.9 Temperature-dependent current-transient for HEMTs with $L_{gd} = 6 \mu\text{m}$. The related differential signals for device with (a) $L_{gd} = 2 \mu\text{m}$, (b) $L_{gd} = 6 \mu\text{m}$ and (c) Arrhenius plot.

4.6 TCAD 2D numerical simulations of the electrical field dependent trapping mechanism

For further confirmation, the 2-D transient simulations were performed using Silvaco TCAD. An additional differential rate equation was solved for simulating the emission and capture processes. The experimentally determined trap parameters were incorporated into the model. No fixed charges or traps were defined in the $\text{Si}_3\text{N}_4/\text{AlGa}\text{N}$ interface because, no significant trapping was observed due to the surface related trapping phenomenon under the gate-lag measurements based on the pulsed I_D - V_D characterization. Since our devices had gone through $[(\text{NH}_4)_2\text{S}_x]$ treatment followed by SiN passivation [121], the surface related trapping effects were significantly mitigated. Similarly, an OFF-state stress of $(V_G, V_D) = (-5, 40)$ V was applied for 1000 ms.

The simulated current-transients ($I_D/I_{D\text{max}}$) for HEMTs with $L_{\text{gd}}=2$ and $5\mu\text{m}$ in the linear region [$V_D = 3$ V] and the saturation region [$V_D = 8$ V] are shown in Fig. 4.10 (a) and (b), respectively. From the simulations, the current collapse in the linear and saturation region for device with $L_{\text{gd}} = 2 \mu\text{m}$ is 12% and 7%, respectively; and for HEMTs with $L_{\text{gd}} = 5 \mu\text{m}$ is 6% and 11%, respectively. The current collapse trend from the TCAD simulation matches our experimental results. Both simulation and experiment show high current collapse for the device with $L_{\text{gd}}=2 \mu\text{m}$ in the linear region, {represented as $\text{dyn-}R_{\text{DS[ON]}}$ degradation in Fig. 4.6 (a)}, whereas high current collapse in the saturation region for the device with $L_{\text{gd}} = 5 \mu\text{m}$. The opposite trend of current collapse for the devices with $L_{\text{gd}} = 2$ and $5 \mu\text{m}$ is

due to the difference in the distribution of the lateral electric field in the gate-drain access region.

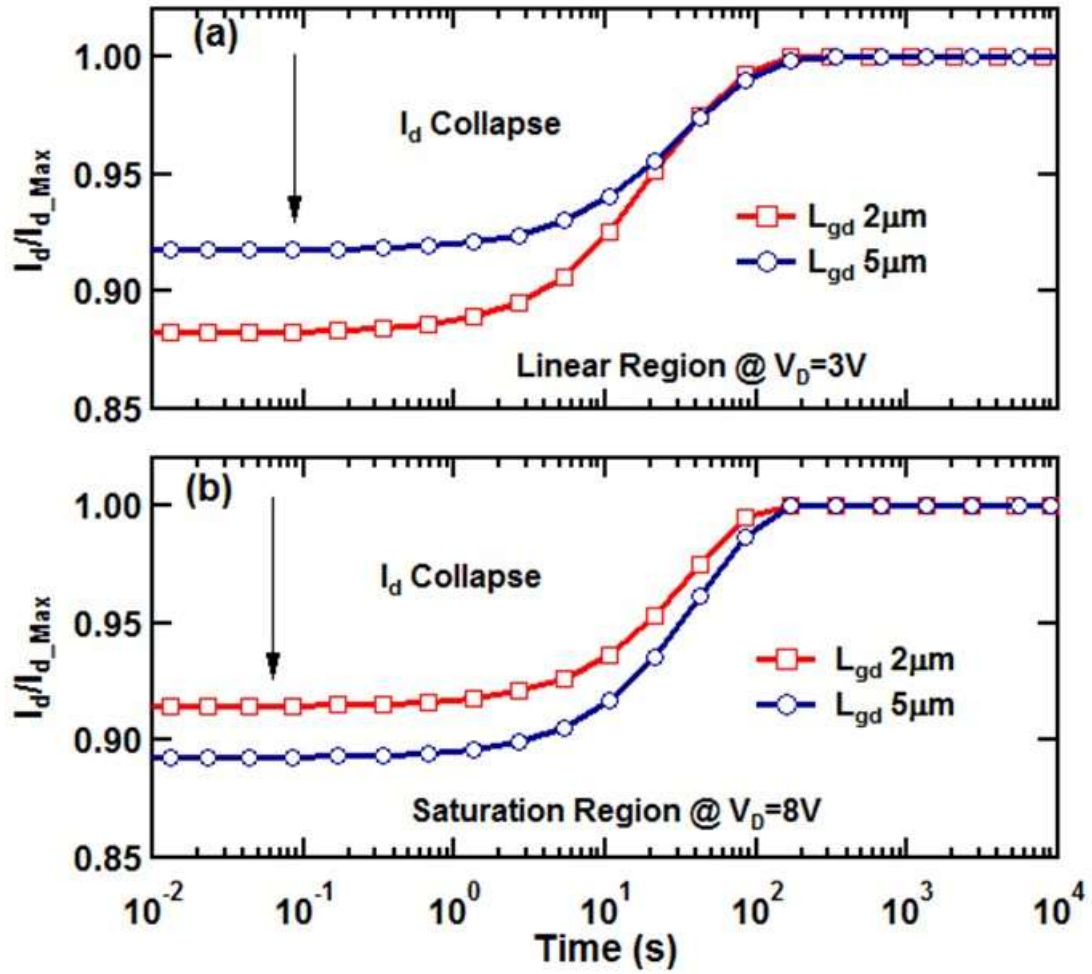


Figure 4.10 2D-transient TCAD simulations (normalized) for AlGaIn/GaN HEMTs with $L_{gd} = 2$ and $5 \mu m$; at (a) linear region ($V_D = 3 V$), (b) saturation region ($V_D = 8 V$).

The simulated average electric field [along the x-axis](#) in the AlGaIn barrier, as a function of device L_{gd} under $(-5, 40) V$ Q-bias is shown in Fig. 4.11 (a). The device with $L_{gd} = 2 \mu m$ ($\sim 3.4 MV/cm$) experiences ~ 2 times higher electric field than the device with $L_{gd} = 5 \mu m$ ($\sim 1.4 MV/cm$). Under negative gate-bias, electrons tunnel through the gate contact barrier [101] into the AlGaIn

barrier by a tunnelling-assisted Poole-Frenkel (TAPF) conduction mechanism [139]. O. Mitrofanov et al [101] reported that the potential-well-height of the trap is lowered by ~ 0.2 to 0.25 eV under the influence of electric field. The difference between the Schottky barrier height (0.61 eV) in the devices-under-test and the reduced potential-well-height closely matches with our experimentally determined E_a (0.33 eV).

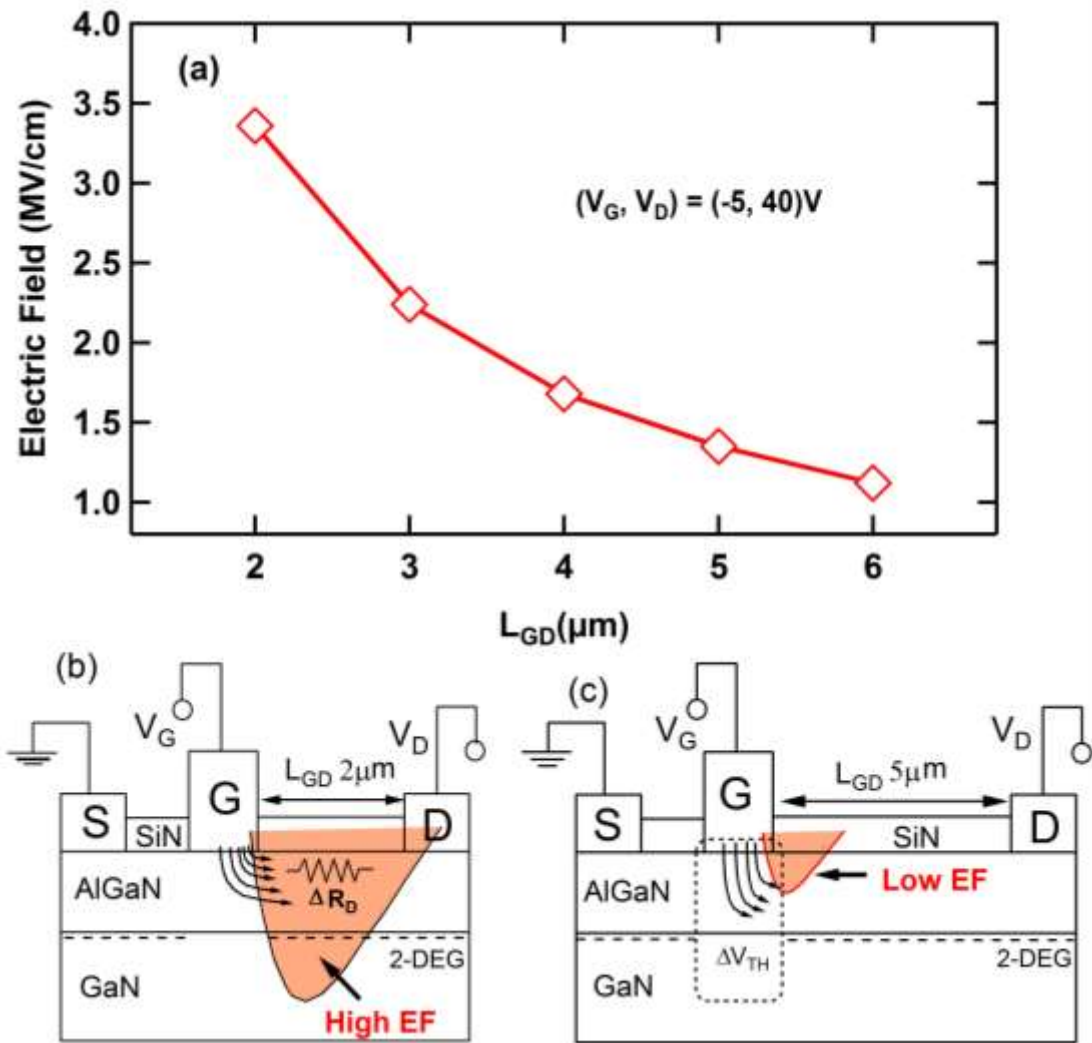


Figure 4.11 (a) Simulated average electric field (EF) in the AlGaIn barrier along the x-axis under $(-5, 40)$ V Q-bias condition for HEMTs as a function of L_{gd} ; Electron injection from gate metal into the AlGaIn barrier under $(-5, 40)$ V Q-bias condition for HEMTs with (b) $L_{gd} = 2 \mu\text{m}$, and (c) $L_{gd} = 5 \mu\text{m}$.

For the device with $L_{gd} = 2 \mu\text{m}$, due to high electric field in the gate-drain access region, the tunnelled gate electrons which faces a higher Coulomb force of attraction, are drawn and trapped in the extrinsic region of the AlGaIn barrier as shown in Fig. 4.11 (b), causing higher $\text{dyn-}R_{DS[ON]}$ degradation. On the contrary, for HEMTs with $L_{gd} = 5 \mu\text{m}$ experiencing low electric field, extent of the tunnelled electrons being drawn and trapped into the gate-drain access region is much lesser. Thus most of the trapping is confined to the AlGaIn barrier directly under the gate as shown in Fig 4.11 (c), resulting in ΔV_{th} . This shows that the electric field plays a vital role in governing the location of electron trapping affecting the $\text{dyn-}R_{DS[ON]}$ or V_{th} of the devices.

4.7 Summary

In conclusion, comprehensive OFF-state stress based trap studies were performed on AlGaIn/GaN HEMTs using pulsed current voltage and temperature-dependent current-transient techniques. The devices exhibited a very low current collapse of $\sim 3\%$ under the gate-lag measurement condition $(-5, 0) \text{ V}$. Since the devices were subjected to $(\text{NH}_4)_2\text{S}_x$ treatment followed by Si_3N_4 passivation [121], trapping due to the surface states in the $\text{Si}_3\text{N}_4/\text{GaN}$ interface at the gate drain access region was well mitigated. However, under the gate- and drain-lag condition, the $\text{dyn-}R_{DS[ON]}$ degradation and current collapse (ΔV_{th}) followed an opposite trend for the devices with $L_{gd} = 2$ and $5 \mu\text{m}$, respectively. This opposite trend in the current collapse is due to the influence of electric field on the location of electron trapping. Under the same OFF-state stress conditions, the HEMTs

with $L_{gd} = 2 \text{ } \mu\text{m}$ suffered larger dyn- $R_{DS[ON]}$ degradation due to increased electron trapping in the gate to drain access region caused by a high electric field; whereas the HEMTs with $L_{gd} = 5 \text{ } \mu\text{m}$ which experiences lower electric field exhibited larger current collapse (ΔV_{th}) due to trapping only under the gate region. The experimental results are found to be in good agreement with the 2-D Silvaco TCAD transient model. The observed anomalies in dyn- $R_{DS[ON]}$ and V_{th} can be mitigated through proper electric field profile engineering and optimized growth conditions, especially in the AlGaIn barrier.

Chapter 5

ON-state stress in AlGaIn/GaN HEMTs

In this chapter, we present trap studies in AlGaIn/GaN HEMTs based on fully ON-state stress conditions. We have used temperature-dependent current-transient characterization for analysing the trap characteristics. Since we have used fully ON-state stress conditions, the obtained trap information is attributed to trap levels present in the GaN buffer. The activation energies (E_a 's) thus obtained from the current-transients exhibited a correlation with the applied stress conditions and increased with the increase of ON-state V_{D_Stress} . We used the multi-trap energy (MTE) model to explain this behaviour and thus propose a distribution of trap energy (DTE) levels in the energy band-gap of buffer GaN. We also propose that the DTE levels result in an effective activation energy (E_{a_eff}), corresponding to the trap energy levels activated by the applied ON-state V_{D_Stress} . We have also validated our observations using the TCAD 2-dimensional numerical simulations.

5.1 Introduction

Even though AlGaN/GaN HEMTs have been reported to show impressive performances in the high-voltage [122] and high-frequency [140] applications, there are still various underlying material based anomalies [53][141] that are yet to be addressed. Optimization of the growth parameters of the AlGaN/GaN heterostructure is in itself a separate area of research. The unintentionally doped GaN buffer contains various defects or trap states [53][141][142], which gives rise to current collapse and other trapping related reliability issues. Numerous techniques are being employed to understand the origin and role of the defects that affect the reliability of the GaN devices.

For highly scaled devices, the choice of the methodology of analysis also becomes very critical. The multi-exponential current-transient technique is reported to be one of the most suitable methods for studying the trap properties in GaN transistors [57][105][130][143]. Most of the reports based on this technique use fully-OFF, semi-ON or fully ON-state bias conditions to study the trapping mechanism. Fully OFF-state stress conditions facilitate the study of surface/barrier related trapping that results in dyn- $R_{DS[ON]}$ degradation and threshold voltage shift [55][130].

In the previous chapter, we have discussed the effects of barrier related trapping in AlGaN/GaN HEMT using OFF-state bias stress and temperature-dependent current-transient measurements. A semi-ON state bias condition resulting in partial depletion of the channel has been adopted to study the buffer related traps [130]. However, the negative bias to the gate electrode

will also induce some surface and barrier related trapping, resulting in both surface/barrier and buffer related components. On the other hand, under fully ON-state stress, when the drain voltage is significantly high, the channel electrons can spill over and gain enough energy at the drain-side gate-edge to reach deep into the GaN buffer [144]. C. -Y. Hu et al [145] reported that even though both surface leakage currents and hot electrons are responsible for the non-localized trapping effects, trapping of hot electrons in the GaN buffer has a dominant effect under fully ON-state stress conditions. This is even more pronounced if the surface related trapping component is suppressed through appropriate surface treatments [140][145]. The energetic electrons which spread [146] into the GaN buffer are trapped by various traps present in the GaN buffer [108][147].

Even though long-hours of ON-state stress result in the generation of interface and surface related traps due to hot electron effects [148][149], the physical origins of the traps have not been distinctly established. Moreover, J. A. del Alamo et al [125] have reported the absence of a hot-electron based degradation signature during their long-time stress tests and attributed “inverse piezoelectric effects” as a possible degradation mode. However, under short period ON-state stress condition, W. D. Hu et al [144] have reported a hot-electron buffer trapping effect. Thus, a short-time ON-state stress condition is a more relevant condition for the study of buffer related traps in AlGaIn/GaN HEMTs [53][150].

By analysing the revival of collapsed current using incident light with varying wavelengths, S. C. Binari et al [108] have reported on the probability

of the presence of DTE-levels. A current collapse model incorporating two distinct trap levels of 1.80 eV and 2.85 eV based on photoionization spectra was proposed by K. B. Klein et al [150]. They have reported that the photoconductivity spectrum of the traps overlap under certain wavelengths used for the photo-induced recovery of the collapsed drain current. However, such photoionization spectral studies are more effective with gateless or semi-transparent gate device structures. A thorough understanding of the DTE-levels in the GaN energy band-gap is still missing for gated devices. In this work, we studied the trapping dynamics under actual device operation conditions involved in AlGaIn/GaN HEMTs by temperature-dependent current-transient measurement technique under different $V_{D[ON]_{Stress}}$ conditions.

We obtained different E_a 's for different $V_{D[ON]_{Stress}}$. The behaviour of the time constants under different $V_{D[ON]_{Stress}}$ conditions at different temperatures will be discussed. In addition, we propose that the obtained effective activation energies ($E_{a_{eff}}$) correspond to different energy levels in the continuous DTE function activated by different $V_{D[ON]_{Stress}}$. This is further verified through TCAD [58] 2-D numerical transient simulations by incorporating the experimentally determined trap parameters.

5.2 Current-transient measurements for ON-state stress conditions

The device heterostructure, fabrication details and device DC characteristics are discussed in Chapter 3 and 4, respectively. The dimensions of the devices used for this study were: $L_{sg}/L_g/W_g/L_{gd} = (2/2/80/6) \mu\text{m}$. The devices exhibited a maximum drain current density of 540 mA/mm, a maximum extrinsic output transconductance of 187 mS/mm and a threshold voltage of -2.5 V. The OFF-state BV_{GD} of the devices were $\approx 640\text{V}$. The device DC, pulsed $I_D - V_D$ and dyn- $R_{DS[ON]}$ characteristics [36], break down and OFF-state stress characteristics are furnished in Chapter 4.

The temperature-dependent current-transient measurements (from 40°C to 120°C, increment of 20°C) under different ON-state V_{D_Stress} conditions were performed using Agilent B1505A power device analyser. Figure 5.1(a) shows the schematic of the AlGaIn/GaN HEMT structure and the trapping of 2DEG channel electrons under high $V_{D[ON]_Stress}$ conditions. The corresponding energy band diagram (cutline position AA'), depicting the downward band-bending as well as the spread of the 2DEG wave function into the GaN buffer region under increasing $V_{D[ON]_Stress}$ conditions is shown in Fig. 5.1(b).

For the measurements, the source terminal was grounded, the gate terminal was biased at (V_{G_Stress}) = 0 V and the drain terminal was stressed at different voltages ($V_{D[ON]_Stress}$) = 10 to 60 V with a step of 10 V. The $V_{D[ON]_Stress}$ or the filling pulse was maintained for a period of 1 s. These biasing conditions

ensure the injection of channel electrons into the various trap levels in the GaN buffer [108][144].

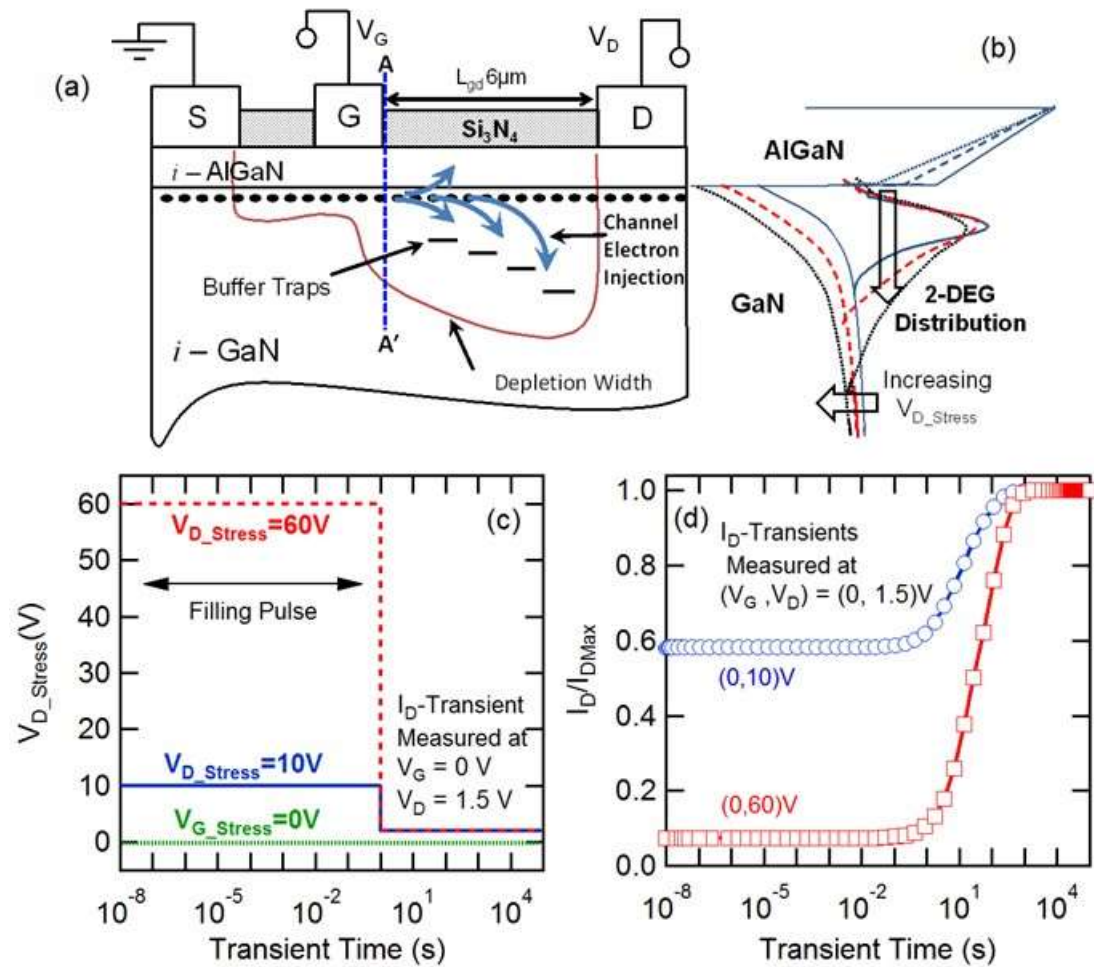


Figure 5.1 (a) Schematic of AlGaN/GaN HEMT structure showing trapping of 2DEG channel electrons at high $V_{D[ON]_{Stress}}$ of (0, 60) V, (b) the Energy band diagram of an AlGaN/GaN heterojunction showing the 2-DEG distribution and band bending under different $V_{D[ON]_{Stress}}$ at the cutline location AA', (c) Time domain representation of $V_{D[ON]_{Stress}}$ for 10 V and 60 V and (d) the corresponding evolution of collapsed current as a function of the transient time.

Consecutively, after the 1 s filling pulse, the current-transient signals were measured as a function of time by ramping down the drain voltage (V_D) to 1.5 V, while maintaining the gate voltage (V_G) at 0 V. To avoid self-heating effects, we chose a low V_D (1.5 V) for transient measurements. The schematic time domain representation of the applied $V_{D[ON]_{Stress}}$ of 10 V and 60 V; and the corresponding current-transients measured at $(V_G, V_D) = (0, 1.5)$ V are shown in Fig. 5.1(c) and (d) respectively. Since the $V_{D[ON]_{Stress}}$ facilitates current collapse due to buffer related trapping, the current-transients obtained after an $V_{D[ON]_{Stress}}$ will be dominated by emission of electrons from various trap energy levels present in the heterostructure bandgap [105][143]. The surface related trapping effects [144] have been neglected since the surface traps were passivated by $[(NH_4)_2S_x]$ surface treatment [55][121][140] followed by Si_3N_4 passivation.

5.3 Activation Energy determination by Arrhenius Analysis

The differential of the obtained current-transients with the corresponding logarithmic of transient time $[\delta I_D / \delta \log_{10}(\text{time})]$ is plotted against $\log_{10}(\text{time})$ for obtaining the emission time constants. The differential signals of the current-transients obtained after the $V_{D[ON]_{Stress}}$ conditions of (0, 10) V to (0, 60) V are shown in Fig. 5.2 (a) to (f), respectively.

A thermally activated electron detrapping process is obvious as the time constants corresponding to the peak position decrease with increasing measurement temperatures. The apparent activation energy E_a and the capture cross-section σ_c associated with the observed electron trap energy level is extracted from the Arrhenius plot of $\ln(\tau T^2)$ vs q/kT . The

temperature dependence of the emission time constant (τ) is described by using the classical Arrhenius equation:

$$\tau^{-1} = CT^2 e^{-E_a/kT}$$

Where, T is the temperature in Kelvin, E_a is the activation energy, τ is the time constant, k is the Boltzmann constant, and C is the fitting factor.

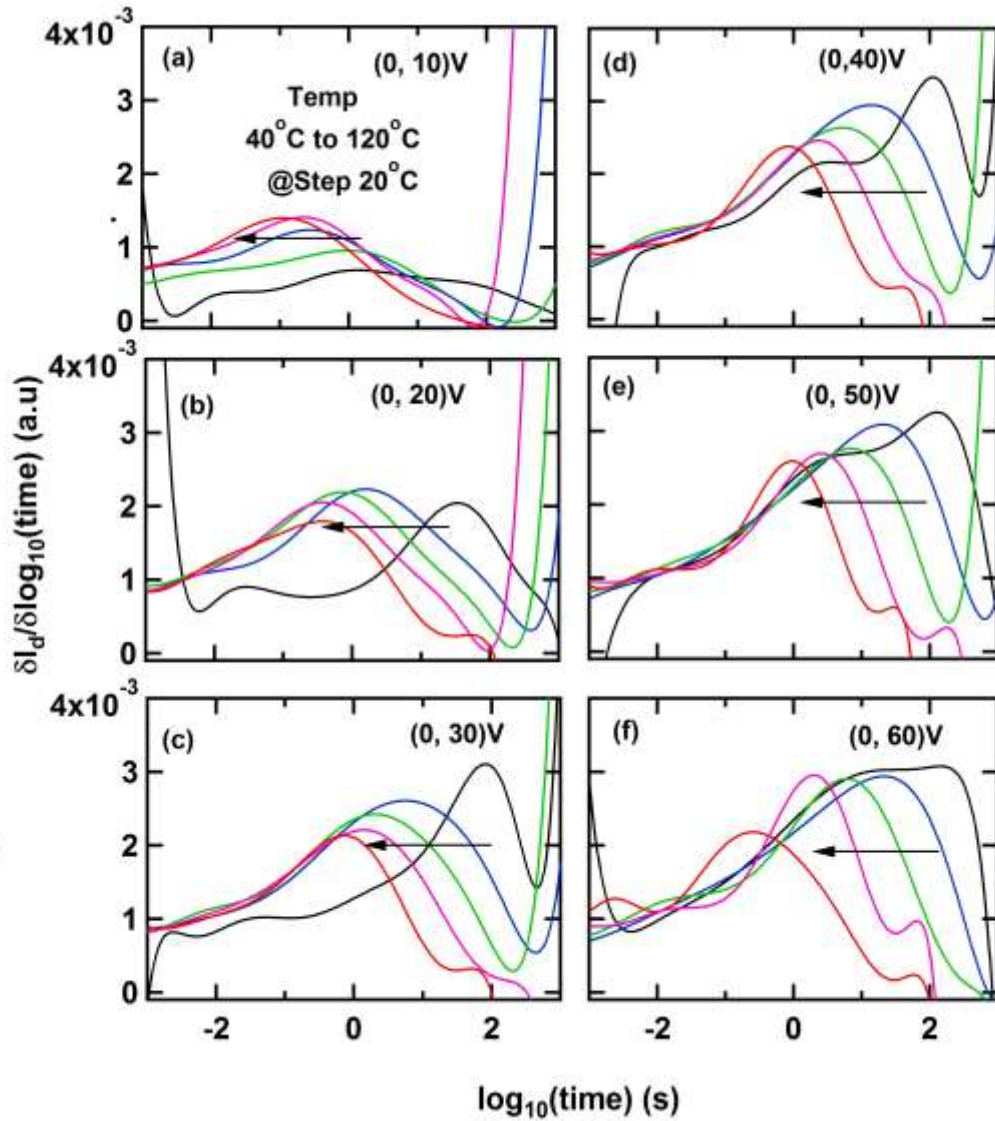


Figure 5.2 Differential signals from the temperature-dependent current-transients at (a) (0, 10) V, (b) (0, 20) V, (c) (0, 30) V, (d) (0, 40) V, (e) (0, 50) V and (f) (0, 60) V.

The activation energies (E_a 's) for the electron emission from the trap levels were determined using the Arrhenius analysis of the temperature-dependent emission-time constants. Figure 5.3 shows the compiled Arrhenius Plots showing the different E_a 's obtained for all the different $V_{D[ON]_{Stress}}$ conditions.

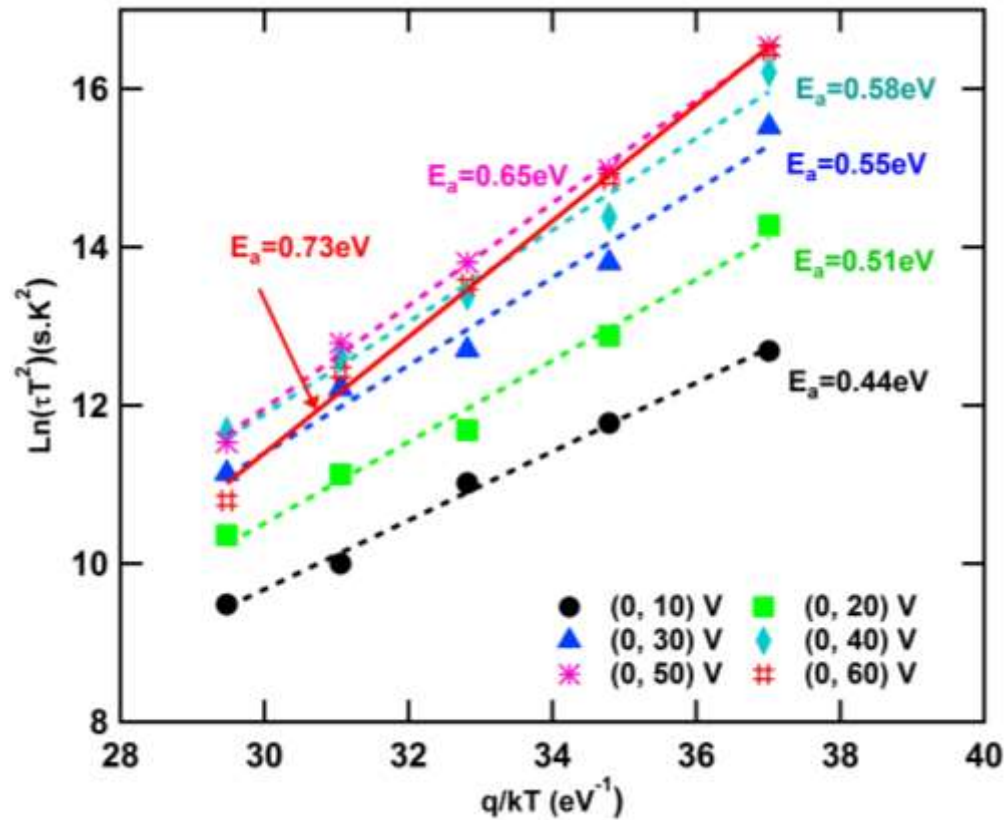


Figure 5.3 Arrhenius plots for determining the activation energies for HEMTs obtained after different $V_{D[ON]_{Stress}}$ conditions.

Based on the measured current-transients after the $V_{D[ON]_{Stress}}$ of 10 to 60 V, step 10 V, six different traps with E_a 's of 0.44 eV, 0.51 eV, 0.55 eV, 0.58 eV, 0.65 eV and 0.73 eV, and the corresponding capture cross sections of $4 \times 10^{-21} \text{cm}^2$, $2.6 \times 10^{-20} \text{cm}^2$, $8.5 \times 10^{-20} \text{cm}^2$, $3.5 \times 10^{-19} \text{cm}^2$, $2.4 \times 10^{-18} \text{cm}^2$ and $4.2 \times 10^{-17} \text{cm}^2$, respectively, were obtained. The physical origins of the obtained trap

activation energies have been given in Table 5.1. The obtained E_a 's exhibited a linear dependency with the applied- $V_{D[ON]_{Stress}}$ conditions.

Table 5.1 *Obtained trap activation energies with the corresponding physical origin.*

<u>Trap Activation Energies</u> (eV)	<u>Physical Origin</u>	<u>Ref</u>
0.44	C/O/H Impurities	[151]
0.51, 0.55	Nitrogen Anti-sites	[152][153][154]
0.58, 0.65	VGa + Oxygen complex	[152][155]
0.73	Nitrogen Interstitials	[156]

This behaviour suggests that the obtained E_a 's may be from DTE levels rather than single discrete trap energy levels. For a better understanding of the above behaviour, a thorough analysis of the differential signals obtained from the current-transients was performed as a function of measurement temperature and applied $V_{D[ON]_{Stress}}$.

5.4 ON-state stress dependent trap activation energy

Figure 5.4 shows the differential signals for all $V_{D[ON]_{Stress}}$ conditions measured at (a) 60°C, (b) 80°C, (c) 100°C and (d) 120°C. For 60°C, the signal peaks shifted towards higher time constants with increasing $V_{D[ON]_{Stress}}$. However, with increasing measurement temperature the signal peaks obtained at the $V_{D[ON]_{Stress}}$ conditions of (0, 50)V and (0, 60)V tends to shift towards lower time constants

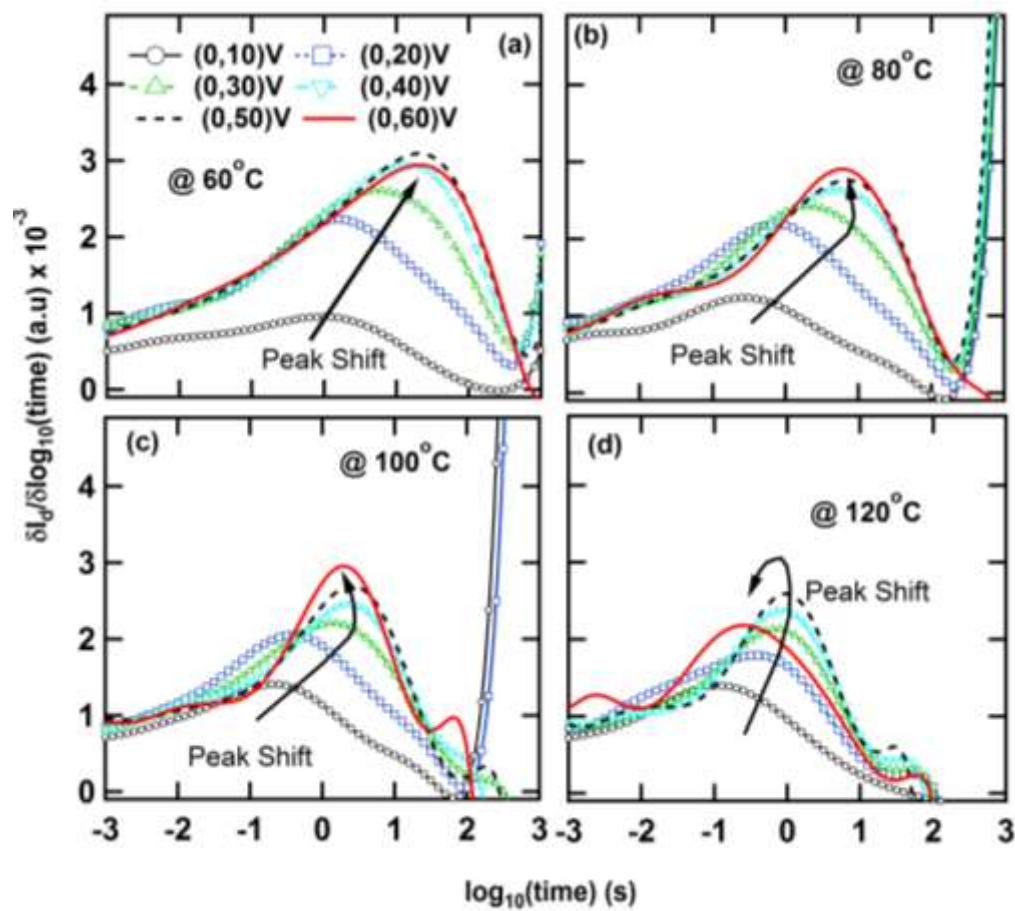


Figure 5.4 Differential signals of the temperature-dependent current-transients obtained for all $V_{D[ON]_{Stress}}$ conditions at, (a) 60°C, (b) 80°C, (c) 100°C and (d) 120°C.

The influence of temperature and the applied $V_{D[ON]_{Stress}}$ conditions on the obtained emission time constants (τ_e) has been plotted in the Fig 5.5.

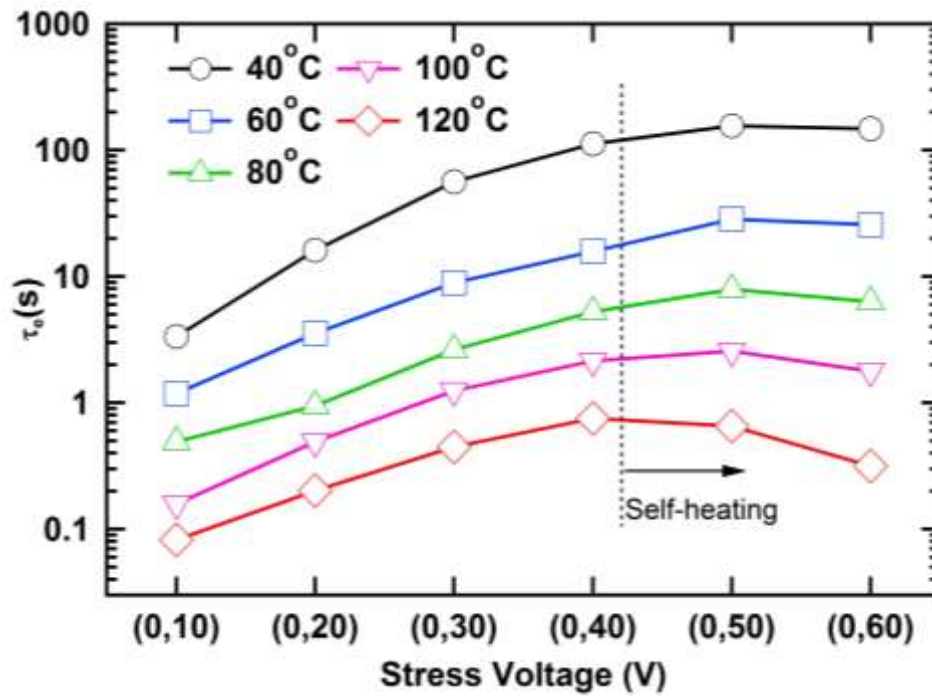


Figure 5.5 Emission time constants vs $V_{D[ON]_{Stress}}$ conditions for all measurement temperatures.

For lower $V_{D[ON]_{Stress}}$ (0, 40) V, τ_e increased **almost** linearly at all measurement temperatures. At measurement temperatures $\leq 80^\circ\text{C}$, the τ_e tends to saturate for $V_{D[ON]_{Stress}}$ conditions of $> (0, 40)$ V. However, the τ_e started decreasing at higher temperatures (100 and 120°C). This anomalous behaviour under the combination of high $V_{D[ON]_{Stress}}$ and high measurement temperature is attributed to self-heating effects in the AlGaIn/GaN HEMTs. Even under a constant $V_{D[ON]_{Stress}}$, the device experiences an increase in the channel temperature due to the self-heating induced by the $V_{D[ON]_{Stress}}$. The influence of self-heating on τ_e due to bias stress and temperature has also been reported by S. A. Albahrani *et al* [136].

5.5 Simulation and verification of distribution of trap energy

(DTE) levels

In order to understand the physics governing the trapping and detrapping mechanisms from DTE levels, 2-D numerical simulations using TCAD were performed with the trap information obtained from the experiments. Poisson's equation along with the carrier continuity equations for electrons and holes were solved by taking into consideration the contribution of mobile and fixed charges and ionized traps. The dynamic traps are modelled by a Shockley–Read–Hall recombination term included in the continuity equations.

For transient trap simulations, an additional differential-rate-equation is solved to account for emission and capture processes. As a filling pulse, both the source and gate terminals were biased at 0V and a drain bias ($V_{D[ON]_{Stress}}$) of 10 to 60 V (step 10 V) was applied for a period of 1 s, with a rise/fall time of 10 ns. For obtaining the current-transient signal, the drain bias was ramped down from the $V_{D[ON]_{Stress}}$ to a measurement voltage of 1.5 V while maintaining the source and gate terminals at 0 V. All the measurements were performed at an isothermal condition of 313 K (40°C). No thermal effects were considered in the simulation.

Thus, the model does not account for self-heating effects. For a discrete single quantum energy level the total trap charge density (Q_{Tr}) in the single trap energy (STE) model is given by

$$Q_{Tr} = qN_{tA} = q \cdot n_t \cdot F_{tA} \quad (1)$$

where, q , $N_{t,A}$, n_t and $F_{t,A}$ are the electronic charge, ionized acceptor density, trap density and probability of ionization, respectively. $N_{t,A}$ increases with increasing $V_{D[ON]_{Stress}}$ due to increasing spread of 2DEG wave-function beyond the channel [see Fig. 5.1(b)] and consequently this increases the $F_{t,A}$. However, the dependency of the τ_e with the applied $V_{D[ON]_{Stress}}$ could not be validated through the STE model. Instead a multi-trap-energy (MTE) model, consisting of several discrete energy levels in the heterostructure band-gap was incorporated into the TCAD environment. In the MTE model, the effective ionized acceptor density ($N_{t,A,eff}$) is given by

$$N_{t,A,eff} = \sum_{j=1}^m N_{t,A,j} \quad (2)$$

where, m is the total number of acceptor-like trap levels present in the energy band-gap and $N_{t,A,j}$ is the ionized acceptor trap density for the j^{th} trap energy level. The probability of ionization ($F_{t,A,j}$) and the electron emission rates ($e_{n,A,j}$) for j^{th} trap energy level, $E_{t,A,j}$ are given by

$$F_{t,A,j} = \frac{v_n \sigma_{c,n,j} n + e_{p,A,j}}{v_n \sigma_{c,n,j} n + v_p \sigma_{c,p,j} p + e_{n,A,j} + e_{p,A,j}} \quad (3)$$

$$e_{n,A,j} = g \cdot v_n \sigma_{c,n,j} n_i e^{\frac{E_{t,A,j} - E_i}{kT}} \quad (4)$$

where $\sigma_{c,n,j}$, $\sigma_{c,p,j}$ are the capture cross-sections and v_n , v_p are the thermal velocities for electrons and holes, respectively, and g is the degeneracy factor of the trap centre [20]. For validating the experimentally observed $V_{D[ON]_{Stress}}$ dependency of the E_a , 2-D transient simulation was performed by separately considering the STE model and the MTE model.

The differential signals of the current-transients for $V_{D[ON]_{Stress}}$ conditions of (0, 20) V, (0, 40) V and (0, 60) V, obtained from the TCAD simulations using the STE model for four individual trap energy levels of $E_a = 0.44$ eV, 0.51 eV, 0.55 eV and 0.58 eV are as shown in Fig. 5.6. (a) to (d) respectively. No considerable peak shift is observed for the differential signals. The emission time do not show any dependency with the applied $V_{D[ON]_{Stress}}$ conditions when simulated with the STE model.

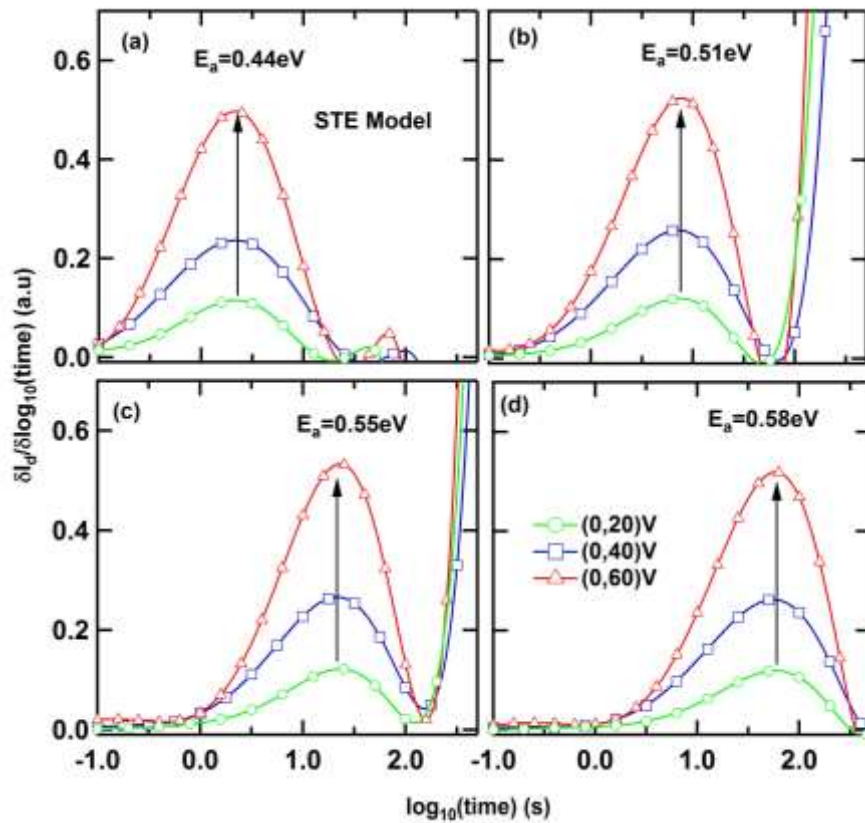


Figure 5.6 Differential signals of the current-transients obtained from the TCAD simulations for individual trap levels at different $V_{D[ON]_{Stress}}$ conditions.

The differential signals of the current-transients for all the $V_{D[ON]_{Stress}}$ conditions obtained from the TCAD simulations using the MTE model (all

the traps incorporated together) is shown in Fig. 5.7. Here only one significant peak is obtained which shifted towards the higher time constant with increasing $V_{D[ON]_{Stress}}$ as also observed experimentally [see Fig. 5.4]. Thus a clear dependency of the emission time constant with the applied $V_{D[ON]_{Stress}}$ conditions can be observed.

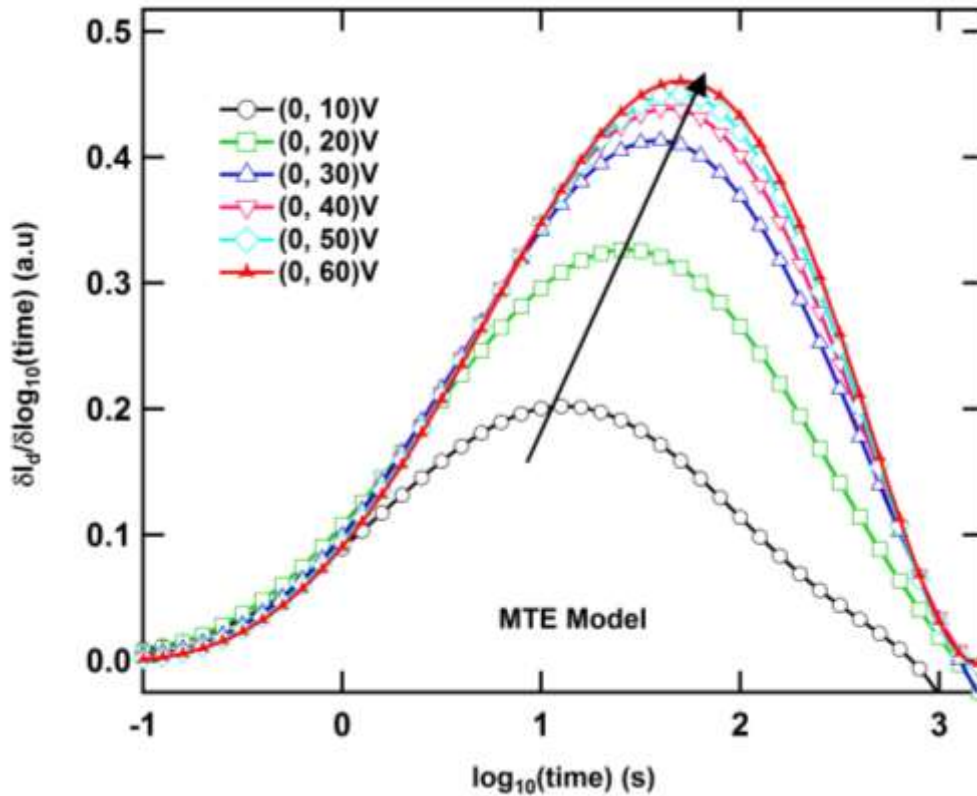


Figure 5.7 Differential signals of the current-transients obtained from the TCAD simulations for multi-trap levels.

For better understanding, a comparison of the τ_e vs $V_{D[ON]_{Stress}}$ characteristics between the experiment and simulation is shown in Fig. 5.8. When simulated with individual trap levels using STE model, the corresponding τ_e (broken lines) show no variations with increasing $V_{D[ON]_{Stress}}$. This is because the emission rate $e_{n,A,j}$ does not change significantly with $V_{D[ON]_{Stress}}$ as given by eq 4. However, the transient

simulations with all traps incorporated together (MTE model), resulted in an effective τ_e (▲ – markers) which increased with increasing $V_{D[ON]_{Stress}}$. This effective τ_e ranged between the τ_e of the upper and the lower limits of the incorporated discrete trap energy levels. As shown in Fig. 5.8, the rate of increase of τ_e with respect to $V_{D[ON]_{Stress}}$ exhibited a similar trend for both experiment (■–markers) and simulation (▲–markers) except with some deviation at high $V_{D[ON]_{Stress}}$ caused by self-heating effects [136]. This shows that the obtained transient signals contain information from various trap energy levels which are activated by the applied $V_{D[ON]_{Stress}}$ [56].

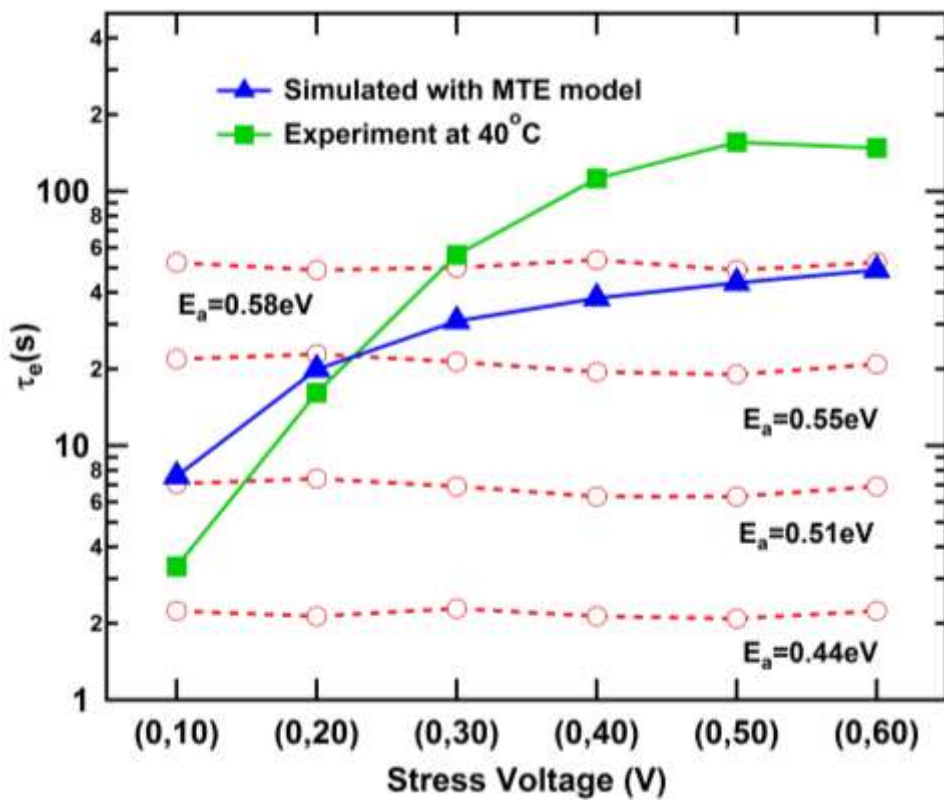


Figure 5.8 Emission time constants vs $V_{D[ON]_{Stress}}$ conditions for all measurement temperatures for individual traps using STE model (broken lines), MTE model (▲ – markers) and compared with the experimentally obtained emission time constant at 40°C (■ – markers)

Thus, it is clearly evident from both experiments and simulations (MTE model) that the τ_e increases with $V_{D[ON]_{Stress}}$. This effect can be explained only if we consider the existence of a DTE function rather than discrete quantum energy levels in the GaN energy bandgap as shown in Fig. 5.9. As the $V_{D[ON]_{Stress}}$ increases, the GaN conduction band bends downwards activating different trap energy levels [56].

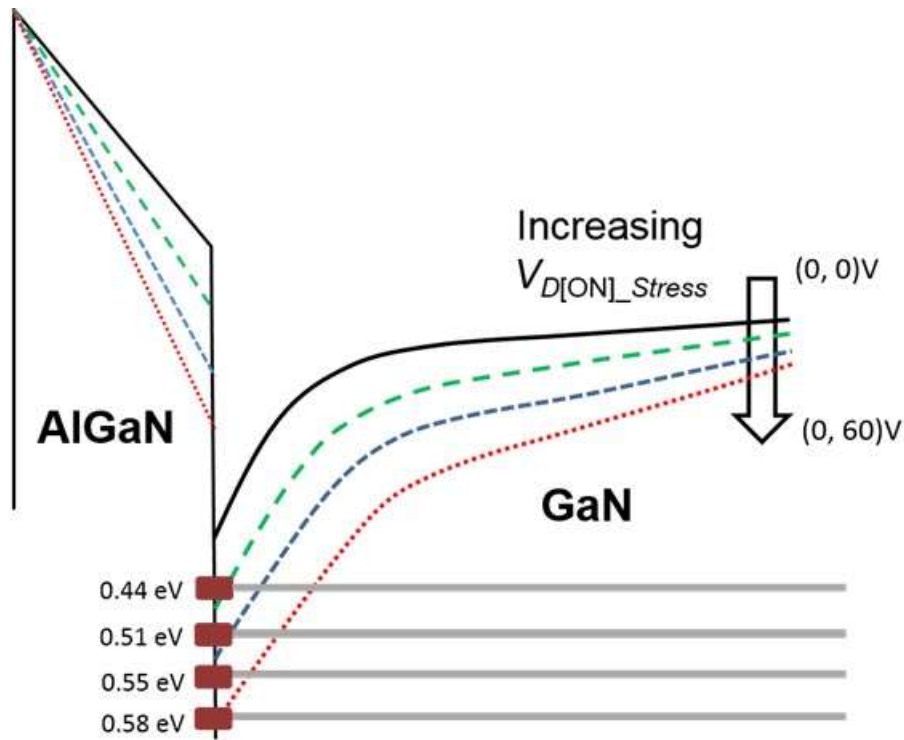


Figure 5.9 Schematic representation of AlGaN/GaN heterojunction energy band bending with different $V_{D[ON]_{Stress}}$ conditions and the distribution of traps in the GaN energy band-gap.

The TCAD simulated probability of ionization ($F_{t,A,j}$) under the applied $V_{D[ON]_{Stress}}$ of (0, 60) V is shown in Fig. 5.10 with the traps incorporated in (a) only in the AlGaN barrier, (b) only in the GaN buffer, and (c) in both AlGaN barrier and GaN buffer.

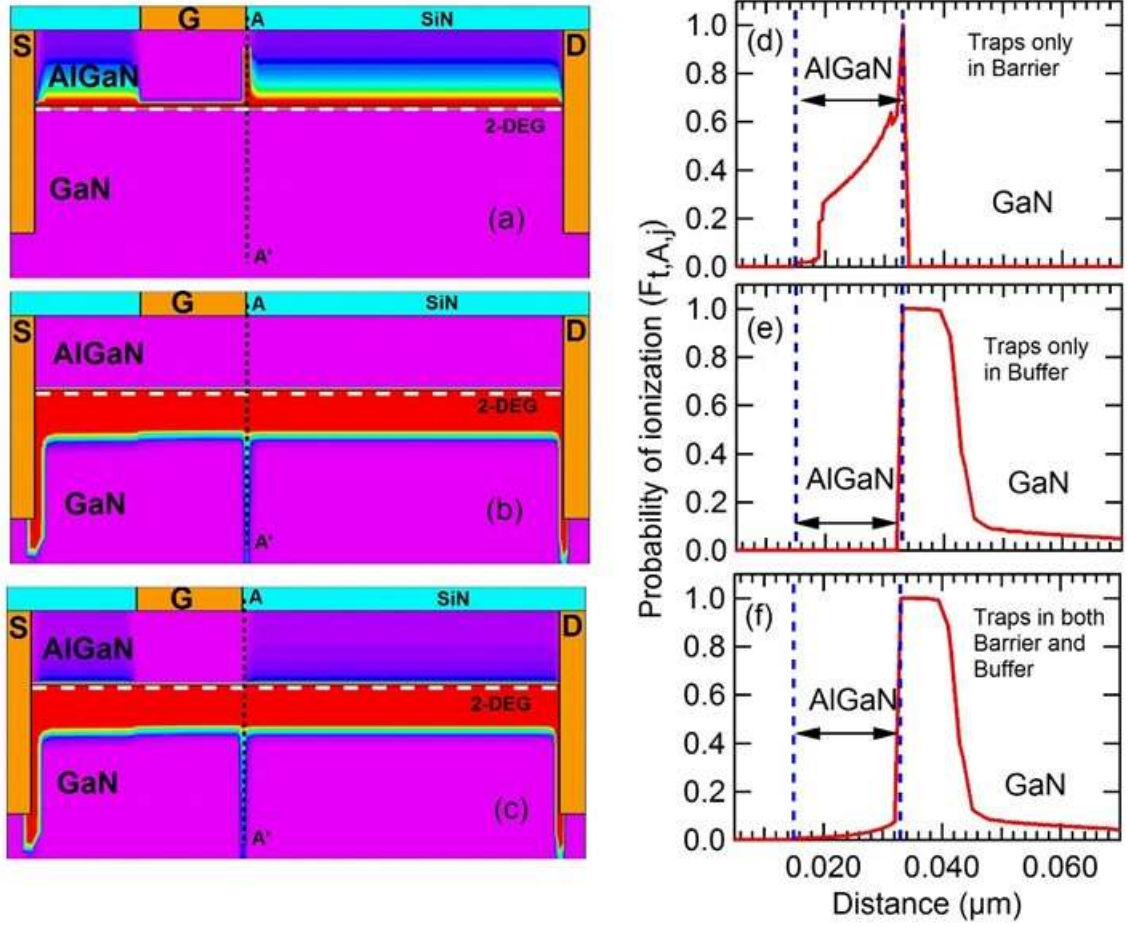


Figure 5.10 TCAD simulated probability of ionization ($F_{t,A,j}$) with the traps incorporated in (a) only in the AlGaN barrier, (b) only in the GaN buffer, and (c) in both AlGaN barrier and GaN buffer; and (d), (e) and (f) shows the corresponding $F_{t,A,j}$ at the cut-line position of AA', under the applied- $V_{D[ON]_{Stress}}$ of (0, 60) V.

Figure 5.10 (d), (e) and (f) shows the corresponding $F_{t,A,j}$ at the cut-line position of AA'. It is evident that when traps are incorporated in both barrier and buffer, the probability of electron trapping under ON-state stress conditions is higher in the GaN buffer [130][144][146][145]. This has also been confirmed by the hydrodynamic model [144]. In the STE model, the $e_{n,A}$

would not change with varying $V_{D[ON]_{Stress}}$. Considering the MTE model, the $N_{t,A,eff}$ increases with increasing $V_{D[ON]_{Stress}}$ and can be expressed as:

$$N_{t,A,eff} = n_t \sum_{j=1}^m F_{t,A,j} \cong n_t \cdot \frac{v_n \sigma_{c,n,eff} n}{v_n \sigma_{c,n,eff} n + e_{n,A,eff}(V_{dq})} \quad (5)$$

where, $e_{n,A,eff}(V_{dq})$ is the new effective emission rate corresponding to the effective activation energy ($E_{a,eff}$) that is a function of the applied $V_{D[ON]_{Stress}}$. Thus, the increase in τ_e with the increase of $V_{D[ON]_{Stress}}$ is due to the presence of DTE levels in the GaN energy band-gap. An accurate functional dependency of emission rate or E_a on the applied stress voltage needs further investigation.

5.6 Summary

Using the temperature-dependent current-transient based trap analysis under fully ON-state stress conditions, we investigated the trap dynamics in AlGaIn/GaN HEMTs on Si. Six different trap activation energies (0.44, 0.51, 0.54, 0.58, 0.65 and 0.73 eV) were obtained for six different $V_{D[ON]_{Stress}}$ conditions with varying capture cross-sections. The trap properties showed a very clear linear dependency with the applied $V_{D[ON]_{Stress}}$ conditions. The dependency of the τ_e with the $V_{D[ON]_{Stress}}$ was observed in both experiments and numerical simulations. We have used both STE and MTE to investigate the behaviour and have presented a clear distinction between STE and MTE models. The dependency of the obtained τ_e with the applied- $V_{D[ON]_{Stress}}$ could be simulated only by incorporating the MTE model. This clearly indicates **that** the obtained trap properties were from a continuous-DTE levels in the GaN energy bandgap. Such a quantitative approach towards

trap characterization will facilitate the device designers in developing a more accurate reliability model for GaN-based HEMTs.

Chapter 6

Current Collapse in AlGaN/GaN MISHEMTs

In this chapter, we have presented a comparison study on the drain current collapse characteristics of conventional AlGaN/GaN HEMTs and SiN/Al₂O₃/AlGaN/GaN MISHEMT fabricated on silicon substrate. Compared to conventional AlGaN/GaN HEMTs, about one order of magnitude lower gate leakage current and ~ 60% reduction in current collapse was observed in the MISHEMTs. We have attributed the reduction in the current collapse and the reduction in the device leakage currents to the reduced interface state density between SiN/Al₂O₃ dielectric stack and the GaN cap layer which was confirmed through the AC-conductance method.

6.1 Introduction

There are two major issues that limit the electrical performance of conventional Schottky gated AlGaN/GaN HEMTs, which need detailed investigation. Firstly, current collapse or drain current dispersion caused by trapping of electrons by the surface states present on the AlGaN surface [100][157] and other process induced traps can compromise the performance window of the devices. Various surface passivation methods, especially passivation through PECVD SiN [116] have helped in mitigating the current collapse phenomenon. Secondly, the high gate-leakage currents limit the positive gate voltage swing and thus the maximum output power

as well the microwave performance [158][159]. To reduce the gate-leakage currents, researchers have tried various gate dielectrics such as SiO₂ [160][161], SiN [162][163], Al₂O₃ [164], MgO [165], Sc₂O₃ [166] and ZrO₂ [94]. Among these, atomic layer deposited (ALD) Al₂O₃ is one of the most preferred gate dielectric schemes for GaN MISHEMTs[93][95][167][168] with its additional advantages such as wide bandgap energy (9 eV), large dielectric constant ($k \sim 10$), high breakdown field (~ 10 MV/cm), high thermal and chemical stability. Bilayer dielectric stacks of SiO₂/SiN, Al₂O₃/SiN [16] and TiO₂/SiN [95] have also been explored as gate insulators for AlGaN/GaN transistors taking advantage of the benefits of each layer. The ALD grown Al₂O₃ on AlGaN/GaN exhibited the presence of a good quality gate oxide [167]. The SiN gate dielectric that helps to alleviate current collapse caused by surface states, experiences high level of reverse leakage current [92]. Combining the advantages of Al₂O₃ for reducing the gate leakage and SiN for current collapse suppression, the bilayer SiN/Al₂O₃ dielectric has been utilized as a passivation layer to suppress the surface-leakage current as well as to improve the OFF-state BV_{GD} of AlGaN/GaN HEMT. In this work the SiN/Al₂O₃ hybrid dielectric stack was employed in order to exploit the combined advantages of Al₂O₃ for reducing gate leakage and SiN for suppressing device current collapse.

6.2 Diode C - V and I - V Characteristics

The device fabrication details and the schematic representations can be found in chapter 3 of this thesis. The capacitance-voltage (C - V) of the Schottky diodes, the SiN/Al₂O₃ MIS-diodes and the DC current-voltage (I_D –

V_D) characteristics of the conventional Schottky gated HEMTs (conventional HEMTs) and the MISHEMTs were measured using the Agilent B1500A semiconductor-parameter analyser. To quantify the current collapse, pulsed $I_D - V_D$ measurements were performed using Accent DIVA D265 system.

Figure 6.1 shows the schematic representation of a circular SiN/Al₂O₃/GaN/AlGaN/GaN MIS diode with a gate electrode of 50 μm diameter used for $C-V$ and $I-V$ characterization. The conventional Schottky-gate AlGaN/GaN diodes fabricated for comparison has the same device structure and fabrication process except that of a 5/5 nm SiN/Al₂O₃ gate dielectric.

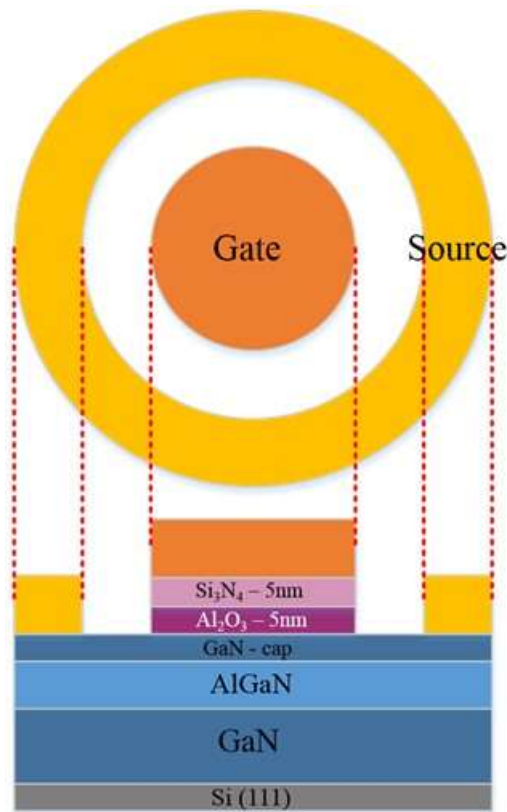


Figure 6.1 Schematic cross-section of the SiN/Al₂O₃/GaN/AlGaN/GaN MIS diode (diameter 50- μm).

The measured diode $C-V$ at a frequency of 1 MHz for the Schottky and MIS-diodes are shown in Fig 6.2 (a). The gate dielectric layer thickness was extracted from the $C-V$ curves using the following equations:

$$(1/C_{\text{MISHEMT}}) = (1/C_{\text{HEMT}}) + (1/C_{\text{ox}}) \quad (1)$$

Where, $C_{\text{ox}} = (\epsilon_{\text{ox}} \epsilon_0 A)/d$.

The values of C_{MISHEMT} and C_{HEMT} are read from the plateau region of the $C-V$ curves for MISHEMT and HEMT, respectively.

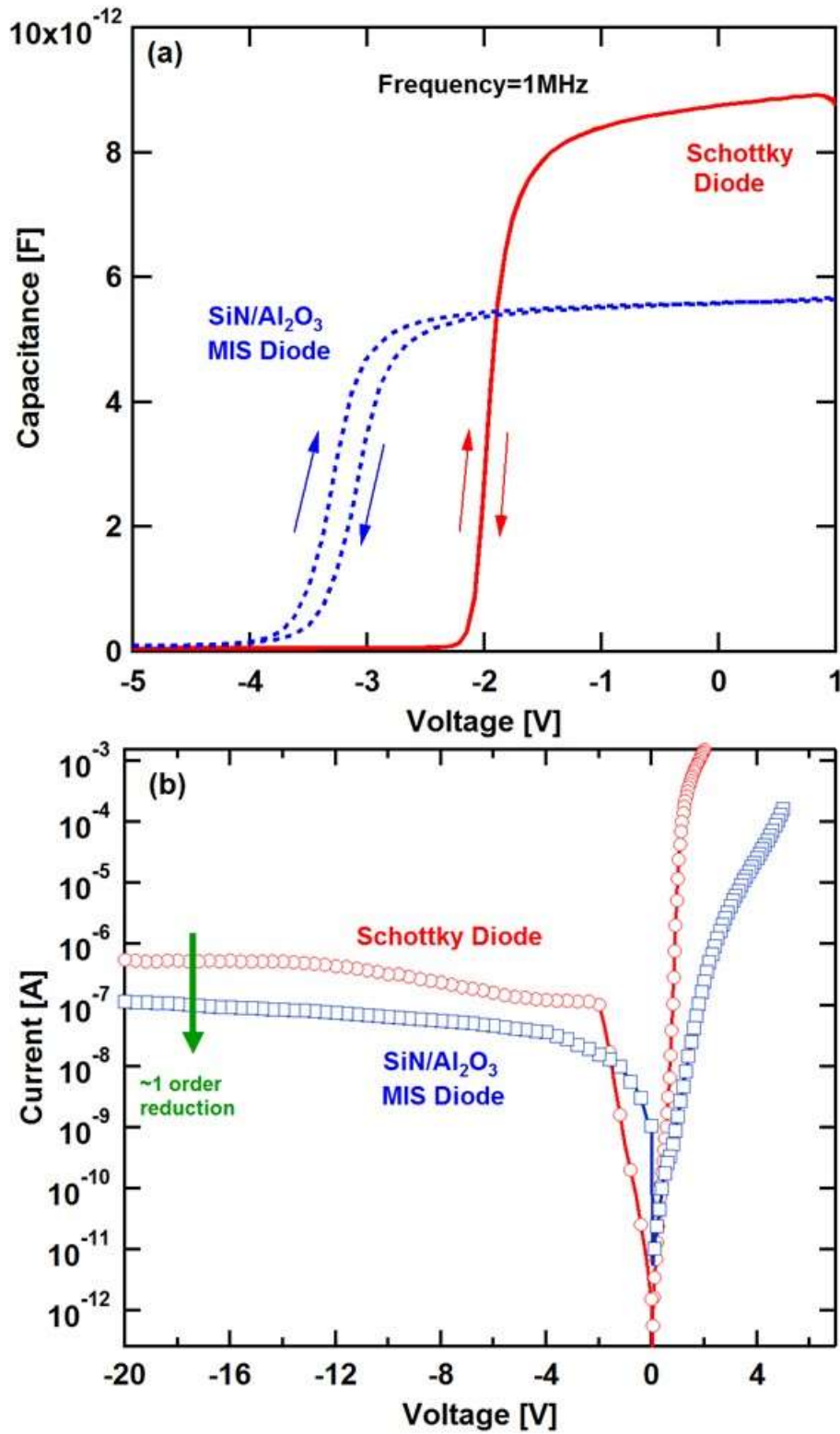


Figure 6.2 (a) C - V and (b) I - V characteristics of the $\text{SiN}/\text{Al}_2\text{O}_3$ / $\text{GaN}/\text{AlGaN}/\text{GaN}$ MIS diode and conventional $\text{GaN}/\text{AlGaN}/\text{GaN}$ Schottky diode (diameter $50\text{-}\mu\text{m}$).

The average dielectric constant (ϵ_{ox}) of the bilayer gate dielectric stack of 5 nm ALD- Al_2O_3 and 5 nm PECVD SiN is determined as ≈ 8.9 using the expression $\epsilon_{ox} = C \cdot d / (A \epsilon_0)$ through separate metal-insulator-metal (MIM) structures, where d is the thickness of the Al_2O_3 and SiN insulators in the MIM structures, measured by an ellipsometer, A is the area, and ϵ_0 is the vacuum permittivity.

The total dielectric layer thickness was thus determined to be 10 nm and is found to be in good agreement with the thicknesses of the Al_2O_3 (5 nm) and SiN (5 nm) gate insulator layers as confirmed by TEM [see Fig. 3.6 of chapter 3]. From the forward and reverse C - V measurements of the MIS-diode, a sharp transition from the deep depletion to accumulation region with a small hysteresis of ≈ 0.2 V was observed, which is indicative of a good quality insulator (ALD- Al_2O_3 and PECVD- SiN) film with low trap density at the $\text{Al}_2\text{O}_3/\text{GaN}$ (insulator/semiconductor) interface. Such small hysteresis indicating some fixed charges in the oxide layer is also observed and reported in references [160] and [167].

Figure 6.2 (b) shows the forward and reverse I - V characteristics of Schottky and MIS diodes. It can be observed that the SiN/ Al_2O_3 MIS diode exhibits at least one order of magnitude reduction in the reverse and forward leakage characteristics compared to the conventional Schottky diode.

6.3 DC and Small-signal Characteristics of Conventional. HEMTs and MISHEMTs

Figure 6.3 (a) and (b) shows the DC I_D - V_D characteristics of conventional HEMTs and MISHEMTs respectively and (c) shows the transfer characteristics of conventional HEMT and MISHEMT. A maximum I_{Dmax} for conventional HEMT of around 700 mA/mm was achieved at $V_G = +1V$ while in comparison, a higher I_{Dmax} of >1000 mA/mm was achieved at $V_G = +2V$ for MISHEMT.

Due to the reduced gate-leakage current as shown in Fig. 6.2 (b), much higher gate bias can be applied for the SiN/Al₂O₃ MISHEMT than the conventional HEMT. At $V_D = 6 V$, a maximum $g_{m,max}$ of 245 mS/mm and 241 mS/mm have been achieved for conventional HEMT and MISHEMTs, respectively. The increase in the gate-to-channel distance results in the negative shift of V_{th} . However, the $g_{m,max}$ of the MISHEMT is comparable to the $g_{m,max}$ of conventional GaN HEMTs. Similar observation was reported by Kanamura et al [169]. The current gain cut-off frequency (f_t) for both HEMTs and MISHEMTs are 24 GHz which also follows a similar trend like the measured $g_{m,max}$ values. The extracted source resistance (R_s) and the intrinsic transconductance (g_{m0}) from the small signal equivalent circuit model were 1.98 Ω & 1.60 Ω and 40 mS & 38 mS for conventional HEMT and MISHEMT, respectively (See equation 2) [170]. The above extracted values are in good agreement with the measured f_t values.

$$g_{m,max} = \frac{g_{m0}}{1+R_s(g_{m0})} \quad (2)$$

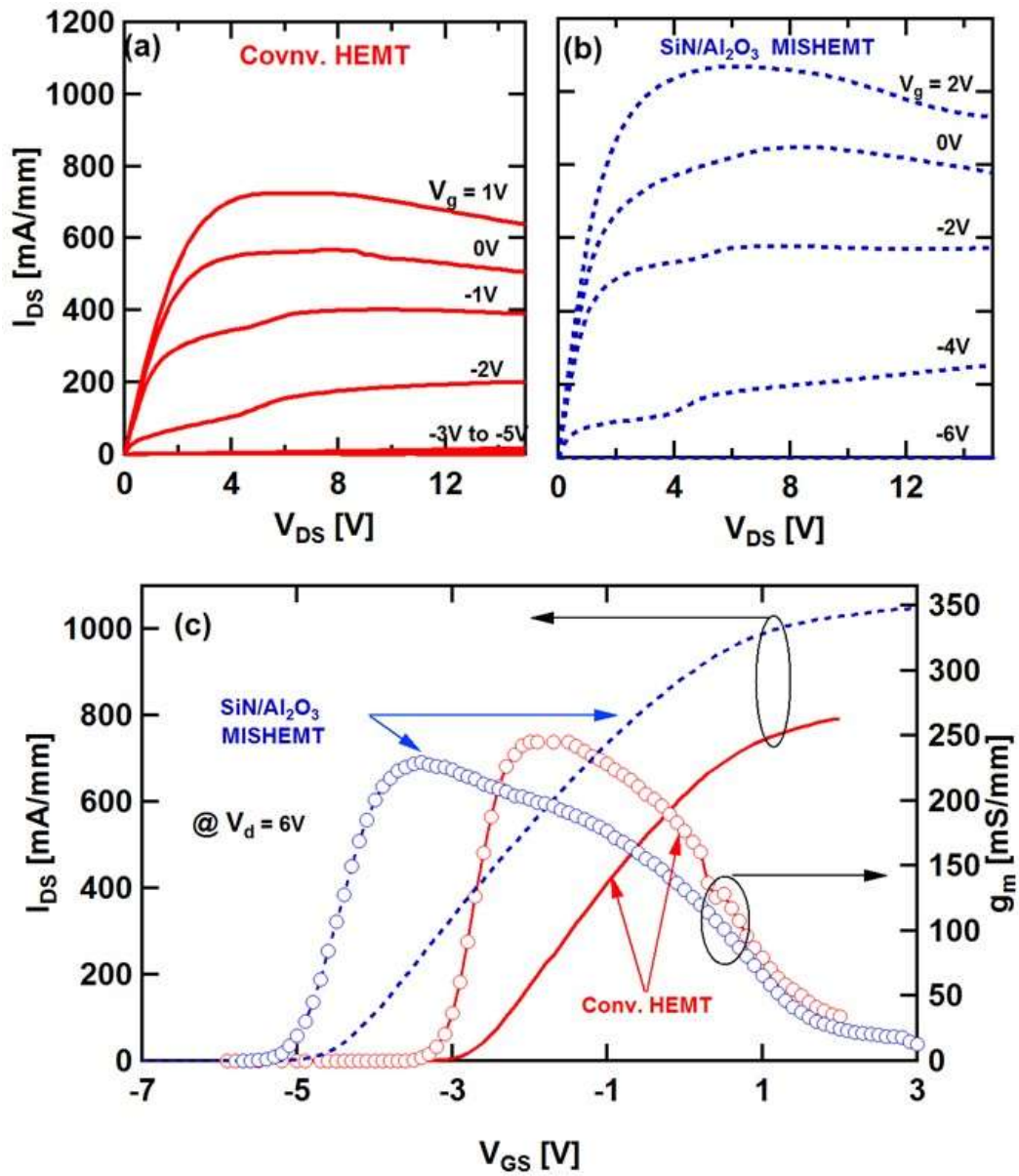


Figure 6.3 DC I_D - V_D characteristics of (a) *conventional HEMT*, (b) *SiN/Al₂O₃/GaN/AlGaIn/GaN MISHEMT* and (c) *transfer characteristics comparison of conventional HEMTs and MISHEMTs*. Device Dimensions: $L_g/L_{gd}/W_g=0.3/1.6/(2 \times 25) \mu m$.

6.4 Pulsed I_D - V_D characterization of Conventional HEMTs and MISHEMTs

Figure 6.4 shows the pulsed I_D - V_D characteristics [pulse width = 200 ns; pulse separation = 1.0 ms] of (a) conventional HEMTs and (b) SiN/Al₂O₃ MISHEMT for different combinations of gate- and drain-Q-bias conditions of (0, 0), (-5, 0) and (-5, 30) respectively.

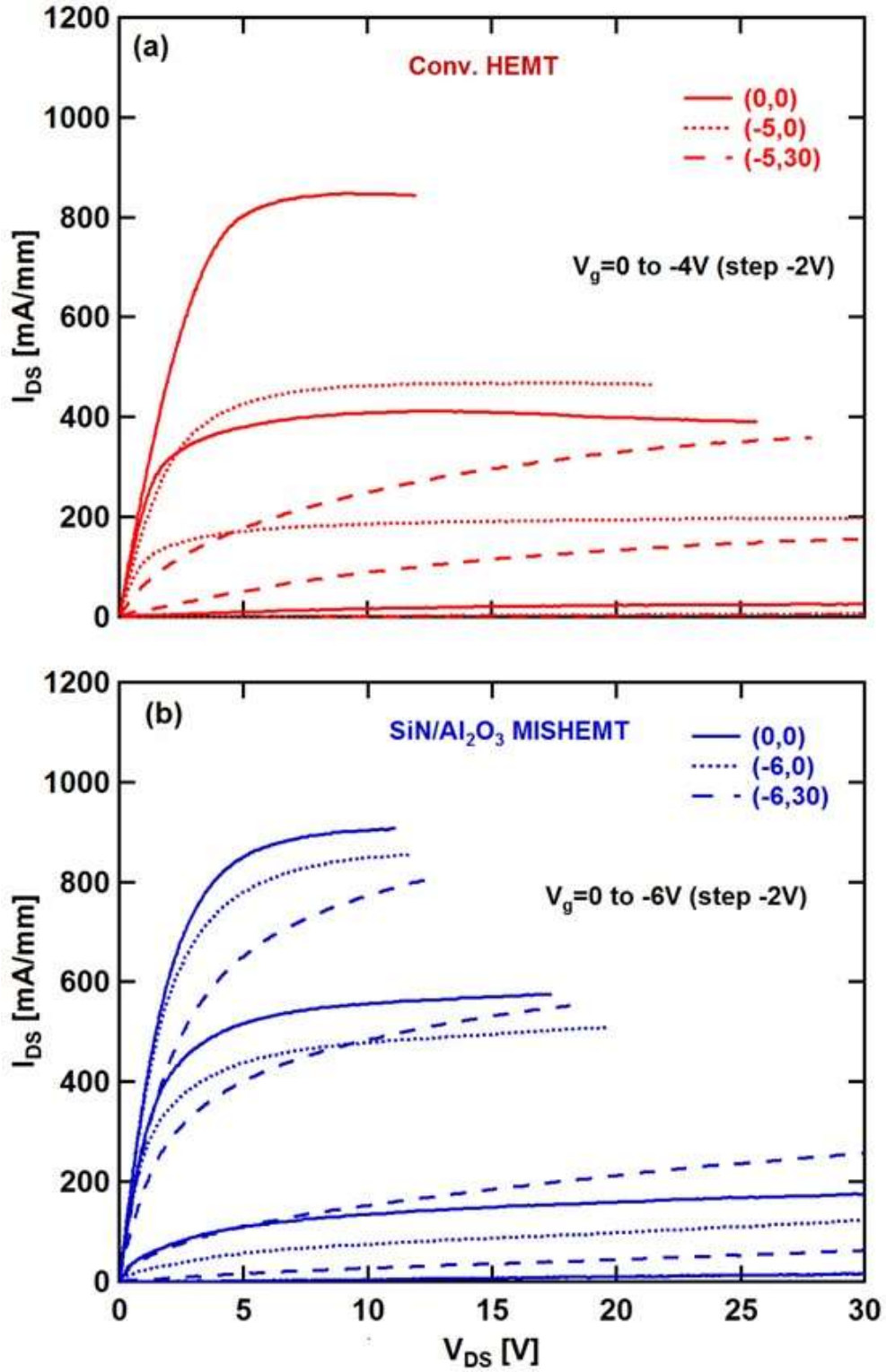


Figure 6.4 Pulsed I_D - V_D characteristics of (a) Conventional HEMTs and (b) SiN/Al₂O₃ MISHEMT for different combinations of gate- and drain-Q-bias conditions. Device dimension: $W_g/L_g/L_{gd} = (2 \times 100)/0.3/2.9 \mu\text{m}$.

Figure 6.5 shows the normalized I_D/I_{Dmax} measured at $V_D = 8$ V obtained from the pulsed I_D - V_D characteristics of conventional HEMTs and MISHEMTs measured under the Q-bias conditions of $[(-5, 10), (-5, 15), (-5, 20), (-5, 25)$ and $(-5, 30)$ V for conventional HEMT and $(-6, 10), (-6, 15), (-6, 20), (-6, 25)$ and $(-6, 30)$ V for MISHEMT].

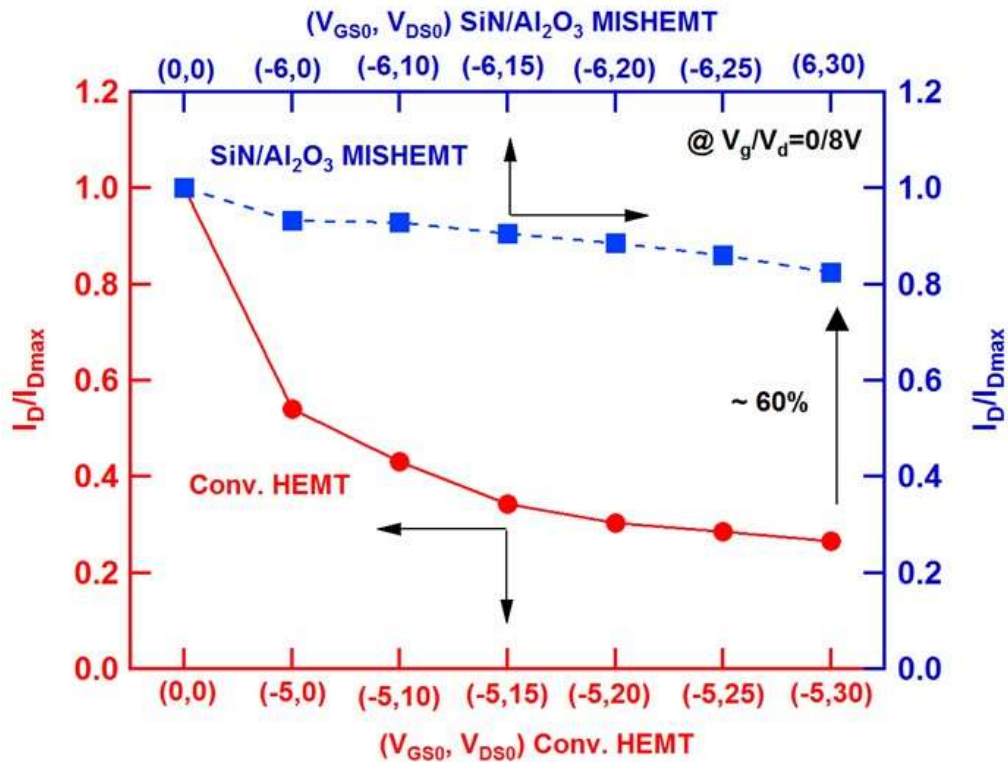


Figure 6.5 Normalized I_{Dmax} observed from pulsed I_D - V_D characteristics of conventional HEMTs and SiN/Al₂O₃ MISHEMT for different combinations of gate- and drain-Q-bias conditions. Device Dimensions: $W_g/L_g/L_{gd}=(2 \times 100)/0.3/2.9 \mu m$.

From these plots, it is clear that the bilayer SiN/Al₂O₃ gate-dielectric layer is helping to suppress the drain current collapse by at least ~60%. Table 6.1 shows the comparison between two different lags (gate-lag and gate-& drain-lag) conditions for conventional HEMT and MISHEMT. For the gate-

lag condition $[(-6, 0) \text{ V for MISHEMT and } (-5, 0) \text{ V for conventional HEMT}]$, only 18 % current collapse was observed in MISHEMTs. However, the conventional HEMT exhibited 82 % current collapse. The bi-layer SiN/Al₂O₃ dielectric layer helps to suppress around 40 % current collapse in MISHEMTs. For the gate- and drain-lag conditions $[(-6, 30) \text{ V for MISHEMT and } (-5, 30) \text{ V for conventional HEMT}]$, only 32 % drain current collapse was observed in MISHEMTs. However, conventional HEMT exhibited 92 % current collapse. Overall, ~60% drain current collapse suppression was observed in MISHEMTs when compared to conventional HEMTs (see Table 6.1 and Fig 6.5). A current collapse suppression of ~ 51% has been reported on a single layer SiN MISHEMT in [162], which suggests that the role of SiN in the bilayer scheme is also effectively passivating the surface related traps.

Table 6.1 Percentage of current collapse measured at $V_G = 0 \text{ V}$, $V_D = 8 \text{ V}$ for conventional HEMT and SiN/Al₂O₃ MISHEMT.

Device	I_{Dmax} (mA/mm)	Gate-lag	Gate- & Drain-lag
Conventional HEMT	873	82% @ (-5, 0)V	92% @ (-5, 30) V
MISHEMT	918	18% @ (-6, 0)V	32% @ (-6, 30) V

The observed suppression of current collapse with a bilayer SiN/Al₂O₃ gate dielectric MISHEMT is also in good agreement with the effective suppression of current collapse in both E-mode and D-mode GaN HEMTs by ammonium sulfide $[(\text{NH}_4)_2\text{S}_x]$ treatment [121]. To further understand the suppression of current collapse in SiN/Al₂O₃ MISHEMTs, the interface trap state density (D_{it}) of bilayer SiN/Al₂O₃/GaN MIS diode was measured using the AC

conductance method [171], the details of which is furnished in the following section.

6.5 Interface-State Density (D_{it}) Measurement

The frequency dependent AC conductance method is a widely accepted technique to determine the interface trap properties in GaN MISHEMTs [171][172]. Although conductance method is a convenient way to extract information on traps, it tends to underestimate the trap density as deeper traps with higher time constants cannot be probed by this technique [173]. However, in this work, conductance method was used as our main focus to analyse qualitatively and compare the interface quality of MISHEMT versus Schottky gate HEMT. The interface trap state density, D_{it} and time constant, τ are evaluated by fitting the measured parallel conductance G_p as a function of radial frequency $\omega=2\pi f$ according to equation (3)

$$\frac{G_p}{\omega} = qD_{it} \left[\frac{\ln[1 + (\omega\tau)^2]}{2\omega\tau} \right] \quad (3)$$

Figure 6.6 shows the G_p/ω versus ω . A strong decrease in the G_p/ω peaks with decreased V_G was observed which implies a sharp decrease in the interface trap state density as $D_{it} \approx (2.5/q) (G_p/\omega)$ [167].

The measured interface state density (D_{it}) by conductance method is $6.39 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ at an energy level of 0.38 eV which is in the same range between $\sim 1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ and $\sim 3 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ of $\text{Al}_2\text{O}_3/\text{GaN}$ interface for the energy level of 0.3 to 0.4 eV below the conduction band [167].

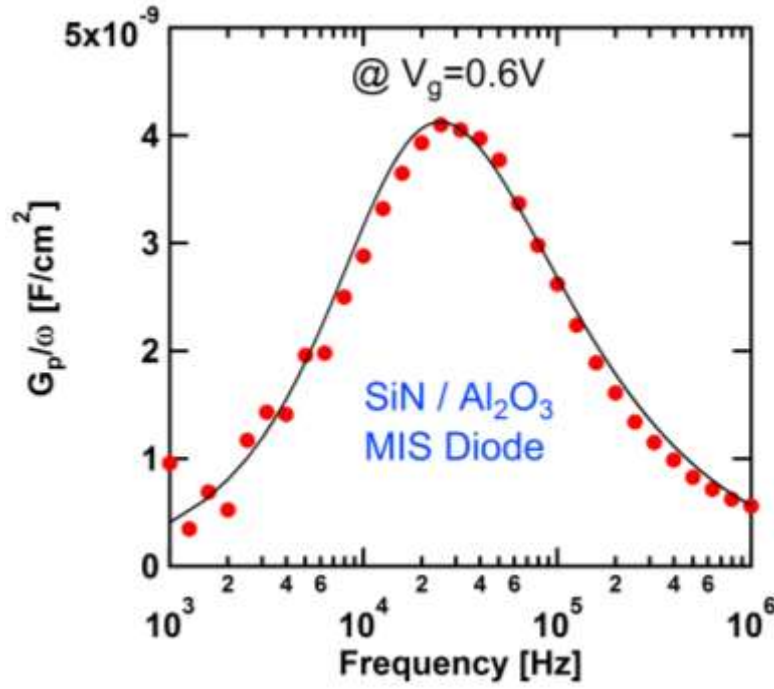


Figure 6.6 Conductance G_p as a function of radial frequency ω for SiN/Al₂O₃ MIS diode measured at gate voltage, $V_G = 0.6$ V, indicating a good fit for the theoretical (solid line) and measured (dotted line) values.

The density of interface traps at the metal-semiconductor junction of a conventional HEMT was determined using the following equation: [84]

$$D_{it} = \left(\frac{ss}{(k_B T/q) \ln 10} - 1 \right) \times \frac{C_b}{q} \quad (4)$$

where the subthreshold slope (ss) of 150mV/dec was obtained from the DC I_D - V_G characteristics of the conventional HEMT, and the barrier capacitance (C_b) was deduced as 4.38×10^{-7} F/cm². Thus, the calculated interface trap density based on equation (4) was $\sim 4.1 \times 10^{12}$ cm⁻² eV⁻¹ at the Schottky gate/GaN interface. Similar D_{it} values for Schottky gated GaN HEMTs have also been reported in [84] and [174]. Thus, in our case we were able to achieve at least ~ 2 orders of magnitude reduced D_{it} with an Al₂O₃/GaN (MIS) interface compared to our metal/semiconductor Schottky gate

interface. J. J Zhu et al [172] and J. Chung et al [174] have also reported a D_{it} reduction in the interface properties of GaN MISHEMTs in direct comparison with their conventional HEMT structures. Thus the overall, drain current collapse suppression by at least ~60% and the reduction of the gate leakage currents is due to the low interface trap state density between the bilayer SiN/Al₂O₃ gate dielectric and GaN cap layer.

6.6 Summary

The fabricated bilayer SiN/Al₂O₃/AlGaIn/GaN MISHEMT exhibited an I_{Dmax} of >1.0 A/mm and $g_{m,max}$ of 241 mS/mm. With reference to the conventional HEMTs, about one order of magnitude lower gate-leakage current has been observed in MISHEMT. The bi-layer SiN/Al₂O₃ gate dielectric MISHEMT suppressed ~60% of drain current collapse. The suppression of current collapse is due to a high quality interface with low interface state density ($6.39 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$) at the bilayer SiN/ Al₂O₃ gate dielectrics and GaN cap layer interface. From the pulsed I_D - V_D measurements, it is confirmed that the bilayer SiN/Al₂O₃ dielectric gate effectively suppress the current collapse due to the reduction of the interface-state density. The suppression of current collapse by using AlGaIn/GaN MISHEMTs with bilayer SiN/Al₂O₃ gate dielectric demonstrates the potential of GaN MISHEMTs for high-power and high-frequency device applications.

Chapter 7

BCB-Encapsulation on AlGa_N/Ga_N HEMT Performance

In this chapter, we present the impact of low-k dielectric benzocyclobutane (BCB) encapsulation layer on the electrical performance and structural stability of AlGa_N/Ga_N HEMTs on Si. The devices after BCB encapsulation exhibited superior BV_{GD} characteristics. Using static and dynamic electrical characterization, we have investigated the influence of the BCB encapsulation layer on the device BV_{GD} characteristics. Compared to devices without BCB encapsulation, the BCB encapsulated devices achieved ~2 orders of magnitude lower gate- and drain-leakage current. An order of magnitude lower surface-leakage current was also observed by BCB encapsulation between adjacent mesa structures. A detailed investigation of the improvement in the device electrical characteristics by BCB encapsulation is presented.

7.1 Introduction

To enhance the long-term reliability of the AlGa_N/Ga_N HEMTs [175], it is essential to protect it from various types of external degradation factors such as humidity, radiation etc. Thus encapsulating the AlGa_N/Ga_N HEMTs and their monolithic integrated circuits becomes very vital for an effective deployment of Ga_N technology under actual operating conditions. However,

AlGaIn/GaN heterostructures are very sensitive to external stress and the device performance greatly depends on various properties of the on-lying layers. Thus, it is imperative that the additional encapsulation layer does not compromise the electrical performance of the devices. The commonly used device encapsulation materials and their dielectric constants are shown in the Table 7.1.

Table 7.1 *Different encapsulation materials and their corresponding dielectric constants [176][177]:*

<u>Encapsulation material</u>	<u>Dielectric Constant (ϵ_r)</u>
PECVD - Si ₃ N ₄	7.5
SiO ₂	3.9
Spin-on-glass (SOG)	3.8
Polyimide	3.5

The high-frequency operating devices are sensitive to the dielectric constant of the encapsulation layer. In order to avoid any parasitic fringing capacitance, low- k ($\epsilon_r = 2.65$) benzocyclobutane (BCB) is a preferred choice [178][179]. The properties and the consequent advantages of BCB encapsulant are as follows:

- (i) low dielectric constant ($\epsilon_r = 2.65$) $\rightarrow$ lower parasitic capacitance,
- (ii) high glass transition temperature ($>350^\circ\text{C}$) $\rightarrow$ larger process window,

(iii) very low moisture absorption → highly reliable hermetic seal,
and

(iv) high degree of planarization [180] → better packaging control.

BCB has also been used as a replacement for Si_3N_4 as an effective surface passivation layer [181]. However, in IC fabrication, it is more relevant to use a thin dielectric layers of Si_3N_4 and/or SiO_2 for device passivation and followed by a thicker encapsulation layer for the final passivation and planarization. Even though Si_3N_4 and SiO_2 can effectively passivate the device [119] by reducing the surface states and/or surface related traps, the use of thick layers of Si_3N_4 or SiO_2 for passivation as well as encapsulation will impose excessive mechanical stress on the AlGaIn/GaN HEMT heterostructure. The mechanical stress on the AlGaIn/GaN heterostructure due to the additional passivation layers results in the reduction of device yield [182]. Furthermore, the high dielectric constants of these materials will result in increased parasitic capacitances. Multiple layers of Si_3N_4 for passivation and eventual encapsulation of AlGaIn/GaN HEMTs can result in tensile stress induced degradation [183]. To reduce the stress, Hampson *et al.* [184] have successfully tried polyimide as a surface passivation for AlGaIn/GaN HEMTs. P. Kurpas et al. [185] have also demonstrated 2.6 μm -thick BCB encapsulation on Si_3N_4 passivated GaN HEMTs on SiC substrates without observing any changes in the DC or small signal performances. This chapter will discuss on the influence of a 9 μm -thick low- k dielectric BCB encapsulation on the DC and RF performances, leakage currents, the break down voltage and their impact on the structural stability of two-finger and

multiple finger Si_3N_4 passivated $0.3\text{ }\mu\text{m}$ gate AlGa N /Ga N HEMTs on Si substrate.

7.2. Experimental methods

The AlGa N /Ga N HEMT structure and the fabrication details are discussed in the Chapter 3. Figure 7.1 shows the schematic cross-section of the fabricated AlGa N /Ga N HEMTs on Si substrate (a) without BCB encapsulation and (b) with $9\text{ }\mu\text{m}$ -thick BCB encapsulation.

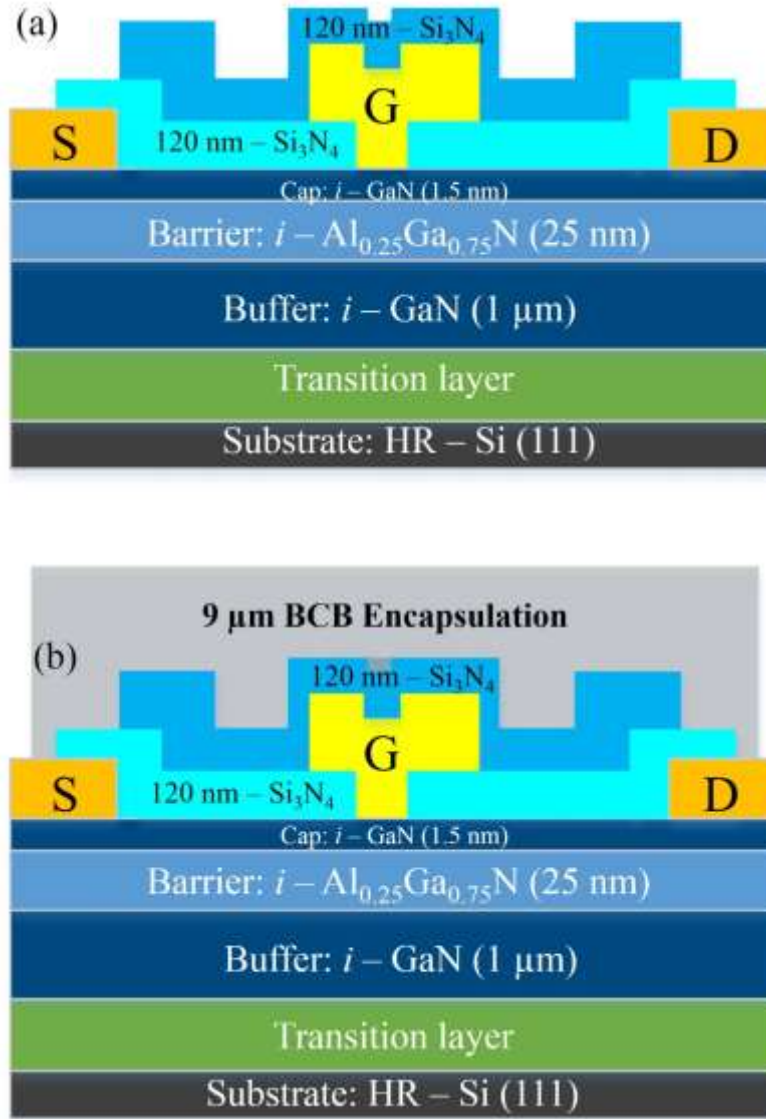


Figure 7.1 Schematic cross sectional view of the fabricated AlGaIn/GaN HEMT on Si substrate (a) without BCB encapsulation, and (b) with 9 μm -thick BCB encapsulation.

The samples after the 120 nm-thick PECVD Si_3N_4 (2nd Si_3N_4) final passivation went through air-bridge formation with 5 μm -thick gold plating process. For comparison, devices on half of the 80 mm wafer were characterized without the BCB encapsulation. The other half wafer went through a 9 μm -thick BCB encapsulation process using a photosensitive BCB

layer by spin-coating followed by the conventional photolithography process. Since the final encapsulation layer is required to completely encapsulate the device structures, including the 5 μm -thick air bridge structures, we have used a 9 μm -thick BCB encapsulation layer. The sample was then oven cured at 280°C for 2 h. The 100% polymerization was confirmed by Fourier transform infrared spectroscopy (FTIR) measurements. Figure 7.2 shows the FTIR spectra measured before and after the curing process. The absorbance signal peak at 1500 cm^{-1} shows a conformational curing after a 2 h baking at 280°C.

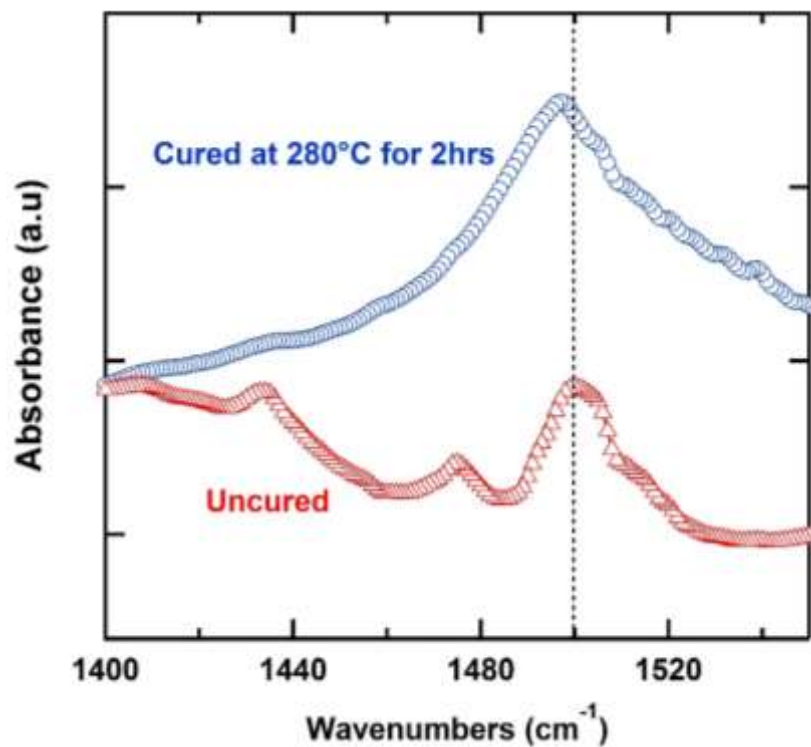


Figure 7.2 FTIR spectra measured before and after the curing of BCB encapsulation.

7.3 Device DC Characteristics

The DC characterization studies were performed using Agilent B1500 .The DC output (I_D - V_D) and transfer (I_D - V_G) characteristics of AlGaIn/GaN HEMTs on Si with and without BCB encapsulation are shown in Fig. 7.3 (a) and (b), respectively.

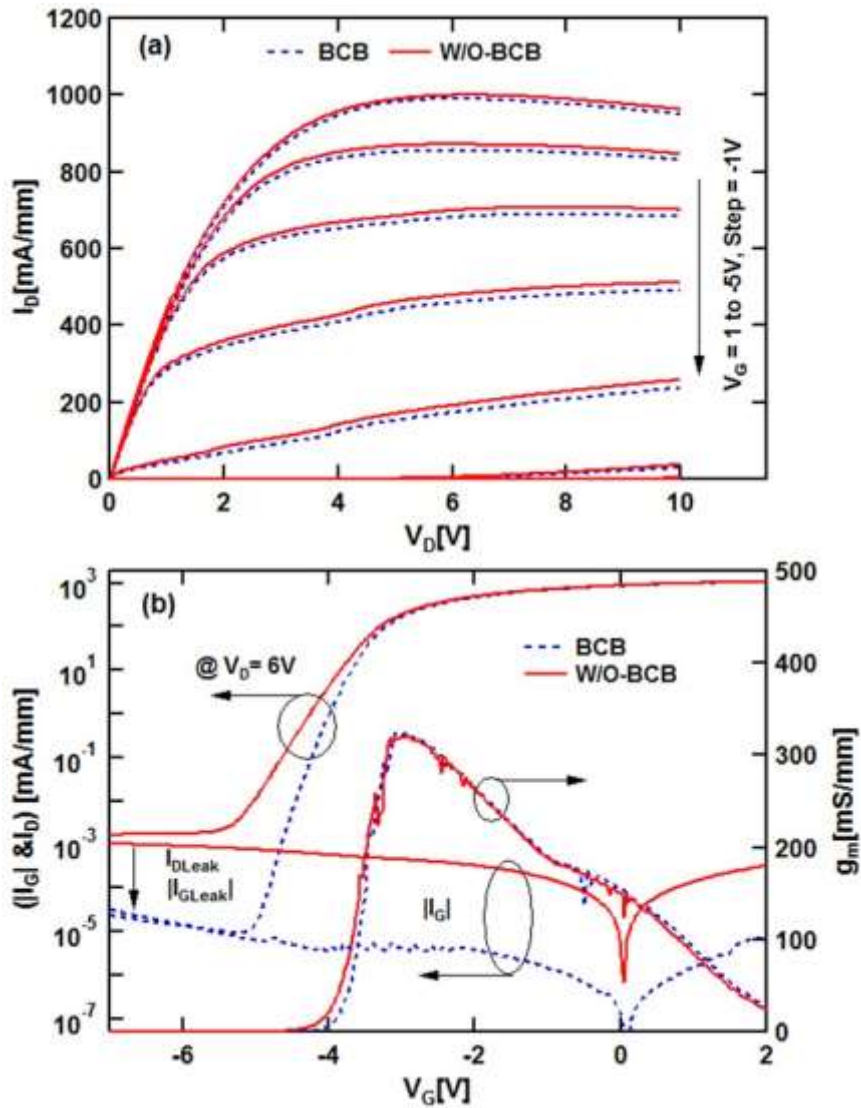


Figure 7.3 (a) I_D - V_D and (b) transfer characteristics of AlGaIn/GaN HEMTs with and without BCB encapsulation. Device dimensions: $L_g/W_g/L_{gd} = 0.15/(2 \times 142)/2.35 \mu\text{m}$.

No considerable changes in the maximum drain current density (I_{Dmax}) or extrinsic transconductance ($g_{m,max}$) could be observed after the 9 μm -thick BCB encapsulation. The threshold voltage (V_{th}) of the devices was also stable at approximately ≈ -3.8 V with and without BCB encapsulation. However, as shown in Fig. 7.3 (b), the BCB encapsulated devices exhibited at least 2 orders of magnitude reduction in the subthreshold drain leakage current (I_{Dleak}) and gate leakage current (I_{Gleak}). The small signal microwave characterization studies were performed using the HP 8510C vector network analyser (VNA). The f_T and f_{max} (maximum oscillation frequency) were extracted from the small-signal microwave characteristics [186] in order to investigate the parasitic effects introduced by the low- k dielectric BCB encapsulation layer. The DC output/transfer and the small signal parameters of four devices with and without BCB encapsulation measured across the wafer for uniformity analysis has been tabulated in Table 7.2.

Table 7.2 DC and microwave parameters of AlGaIn/GaN HEMTs with and without BCB encapsulation. Device dimensions: $L_g/W_g/L_{gd} = 0.15/(2 \times 142)/2.35 \mu\text{m}$.

Device	I_{Dmax} (mA/mm)		V_{th} (V)		g_{mmax} (mS/mm)		f_T (GHz)		f_{max} (GHz)	
	w/o	BCB	w/o	BCB	w/o	BCB	w/o	BCB	w/o	BCB
	BCB		BCB		BCB		BCB		BCB	
1	936	923	-3.47	-3.89	319	299	46	47	47	49
2	1000	990	-3.89	-3.84	320	326	47	52	42	46
3	927	916	-3.84	-3.91	287	282	49	51	43	48
4	950	945	-3.89	-3.78	305	294	47	50	47	46
Average	953	944	-3.77	-3.86	308	300	47	50	45	47
Standard Deviation	32.57	33.37	0.20	0.06	15.44	18.59	1.26	2.38	2.34	1.57

It is evident that the low- k 9 μm -thick BCB encapsulation layer does not introduce any additional parasitic effects that influence the small signal parameters of the devices or the DC characteristics.

7.4 Pulsed I_D – V_D Characteristics

Pulsed I_D – V_D characterization was performed to study the effect of BCB encapsulation on current collapse in the devices. The pulsed I_D – V_D characterization studies were performed using Accent DiVA D265 dynamic I – V analyser. The Q-bias conditions for the pulsed I_D – V_D characterization were: gate-lag (-5, 0) V and gate- and drain-lag (-5, 30) V. The pulse width and pulse separation were 200 ns and 1 ms, respectively. After applying the I_D – V_D , the current I_{DQ} was measured at $V_G = 0$ V and $V_D = 8$ V. The current

I_{DQ0} was similarly measured after a cold Q-bias condition (0, 0) V. Figure 7.4 shows the pulsed I_D - V_D characteristics with (a) gate-lag and (b) gate- and drain-lag condition for the devices with and without BCB encapsulation. The percentage of current collapse obtained from I_{DQ}/I_{DQ0} versus the Q-bias conditions for devices with and without BCB under the gate-lag and gate- and drain-lag is shown in shown in Fig 7.4 (c). The current collapse for the devices increased only by ~3% after BCB encapsulation, which clearly shows that the BCB encapsulation has no significant effect over the dynamic electrical characteristics of the devices.

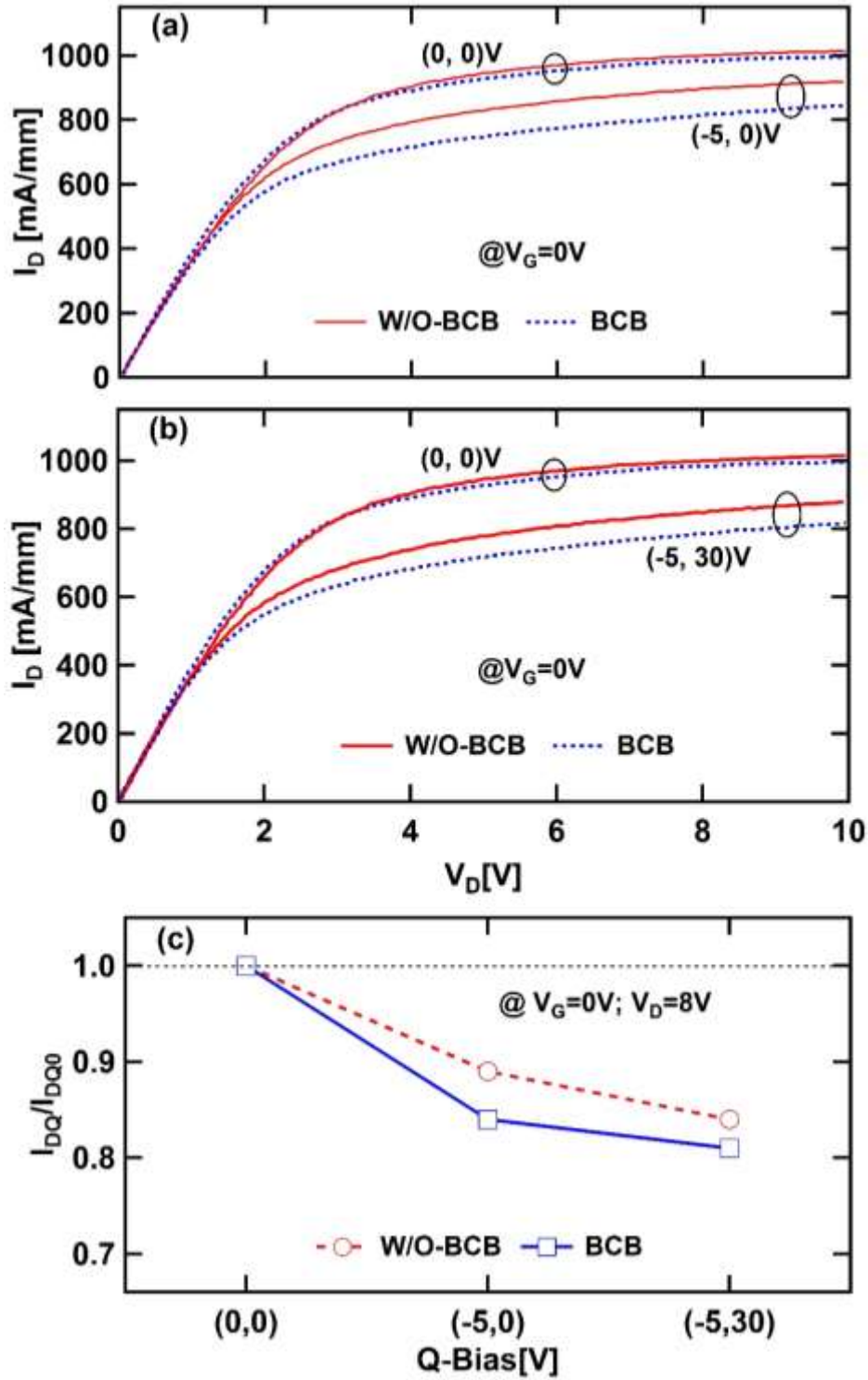


Figure 7.4 Pulsed I_D - V_D characteristics of AlGaIn/GaN HEMTs with and without BCB encapsulation at (a) gate-lag condition, (b) gate- and drain-lag condition, and (c) I_{DQ}/I_{DQ0} versus Q-bias conditions. Device dimensions: $L_g/W_g/L_{gd} = 0.15/(2 \times 142)/2.35 \mu m$.

Furthermore, the fabricated multiple finger devices were also characterized with and without BCB encapsulation. Figure 7.5 shows (a) microscope image (top view) and (b) SEM image of an eight-finger BCB encapsulated AlGaN/GaN HEMT. Visual inspection of the fabricated multi-finger devices shows no deformation or collapse of the air bridge structures after the 9 μm -thick BCB encapsulation.

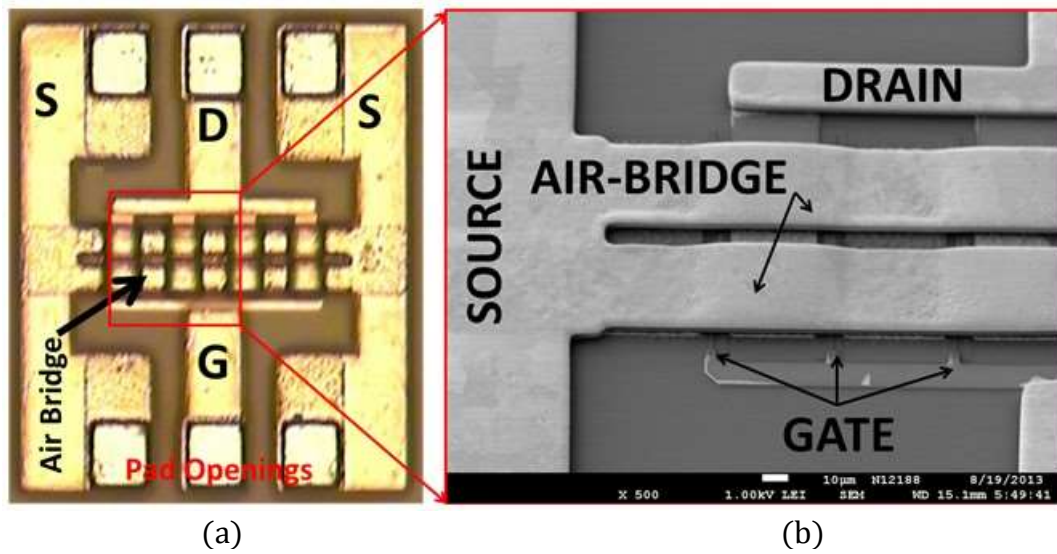


Figure 7.5 (a) SEM image of an eight-finger BCB encapsulated AlGaN/GaN HEMT with pad opened for probing. (b) Zoomed top view SEM image of the BCB encapsulated multi-finger AlGaN/GaN HEMT with air-bridge structures connecting the source electrodes.

The electrical characteristics of the 736 μm multi-finger devices were verified using pulsed $I_D - V_D$ measurement under the cold Q-bias conditions (0, 0) V. The pulsed $I_D - V_D$ method under the cold Q-bias condition was preferred in order to avoid device failure due to very high current density and self-heating related issues. Figure 7.6 shows the pulsed $I_D - V_D$ characteristics measured at a cold Q-bias condition of an eight-finger (8 $\times$ 92 μm) AlGaN/GaN HEMT with and without BCB encapsulation.

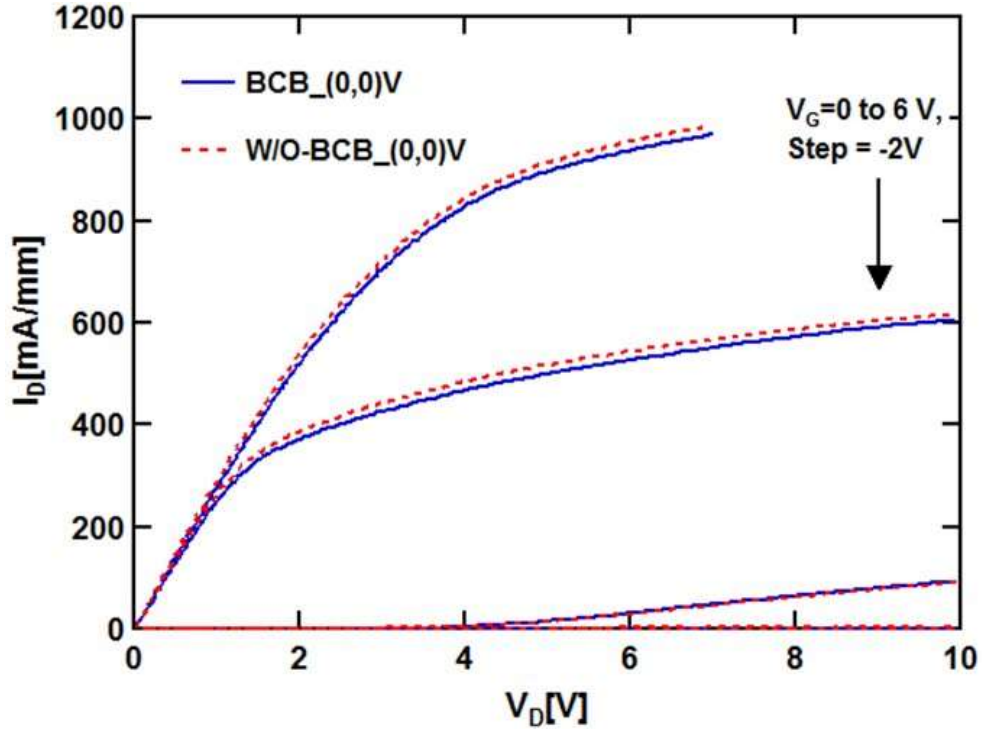


Figure 7.6 Pulsed I_D - V_D characteristics of multi-finger devices. Device dimensions: $L_g/W_g/L_{gd} = 0.15/(8 \times 92)/4 \mu\text{m}$.

The multi-finger devices with and without BCB encapsulation exhibited similar current densities. Moreover, the measured current density closely matched the current density of the 2-finger devices. Thus it was confirmed that the air-bridges were well connected to each sources of the multiple finger devices and the structural stability was not affected after the $9 \mu\text{m}$ -thick BCB encapsulation. The DC output and transfer characteristics of the devices show no variations with and without BCB encapsulation. Since the current density and ON-resistance were unaffected by the BCB encapsulation, we confirmed that the BCB layer does not impose any additional mechanical [183] stress to the device heterostructure.

7.5 OFF-state $B V_{GD}$ Characteristics

The three-terminal OFF-state $B V_{GD}$ characteristics of the devices were measured by ramping up the V_D from an initial 0 V to higher values, while the V_G was maintained at sub-threshold condition of $V_G = -8$ V. The schematic of the circuit showing the three-terminal OFF-state $B V_{GD}$ measurement is shown on Fig. 7.7. The I_D compliance of 1 mA/mm was fixed in order to limit the excessive current from catastrophically destroying the devices. The source terminal was grounded all through the measurements. Devices with different L_{gd} spacing were used for this study.

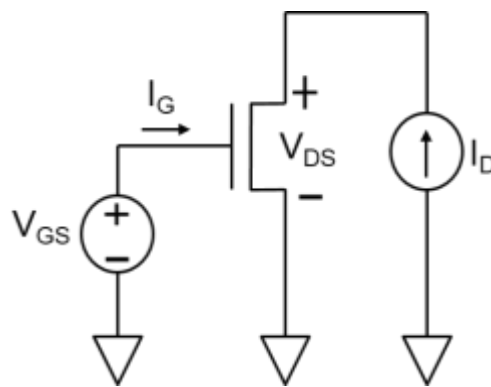


Figure 7.7 Schematic of the circuit representing the three-terminal OFF-state $B V_{GD}$ measurements.

Figure 7.8 (a) shows the three-terminal OFF-state $B V_{GD}$ characteristics of AlGaIn/GaN HEMTs with and without BCB encapsulation and (b) shows the breakdown voltage characteristics of devices as a function of their gate to drain distance. The devices without BCB encapsulation reached the $B V_{GD}$ point well in advance compared to the BCB encapsulated devices. As shown in Fig. 7.8 (a), the $B V_{GD}$ of a device with $L_{gd} = 8$ μm is 66 V without BCB encapsulation, but it increases by at least ~ 2 times reaching 144 V after BCB

encapsulation. A similar trend is also observed as a function of device L_{gd} as shown in Fig 7.8 (b).

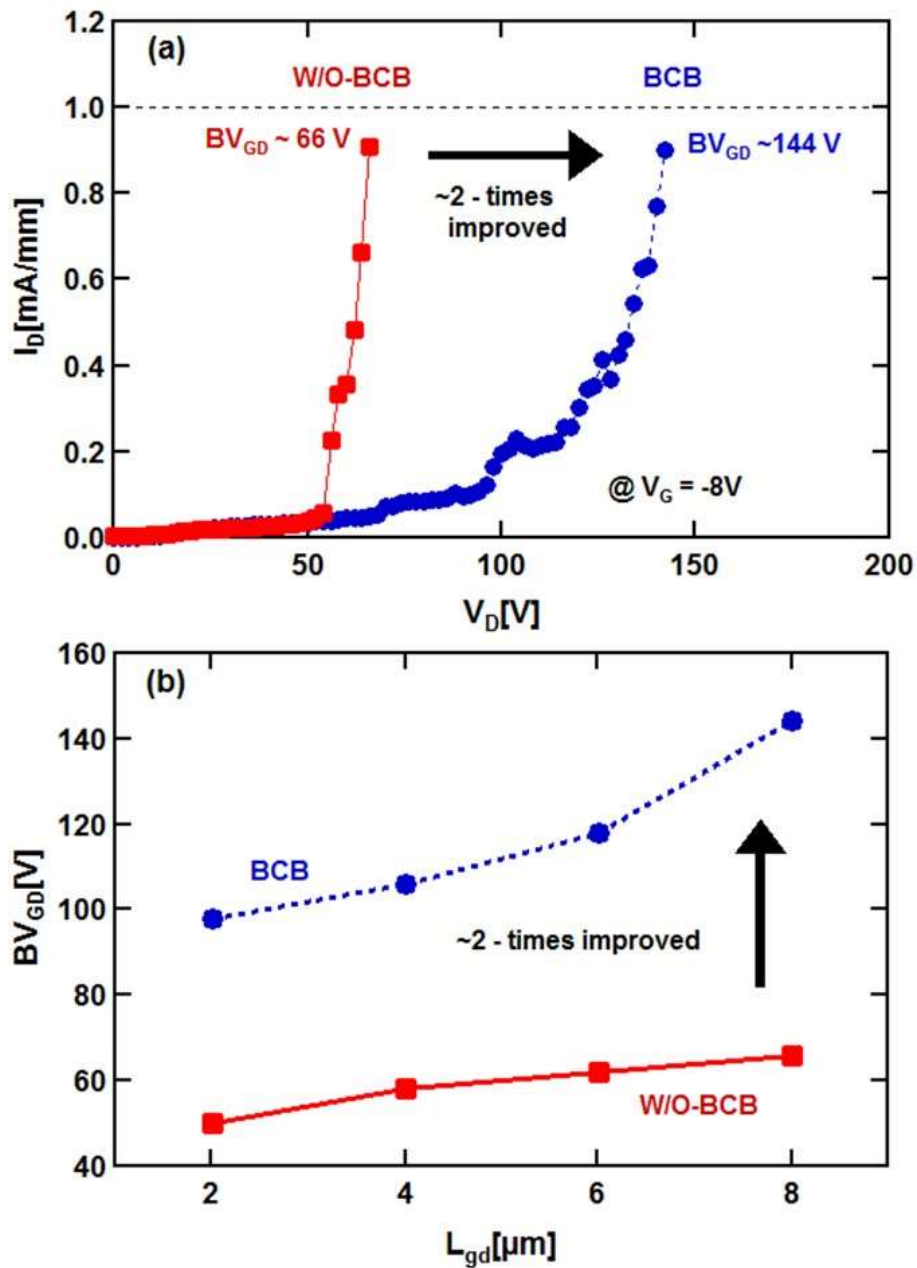


Figure 7.8 (a) OFF-state BV_{GD} characteristics of AlGaIn/GaN HEMTs with and without BCB encapsulation. Device dimensions: $L_g/W_g/L_{gd} = 0.15/80/8 \mu m$, (b) BV_{GD} for AlGaIn/GaN HEMTs with different L_{gd} . Device dimensions: $L_g/W_g = 0.15/80 \mu m$.

7.6 Influence of oven baking

To investigate whether the temperature during BCB curing process has any influence on the device DC characteristics and a subsequent enhancement of BV_{GD} , we subjected the devices without the BCB encapsulation for oven baking at 280°C for 2 hrs which is similar to the BCB curing process. Figure 7.9 shows the DC characteristics of a device without BCB encapsulation before and after subjecting it to the baking test. However, no considerable changes were observed in the DC $I_D - V_D$ characteristics (I_{Dmax} , I_{Dleak} , I_{Gleak} , $g_{m,max}$, and V_{th}) due to the curing process. Thus, we have ruled out the influence of BCB curing process in the reduction of device leakage currents and in the increase of BV_{GD} .

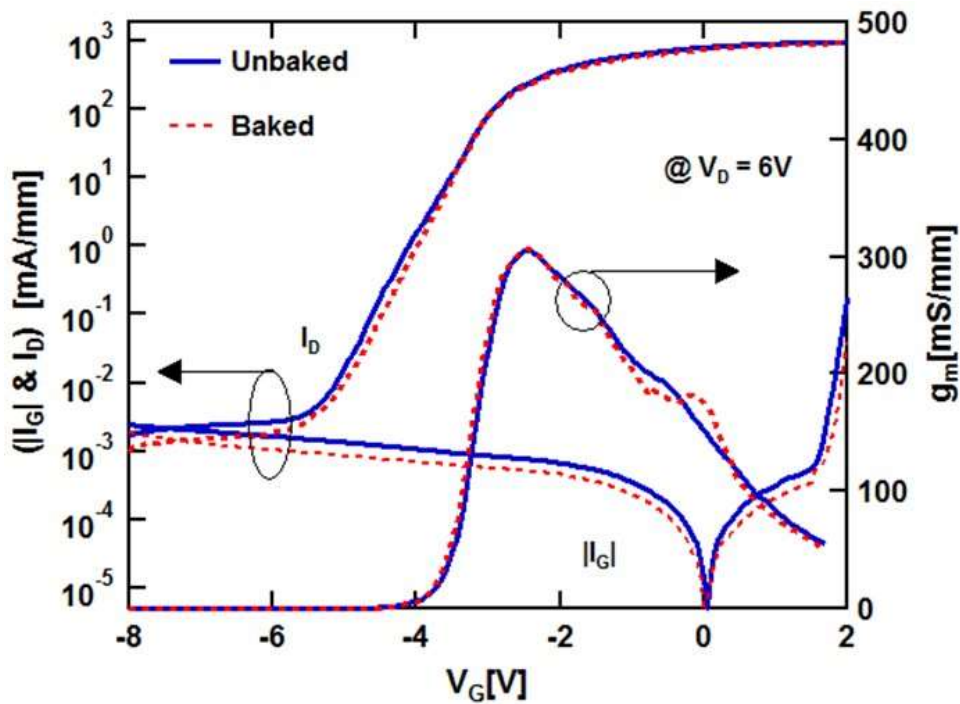


Figure 7.9 DC transfer characteristics of AlGaIn/GaN HEMTs without BCB encapsulation before and after baking at a curing temperature of 280°C for 2 hrs. Device dimensions: $L_g/W_g/L_{gd}=0.15/(2\times142)/2.35\ \mu\text{m}$.

7.7 Leakage Current Studies

Since a considerable decrease in the sub-threshold I_{Dleak} and I_{Gleak} was observed as in Fig. 7.3 (b) for devices with BCB encapsulation, a thorough study of the leakage currents in the devices was carried out. Both three- and two- terminal leakage current studies were performed in devices with and without BCB encapsulation. Figure 7.10 (a) shows the semi-log plot of I_{Dleak} and I_{Gleak} versus V_D by three-terminal measurements. The inset of Figure 7.10 (a) shows the measurement configuration for three-terminal leakage current measurements. For this measurement the gate bias was maintained at sub-threshold voltage of -8 V and the source was grounded. The V_D was ramped from 0 V until it reached a current compliance of 1 mA/mm (i.e. limiting current for B V_{GD}). Both I_{Dleak} and I_{Gleak} were monitored during this measurement. It can be observed that both I_{Dleak} and I_{Gleak} of the devices with and without BCB encapsulation reached the current compliance at the same time. I_{Gleak} can have a major influence on the device B V_{GD} as also reported by other researchers [76][140][187].

In order to study the gate leakage (I_{GLeak}) characteristics, a two terminal reverse gate leakage measurement was performed between the gate and the drain terminals. Figure 7.10 (b) shows the two-terminal I_{GLeak} measured between the gate and the drain terminals. (Inset – the corresponding two-terminal leakage current measurement configuration). The source terminal was allowed to float during these measurements and a negative V_G sweep was performed while the drain terminal was grounded. From the Fig. 7.10 (b), it can be seen that the devices exhibited at least 2 orders of magnitude

reduction in the I_{GLeak} after the BCB encapsulation. Thus we were able to confirm that the BCB encapsulation helps in suppressing the I_{GLeak} of the devices which in turn leads to the enhancement of $B V_{GD}$.

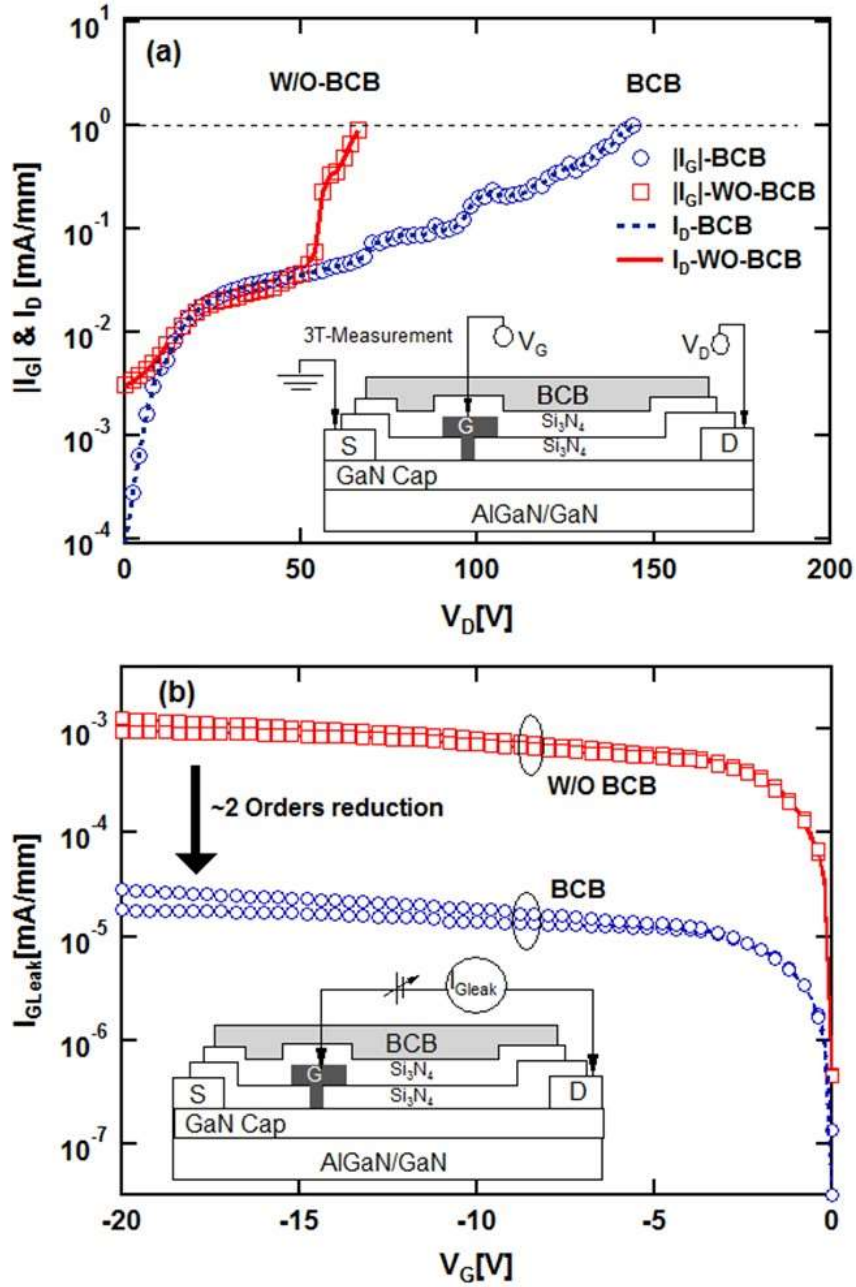


Figure 7.10 (a) Semi-log plot of three-terminal OFF-state I_{GLeak} and I_{DLeak} and (b) two-terminal reverse I_{GLeak} of GaN HEMTs with and without BCB encapsulation. Device dimensions: $L_g/W_g/L_{gd} = 0.15/80/8 \mu m$; Inset – Schematic representation of measurement configuration.

However, it is more important to also identify the leakage path in the devices to understand the role of the BCB encapsulation layer in the reduction of the I_{GLeak} . Since our devices were subjected to $[(\text{NH}_4)_2\text{S}_x]$ treatment followed by the 1st Si_3N_4 passivation layer deposition, the leakage current path is unlikely to exist in the $\text{Si}_3\text{N}_4/\text{GaN}$ interface. A detailed report on the reduction of leakage currents by $[(\text{NH}_4)_2\text{S}_x]$ surface treatment has been presented in the previous work [140]. Similar reduction in the surface leakage currents (I_{Surf}) through proper surface treatments, for example, ammonia (NH_4OH) dip before the deposition of Si_3N_4 passivation layer was also reported by Karouta *et al* [188]. Thus, the most likely leakage path is on the surface of the 2nd Si_3N_4 passivation layer deposited immediately after the gate formation.

7.8 Surface Leakage Currents (I_{Surf})

For the study of I_{Surf} , mesa isolation patterns were used. The I_{Surf} was monitored between the mesa isolation patterns with a 10 μm gap after different process steps. For the two-terminal I_{Surf} measurements, one of the terminals were grounded and the bias sweep of up to 100 V was applied to the other terminal. The different mesa isolation patterns are as shown in Fig. 7.11 (a) with A: (1st Si_3N_4 +2nd Si_3N_4), B: (1st Si_3N_4 +2nd Si_3N_4 +BCB), C: Only BCB and D: Unpassivated. The I_{Surf} thus obtained from the corresponding mesa isolation patterns is shown in Figure 7.11 (b). It can be seen that the mesa isolation pattern with only 1st Si_3N_4 +2nd Si_3N_4 passivation exhibited a very high I_{Surf} .

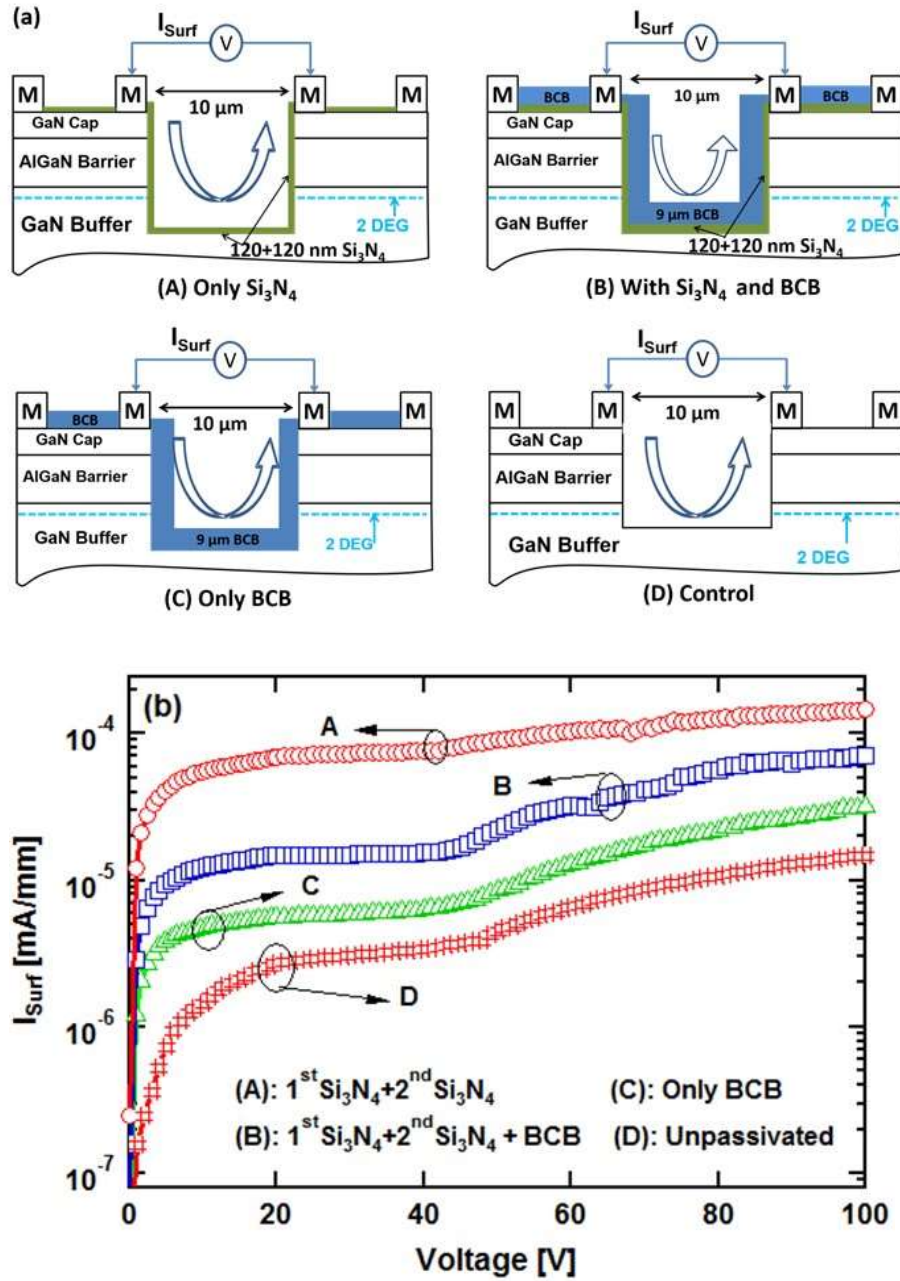


Figure 7.11 (a) Schematic representation of measurement between isolated mesa's with A: (1st Si₃N₄+2nd Si₃N₄), B: (1st Si₃N₄+2nd Si₃N₄+BCB), C: (Only BCB) and D: Unpassivated. (b) I_{surf} measured between the two adjacent isolated mesa's (gap=10 μm; width=50 μm) with A: (1st Si₃N₄+2nd Si₃N₄), B: (1st Si₃N₄+2nd Si₃N₄+BCB), C: (Only BCB) and D: Unpassivated.

With the introduction of the BCB encapsulation layer over the 1st Si₃N₄+2nd Si₃N₄ passivation layers, the I_{surf} reduced by at least one order of magnitude. However, the I_{surf} between two adjacent mesa isolation patterns with only BCB encapsulation was as low as the I_{surf} of the un-passivated (without Si₃N₄ passivation and BCB encapsulation) patterns. Based on the experimental results, the source of the I_{surf} can be attributed to the surface of the second layer of PECVD deposited Si₃N₄. This I_{surf} component can be also present during the I_{leak} and I_{dleak} measurements which in turn affects the break down characteristics of the devices. Similarly, Tan et al [189] has also realized the increase of I_{surf} in the GaN HEMTs after Si₃N₄ passivation. [Various reports that demonstrate the role of BCB in the reduction of surface leakage currents can be found in literature \[190\]–\[192\].](#) In our case, the BCB encapsulation layer has suppressed the I_{surf} that was present on the surface of the 2nd Si₃N₄ layer thus resulting in ~2 times enhancement in the B V_{GD} of AlGa_{0.2}N/GaN HEMTs.

7.9 Summary

The influence of a low- k dielectric BCB encapsulation on the electrical performance of AlGa_{0.2}N/GaN HEMTs on Si substrate was investigated. Even after the 9 μm -thick BCB encapsulation layer, no degradation of device drain current density, extrinsic transconductance and small signal microwave performances was observed. However, the leakage currents (I_{leak} and I_{dleak}) were suppressed by at least two orders of magnitude in the BCB encapsulated devices. In addition, the air-bridge was also structurally stable, intact and well connected with the sources of the device. Subsequently, a two

order of magnitude enhancement in the BV_{GD} was observed in devices with BCB encapsulation. Through experimental methods, we were able to confirm that the BCB encapsulation was able to effectively suppress the I_{surf} that was present on the surface of the 2nd Si₃N₄ layer, consequently resulting in enhanced device BV_{GD} of the devices. Hence, the low- k dielectric BCB encapsulation is believed to be a viable solution to protect AlGaN/GaN HEMTs and its integrated circuits.

Chapter 8

Conclusions and Recommendations for future work

8.1 Conclusions

AlGaN/GaN HEMTs are promising for high-performance robust power and communication electronic systems. The superior properties of the GaN based material system allow it to be exploited in applications requiring extreme operation conditions. However, for a technology to be fully commercialized, it is necessary to establish a consistent and a long-term reliable performance record. Thus, great efforts are spent in order to study and understand the various failure mechanisms that undermine the reliability of the technology. In this thesis, a comprehensive study and analysis of the trapping based failure mechanisms of AlGaN/GaN HEMTs on Si has been presented.

In this thesis we have presented our work on trap analysis in AlGaN/GaN HEMTs on Si, which aims to add on to the further understanding of the source, location and the various consequences of trapping under operating conditions.

To understand the influence of the electric-field on the location of trapping based on fully-OFF-state stress conditions, the effects of high-electric-field on the important parameters such as the $\text{dyn-}R_{\text{DS[ON]}}$ and the V_{th} of GaN HEMTs were investigated for the first time. We have analysed the current collapse by treating the dispersion in the linear and the saturation region of pulsed $I_{\text{D}}-V_{\text{D}}$ characteristics as two separate events. The pulsed gate- and drain-lag ($I_{\text{D}}-V_{\text{D}}$) measurements and pulsed transfer ($I_{\text{D}}-V_{\text{G}}$) characteristics were used to quantify the current collapse and $\text{dyn-}R_{\text{DS[ON]}}$ degradation. Using the temperature-dependent current-transient technique, we have identified a trap energy level with an activation energy (E_{a}) of 0.33 ± 0.05 eV present in the AlGaN barrier which was responsible for the current dispersion in these devices. The results were verified using the TCAD simulations.

To study the trapping mechanism due to the buffer related traps, temperature-dependent current-transient technique using fully-ON-state stress ($V_{\text{D[ON]_Stress}}$) conditions were performed on GaN HEMTs. We obtained different E_{a} 's for different $V_{\text{D[ON]_Stress}}$ conditions. The time constants exhibited a linear dependency on the applied $V_{\text{D[ON]_Stress}}$ conditions. Using Arrhenius analysis we obtained six different E_{a} 's corresponding to six different $V_{\text{D[ON]_Stress}}$ conditions. We also claimed that the obtained E_{a} 's were an effective activation energies ($E_{\text{a,eff}}$) corresponding to different energy levels in the continuous distribution of trap energy (DTE) function activated by different $V_{\text{D[ON]_Stress}}$. In order to validate this observation using TCAD 2-D numerical transient simulations, we have incorporated the experimentally determined trap parameters into a multi-trap energy (MTE) model in

contrast to the conventional single-trap energy (STE) model. We have also verified our claim by proposing a physical model behind this observation using mathematical interpretations and band energy representations.

To reduce the gate-leakage currents, bilayer SiN(5-nm)/Al₂O₃(5-nm) gate dielectric stack-based AlGa_N/Ga_N MISHEMTs were fabricated. Enhanced device performance with 60 % drain current collapse suppression was thus realized. In addition, we have also confirmed that a low interface state density ($D_{it}=6.39\times10^{10} \text{ cm}^{-2}\text{eV}^{-1}$) in the metal-oxide-semiconductor interface lead to the suppression of current collapse.

To improve the reliability of the fabricated Ga_N HEMTs, low- k dielectric BCB encapsulation was used as the final passivation layer. Though the HEMTs were passivated with SiN, the additional BCB encapsulation helps to reduce the surface leakage current (I_{surf}) by 2 orders of magnitude without affecting the drain current collapse and high-frequency performances. Due to the reduction of I_{surf} in BCB encapsulated AlGa_N/Ga_N HEMTs, ~2 times higher BV_{GD} was observed.

8.2 Key Contributions of this work

- For GaN HEMTs operating as high-power switches, $\text{dyn-}R_{\text{DS[ON]}}$ degradation is a prime issue to be addressed. By using OFF-state stress studies, we have identified the trap locations and the trap activation energy that causes $\text{dyn-}R_{\text{DS[ON]}}$ degradation. Furthermore we have reported for the first time the influence of electric-field on the location of trapping. This understanding will help the optimization of the device structure (e.g. field plates) as well as the epi growth properties (e.g. doping concentration, lattice matching components etc) which can address the electric-field related trapping phenomenon in the gate-drain access region of the AlGaIn/GaN HEMTs on Si substrate.
- Using a series of ON-state stress conditions, we subjected the GaN HEMT devices to hot-electron effects and presented its influence on V_{th} and $\text{dyn-}R_{\text{DS[ON]}}$. This fully-ON-state test condition lead to the identification of a Distribution of Trap Energy (DTE) levels in the GaN buffer region. We have thus unambiguously showcased the presence of DTE in the GaN buffer.
- Based on the identification of DTE in the GaN buffer, we incorporated a Multi-Trap Energy (MTE) model in the TCAD environment. We were thus able to ascertain that such DTE gives rise to an effective E_a which is bias dependent. Thus the MTE model will give the circuit designers a guideline for the safe operating area (SOA) of the devices designed for high-power applications.

- By employing a SiN/Al₂O₃ bilayer gate dielectric stack in AlGaN/GaN MISHEMT, we were able to achieve one order reduction of the gate-leakage current and a suppression of current collapse by 60% when compared to conventional Schottky gated HEMTs. We attribute the current collapse suppression to the reduction of interface-state density in metal-insulator-semiconductor interface.
- By BCB encapsulation of the Si₃N₄ passivated AlGaN/GaN HEMTs, the surface leakage currents that prevailed after device passivation were mitigated by at least two orders. This subsequently led to a two times enhancement of the device B V_{GD} .

8.3 Recommendations for Future Work

GaN's ability to withstand a critical electric field of 3 MV/cm has led to its deployment in very high voltage applications. While operating at very high voltages, GaN HEMTs are subjected to the influence of high electric fields. Especially, the peak electric field at the drain side gate edge of GaN HEMTs pose a serious threat to its reliability. Punch-through, tunnelling, hot-electron effects, defect formation, surface pitting, trapping etc. are some of the deleterious effects of high electric field. We have presented the influence of electric field on the location of trapping in Schottky gated GaN HEMTs using OFF-state stress conditions. This study can further be extended towards MISHEMTs, where tunnelling of gate electrons is not crucial due to gate insulation. The electric field distribution will also be different in MISHEMTs, thus making it an interesting area to be explored.

The complexities involved in the growth and fabrication of GaN based HEMTs lead to various anomalies that affect the performance of the devices. In particular, the discrepancies involved in the heterostructure growth manifests itself as point defects, traps, dislocations etc. The GaN buffer layer hosts various defect states and traps that require severe scrutiny. The ON-state stress based investigation which depended on hot electron effects helped us to identify the presence of DTE in the GaN buffer layer. Since the GaN buffer layer properties are highly dependent on growth parameters, it would be useful and relevant to extend this study by comparing MBE and MOCVD grown epi-layers.

The immediate unavailability of native GaN substrates has led to the growth of AlGaIn/GaN heterostructures on foreign substrates such as sapphire, SiC and Si. However, these lattice mismatched substrates give rise to threading dislocations leading to the formation of trap states. A comparison study of the DTE in GaN buffer grown on different substrates can help us further understand the effects of the lattice parameters on the trapping phenomenon. This also further leads to the question of how the devices fabricated from lattice-matched epi structures perform. Thus extending the same study on lattice matched structures can give better insights on the other trapping mechanisms devoid of dislocations.

So far, we have studied the trapping effects on D-mode devices using our proposed techniques. These techniques can be also extended to E-mode (normally-OFF) GaN HEMTs or MISHEMTs. Because high breakdown voltage E-mode devices plays major role for power switching devices.

List of Publications

Journals (as first author):

1. M. J. Anand, G. I. Ng, S. Arulkumaran, K. Ranjan, S. Vicknesh and K. S. Ang, “*Reduction of Current Collapse in AlGa_N/Ga_N MISHEMT with Bilayer Si₃N₄/Al₂O₃ Dielectric Gate Stack*”, Physica Status Solidi (C) 10, pp. 1421–1425 (2013).
2. M. J. Anand, G. I. Ng, S. Arulkumaran, K. Ranjan, S. Vicknesh and K. S. Ang, “*Low k -dielectric benzocyclobutane encapsulated AlGa_N/Ga_N HEMTs with Improved off-state breakdown voltage*”, Japanese Journal of Applied Physics 54, 036504 (2015).
3. M. J. Anand, G. I. Ng, S. Arulkumaran, C. M. M. Kumar, K. Ranjan, S. Vicknesh, S. C. Foo, B. Syamal and X. Zhou, “*Effect of OFF-state stress induced Electric Field on Trapping in AlGa_N/Ga_N HEMTs on Si (111)*”, Applied Physics Letters 106, 083508 (2015).
4. M. J. Anand, G. I. Ng, S. Arulkumaran, B. Syamal and X. Zhou, “*Studies of Trap Energy Level Distribution in AlGa_N/Ga_N high-electron-mobility transistors on Si under ON-state stress*”, Applied Physics Express 8, 104101 (2015).

Journals (as contributor):

1. G. Ye, H. Wang, S. Arulkumaran, G. I. Ng, R. Hofstetter, Y. Li, M. J. Anand, K. S. Ang, Y. K. T. Maung and S. C. Foo, “*Atomic layer deposition of ZrO₂ as gate dielectrics for AlGa_N/Ga_N metal-insulator-semiconductor high electron mobility transistors on silicon*”, Applied Physics Letters, 103, 142109 (2013).

2. Y. Li, G. I. Ng, S. Arulkumaran, C. M. M. Kumar, K. S. Ang, M. J. Anand, H. Wang, R. Hofstetter and G. Ye, "*Low Contact Resistance Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contacts on Un-doped AlGa_N/Ga_N High-Electron-Mobility Transistors Grown on Silicon*", Applied Physics Express 6, 116501 (2013).
3. Y. Li, G. I. Ng, S. Arulkumaran, G. Ye, C. M. M. Kumar, M. J. Anand, and Z. H. Liu, "*Conduction mechanism of non-gold ohmic contact in AlGa_N/Ga_N high-electron-mobility transistors*", Applied Physics Express 8, 041001 (2015).

Conferences (as first author):

1. M. J. Anand, G. I. Ng, S. Arulkumaran, S. Vicknesh, and S. C. Foo, "*Trapping Analysis by Pulsed Current-Voltage Characteristics for AlGa_N/Ga_N HEMTs on 4-inch Si (111)*", ISPlasma 2012, Chubu University, Japan.
2. M. J. Anand, G. I. Ng, S. Arulkumaran, H. Wang, Y. Li, S. Vicknesh, and T. Egawa, "*Low specific ON-resistance and high Figure-of-merit AlGa_N/Ga_N HEMTs on Si substrate with non-gold metal stacks*", Device Research Conference (DRC), 23-26 June 2013, Notre Dame.
3. M. J. Anand, S. Vicknesh, G. I. Ng, and S. Arulkumaran, "*Suppression of Current Collapse with bilayer Si₃N₄/Al₂O₃ gate dielectric in AlGa_N/Ga_N Metal-Insulator-Semiconductor High-Electron-Mobility Transistors on Si (111)*" ISCS, 19-23 May 2013, Kobe, Japan.
4. M. J. Anand, G. I. Ng, S. Arulkumaran, K. Ranjan, S. Vicknesh and K. S. Ang, "*Enhanced OFF-state breakdown voltage in AlGa_N/Ga_N HEMTs*"

on Si with low-k Benzocyclobutane (BCB) Encapsulation", ICNS, 25 – 30 August 2013, Washington DC, USA.

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1. S. Arulkumaran, G. I. Ng, S. Vicknesh, C. M. M. Kumar, M. J. Anand, H. Wang, K. S. Ang, S. L. Selvaraj, W. Z. Wang, G.-Q. Lo, S. Tripathy, "*Uniformity Studies of AlGa_N/Ga_N HEMTs on 8-in Diameter Si (111) Substrate*", International Conference on Compound Semiconductor Manufacturing Technology (CSMANTECH); USA, May 2013.
2. Y. Li, G. I. Ng, S. Arulkumaran, C. M. M. Kumar, K. S. Ang, H. Wang, G. Ye, R. Hofstetter, and M. J. Anand, "*Investigations of CMOS-compatible Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contact for AlGa_N/Ga_N HEMT on Si with Low Contact Resistance*", International Conference Nitride Semiconductors (ICNS), USA, August 2013.
3. Y. Li, G. I. Ng, S. Arulkumaran, C. M. M. Kumar, K. S. Ang, H. Wang, G. Ye, R. Hofstetter, and M. J. Anand, "*Contact Mechanism and Temperature studies of Non-Gold Ta/Si/Ti/Al/Ni/Ta Ohmic Contact for AlGa_N/Ga_N HEMT on Si*", International Workshop on Nitride Semiconductors (IWN), Poland, August 2014.

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