Silicon Backplane Design for OLED-on-Silicon Microdisplay

WANG YING

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University in

fulfillment of the requirement for the degree of Master of Engineering

2011

STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Wang Ying

Acknowledgments

With a deep sense of gratitude, I wish to express my sincere thanks to my supervisor, Associate Professor Sun Xiao Wei, for his continuous insight, enthusiasm and encouragement. His deep passion for various scientific problems has taught me a lot. His guidance during the development of my research has been invaluable. I also would like to thank Dr. Gu Jiang Min, Mr. Zhang Liang, Dr. Shi Xiao Meng, Dr. Wang Chao, Dr. Luo Jian Wen, and Mr. Fan Zhong Cheng. Their professional attitudes, continuous supports and management skills deserve special acknowledgment. I would like to extend my special thanks to people at Nanoelectronic Lab have contributed to this work. I had the most wonderful learning experience working with a team of very active and bright Ph.D. and master students. It would have been impossible to achieve these research results without the consistent technical support of Mrs. Neo Bee Geok and Mr. Hasman Bin Hassan at Nanoelectronic Lab I, Mrs. Seow-Guee, Geok and Mrs. Leong-Tan Min Lin at IC Design Lab II, and Mr. Goh Mia Yong, Jimmy at Center for Integrated Circuit & System.

I will never find words enough to express the gratitude that I owe to my family in China. Tender love and support from my parents, my brother and my sister-in-law, especially my cute niece, have always been the cementing force for building the blocks of my research. Finally, I also want to thank my dear friends: Mr. Xie Zi Li, Ms. Li Dan, and Ms. Jia Ying and others who encourage and inspire me and never abandon me for all the time.

Abstract

Microdisplay technology has attracted the attention as projection displays and near to eye (NTE) displays due to its advantages of high resolution, tiny physical display size and low power consumption. Combined with complementary metal oxide semiconductor (CMOS) technology, several display technologies are employed to implement a microdisplay application, such as liquid crystal or electroluminescent display. Compared with liquid crystal on silicon (LCoS) technology, organic light emitting diode (OLED) microdisplay technology is more attractive as the NTE display because of its simple optics, high luminance, fast response and ultra low power dissipation. With CMOS technology, complex circuitry is integrated into the silicon backplane to realize compact OLED-on-Silicon microdisplay.

The research work is to exploit and develop efficient circuit architecture of the silicon backplane for OLED-on-Silicon microdisplay. The design of the silicon backplane must fulfill the characteristics of the display technology. The luminance of OLEDs is proportion to the driving current density, so proper current signals are expected to be generated for the OLEDs. The challenge mainly lies in the extremely small current for low level gray scale. Accurate current signal processing technologies are employed in the design of the silicon backplane.

First, based on the reviews of the active matrix OLEDs (AMOLEDs) employing amorphous silicon (α-Si) and poly-silicon (poly-Si), voltage driving scheme and current driving scheme are the two main technologies used in the pixel circuit design. We develop a current driving pixel circuit because of the linear relationship

between the driving current and the display luminance. Compensation technology is employed to satisfy the current accuracy at low gray scale level, and usually the pixel current is as low as several hundreds of nano amperes. In comparison with conventional current driving pixel circuit based on the current copier, we show that the proposed pixel circuit fits the design targets and shows good circuit performance even at the low current level.

Secondary, since the input display data is digital signal, digital to analog converter (DAC) is required to transform the input digital display data into analog current signal. Current mode DACs are preferable when current driving scheme is employed in the pixel circuit design. For a successful microdisplay, the chip area is one key consideration. A current mode DAC based on the current dividing operation is proposed to optimize the chip area. Compared with the common binary-weight current steering DAC with the same resolution, the chip area noticeably decreases and the performance of the proposed DAC achieves the design objectives.

Finally, a prototype with the resolution of 160×120 is implemented based on Semiconductor Manufacturing International (Shanghai) Corporation (SMIC) 0.35μm custom silicon process.

Table of Contents

List of Figures

List of Tables

Acronyms and Symbols

Abbreviations

α-Si	Amorphous Silicon
AMOLED	Active Matrix Organic Light Emitting Diode
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip on Board
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
ETL	Electron Transporting Layer
HMD	Head Mounted Display
HTL	Hole Transporting Layer
HS	Horizontal Synchronization
INL	Integral Non-Linearity
ITO	Indium Tin Oxide
LCoS	Liquid Crystal on Silicon
LSB	Least Significant Bit

MIM	Metal Insulator Metal
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NTE	Near to Eye
OLED	Organic Light Emitting Diode
PIP	Poly Insulator Poly
POLED	Polymer Organic Light Emitting Diode
Poly-Si	Poly Silicon
rms	*root mean square*
SMIC	Semiconductor Manufacturing International (Shanghai) Corporation
SMOLED	Small Molecule Organic Light Emitting Diode
TFT	Thin Film Transistor
VGA	Video Graphics Array
VS	Vertical Synchronization

Symbols

C_{gd}	Gate to drain overlap capacitance

C_{gs}	Gate to source overlap capacitance
C_{OX}	Oxide capacitance per unit area
C_s	Storage capacitor of the pixel circuit
D_k	Digital input of DAC
E_{gain}	Gain error of DAC
E_{off}	Offset error of DAC
GND	Ground
g_m	Small signal transconductance
I_d	Drain current of MOS transistor
I_{data}	Input data current of the pixel circuit
I_{OLED}	Driving current for OLEDs
I_{ref}	Reference current
L	Length of MOS transistor
Q_s	Stored charge in the storage capacitor of the pixel circuit
SW	Switch signal
$\overline{SW}$	Complementary switch signal

VDD	Power supply signal
V_{bias}	Bias voltage
V_{ds}	Source to drain voltage of MOS transistor
V_{eff}	Effective gate to source voltage
V_g	Gate voltage of MOS transistor
V_{gs}	Gate to source voltage of MOS transistor
V_{LSB}	Voltage change when on LSB changes
V_{ref}	Reference voltage
V_t	Threshold voltage of MOS transistor
V_{TN}	Threshold voltage of NMOS transistor
V_{TP}	Threshold voltage of PMOS transistor
W	Width of MOS transistor
$Y_k^{'}$	Actual analog output value of DAC
Y_k	Ideal analog output value of DAC
λ	Channel length modulation factor of MOS transistor

μ	Mobility of MOS transistor
μ_{eff}	Effective mobility of MOS transistor

Chapter 1

Introduction

1.1 Background and Motivation

Microdisplay is a general term for a display system with a typical display screen size of less than 1.5" in diagonal. It is often used for projection and near to eye (NTE) displays. Head mounted display (HMD) and liquid crystal on silicon (LCoS) TV are examples of the existing microdisplay applications. Microdisplays are regarded as the combination of the display technology and the complementary metal oxide semiconductor (CMOS) technology to induce a compact display system with low overall system cost. The display devices are deposited on the CMOS silicon backplane to produce an information-rich, high performance and compact microdisplay. [1] [2]

Organic light emitting diode (OLED) technology shows its attractiveness for a microdisplay application, especially for NTE display. First, OLED technology is kind of emissive display so the backlight is no longer required when it is used to implement a microdisplay application. Second, the fast responce rate of OLED devices enables the fast switching ability of OLED-on-Silicon microdisplay. Furthermore, the attraction of OLED technology includes the low power consumption. This is important for portable or wearable, battery-powered display applications because it is possible to prolong battery life or the use of smaller and lighter batteries. [2]

Compared with the amorphous silicon (α-Si) backplane and the poly silicon (poly-Si) backplane which are the two common technologies used in the active matrix OLED display (AMOLED), the CMOS technology shows its advantages to be integrated in a microdisplay application, especially the NTE display system. First, the smooth surface of the CMOS process is a perfect contact interface for the OLED layers. Second, the compaction and complexity of the CMOS circuit lead to the small pixel-pitch of microdisplay which results in small driving current. The extremely small current for the pixel circuit leads to lower power dissipation. Third, the mature CMOS industries provide a low manufacture cost, especially massive product.

Based on studies and summarizes of the features of both the OLED technology and the CMOS technology, the combination of these two technologies illustrates the possibility of a successful microdisplay application. The motivation to investigate and develop a silicon backplane is to provide a design strategy of a practical OLED-on-Silicon microdisplay. Nowadays, the OLED-on-Silicon microdisplay is less mature and developed than LCoS microdisplay. The challenges of the research work mainly lie in two aspects. First we must consider the precise current process and the compensation in the circuit design which also lie in the conventional OLED direct view. Second the tight circuit structure is notable based on the specific requirement of the microdisplay application. We aim at providing a design methodology to solve the similar situation when the silicon backplane is expected for a new microdisplay application.

1.2 Objectives

The main objective of the research work is to explore and apply a design of the silicon backplane for the OLED-on-Silicon microdisplay.

The specifications for the OLED-on-Silicon microdisplay application require special design considerations. First, the chip area is expected to be as small as possible to satisfy the portable and wearable display application of the microdisplay. Second, owing to the proportional relation of OLED display luminance and the driving current density, accurate current signal processing technology is one important topic we face in the design of the silicon backplane.

1.3 Major Contributions

In this thesis, two main contributions are presented for the implementation of the silicon backplane for OLED-on-Silicon microdisplay employing the active matrix addressing technology and the current driving scheme. First, an efficient pixel circuit architecture for the current driving scheme is developed. Compensation technology is introduced in the pixel circuit design. Compared with the conventional pixel circuit based on a current copier, the performance of the proposed pixel circuit is noticeably improved. Second, a current mode digital-to-analog converter (DAC) is investigated upon the current dividing operation to provide the display current data for the pixel circuit. With such circuit architecture, the chip area of the proposed current mode DAC greatly decreases in comparison with the binary-weighted current mode DAC of the same resolution.

1.4 Thesis Organization

Seven chapters constitute this thesis.

The motivations and objectives of the research work are introduced in Chapter 1.

In Chapter 2, an overview of the OLED-on-Silicon microdisplay technology is presented. The basic operation principle and the practical device structure of OLEDs are addressed. Then, we focus on features of CMOS technology for the microdisplay application. For the backplane of a microdisplay application, the comparison of CMOS technology, α-Si technology and poly-Si technology is analyzed. Next, the basic operation of the metal oxide semiconductor (MOS) transistors is studied for the silicon backplane design of the OLED-on-Silicon microdisplay. Finally, design considerations are presented based on the features of the OLED microdisplays.

The addressing circuit of the OLED-on-Silicon is implemented in Chapter 3. Functional block diagram is presented to explain the data process of the OLED-on-Silicon microdisplay. A D type flip-flop is the key element of the addressing circuit, so the optimization of the D type flip-flop assists to improve the circuit performance. With the standard cells of the CMOS foundry, an efficient and compact circuit layout is implemented according to the design guidelines of the mixed-signal integration circuit. The simulation results of an 8 × 8 diagram indicate that the addressing circuit which works properly and satisfies the design objectives.

The design of the pixel circuit for the OLED-on-Silicon microdisplay is stated in Chapter 4. Both the voltage driving scheme and the current driving scheme are

used for AMOLED pixel circuit implementation. Based on the reviews of AMOLED pixel circuit, we choose the current driving scheme in our design. The designed pixel circuit with compensation technology produces the proper current to drive the OLEDs. Simulation results of the proposed pixel circuit and the conventional current driving circuit indicate the advantages of the proposed architecture.

The current mode DAC is implemented to provide the required driving current for the OLED pixel circuit. In Chapter 5, the design of the current mode DAC is presented. The design considerations are introduced by analyzing the features of current mode DACs. A current mode DAC based on the current dividing operation is proposed with smaller chip area for a microdisplay application.

The photograph and the measurement results of the prototype of the silicon backplane for a 160 × 120 OLED-on-Silicon microdisplay are presented in Chapter 6.

In Chapter 7, conclusions are drawn and recommended work for the future are described in detail.

Chapter 2

OLED-on-Silicon Microdisplay

2.1 Introduction

OLED technology was first introduced by Tang and Van Slyke of Kodak in 1987 [3] and has been studied extensively as an important flexible display technology in the recent years. OLEDs used for both large area flexible display and direct view mobile display have been studied in references [4-13].

OLED-on-Silicon microdisplays have drawn attention in recent years. They perfectly combine mature CMOS technology with a promising OLED technology. Some successful designs have been turned into commercial product [14-18]. For microdisplay applications, OLED technology is a natural choice for NTE display due to its advantages, such as fast response, high luminance, high contact ratio, thin structure, *etc* and low temperature processing.

2.1.1 Basic Operation of OLEDs

The basic theory of organic materials, including material classification, the physical phenomenon, device structure and applications are documented in [3] [19-26].

The conventional bottom emitting structure of small molecule OLEDs (SMOLEDs) is shown in Figure 2.1. Indium tin oxide (ITO) layer is deposited on the glass substrate as the transparent anode to allow the light to pass through the device. The metals, such as Mg or Ag, are used as the cathode. Two organic layers are inserted

into the two electrodes, and these two organic layers are the hole transporting layer (HTL) and electron transporting layer (ETL). Holes and electrons are transported by the HTL and ETL respectively.

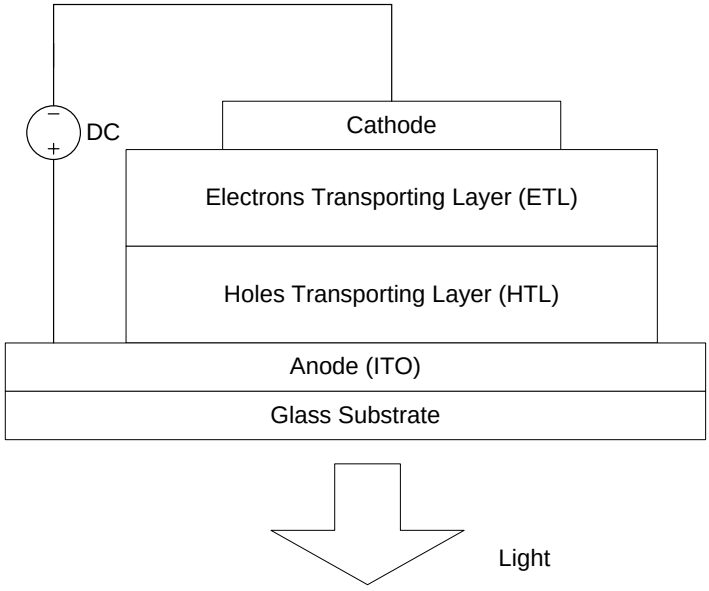


Figure 2.1 The basic bottom emitting OLED structure

Light emission from hole-electron recombination is the basic physical process for OLED display, indicated in Figure 2.2. When the electric field is applied to the OLED device, positive and negative carriers are injected from the electrodes and transported in the organic layers. The holes and the electrons recombine at the interface of HTL and ETL to produce light. The light is transmitted through the ITO glass as shown in Figure 2.1.

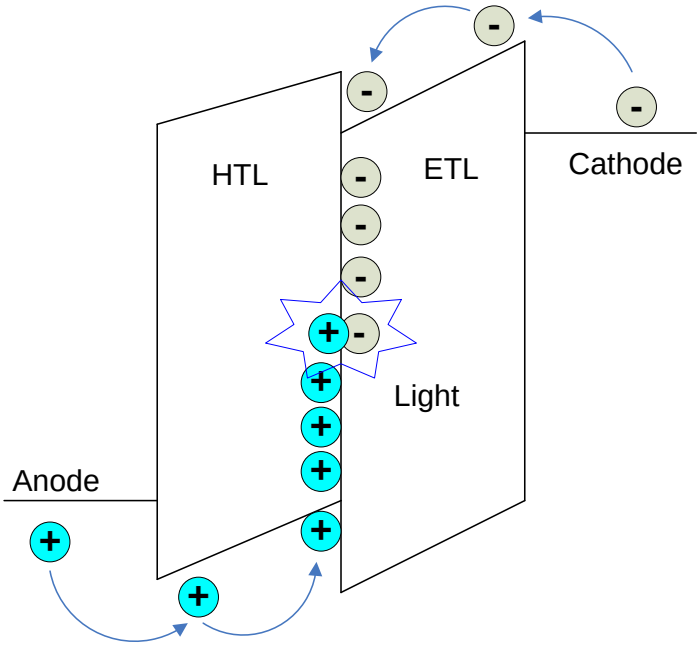


Figure 2.2 The OLED working principle

For an OLED-on-Silicon microdisplay, due to the opaque silicon substrate, the bottom emitting structure is limited. The OLED device is deposited on the opaque silicon backplane to form a top emitting architecture (Figure 2.3).For the cathode, a thin layer of metal was used to allow light transmission. The MOS transistor of the CMOS process is used as the current source or the current sink to provide the driving current for the OLED devices. The top metal layer of the CMOS process is used as the anode contact.

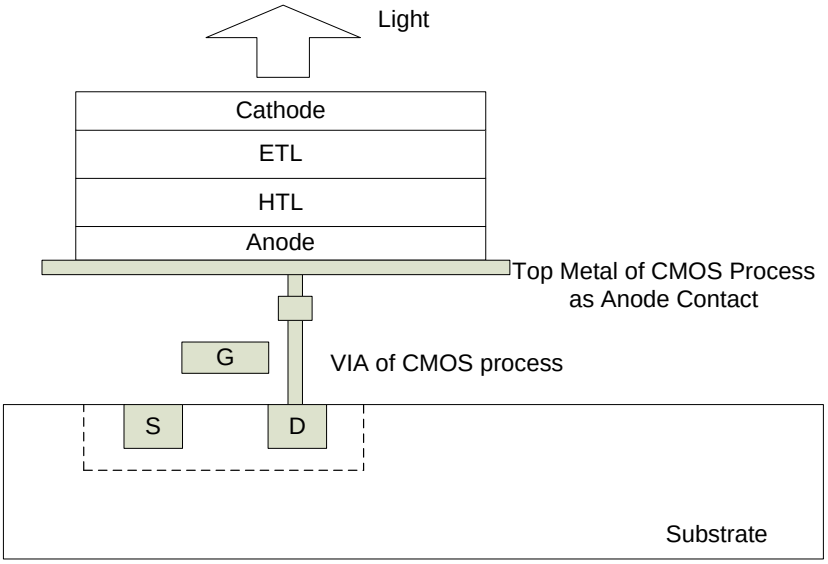


Figure 2.3 The top emitting structure of OLED-on-Silicon microdisplay

2.1.2 Electrical Characteristics of OLEDs

The I-V characteristics of OLED are similar to a p-n junction diode. The current-voltage characteristic of our OLED under DC operating voltage is shown in Figure 2.4.

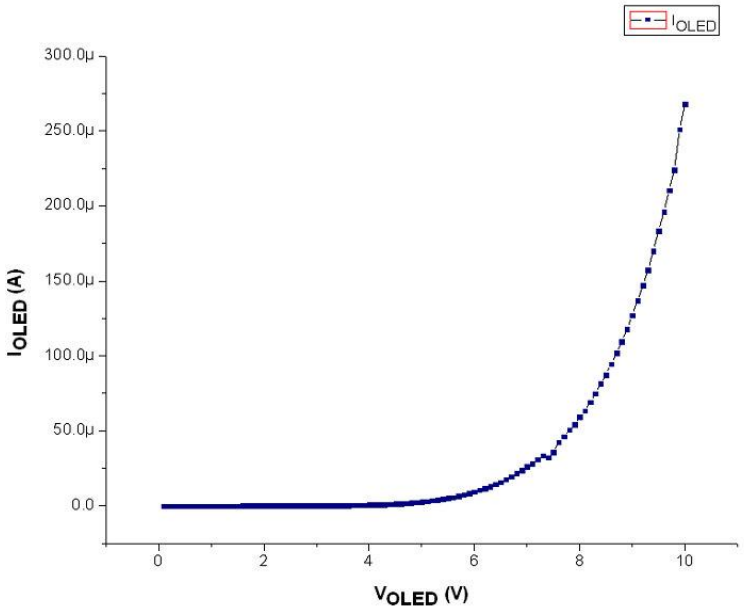


Figure 2.4 The I-V curve of the OLED in our research

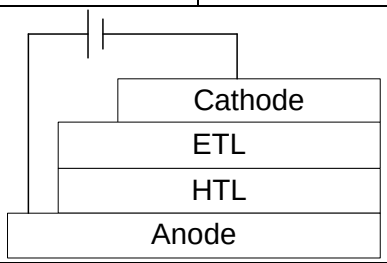
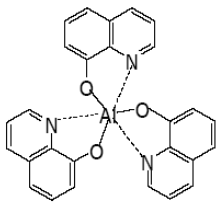
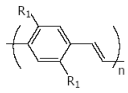
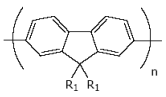
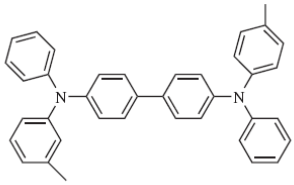
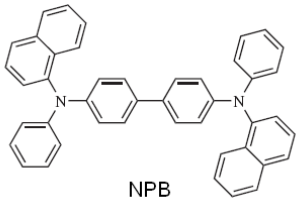
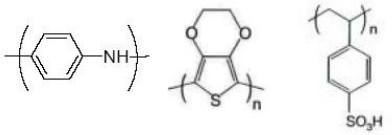
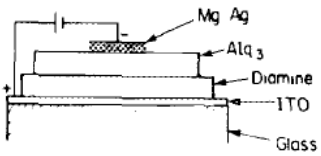
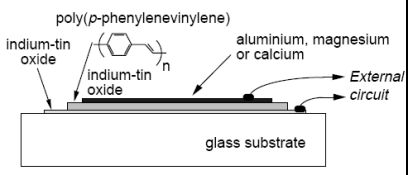
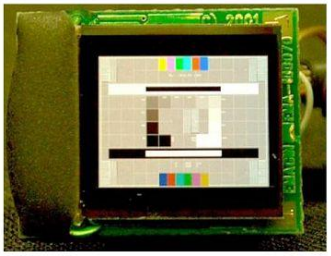
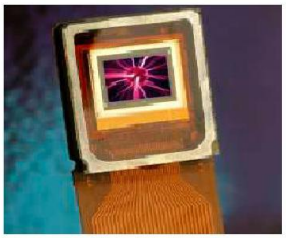
The I-V curve is measured with the OLED sample which is fabricated in the size of 50mm × 50mm. 70nm of NPB is used as the hole transporting layer and 70nm of Alq3 layer is the electron transporting layer. The forward bias driving voltage starts from 0V and it is noticed that there is little current. With the voltage increasing, the current increases slowly with the voltage until the voltage reaching a threshold voltage. The threshold voltage is typically a few volts. Beyond the threshold voltage, the light is produced and the current increases exponentially. A useful voltage range with relative display luminance levels is from several volts above this threshold voltage. In our design, the power supply for the OLED display is from 5V to 10V.

2.1.3 Organic Materials for Microdisplays

Mainly two organic emissive materials are used to fabricate OLEDs: small molecule materials and polymer materials. The fabrication methods of the small molecule OLEDs (SMOLEDs) and the polymer OLEDs (P-OLEDs) are extremely different and the process complexity is an important consideration in practical production manufacture. Vacuum deposition is the main technique applied for SMOLED fabrication while POLEDs are mainly deposited by spin coating or inkjet printing. The reason is the polymer materials used are soluble materials. Both materials are used to build OLED-on-Silicon microdisplays. Materials for SMOLEDs are easy to purify and prepare. The advantages of POLEDs include low manufacture cost, low operation voltage and high temperature stability. But neither spin coating nor inkjet printing is easily implemented for microdisplay manufacture. In our design, SMOLEDs are used to implement the OLED-on-

Silicon microdisplay. The main OLED device architectures and materials are listed in Table 2.1.

Table 2.1 Device architectures and materials for SMOLEDs and POLEDs

Items	SMOLED	POLED
Basic Device Architecture		
Cathode	Low Work Function Metals or Alloys, e.g. Mg:Ag or Al	
ETL	 Alq3	 R-PPV  PF
HTL	 TPD  NPB	 PANI PDOT PSS
Anode	ITO	
Device Examples [3][22]		
Microdisplay Application Examples [14][18]	 eMagin SVGA+ SMOLED Microdisplay	 MED ME3204 POLED Microdisplay

2.2 CMOS Technology for Microdisplays

CMOS technology is a generic technology which allows the designer to optimize the circuit structure for specific applications. Combined with a specific display technology, CMOS technology promotes the emergence of new microdisplay applications with the features of smaller size and lower cost. The features of CMOS-based microdisplays are: small pixel size, small display panel size, light weight, high fill factor, low power consumption, low voltage operation of CMOS electronics, low cost and high level of integration of driver circuits.

2.2.1 Comparisons of CMOS, Amorphous Silicon, and Poly-Silicon Technologies

Thin film transistor (TFT) based active matrix displays have achieved high resolution and high quality flat panel displays. The backplane circuits are designed with amorphous silicon (α-Si) and poly-silicon (poly-Si). α-Si is the most mature of the active matrix technology but it has the lowest mobility and integration capability. Poly-Si has higher mobility and greater integration potential than α-Si but poor uniformity. [27] For microdisplays, the electronic properties of α-Si are restricted, while the poor uniformity of poly-Si TFTs will lead to non-uniform display luminance in the microdisplay. A microdisplay panel with a size less than 1.5'' diagonal, is possible, even preferable, using a CMOS silicon wafer as the backplane. The comparisons of these three process technologies are listed in Table 2.2.

Table 2.2 Comparisons of α-Si, poly-Si and CMOS technologies

Items	α-Si	poly-Si	CMOS
Complexity of Process	Simple Process	Complex Process	Mature Commercial Process
Carrier Type	Only Electron	Both Hole and Electron	Both Hole and Electron
Mobility of Carriers	Low	Medium	High
Transistor Types	No p-type Available	Both n-type and p-type Available	Both n-type and p-type Available
Integration Capability	Low	Medium	High
Device Performance	Poor	Good	Good
Display Uniformity	Good	Poor	Good
Display Area Size	Medium to Large	Small to Large	Small or Tiny

Some features of CMOS technology are remarkable for the backplane of microdisplay. First, the planarization of the substrates is the key factor to achieve a uniform layer thickness of the optical device above. With CMOS technology, a rather flat single contact surface is well prepared on which the optical devices can be built. Another advantage is the convenience of the connection of the optical device and the integrated driving circuit because all the contact elements lie close to the surface. Second, compared with other processes, CMOS technology is considered a low power technology. The power supply voltage for CMOS components can be as low as 0.9V. Third, in CMOS process, the transistors and other active and passive devices have very tiny sizes and a high integration capability. But it is found that the best resolution of the CMOS silicon backplane tends to be 0.35μm to 0.18μm, although 65nm foundry is available nowadays. Finally, a mature semiconductor industry offers the low manufacture cost and high quality supporting services, such as advance and smart IC design software, many low cost wafer foundries and easily available wafer cutting, die packaging services and so on.

2.2.2 Basic Operation of MOS Transistors

MOS transistors are the basic functional elements of CMOS technology. Analyzing an MOS transistor' behaviors helps to specific circuit design according to the characteristics of different microdisplay technologies.

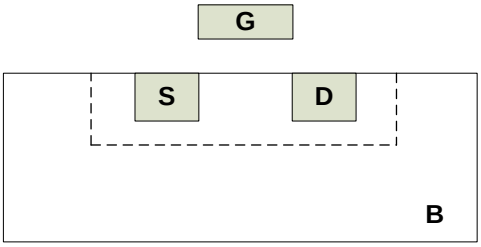


Figure 2.5 Basic structure of the MOS transistor

An MOS transistor is a four-terminal device: the gate (G), drain (D), source (S) and substrate bulk (B) (shown in Figure 2.5). An MOS transistor is a kind of voltage controlling current device. A current flows from the source to the drain and appears when a sufficiently large voltage is applied to the gate. In this case, the transistor is 'ON' and the minimum value of the gate voltage when this channel connects drain and source is called the threshold voltage. Otherwise, when no voltage is applied, the MOS transistor acts like two p-n junction diode and little current flows from the source to the drain, hence it is called the 'OFF' state.

The basic three operational regions of a MOS transistor are "cut-off", "linear" and "saturation". The drain currents in different operational regions are given with the supplied voltage on the MOS transistors. [28]

In the cut-off region, $V_{gs} \geq V_t, I_d = 0$ (2-1)

In the linear region, $V_{gs} \geq V_t, V_{ds} < V_{gs} - V_t, I_d = \frac{W}{L} \mu_{eff} C_{OX} \left(V_{gs} - V_t\right) V_{ds}$ (2-2)

In the saturation region, $V_{gs} \geq V_t, V_{ds} < V_{gs} - V_t, I_d = \frac{W}{L} \mu_{eff} C_{OX} \left(V_{gs} - V_t\right)^2$ (2-3)

Where V_{gs} is the gate-source voltage, V_{ds} is the drain-source voltage, V_t is the threshold voltage, I_d is the channel current, W is the channel width, L is the channel length, μ_{eff} is the carrier mobility, and C_{ox} is the normalized capacitance of the gate dielectric.

For a microdisplay, the operation of MOS transistors is different based on the different display technologies. For an LCoS microdisplay technology, the transistor only works as a switch, so when the condition of the linear region is fulfilled, the circuits work properly. But for an OLED-on-silicon microdisplay, the silicon backplane circuit must provide efficient current to drive the OLED devices, so transistors working in the saturation region can be considered as a current source to provide a constant driving current to illuminate the OLEDs.

2.3 OLED-on-Silicon Microdisplay

A combination of a certain display technology and CMOS is the primary success factor of a microdisplay panel. The usage of CMOS technology permits an active matrix pixel array and driver circuit to be packaged on a small silicon backplane. Video interface circuit processes the input video data (e.g. computer video output

or television video signals) to satisfy the requirements of the specific mirodisplay panel. The optical system recreates the virtual image for viewing.

The challenges of the silicon backplane design for OLED-on-Silicon microdisplay are associated with the features of the display system.

1. The light blocking function must be taken into account when a top-emitting structure is adopted. Leaking light might destroy the functional integrated circuits. Thanks to the multiple levels of metal interconnect of the modern CMOS process, this prevented by a properly designed overlapping structure of metal layers.

2. The generation of accurately designed levels of driving current will provide different levels of grayscale displays. The difference is the value of the driving current is smaller and the more levels of grayscale are required. In general, the current driving scheme is more attractive because uniform luminance can be achieved as a result of the constant driving current for this method. In this case, a current mode DAC is essential to provide accurate current data for each pixel. An efficient architecture of the pixel circuit is necessary in order to duplicate this current data to the OLED devices.

3. Current or charge sharing between the adjacent pixels must be carefully controlled. In the worst case, when a pixel is ‘ON’, the driving current is injected into the OLED devices. A part of the driving current will leak to adjacent pixels. The luminance of this ON pixel reduces and the increasing luminance of the adjacent OFF pixel is unexpected. This phenomenon is like crosstalk in passive matrix addressing.

2.4 Conclusion

In this chapter, an overview of OLED-on-Silicon microdisplay technology was presented, including the operation principle and characteristics of OLEDs devices, as well as the silicon backplane technologies related to microdisplay applications, e.g., the basic operation of MOS devices. Features of OLED-on-Silicon microdisplay technology were introduced and discussed.

Chapter 3

Design of Addressing Circuit for OLED-on-Silicon Microdisplay

3.1 Introduction

In display applications, the display data is transferred into the pixel array due to the scan manner. All the data are scanned from left to right, from top to bottom. The addressing circuits control the scan manner of the display data. According to the driving scheme, displays based on OLEDs technology are classified as passive matrix or active matrix. The important distinguishing feaure of these two driving schemes is whether there is an individual active device (e.g. transistors) to control the switch behavior of each pixel. The addressing technologies for OLEDs are presented in reference [29-31].

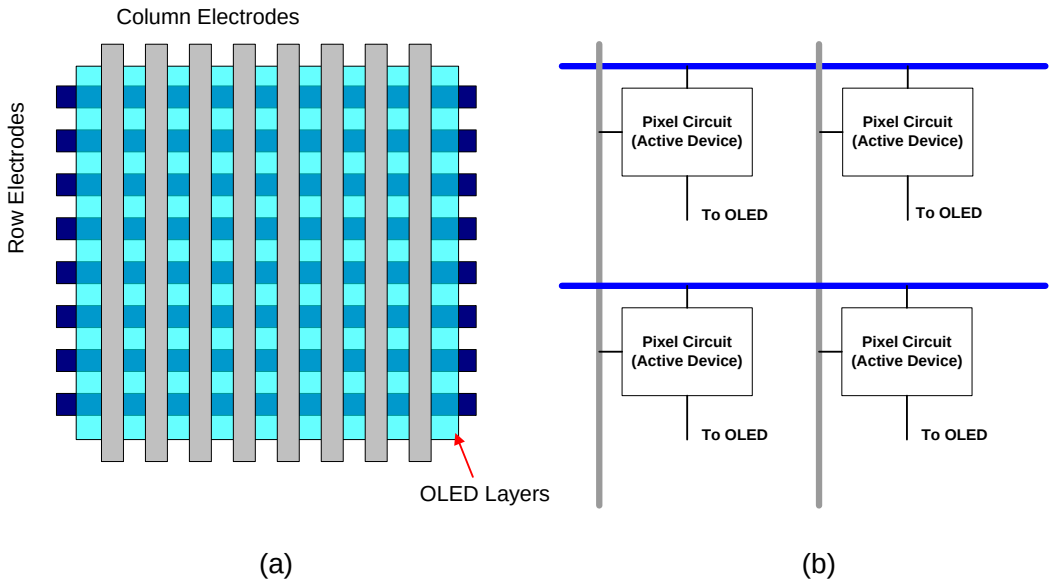


Figure 3.1 (a) Passive matrix display (b) Active matrix display

In passive addressing, the pixel matrix is connected directly to row and column electrodes and the pixels are activated row by row. Passive addressing is mainly limited to small size displays, because no memory function is enabled to each pixel and the duty cycle must be short. However, the main advantages of the passively addressed display are low manufacture cost and the simplicity of structure.

In active matrix scheme, each pixel is attached to an active component, such as transistor or diode. The transistor works as a switch which actively maintains the pixel state while other pixels are being addressed. It also prevents crosstalk.

For passive address OLEDs, another limitation is that the OLED must be driven by large current to maintain the luminance. The reason is that the pixel voltage will decline immediately when no voltage is applied to pixels which are built without memory components. And the power dissipation is high when such a large discharge current occurs all of the time. For microdisplay applications, the passive addressing scheme is not practical because low power dissipation is a significant requirement of microdisplays.

In active addressing OLEDs, a relatively small steady current is used to drive a pixel, rather than the large current for a passive addressing scheme. Each pixel remains ‘ON’ even during the hold period. With the memory elements, a transistor in the pixel circuit maintains the driving current even when the addressing signal is removed from the pixel circuit within one refreshing period of the display data. Thus the overall power consumption is decreased and the OLED lifetime is increased when the driving current decreases with the active matrix addressing technology.

The active matrix addressing scheme offers light weight, high luminance, low power dissipation, and low cost processing. It is suitable to realize the OLED-on-Silicon microdisplay.

3.2 Active Matrix Addressing circuit for OLED-on-Silicon Microdisplay

3.2.1 Silicon Backplane Electronics

Based on studies of the designs in references [32-34], the OLED-on-Silicon microdisplay functional block diagram is proposed in Figure 3.2. The entire system is mainly divided into the addressing circuit and the pixel matrix.

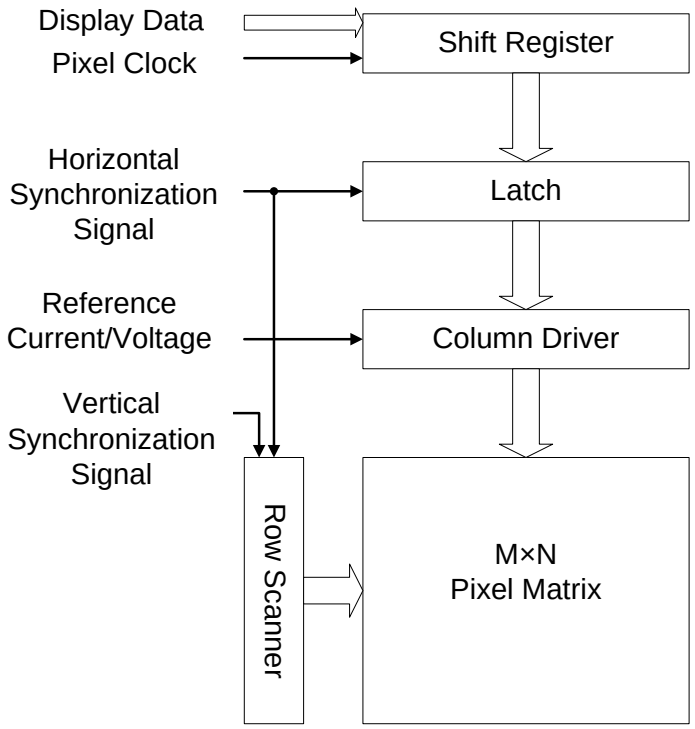


Figure 3.2 The functional block diagram of OLED-on-Silicon microdisplay

Digital display data of a whole line will be transferred into the shift register by the pixel clock signal. The data shift manner starts on the rising edge of horizontal synchronization (HS) signal and the data shift from left to right for one bit on each rising edge of the pixel clock signal. The data of one entire row will be loaded into

the shift register for further processing. On the next rising edge of the HS signal, the prepared entire row data will be injected into the data latch and the data shift motion will be repeated within the shift register. The data latch will hold the data for one horizontal row period and then the input digital data will be converted into specific voltage value with the DACs in the column driver. The pixel matrix is programmed by the converted analog signals with the control of the row scan signal. The pixels of the entire row will be enabled by the row scanner at the beginning of the horizontal period and remain connecting to the column lines until the data of the next row are well prepared.

3.2.2 Addressing Scheme for OLED-on-Silicon Microdisplay

The addressing circuit is usually divided into the column part and the row part. The column circuit consists of shift register, data latch and DAC. The display data are sorted, stored in the column circuit and converted in DACs before being transferred into the pixel matrix. The row circuit mainly provides the proper signals to control the row scan manner.

The structure and the time scheme of the shift register and the data latch for 1 bit digital input are shown in Figure 3.3 and Figure 3.4. The 1 bit input data will be transferred into the shift register bit by bit under the pixel clock. The shift register works as a serial-to-parallel converter. The data of a whole row will be stored in the data latch first then under the control of the HS signal, the data are loaded to DACs for further processing.

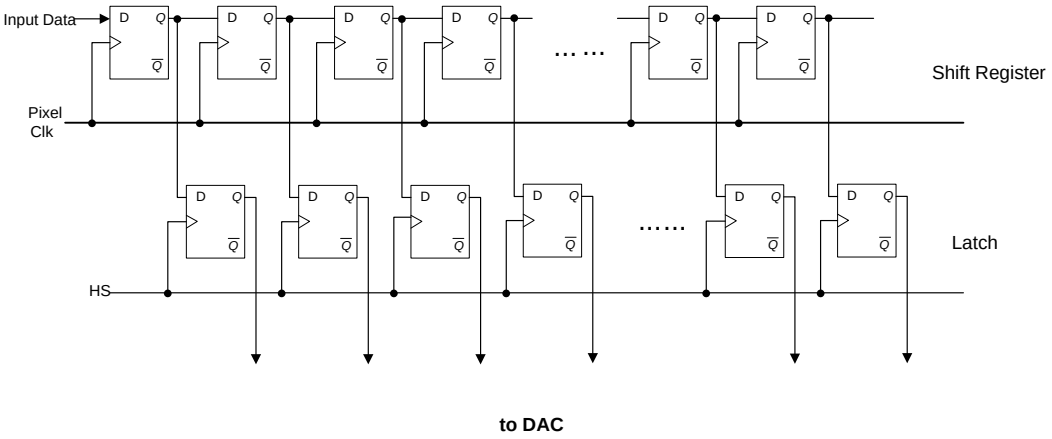


Figure 3.3 The structure of the shift register and the data latch

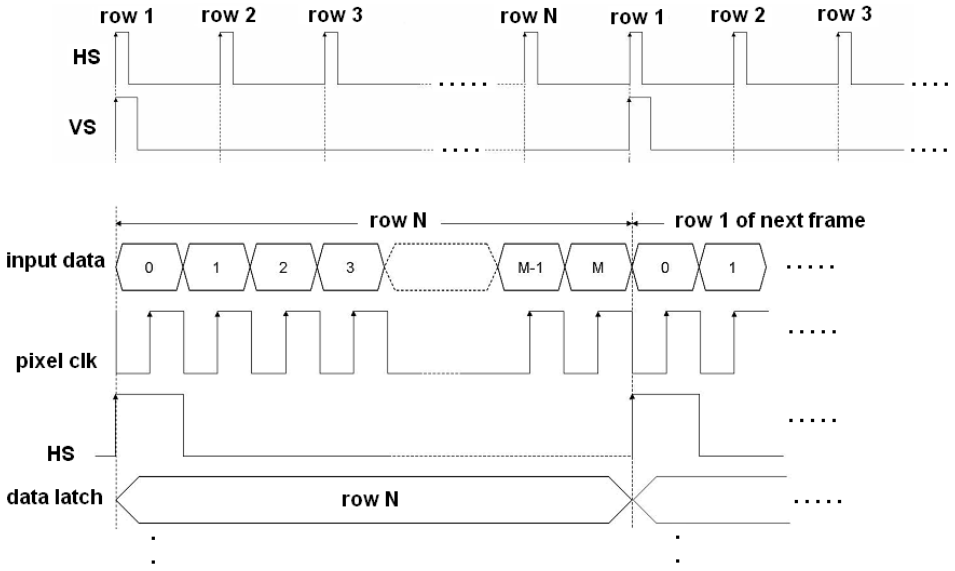


Figure 3.4 The time scheme of the shift register and the data latch

The schematic of the row scanner is shown in Figure 3.5. The row scanner consists of D flip-flops to form a shift register clocked by the HS signal. On every rising edge of HS signal, the row select signal will shift down by one row and enable this specific row. And the whole process will be repeated from the very first D flip-flop on the rising of the vertical synchronization (VS) signal. The time scheme of the row scanner is shown in Figure 3.6.

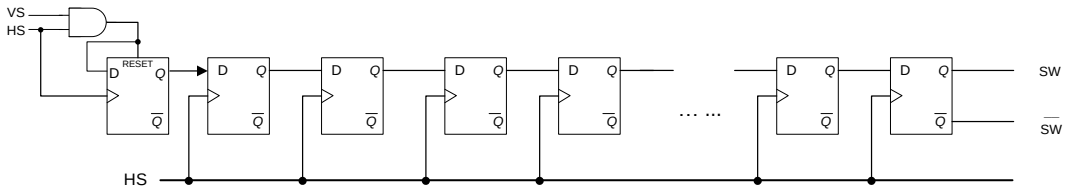


Figure 3.5 The schematic of the row scanner

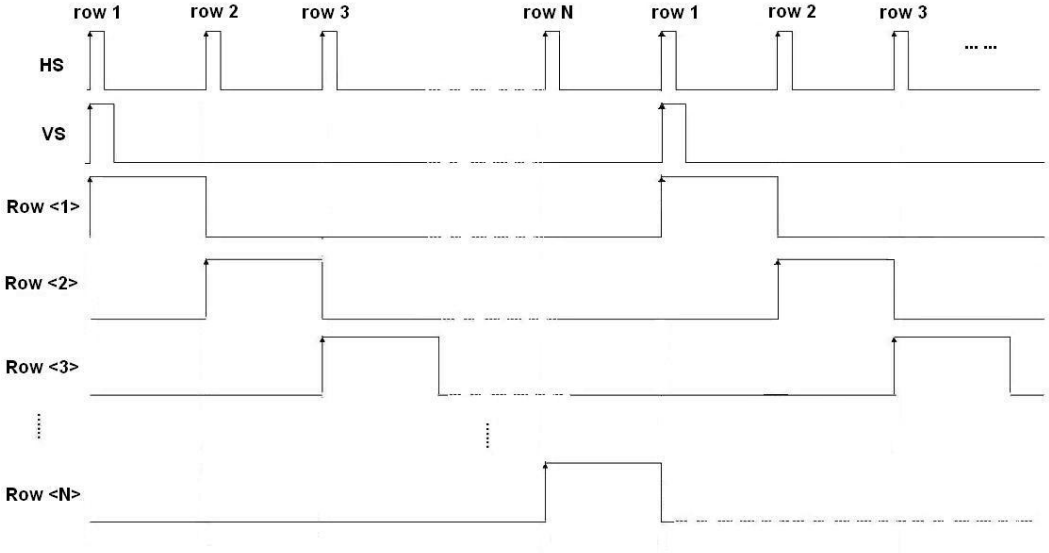


Figure 3.6 The time scheme of the row scanner

3.3 Optimizations of the Addressing Circuit for OLED-on-Silicon Microdisplay

The addressing circuit consists of D flip-flops as the basic building block. The characteristics of the D flip-flop must be considered due to the accurate synchronization required for the display data. Usually, two kinds of D flip-flop design are used: static D flip-flop and dynamic D flip-flop. Static D flip-flop consists of static memories which can preserve the state as long as the power is "ON". The static memories, consisting of two cross-coupled inverters (shown in Figure 3.7), have two stable states that represent logic "0" and logic "1". When inverter *a* has logic "1" at output node, because of the feedback circuit topology

inverter *b* has definite logic "1"at input node and logic "0" at output node to prevent the input of inverter a from floating.

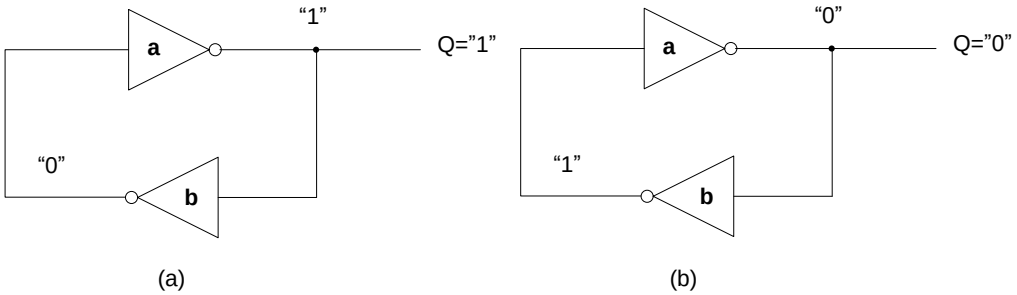


Figure 3.7 (a) The two cross-coupled inverters to store "1" (b) The two cross-coupled inverters to store "0"

A static D flip-flop used in this design is shown in Figure 3.8. CMOS transmission gate is used to realize the accessing motion of the D flip-flop.

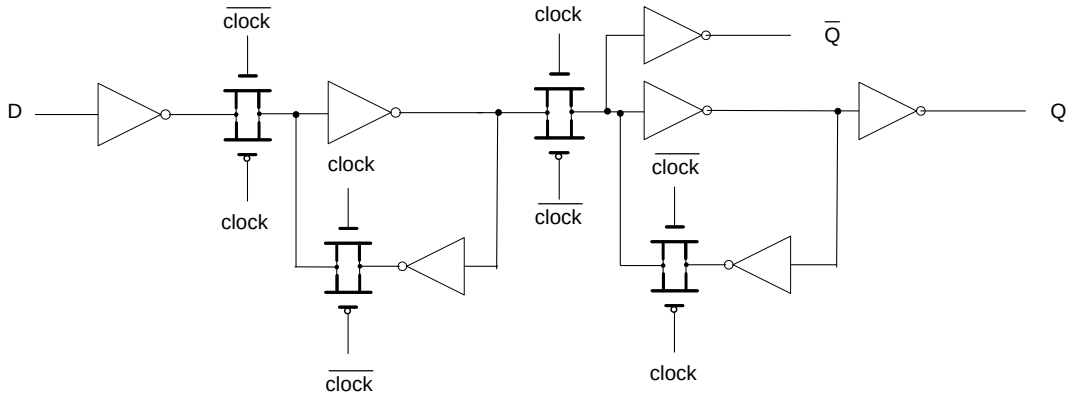


Figure 3.8 The static D flip-flop

The clock signals of the CMOS transmission gate are complementary. When *clock* signal is logic "1", both NMOS and PMOS transistors are on and the input signal will pass the gate. The signals transmitting process through the CMOS transmission gate is shown in Figure 3.9.

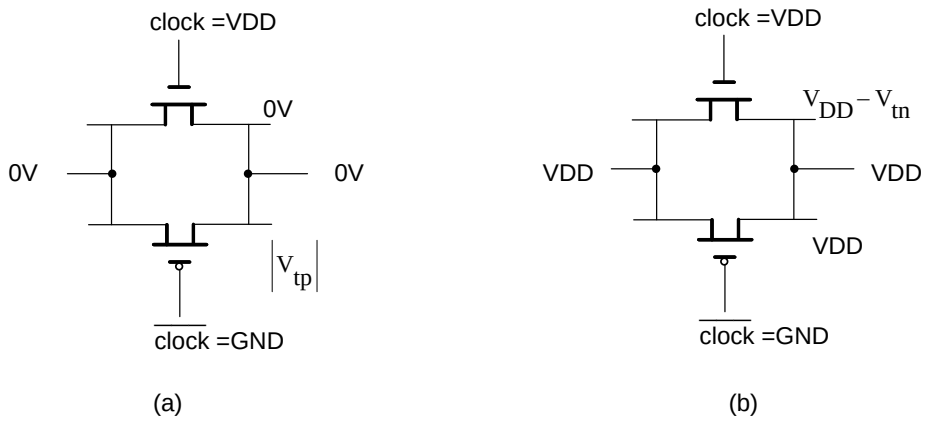


Figure 3.9 (a) Transmission of logic "0" through the transmission gate (b) Transmission of logic "1" through the transmission gate

In this static D flip-flop design, a master-slave construction is used. For the input, the inverting latch (Figure 3.10) is preferred to control the input noise. And a robust transparent latch (Figure 3.11) is used to reduce the output noise sensitivity. The static noise is isolated from the output noise and the output node swings rail-to-rail.

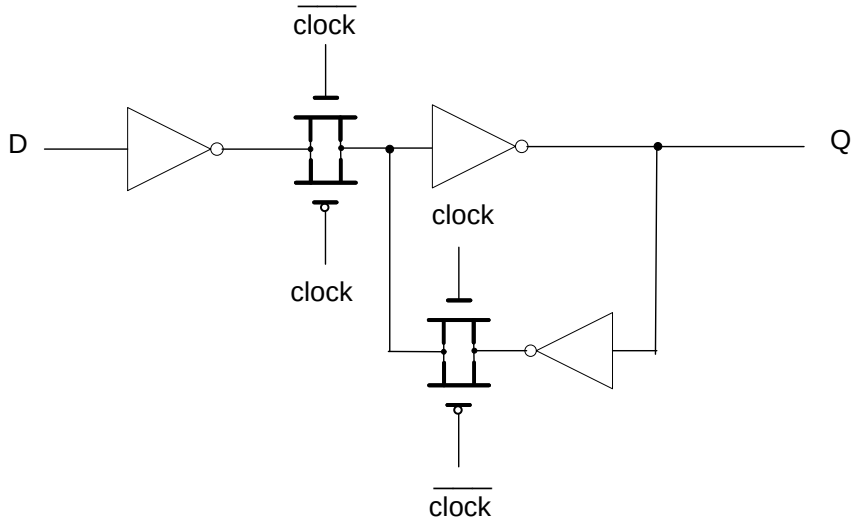


Figure 3.10 The inverting latch

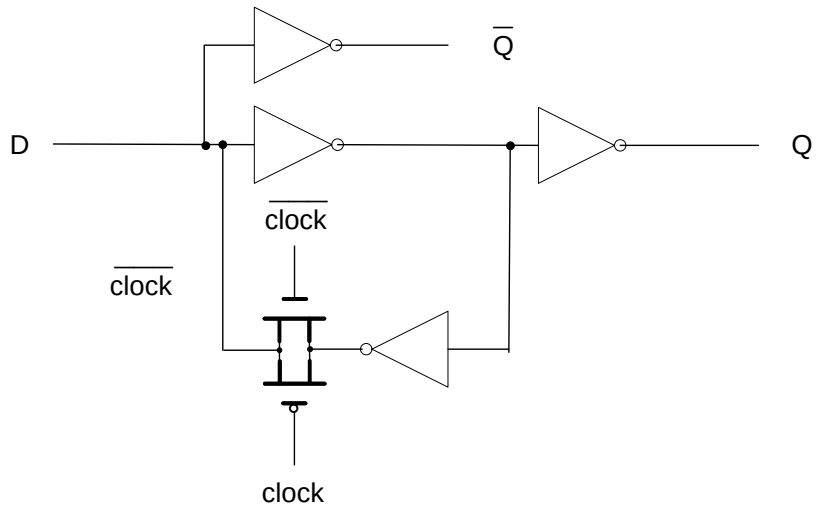


Figure 3.11 The robust transparent latch

Compared with the static D flip-flop, dynamic D flip-flop keeps state for only a certain time. The operation is realized by temporary charge storage in the parasitic capacitors. Dynamic D flip-flops are also based on a master-slave construction as shown in Figure 3.12.

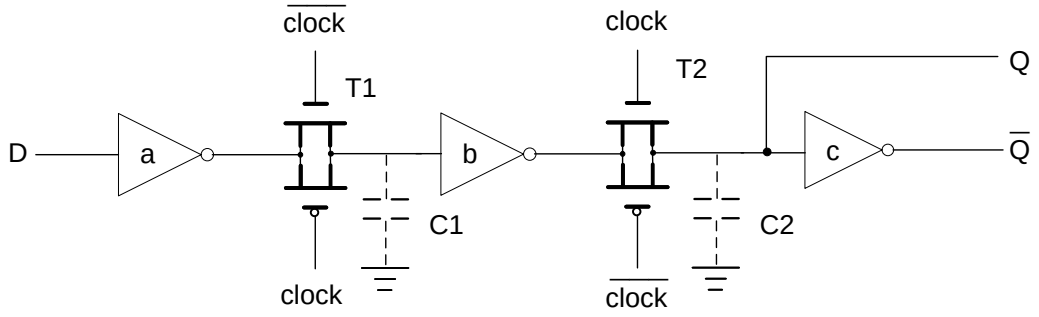


Figure 3.12 The dynamic D flip-flop

As shown in Figure 3.12, C1 is the equivalent capacitor to represent the gate capacitance of inverter *b* together with the junction capacitance and the overlap gate capacitance of transmission gate T1. When clock signal is logic "0", the logic signal $\overline{D}$ is store in C1 of the master stage. And the slave stage is in a hold mode. Output Q is in a high-impedance state. On the rising edge of clock signal, the

transmission gate T2 turns on, and the sample data on C1 will propagate to slave stage and the C2 will store the output Q for a period of time. If we want to preserve the output for a longer time, refreshing is necessary. And during the hold period of slave stage, the output Q is floating and that may cause the misjudgment of the logic level. On the other hand, the output is stored in the capacitor, so the leakage of the circuit will also distort the value of output signal.

Static D flip-flop is more suitable for microdisplay application, because in a modern process the subthreshold leakage is large enough to cause an incorrect judgment of the signal logic level. The simulation results for the static D flip-flop and the dynamic D flip-flop are shown in Figure 3.13. $Q1$ is the output of the static D flip-flop while $Q2$ is the output of the dynamic D flip-flop. From the simulation results, we notice the fluctuation of $Q2$ when the clock signal is logic "0". Ideally, when the clock is logic "0", T1 turns on and T2 turns off. $\overline{Din}$ will be stored in C1 and the slave stage is in a hold mode. The output node $Q2$ should be isolated from other parts of the circuit and present the previous value stored in C2. One possible reason for the fluctuation is the clock feedthrough (refer to section 4.3.3) or the leakages.

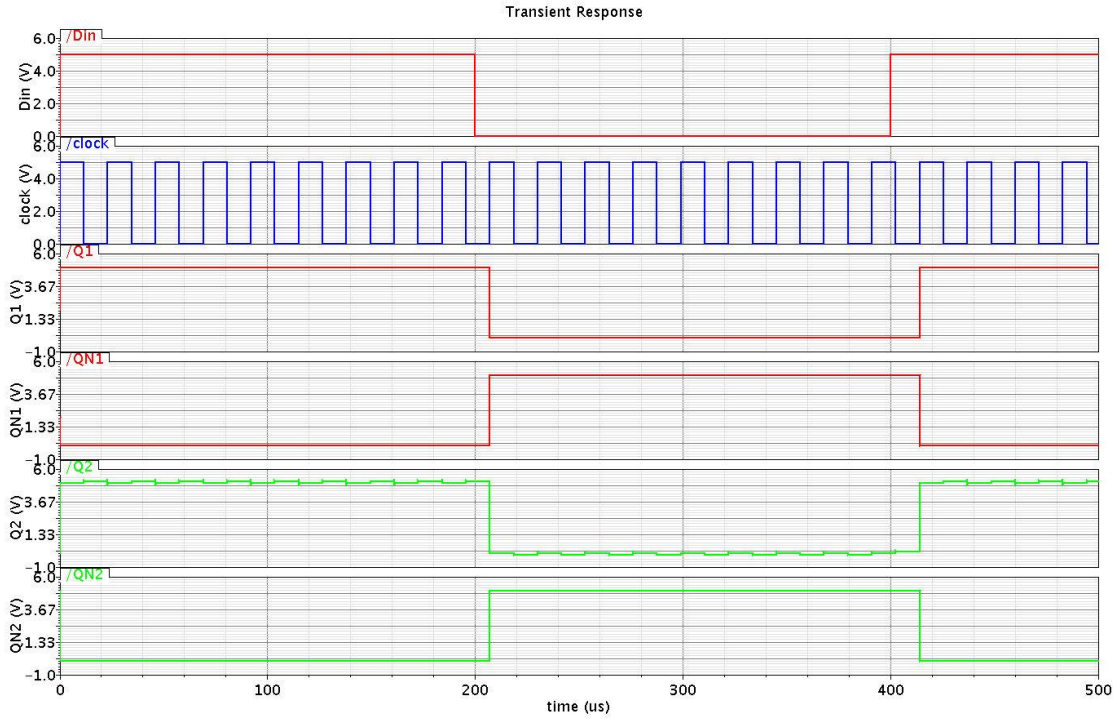


Figure 3.13 Simulation results of the static D flip-flop and the dynamic D flip-flops

Shown in Figure 3.14, when the rise and fall time of the input signal *Din* pulse is set to be 10ns, we can see that the rising edge of the Q1 is much sharper than that of Q2. So it decreases the possibility that the misjudgment of the logic level that happens at the edge of the output signal.

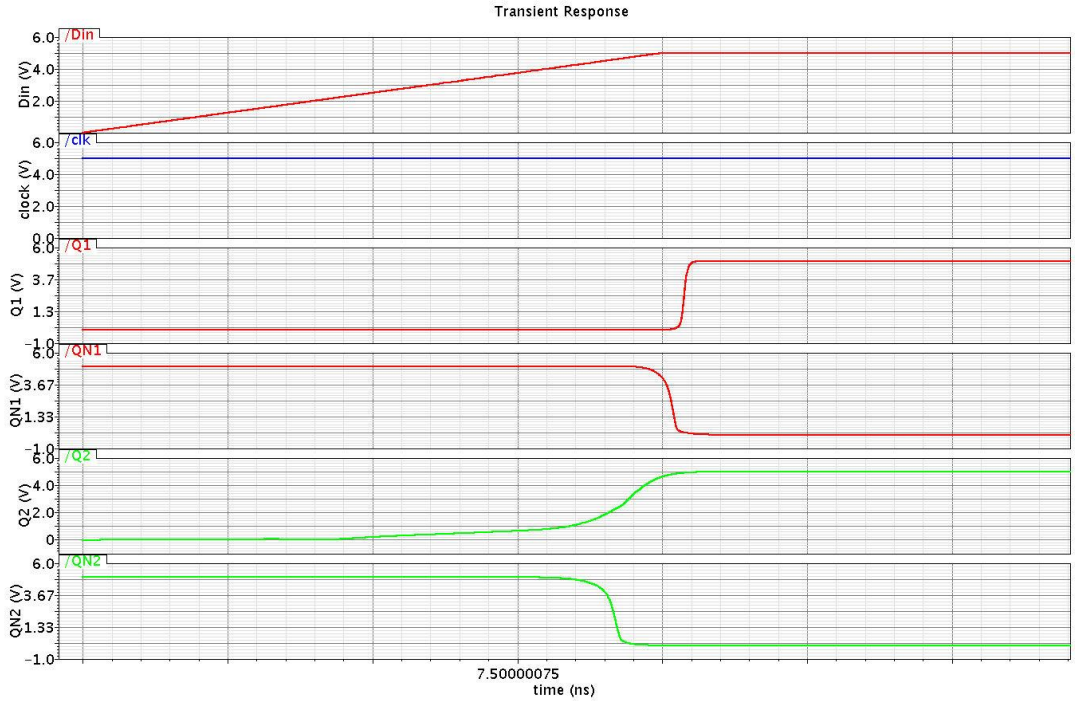


Figure 3.14 The rising edge of output signals of the static and the dynamic D flip-flops

3.4 Layout Considerations

From the functional block diagram, it is found that the circuit of the silicon backplane is a kind of mixed-signal circuit. The addressing circuit is mainly the digital circuit while the DAC for the column driver is mixed-signal itself, and the pixel matrix consists of mainly analog elements. Some basic rules for the layout implementation of the mixed-signal circuit should be noticed. The analog part should be protected from the noise source because the analog circuit is more sensitive to noise than the digital circuit. [36-37].

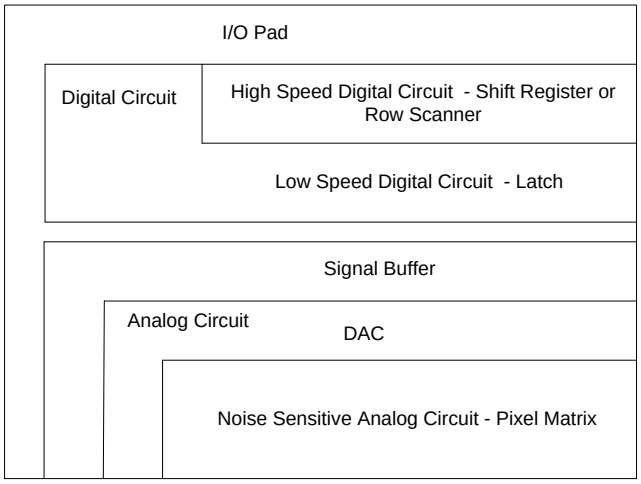


Figure 3.15 Layout arrangement of the mixed-signal circuit

In this design, the switch frequency of the shift register or the row scanner is high, so these digital parts should be placed far from the noise sensitive analog circuit, the pixel array. As signal buffer should be used before the analog signals from the data latch are transferred to DACs (shown in Figure 3.15).

Another layout consideration is the power supply for the analog part and the digital part should be separated. There are two separate couples of power pads as analog-VDD, analog-GND, digital-VDD, and digital-GND. And the dummy pad of the SMIC process is used to separate the analog signal pads and the digital signal pads. Figure 3.16 illustrates the I/O pads placement. [38]

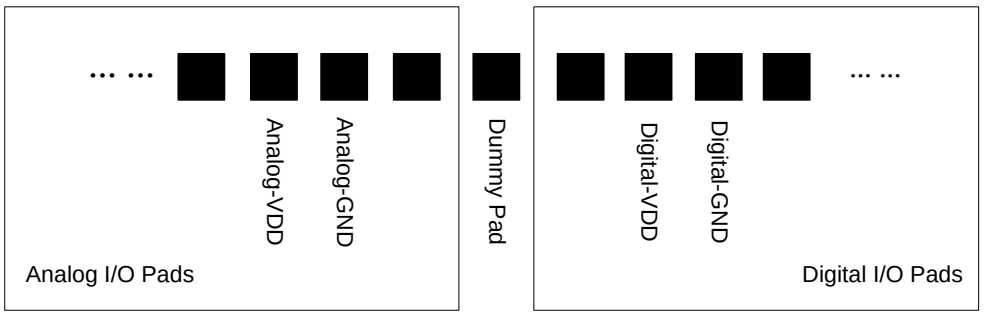


Figure 3.16 I/O pads placement

3.5 Simulation Results of the Addressing Circuit

An 8 × 8 block diagram of an OLED-on-Silicon microdisplay is shown in Figure 3.17. We use this block to evaluate the address circuit for the OLED-on-Silicon microdisplay because of the consideration of analysis efficiency in this case. As shown in Figure 3.18 (a), each shift register block consists of four D flip-flops in parallel to receive the 4 bit input digital data under the control of pixel clock signal. Four D flip-flops are formed as the data latch (Figure 3.18 (b)) to hold the 4 bit data from the shift register.

The simulation is run to verify the functionality of the digital circuit. Simulators use device models and a circuit netlist to predict circuit voltages and currents which indicate the circuit performance. The required inputs and the expected outputs of the addressing circuit are specified. Source components, e.g. DC voltage source or DC current source, will be used to produce the required input signals for simulation. Comparison will be implemented between the expected outcomes and the simulation results. Only when expectation and simulation match each other, the correct logical function of the addressing circuit is verified. [39]

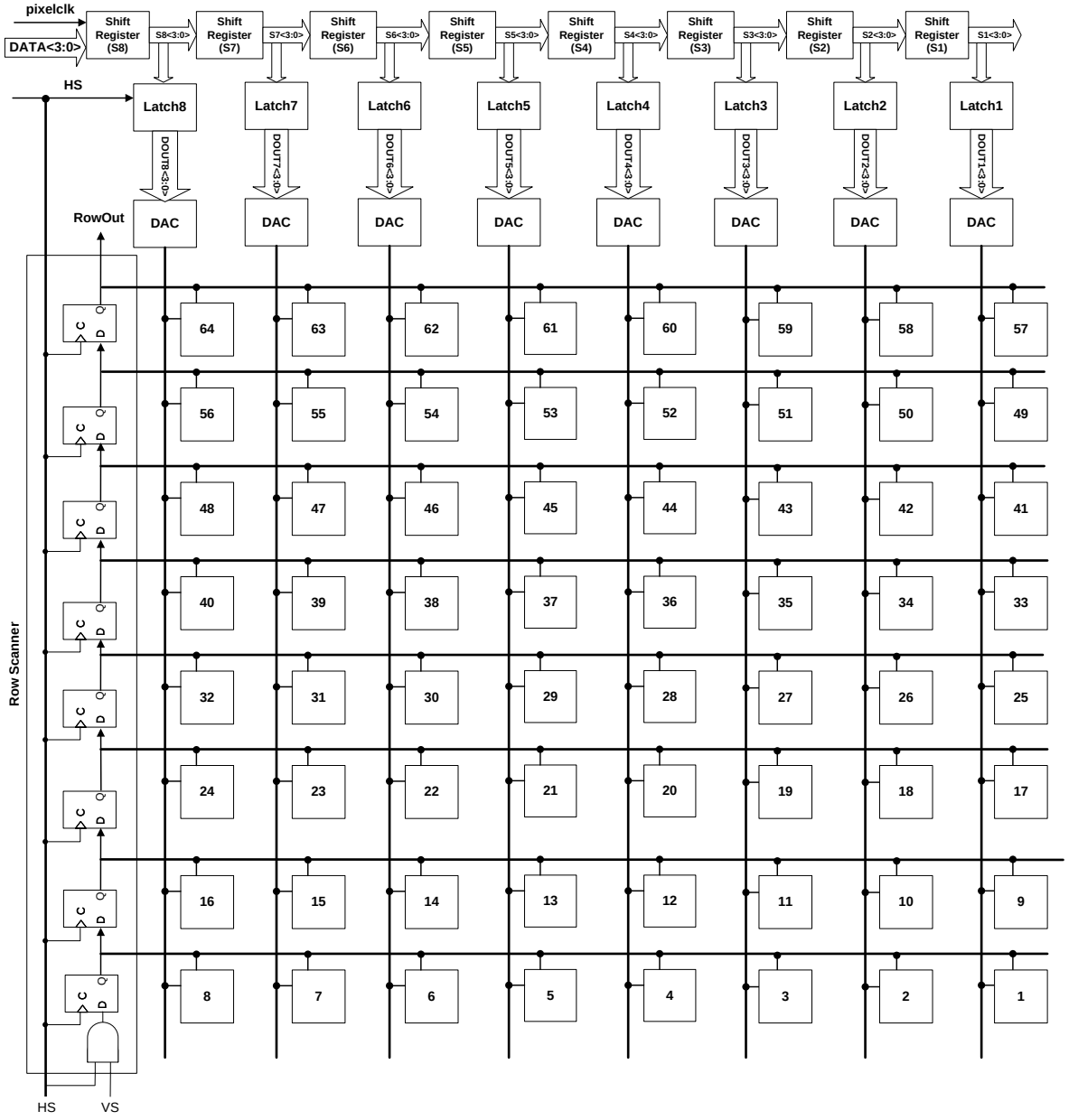


Figure 3.17 The 8 ×8 block diagram of OLED-on-Silicon microdisplay

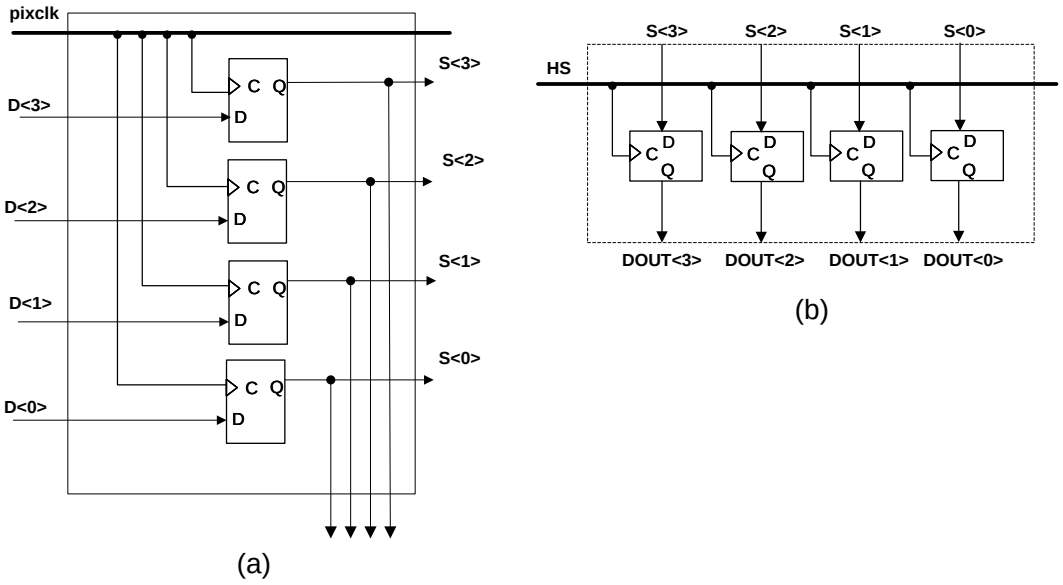


Figure 3.18 (a) The shift register (b) The data latch

To inspect the working state of the column addressing circuit, continuously digital input signals are loaded into the shift registers. The waveforms of the input signal are indicated in Figure 3.19. In two horizontal line periods, 4 bit digital input signal changes from '1111' to '0000' in binary countdown mode.

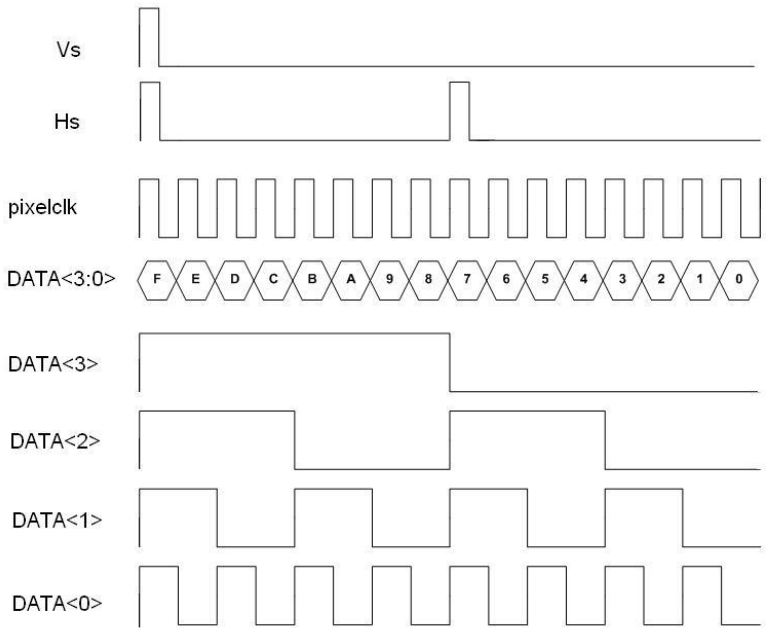


Figure 3.19 Input signals for simulation

The input data is clocked by “pixelclk” signal. The rising edge of HS signal indicates that the data of a horizontal line start to load into the column addressing circuit. Although only an 8×8 block diagram is used for simulation, the frequency of signal “pixelclk” is set as the same as the one used for the 160×120 prototype to evaluate whether the performance of the proposed circuit can fulfill the design targets. Since the frame refresh frequency equals to 60Hz, the frequency of the “pixelclk” signal is calculated by

$$f_{pixelclk} = 60Hz \times 120 \times 160 = 1.152MHz$$

The parameters of input signals are listed in Table 3.1.

Table 3.1 Input signals for the addressing circuit simulation

Signal	Frequency	Period	Duty Cycle
Pixelclk	1.152 MHz	868 ns	< 1%
HS	36 KHz	6944 ns	< 10%
VS	18 KHz	55.552 μs	< 5%
Data<3>	72 KHz	13888 ns	50%
Data<2>	114 KHz	6944 ns	50%
Data<1>	288 KHz	3472 ns	50%
Data<0>	576 KHz	1736 ns	50%

Cadence Virtuoso Spectre Circuit Simulator is employed to estimate the behavior of the circuit and *SimVision* is used for analyzing the virtual simulation results. *Virtuoso Spectre Circuit Simulator* is an advanced simulator that simulates analog and digital circuits supporting by device simulation models. The device models represent the behavior of transistors, resistors and other components in circuit simulation and in our design, the device models are provided by SMIC 0.35μm 3.3V/5.0V CMOS process. With component simulation models, simulation is run for functionality tests. And the Spectre simulator uses a netlist to list the components in a circuit, the modes that the components are connected to, and parameter values to support the simulation. The *SimVision* analysis environment is

a unified graphical debug environment. The *SimVision* environment features advanced debug and analysis tools and innovative high-level design and visualization capabilities. The Spectre simulator can run DC, AC, transient analyses and so on. Transient analysis computes the response of a circuit as function of time. In our design, the time response of output signals is what we concern, especially for the addressing circuit, so the transient analysis is presented to show whether the circuit function is fulfilled. [40]

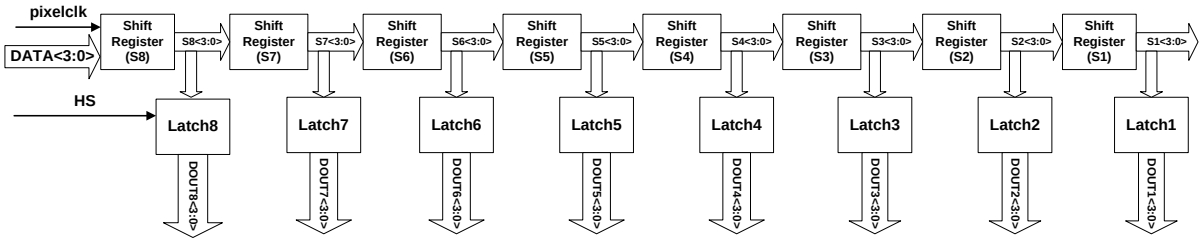


Figure 3.20 The column addressing circuit for 8 × 8 block diagram

The column addressing circuit for 8 × 8 block diagram is shown in Figure 3.20 and the simulation results are shown in Figure 3.21. S_n<3:0>, n=8 to 1, represents the 4-bit output of the shift registers. $DOUT_n$<3:0>, n=8 to 1, represents the 4-bit output of the latches. From the simulation results, we can notice the input data is shifted in the shift registers clocked by the "pixelclk" signal. At each rising edge of the "pixelclk" signal, the 4 bit input data shift forward by one stage. While only at the rising edge of the HS signal, the exact data in the shift register are loaded to the corresponding data latch.

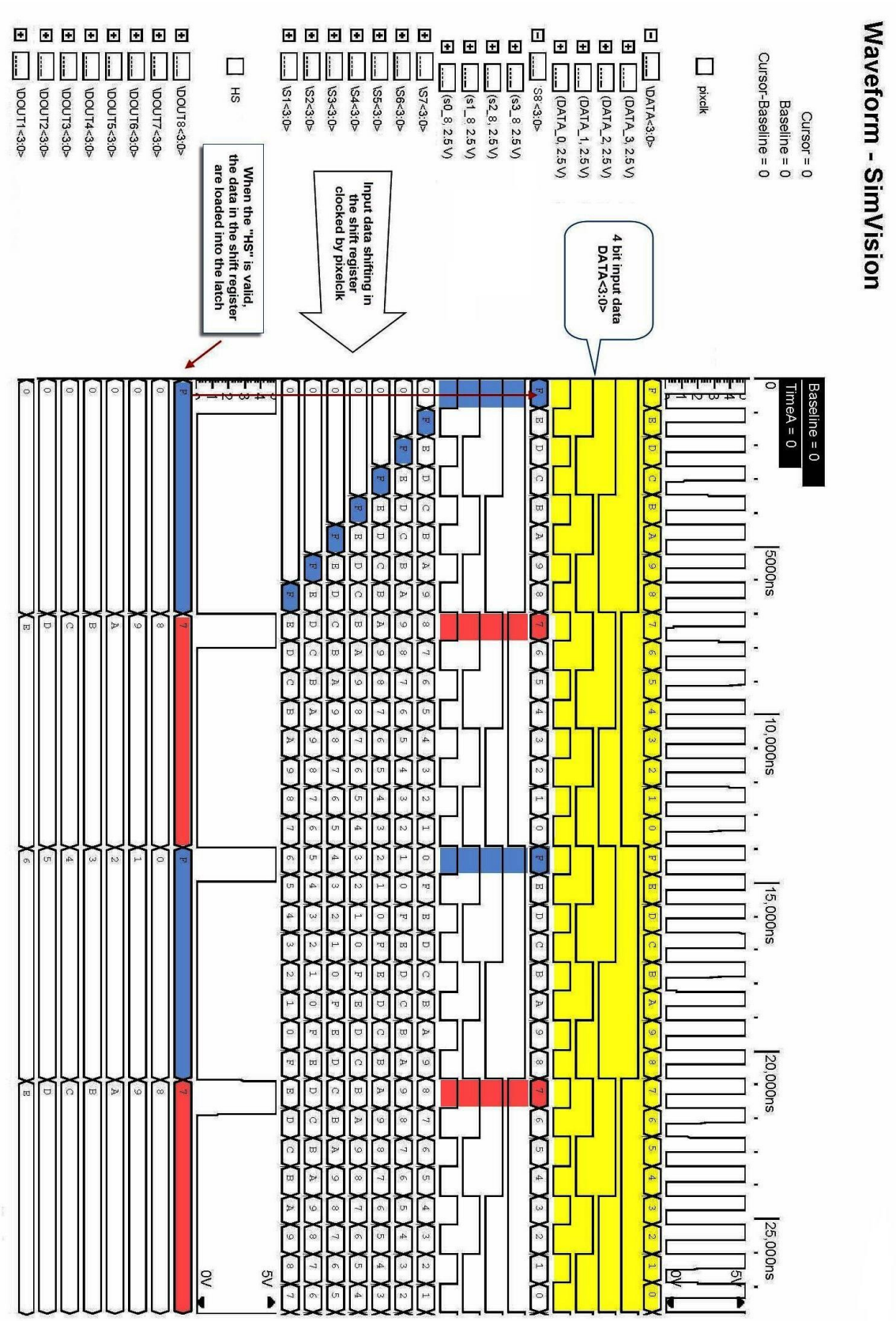


Figure 3.21 The column addressing circuit simulation results of the 8 × 8 block diagram of OLED-on-Silicon microdisplay

The row scan circuit of 8 × 8 block diagram is shown in Figure 3.22. The first D flip-flop of the row scanner has a *reset* bit. With an AND gate, only when both the VS signal and the HS signal are logic high, a logic "1" will reset the very first D flip-flop and be used as the input of the row scanner

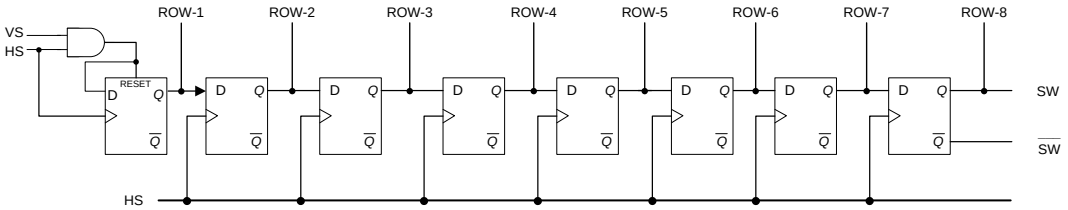


Figure 3.22 The row scan circuit of 8 × 8 block diagram

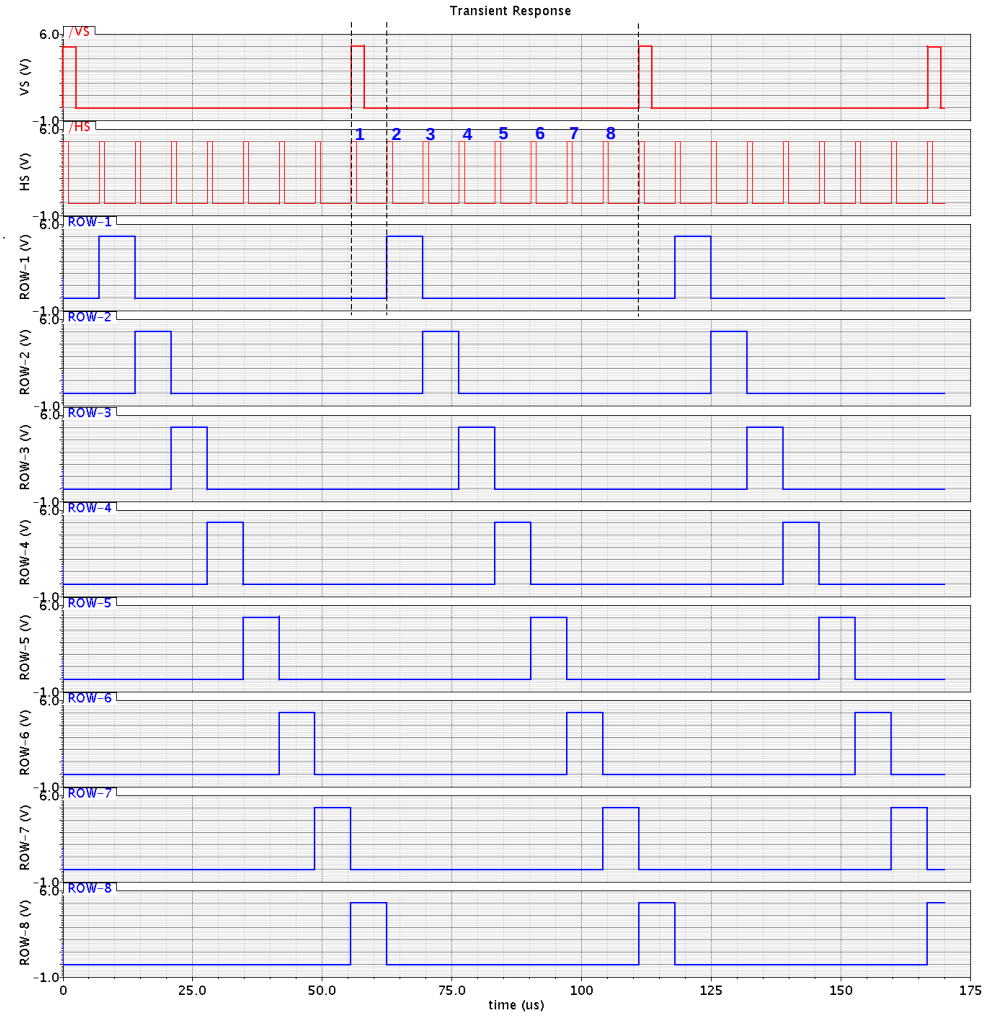


Figure 3.23 The row scanner circuit simulation results of the 8 × 8 block diagram of OLED-on-Silicon microdisplay

The row selection signals (ROW-n, n=8 to 1) are shifted from the first to the last line of one frame clocked by HS signal. The whole scan manner will be repeated at the rising edge of the next VS signal. The simulation result of the row scanner circuit is shown in Figure 3.23.We should notice that the row scanner outputs the row selection signal at the rising edge of the second HS signal. As described in the previous paragraphs, the reason is that it costs one horizontal line time for the data shifting and sorting in the shift register, so only during the period of the second line, the data loading into the pixel circuit are exactly the display data and the pixel circuits in the same row should be turned on by the exact row selection signal at the same time.

3.6 Conclusion

In this chapter, the addressing circuit for OLED-on-Silicon microdisplay is introduced. The functional blocks of the addressing circuit and the time schedule are presented to show the working principle of the display data scanning motion for OLED-on-Silicon microdisplay. The optimization of the D flip-flop is necessary because the D flip-flop is the basic element of this addressing circuit. Static logic D flip-flop is chosen due to its advantages presented in the analysis. Simulation results based on an 8 × 8 block show the addressing circuit works properly.

Chapter 4

Design of Pixel Circuit for OLED-on-Silicon Microdisplay

4.1 Introduction

Design of the pixel circuit for OLED-on-Silicon microdisplay faces the challenges that are derived from not only the electrical property but also the opto-electronic property of the OLED devices. The parasitic parameters in pixel matrix also affect the performance of the pixel circuit. In an OLED-on-Silicon microdisplay, the luminance of the OLED is proportional to the driving current density. The MOS transistor is used as the current source or the current sink to drive the OLEDs. To produce the proper driving current for the pixel circuit in the OLED-on-Silicon microdisplay, two approaches are employed: the voltage driving scheme and the current driving scheme. [2]

In a voltage driving scheme, the gate voltage of the current source transistor is controlled by the input voltage signal. The simplest possible pixel circuit using PMOS transistors is shown in Figure 4.1. The pixel circuit consists of a switch transistor (T1), a drive transistor (T2) and a storage capacitor (Cs).The switch transistor T1 controls the input data flow, and the driving transistor T2 is directly connected to the OLEDs to provide the driving current. The storage capacitor Cs is used as a memory element to record the gate voltage of T2.

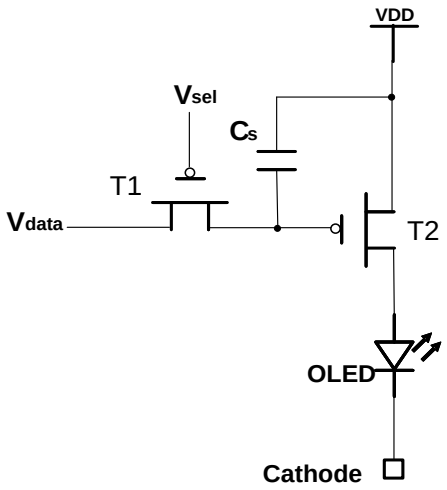


Figure 4.1 The 2-T pixel circuit of OLED-on-Silicon microdisplay

The operation of the pixel circuit is divided into two parts: the programming period and the driving period. In the programming period, the input signal flows into the pixel circuit with the switch transistor T1 turning on. The gate voltage of the driving transistor T2 and the capacitor Cs will be charged to a certain designed level. A drain current is yielded according to the working state of the driving transistor. Then in the driving period, the pixel circuit is isolated from the input data source. The gate voltage of the driving transistor that is stored in the storage capacitor Cs will keep the drain current flowing until the new display data is injected into the pixel circuit.

In the current driving scheme, the input video signal from computers, televisions or other video source is converted into a current signal to drive the OLEDs. The input current data is directly injected into the pixel circuit and the pixel circuit transfers the driving current to drive the OLEDs. The current mirror is the basic element used in the design. Modifications on the architecture of the current mirror enable the high performance of the current duplication action. In our design, a current

driving scheme is implemented due to its advantages that are presented in the following paragraphs.

4.2 Reviews of AMOLEDs Driving Scheme

AMOLEDs technologies used for direct view display which employs α-Si or poly-Si have been studied for years, so reviewing such pixel circuits provides us referential experience and helps us establish the design objectives. The pixel circuit designs based on α-Si and poly-Si in references [41-58] are reviewed and typical pixel circuit design technologies based on both voltage driving scheme and current driving scheme are analyzed in the following paragraphs.

4.2.1 Voltage Driving Scheme

In the basic pixel circuit (shown in Figure 4.1), it is preferable that the working state of the driving transistor falls in the saturation region; in this case, the drain current

$$I_d = \frac{1}{2}\mu_{eff} C_{OX} \frac{W}{L}\left(V_{gs} - V_t\right)^2 \quad (4\text{-}1)$$

is relatively stable with a certain value of the gate voltage. However, any modifications of the V_{gs} of T2 will lead to different currents flowing through the OLEDs. The V_{gs} varies with the input data voltage. So with different values of input data signals, the injecting current is different resulting in different luminance. Furthermore, the non-uniformity of transistor characteristics, such as the threshold voltage (V_t) and the mobility (μ), causes non-uniformity in the luminance of the

display. Compensation circuit is carefully designed to make the output current to be independent of the parameters, V_t, μ and *etc*.

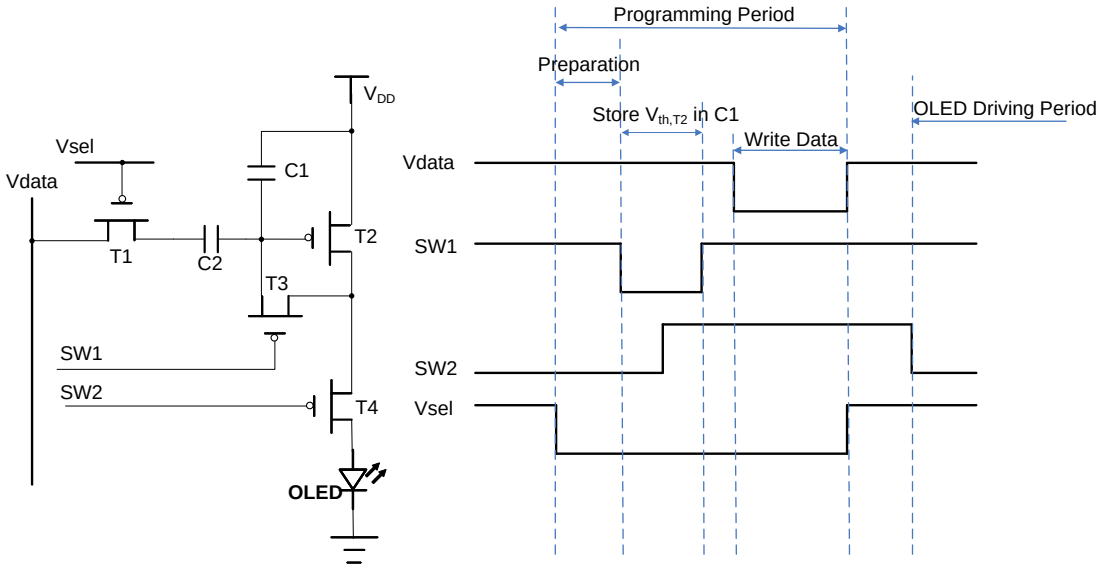


Figure 4.2 The voltage compensation pixel circuit

In the voltage compensation pixel circuit [49] (shown in Figure 4.2), there are 4 transistors and 2 capacitors. The basic principle is to use the diode-connected structure of the transistor to sample and hold the threshold voltage of the driving transistor T2. The transistors T3 and T4 are used to memorize and reset the threshold voltage of driving transistor T2. In this design, T3 and T2 form a diode-connected structure when T3 is 'ON' and T4 is 'OFF'. The gate voltage of T2 $V_{g,T2} = V_{DD} - V_{t,T2}$, due to the diode-connected structure. So the voltage across the capacitor C1 is $V_{t,T2}$. When T2 is disconnected and V_{data} is applied, the voltage of T2 is

$$V_{t,T2}^{'} = (V_{DD} - V_{data})\frac{C2}{C1+C2} + V_{t,T2} \quad (4\text{-}2)$$

and during the driving period, the driving current of OLED is independent of $V_{t,T2}$ of T2 and is given by

$$I_{OLED} = \frac{1}{2}\frac{W}{L}\mu_{eff}C_{OX}\left[(V_{DD} - V_{data})\frac{C2}{C1+C2}\right]^2 \quad (4\text{-}3).$$

Therefore, the driving current is independent of the threshold voltage of the driving transistor $V_{t,T2}$ in the voltage compensation pixel circuit.

4.2.2 Current Driving Scheme

An OLED device is a current driving device and the luminance of display is proportion to the driving current so a current driving scheme is a natural choice for the pixel circuit of an OLED-on-Silicon microdisplay.

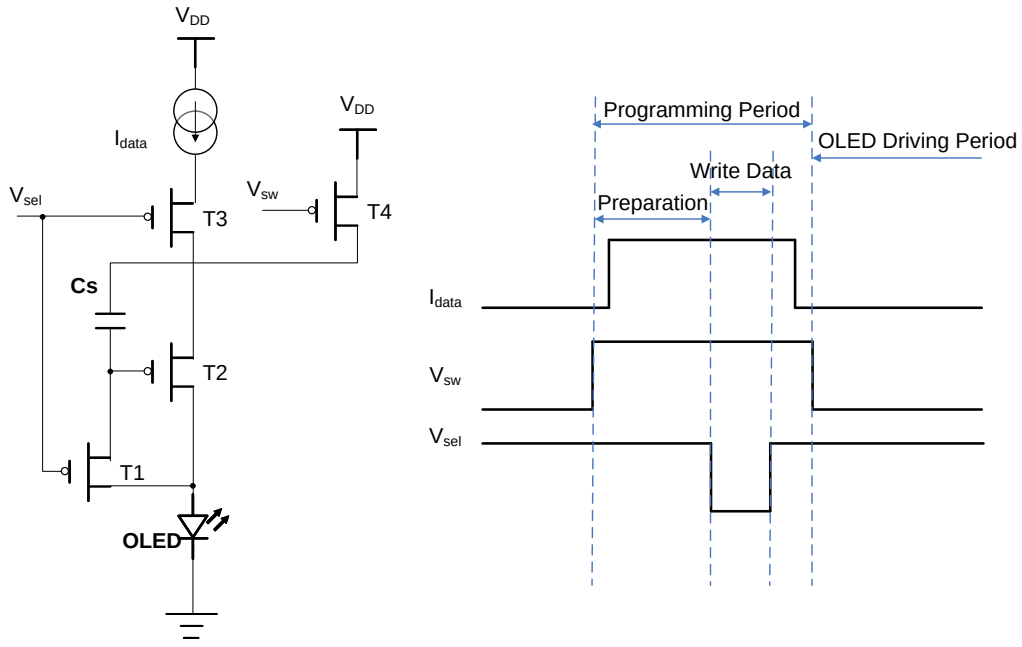


Figure 4.3 The pixel circuit based on the current copier

A current driving pixel circuit based on the current copier circuit is presented in Figure 4.3. The working principle of such pixel circuit is to use the current copier

to sample and hold the input current. The driving scheme of such a pixel structure is also divided into two periods: the programming period and the driving period. In the programming period, when I_{data} flows in the pixel circuit, switch transistors T1 and T3 turn on and the current flows to T2. The gate voltage of T2 will be charged to a certain value $V_{g,T2}$ according to I_{data}. While the gate voltage $V_{g,T2}$ also is memorized by the capacitor Cs. The variation of mobility μ_{eff} and threshold voltage of T2 $V_{g,T2}$ will be compensated by the voltage stored in Cs. Then in the driving period, T4 turns on while T1 and T3 turn off, the drain current of T2 flows into the OLED to emit light. The luminance of the display depends on the gate voltage of T2 stored across Cs according to I_{data}. Ideally the OLED current I_{OLED} should be equal to I_{data} and independent of μ_{eff} and $V_{g,T2}$. However, one difficulty for such a structure is that the requirement of channel-to-channel current accuracy is very high, especially at a low level of grayscale when the I_{data} is as low as several nano amperes. Also, a long programming time is observed in the case that the storage capacitor Cs is charged by such a low data current. The charge distribution is also due to parasitic parameters of the column lines connecting to each pixel circuit. With the increase of the display resolution and the image quality, the programming time will increase

The pixel circuit based on the current mirror is shown in Figure 4.4. The current mirror is the basic element of such a pixel circuit structure. The operation principle is similar to the current copier structure. The data current I_{data} will be converted to a certain value of gate voltage of T1 stored across Cs during the programming period. Then in the driving period, this driving current I_{data} will be copied to the

OLED device with the current mirror pair of T1 and T2. The advantage of current mirror structure is by adjusting the W/L ratio of the current mirror pair, the larger value of the data current , I_{data} ,can be used in the programming period in order to improve the accuracy and shorten the programming time. In practice, the dimensions of T1 and T2 are design as $\left(\frac{W}{L}\right)_{T1} = k\left(\frac{W}{L}\right)_{T2}$, where k is larger than 1. The data current I_{data} scales down in order to provide a proper OLED current I_{OLED} according to k.

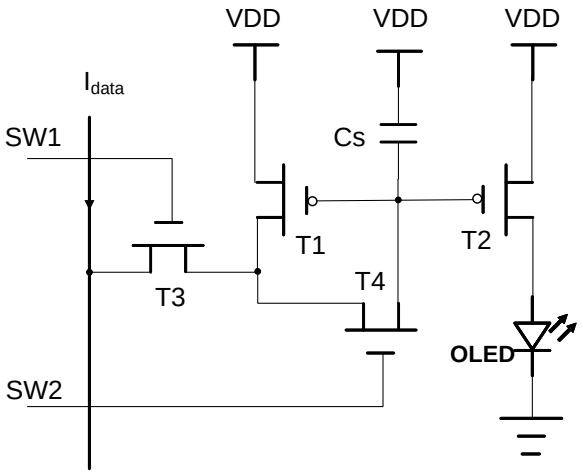


Figure 4.4 The pixel circuit based on the current mirror

4.3 Design Considerations for Pixel Circuit of OLED-on-Silicon Microdisplay

The luminance of the OLEDs is proportion to the driving current density. The current driving scheme is the natural choice to produce an OLED display. Current signal process technologies are reviewed for the design of the pixel circuit in references [59-65].

4.3.1 PMOS Transistors for OLED-on-Silicon Mirodisplay

The reason why a PMOS transistor is preferred in the pixel circuit is mainly due to the non-linear characteristic of an OLED device and the top-emitting structure of the OLED-on-Silicon microdisplay.

The conventional current driving pixel circuits using only NMOS or only PMOS transistors are shown in Figure 4.5.[13] When PMOS driving transistor T2 is directly connected to the OLED device to inject the driving current, the source of T2 connecting directly to VDD, the gate-source voltage V_{gs} is not affected by the non-linear current-voltage characteristics of the OLED device. It is much easier to control the driving current. If an NMOS transistor simply replaces the PMOS transistor, in order to precisely control the value of V_{gs}, the source of the NMOS transistor should be directly connected to ground. V_{gs} is reduced when the voltage drop increases through the OLED device. The drain current of the NMOS transistor will also decrease with V_{gs} and the luminance of the OLED will reduces with the current at the same time.

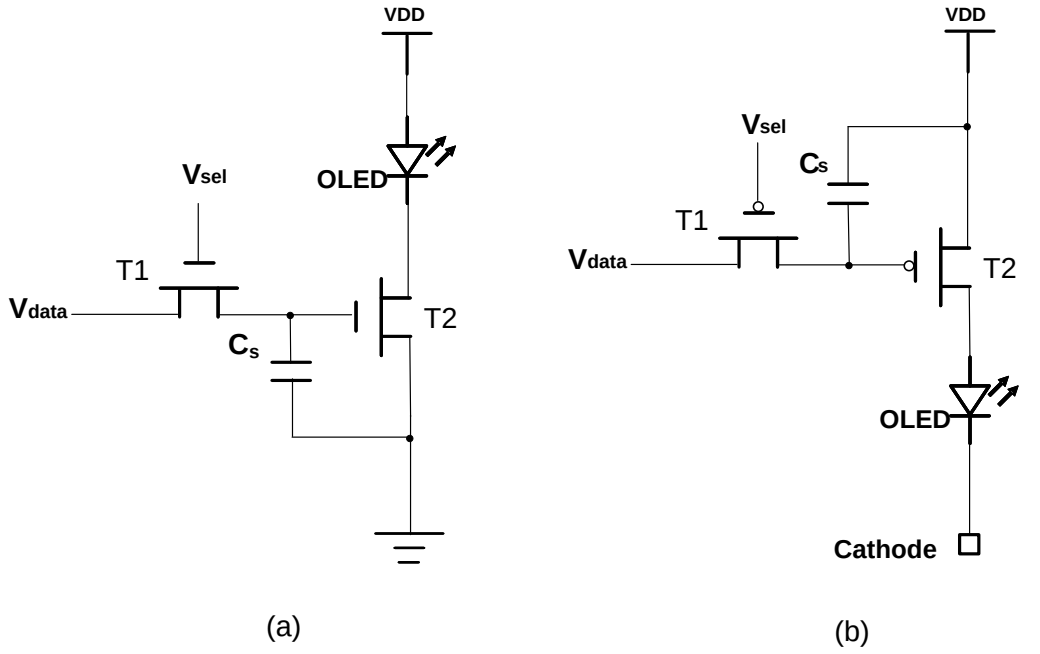


Figure 4.5 (a) The 2-T pixel circuits using NMOS (b) The 2-T pixel circuits using PMOS

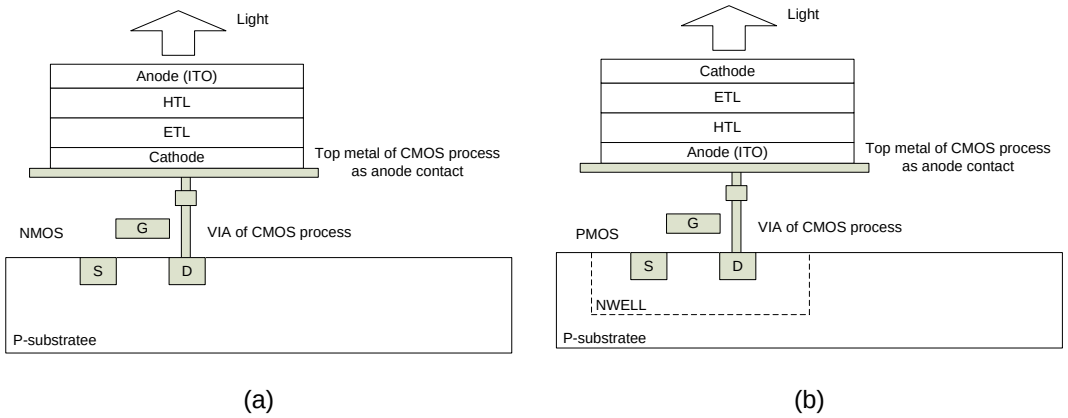


Figure 4.6 (a)The top-emitting structure of OLED-on-Silicon microdisplay using NMOS and (b) The top-emitting structure of OLED-on-Silicon microdisplay using PMOS

On the other hand, the opaque silicon backplane leads to the top-emitting structure and the PMOS transistor is preferable. As shown in Figure 4.6, with the use of PMOS transistor, a CMOS wafer will be used as the positive terminal of the top-emitting structure and the top metal layer of CMOS wafer is used as contact for the deposition of ITO anode. Otherwise, when the NMOS transistor is used, to achieve the successful top-emitting structure, the CMOS wafer is the negative terminal of

this OLED-on-Silicon microdisplay so the ITO layer will be sputtered directly on the OLED layers. Sputter deposition is a physical vapor thin film deposition method. Sputtered atoms ejected from the source material target have a wide energy distribution, typically up to tens of electronic volts. It takes the risk of destroying the OLED device layers when these high energy atoms collide with the OLED layers. The reason why PMOS is preferred for top-emitting OLED structure is based on the consideration of the high product yield.

4.3.2 Switch Charge Feedthrough

In the pixel circuit, when MOS transistors are used as switches, the switch charge feedthrough must be taken into consideration.

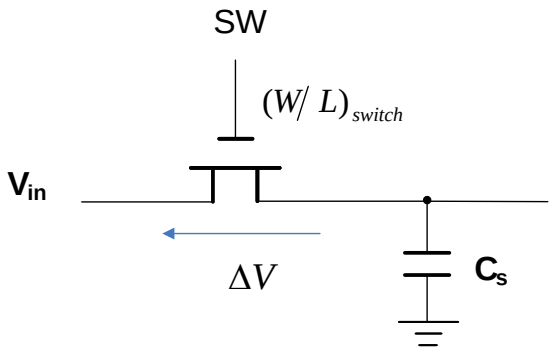


Figure 4.7 The switch charge feedthrough

The cause of the switch charge feedthrough is the current from the inversion layer of the MOS transistors. When the MOS transistors turn off, the charge of the inversion layer will flow into the source, the drain and the substrate. In consequence, the stored voltage of Cs changes by ΔV , creating a relative change in the output current $\Delta I = g_m \Delta V$, where g_m is the transistor transconductance.

Assuming a single n-channel transistor acting as the switch, if half of the charge Q_s in the inversion layer of the switch transistor spills onto Cs and since the switch is operated in the linear region, the voltage variation

$$\Delta V = \frac{1}{2}\left(\frac{Q_s}{C_s}\right) = \frac{1}{2}\left(\frac{WLC_{OX}\left(V_{gs}-V_t\right)}{C_S}\right)_{switch} \quad (4\text{-}4).$$

The driving transistor is operated in saturation region, and the resulting change in the OLED current is

$$\Delta I = g_m \Delta V = \frac{1}{2}\left[\frac{\mu C_{OX} W_1 (V_{gs}-V_t)}{L_1}\right]_{driving}\left[\frac{W_2 L_2 C_{OX}(V_{gs}-V_t)}{C_s}\right]_{switch} \quad (4\text{-}5).$$

Where W_1 and L_1 are the width and length of switch transistor, W_2 and L_2 are the dimensions of driving transistor.

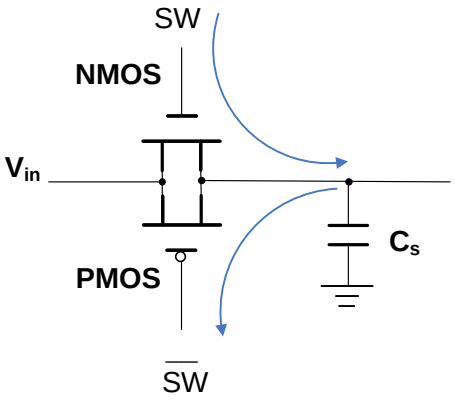


Figure 4.8 The CMOS switch used as the switch element

A transmission gate replaces the switch transistor as the switch component. The variation of the voltage is calculated as

$$\Delta V = \frac{C_{OX} WL}{2C}(2V_{in} - |V_{TP}| + V_{TN} - V_{DD}) \quad (4\text{-}6).$$

If the size of the NMOS and PMOS transistors are carefully selected to make the absolute value of the threshold voltage of the PMOS transistor ($|V_{TP}|$) equal to the threshold voltage of the NMOS transistor (V_{TN}), the charge injection due to each transistor is complementary to each other. In addition, in the driving period, the leakage current appears. The error caused by the leakage current gives a slow change in the output port. The leakage current can be reduced when a CMOS switch pair is used because the leakage current from the NMOS and PMOS transistors are cancelled by each other.

4.3.3 Clock Feedthrough

Driving by a clock signal, a switch transistor presents two states: ON or OFF. Ideally, this clock signal should not influent the output of this switch transistor directly. But when the switch transistor just turns off under the control of the clock signal, charge redistribution happens due to the gate-drain capacitor C_{gd} or the gate-source capacitor C_{gs}. This redistribution of charge forces the output voltage to drop. This phenomenon that the effect of the clock signal appears at the output node is called clock feedthrough.

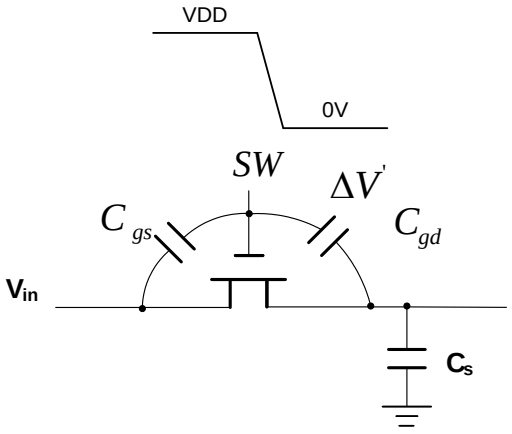


Figure 4.9 The clock feedthrough

When the control clock signal swings from VDD to 0V, the switch transistor turns off and the output node is high impedance state. The capacitors C_{gd}, C_{gs} and the load capacitor Cs are isolated. As the gate voltage decreases, the charges associated with these two capacitors redistribute to maintain equality. The redistribution motion causes the voltage at the output node drop an amount. The output voltage change $\Delta V^{'} = V_{DD} \frac{C_1}{C_1 + C_S}$ (4-7),

where $C_1 = C_{gs} + C_{gd}$ is the total overlap capacitance, Cs is the capacitance of the load. Usually $C_{gd} + C_{gs} << C_S$, the error caused by clock feedthrough is much smaller than the one caused by switch charge injection. If the Cs is large enough, usually the error caused by the clock feedthrough at the output is neglected.

4.3.4 Time Response of the Storage Elements

The basic working principle of pixel circuit is to control the working state of the driving transistor. Usually, voltage mode or current mode display data are applied to the pixel circuit during the programming period, and correspondingly, a properly designed gate voltage is generated to the driving transistor in saturation region. A storage capacitor is necessary to remember this gate voltage in order to keep the current flowing during the driving period. Evaluating the time response of the capacitor helps to analyze the performance of the pixel circuit. Basic elements (shown in Figure 4.10) are used to indicate the charge and discharge at the storage capacitor of the pixel circuit for the OLED-on-Silicon microdisplay. As discussed, a PMOS transistor is preferred to use as the driving transistor in the pixel circuit. The capacitor Cs is used to store the gate voltage of this transistor.

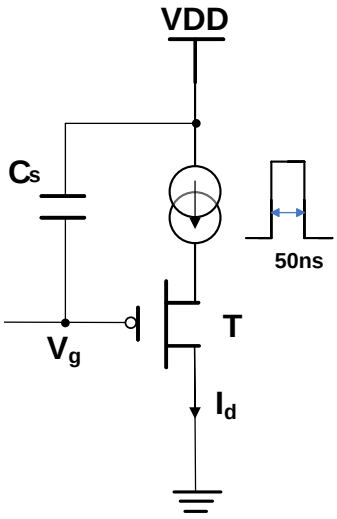


Figure 4.10 The basic elements used for evaluating the time response

A current pulse with pulse width of 50ns is injected into the circuit. The capacitance of Cs and the W/L ratio of the driving transistor will affect the drain current, as well as the gate voltage stored in capacitor.

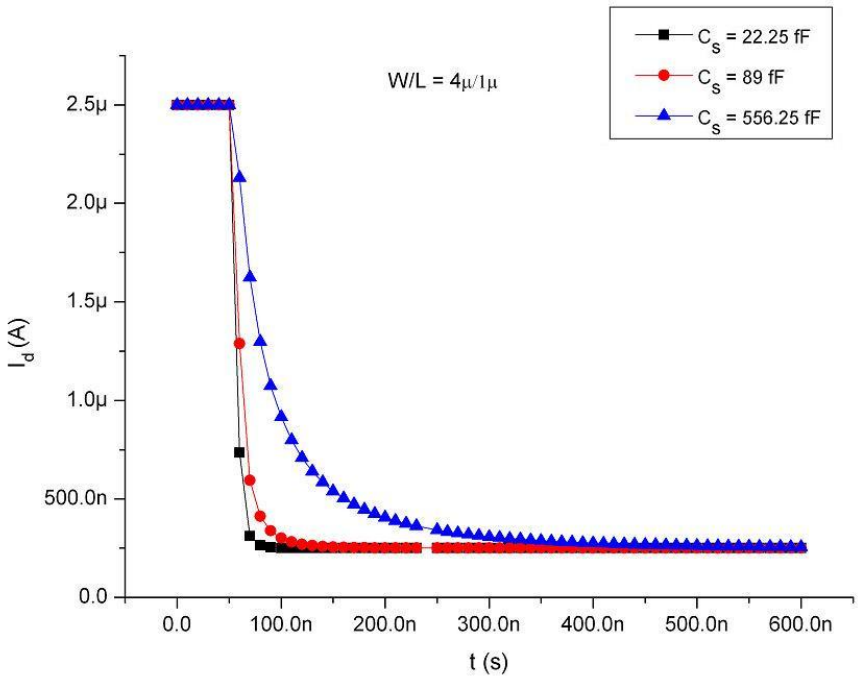


Figure 4.11 The drain current I_d with the different capacitances of C_s

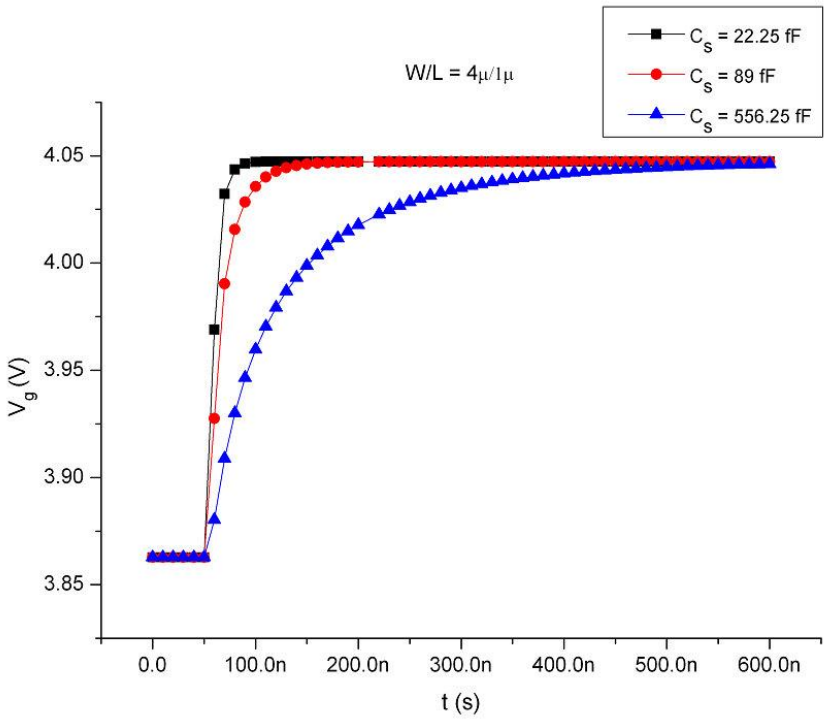


Figure 4.12 The gate voltage V_g with the different capacitances of C_s

In Figure 4.11 and Figure 4.12, the simulation results show that a large capacitance needs a long response time. If a fast response is crucial, small capacitance is preferable. But large capacitance is helpful to sustain the gate voltage in the driving period. A tradeoff must be considered in the design.

Then, constant capacitance is used and only the W/L ratio of the driving transistor is changed to observe the circuit performance. The simulation results are presented in Figure 4.13 and Figure 4.14. For a microdisplay application, the variation of the W/L ratio is in a narrow range. In this case the drain current I_d is not affected greatly but the gate voltage will increase when enlarging the W/L ratio. The W/L ratio should be properly design to offer the appropriate gate voltage.

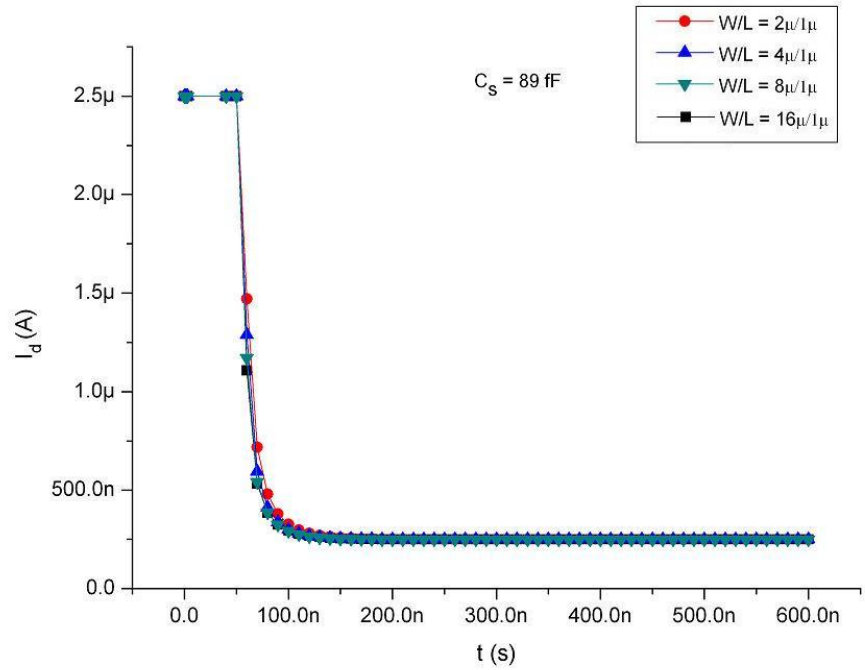


Figure 4.13 The drain current I_d with the different W/L ratios

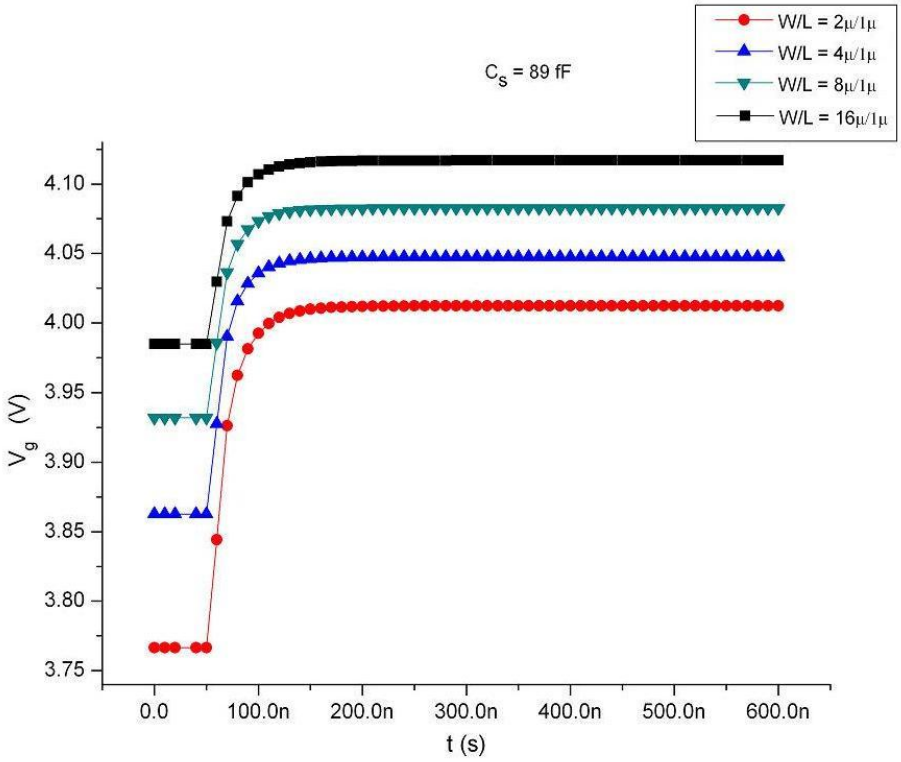


Figure 4.14 The gate voltage V_g with the different W/L ratios

Besides the W/L ratio, the transistor size is also considered. Comparisons are shown in Figure 4.15 and Figure 4.16. Increasing the physical dimension of transistors, the gate voltage will also increase but the drain currents are almost the same. So it will take a longer time to lock the stable working state of the large size driving transistor.

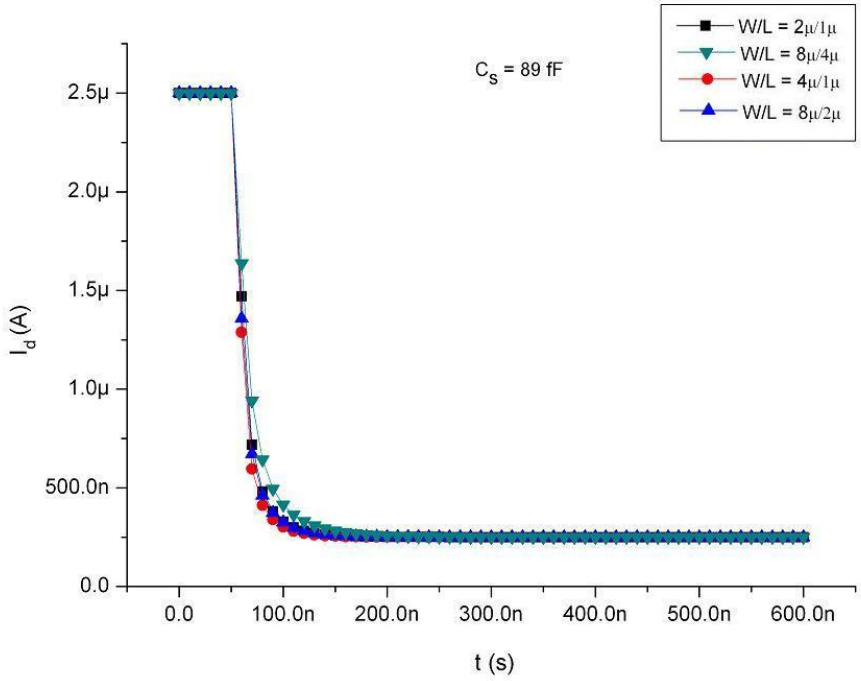


Figure 4.15 The drain current I_d with the different transistor size

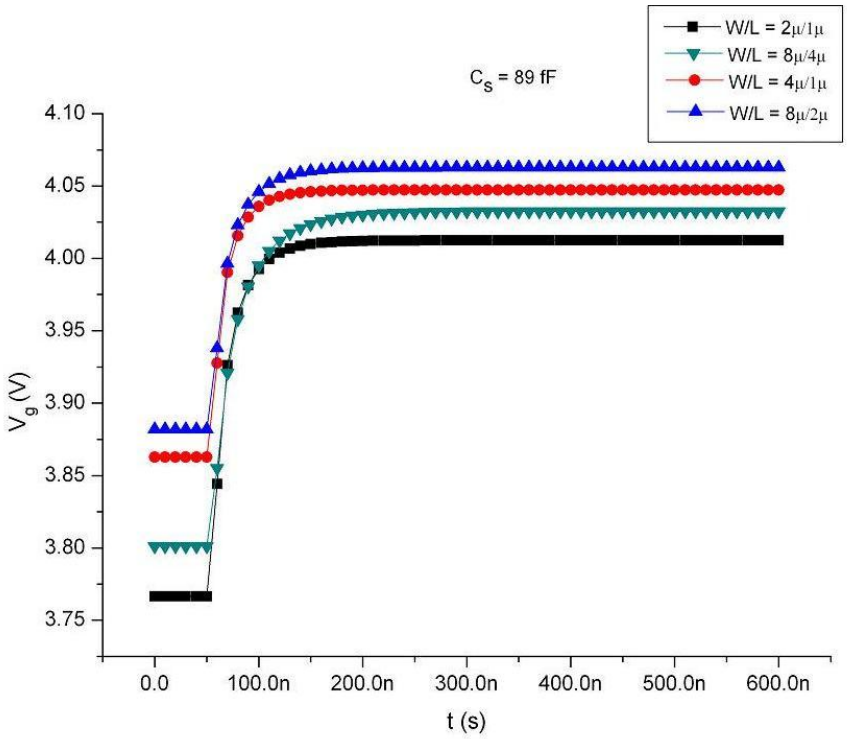


Figure 4.16 The gate voltage V_g with the different transistor size

Simulation results with this basic circuit indicate that the response time of the storage capacitor depends on the capacitance of the storage capacitor as well as the transistor size. The dimension of the storage capacitor and the driving transistor should be selected carefully if the time sequence requirement is strict.

The switch time of OLED device is fast, usually in the nano second range, so the lower limit of the time response is dependent on the RC constant of the pixel circuit, or particularly, the charge time of the storage capacitor. According to the simulation results above, we find the charging time for the capacitor used is around tens of nano seconds. It matches the switch time of the OLED device, so the lower limit of the time response can be satisfied with the capacitor provided by the foundry used in our design.

4.4 Implementation of the Proposed Pixel Circuit

From the analysis, we find that the main challenge of the pixel circuit design is to provide a stable driving current for the OLEDs especially when this current is extremely small for the lower level grey scale display, which is in the range of nano amperes. Compensation is a common strategy used to maintain a stable working state of the pixel circuit.

In the proposed pixel circuit, T2 and T3 are used to maintain the gate voltage of driving transistor T1 when distortion happens during the driving period.

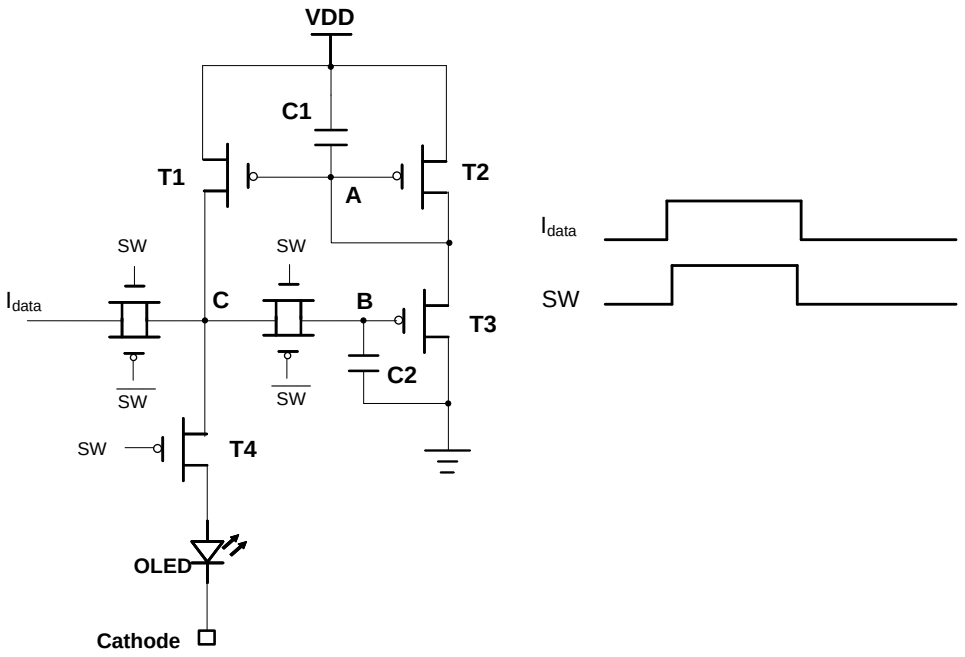


Figure 4.17 The proposed pixel circuit for OLED-on-Silicon microdisplay

When the SW signal is valid and the display data current flows into the pixel circuit, the gate voltage of T1 is charged appropriately to a certain value to produce the current I_{T1} which is equal to the input data current I_{data}. At the same time, both storage capacitors C1 and C2 are charged and due to the current mirror structure, $I_{T1} = I_{T2} = I_{T3}$.This is the programming period of the pixel circuit operation.

Then in the driving period, when the current source is removed, due to the switch feedthrough, or the leakage current, the stored gate voltage of T1 is distorted. The protection of the gate voltage is implemented by the branch circuit consisting of T2 and T3.

In the driving period, the variation of the voltage at point A is given by

$$\Delta V_A = \frac{\Delta I_{T2}}{g_{m2}} = \frac{\Delta I_{T1}}{g_{m1}} \quad (4\text{-}8),$$

where $g_m = \mu C_{ox} \frac{W}{L} \left| V_{gs} - V_t \right|$ is the transconducatance in the saturation region.

Due to the current flow, the drain current of T3 also varies by $\Delta I_{T3} = \Delta I_{T2} = \Delta I_{T1}$. So the gate voltage of T3 also changes by ΔV_B which is calculated by

$$\Delta V_B = \frac{\Delta I_{T3}}{g_{m3}} = \frac{\Delta I_{T2}}{g_{m2}} = \frac{\Delta I_{T1}}{g_{m1}} \quad (4\text{-}9).$$

The variation of the gate voltage causes the discharge of the storage capacitor C2 and the discharge current $I' = \Delta V_B C_2$. The discharge current flows into the point C to compensate I_{T1}, the drain current of T1. If we can ensure $I' = \Delta I_{T1}$, the driving current can be perfectly compensated. With carefully designed components' parameters, the relationship of $I' = \Delta I_{T1}$ can be fulfilled and the performance of the pixel circuit improves greatly.

Due to the chip area limitation for the OLED-on-Silicon microdisplay, the size of the component is expected to be smaller so the selection of the parameters is

limited in a narrow range. The parameters used for simulation are listed in Table 4.1 and the simulation results are shown in Figure 4.18.

Table 4.1 Components parameters of the proposed pixel circuit

W(T1, T2, T3)	4 μm
L (T1, T2, T3)	2 μm
C1	22.5 fF
C2	22.5 fF
VDD	5 V
I_{data}	2500 nA ~ 156.25 nA 16 steps and 1 step = 156.25 nA

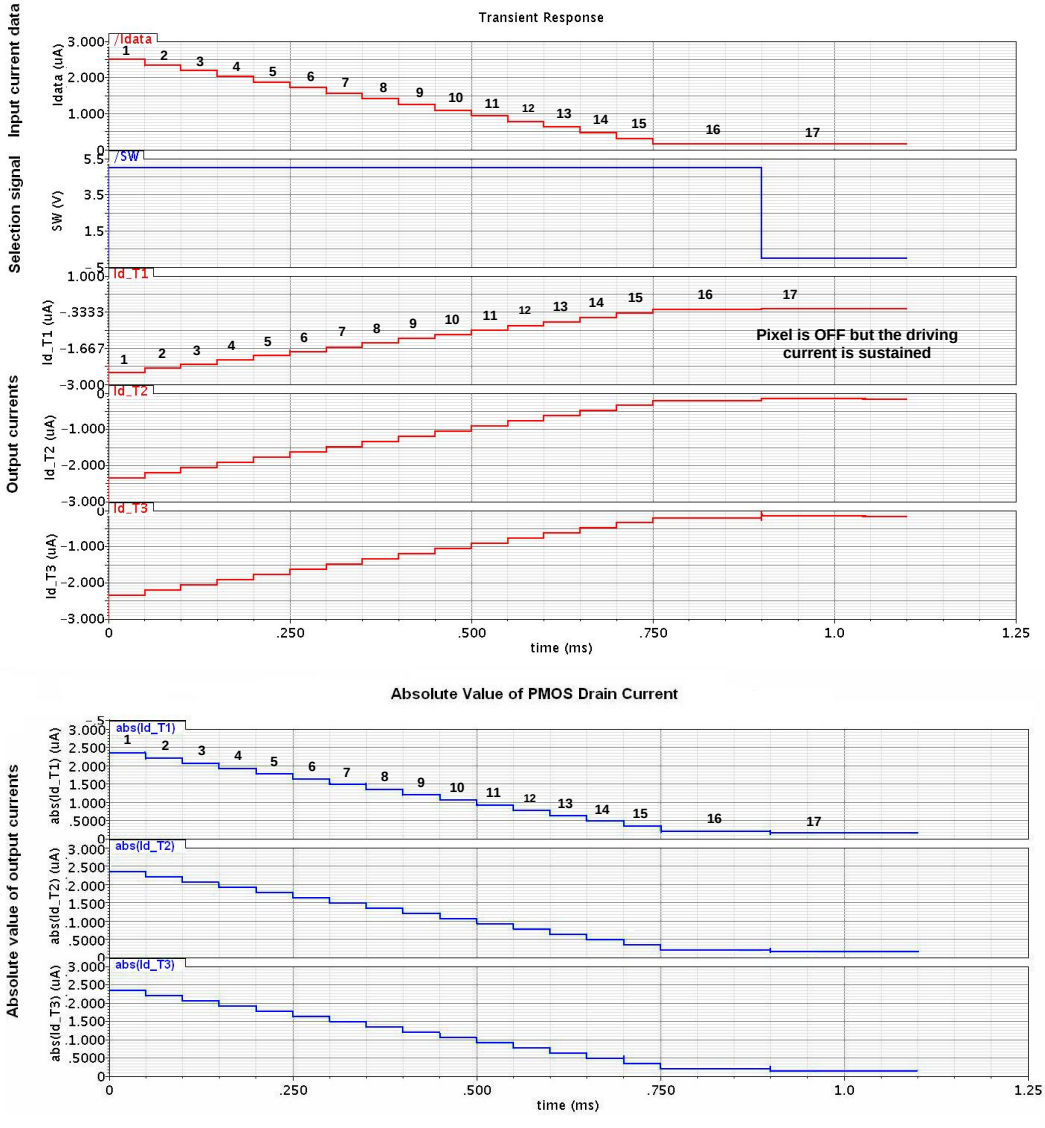


Figure 4.18 Simulation results of the proposed pixel circuit

Shown in Figure 4.18, we can find that when the pixel circuit stays on, the pixel driving current varies following the variation of the input data current. When the pixel circuit is off, the pixel current keeps the same level because the storage capacitor assists to sustain the same gate voltage of the transistors.

The simulation results of the proposed pixel circuit are also listed in Table 4.2.

Table 4.2 Simulation results of the proposed pixel circuit

No.	I_{data} (nA)	I_{d_T1} (nA) (Absolute Value)	I_{d_T2} (nA) (Absolute Value)	I_{d_T3} (nA) (Absolute Value)
1	2500.00	2567.9697	2351.2746	2351.2722
2	2343.75	2412.0466	2207.2143	2207.2119
3	2187.50	2256.1331	2063.1763	2063.1739
4	2031.25	2100.2300	1919.1658	1919.1633
5	1875.00	1944.3385	1775.1891	1775.1866
6	1718.75	1788.4601	1631.2549	1631.2524
7	1562.50	1632.5965	1487.3750	1487.3725
8	1406.25	1476.7497	1343.5652	1343.5626
9	1250.00	1320.9226	1199.8477	1199.8451
10	1093.75	1165.1188	1056.2540	1056.2514
11	937.50	1009.3433	912.8302	912.8302
12	781.25	853.60375	769.6449	769.6422
13	625.00	697.91155	626.8054	626.8026
14	468.75	542.28652	484.4862	484.4834
15	312.50	386.76745	342.9945	342.9916
16	156.25	231.45082	202.9417	202.9387
17	156.25	216.38265	155.0537	155.0523

Current duplication can also be achieved with the current copier circuit. Comparison is implemented between the proposed pixel circuit and the current copier (shown in Figure 4.18). Table 4.3 lists the parameters of the current copier.

Table 4.3 Component' parameters of the current copier

W (T1)	4 μm
L (T1)	2 μm
C1	22.5 fF
VDD	5V
I_{data}	2500 nA ~ 156.25 nA 16 steps and 1 step = 156.25 nA

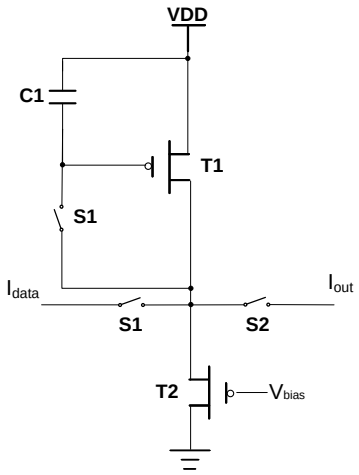


Figure 4.19 The current copier

The simulation results of the current copier are listed in Table 4.4.

Table 4.4 Ideal value and the simulation results of both the proposed pixel circuit and the current copier

No.	I_{data} (nA)	I_{d_T1} (nA) (Absolute Value)	$I_{current\ copier}$ (nA) (Absolute Value)
1	2500.00	2567.9697	2317.2793
2	2343.75	2412.0466	2171.5318
3	2187.50	2256.1331	2025.9010
4	2031.25	2100.23	1880.3880
5	1875.00	1944.3385	1734.9943
6	1718.75	1788.4601	1589.7207
7	1562.50	1632.5965	1444.5685
8	1406.25	1476.7497	1299.5389
9	1250.00	1320.9226	1154.6332
10	1093.75	1165.1188	1009.8526
11	937.50	1009.3433	865.1983
12	781.25	853.6038	7206.717
13	625.00	697.9116	576.2741
14	468.75	542.2865	432.0067
15	312.50	386.7675	287.8710
16	156.25	231.4508	143.8683
17	156.25	216.3827	141.7829

The differences between the actual output pixel currents and the ideal values $\Delta I_k = I_k - I_{ideal,k}$ are indicated in Figure 4.20. We can point out that the output current variation of the proposed pixel current is much more crucial than that of the current copier. We should notice that the output current of the current

copier is smaller than the input data current. The possible reasons lie in the switch feedthrough, clock feedtrough and leakage current as mentioned. With the compensation circuit, the output current of the proposed pixel circuit is efficiently compensated and the match of the input and output current is improved to provide a more accurate driving current for the OLED devices.

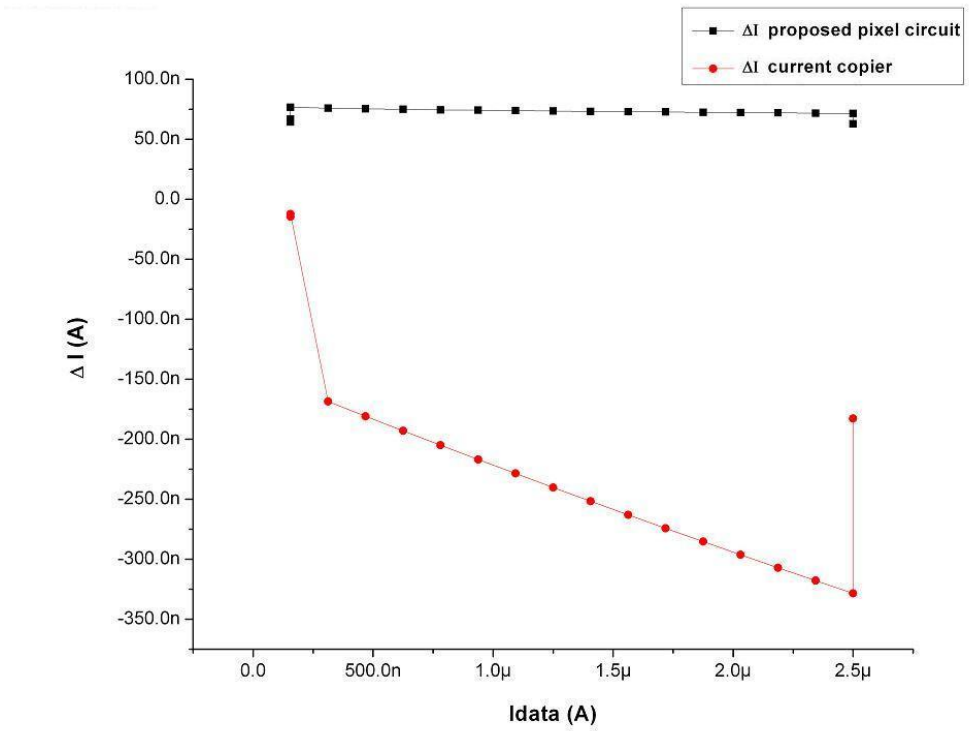


Figure 4.20 Comparisons of the proposed pixel circuit and the current copier

4.5 Layout Considerations

A current mirror is the basic element of the pixel circuit for a OLED-on-Silicon microdisplay. The match of the transistor pair is crucial to the performance of the pixel circuit. In the layout design, the transistor pair should be put as close as possible in order to reduce the mismatch caused by process variations of transistor width, length and doping concentration.

A capacitor is used to memorize the gate voltage of driving transistor for the driving period in this case; the value of the capacitor should not be too small. However, when the chip area is also concerned, a smaller size capacitor is preferred. In the CMOS process, metal-insulator-metal (MIM) and poly-insulator-poly (PIP) capacitors are commonly used. A PIP capacitor has larger capacitance per unit so it is suitable for the microdisplay application when the small chip area is a concern. [65]

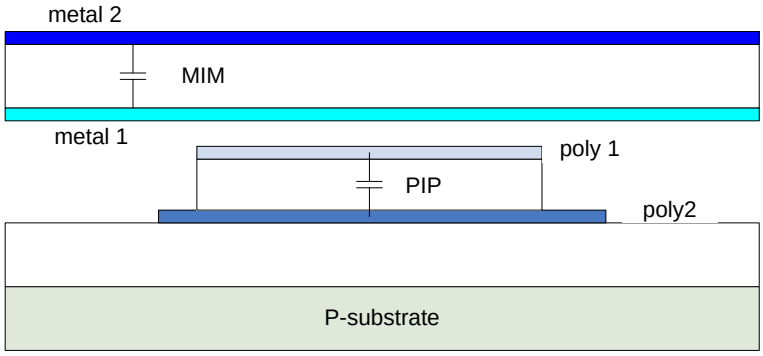


Figure 4.21 Different types of CMOS capacitors

But a PIP capacitor needs an additional poly layer and the manufacture cost increases. Another solution is to use the gate capacitor of an MOS transistor, which has a very thin dielectric layer for maximizing the capacitance.

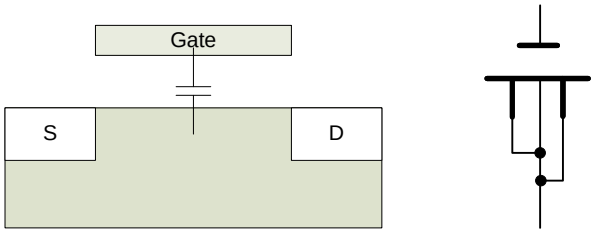


Figure 4.22 The gate capacitor of the MOS transistor

4.6 Conclusion

In this chapter, the working principle of the pixel circuit for the OLED-on-Silicon microdisplay is introduced. A voltage driving scheme and a current driving scheme are both reviewed. The luminance of the OLED is proportion to the current density, so the current driving scheme is our natural choice. Design considerations of the pixel circuit are discussed, like switch feedthrough, clock feedthrough and the transistor type. A pixel circuit based on the current driving scheme is proposed. Driving current compensation is implemented. Layout for the pixel circuit is carefully accomplished.

Chapter 5

Design of Current Mode DAC for OLED-on-Silicon Microdisplay

5.1 Introduction

A digital to analog converter (DAC) is used to transfer the digital signal of the discrete time domain to the analog signal used in the continuous time domain. It plays the important role in the mixed-signal circuit. DACs typically can be classified as the voltage mode or the current mode according to the output signal type. Commonly DACs are mainly formed by digital logic circuitry, switch network, reference circuits and analog active elements. A typical voltage mode DAC is shown in Figure 5.1. [66]

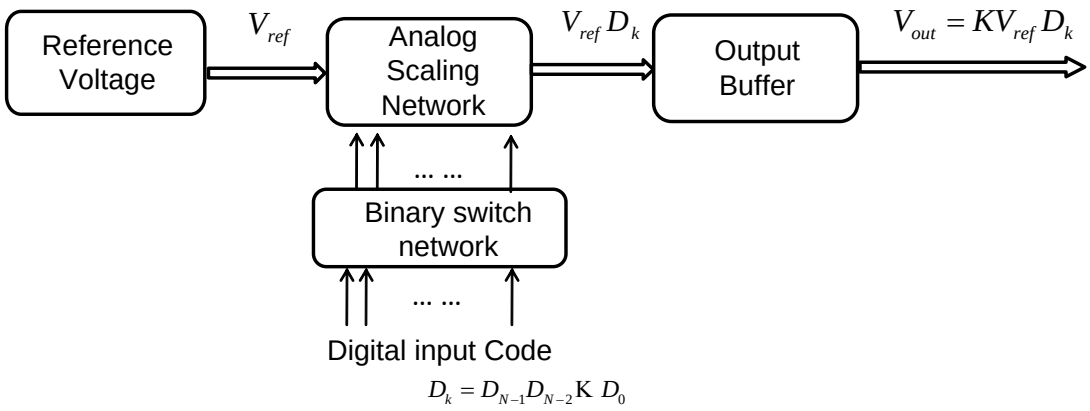


Figure 5.1 The basic voltage mode DAC

For an N-bit DAC, the digital input D_k is defined as

$$D_k = D_0 2^0 + D_1 2^1 + \mathrm{K} + D_{N-1} 2^{(N-1)} \quad (5\text{-}1)$$

Where each bit D_i is either '1' or '0', and D_{N-1} is the most significant bit (MSB) and D_0 is the least significant bit (LSB). And the LSB unit is defined as $1LSB = 1/2^N$.

The analog output signal V_{out} is related to the digital signal D_k using an analog reference voltage V_{ref} . The output voltage is calculated as

$$V_{out} = KV_{ref}\left(D_0 2^0 + D_1 2^1 + \Lambda + D_{N-1} 2^{(N-1)}\right) = KV_{ref} D_k \quad (5\text{-}2)$$

where K is a constant.

Another widely used DAC type is the current mode DAC. Advantages of current mode DACs lie in their high-current driving ability, high speed, high resolution and small circuit area. For an OLED-on-Silicon microdisplay, a DAC is used to convert the input digital video signal into analog current display data for the pixel circuit. A current mode DAC is easily to be integrated and is very suited for OLED driving. The basic structure of a binary-weighted current-steering DAC is shown in Figure 5.2.

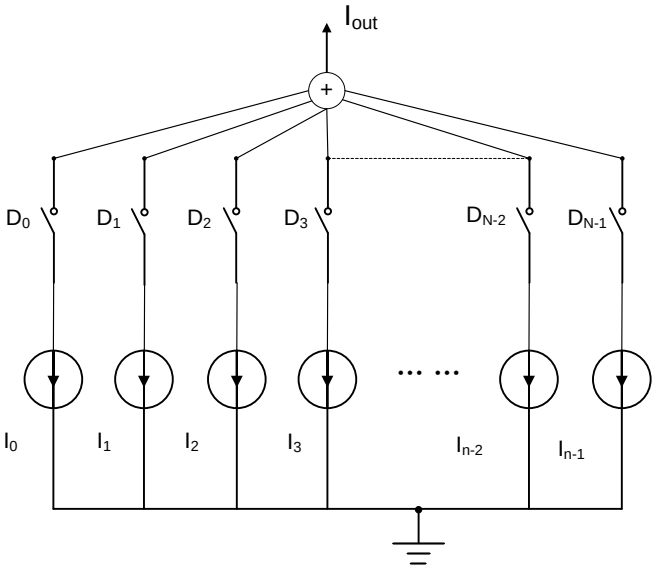


Figure 5.2 The Binary-weighted current-steering DAC

As shown in Figure 5.2, the output current is defined as $I_{out} = \sum_{k=0}^{N-1} D_k I_k$ (5-3),

where D_k is the input digital code which can be either binary weighted code or thermometer code (refer to section 5.3.2).

Based on the reviews of references [64, 66-77], the characteristics and the circuit architectures of the DACs are summarized. With the analysis of the previous work, our DAC design are exploited and implemented.

5.2 The Characteristics of the DACs

Resolution

The resolution of a DAC is defined as the number of distinct analog levels corresponding to the different input digital words. So N-bit resolution implies that the DAC can resolve 2^N distinct analog levels.

Differential non-linearity (DNL) and Integral non-linearity (INL)

Differential non-linearity (DNL) and integral non-linearity (INL) are the most important indicators of a DAC's static performance. DNL and INL are illustrated in Figure 5.3. The black dotted line indicates the ideal output curve of the DAC while the blue solid line presents the actual output of the DAC.

DNL is defined as the variation in analog step sizes away from 1 LSB,

$$DNL = Y'_{K+1} - Y'_K - LSB \quad (5\text{-}4)$$

where Y'_K is the actual analog output value.

INL is defined as the deviation from the ideal line

$$INL = \frac{Y'_K - Y_K}{LSB} \quad (5\text{-}5),$$

where Y'_K is the actual analog output value and Y_K is the ideal analog output value.

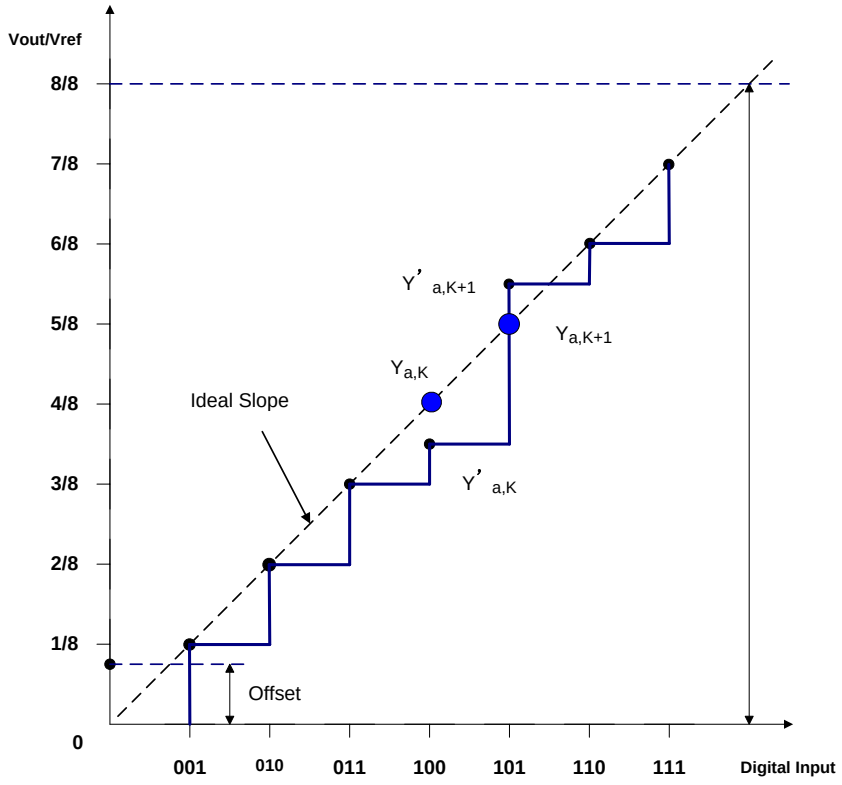


Figure 5.3 INL and DNL errors for DAC transfer function

An ideal DAC has a uniform step size and shows a linear characteristic of the data transfer function. But a real DAC will have variance in step size and a curvature to its transfer function. DNL and INL indicate how close the performance of the real DAC is to that of an ideal DAC.

Monotonicity

Monotonicity is an important characteristic of the static transfer function of DAC. A monotonic DAC is defined by the condition that the output always increases as the input increases; otherwise, it decreases as the input decreases. That means the variation of the DAC's transfer response of two adjacent stages is either positive or negative all of the time.

Offset and Gain error

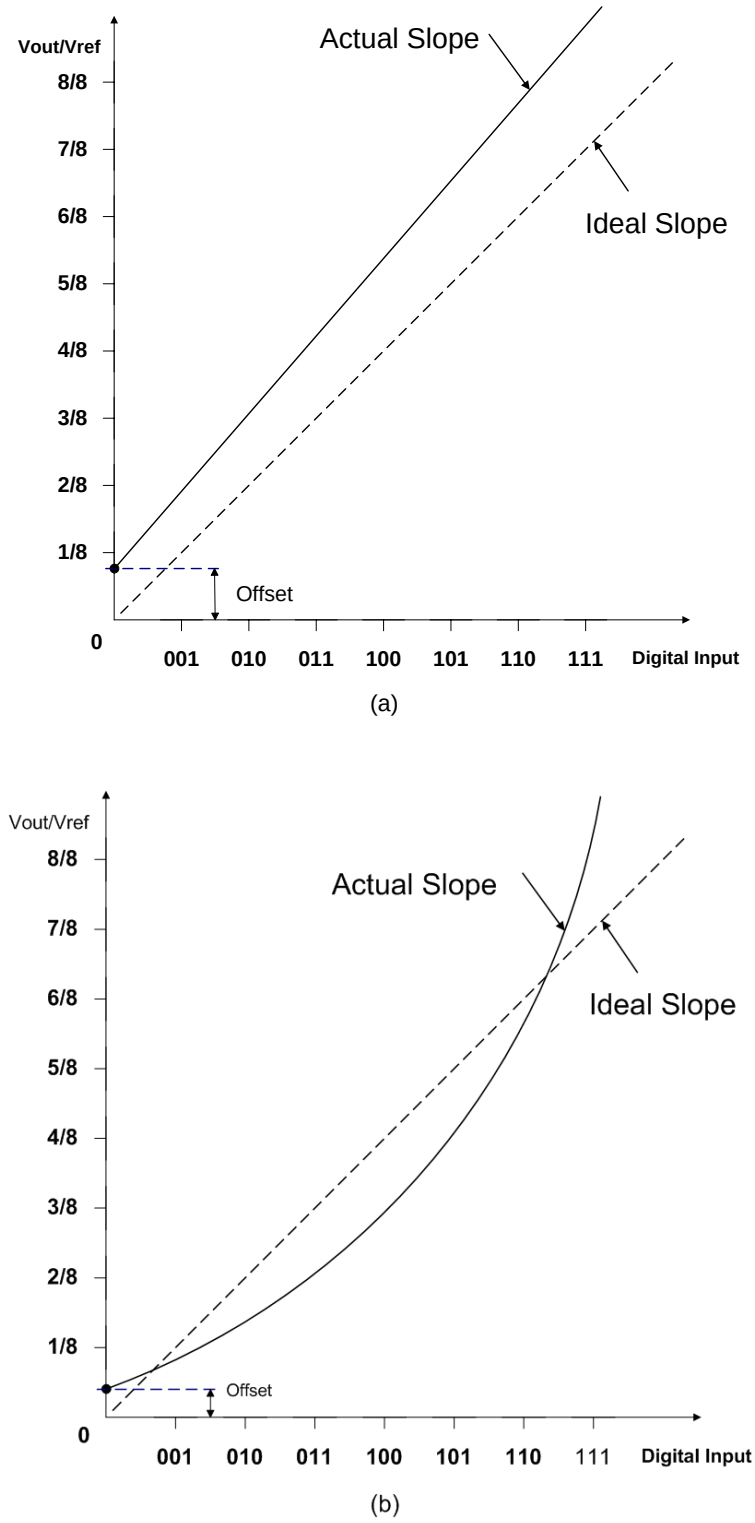


Figure 5.4 (a) The offset error (b) The gain error of DAC

The offset error E_{off} is defined to be the output that occurs for the input code that should produce zero output

$$E_{off} = \frac{Offset}{V_{LSB}} \quad (5\text{-}6).$$

The gain error is defined as the difference at the full-scale value between the ideal and actual curve when the offset error has been reduced to zero. The gain error indicates the error of the actual output and it can be linear or non-linear.

The actual output with a linear gain and offset error can be expressed as

$$Y' = E_{gain} Y + offset \quad (5\text{-}7),$$

where E_{gain} is the gain error

While the actual output with a non-linear gain error is

$$Y'_a = (\sum_{k=1}^{N-1} E_{gain,K} Y_{a,K}) + offset \quad (5\text{-}8)$$

Dynamic range

The dynamic range of DAC is specified as the ratio of the root mean square (rms) value of the maximum amplitude input sinusoidal signal to the rms output noise plus the distortion measured when the same sinusoid is present at the output. The dynamic range can be expressed as 2^N.

Glitch

Glitches are caused by the switch time difference during switching input signal bits. If glitches happen when the digital input 0111 1111 changes to 1000 0000, it is possible that the output current temporarily falls to zero in which case the LSBs

turn off slightly before the MSB. Contrarily, the output will temporarily increase to the maximum value.

5.3 Architectures of Current Mode DACs

5.3.1 Binary-weighted Current Mode DACs

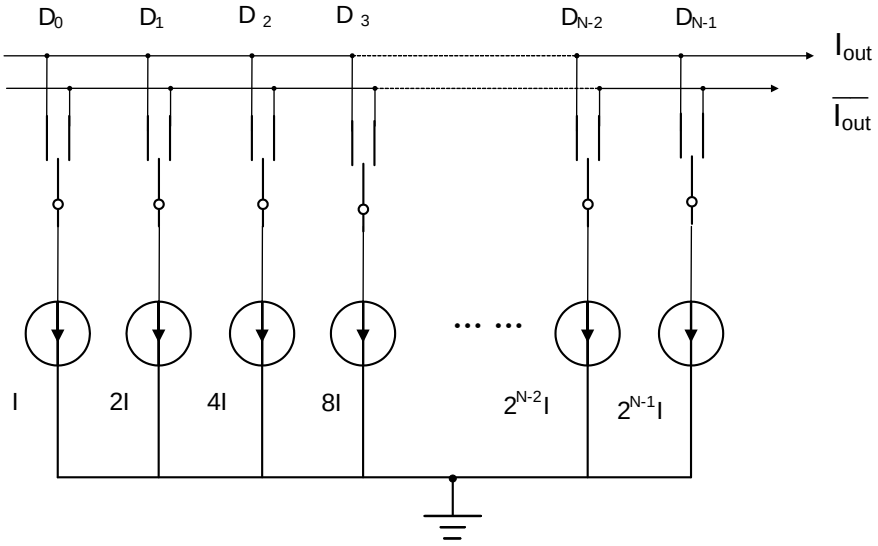


Figure 5.5 The binary-weighted current mode DAC

The binary weighted architecture is mentioned in the previous paragraphs. A typical binary-weighted current mode DAC is shown in Figure 5.5. In this binary-weighted current mode DAC, the dimensions of the current sources are one, two, four and eight, the power of 2 times of the reference current source. The current sources are controlled by the digital input bits. Small chip area and high speed can be achieved by this architecture. Glitch is the main disadvantage of such structure. It is also sensitive to device mismatch.

5.3.2 Thermometer-code Current Mode DACs

Glitches are minimized in the thermometer-code current mode DACs. Thermometer-code is different from binary code. The thermometer code is

numerical based system and it works similarly to a thermometer. In thermometer code, there is one digital level for each possible output code, e.g. 8 levels for 3 bit, and for a given analog input at all digital levels below the input value are '1' and all above are '0'. It has $2^N - 1$ digital inputs to represent 2^N different values so it has the advantage of low DNL, good monotonicity and less glitches. The conversion of the thermometer code and 3 bit binary code is shown in Table 5.1

Table 5.1 The transformation of thermometer code and binary code

Decimal Code	Binary Code			Thermometer Code						
	B1	B2	B3	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

In the thermometer code current mode DACs, the current source matrix consisting of the same size current cell is addressed by the row and column decoders. The graded matching error of the binary weighted current sources is minimized. The output changes only 1 LSB at a time so the glitches are greatly reduced. The basic structure of the thermometer code current mode DAC and the basic current cell are shown in Figure 5.6(a) and 5.6(b) respectively.

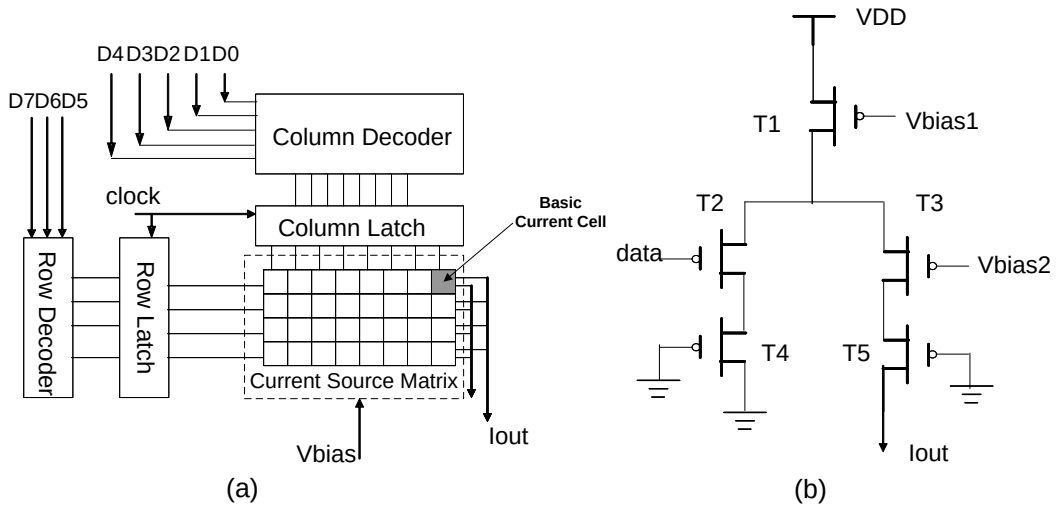


Figure 5.6 (a) The basic architecture of thermometer code current mode DAC (b) The basic current cell used for thermometer code current mode DAC

One disadvantage is a full thermometer code current mode DAC will consume a large amount of chip area. It is challenging to use full thermometer code to represent all bits of high resolution data conversion. The number of switches and the complexity of the circuit grow exponentially with increasing resolution. For microdisplay application, with the strict requirement of the small chip area, the thermometer code current mode DAC loses its competitiveness.

5.3.3 Segmented Current Mode DACs

Segmented current mode DACs (shown in Figure 5.7) provide the most popular solution for good linearity and minimum glitches. In this approach, the MSBs are usually realized by thermometer coding and the LSBs are formed by binary weighted current sources. The thermometer code current mode DAC architecture ensures the monotonicity and reduced glitch noise. And the usage of binary-weighted current mode DACs architecture optimizes the chip area.

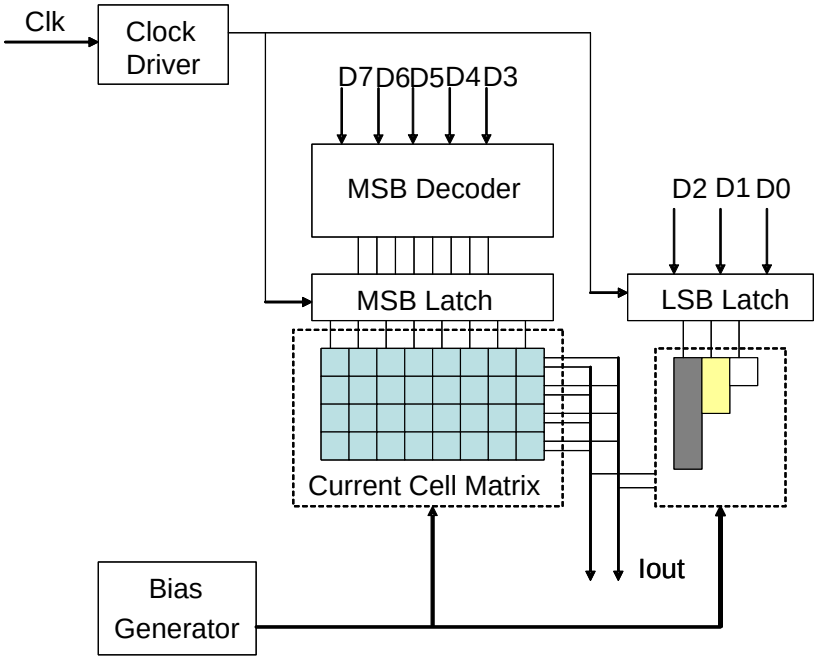


Figure 5.7 The segment current mode DAC

But for a microdisplay, the chip area consumption of segmented current mode DACs is still too large and with increasing resolution, the number of DAC cells increases greatly. In this case, optimized current mode DAC architecture needs to play a delicate tradeoff with the chip area and the circuit complexity, and the circuit performance.

5.4 Implementation of the Proposed Current Mode DACs

A current mode DAC based on the current dividing operation is employed in order to optimize the chip area. For OLED-on-Silicon microdisplay, very tight area constraint is on the current mode DAC for each column drivers, especially with the increase of the pixel density for the microdisplay with high resolution.

The architecture of the 4-bit proposed current mode DAC is illuminated in Figure 5.8. The current mirror is used to divide the current I_{ref} into two equal current flows. The current mirror can be used as a kind of the current divider. If the

matching between T1 and T2 is sufficient and the two drain currents $I_{d,T1}$ and $I_{d,T2}$ are equal to each other with the value of $I_{ref}/2$.

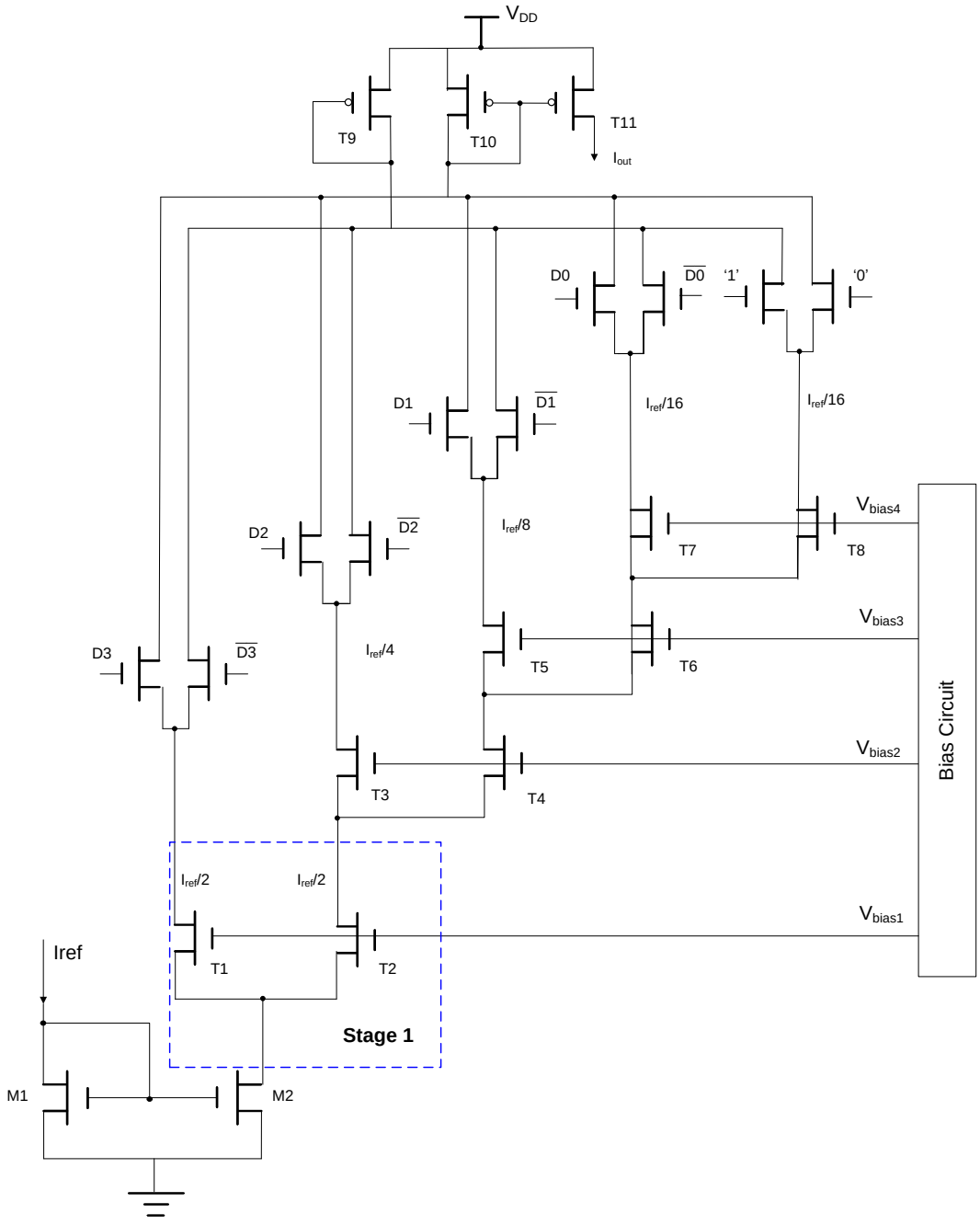


Figure 5.8 The 4-bit proposed current mode DAC using common current mirror

The main advantage of such cascade architecture is the less chip area used in the design. Comparison is demonstrated between the 4-bit binary-weighted current mode DAC (shown in Figure 5.9 (a)) and the 4-bit proposed current mode DAC

using common current mirror (shown in Figure 5.9 (b)). The chip area of the unit current mirror pair is assumed as S_0. The total chip area of 4-bit binary-weighted current mode DAC is $15S_0$ while the proposed current DAC is $10S_0$. For this design, the chip area is reduced by 30%.

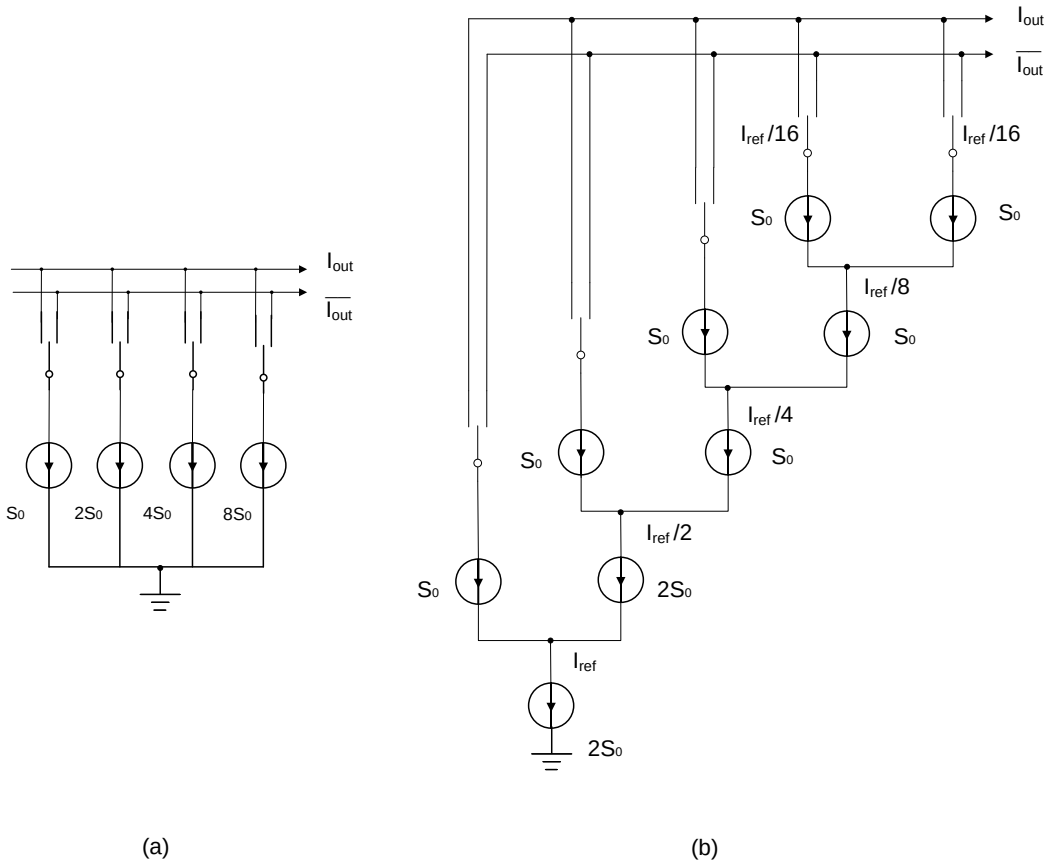


Figure 5.9 (a) The chip area of 4-bit binary-weighted current mode DAC (b) The chip area of 4-bit proposed current mode DAC using common current mirror

With increasing resolution, the chip area of the proposed architecture is much less than that of the binary-weighted structure. In Table 5.2, the comparison results are listed.

Table 5.2 The chip areas of the binary-weighted current mode DAC and the proposed current mode DAC using common current mirror

Resolution (N bit)	Chip area of the binary-weighted current mode DAC (in unit area S_0)	Chip area of the proposed current mode DAC using common current mirror (in unit area S_0)
4	15	10
8	255	18
10	511	22
12	3580	26

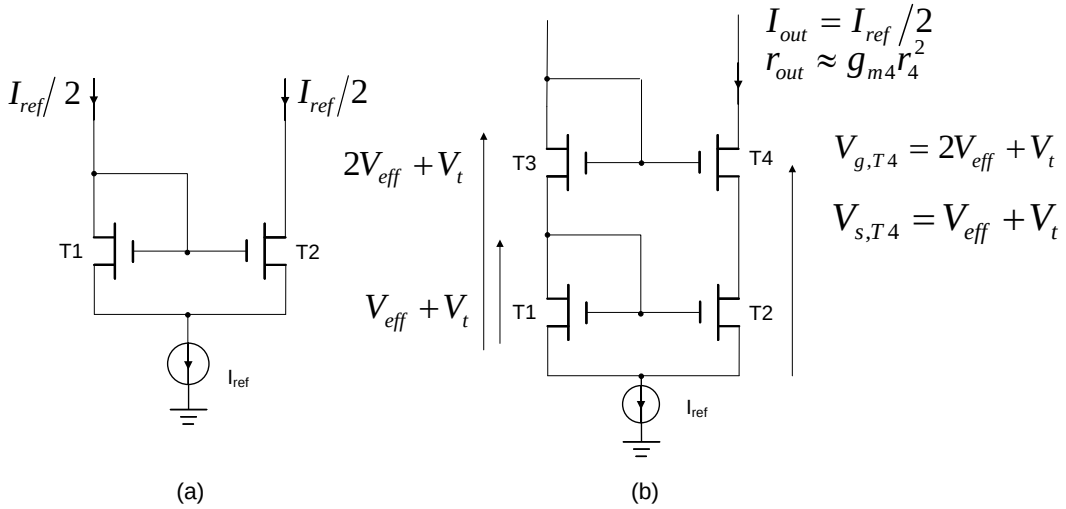


Figure 5.10 (a) The basic current mirror pair (b) The cascode current mirror

In practice, the channel length modulation λ should be taken into consideration and high accuracy of the current mirror pair is required. In the basic current mirror pair (as shown in Figure 5.10(a)), if the channel length modulation λ_1 and λ_2 are not close to zero, the current ratio is

$$\frac{I_{d,T2}}{I_{d,T1}} = \frac{W_2/L_2}{W_1/L_1}\frac{\lambda_2}{\lambda_1} \quad (5\text{-}9).$$

Since $\lambda \propto V_{ds}$, the output current also depends on the drain to source voltage V_{ds}. The variation of V_{ds} will introduce a difference between $I_{d,T1}$ and $I_{d,T2}$. To reduce the channel length modulation effect, one direct way is to increase the channel length L. But the large channel length will increase the size of the circuit chip area

as well as the parasitic parameters. One solution is to modify the basic current mirror pair. The cascode current mirror structure used for this DAC is shown in Figure 5.10(b). By using additional transistors T3 and T4, the cascode current mirror is formed. Because T1 and T3 are diode-connected transistors, the gate voltage of T4 is $V_{g,T4} = 2V_{eff} + V_t$, where $V_{eff} = V_{gs} - V_t$, and V_t is the threshold voltage and the source voltage of T4 is $V_{s,T4} = V_{eff} + V_t$. In this case, the drain-source voltage of T4 equals $V_{ds,T4} \geq V_{gs,T4} - V_t = V_{eff}$, so T4 remains in the saturation region. At the same time, the output resistance

$$r_o = r_4(1 + g_{m,T4}r_2) + r_2 \approx g_{m,T4}r_4^2 \quad (5\text{-}10),$$

assuming $r_4 = r_2$. The output resistance of the current mirror pair increases by 10-100 times to improve the circuit performance.

With the cascode current mirror pair for our design, the proposed 4-bit current mode DAC is redesigned as shown in Figure 5.11. Each output branch includes a cascode current mirror pair. At the same time, the MOS switch pair is used to control the output current flow. The digital logic signal (D_i) and the complementary logic signal ($\overline{D_i}$) are used to control the switch manner.

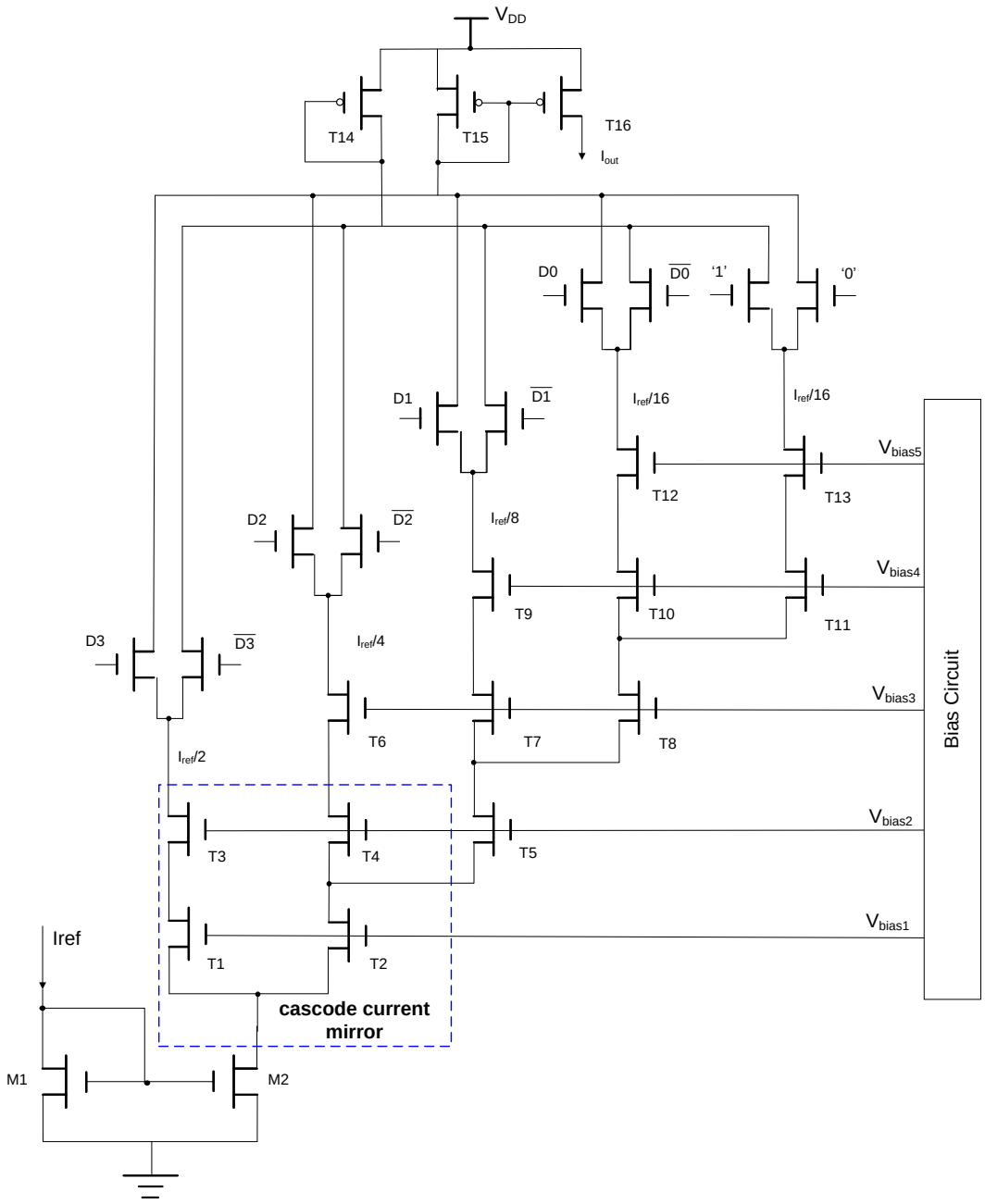


Figure 5.11 The 4-bit proposed current mode DAC using cascode current mirror

With a cascode current mirror, the chip area of the proposed 4 bit current mode DAC increases but for high resolution, the chip area of the proposed structure is still much smaller than the binary-weighted current mode DAC. Table 5.3 shows the comparison results.

Table 5.3 The chip areas of the binary-weighted current mode DAC and the proposed current mode DAC using cascode current mirror

Resolution (n bit)	Chip area of the binary-weighted current mode DAC (in unit area S_0)	Chip area of the proposed current mode DAC using cascode current mirror (in unit area S_0)
4	15	15
6	63	20
8	255	25
10	511	30

Another consideration of the current mode DAC is the voltage range. Similar to the analysis for the cascode current mirror pair, assuming all the transistors fall in the saturation region, the output voltage of the cascode current mirror network in our design is

$$\begin{aligned} V_1 &= V_{DS,M2} + V_{DS,T2} + V_{DS,T5} + V_{DS,T8} + V_{DS,T11} + V_{DS,T13} \\ &= \sqrt{\frac{I_{ref}}{\mu_n C_{OX}(W/L)_{M2}}} + \sqrt{\frac{I_{ref}/2}{\mu_n C_{OX}(W/L)_{T2}}} + \sqrt{\frac{I_{ref}/4}{\mu_n C_{OX}(W/L)_{T5}}} + \sqrt{\frac{I_{ref}/8}{\mu_n C_{OX}(W/L)_{T8}}} + 2\sqrt{\frac{I_{ref}/16}{\mu_n C_{OX}(W/L)_{T11}}} \end{aligned} \quad (5\text{-}11)$$

If the $(W/L)_{NMOS}$ ratios of all the NMOS transistors are the same, the output voltage V_1 is given by

$$V_1 = \frac{1-\left(\frac{1}{\sqrt{2}}\right)^5}{1-\frac{1}{\sqrt{2}}}\sqrt{\frac{I_{ref}}{\mu_n C_{OX}(W/L)_{T1}}} \approx 2.811\sqrt{\frac{I_{ref}}{\mu_n C_{OX}(W/L)_{T1}}} \quad (5\text{-}12)$$

If we have $I_{ref} = 2.5uA$, $(W/L)_{T1} = 1um/1um$ and according to the process used in our design, $\mu_n C_{OX} = 7\times10^{-5}$, the output voltage $V_{out} = 0.5312V = 531.2mV$, It is much less than the supply voltage.

On the other hand, when the output current reaches the maximum, $I_{out} = I_{ref}$ the voltage across the output PMOS pair is

$$V_{PMOS} = \sqrt{\frac{2I_{ref}}{\mu_p C_{OX}(W/L)_{T15}}} \quad (5\text{-}13)$$

If we have $I_{ref} = 2.5uA, (W/L)_{T15} = 3um/1um$ and according to the process $\mu_p C_{OX} = 2\times10^{-5}$, the voltage drop $V_{PMOS} = 0.2887V = 288.7mV$

So the maximum supply voltage for the cascode current mirror network is

$V_2 = V_{DD} - V_{PMOS} = 4.7113V$, where $V_{DD} = 5V$

$V_2 > V_1$, in this case, with careful design, we can satisfy the requirement of the voltage to make sure all the transistors in the cascode current mirror network work in the saturation region.

In the DAC circuit, bias reference is important because the transistors fall into the proper operation region when carefully designed bias voltage is applied. In the current mode DAC circuit design, bias voltage is derived from the power source using the MOS transistors. The basic bias circuit using MOS transistors can be designed as shown in Figure 5.12(a).

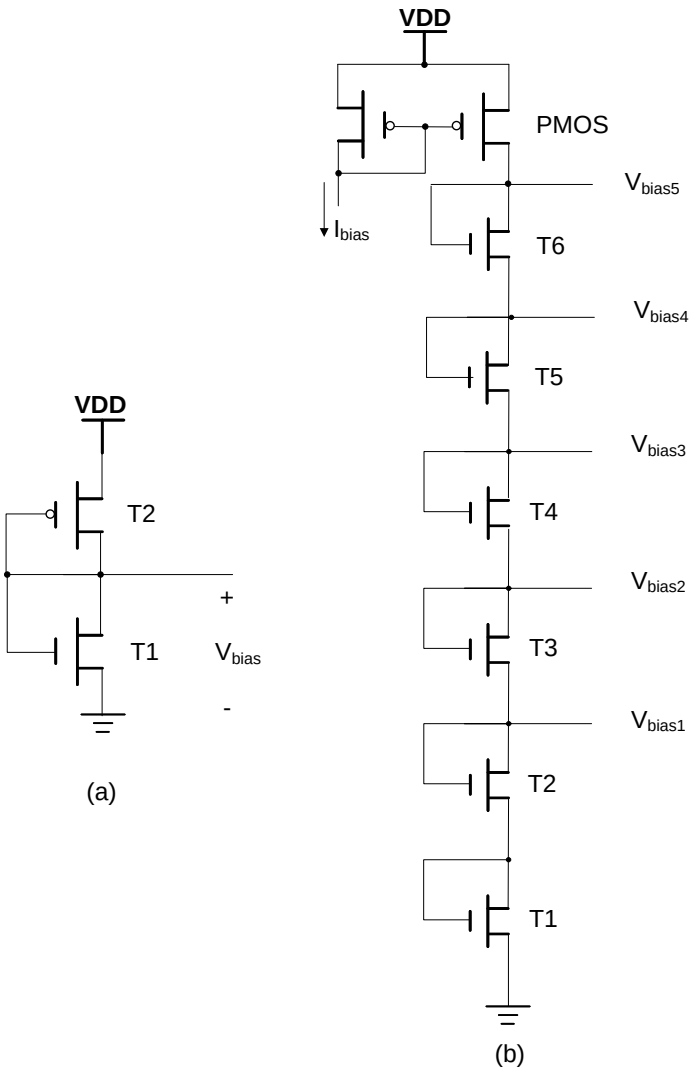


Figure 5.12 (a) The basic structure of the bias circuit using MOS transistors (b) The proposed bias circuit

Since $I_{D,NMOS} = I_{D,PMOS}$, we have

$$\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_n \left(V_{bias} - V_{TN}\right)^2 = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_p \left(V_{DD} - V_{TP}\right)^2 \quad (5\text{-}14)$$

The bias voltage is given by

$$V_{bias} = \frac{V_{DD} - V_{TP} + V_{TN}\sqrt{\dfrac{\mu_n C_{OX}\left(W/L\right)_n}{\mu_p C_{OX}\left(W/L\right)_P}}}{1 + \sqrt{\dfrac{\mu_n C_{OX}\left(W/L\right)_n}{\mu_p C_{OX}\left(W/L\right)_P}}} \quad (5\text{-}15)$$

With carefully designed W/L ratio, we can derive the bias voltage from the MOS only voltage divider.

If the bias voltage and the power supply voltage are known, the dimension of the transistors is calculated as

$$\frac{\mu_n C_{OX}(W/L)_n}{\mu_p C_{OX}(W/L)_p} = \left(\frac{V_{DD} - V_{bias} - V_{TP}}{V_{bias} - V_{TN}} \right)^2 \quad (5\text{-}16)$$

Moreover, by computing the partial derivatives of V_{bias} with respect to V_{DD}, the sensitivity of V_{bias} related to V_{DD} is given by

$$S_{V_{DD}}^{V_{bias}} = \frac{V_{DD}}{V_{DD} - V_{TP} + V_{TN}\sqrt{\frac{\mu_n C_{OX}(W/L)_n}{\mu_p C_{OX}(W/L)_p}}} \quad (5\text{-}17)$$

The MOS only bias voltage generator is sensitive to the power supply voltage, so a stable power supply is critical in the bias circuit design.

In order to generate suitable bias voltages for the proposed current mode DAC, a cascaded architecture for the bias circuit is shown in Figure 5.12(b). The bias voltage for the Nth-stage is

$$V_{bias,n} = \sqrt{\frac{2I_D}{\mu_n C_{OX}(W/L)_n}} + V_{bias,n-1} \quad (5\text{-}18).$$

By simply changing the dimension of MOS transistors, we can vary the bias voltage to fit for the requirement. In the cascode current mirror network in the proposed current mode DAC, the output current of each stage is decreased from

the bottom to top. So in the proposed bias circuit (shown in Figure 5.12(b)), from the bottom to top, the device area of each stage is increased in order to provide suitable bias voltage to keep the MOS transistors working in the saturation region. The bias current I_{bias} is set equal to the reference current I_{ref} of the current mode DAC. Table 5.4 shows the scaling of the transistor dimensions used in the proposed bias circuit.

Table 5.4 The transistors dimension scaling of the proposed bias circuit

T1	T2	T3	T4	T5	T6
$(W/L)_{T1}$	$2(W/L)_{T1}$	$4(W/L)_{T1}$	$8(W/L)_{T1}$	$16(W/L)_{T1}$	$32(W/L)_{T1}$

5.5 Layout Considerations

In the integrated circuit design, careful design of the layout can help to minimize the negative effect of device mismatch. For a basic current mirror, the process errors can cause the mirrored current to be significantly different from the reference current. Gate-oxide thickness, lateral diffusion, oxide encroachment and oxide charge density, *etc* will affect the performance of the current mirror. Layout methods can be used to reduce the effect of the parameter variations.

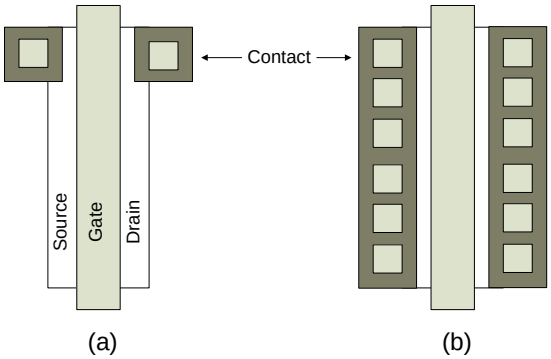


Figure 5.13 Contacts issue in the layout design for the current mirror

First, enlarge the channel length can reduce the channel length modulation λ.But large device results in larger parasitics. To reduce the diffusion resistance, more contact can be added along the width of both source and drain. More contacts give lower resistance, large current capability (as shown in Figure 5.14).

For a current mirror pair, to improve device matching, the two transistors are oriented in the same direction and the MOS transistors are also split into parallel devices, as illustrated in Figure 5.14 (a) or Figure 5.14(b).

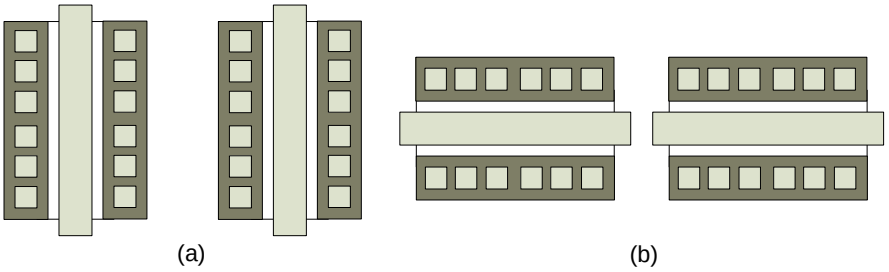


Figure 5.14 The transistor orientations of the current mirror pair

A practical method to arrange the current mirror pair is indicated in Figure 5.15. A common centriod strategy is used for the transistor placement to improve the matching. Such symmetrical structure is preferable to reduce the effect of the parasitic parameters. [77]

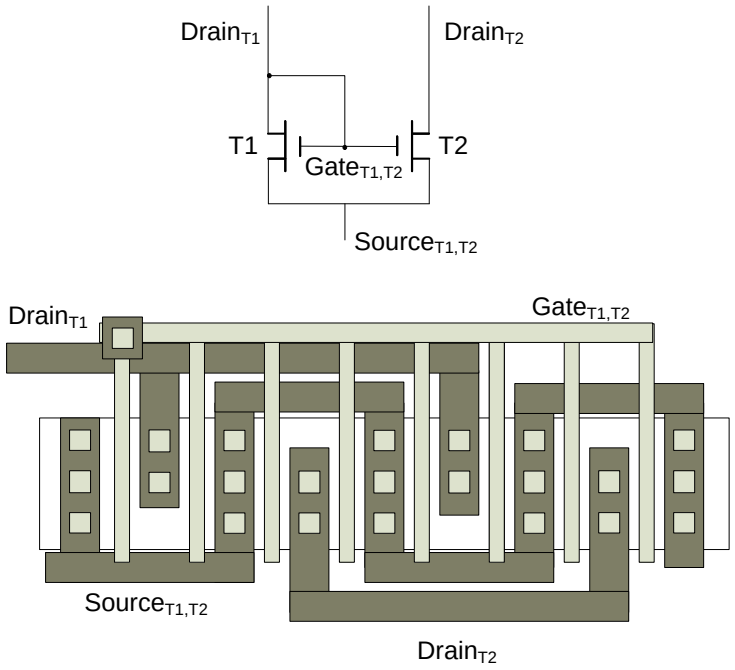


Figure 5.15 Common centroid placement of the current mirror pair

5.6 Simulation Results of the Proposed Current Mode DACs

The 4-bit proposed current mode DAC simulation results are shown in Figure 5.16(a) and 5.16(b). 16 levels of the output current vary from 2500nA to 156.25nA for a 16 level gray scale display.

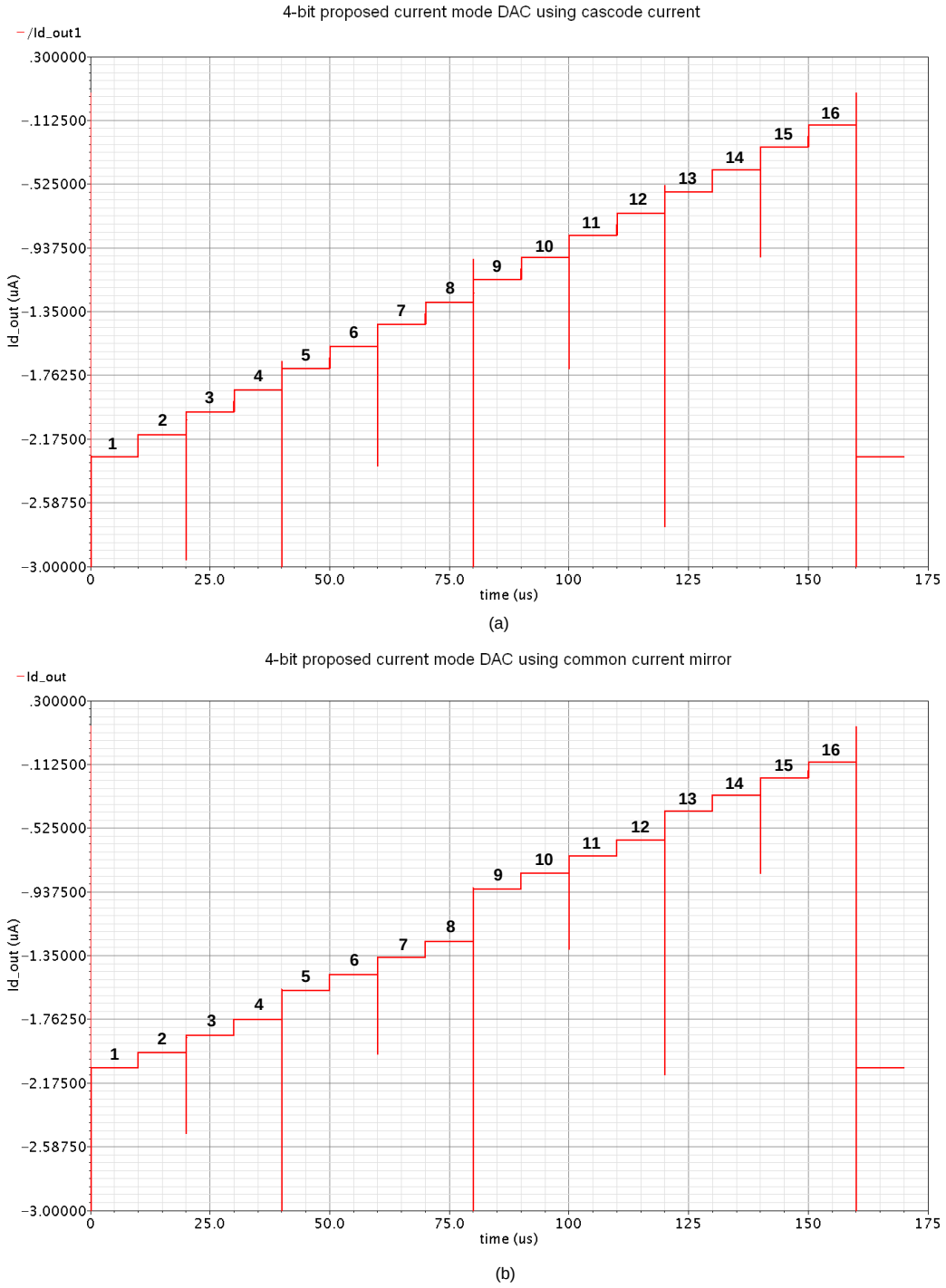


Figure 5.16 (a) Simulation results of 4-bit current mode DAC using cascode current mirror (b) Simulation results of 4-bit current mode DAC using common current mirror

The ideal output current and the actual output currents are indicated in Table 5.5 and Figure 5.17.

Table 5.5 The ideal output currents and the actual output currents of the proposed current-mode DAC

No.	I_{data} (nA) Ideal Value	$\lvert I_{d1} \rvert$ (nA) Using Casdode Current Mirror (Absolute Value)	$\lvert I_{d2} \rvert$ (nA) Using Common Current Mirror (Absolute Value)
1	2500.00	2291.048	2078.7996
2	2343.75	2148.0591	1978.1963
3	2187.50	2002.4696	1865.7002
4	2031.25	1859.2951	1765.2034
5	1875.00	1720.6399	1574.7141
6	1718.75	1577.6582	1474.2052
7	1562.50	1431.9915	1361.6913
8	1406.25	1288.9523	1261.2289
9	1250.00	1145.3044	918.03273
10	1093.75	1002.3919	817.57062
11	937.50	856.59816	705.02472
12	781.25	713.48214	604.59747
13	625.00	574.89347	413.99372
14	468.75	432.12491	313.60105
15	312.50	285.88599	200.98887
16	156.25	143.423	100.59104

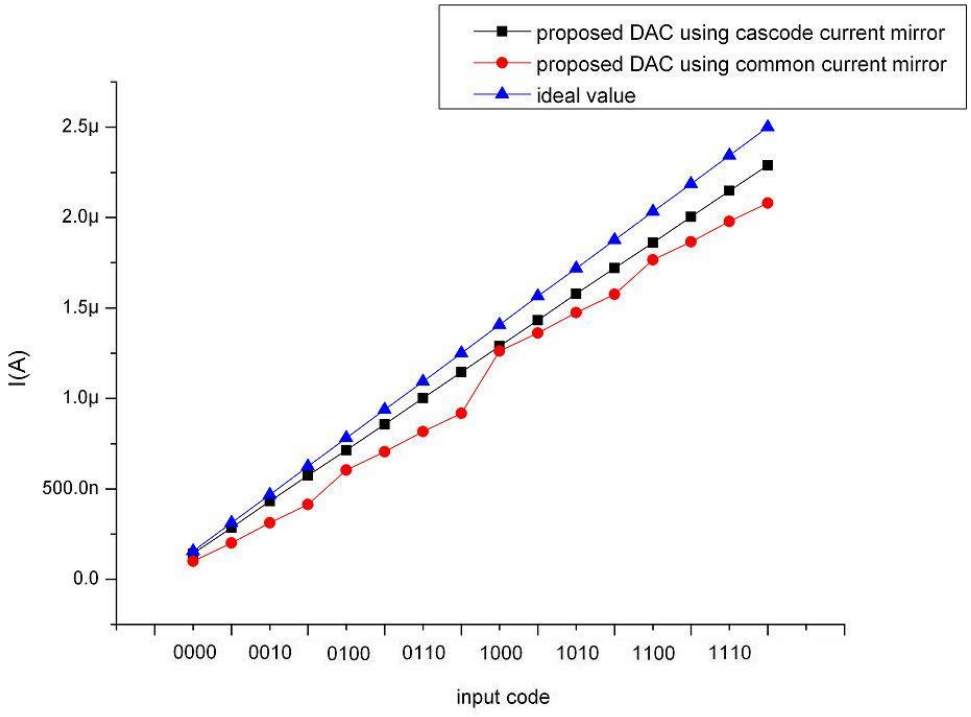


Figure 5.17 The ideal output current and the actual output currents of the 4-bit proposed current mode DACs

From the simulation results, we can say the offset error of the current mode DAC using a cascode current mirror is smaller than that of the current mode DAC using a common current mirror.

$$E_{off,DAC\ use\ cascode\ current\ mirror} = \frac{offset}{LSB} = \frac{(143.42nA) - (156.25nA)}{156.25nA} = -0.082$$

and $$E_{off,DAC\ use\ common\ current\ mirror} = \frac{offset}{LSB} = \frac{(100.59nA) - (156.25nA)}{156.25nA} = -0.36$$

The linearity of the current mode DAC using a cascode current mirror is better than that of the current mode DAC using a common current mirror. The gain error of the current mode DAC using a cascode current mirror is almost linear while the gain error of the current mode DAC using a common current mirror is non-linear. The gain errors are as shown in Figure 5.18.

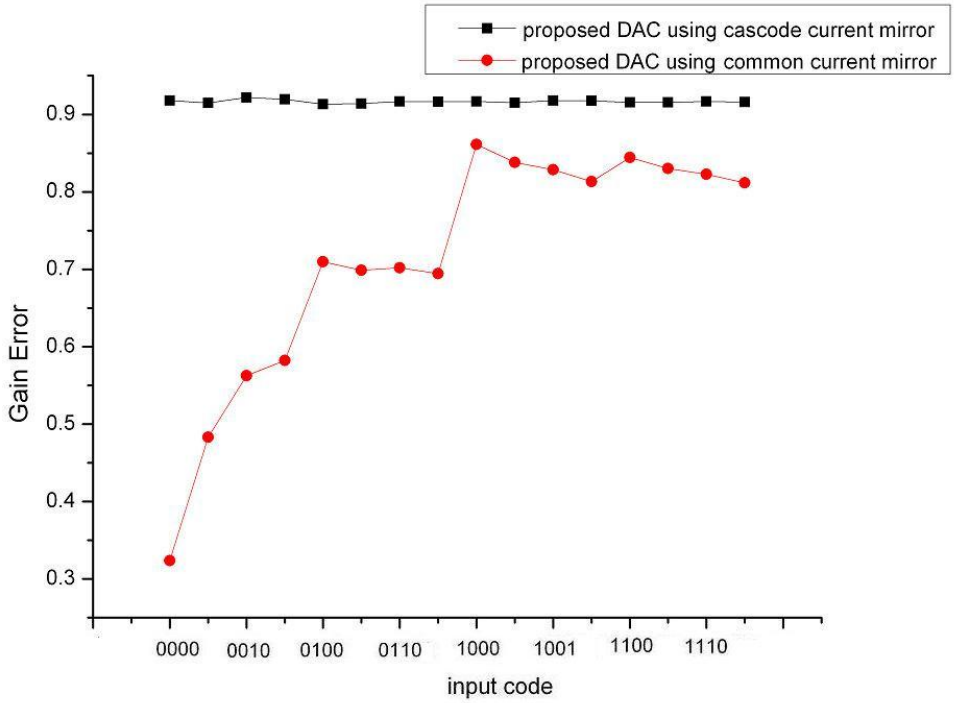


Figure 5.18 Gain errors of the 4-bit proposed current mode DACs

Besides the offset error and the gain error, the INL and DNL of the proposed current mode DACs are calculated and plotted as shown in Figure 5.19 and Figure 5.20.

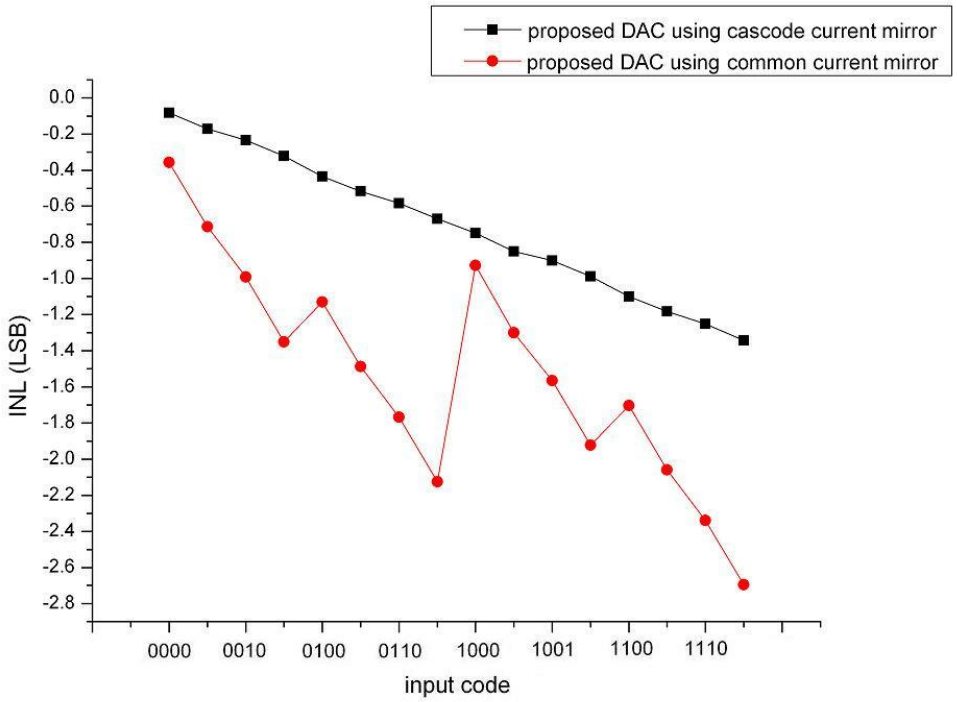


Figure 5.19 INLs of the 4-bit proposed current mode DACs

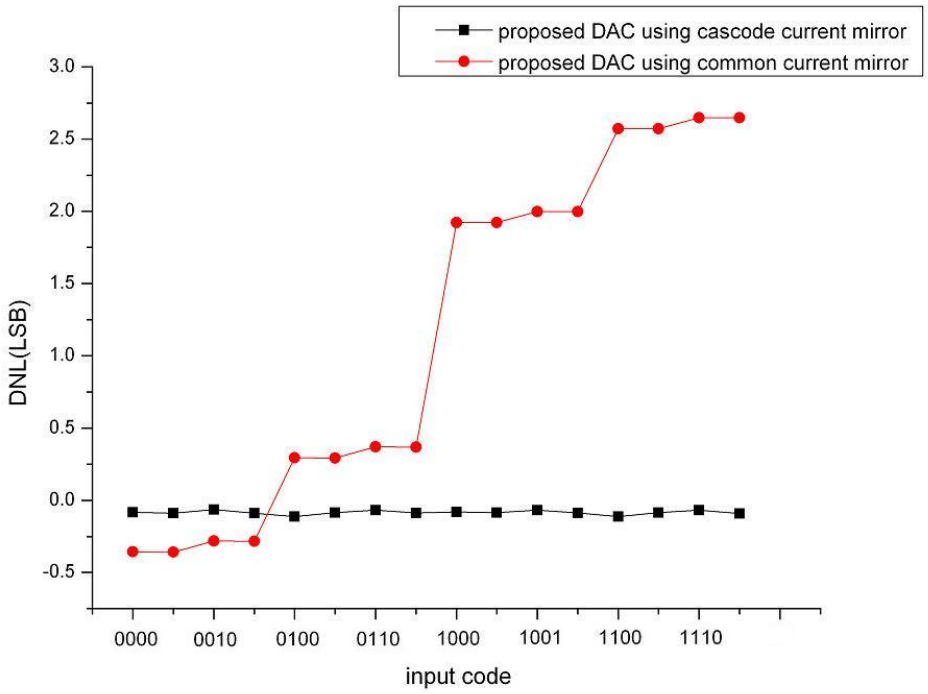


Figure 5.20 DNLs of the 4-bit proposed current mode DACs

From Figure 5.17, Figure 5.18, Figure 5.19 and Figure 5.20, we can find that the performances of the 4-bit proposed current mode DAC which uses a cascode current mirror are improved.

Table 5.3 summarizes the specifications of the 4-bit proposed current mode DACs. From the comparison, we point out that with the cascode current mirror, good INL and DNL performances are achieved. It is shown that the proposed current mode DAC using a cascode current mirror can work properly as we designed.

Table 5.6 Specifications of the proposed current mode DACs

Items	**4-bit current mode DAC using cascode current mirror**	**4-bit current mode DAC using common current mirror**
Technology	SMIC 0.35μm 3.5V/5.0V CMOS process	
Resolution	4 bit	
Power Supply	5V	
Power Dissipation	11.45μW ($I_{DAC,OUT,MAX}$=2.29 μA)	10.4 μW ($I_{DAC,OUT,MAX}$=2.08 μA)
INL	-0.11 LSB (worst case)	-2.34 LSB (worst case)
DNL	-0.08 LSB (worst case)	-2.65 LSB (worst case)

5.7 Conclusion

In this chapter, a current mode DAC is proposed for an OLED-on-Silicon microdisplay. Considering the tight chip area requirement of microdisplay application, the compact architecture of the current mode DAC is realised to reduce the circuit chip area. Comparing with the conventional binary-weighted current mode DAC, the proposed current mode DAC fulfills the main DAC performance specifications with the reduced chip area.

Chapter 6

Prototype of OLED-on-Silicon Microdisplay

6.1 Prototype of OLED-on-Silicon Microdisplay

A silicon backplane of a 160 × 120 OLED-on-Silicon microdisplay is implemented using Semiconductor Manufacturing International (Shanghai) Corporation (SMIC) 0.35μm custom silicon process. It opens opportunity to manufacture our own OLED-on-Silicon microdisplay application. The whole area of this circuitry is 8mm×6mm with the pixel size of 50μm×50μm. Line-at-a-time refresh mode is implemented with the integrated data buffer. 16 levels gray scales are achieved. The OLED layer will be deposited on the silicon backplane.

The die photo of the prototype is shown Figure 6.1. To protect the circuit from the light, the top metal layer of the CMOS process is used to shade the light. The bond ring is laid around the function circuit to indicate the die area.

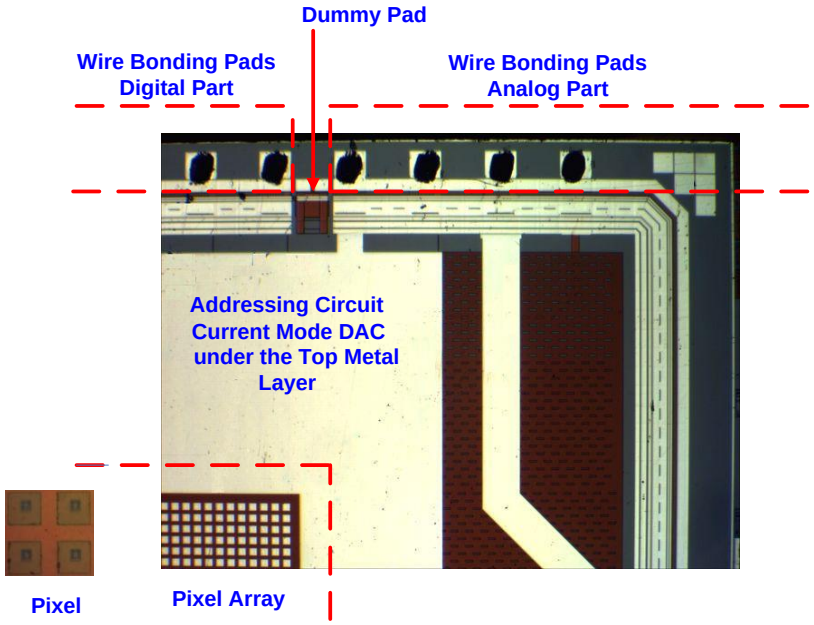


Figure 6.1 The top right corner of OLED-on-Silicon microdisplay prototype photograph

The OLED-on-Silicon is packaged employing the Chip-on-Board (COB) technique (illustrated in Figure 6.2). The microdisplay die is directly mounted on and electrically interconnected to its final circuit board, instead of undergoing traditional assembly or packaging as an individual IC. The pixel array is exposed for the OLEDs deposition.

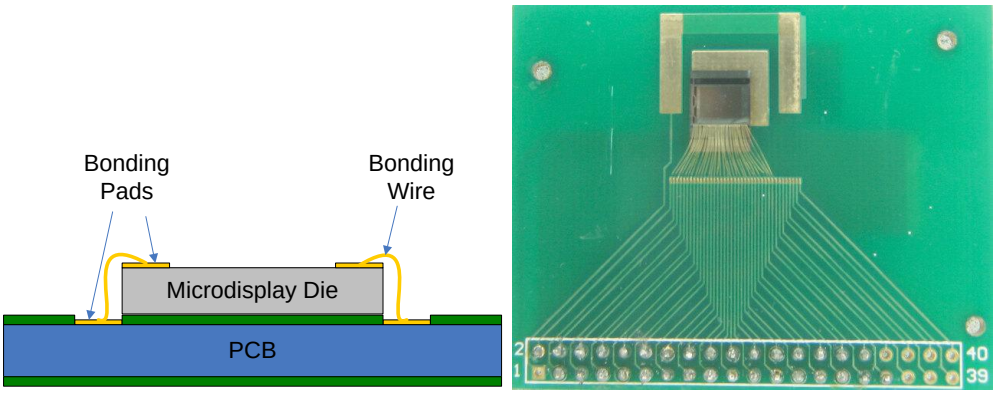


Figure 6.2 The COB package of OLED-on-Silicon microdisplay die

6.2 Measurement Results of the Prototype of OLED-on-Silicon Microdisplay

To test the prototype of the OLED-on-Silicon microdislay, a data generator is used to produce a sequence of stimuli to the chip under test and an oscilloscope is used to monitor and record the results. A Sony/Tektronix data generator DG2020A with P3420 pods are used to generate the input digital data and the clock signals for the prototype verifications. The maximum data rate is 200Mb per second and the amplitude of the signal can sweep from -3V to 7V. The test program is compiled in DG2020A and applied to the prototype under test. [79] The features of DG2020A and P3420 pods are listed in Table 6.1

Table 6.1 Specifications of DG 2020A and P3420 pods

Items	Description
DG2020A	
Data Rate	200 Mb/s
Data Resolution	4 digits
Data Width	Standard 12 bits, optional 24 or 36 bits
Pattern Depth	64K/chanel speeds
Variation of Output	Variable output delay and variable output level
System Interface	GPIB or RS-232
P3420 pods	
No. of Channels	12
Output Voltage Range	-3V to 7V
Resolution	0.1V
Output Current	< 500mA
Raise/Fall Time	< 2ns at 5 V_{p-p} swing

The prototype of OLED-on-Silicon microdisplay is bonded to a PCB with the connection header as the interface of the data generator and oscilloscope. The measurement setup is shown in Figure 6.3 and appendix section.

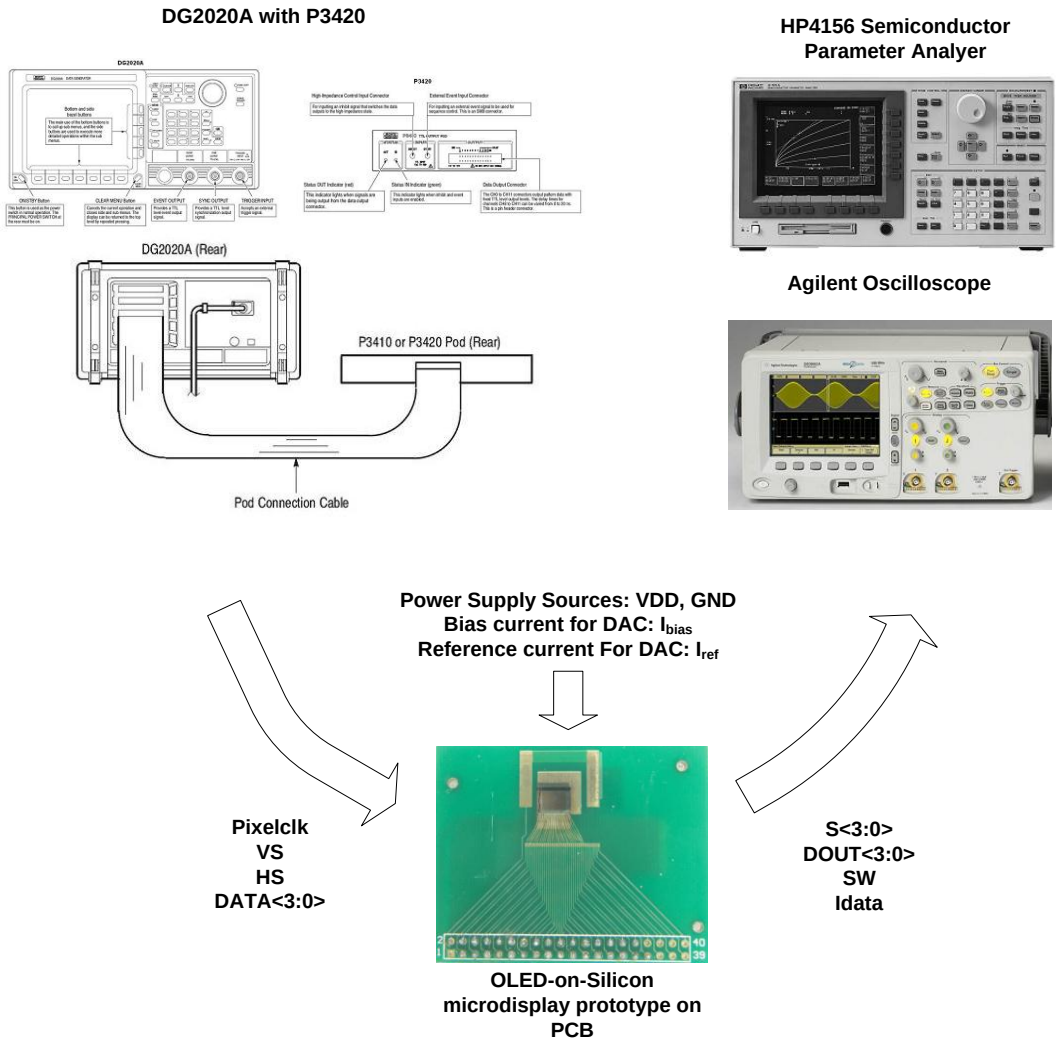


Figure 6.3 The OLED-on-Silicon microdisplay prototype measurement setup

For the measurement, first, we ramp the supply voltage from 0V to VDD, the current of the digital part remain zero because there is no clock signal applied. Then we enable the clock signals, dynamic current appears to indicate that the chip can be powered by the input data. The output waveform will be monitored and recorded in the oscilloscope. Analysis will be introduced in the following paragraphs.

4 bit digital input data DATA<3:0> are generated by DG2020A using the binary down counter data pattern that is the same as used in simulation. The data count

down from “1111” to “0000” in the time slot of two horizontal lines. The waveforms of the input signals are shown in Figure 6.4.

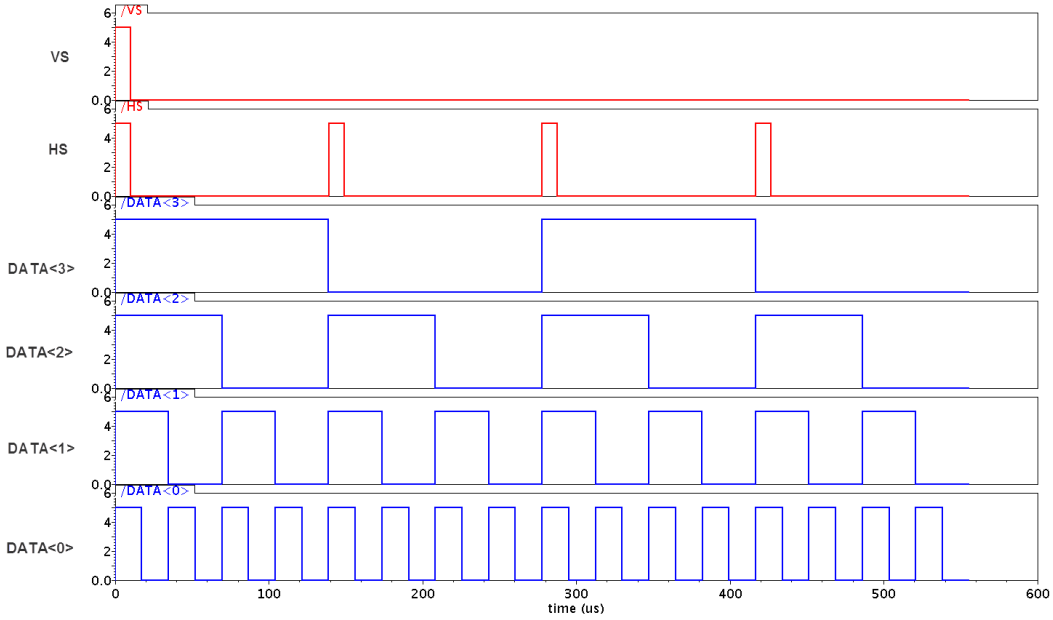


Figure 6.4 Input signals for OLED-on-Silicon microdisplay prototype circuit testing

Due to the consideration for the manufacture cost, as shown in Figure 6.5, only 1st stage of the shift register and the data latch are connected to the output pins for measurement.

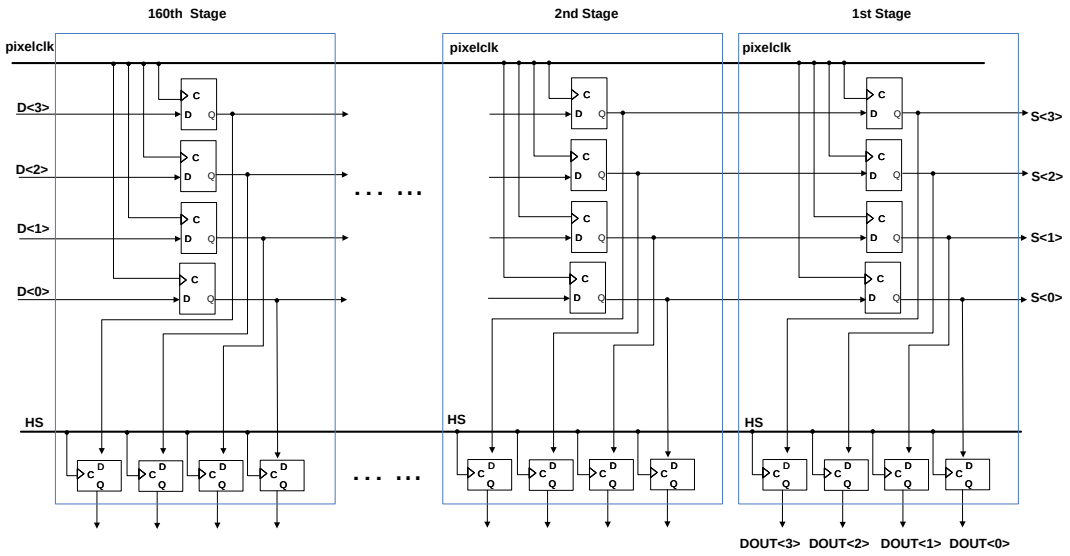


Figure 6.5 The data flow of the column addressing circuit of OLED-on-Silicon microdisplay prototype

S<3:0> is the output of the 1st stage shift register. Due to the shifting motion of the input data, the exact data of S<3:0> should be measured at the beginning of the second line. The exact data loaded in the 1st stage data latch should be sampled at every rising edge of the HS signal, so the expect output DOUT<3:0> switch between“1111” and “0111” clocked by the HS signal. And the expected output results of the column addressing circuit are shown in Figure 6.6.

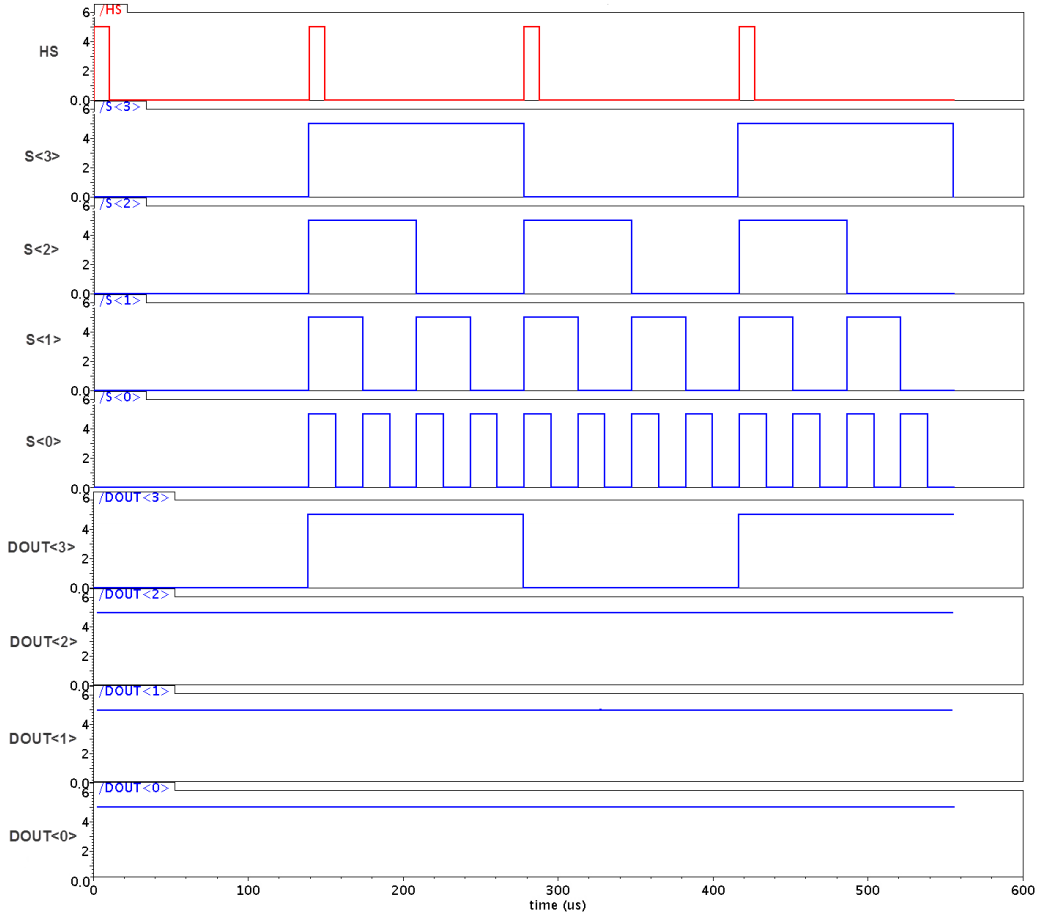


Figure 6.6 The expected output signals for the column addressing circuit of OLED-on-Silicon microdisplay prototype

As described in the Chapter 4, the CMOS switch is preferred to control the accessing motion of the pixel circuit. Two complementary signals ROWN and ROWP are generated by the row scanner to implement the row selection motion.

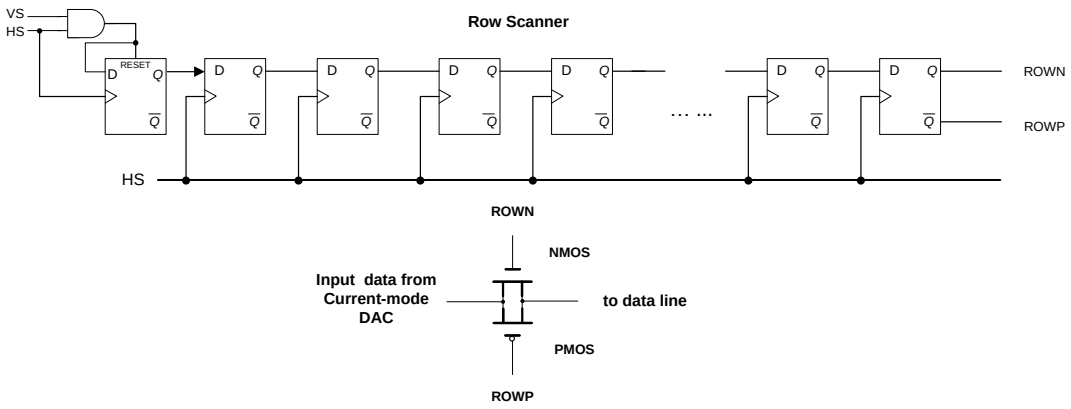


Figure 6.7 The row scanner of OLED-on-Silicon microdisplay prototype

As shown in Figure 6.7, due to the same consideration of the manufacture cost, only the 1st stage of the row scanner is testable. The expected output signals of the row scanner are shown in Figure 6.8. The ROWN signal has the period of one frame time and the pulse width of one line time.

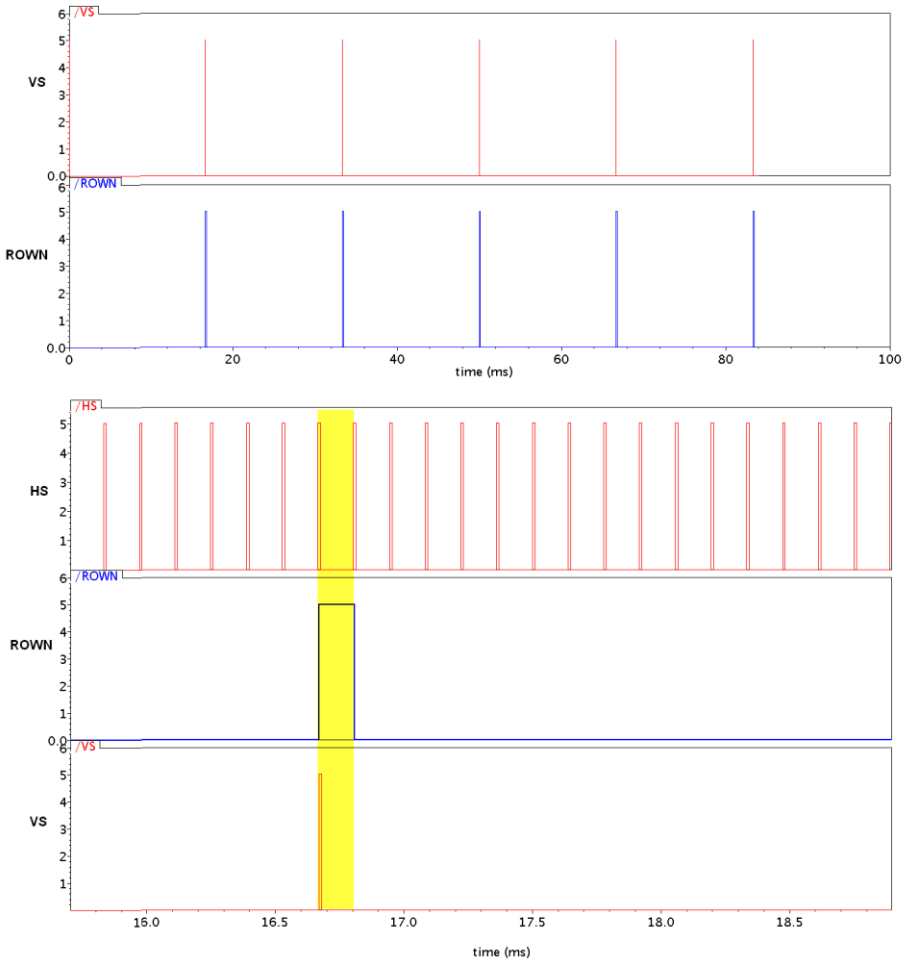


Figure 6.8 The expected output signals for the row scanner of OLED-on-Silicon microdisplay prototype

In summary, the signals specifications of OLED-on-Silicon microdisplay prototype testing are listed in Table 6.2

Table 6.2 Signals specifications for OLED-on-Silicon microdisplay prototype testing

Power Supply		
AVDD	Analog-VDD	+5V
AGND	Analog Ground	0V
DVDD	Digital-VDD	+5V
DGND	Digital-GND	0V
OLED Electrode	OLED Cathode	-5V
Input Signals		
pixelclk	Pixel Clock	$f_{pixelclk} = 1.152MHz$
HS	Horizontal Synchronization	$f_{HS} = 7.2KHz$
VS	Vertical Synchronization	$f_{VS} = 60Hz$
DATA<3:0>	4 bit Digital Input Data DATA<3>: MSB DATA<0>: LSB Logic “1” : 5V Logic “0” : 0V	$f_{DATA<3>} = f_{HS}/2$ $f_{DATA<2>} = f_{HS}$ $f_{DATA<1>} = 2f_{HS}$ $f_{DATA<0>} = 4f_{HS}$
I_{ref}	Reference Current for Current Mode DAC	$2.5\mu A$
I_{bias}	Bias Circuit of Current Mode DAC	$2.5\mu A$
Expected Output Signals		
S<3:0>	Outputs of Shift Register S<3> : MSB S<0> : LSB Logic “1” : 5V Logic “0” : 0V	$f_{s<3>} = f_{HS}/2$ $f_{s<2>} = f_{HS}$ $f_{s<1>} = 2f_{HS}$ $f_{s<0>} = 4f_{HS}$
DOUT<3:0>	Outputs of Data Latch DOUT<3>:MSB DOUT<0>:LSB Logic “1” : 5V Logic “0” : 0V	$f_{DOUT<3>} = f_{HS}/2$ $DOUT<2> = '1'$ $DOUT<1> = '1'$ $DOUT<0> = '1'$
ROWN	Test Pin of Row Scanner	$f_{ROWN} = f_{VS}$ $pulse\ width = 1/f_{HS}$
ROWP	Test pin of Row Scanner	Complement of ROWN

The input data signal DATA<3:0> and the output signal S<3:0> are shown in Figure 6.9.

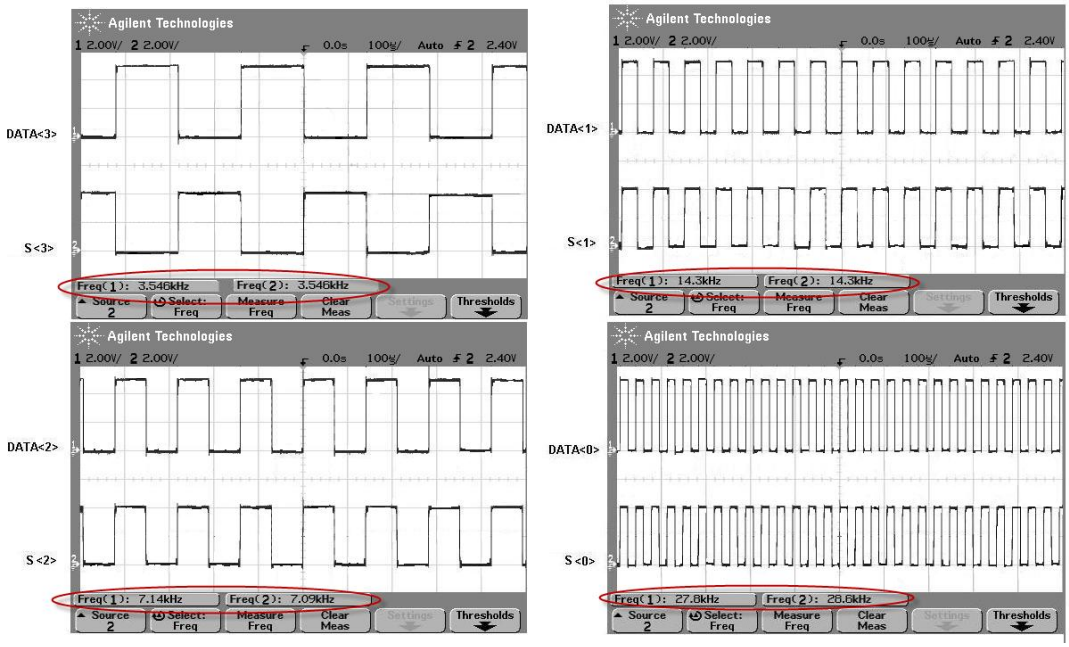


Figure 6.9 Measurement results of DATA<3:0> and S<3:0>

It will take a period of one line time for the data shifting from the beginning to the end of the shift register. From the waveform, we can notice the data shifting motion. S<3:0> first appear at the beginning of the second horizontal line of one frame of the display image. Due to distortion, the logic level of the output signal decreases a little but it still can to be identified as logic '1' for digital data process.

The waveforms of VS signal and the LSB S<0> of the 1st stage shift register are shown in Figure 6.10. It clearly illustrates the amount of time it takes to transfer the input data from the beginning to the end of the shift register when the image frame refresh cycle begins.

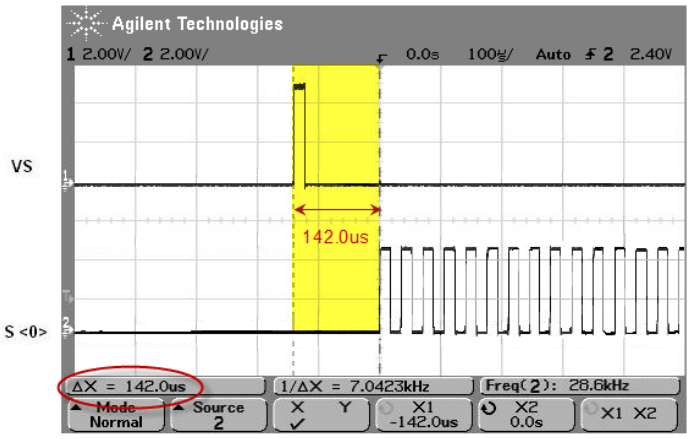


Figure 6.10 Measurement results of VS signal and S<0>

The waveforms of the HS signal and the DOUT<3:0>, the output of 1st stage data latch in the line, are shown in Figure 6.11. And only when the HS signal is valid, the exact data will be loaded into the data latch. In our design, DOUT<3:0> will switch between "1111" and "0111" clocked by HS as described in previous paragraphs.

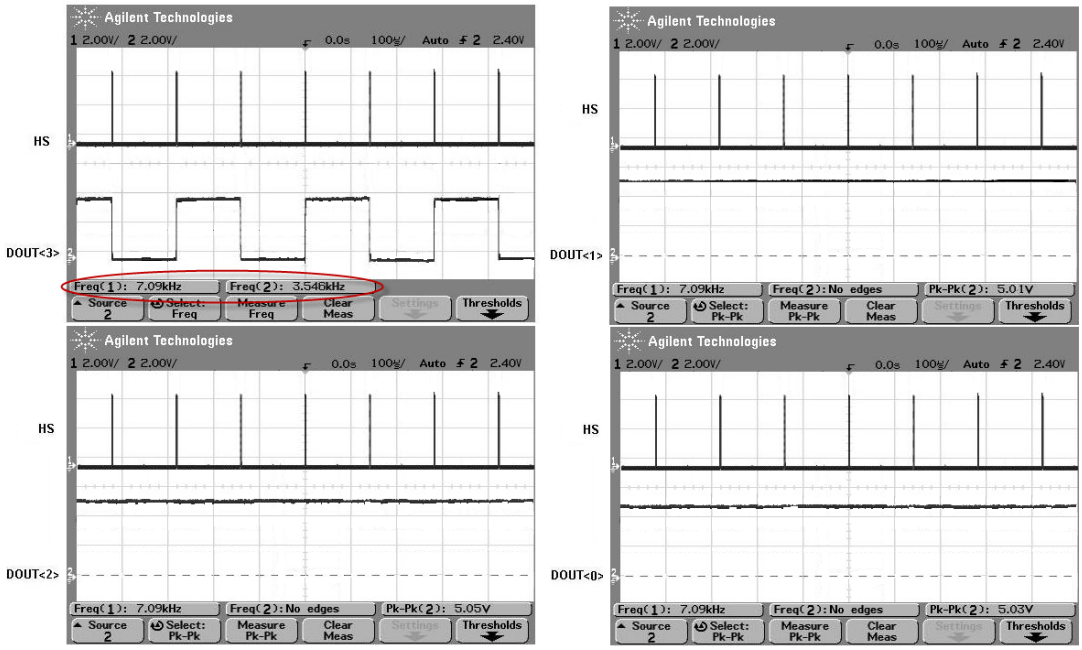


Figure 6.11 Measurement results of HS and DOUT<3:0>

The measurement results of the row scanner are shown in Figure 6.12. The row selection signal ROWN is clocked by the VS signal and the duration of the pulse of the ROWN signal sustains for a span of one horizontal line time.

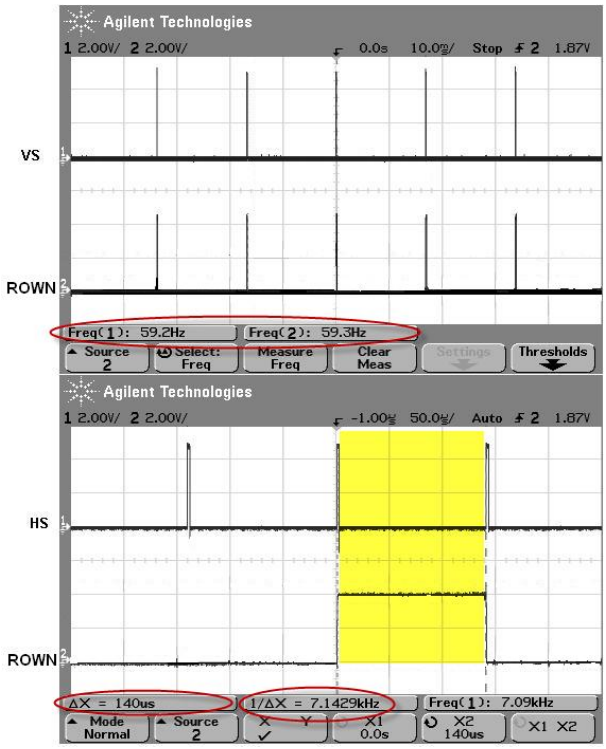


Figure 6.12 Measurement results of the row scanner

The probe station and the HP 4156 semiconductor parameter analyzer are used to measure the output current of the pixel circuit. With HP 4156, we can realize high accuracy performance evaluation and functionality analysis of semiconductor devices or integrated circuits, such as the digital parameter sweeping, pulse analysis, reliability testing, *etc*. Setup and measurement are achieved by programming the parameters from front-panel keys, keyboard, or GPIB interface. The measurement and analysis results are displayed on the color LCD of the front panel, and/or graphics will be stored in memories for comparison. The measurements which can be implemented by HP4156 are V-I test, C-V test, time domain test and so on. [80] The main features of HP4156 are listed in Table 6.3.

Table 6.3 Specifications of HP4156

Items	Description
Measurement Type	V-I, C-V, time domain, ultra low current *and so on*
Voltage Accuracy	1μV-200V
Current Accuracy	1fA-1A
Parameter Sweep Mode	DC mode, staircase mode and pulse mode
Parameter Program Mode	Front-panel keys, keyboard or GPIB
Data Output	Graphic on LCD monitor or data stored in internal memory

As the input digital data changes from ‘1111’ to ‘0000’, the output current also decreases. Shown in Figure 6.13, 16 different levels of output current result in 16 difference levels of gray scale for the OLED microdisplay.

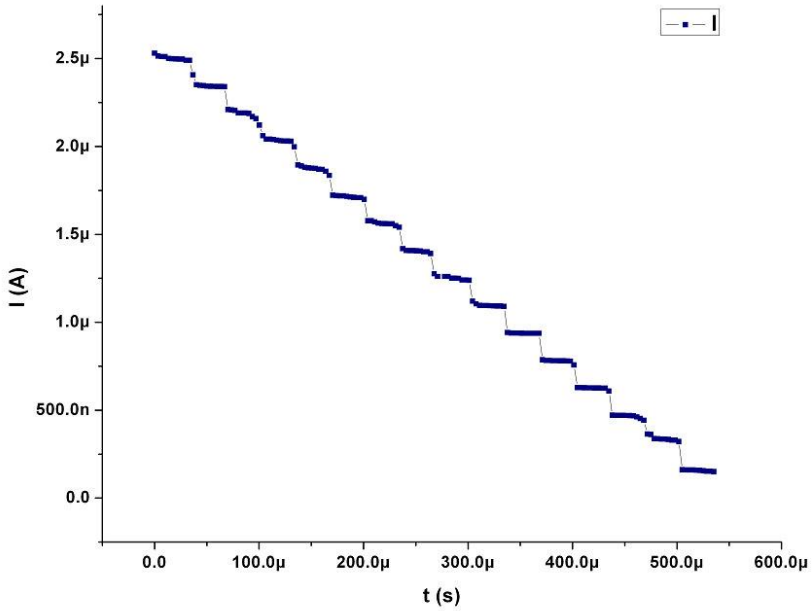


Figure 6.13 Measurement results of the pixel circuit output current

6.3 Conclusion

A prototype of the silicon backplane of a 160 × 120 OLED-on-silicon microdisplay is implemented using the SMIC 0.35μm process. The specifications of the prototype are listed in Table 6.4.

Table 6.4 Specifications of the OLED-on-Silicon microdisplay prototype

Technology	SMIC 0.35μm 3.3V/5.0V CMOS process
Die size	8mm × 6mm
Resolution	160 × 120
Pixel Size	50μm × 50μm
Driving Scheme	Current Driving
Frame Rate	60Hz (VGA video signals)
Pixel Clock Rate	1.152MHz
Gray Scale Levels	16 levels

The measurement results of the addressing circuit and the pixel circuit show that the yield targets of the design of the silicon backplane are fulfilled.

Chapter 7

Conclusions

7.1 Conclusions

In this research work, efficient silicon backplane circuit architecture for an OLED-on-Silicon microdisplay is developed and investigated.

1. We present the motivation and the objective of this research work. Two main contributions and the organization of the thesis are also introduced.

2. The basic operation of the OLEDs is introduced, especially the electrical characteristics of the OLEDs. Architectures of both the bottom emitting OLED and the top emitting OLED are presented. CMOS technology for microdisplay is studied. Comparisons of CMOS, amorphous silicon, and poly silicon technologies indicate that CMOS technology is more suitable for microdisplay applications. Features of an OLED-on-Silicon microdisplay introduce the design considerations of the silicon backplane design.

3. We focus on the electronic addressing technology for OLED-on-Silicon microdisplay. Active matrix addressing, rather than passive matrix addressing, is preferred due to its advantages of high resolution, low power consumption and almost no cross-talk for microdisplay application. The functional block diagram of silicon backplane circuit is introduced and the timing schedule of the addressing circuit is analyzed. From the analysis, it is found that the D flip-flop is the key element of the addressing circuit so the optimization of the D flip-flop greatly affects the performance of the addressing circuit. The static logic D flip-flop is

more practical for microdisplay application because it offers more stable working state than the dynamic logic D flip-flop. Comparison results evaluate the situation. Simulation results with an 8×8 block diagram show the input signal transmission and the timing signal synchronization within the addressing circuit. Measurement results further approve the addressing circuit can provide the correct display data and the synchronization signals for OLED-on-Silicon microdisplay.

4. To provide efficient driving current to OLEDs, the pixel circuit for a OLED-on-Silicon microdisplay must be carefully designed. We present the investigation and development of the pixel circuit in this thesis. Both a voltage driving scheme and a current driving scheme are reviewed. Since the luminance of OLED is proportion to its driving current, the current driving scheme is superior to the voltage driving scheme for the OLED-on-Silicon microdisplay. The pixel circuit of the current driving scheme is mainly based on the elemental current process circuits, like the current mirror. Input current display data is transferred to the OLED by the pixel circuit. The main challenge is to process the extremely small current used for the low grey scale display. Precious current process technology is employed in the pixel circuit design to solve the mismatch of input and output current caused by the switch charge feedthrough, clock feedthrough or leakage. In our proposed design, the compensation technology is adopted to compensate for the driving current and to provide the stable work state of the pixel circuit. The simulation results show that the input data current is precisely transferred to the OLEDs by the proposed pixel circuit.

5. Current driving scheme is employed in the pixel circuit design and the current mode input data is required. A 4-bit current mode DAC is implemented to covert

the digital input data to analog current data for the pixel circuit. With a carefully designed architecture, the chip area of the proposed current mode DAC is reduced compared with the binary-weighted current mode DAC, especially when the resolution becomes high. Since the chip area of circuitry for microdisplay application is limited, less chip area consumption is one of the most valuable features of the proposed DAC for the silicon backplane design of the OLED-on-Silicon microdisplay. At the same time, to achieve design goals of the current mode DAC, a bias circuit is implemented to guarantee the accurate working state of the transistors in the current mode DAC. A bias circuit using only MOS transistors also shows its attraction owning to the compact circuit architecture. The simulation results illustrate the good performance of the proposed current mode DAC.

6. A prototype of OLED-on-Silicon microdisplay with the resolution of 160 $\times$ 120 is introduced. The measurement results of the prototype show the design objectives are fulfilled with our design.

In summary, the design methodology of the silicon backplane is presented. Design of the main functional blocks is introduced in detail, like the addressing circuit, the current mode DAC and the pixel circuit. Simulation results and measurement results show the proposed prototype of the silicon backplane work properly as expected.

7.2 Recommendations for the Future Work

Based on the prototype of the OLED-on-Silicon, and the studies on the materials [81-87], several potential improvements are recommended for the future research work.

First, as described in previous chapters, for the current driving scheme, long programming time is noticed when the storage capacitor C_s is charged with an extremely small driving current for a low level gray scale display. Precharging the pixel circuit stands a chance to minimize programming time. By precharging the pixel circuit to the level for the lowest gray scale display, the speed of the pixel circuit is improved.

Secondly, a feedback method is applied to enable a stable working stare of the driving transistors in the proposed pixel circuit design. But discharge of the storage capacitors still can not be eliminated during the driving period that will cause the decay of the output driving current and the non-uniform lamination of OLEDs. A possible solution to solve this problem is to recharge the storage capacitor during the driving period. A sample and hold element is included in the pixel circuit assisting to memory the input display data for data refreshing. Based on those points above, the possible modification of the pixel circuit is shown in Figure 7.1.

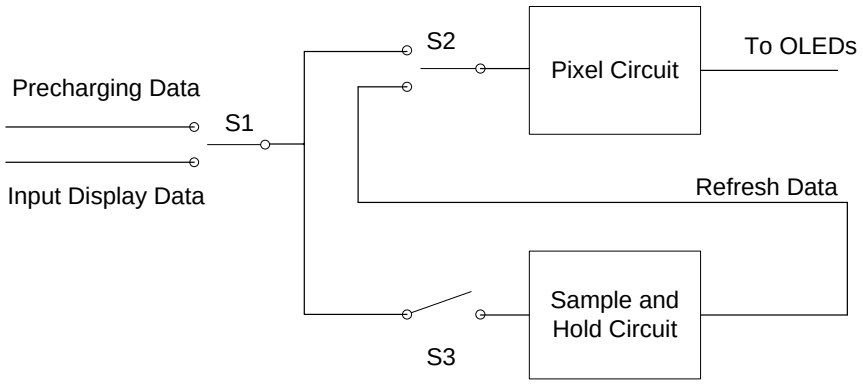


Figure 7.1 Possible modifications of the pixel circuit

But the challenge of the pixel circuit modification is the additional chip area cost. And the timing schedule of the different signal flows must be organized carefully to avoid the risk of the signal competition in one signal channel.

Third, although cascode current mirror pair is used in the DAC design to reduce the V_{ds} mismatch and increase the output impendence, the variations of the operating conditions can not be composited. The instability of reference current, the self-heating, the component aging and other potential causes will affect the performance of the current mode DAC. Self-calibration technology is one possible solution. The basic concept of self-calibration is to use accurate references to trim the circuit. The output of the DAC will be arranged in a designed range by the aid of a comparator. The diagram of the DACs with calibration is shown in Figure 7.2.

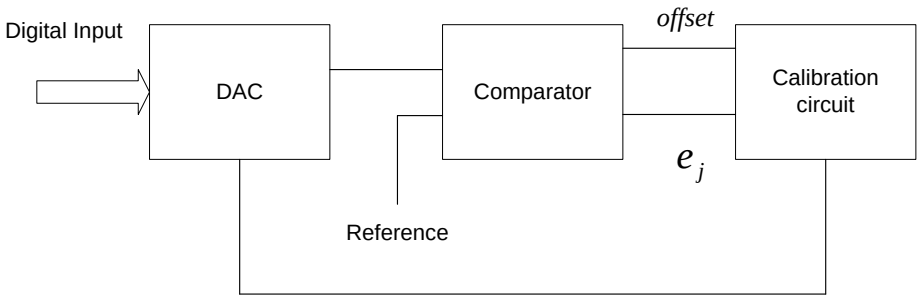


Figure 7.2 The DAC with calibration circuit

When all the inputs of DAC are set to be '0', the comparator measure the difference between the output of the DAC and the ideal reference, this value is the offset error of the DAC. This measured value will be used for calibration. And a tolerant error range will be defined within $[V_{\max}, V_{\min}]$. For the jth level of the output, the difference between the actual output and the ideal value is measured by the comparator and be marked as e_j. If e_j falls in the range $[V_{\max}, V_{\min}]$, no action will be taken in the calibration circuit. But if $e_j > V_{\max}$, the output of the DAC will decrease with the assisting of the calibration circuit. Similarly, when $e_j < V_{\min}$, the calibration results in the increase of the DAC output.

Furthermore, to provide a practical microdisplay product, the optical system setup is important. As described in the previous chapters, the OLED-on-Silicon microdisplay is an appropriate choice to build a near-to-eye display system. The optical design takes the challenges to provide good viewing contract and wide view angle. And an interface circuit is also necessary to enable the connection of the OLED-on-Silicon microdisplay to variable video inputs, like personal computers, TV sets and DVD players, *etc.*

Reference

[1] I. Underwood, "A review of microdisplay technologies," *Electronic Information Displays, London*, pp. 77-92, Nov 2000.

[2] I. U. David Armitage, Shin-Tson *Introduction to microdisplays* John Wiley and Sons, 2006.

[3] C. W. Tang and S. A. Vanslyke, "ORGANIC ELECTROLUMINESCENT DIODES," *Applied Physics Letters*, vol. 51, pp. 913-915, Sep 1987.

[4] B. Geffroy, P. Le Roy, and C. Prat, "Organic light-emitting diode (OLED) technology: materials, devices and display technologies," *Polymer International*, vol. 55, pp. 572-582, Jun 2006.

[5] J. Y. Park, "Progress of AMOLED technology," in *Light-Emitting Diode Materials and Devices*. vol. 5632, G. Yu, C. T. Chen, and C. H. Lee, Eds. Bellingham: Spie-Int Soc Optical Engineering, pp. 17-24,2005.

[6] J. N. Bardsley, "International OLED technology roadmap," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 10, pp. 3-9, 2004.

[7] G. Gu and S. R. Forrest, "Design of flat-panel displays based on organic light-emitting devices," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 4, pp. 83-99, 1998.

[8] C. Ho-Kyoon, K. Hye-Dong, and K. Boris, "40.1: Invited Paper: AMOLED Technology for Mobile Displays," *SID Symposium Digest of Technical Papers*, vol. 37, pp. 1447-1450, 2006.

[9] M. Rui-Qing, H. Richard, R. Kamala, S. Jeff, U. Ken, H. Michael, and J. B. Julie, "Flexible active-matrix OLED displays: Challenges and progress," *Journal of the Society for Information Display*, vol. 16, pp. 169-175, 2008.

[10] G. P. Crawford, *Flexible flat panel displays*: John Wiley and Sons, 2005.

[11] S. M. Kelly, *Flat panel displays: advanced organic materials*: Royal Society of Chemistry, 2000.

[12] D. N. L. Jiun-Haw Lee, Shin-Tson Wu, *Introduction to Flat Panel Displays*: Wiley, 2008.

[13] Z. L. Achintya K. Bhowmik, Philip J. Bos, *Mobile Displays: Technology and Applications*: J. Wiley & Sons, 2008

[14] L. S. James and S. S. Eugene, "24.2 Direct View Active Matrix VGA OLED-on-Crystalline-Silicon Display," *SID Symposium Digest of Technical Papers*, vol. 32, pp. 376-379, 2001.

[15] W. E. Howard and O. F. Prache, "Microdisplays based upon organic light-emitting diodes," IBM Journal of Research and Development, vol. 45, pp. 115-127, 2001.

[16] G. W. Jones, "11.1: Invited Paper: Active Matrix OLED Microdisplay," *SID Symposium Digest of Technical Papers*, vol. 32, pp. 134-137, 2001.

[17] O. Prache, "Active matrix molecular OLED microdisplays," *Displays*, vol. 22, pp. 49-56, May 2001.

[18] O. Prache, "Full-color SVGA+ OLED-on-silicon microdisplay," *Journal of the Society for Information Display*, vol. 10, pp. 133-138, 2002.

[19] J. Kido, K. Hongawa, K. Nagai, and K. Okuyama, "CHARGE-TRANSPORT POLYMERS FOR ORGANIC ELECTROLUMINESCENT DEVICES," *Macromolecular Symposia*, vol. 84, pp. 81-90, Jul 1994.

[20] J. R. Sheats, H. Antoniadis, M. Hueschen, W. Leonard, J. Miller, R. Moon, D. Roitman, and A. Stocking, "Organic electroluminescent devices," *Science*, vol. 273, pp. 884-888, Aug 1996.

[21] D. Kalinowski, "Electroluminescence in organics," *Journal of Physics D-Applied Physics*, vol. 32, pp. R179-R249, Dec 1999.

[22] R. H. Friend, R. W. Gymer, A. B. Holmes, J. H. Burroughes, R. N. Marks, C. Taliani, D. D. C. Bradley, D. A. Dos Santos, J. L. Bredas, M. Logdlund, and W. R. Salaneck, "Electroluminescence in conjugated polymers," *Nature*, vol. 397, pp. 121-128, Jan 1999.

[23] H. S. N. Seizō Miyata, *Organic electroluminescent materials and devices*: CRC Press, 1997.

[24] J. Shinar, *Organic light-emitting devices: a survey*: Springer, 2004.

[25] U. S. Klaus Müllen, *Organic light-emitting devices: Synthesis, properties, and applications*: John Wiley and Sons, 2006.

[26] W. Brütting, *Physics of organic semiconductors*: Wiley-VCH, 2008.

[27] L. Jiin-Jou, S. Chih-Feng, L. Chun-Huai, H. Tiao-Hung, and L. Hsin-Hung, "Comparison of a-Si and Poly-Si for AMOLED displays," *Journal of the Society for Information Display*, vol. 12, pp. 367-371, 2004.

[28] T. H. N. Yuan Taur, *Fundamentals of Modern VLSI Devices*: Cambridge University Press, 1998.

[29] D. Pribat and F. Plais, "Matrix addressing for organic electroluminescent displays," *Thin Solid Films*, vol. 383, pp. 25-30, Feb 2001.

[30] D. Pribat and F. Plais, "Addressing of organic electroluminescent displays," in *Polycrystalline Semiconductors Iv Materials, Technologies and Large Area Electronics*. vol. 80-81, O. Bonnaud, T. MohammedBrahim, H. P. Strunk, and J. H. Werner, Eds. Zurich-Uetikon: Trans Tech Publications Ltd, pp. 385-390,2001.

[31] A. Nathan, D. Striakhilev, R. Chaji, S. Ashtiani, C. H. Lee, A. Sazonov, J. Robertson, and W. Milne, "Backplane requirements for active matrix organic light emitting diode displays," in *Amorphous and Polycrystalline Thin-Film Silicon Science and Technology 2006*. vol. 910, S. Wagner, V. Chu, H. A. Atwater, K. Yamamoto, and H. W. Zan, Eds. Warrendale: Materials Research Society, pp. 373-387, 2007.

[32] M.-h. Xu, Q. Zhang, F. Ran, and L.-z. Wang, "Study and AISC design of a high efficiency OLED scan controller," in *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on*, pp. 2156-2159，2008.

[33] W. Ihor and P. Olivier, "41.3: A Low-Power AMOLED Microdisplay with Ultra-High Pixel Density and Extended Operating Temperature Range," *SID Symposium Digest of Technical Papers,* vol. 38, pp. 1374-1377, 2007.

[34] G. B. Levy, W. Evans, J. Ebner, P. Farrell, M. Hufford, B. H. Allison, D. Wheeler, L. Haiqing, O. Prache, and E. Naviasky, "An 852×600 pixel OLED-on-silicon color microdisplay using CMOS subthreshold-voltage-scaling current drivers," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 1879-1889, 2002

[35] Y. L. Sung-Mo Kang, *CMOS digital integrated circuits: analysis and design*: McGraw-Hill Professional, 2003.

[36] R. J. Baker, *CMOS: mixed-signal circuit design*: Wiley, 2002.

[37] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Second Edition* Wiley-IEEE Press, 2004.

[38] J. S. Christopher Saint, *IC mask design: essential layout techniques*: McGraw-Hill Professional, 2002.

[39] H. E. Weste, David F. Harris, *CMOS VLSI design: a circuits and systems perspective,* Pearson-Addison-Wesley, 2005.

[40] “Virtuoso Spectre Circuit Simulator User Guide”, Cadence, June, 2008

[41] L. S. James and R. L. Frank, "4.2: TFT AMOLED Pixel Circuits and Driving Methods," *SID Symposium Digest of Technical Papers,* vol. 34, pp. 10-13, 2003.

[42] A. Kumar, K. Sakariya, P. Servati, S. Alexander, D. Striakhilev, K. S. Karim, A. Nathan, M. Hack, E. Williams, and G. E. Jabbour, "Design considerations for

active matrix organic light emitting diode arrays," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 150, pp. 322-8, 2003.

[43] K. Sakariya, P. Servati, and A. Nathan, "Stability analysis of current programmed a-Si:H AMOLED pixel circuits," *Electron Devices, IEEE Transactions on*, vol. 51, pp. 2019-2025, 2004.

[44] A. Nathan, G. R. Chaji, and S. J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," *Display Technology, Journal of*, vol. 1, pp. 267-277, 2005.

[45] S. Alexander, P. Servati, G. R. Chaji, S. Ashtiani, R. Huang, D. Striakhilev, K. Sakariya, A. Kumar, A. Nathan, C. Church, J. Wzorek, and P. Arsenault, "Pixel circuits and drive schemes for glass and elastic AMOLED displays," *Journal of the Society for Information Display*, vol. 13, pp. 587-595, 2005.

[46] R. M. A. Dawson and M. G. Kane, "24.1: Invited Paper: Pursuit of Active Matrix Organic Light Emitting Diode Displays," *SID Symposium Digest of Technical Papers*, vol. 32, pp. 372-375, 2001.

[47] G. Joon-Chul, C. Hoon-Ju, J. Jin, and H. Chul-Hi, "A new pixel circuit for active matrix organic light emitting diodes," *Electron Device Letters, IEEE*, vol. 23, pp. 544-546, 2002.

[48] D. Yoshito, O. Tetsuro, N. Fumihisa, T. Hitoshi, Y. Atsuhiro, and T. Hiroshi, "36.5L: Late-News Paper: Development of Source Driver LSI for AMOLED Displays Using Current Driving Method," *SID Symposium Digest of Technical Papers*, vol. 34, pp. 1138-1141, 2003.

[49] L. Jae-Hoon, N. Woo-Jin, J. Sang-Hoon, and H. Min-Koo, "A new current scaling pixel circuit for AMOLED," *Electron Device Letters, IEEE,* vol. 25, pp. 280-282, 2004.

[50] L. S. James and R. L. Frank, "Vt Compensated voltage-data a-Si TFT AMOLED pixel circuits," *Journal of the Society for Information Display,* vol. 12, pp. 65-73, 2004.

[51] A. Kumar, A. Nathan, and G. E. Jabbour, "Does TFT mobility impact pixel size in AMOLED backplanes? ," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 2386-2394, 2005.

[52] S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan, "A 3-TFT current-programmed pixel circuit for AMOLEDs," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 1514-1518, 2005.

[53] S. J. Ashtiani and A. Nathan, "A driving scheme for active-matrix organic light-emitting diode displays based on feedback," *Display Technology, Journal of,* vol. 2, pp. 258-264, 2006.

[54] S. J. Ashtiani and A. Nathan, "A Driving Scheme for AMOLED Displays Based on Current Feedback," in *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE,* pp. 289-292, 2006.

[55] L. Geon-Ho, K. Sang-Kyung, S. Young-Suk, J. Jin-Yong, J. Yong-Joon, and C. Gyu-Hyeong, "P-45: A Fast Driving Circuit for AMOLED Displays Using Current Feedback," *SID Symposium Digest of Technical Papers,* vol. 37, pp. 363-365, 2006.

[56] F. H. Wang, H. C. Lin, P. S. Shin, L. Y. Lin, and H. W. Liu, "New Current Programmed Pixel Circuit for Active-Matrix Organic Light-Emitting-Diode Displays," in *Electron Devices and Solid-State Circuits, 2007. EDSSC 2007. IEEE Conference on*, pp. 1151-1154, 2007

[57] C. L. Lin and Y. C. Chen, "A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OLED Degradation for AMOLED," *Electron Device Letters, IEEE,* vol. 28, pp. 129-131, 2007.

[58] L. Chih-Lung, T. Tsung-Ting, and C. Yung-Chih, "A Novel Voltage-Feedback Pixel Circuit for AMOLED Displays," *Display Technology, Journal of,* vol. 4, pp. 54-60, 2008.

[59] S. J. Daubert and D. Vallancourt, "Operation and analysis of current copier circuits," *Circuits, Devices and Systems, IEE Proceedings G,* vol. 137, pp. 109-115, 1990.

[60] G. Wegmann and E. A. Vittoz, "Basic principles of accurate dynamic current mirrors," *Circuits, Devices and Systems, IEE Proceedings G,* vol. 137, pp. 95-100, 1990.

[61] F. J. L. C. Toumazou, David Haigh, *Analogue IC design: the current-mode approach*: IET, 1993.

[62] K. L. Fong, "Techniques for improving the performance of current-mode circuits." vol. M.A.Sc.: University of Toronto 1993.

[63] N. S. Daoud, "Novel CMOS current mirrors design and their applications." vol. M.A.Sc.: Concordia University (Canada),1993.

[64] M. Ehsanian-Mofrad, "Design and test of high-performance analog-to-digital converter based on subranging architecture." vol. Ph.D: Ecole Polytechnique, Montreal (Canada), 1998.

[65] K. W. M. David Johns, *Analog integrated circuit design*: John Wiley & Sons, 1997.

[66] R. A. Hastings, *The art of analog layout*: Pearson Prentice Hall, 2006.

[67] R. J. v. d. Plassche, *CMOS integrated analog-to-digital and digital-to-analog converters*: Springer, 2003.

[68] H. Chun-Yueh, H. Tsung-Tien, and W. Hung-Yu, "A 12-bit 250-MHz current-steering DAC," in *ASIC, 2005. ASICON 2005. 6th International Conference On*, pp. 411-414, 2005.

[69] Y. Ling, N. Weining, S. Yin, and F. F. Dai, "A 10-bit 2GHz Current-Steering CMOS D/A Converter," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pp. 737-740, 2007.

[70] C. Yunyoung and M. Franco, "Current steering high-speed DAC: architecture analysis and simulation results," in *Low Power/Low Voltage Mixed-Signal Circuits and Systems, 2001. (DCAS-01). Proceedings of the IEEE 2nd Dallas CAS Workshop on*, pp. P27-P30, 2007.

[71] L. Fang-Jie, Y. Yong-Sheng, L. Shang-Quan, and G. Ming-Lun, "Current switch driver and current source designs for high-speed current-steering DAC," in *Anti-counterfeiting, Security and Identification, 2008. ASID 2008. 2nd International Conference on*, pp. 364-367, 2008.

[72] H. Chun-Yueh, H. Tsung-Tien, C. Chi-Chieh, and W. Hung-Yu, "Design of 12-bit 100-MHz current-steering DAC for SOC applications," in *System-on-Chip for Real-Time Applications, 2005. Proceedings. Fifth International Workshop on*, pp. 117-122, 2005.

[73] R. Ki-Hong, Y. Kwang Sub, and M. Hong Ki, "Design of a 3.3 V 12 bit CMOS D/A converter with a high linearity," in *Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on*, pp. 538-541, 1998.

[74] W. Chen, J. Bauwelinck, P. Ossieur, X. Z. Qiu, and J. Vandewege, "A Digitally Controlled On-chip Monotonic Reference Current Generator With Low LSB Current For Fast And Accurate Optical Level Monitoring," in *Mixed Design of Integrated Circuits and System, 2006. MIXDES 2006. Proceedings of the International Conference*, pp. 192-197, 2006.

[75] J.-S. Wang, "Design of high-performance and low-power CMOS switched-current data converters." vol. Ph.D: Michigan: Michigan State University, 1998.

[76] D. Seo, "1-GS/s, 14-bit digital-to-analog converter and track-and-hold amplifier.." vol. Ph.D: University of Illinois at Urbana-Champaign, 2000.

[77] Y. Cong, "Design techniques for high-performance current-steering digital-to-analog converters." vol. Ph.D: Iowa State University, 2002.

[78] A. Sepehr, "10-bit double-segemented thermometer-coded current-steering DAC." vol. M.A.Sc: Ryerson University, 2003.

[79] DG2020A data generator with P3410 & P3420 Pods user manual, Sony & Tektronix Inc., 2004

[80] Semiconductor Parameter Analyzer HP 4155B/4156B User's Guide: General Information, Hewlett Packard Inc., 1997

[81] L. Mao-Feng, A. Tammineedi, and R. Geiger, "A new current mirror layout technique for improved matching characteristics," in *Circuits and Systems, 1999. 42nd Midwest Symposium on*, 1999, pp. 1126-1129 vol. 2.

[82] C. Yonghua and R. L. Geiger, "A 1.5-V 14-bit 100-MS/s self-calibrated DAC," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 2051-2060, 2003.

[83] H. Hristov, "A low-complexity calibration algorithm for current steering DACs," in *Electronics Technology: Meeting the Challenges of Electronics Technology Progress, 2004. 27th International Spring Seminar on*, vol.1, pp. 162-166, 2004.

[84] G. I. Radulov, P. J. Quinn, H. Hegt, and A. van Roermund, "An on-chip self-calibration method for current mismatch in D/A converters," in *Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European*, pp. 169-172, 2005.

[85] Z. Guangbin, S. Sooping, L. Jin, S. Sterrantino, D. K. Johnson, and J. Sungyong, "An accurate current source with on-chip self-calibration circuits for low-voltage current-mode differential drivers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, pp. 40-47, 2006.

[86] A. R. Chen, A. I. Akinwande, and L. Hae-Seung, "CMOS-based microdisplay with calibrated backplane," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2746-2755, 2005.

[87] H. B. Gabbouj, N. Hassen, and K. Besbes, "Low supply voltage high speed CMOS current mirror for analog design," in *Microelectronics, 2007. ICM 2007. International Conference on*, pp. 369-372, 2007.

Publications

Y. Wang, X. W. Sun, "Silicon Backplane Design for OLED-on-silicon microdisplay" The First International Conference on Science and Engineering (ICSE), Dec. 2009.

Y. Wang, X. W. Sun, "A Field Sequential Color LCoS microdisplay" ASID07, August. 2007.

W. Piecek, Z. Raszewski, P. Perkowski, P. Morawiak, G. Pajchrowski, and *Y. Wang*, "Transient Light Scattering Mode of an Orthoconic Antiferroelectric Liquid Crystal," *Molecular Crystals and Liquid Crystals*, vol. 507, pp. 150-160, 2009.

Accepted publications

Y. Wang, X. W. Sun, "Design for OLED Microdisplay" PrimeAsia2010, September 2010.

Appendix

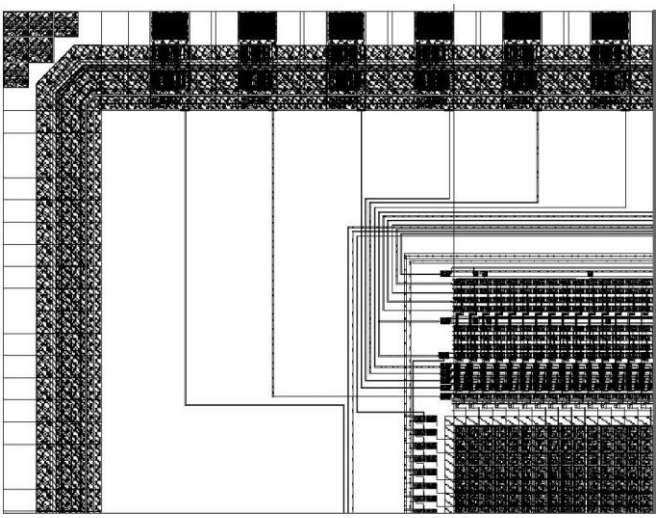


Figure 1. The top left corner of the layout for the OLED-on-Silicon microdisplay

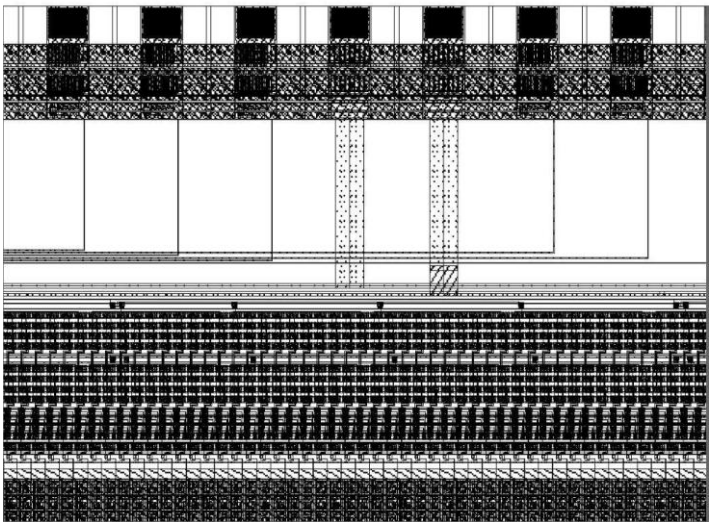


Figure 2 The top middle part of the layout for the OLED-on-Silicon microdisplay

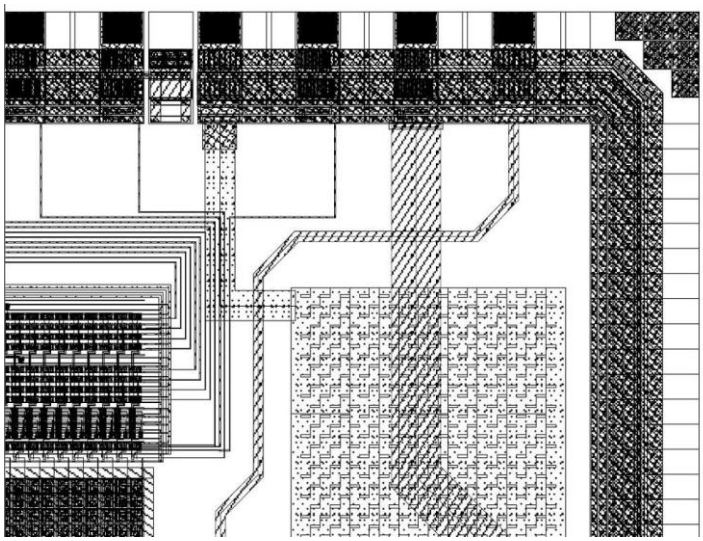


Figure 3 The top right corner of the layout for the OLED-on-Silicon microdisplay

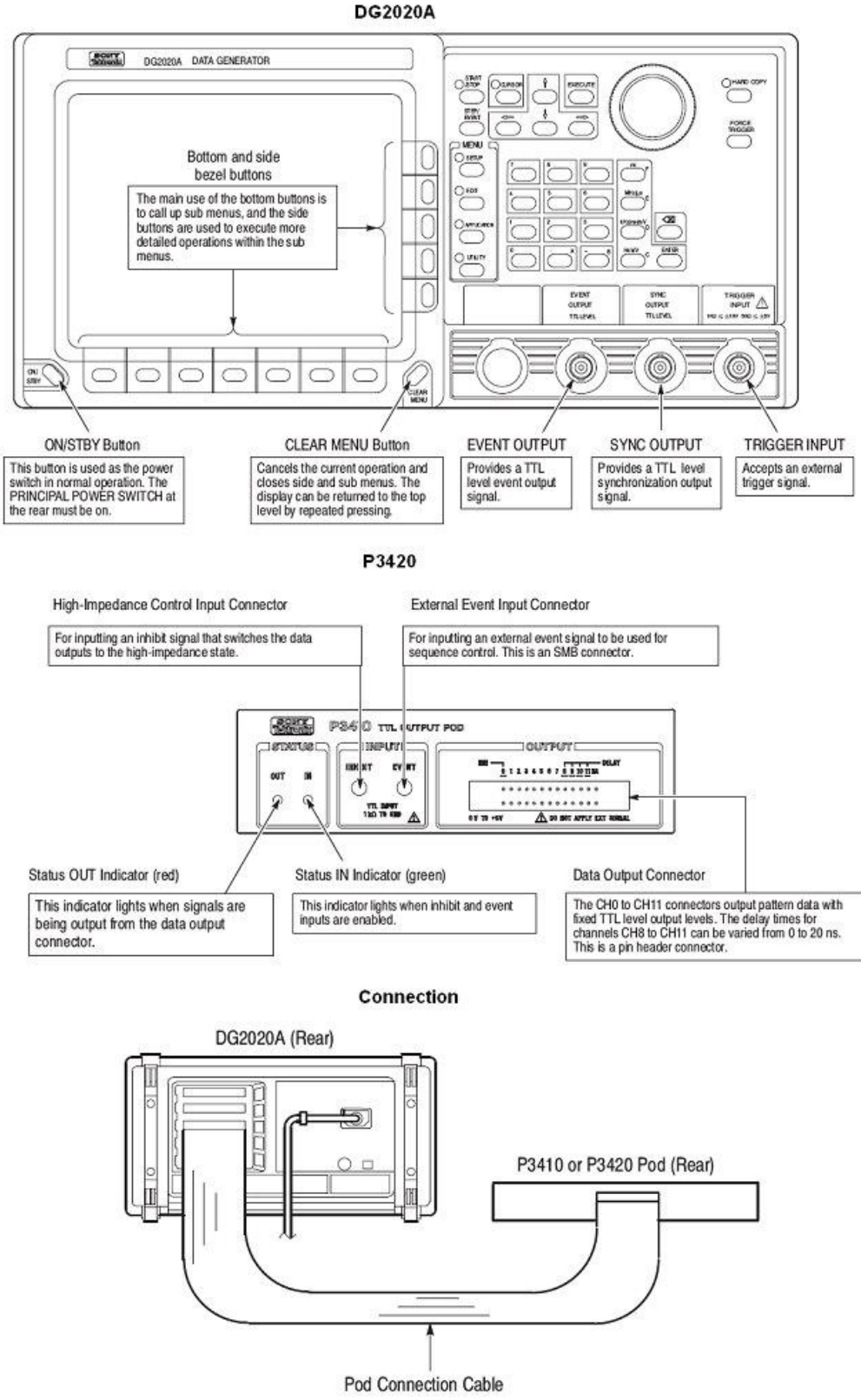


Figure 4 The DG2020A with P3420

1) Power Button
2) Display
3) 3.5' Disk Driver
4) Soft Keys
5) Channel Menu Button
6) Measurement Menu Button
7) Display Menu Button
8) Graph/List Menu Button
9) System Menu Button
10) Thumbwheel
11) Cursor Movement and Field Selection Buttons
12) The Signal Button
13) The Repeat Button
14) The Stop Button
15) The Append Button
16) Text/Number Entry Keys

Figure 5 The HP4156

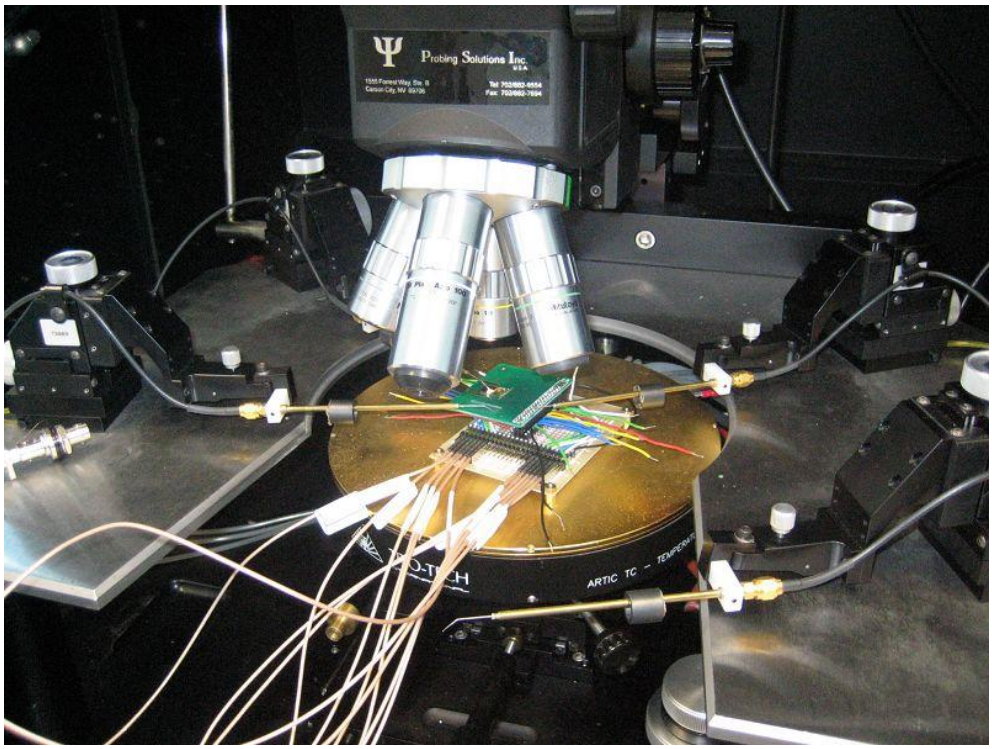


Figure 6 The prototype under testing

Figure 7 The measurement setup