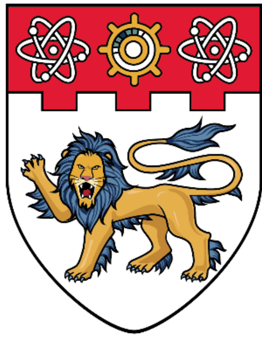

NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

DESIGN, FABRICATION, AND CHARACTERIZATION OF THREE-DIMENSIONAL EMBEDDED CAPACITOR IN THROUGH-SILICON VIA

LIN YE

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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(On the Spine) DESIGN, FABRICATION, AND CHARACTERIZATION OF 3-D EMBEDDED CAPACITOR IN TSV LIN YE 2019

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LIN YE

(B. Eng., Nanyang Technological University)

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

A thesis submitted to the Nanyang Technological University in partial fulfillment of the requirement for the degree of Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

28 May 2019

Date

Tan Chuan Seng

Authorship Attribution Statement

This thesis contains material from 6 papers published in the following peer-reviewed journals and from papers accepted at conferences in which I am listed as an author.

Chapter 3-5 are published in the following papers:

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- Assoc Prof Tan Chuan Seng provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I performed all the design, modeling, fabrication, and characterization of 3-D embedded capacitors.

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Date

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Executive Summary

In this thesis, a novel integrated capacitor, called "three-dimensional (3-D) embedded capacitor" is proposed, designed, fabricated, and characterized for application in integrated circuits (ICs) with through-silicon vias (TSVs). A significant capacitance density enhancement can be achieved for this 3-D embedded capacitor, because it leverages on the existing TSVs. Compared to conventional trench capacitor, this technology does not consume much additional silicon area because it is embedded in the trenches of TSVs, instead of in the dedicated trenches.

Firstly, two types of 3-D embedded capacitors are designed with different electrode deposition methods. The atomic layer deposition (ALD) type 3-D embedded capacitor features an extremely high capacitance density for high-end applications, whereas the sputtering type 3-D embedded capacitor features a higher electrode deposition rate and ease of integration for low-cost applications. Secondly, an electrical model of the 3-D embedded capacitor is constructed with analytical equations to predict its capacitance based on the physical design parameters. An ultra-high capacitance density, 5,621.8 nF/mm^2, can be envisioned for the 3-D embedded capacitor in the trench of a TSV with a diameter of 50 μm and a depth of 30 μm. In addition, a finite element simulation is performed to ensure the structural integrity of the 3-D embedded capacitor and its surrounding components. The simulation result shows that the maximum thermo-mechanical stress changes only slightly from 1567.8 to 1576.8 MPa when a 3-D embedded capacitor is included.

Next, prototypes of 3-D embedded capacitors are fabricated successfully with an optimized process flow design and implementation. Six types of test vehicles are included in each unit cell repeated over the entire wafer: (1) the de-embedded ALD type, (2) the embedded rough-ALD type, (3) the embedded smooth-ALD type, (4) the de-embedded sputtering type, (5) the embedded rough-sputtering type, and (6) the embedded smooth-sputtering type. Among them, the de-embedded test vehicles are just planar parallel capacitors without 3-D embedded capacitors for the purpose of

benchmarking. After the fabrication, cross-sectional scanning electron microscope (SEM), transmission electron microscopy (TEM), and energy-dispersive X-ray spectroscopy (EDX) are performed on both ALD type and sputtering type test vehicles. The SEM and TEM pictures show ~100% step coverage of ~50 nm TiN and ~10 nm Al_2O_3 layers for ALD type test vehicles but poor step coverage of TiN layer for sputtering type test vehicles (the thickness drops from 400 nm on the top surface to 200 nm on the top part of the sidewall). The EDX line-scans across the stacked layers provide semi-quantitative proof of correct stoichiometries of TiN/Al_2O_3/TiN/SiO_2/Si layers.

Lastly, capacitance-voltage (*C*-*V*) and current-voltage (*I*-*V*) characterizations are performed to evaluate the electrical performance of the test vehicles of 3-D embedded capacitors. The *C*-*V* characterization results show that, as the trench diameter increases from 10 to 50 μm, the capacitance increases from 98.7 to 625.2 pF for ALD type 3-D embedded capacitors. It also increases from 3.6 to 138.7 pF for sputtering type 3-D embedded capacitors. As a result, the capacitance density can reach up to 3856.4 nF/mm^2 for fabricated porotypes in this study. These measurement results of the ALD type test vehicles are found to be in good agreement with the corresponding electrical modelling results, which are calculated based on the analytical equations derived early in the study. However, this is not the case for the sputtering test vehicles. The difference is due to the super conformal step coverage of electrodes provided by ALD and the poor step coverage of electrodes provided by sputtering. Furthermore, the results of the other set of *C*-*V* characterizations show that the dielectric composition and the total amount of trapped charges in the dielectric layer tend to be instable when the sidewall roughness increases from 30 nm to 290 nm. From the *I*-*V* characterization results, it can be observed that the leakage currents of the ALD type embedded test vehicles do not deviate from those of their planar capacitor counterparts, but the leakage currents of the sputtering type embedded test vehicles degrade from the leakage currents of their planar capacitor counterparts. The suspected cause is the rough trench sidewall due to sputtering deposition method. Then, the *I*-*V* characterization results are normalized to the current density (*J*-*E*) plots, showing that the leakage current density is ~2×10^{-7} A/cm^2 at 2

MV/cm and the dielectric strength is ~9.7 MV/cm for the ALD type test vehicles; whereas the leakage current density is ~3×10^{-9} A/cm^2 at 2 MV/cm and the dielectric strength is ~8.0 MV/cm for the sputtering type test vehicles. Based on the *J*-*E* plots, leakage current conduction mechanisms have been identified for all test vehicles. The Schottky emission, FN tunneling, PF emission, and hopping conduction can be fitted for the ALD type test vehicles; whereas FN tunneling, and PF emission can be fitted for the sputtering type test vehicles.

This technology is promising in integration of ultrahigh-density on-chip capacitor. The above merits will pave the way for on-chip energy storage element, integrated voltage regulator, capacitively coupled wireless module and many other possibilities.

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Chapter 1 Introduction

1.1 Background

The first solid-state device was invented by Bardeen, Brattain, and Shockley in 1947 [1]. Soon Gordon E. Moore in 1965 observed the exponential growth of integrated devices in quantity and made an empirical prediction [2]. According to Moore's law, the number of transistors on a chip is expected to double after every 18 months. Although this prediction is not made based on any physical law, the semiconductor industry has invested great effort into keeping up with it over the past 50 years. The benefits of device scaling are two-fold. Firstly, the shrinking size make it possible to cram more devices into the same-sized chip. Secondly, due to the shorter channel length, a transistor is able to switch faster as well.

In 2000, silicon metal–oxide–semiconductor field-effect transistors (Si MOSFETs) reached a technology node below 100 nm. More recently, they have reached sub 10 nanometers and are approaching their physical limitation. The Intel development roadmap shows this trend in Figure 1.1 [3]. Both technical and economic challenges are slowing down the development of integrated circuits.

Figure 1.1: Intel follows Moore's law as an industrial leader [3].

To tackle this issue, researchers are actively looking for alternative solutions to future IC development. In addition to "More Moore" miniaturization, another research path has been proposed to extend the diversification of devices, called "More than Moore" [4]–[10]. The aim of "More than Moore" is to apply the well-developed silicon process technology to many diversified emerging applications (including but not limited to passive device integration technologies, radio frequency (RF) technologies, optical technologies, and sensing technologies). Furthermore, high value electronics systems can be enabled when the two approaches, "More Moore" miniaturization and "More than Moore" diversification, are combined.

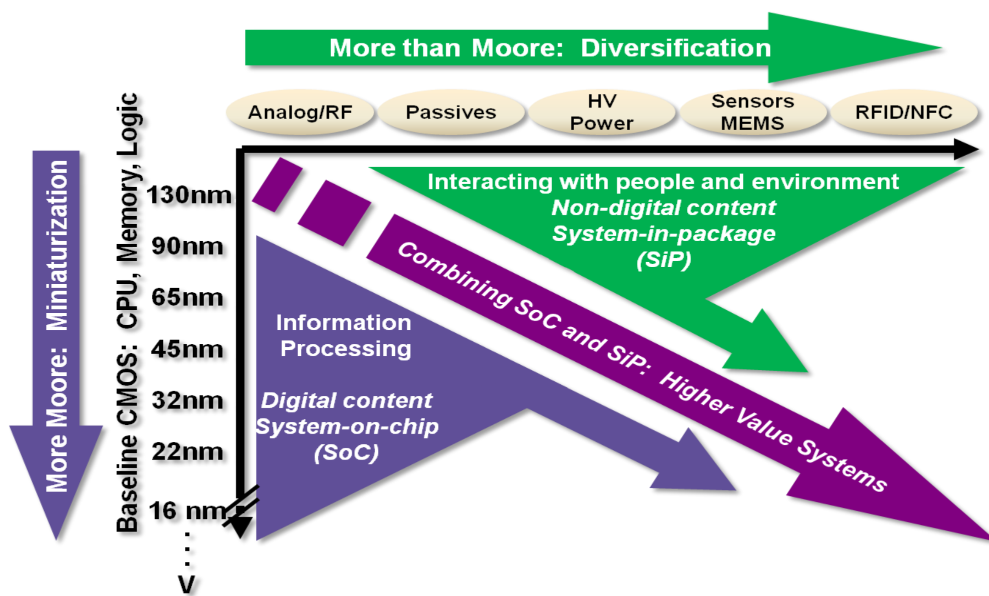
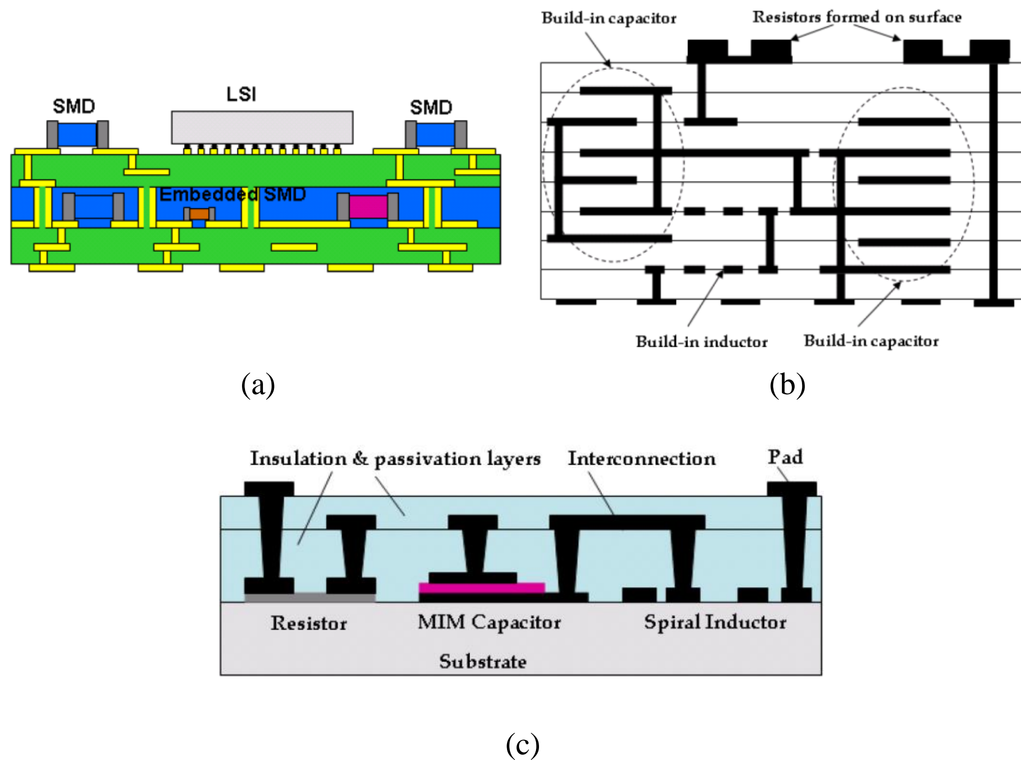


Figure 1.2: The chip industry treadmill involves tackling a constant series of challenges. Intel has maintained the ability to predict what will happen for about the next decade [11].

1.2 Motivation for the Development of Thin Film-Based Passive Integration Technology

The fast bloom of electronic gadgets owns credits to Moore's law, which has been a guideline in the semiconductor industry for the past few decades [12]–[14]. Researchers and engineers are endeavoring to scale down the size of transistors so that chips can be more powerful with a smaller form factor. However, passive devices (e.g., resistor, capacitor, inductor) are still considered bulky in size, not being well scaled compared with transistors. In fact, it is very difficult to scale down passive devices, because they need a large surface area to achieve their target component value.

Instead of scaling, a more realistic solution is to integrate passive devices in a more compact way. Currently, there are three major integration technologies of passive devices available to tackle this issue: (1) laminate-based passive integration technology, (2) low temperature co-fired ceramic (LTCC)-based passive integration technology, and (3) thin film-based passive integration technology [15]. For laminate-based passive integration technology, discrete passive devices (e.g., surface-mounted devices) are embedded in multilayer organic substrates as shown in Figure 1.3(a) [16]–[18]. For LTCC-based passive integration technology, passive devices are printed on LTCC tapes with adhesives, laminated together with other layers, and co-fired at around 850 to 900°C as shown in Figure 1.3(b) [19]–[21]. For thin film-based passive integration technology, passive devices are built onto the surfaces of substrates using standard IC fabrication processes as shown in Figure 1.3(c) [22]–[24].



(a) (b)

(c)

Figure 1.3: The schematics of the three major integration technologies of passive devices: (a) laminate-based passive integration technology, (b) LTCC-based passive integration technology, and (c) thin film-based passive integration technology [15].

Among these three integration methods, the thin film-based passive integration method is considered the most promising technology due to its unparalleled advantages over the first two methods: high precision, high quality factor, high self-resonant frequency, high density, and small size. These features are possible because of the IC fabrication processes used for film-based passive integration technology, which enable the best dimensional accuracy for patterns and thickness of layers down to the nanometer range. Moreover, the only drawback is its high cost, which will be gradually mitigated as the wafer size increases from 8 to 12 inches or even beyond 18 inches. Therefore, it is worth exploring the further development of thin film-based passive integration technology to meet the higher demand for integrated passive devices, as more electronic devices are being crammed into an IC package.

1.3 Objectives

Given the demand for integrared passives, this thesis aims to study a new type of integrated capacitor for 3-D ICs called a "3-D embedded capacitor." The detailed objectives are to:

- Design the structure of a 3-D embedded capacitor and achieve a capacitance density up to 5,000 nF/mm^2, which is 10× higher than that of conventional trench capacitors. Build an electrical model with analytical equations for a 3-D embedded capacitor so that its capacitance value can be predicted according to physical design parameters. Run finite element simulations for a 3-D embedded capacitor to ensure the structural integrity of each component under thermo-mechanical stress.
- Propose a process flow, optimize process parameters, and fabricate various types of test vehicles for a 3-D embedded capacitor. Apply physical characterization methods on the test vehicles to measure their geometries and chemical components.
- Evaluate the electrical performance of 3-D embedded capacitor by characterizing its capacitance, leakage current and breakdown voltage. Calculate the capacitance density, extract the voltage coefficients of capacitance, and investigate the leakage current conduction mechanisms based on the characterization results above.

1.4 Major Contribution of the Thesis

A comprehensive study on a 3-D embedded capacitor has been carried out in this thesis. Firstly, the structure of a 3-D embedded capacitor has been proposed and designed to realize significant capacitance density enhancement by leverage on the existing TSV trenches. Two types of 3-D embedded capacitor have been suggested based on their electrode deposition methods for different end-applications. The ALD type 3-D embedded capacitor features an extremely high capacitance density, whereas the sputtering type 3-D embedded capacitor features a low cost and ease of integration. Secondly, analytical modelling has been constructed to predict the capacitance of the 3-D embedded capacitor based on its physical design parameters. An extremely high capacitance density, up to 5,621.8 nF/mm^2, can be envisioned. Finite element simulation has also been done to ensure the structural integrity of the components. Next, various types of test vehicles have been successfully fabricated after the steps of photomask design, process flow design, and process optimization. Lastly, *C-V* and *I-V* characterizations have been performed to evaluate the electrical performance of the test vehicles. The *C-V* characterization results show that, with a trench diameter increasing from 10 to 50 μm, the capacitance of 3-D embedded capacitors varies from 98.7 to 625.2 nF/mm^2 for ALD type test vehicles and it varies from 3.6 to 138.7 nF/mm^2 for sputtering type test vehicles. The dielectric composition and the total amount of trapped charges in the dielectric layer become instable due to sidewall roughness. The *I-V* characterization results have been normalized to the *J-E* plots, which show that the leakage current density is ~2×10^{-7} A/cm^2 at 2 MV/cm and the dielectric strength is ~9.7 MV/cm for ALD type test vehicles; whereas the leakage current density is ~3×10^{-9} A/cm^2 at 2 MV/cm and the dielectric strength is ~8.0 MV/cm for sputtering type test vehicles. Based on the *J-E* plots, leakage current conduction mechanisms have been identified: Schottky emission, FN tunneling, PF emission, and hopping conduction have been fitted for ALD type test vehicles; whereas FN tunneling, and PF emission have been fitted for sputtering type test vehicles. In summary, the major contribution of this thesis is the design, fabrication, and characterization of a 3-D embedded capacitor. And this novel high-density capacitor will contribute to the further development of on-chip energy storage element, integrated voltage regulator, and capacitively coupled wireless module.

1.5 Organization of the Thesis

The organization of this thesis is outlined below:

- In Chapter 1, a brief introduction to the device scaling of microelectronics is given followed by the motivation, objectives, and major contribution of this thesis.
- In Chapter 2, a literature review is presented on the state-of-the-art integrated capacitor technologies for 3-D ICs.
- In Chapter 3, a novel integrated capacitor called the "3-D embedded capacitor" is proposed and designed; an electrical model is built to predict its capacitance; and a finite element simulation is performed to ensure the structural integrity of the 3-D embedded capacitor and its surrounding components.
- In Chapter 4, the photomask design and detailed process flows are presented, and the proper process recipes are developed for the fabrication of various test vehicles.
- In Chapter 5, *C*-*V* and *I*-*V* characterization results are presented and analyzed to evaluate the electrical performance of 3-D embedded capacitor test vehicles.
- In Chapter 6, a summary of this thesis and recommendations for future work are provided.

1.6 References

[1] J. Bardeen and W. H. Brattain, "Physical principles involved in transistor action," *Phys. Rev.*, vol. 75, no. 8, pp. 1208–1225, Apr. 1949.

[2] G. E. Moore, "Cramming more components onto integrated circuits," Reprinted from Electronics, vol. 38, no. 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Newsl.*, vol. 20, no. 3, pp. 33–35, Sep. 2006.

[3] Intel, "Leading at the edge: Intel technology and manufacturing." [Online]. Available:https://newsroom.intel.com/press-kits/leading-edge-intel-technology-manufacturing/.

[4] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore white paper," *Version*, vol. 2, p. 14, 2010.

[5] C. B. Les, "Image sensor market: Changing, but moving upward." Laurin Publ Co Inc Berkshire Common PO Box 1146, Pittsfield, MA 01202 USA, 2009.

[6] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 6–20, 2005.

[7] G. K. Fedder, R. T. Howe, T.-J. K. Liu, and E. P. Quevy, "Technologies for cofabricating MEMS and electronics," *Proc. IEEE*, vol. 96, no. 2, pp. 306–322, 2008.

[8] J. Tsai, "The evolution of MEMS displays," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1057–1065, 2009.

[9] T. Skotnicki and F. Boeuf, "Optimal scaling methodologies and transistor performance," in *High Dielectric Constant Materials*, Springer, 2005, pp. 143–194.

[10] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and engineering beyond Moore's Law," *Proc. IEEE*, vol. 100, no. Special Centennial Issue, pp. 1720–1749, May 2012.

[11] Stephen Shankland, "Moore's Law: The rule that really matters in tech." [Online]. Available: http://www.cnet.com/news/moores-law-the-rule-that-really-matters-in-tech/.

[12] G. E. Moore, "Cramming more components onto integrated circuits," *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, Jan. 1998.

[13] G. E. MOORE, "Lithography and the future of Moore's Law," *SPIE milestone Ser.*, vol. 178, pp. 182–197, 2004.

[14] R. R. Schaller, "Moore's Law: past, present and future," *IEEE Spectr.*, vol. 34, no. 6, pp. 52–59, Jun. 1997.

[15] X. Mi and S. Ue, "Integrated passives for high-frequency applications," in *Advanced Microwave Circuits and Systems*, InTech, 2010.

[16] Y. Sugaya, "A new 3-D module using embedded actives and passives," in *2001 International Symposium on Microelectronics, 10*, 2001.

[17] S.-M. Wu, E. Jahja, W.-K. Yen, and J.-W. Wang, "Study of discrete capacitor embedded process and characterization analysis in organic-base substrate," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 125–129.

[18] S. Shibasaki *et al.*, "Development of buried bump interconnection technology with embedded passive devices," in *Proceedings of International Conference on Electronic Packaging*, 2004, pp. 113–118.

[19] D.-W. Lew, J.-S. Park, D. Ahn, N.-K. Kang, C. S. Yoo, and J.-B. Lim, "A design of the ceramic chip balun using the multilayer configuration," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 1, pp. 220–224, 2001.

[20] R. L. Brown, P. W. Polinski, and A. S. Shaikh, "Manufacturing of microwave modules using low-temperature cofired ceramics," in *Microwave Symposium Digest, 1994, IEEE MTT-S International*, 1994, pp. 1727–1730.

[21] A. Sutono, D. Heo, Y.-J. E. Chen, and J. Laskar, "High-Q LTCC-based passive library for wireless system-on-package (SOP) module development," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 10, pp. 1715–1724, 2001.

[22] G. W. Dahlmann, E. M. Yeatman, P. Young, I. D. Robertson, and S. Lucyszyn, "High Q achieved in microwave inductors fabricated by parallel self-assembly," in *Transducers' 01 Eurosensors XV*, Springer, 2001, pp. 1070–1073.

[23] X. Mi, T. Takahashi, and S. Ueda, "Integrated passives on LTCC for achieving chip-sized-modules," in *Microwave Conference, 2008. EuMC 2008. 38th European*, 2008, pp. 607–610.

[24] L. Doyle, "Integrated passive and active devices using CSP," *DFN QFN Packag. Wirel. Appl. Microw. Eng. Eur.*, pp. 36–40, 2005.

Chapter 2 A Review on Integrated Capacitor Technologies for Three-Dimensional Integrated Circuits

2.1 Three-Dimensional Integrated Circuit

2.1.1 Three-Dimensional Integration

Three-dimensional (3-D) integration is a key technology to integrate heterogenous components with diversified functions. The staked chips are called "three-dimensional integrated circuits" (3-D ICs) [1]–[7]. Compared with conventional two-dimensional (2D) planar integration, 3-D integration technology provides many benefits. Firstly, electrical interconnects in vertical integration systems can be much shorter: thus, introducing less resistive-capacitive (RC) delay, as shown in Figure 1.1. Secondly, chip stacking helps to reduce the form factor, which is vital for portable and wearable electronics. Thirdly, because of 3-D integration, the number of interconnects between different chips can be increased dramatically: therefore enabling high-bandwidth communication between multiple integrated circuits [7].

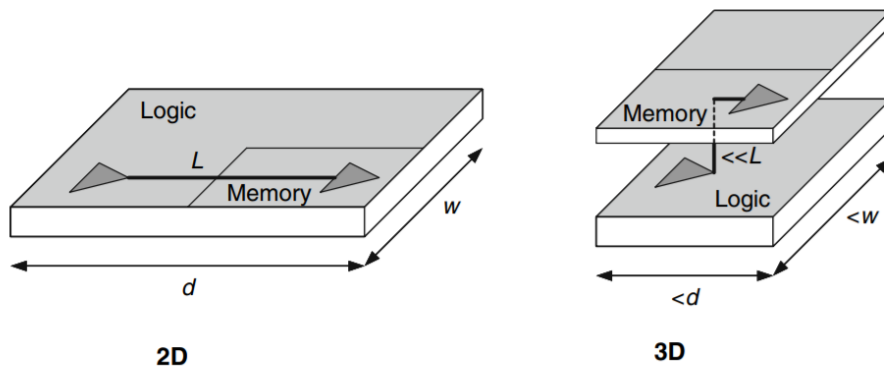


Figure 2.1: Three-dimensional integration can replace long global and semiglobal wires with shorter vertical interconnects [7].

There are three major categories in 3-D integration technology: (1) 3-D IC packaging, (2) 3-D IC integration, and (3) 3-D Si integration, as shown in Figure 2.2 [8]–[10]. The first category, 3-D packaging, can be implemented by either die stacking with wire bonds or package-on-package stacking (PoP). The electronic packaging industry has adopted 3-D IC packaging for mass production due to its low cost. 3-D IC packaging helps to achieve smaller form factors of IC packages, and it is especially favorable in the field of mobile electronics. However, the limitation of this integration method is that wires can only be placed at the edge areas of chips, so the total number of interconnects is very limited. Therefore, it can only be applied to low input/output (I/O) applications. The remaining two categories, 3-D IC integration and 3-D Si integration, are similar because signal and power are transmitted between vertical layers by through-silicon vias (TSVs), instead of wire bonds. However, they differ in terms of the chips/wafers being stacked with microbumps in 3-D IC integration, whereas the stacking of chips/wafers occurs bumplessly in 3-D Si integration. The advantage of 3-D Si integration over 3-D IC integration is that finer pitch and better electrical performance of interconnects can be achieved with bumpless stacking. Nevertheless, 3-D Si integration is still at the research stage, as it requires much more stringent conditions to be met for contact surface preparation. The cross-sectional views of 3-D IC integration and 3-D Si integration bonding interfaces are shown for comparison in Figure 2.3.

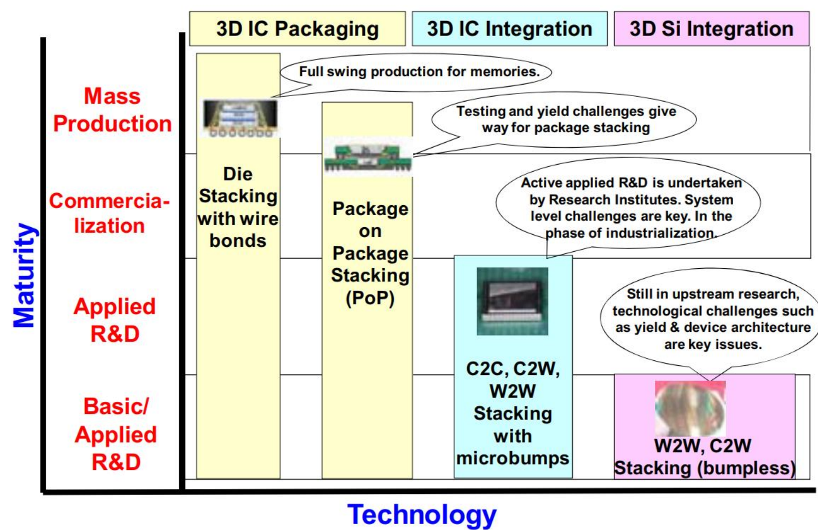
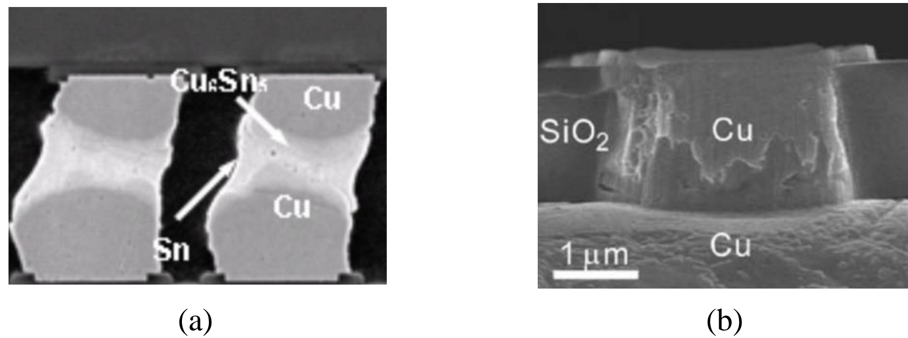


Figure 2.2: Maturity of 3-D integration technologies: 3-D IC Packaging, 3-D IC integration, and 3-D Si integration [8].



(a) (b)

Figure 2.3: (a) Cross-section of micro joints with a Cu/Sn solder micro bump joined to a Cu/Sn solder micro bump [11]. (b) Scanning electron microscopy image of a 4 µm Cu interconnect bonded to a Cu pad showing a high-quality Cu-to-Cu bonding interface [12].

In addition to the 3-D integration technologies mentioned above, there is a similar approach, Si interposer technology, to realize fine-pitch, high I/O, high density, and low-cost IC integration [13]–[15]. Using this technology, chips can be mounted side-by-side on the top surface of the Si interposer and interconnected closely via redistribution layers (RDLs). The I/O density is greatly improved due to high resolution fabrication processes on the Si substrate compared with coarse fabrication processes on the organic substrate. Then the signal and power pins are extended to the bottom of the interposer by TSVs, which provide vertical interconnection to the package substrate. Figure 2.4 shows the world’s first interposer product, which is a FPGA demonstrated by Xilinx in 2011 [16]. Although Si interposer integration is also called “2.5-D integration,” it is considered a separate technology rather than an evolutionary one between 2-D and 3-D integration technologies.

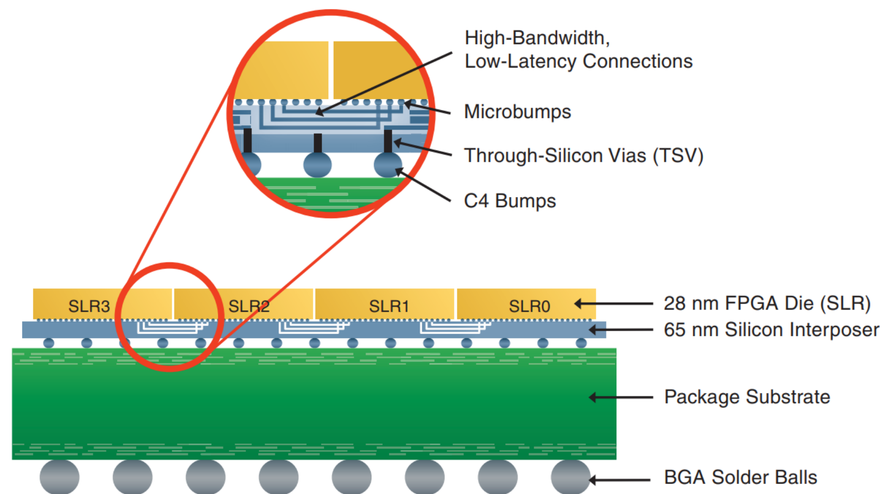


Figure 2.4: Virtex®-7 2000T FPGA as the first Si interposer product [16].

2.1.2 Through-Silicon Via

Through-silicon via (TSV) is not a new idea, as William Shockley filed it as a patent in 1958 [17]. Figure 2.5 shows that the original thought was to drill a hole in the Si substrate and connect two wafers together, but this was not intended for 3-D integration.

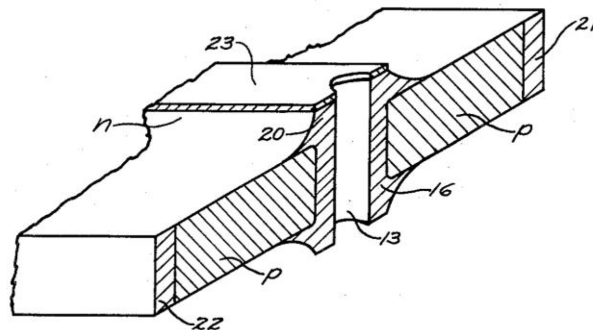


Figure 2.5: Through-silicon via as invented by William Shockley [17].

Today, TSV is a key enabler in 3-D IC, 3-D Si, and 2.5D integration technologies. This basic component provides a vertical electrical connection between different layers [18], [19]. Both the signal and power are transmitted through TSVs.

The obvious benefits of TSV compared with conventional planar 2D interconnects are a much shorter length (therefore, lower RC delay) and a higher bandwidth.

a. Fabrication Process

There are three mainstream approaches and one simplified one to implement TSVs in 3-D ICs, as illustrated in Figure 2.6. The three mainstream approaches are the via-first, the via-middle, and the via last [20].

- The via-first approach: TSVs are formed before the device front-end of line (FEOL) fabrication process.
- The via-middle approach: TSVs are formed before the interconnect back-end of line (BEOL), but after the device front-end of line (FEOL) fabrication process.
- The via-last approach: TSVs are formed after the interconnect back-end of line (BEOL) fabrication process.

Besides, the simplified approach with cost reduction is called “backside via-last.” It is widely used to form large and tapered TSVs in image sensors and microelectromechanical systems (MEMS) [21].

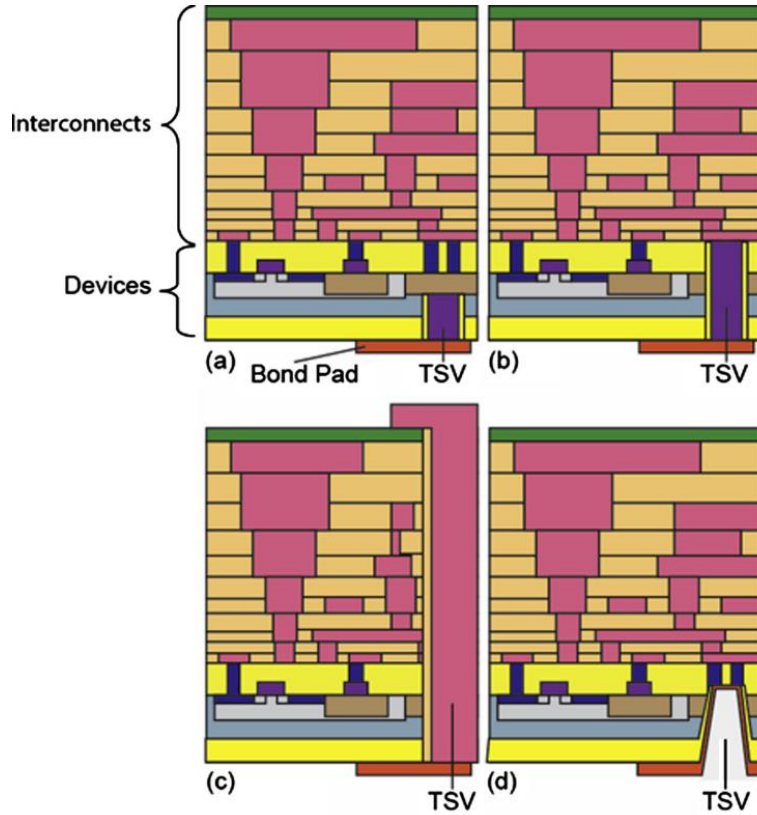


Figure 2.6: Schematic of (a) frontside via-first, (b) frontside via-middle, (c) frontside via-last, and (d) backside via-last structures [20].

The fabrication process of TSV generally consists of four major steps: (1) TSV etching, (2) TSV insulation, (3) TSV metallization, and (4) overburden removal by chemical mechanical polishing (CMP), which are depicted as Steps (2)-(5) in Figure 2.7. The rest of the steps in the figure need to be carried out if a complete series of 3-D integration with other chips/wafers is desired.

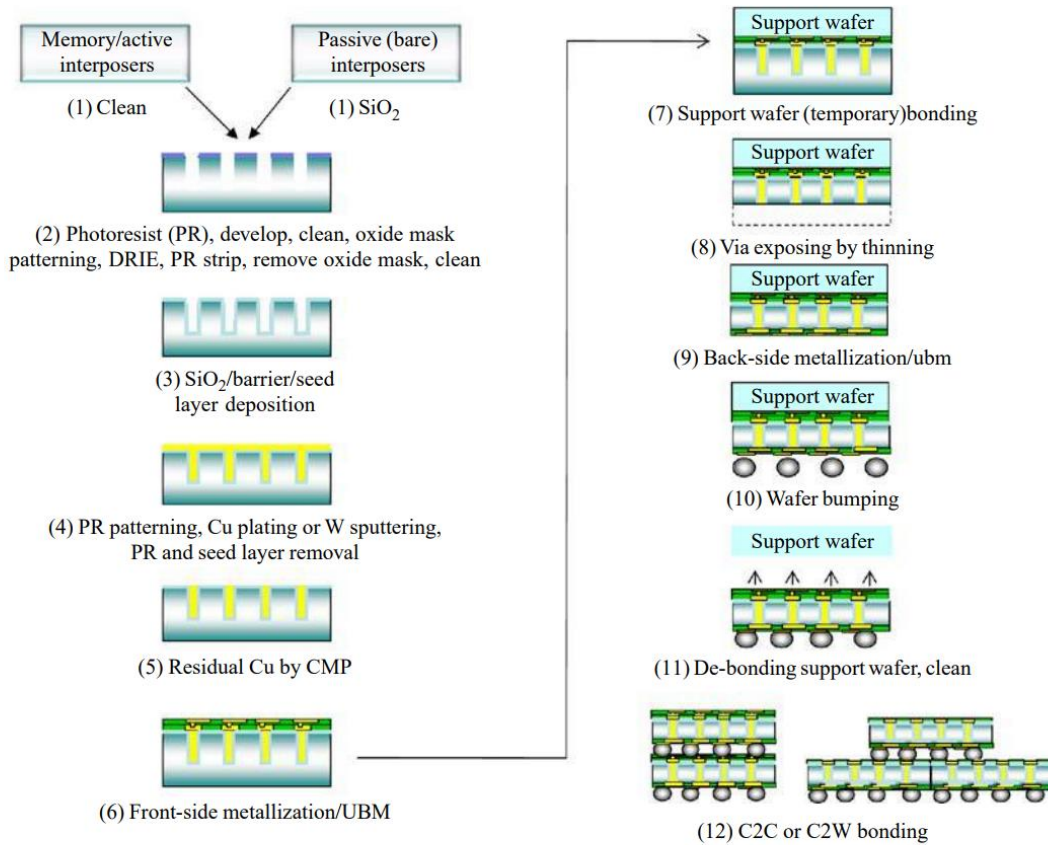


Figure 2.7: Complete TSV fabrication process and integration steps [8].

TSV Etching

Deep reactive ion etching (DRIE) is a typical method to etch deep trenches for TSVs. It was initially invented by Bosch in the 1990s for MEMS fabrication [22]. The feature of the Bosch process is the alternating steps of etching and passivation, so that trenches with a high aspect ratio and anisotropic profile can be formed [23]. During passivation steps, CF_2-species are deposited on the sidewall as a passivation layer, whereas for etching steps, F-species are directed to the bottom of trenches (removing all vertical passivation and a part of the sidewall passivation). These steps are performed subsequently to etch deep into the silicon, as illustrated in Figure 2.8. After etching, the trench profile can be seen, as shown in Figure 2.9 [24]. However, the Bosch process inevitably leaves a series of small ridges on the sidewall of trenches known as “scallops,” as shown in Figure 2.10 [25].

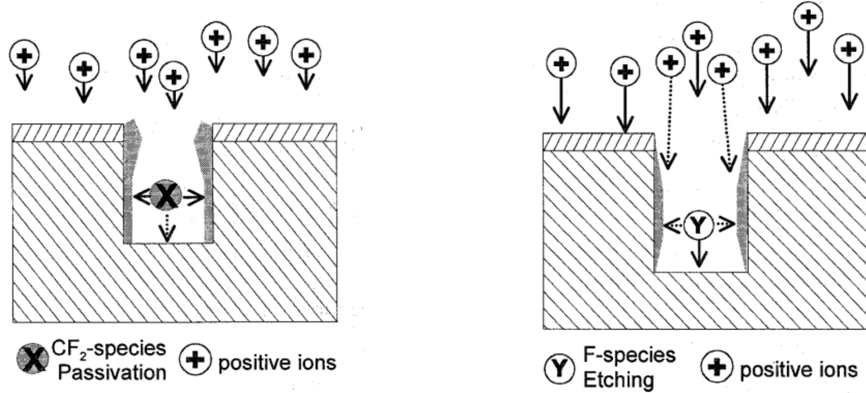


Figure 2.8: Sidewall passivation mechanism of the Bosch deep silicon etching process. The protecting film deposited in the passivation step extends deeper into the trenches during the etch step to yield a smooth sidewall [23].

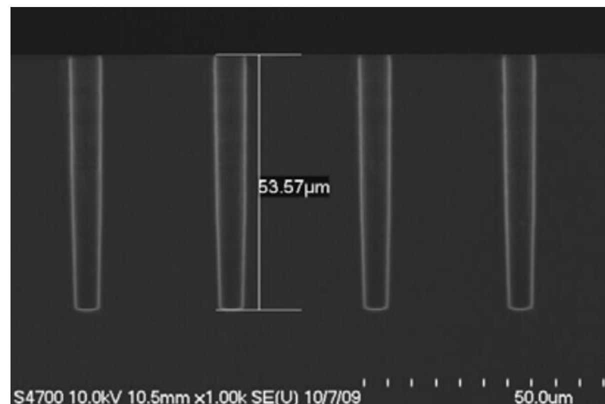
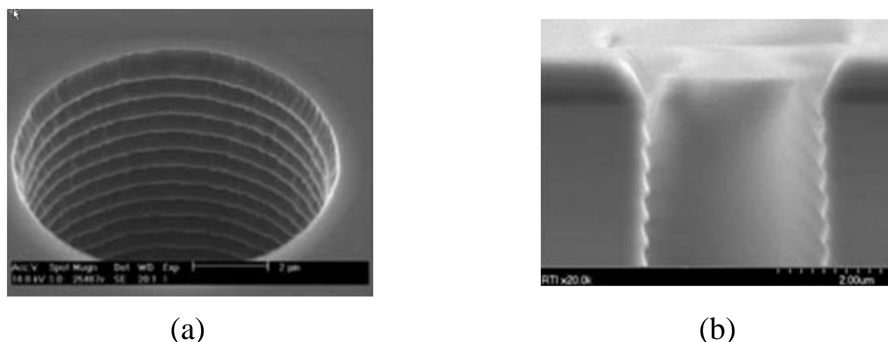


Figure 2.9: Via formation after the Bosch DRIE process with ~5 μm in diameter and ~50 μm in depth [24].



(a) (b)

Figure 2.10: DRIE features etched in Si. (a) Top view of TSV with sidewall scallops. (b) Cross-sectional view of scallops in the Si trench [25].

TSV Insulation

After DRIE and post-etching chemical cleaning, a conformal SiO_2 layer is deposited on the trench sidewall by chemical vapor deposition (CVD). It electrically insulates TSV from the surrounding Si substrate, known as the "TSV liner." The thickness of the insulation layer depends on the requirements of leakage current, the breakdown voltage, and parasitic capacitance for different applications. Typically, two CVD options are available for TSV insulation. When high conformality is required for the insulation layer, sub-atmospheric chemical vapor deposition (SACVD) is preferred using O_3/Tetra-Ethyl-Ortho-Silicate (TEOS). However, this option is sometimes limited by its high thermal activation temperature. When a lower process temperature is required, plasma enhanced chemical vapor deposition (PECVD) is an excellent choice for depositing SiO_2 insulation due to its lower process temperature (around 250°C). A comparison of SiO_2 insulation layer step coverage along the sidewall is made between these two CVD options, as shown in Figure 2.11 [26].

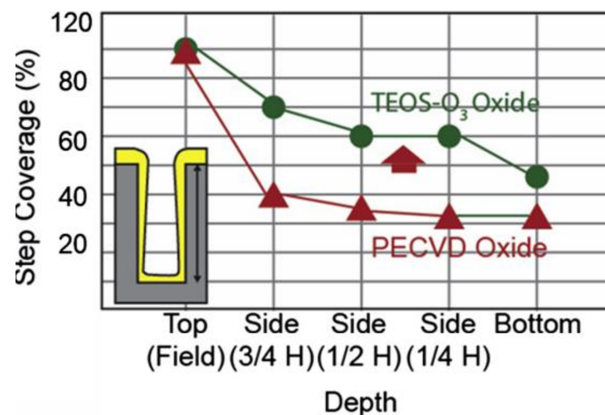


Figure 2.11: Step coverage along the sidewalls and bottom of TSV for SiO_2 deposited with PECVD and SACVD [26].

TSV Metallization

Copper electroplating is the core filling method for most TSVs at the current stage because of copper's superior electrical conductivity. Other possible materials

are tungsten and polysilicon. Before Cu TSV metallization, a diffusion barrier layer needs to be sputtered between the Cu and SiO_2 insulation layer. Usually TiN, TaN, and Ta can be considered ideal candidate materials. Then the Cu seed layer is sputtered to prepare the sidewall for electroplating. A cross-section of the sidewall can be seen in Figure 2.12 after diffusion barrier/seed layer deposition [27]. The conventional electroplating method may cause various Cu voids when a high aspect ratio TSV trench needs to be fully filled, as shown in Figure 2.13 [26]. But fortunately, significant technique advances have been made in Cu electroplating in terms of highly engineered plating chemistries and process equipment [28]. A "bottom-up" growth approach has been developed for void-free Cu filling.

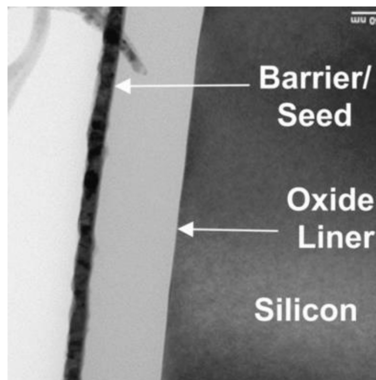


Figure 2.12: TEM section of the TSV sidewall showing the scallop free etch profile, conformal SACVD oxide liner, and continuous barrier/seed [27].

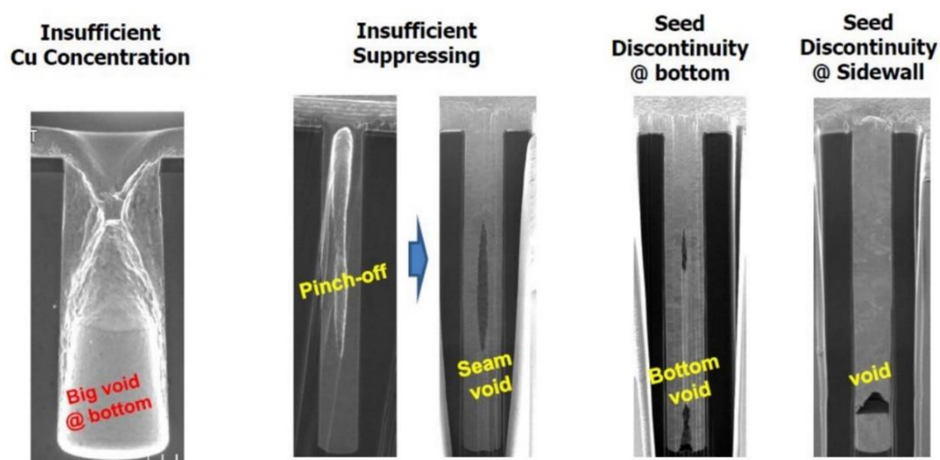


Figure 2.13: Root causes of various Cu voids [26].

Overburden Removal

As the last step of TSV formation, chemical mechanical polishing (CMP) is used to remove copper, the diffusion barrier lay, and the insulation layer to realize surface planarization [29], [30]. The total thickness of the overburden is usually higher than 2D planar interconnects. In order to ensure that Cu is removed from all parts of the wafer, over-polishing needs to be conducted. Figure 2.14 shows a typical TSV after high-rate Cu CMP [31]. Cu CMP usually involves two major steps: (1) Cu removal, stopping at the barrier layer, and (2) barrier removal, stopping at the insulation layer.

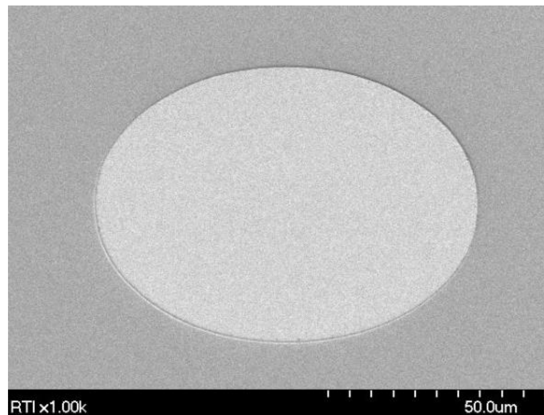


Figure 2.14: Typical TSV after high-rate Cu chemical mechanical polishing [31].

b. Electrical Modeling

Through-silicon via is a key enabler in 3-D integration, as it forms the vertical interconnect between different stacked chips. However, it has its own parasitic resistance, capacitance, and inductance. The electrical behavior of TSVs has a great impact on the overall performance of 3-D ICs [31]. Thus, it is important to understand and perform the electrical modelling of TSVs with different design parameters. Essentially, a TSV can be regarded as a vertical metal-oxide-semiconductor (MOS) structure with a metal conductive core and the Si substrate as the semiconductor [31]. An illustration is shown in Figure 2.15. The resistance, capacitance, and inductance of TSVs have been characterized by different groups of researchers [32]–[35]. A

simple closed-form model was derived by [36]–[40] based on scalable physical dimensions and material characteristics.

The DC resistance of TSV can be expressed as:

$$R_{\mathrm{TSV_DC}} = \frac{\rho l_{\mathrm{TSV}}}{\pi r_{\mathrm{TSV}}^2} \tag{2.1}$$

where ρ is the resistivity of the core material, r_{TSV} is the radius of TSV, and l_{TSV} is the length of TSV. For the resistance of TSV at a higher frequency, the skin effect should be taken into account [41].

The capacitance of TSV can be expressed as:

$$C_{\mathrm{TSV}} = \frac{2\pi\varepsilon_{0x} l_{\mathrm{TSV}}}{\ln\left(\frac{R_{\mathrm{dep}}}{R_{\mathrm{Metal}}}\right)} \tag{2.2}$$

where $\varepsilon_{\mathrm{ox}}$ is the permittivity of the oxide layer. Because of the nature of the MOS structure, the radius of the depletion layer will change in accordance to the bias condition. Therefore, the capacitance of a TSV is not a constant value and varies with operating voltage.

The inductance of TSV can be expressed as (partial self-inductance):

$$L_{\mathrm{TSV}} = \frac{\mu_0}{4\pi}\left[2l_{\mathrm{TSV}} \ln\left(\frac{2l_{\mathrm{TSV}} + \sqrt{r_{\mathrm{TSV}}^2 + (2l_{\mathrm{TSV}})^2}}{r_{\mathrm{TSV}}}\right) + \left(r_{\mathrm{TSV}} - \sqrt{r_{\mathrm{TSV}}^2 + (2l_{\mathrm{TSV}})^2}\right)\right] \tag{2.3}$$

where μ_0 is the permeability of free space.

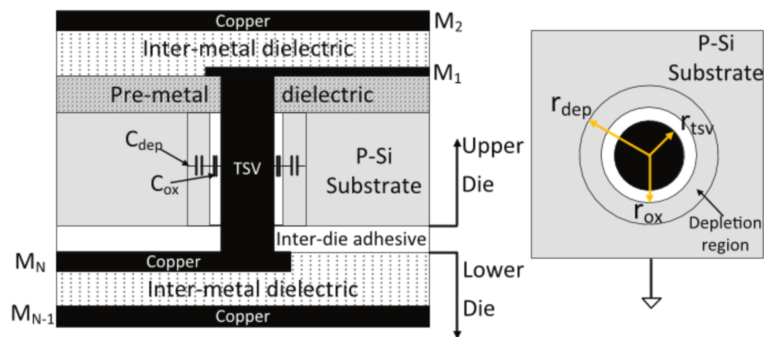


Figure 2.15: The equivalent electrical model of a typical TSV [31].

2.1.3 Power Integrity

Researchers have put much effort into the study of power integrity, as it is one of the biggest challenges in 3-D ICs [42]–[45]. With the advance of the technology node, more transistors are now being integrated into a chip. Moreover, in 3-D ICs, the number of transistors is even higher due to multiple chip layers being stacked vertically into the same footprint. The negative effect of this increasing integration density is two-fold. First, it leads to a higher demand for current supply (thus, a higher IR drop). Secondly, since more transistors are switching at the same time, the simultaneous switching noise (SSN, otherwise known as *Ldi/dt* noise) is greater: causing a higher supply voltage fluctuation. Power integrity in 3-D ICs can be mitigated from two aspects: (1) the design of power delivery network (PDN) and (2) the integration of voltage regulator.

A diagram of the power delivery network (PDN) for a general microelectronic system is illustrated in Figure 2.16 [24]. It shows a voltage regulation module (VRM) on the PCB board and different levels of decoupling capacitors (from PCB, packaging, BEOL, to FEOL). They together store energy temporarily for emergency, in case there is a demand for current supply due to the simultaneous switching of transistors. From impedance's point of view, a methodology called "target impedance" was proposed for the PDN design [46].

$$Z_{\text{target}} = \frac{(\text{power supply voltage}) \times (\text{allowed ripple})}{\text{current}} \quad (2.4)$$

The output impedance of a well-designed PDN should be always below a specified target impedance over the desired operating frequency region. Decoupling capacitors help to decrease PDN impedance, so that the overall PDN impedance falls approaching the target impedance in Figure 2.17. With suitable capacitors, a large current surge would eventually lead to acceptable voltage ripples: preserving power integrity [47]. Decoupling capacitors, from the PCB level to FEOL level, generally are decreasing in capacitance value, but have higher resonant frequencies. This demonstrates that decoupling capacitors from different levels suppresses PDN impedance in respective frequency domains.

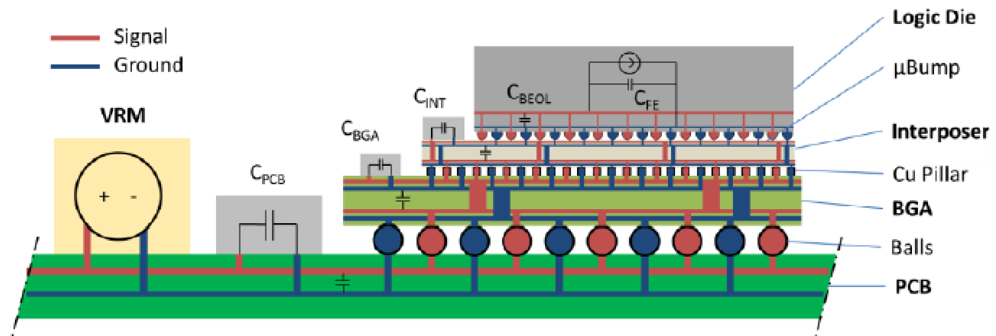


Figure 2.16: A diagram of the power delivery network (PDN) for microelectronic systems [24].

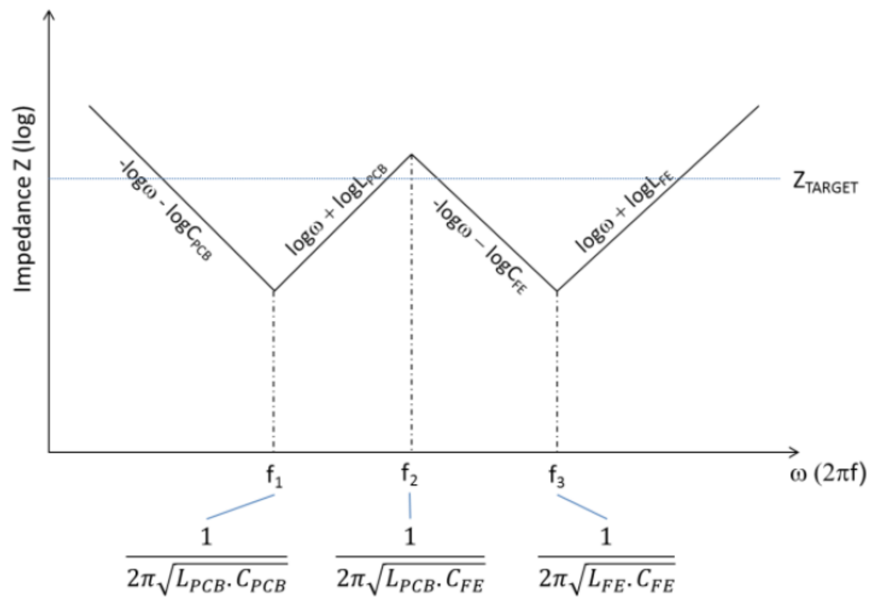


Figure 2.17: A simplified resonator model including two decoupling capacitors [47].

2.2 Integrated Capacitor Technologies

Integrated capacitor technologies can be classified into three major groups: (1) laminate-based integrated capacitors, (2) low temperature co-fired ceramic (LTCC) -based integrated capacitors, and (3) thin film-based integrated capacitors [48].

2.2.1 Laminate-based Integrated Capacitor

A laminate-based integrated capacitor is a capacitor embedded in a printed circuit board (PCB) [45]. It can be further classified into two sub-types: (1) the embedded discrete capacitor and (2) the embedded planar capacitor as shown in Figure 2.18. An embedded discrete capacitor is a surface mounted capacitor embedded in a PCB instead of on the top surface of the PCB. It is then connected to other components on the top surface through conductive vias. An embedded planar capacitor is a laminate embedded in a PCB as a planar capacitor, whose dielectric layer is usually 10 to 50 μm thick.

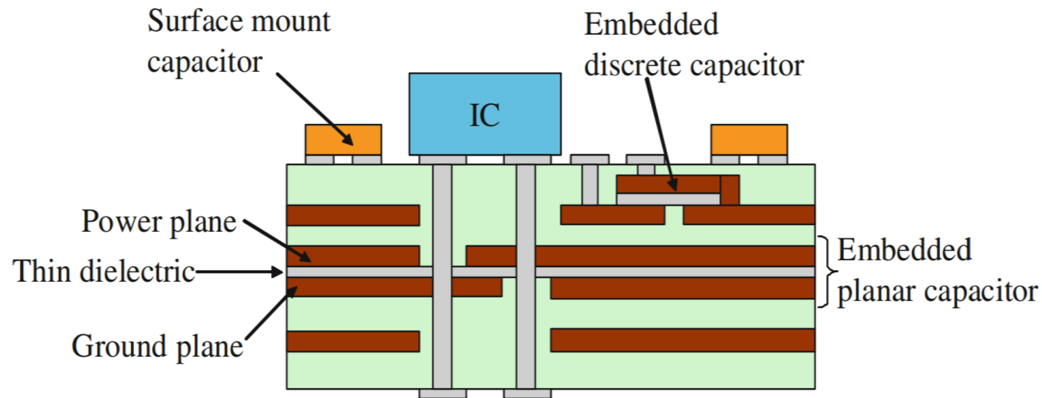


Figure 2.18: Embedded discrete and embedded planar capacitors in a printed circuit board [45].

The dielectric materials used in laminate-based integrated capacitors should have a low processing temperature, because the thermal budget for processing is limited by the organic substrate of the PCB. Therefore, the dielectric materials are mostly ferroelectric and paraelectric types [45]. The ferroelectric dielectrics (e.g., $BaTiO_3$, $Pb_xZr_{1-x}TiO_3$, and $Ba_xSr_{1-x}TiO_3$) can exhibit extremely high dielectric

constants because of the total contribution from electronic polarization, ionic polarization, and dipole polarization [49]–[51]. But the drawback is that they are strongly frequency and temperature dependent. The paraelectric dielectrics (e.g., Al_2O_3, TiO_2, Ta_2O_5, polyimide and epoxy) show relatively low dielectric constants compared with those of ferroelectric dielectrics, but they are more stable with respect to frequency and temperature [52]–[57].

2.2.2 Low Temperature Co-Fired Ceramic-Based Integrated Capacitor

A low temperature co-fired ceramic-based integrated capacitor (LTCC)-based integrated capacitor is similar to a laminate-based integrated capacitor in two aspects: (1) both types of integrated capacitors are embedded in substrate; and (2) both types of integrated capacitors are patterned by a screen-print technique, which has less precision in terms of pattern size and layer thickness [48]. In addition to the conventional implementation of the LTCC parallel plate capacitor in Figure 2.19(a), an alternative approach called "vertically interdigitated configuration" is also available to realize the same target capacitance with much less planar area as shown in Figure 2.19(b).

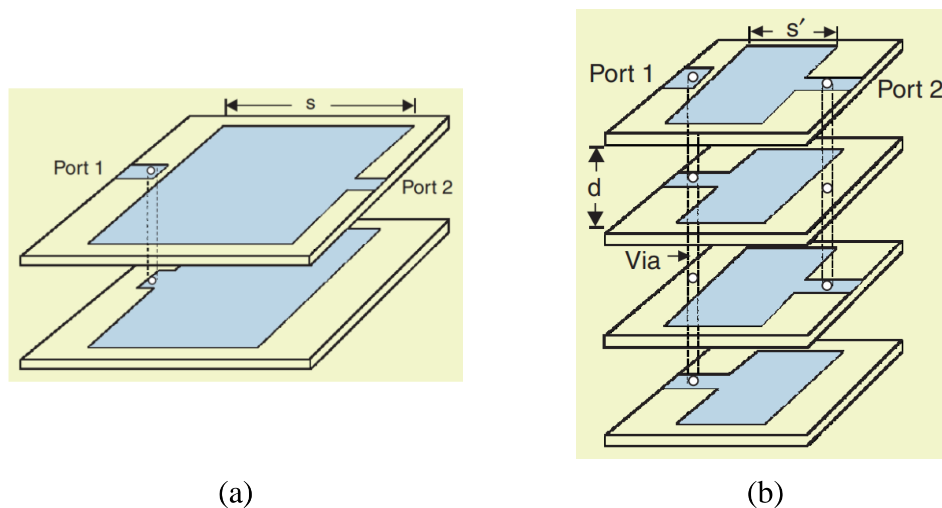


Figure 2.19: Illustrations of the two types of LTCC-based integrated capacitors: (a) a parallel plate capacitor and (b) a vertically interdigitated configuration capacitor.

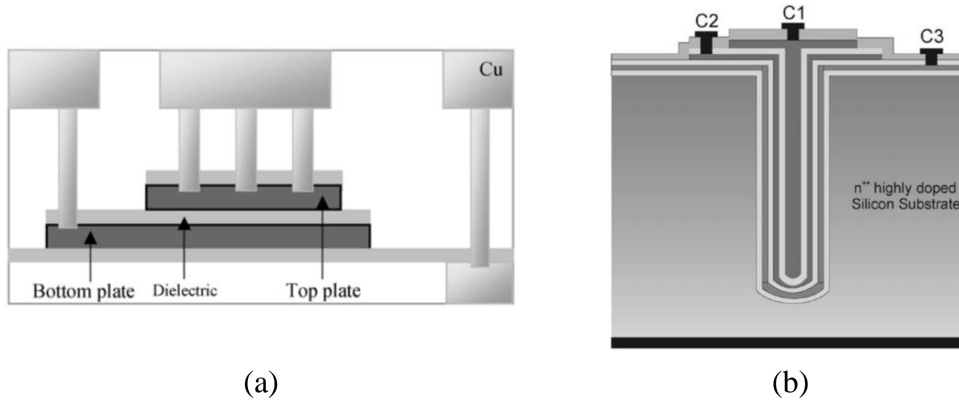
The dielectric materials used in LTCC-based integrated capacitors have a higher thermal budget for processing compared to the materials in laminate-based ones. But the melting point of metals used in LTCC still makes it challenging to develop high-κ ceramic dielectric materials for capacitor applications. Also, the typical firing temperature is set in the range of 850–950°C [58]. Table 2.1 presents a summary to compare the dielectric materials used for integrated capacitors in LTCC, high temperature co-fired ceramics (HTCC), FR4, and glass [48]. It shows that the dielectric materials compatible with LTCC tend to have higher dielectric constants and lower loss tangents, which are in favor of integrated capacitors.

Table 2.1: Dielectric materials used for embedded capacitors [48].

	Electrical			Thermal		Mechanical	
	ε	**tan δ** (10^{-4})	**Resistivity** (Ω cm)	CTE (ppm/K)	**Thermal Conductivity** (W/mK)	**Flexural Strength** (MPa)	**Young's Modulus** (GPa)
LTCC	5 - 80	2.5 - 40	$>10^{14}$	3-12	1.2-5	170-400	74-188
HTCC	8.5 - 10	5-25	$>10^{14}$	6.9-7.2	10-25	400-460	260-310
ALN	8.7	170	$>10^{14}$	4.7	150-230	400	320
FR4/ glass	4.5 - 5.5	200 - 300	$>10^{14}$	xy:16-20 z:50-70	0.2	430	—

2.2.3 *Thin film-based passive integrated capacitor*

A thin film-based integrated capacitor is built onto the surface of the substrate instead of being embedded in the substrate. It has higher precision, a higher quality factor, higher self-resonant frequency, higher capacitance density, and a smaller size than other integrated capacitor technologies because it is made with standard IC fabrication processes [48]. A typical implementation is to build planar metal-insulator-metal (MIM) layers in the back-end-of-line layers as shown in Figure 2.20(a) [59]–[64]. Another implementation method is proposed to reduce the planar surface area significantly by leveraging on the depth of the substrate. This method is called the “trench MIM capacitor” [65], [66].



(a) (b)

Figure 2.20: Illustrations of the two types of thin film-based integrated capacitors: (a) a planar MIM capacitor and (b) a trench MIM capacitor [64], [65].

The dielectric materials used in thin film-based integrated capacitors are tabulated in Table 2.2. These high-κ dielectric materials have been extensively studied for analog, mixed signal, and radio frequency (RF) applications [67]–[74].

Table 2.2: Dielectric materials used for thin film-based integrated capacitors [48].

	Dielectric Constant	Dielctric Loss (10^{-4})	Breakdown Field (MV/cm)	Demonstrated C-dencity (nF/mm^2)
SiO_2	4.2	10	10	1
Si_3N_4	7.6	11	7	2
Al_2O_3	7.9	30	8	3.5
HfO_2	17-21	500	6	5, 13
Ta_2O_5	22-25	100	5	5
ZrO_2	45	-	4	-
$SrTiO_3$	150	200	1	10
BaTiO3	800	<60		80
PZT	900			

2.3 Summary

In this chapter, firstly we reviewed different types of 3D-IC integration methods, including (1) 3-D IC packaging, (2) 3-D IC integration, (3) 3-D Si integration, and (4) interposer integration. The choice of implementation depends on the trade-offs between performance, form factor, and cost. Secondly, the fabrication steps and electrical modelling of TSV were studied. The literatures on these topics revealed both challenges and opportunities of interconnects in 3-D ICs. Lastly, integrated capacitor technologies were discussed based on three major groups: (1) laminate-based integrated capacitors, (2) low temperature co-fired ceramic (LTCC) -based integrated capacitors, and (3) thin film-based integrated capacitors. Based on these prior arts, a novel integrated capacitor for ICs with TSVs will be proposed to achieve ultrahigh capacitance density in the next chapter.

References

[1] Y. Xie, J. Cong, and S. Sapatnekar, "Three-dimensional integrated circuit design," *EDA, Des. Microarchitectures, New York Springer*, vol. 20, pp. 194–196, 2010.

[2] J. U. Knickerbocker *et al.*, "Three-dimensional silicon integration," *IBM J. Res. Dev.*, vol. 52, no. 6, pp. 553–569, 2008.

[3] C. T. Ko and K. N. Chen, "Wafer-level bonding/stacking technology for 3D integration," *Microelectron. Reliab.*, vol. 50, no. 4, pp. 481–488, 2010.

[4] P. Garrou, M. Koyanagi, and P. Ramm, *Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits - Vol 3*. John Wiley & Sons, 2014.

[5] W. Banqiu, A. Kumar, and S. Ramaswami, *3D IC Stacking Technology*. McGraw-Hill New York, USA, 2011.

[6] A. Papanikolaou, D. Soudris, and R. Radojcic, *Three dimensional system integration: IC stacking process and design*. Springer Science & Business Media, 2011.

[7] C. S. Tan, R. J. Gutmann, and L. R. Reif, "Wafer Level 3-D ICs Process Technology," C. S. Tan, R. J. Gutmann, and L. R. Reif, Eds. Boston, MA: Springer US, 2008, pp. 1–11.

[8] J. H. Lau, "Evolution, challenge, and outlook of TSV, 3D IC integration and 3d silicon integration," in *Proceedings - International Symposium on Advanced Packaging Materials*, 2011, pp. 462–488.

[9] J. H. Lau, *Reliability of ROHS-compliant 2D and 3D IC Interconnects*. McGraw Hill Professional, 2011.

[10] J. H. Lau, "Evolution and outlook of TSV and 3D IC/Si integration," in *2010 12th Electronics Packaging Technology Conference, EPTC 2010*, 2010, pp. 560–570.

[11] A. Yu *et al.*, "Study of 15μm pitch solder microbumps for 3D IC integration,"

in *Proceedings - Electronic Components and Technology Conference*, 2009, pp. 6–10.

[12] K. Chen *et al.*, “Structure , Design and Process Control for Cu Bonded Interconnects in 3D Integrated Circuits,” in *IEEE Electron Devices Meeting*, 2006, pp. 8–11.

[13] D. M. Jang *et al.*, “Development and evaluation of 3-D SiP with vertically interconnected Through Silicon Vias (TSV),” in *Proceedings - Electronic Components and Technology Conference*, 2007, pp. 847–852.

[14] M. Jin, “3D Si Interposer design and electrical performance study,” *Des. 2013*, 2013.

[15] K. Takahashi *et al.*, “Current Status of Research and Development for Three-Dimensional Chip Stack Technology,” *Jpn. J. Appl. Phys.*, vol. 40, no. 4S, pp. 3032–3037, 2001.

[16] P. Dorsey, “Xilinx stacked silicon interconnect technology delivers breakthrough fpga capacity, bandwidth, and power efficiency,” 2010.

[17] W. Shockley, “Semiconductive Wafer and Method of Making the Same Field,” 1962.

[18] E. Beyne, “3D System Integration Technologies,” in *2006 International Symposium on VLSI Technology, Systems, and Applications*, 2006, pp. 1–9.

[19] M. Shapiro *et al.*, “Reliable through silicon vias for 3D silicon applications,” in *Proceedings of the 2009 IEEE International Interconnect Technology Conference, IITC 2009*, 2009, pp. 63–65.

[20] “International Technology Roadmap for Semiconductors, in: Interconnect.”

[21] D. Henry *et al.*, “Through silicon vias technology for CMOS image sensors packaging,” in *Proceedings - Electronic Components and Technology Conference*, 2008, pp. 556–562.

[22] F. Laermer and S. Andrea, “Method of anisotropically etching silicon,” US 5501893A, 1996.

[23] F. Laerme, A. Schilp, K. Funk, and M. Offenberg, "Bosch deep silicon etching: improving uniformity and etch rate for advanced MEMS applications," in *Technical Digest. IEEE International MEMS 99 Conference. Twelfth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.99CH36291)*, 1999, pp. 211–216.

[24] J. Dukovic *et al.*, "Through-silicon-via technology for 3D integration," in *2010 IEEE International Memory Workshop*, 2010, pp. 1–2.

[25] D. Malta, "TSV Formation Overview," in *Handbook of 3D Integration*, Weinheim, Germany: Wiley-VCH Verlag GmbH & Co. KGaA, 2014, pp. 65–78.

[26] K. J. Moon, "A robust TSV middle scheme for 3D interconnects technology," in *Advanced Metallization Conference (AMC)*, 2010.

[27] J. Dukovic *et al.*, "Through-silicon-via technology for 3D integration," in *2010 IEEE International Memory Workshop*, 2010, pp. 1–2.

[28] R. Beica, P. Siblerud, and D. Erickson, "Advanced TSV Copper Electrodeposition for 3D Interconnect Applications," *Addit. Conf. (Device Packag. HiTEC, HiTEN, CICMT)*, vol. 2010, no. DPC, pp. 000774–000802, Jan. 2010.

[29] M. R. Oliver, Ed., *Chemical-Mechanical Planarization of Semiconductor Materials*, vol. 69. Berlin, Heidelberg: Springer Berlin Heidelberg, 2004.

[30] Y. Hayashi *et al.*, "A new two-step metal-CMP technique for a high performance multilevel interconnects featured by Al- and 'Cu in low ε, organic film'-metallizations," in *1996 Symposium on VLSI Technology. Digest of Technical Papers*, pp. 88–89.

[31] L. R. Robert, "Overview of CMP for TSV Applications." [Online]. Available: http://www.entrepix.com/docs/papers-and-presentations/Rhoades-CMP-for-TSV-AVS-June2013-shareable.pdf.

[32] J. Van Olmen *et al.*, "3D stacked IC demonstration using a through Silicon Via First approach," in *2008 IEEE International Electron Devices Meeting*, 2008,

pp. 1–4.

[33] Chunghyun Ryu, Daehyun Chung, Junho Lee, Kwangyong Lee, Taesung Oh, and Joungho Kim, "High frequency electrical circuit model of chip-to-chip vertical via interconnection for 3-D chip stacking package," in *IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging, 2005.*, pp. 151–154.

[34] L. L. W. Leung and K. J. Chen, "Microwave characterization and modeling of high aspect ratio through-wafer interconnect vias in silicon substrates," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 8, pp. 2472–2480, Aug. 2005.

[35] E. M. Chow *et al.*, "Process compatible polysilicon-based electrical through-wafer interconnects in silicon substrates," *J. Microelectromechanical Syst.*, vol. 11, no. 6, pp. 631–640, Dec. 2002.

[36] G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, "Electrical Modeling and Characterization of Through Silicon via for Three-Dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 256–262, Jan. 2010.

[37] C. Bermond, L. Cadix, A. Farcy, T. Lacrevaz, P. Leduc, and B. Flechet, "High frequency characterization and modeling of high density TSV in 3D integrated circuits," in *2009 IEEE Workshop on Signal Propagation on Interconnects*, 2009, pp. 1–4.

[38] D. M. Jang *et al.*, "Development and Evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV)," in *2007 Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 847–852.

[39] Jun So Pak *et al.*, "PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 208–219, Feb. 2011.

[40] Joohee Kim *et al.*, "High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 181–195, Feb. 2011.

[41] M. E. Goldfarb and R. A. Pucel, “Modeling via hole grounds in microstrip,” *IEEE Microw. Guid. Wave Lett.*, vol. 1, no. 6, pp. 135–137, Jun. 1991.

[42] H. Yu, J. Ho, and L. He, “Allocating power ground vias in 3D ICs for simultaneous power and thermal integrity,” *ACM Trans. Des. Autom. Electron. Syst.*, vol. 14, no. 3, pp. 1–31, 2009.

[43] Z. Li, H. Shi, J. Xie, and A. Rahman, “Development of an optimized power delivery system for 3D IC integration with TSV silicon interposer,” in *Proceedings - Electronic Components and Technology Conference*, 2012, pp. 678–682.

[44] G. Huang, M. S. Bakir, A. Naeemi, and J. D. Meindl, “Power delivery for 3-D chip stacks: Physical modeling and design implication,” in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2012, vol. 2, no. 5, pp. 852–859.

[45] S. K. Lim, “Physical design for 3D system on package,” *IEEE Des. Test Comput.*, vol. 22, no. 6, pp. 532–539, 2005.

[46] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, “Power distribution system design methodology and capacitor selection for modern CMOS technology,” *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284–291, 1999.

[47] O. Guiller, S. Joblot, Y. Lamy, A. Farcy, E. Defay, and K. Dieng, “Through Silicon Capacitor co-integrated with TSV as an efficient 3D decoupling capacitor solution for power management on silicon interposer,” in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 1296–1302.

[48] X. Mi and S. Ueda, “Integrated Passives for High-Frequency Applications,” in *Advanced Microwave Circuits and Systems*, InTech, 2003, pp. 249–291.

[49] C. Kittel and H. Y. Fan, *Introduction to Solid State Physics*, vol. 25, no. 5. Wiley New York, 1957.

[50] R. Ulrich, L. Schaper, D. Nelms, and M. Leftwich, “Comparison of

Paraelectric and Ferroelectric Materials for Applications as Dielectrics in Thin Film Integrated Capacitors," *Int. J. Microcircuits Electron. Packag.*, vol. 23, no. 2, pp. 172–181, 2000.

[51] W. T. Liu *et al.*, "Low-Temperature Fabrication of Amorphous BaTiO<inf>3</inf>Thin-Film Bypass Capacitors," *IEEE Electron Device Lett.*, vol. 14, no. 7, pp. 320–322, 1993.

[52] T. R. R. Bhattacharya, Swapan K, "Epoxy Nanocomposite Capacitors for Application as MCM-L Compatible Integral Passives," *J. Electron. Packag.*, vol. 124, no. March, pp. 1–6, 2002.

[53] T. Takken and D. Tuckerman, "Integral decoupling capacitance reduces multichip module ground bounce," in *Multi-Chip Module Conference, 1993. MCMC-93, Proceedings., 1993 IEEE*, 1993, pp. 79–84.

[54] Z. Nami, O. Misman, A. Erbil, and G. S. May, "Effect of growth parameters on TiO$_2$ thin films deposited using MOCVD," *J. Cryst. Growth*, vol. 179, no. 3–4, pp. 522–538, 1997.

[55] H. A. Pohl, "Superdielectrics Polymers," *IEEE Trans. Electr. Insul.*, vol. EI-21, no. 5, pp. 683–692, 1986.

[56] H. S. Nalwa, *Ferroelectric Polymers: Chemistry: Physics, and Applications*. CRC Press, 1995.

[57] S. K. Bhattacharya and R. R. Tummala, "Next generation integral passives: Materials, processes, and integration of resistors and capacitors on PWB substrates," *J. Mater. Sci. Mater. Electron.*, vol. 11, no. 3, pp. 253–268, 2000.

[58] M. A. Alam, M. H. Azarian, and M. G. Pecht, "Embedded capacitors in printed wiring board: A technological review," *J. Electron. Mater.*, vol. 41, no. 8, pp. 2286–2303, Aug. 2012.

[59] T. Bertaud *et al.*, "Frequency Effect on Voltage Linearity of ZrO 2 -Based RF Metal – Insulator – Metal Capacitors," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 114–116, 2010.

[60] B.-Y. Tsui, H.-H. Hsu, and C.-H. Cheng, “High-Performance Metal Insulator Metal Capacitors With \hbox {HfTiO}/\hbox {Y}_{2}\hbox {O}_{3} Stacked Dielectric,” *Electron Device Lett. IEEE*, vol. 31, no. 8, pp. 875–877, 2010.

[61] S. Mondal, S. J. Shih, F. H. Chen, and T. M. Pan, “Structural and electrical characteristics of Lu2O3dielectric embedded MIM capacitors for analog IC applications,” *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1750–1756, 2012.

[62] O. Khaldi, F. Jomni, P. Gonon, C. Mannequin, and B. Yangui, “Investigation of electrical properties of HfO2 metal-insulator-metal (MIM) devices,” *Appl. Phys. A Mater. Sci. Process.*, vol. 116, no. 4, pp. 1647–1653, 2014.

[63] C. Mahata *et al.*, “High performance TaYO<inf>x</inf>-based MIM capacitors,” *Microelectron. Eng.*, vol. 86, no. 11, pp. 2180–2186, 2009.

[64] C. H. Ng, C.-S. Ho, S.-F. S. Chu, and S.-C. Sun, “MIM Capacitor Integration for Mixed-Signal/RF Applications,” *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1399–1409, Jul. 2005.

[65] J. H. Klootwijk *et al.*, “Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon,” *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 740–742, Jul. 2008.

[66] P. Banerjee, I. Perez, L. Henn-Lecordier, S. B. Lee, and G. W. Rubloff, “Nanotubular metal–insulator–metal capacitor arrays for energy storage,” *Nat. Nanotechnol.*, vol. 4, no. 5, pp. 292–296, May 2009.

[67] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, “High-density MIM capacitors using Al 2 O 3 and AlTiO x dielectrics,” *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 185–187, 2002.

[68] H. Hu, C. Zhu, Y. F. Lu, M. F. Li, B. J. Cho, and W. K. Choi, “A high performance MIM capacitor using HfO 2 dielectrics,” *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 514–516, 2002.

[69] X. Yu *et al.*, “A high-density MIM capacitor (13 fF/μm/sup 2/) using ALD HfO 2 dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 63–65, 2003.

[70] S. J. Kim *et al.*, “Improvement of voltage linearity in high-/spl kappa/MIM capacitors using HfO/sub 2/-SiO/sub 2/stacked dielectric,” *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 538–540, 2004.

[71] H. Hu *et al.*, “MIM capacitors using atomic-layer-deposited high-/spl kappa/(HfO/sub 2/)/sub 1-x/(Al/sub 2/O/sub 3/)/sub x/dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 60–62, 2003.

[72] K. C. Chiang *et al.*, “Very high-density (23 fF//spl mu/m/sup 2/) RF MIM capacitors using high-/spl kappa/TaTiO as the dielectric,” *IEEE Electron device Lett.*, vol. 26, no. 10, pp. 728–730, 2005.

[73] K.-H. Allers, “Prediction of dielectric reliability from I–V characteristics: Poole–Frenkel conduction mechanism leading to√ E model for silicon nitride MIM capacitor,” *Microelectron. Reliab.*, vol. 44, no. 3, pp. 411–423, 2004.

[74] P. Zurcher *et al.*, “Integration of thin film MIM capacitors and resistors into copper metallization based RF-CMOS and Bi-CMOS technologies,” in *Electron Devices Meeting, 2000. IEDM’00. Technical Digest. International*, 2000, pp. 153–156.

Chapter 3 Design and Modeling of the Three-Dimensional Embedded Capacitor

3.1 Introduction

In this chapter, we introduce a new type of on-chip integrated capacitor, called a “three-dimensional (3-D) embedded capacitor,” to meet the ever-increasing demand of on-chip capacitance. Firstly, the proposed structure of the 3-D embedded capacitor is presented. This new type of 3-D embedded capacitor leverages on the existing through-silicon vias (TSVs) to enhance the capacitance density greatly. Secondly, various design options and physical design parameters are discussed for 3-D embedded capacitors for different applications. The design of test vehicles is also provided to enable prototype fabrication and electrical characterization of 3-D embedded capacitors in the next two chapters. Next, an electrical modelling of a 3-D embedded capacitor is derived based on the proposed structure using the analytical method. It is modified from a coaxial capacitance model to predict the capacitance and the capacitance density of the 3-D embedded capacitor. Finally, two models are built in the COMSOL Multiphysics program, using finite element analysis (FEA), to simulate the thermomechanical stress between TSV, the 3-D embedded capacitor, and the Si substrate and ensure their structural integrity.

3.2 Proposed "Three-dimensional Embedded Capacitor"

In recent years, there has been considerable interest in the integration of passive devices into electronic packages. The integration approach brings these benefits:

- reduced system mass, volume, and footprint.
- improved electrical performance.
- increased design flexibility.
- improved reliability.
- reduced unit cost [1]–[4].

Among integrated passive devices (IPDs), the integrated capacitor is one of the most critical components due to its wide applications in integrated circuits (ICs) and systems. For example, an integrated capacitor can be used to improve the power integrity of the power distribution network (PDN) because of its charge storage capability [4], [5]. However, its significant consumption of premium silicon area is a major drawback [6].

Several approaches have been proposed to mitigate the area penalty by improving the capacitance density. They can be classified into two major categories: material and structure. In the first category, many high-κ dielectric materials have been extensively studied to replace conventional SiO_2 [7]. Some extra effort was invested to optimize the trade-off between the dielectric constant and the bandgap for minimization of the leakage current [8], [9]. In the second major category, the total surface area of capacitors can be expanded by utilizing the Z direction [10]–[12]. For example, trench capacitors make good use of the depth of the substrate and achieve an extremely high capacitance density [13], [14]. Additionally, heterogenous integration enables the processing of capacitors in a separated die so that they do not have to compete with transistors for surface areas [15]–[18]. Nevertheless, with all available current technologies, the size of capacitors is still a few times greater than that of the logic circuits in many capacitance-hungry applications such as integrated voltage regulators (IVRs) [19]. Even with the most advanced technology, most of the die area is occupied by deep trench capacitors as shown in Figure 3.1 [20]. This issue becomes more challenging as we enter the era of three-dimensional integrated circuits

(3-D ICs), because more dies are being stacked within a single IC package and the demand for capacitance increases explosively [21], [22]. Therefore, a large surface area will be used to realize the desired high capacitance.

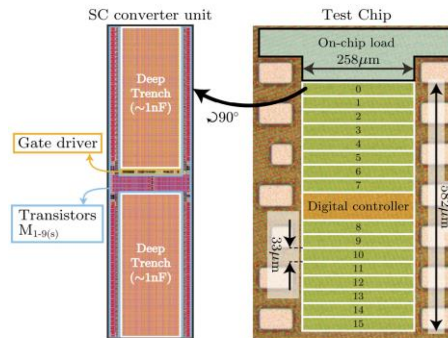


Figure 3.1: The chip micrograph of a switched-capacitor integrated voltage regulator [20].

However, 3-D IC integration provides not only challenges but also opportunities. In 3-D ICs, through-silicon-vias (TSVs) are electrical interconnects for vertical chip stacks [23]. The trenches of TSVs provide ideal locations to host the integrated trench capacitor due to their structural similarity. Figure 3.2 shows that both a TSV and a MIM trench capacitor reside in the substrate and share a cylindrical shape.

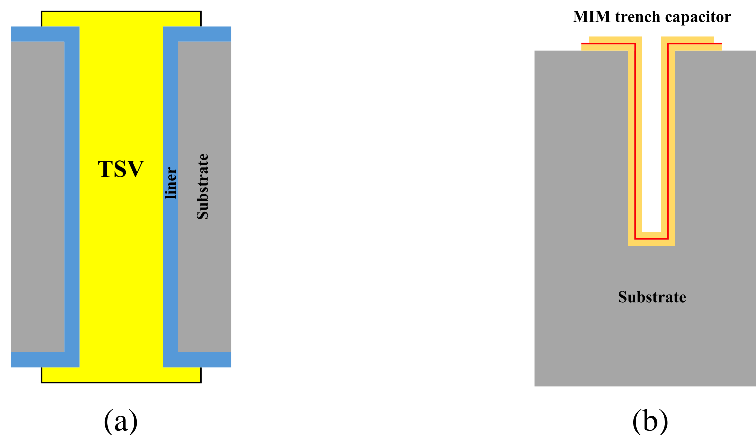


Figure 3.2: Structure similarity between (a) TSV and (b) MIM trench capacitor.

Therefore, we propose a new method of implementing integrated capacitors to improve the capacitance density further. Metal-insulator-metal (MIM) layers can be embedded into the trenches of TSVs prior to copper filling. The name "3-D embedded capacitor" is coined, because it utilizes the third dimension of the substrate and the capacitor is embedded in the trench of the TSV. In this way, the hollow space in the middle of trench capacitors can be occupied by useful TSVs instead of by dummy insulating filling material. Consequently, the capacitance density of a 3-D embedded capacitor is greatly enhanced compared with that of a conventional trench capacitor. Figure 3.3 shows the difference between conventional stand-alone trench capacitors with TSVs and 3-D embedded capacitors with TSVs. The top surface area in the middle of the substrate is freed up in Figure 3.3(b), as the integrated capacitors are implemented in the trenches of TSVs. As the thicknesses of the capacitor layers (hundreds of nanometers) are much thinner than the TSV diameter (tens of micrometers), negligible change in the electrical performance of the TSV is expected.

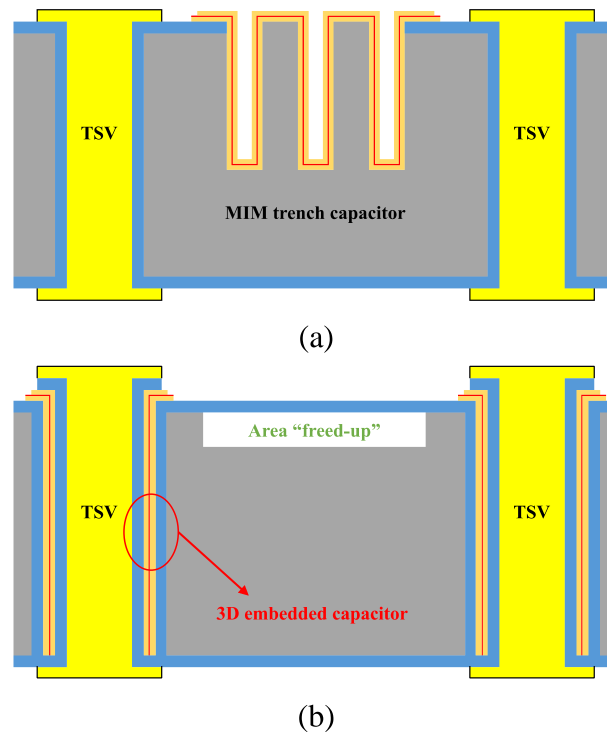


Figure 3.3: (a) Conventional stand-alone MIM trench capacitors. (b) 3-D embedded capacitors in TSVs. The top surface area is thus freed up.

3.3 Design of Three-Dimensional Embedded Capacitor

Two types of 3-D embedded capacitors have been designed for different applications as illustrated in Figure 3.4. The variation takes place in the choice of capacitor electrode deposition methods: the left one with the atomic layer deposition (ALD) process is suitable for high-end applications, whereas the right one with the sputtering process is suitable for low-cost applications. For the ALD type, perfect step coverage can be realized for both top and bottom electrodes, which maximizes the effective surface area of capacitor and prevents any possible increment of parasitic resistance caused by layer thinning at the bottom. The sputtering type can be made with a much lower cost because of two reasons: (1) the cost of electrode deposition by sputtering is greatly reduced compared to that of ALD, and (2) no extra insulation step for electrodes is needed after the back-grinding process, since no electrode is exposed due to the sputtering's non-ideal step coverage.

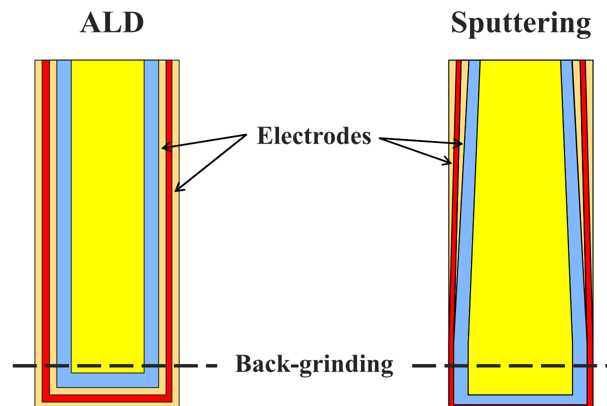


Figure 3.4: Two types of 3-D embedded capacitors. The left one with the ALD process is suitable for high-end applications, whereas the right one with the sputtering process is suitable for low-cost applications.

A top view is illustrated in Figure 3.5, which can be used to represent both types of 3-D embedded capacitors. The conductive core of the TSV is in the center with a dielectric liner surrounding it. The MIM layers are wrapped around the TSV liner and separated from the silicon substrate by an insulation layer. The physical design parameters of the two types of 3-D embedded capacitors are listed in Table

3.1. The parameters are set in accordance with the consideration of both the industrial standards of TSVs and Nanyang NanoFabrication (N2FC) fabrication capabilities at university. For a typical TSV, the trench radius ranges from 1 to 25 µm; the trench depth ranges from 50 to 100 µm. In this study, we set the trench radius to be 5, 10, 15, 20, and 25 µm and the trench depth to be 60 µm (a target for the trench with a radius of 25 µm). A typical thickness of 200 nm is also adopted for the TSV liner. In addition, the thicknesses of the MIM layers are chosen to optimize the electrical performance of 3-D embedded capacitor. For the ALD type, the thickness of electrodes is set to be 50 nm; for the sputtering type, the thickness of electrodes is set to be 400 nm to ensure more surface area can be covered at the bottom of the trench. TiN and Al_2O_3 (κ=9) are chosen as the electrode and dielectric materials, respectively.

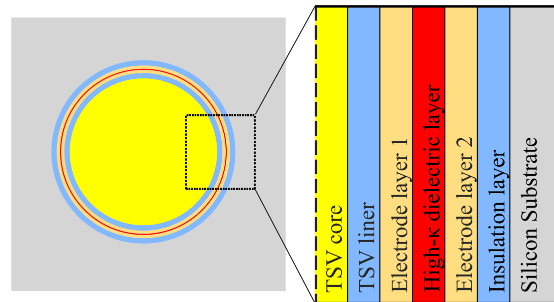


Figure 3.5: Top view of a TSV with a 3-D embedded capacitor.

Table 3.1: Physical design parameters of 3-D embedded capacitors.

Parameter	Symbol	Value	
		ALD	Sputtering
Radius of the trench (μm)	R_{trench}	5, 10, 15, 20, 25	
Depth of the trench (μm)	H	60	
Thickness of the TSV liner (nm)	T_{liner}	200	
Thickness of electrode layer1 (nm)	T_{el1}	50	400
Thickness of the high-κ dielectric layer (nm)	$T_{high-\kappa}$	10	
Thickness of electrode layer2 (nm)	T_{el2}	50	400
Thickness of the insulation layer (nm)	T_{ins}	10	

Two test vehicle structures (a de-embedded structure and an embedded structure) have been designed for the extraction of capacitance. Their cross-sectional view is illustrated in Figure 3.6(a). The de-embedded structure contains one planar MIM capacitor to be used as a benchmark. The embedded structure contains one planar MIM capacitor and a 3×3 array (9 units) of 3-D embedded capacitors. Both de-embedded and embedded structures were designed to occupy the same planar area, so that the difference of capacitance extracted from them equals the net capacitance contributed from 9 units of 3-D embedded capacitors. Furthermore, the planar area size of both de-embedded and embedded structures varies from 200×100, 400×200, 600×300, 800×400 to 1000×500 μm^2, so that the trenches with a radius ranging from 5, 10, 15, 20 to 25 μm can be accommodated, respectively. The design is shown in Figure 3.6(b).

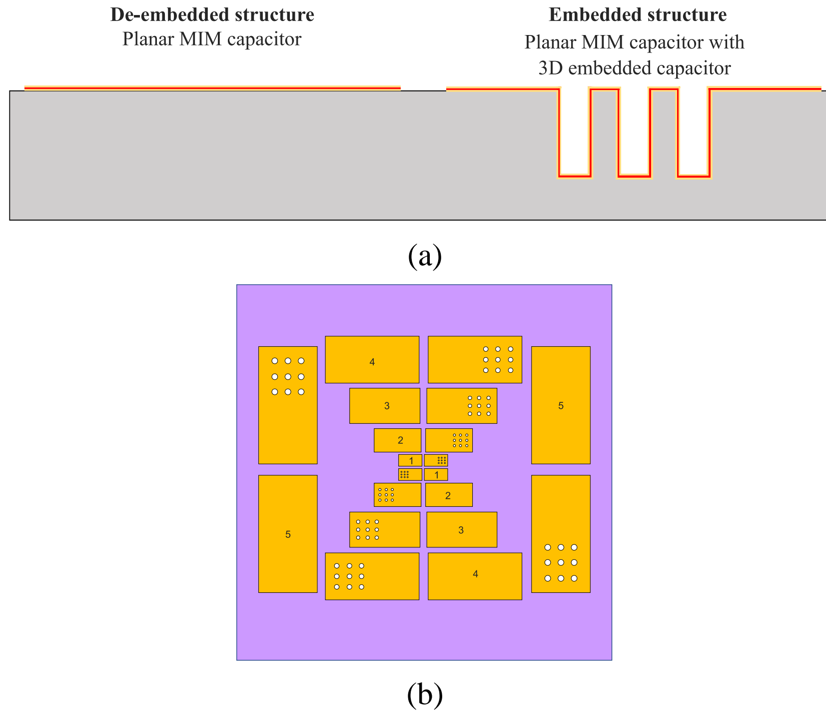


Figure 3.6: Design of test vehicles for 3-D embedded capacitors. (a) Cross-sectional view of a de-embedded structure and an embedded structure. (b) Top view of test vehicles with five scalable geometries on the left and the same number duplicated on the right.

For simplicity, only the ALD type 3-D embedded capacitor will be used as a workout example for the following sections in this chapter, because its excellent step coverage of electrodes makes it much easier for analytical modeling and the finite element method simulation. However, both ALD and sputtering types test vehicles will be demonstrated in Chapters 4 and 5 for their fabrication and electrical characterization parts, respectively.

3.4 Electrical Modeling of Three-Dimensional Embedded Capacitor Using the Analytical Method

In this section, a first-order analytical model of a 3-D embedded capacitor is constructed. The capacitance density is the ratio between the capacitance and its occupied planar area. Next, a more generalized model is derived for a 3-D embedded capacitor with more electrode and dielectric layers, and the results are compared to state-of-the-art trench capacitor technology. Lastly, the impact of various 3-D embedded capacitors on the electrical properties of the TSV is estimated.

The capacitance is derived based on the coaxial capacitance model [24]. Therefore, according to the symbols defined in Table 3.1, the cylindrical capacitance of a 3-D embedded capacitor is:

$$\text{Capacitance} = \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{trench} - T_{ins} - T_{el2}}{R_{trench} - T_{ins} - T_{el2} - T_{high-\kappa}}\right)} \tag{3.1}$$

The occupied planar area of a 3-D embedded capacitor is only the narrow section between the TSV line and the rim of the trench:

$$\text{Area} = \pi \times \left[{R_{trench}}^2 - (R_{trench} - T_{ins} - T_{el2} - T_{high-\kappa} - T_{el1})^2\right] \tag{3.2}$$

The capacitance density is defined as the ratio between the capacitance and the occupied planar area:

$$\text{Capacitance Density} = \text{Capaictance/Area} \tag{3.3}$$

With the physical design parameters in Table 3.1, the values calculated based on the analytical equations are listed for capacitance, area, and capacitance density for trenches with a different radius (capacitance density unit in nF/mm^2 for the ease of comparison with those of other capacitor technologies). The results show that the capacitance density of each 3-D embedded capacitor stays around 3980 nF/mm^2, even though the trench radius changes from 5 to 25 μm. Compared with the parasitic capacitance of TSV, 3-D embedded capacitor provides 45 × higher capacitance. The

enhancement of capacitance is two-folded: the dielectric thickness is 20 times thinner (10 nm vs. 200 nm); the dielectric constant is 2.25 times higher (9 vs. 4).

Table 3.2: Analytical results of capacitance, area, and capacitance density for 3-D embedded capacitors.

Trench Radius (μm)	Capacitance (pF)	Area (μm^2)	Capacitance Density (nF/mm^2)
5	14.8	3.7	3978.5
10	29.8	7.5	3980.5
15	44.8	11.3	3981.2
20	59.8	15.0	3981.5
25	74.8	18.8	3981.7

Add in the change of dielectric thickness as well (plots)

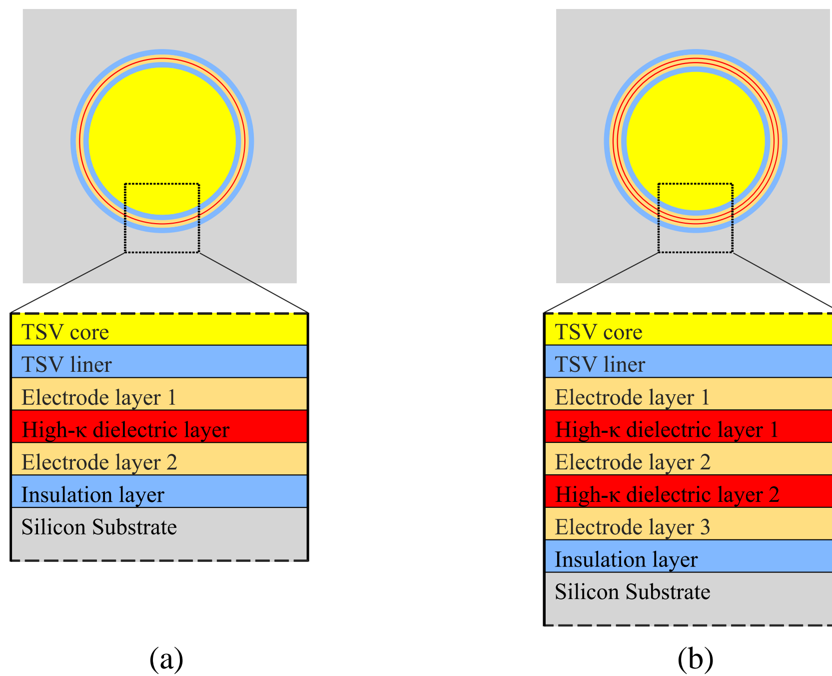


Figure 3.7: Top views with layer breakdown of (a) a TSV with a MIM 3-D embedded capacitor and (b) a TSV with a MIMIM 3-D embedded capacitor.

The most basic configuration of a 3-D embedded capacitor is illustrated in Figure 3.7(a), whereas a more advanced configuration is illustrated in Figure 3.7(b) to show that an electrode and dielectric layers can be inserted to form an MIMIM 3-D embedded capacitor. Figure 3.7 shows the top views of both configurations with a detailed layer breakdown. The analytical model needs to be generalized for multi-MIM 3-D embedded capacitors, because more electrode and dielectric layers can be added alternately to further enhance the capacitance of 3-D embedded capacitor. Based on the derivation of the configuration in Figure 3.7(b), one should be able to generalize the model to predict the capacitance density of all other 3-D embedded capacitors with more electrode and dielectric layers. The physical design parameters are defined and listed in Table 3.3. The analytical equations for capacitance and area are modified accordingly:

$$\text{Capacitance} = C_{MIM1} + C_{MIM2}$$

$$= \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{trench} - T_{ins} - T_{el3} - T_{high-\kappa 2} - T_{el2}}{R_{trench} - T_{ins} - T_{el3} - T_{high-\kappa 2} - T_{el2} - T_{high-\kappa 1}}\right)} + \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{trench} - T_{ins} - T_{el3}}{R_{trench} - T_{ins} - T_{el3} - T_{high-\kappa 2}}\right)} \quad (3.4)$$

$$\text{Area} = \pi \times \left[R_{trench}{}^2 - (R_{trench} - T_{ins} - T_{el3} - T_{high-\kappa 2} - T_{el2} - T_{high-\kappa 1} - T_{\mathrm{el}1})^2\right] \quad (3.5)$$

Table 3.3: Physical design parameters of MIMIM 3-D embedded capacitors.

Parameter	Symbol
Capacitance of MIM structure1	C_{MIM1}
Capacitance of MIM structure2	C_{MIM2}
Thickness of the insulation layer	T_{ins}
Thickness of electrode layer1	T_{el1}
Thickness of high-κ dielectric layer1	$T_{high-\kappa1}$
Thickness of electrode layer2	T_{el2}
Thickness of high-κ dielectric layer2	$T_{high-\kappa2}$
Thickness of electrode layer3	T_{el3}
Thickness of the TSV liner	T_{liner}
Radius of the trench	R_{trench}
Depth of the trench	H
High-κ dielectric constant	$\varepsilon_{high-\kappa}$

The generalized analytical equations now enable a fair comparison of the capacitance density of the 3-D embedded capacitor and that of a state-of-the-art trench capacitor. For example, an MIMIM trench capacitor can provide 440.0 nF/mm^2; whereas a 3-D embedded capacitor with the same physical design parameters can provide 5,621.8 nF/mm^2, which is ~13× higher [13].

$\left(T_{ins} = 5\text{ nm}, T_{el1} = 20\text{ nm}, T_{high-\kappa1} = 10\text{ nm}, T_{el2} = 20\text{ nm}, T_{high-\kappa2} = 10\text{ nm}, T_{el3} = 20\text{ nm}, R_{trench} = 50\ \mu\text{m}, H = 30\ \mu\text{m}, \varepsilon_{high-\kappa} = 9\right)$

The significant capacitance improvement can be easily understood by reviewing a cross-sectional image of a MIMIM trench capacitor in Figure 3.8. The picture shows that most of the space in the middle of the MIMIM trench capacitor is occupied by dummy filling material: making the planar surface area much larger than the actual effective planar area. Replacing filling materials with a TSV makes the footprint of the MIMIM layers much smaller: therefore, making the capacitance density of the capacitor much higher.

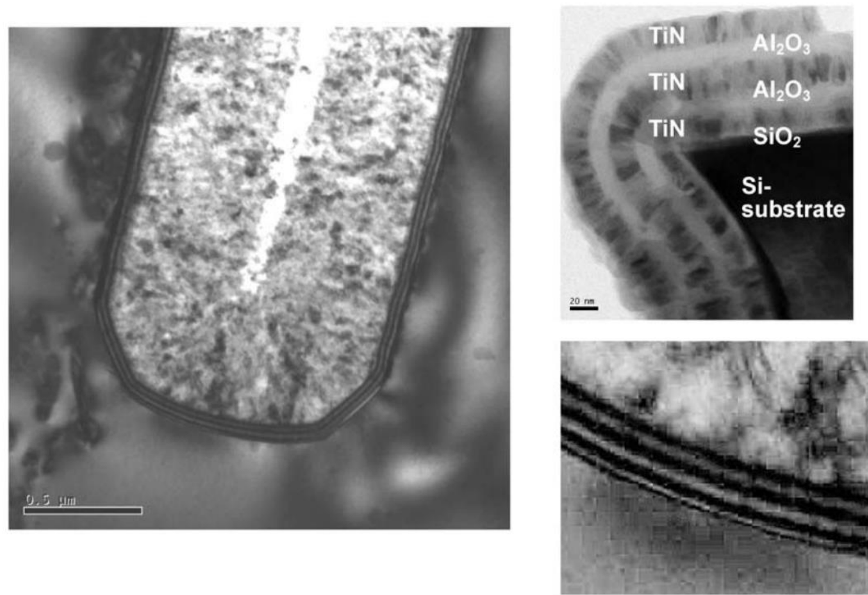


Figure 3.8: Bright-field cross-sectional TEM images of the MIM trench capacitor, in which most of the space in the middle is occupied by filling material [13].

Lastly, the impact on the electrical properties (i.e., resistance and capacitance) of the TSV due to the insertion of the 3-D embedded capacitor is estimated. The resistance is inversely proportional to the cross-sectional conductive area of the TSV:

$$\text{TSV resistance} = \rho_{copper} \times H / \left(\pi \times {R_{core}}^2\right) \tag{3.6}$$

where $R_{core} = R_{trench} - T_{ins} - T_{el2} - T_{high-\kappa 2} - T_{el2} - T_{high-\kappa 1} - T_{el1}$. The capacitance (in the accumulation state) is related to the circumference of the TSV and the liner thickness:

$$\text{TSV capacitance} = \frac{2\pi \times \varepsilon_0 \times \varepsilon_{SiO2} \times H}{\ln\left(\frac{R_{core} + T_{liner}}{R_{core}}\right)} \tag{3.7}$$

The estimation is made based on the physical design parameters of 3-D embedded capacitors introduced in Section 3.3. The results are listed in Table 3.4. They reveal that the change of both TSV resistance and capacitance due to the insertion of the 3-D embedded capacitor is insignificant (variation < 5%). The reason for this is that the total thickness of the MIM layers is much smaller compared with the trench radius (i.e., ~100 nm vs. ~10 µm).

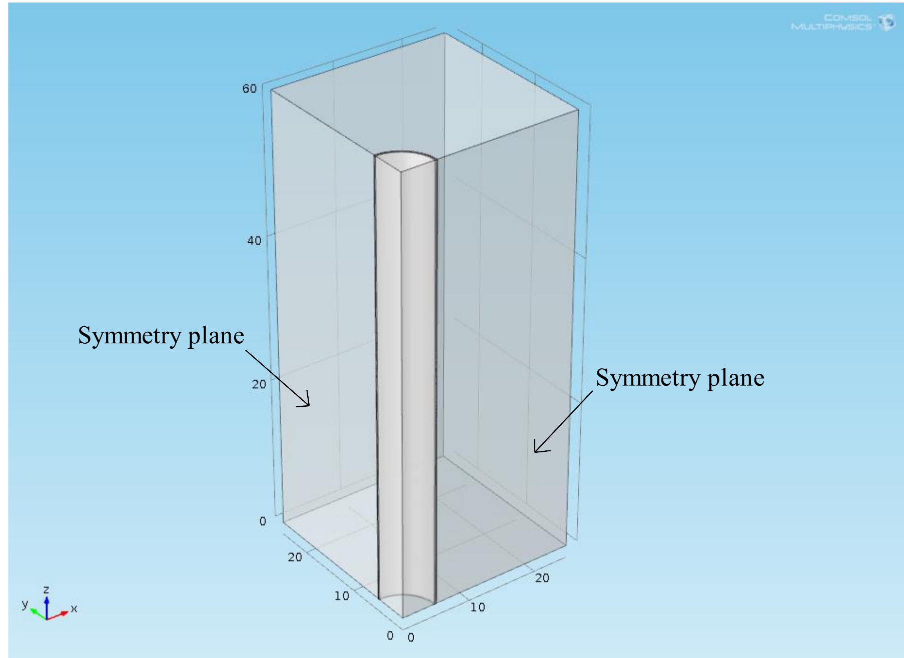
Table 3.4: Impact on the electrical properties of TSVs.

Trench Radius (µm)	Resistance Variation (%)	Capacitance Variation (%)
5	-4.9	-2.5
10	-2.4	-1.2
15	-1.6	-0.8
20	-1.2	-0.6
25	-1.0	-0.5

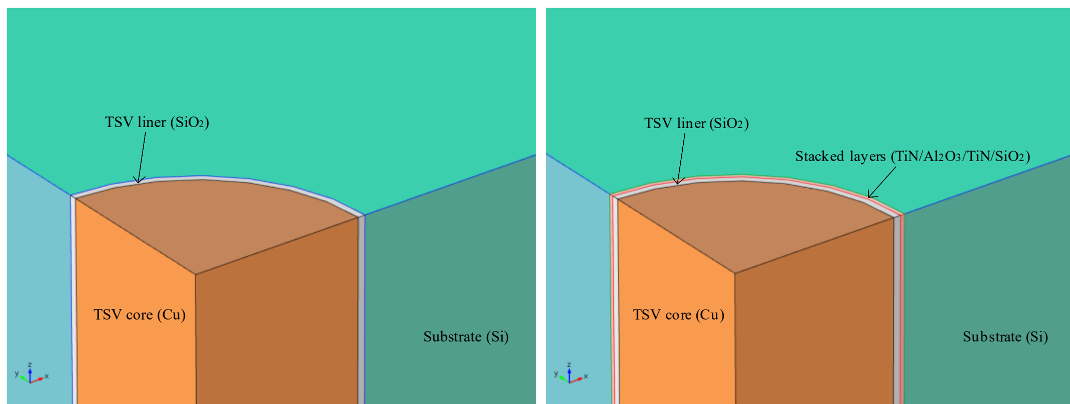
3.5 Thermo-Mechanical Simulation of Three-Dimensional Embedded Capacitor Using Finite Element Analysis

Extensive studies have been carried out to investigate the thermomechanical stress between the TSV and the surrounding Si substrate [25]–[29]. Generated during the annealing and cooling steps in the fabrication processes, the stress is essentially due to the coefficient of the thermal expansion (CTE) mismatch of Cu, SiO2, and Si materials. However, the thermomechanical stress has not yet been studied when a 3-D embedded capacitor is inserted between the TSV and the Si substrate. Thus, two FEA models have been built in the COMSOL Multiphysics program to estimate the thermomechanical stress and ensure the structural integrity of the TSV, 3-D embedded capacitor, and Si substrate. The first model is the TSV + Si substrate, whereas the second model is the TSV + 3-D embedded capacitor + Si substrate for comparison. In this section, the structures of models are introduced firstly, and then the properties of materials and the thermal loading conduction are described. Lastly, the simulation results are presented and discussed.

The physical design parameters of TSVs and 3-D embedded capacitors were shown in Table 3.1. Due to the symmetry of the structure, only a quarter of the complete structures need to be constructed for both models. In this case, a trench with a radius of 5 μm was chosen as an example as shown in Figure 3.9(a). The difference between the two models is illustrated. Apart from the TSV core (Cu), the TSV liner (SiO_2), and the substrate (Si) in Figure 3.9(b), a few stacked layers are added as a 3-D embedded capacitor in Figure 3.9(c). The stacked layers ($TiN/Al_2O_3/TiN/SiO_2$) are considered one whole TiN layer, because 10 nm thick layers are too thin to be meshed properly for FEA simulation and the thickness of two TiN layers accounts for 83.3% of the total thickness of stacked layers (i.e., 100 nm/120 nm). Therefore, it is assumed that this simplification has an insignificant impact on the final simulation results.



(a)



(b) (c)

Figure 3.9: (a) A quarter of the FEA model with two symmetry planes. (b) The first model: TSV + Si substrate, and (c) the second model: TSV + 3-D embedded capacitor + Si substrate. The stacked layers (TiN/Al_2O_3/TiN/SiO_2) are considered as only a whole TiN layer with a thickness of 120 nm.

The properties of materials used in FEA simulations are described in Table 3.5. These materials have been assigned to different parts in the FEA model: Cu is the TSV core material; SiO_2 is the TSV liner material; TiN is the stacked layers material; and Si is the substrate material. It is worth pointing out that the CTEs of the two major components Cu and Si are significantly different: 17.0 vs. 2.3 ppm/K. It

can be predicted that the stress level will be considerably high as the thermal loading increases. In addition, all materials have their constant values for Young's modulus except Si, because Si is a single crystalline material, which responds to stress differently depending on the orientation [30]. The anisotropic property of the Si substrate is given in the stiffness matrix:

$$\begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} = \begin{bmatrix} 194.5 & 35.7 & 64.1 & 0 & 0 & 0 \\ 35.7 & 194.5 & 64.1 & 0 & 0 & 0 \\ 64.1 & 64.1 & 165.7 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.6 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.6 & 0 \\ 0 & 0 & 0 & 0 & 0 & 50.9 \end{bmatrix} \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} \tag{3.8}$$

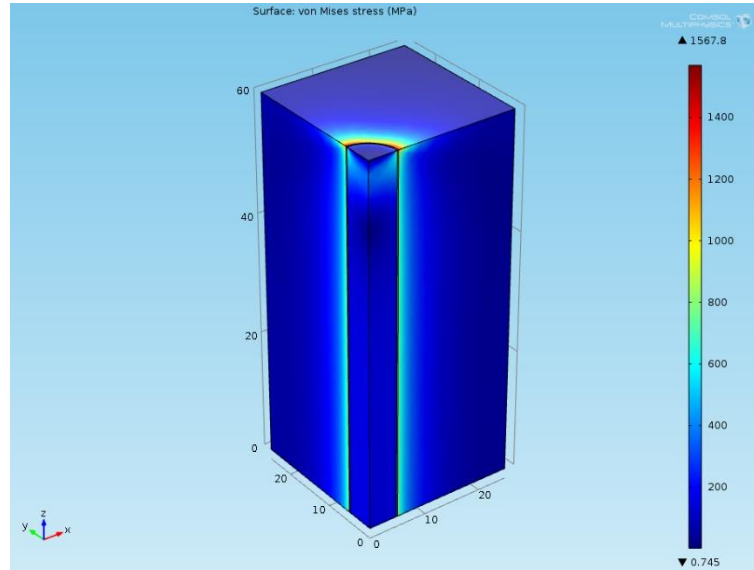
For the typical via-middle process, fabricated TSVs have to undertake a thermal budget from the back-end-of-line process, which is usually 400 °C [31]. So a thermal annealing step at 400 °C is proposed to be carried out after the fabrication of the TSV [29]. In this way, Cu grain growth takes place in advance to avoid the hysteretic behavior later. After multiple cycles of high temperature annealing, the stress-free reference temperature has been confirmed to be 280 °C for the TSV and Si substrate [32]. Therefore, in this study, a thermal loading of -250 °C was applied to both FEA models to mimic the cooling-induced thermomechanical stress at room temperature.

Table 3.5: Physical properties of materials used in the FEA simulation.

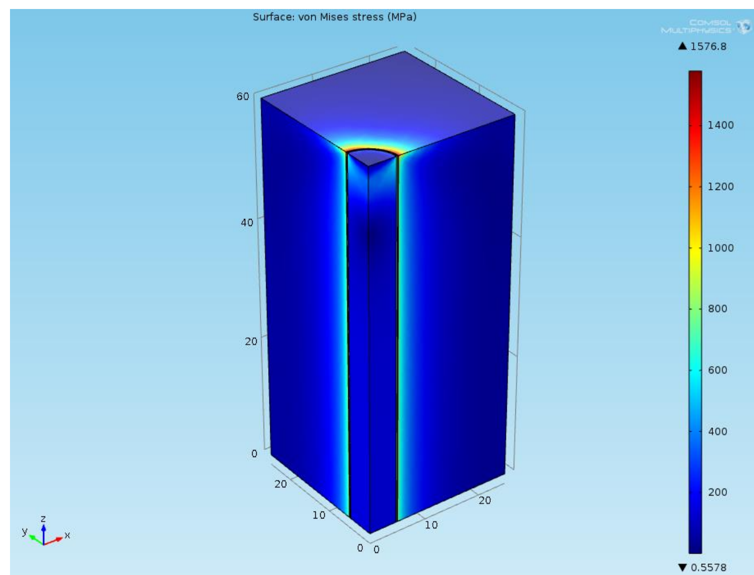
Materials	CTE (ppm/K)	Young's Modulus (GPa)	Poisson Ratio
Cu	17.0	110	0.35
SiO_2	0.5	71	0.16
Si	2.3	anisotropic	0.28
TiN	9.4	500	0.25

The simulation results of von Mises stress in both models are presented in Figure 3.10(a) and (b), respectively. The highest von Mises stress resides on the top parts of the models. For comparison, the highest von Mises stress increases from 1567.8 to 1576.8 MPa, when a 3-D embedded capacitor is included. More zoom-in pictures of the top and bottom parts of the two models are shown in Figure 3.11. It can be seen that the stress accumulates around the top surface of the SiO_2 TSV liner and surrounding Si substrate, and the stress level of the rest also happens near the SiO_2 TSV liner but below 1000 MPa. Then two directions, [110] and [100] shown in Figure 3.12, are assigned on the top surface to study the orientation dependent stress levels in the anisotropic Si substrate. In Figure 3.13, one-dimensional plots are presented for a comparison of stress levels along different directions. Figure 3.13(a) depicts the stress along the [110] direction in the first model with the a peak stress of 1423.9 MPa; Figure 3.13(b) depicts the stress along the [100] direction in the first model with a peak stress of 1287.8 MPa; Figure 3.13(c) depicts the stress along the [110] direction in the second model with a peak stress of 1487.8 MPa; and Figure 3.13(d) depicts the stress along the [100] direction in the second model with a peak stress of 1206.0 MPa. It can be concluded that the stress along the [110] direction is higher than the stress along the [100] direction for both models. When a 3-D embedded capacitor is involved, the stress along the [110] direction increases, but the

stress along the [100] direction decreases. Lastly, other trenches with a radius from 5 to 25 μm have been simulated as well, and the results show that the peak stress level increases from 1576.8 to 2278.0 MPa as shown in Table 3.6.



(a)



(b)

Figure 3.10: Von Mises stress of (a) the first model of the TSV + Si substrate and (b) of the second model of the TSV + 3-D embedded capacitor + Si substrate.

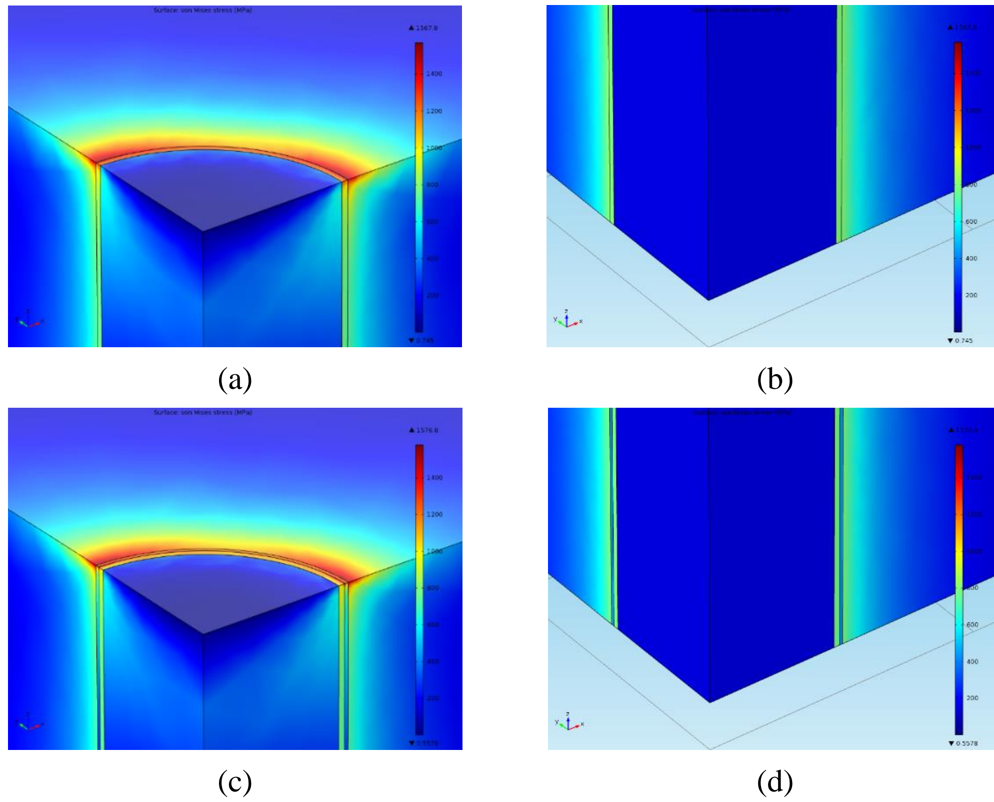


Figure 3.11: Zoom-in pictures of (a) the top of the first model, (b) the bottom of the first model, (c) the top of the second model, and (d) the bottom of the second model.

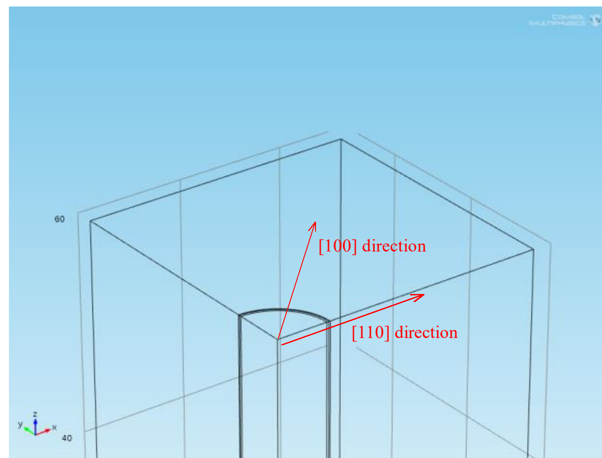


Figure 3.12: The [110] and [100] directions on the top surface.

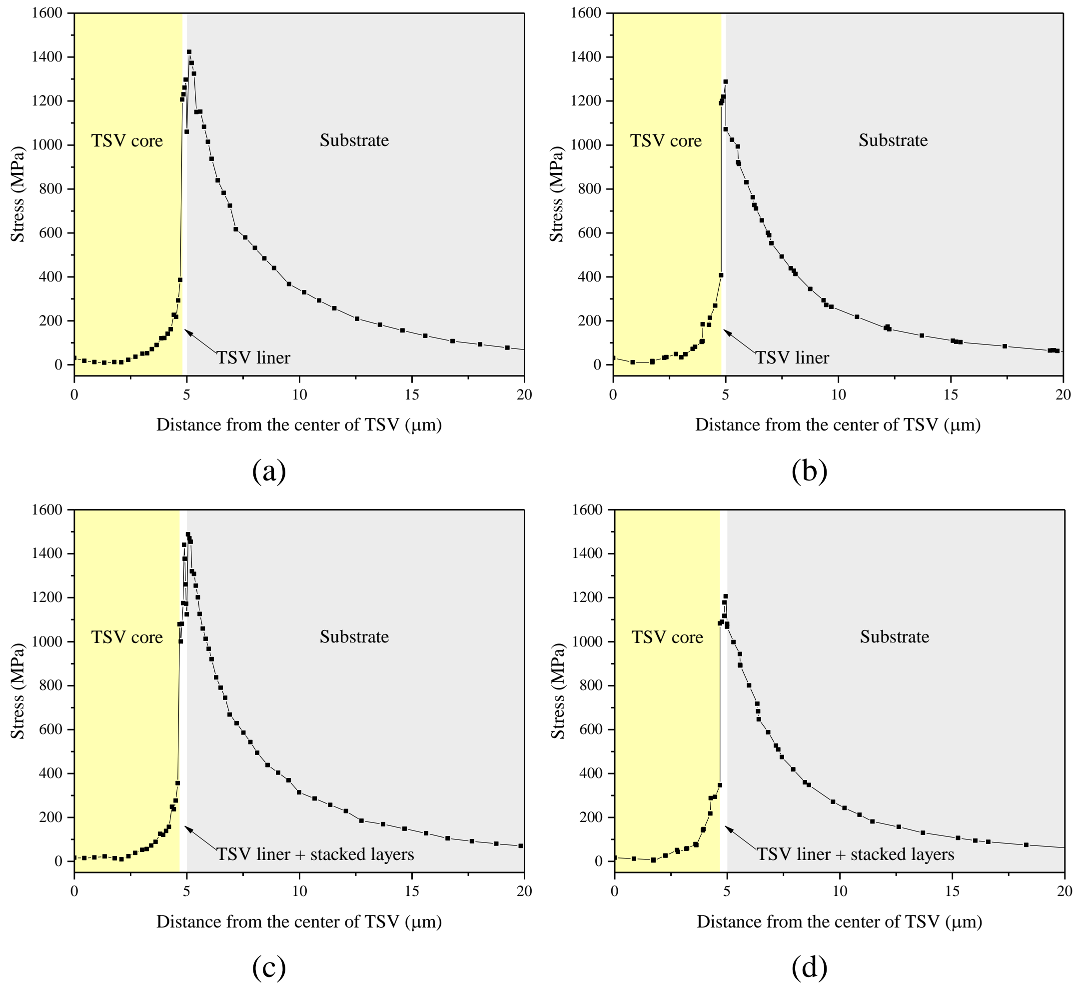


Figure 3.13: The stress level along (a) the [110] direction in the first model, (b) the [100] direction in the first model, (c) the [110] direction in the second model, and (d) the [100] direction in the second model.

Table 3.6: Von Mises stress for trenches with different radius.

Radius (μm)	Max von Mises Stress (MPa)
5	1576.8
10	1928.6
15	2160.8
20	2215.8
25	2278.0

3.6 Summary

In this chapter, we have described the proposed structure of the 3-D embedded capacitor and its benefits. Two types of 3-D embedded capacitors (ALD and sputtering) have shown their own advantages for various end-applications. Moreover, an electrical model has been derived for a 3-D embedded capacitor to predict its capacitance using the analytical method. The calculated result shows that a significant capacitance density enhancement can be achieved for this new type of capacitor compared with convention trench capacitor technologies (e.g. from 440.0 to 5621.8 nF/mm^2 by ~13 times). Furthermore, this analytical model has also been extended to fit multi-MIM layer 3-D embedded capacitors. Lastly, two FEA models have been built to estimate thermo-mechanical stress and ensure the structural integrity of the TSV, 3-D embedded capacitor, and Si substrate. One is a TSV model without a 3-D embedded capacitor, while the other is a TSV model with a 3-D embedded capacitor. The FEA simulation results show that no significant difference can be observed from these two models: the maximum von Mises stress only increases from 1567.8 to 1576.8 MPa due to the inclusion of a 3-D embedded capacitor.

References

[1] S. K. Bhattacharya and R. R. Tummala, "Next generation integral passives: Materials, processes, and integration of resistors and capacitors on PWB substrates," *J. Mater. Sci. Mater. Electron.*, vol. 11, no. 3, pp. 253–268, 2000.

[2] P. Chahal, R. R. Tummala, M. G. Allen, and G. E. White, "Electroless Ni-P/Ni-WP thin-film resistors for MCM-L based technologies," in *Electronic Components & Technology Conference, 1998. 48th IEEE*, 1998, pp. 232–239.

[3] J. Rector, J. Dougherty, V. Brown, J. Galvagni, and J. Prymak, "Integrated and integral passive components: A technology roadmap," in *Electronic Components and Technology Conference, 1997. Proceedings., 47th*, 1997, pp. 713–723.

[4] R. K. Ulrich, "Introduction," in *Integrated Passive Component Technology*, R. K. Ulrich and L. W. Schaper, Eds. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2003, pp. 1–32.

[5] H. Lee, Y.-S. Choi, E. Song, K. Choi, T. Cho, and S. Kang, "Power Delivery Network Design for 3D SIP Integrated over Silicon Interposer Platform," in *Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 1193–1198.

[6] T. Van Breussegem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY: Springer New York, 2013.

[7] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, "Alternative dielectrics to silicon dioxide for memory and logic devices," *Nature*, vol. 406, no. 6799, pp. 1032–1038, Aug. 2000.

[8] Shi-Jin Ding *et al.*, "High-performance MIM capacitor using ALD high-k HfO2-Al2O3 laminate dielectrics," *IEEE Electron Device Lett.*, vol. 24, no. 12, pp. 730–732, Dec. 2003.

[9] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "High-density MIM capacitors using Al2O3 and AlTiOx dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 185–187, Apr. 2002.

[10] M. Koyanagi, H. Sunami, N. Hashimoto, and M. Ashikawa, “Novel high density, stacked capacitor MOS RAM,” in *1978 International Electron Devices Meeting*, 1978, pp. 348–351.

[11] J. Lutzen *et al.*, “Integration of capacitor for sub-100-nm DRAM trench technology,” in *2002 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.01CH37303)*, pp. 178–179.

[12] H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, “A corrugated capacitor cell (CCC) for megabit dynamic MOS memories,” *IEEE Electron Device Lett.*, vol. 4, no. 4, pp. 90–91, Apr. 1983.

[13] J. H. Klootwijk *et al.*, “Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon,” *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 740–742, Jul. 2008.

[14] F. Roozeboom, R. Elfrink, J. Verhoeven, J. van den Meerakher, and F. Holthuysen, “High-value MOS capacitor arrays in ultradeep trenches in silicon,” *Microelectron. Eng.*, vol. 53, no. 1–4, pp. 581–584, Jun. 2000.

[15] B. Dang *et al.*, “Three-Dimensional Chip Stack With Integrated Decoupling Capacitors and Thru-Si Via Interconnects,” *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1461–1463, Dec. 2010.

[16] K. Dieng *et al.*, “Modeling and Frequency Performance Analysis of Through Silicon Capacitors in Silicon Interposers,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 7, no. 4, pp. 477–484, Apr. 2017.

[17] O. Guiller, S. Joblot, Y. Lamy, A. Farcy, E. Defay, and K. Dieng, “Through Silicon Capacitor co-integrated with TSV as an efficient 3D decoupling capacitor solution for power management on silicon interposer,” in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 1296–1302.

[18] A. Shibuya, A. Ouchi, and K. Takemura, “A Silicon Interposer with an Integrated SrTiO3 Thin Film Decoupling Capacitor and Through-Silicon Vias,” *IEEE Trans. Components Packag. Technol.*, vol. 33, no. 3, pp. 582–587, Sep.

2010.

[19] L. Chang, R. K. Montoye, B. L. Ji, A. J. Weger, K. G. Stawiasz, and R. H. Dennard, “A fully-integrated switched-capacitor 2：1 voltage converter with regulation capability and 90% efficiency at 2.3A/mm2,” in *2010 Symposium on VLSI Circuits*, 2010, pp. 55–56.

[20] T. M. Andersen *et al.*, “4.7 A sub-ns response on-chip switched-capacitor DC-DC voltage regulator delivering 3.7W/mm2 at 90% efficiency using deep-trench capacitors in 32nm SOI CMOS,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 90–91.

[21] P. Falkenstern, Y. Xie, Y. W. Chang, and Y. Wang, “Three-dimensional integrated circuits (3D IC) floorplan and power/ground network co-synthesis,” in *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC*, 2010, pp. 169–174.

[22] N. H. Khan, S. M. Alam, and S. Hassoun, “System-level comparison of power delivery design for 2D and 3D ICs,” in *IEEE International Conference on 3D System Integration*, 2009, pp. 1–7.

[23] C. S. Tan, R. J. Gutmann, and L. R. Reif, Eds., *Wafer Level 3-D ICs Process Technology*. Boston, MA: Springer US, 2008.

[24] M. N. O. Sadiku, *Elements of Electromagnetics*, 6th ed. Oxford University Press, 2015.

[25] C. Cassidy *et al.*, “Through Silicon Via Reliability,” *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 2, pp. 285–295, Jun. 2012.

[26] C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng, “A Detailed Failure Analysis Examination of the Effect of Thermal Cycling on Cu TSV Reliability,” *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 15–22, Jan. 2014.

[27] C. Zhang and L. Li, “Characterization and Design of Through-Silicon Via Arrays in Three-Dimensional ICs Based on Thermomechanical Modeling,”

IEEE Trans. Electron Devices, vol. 58, no. 2, pp. 279–287, Feb. 2011.

[28] Y. Yang *et al.*, “Through-Si-via (TSV) Keep-Out-Zone (KOZ) in SOI Photonics Interposer: A Study of the Impact of TSV-Induced Stress on Si Ring Resonators,” *IEEE Photonics J.*, vol. 5, no. 6, pp. 2700611–2700611, Dec. 2013.

[29] S.-K. Ryu *et al.*, “Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique,” *Appl. Phys. Lett.*, vol. 100, no. 4, p. 041901, Jan. 2012.

[30] M. A. Hopcroft, W. D. Nix, and T. W. Kenny, “What is the Young’s Modulus of Silicon?,” *J. Microelectromechanical Syst.*, vol. 19, no. 2, pp. 229–238, Apr. 2010.

[31] J. P. Gambino, S. A. Adderly, and J. U. Knickerbocker, “An overview of through-silicon-via technology and manufacturing challenges,” *Microelectron. Eng.*, vol. 135, pp. 73–106, Mar. 2015.

[32] S.-K. Ryu, K.-H. Lu, T. Jiang, J.-H. Im, R. Huang, and P. S. Ho, “Effect of Thermal Stresses on Carrier Mobility and Keep-Out Zone Around Through-Silicon Vias for 3-D Integration,” *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 2, pp. 255–262, Jun. 2012.

Chapter 4 Fabrication of Three-Dimensional Embedded Capacitor

4.1 Introduction

In this chapter, we start with the layout design for 6-inch wafer fabrication, which consists of three parts: (a) de-embedded and embedded structures for electrical characterization, (b) alignment marks for the second mask alignment, and (c) dummy arrays for cross-sectional sample preparation. Then the detailed process flow of the 3-D embedded capacitor is described for both the proposed structure and a modified version compatible with our limited fabrication capability. Generally, the process steps begin with trench formation followed by the deposition of stacked layers (insulation layer and metal-insulator-metal layers). They then finish with a conventional through-silicon via process. Finally, various process options are explored and evaluated in the section about process control and optimization. The emphasis is placed on trench formation, layer deposition, and electrode patterning.

4.2 Photomask Design

The photomasks of 3-D embedded capacitors are designed for prototype fabrication at Nanyang NanoFabrication Centre (N2FC). The same design is applicable to both atomic layer deposition (ALD) and sputtering type 3-D embedded capacitors.

The photomask design is suitable for 6-inch wafer fabrication. It includes three parts: (a) de-embedded and embedded structures, (b) alignment marks, and (c) dummy arrays. The completed two-layer design with annotations is shown in Figure 4.1.

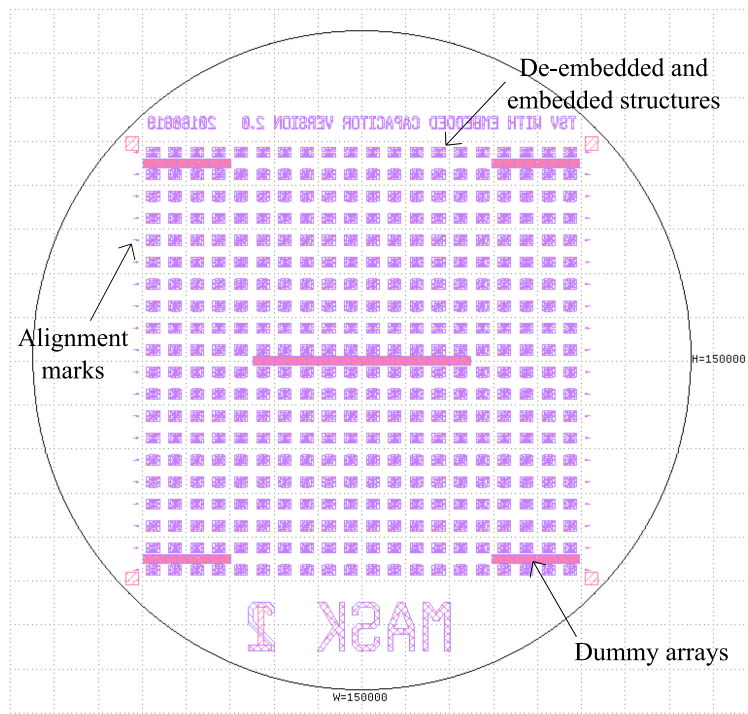


Figure 4.1: The complete photomask design includes three parts: (1) de-embedded and embedded structures, (2) alignment marks, and (3) dummy arrays.

The layout patterns of de-embedded and embedded structures are repeated over the whole wafer for 20×20 units. Each unit includes the design of test vehicles with various geometries as shown in Figure 4.2.

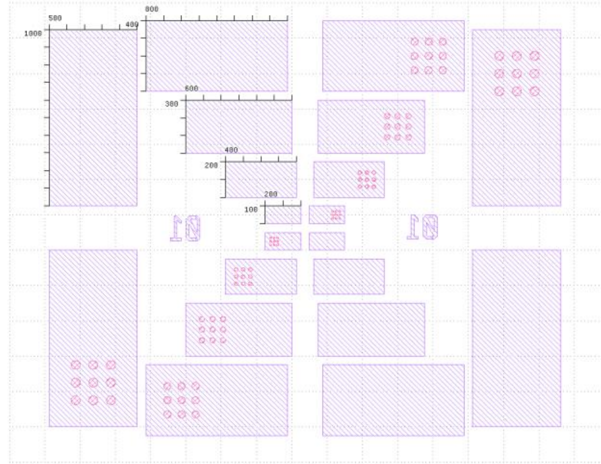


Figure 4.2: The layout design of de-embedded and embedded structures.

Alignment marks are needed for second-time wafer-mask alignment after the first few process steps. Twenty units of them form a column each on the left and right side of the main layout design. Each unit contains two cross structures for alignment and two numbers for counting. The line gap is 8 µm for the smaller cross structure and 20 µm for the larger cross structure.

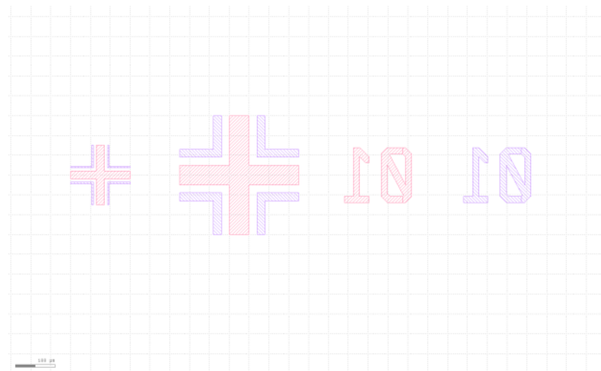


Figure 4.3: Layout design of alignment marks.

Dummy arrays, in a bar shape, reside at the four corners and the center of the wafer layout. The rows of dummy arrays are slightly misaligned so that a single cut will hit trenches that have a different radius. This makes cross-sectional sample preparation much easier compared with cutting across a single trench.

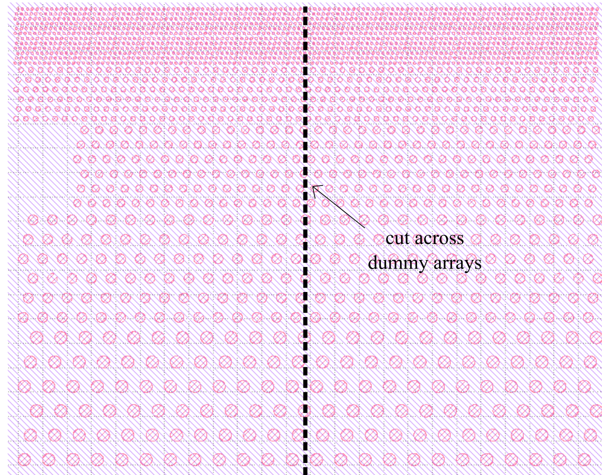


Figure 4.4: The layout design of dummy arrays.

4.3 Process Flow

The detailed proposed process flow is illustrated in Figure 3.5, which is applicable to both ALD and sputtering type 3-D embedded capacitors. A 6-inch *p*-type Si wafer with resistivity in the range of 1–10 Ω·cm is first patterned with photoresist (PR), and a trench with a depth of 60 μm is formed by deep reactive ion etching (DRIE) in steps (a)-(c). The O_2 rapid thermal process (RTP) is applied to form a 10 nm SiO_2 insulation layer on the sidewall of the trench in step (d), so that the 3-D embedded capacitor is electrically insulated from the substrate. Then, the process starts to deviate for the ALD type and sputtering type 3-D embedded capacitors. For both bottom and top electrodes, the former is deposited with 50 nm TiN by ALD, and the latter is deposited with 400 nm TiN by sputtering. In between, 10 nm Al_2O_3 is deposited by ALD as a high-κ dielectric layer, which is illustrated in steps (e)-(g). More electrode and dielectric layers can be added alternately to form a multi-layer MIM structure. The following conventional TSV process steps include the plasma-enhanced chemical vapor deposition (PECVD) of the SiO_2 liner, the sputtering of TiN as a diffusion barrier layer, the sputtering of a Cu seed layer, and the electroplating of the Cu TSV core, as shown in steps (h)-(j). Then, the top surface is planarized by chemical-mechanical polishing (CMP) and patterned by PR again in steps (k)-(l). After that, an etching step is used to remove SiO_2/TiN/Al_2O_3 layers sequentially to define the size of the top electrode in step (m). Lastly, back-grinding and CMP are applied to thin down the substrate and expose the bottom of the TSV for backside processing in step (n).

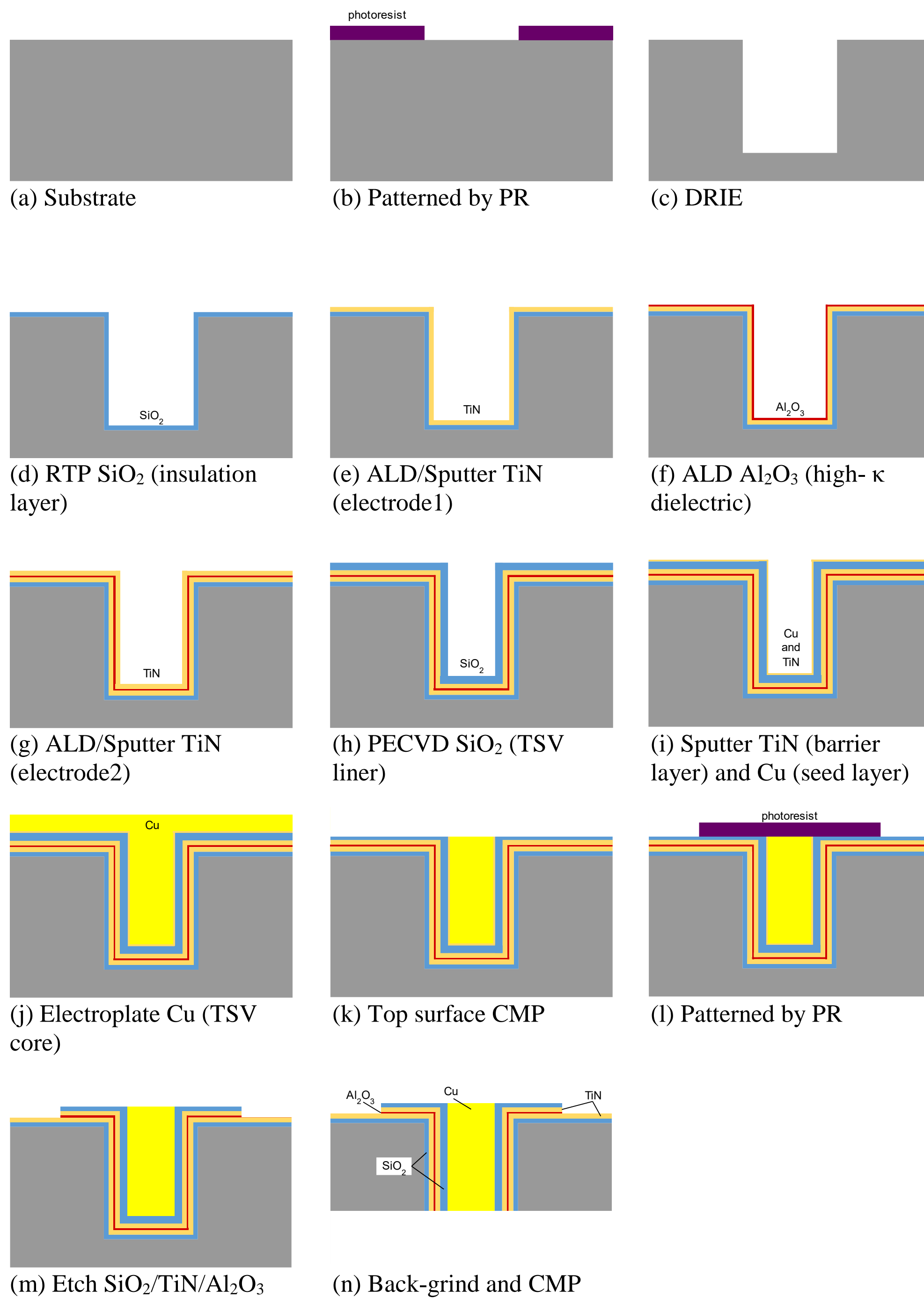
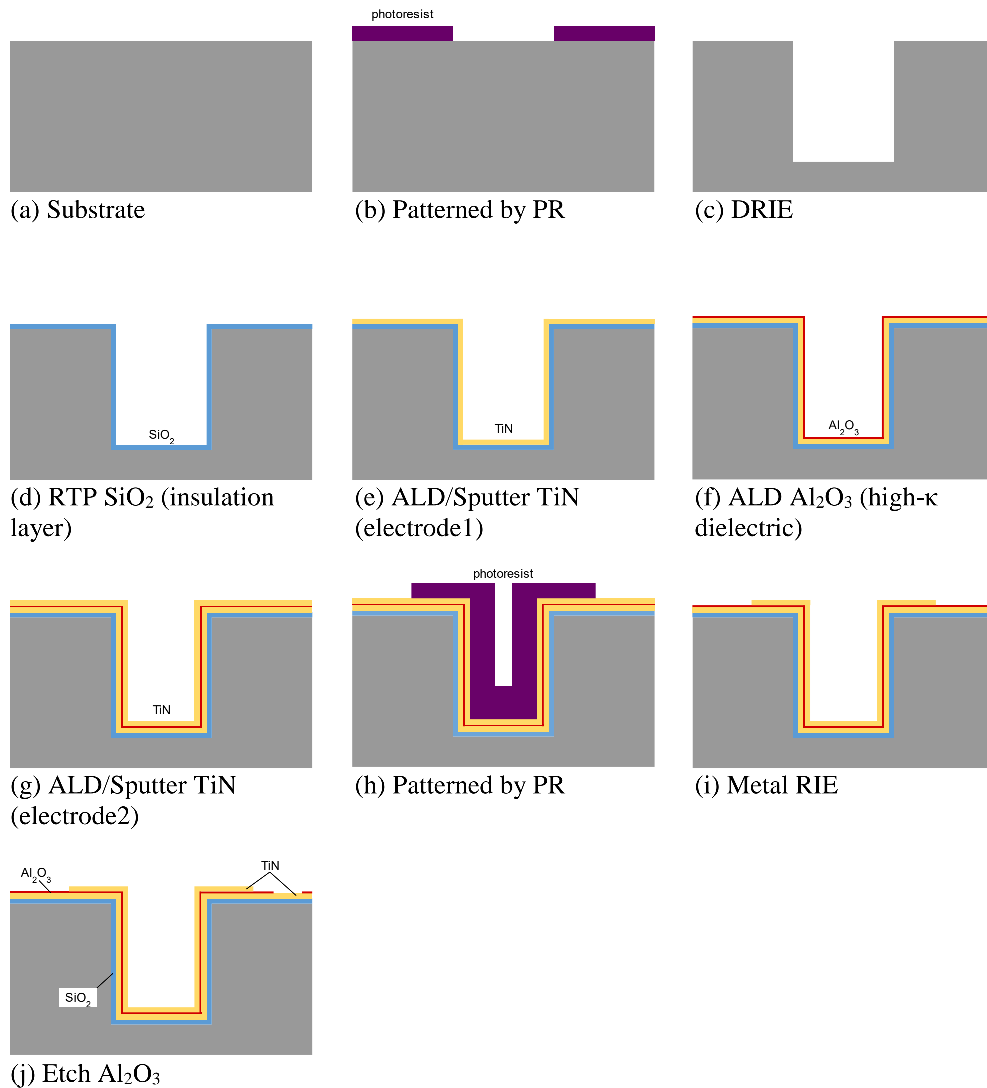


Figure 4.5: Proposed process flow of the 3-D embedded capacitor with the integration of a TSV.

Due to our limited fabrication capability at N2FC, 3-D embedded capacitors were built and characterized without a TSV. As a result, the process flow has been

modified accordingly from the previous one with TSV integration. The actual executed process flow is illustrated in Figure 4.6. The process flow starts to deviate from the proposed one in step (h). After the deposition of MIM layers, the wafer is patterned with PR again, followed by metal reactive ion etching (RIE) to define the top electrodes. Lastly, a potassium hydroxide (KOH) solution is used to etch part of the Al_2O_3 away, so that the bottom electrodes can be exposed for electrical characterization.



(a) Substrate (b) Patterned by PR (c) DRIE

(d) RTP SiO_2 (insulation layer) (e) ALD/Sputter TiN (electrode1) (f) ALD Al_2O_3 (high-κ dielectric)

(g) ALD/Sputter TiN (electrode2) (h) Patterned by PR (i) Metal RIE

(j) Etch Al_2O_3

Figure 4.6: Actual process flow of the 3-D embedded capacitor without the integration of a TSV.

4.4 Process Control and Optimization

In this section, the process steps mentioned above will be introduced with more detail, and process tuning attempts to achieve the optimization of the test vehicle fabrication are discussed. The section is divided into three major subsections: (1) trench formation, (2) deposition of the stacked layers, and (3) patterning of the top and bottom electrodes.

4.4.1 Trench Formation

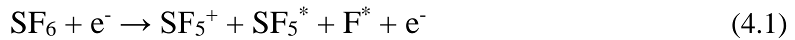
Trench formation involves multiple process steps: priming, PR spin-coating, soft-baking, exposure, developing, hard-baking, etching, and PR ashing. Firstly, the wafers were primed with hexamethyldisilizane (HDMS) in a YES-310TA priming oven to promote the PR adhesion on wafers. Secondly, photoresist MICROPOSIT S1813 was uniformly spin-coated on the wafers to achieve a thickness of 1.2 μm in a Suss RCD8 spin coater. Thirdly, the wafers were soft-baked in a hotplate at 130℃ for 2 minutes to remove the moisture residue in the PR. Fourthly, the wafers were loaded into a Karl Suss MA-6 mask aligner to be exposed under the designed Soda Lime photomask1 for 14 seconds. Then these wafers were taken out and developed manually in tetramethylammonium hydroxide (TMAH) solution, and the moisture on the wafers was removed in a Verteq 1600-55M spin rinse dryer. Next, the wafers were put into the hotplate again and hard-baked at 130℃ for another 2 minutes. After the PR patterning, the wafers were etched for a target depth of 60 μm in an Oxford PlasmaPro 100 Estrelas etch with a Bosch process recipe. Lastly, the processed wafers were loaded into a Tepla O_2 plasma asher for PR removal.

Among all these process steps, the key challenges of trench formation are mostly associated with DRIE. The Bosch process, also known as time multiplexed deep etching (TMDE), is one of the most effective etching approaches to realize highly anisotropic Si etching. Firstly invented by Laermer and Schilp of Robert Bosch GmbH in 1996 [1], the main feature of the Bosch process is its cyclic nature, where repetitive etching and passivation steps take place until a target etching depth is reached [2]. In the following paragraphs, the Bosch process/TMDE will be discussed

from several important perspectives: (1) reaction mechanism, (2) sidewall scallop, (3) aspect ratio dependent etching (ARDE), and (4) selectivity.

Many modified versions of TMDE have been proposed to realize etching and passivation steps in a number of different ways for various applications based on the same cyclic mechanism [3]–[7]. One of the well-adopted modifications is to replace the originally proposed passivation gases CHF_3 and Ar with C_4F_8 gas, which provides better passivation performance [2]. A schematic of the Bosch process is illustrated in Figure 4.7(a) and (b), where C_4F_8 is used as the passivation gas for isotropic sidewall protection and SF_6 is used as the etching gas for anisotropic downward etching [8]. The simplified chemical reactions involved in the Bosch process are explained below:

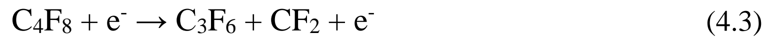
(etching cycle)



$$SF_6 + e^- \rightarrow SF_5^+ + SF_5^* + F^* + e^- \quad (4.1)$$

$$Si_{(s)} + 4F^*_{(g)} \rightarrow SiF_{4(g)} \quad (4.2)$$

(passivation cycle)



$$C_4F_8 + e^- \rightarrow C_3F_6 + CF_2 + e^- \quad (4.3)$$

$$nCF_2 \rightarrow (CF_2)_n \quad (4.4)$$

where SF_5^* and F^* are free radicals in plasma [9]–[11].

In this study, SF_6 and C_4F_8 are chosen as the etching and passivation gases, respectively, for the Bosch process.

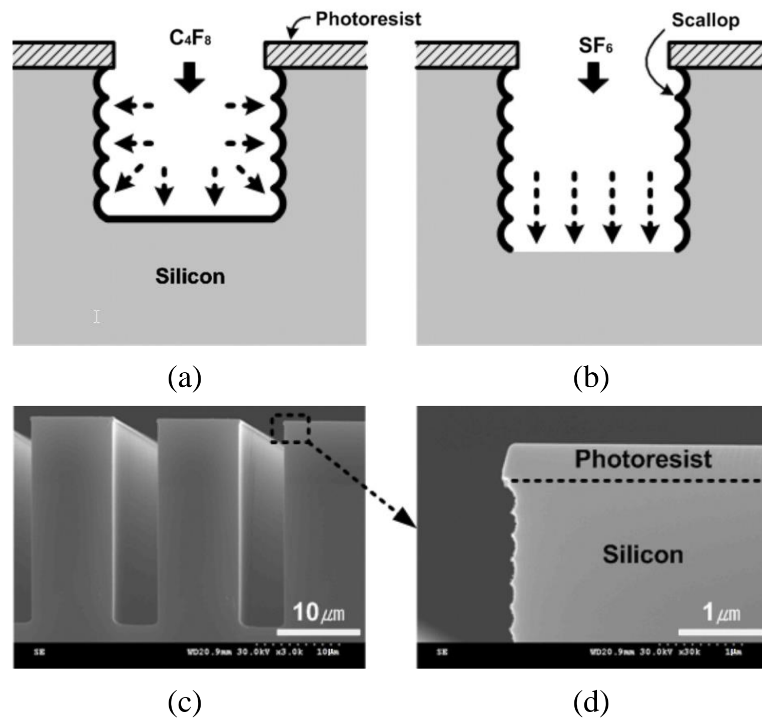


Figure 4.7: The Bosch process: (a) sidewall passivation using C_4F_8 gas, (b) silicon isotropic etching using SF_6 gas, (c) scanning electron microscope (SEM) image of the deep trench etched by DRIE, and (d) magnified SEM image of the sidewall with nanoscallops of the silicon microstructure [8].

However, regardless of the choice of etching and passivation gases, the cyclic nature of the Bosch process inevitably introduces scallops along the sidewall surface of the trench as shown in Figure 4.7(d). Generally, a smooth sidewall is preferred for a trench after DRIE, because sidewall scallops may cause quality degradation of thin films deposited afterwards. For example, for the 3-D embedded capacitor, the sharp peaks may lead to an enhanced electrical field in the thin dielectric layer. As a result, a higher leakage current density and lower dielectric strength can be expected. More on its impact will be discussed in Chapter 6. Many approaches have been made to minimize the peak-to-valley distance and therefore smoothen the sidewall surface [8]–[16]. These approaches include adding another round of global isotropic etching, reducing the time durations of both etching and passivation, increasing the power to the pressure ratio, and others.

The first two methods, due to their simplicity, have been carried out to lower the peak-to-valley distance on the trench sidewalls. For global isotropic etching, the wafers were loaded to a RIE etcher for SF_6 isotropic etching after the standard Bosch process. The effects of scallop reduction with different etching times are presented in Figure 1.3(a), (b), and (c). Figure 1.3(a) shows the as-etched scallops with a peak-to-valley distance of about 351 nm. After 2 minutes of SF_6 global isotropic etching, the peak-to-valley distance decreases to about 99 nm in Figure 1.3(b). Furthermore, when the etching time increases to 4 minutes, the scallops can be barely observed in Figure 1.3(c). As a result, this method of global isotropic etching is proven to be highly effective in removing the scallops on sidewall.

Nevertheless, Figure 1.3(d) shows a critical drawback which cannot be ignored. A large undercut of around 3.8 μm is observed below the PR. It makes the pattern size become out of control and the profile of the trench no longer straight. Thus, the first method of global isotropic is not considered in real fabrication despite its effectiveness in removing scallops. For the second method, both the time durations of etching and passivation were reduced in the recipe of the Bosch process to reduce the peak-to-valley distance of scallops. For comparison, the time duration of each step was reduced from a few seconds (the standard Bosch process) to hundreds of microseconds. Because of the fast switching operations, the passivation gas cannot be pumped out completely before the start of etching cycle: leading to passivation gas residue in the etching cycle. The same thing happens to the etching gas in the passivation cycle. Therefore, etching and passivation reactions take place simultaneously with the existence of both gases in the etcher chamber. The term "pseudo-Bosch process" is used to describe this modified version of the Bosch process with the coexistence of both gases [17], [18]. The SEM images of the etched trenches by the standard Bosch process and by the fast switching pseudo-Bosch process are shown in Figure 4.9(a) and (b), respectively. In fact, this method is so effective that the scallops can be barely recognized on the trench sidewall with our modified recipe. At the same time, no undercut below the PR is observed this time, which means the original pattern is transferred from the photomask well. Therefore, two DRIE recipes have been developed for the test vehicle fabrication using the time duration reduction method. One is the standard Bosch process to generate a peak-to-

valley distance of 290 nm; whereas, the other is a fast switching pseudo-Bosch process to generate a peak-to-valley distance of only 30 nm. The target depth of both recipes is 60 μm. These two recipes were adopted as main DRIE processes for the fabrication of test vehicles in this study. It is also worth pointing out that some vertical striations are seen along the depth of trenches in both images. These vertical striations are probably caused by the wrinkling of photoresists on top. This problem is likely to be solved when better photomasks and lithography steps are adopted.

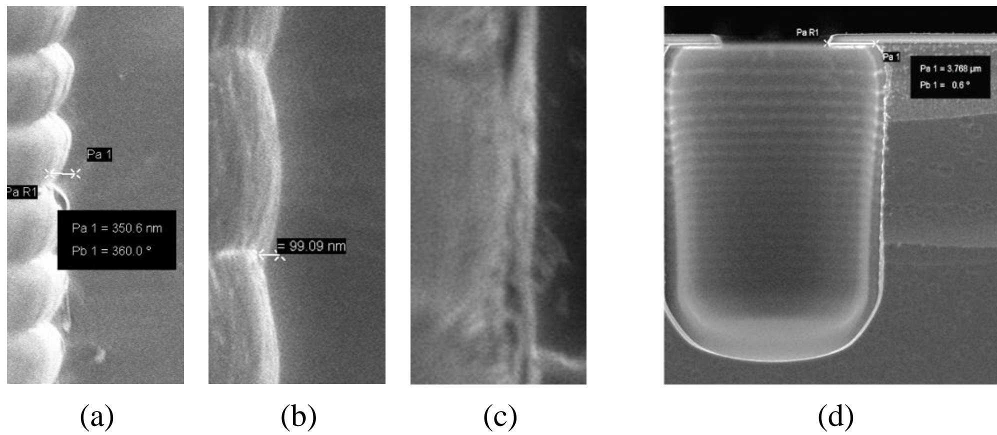


Figure 4.8: The effects of SF_6 global isotropic etching after the Bosch process: (a) as-etched, (b) 2 mins of isotropic etching, (c) 4 mins of isotropic etching, and (d) a large undercut below the PR due to a long duration of global isotropic etching.

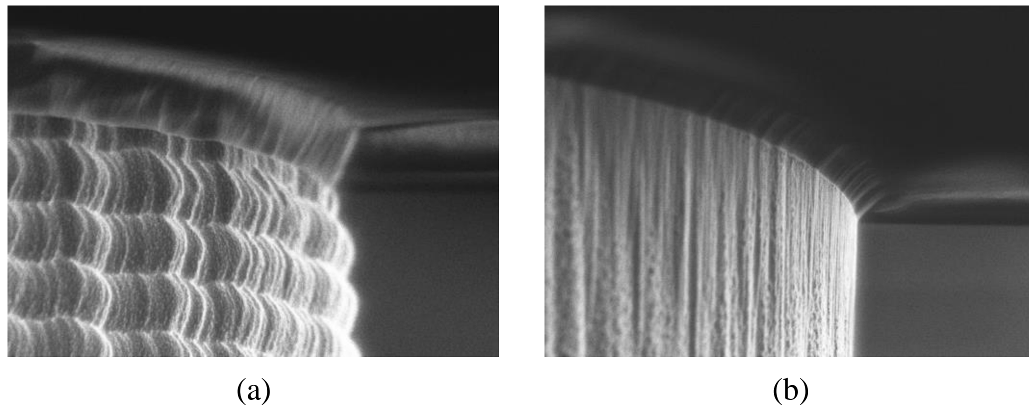


Figure 4.9: The effects of time duration reduction of both etching and passivation in the recipe of the Bosch process: (a) as-etched and (b) the time duration of each step reduced from a few seconds to hundreds of microseconds.

Aspect ratio dependent etching (ARDE), also known as RIE lag, happens when trenches with different pattern sizes are etched simultaneously. Trenches with smaller diameters tend to be etched slower, whereas trenches with larger diameters tend to be etched faster [2]. In addition, the etch rate reduces as the depth increases, and it may even fall to zero at the "critical aspect ratio" [19]–[21]. A conceptual depiction of etch rate as a function of the aspect ratio is shown in Figure 4.10 [21]. In this work, the trench radius was set to vary from 5, 10, 15, 20 to 25 µm, and the target depth was set to be 60 µm based on the actual size of TSVs. Figure 4.11(a) shows five trenches with increasing radius from left to right etched by the standard Bosch process, while Figure 4.11(b) shows five trenches with increasing radius from left to right etched by the fast switching pseudo-Bosch process. Their respective measured geometries results are summarized in Table 4.1. For trenches with rough sidewalls, the depth increases from 38.9 to 54.4 µm, as the measured diameter increases from 9.6 to 49.5 µm. For trenches with smooth sidewalls, the depth increases from 43.1 to 58.1 µm as the measured diameter increases from 9.3 to 49.5 µm. It can be calculated that the ARDE lag is 28.5% for the former ones, and it is 25.8% for the latter ones. In this case, the results are sufficient to serve the purpose of representing the actual size of TSV geometries. In fact, one could further mitigate the effect of ARDE by tuning the etching step, because depletion of the fluorine content at the bottom of the trench is the dominant reason for ARDE [22]. It has been reported that negligible ARDE lag (only 2% to 3% variation) can be achieved across a width range of 2.5 to 100 µm at a 2 µm/min etch rate [23]. In addition, some vertical striations mentioned above can be easily recognized in all of these trenches, and it seems that they are more obvious in trenches etched by the fast switching pseudo-Bosch process. Further investigation is required to find out the reason for the difference.

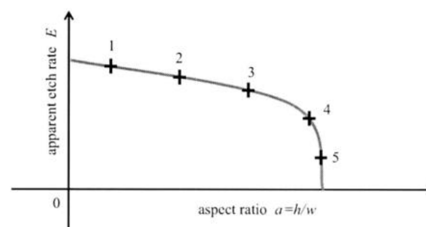
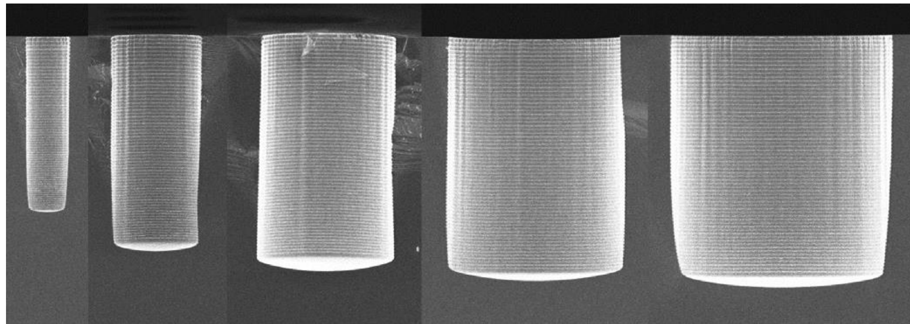
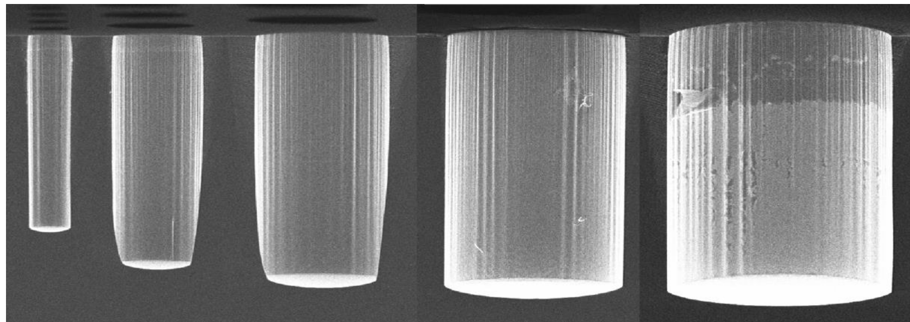


Figure 4.10: A conceptual depiction of the etch rate as a function of the aspect ratio [21].



(a)



(b)

Figure 4.11: The trenches etched by two different DRIE recipes: (a) the Bosch process and (b) the fast switching pseudo-Bosch process.

Table 4.1: Measurement results of trench geometries for test vehicle fabrications.

	Standard Bosch (Rough Sidewall)		Fast Switching Pseudo-Bosch (Smooth Sidewall)	
	Diameter [µm]	Depth [µm]	Diameter [µm]	Depth [µm]
1	9.6	38.9	9.3	43.1
2	19.7	46.0	19.5	51.3
3	29.7	50.4	29.6	54.5
4	39.6	52.1	40.1	57.1
5	49.5	54.4	49.5	58.1

Selectivity is another important aspect of the DRIE process, which is referred to as the etch rate ratio of Si and its mask material. Mask protection is very critical for the structural integrity of trenches: the mask can be possibly depleted even before a certain target depth is reached if the selectivity is not high enough. As mentioned above, 1.2 μm thick PR can withstand 43.1 μm deep etching for trenches with diameters as small as 9.3 μm. However, this mask protection becomes insufficient for more demanding etching processes. Thus, two other mask preparation methods have been developed for future requirements: (1) TSVs for high density application (trench diameter = 3 μm, trench depth = 30 μm) and (2) TSVs for Si interposer application (trench diameter = 10 μm, trench depth = 100 μm). For the first application, a thicker PR (1.9 μm) was deposited and a longer hard-baking time (4 minutes) was set to enhance the selectivity between Si and PR. As a result, trenches with a diameter of 3.1 μm and depth of 28.2 μm have been successfully etched as shown in the SEM picture in Figure 4.12. For the second application, a 200 nm SiO_2 layer hard mask was adopted instead of PR to achieve a higher selectivity as shown in Figure 4.13. The etched trenches with various openings are shown in Figure 4.13: the trench with a diameter as small as 11.5 μm reaches 92.7 μm deep, whereas the trench with a diameter as large as 51.1 μm reaches 143.2 μm deep. The measurement results are summarized in Table 4.2. Therefore, the requirements for both high density and Si interposer applications have been met with better mask selectivity, which are realized by either PR enhancement or hard mask replacement.

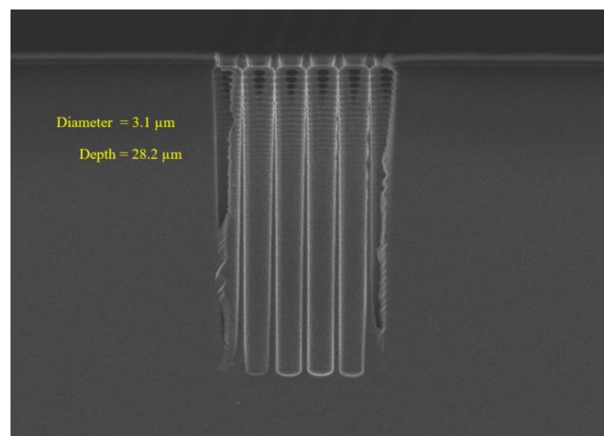


Figure 4.12: A SEM picture of small trenches after DRIE enabled by enhanced PR mask protection.

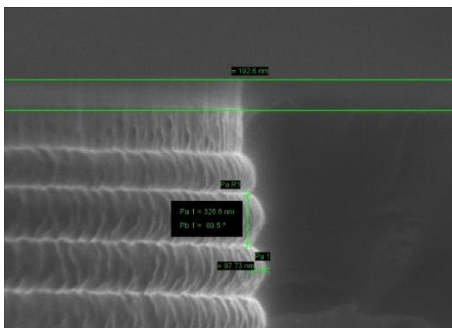


Figure 4.13: The PR is replaced by SiO_2 as a hard mask for higher selectivity.

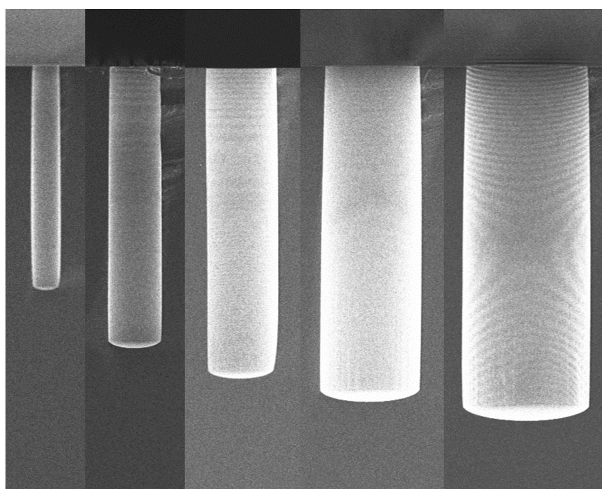


Figure 4.14: A SEM picture of deep trenches after DRIE enabled by SiO_2 hard mask protection.

Table 4.2: Measurement results of trench geometries for Si interposer application.

	Diameter [µm]	Depth [µm]
1	11.5	92.7
2	21.8	114.4
3	30.2	128.1
4	41.0	136.8
5	51.4	143.2

4.4.2 Deposition of Stacked Layers

The stacked layers include a thin SiO_2 layer for insulation and $TiN/Al_2O_3/TiN$ layers as an MIM capacitor. After the trench formation, the wafers are loaded into an AS-One rapid thermal processing (RTP) furnace. The RTO process is chosen mainly because of its fast processing time. The RTO recipe is applied to form a 10 nm thick SiO_2 layer in a O_2 environment at 1000°C across the top surface of wafers. For actual manufacturing with other devices on wafers, this step can be replaced by a CVD process to keep the process temperature below the back-end-of-line (BEOL) thermal budget of 400°C.

With the SiO_2 insulation layer, two process methods were developed to deposit $TiN/Al_2O_3/TiN$ layers for two types of 3-D embedded capacitors. Both TiN and Al_2O_3 have been successfully deposited with various ALD and sputtering methods [22], [23], [32]–[36], [24]–[31]. The recipes used in this study are summarized in Table 4.3. For the ALD type, all three layers of $TiN/Al_2O_3/TiN$ were deposited by ALD. The wafers were loaded to a Picosun plasma enhanced atomic layer deposition (PEALD) reactor to deposit a 50 nm thick TiN bottom electrode, in which $TiCl_4$ and NH_3 were used as precursors. Then the wafers were removed and put into another ALD reactor to deposit a 10 nm thick Al_2O_3 dielectric layer conformally with trimethylaluminum (TMA) and H_2O as precursors. Lastly, the same ALD process was repeated to deposit a 50 nm thick TiN top electrode in the PEALD reactor. For the sputtering type of 3-D embedded capacitor, both top and bottom TiN electrodes were deposited by reactive direct current (DC) sputtering, but the Al_2O_3 dielectric layer in-between was deposited by ALD. The wafers were firstly loaded into an Evatec Clusterline CLC200 sputterer for 400 nm TiN bottom electrode deposition, in which Ti was used as the target material and Ar/N_2 gas flowed through with a ratio of 5/2. Then the wafers were taken out and put into a Picosun ALD reactor to deposit a 30 nm thick Al_2O_3 dielectric layer conformally with TMA and H_2O as precursors. Lastly, the same sputtering process was repeated to deposit a 400 nm thick TiN top electrode. The dielectric layer of the sputtering type was set thicker than that of the ALD type (i.e., 10 nm vs. 30 nm), because the surface of the sputtered electrodes may be rough, leading to quality degradation of the dielectric thin film. For both methods, the temperature was kept below the BEOL thermal budget of

400°C. Sputtering was operated at room temperature for TiN, whereas ALD was operated at 300°C for both TiN and Al_2O_3.

Table 4.3: The deposition methods of TiN and Al_2O_3 layers.

Sputtering TiN				
Target	Pressure	Ar/N_2 ratio	Temperature	Power
Ti	1×10^{-3} mbar	5/2	25 °C	7800 W
ALD TiN				
Precursor 1	Precursor 2	Temperature		
$TiCl_4$	NH_3	300 °C		
ALD Al_2O_3				
Precursor 1	Precursor 2	Temperature		
TMA	H_2O	300 °C		

As a result, four different types of test vehicles have been fabricated combining two options for DRIE (the Bosch process vs. the fast switching pseudo-Bosch process) with two options for stacked layer deposition (ALD vs. sputtering). In summary, these four types of test vehicles are named as (1) rough-ALD, (2) smooth-ALD, (3) rough-sputtering, and (4) smooth-sputtering. For simplicity, “rough” and “smooth” refer to the Bosch process and fast switching pseudo-Bosch process, respectively. After the deposition of the MIM layer, all four types of test vehicles were cleaved and examined under SEM and transmission electron microscope (TEM) to investigate their structural integrity and layer compositions.

The SEM pictures of the first two types of test vehicles, rough-ALD and smooth-ALD, are shown in Figure 4.15(a) and (b), respectively. Despite the sidewall scallops caused by the Bosch process, the stacked layers continuously cover the top, middle, and bottom parts of the rough surface just as they do on the smooth sidewall. Two TEM pictures with much higher resolution provide more detail as shown in

Figure 4.16(a) and (b). A sharp peak can be observed in Figure 4.16(a) for the rough-ALD type test vehicle, but no significant thinning of any layer is seen in the picture. Thus, excellent step coverage is demonstrated with the developed ALD recipes for TiN and Al_2O_3. Furthermore, columnar poly-crystalline TiN grains can be observed for both top and bottom electrodes, and the Al_2O_3 dielectric layer remains amorphous in Figure 4.16(a) and (b). Good crystallinity in a TiN layer is essential for good electrical conductivity, whereas the amorphous phase of Al_2O_3 is essential for good electrical insulation [37]–[39]. The measurement results show that the MIM layers of the rough-ALD test vehicle are 48.6 nm TiN layer as the top electrode, 9.7 nm Al_2O_3 layer as the dielectric layer, and 57.4 nm TiN layer as the bottom electrode. In contrast, the MIM layers of the smooth-ALD test vehicle are 51.4 nm TiN layer as the top electrode, 11.0 nm Al_2O_3 layer as the dielectric layer, and 53.2 nm TiN layer as the bottom electrode. The top electrodes from both rough-ALD and smooth-ALD types are slightly thinner than their corresponding bottom electrodes (48.6 nm vs. 57.4 nm and 51.4 nm vs. 53.2 nm) even though the same ALD recipe was applied. This result may be due to some oxidation of TiN occurring for the top electrodes, which are exposed to the air.

An energy-dispersive X-ray spectroscopy (EDX) line scan was performed across the cross-sectional surface of the rough-ALD test vehicle to characterize the elemental composition of the stacked layers. Figure 4.17(a) shows the location where the EDX line scan was undertaken, and Figure 4.17(b) shows the atomic percentage of each element with respect to the distance along the scanning direction. The result in Figure 4.17(b) confirms good stoichiometry of the TiN and Al_2O_3 layers deposited by ALD. At distances of 40 to 90 nm and 100 to 150 nm, Ti and N are predominant, where the atomic percentage of Ti is slightly higher than that of N for both top and bottom TiN electrodes. At a distance of 90 to 100 nm, Al and O are predominant, where the atomic percentage of O is slightly higher than that of Al for the Al_2O_3 dielectric layer. Besides, at the distances ~50 and ~150 nm, another two peaks of O are shown in the plot. The left peak suggests that some oxidation of the TiN top electrode layer might happen after exposure to air, and the right one corresponds to O in the SiO_2 insulation layer.

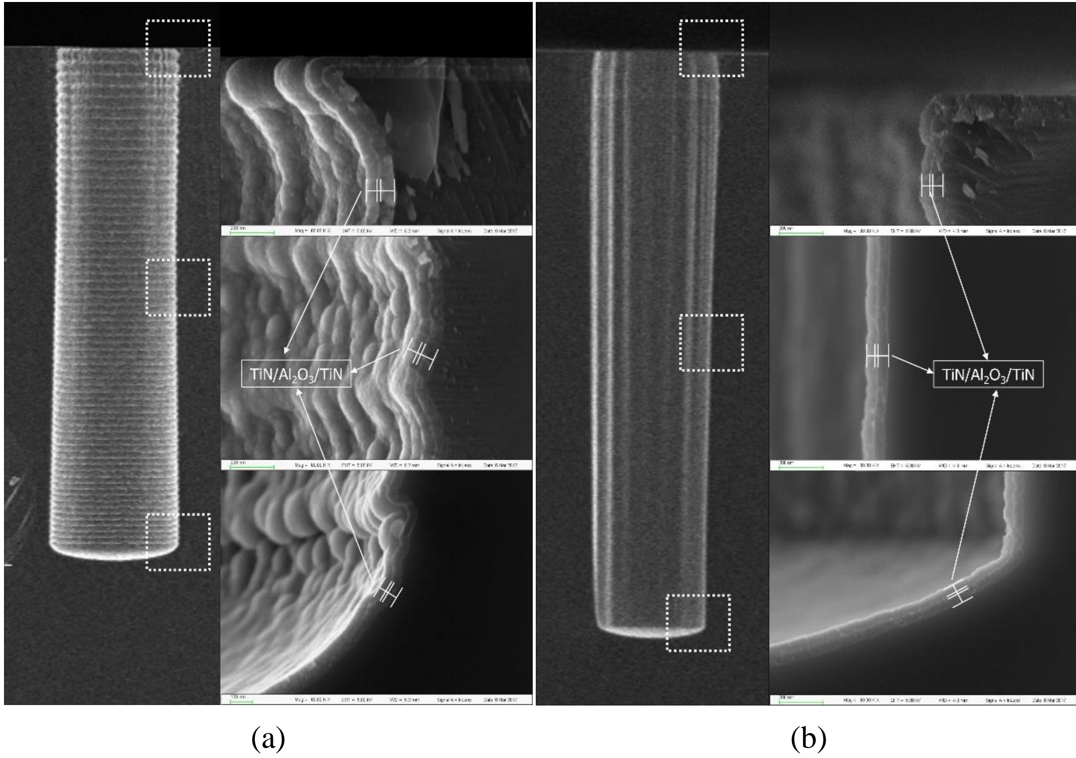


Figure 4.15: SEM pictures of the two types of test vehicles: (a) rough-ALD and (b) smooth-ALD.

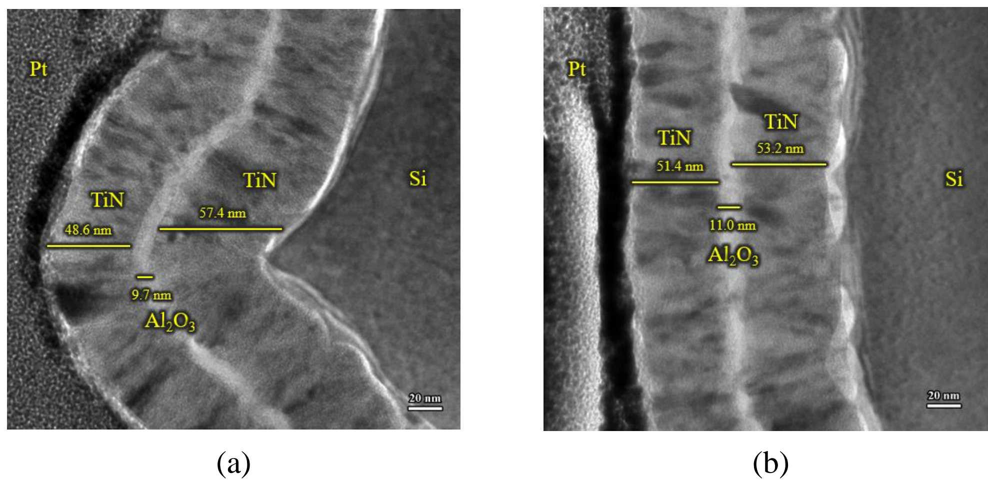
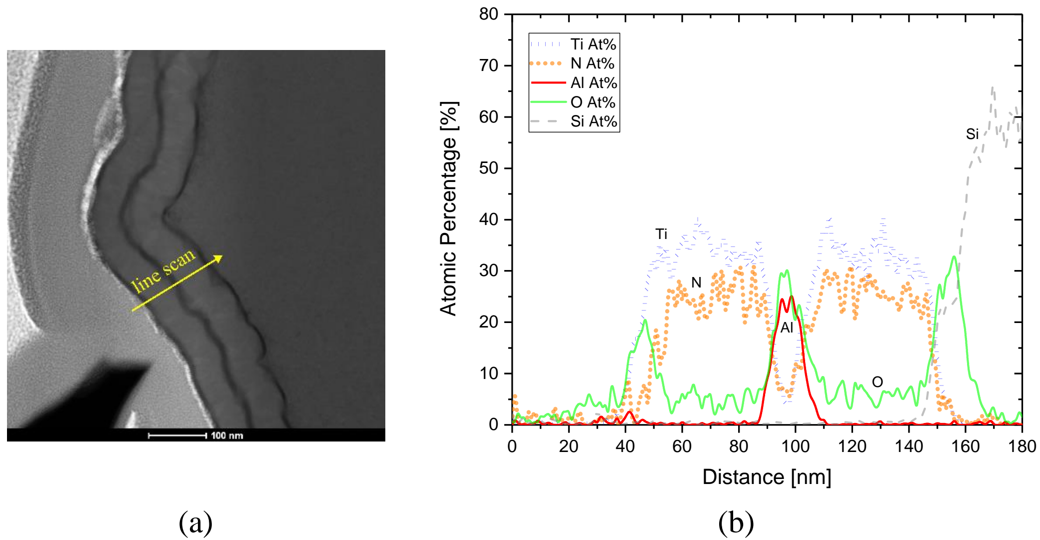


Figure 4.16: TEM pictures of the two types of test vehicles: (a) rough-ALD and (b) smooth-ALD.



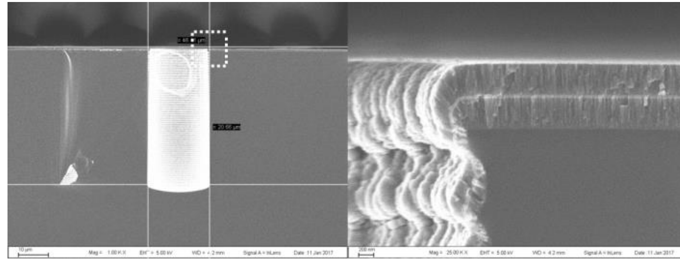
(a) (b)

Figure 4.17: (a) The location where the EDX line scan was undertaken on a rough-ALD test vehicle and (b) the atomic percentage of each element with respect to the distance along the scanning direction.

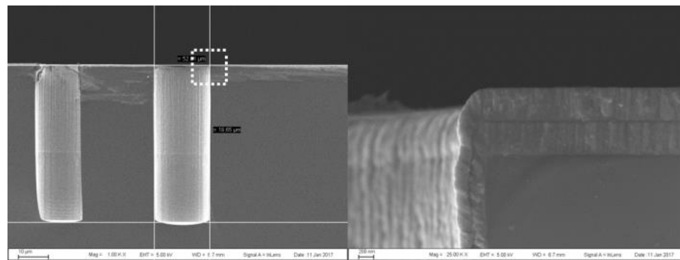
The SEM pictures of the first two types of test vehicles, rough-sputtering and smooth-sputtering, are shown in Figure 4.18(a) and (b), respectively. Unlike the conformal layer depositions by ALD on both rough and smooth sidewalls, sputtered TiN layers suffer much from poor step coverage. The thickness of the sputtered TiN reduces significantly from 400 nm on the planar surface to only 200 nm even on the top part of the sidewall for both sputtering types of test vehicles. The sidewall roughness causes drastic thinning of sputtered TiN layers deposited on the lower part of the scallop peaks. But on the smooth sidewall, the sputtered TiN layer is continuous, and its thickness decreases along the depth gradually. The step coverage of the sputtered TiN is also affected by the size of the trench openings. Figure 4.19(a) and (b) show the step coverage difference of the sputtered TiN layers on smooth sidewalls between a trench with a diameter of 10 µm and another with a diameter of 40 µm. The insets of the pictures were both taken from the parts which are 30 µm below the top surface. For the trench with a diameter of 10 µm, the TiN layer can be hardly noticed: leaving only a 32 nm thick Al_2O_3 dielectric layer on the sidewall. In contrast, for the trench with a diameter of 40 µm, both top and bottom electrodes TiN layers remain on the sidewall and are measured to be around 46 µm under SEM. This indicates the surface area reduction, and therefore the capacitance reduction, of the

capacitor induced by the limited step coverage of sputtering as an electrode deposition method, which has to be carefully considered for the future design of sputtering type 3-D embedded capacitors.

Two TEM pictures with much higher resolution provide more detail as shown in Figure 4.20(a) and (b). The drastic thinning of the sputtered TiN layer on the scallop peak is clearly shown in Figure 4.20(a), but it still physically forms a continuous layer over that peak. For comparison, the sputtered TiN layers in Figure 4.20(b) are uniformly distributed on the smooth sidewall. It should also be pointed out that the columnar crystallites of the sputtered TiN layers are smaller in diameter and slightly disorientated compared to the columnar crystallites of the ALD TiN layers. This result occurred because of different growth nucleation mechanisms: columnar growth from "point-nucleus" in sputtering and columnar growth from "2-dimensional nucleation" in ALD, respectively, as shown in Figure 4.21 [36]. The measurements performed on the top part of the sidewall show that the MIM layers of the rough-sputtering test vehicle are 206.7 nm TiN layer as the top electrode, 32.3 nm Al_2O_3 layer as the dielectric layer, and 210.2 nm TiN layer as the bottom electrode; whereas the MIM layers of the smooth-sputtering test vehicle are 151.9 nm TiN layer as the top electrode, 32.7 nm Al_2O_3 layer as the dielectric layer, and 204.1 nm TiN layer as the bottom electrode. Then another EDX line scan was performed across the cross-sectional surface of the rough-sputtering test vehicle to characterize the elemental composition of the stacked layers. Figure 4.22(a) shows the location where the EDX line scan was undertaken, and Figure 4.22(b) shows the atomic percentage of each element with respect to the distance along the scanning direction. The results confirm the good stoichiometry of those stacked layers deposited by sputtering/ALD/sputtering processes sequentially (similar to the analysis mentioned above for Figure 4.17).

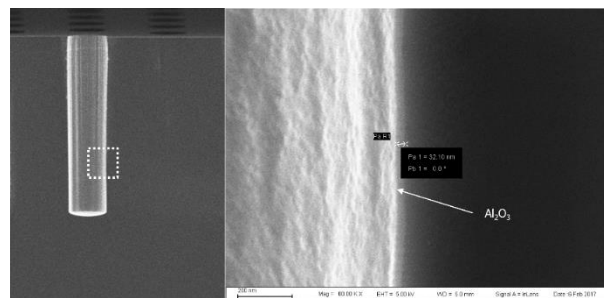


(a)

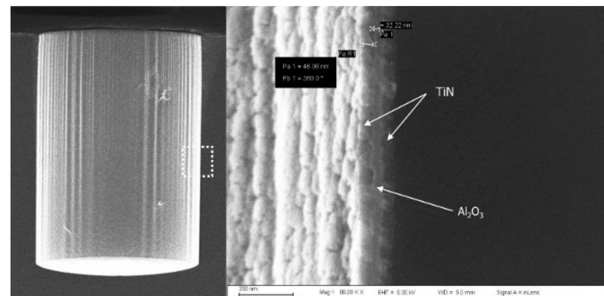


(b)

Figure 4.18: SEM pictures of the two types of test vehicles: (a) rough-sputtering and (b) smooth-sputtering.

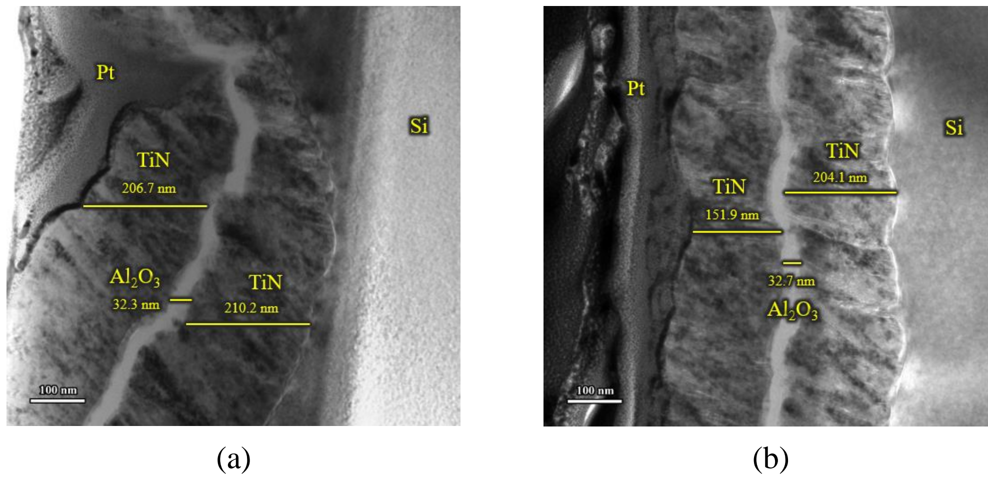


(a)



(b)

Figure 4.19: Step coverage of sputtered TiN electrodes on the smooth sidewalls in (a) a trench with diameter of 10 µm and (b) a trench with diameter of 40 µm. Both insets of pictures were taken from parts that are 30 µm below the top surface.



(a) (b)

Figure 4.20: TEM pictures of the two types of test vehicles: (a) rough-sputtering and (b) smooth-sputtering.

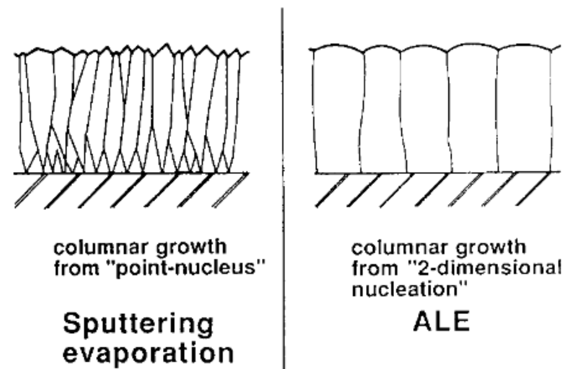
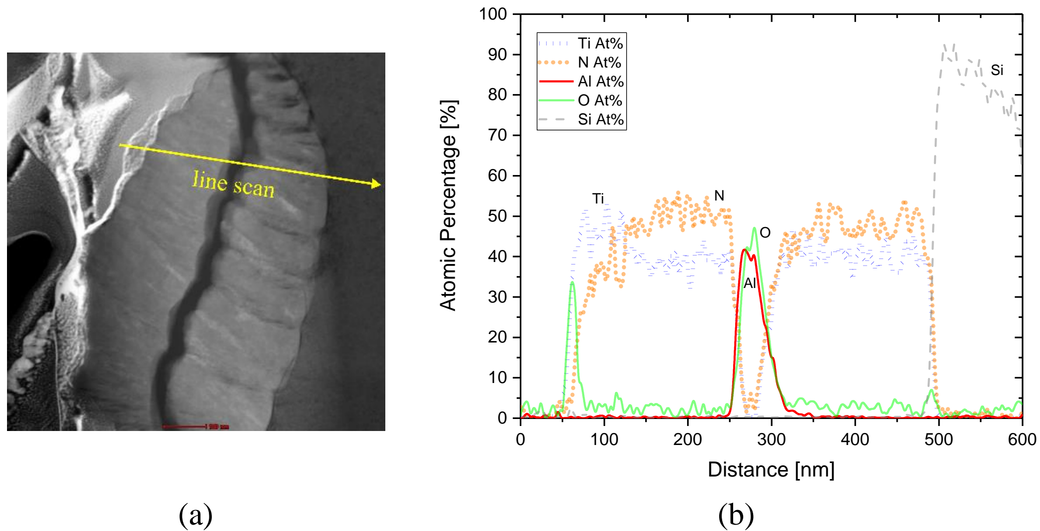


Figure 4.21: Comparison of the basic nucleation mechanisms for sputtered or evaporated and atomic layer epitaxy (ALE) thin films (ALE is another name for ALD) [36].



(a) (b)

Figure 4.22: (a) The location where the EDX line scan was undertaken on a rough-sputtering test vehicle and (b) the atomic percentage of each element with respect to the distance along the scanning direction.

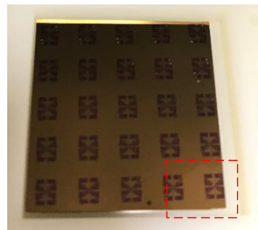
4.4.3 Patterning of the Top and Bottom Electrodes

After trench formation and stacked layer deposition, the test vehicles on the wafers need to be patterned for their top and bottom electrodes.

For the patterning process of the top electrodes, another round of lithography was performed, and the second piece of photomask was used and aligned to the alignment marks designed in Figure 4.3. With the patterned PR, the wafers were sent to a Cello Nasca-20L etcher for metal RIE. The uncovered part of the top layer was removed with either the 50 nm TiN etching recipe for ALD type test vehicles or the 400 nm TiN etching recipe for sputtering type test vehicles.

For the patterning process of the bottom electrodes, the patterns can be chosen to be any place where there is no test vehicle structure. Two wet etching methods have been developed for Al_2O_3 for different purposes. The first method is the fast wet etching of Al_2O_3 by a KOH solution. It took about 2 minutes to remove the 10 nm Al_2O_3 layer and 6 minutes to remove the 30 nm Al_2O_3 layer. The finished samples are shown in Figure 4.23(a) and (b) for ALD type and sputtering type test vehicles, respectively. The red dashed line squares indicate the places where the Al_2O_3 was etched away. The second method is a well-controlled process to gradually remove the

Al_2O_3 layer. A tetramethylammonium hydroxide (TMAH) based developer, ma-D 533, was used to etch the Al_2O_3 layer at a much slower rate. It took 1 minute to remove the 1.4 nm Al_2O_3 layer and 10 minutes to remove the 15.2 nm Al_2O_3 layer. In this way, the electrical properties of partial dielectric layers could be studied in the future to obtain better physical insight into the ALD Al_2O_3 thin film.



(a)

(b)

Figure 4.23: A KOH solution was used for wet etching to remove (a) the 10 nm Al_2O_3 layer and (b) the 30 nm Al_2O_3 layer.

4.5 Summary

In this chapter, the photomask design has been firstly presented for prototype fabrication. Each unit cell contains test vehicles with five different geometries. Secondly, the two versions of the process flow have been illustrated. The second version, which does not include Cu filling, is used for the fabrication of the samples in this study. Next, process control and optimization have been made to ensure that the test vehicles can be fabricated as designed earlier. Therefore, two DRIE recipes are developed to etch deep trenches in the Si substrate with rough and smooth scallops, respectively. Also, two different electrode deposition methods, ALD and sputtering, are explored to intentionally form MIM layers with excellent and poor step coverage, respectively. In addition, a metal RIE recipe has been developed to pattern the top electrodes, whereas a wet etching recipe has been developed to expose the contact windows for the bottom electrodes. In total, six different types of test vehicles have been successfully fabrication for characterization: (1) the de-embedded ALD type, (2) the embedded rough-ALD type, (3) the embedded smooth-ALD type, (4) the de-embedded sputtering type, (5) the embedded rough-sputtering type, and (6) the embedded smooth-sputtering type.

References

[1] F. Laermer and S. Andrea, “Method of anisotropically etching silicon,” US 5501893A, 1996.

[2] B. Wu, A. Kumar, and S. Pamarthy, “High aspect ratio silicon etch: A review,” *J. Appl. Phys.*, vol. 108, no. 5, p. 051101, Sep. 2010.

[3] J. Hopkins, H. Ashraf, J. K. Bhardwaj, A. M. Hynes, I. Johnston, and J. N. Shepherd, “The benefits of process parameter ramping during the plasma etching of high aspect ratio silicon structures,” *MRS Proc.*, vol. 546, p. 63, Jan. 1998.

[4] K. W. Kok, W. J. Yoo, K. Sooriakumar, J. S. Pan, and E. Y. Lee, “Investigation of in situ trench etching process and Bosch process for fabricating high-aspect-ratio beams for microelectromechanical systems,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 20, no. 5, p. 1878, Oct. 2002.

[5] J. Van Aelst, H. Struyf, W. Boullart, and S. Vanhaelemeersch, “High aspect ratio via etch development for Cu nails in 3-D-stacked ICs,” *Thin Solid Films*, vol. 516, no. 11, pp. 3502–3506, Apr. 2008.

[6] Dacleng Zhang, Jianwei Wan, Guizheng Yan, Ting Li, Dayu Tian, and Ke Deng, “High aspect ratio Si etching technique and application,” in *5th International Conference on Solid-State and Integrated Circuit Technology. Proceedings*, 1998, pp. 91–93.

[7] S.-B. Jo, M.-W. Lee, S.-G. Lee, E.-H. Lee, S.-G. Park, and B.-H. O, “Characterization of a modified Bosch-type process for silicon mold fabrication,” *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 23, no. 4, pp. 905–910, Jul. 2005.

[8] C. K. Kang, S. M. Lee, I. D. Jung, P. G. Jung, S. J. Hwang, and J. S. Ko, “The fabrication of patternable silicon nanotips using deep reactive ion etching,” *J. Micromechanics Microengineering*, vol. 18, no. 7, p. 075007, Jul. 2008.

[9] H. Jansen, M. de Boer, J. Burger, R. Legtenberg, and M. Elwenspoek, “The black silicon method II:The effect of mask material and loading on the reactive

ion etching of deep silicon trenches," *Microelectron. Eng.*, vol. 27, no. 1–4, pp. 475–480, Feb. 1995.

[10] H. M. Anderson, J. A. Merson, and R. W. Light, "A kinetic model for plasma etching silicon in a SF6/O2 RF discharge," *IEEE Trans. Plasma Sci.*, vol. 14, no. 2, pp. 156–164, 1986.

[11] A. M. Hynes, H. Ashraf, J. K. Bhardwaj, J. Hopkins, I. Johnston, and J. N. Shepherd, "Recent advances in silicon etching for MEMS using the ASE™ process," *Sensors Actuators A Phys.*, vol. 74, no. 1–3, pp. 13–17, Apr. 1999.

[12] R. Nagarajan, K. Prasad, L. Ebin, and B. Narayanan, "Development of dual-etch via tapering process for through-silicon interconnection," *Sensors Actuators A Phys.*, vol. 139, no. 1–2, pp. 323–329, Sep. 2007.

[13] N. Ranganathan, K. Prasad, N. Balasubramanian, and K. L. Pey, "A study of thermo-mechanical stress and its impact on through-silicon vias," *J. Micromechanics Microengineering*, vol. 18, no. 7, p. 075018, Jul. 2008.

[14] I. U. Abhulimen, S. Polamreddy, S. Burkett, L. Cai, and L. Schaper, "Effect of process parameters on via formation in Si using deep reactive ion etching," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 25, no. 6, p. 1762, 2007.

[15] F. Gao, S. Ylinen, M. Kainlauri, and M. Kapulainen, "Smooth silicon sidewall etching for waveguide structures using a modified Bosch process," *J. Micro/Nanolithography, MEMS, MOEMS*, vol. 13, no. 1, p. 013010, Mar. 2014.

[16] N. Ranganathan, D. Y. Lee, L. Youhe, G.-Q. Lo, K. Prasad, and K. L. Pey, "Influence of Bosch etch process on electrical isolation of TSV structures," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 1, no. 10, pp. 1497–1507, Oct. 2011.

[17] M. D. Henry, M. J. Shearn, B. Chhim, and A. Scherer, "Ga + beam lithography for nanoscale silicon reactive ion etching," *Nanotechnology*, vol. 21, no. 24, p. 245303, Jun. 2010.

[18] M. D. Henry, S. Walavalkar, A. Homyk, and A. Scherer, "Alumina etch masks for fabrication of high-aspect-ratio silicon micropillars and nanopillars," *Nanotechnology*, vol. 20, no. 25, p. 255305, Jun. 2009.

[19] J. Yeom, Y. Wu, J. C. Selby, and M. A. Shannon, "Maximum achievable aspect ratio in deep reactive ion etching of silicon due to aspect ratio dependent transport and the microloading effect," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 23, no. 6, p. 2319, 2005.

[20] M. A. Blauw, T. Zijlstra, and E. van der Drift, "Balancing the etching and passivation in time-multiplexed deep dry etching of silicon," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 19, no. 6, p. 2930, 2001.

[21] J. Yeom, Y. Wu, and M. A. Shannon, "Critical aspect ratio dependence in deep reactive ion etching of silicon," in *International Conference on Solid-State Sensors, Actuators and Microsystems. Digest of Technical Papers*, 2003, vol. 2, pp. 1631–1634.

[22] M. A. Blauw, T. Zijlstra, R. A. Bakker, and E. van der Drift, "Kinetics and crystal orientation dependence in high aspect ratio silicon dry etching," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 18, no. 6, p. 3453, 2000.

[23] S. L. Lai, D. Johnson, and R. Westerman, "Aspect ratio dependent etching lag reduction in deep silicon etch processes," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 24, no. 4, pp. 1283–1288, Jul. 2006.

[24] M. Sridharan, M. Sillassen, J. Bøttiger, J. Chevallier, and H. Birkedal, "Pulsed DC magnetron sputtered Al2O3 films and their hardness," *Surf. Coatings Technol.*, vol. 202, no. 4–7, pp. 920–924, Dec. 2007.

[25] R. S. Nowicki, "Properties of rf-sputtered Al 2 O 3 films deposited by planar magnetron," *J. Vac. Sci. Technol.*, vol. 14, no. 1, pp. 127–133, Jan. 1977.

[26] S. M. George, "Atomic Layer Deposition: An Overview," *Chem. Rev.*, vol. 110, no. 1, pp. 111–131, Jan. 2010.

[27] M. D. Groner, J. W. Elam, F. H. Fabreguette, and S. M. George, "Electrical characterization of thin Al2O3 films grown by atomic layer deposition on

silicon and various metal substrates," *Thin Solid Films*, vol. 413, no. 1–2, pp. 186–197, Jun. 2002.

[28] M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George, "Low-Temperature Al 2 O 3 Atomic Layer Deposition," *Chem. Mater.*, vol. 16, no. 4, pp. 639–645, Feb. 2004.

[29] P. Kelly and R. Arnell, "Magnetron sputtering: a review of recent developments and applications," *Vacuum*, vol. 56, no. 3, pp. 159–172, Mar. 2000.

[30] G. Lemperière and J. M. Poitevin, "Influence of the nitrogen partial pressure on the properties of d.c.-sputtered titanium and titanium nitride films," *Thin Solid Films*, vol. 111, no. 4, pp. 339–349, Jan. 1984.

[31] Y. Massiani, A. Medjahed, P. Gravier, L. Argème, and L. Fedrizzi, "Electrochemical study of titanium nitride films obtained by reactive sputtering," *Thin Solid Films*, vol. 191, no. 2, pp. 305–316, Oct. 1990.

[32] H. Jeon, J.-W. Lee, Y.-D. Kim, D.-S. Kim, and K.-S. Yi, "Study on the characteristics of TiN thin film deposited by the atomic layer chemical vapor deposition method," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 18, no. 4, pp. 1595–1598, Jul. 2000.

[33] M. Juppo, M. Ritala, and M. Leskelä, "Use of 1,1-Dimethylhydrazine in the Atomic Layer Deposition of Transition Metal Nitride Thin Films," *J. Electrochem. Soc.*, vol. 147, no. 9, p. 3377, 2000.

[34] M. Ritala, M. Leskelä, J.-P. Dekker, C. Mutsaers, P. J. Soininen, and J. Skarp, "Perfectly Conformal TiN and Al2O3 Films Deposited by Atomic Layer Deposition," *Chem. Vap. Depos.*, vol. 5, no. 1, pp. 7–9, Jan. 1999.

[35] M. Ritala and M. Leskelä, "Atomic layer epitaxy - a valuable tool for nanotechnology?," *Nanotechnology*, vol. 10, no. 1, pp. 19–24, Mar. 1999.

[36] T. Suntola, "Atomic layer epitaxy," *Thin Solid Films*, vol. 216, no. 1, pp. 84–89, Aug. 1992.

[37] D. Kim, J. D. Doll, and D. L. Freeman, "Dynamic path integral methods: A maximum entropy approach based on the combined use of real and imaginary time quantum Monte Carlo data," *J. Chem. Phys.*, vol. 108, no. 10, pp. 3871–3875, Mar. 1998.

[38] K.-E. Elers *et al.*, "Atomic layer deposition of WxN/TiN and WNxCy/TiN nanolaminates," *Thin Solid Films*, vol. 434, no. 1–2, pp. 94–99, Jun. 2003.

[39] S. Li, C. Q. Sun, and H. S. Park, "Grain boundary structures of atomic layer deposited TiN," *Thin Solid Films*, vol. 504, no. 1–2, pp. 108–112, May 2006.

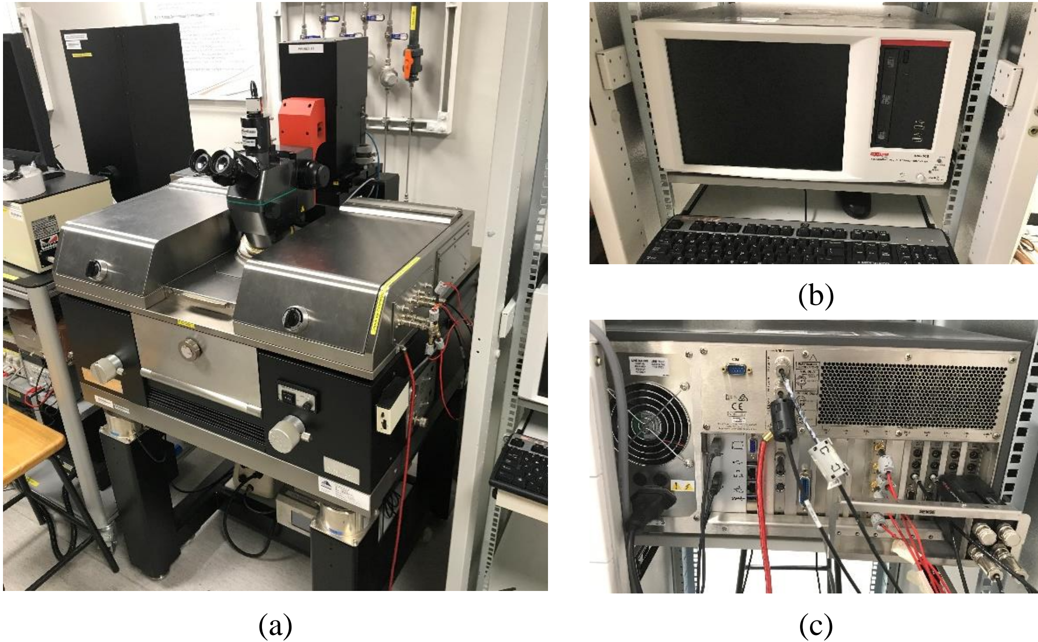
Chapter 5 Electrical Characterization of Three-Dimensional Embedded Capacitor

5.1 Introduction

In this chapter, we discuss the electrical performance of 3-D embedded capacitors based on the results of their capacitance-voltage (*C*-*V*) and current-voltage (*I*-*V*) characterizations. Firstly, the characterization setup is described for both measurement equipment and test vehicles. Then, one set of *C*-*V* characterizations is performed on the test vehicles to extract their capacitance. The results of all six types of test vehicles are compared with the theoretical results calculated based on the electrical model built in Chapter 2. The voltage coefficients of capacitance are also extracted with the other set of *C*-*V* characterizations. Finally, *I*-*V* characterizations are performed on all the test vehicles to evaluate their leakage current and breakdown voltage. After that, the data are normalized to current density-electrical field strength results and different types of leakage current conduction mechanisms are identified for these test vehicles.

5.2 Characterization Setup

The correct characterization setup is essential for the successful electrical characterizations of 3-D embedded capacitors. After the fabrication, the samples were loaded into a Cascade Microtech 200 mm shielded probe system, and a Keithley 4200-SCS parameter analyzer was used for *C-V* and *I-V* measurements. Figure 5.1(a) shows the probe system on a vibration isolation table, and Figure 5.1(b) and (c) show the front side and back side of the parameter analyzer, respectively.



(a) (b) (c)

Figure 5.1: Equipment used for electrical characterizations: (a) the Cascade Microtech 200 mm shielded probe system on a vibration isolation table and the Keithley 4200-SCS parameter analyzer from (b) the front and (c) the back.

The top views of the de-embedded structure and the embedded structure of the test vehicles are shown in Figure 5.2(a) and (b), respectively. In the figure, the acronym "TE" refers to the top electrode while "BE" refers to the bottom electrode. The irregular shape of the bottom electrode is due to the wet etching of the Al_2O_3 layer at a random location to open a contact window for the bottom electrode. Since all test vehicles on a piece of sample share the same blanket bottom electrode, the capacitance of each test vehicle is determined by the size of its patterned top electrode. The design of the de-embedded structure and embedded structure has been described

in Chapter 2. Only one planar metal-insulation-metal (MIM) capacitor is included in a de-embedded structure as a benchmark for comparison; while an extra 3×3 array (9 units) of 3-D embedded capacitors are included in an embedded structure in addition to a planar MIM capacitor. Both de-embedded and embedded structures have the same planar area, so that the net contribution of capacitance from nine units of 3-D embedded capacitors can be extracted based on the capacitance difference between a de-embedded structure and its corresponding embedded structure. The placements of two probes are shown in Figure 5.2(c): one probe tip was connected to a top electrode and the other probe tip was connected to a bottom electrode. The same configuration was applied to both *C*-*V* and *I*-*V* measurements. Figure 5.2(d) shows the actual probe tips in contact with top and bottom electrode of an embedded structure test vehicle under a microscope. The picture shows that the planar area of both de-embedded and embedded structures varies from 200×100, 400×200, 600×300, 800×400, to 1000×500 μm^2 to accommodate trenches with a radius ranging from 5, 10, 15, 20 to 25 μm.

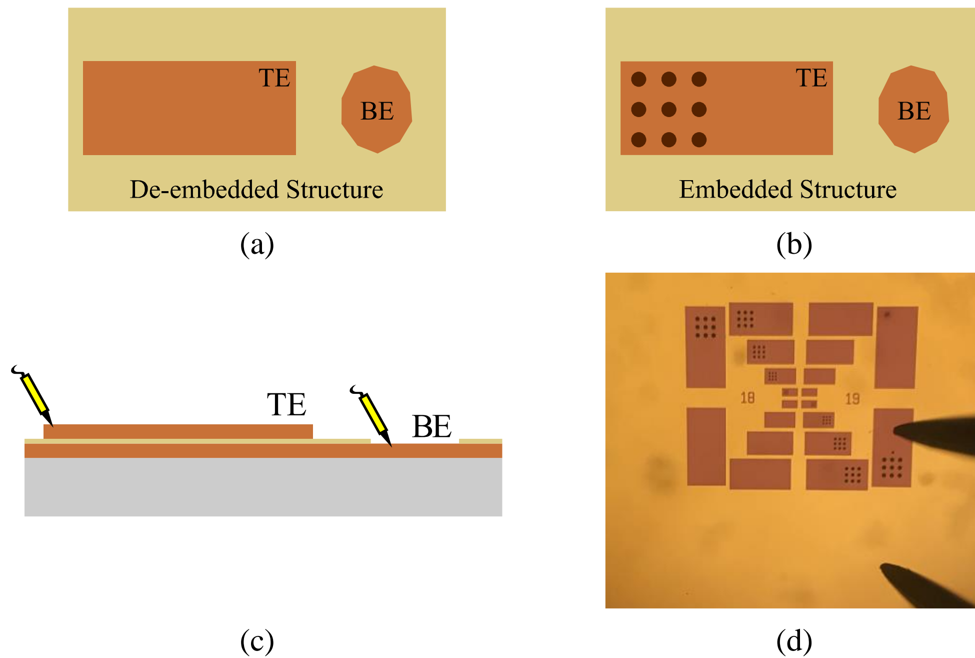


Figure 5.2: (a) Top view of a de-embedded structure, (b) top view of an embedded structure, (c) cross-sectional view of the characterization configuration, and (d) microscopic picture of the probe tips in contact with the top and bottom electrodes.

5.3 Electrical Capacitance-Voltage Characterization

In this study, different C-V characterizations were performed on the test vehicles using Keithley 4200SCS. Firstly, all the test vehicles were characterized at 100 kHz without voltage bias. From that, the capacitance of the de-embedded and embedded structures was extracted from all four types of test vehicles. Then, the measurement results were compared with the simulation results, which are based on the analytical model built in Chapter 3. Next, the capacitance density was calculated as the ratio of the capacitance and its corresponding effective planar surface area. Finally, a few more other C-V characterizations with bias of -5 V to +5 V were performed at 100 kHz on the ALD type test vehicles to investigate the effect of surface roughness on the electrical performance of ALD 3-D embedded capacitors.

Firstly, the measurement results of capacitance are grouped under two major categories (the ALD type and the sputtering type), which are tabulated in Table 5.1. The ALD type test vehicles comprise MIM layers of 50 nm TiN/10 nm Al_2O_3/50 nm TiN, whereas the sputtering type test vehicles comprise MIM layers of 400 nm TiN/30 nm Al_2O_3/400 nm TiN. In each type, one set of results is shown for the de-embedded structure, and two sets of results are shown for the embedded structures. This is because both rough-ALD and smooth-ALD test vehicles have the same de-embedded structures, but their structures are different due to different trenches etched with two DRIE recipes. This happened to the sputtering type test vehicles as well. According to the design, the capacitance of planar capacitors in the de-embedded test vehicles increases by a factor of 1×, 4×, 9×, 16×, 25× for both ALD and sputtering type test vehicles, as the size of the top electrodes increases from 100 μm × 200 μm, 200 μm × 400 μm, 300 μm × 600 μm, and 400 μm × 800 μm to 500 μm × 1000 μm, respectively. The results of the *C-V* measurements agree quite well with the design: the capacitance increases from 160.7 to 3800.3 pF gradually by a factor of 1.0×, 4.0×, 8.8×, 15.4×, 23.6× for the ALD de-embedded structures. The capacitance increases from 43.9 to 1085.0 pF gradually by a factor of 1.0×, 4.0×, 8.9×, 15.8×, 24.7× for the sputtering de-embedded structures.

However, the results show that the capacitance deviates more from the ideal value when the size of the top electrode increases. Two possible explanations are

proposed: (1) the deviation may be due to the fringing effect of capacitance, which is stronger for the ones with a smaller surface area and weaker for the ones with a larger surface area; or (2) it may be caused by the increasing parasitic resistance of the ones with a larger surface area, combined with the equivalent series circuit model used in the parameter analyzer. Each capacitance of the embedded test vehicles is higher than that of their de-embedded counterparts due to extra contribution from the trench structures, as expected. It is also found that the capacitance ratio between an ALD de-embedded structure is about 3.6 times higher than its sputtering counterpart with the same surface area, which generally agrees with the design of a three times thinner dielectric layer for ALD test vehicles. The deviation of 3.6 from 3 could be due to the minor dielectric constant variation from batch to batch and the small thickness variation for the actual dielectric layers deviating from 10 nm and 30 nm, respectively. For ALD de-embedded structure test vehicles, the capacitance of rough-ALD ones tends to be higher than that of smooth-ALD ones, even though the trenches etched by the Bosch process are slightly shallower. This is because the rough sidewall increases the total surface area for rough-ALD ones. In contrast, for sputtering de-embedded structure test vehicles, the capacitance of rough-sputtering ones is lower than that of smooth-sputtering ones due to the less conformal coverage of TiN electrodes caused by sputtering on rough sidewalls.

Table 5.1: Measured capacitance from all test vehicles at 100 KHz without voltage bias.

#	Capacitance (pF)					
	ALD			Sputtering		
	(50 nm TiN/10 nm Al_2O_3/50 nm TiN)			(400 nm TiN/30 nm Al_2O_3/400 nm TiN)		
	De-embedded structure	Embedded structure		De-embedded structure	Embedded structure	
	Planar	Rough	Smooth	Planar	Rough	Smooth
1	160.7	267.6	259.4	43.9	47.5	52.1
2	638.7	866.0	860.0	174.2	187.9	209.4
3	1415.7	1782.5	1732.6	390.7	416.8	460.8
4	2472.1	2954.8	2929.6	694.2	731.2	803.4
5	3800.3	4412.8	4425.5	1085.0	1178.5	1223.7

Next, the capacitance difference of various de-embedded and embedded test vehicles is calculated and compared with the simulation results, as shown in Figure 5.3. The simulation was carried out based on the first-order model constructed in Chapter 3, the physical properties of MIM layers, and the trench geometries measured in Chapter 4. For simplicity, perfect conformal coverage is assumed for all layers of the test vehicles. The equation involved is provided below:

$$\text{Capacitance} = \frac{2\pi \times \varepsilon_0 \times \varepsilon_{high-\kappa} \times H}{\ln\left(\frac{R_{trench} - T_{ins} - T_{el2}}{R_{trench} - T_{ins} - T_{el2} - T_{high-\kappa}}\right)} \tag{5.1}$$

For both rough-ALD and smooth-ALD test vehicles, the measurement results are generally in agreement with the simulation results, because ALD provides conformal layer coverage on the trenches. In Figure 5.3(a) and (b), the simulation results deviate from the measurement results by -21.3%, -10.3%, -8.2%, 3.8%, and -1.0% for rough-ALD ones, as the trench diameter increases from 10, 20, 30, 40 to 50 μm. In contrast, the deviation is -8.6%, 1.8%, 14.6%, 12.7%, and 3.6% for smooth-ALD ones. It can be seen from the comparison that the measurement results of rough-ALD test vehicles are higher than their corresponding simulation results, which is probably due to the fact that the roughness of the sidewalls increases the effective surface area along the sidewalls for rough-ALD ones: thus, leading to higher measured capacitance. In contrast, for both rough-sputtering and smooth-sputtering test vehicles, the simulation results of sputtering samples are significantly higher than their corresponding measurement results by up to 4.5× because of the poor step coverage of the sputtered electrodes. In Figure 5.3(c) and (d), the simulation results deviate from the measurement results by 450.0%, 251.1%, 204.2%, 195.9%, and 52.8% for rough-sputtering ones, as the trench diameter increases from 10, 20, 30, 40 to 50 μm; whereas the deviation is 159.8%, 50.9%, 22.1%, 11.3%, and 10.0% for smooth-sputtering ones. It is evident that the rough surface makes the sidewall coverage of sputtered electrodes even worse, especially for high aspect ratio trenches. Nevertheless, the deviation drops to less than 22.1% for smooth-sputtering test

vehicles when the trench diameter increases to greater than 30 μm. This result suggests that the sputtered electrodes go much deeper into the trenches as their aspect ratio decreases to lower than 2:1. In conclusion, the analytical simulation model can be used to predict the capacitance for all ALD type 3-D embedded capacitors, but it is only applicable for sputtering type 3-D embedded capacitors implemented in trenches with smooth sidewalls (30 nm peak-to-valley distance) and a low aspect ratio (2:1).

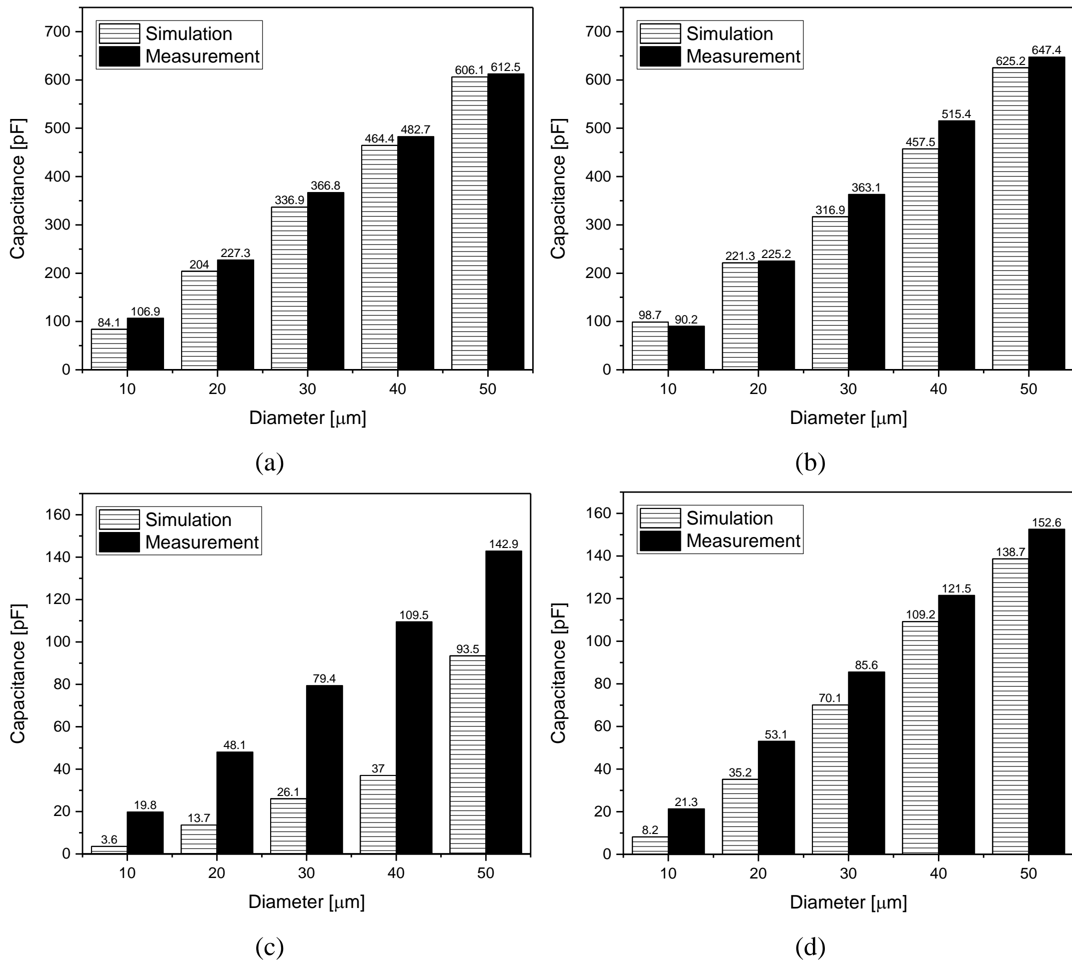


Figure 5.3: Comparison of capacitance between the simulation results and the measurement results for all test vehicles: (a) rough-ALD, (b) smooth-ALD, (c) rough-sputtering, and (d) smooth-sputtering.

Next, the effective capacitance density of the 3-D embedded capacitors was calculated by finding the ratio of capacitance and the effective planar surface area.

The measurement results of the former capacitor have been reported above, and the measurements of the latter 3-D embedded capacitor was calculated according to the illustration shown in Figure 3.7. The ALD type stacked layers of 10 nm SiO_2/50 nm TiN/10 nm Al_2O_3/50 nm TiN are much thinner than the sputtering type stacked layers of 10 nm SiO_2/400 nm TiN/30 nm Al_2O_3/400 nm TiN. The calculated results of capacitance density are shown in Table 5.2. For the ALD type test vehicles, the capacitance density varies from 3327.6 to 3856.4 nF/mm^2. For the sputtering type test vehicles, the capacitance density varies from 30.6 to 227.6 nF/mm^2. Compared with other state-of-the-art trench capacitor technologies of less than 1000 nF/mm^2, this work provides an extremely high capacitance density of up to 3856.4 nF/mm^2 [1]–[5]. It has also been demonstrated by simulation in Chapter 3 that the capacitance density of a 3-D embedded capacitor can be up to ~13× higher than a MIMIM trench capacitor when the same physical design parameters are applied. Thus, it can be concluded that the capacitance density is greatly enhanced when MIM layers are embedded in TSV trenches to form 3-D embedded capacitors. Besides, ALD is proven as an excellent choice of the electrode deposition method for high performance 3-D embedded capacitors due to its superb step coverage, whereas sputtering can be considered a potential candidate for low cost, moderate performance applications due to its ease of integration (as described in Chapter 3).

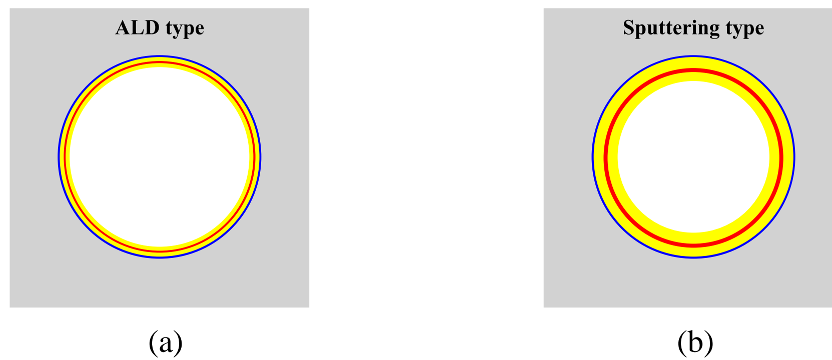


Figure 5.4: Effective planar surface area of (a) ALD type test vehicles with stacked layers of 10 nm SiO_2/50 nm TiN/10 nm Al_2O_3/50 nm TiN and (b) sputtering type test vehicles with stacked layers of 10 nm SiO_2/400 nm TiN/30 nm Al_2O_3/400 nm TiN.

Table 5.2: Calculated capacitance density for all test vehicles.

	ALD (10 nm SiO_2/50 nm TiN/ 10 nm Al_2O_3/ 50 nm TiN)					Sputtering (10 nm SiO_2/400 nm TiN/ 30 nm Al_2O_3/ 400 nm TiN)				
	Capacitance Difference (pF)		Surface area (mm^2)	Capacitance Density (nF/mm^2)		Capacitance Difference (pF)		Surface area (mm^2)	Capacitance density (nF/mm^2)	
	Rough	Smooth		Rough	Smooth	Rough	Smooth		Rough	Smooth
1	106.9	98.7	3.24×10^{-5}	3327.6	3072.4	3.6	8.2	1.18×10^{-4}	30.6	69.7
2	227.3	221.3	6.48×10^{-5}	3517.3	3424.4	13.7	35.2	2.40×10^{-4}	57.0	146.4
3	366.8	316.9	9.72×10^{-5}	3776.6	3262.9	26.1	70.1	3.64×10^{-4}	71.8	192.9
4	482.7	457.5	1.30×10^{-4}	3723.9	3529.5	37.0	109.2	4.86×10^{-4}	76.1	224.5
5	612.5	625.2	1.62×10^{-4}	3778.0	3856.4	93.5	138.7	6.09×10^{-4}	153.5	227.6

Lastly, a few sets of C-V characterizations with bias from -5 V to +5 V were performed at 100 kHz on the ALD type test vehicles at five different spots across the wafers. The aim was to study the effects of sidewall roughness on the electrical performance of ALD type test vehicles despite its excellent step coverage. The measurement results of those test vehicles were then fit by the following second order polynomial equations to extract their voltage coefficients of capacitance (VCCs):

$$C(V) = C_o(\alpha V^2 + \beta V + 1) \quad (5.2)$$

where C_o is the capacitance at zero bias, α is the quadratic VCC, and β is the linear VCC [6]–[12]. The results are tabulated in Table 5.3. Mostly, the quadratic and linear VCCs of embedded smooth-ALD test vehicles are similar to those of de-embedded ALD planar test vehicles, whereas those of embedded rough-ALD test vehicles are distant from the general trend for some samples. For example, in the smallest test vehicles (trench diameters = 10 μm), the average value of both quadratic and linear VCCs are calculated to be 1.60 ppm/V^2 and 4.93 ppm/V, respectively. The extracted VCCs of de-embedded and embedded smooth-ALD test vehicles are consistent with the average values, with a deviation less than 12.2%. But for embedded rough-ALD test vehicles, the deviation of quadratic VCC goes up to 27.8%, and the deviation of linear VCC even rises up to 35.8%. The value of quadratic VCC is correlated with polarization condition of the dielectric layer, and the value of linear VCC is determined by the amount of trapped charges in the dielectric layer [13], [14]. Therefore, these C-V characterization results suggest that the dielectric composition and the total amount of trapped charges in the dielectric layer become instable as trench sidewall roughness becomes higher in spite of the conformal deposition of the stacked layer by ALD. This physical insight can be useful in the performance optimization and future assessment of long-term reliability of ALD type 3-D embedded capacitors.

Table 5.3: Voltage coefficients of capacitance of all test vehicles.

De-Embedded Structure of ALD Type Test Vehicles (ppm/V² for α and ppm/V² for β)									
100 μm × 200 μm		200 μm × 400 μm		300 μm × 600 μm		400 μm × 800 μm		500 μm × 1000 μm	
α	β	α	β	α	β	α	β	α	β
1.57×10^{-3}	4.33×10^{-3}	1.59×10^{-3}	4.70×10^{-3}	1.56×10^{-3}	5.06×10^{-3}	1.57×10^{-3}	4.32×10^{-3}	1.51×10^{-3}	5.50×10^{-3}
1.60×10^{-3}	4.31×10^{-3}	1.57×10^{-3}	5.08×10^{-3}	1.59×10^{-3}	4.62×10^{-3}	1.56×10^{-3}	4.68×10^{-3}	1.52×10^{-3}	5.45×10^{-3}
1.60×10^{-3}	4.33×10^{-3}	1.59×10^{-3}	5.07×10^{-3}	1.57×10^{-3}	5.02×10^{-3}	1.57×10^{-3}	4.62×10^{-3}	1.75×10^{-3}	3.89×10^{-3}
1.60×10^{-3}	4.51×10^{-3}	1.62×10^{-3}	5.16×10^{-3}	1.57×10^{-3}	5.08×10^{-3}	1.54×10^{-3}	5.04×10^{-3}	1.94×10^{-3}	2.99×10^{-3}
1.61×10^{-3}	4.48×10^{-3}	1.63×10^{-3}	4.77×10^{-3}	1.59×10^{-3}	5.12×10^{-3}	1.62×10^{-3}	4.46×10^{-3}	2.00×10^{-3}	3.32×10^{-3}
Embedded Structure of Smooth-ALD Type Test Vehicles									
Diameter = 10 μm		Diameter = 20 μm		Diameter = 30 μm		Diameter = 40 μm		Diameter = 50 μm	
α	β	α	β	α	β	α	β	α	β
1.55×10^{-3}	4.35×10^{-3}	1.57×10^{-3}	4.58×10^{-3}	1.61×10^{-3}	5.03×10^{-3}	1.56×10^{-3}	4.89×10^{-3}	1.60×10^{-3}	2.86×10^{-3}
1.57×10^{-3}	4.30×10^{-3}	1.56×10^{-3}	4.95×10^{-3}	1.55×10^{-3}	4.90×10^{-3}	1.56×10^{-3}	4.99×10^{-3}	1.58×10^{-3}	3.50×10^{-3}
1.54×10^{-3}	4.25×10^{-3}	1.58×10^{-3}	4.92×10^{-3}	1.55×10^{-3}	4.94×10^{-3}	1.61×10^{-3}	5.08×10^{-3}	1.58×10^{-3}	3.33×10^{-3}
1.56×10^{-3}	4.93×10^{-3}	1.60×10^{-3}	4.70×10^{-3}	1.60×10^{-3}	4.76×10^{-3}	1.72×10^{-3}	4.27×10^{-3}	1.62×10^{-3}	2.87×10^{-3}
1.59×10^{-3}	4.71×10^{-3}	1.57×10^{-3}	4.99×10^{-3}	1.58×10^{-3}	5.07×10^{-3}	1.61×10^{-3}	4.76×10^{-3}	1.56×10^{-3}	3.44×10^{-3}
Embedded Structure of Rough-ALD Type Test Vehicles									
Diameter = 10 μm		Diameter = 20 μm		Diameter = 30 μm		Diameter = 40 μm		Diameter = 50 μm	
α	β	α	β	α	β	α	β	α	β
1.56×10^{-3}	5.35×10^{-3}	1.52×10^{-3}	5.56×10^{-3}	1.50×10^{-3}	5.44×10^{-3}	1.51×10^{-3}	5.50×10^{-3}	1.50×10^{-3}	5.29×10^{-3}
1.58×10^{-3}	5.27×10^{-3}	1.58×10^{-3}	5.33×10^{-3}	1.63×10^{-3}	4.70×10^{-3}	1.52×10^{-3}	5.45×10^{-3}	1.68×10^{-3}	4.14×10^{-3}
1.85×10^{-3}	3.17×10^{-3}	1.69×10^{-3}	4.34×10^{-3}	1.75×10^{-3}	3.98×10^{-3}	1.75×10^{-3}	3.89×10^{-3}	1.74×10^{-3}	3.79×10^{-3}
1.77×10^{-3}	3.78×10^{-3}	1.88×10^{-3}	3.17×10^{-3}	1.98×10^{-3}	2.74×10^{-3}	1.94×10^{-3}	2.99×10^{-3}	1.69×10^{-3}	4.23×10^{-3}
2.04×10^{-3}	2.82×10^{-3}	2.07×10^{-3}	2.09×10^{-3}	2.18×10^{-3}	2.62×10^{-3}	2.00×10^{-3}	3.32×10^{-3}	1.84×10^{-3}	3.23×10^{-3}

5.4 Electrical Current-Voltage Characterization

In this section, the *I-V* characterizations results of all test vehicles are firstly presented. Then they are normalized to current density-electric field (*J-E*) plots based on their respective surface area and dielectric layer thickness. Finally, the analysis of the conduction mechanism is done for the test vehicles of 3-D embedded capacitors.

Firstly, *I-V* characterizations were performed on all test vehicles with the same probing configuration as illustrated in Figure 5.2(c). The *I-V* characterization results of ALD type test vehicles with various geometries are shown in Figure 5.5, Figure 5.6, and Figure 5.7, which refer to the de-embedded ALD test vehicles, the embedded rough-ALD ones, and the embedded smooth-ALD ones, respectively. Similarly, the *I-V* characterization results of sputtering type test vehicles with various geometries are shown in Figure 5.8, Figure 5.9, and Figure 5.10, which refer to the de-embedded sputtering test vehicles, the embedded rough-sputtering ones, and the embedded smooth-sputtering ones, respectively. "D" in the plots means "diameter." For example, "D10" refers to the 100 μm × 200 μm planar test vehicle for the de-embedded structure or the test vehicle with 10 μm diameter trenches for the embedded structures. For ALD type 3-D embedded capacitors, the *I-V* characterization results of various de-embedded and embedded structure test vehicles exhibit similar current conduction behaviors: the current rises sharply with a bias increasing from 0 V to ~1.5 V, saturates with a bias ranging from ~1.5 V to ~4.5 V, and takes off afterwards until dielectric breakdown happens at ~9.5 V. For sputtering type 3-D embedded capacitors, the *I-V* characterization results of various de-embedded and embedded structure test vehicles also exhibit similar current conduction behaviors: the current increases gradually with a bias from 0 V to ~10.0 V (slightly after 10.0. V for de-embedded structures, but well below 10.0 V for embedded structures), and it rises quickly until dielectric breakdown occurs at ~26.0 V.

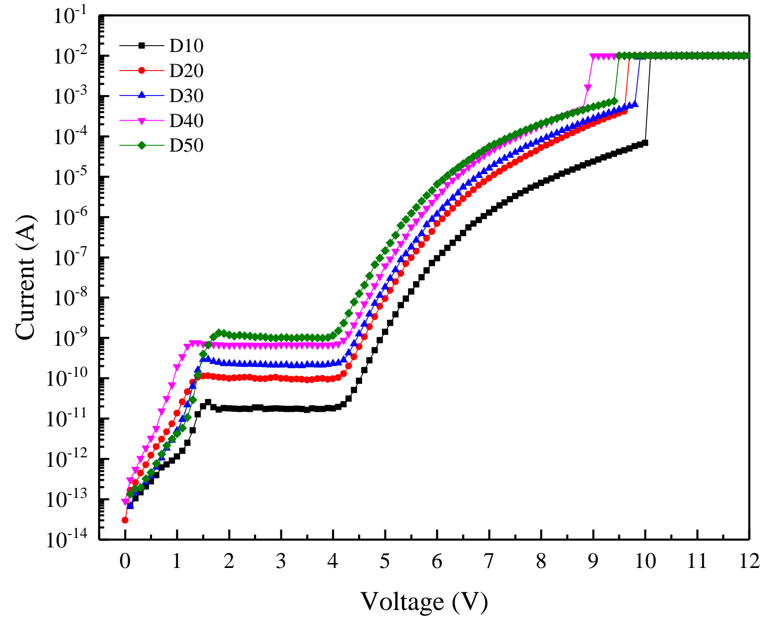


Figure 5.5: *I*-*V* characterization results of de-embedded ALD type test vehicles.

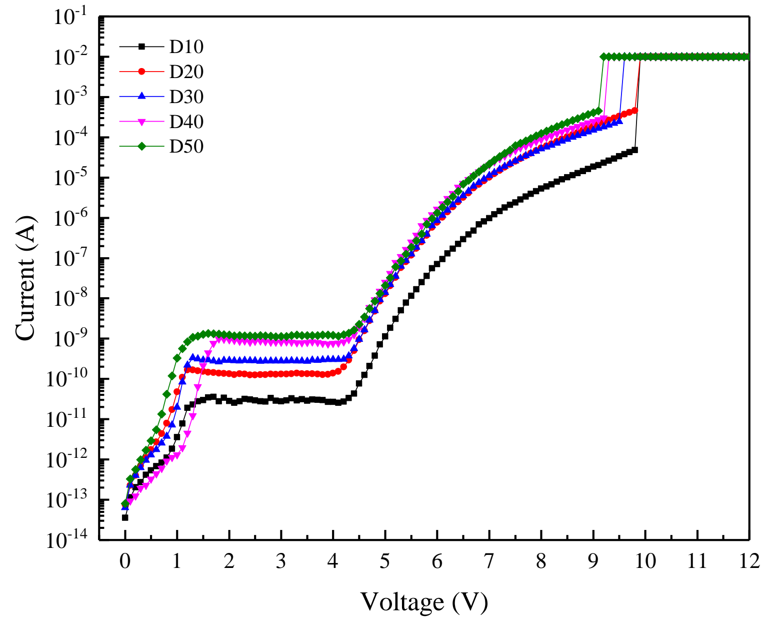


Figure 5.6: *I*-*V* characterization results of embedded rough-ALD test vehicles.

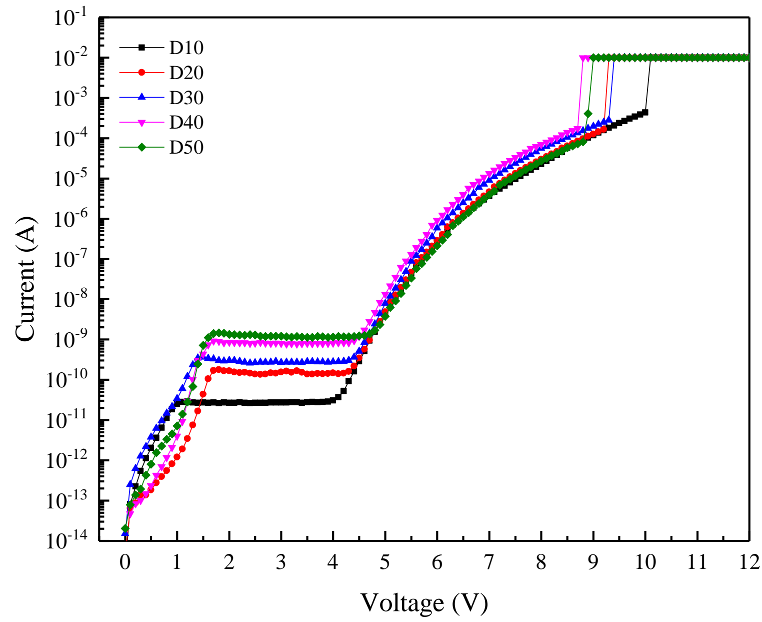


Figure 5.7: *I-V* characterization results of embedded smooth-ALD test vehicles.

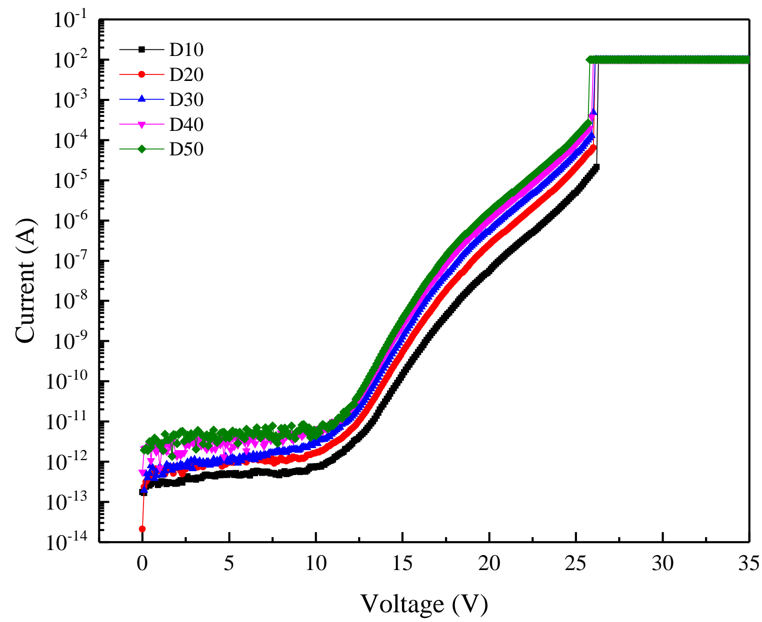


Figure 5.8: *I-V* characterization results of de-embedded sputtering type test vehicles.

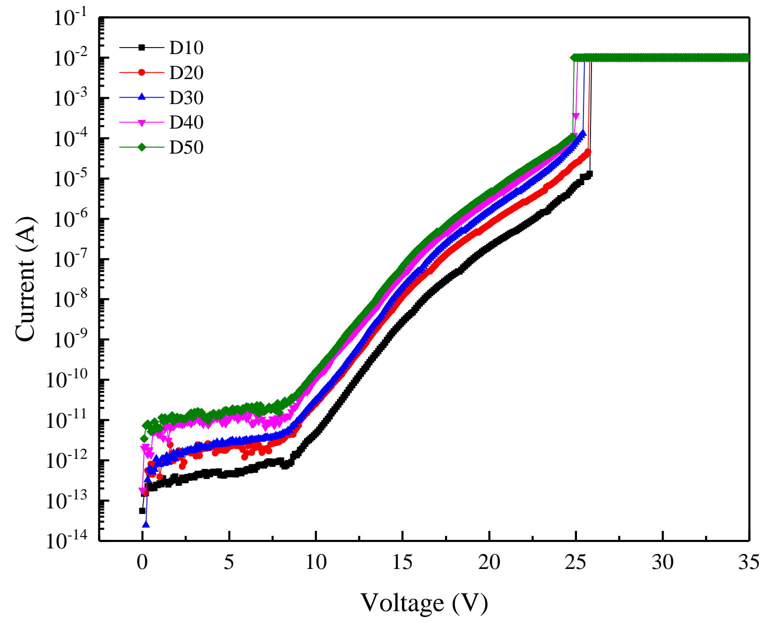


Figure 5.9: *I-V* characterization results of embedded rough-sputtering test vehicles.

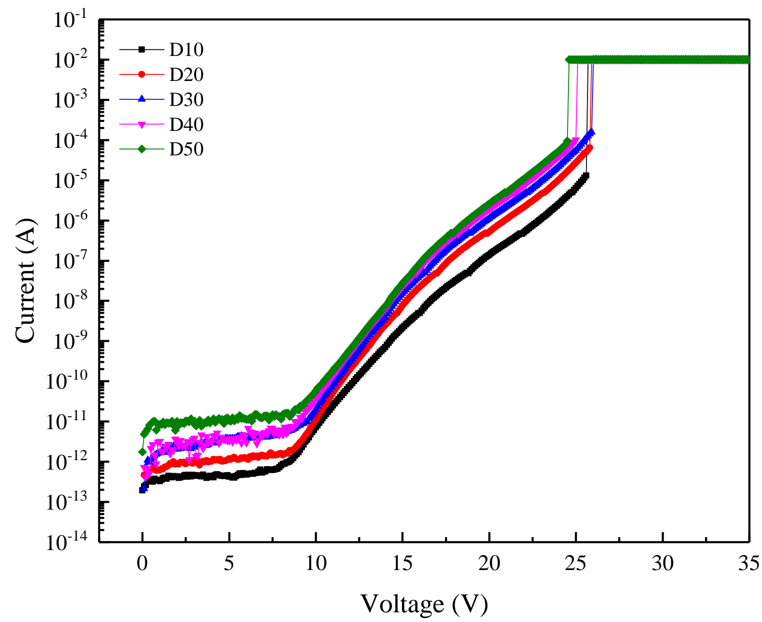


Figure 5.10: *I-V* characterization results of embedded smooth-sputtering test vehicles.

The characterization results are normalized based on their surface area and dielectric layer thickness to obtain *J-E* plots for fair comparison between different test vehicles. For simplicity, only *J-E* plots for D30 ALD and sputtering type D30 test vehicles are shown for further detailed analysis in Figure 5.11 and Figure 5.12, respectively. For the other test vehicles with different geometries, a similar conclusion can be applied because they show similar current conduction behaviors. This shows that no significant difference of *J-E* plots can be observed for the three ALD type test vehicles in Figure 5.11, whereas the *J-E* plots of the three sputtering type test vehicles show different trends in Figure 5.12. In fact, the current densities of both embedded rough-sputtering and smooth-sputtering test vehicles mostly overlap under all bias conditions, but they are noticeably higher than that of the planar counterpart. The drastic increase in the current densities also takes place at a lower electrical field than that of the planar one (~2.8 MV/cm vs. ~3.5 MV/cm). However, the dielectric strength of these sputtering type test vehicles is at ~8MV/cm.

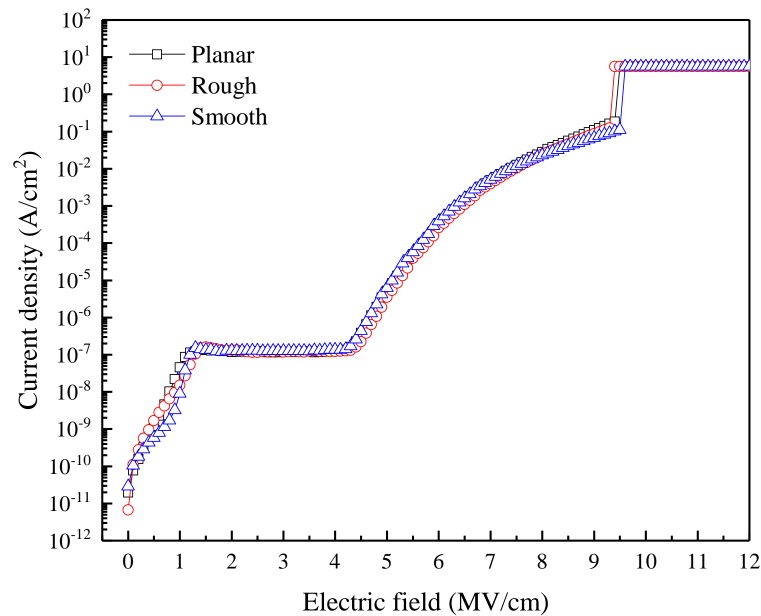


Figure 5.11: Combined *J-E* plots from the three ALD type D30 test vehicles.

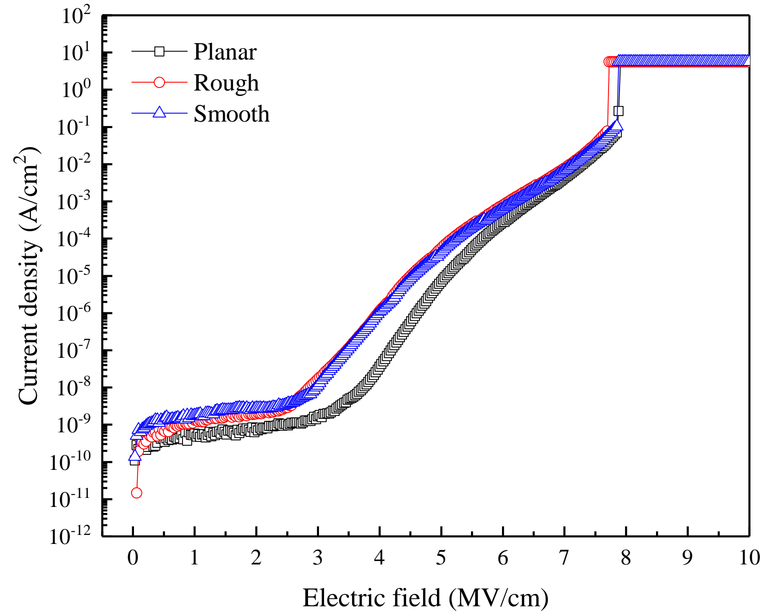


Figure 5.12: Combined *J-E* plots from the three sputtering type D30 test vehicles.

Finally, more physical insights can be obtained from the analysis of the leakage current conduction mechanisms for the 3-D embedded capacitors. The analysis is done for all of the test vehicles based on the conduction models reviewed in Ref [15], including both electrode-limited and bulk-limited conduction mechanisms [16]–[20]. In this study, four types of well-known conduction mechanisms were tried to be fitted for the Al_2O_3 layer deposited by ALD: (1) Schottky emission, (2) Fowler-Nordheim (FN) tunneling, (3) Poole-Frenkel (PF) emission, and (4) Hopping conduction.

Firstly, the Schottky emission conduction mechanism is fitted as shown in Figure 5.13 and Figure 5.14 for ALD and sputtering test vehicles, respectively. For the ALD test vehicles, reasonable physical parameters are extracted: 2.16 as the optical dielectric constant and 2.12 eV as the Schottky barrier height, respectively. However, for the sputtering test vehicles, the optical dielectric constants greater than 100 are extracted, which are too high compared with the value of 3.1 reported in the literature [21]–[26]. Thus, the Schottky emission mechanism is identified in the low bias region for the ALD test vehicles, but not for the sputtering test vehicles.

Secondly, the FN tunneling conduction mechanism is fitted as shown in Figure 5.15 and Figure 5.16 for the ALD and sputtering test vehicles, respectively. Both types of test vehicles show good linear fitting, and the extracted barrier heights ranging from 1.66 to 2.21 eV are consistent with the values calculated from the previous Schottky emission analysis. Thus, FN tunneling can be identified for all the test vehicles in the high bias region, and an energy barrier is confirmed at the TiN/Al_2O_3 interface with a height of ~ 2.0 eV.

Thirdly, the PF emission conduction mechanism is fitted as shown in Figure 5.17 and Figure 5.18 for ALD and sputtering test vehicles, respectively. PF emission can be identified in the middle bias region, because the extracted optical dielectric constants range from 1.98 to 3.69, which are close to the reported value of 3.1 [21]–[26].

Lastly, the hopping conduction mechanism is fitted as shown in Figure 5.19 and Figure 5.20 for the ALD and sputtering test vehicles, respectively. However, this conduction mechanism can only be identified for the ALD test vehicles, because the evaluated mean hopping distance of the sputtering test vehicles is much smaller than the reported value by an order of magnitude [21]–[26]. After the fitting of these four types of leakage current conduction mechanisms, all of the analytical results are summarized in Table 5.4 for comparison with bias conditions and extracted physical parameters. One observation is that the onset points of FN tunneling are consistent for all the test vehicles: implying a relatively uniform thickness of the dielectric layers. This observation confirms that the leakage current degradation of the embedded rough-sputtering and the smooth-sputtering test vehicles is not due to the thinning of the dielectric layers deposited on the vertical sidewalls. It is also worth noting that PF emission is observed at a lower field for the embedded rough-sputtering and the smooth-sputtering test vehicles than for their planar counterparts. This observation suggests that the sputtered electrodes cause more traps in the dielectric layers on the trench sidewalls than they do in the planar dielectric layers. Therefore, the higher leakage current density is attributed to the sputtering process. Since the embedded ALD type test vehicles do not suffer from leakage current density degradation, the ALD process is preferred over the sputtering process as an electrode deposition method to fabricate high performance 3-D embedded capacitors.

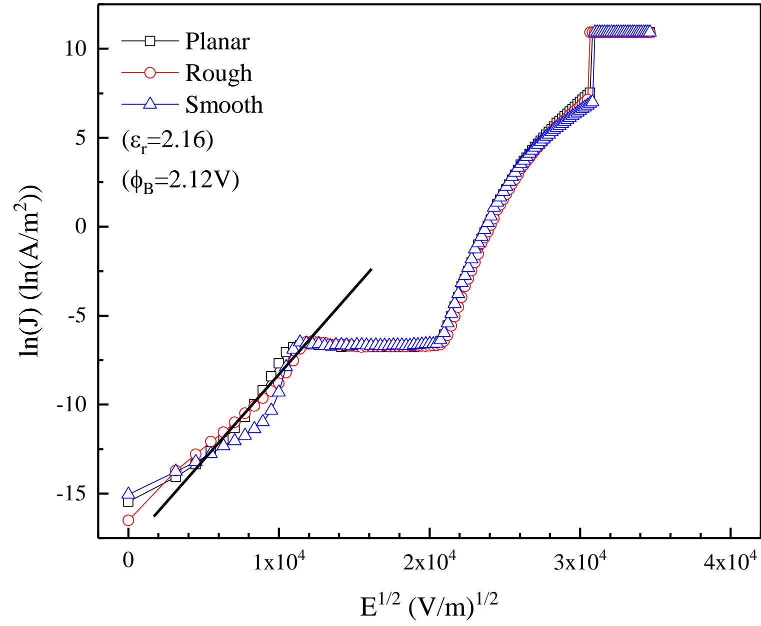


Figure 5.13: Schottky emission fitting of the three ALD type D30 test vehicles.

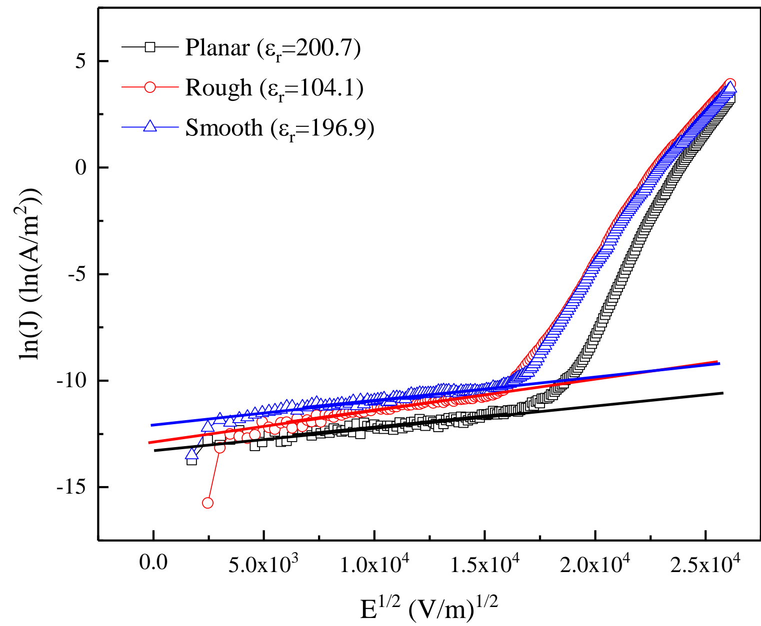


Figure 5.14: Schottky emission fitting of the three sputtering type D30 test vehicles.

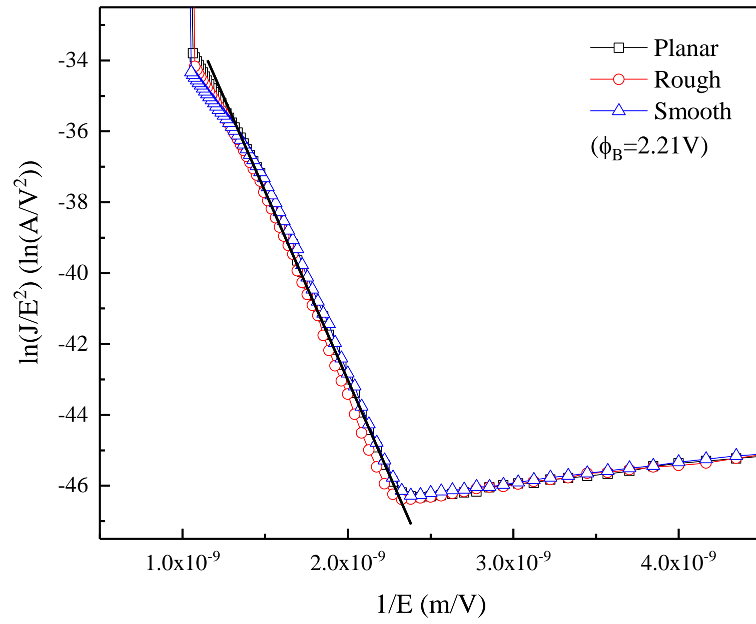


Figure 5.15: FN tunneling fitting of the three ALD type D30 test vehicles.

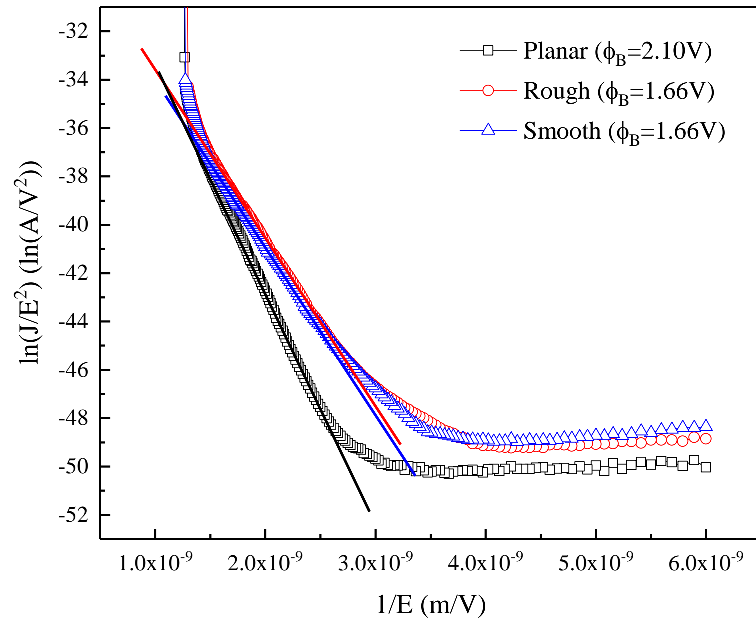


Figure 5.16: FN tunneling fitting of the three sputtering type D30 test vehicles.

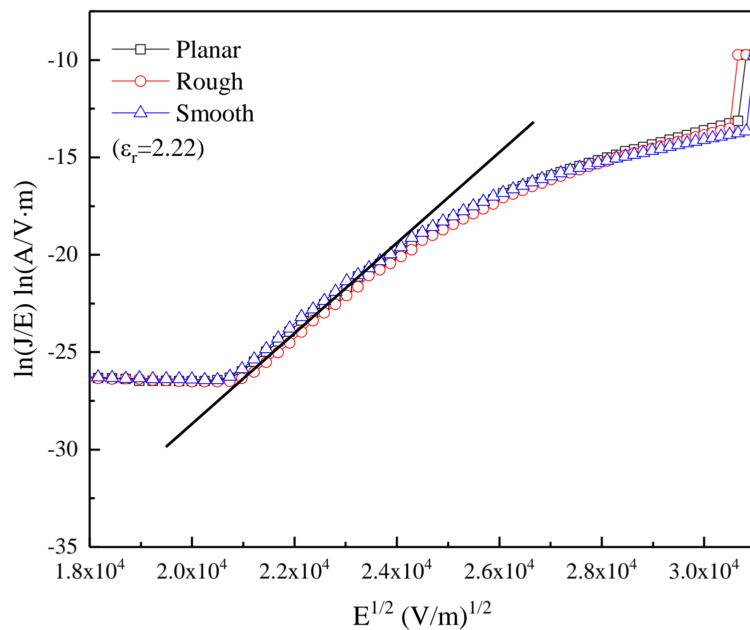


Figure 5.17: PF emission fitting of the three ALD type D30 test vehicles.

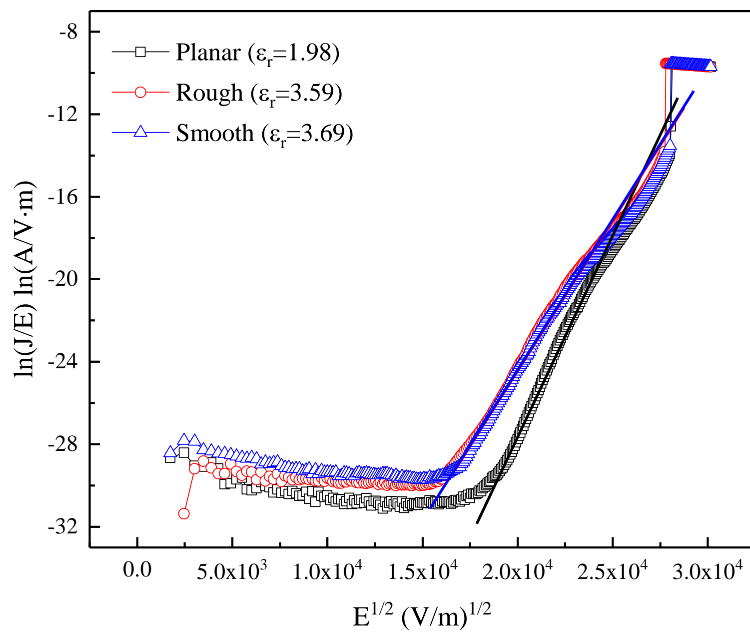


Figure 5.18: PF emission fitting of the three sputtering type D30 test vehicles.

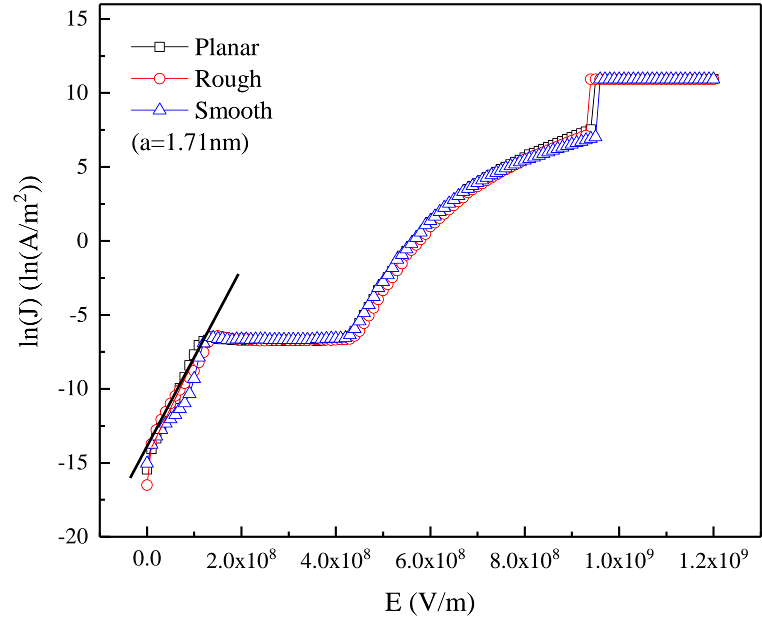


Figure 5.19: Hopping conduction fitting of the three ALD type D30 test vehicles.

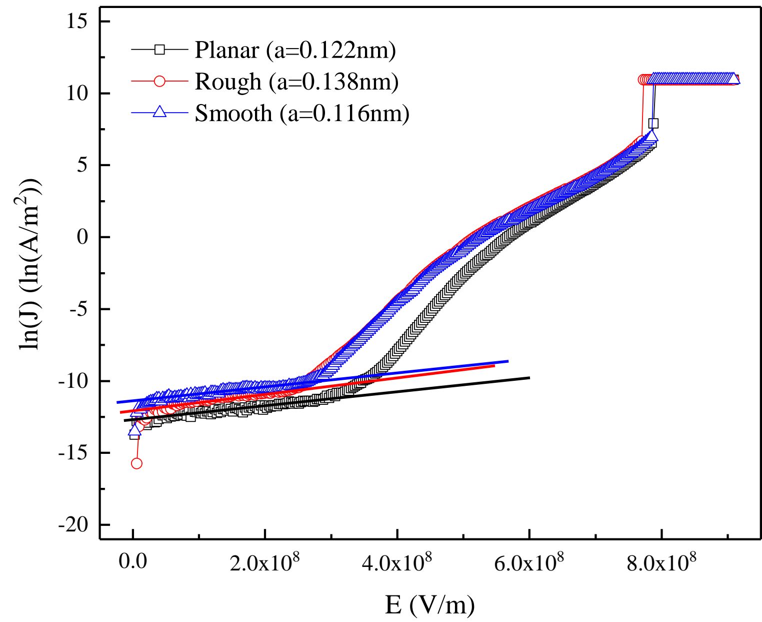


Figure 5.20: Hopping conduction fitting of the three sputtering type D30 test vehicles.

Table 5.4: A summary of leakage current conduction mechanisms.

Test Vehicles		Schottky Emission	FN Tunneling	PF Emission	Hopping Conduction
ALD type	Same	[0,1.2] MV/cm Φ_B=2.12 V ε_r=2.16	[4.1,7.2] MV/cm Φ_B=2.21V	[3.7,5.2] MV/cm ε_r=2.22	[0,1.2] MV/cm a=1.71 nm
Sputtering type	Planar	N.A.	[4.1,7.2] MV/cm Φ_B=2.1 V	[3.7,5.2] MV/cm ε_r=1.98	N.A.
	Rough	N.A.	[3.9,6.5] MV/cm Φ_B=1.66 V	[3.2,5.4] MV/cm ε_r=3.59	N.A.
	Smooth	N.A.	[4.0,6.7] MV/cm Φ_B=1.66 V	[3.0,5.3] MV/cm ε_r=3.69	N.A.

5.5 Summary

In this chapter, we evaluated the electrical performance of 3-D embedded capacitors via *C*-*V* and *I*-*V* characterizations. The characterization setup was firstly described in detail for proper probing. The *C*-*V* characterizations showed that the theoretical results of the ALD type test vehicles fit well with the measurement results due to the excellent step coverage. In contrast, the theoretical results of the sputtering type test vehicles deviated significantly from the measurement results due to the poor step coverage. Also, the capacitance density of an ALD type test vehicle can achieve an extremely high value (up to 3856.4 nF/mm^2). Furthermore, it was found that the rough sidewall can cause dielectric composition and the total amount of trapped charges in the dielectric layer becomes instable. The *I*-*V* characterizations showed that the leakage current degradation happened to the de-embedded sputtering test vehicles, but not to the de-embedded ALD test vehicles. After that, various physical parameters were extracted from the *J*-*E* plots. From the analysis of conduction mechanisms, it was concluded that Schottky emission, FN tunneling, PF emission, and hopping conduction were identified for the ALD type test vehicles; but only FN tunneling and PF emission were identified for the sputtering type test vehicles.

References

[1] M. Brunet and P. Kleimann, "High-density 3-D capacitors for power systems on-chip: Evaluation of a technology based on silicon submicrometer pore arrays formed by electrochemical etching," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4440–4448, Sep. 2013.

[2] P. Banerjee, I. Perez, L. Henn-Lecordier, S. B. Lee, and G. W. Rubloff, "Nanotubular metal–insulator–metal capacitor arrays for energy storage," *Nat. Nanotechnol.*, vol. 4, no. 5, pp. 292–296, May 2009.

[3] J. H. Klootwijk *et al.*, "Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 740–742, Jul. 2008.

[4] M. Kemell, M. Ritala, M. Leskelä, E. Ossei-Wusu, J. Carstensen, and H. Föll, "Si/Al2O3/ZnO:Al capacitor arrays formed in electrochemically etched porous Si by atomic layer deposition," *Microelectron. Eng.*, vol. 84, no. 2, pp. 313–318, Feb. 2007.

[5] F. Roozeboom *et al.*, "ALD options for Si-integrated ultrahigh-density decoupling capacitors in pore and trench designs," in *ECS Transactions*, 2007, vol. 3, pp. 173–181.

[6] V. Mikhelashvili, G. Eisenstein, and A. Lahav, "High capacitance density metal-insulator-metal structure based on Al2O3–HfTiO nanolaminate stacks," *Appl. Phys. Lett.*, vol. 90, no. 1, p. 013506, Jan. 2007.

[7] S. Bécu, S. Crémer, and J.-L. Autran, "Microscopic model for dielectric constant in metal-insulator-metal capacitors with high-permittivity metallic oxides," *Appl. Phys. Lett.*, vol. 88, no. 5, p. 052902, Jan. 2006.

[8] L. Goux, H. Vander Meeren, and D. J. Wouters, "Metallorganic chemical vapor deposition of Sr-Ta-O and Bi-Ta-O films for backend integration of high-k capacitors," *J. Electrochem. Soc.*, vol. 153, no. 7, p. F132, 2006.

[9] C. Durand *et al.*, “Electrical property improvements of yttrium oxide-based metal-insulator-metal capacitors,” *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 24, no. 3, pp. 459–466, May 2006.

[10] H. Hu *et al.*, “Physical and electrical characterization of HfO2 metal–insulator–metal capacitors for Si analog circuit applications,” *J. Appl. Phys.*, vol. 94, no. 1, pp. 551–557, Jul. 2003.

[11] S. Blonkowski, M. Regache, and A. Halimaoui, “Investigation and modeling of the electrical properties of metal–oxide–metal structures formed from chemical vapor deposited Ta2O5 films,” *J. Appl. Phys.*, vol. 90, no. 3, pp. 1501–1508, Aug. 2001.

[12] J. A. Babcock *et al.*, “Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics,” *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230–232, May 2001.

[13] D. Kannadassan, R. Karthik, M. Shojaei Baghini, and P. S. Mallick, “Modeling the voltage nonlinearity of high-k MIM capacitors,” *Solid. State. Electron.*, vol. 91, pp. 112–117, Jan. 2014.

[14] C. Besset, S. Bruyère, S. Blonkowski, S. Crémer, and E. Vincent, “MIM capacitance variation under electrical stress,” *Microelectron. Reliab.*, vol. 43, no. 8, pp. 1237–1240, Aug. 2003.

[15] F.-C. Chiu, “A review on conduction mechanisms in dielectric films,” *Adv. Mater. Sci. Eng.*, vol. 2014, pp. 1–18, 2014.

[16] J. Cohen, “Mechanisms of electrical conduction in thin insulating films,” *J. Appl. Phys.*, vol. 35, no. 10, pp. 3056–3057, Oct. 1964.

[17] A. Davison, “The synthesis and characterization of inorganic compounds,” *Science (80-.).*, vol. 170, no. 3961, pp. 966–966, Nov. 1970.

[18] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proc. R. Soc. A Math. Phys. Eng. Sci.*, vol. 145, no. 855, pp. 523–529, Jul. 1934.

[19] J. J. O'Dwyer, "Theory of dielectric breakdown in solids," *J. Electrochem. Soc.*, vol. 116, no. 2, p. 239, 1969.

[20] K. C. Kao, W. Hwang, and S. Choi, "Electrical transport in solids," *Phys. Today*, vol. 36, no. 10, pp. 90–90, Oct. 1983.

[21] H. Spahr, S. Montzka, J. Reinker, F. Hirschberg, W. Kowalsky, and H.-H. Johannes, "Conduction mechanisms in thin atomic layer deposited Al2O3 layers," *J. Appl. Phys.*, vol. 114, no. 18, p. 183714, Nov. 2013.

[22] M. Specht, M. Städele, S. Jakschik, and U. Schröder, "Transport mechanisms in atomic-layer-deposited Al2O3 dielectrics," *Appl. Phys. Lett.*, vol. 84, no. 16, pp. 3076–3078, Apr. 2004.

[23] T.-H. Chiang and J. F. Wager, "Electronic conduction mechanisms in insulators," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 223–230, Jan. 2018.

[24] N. Novkovski, A. Paskaleva, A. Skeparovski, and D. Spassov, "Analysis of conduction and charging mechanisms in atomic layer deposited multilayered HfO 2 /Al 2 O 3 stacks for use in charge trapping flash memories," *Adv. Condens. Matter Phys.*, vol. 2018, pp. 1–9, 2018.

[25] Y. Chang *et al.*, "Surface preparation and post thermal treatment effects on interface properties of thin Al2O3 films deposited by ALD," *Microelectron. Eng.*, vol. 72, no. 1–4, pp. 326–331, Apr. 2004.

[26] C.-Y. Lin, C.-Y. Wu, C.-Y. Wu, C. Hu, and T.-Y. Tseng, "Bistable resistive switching in Al[sub 2]O[sub 3] memory thin films," *J. Electrochem. Soc.*, vol. 154, no. 9, p. G189, 2007.

Chapter 6 Conclusion and Future Work

6.1 Conclusion

To conclude, a comprehensive study on 3-D embedded capacitors has been proposed and carried out in this thesis, comprising of modeling, design, fabrication, and characterization. Firstly, a novel integrated capacitor for 3-D ICs called the "3-D embedded capacitor" has been proposed and designed to achieve significant capacitance density enhancement by taking advantage of existing TSV trenches. Two types of 3-D embedded capacitor have been proposed based on their electrode deposition methods for different end-applications. The ALD type 3-D embedded capacitor features an extremely high capacitance density, whereas the sputtering type 3-D embedded capacitor features a low cost and ease of integration. Secondly, an electric model has been constructed to predict the capacitance of the 3-D embedded capacitor based on its physical design parameters. The analytical model is developed with reference to the MIM coaxial capacitor. An ultra-high capacitance density, up to 5,621.8 nF/mm^2, can be envisioned from the model. Additionally, a finite element simulation has been carried out to ensure the structural integrity of the components of the 3-D embedded capacitor. The simulation results show that the maximum thermo-mechanical stress does not change noticeably with the inclusion of a 3-D embedded capacitor. Next, various types of test vehicles have been successfully fabricated after photomask design, process flow design, and process optimization. In total, six types of test vehicles are included in each unit cell repeated over the entire wafer: (1) the de-embedded ALD type, (2) the embedded rough-ALD type, (3) the embedded smooth-ALD type, (4) the de-embedded sputtering type, (5) the embedded rough-sputtering type, and (6) the embedded smooth-sputtering type. Lastly, *C-V* and *I-V* characterizations have been performed to evaluate the electrical performance of the test vehicles. The *C-V* characterization results show that, with trench diameter increasing from 10 to 50 μm, the capacitance of 3-D embedded capacitors varies from 98.7 to 625.2 pF for ALD type test vehicles, and it varies from 3.6 to 138.7 pF for

sputtering type test vehicles. These measurement results agree well with the calculated results based on the electrical model developed earlier for the ALD type test vehicles, but not for the sputtering test vehicles. The results show that ALD provides super conformal step coverage of electrodes, while sputtering provides poor step coverage of electrodes. Furthermore, the results of the other set of *C-V* characterization with different configuration show that the dielectric composition and the total amount of trapped charges in the dielectric layer become instable due to the rough sidewall. From the *I-V* characterization results, it can be observed that the leakage current of ALD type test vehicles does not degrade compared with planar MIM capacitor, but the leakage current of sputtering type test vehicles degrades compared with their planar counterparts. Then, the *I-V* characterization results are normalized to the *J-E* plots for ease of comparison, and they show that the leakage current density is ~2×10^{-7} A/cm^2 at 2 MV/cm and the dielectric strength is ~9.7 MV/cm for the ALD type test vehicles; whereas the leakage current density is ~3×10^{-9} A/cm^2 at 2 MV/cm and the dielectric strength is ~8.0 MV/cm for the sputtering type test vehicles. Based on the *J-E* plots, several leakage current conduction mechanisms have been identified. Schottky emission, FN tunneling, PF emission, and hopping conduction can be fitted for the ALD type test vehicles; whereas FN tunneling and PF emission can be fitted for the sputtering type test vehicles.

This technology will serve as a compliment, not a complete replacement, to the existing capacitor technologies, since it is implemented with available TSVs. For ICs with a large number of TSVs, 3-D embedded capacitor provides superb capacitance density and thus great area reduction for capacitors. It be used to realize the integration of ultrahigh-density on-chip capacitor and will contribute to the further development of on-chip energy storage element, integrated voltage regulator, and capacitively coupled wireless module.

6.2 Future Work

Beyond the scope of this study, the following recommendations are suggested for future work:

a. *A complete structure with Cu filling*

We suggest that a complete structure of the 3-D embedded capacitor with a TSV Cu filling should be fabricated in the future. The potential impact could be two-folded. Firstly, the coefficient of thermal expansion mismatch between Cu and Si could possibly degrade the structural integrity of 3-D embedded capacitor. Secondly, the signal/power transmission in the TSV could possibly cross talk to the surrounding 3-D embedded capacitor, causing the degradation of signal/power integrity. Besides, the 3-D embedded capacitor could be implemented with thermal TSV, which only conducts heat not electricity, to avoid the issue.

Therefore, it would be interesting to study these two aspects of the complete structure: (1) the effect of thermo-mechanical stress on the electrical performance of the 3-D embedded capacitor due to the existence of Cu filling and (2) the cross talk and the mutual capacitance between the 3-D embedded capacitor and the TSV Cu core.

b. *Reliability test*

We suggest that reliability tests (e.g., thermal cycling test and humidity test) should be carried out for the complete structures with copper filling. The difference in electrical performance for test vehicles before and after the reliability tests will be compared to ensure the robust operation of both TSV and 3-D embedded capacitors in harsh environments.

c. *A detailed electrical model*

We suggest that a more detailed electrical model should be built for the 3-D embedded capacitor, including components like equivalent series resistance and equivalent series inductance. Furthermore, a high frequency model of this capacitor could also be developed for up to 100 GHz, which would enable high frequency applications. With a better electrical model, the 3-D embedded capacitor could be readily used in circuit simulators and become friendly to circuit designers.

d. *Dielectric materials with higher dielectric constant*

We suggest that the search for other high-κ dielectric materials should continue to replace the currently used Al_2O_3 to achieve better electrical performance of the 3-D embedded capacitor.

e. *Implementation with Applications*

We suggest that the 3-D embedded capacitor could be implemented with real end-applications (e.g., integrated voltage regulator). The performance evaluation of the system will provide more valuable insight into this technology.

List of Publications

Patent:

[1] Y. Lin and C. S. Tan, “Semiconductor Devices and Methods of Forming the Same.”

Patent Office	Application Number	Filing date
US	15/761,384	19th Mar 2018
Korea	2018-7011193	20th Apr 2018
China	201680054722.2	20th Mar 2018
Taiwan	105130547	22nd Sep 2016
PCT	PCT/SG2016/050461	21st Sep 2016

Journal Papers:

[1] Y. Lin and C. S. Tan, "Modeling, Fabrication, and Characterization of 3-D Capacitor Embedded in Through-Silicon Via," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 9, pp. 1524-1532, Sept. 2018.

[2] Y. Lin and C. S. Tan, “Leakage current conduction mechanism of three-dimensional capacitors embedded in through-silicon vias,” *Japanese Journal of Applied Physics*, vol. 57, no. 7S2, p. 07MF01, Jul. 2018.

Conference Papers:

[1] Y. Lin and C. S. Tan, “Dielectric Quality of 3-D Capacitor Embedded in Through-Silicon Via (TSV),” in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018.

[2] Y. Lin and C. S. Tan, “Leakage Current Conduction Mechanism of 3-D Capacitor Embedded in Through-Silicon Via (TSV),” in *Advanced Metallization Conference 2017: 27th Asian Session*, 2017, p. 12.

[3] Y. Lin and C. S. Tan, “Physical and Electrical Characterization of 3-D Embedded Capacitor: A High-Density MIM Capacitor Embedded in TSV,” in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, 2017, pp. 1956–1961.

[4] Y. Lin and C. Seng Tan, “Through-substrate via (TSV) with embedded capacitor as an on-chip energy storage element,” in *2016 IEEE International 3-D Systems Integration Conference (3-DIC)*, 2016, pp. 1–4.