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**InAlN/GaN High Electron Mobility Transistors on Si
for RF Applications**

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InAlN/GaN High Electron Mobility Transistors on Si for RF Applications

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

Date

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Abstract

Conventional AlGaN/GaN High Electron Mobility Transistors (HEMTs) have been proven to be a strong competitor in both high voltage and high frequency applications resulting from the intrinsic material properties of GaN such as large bandgap, high electron mobility, high electron saturation velocity and high thermal conductivity. In the past decades, GaN HEMTs have emerged as one of the hottest research topics and intensively studied. The performance of conventional AlGaN/GaN HEMTs have been improved significantly and continuously in the past decades, such as high output power, high operation frequency and low noise figure. Recently, a novel heterostructure with a thin layer of InAlN on top of GaN have been demonstrated to further improve the high frequency performance of GaN HEMTs. Benefiting from the unique properties of InAlN/GaN hetrostructure such as very thin top barrier thickness, high electron density and lattice match, the high frequency performance of GaN HEMTs have been pushed to the next level. On the other hand, there are still some critical challenges limiting the applications of GaN HEMTs.

On key issue is that most of the high frequency results, especially those above 200 GHz, were reported from devices grown on SiC substrates. SiC has the advantages of small lattice mismatch to GaN epilayers, very high resistivity and thermal conductivity. Thus, GaN HEMTs grown on SiC can achieve higher RF performance than those grown on Si. However, GaN HEMT on SiC is not cost-effective and is only available in smaller sizes (≤ 6 inch) which make it less attractive to be adopted commercially.

To reduce the cost of GaN HEMTs, Si substrates have attracted increasing interest in recent years, not only in power electronics applications but also in RF applications. Significant efforts have been made on improving the epitaxial quality of GaN on Si substrates as well as the device fabrication technology. As a result, the performance of RF GaN HEMTs on Si has improved significantly. However, the high frequency performance of GaN HEMTs on Si still lags behind their counterparts on SiC. The best reported AlGaIn/GaN HEMT on Si only exhibited a f_T of 176 GHz with for a gate length of 80 nm.

Another drawback is the poor linearity performance of deeply scaled GaN HEMTs. Linearity is an important parameter for GaN HEMTs to be applied as amplifiers in modern communication system. GaN HEMT is expected to maintain high operation frequency at high gate bias to support its application for large signal RF operation. However, poor linearity characteristics have been observed in the conventional GaN HEMTs. It is manifested by a non-flat transconductance (g_m) and f_T , f_{max} versus gate bias (or drain current). After reaching its maximum point, g_m or f_T , f_{max} decrease drastically with the increasing gate bias. Linearity of GaN transistors ultimately limits the power density and efficiency of these devices in many applications, as the operating point of the device typically needs to be backed-off to meet the linearity specifications. In fact, as the operating frequency increases into the mm-wave range by shrinking the gate length, the linearity is expected to degrade even further.

This thesis mainly focuses on these two issues. Novel approaches are employed to resolve them and much improved device performance were obtained. The major contributions of the thesis are listed as below.

(1) The factors that limit the devices' high frequency performance are investigated. A thin InAlN top barrier is applied instead of conventional AlGaIn top barrier in order to minimize the impact of decreased gate length-to-barrier thickness ratio and thereby degradation of the gate modulation efficiency. Sub-100 nm gate was developed using electron beam lithography (EBL) technology to minimize gate induced intrinsic delay. Parasitic charging delay was minimized benefiting from the short source-to-drain distance down to 300 nm and low contact resistance R_c of 0.2 Ω .mm. Maximum f_T of 250 GHz was obtained in a 40-nm gate device, which is the highest among any other GaN HEMTs demonstrated on Si substrate previously. Surface passivation effects on DC and RF performance were also investigated.

(2) The mechanism of the poor linearity performance of the g_m and f_T at high gate bias was investigated. A novel planar-nanostrip GaN HEMTs structure using ion implantation technology was developed to improve the linearity performance and maintain f_T at a high level without introducing too much gate parasitic capacitance. The fabrication process was described in details including As ion implantation for isolation application, nanostrip-channel formation using different approaches. Moreover, the planar-nanostrip device also showed much improved maximum drain current I_{dmax} up to 2.6 A/mm, which is close to the theoretical limit. Also, device geometries including gate length, line-to-space ratio of the nanostrip-channel and gate-to-source distance have been studied. These results do not only identify the origin of the non-linear performance in GaN HEMTs, but also

illustrate the direction of design improvement of RF GaN HEMTs for high linearity application.

- (3) A Planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMTs on Si was demonstrated. A thin layer of oxide between the metal gate and the thin InAlN barrier and form a metal-insulator-semiconductor (MIS) gate in the Planar nanostrip-channel GaN HEMT, gate leakage current was reduced and thus increase the gate voltage swing and drain current swing. The results show that the Planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMTs is able to work at up to $V_g = +4$ V and the linearity performance was further improved. Two-tone intermodulation characterizations are discussed for conventional HEMT, Planar nanostrip-channel HEMT and MISHEMT. The lower IM3-to-carrier ratio ($-C/\text{IM3}$) and larger third order intercept OIP3 values of the Planar nanostrip-channel MISHEMT clearly indicate that the linearity of GaN HEMT was improved by the planar nanostrip-channel structure as well as the insertion of 6-nm Al_2O_3 gate insulator.

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Chapter 1 Introduction

1.1. Overview of GaN based high-electron-mobility transistors (HEMTs) for RF application

In the last few decades, GaN based semiconductor technology has witnessed significant advancement. The unique properties of GaN based materials have stimulated the applications in many fields such as optoelectronics [1-5] microelectromechanical systems (MEMS) [6-11] and electronics [12-17]. Among all these applications, AlGaN/GaN high electron mobility transistors (HEMTs) are especially attractive due to their excellent capabilities in high power [12], high frequency [13, 14] and high temperature operations [17].

Table 1.1 compare the key intrinsic electronic propertied of GaN to other major semiconductor materials. It can be concluded that GaN has several major advantages over Si, GaAs and InP. Benefiting from its wider band-gap (E_g), GaN has an up to ten time higher critical electrical field (E_c) than Si, GaAs and InP. The high E_c of GaN leads to much higher breakdown voltage of GaN HEMTs compared to other semiconductor device thus making GaN very suitable for high voltage and high power applications. In addition, the high breakdown voltage helps to improve the circuit robustness based on GaN transistors. The outstanding electron mobility and saturation drift velocity together with the high 2DEG concentration enable these devices to operate at very high frequencies with high drain current, which is important for high power RF applications. As a wide band-gap material, the intrinsic carrier generation rate n_i is very much lower

than Si, GaAs or InP, which makes GaN based transistors able to operate at high voltage and meanwhile keeping the leakage current at a low level [5]. Moreover, the high thermal conductivity allows GaN based device to work at extreme environments.

Table 1.1 Key intrinsic electronic properties of GaN and other semiconductor materials

Material	Si	4H-SiC	GaN	GaAs	InP
$E_g(\text{eV})$	1.1	3.26	3.4	1.4	1.34
$E_c(\text{MV/cm})$	0.3	2.0	3.3	0.4	0.5
$n_i (\text{/cm}^3)$	1.5×10^{10}	8.2×10^{-9}	1.9×10^{-10}	2.1×10^6	1.3×10^7
ϵ_r	11.8	10	9.0	12.8	10
$\mu_n(\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1})$	1350	720	900	8500	5400
$v_{\text{sat}}(10^7 \text{ cm/s})$	1.0	2.0	2.5	2.0	0.9
$\kappa(\text{W} \cdot \text{cm}^{-1} \cdot \text{K}^{-1})$	1.5	4.5	1.3	0.5	0.68

E_g : band gap energy, E_c : breakdown electric field, ϵ_r : relative dielectric constant, n_i : intrinsic carrier generation rate, μ_n : electron mobility, v_{sat} : saturated drift velocity of electron, κ : thermal conductivity.

As shown in Table 1.1, many properties of SiC are similar to GaN. However, there are some critical challenges such as difficulties in forming heterostructure and developing fabrication techniques ultimately limit its applications. On the other hand, GaN is able to form heterostructure with other GaN based material such as AlGaIn and thus form a HEMT structure. Moreover, benefiting from the existence of high density 2DEG (for AlGaIn/GaN heterostructure, $n_i \sim 1 \times 10^{13} / \text{cm}^3$; $\mu_n \sim 1500 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$) induced by the high

polarization effect near the heterojunction interface, the fabrication process of AlGaIn/GaN HEMTs is simple since there is no need of additional doping process.

Due to the advantages mentioned above, AlGaIn/GaN HEMTs are commercially very attractive in RF high power amplifications in 5G communication systems and imaging applications, such as vehicle to vehicle communication, automobile radar in auto-driving system, internet-of-things, HDTV (High Definition Tele-Vision), IoTs (Internet of Things), and imaging systems etc.

As for RF power amplifiers, the most important parameters are maximum output power and operating frequency. Since these two parameters are significantly affected by breakdown voltage, mobility and electron saturation velocity as mentioned above, AlGaIn/GaN HEMT is an excellent candidate to be used as power amplifiers with the potential to obtain outstanding performance as shown in Figure 1.1 [18].

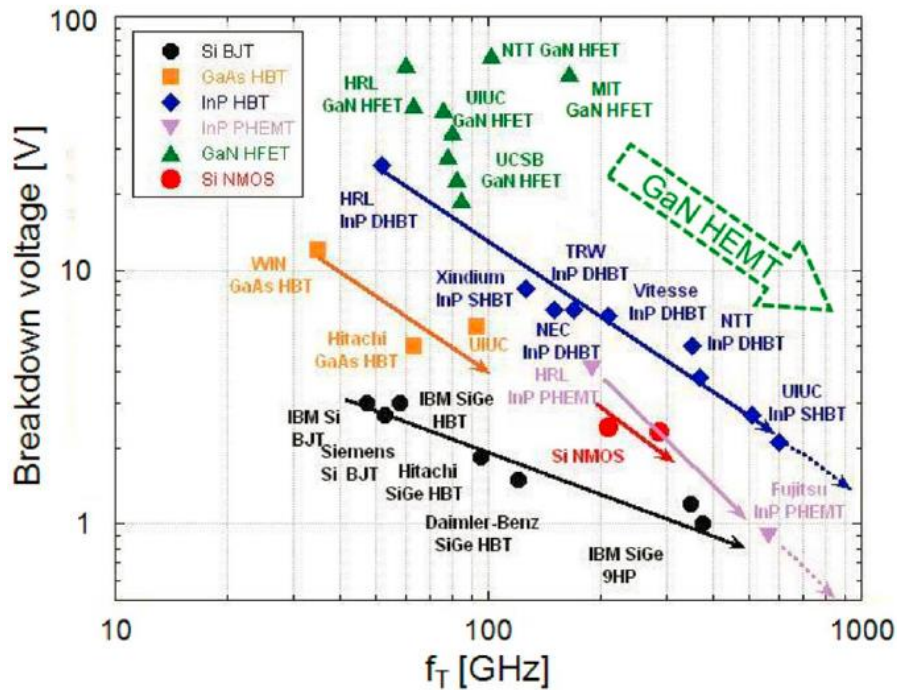


Fig.1.1 Device breakdown voltage versus current gain cutoff frequency (f_T) of GaN and other semiconductor materials [18]

The AlGaIn/GaN HEMTs' microwave characteristics were firstly reported in 1994 [7]. Since then, a lot of efforts have been made for the improvement of their performance, particularly on the large-signal power and small-signal frequency performance.

Two of the most important large-signal power figure-of-merits of AlGaIn/GaN HEMTs are the maximum output power (P_{out}) and power-added-efficiency (PAE). The first large-signal RF characteristics for an AlGaIn/GaN HEMT was reported in 1996 [19]. The device had a gate length of 1 μm . At 2 GHz, it showed a maximum P_{out} of 1.1 W/mm and PAE of 18.6 %. Since then, both the high power performance and operation frequency of AlGaIn/GaN HEMTs have been improved dramatically. In 1997, Wu *et al.* demonstrated a device with P_{out} of 3.3 W/mm and PAE of 18.2 % at 18 GHz [20]. In the same year, Moon *et al.* reported a 0.15 μm -gate device with P_{out} of 6.6 W/mm and PAE of 35 % at 20 GHz [21]. Benefiting from the use of a field-plate technology [22], Chini *et al.* pushed the devices' P_{out} to 12 W/mm and PAE to 58 % at 4 GHz in 2004 [23]. In the same year, Wu *et al.* improved P_{out} significantly to 41.4 W/mm with PAE of 60 % at 4 GHz [24]. In 2005, Palacios *et al.* reported a device with P_{out} of 10.5 W/mm and PAE of 33 % at 40 GHz [25]. In 2007, Wu *et al.* improved P_{out} to 13.7 W/mm and PAE to 40 % at 30 GHz [26]. Moreover, many promising high power results of AlGaIn/GaN HEMTs in high frequency range have also been reported [27, 28].

For small-signal RF characterizations, by measuring the device S-parameters, one can extract the maximum operation frequency of an AlGaIn/GaN HEMT. Generally, the most important figure-of-merits (FOMs) in the small-signal performance are current gain

cutoff frequency (f_T) and power gain cutoff frequency (f_{max}). They are the most straight forward parameters to evaluate the speed performance of a device. The first small-signal microwave characteristics of AlGaIn/GaN HEMT were reported by Khan *et al.* on a device with 0.25 μm gate in 1994. The device showed a f_T of 11 GHz and f_{max} of 35 GHz [29]. Since then, both f_T and f_{max} of AlGaIn/GaN HEMTs have increased significantly. The maximum f_T and f_{max} have been increased to 36.1 GHz and 70.8 GHz, respectively by Khan *et al.* in 1996 in a 0.25 μm -gate device [30]. Wu *et al.* reported a 0.2 μm -gate device with f_T of 50 GHz and f_{max} of 92 in 1997 [31]. In 2000, by shrinking the gate length to 0.15 μm , Micovic *et al.* improved the f_T to 110 GHz and f_{max} to 140 [32]. Kumar *et al.* demonstrated a 0.12 μm -gate device with f_T of 121 GHz and f_{max} of 162 GHz [33]. A 90 nm-gate device with f_T of 163 GHz and f_{max} of 185 GHz was reported by Palacios *et al.* in 2005 [34]. By applying an InGaIn back barrier structure in a 100 nm-gate device in 2006, f_{max} of 230 GHz was achieved by Palacios *et al.* [35]. In the same year, Higashiwaki *et al.* pushed the f_T to 181 GHz by scaling the gate length down to 30 nm [36]. A device with 60 nm gate AlGaIn/GaN HEMT and a thinner top barrier was demonstrated by Higashiwaki *et al.* in 2008. f_T of 190 GHz and f_{max} of 251 GHz were obtained in this device [37]. Finally, in 2010, a new record performance was reported by Chung *et al.*. The device in this work exhibited high f_T of 225 GHz and f_{max} of 300 GHz, respectively [38], [39].

1.2. Issues in GaN HEMTs for RF applications

As discussed in the last section, great improvements have been made on the performance of GaN HEMTs for RF applications. However, despite all these significant improvements, there are still some critical issues for GaN HEMTs. One key issue is that

the performance of GaN HEMTs reported on low-cost Si substrate still lags behind that on SiC substrate. The other one is that the poor linearity performance of GaN HEMTs especially for sub-100 nm gate limits its application at high gate bias condition.

1.2.1. Lack of High Frequency GaN HEMTs on Si substrate

Resulting from the lack of large size bulk GaN substrate as well as the high cost and the difficulties of synthesis, GaN based heterostructures are usually grown on non-native substrates such as sapphire (Al_2O_3), SiC and Si (111). The properties of commonly used substrates are listed in Table 1- 2.

Table 1.2 Properties of commonly used substrates for GaN growth

Material	Al_2O_3 (100)	6H-SiC	GaN (0001)	Si (111)
a (Å)	4.758	3.081	3.189	3.846
a mismatch	-33%	3.5%	0	-17%
α (10^{-6}K^{-1})	7.3	4.5	5.6	2.6
α mismatch	-23%	24%	0	116%
κ (W/cm·K)	0.5	4.5	1.3	1.5
Max. D (mm)	200	150	50	300
Cost	Medium	Very high	Extremely high	Low

a: Lattice constant; α : Thermal expansion coefficient; κ : Thermal conductivity; D: substrate diameter.

As shown in Table 1.2, SiC has the advantages of smaller lattice mismatch to GaN epilayers and has very high resistivity and thermal conductivity. Thus, GaN HEMTs grown on SiC can achieve higher RF performance than those grown on Si. However, GaN HEMT on SiC is not cost-effective and is only available in smaller sizes (≤ 6 inch) which make it less attractive to be adopted commercially.

To reduce the cost of GaN HEMTs, Si substrates have attracted increasing interest in recent years, not only in power electronics applications but also in RF applications. Significant efforts have been made on improving the epitaxial quality of GaN on Si substrates as well as the device fabrication technology. As a result, the performance of conventional AlGaIn/GaN HEMTs on Si has improved significantly [40]-[46]. However, the high frequency performance of GaN HEMTs on Si still lags behind their counterparts on SiC. Large lattice mismatch (17%, versus 3.6% between GaN and SiC) and thermal expansion coefficient difference between GaN and Si (111) substrate lead to higher density of dislocations in the epitaxial GaN materials [47, 48]. The low resistance Si substrate, nitride/Si interface and GaN buffer also bring significant RF loss for the devices [49]. Besides, novel barrier materials such as InAlN, AlN, InAlGaIn and AlGaIn with high Al concentration [36, 37, 50-56] with thin thickness have already been applied on the devices fabricated on SiC substrate. Combined with deeply scaled gate length, these devices showed dramatically improved maximum operation speed [57]. In contrast, there is very limited study on deep sub 100-nm-gate GaN HEMTs on Si with novel thin InAlN barrier layer. As a result, most of high frequency results, especially those above f_T of 200 GHz, were reported from devices grown on SiC substrates. The best reported GaN HEMT on Si only exhibited a f_T of 176 GHz with for a gate length of 80 nm [58]. As

shown in Fig. 1.2, the f_T values of GaN HEMTs on Si substrate reported in literatures are much lower than that of on SiC.

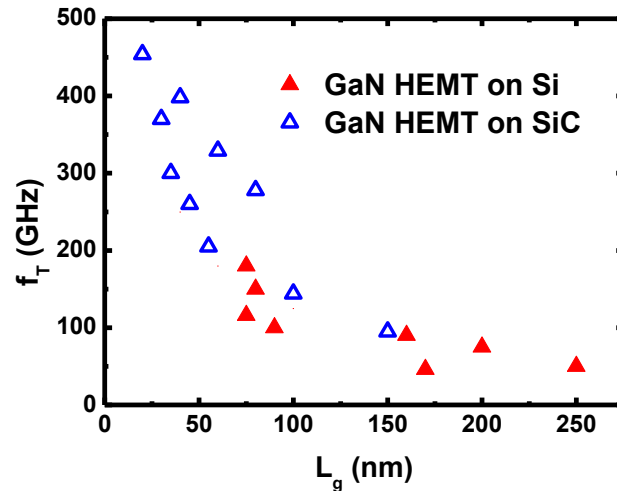


Fig. 1.2 Comparison of the cut-off frequencies (f_T) of GaN HEMTs on Si [41], [43], [46], [58]-[60] and GaN HEMTs on SiC [57], [61]-[65]

1.2.2. Poor Linearity performance of deeply scaled GaN HEMTs at high gate bias

Beside operation frequency and output power, linearity performance needs to be particularly considered in the GaN HEMT devices. The next generation communication systems will widely adopt the techniques of CA (carrier and MIMO (multiple input multiple output), and these techniques will result in greater signal intermodulation and communication channel interference. High linearity amplifiers and switches are needed in these systems. However, the linearity of GaN transistors ultimately limits the power density and efficiency of these devices in many applications, as the operating point of the device typically needs to be backed-off to meet the linearity specifications. In fact, as the

operating frequency increases into the mm-wave range by shrinking the gate length, the linearity is expected to degrade even further [66, 67]. Circuit designers are putting efforts to add more functional sub-circuits such as DPD (Digital Pre-Distortion) to solve the linearity issue. However, this will definitely increase the system complexity, chip size, and design cost, and degrades the system robustness. Several theories have been brought forward to explain the non-linearity in GaN HEMTs, such as alloy and interface scattering [68], enhanced phonon scattering [69] and the increased access resistance at high channel current [66, 70, 71]. Techniques like self-align GaN HEMT [72] and etched nanowire channel HEMT [67] have been studied to suppress the nonlinear effect. However, these techniques still have their own limitations. Low breakdown voltage has been observed for the self-aligned HEMT due to the small gate-to-source and gate-to-drain access regions. The etched nanowire channel introduces too much parasitic capacitance and therefore degrades the device performance. Further improvement on linearity performance of GaN HEMTs is hence needed.

1.3. Project goal and thesis outline

This thesis mainly focuses on the two key issues in GaN HEMTs for RF application as discussed in the last section. First, in order to obtain high operation frequency in GaN HEMTs on Si substrate, delay components of the devices have been analyzed in detail. The limitations of device speed have been clarified. Device fabrication technologies have been developed for deeply scaled InAlN/GaN HEMTs on Si and pushed the devices' operation frequency to higher level. Then, the origin of the poor linearity performance of GaN HEMTs at high gate bias (or drain current) is studied. Novel technologies and device design have been developed to obtain high linearity in GaN HEMTs.

In chapter 2, the fundamentals of conventional AlGaIn/GaN HEMT technology are briefly presented. The device physics including heterostructures formation and device operation mechanism are described. Typical fabrication process of a conventional AlGaIn/GaN with T-shaped gate and its DC/RF characterizations are explained.

In chapter 3, the factors that limit the devices' high frequency performance are investigated. A thin InAlN top barrier is applied instead of conventional AlGaIn top barrier in order to minimize the impact of the decreased gate length-to-barrier thickness ratio and thereby degradation of the gate modulation efficiency. Sub-100 nm gate was developed using electron beam lithography (EBL) technology to minimize gate induced intrinsic delay. Parasitic charging delay was minimized benefiting from the short source-to-drain distance down to 300 nm and low contact resistance R_c of 0.2 Ω .mm. Maximum f_T of 250 GHz was obtained in a 40-nm gate device which is the highest value ever reported for GaN HEMTs on Si substrate previously. Surface passivation effects on DC and RF performance was also investigated.

In chapter 4, the mechanism of the poor linearity performance of the g_m and f_T at high gate bias are clarified. A novel planar nanostrip-channel GaN HEMTs structure using ion implantation technology is implemented to improve the linearity performance and maintain a high f_T by not introducing too much gate parasitic capacitance. The fabrication process was described in details including Arsenic ion implantation for isolation application, nanostrip-channel formation using different approaches. Moreover, the planar nanostrip-channel device also showed much improved maximum drain current I_{dmax} up to 2.6 A/mm, which is close to the theoretical prediction. Also, studies on the device geometries including gate length, line-to-space ratio of the nanostrip-channel and

gate-to-source distance are carried out. These results do not only identify the origin of the non-linear performance in GaN HEMTs, but also provide the direction on how to improve the design of RF GaN HEMTs for high linearity application.

In chapter 5, A Planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMTs on Si are demonstrated. A thin layer of oxide was introduced between the metal gate and the thin InAlN barrier to form a metal-insulator-semiconductor (MIS) gate in the Planar nanostrip-channel GaN HEMT. As a result the gate leakage current was reduced which in turn increase the gate voltage swing and drain current swings. The results show that the Planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMTs are able to work at a positive gate bias voltage up to 4 V and at the same time improves the linearity performance. Two-tone intermodulation characterizations are discussed for conventional HEMT, Planar nanostrip-channel HEMT and MISHEMT. The lower IM3-to-carrier ratio ($-C/\text{IM3}$) and larger third order intercept OIP3 values of the Planar nanostrip-channel MISHEMT clearly indicate that the linearity of GaN HEMT was improved by the planar nanostrip-channel structure as well as the insertion of 6-nm Al_2O_3 gate insulator.

Finally, the main results of this thesis are summarized in chapter 6. In addition, the recommendations for future improvement of GaN HEMTs for RF applications are also presented.

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Chapter 2 Fundamentals of GaN HEMTs

In this chapter, the fundamentals of conventional AlGa_N/Ga_N HEMT technology are briefly introduced. The device physics including heterostructures formation and device operation mechanism will be described. Typical fabrication process of a conventional AlGa_N/Ga_N with T-shaped gate and its DC/RF characterizations will be briefly explained.

2.1. Physics and device design in conventional AlGa_N/Ga_N HEMTs

The most general Ga_N crystalline structure is wurtzite. In such a crystal unit cell, Gallium (Ga) and Nitrogen (N) atoms are bounded ionically. Due to the electron affinity difference between Ga and N atoms, the distribution of valence electrons in the bonding is strongly asymmetric [1]. Unlike other semiconductors such as GaAs and InP with zincblende crystal structure, the wurtzite structure in Ga_N is not symmetrical, and thus a strong net polarization field is induced. Typically, based on the growth direction, there are two types of Ga_N material namely Ga-face and N-face. The directions of the polarization field in the two types of Ga_N are opposite as shown in Fig. 2.1 [1]. In this work, Ga-face Ga_N material was used for all the devices. This polarization field is called spontaneous polarization because it is an intrinsic property of Ga_N material and induced by the crystalline structure and elemental composition.

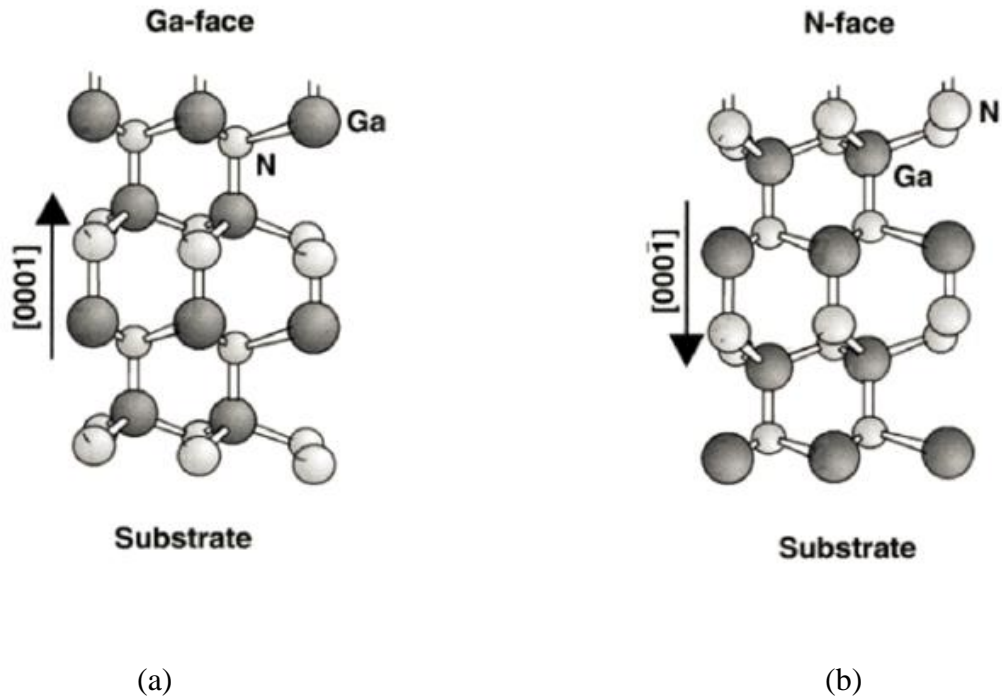


Fig. 2.1 Crystal structure and polarization field in (a) Ga-face and (b) N-face GaN [1].

In addition to the spontaneous polarization, another polarization namely piezoelectric polarization exists in lattice mismatched GaN based heterostructures such as AlGaN and AlN. This polarization component is induced by the strain between two different materials. If the thickness of AlGaN or AlN barrier is below their critical thickness, the strain cannot be eliminated and gives rise to piezoelectric polarization [2]. Together with spontaneous polarization, these two polarization components determine the basic electric properties of GaN based heterostructures and enable the possibility of a high electron mobility transistor (HEMT).

Fig. 2.2 shows a typical structure of the AlGaN/GaN HEMT and its band diagram used in this work. It consists of a undoped GaN cap layer, AlGaN top barrier layer, AlN spacer layer, GaN channel/buffer layer and transition/seeding layer. Benefitting from the

bandgap difference between AlGaN barrier (larger bandgap) and GaN channel (smaller bandgap) and high polarization field, a quasi-triangular potential well is formed several nanometers under the interface of the heterostructure and a high density two dimensional electron gas (2DEG) is confined in this well. The gate electrode controls the channel by modulating the concentration of 2DEG through the gate voltage. The functions of each layer in the GaN HEMT structure are listed as follow:

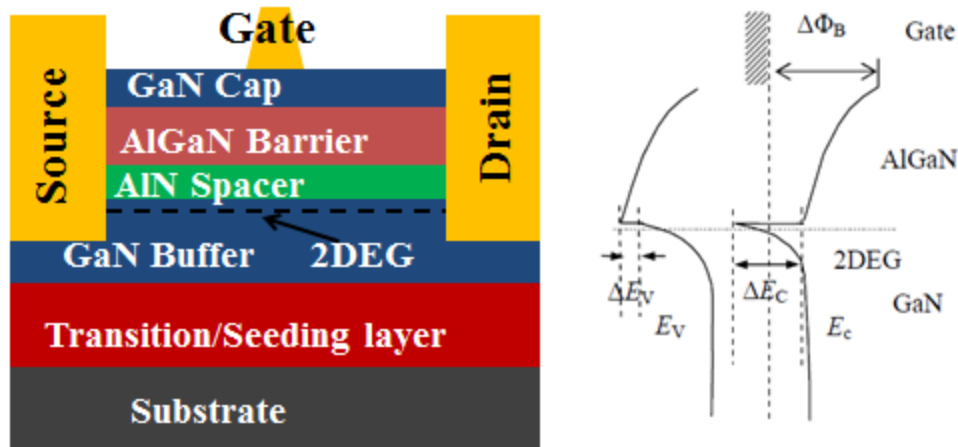


Fig. 2.2 (a) The schematic of the cross section and (b) energy band diagram of a typical GaN HEMT

a. Undoped GaN cap layer

A thin layer of in-situ GaN is usually grown on top of the barrier layer. Generally, the cap layer can be either n^+ doped or undoped. The undoped GaN cap layer used in this work has the advantage that the Schottky barrier height is large ($> 1.0 \text{ eV}$) and thus the gate metal can be directly deposited on the GaN cap layer. In this case, the device fabrication process can be simplified and better device performance uniformity can also be achieved.

b. *AlGa_xN barrier layer*

Barrier layer mainly plays two roles in GaN HEMT structure. One is to generate high density electrons in the channel and the other is to isolate the gate electrode from the channel. In order to have high electron concentration, barrier layer need to have a larger bandgap than GaN channel. Conventionally, Al_xGaN_{1-x} is used for top barrier. Aluminum concentration is expected to be higher in order to have a larger bandgap difference ΔE_c compared with GaN and thus generates higher 2DEG concentration and prevents hot electrons from injecting into the barrier. However, Aluminum concentration is usually kept lower than 30%. This is because if the Al composition is too high, it will introduce high strain between top barrier and channel due to enlarged lattice mismatch [3]. Furthermore, higher Al composition will potentially impact the long-term reliability as reported in [4].

c. *AlN spacer layer.*

The high bandgap undoped spacer layer can be grown in between the barrier layer and the channel layer to increase the 2DEG density by further increasing bandgap difference. At the same time, the spacer layer can increase the electron mobility by reducing the remote coulomb scattering of the electrons in the channel. A 10% increase in 2DEG density and 50% in electron mobility was reported in [5].

d. *Undoped GaN channel layer*

As discussed above, a conductive channel is formed several nanometers under the interface between the barrier and buffer layer. As the GaN buffer layer has a lower bandgap compared with AlGa_xN barrier, a quasi-triangular potential well is formed

between the two types of materials. Due to the large spontaneous and piezoelectric polarization difference between the AlGa_N and GaN, a high density 2DEG is formed and confined in the quasi-triangular potential well. As a result, there is no need of additional doping process to generate electrons in the channel.

e. **GaN buffer layer**

Insulating buffer layer is necessary for GaN HEMTs to reduce the buffer leakage current and the parasitic capacitance between electrodes and conductive buffer. Generally, both un-doped and Fe or C doped GaN can be used for this purpose.

f. **1 μm GaN and transition/seeding layer**

Typically, GaN epi layers are grown on a foreign substrate with different material because it is still hard to achieve high quality GaN substrate with large wafer size. The lattice mismatch between the substrate material and GaN is relatively large, for example, the corresponding mismatch between GaN and SiC/sapphire/Si are 3.6%/ 13.8% /17% respectively. The purpose of the transition/seeding layer is to accommodate the strain and TEC mismatch between substrate and GaN buffer [6]. Thus, the design and growth of this layer is very important to realizing high quality GaN epi layers.

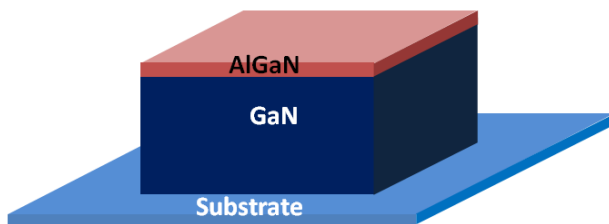
g. **Substrate**

Generally, there are three types of substrate materials for GaN growth which are SiC, Sapphire and Si. The properties of these materials have been discussed in the first chapter of this thesis. In this work, all the devices are fabricated using GaN-on-Si for low-cost purpose.

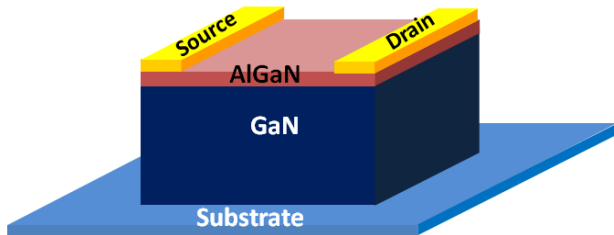
2.2. Key fabrication process for conventional GaN HEMTs

HEMTs

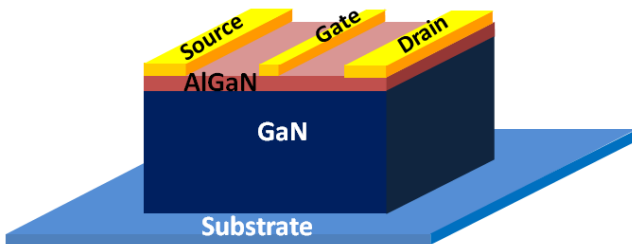
The fabrication process of conventional AlGaN/GaN HEMT can be roughly divided into four steps, which are: mesa isolation, ohmic contact formation, gate formation and surface passivation. Fig. 2.3 shows the process flow.



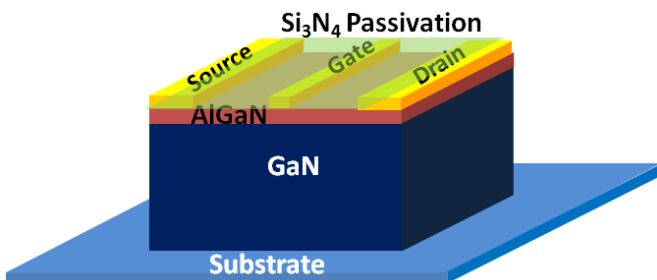
- Mesa isolation by Cl_2/BCl_3 plasma dry etching.



- Ohmic contact formation by Ti/Al/Ni/Au metallization and high temperature annealing.



- Gate formation by EBL and Ni/Au metallization.



- Si_3N_4 passivation.

Fig. 2.3 Key fabrication processes for conventional AlGaIn/GaN HEMTs

2.2.1. Mesa Isolation

The fabrication of the device starts from device isolation. This step is to prevent short circuit or current leakage between adjacent devices. The device performance is highly dependent on the quality of mesa isolation. If the leakage current is high, the device will not be able to pinch-off. For effective mesa isolation, the leakage current should be less than 10^{-6} A/mm at operation biases.

Usually, this isolation can be achieved by wet etching and dry etching. Since wet etching is difficult to use for etching in GaN based material, dry etching processes like Reactive-Ion-Etching (RIE) or Inductive-coupled-Plasma (ICP) are more commonly used. The mesa pattern is realized by photolithography and followed by Cl_2/BCl_3 plasma dry etch.

The mesa isolation process starts by cleaning the wafer with acetone and IPA by ultrasonic. The wafer was first coated with a 1.4 μm AZ5214 photoresist using a spin coater at 4000 rpm for 30 secs. Soft bake of the wafer at 105 $^{\circ}\text{C}$ for 2 minutes was adopted to evaporate the solvent in the photoresist. The sample was then patterned using UV-light (320nm) exposure and developed in CD 26 developer for 30 secs. O_2 plasma treatment was used to remove the residue of photoresist. The dry etching was carried out with Cl_2/BCl_3 of 20/40 sccm at RF power of 100w for 100 s to remove the top 100-120nm GaN and AlGaIn layers. The measured leakage current for a 10 μm gap is typically lower than 10^{-7} A/mm at 20 V, which indicates that the mesa isolation and the buffer quality is acceptable.

2.2.2. Ohmic Contact Formation

To achieve high drain current density and high maximum operation frequency, low source and drain contact resistance are necessary. The contact resistance is influenced by many factors such as wafer structure, growth quality, process technique, metal deposited and annealing temperature etc. To form a low resistance ohmic contact, the metal to be deposited needs to fulfill several characteristics such as low work function and resistivity and highly thermal conductive. Ti/Al/Ni/Au multilayer metal stack is commonly used as the metal scheme to form the ohmic contact. A high temperature (typically 800 °C) annealing is required after the metal deposition. During the annealing, Ti and Al will react with the N atoms of the under layer semiconductor materials including GaN and AlGaN barrier and form TiAlN [7]. Thus, lots of N vacancies were generated in the barrier and these vacancies are working as n-dopants, which pull down the conduction band of the nitrides and help to form the ohmic contact. Au is used to prevent Ti/Al from being oxidized and improve both the electrical and thermal conductivity. Ni is inserted as a blocking layer between Ti/Al and Au to prevent the inter-diffusion of Ti/ Al and Au.

For the ohmic contact formation, the wafer was treated with H_2SO_4/H_2O_2 3:1 (Piranha) to remove the surface contaminant. The ohmic contact patterns were defined using the image reversal process of AZ5214. After coating with 1.4 μ m photoresist, the wafer was soft baked at 105°C for 2 minutes and followed by the first exposure with contact mask aligner. Then hard bake was carried out at 120°C for 2 minutes followed by flood exposure without any mask. CD26 developer was used for development. This image reversal photolithography process is able to give minimum 1 μ m linewidth with good undercut, which is useful for the metal lift-off process. After O_2 plasma descum, a BOE

(buffered oxide etchant) treatment was applied to the wafer to remove the native oxide. This is important to form low resistance ohmic contact because the native oxide can form a barrier between the deposited metal and the AlGaIn barrier, thus deteriorate the ohmic contact between the Ti/Al/Ni/Au alloys and the semiconductor material. A four-layer Ti/Al/Ni/Au 20/120/40/50 nm was deposited using an electron beam evaporator system. Lift-off was used to remove the unwanted metal. The post metallization annealing is needed to form the ohmic contact. The ohmic contact resistance (R_c) can be measured with the Transmission Line Model (TLM) method. The optimization of the annealing temperature was carried out in this work. Fig. 2.4 shows that the lowest contact resistance can be achieved at 775°C. For the wafer in this work, the contact resistance $R_c = 0.32\sim 0.36 \Omega\text{-mm}$ has been measured.

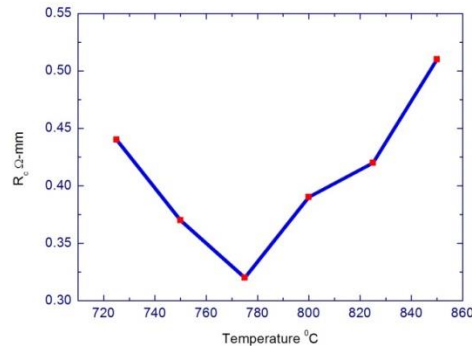


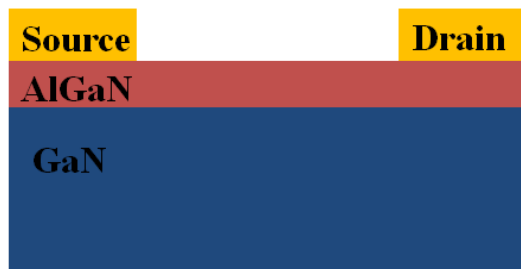
Fig. 2.4 R_c versus annealing temperature

After the ohmic contact formation, a two layer Ti/Au 50/300 nm was deposited for interconnect and pads.

2.2.3. Gate Formation

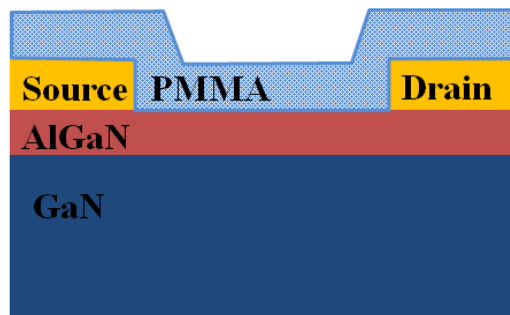
Good Schottky gate formation is one of the keys to realize high device performance. To minimize the gate leakage current, the gate metal should have a high work function and with a high Schottky barrier height. Ni/Au double layer is usually used to form the metal gate. Au deposited on top of Ni is used to reduce the gate metal resistance.

The speed of the device is directly dependent on the gate length (L_g) as the time that the electron travels across the channel is proportional to L_g . Thus, a short gate length (L_g) is crucial to achieve high operation speed in GaN HEMT. However, the gate resistance (R_s) increases proportional to the L_g for a rectangular gate. High R_s will degrade large signal performance of GaN HEMTs. To solve this problem, a T-shaped gate (also known as mushroom-shaped) with a short gate foot length and larger gate head length can be applied to increase the cross section area of the gate and thus can achieve short gate length as well as low gate resistance. In this chapter, a T-shaped gate was formed with Bi-layer MMA-PMMA process using an Electron Beam Lithography (EBL) system (EBL system will be discussed in details in chapter 3). The gate formation process flow is listed in Fig. 2.5.

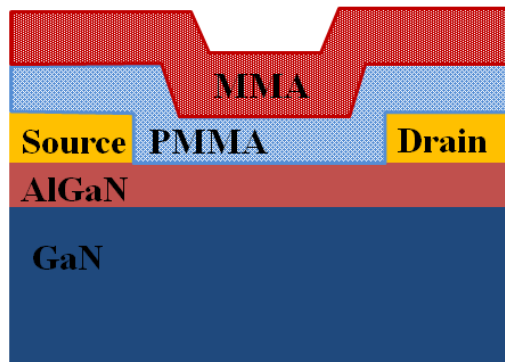


- After mesa isolation and ohmic contact formation.

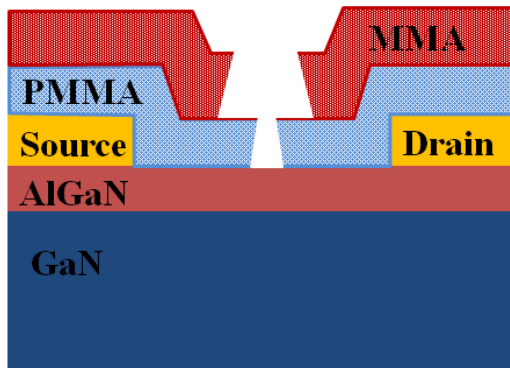




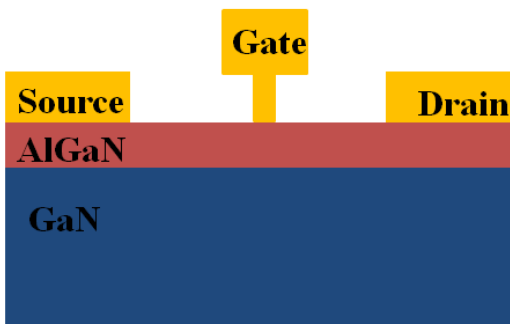
- To spin coat PMMA



- To spin coat MMA



- Electron beam exposure



- Gate metallization and lift-off

Fig. 2.5 Process flow for Bi-layer T-shaped gate formation

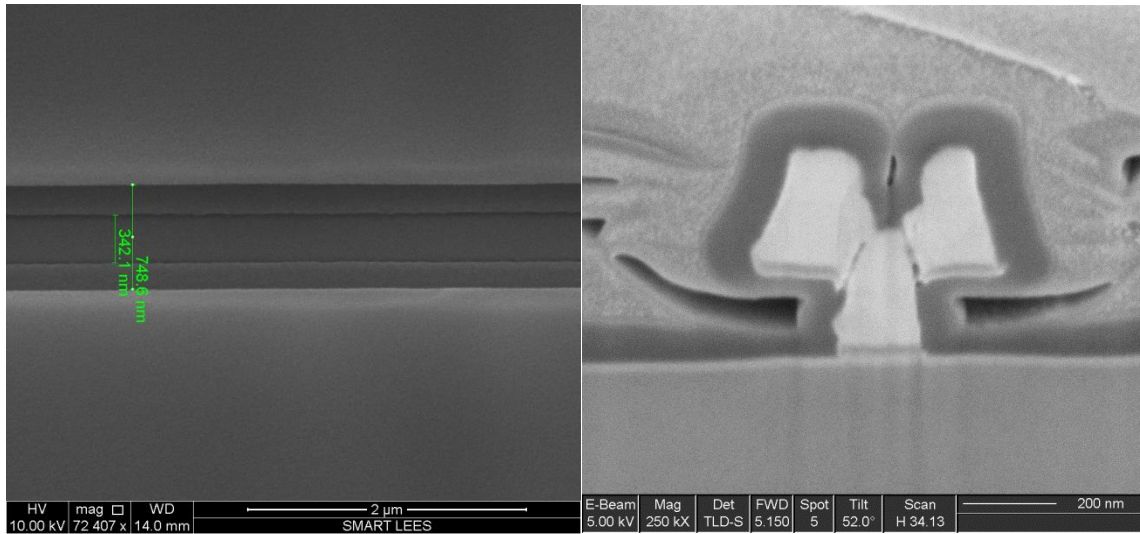


Fig. 2.6 SEM images of typical (a) MMA-PMMA resist stack after exposure and (b) cross section of fabricated T-shaped gate

For the gate formation process, the wafer was first spin coated with bi-layer PMMA (poly methyl methacrylate) and MMA (methyl methacrylate) resist stack. Vistech 5200 EBL system was used to write the gate pattern directly on the resist stack. The sensitivity to electron beam of MMA on top is higher than that of PMMA underneath. So, the dosage use for gate head writing is lower than that for gate foot. During gate head writing, by carefully control the dosage, the PMMA layer will not be exposed. After the writing of gate head, a higher dosage was used for gate foot writing. After electron beam exposure, a Methyl Iso-Butyl Ketone (MIBK): Isopropanol (IPA) =1:3 solution at room temperature was used to develop the sample for 90 secs. A T-shaped resist stack was formed as shown in Fig. 2.6 (a). After gate metallization and lift-off, T-shaped gate was fabricated as shown in Fig 2.6 (b). It is worth noting that the dosage for gate head writing is crucial to obtain an accurate profile for the T-shaped gate. For example, if the dosage used for gate head writing is too high, the PMMA underneath will also be exposed and

thus change the gate foot profile. Fig. 2.7 presents an example for the over dose of gate head.

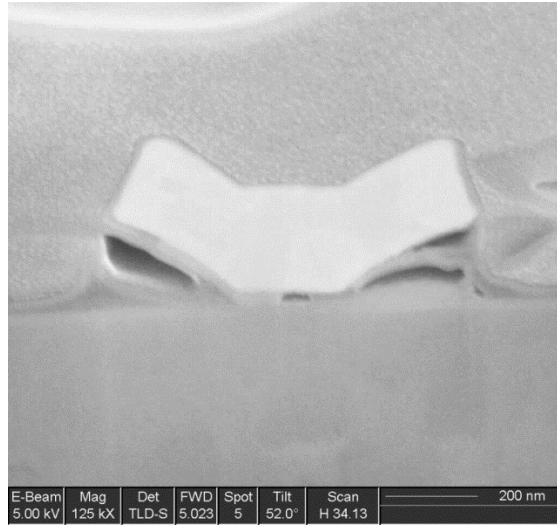


Fig. 2.7 V-shaped gate by overdose of gate head

Fig.2.8 represents the top view SEM image of the fabricated conventional AlGaN/GaN HEMT with a T-shaped gate. In this device, the gate foot length L_g was 250 nm while the gate head length was 700 nm. 50/300 nm Ni/Au metal stack was used for the gate metal. The source-to-gate distance L_{gs} was 750 nm and the drain-to-gate distance was 3 μm . The channel width of the device was 50 $\mu\text{m} \times 2$.

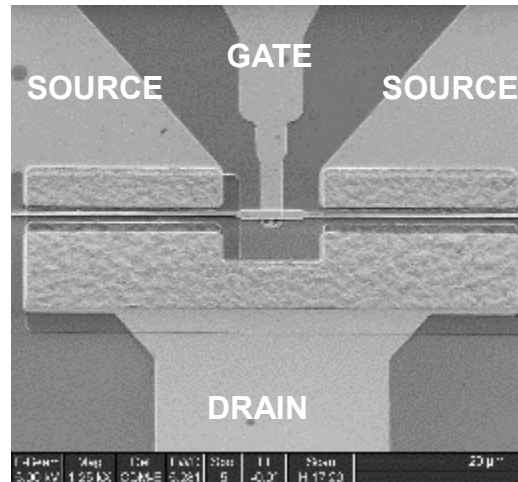


Fig. 2.8 Top view SEM image of the fabricated AlGaIn/GaN HEMT with T-shaped gate

2.2.4. Surface Passivation

As the final step, a layer of dielectric material is deposited on top of the device as passivation layer to reduce the surface states. Usually, on the surface of source and drain access regions, there are a large number of surface states which can degrade both the DC and RF performance of GaN HEMTs. These surface states may come from the damage induced during processing, or the dangling bonds of the atoms on the surface of semiconductor material, or even surface contaminations.

Several dielectrics can be used to suppress the effect of surface states, like Si_3N_4 , SiO_2 and Al_2O_3 . Among them, Si_3N_4 is most commonly used. Also, dielectric free passivation has been shown to be able to effectively passivate the surface and at same time introduce less parasitic capacitance [8]. In this work, Si_3N_4 of 200 nm deposited by plasma enhanced chemical vapor deposition (PECVD) was used for surface passivation. After Acetone/IPA cleaning, the wafer was loaded into PECVD growth chamber. Si_3N_4 was deposited using SiH_4 , NH_3 and N_2 plasma. A chamber temperature of 300 °C, chamber pressure of 1000 mTorr and RF power of 20W was used for deposition. This deposition condition gave a deposition rate of 0.9 nm/s. After 200 nm Si_3N_4 deposition, contact windows was patterned using optical lithography and etched using HCF_3 and CF_4 plasma for probing purpose.

2.3. DC characteristics for GaN HEMTs

The DC characteristics including output (I_d - V_d) and transfer (I_d - V_g) characteristics of the fabricated GaN HEMTs were measured using an Agilent B1500A semiconductor

analyzer and shown in Fig. 2.9 (a) and (b). At a fixed gate bias (V_g), drain current increases with the drain bias (V_d) linearly before saturation. The on-resistance (R_{on}) is defined as the slope in this region, which is determined by the total resistance of the device including electrode contact resistance, drain and source access resistance and channel resistance. At high drain bias, I_d saturates and the saturation current is determined by gate bias because the gate modulates the charge density in the channel. The transconductance (g_m) is defined as the ratio of the drain current change to the gate bias change. As it represents the control ability of the gate on the channel and thus relates to the high frequency performance of the device, it is an important parameter in the transfer characteristics. As shown in Fig. 2.9, the device is usually working at negative gate bias as it is a depletion mode GaN HEMT. A negative gate bias is needed to induce electric field to pinch off the channel.

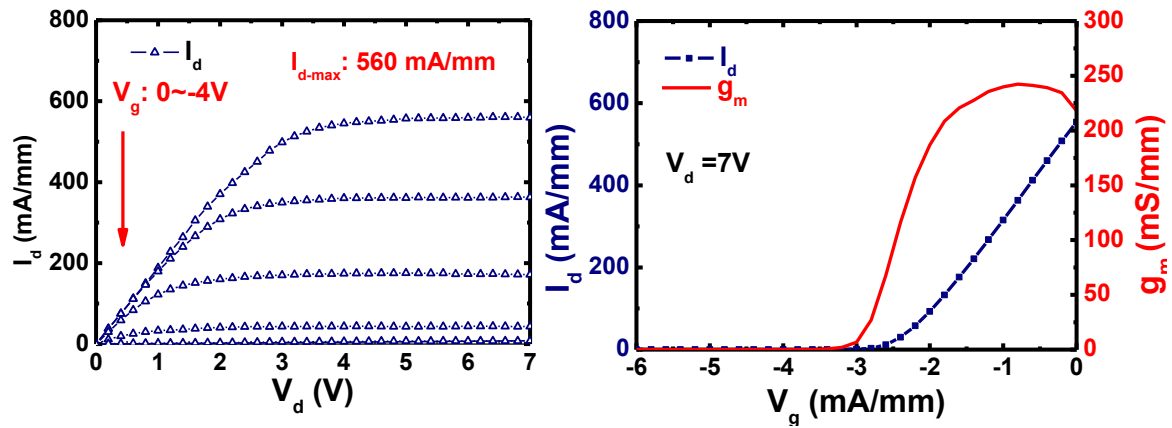


Fig. 2.9 (a) output and (b) transfer characteristics of fabricated conventional AlGaN/GaN HEMT

2.4. RF characteristics for GaN HEMTs

In this work, small signal RF performance was measured by a Keysight N5242 PNA Network Analyzer. The setup of the RF measurement system is shown in Fig. 2.10.

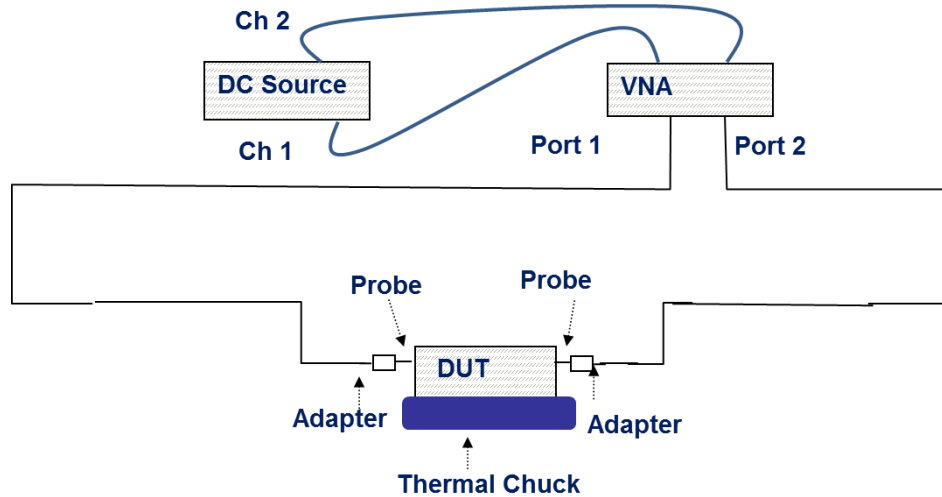


Fig. 2.10 System setup for small signal RF measurement

DC bias generated from the DC power supply (Agilent B2900A) is combined with the high frequency small signal from VNA by the internal bias tee of the VNA. Then the mixed DC-RF signal is applied to the device under test (DUT) by the 150 μm microwave probe. Before measurement, a standard Short-Open-Load-Through (SOLT) calibration procedure is needed to remove the influence of the S-parameters from the cables, adaptors and the VNA's internal parts.

By measuring the input and output signal of the two-port HEMT device, the S-parameters which are used to calculate the RF performance of the DUT can be obtained. Current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are two of the most important parameters to represent the small signal RF performance of a GaN

HEMT. f_T is defined as the frequency that the magnitude of the current gain (h_{21}) which is the ratio of the small signal output current (I_d) and input current (I_g), becomes unity. Generally, h_{21} rolls off with -10 dB/decade slope at high frequency range and closely related to the electron transit time of the device. The definition of f_{max} is the frequency that the power gain (G_u) becomes unity. It represents the maximum frequency at which the RF device can operate as an amplifier.

For the fabricated GaN HEMT device, its equivalent circuit (will be discussed in detail in chapter 3) consists of both intrinsic and extrinsic components. The S-parameters measured by the RF measurement system include the impact of resistance, capacitance and inductance introduced by the interconnect pad and the access region, etc.

The devices in this work have the layout with contact pads for characterize purpose. For the device with a long channel region, the effect of the extrinsic components is minimal because the pad capacitance is small compared with the gate capacitance. However, for a deeply scaled device, the difference between the intrinsic and extrinsic device performance becomes non-negligible. It is important to extract the accurate intrinsic parameters to evaluate the device performance by de-embedding.

There are two commonly used de-embedding methods which are cold/hot FET de-embedding [9] and open-short de-embedding [10]. For the cold/hot FET de-embedding method, the parasitic resistance and inductance are obtained by measuring the device at ON-state (hot FET). And the parasitic capacitance is obtained by measuring the device at pinch-off state (cold FET) [9]. However, since this method is based on device modeling, there is a high possibility that the calculated device parameters are different from real

device which can result in error. The other de-embedding method, open-short de-embedding requires additional open and short structures for parameter extraction, which are shown in Fig. 2.11. The basic layout of the open and short structures is the same as the device under test. While for the open structure, the source and drain are isolated with each other by mesa etching, which means it doesn't have a channel region or gate electrode. For the short structure, the source and drain electrodes are shorted with metal. The intrinsic performance of the device without pad parasitic effect can be calculated with the measured S-parameters of the DUT, open structure and short structure [10]. The measured S-parameters of all structures and device were firstly transformed to Y-parameters. And then the de-embedded Y-parameters of the measured device can be obtained through the equation as following [10].

$$Y_{de-embedded} = [(Y_{Dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}]^{-1} \quad (2.1)$$

Since for this de-embedding method, the de-embedded S-parameters are obtained directly through subtracting the measured pad data from device data instead of extracting every component through the calculation based on device modeling, it helps to avoid the error effect in the cold/hot FET de-embedding method. In this work, open-short de-embedding method was used for all the fabricated devices.

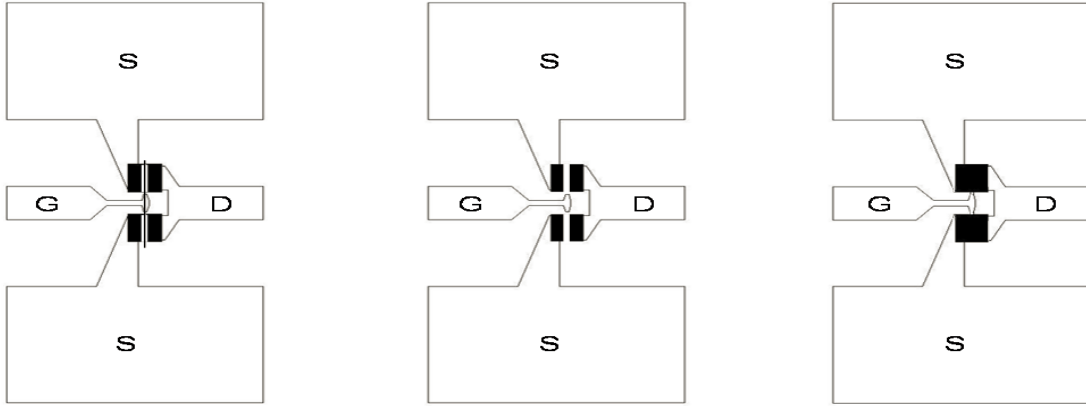


Figure 2-11 (a) device under test, (b) open structure, and (c) short structure [10]

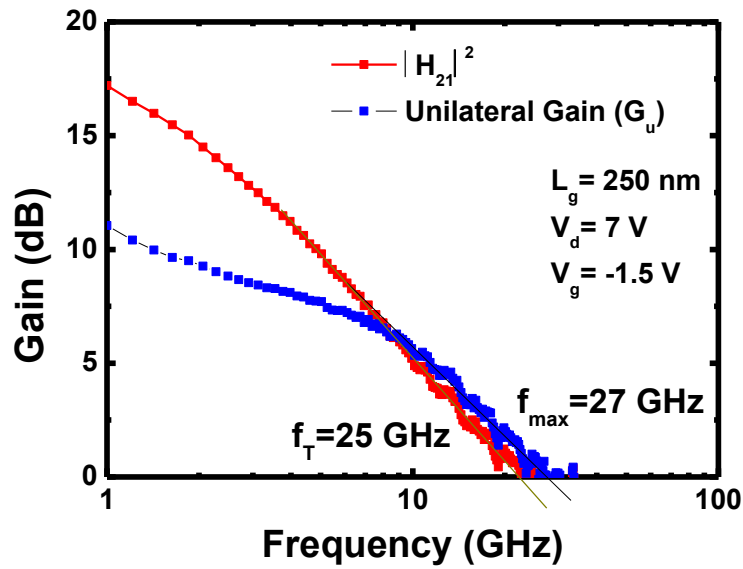


Fig. 2.12 RF characteristics of AlGaIn/GaN HEMT with gate length of 250 nm

A typical small signal microwave characteristic of conventional AlGaIn/GaN HEMT with gate length of 250 nm is shown in Fig. 2.12. At V_d of 7 V and V_g of -1.5 V, maximum f_T of 25 GHz and f_{max} of 27 GHz were obtained, respectively. This bias condition is close to that with maximum g_m . Generally, the f_T and f_{max} will increase by shrinking down the gate length due to the increase in the vertical electric field and

decrease of the gate capacitance. The more detailed analysis of RF performance of GaN HEMTs will be discussed in the next chapter.

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Chapter 3: InAlN/GaN HEMTs on Si with high operation frequency

3.1. Introduction

In the past decades, conventional AlGaIn/GaN HEMT for high frequency application have been extensively studied [1-11]. As mentioned in the last chapter, f_T is one of the most important parameters to represent the high frequency performance of GaN HEMTs and can be expressed by the following equation:

$$f_T \approx \frac{v_e}{2\pi L_g} \quad (3.1)$$

where v_e represents the electron drift velocity under the gate region. To improve the high frequency performance, scaling of the gate length has always been one of the most straight forward and effective methods. To date, the gate length of AlGaIn/GaN HEMTs reported is as small as 30 nm with a f_T of 181 GHz [8]

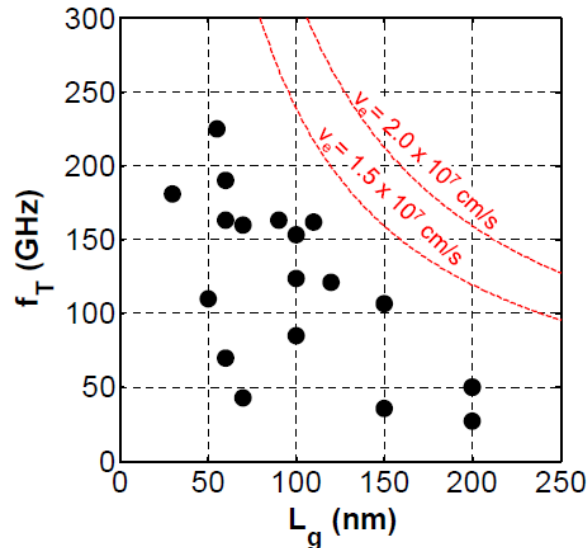


Fig. 3.1 Reported f_T values of AlGaIn/GaN HEMTs versus gate length in literatures

f_T values versus gate length for AlGaIn/GaN HEMTs reported in literatures are shown in Fig. 3.1. The red dash lines represent the theoretical expected f_T of ideal AlGaIn/GaN HEMTs. As shown in the figure, in spite of the successful scaling of gate length, the maximum operation speed of AlGaIn/GaN HEMT is still much lower than the theoretical expectation based on electron saturation velocity of AlGaIn/GaN heterostructure. In addition, the high frequency performance of scaled AlGaIn/GaN HEMTs is lower than that projected from the performance of device with longer gate length, which indicates the less effectiveness of gate scaling. Moreover, the variation in f_T increases as gate length scales down. Hence, the mechanisms behind the operation speed of GaN HEMTs need to be better understood.

Limitations of high frequency performance of GaN HEMTs are complicated. The speed of a device is affected simultaneously by the intrinsic and extrinsic factors of a device. The intrinsic device represents the area right underneath the gate, which is the essential component of a transistor and the extrinsic part represents all other factors that exclude the intrinsic region. A systematic study of the limiting factors is necessary in order to point to the right direction for optimization of device's high speed performance.

Another concern of GaN HEMTs for high frequency application is the lack of deeply scaled high speed device fabricated on Si. Most of the GaN HEMTs with high performance were reported on SiC. However, GaN HEMT on SiC is not cost-effective and is only available in smaller sizes (≤ 6 inch) which make it less attractive to be adopted commercially. To reduce the cost of GaN HEMTs, Si substrates have attracted

increasing interest in recent years, not only in power electronics applications but also in RF applications. Significant efforts have been made on improving the epitaxial quality of GaN on Si substrates as well as the device fabrication technology. As a result, the performance of RF GaN HEMTs on Si has improved significantly [12]-[18]. However, the high frequency performance of GaN HEMTs on Si still lags behind their counterparts on SiC. The best reported GaN HEMT on Si only exhibited a f_T of 176 GHz with for a gate length of 80 nm [18].

In this chapter, both intrinsic and extrinsic limiting factors in GaN HEMTs for high frequency application will be investigated. Key parameters affecting the device operation speed will be discussed. Novel device design and various fabrication techniques will be introduced. Finally, a novel 40-nm gate InAlN/GaN HEMT on Si substrate with a record f_T of 250 GHz is demonstrated.

3.2. Limiting factors in GaN HEMTs for high frequency operation

3.2.1. Delay analysis model of GaN HEMTs

In order to investigate the limiting factors in GaN HEMTs which affect the f_T value, a proper analysis tool is necessary. By its definition, f_T is the frequency point that the small signal short circuit gain (h_{21}) becomes unity and it is closely related with delay components of a GaN HEMT device as shown in the equations below [19]:

$$\tau_T = \frac{1}{2\pi f_T} \quad (3.2)$$

$$\begin{aligned}\tau_T &= \frac{C_{gs.int} + C_{gd.int}}{g_{m.int}} + \frac{C_{gs.ext} + C_{gd.ext}}{g_{m.int}} + (R_s + R_d)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{sd}}{g_{m.int}}] \\ &= \tau_{int} + \tau_{ext} + \tau_p\end{aligned}\quad (3.3)$$

The total delay τ_T of a HEMT can be divided into three components namely intrinsic delay τ_{int} , extrinsic delay τ_{ext} and parasitic charging delay τ_p . $C_{gs.int}$ and $C_{gd.int}$ are the intrinsic gate-to-source and gate-to-drain capacitances, respectively, which are due to the direct coupling between the gate electrode and the intrinsic channel under the gate. $C_{gs.ext}$ and $C_{gd.ext}$ are the extrinsic gate-to-source and gate-to-drain capacitance, respectively, from the coupling between the gate electrode and the 2DEG channel outside the intrinsic region. $g_{m.int}$ is the intrinsic transconductance; R_s and R_d are source and drain resistances, respectively; and g_{sd} is the output conductance. This delay analysis model was first proposed in [19] for the study of InGaAs HEMTs with ultrahigh operation frequency of 600 GHz. Based on this model, the schematic diagram and its small signal equivalent circuit of a GaN HEMT are shown in Fig. 3.2. Different from other conventional delay analysis models, the gate capacitance is divided into two parts which are intrinsic gate capacitance and extrinsic gate capacitance. Benefiting from the deep understanding in device physics and systematical mathematical analysis, this delay analysis method is a valuable tool to study the high frequency performance of GaN HEMTs.

In this chapter, limiting factors of the three delay components will be discussed and some novel methods to overcome these limitations will be investigated.

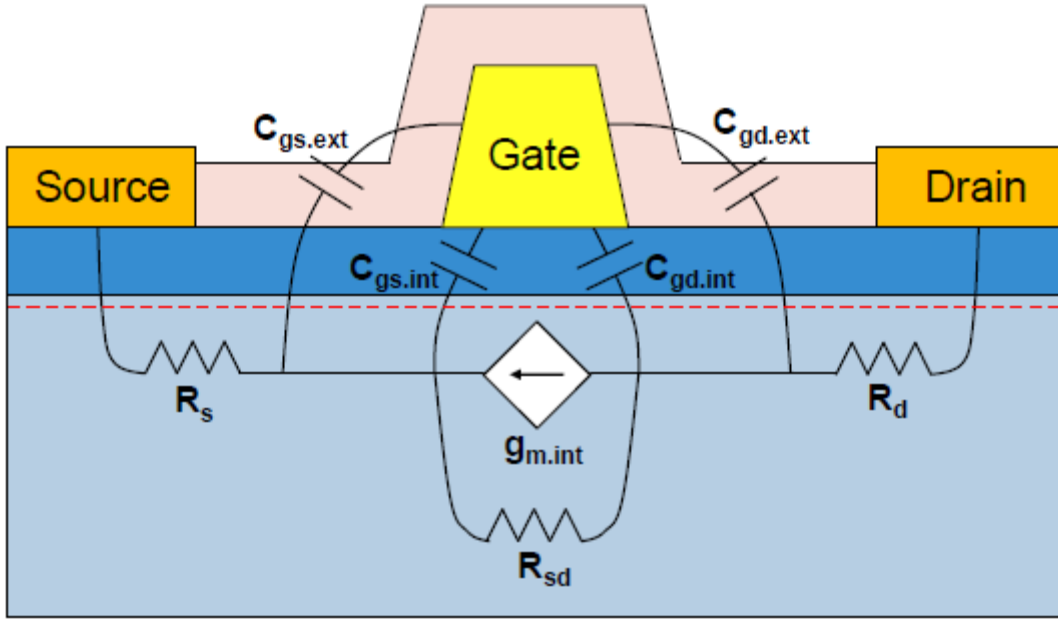


Fig. 3.2 Schematic diagram and its small signal equivalent circuit of a GaN HEMT

3.2.2. Intrinsic limits in GaN HEMTs

The intrinsic delay is the essential delay component in a field effect transistor (FET). As the RF signal injects from the gate terminal, V_g and electric field in the channel vary with time. Following the changing electric field, the electrons in the channel are charged or discharge. The intrinsic delay represents the time needed for electrons to response to the change of V_g and can be expressed as follows:

$$\tau_{int} = \frac{\partial(-q_{int.c})/\partial V_{gs}}{\partial i_d/\partial V_{gs}} = \frac{C_{gs.int} + C_{gd.int}}{g_{m.int}} \quad (3.4)$$

where $q_{int.c}$ is the intrinsic channel charge; i_d is the drain current; V_{gs} is the gate to source voltage and $g_{m.int}$ is the intrinsic transconductance of the device. As shown in equation (3.4), in order to achieve low intrinsic delay τ_{int} , the intrinsic gate capacitance ($C_{gs.int} +$

$C_{gd.int}$) should be minimized while the intrinsic transconductance $g_{m.int}$ should be maximized. From equation (3.3), $g_{m.int}$ also affects the extrinsic and parasitic charging delays. Nevertheless, a higher $g_{m.int}$ will result in lower τ_{ext} , τ_p and thus τ_T . As $g_{m.int}$ is the key parameter of the intrinsic device and reflects the relationship between the gate and intrinsic channel, it is mainly discussed in this section. The intrinsic gate capacitance and transconductance of a scaled HEMT can be expressed by the following equations [20]:

$$C_{gs.int} + C_{gd.int} = \alpha \cdot C_{g.unit} \cdot W_g \cdot L_g \quad (3.5)$$

$$g_{m.int} = \beta \cdot C_{g.unit} \cdot W_g \cdot v_{sat} \quad (3.6)$$

where $C_{g.unit}$ is the gate capacitance of a unit area, W_g is the gate width, L_g is the gate length. As for α , it is related to the electron distribution in the underneath the gate electrode. At saturation condition, its value is close to 2/3. On the other hand, β is a factor represents the electrons' drift velocity and the modulation efficiency of gate electrode. As the lateral electric field under the gate increases, more and more electrons reach their saturation velocity. The value of β factor will also increase and close to unity with the increasing number of electrons reaching their saturation velocity [20]. However, if the electric field is too high, it has a negative effect on β due to lowered gate modulation efficiency [20]. Intrinsic delay can be simplified as the equation below.

$$\tau_{int} = \frac{\alpha \cdot L_g}{\beta \cdot v_{sat}} \quad (3.7)$$

Based on this equation, there are two possible approaches to achieve low intrinsic delay. The first approach is by gate length scaling. By shortening L_g , intrinsic gate capacitance

can be minimized and higher value of β can be expected by increased electric field in the channel. The other approach is to maintain good gate modulation efficiency when the device scales down. For example by applying thinner top barrier [21]

3.2.3. Extrinsic limits in GaN HEMTs

The intrinsic factors limiting GaN HEMTs working at high frequency have been discussed in the last section. Through the analysis, it can be concluded that if the gate modulation efficiency is maintained as the gate length is scaled down, the intrinsic delay decreases linearly with gate length. However, it is not the same case for the extrinsic limiting factors. For extrinsic delay and parasitic charging delay, they are closely related to extrinsic gate capacitance and source/drain resistance, respectively, as shown in equation (3.3). Thus, they will not decrease with gate length. Fig. 3.3 shows the delay components of the devices with difference gate length reported in [21]. It clearly indicates that extrinsic delay component plays a more and more important role as gate length scales down. As shown in the figure, for the device with L_g of 122 nm, intrinsic delay dominates in the total delay. In this case, gate scaling is the best strategy to improve device's speed performance. On the other hand, for the device with L_g of 30 nm, as intrinsic delay has already been minimized, parasitic charging delay and extrinsic delay are more significant limiting factors for the device. Thus, it is important to have a good understanding on the extrinsic limiting factors in deeply scaled GaN HEMTs to further improve the high frequency performance.

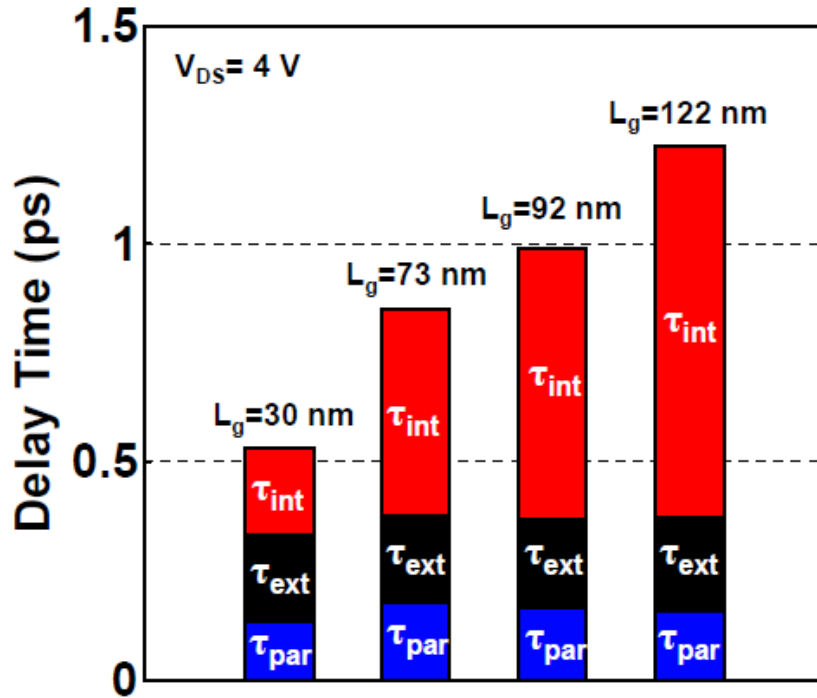


Fig. 3.3 Delay components of devices with different gate length [21]

3.2.3.1. Parasitic charging delay

As mentioned previously in this chapter, parasitic charging delay can be expressed as

$$\tau_p = (R_s + R_d)[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{sd}}{g_{m.int}}] \quad (3.8)$$

It can be easily concluded that the parasitic charging delay originates from the source and drain parasitic resistance. Fig 3.4 (a) shows a small signal equivalent circuit of an intrinsic GaN HEMT without R_s or R_d and the output resistance is infinite. For this model, the total delay can be simply expressed as

$$\tau_T = \frac{C_{gs} + C_{gd}}{g_{m.int}} \quad (3.9)$$

The total delay is exactly the time needed for the drain current to charge the gate capacitance ($C_{gs} + C_{gd}$). However, on actual device with R_s , R_d and finite output resistance, the equivalent circuit should be modified as Fig. 3.4 (b) (here we still ignore the effect of gate parasitic capacitance. It will be discussed in the next section.)

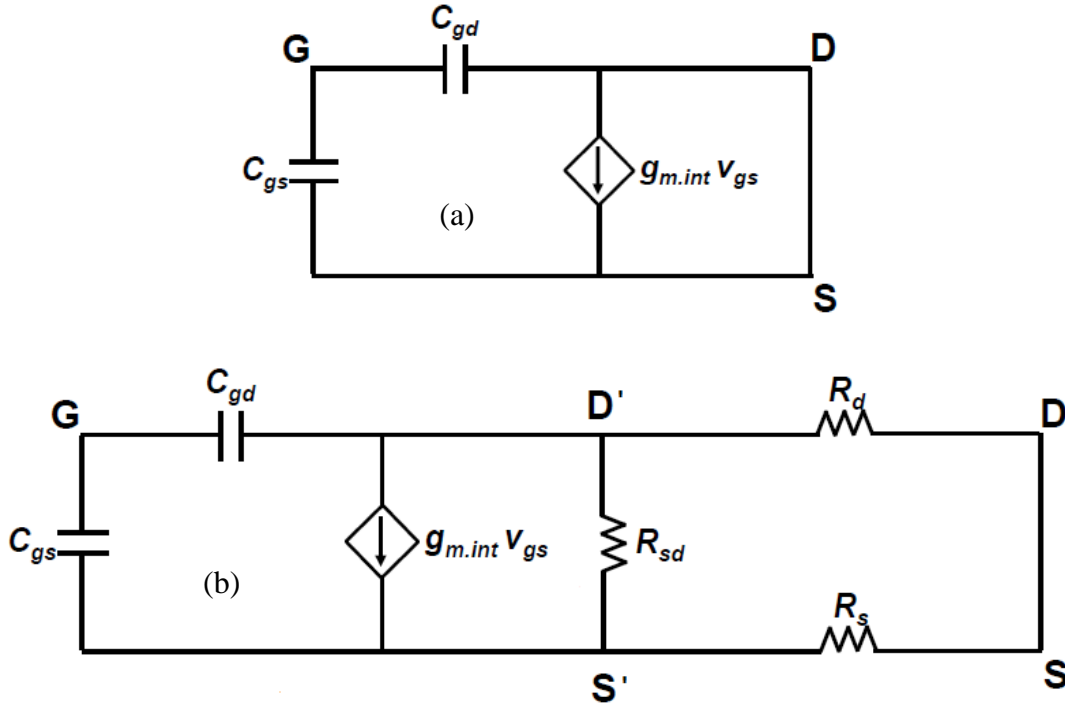


Fig. 3.4 Small signal equivalent circuits of (a) intrinsic device and (b) device with R_s , R_d and finite output resistance

With the effect of R_s , R_d and R_{sd} , the expression of the total delay need to be modified accordingly. Firstly, as R_{sd} is finite, there will be an output current i_o passing through R_{sd} .

It can be expressed as

$$i_o = \frac{i_d \cdot (R_s + R_d)}{R_s + R_d + R_{sd}} = \frac{g_{m.int} \cdot V_{gs}}{1 + R_{sd}/(R_s + R_d)} \quad (3.10)$$

Thus, the effective drain current used to charge the gate capacitance ($C_{gs} + C_{gd}$) will become:

$$i_{d.eff} = i_d - i_o = \frac{g_{m.int} \cdot V_{gs}}{1 + (R_s + R_d)/R_{sd}} \quad (3.11)$$

In this case, the effective intrinsic transconductance should be transformed into:

$$g_{m.int.eff} = \frac{i_{d.eff}}{V_{gs}} = \frac{g_{m.int}}{1 + (R_s + R_d)/R_{sd}} \quad (3.12)$$

Secondly, as an amplifier, the voltage drop on R_{sd} is the output voltage V_o , Z is the impedance between gate electrode G and output point D' as shown in Fig. 3.4 (b) and V_{gs} is the input voltage. The output voltage has a Miller effect on the input capacitance C_{gd} . The gain of the device is given by

$$A_v = \frac{V_o}{V_{gs}} = \frac{-i_o \cdot R_{sd}}{V_{gs}} = \frac{-g_{m.int}}{1/R_{sd} + 1/(R_s + R_d)} \quad (3.13)$$

The input current i_{in} passes through C_{gd} is given by

$$i_{in} = \frac{V_{gs} - V_o}{Z} = \frac{V_{gs}(1 - A_v)}{Z} \quad (3.14)$$

Thus, the input impedance is given by:

$$Z_{in} = \frac{V_{gs}}{i_{in}} = \frac{Z}{(1 - A_v)} \quad (3.15)$$

As the impedance is a capacitance C_{gd} , the impedance can thus be expressed as

$$Z = \frac{1}{j\omega C_{gd}} \quad (3.16)$$

If we insert equation (3.16) back into equation (3.15), the input impedance will become:

$$Z_{in} = \frac{1}{C_{gd}(1 - A_v)j\omega} = \frac{1}{C'_{gd}j\omega} \quad (3.17)$$

where C'_{gd} is the input impedance after take Miller effect into consideration.

$$C'_{gd} = C_{gd} \cdot (1 - A_v) = \left(1 + \frac{g_{m.int}}{1/R_{sd} + 1/(R_s + R_d)}\right) C_{gd} \quad (3.18)$$

Finally, we put equation (3.12) and (3.18) back into (3.9), and let $g_{m.int,eff}$ and C_{gd}' replace the original $g_{m.int}$ and C_{gd} , the total delay will become:

$$\tau_T = \frac{C_{gs} + C_{gd}}{g_{m.int}} + (R_s + R_d) \cdot C_{gd} + (R_s + R_d) \cdot [(C_{gs} + C_{gd}) \frac{g_{sd}}{g_{m.int}}] \quad (3.19)$$

where g_{sd} is the output conductance which is inverse to output resistance. Compared to equation (3.9), the first part in equation (3.19) represents the original intrinsic delay while the additional two parts represent the parasitic charging delay τ_p . It is obvious that in order to minimize τ_p , one way is to minimize the source and drain resistance and the other way is to increase the output resistance.

3.2.3.2. Extrinsic delay

The extrinsic delay is given by:

$$\tau_{ext} = \frac{C_{gs.ext} + C_{gd.ext}}{g_{m.int}} \quad (3.20)$$

As described in the last section, $(C_{gs.ext} + C_{gd.ext})$ is the extrinsic gate capacitance and thus the extrinsic delay represents the time needed for the drain current to charge this additional capacitance. Different from the intrinsic gate capacitance which is caused by

the coupling between the gate electrode and 2DEG underneath gate bottom, the extrinsic gate capacitance is caused by the coupling between the gate metal and 2DEG outside the intrinsic device region. Thus, unlike the intrinsic gate capacitance, the extrinsic gate capacitance does not decrease with gate length. As shown in Fig. 3.3, as gate length scales from 122 nm to 30 nm, the extrinsic delay component stay almost unchanged and becomes more and more important as the device scales down. Similar with the parasitic charging delay, the extrinsic delay needs to be studied and minimized to improve the high frequency performance of the device especially with deep sub-100 nm gate length.

It is challenging to systematically investigate extrinsic delay because unlike the analysis for other delay components, the extrinsic gate capacitance cannot be directly expressed by an equation. There are many factors which will affect the extrinsic gate capacitance, such as heterostructure design and gate geometry (gate foot height and gate head length of a T-gate). Passivation also has significant impact on extrinsic gate capacitance, including the thickness of passivation layer and the permittivity of the passivation material. To minimize the extrinsic delay, the gate head of a T-gate device should be kept away from 2DEG which means the height of gate foot should be high enough. Thin layer low-k dielectric material can be applied as passivation layer to avoid increasing extrinsic gate capacitance too much.

3.3. Device scaling

The limiting factors of GaN HEMTs for high frequency have been discussed in the last section. The intrinsic delay, extrinsic delay and parasitic charging delay have also been studied theoretically. As mentioned in section 3.2.2, to minimize the intrinsic delay, gate

scaling is the most straightforward approach. The intrinsic delay is inversely proportional to the square of gate length if the gate modulation efficiency keeps constant as gate length scales down. As for the parasitic charging delay, the key method to minimize its impact is to lower the source and drain resistance.

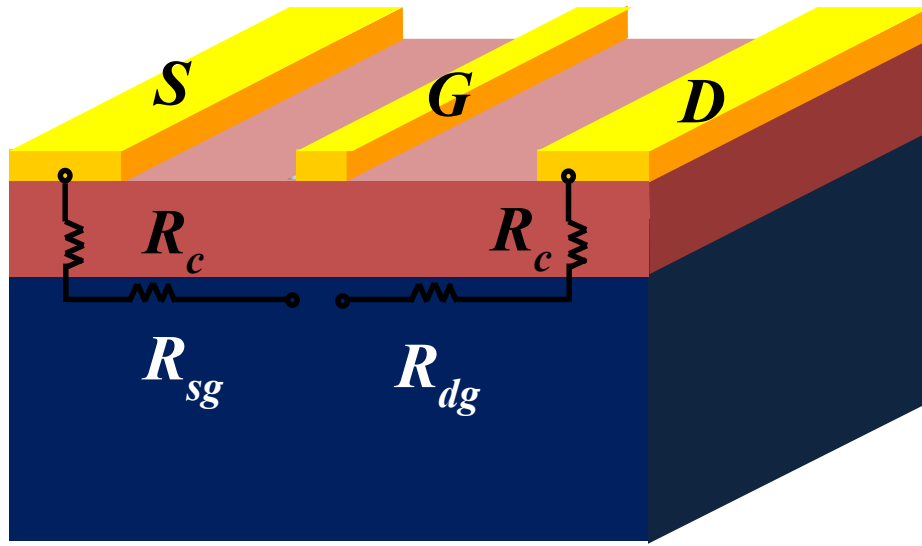


Fig. 3.5 Source and drain resistance in a GaN HEMT

As shown in Fig 3.5, the total R_s or R_d is the combination of contact resistance between ohmic contact metal and 2DEG and sheet resistance of the access region which is between source/drain edge and gate edge. If constant electric field in the channel is assumed, the access resistance is proportional to the source/drain to gate distance (L_{sg} and L_{dg}). Thus, shrinking L_{sg} and L_{dg} is an effective approach to minimize parasitic charging delay.

In conclusion, device scaling is a straightforward strategy to obtain high operation frequency in GaN HEMTs. For examples, a f_T of 300 GHz was reported by D.S. Lee in a device with L_g of 30 nm and L_{sd} of 1 μm in 2011 [21]. Y. Yue also reported a high f_T of

400 GHz in a device with L_g of 30 nm and L_{sd} of 865 nm in 2012 [22]. Finally, by applying 20 nm T-gate and 100 nm source-to-drain distance, Y. Tang pushed the f_T and f_{max} to 454 and 444 GHz [23]. In this section, the key challenges and methods for device scaling will be discussed.

3.3.1. Electron beam lithography technology

The essential challenge to achieve device scaling is to perform pattern transform in deep sub-micron scale. Till now, there are various technologies to realize this goal including electron beam lithography (EBL) [24], x-ray lithography [25] and deep UV Phase Shifting Mask Lithography [26], etc. Among them, EBL technology has the advantages in both the flexibility and resolution. In this work, a Vistech-5200 EBL system was used for sub-micron patterning.

The electron optical column and the functions of the main components are shown in Fig. 3.6 [27]. By applying high voltage on the emitter, electron beam is generated and then modulated by the electron optical system. Finally, the electron beam reaches the sample surface and interacts with the electron beam resist. The spot of the electron beam can be as small as several nanometers and thereby making the pattern in nanoscale possible.

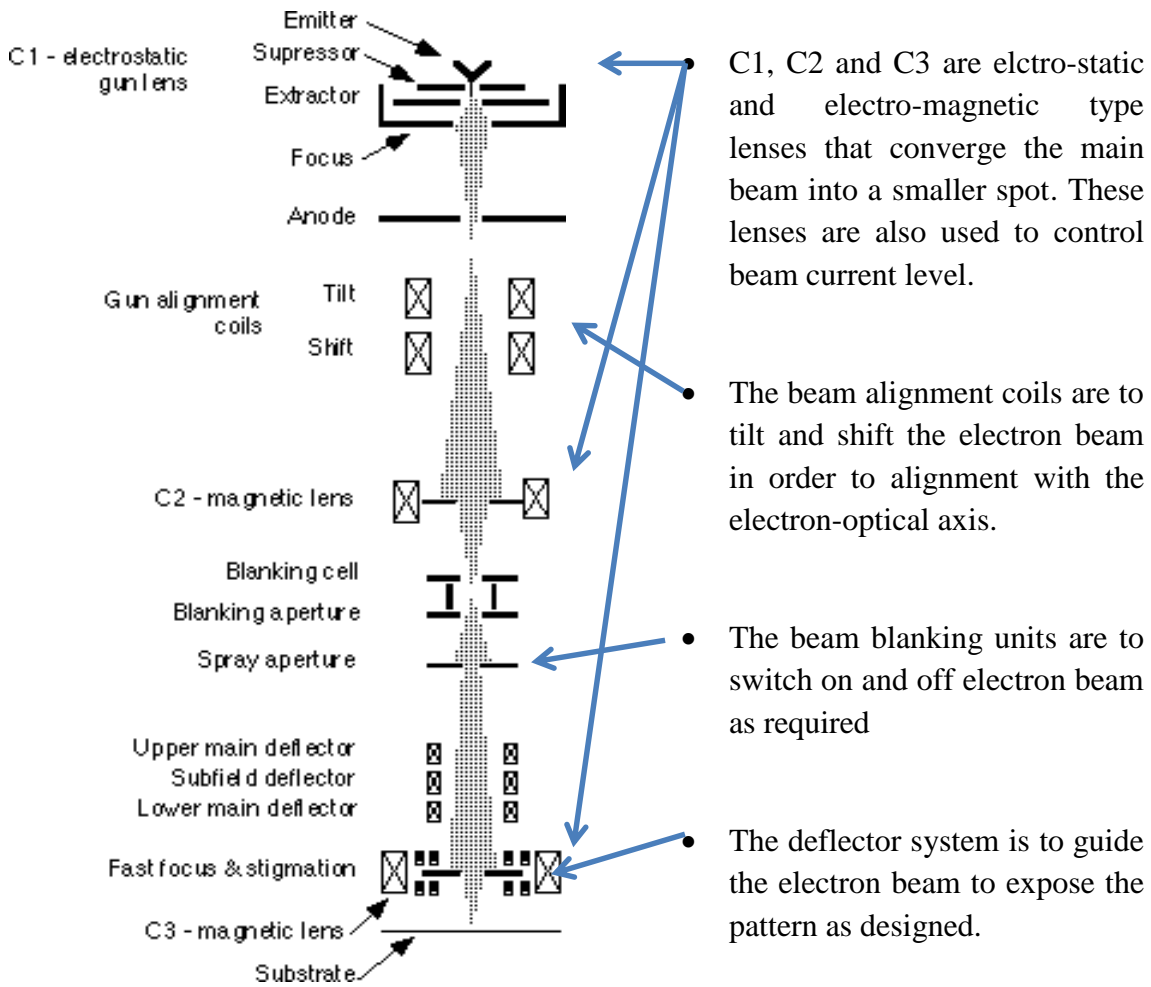


Fig. 3.6 Schematic of an electron-optical column in EBL system and functions of the main components

For a typical EBL process, it mainly consists of the following five steps:

EBL Marker formation

Alignment accuracy is one of the most critical factors for an EBL process, especially for deeply scaled device. Since the channel is only several hundred nanometers, a tiny misalignment of gate may cause serious problem for device performance such as low breakdown voltage due to the shortened drain to gate distance and even short circuit may

occur between gate and source or gate and drain. As for the gate-last process used in this work, all the subsequent layers are aligned with the ohmic contact layer. Thus, the alignment marker should be also fabricated at the same layer as the ohmic contact to minimize any misalignment issue. However, the formation of alignment marker is not that straight forward. Different from other semiconductor device based on GaAs or InP, a high temperature RTA up to 800 °C is necessary for GaN HEMTs to form good ohmic contact with low R_c as discussed in chapter 2. After the annealing, the sample surface is no longer smooth and thereby makes it very difficult for the EBL system to detect the marker.

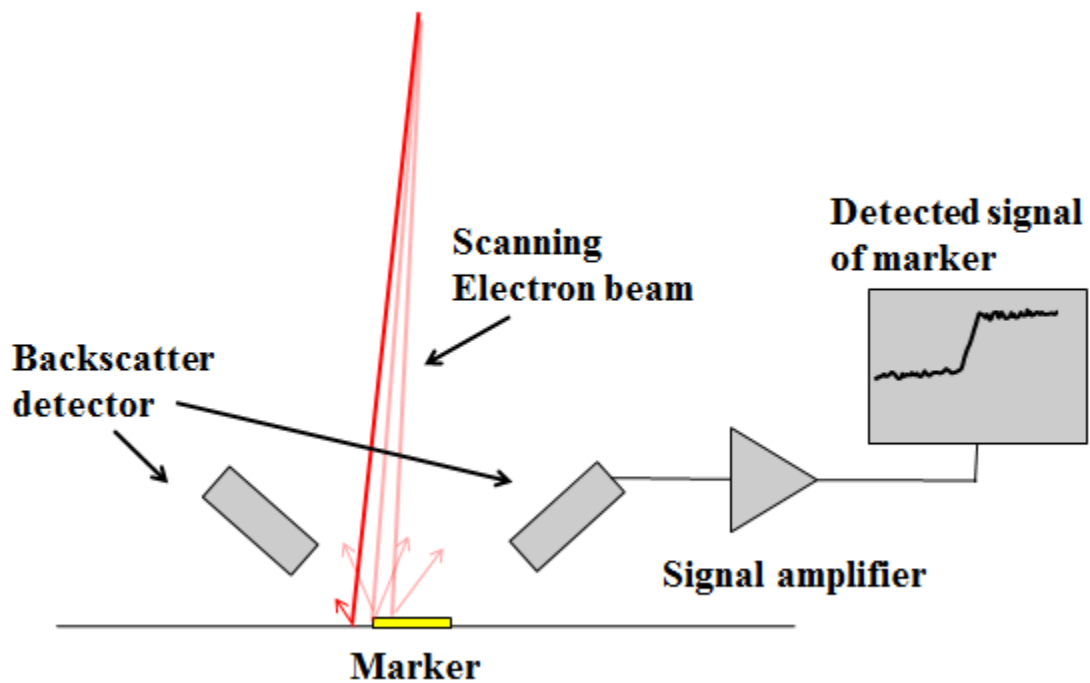
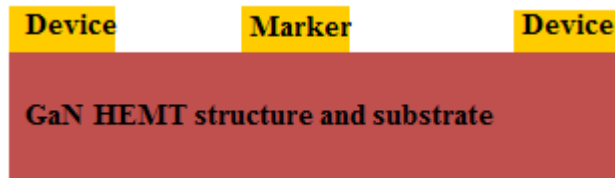


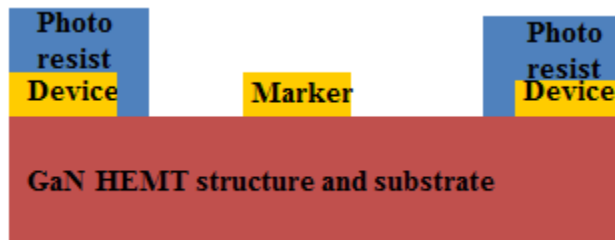
Fig. 3.7 Alignment marker detection

As shown in Fig. 3.7, an alignment marker is detected by the contrast of backscatter signal between the marker and adjacent area. For a good contrast level, the signal from

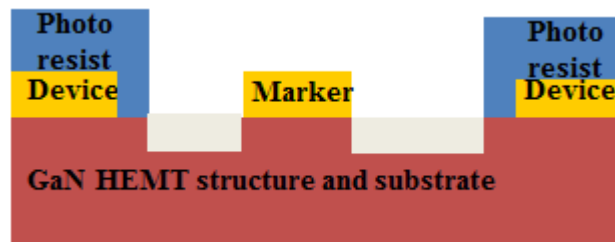
marker should be remained at a stable level, which cannot be realized on the ohmic metal after RTA for GaN HEMTs. In order to solve this problem, an additional step was involved to form the alignment marker before RTA as shown in Fig. 3.8:



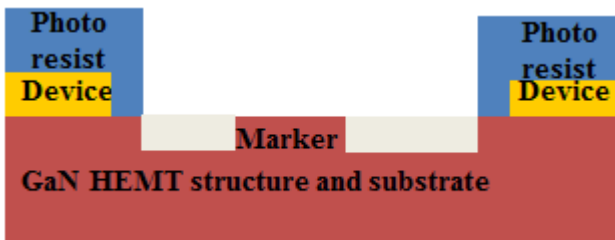
- Start from ohmic metal lift-off



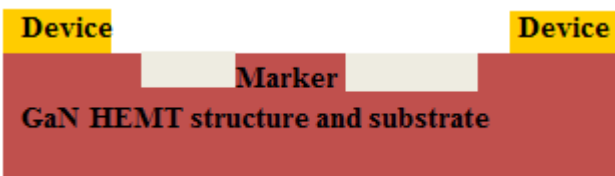
- Device regions are protected by photo resist

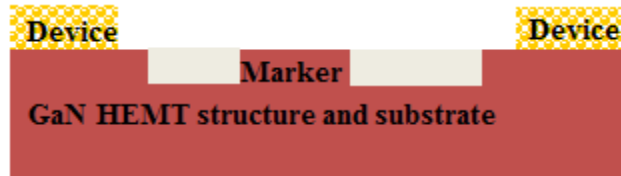


- 500 nm ICP etch of the adjacent area of marker



- Marker metal removal





- RTA of ohmic metal

Fig. 3.8 EBL alignment marker formation

The key method of this additional marker formation step is to form a smooth GaN mesa and use it as the alignment marker instead of the rough ohmic metal after annealing. The process started from ohmic metal lift-off. Then the whole sample was spin-coated with photoresist followed by opening a etch window enclosing the alignment marker by photolithography. Cl_2/BCl_3 plasma ICP dry etching was used to etch down the sample for around 500 nm. During the etching process, the ohmic metal of marker region served as a self-aligned hard mask to protect the GaN underneath. The region outside the etch window is protected by photoresist. Ohmic metal was then removed by aqua regia ($\text{HCl}:\text{HNO}_3 = 1:3$) and BOE. Finally, after stripping off the photo resist, the sample was subjected to RTA for ohmic contact formation. Without metal on top, the marker surface will remain smooth after RTA, which is desirable for subsequent marker detection by the EBL system.

It is also worth noting that the etching depth of 500 nm is an optimized value for this process. Theoretically, the deeper the mesa, the better contrast can be obtained for the subsequent marker detection process. However, there are two drawbacks if the sample is over etched. One is that the mesa marker edge has a finite slope. It means that if the depth is too large, the size of the marker may vary and therefor causes misalignment. Another problem is that a deeper mesa needs a longer etch time. As the temperature increases with

time in ICP chamber, it will harden the resist and makes it difficult to be stripped off. Thus, an optimized thickness of 500 nm was used for all the EBL markers in this work.

Sample Preparation

Similar to photolithography, the sample needs to be spin-coated with resist and baked before exposure in EBL system. Various types of resist can be used in EBL, such as PMMA (poly-methyl methacrylate), MMA (methyl methacrylate), HSQ (hydrogen silsesquioxane) and ZEP 520. Each of them has its pros and cons. PMMA is a high resolution positive resist can be used for general patterning, metal lift-off and usually used to fabricate T-gate together with MMA with a bi-layer process. HSQ is a high resolution negative resist. Its unique property is that after exposure and post bake, it will transform to polycrystalline SiO₂ and thus can be used as hard mask for subsequent plasma dry etching or ion implantation. ZEP 520 is a high resolution positive resist can be used as hard mask for the next processing steps. Here we take a simple one-layer process for ohmic metal lift-off using PMMA950-A4 as an example. Firstly, the sample is cleaned in acetone and IPA with heating and ultrasonic cleaning. The sample is then baked at 105°C to remove the residual solvent. The sample is spin-coated with PMMA at 1200 rpm for 70 seconds, follow by baking at 180 °C for 120 seconds. The cross-section of PMMA after baking is shown in Fig. 3.9. A stable PMMA layer with a thickness of 370 nm was formed on top of the substrate.

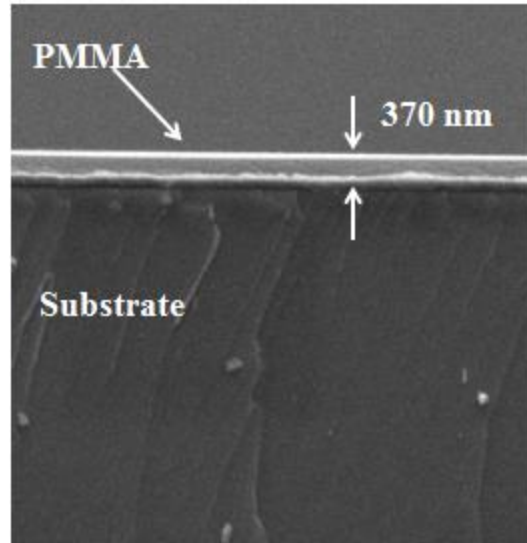


Fig. 3.9 Cross section of a Si sample after spin-coated with PMMA at 1200 rpm for 70 seconds and baked at 180 °C for 120 seconds

Job Generation

This step is to convert the design (in GDS format) to a job file (GPF format for Vistech 5200). EBL has the advantage that the design can be easily modified for each exposure by only regenerate a job file without the need of physical mask. This gives a great flexibility to customize the designs for different device variations. The software “BEAMER” from GenISys was used for this conversion process.

The most important step is the proximity effect correction (PEC) for a job preparation. PEC is the essential method to obtain high feature quality, especially for small features and sharp edges. During exposure, as the electron beam injects onto the sample surface, electrons penetrate into the resist and semiconductor material and react with resist. However, scattering occurs in both resist and substrate material. Forward scattering occurs in resist material and it depends on the electron acceleration voltage, resist

material property and resist thickness. Forward scattering has an impact range of 1 to 10 nm. Back scattering is due to the scattering between the injected electrons and the atoms in substrate. It is closely related to electron acceleration voltage and substrate material property. It has a longer impact range of around 10 μm . Electron trajectories as a function of acceleration voltage is shown in Fig. 3.10 [28]. These scattering effects influence the exposed pattern shape significantly. That is, for a specific area, we should not only consider the dosage applied directly on it, but also the scattering electrons from adjacent region. In this case, the dosage needed for different region in one job could be different. For example, for the region located in the center of a bulk pattern, it will be highly affected by nearby scattering electrons and thus relatively small dosage is enough for full exposure. On the other hand, for an isolated dot or very thin line, relatively high dosage is needed as there are fewer scattering electrons coming from adjacent area. The PEC function takes this effect into consideration. By simulating the absorbed energy in resist versus the distance from electron beam center using Mont Carlo method, interaction between the adjacent features can be calculated. Then, the system will recalculate the dosage needed for different region as shown in Fig. 3.11.

Fig. 3.11 presents a real example after PEC. The features in the figure is colored by dosage, red color represents higher dosage while blue color represents lower dosage and green color is in between. For the center area of the big cross in the left, the assigned dosage is relatively low while for the edge of the small features in the right, the assigned dosage is relatively high. By this way, correct feature shape and sharp edge can be obtained.

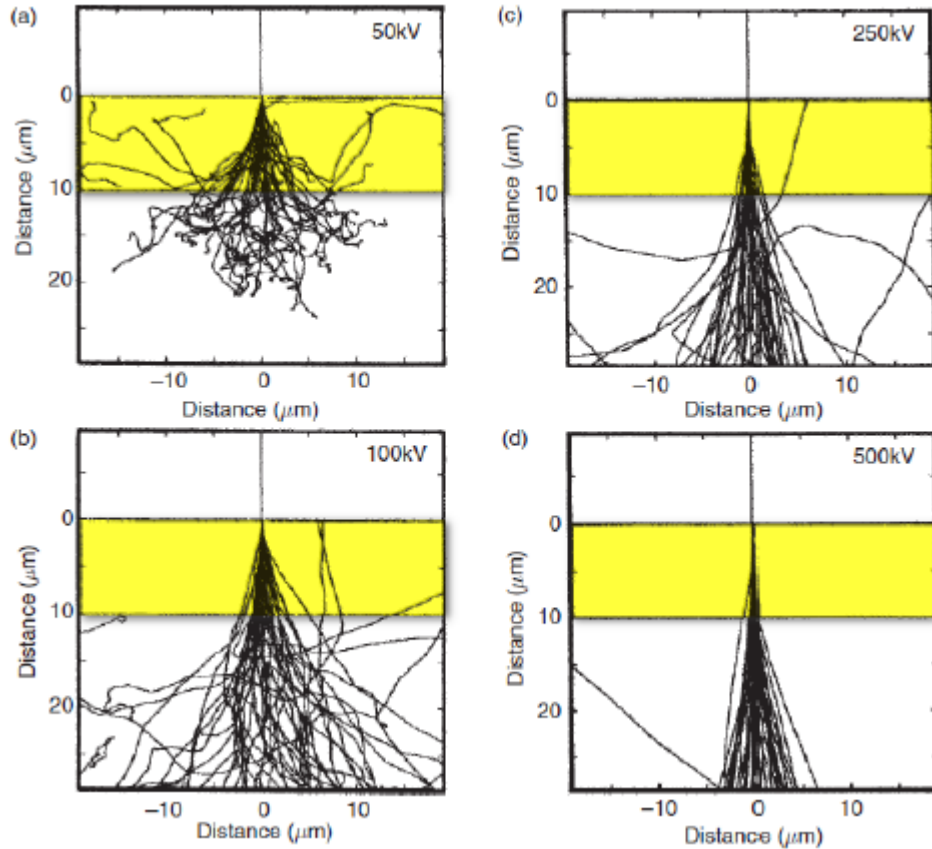


Fig. 3.10 Electron trajectories as function acceleration voltage [28]

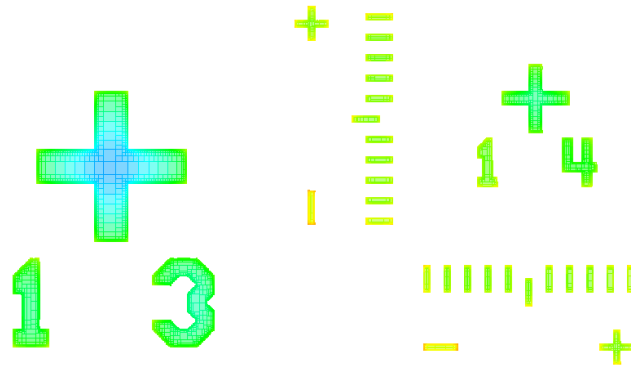


Fig. 3.11 Different dosages assigned for bulk and small features

The last step is to export the edited job. In this step, important factors such as electron acceleration voltage, resolution and beam step size can be adjusted. For the electron

acceleration voltage, Vistech 5200 system works at 100 kV by default. Resolution represents the writing grid resolution of the job. Usually 1 nm is used for optimal result. Beam step size is also known as shot pitch. It indicates the pitch between two shots. Beam step should always be a multiple of writing grid resolution and smaller than electron beam spot size. Otherwise, under dose or roughness may occur.

Exposure

After sample preparation and job generation, sample is ready for the exposure process.

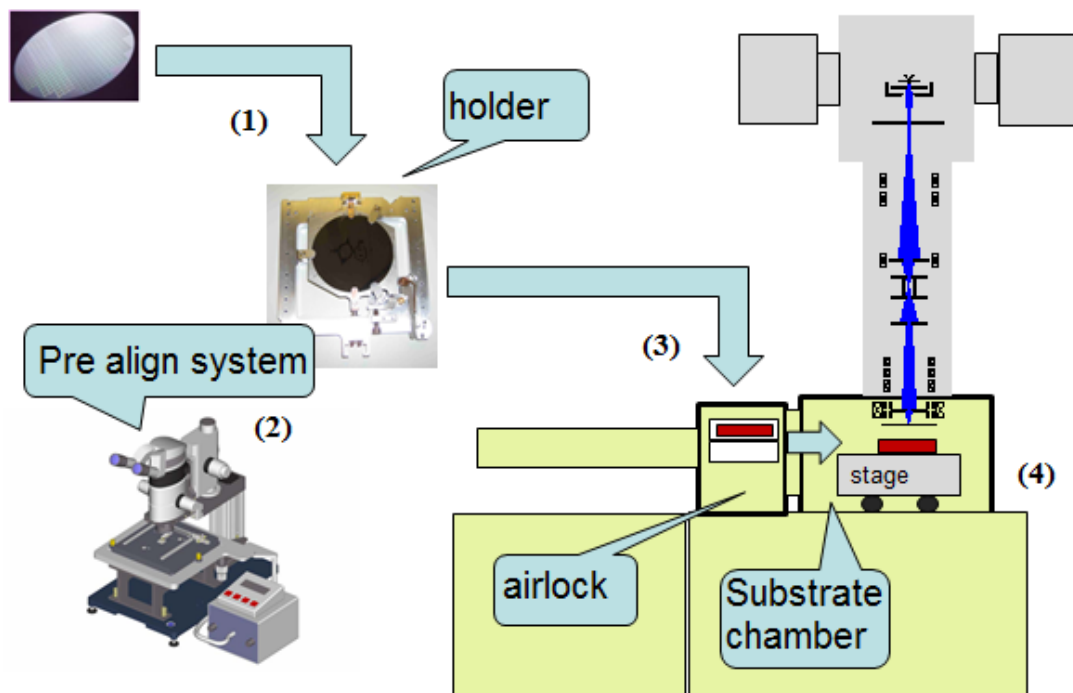


Fig. 3.12 Position of sample in writing chamber [27]

As shown in Fig. 3.12 [27], to position the sample in the writing chamber, the sample should be firstly put onto a holder suitable to its size and make sure the sample surface is in the same plane. Then, the pre-align system is used to locate the alignment markers and record the coordinates. The holder is then put together with the sample into the airlock.

After reaching the desired vacuum level, the holder is transported into the writing chamber and then the system is ready for alignment based on the maker coordinates and then then follow by electron beam exposure. For electron beam writing, different beam current can be used. Generally, a larger beam current has a larger beam spot size and thus lower in resolution but higher in writing speed while a smaller beam current gives the opposite effect. Hence, a tradeoff is necessary between the resolution and speed. The choice of beam current is highly related to the feature to be written. For bulk features, resolution is usually not the first concern and it is more attractive to save process time. On the other hand, for very small features, resolution is more important and the writing time is usually not a problem because the exposed area is relatively small.

Developing and descum

After exposure, the resist stack is developed in 1:3 MIBK (Methyl isobutyl ketone) to IPA solution for 90 seconds followed by rinsing in IPA for another 30 seconds to make sure there is no residual MIBK on the sample surface. A post exposure bake at 105 °C for 2 minutes is optional to hardening the resist stack. Fig. 3.13 shows a SEM image of PMMA pattern after developing.

After checking the patterns under the microscope, a descum process is needed to make sure there is no residual resist on the exposed region. O₂ plasma is used to strip off about 30 nm of the resist. After the subsequent processes such as metal deposition and plasma dry etching, PMMA can then be easily removed by acetone.

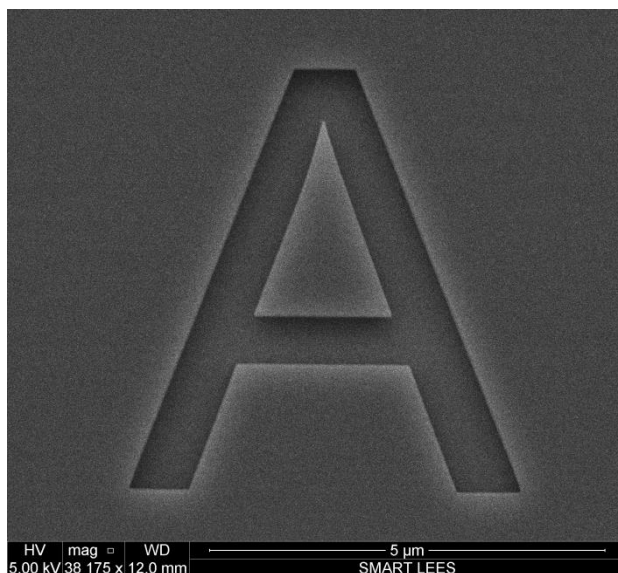


Fig. 3.13 PMMA after developing

3.3.2. Deeply scaled gate and sub-micron channel

Taking the advantage of the high resolution EBL system, deeply scaled gate and sub-micron channel have been developed for GaN HEMTs to achieve low intrinsic and parasitic charging delay as discussed previously in this chapter.

PMMA 950 series resist is used for the developing of short gate and channel. PMMA has a high resolution, high contrast and relatively wide process window for dosage. On the contrast, other positive resist such as MMA, is too sensitive for the dosage applied and a small change in dosage can lead to feature size difference which makes it unsuitable for small features. Processed with the Vistech 5200 EBL system, sharp line with the width down to 16 nm can be obtained on 370 nm PMMA stack as shown in Fig. 3.14.

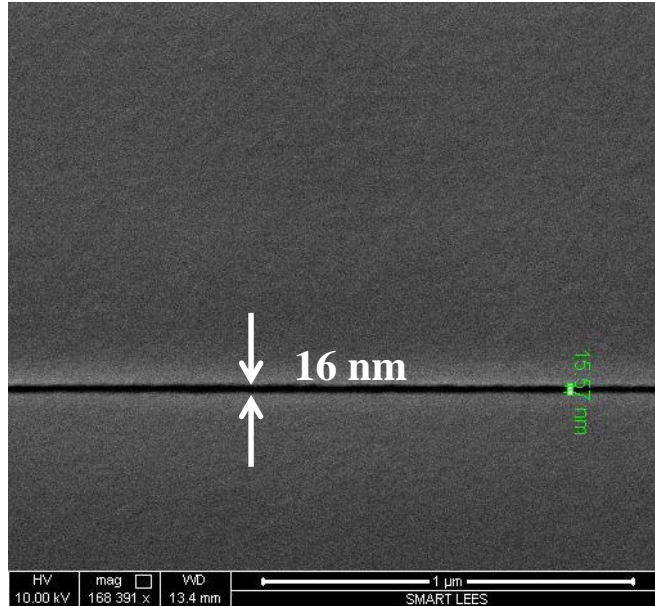


Fig. 3.14 16 nm isolated line on PMMA with thickness of 370 nm

Generally, gate technology used for RF device is based on T-shaped gate as discussed in chapter 2 in order to maintain low gate resistance at short gate length. However, as gate length goes down to sub-100 nm, the formation of T-gate becomes challenging. T-gate is usually formed by a bi-layer (MMA-PMMA) process. With a relatively thick resist stack, the scattering issue discussed in the last section becomes worse and difficult to obtain sub-100 nm gate foot. In fact, based on the bi-layer technique with resist stack of MMA 500 nm and PMMA 150 nm, the shortest gate foot print achieved in this work was 80 nm. An alternative method which consists of two-time exposures can overcome this issue [29]. Different from the bi-layer process, gate foot and head are written separately. With a thinner resist stack, shorter gate foot print can be achieved. However, the plasma dry etch process involved usually degrades device performance by damaging the channel surface. Moreover, as discussed in previous section, extrinsic gate capacitance is the origin of extrinsic delay and it becomes more significant as device

scales down. The coupling between large gate head and 2DEG will increase the extrinsic gate capacitance and thereby degrading the high speed performance of the device.

In order to avoid the issues mentioned above, sub-100 nm rectangular gate was developed in this work. Although the gate resistance is high due to the relatively smaller cross sectional area compared with T-gate, it does not affect the speed analysis of device based on f_T . Moreover, a single layer one-time exposure process of proposed rectangular gate simplifies the device fabrication.

Following the process flow for the EBL process described in the last section, PMMA was firstly spin-coated on sample. Different from the resist stack of 370 nm used for ohmic contact, a thinner resist of 200 nm was used in order to have higher resolution for the development of short gate. Very small beam current of 0.1 nA with beam spot size of 25 nm was used for exposure to have the best resolution. During exposure, the scattering effect will create an undercut profile as shown in Fig. 3.15. Finally, bi-layer gate metal stack of Ni and Au for 30 and 100 nm was deposited and followed by lift-off.

As isolated patterns, the dosage needed for sub-100 nm gate is much higher than bulk patterns. Dosage of $1400 \mu\text{C}/\text{cm}^2$ was used to fully expose the sharp edge of the gate. Finally, deeply scaled rectangular gates with lengths down to 40 nm were successfully developed on GaN HEMTs.

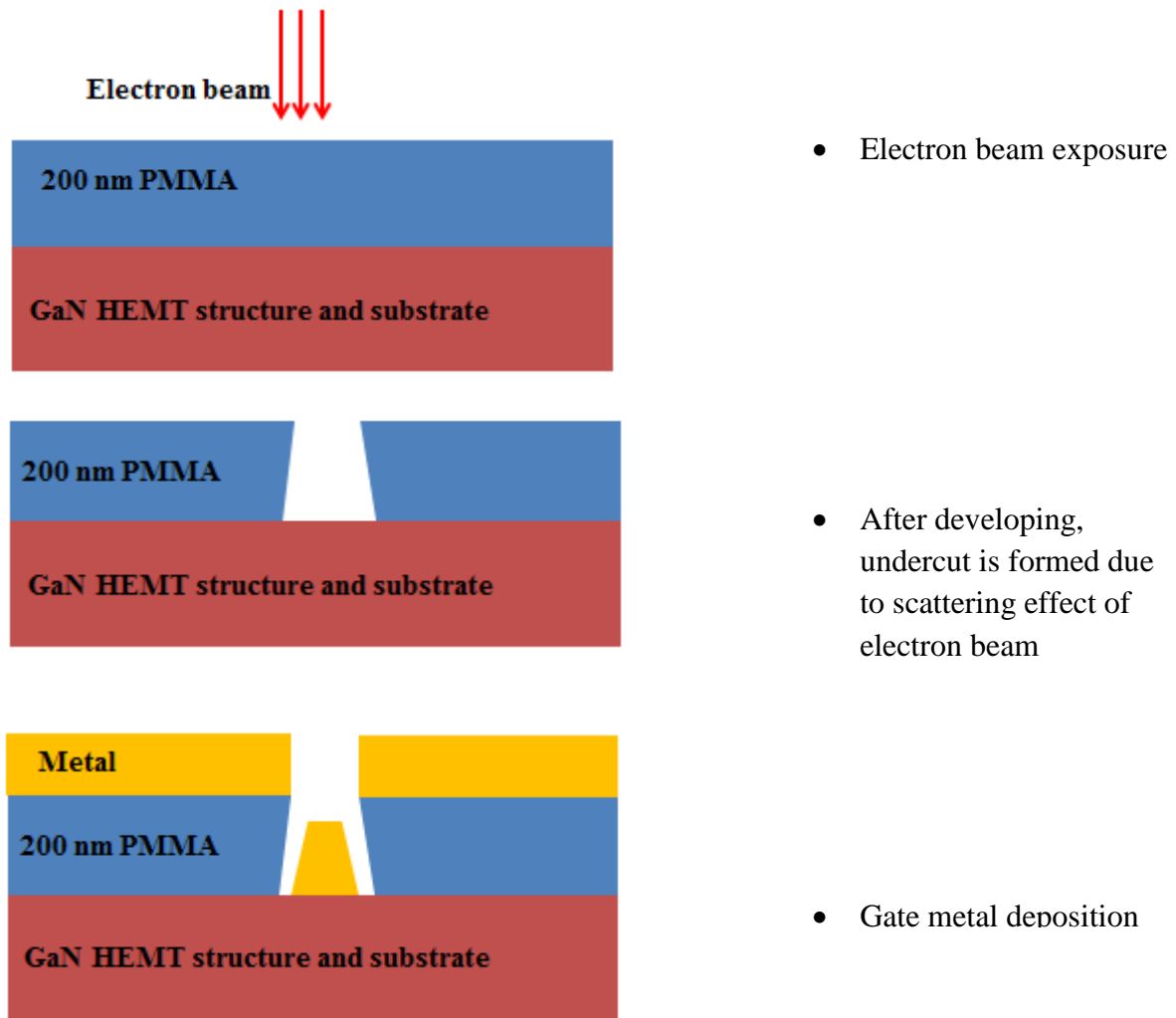


Fig.3.15 Process flow for gate formation

For the development of short channel, the process is basically the same as gate formation. The difference is that the resist stack for ohmic metal is 370 nm because the thickness of four layer ohmic metal stack of Ti/Al/Ni/Au is more than 200 nm, which is much thicker than gate metal. The process flow of channel formation is shown in Fig. 3.16.

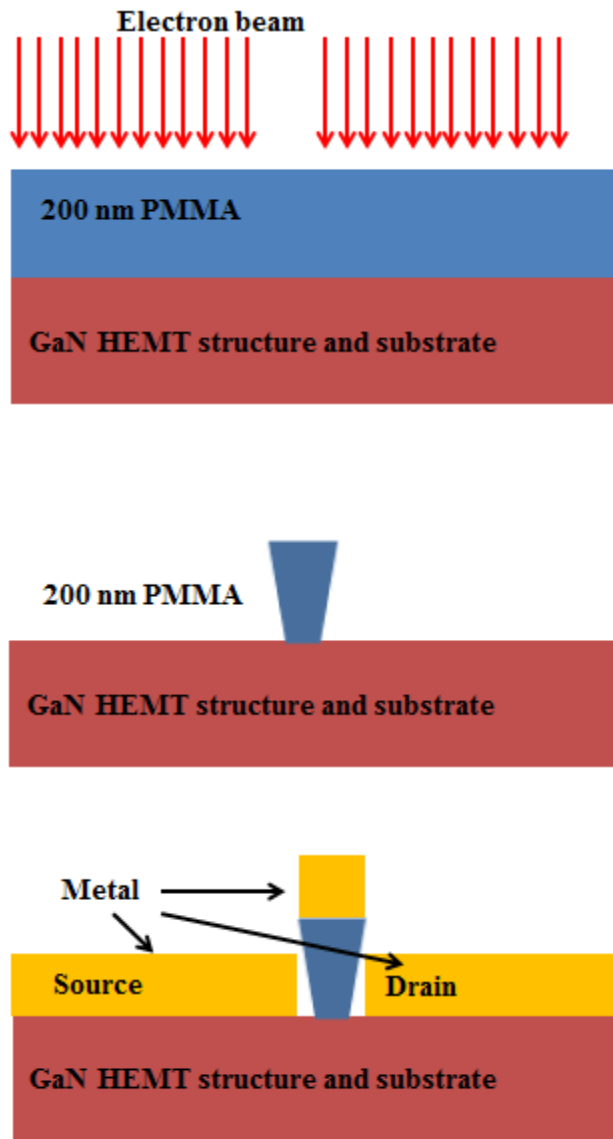


Fig.3.16 Process flow for channel formation

In contrast to gate formation, the formation of the ohmic pattern for source and drain requires only a narrow stack (which is source-to-drain distance) of PMMA to be remained on the sample after exposure and developing. It is challenging because the unexposed PMMA region is very easy to be affected by the surrounding area as discussed in the last section. Actually, for the same EBL system, the resolution for an isolated line is always higher than a pitch between two bulk patterns [28]. Proximity effect correction

is necessary to obtain a channel with uniform length. Different dosage was assigned for different regions. For example, a lower dosage is needed for the center of the channel while a higher dosage is needed for the edge of the channel.

Another issue for channel formation is that as discussed in chapter 2, high temperature RTA is needed for alloy-based ohmic contact formation in GaN HEMTs. After annealing, not only the surface of ohmic metal becomes rough, but also the edges of the metal. The SEM images of a channel before and after RTA are shown in Fig. 3.17.

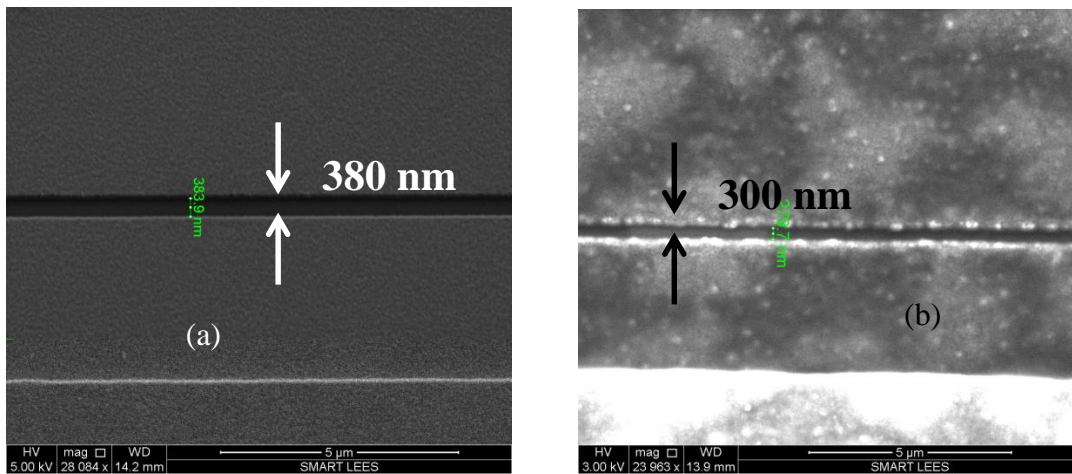


Fig. 3.17 SEM image of a short channel (a) before and (b) after annealing

As shown in Fig.3.17 (a), the ohmic metal surface is smooth and the channel edges are sharp. However, after RTA, as shown in Fig.3.17 (b), both the metal surface and channel edges became rough. The roughness at the edges of ohmic metal can be several tens of nanometers. This is negligible for device with channel length of several microns. However, it becomes non-negligible as channel length scales down. This roughness may cause short circuit between ohmic metal and gate. Another phenomenon worth to notice is that after RTA, there is an expansion of ohmic metal. As a result the channel length is

shrunk from 380 nm to 300 nm. This effect needs to be taken into consideration when designing the device layout.

In this work, a minimum channel length of 300 nm was developed for GaN HEMTs with alloy ohmic contact. To further shrink the channel, other ohmic contact technology such as n^{++} regrowth without surface and edge roughness issue can be applied [23].

3.4. Thin InAlN top barrier GaN HEMTs on Si

Based on the delay analysis in this chapter, besides lateral device scaling, other factors such as gate modulation efficiency and ohmic contact resistance also have great impact on high frequency of GaN HEMTs through both the intrinsic and parasitic delay components. In particular for deeply scaled device, gate modulation efficiency becomes a serious concern and ultimately limits GaN HEMTs for high frequency application [8]. Also, the contact resistance R_c plays a more important role in the total parasitic charging delay as the access resistance has already been minimized by channel scaling. In this work, a GaN HEMT on Si with novel thin InAlN top barrier is successfully demonstrated with excellent high speed performance.

3.4.1. Advantages in InAlN as top barrier

For a field effect transistor, in order to ensure proper operation of the device, the vertical electric field induced by gate electrode should be significantly larger compared with the lateral electric field in the channel. Under this condition, the gate electrode has an effective modulation to the drain current through controlling the electron density in the channel. However, as gate length scales down, the vertical electric field is reduced by the increased lateral electric field, especially for the device with sub-100 nm gate. By losing

its controllability to the channel charge density, gate modulation efficiency decreases. As discussed in chapter 2, most of the conventional GaN HEMTs are based on $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ ($x < 0.35$) heterostructure with a thickness of 20 to 30 nm to generate enough 2DEG density as well as prevent gate leakage current. The thickness of AlGaN barrier is small enough to have a good gate modulation efficiency for long-gate device ($L_g > 200$ nm) [1, 2]. However, poor gate electrostatics were observed in short gate AlGaN/GaN HEMTs as shown in Fig. 3.1 [8].

To solve this problem, vertical electric field needed to be increased by using a thinner top barrier. One method is to grow a thinner AlGaN layer for the device. However, a thin AlGaN barrier leads to lower 2DEG density, thus causing the increase in access/contact resistance and the decrease in current drivability. Another way is to thin down the top barrier by gate recess technology based on plasma etching [10, 30, 31]. However, since the gate length is very small, it is challenging to obtain uniform recess profile. Moreover, the plasma etching process involved induces damage to the channel which in turn will degrade the electron transport property as reported in [32-34].

Besides conventional AlGaN top barrier with low Al concentration, novel materials with higher Al concentration including $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($x > 0.35$), AlN, InAlN and InAlGaN have been investigated to solve this problem [8, 35-42]. These materials can provide high 2DEG density even with a smaller thickness due to the much higher polarization field compared with conventional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($x > 0.35$). Among them, $\text{In}_x\text{Al}_{1-x}\text{N}$ ($x = 0.17$) is especially attractive due to its unique properties.

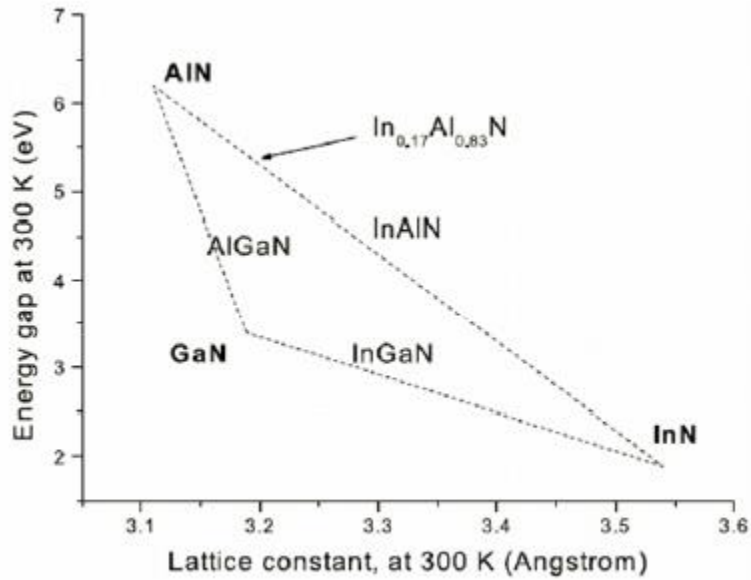


Fig.3.18 Energy gap and lattice constant for different III-Nitride alloy materials [40]

Energy gap and lattice constant of III-Nitride based materials are shown in Fig.3.18 [40]. It can be seen that $In_{0.17}Al_{0.83}N$ is lattice matched to GaN. Hence, by combining InAlN and GaN, one is able to eliminate the strain induced reliability issues in heterostructures with other material such as AlGaN and AlN as the top barrier. Moreover, thanks to the high energy gap difference and strong spontaneous polarization, although there is no piezoelectric polarization in InAlN/GaN heterostructure, it still provides a much higher charge density with a small thickness (less than 10 nm) compared with conventional AlGaN/GaN heterostructure as shown in Fig.3.19 [43]. In addition, the small thickness of top barrier and high 2DEG density are helpful for ohmic contact formation. Electron path through top barrier is easier to be formed and lower contact resistance can be achieved.

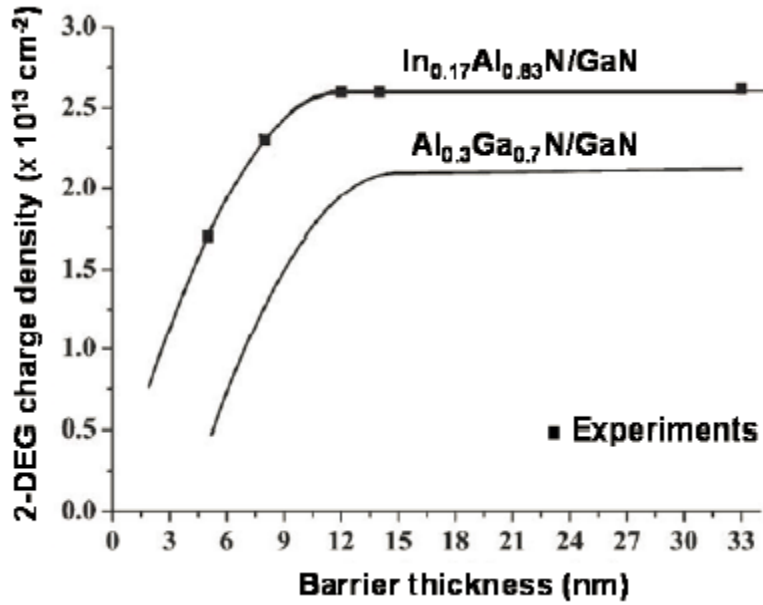


Fig.3.19 Simulated 2DEG density as function of barrier thickness for In_{0.17}Al_{0.83}N and Al_{0.3}Ga_{0.7}N [43]

Due to the advantages discussed above, In_{0.17}Al_{0.83}N/GaN attracts more and more attention for high frequency applications. Several promising results have been reported in [21, 22, 43-47].

3.4.2. Challenges for high performance GaN HEMTs on Si

As discussed in chapter 1, GaN HEMTs on Si substrate have attracted increasing interest in recent years, not only in power electronics applications but also in RF applications. However, the high frequency performance of GaN HEMTs on Si still lags behind their counterparts on SiC. Most of high frequency results, especially those above f_T of 200 GHz, were reported from devices grown on SiC substrates. The best reported

GaN HEMT on Si only exhibited a f_T of 176 GHz with for a gate length of 80 nm [18]. In contrast, the maximum f_T for GaN HEMTs on SiC has been pushed to 454 GHz [23].

This is mainly due to two reasons. Firstly, obtaining high quality GaN heterostructure on Si substrate is challenging. Large lattice mismatch (17%, versus 3.6% between GaN and SiC) and thermal expansion coefficient difference between GaN and Si (111) substrate lead to higher density of dislocations in the epitaxial GaN materials and wafer bowing [48, 49]. The low resistance Si substrate, nitride/Si interface and GaN buffer also bring significant RF loss for the devices [50].

To solve this problem, transition layers (TLs) have been used in wafer growth to release the stress between Si substrate and epitaxial GaN. Various types of TLs have been developed, such as $\text{Al}_x\text{Ga}_{1-x}\text{N}$ buffer layer with graded Al concentration [51], GaN/AlN super lattice structure [52], single $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with low Al mole fraction [53], AlN [54] or periodic SiN [55], etc.. With these improved growth techniques high quality GaN epitaxial layers on Si has been realized for the fabrication of AlGaN/GaN HEMTs with good high frequency performance.

Secondly, very limit study was reported regarding to GaN HEMTs on Si with deeply scaled gate and channel or InAlN as top barrier. Based on the analysis in the last two sections, device scaling together with the use of thin InAlN barrier are effective strategy to improve the high speed performance of GaN HEMTs by minimize both intrinsic and parasitic delay and improve gate modulation efficiency simultaneously. In this work, we demonstrated deeply-scaled GaN HEMTs on Si substrates with a thin 9 nm InAlN top

barrier and gates from 40 to 200 nm. The device with a 40 nm gate shows a record high f_T up to 250 GHz

3.5. Device fabrication

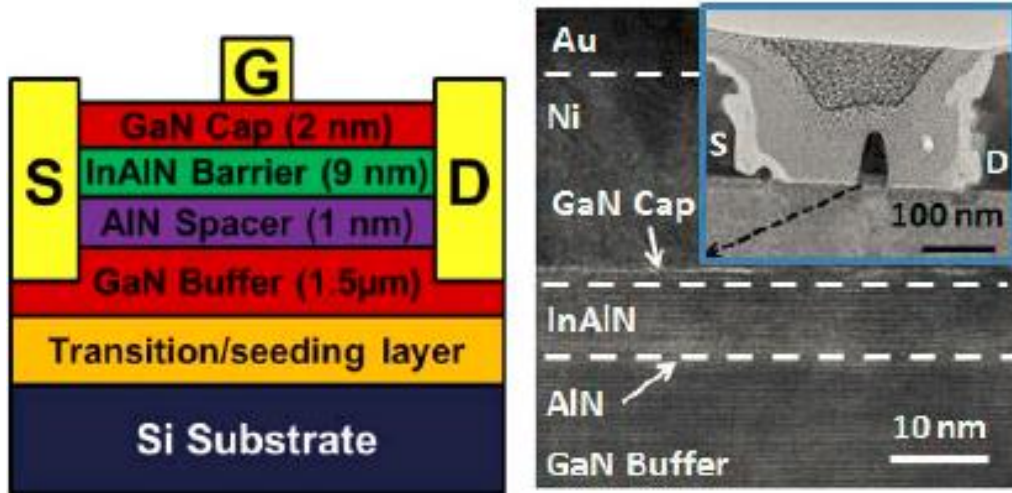


Fig.3.20 Schematic diagram and TEM image (gate region) of a 40-nm gate InAlN/GaN on Si

The transistors in this work have an InAlN/GaN heterostructure grown on a high-resistivity ($\geq 6000 \Omega \cdot \text{cm}$) Si (111) substrate by metalorganic chemical vapor deposition (MOCVD). The schematic diagram and TEM image (gate region) of the cross-section of the 40-nm gate device is shown in Fig.3.20. It consists of a 2 nm of GaN cap, a 9 nm unintentionally doped $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ barrier, a 1 nm of AlN spacer and a 1.5 μm unintentionally doped GaN buffer layer. As previously discussed, the lattice-matched InAlN barrier layer does not induce extra strain in the barrier layer, and the InAlN/GaN heterostructure can realize a high 2-dimensional electron gas (2DEG) density with a thin barrier thickness [43]. A thin barrier layer is required in a deeply-scaled transistor to reduce the gate-to-channel distance and thus suppress the short-channel effect [21]. The 1-nm AlN spacer layer in between the InAlN barrier and GaN channel screens the

scattering of the channel electrons from the barrier and thus improves the electron mobility. Hall measurement shows that the 2DEG mobility and density are $1190 \text{ cm}^2/\text{Vs}$ and $2.04 \times 10^{13} \text{ cm}^{-2}$, respectively.

The device fabrication started with mesa isolation using Cl_2/BCl_3 plasma dry etching. The mesa height is around 120 nm. Four layer metal stack consisting Ti/Al/Ni/Au with thickness of 20/120/40/50 nm were deposited and followed by rapid thermal annealing (RTA) at 725°C for 30 seconds in N_2 atmosphere to form the source and drain ohmic contact. Thanks to the high 2DEG density and thin barrier thickness, low sheet resistance (R_{sh}) of $270\Omega/\square$ and contact resistance (R_{C}) of $\sim 0.2 \Omega.\text{mm}$ have been measured using transmission line model (TLM) patterns. Submicron gates with foot print from 40 to 200 nm were defined by electron beam lithography (EBL) and followed by Ni/Au (30/70 nm) metallization. Interconnect and probe pads were formed by Ti/Au metallization. The surface of the device in this work was initially not passivated to avoid introducing extra gate fringing capacitance. The passivation effects will be studied later. The device with 40-nm gate has a source-to-drain distance (L_{sd}) of 300 nm while those devices with other gate lengths have L_{sd} of 700 nm. The gate width (W_{g}) is $2 \times 50 \mu\text{m}$ for all devices. DC characterization was carried out using an Agilent B1505 semiconductor device analyzer, and RF characterization was performed using an Agilent PNA N5244A network analyzer.

3.6. Device characterizations

3.6.1. DC and RF characterizations

The DC output and transfer characteristics of a device with $L_{\text{g}} = 40 \text{ nm}$ are shown in Fig. 3.21 (a) and (b) respectively. Benefiting from the thin InAlN barrier (9 nm) and

small (300 nm) source-drain space, a maximum drain current I_{dmax} of 2.6 A/mm is obtained at $V_g = 2$ V and $V_d = 6$ V with an on-resistance (R_{on}) of 1.3 Ω .mm. Based on the calculation by adding the source and drain contact resistances and the drain and sheet resistance of the access region, the R_{on} is found to be around 0.5 Ω .mm. However, the measured R_{on} was 1.3 Ω .mm instead. This discrepancy is believed to be due to the contact resistance between the probe and the metal pads. The R_c and R_{sh} were measured using 4-point TLM method; while for characterize of the fabricated devices, the output curve ($I_d V_d$) was measured using one probe for each terminal pad. We have observed an obvious difference between the measured resistance values between two metal pads on a mesa using two probes and four probes. Similar results have been observed in [22]. The peak transconductance g_m value of 426 mS/mm was measured at $V_g = -2.5$ V and $V_d = 6$ V. Compared with the device on SiC with similar L_g reported in [21], our 40-nm gate device exhibited a similar I_d , and slightly lower g_m (426 vs 520mS/mm). The lower g_m is related to the relatively lower mobility (1190 vs 1581 cm^2/Vs) and thicker barrier in our device (12 vs 9.4 nm). Benefiting from the scaled device geometry and the use of InAlN top barrier, our device has a more than two times higher current drivability and also higher g_m compared with the device on Si with highest f_T so far [18].

The gate leakage current I_g of a 40 nm gate device is shown in Fig.3.22. The high I_g is due to the thin InAlN barrier and the high peak electrical field in the deeply-scaled gate HEMT.

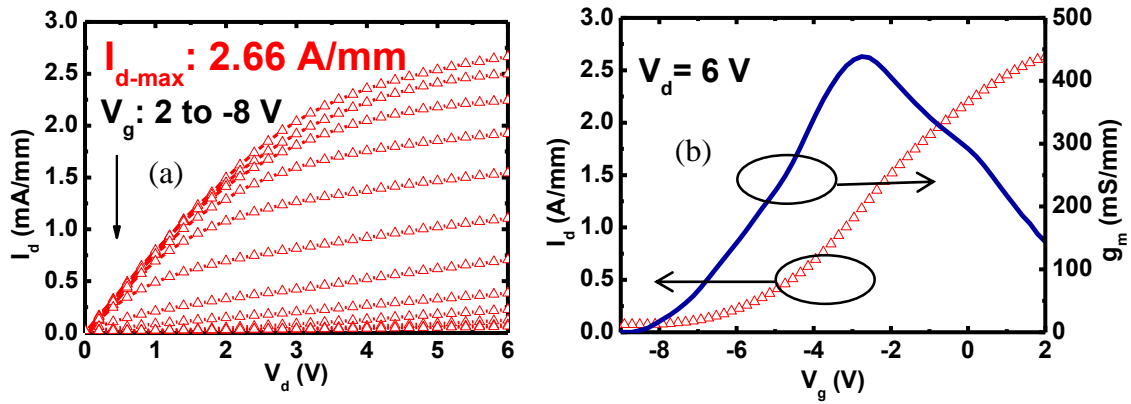


Fig. 3.21 (a) output and (b) transfer characteristics of an InAlN/GaN HEMT on Si with a 40-nm gate

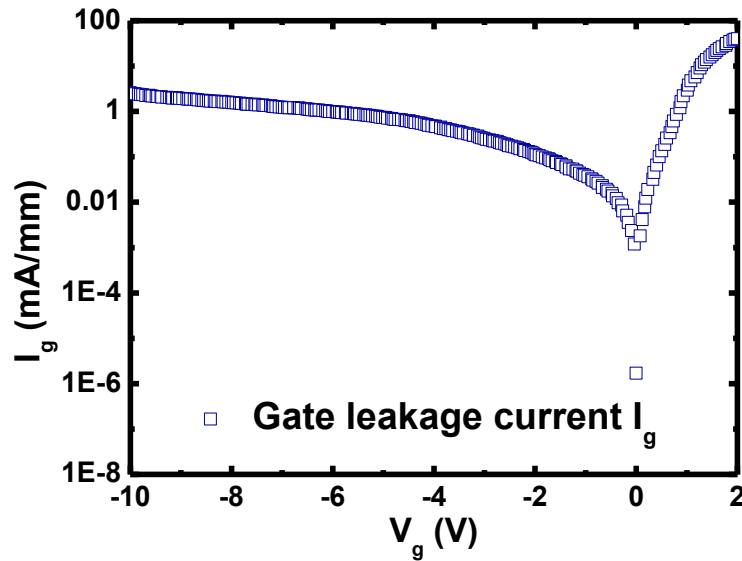


Fig. 3.22 Gate leakage current characteristic of an InAlN/GaN HEMT on Si with a 40-nm gate

The devices described in this chapter were aimed to achieve high operation frequency and were not optimized for high voltage application. The breakdown voltage defined by

$I_D = 1$ mA/mm at $V_g = -8$ V for the 40-nm gate device is only around 10 V. However, this leakage current is mainly due to the drain induced barrier lowering (DIBL) effect of the short gate device. The real hard breakdown (device burning) between gate and drain usually happens at $V_d > 20$ V. Compared with the devices reported on SiC substrate with similar dimensions, this result is slightly lower [21].

Drain-induced-barrier-lowering (DIBL) of the devices with different gate length were extracted at the condition of $I_d = 1$ mA, $V_d = 1$ and 6 V. The results are shown in Fig.3.23. Compared with conventional 40-nm gate AlGaIn/GaN HEMTs which has a DIBL value of around 600 mV/V [56], our 40-nm gate devices with thin InAlN barrier showed much lower DIBL of 410 mV/V and thus indicates better gate modulation efficiency.

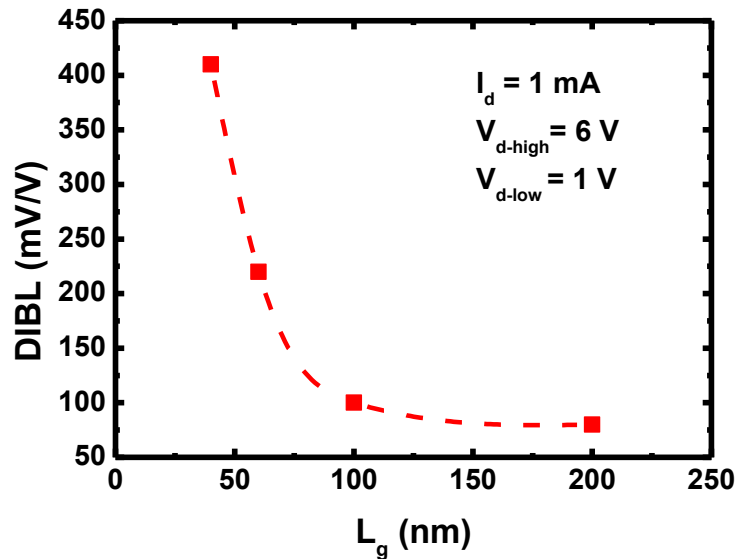


Fig. 3.23 DIBL of InAlN/GaN HEMTs with different gate length

For RF characterizations, current gain $|h_{21}|^2$ and unilateral gain G_u for a HEMT with 40-nm gate length as a function of frequency at $V_d = 6$ V and $V_g = -3.5$ V are plotted in Fig. 3.24 (a). On-wafer open structure was used to subtract the influence of the probe

pads [57]. A f_T of 250 GHz and a maximum oscillation frequency f_{max} of 60 GHz were obtained by extrapolating $|h_{21}|^2$ and G_u by -20 dB/Dec. To the best of our knowledge, this f_T value is the highest among the reported GaN-based transistors on Si substrates. A relatively low f_{max} is due to the high resistance of the short rectangular shape gate, which can be improved by using T-shape gate structure [23]. The f_T and f_{max} values of the 40-nm gate device were plotted in Fig. 3.24 (b) as a function of gate bias V_g .

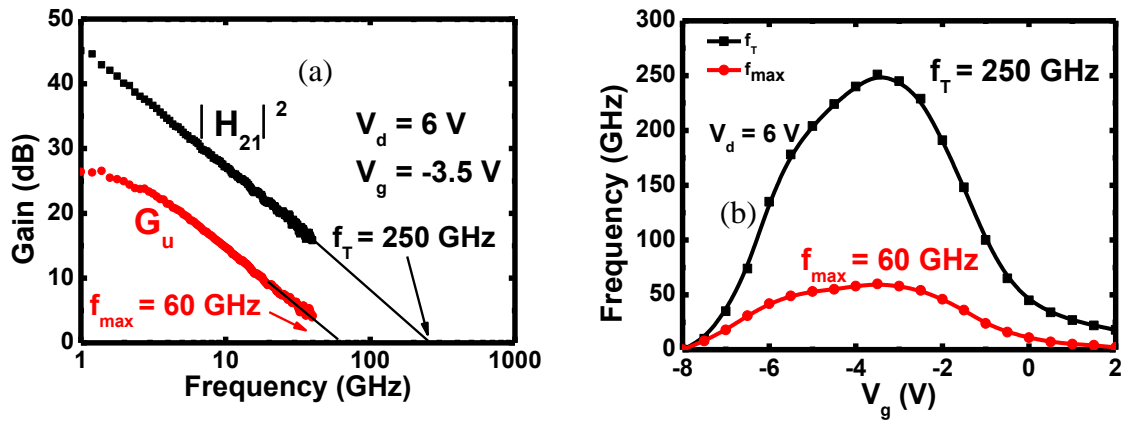


Fig. 3.24 (a) de-embedded RF small signal at $V_d= 6$ V and $V_g = - 3.5$ V and (b) de-embedded f_T and f_{max} as a function of V_g of 40-nm gate device

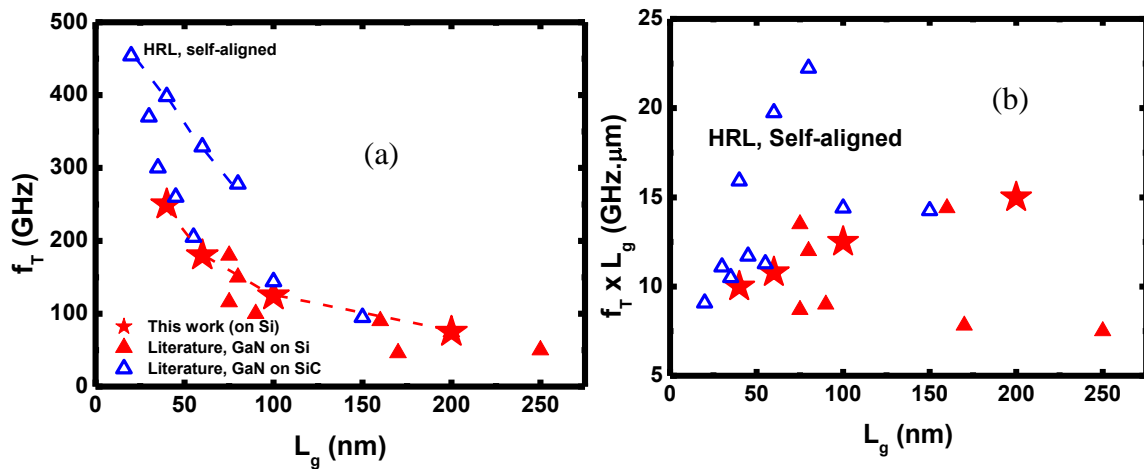


Fig. 3.25 (a) comparison of the cut-off frequencies (f_T) of GaN HEMTs on Si in this work with other reported GaN HEMTs on Si [13], [15], [18], [58-60] and GaN HEMTs on SiC [21-23], [43-47] and (b) shows the L_g dependence of $f_T \cdot L_g$ product

The state-of-the-art f_T values as a function of gate length that have been reported for the GaN transistors on Si and SiC substrates are summarized in Fig. 3.25. In this work, f_T values of 75, 125, 180 and 250 GHz were achieved for the devices with 200, 100, 60 and 40-nm gates, respectively. The best f_T of 454 GHz was reported by HRL [23] using AlN/GaN HEMTs on SiC with 20nm self-aligned gate (SAG). Except this reported work which uses more complicated process, our GaN HEMTs on Si showed comparable f_T with the GaN transistors on SiC in [21, 22]. These excellent results show the great potential of InAlN/GaN HEMTs on Si for future mm-wave and sub-THz applications. In addition, as shown in Fig. 3.24 (b), the $f_T \times L_g$ product decreases as the gate length scales down (15 GHz \cdot μm for $L_g = 200$ nm and 10 GHz $\cdot\mu\text{m}$ for $L_g = 40$ nm), especially when the gate length is shorter than 100 nm. This phenomenon is consistent with the fact that as the gate length scales down, the parasitic components play more important roles in the high-frequency performance [21].

3.6.2. Delay analysis and future optimization

The effective electron velocity v_{eff} was extracted using the delay analysis method described previously in this chapter.

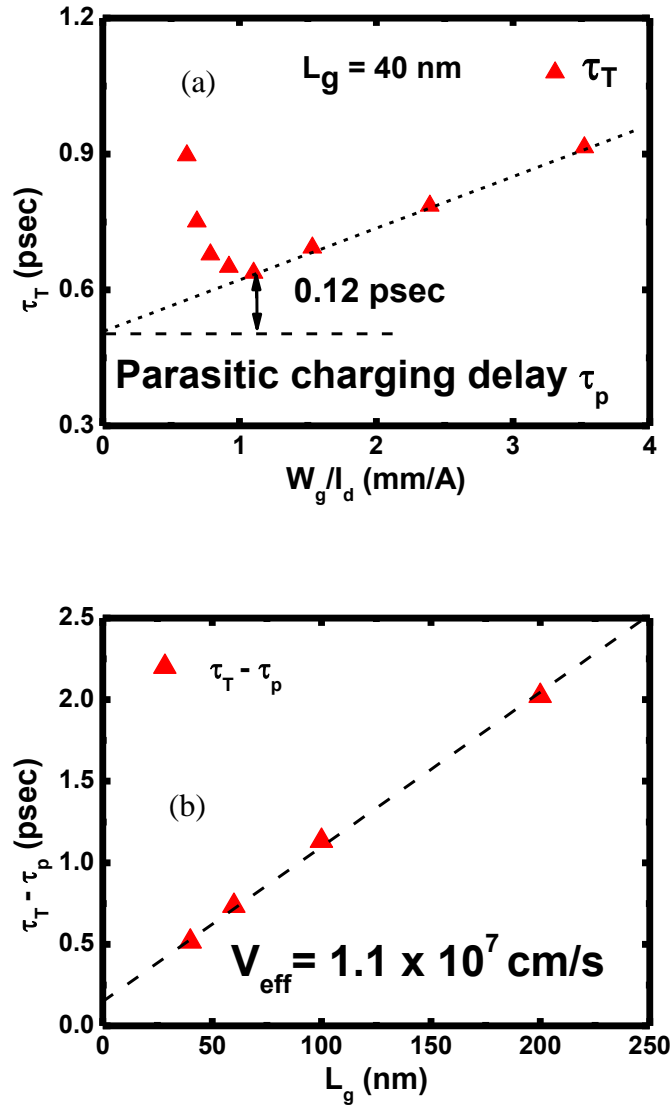


Fig. 3.26 (a) τ_T as a function of W_g/I_d for the device with 40 nm gate and (b) $\tau_T - \tau_p$ as a function of L_g

$\tau_T - \tau_p$ was first extracted by finding the intercept of the plot of τ_T as a function of W_g/I_d , as shown in Fig. 3.26 (a). $\tau_T - \tau_p$ for other devices with different gate length were extracted using the same method. Fig. 3.26 (b) plots the $\tau_T - \tau_p$ as a function of gate length L_g , and τ_{ext} can be extracted from the slope of the curve. Here we assume the extrinsic delays for all devices are the same. From definition, the extrinsic delay originates from

the extrinsic gate capacitance due to the coupling between the gate and 2DEG outside the intrinsic channel. It is more related to the gate shape (gate head length/ gate foot height of a T-gate), passivation thickness and material property (k value) and the heterostructure barrier thickness etc. Usually for those devices with different gate lengths and gate-to-source/drain distances, a constant extrinsic delay can be assumed [21]. As shown in Fig. 3.26 (b), the point of $(\tau_T - \tau_p)$ for the device with 300 nm channel length falls on the same line as other devices, so we believe that such an assumption is valid and so is the extraction. The delays for the 40-nm gate device are extracted to be $\tau_{int} = 0.37$ psec, $\tau_{ext} = 0.15$ psec and $\tau_p = 0.12$ psec, respectively, and the effective electron velocity v_{eff} of 1.1×10^7 cm/s was obtained from the slope of the curve in Fig. 3.27 (b) based on equation (3.21):

$$v_{eff} = \frac{L_g}{\tau_{int}} \quad (3.21)$$

This value of electron velocity is comparable to those reported in GaN HEMTs on SiC substrates [21, 22]. As the gate is deeply scaled down to 40 nm, the electron saturation velocity other than the mobility determines the intrinsic delay and thus the intrinsic f_T . For our devices, the parasitic charging delay only occupies 19% of the total delay. This is benefiting from the relatively higher 2DEG density (2.04 versus 1.65×10^{13} cm⁻² in [21]) and lower contact resistance (0.2 versus 0.3 $\Omega \cdot \text{mm}$ in [21]), Furthermore, the low charging delay is also due to our rectangular gate configuration which results in lower parasitic fringing capacitance as compared to a T-gate device.

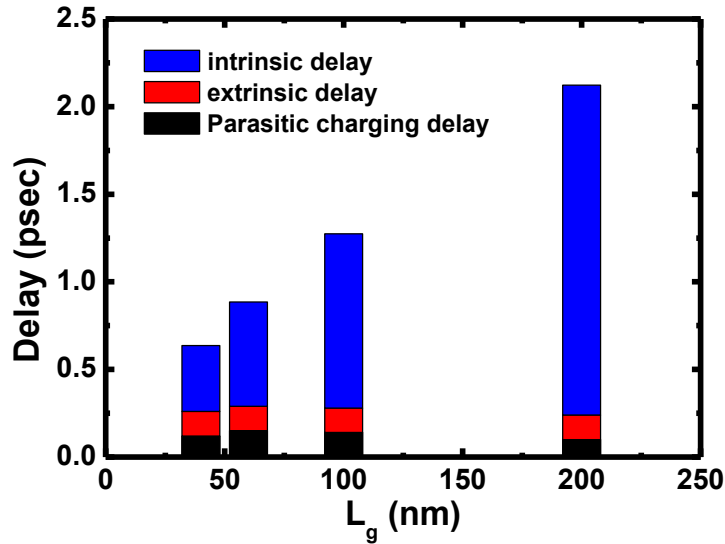


Fig. 3.27 Extracted delay components for the devices with different gate length in this work

Fig. 3.27 shows the extracted delay components for all devices. As shown in the figure, for the 200-nm gate device, intrinsic delay dominant in the total delay, suggesting that the speed is limited by intrinsic factor namely the gate length. As gate length scales down to 40 nm, the intrinsic component becomes about 50% of the total delay while the extrinsic limiting factors play more important roles. This result is consistent with the analysis in the beginning of this chapter and provides direction for further device optimization.

In conclusion, the achieved high frequency performance of our GaN HEMTs on Si is comparable with that on SiC. It is worth noting that only standard fabrication techniques for ohmic contact and gate formation were used in this work. With a shorter gate length and source-to-drain distance (the shortest L_g and L_{sd} reported for GaN HEMTs on SiC is 20 nm and 100 nm using a self-align approach [23]), and/or adoption of other advanced technologies such as regrown n^{++} GaN for ohmic contact, the high frequency performance of the GaN HEMTs on Si can be further improved and reaching closer to

those on SiC. For example, by further scaling down L_g to 20 nm and L_{SD} to 150 nm, and adopting regrown n^{++} GaN ohmic contact ($R_c \sim 0.1 \Omega \cdot \text{mm}$ [23]), the total delay τ_T of around 0.36 psec and a much higher f_T of 440 GHz is projected according to the delay analysis given above (see equation (3.3)), which is very close to the best value reported on SiC [23].

3.7. Passivation effects on deeply scaled InAlN/GaN

HEMTs

Besides the high frequency performance, large signal RF performance is another main concern for GaN HEMTs. However, generally high density surface states exist on GaN surface caused by dislocations, defects, dangling bonds and foreign contaminations. These surface states act as carrier traps, leading to serious current collapse and DC-to-RF dispersion. Although these effects have little impact on small signal high frequency performance, they ultimately limit the larger signal RF characterizations of GaN HEMTs. To solve this problem, Si_3N_4 and SiO_2 are usually used for passivation of the GaN HEMTs' surface to suppress surface trapping effects and thus improve the RF output power [63, 64]. However, for Si_3N_4 and SiO_2 , generally a relatively thick (> 100 nm) layer is needed to effectively passivate the device surface. As discussed previously in this chapter, the extrinsic delay is closely related to the gate fringing capacitance. A thick passivation layer will degrade the high frequency performance of GaN HEMTs, especially for the deeply scaled device because the extrinsic delay components play more important role in the total delay.

Materials with low permittivity such as Al_2O_3 and surface oxidation [21, 62] have been developed for better performance of GaN HEMTs for surface passivation. In this work, a 10 nm Al_2O_3 deposited by atomic layer deposition was applied for surface passivation. The passivation effects on DC, pulsed I-V and small signal RF characteristics of deeply scaled InAlN/GaN HEMTs are investigated in this section.

3.7.1. Al_2O_3 deposited by atomic layer deposition (ALD) as passivation layer.

In order to obtain optimal passivation effect, the quality of material is the key factor. Also, to avoid introducing too much gate fringing capacitance, the thickness of the passivation layer need to be well controlled. It should be thin enough to effectively passivate the device surface and at the same time not introducing excessive fringing capacitance. In this work, ALD is used because the thickness of the film can be deposited with atomic scale precision and with good quality.

ALD belongs to the same family of chemical vapor deposition (CVD) techniques. Different from other CVD method such as plasma enhanced CVD (PECVD) and low pressure CVD (LPCVD), the deposition process for ALD can be divided into two parts and the precursor materials are introduced separately into the reaction chamber. For this work, TMA (Tri-methyl aluminum) is first introduced into the chamber for 0.015 sec and react with Hydroxyl (OH) on the sample surface. Next, the reaction chamber is pumped to remove residual TMA. After that, the other precursor which is H_2O is introduced into the chamber for 0.015 sec and reacts with TMA on the sample surface to form a monolayer of Al_2O_3 . For the etch deposition cycle which consists of a pair of TMA and

H₂O gas pulse, exactly one monolayer of Al₂O₃ is formed [65]. Hence, the thickness of Al₂O₃ can be controlled precisely by the number of the total deposition cycles.

In this work, the heterostructure and fabrication process are the same with that in the last section except the final passivation step. Before ALD deposition, the sample was cleaned with solvents and acid to remove foreign contaminations. Then ALD deposition was performed at 250 °C for 84 cycles to obtain 10 nm thick Al₂O₃.

3.7.2. Passivation effect on device characteristics

The DC output and transfer characteristics of a 40-nm gate device before and after passivation are plotted in Fig. 3.28 (a) and (b), respectively. After passivation, the maximum drain current I_{d-max} at $V_g = 1$ V increased by 25.4 %, from 1.85 A/mm to 2.32 A/mm. The on-resistance, R_{on} decreased by 18% from 1.3 Ω .mm to 1.06 Ω .mm. g_m of the device also increased by 8.5% from 389 to 422 mS/mm. This is believed to be mainly due to the increased 2DEG density and electron mobility [63, 64, 66] and thereby lower sheet resistance. TLM measurement indicates that the sheet resistance R_{sh} decreased from 270 to 235 Ω/\square . On the other hand, the device after passivation showed degraded sub-threshold performance. DIBL of the 40-nm gate device increased from 420 to 650 mV/V after passivation. Before passivation, the surface states density in the access region is high. Under sub-threshold bias condition, due to the high electric field in the access region near the gate, electrons are trapped in these surface states and thereby deplete the 2DEG in the channel underneath. In this case, the effective gate length increased and thus resulting in lower DIBL. However, after passivation, the passivation layer suppresses the trapping effect in the access region to prevent the electrons to be trapped under high

electric field. Thus, higher DIBL was observed as the effective gate length was not increased. This phenomenon together with the increased 2DEG density after passivation, are believed to be the reasons of the slightly negative-shift of threshold voltage V_{th} observed after passivation as shown in Fig. 3.28 (b).

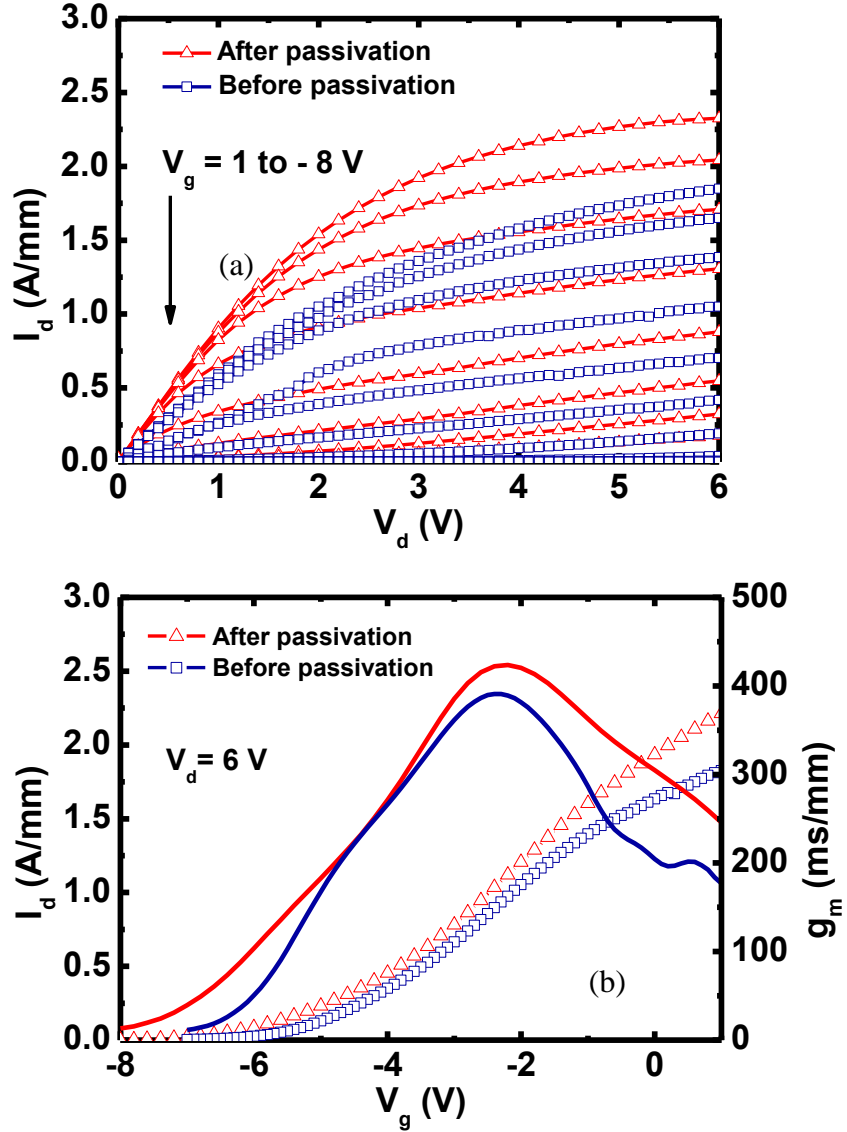


Fig. 3.28 (a) output and (b) transfer characteristics of a 40-nm gate device before and after 10 nm Al_2O_3 passivation

Pulsed-IV measurement with a pulse width of 200 ns was performed for the 40-nm gate device at quiescent biases ($V_{gq} = 0$ V, $V_{dq} = 0$ V), ($V_{gq} = -8$ V, $V_{dq} = 0$ V) and ($V_{gq} = -$

8 V, $V_{dq} = 6$ V). The measured drain currents at $V_g = 1$ V for each quiescent bias condition of the device before and after passivation are plotted in Fig. 3.29 (a) and (b), respectively.

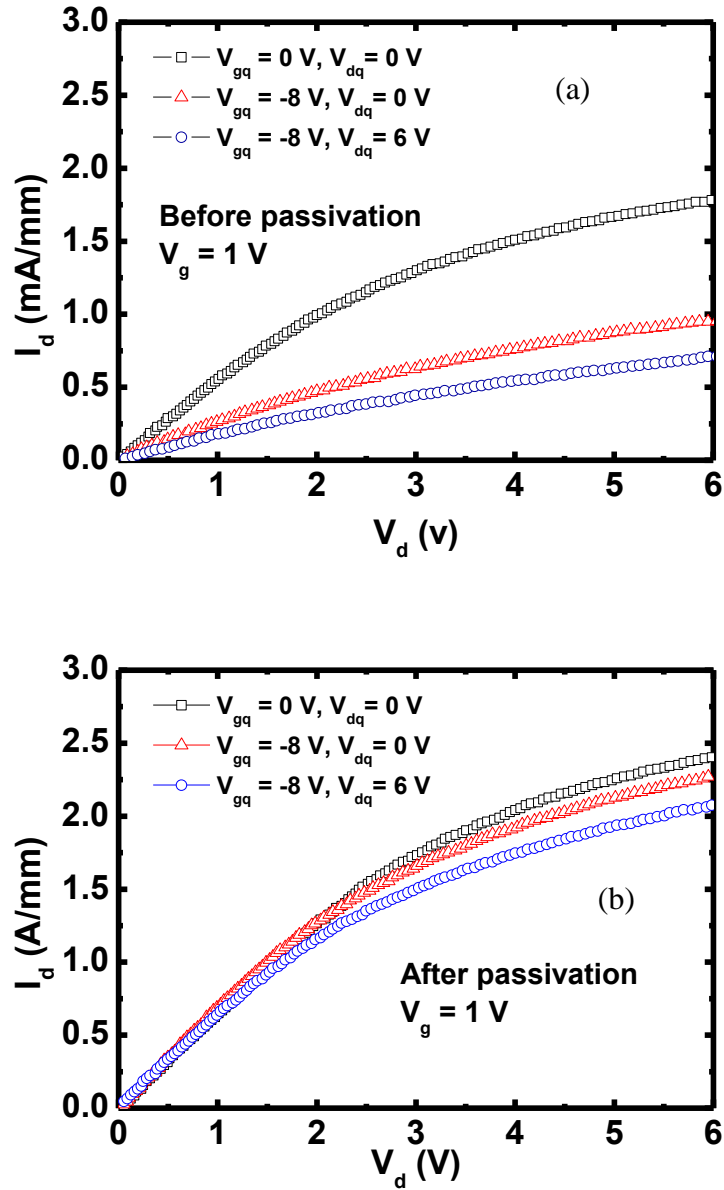


Fig. 3.29 Pulsed-IV measurement for the 40-nm gate device (a) before and (b) after passivation

The current collapse for each quiescent bias condition is calculated as follows.

$$\text{current collapse} = \frac{I_{d0} - I_{dq}}{I_{d0}} \times 100\% \quad (3.22)$$

where I_{d0} represents the drain current at quiescent bias ($V_{gq} = 0$ V, $V_{dq} = 0$ V) and I_{dq} is the drain current at other quiescent bias. Before passivation, the current collapse was 58% under quiescent biases ($V_{gq} = -8$ V, $V_{dq} = 6$ V), and 46% under quiescent biases ($V_{gq} = -8$ V, $V_{dq} = 0$ V), respectively. After passivation, due to the suppressed surface trapping effect, the current collapse decreased to 15% under quiescent biases ($V_{gq} = -8$ V, $V_{dq} = 6$ V), and 5% under quiescent biases ($V_{gq} = -8$ V, $V_{dq} = 0$ V), respectively. This excellent result indicates that the 10 nm Al_2O_3 passivation layer effectively improve the channel surface, the achieved low current collapse is important for stable large signal operation.

However, for high frequency performance, due to the introduction of addition gate fringing capacitance, the f_T values decreased slightly after passivation, especially for the device with shorter gate length. The comparison of the maximum f_T values of the device with gate length range from 40 to 200 nm is presented in Fig. 3.30. For the 40-nm gate device, the maximum f_T decreased from 250 to 235 GHz while that of the 200-nm gate device remained almost unchanged (75 to 74 GHz). The details of the reasons are discussed next.

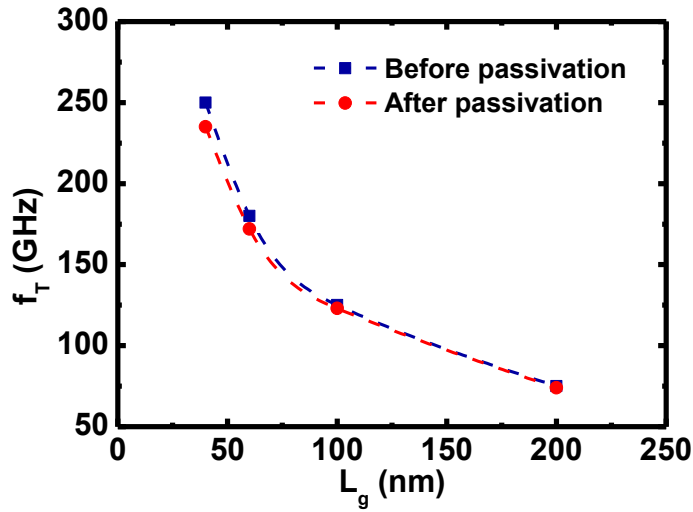
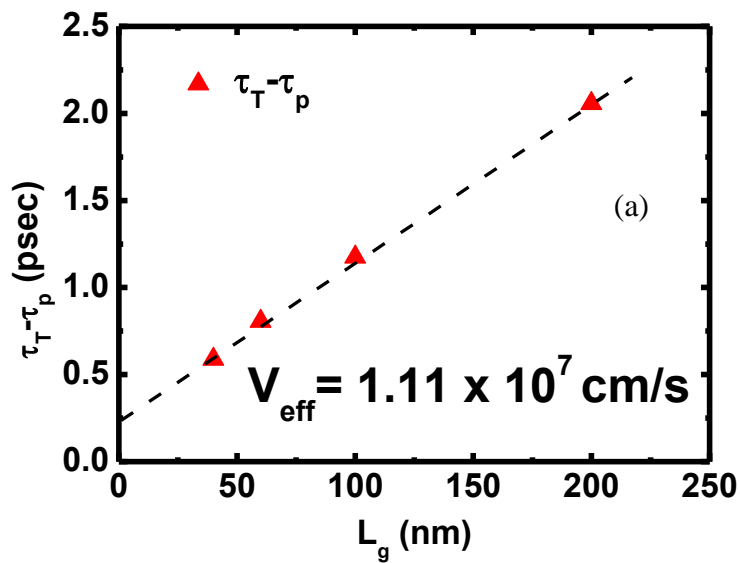


Fig. 3.30 Comparison of maximum f_T s before and after passivation

For a better understanding of the impact of passivation on the device operation speed, delay components extraction was performed for the devices using the same method described in the last section. Fig. 3.31 plots the effective electron velocity v_{eff} extraction and the extracted delay components after passivation.



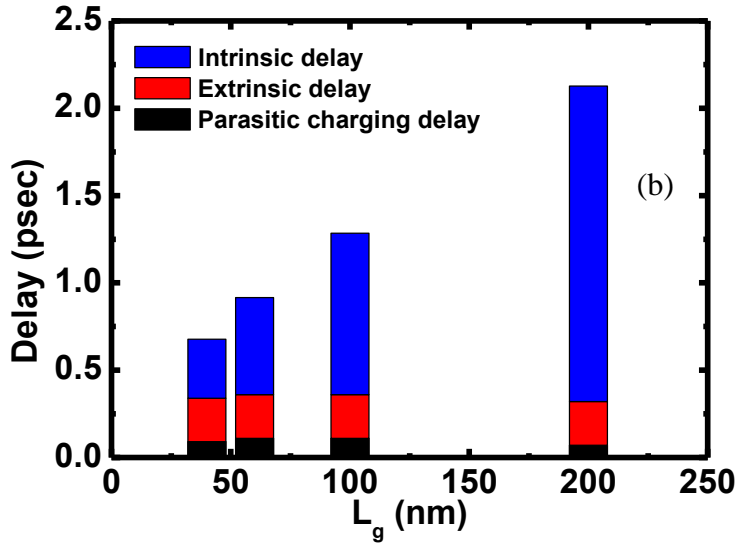


Fig. 3.31 (a) v_{eff} extraction and (b) the extracted delay components after passivation

As shown in the figure, the extracted v_{eff} of 1.11×10^7 cm/s is almost the same as the value before passivation (1.1×10^7 cm/s). Taking the device with 40-nm gate as an example, the extracted intrinsic delay slightly decreased from 0.377 to 0.338 psec, and the parasitic charging delay decreased from 0.12 to 0.09 psec after passivation. This result is consistent with increased maximum drain current and transconductance after passivation due to the increased 2DEG density and electron mobility. However, for the extrinsic delay which is associated with the extrinsic capacitance, it increased from 0.14 to 0.25 psec after passivation due to the introducing of addition gate fringing capacitance. Affected by intrinsic and extrinsic factors together, the total delay of the device increased by 6% and thus a lower f_T was obtained after passivation. For the device with 200-nm gate, the degradation in maximum f_T of 200-nm gate device is negligible. This is because though the extrinsic delay also increased by 0.11 psec, the intrinsic delay of 1.812 psec is the dominant delay in the total delay.

To avoid f_T degradation for deeply scaled device, thin thickness native oxidation [56] or low-k material can be applied as passivation layer. By suppress the increase in gate fringing capacitance, it is possible to realize a higher f_T or similar to the un-passivated value by using low k dielectric as passivation material in the future.

3.8. Conclusion

In this chapter, the limitation of GaN HEMTs speed has been studied through both experiment and analysis of the device physics. The intrinsic and extrinsic limiting factors in the device performance have been systematically investigated.

It has been clarified that the fundamental strategy to overcome intrinsic limitation of GaN HEMT device is to scale down the gate and maintain good gate modulation efficiency. For the extrinsic delay, sheet resistance of heterostructure and ohmic contact resistance between ohmic metal and 2DEG are two of the most concerned factors. Extrinsic delay is closely related to device design including gate geometry and heterostructure properties. Passivation also has influence on extrinsic delay through introducing gate fringing capacitance.

Based on the theoretical analysis, a deeply scaled GaN HEMT structure with thin InAlN lattice matched top barrier on Si substrate has been used to improve the high frequency performance. The combination of deeply scaled gate and channel help to decrease both intrinsic and parasitic charging delay through lowering intrinsic gate capacitance and access resistance. The use of thin InAlN top barrier instead of conventional AlGaIn not only resulted in improved gate modulation efficiency, lower ohmic contact resistance and higher current drivability, but also has the potential for

highly reliable application of GaN HEMTs due to absence of strain between InAlN and GaN interface. The use of Si substrate is preferred for commercialization of the devices due to low cost.

Electron beam lithography (EBL) technology was introduced. Sub-100 nm gate and sub-micron channel have been developed based on the EBL system. Maximum f_T of 250 GHz was successfully obtained in a 40-nm gate device which is the highest among any reported GaN HEMTs on Si substrate to-date. The achieved f_T performance of our device is comparable with that on SiC with similar geometry, which indicates the great potential of GaN HEMTs on Si for high frequency and low cost application. 10 nm Al_2O_3 as surface passivation was performed. The effects on DC and RF performance were also investigated. Current collapse was greatly suppressed but slight speed degradation was observed. With further optimization, such as even shorter gate and channel length, n^{++} regrowth ohmic contact and novel passivation technologies, better high speed performance in GaN HEMTs can be expected.

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Chapter 4 Planar Nanostrip-Channel InAlN/GaN HEMTs on Si with Improved g_m and f_T Linearity

4.1. Introduction

Beside high operation frequency discussed in the previous chapter, linearity performance also needs special attention in the GaN HEMT devices. The next generation communication systems will widely adopt the techniques of CA (carrier and MIMO (multiple input multiple output)), and these techniques will greatly increase the risks of signal intermodulation and communication channel interference. As a result, high linearity amplifiers and switches are needed in these systems. However, the linearity of GaN transistors ultimately limits the power density and efficiency of these devices in many applications, as the operating point of the device typically needs to be backed-off to meet the linearity specifications. In fact, as the operating frequency increases into the mm-wave range by shrinking the gate length, the linearity is expected to degrade even further [1, 2]. Circuit designers are putting efforts to add more functional sub-circuits such as DPD (Digital Pre-Distortion) to solve the linearity issue. However, this will definitely increase the system complexity, chip size, and design cost, and degrades the system robustness. High linearity performance at the transistor level is therefore crucial. In this chapter, the origins of the non-linearity in g_m and f_T for a GaN HEMT are investigated. Through this analysis, a novel planar nanostrip-channel InAlN/GaN HEMT on Si with improved g_m and f_T linearity is successfully demonstrated.

4.2. Non-linear g_m and f_T in GaN HEMTs at high gate bias

High linearity requires the device to have a constant transconductance (g_m) over a large gate bias range. Theoretically, in an ideal transistor, the g_m increases with the gate bias until it reaches its saturation point and then remains almost flat with the further increase of the gate bias (or drain current) [3]. This trend can also be applied to the current cut-off frequency (f_T). However, it is shown that the real conventional GaN HEMTs have a nonlinear extrinsic transconductance behavior. Fig. 4.1 shows two typical curves of g_m - I_{ds} and f_T - I_{ds} in GaN HEMTs, respectively. Fig.4.1 (a) indicates that after reaching its maximum value, g_m decreases significantly with the increasing drain current. As shown in Fig. 4.1 (b), the reduction of f_T can be as much as 30% after the peak point [1].

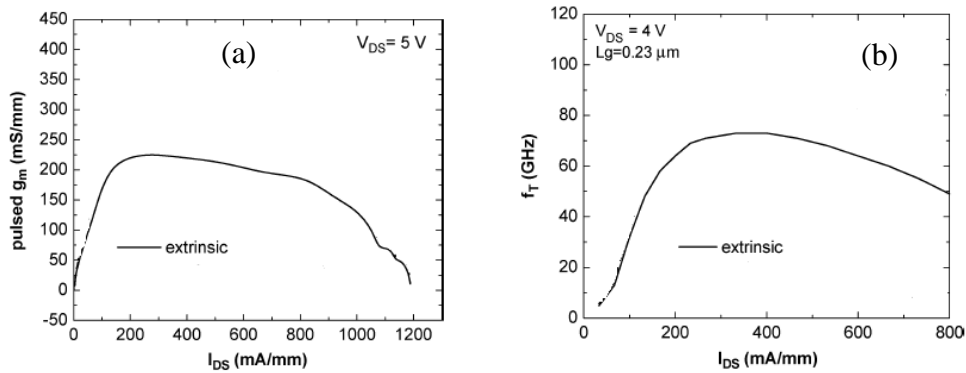


Fig.4.1 (a) g_m and (b) f_T decrease significantly with the increasing drain current

4.2.1. Origins of the non-linear performance

Till now, several explanations have been put forward to explain the non-linear g_m behavior at high gate bias (or drain voltage). J. Liu et al. claimed that alloy and interface scattering of 2DEG is the main reason of nonlinear effect [4], [5]. In this theory, the vertical electric field in the channel increases significantly as the gate bias increases. The electrons will move to the surface of the material, resulting in the increased scattering effect, which reduces the electron mobility and the current. Actually, this explanation came from Si MOSFETs and it has been proven that surface scattering effect is the main reason for the nonlinear effect in Si MOSFETs [6]. However, as the quality of the interface of GaN HEMT structures are generally high benefiting from the in-situ growth, it is doubtful whether this explanation is applicable to GaN HEMTs. Moreover, the nonlinearity was also observed in GaN HEMTs grown by MBE which has an even sharper interface compared with that grown by MOCVD [7-10].

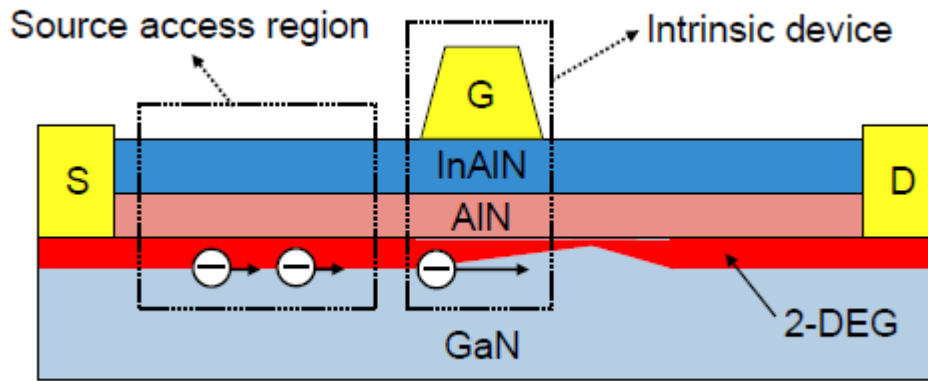
Another explanation claims that the self-heating effect is the main origin of the nonlinear behavior [11]. As the drain current increases, the power dissipation becomes higher and the channel temperature increases significantly. Therefore, the mobility and velocity of the electrons will decrease and lead to g_m and f_T drop. However, the self-heating effect cannot explain all the nonlinear effects in GaN HEMTs [8], [12-14].

T. Palacios et. al. have shown that the increase of access resistance plays an important role in the non-linear g_m and f_T of a GaN HEMT at high gate bias. The simulation results and experimental results of self-aligned GaN HEMTs indicate that the nonlinear effect can be suppressed by removing the impact of the increase of access resistance [1].

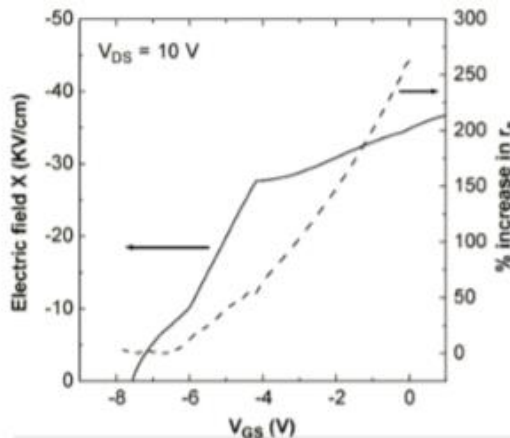
The cross section of a conventional non-self-aligned GaN HEMT at saturation regime is shown in Fig. 4-2 (a). The maximum current drivability of the intrinsic GaN HEMT device under high gate bias can be expressed by the following equation:

$$I_{d,max,int} = q \cdot n_s \cdot v_{sat} = 4 \sim 6 \text{ A/mm} \quad (4.1)$$

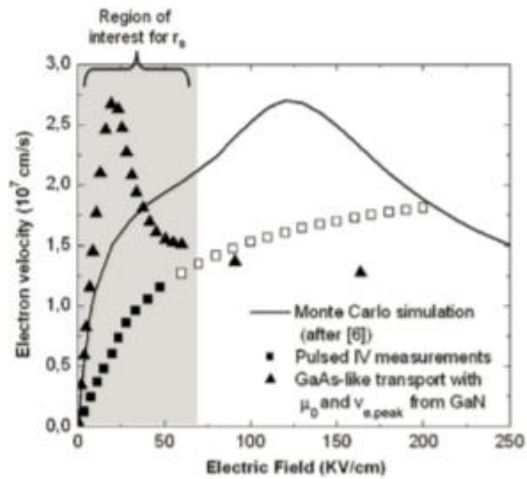
where q is electron charge, n_s is the density of 2-DEG and v_{sat} is electron saturation velocity.



(a)



(b)



(c)

Figure 4.2 (a) Cross-section of the conventional GaN HEMT under saturation [2], (b) simulation of the increases in longitudinal electric field and source access resistance increase [1] and (c) electric field dependence of electron velocity for different model [1]

For the intrinsic device under the gate electrode, the electric field is high enough for the electron velocity to reach its saturation value. However, it is not the same situation for the access regions because the electric field in these regions is not high enough and limits the electron to be in the “quasi-saturation” regime ($10 \text{ kV/cm} < E \ll 100 \text{ kV/cm}$) as shown in Fig. 4.2 (c) [1]. Thus, the current drivability of the extrinsic device is limited. It is shown in Fig. 4.2 (c) that for other material like GaAs, as the quasi-saturation occurs under much lower electric field than GaN, it is difficult to be distinguished from the standard saturation [1]. In GaN HEMTs, with the increasing drain current, the current drivability of the access region is limited by the velocity limitation in “quasi-saturation” regime. What’s more, for a deep sub-micron device under saturation operation, the potential of the drain side of the channel almost remains unchanged and most of the additional drain bias drops in the drain access region rather than source region. Moreover, when the gate-to-drain distance is designed to be small for high frequency applications, the whole drain access region will be depleted at saturation operation points. The electric field in the source access region is hard to be increased as the source is unbiased. Therefore, the nonlinear behavior of GaN HEMTs at high gate bias is due to the limited current drivability of source access region. Thus, to increase the linearity performance of GaN HEMT, the key method is to increase the current supply from the source access region. To achieve this, we can either increase the electron velocity in the source access

region or, increase the number of electrons in the source access region compared with channel region [2].

4.2.2. Current status of high linearity GaN HEMTs

4.2.2.1. Self-aligned GaN HEMTs

Self-aligned GaN HEMT is the most direct way to realize the device performance close to the intrinsic GaN HEMT. Since the ideal self-aligned HEMT doesn't have large access region, the impact of access resistance is negligible [15].

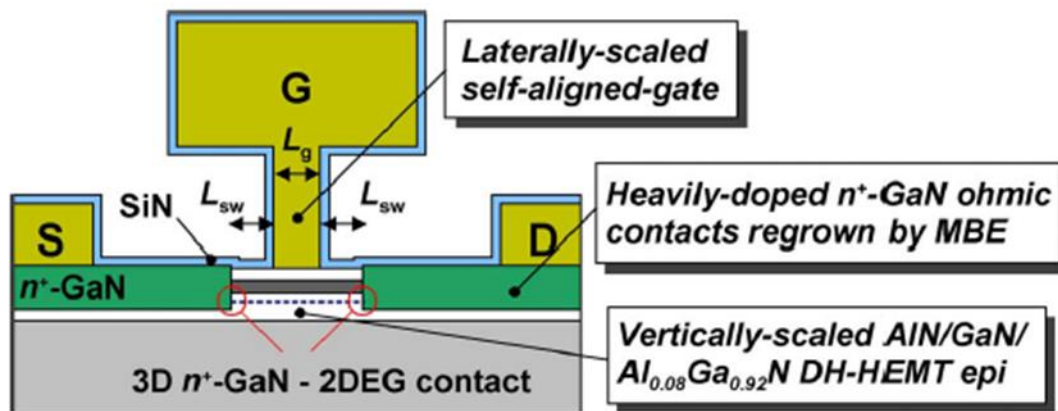


Fig. 4.3 Device structure of a self-aligned GaN HEMT [15]

Shinohara et al. demonstrated a self-aligned GaN HEMT in 2012 as shown in Fig.4.3. The fabricated device has very small access regions and Fig.4.4 shows that the self-aligned HEMT is able to maintain flat g_m and f_T even at high gate bias. This work indicates that GaN HEMTs have the potential to operate at large drain current level (3~4 A/mm) with high speed. However, since the access region of self-aligned HEMT is very small, poor breakdown characteristic has been observed in the reported device, thus limits

the application of the device. The access region between gate and drain is needed to support high breakdown voltage operation [15].

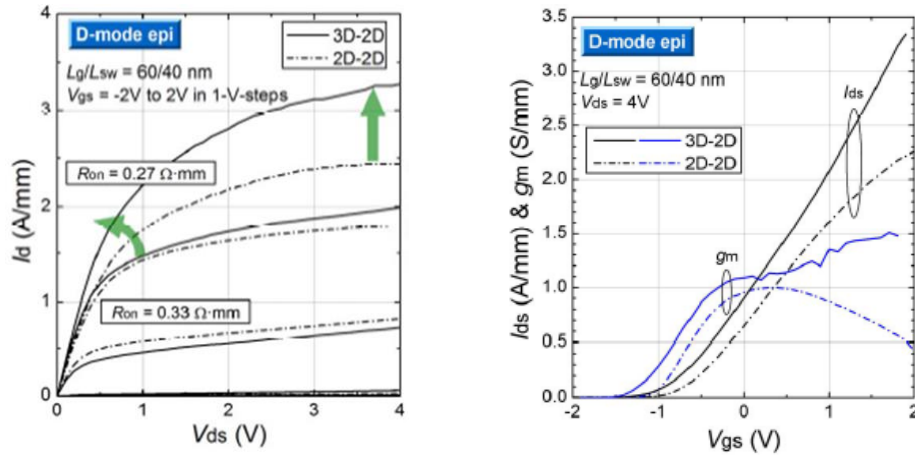


Fig. 4.4 DC characteristics of the Self-aligned GaN HEMT [15]

4.2.2.2. Fin-like nanowire GaN HEMTs

In 2013, D.S. Lee reported a nanowire channel GaN HEMT with improved linearity.

The device structure is shown in Fig.4.5 [2].

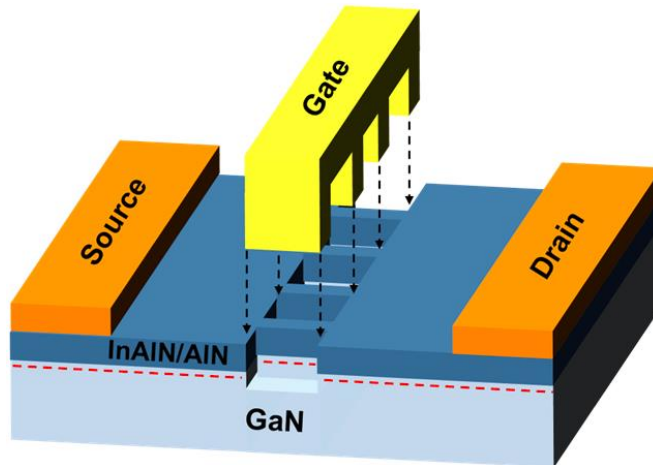


Fig. 4.5 Device structure of etched nanowire channel GaN HEMT [2]

As shown in Fig. 4.5, the InAlN barrier and GaN buffer under the gate are partially etched and nanowire channels are formed. As the effective channel width is reduced and the source access region remains planar, the current drivability of source access region is improved. The effect of access resistance increase at high drain current can be suppressed even at high drain current level. The device has much improved linearity performance as shown in Fig. 4.6 [2].

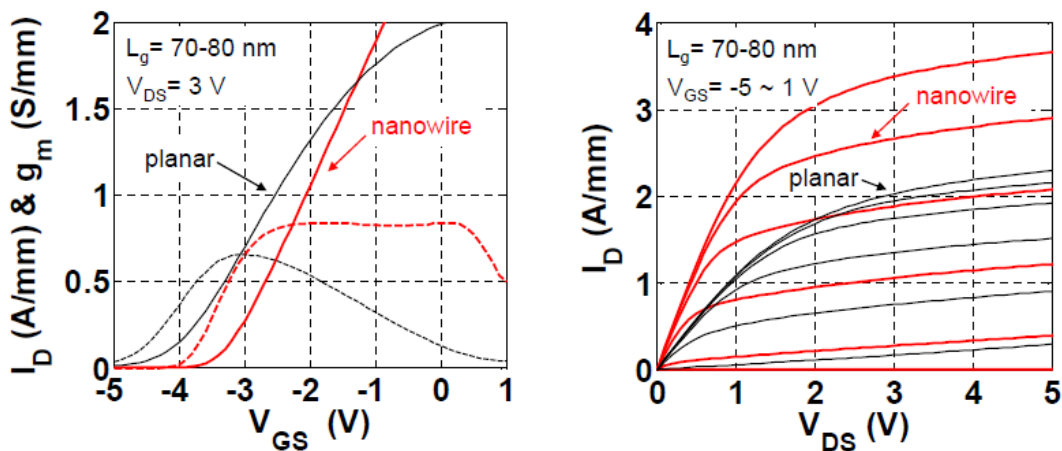


Fig.4.6 Transfer and output characteristic of the reported nanowire channel GaN HEMTs [2]

However, because the channel region is partially etched and the metal gate is surrounding the channel, larger fringing capacitance is introduced to the device. There are two major sources of the additional fringing gate capacitance, one is the capacitance between the gate metal and 2DEG, the other is induced by the electric coupling between gate metal and additional access region which is shown in Fig. 4.7 which leads to an obvious f_T drop [2]. Furthermore, the plasma etch introduces damages to the etched surface and nanowire sidewall.

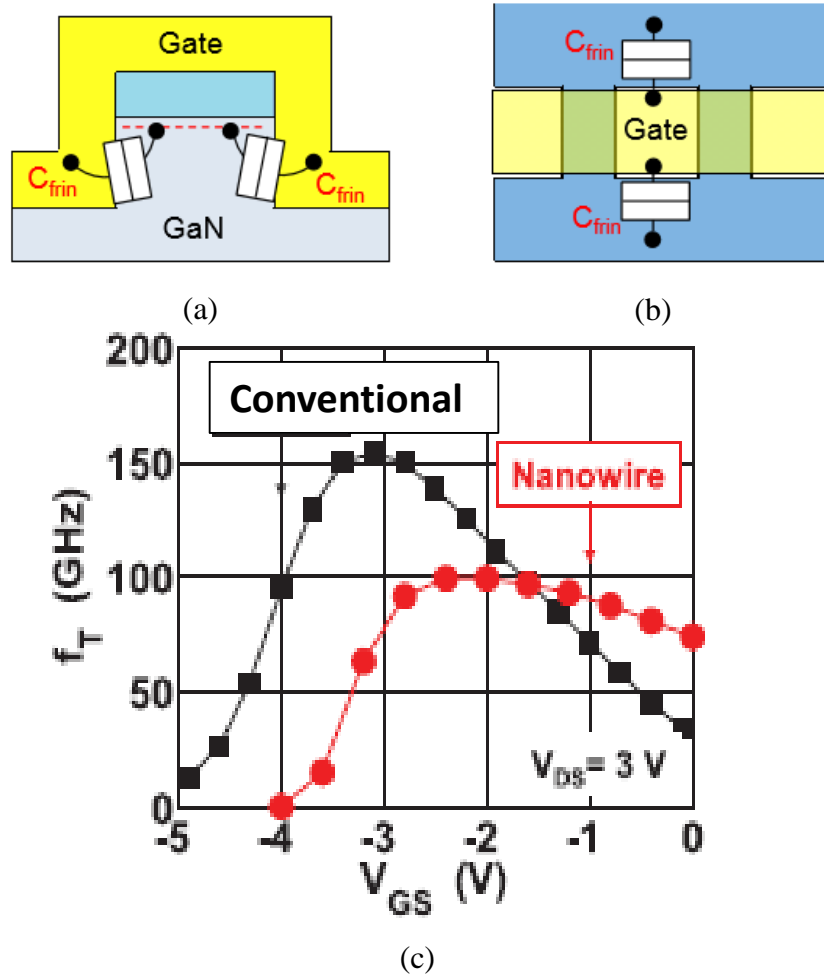


Fig. 4.7 Fringing capacitance between (a) gate and 2DEG, (b) gate and additional access region and (c) degraded f_T performance [2]

4.3. Planar nanostrip-channel InAlN/GaN HEMTs

To solve the issues discussed above, in this work, we propose a novel planar nanostrip channel to improve the GaN HEMT's linearity while at the same time reducing the extra parasitic capacitance thus avoid RF performance degradation.

4.3.1. Importance of gate fringing capacitance

As discussed in the last chapter, extrinsic delay is an important limiting factor of GaN HEMTs for high frequency applications and it is closely related with gate fringing capacitance. Simulation was first carried out using the Silvaco TCAD tool to verify the concept of the planar nanostrip channel structure. Fig. 4.8 shows the comparison of the simulated results of gate capacitance (C_g) versus gate voltage (V_g) for three different device structures namely, a conventional HEMT, a fin-like nanowire channel HEMT, and a planar nanostrip channel HEMT. The HEMTs in the simulation have an $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ heterostructure with barrier thickness of 10 nm. The width and height of the fin-like nanowire and the width of the planar nanostrip were all 100 nm. As seen from Fig. 4.8, compared with the fin-like nanowire channel device, the planar nanostrip-channel device has less parasitic gate capacitance with increasing $V_g - V_{th}$ (threshold voltage) benefiting from the absence of the sidewalls covered by the gate metal. This result indicates that the Planar nanostrip-channel structure has the potential to achieve better high frequency performance than Fin-like nanowire-channel device [16].

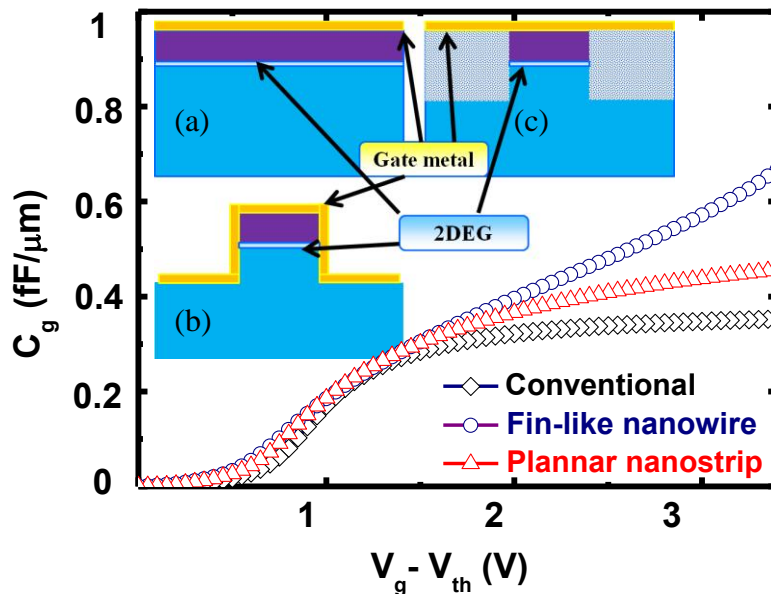


Fig. 4.8 Simulated gate capacitance versus gate voltage of the conventional, planar nanostrip-channel and fin-like nanowire-channel GaN HEMTs. Inset: cross-section of the gate stack in (a) conventional HEMT (b) fin-like nanowire HEMT and (c) planar nanostrip HEMT

4.3.2. Novel device fabrication techniques

The basic fabrication process of the planar nanostrip-channel GaN HEMT was similar to conventional device. The main challenges involved are to achieve damage free planar isolation and nanostrip formation with high accuracy.

4.3.2.1. As⁺ implantation for isolation

To partially isolate the channel region under the gate and remain a planar surface at the same time, ion implantation is the ideal technology for this application. Ion implantation is well studied for mesa isolation in GaN HEMTs [17]. Light ions such as Argon and Helium are usually used for mesa isolation. In this project, since the hard mask designed to be used for channel isolation process are PMMA (400 nm), HSQ (150 nm) and SiO₂ (100 nm) with a thin thickness, a heavy ion is preferred because its penetration depth is shallower than the light ions under the same energy. Based on our cleanroom facility (Varian EHP 200 implanter), Arsenic was chosen for the implantation ion. Two implantation conditions have been tried. In the first experiment, ion energy of 50 keV and dosage of $2 \times 10^{15} \text{ cm}^{-2}$ were used while in the second experiment, ion energy of 30 Kev and dosage of $3 \times 10^{15} \text{ cm}^{-2}$ was used. The sample was tilted at 7° during ion implantation. Hall measurement is the most straightforward method to evaluate the implantation effect by giving the electron density and mobility of a sample. However, the ohmic contact

between metal and 2DEG after implantation is very difficult to be formed due to the very low electron density thus making Hall measurement impractical. In this case, the implantation effect was evaluated by measuring the current in a test structure with an electrode gap of 6 μm and width of 100 μm under 5 V. Bare samples, samples covered by 400 nm PMMA, 150 nm HSQ and 100 nm SiO_2 were compared in this experiment. The measured results before and after implantation are shown in table 4.1 (a) and (b).

Table 4.1 (a) measured current in the test structure under 5 V before and after ion implantation with ion energy of 50 keV and dosage of $2 \times 10^{15} \text{ cm}^{-2}$ and (b) 40 KeV and dosage of $3 \times 10^{15} \text{ cm}^{-2}$

50 KeV, $2 \times 10^{15} \text{ cm}^{-2}$	Bare Sample			HSQ 150 nm			PMMA 400 nm			SiO ₂ 100 nm		
I_{before} (mA)	70	68	69	51	47	45	62	65	66	65	65	67
I_{after} (mA)	0.38	0.42	0.42	37	32	31	52	59	57	51	52	53

(a)

40KeV, $3 \times 10^{15} \text{ cm}^{-2}$	Bare Sample			HSQ 150 nm			PMMA 400 nm			SiO ₂ 100 nm		
I_{before} (mA)	55	51	61	81	74	72	95	92	92	93	93	94
I_{after} (mA)	0.36	0.29	0.33	79	75	71	93	97	99	92	95	95

(b)

The results shown in the tables indicate that both the implantation conditions offer good isolation effect as the current decreased by more than one order of magnitude after ion implantation. But at 50 KeV, the samples protected by hard masks are also affected

by the implantation and a current drop can be observed. In this case, the second implantation of ion energy of 40 keV and dosage of $3 \times 10^{15} \text{ cm}^{-2}$ is found to be able to fully satisfy the isolation requirement.

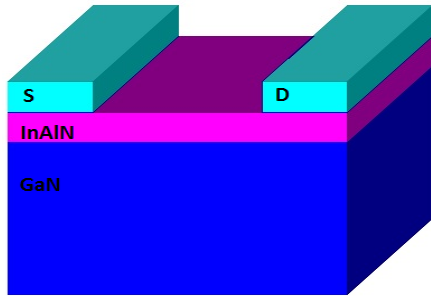
4.3.2.2. Nanostrip-channel formation

Taking the advantage of the high resolution EBL system discussed in the last chapter, patterns in nanoscale can be obtained. However, to form the Planar nanostrip-channel structure is not as simple as just obtaining a small feature size on resist stack. The following process such as dry etching and ion implantation need to be taken into consideration.

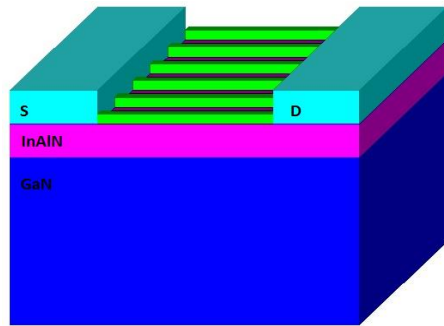
Planar nanostrip-channel formation was firstly designed to use a HSQ-PMMA self-aligned approach. However, this approach encountered gate shape and implantation damage issues. To solve this problem, a SiO_2 -PMMA approach was designed and has demonstrated excellent result.

4.3.2.2.1. HSQ-PMMA self-aligned approach

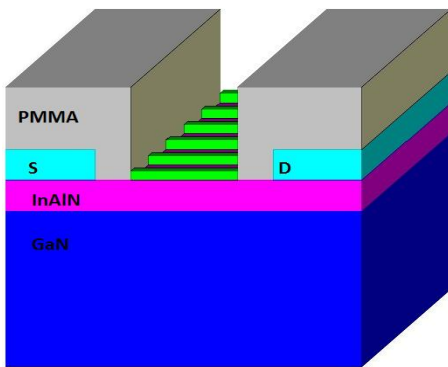
A self-aligned process was firstly designed. The fabrication process of nanowire channel GaN HEMTs is similar to the conventional ones, except that after the mesa isolation and ohmic contact formation, the nanostrip channels were realized by Hydrogen silsesquioxane (HSQ) patterning and ion implantation before the gate patterning and metallization. The process flow to fabricate nanowire channels is shown in Fig. 4.9.



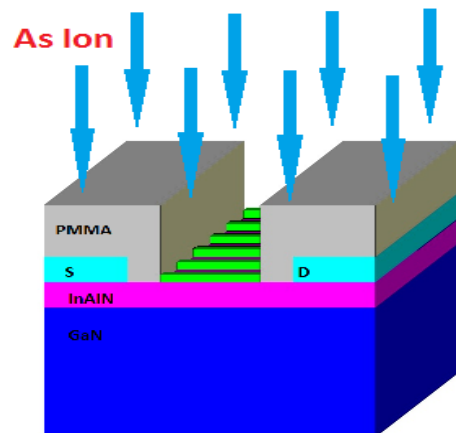
- Start from ohmic contact formation.



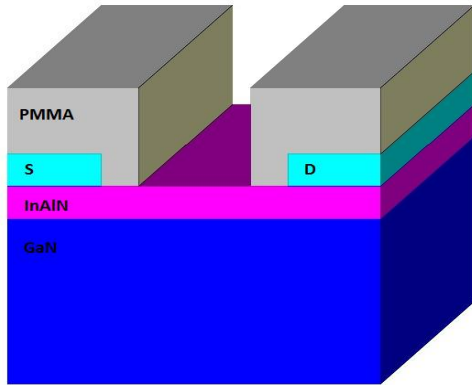
- HSQ nanostrip formation by EBL



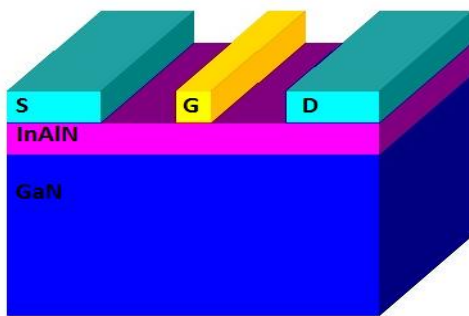
- Define gate with PMMA by EBL.



- Arsenic ion implantation to partially isolate the channel.



- Remove HSQ nanostrip by BOE.



- Gate metallization and lift-off.

Fig. 4.9 Process flow of HSQ-PMMA self-aligned approach

The designed fabrication process started with normal mesa isolation and ohmic contact formation using Ti/Al/Ni/Au annealed at 725 °C. HSQ nanostrip masks with line-to-space ratio of 90:110 nm was formed by EBL. A standard HSQ process was applied. The sample was spin coated with 6% HSQ at 1200 rpm for 70s followed by hot plate bake at 250 °C for 2 minutes. The measured thickness of HSQ layer was 150 nm. $500\mu\text{C}/\text{cm}^2$ was used for exposure. After exposure, sample was developed in MF-322 for 100 seconds. An SEM image of 100 nm lines with 1:1 line and spacing ratio is shown in Fig. 4.10.

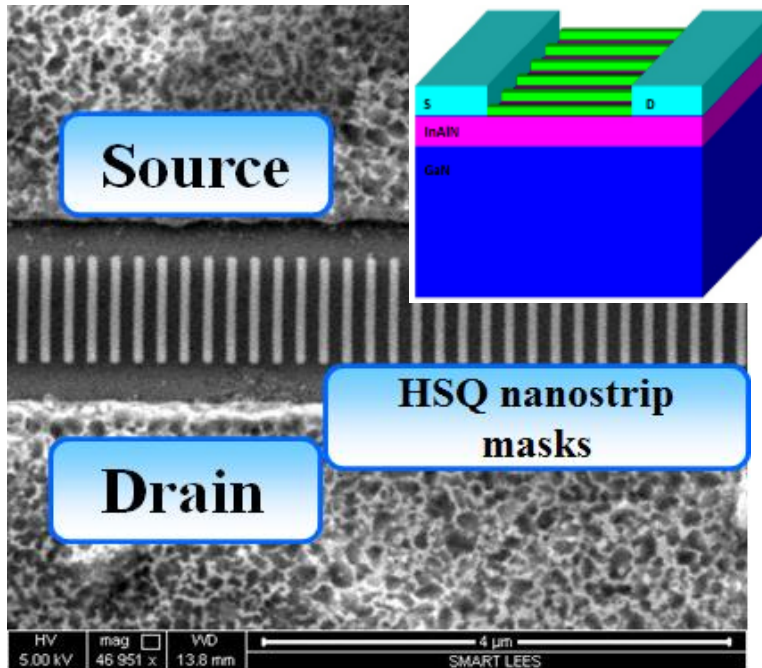
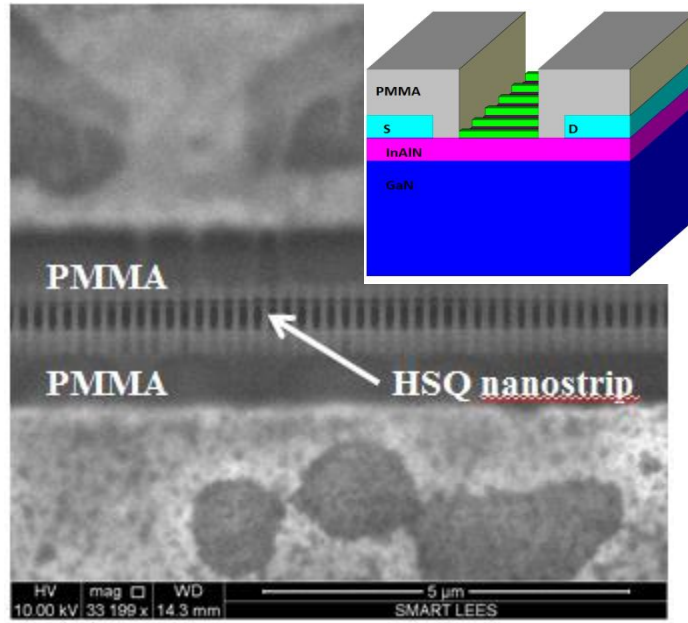


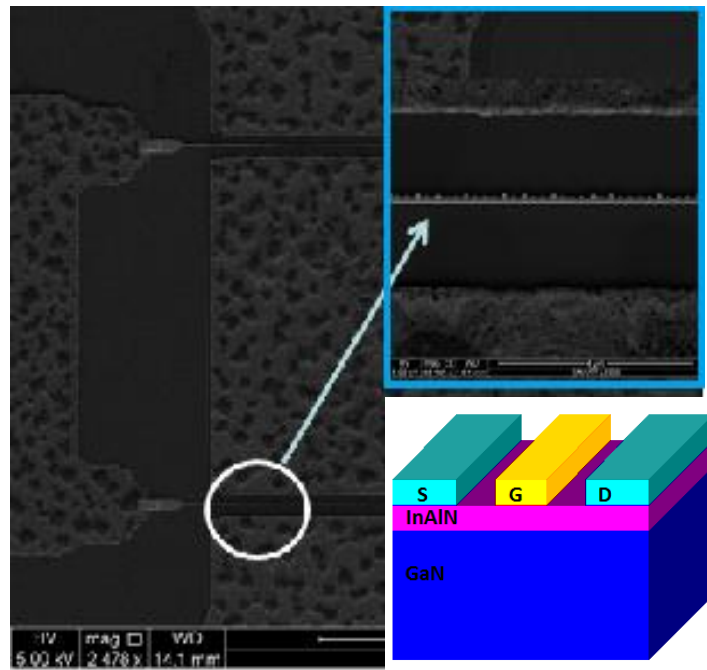
Fig. 4.10 SEM image of HSQ nanostrrips

PMMA gate patterns were also defined by EBL. 30 keV Arsenic ions were implanted to partially isolate the channel and form the planar nanostrrips. After HSQ was removed, Ni/Au gate metal was deposited.

However, this approach encountered two problems. One is that the fabricated gate has comb-like shape and the other one is that the drain current of a device is lower than expected, which is believed to be due to implantation damage.



(a)



(b)

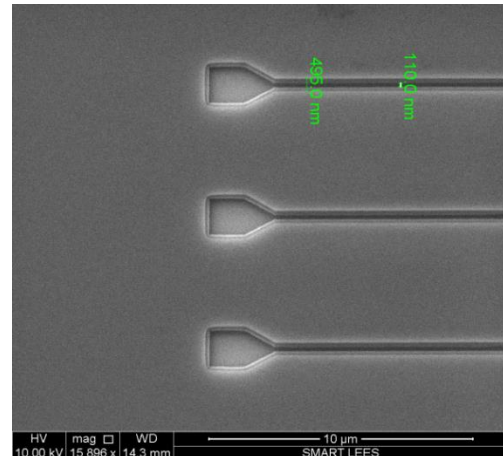
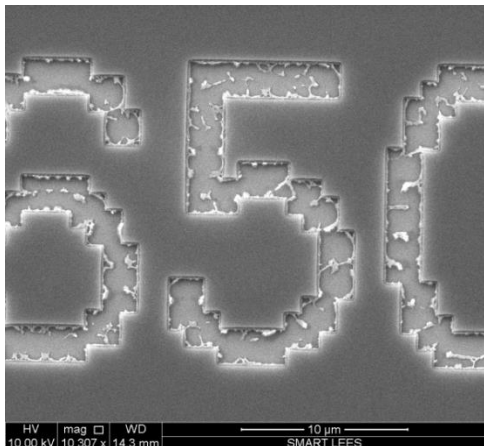
Fig. 4.11 SEM images of (a) PMMA gate pattern on HSQ nanostrip and (b) fabricated gate with a comb-like shape

As discussed in the last chapter, for EBL exposure, as the electron beam injects onto the sample surface, electrons penetrate into the resist and semiconductor material and react with resist. At the same time, scattering occurs in both the resist and the substrate material. Both forward scattering occurs in the resist and back scattering occurs in the substrate material affect the feature quality and size greatly. The PEC process reassigns dosage for each area by taking adjacent scattering into consideration. However, this no longer works for the designed process. As shown in Fig. 4.11 (a), gate pattern was defined with PMMA on top of HSQ nanostrips. In this case, the thickness of PMMA is not uniform. For the PMMA stacks on top of a HSQ nanostrip, its thickness is thinner while the thickness of PMMA stacks between two HSQ nanostrips is thicker. In addition, as discussed in the last chapter, back scattering depends on the properties of substrate material. However, HSQ nanostrips and GaN channel will give different back scattering characters. As a result, the gate profile was affected. A comb-like gate is shown in Fig. 4.11 (b). This gate profile makes it difficult to give the accurate gate length and thus complicates the analysis of the device. Moreover, the protrusion of the gate metal may cause sharp electric field and leads to low breakdown voltage and reliability.

The other issue is that the measured drain current of the planar nanostrip-channel devices are lower than expectation. Theoretically, current drivability of a planar nanostrip is higher than conventional device because the width of access region is larger compared with intrinsic channel region. This phenomenon is believed to be due to the ion implantation damage to the channel. The implantation effect experiment discussed in the last section indicated that 400 nm PMMA and 150 nm HSQ are sufficient to prevent the channel from being damaged by Arsenic ion. In this case, the thickness of PMMA stack

used to protect the channel must have been changed. Thinner PMMA due to high density nanostrip patterns was firstly suspected. However, the cross section of PMMA and HSQ stack shows there was no changes compared with unexposed resist stacks. Finally, it was found that the reaction between Arsenic ions and PMMA/HSQ during implantation process is the main reason which gives rise to the problem. Benefiting from the high resolution EBL system and carefully developed exposure recipes for various types of resist, generally the feature quality after exposure and developing is very good as showed in the last chapter. However, ion implantation significantly damaged the profile of exposed feature on the resist stack.

As shown in Fig. 4.12 (a) and (b), the patterns on PMMA stack were damaged by the ion implantation process. Fig. 4.12 (b) indicates that the profile of the gate pattern after ion implantation was no longer smooth. Actually, it can be seen that the arsenic ion beam caused the PMMA at the edge of gate pattern to shrink. The affected region was almost as large as five times of the gate length. As shown in Fig. 4.12 (c), the affected PMMA was not thick enough to protect the 2DEG underneath and thus resulting in lower drain current. In addition, since the undercut profile of PMMA was damaged, gate metal lift-off process could be difficult.



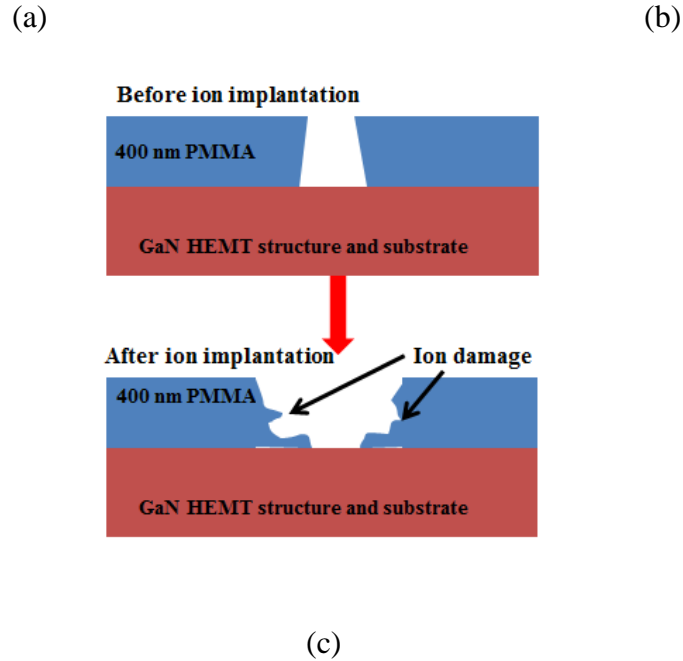


Fig. 4.12 (a), (b) SEM images of PMMA patterns after ion implantation and (c) schematic of the cross section of PMMA stack before and after ion implantation

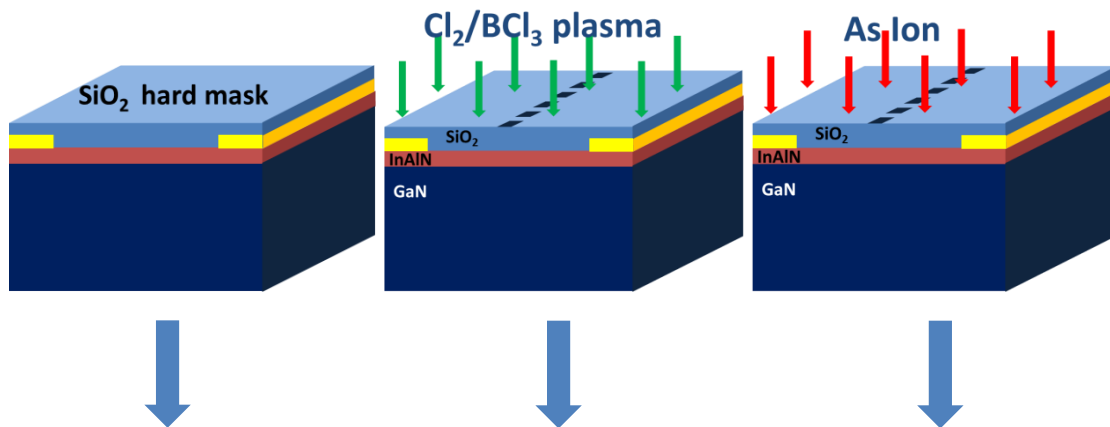
4.3.2.2.2. SiO₂-PMMA approach

To solve the problem involved in the HSQ-PMMA self-aligned approach, a new SiO₂-PMMA process has been developed. In this approach, nanostrips were firstly formed on SiO₂ hard mask. After ion implantation process, the SiO₂ hard mask was removed by BOE and gate pattern was formed at the last. By this way, PMMA was not exposed to Arsenic ion beam and thus no change in the gate profile. The main challenge for this approach was alignment because self-aligned process was not applied. Nanostrip channel and gate were not formed simultaneously. With high quality alignment marker discussed in the last chapter, the misalignment can be as low as 10 nm using the Vistech-5200 EBL system. This gave the feasibility of the SiO₂-PMMA approach. Using this process, conventional, Fin-like nanowire-channel and Planar nanostrip-channel GaN HEMTs were

fabricated on the same sample for comparison purpose. The fabricated planar nano-strip-channel device showed improved linearity in g_m and f_T compared with conventional device and less degradation in operation frequency compared with Fin-like nanowire-channel device.

The devices in this work were fabricated on an InAlN/GaN heterostructure grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The heterostructure in this work is the same as the high speed device developed in the last chapter. Its epilayers include a 2 nm of GaN cap, a 9 nm unintentionally doped $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$, a 1 nm of AlN spacer and a 1.5 μm of unintentionally doped GaN buffer layer. The measured 2-dimensional electron gas (2DEG) mobility and density are $1250 \text{ cm}^2/\text{Vs}$ and $1.65 \times 10^{13} \text{ cm}^{-2}$, respectively.

Three different devices including a conventional GaN HEMT, a fin-like nanowire channel HEMT and a planar nano-strip channel HEMT were fabricated together for comparison. The process flow for the fabrication is illustrated in Fig. 4.13.



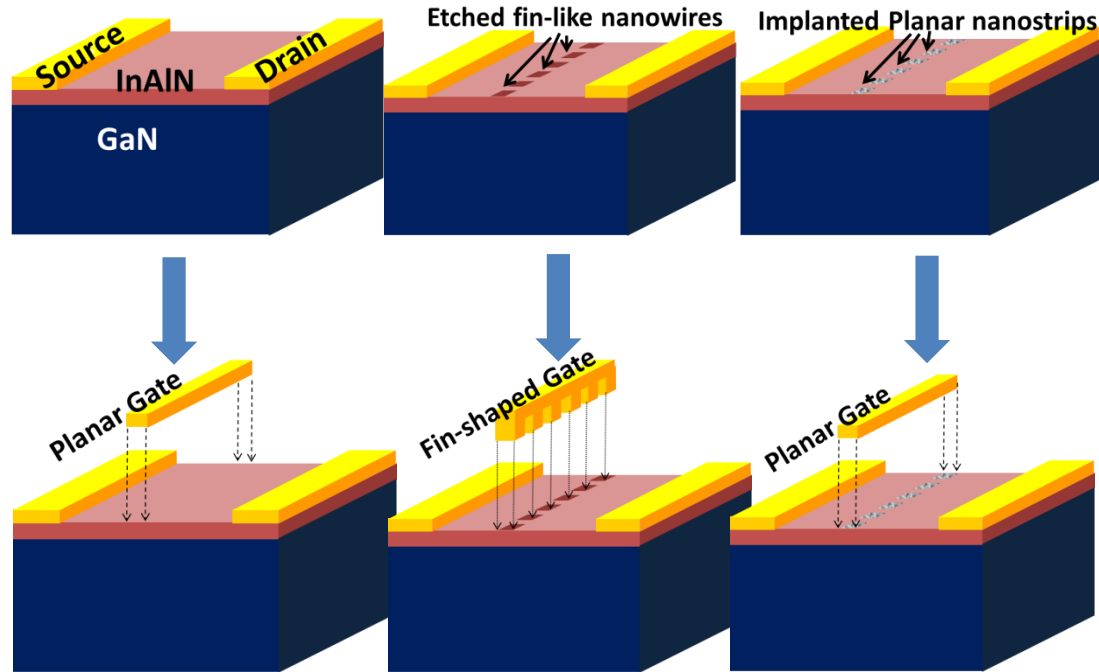
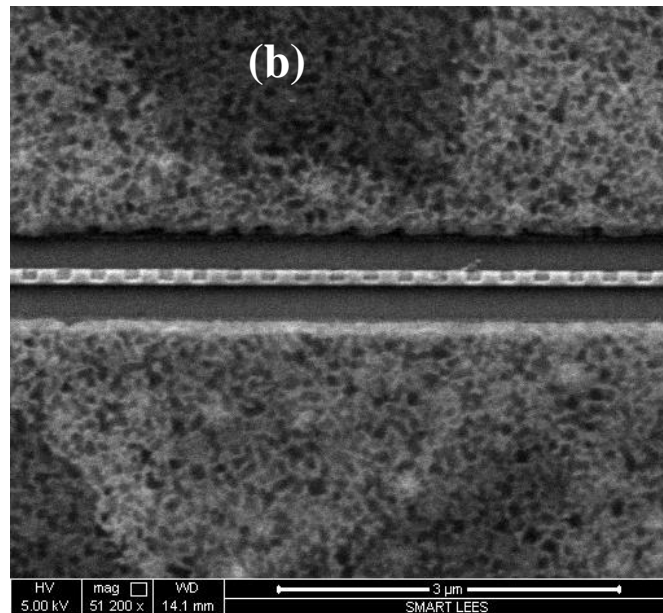
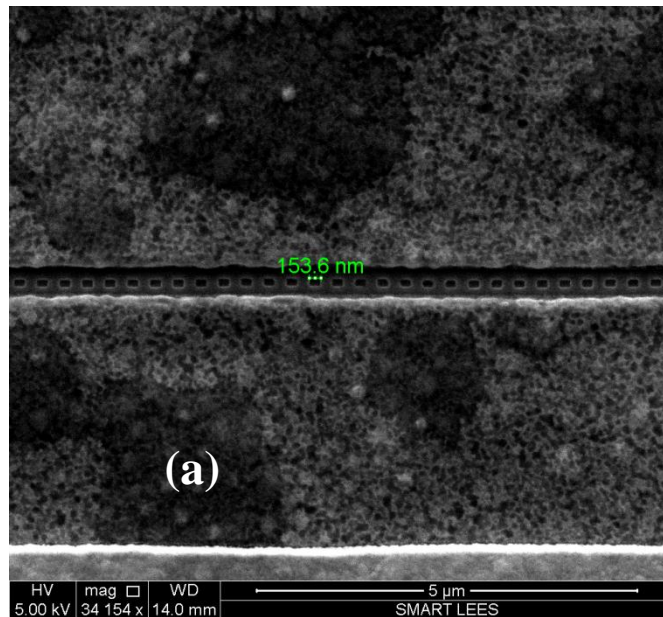


Fig. 4.13 Fabrication flow of the (a) conventional (b) fin -like nanowire and (c) planar nanostrip GaN HEMTs

All the device fabrication started from mesa isolation by dry etching using Cl_2/BCl_3 plasma. The mesa height is around 120 nm. Ti/Al/Ni/Au (20/120/40/50 nm) was deposited and annealed at 725 °C for 30 s in N_2 atmosphere to form the source and drain ohmic contacts (contact resistance $R_c \sim 0.2 \Omega\text{-mm}$). For the planar nanostrip channel devices, after ohmic contact formation a 100-nm SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). The nanostrip channel was patterned by electron beam lithography (EBL) using PMMA 950 A4 resist and dry etched in CF_4 and CHF_3 plasma to form the hard mask for the subsequent ion implantation. The line-to-space ratio of SiO_2 hard mask is 150: 150 nm. Arsenic ions at 30 keV were implanted to partially isolate the channel and form the planar nanostrips. After the removal of the SiO_2 hard mask, the gate was defined by electron beam lithography with PMMA 950 A4 resist

and 30/70 nm Ni/Au metallization. For the fin-like nanowire GaN HEMT, the partial channel isolation was realized by dry etching to a depth of around 80 nm instead of ion implantation. During the fabrication of the conventional GaN HEMT, the SiO₂ hard mask patterning and the partial channel isolation steps were skipped. All the devices in this work have a gate length $L_g=80$ nm and a source-to-drain distance $L_{sd}=1$ μm .



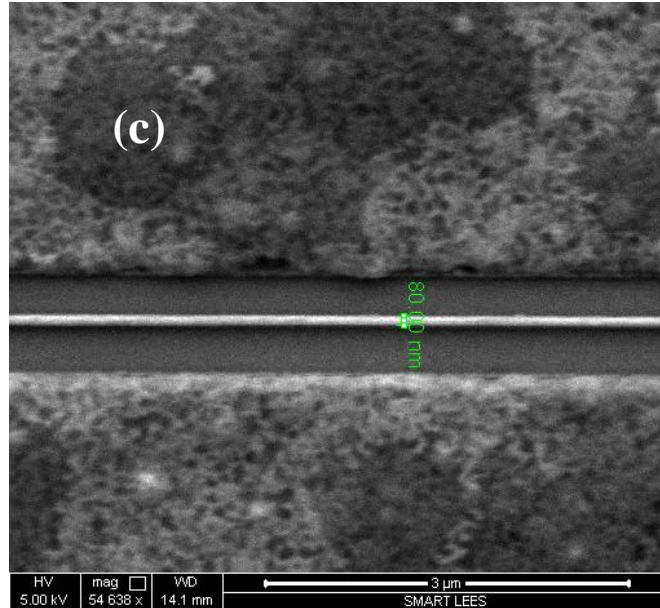


Fig. 4.14 SEM images of (a) etched nanostrip-channel, (b) good alignment between gate metal and nanostraps and (c) fabricated planar nanostrip-channel device

SEM image of etched nanostraps with line-to-space ratio of 150:150 nm is shown in Fig. 4.14 (a). As shown in Fig. 4.15 (b), the misalignment between the etched-nanostraps and the gate metal was very small. The fabricated planar nanostrip-channel device is shown in Fig. 4.14 (c). As the ion implantation process was not destructive, the channel surface remained planar and looked similar to a conventional device.

To evaluate the impact of Arsenic ion implantation, several gateless devices with channel length $L_{sd}=3\ \mu\text{m}$ and channel width $W_c=50\ \mu\text{m}$ were used to monitor the process. Some devices were exposed to Arsenic implantation; some were exposed to Cl_2/BCl_3 plasma dry etching; and others were protected by SiO_2 hard mask during implantation or dry etching. The drain current for all the devices were measured for $V_d=0$ to 10 V. The typical measured I_d of all types of devices is shown in Fig. 4.15.

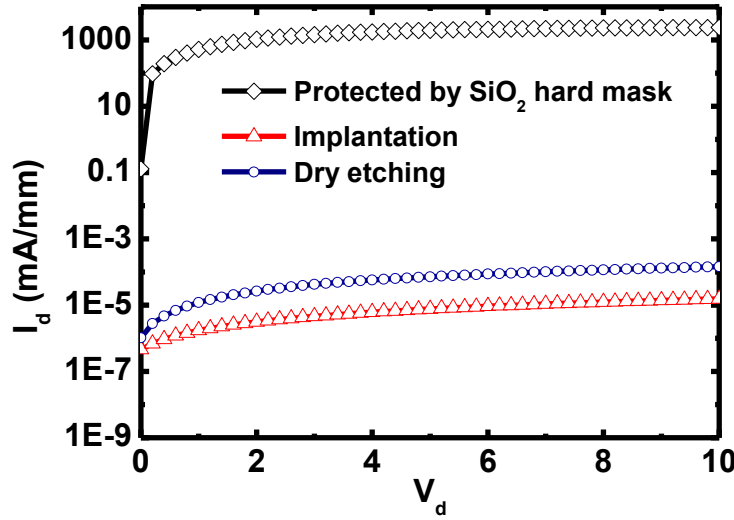


Fig. 4.15 Isolation effect of dry etching and arsenic ion implantation

As shown in Fig. 4.15, the drain current of implantation and dry etching devices are around eight to nine orders of magnitude lower than that of the devices covered by SiO₂ hard mask. In this case, it is evident that the 2DEG of the unmasked region is fully removed after Arsenic ion implantation. In addition, compared with dry etching isolation, Ion implantation showed even better isolation effect.

4.3.3. Device Characterizations

The dc characteristics of the conventional, fin-like nanowire and planar nanostrip channel GaN HEMTs are shown in Fig. 4. For both planar-nanostrip device and fin-like nanowire device, the dc current and transconductance g_m were normalized by the effective electrical channel width $W_{\text{eff}} = 150 \text{ nm} / (150 + 150) \text{ nm} \times W_{\text{total}} = 100 \text{ } \mu\text{m}$. Where $W_{\text{total}} = 200 \text{ } \mu\text{m}$ is the total width of the ohmic contacts and 150 nm is the line or space width of the SiO₂ hard mask.

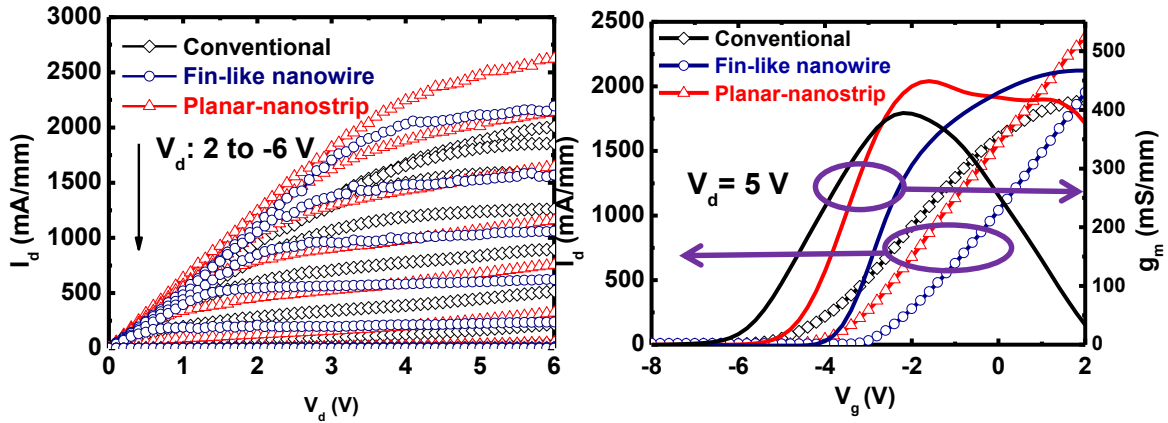


Fig. 4.16 DC characteristics of planar nanostrip, fin-like nanowire and conventional GaN HEMTs

As can be seen in Fig. 4.16, the maximum output current density of the fin-like nanowire channel device and the planar nanostrip channel device are higher than that of the conventional device. This is consistent with the expectation that the former two types of structures have higher current drivability than the latter conventional structure [1, 2]. The planar nanostrip channel device shows a higher current density than the fin-like nanowire device, which is believed to be due to the damage caused by the dry etching in the fin-like nanowire channel device.

The planar-nanostrip and fin-like nanowire channel devices clearly show better linearity in g_m (See Fig. 4.16). To quantitatively evaluate the linearity performance of different types of devices, we define a figure of merit namely gate-voltage-swing (GVS) which is the gate voltage range that the parameters (g_m and f_T) remain not smaller than 80% of their peak value, similar to that in [18]. For transconductance g_m , the corresponding GVS values of conventional, fin-like nanowire channel and planar nanostrip channel

devices are 1.8 V (from -2.8 to -1V), higher than 3.3 V (from -1.3 to >2 V) and higher than 4.8 V (from -2.8 to >2 V) , respectively.

The higher linearity in g_m of the nanowire/nanostrip channel devices validates the reported mechanism described in [2], namely the reduction of the increase of source resistance R_s at a high channel current. R_s affects the measured g_m through

$$g_m = \frac{g_{m.int}}{1 + R_s \cdot g_{m.int}} \quad (4.2)$$

where $g_{m,int}$ is the intrinsic transconductance. The measured R_s as a function of drain current for all the three types of devices are shown in Fig. 4.17. The R_s was measured using a standard method for field effect transistors namely the current injection method as described in [19]. The measurement setup was illustrated in the inset of Fig. 4.17. During this measurement, the gate electrode was injected with a very small constant current so that voltage drop between the gate electrode and the channel below gate was kept constant, which is the turn-on voltage V_{on} of the Schottky gate diode. Thus, the gate voltage V_g is equal to the voltage at the source edge of the gate V_s plus V_{on} [19]. The derivative of the gate voltage with respect to the drain current gives the source access resistance [19]. As shown in the formula below.

$$R_s = \frac{dV_s}{dI_{ds}} \quad (4.3)$$

since $V_g = V_s + V_{on}$, R_s can be expressed as

$$R_s = \frac{dV_g}{dI_{ds}} \quad (4.4)$$

As the drain current increases, the R_s of both planar nanostrip channel and fin-like nanowire channel devices remains nearly unchanged, while it increases obviously for the conventional device. This result agrees with the previous publication by D. S. Lee *et. al.* in [2] and suggests that the dynamic source resistance plays an important role in the nonlinearity of GaN HEMTs. Also, thanks to the smaller access and contact resistance normalized by the active channel width, the planar nanostrip and fin-like nanowire channel device show 14% and 18% larger maximum transconductance $g_{m,max}$ than the conventional device. Due to the enhanced gate static control, the threshold voltage shifts positively by 1 V and 2 V for the planar nanostrip channel and fin-like nanowire channel device, respectively, as compared with the conventional device.

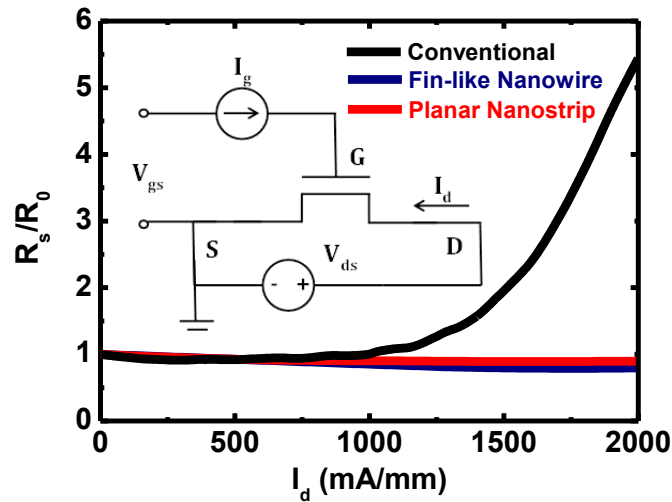


Fig. 4.17 The source resistance (R_s) of the conventional, fin-like nanowire channel and planar nanostrip channel GaN HEMTs, R_{s0} is the source resistance when $I_d=0$ mA/mm

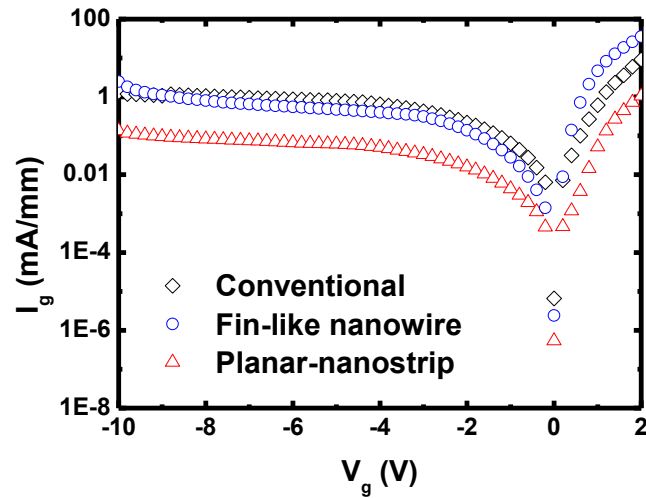


Fig. 4.18 Gate leakages of conventional, fin-like nanowire and planar-nanostrip HEMTs

The gate leakages I_g of the three types of devices are shown in Fig. 4.18. At positive gate bias, the fin-like nanowire device shows higher I_g while the I_g of planar-nanostrip device is lower compared with that of conventional device. At reverse gate biases, the gate leakage currents of the conventional and fin-like nanowire channel devices are similar, and the planar-nanostrip devices are about one order of magnitude lower. The high gate leakage current can be reduced by applying a thin layer of dielectric between the gate and top barrier to form a MIS structure [18], which will be discussed in the next chapter.

Benefitting from the better gate electrostatic control of the 2DEG, the Planar nanostrip-channel HEMTs also showed two-order of magnitude lower leakage current (from 7.6×10^{-2} to 8.2×10^{-4} mA/mm) and lower subthreshold swing (SS) (from 339 to 189 mV/dec) as shown in Fig. 4.19. Moreover, due to the same reason, the DIBL of a planar nanostrip-channel device is also lower than that of the conventional device (from 130 to 80 mV/V).

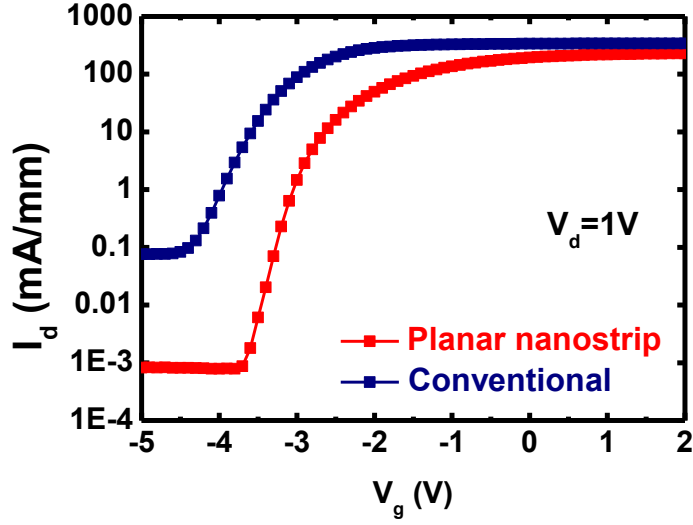


Fig. 4.19 Subthreshold swing characteristics of conventional and planar nanostrip-channel device

Small signal S-parameters were measured and the cut-off frequency f_T , after de-embedding the pad capacitance, of all three devices as a function of the gate bias V_g at $V_d = 5 \text{ V}$ were shown in Fig. 4.20. The f_T of the conventional device decreases significantly at a high gate bias or a high drain current. The source and drain resistance R_s and R_d affect f_T significantly through the expression:

$$f_T = \frac{g_{m,\text{int}}}{2\pi(C_{gs} + C_{gd}) + [(R_s + R_d)[g_{m,\text{int}}(C_{gs} + C_{gd}) + g_{m,\text{int}}C_{gd}]} \quad (4.5)$$

where C_{gs} and C_{gd} are the gate-source capacitance and gate-drain capacitance respectively. By suppressing the access resistance increase at high current levels, the planar nanostrip and fin-like nanowire devices showed much flatter f_T curves. The GVS values for f_T of the conventional, fin-like nanowire channel and planar nanostrip channel devices, are 1.3 V

(from -2.5 to -1.2 V), 3.6 V (from -2 to 1.6 V) and 3.5 V (from -2.4 to 1.1 V) respectively.

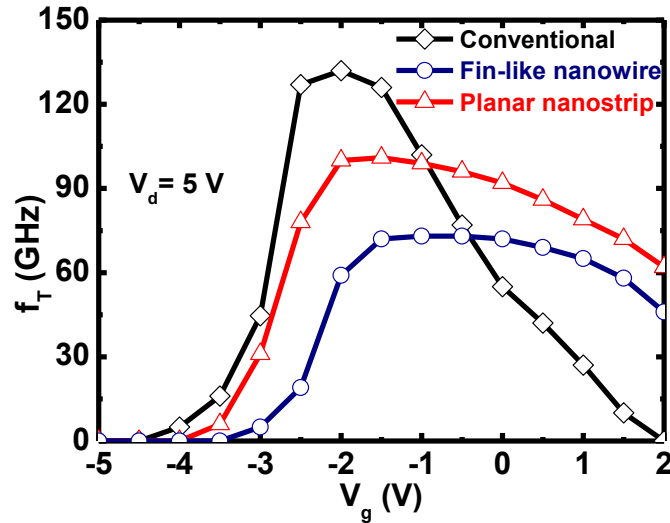


Fig. 4.20 f_T as a function of V_g after pad capacitance de-embedded of conventional, fin-like nanowire and planar-nanostrip HEMTs

The maximum f_T of the conventional, planar nanostrip and fin-like nanowire at $V_d=5$ V are 126 GHz, 96 GHz and 67 GHz respectively (See Fig. 4.20). Compared with the conventional HEMT, the peak f_T of the planar nanostrip channel device and fin-like nanowire channel device is 24% and 45% less, respectively. This is due to the extra parasitic capacitance introduced by the gate metal in the isolated channel regions, as can be seen in Fig. 4.9. The f_T of planar nanostrip channel device is higher than that of the fin-like nanowire device at all gate bias. This agrees with the simulated results of gate capacitance in Fig. 4.9, and indicates that the planar nanostrip structure can introduce less parasitic capacitance than the fin-like nanowire device, thus providing good RF performance with enhanced linearity.

4.4. Geometry effect on InAlN/GaN HEMTs

As discussed in the last section, the increase of source access resistance has been proven to be the main reason of nonlinearity in g_m and f_T of GaN HEMT device. Planar nanostrip-channel device is an effective approach to obtain high linearity performance. For a better understanding of the performance of such devices and a clear direction of device design, geometry effect including nanostrip size and gate-to-source distance L_{gs} has been investigated.

Nanostrip-to-space Ratio

In terms of device design of Planar nanostrip-channel GaN HEMTs, the nanostrip and space sizes are the most important parameters affecting device performance through current distribution and gate fringing capacitance. As shown in Fig. 4.21, $W_{\text{nanostrip}}$ represents the width of the nanostrip while W_{space} is the width of the isolated region by ion implantation. In this study, W_{space} was fixed at 100 nm and $W_{\text{nanostrip}}$ was 100, 150 and 200 nm.

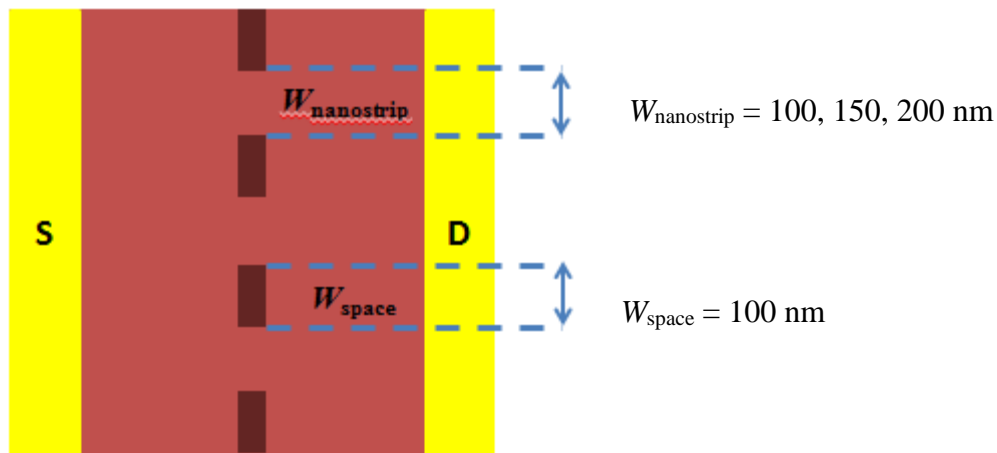


Fig. 4.21 Variation of nanostrip width in the device layout

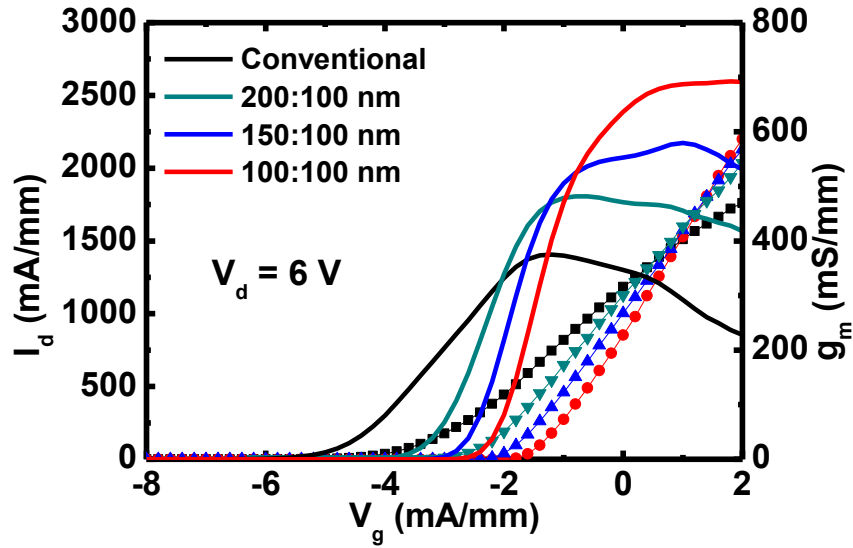


Fig. 4.22 Transfer characteristics of the planar nanostrip-channel device with different nanostrip widths

The DC transfer characteristics of the planar nanostrip-channel device with different nanostrip widths are shown in Fig. 4.22. The device with smaller $W_{\text{nanostrip}}$ exhibited higher current drivability and g_m . In addition, better linearity in g_m was also observed. This result is consistent with the analysis in the last section. In this work, as the width of isolated region was fixed, a smaller $W_{\text{nanostrip}}$ means a relatively larger ratio of access region to nanostrip channel. In this case, the current through the device is not limited by the source access region and it serves more like an idea source. Thus, the device performance becomes closer to the intrinsic device with high current drivability and linearity.

With enhanced gate static control due to the increased coupling between the additional gate and 2DEG as shown in Fig. 4.23, the device with smaller $W_{\text{nanostrip}}$ also showed less negative threshold voltage.

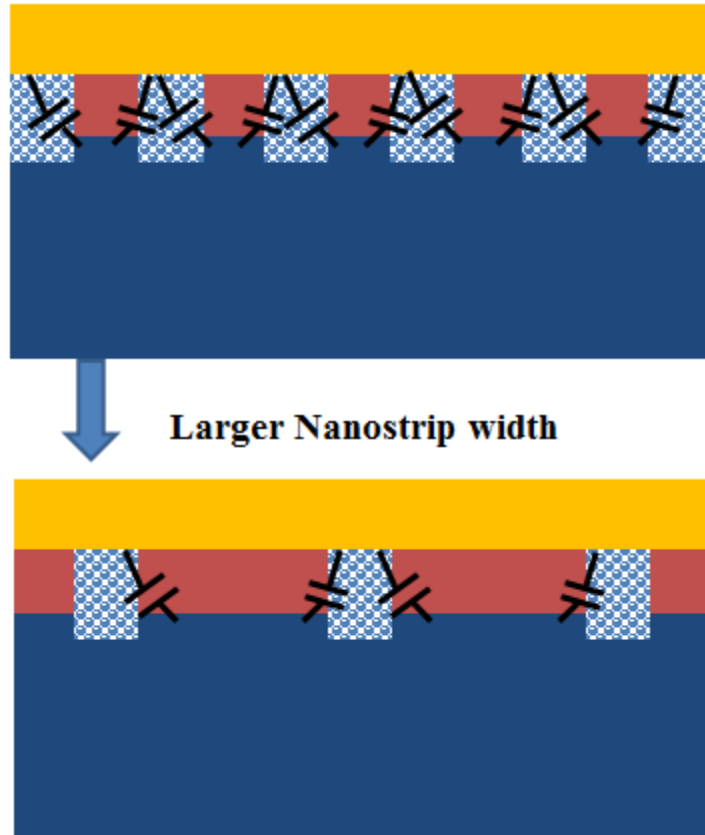


Fig. 4.23 Coupling between additional gate and channel of device with different nanostrip width

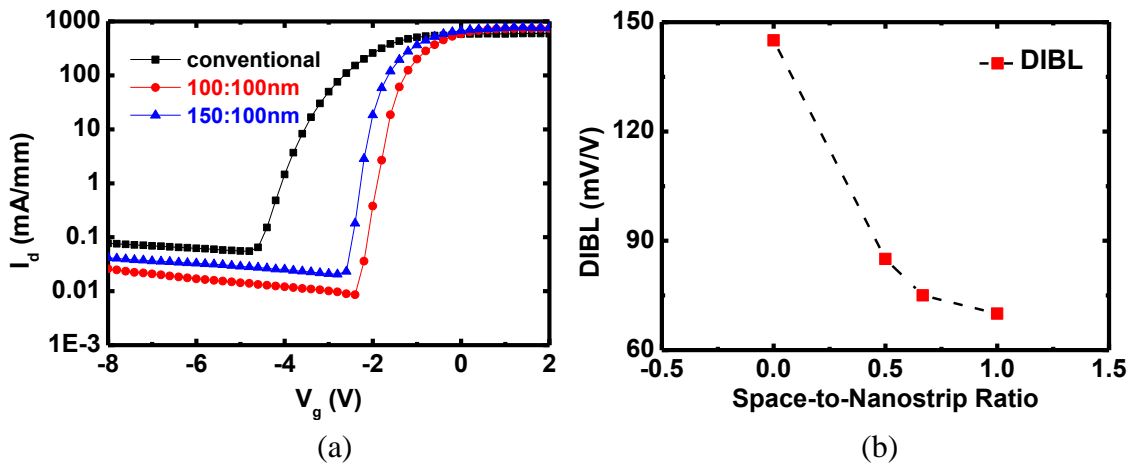


Fig. 4.24 (a) subthreshold characteristics and (b) DIBL of devices with different $W_{\text{nanostrip}}$

Due to the same reason, device with smaller $W_{\text{nanostrip}}$ exhibited lower leakage current, subthreshold swing and DIBL as shown in Fig. 4.24 (a) and (b). For Fig. 4.24 (b), the space-to-nanostrip ration is defined as

$$R = \frac{W_{\text{space}}}{W_{\text{nanostrip}}} \quad (4.4)$$

As W_{space} was fixed at 100 nm, the R value for the devices with nanostrip width of 100, 150 and 200 nm are 1, 0.67 and 0.5, respectively. Since there is no isolated region for a conventional device, its R value equals to 0.

De-embedded f_T as function of gate bias for the devices with different nanostrip width is shown in Fig. 4.25. Similar with the g_m trend shown in Fig. 4.23, as gate bias increases, the f_T value of a device with smaller $W_{\text{nanostrip}}$ drops slower. However, due to the increased gate fringing capacitance, lowest maximum f_T was observed in the device with $W_{\text{nanostrip}}$ of 100 nm.

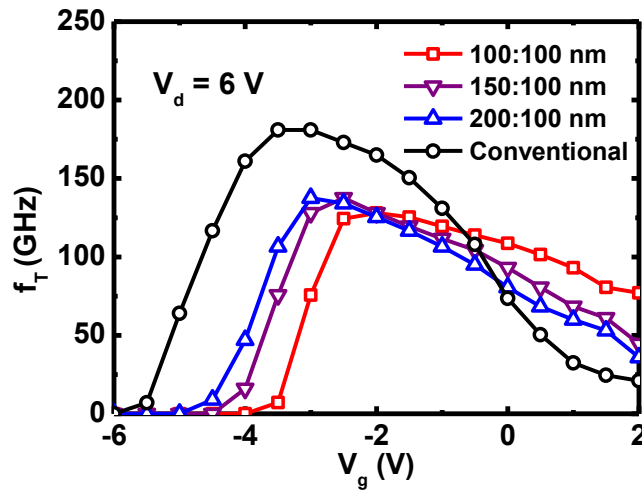


Fig. 4.25 De-embedded f_T for the devices with different $W_{\text{nanostrip}}$

In conclusion, a smaller nanostrip width will lead to better linearity in g_m and f_T , better subthreshold performance and lower DIBL. However, the maximum operation speed of the device decreases with the nanostrip width. Thus, tradeoff is necessary between the linearity and high speed performance.

Effect of gate-to-source distance

Since the linearity performance is limited by the increase of source access resistance, shrinking the gate-to-source distance is another possible strategy to obtain high linearity performance in GaN HEMTs. In this study, the source-to-drain distance was fixed at 3 μm while the gate-to-source distance was 0.9, 1.3 and 1.7 μm . Gate length was 100 nm for all the devices.

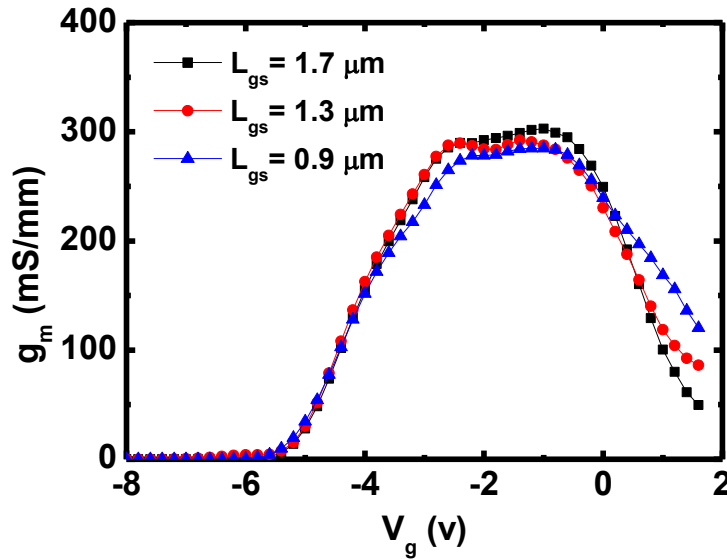


Fig. 4.26 g_m as function of gate bias for the device with different gate-to-source distance
 g_m as function of gate bias for the devices with different gate-to-source distance is shown in Fig. 4.26. For the device with shorter L_{gs} , its g_m drops slower than that of a device with

longer L_{gs} . However, this difference is very small. Overall, the g_m curves for the different devices looks very similar to each other and no increase in the current drivability was observed in the device with shorter L_{gs} . This is believed to be due to the fact that although the gate-to-source distance was shrunk, L_{gs} of 0.9 μm is still quite large to achieve high linearity. In addition, the electron velocity in the source access region is still lower than that under the gate. As the width of the source access region is the same as that of the intrinsic device, current drivability was not improved.

To solve this issue, gate-to-source can be further shrunk to achieve a near-self-aligned source and drain while the gate-to-drain distance remains constant to avoid lower breakdown voltage.

4.5. Conclusion

In this chapter, the mechanisms of the poor linearity performance of the g_m and f_T at high gate bias were clarified. It has been proven that this problem is caused by extrinsic device limiting elements of highly scaled GaN HEMTs rather than the intrinsic limitation of GaN HEMTs device. To overcome the poor linearity in GaN HEMTs, a novel planar-nanostrip GaN HEMTs structure using ion implantation technology was developed to improve the linearity performance and maintain f_T at a high level without introducing too much gate parasitic capacitance. Novel fabrication techniques were developed including Arsenic ion implantation for isolation application, nanostrip-channel formation using HSQ-PMMA self-aligned and SiO_2 -PMMA approaches. Moreover, the planar-nanostrip device also showed much improved maximum drain current I_{dmax} up to 2.6 A/mm, which is close to theoretical expectation. Also, device geometries including line-to-space ratio

of the nanostrip-channel and gate-to-source distance have been studied. These results do not only identify the origins of the non-linear performance in GaN HEMTs, but also provides good guidelines for designing GaN HEMTs with improved RF performance for high linearity applications.

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Chapter 5 Planar nanostrip-channel

$\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMTs on Si

5.1. Introduction

Another critical issue in GaN HEMTs is the gate leakage current. Generally, a high gate leakage current will lower the power added efficiency (PAE) and breakdown voltage, which ultimately limit the device high power performance. In the previous chapter, a planar nanostrip-channel GaN HEMT has been successfully demonstrated. In contrast to the conventional planar GaN HEMT, for a Fin-like nanowire-channel or planar-nanostrip device the transconductance g_m and current-gain cut-off frequency f_T drops very little at a high gate bias $V_g > +1$ V from their peak values [1], [2]. However, the gate leakage current of Schottky-gate HEMTs increases very rapidly with increase positive gate bias, which in turns prevents the device from operating at a gate voltage higher than +1 V. This gate leakage problem is even worse for a device with a thin InAlN barrier [2].

A metal-insulator-semiconductor (MIS) gate structure has been reported as an efficient approach to solve the issues of gate leakage current in GaN HEMT [3]. Fig. 5.1 presents a typical band diagram of a GaN MISHEMT. As shown in the figure, by inserting a dielectric layer between the gate metal and barrier layer, a significant larger potential barrier will be formed in between of the gate and channel. Thus, the high gate leakage current can be suppressed.

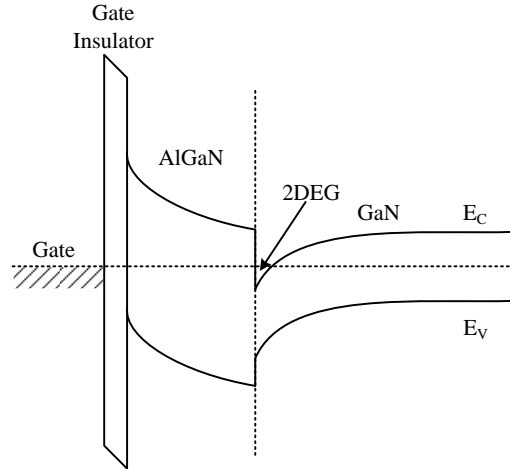


Fig. 5.1 A typical band diagram of a GaN MISHEMT

In addition to the suppressed gate leakage current, the inserted dielectric layer also has the potential to serve as a passivation layer to minimize the surface states induced anomalous such as current collapse and surface leakage [3].

In addition, a MISHEMT has a broader g_m versus gate bias than a Schottky-gate HEMT and thus can further improve the linearity performance of the device [3, 4]. In this work, a thin layer of aluminum oxide was introduced between the metal gate and the thin InAlN barrier and thereby formed a metal-insulator-semiconductor (MIS) gate in the planar nanostrip-channel GaN HEMT. This approach reduces the gate leakage current and increases the gate voltage swing and drain current swing, thus further improving the device linearity performance.

5.2. Al_2O_3 as gate dielectric

Due to the advantages of MISHEMT structure, various dielectric materials have been studied as gate insulator. In the earlier stage, Si_3N_4 [5, 6] and SiO_2 [7] have been widely applied as gate dielectric for GaN MISHEMTs. Significantly improved device

performance in both gate leakage current and current collapse has been reported [3]. However, due to the relatively low dielectric constant of these two materials, unexpected degradation in g_m and f_T has been observed, which is not desired for high frequency applications [8]. As discussed in chapter 3, gate modulation efficiency is a serious concern for deeply scaled GaN HEMTs for high frequency applications. For a field effect transistor, in order to ensure good gate modulation efficiency, the electric field along vertical direction induced by gate electrode should be significantly larger than that along lateral direction across the channel. Under this condition, the gate electrode can modulate the drain current more effectively through better control of the electron density in the channel. However, by inserting a gate dielectric layer with low dielectric constant, the vertical electric field under the gate electrode decreases. Thus, by losing its controllability to the channel charge density, gate modulation efficiency decreases.

To solve this problem, materials with higher dielectric constant can be applied. Recently, high-k material including Al_2O_3 , HfO_2 and ZrO_2 as gate insulators have been reported and showed excellent results [9-12]. Among them, high quality Al_2O_3 deposited by ALD is the most mature technique. In addition, the study of passivation effect in chapter 3 has proven Al_2O_3 to be an effective passivation material to suppress current collapse. In this work, a 6-nm Al_2O_3 dielectric layer was deposited by ALD using the same recipe as described in chapter 3 for passivation purpose. The thickness is optimized to achieve high gate voltage swing, effective passivation as well as reasonable g_m and f_T .

5.3. Device fabrication

The transistors in this work have an InAlN/GaN heterostructure grown on a high-resistivity ($\geq 6000 \text{ } \Omega\cdot\text{cm}$) Si substrate by metalorganic chemical vapor deposition (MOCVD). The schematic of the cross-section of the devices is shown in Fig. 5.2. It consists of a 2 nm of GaN cap, a 9 nm unintentionally doped $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ barrier, a 1 nm of AlN spacer and a $1.5 \text{ } \mu\text{m}$ unintentionally doped GaN buffer layer. The structure is the same as the one used in the previous chapter. The 2DEG mobility and density are measured to be $1190 \text{ cm}^2/\text{Vs}$ and $2.04 \times 10^{13} \text{ cm}^{-2}$, respectively.

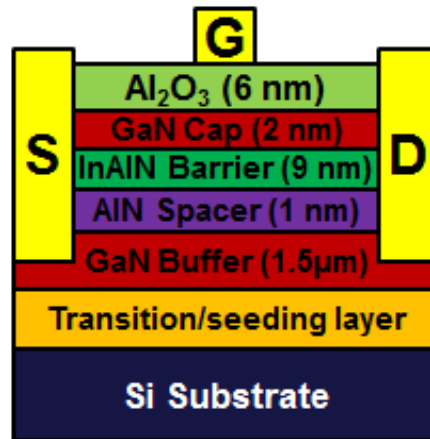
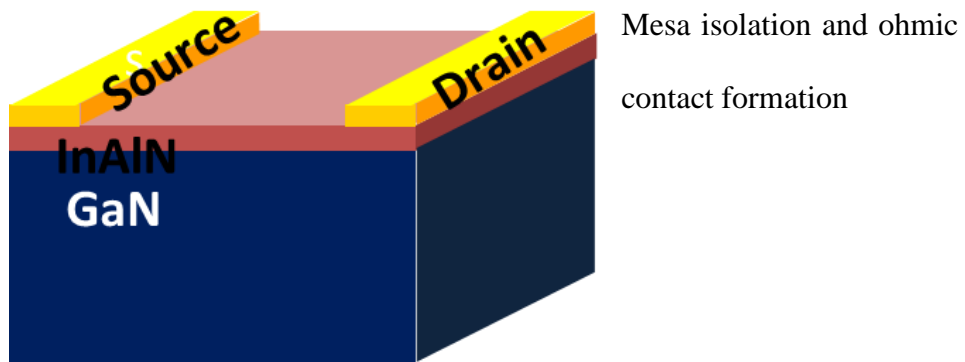
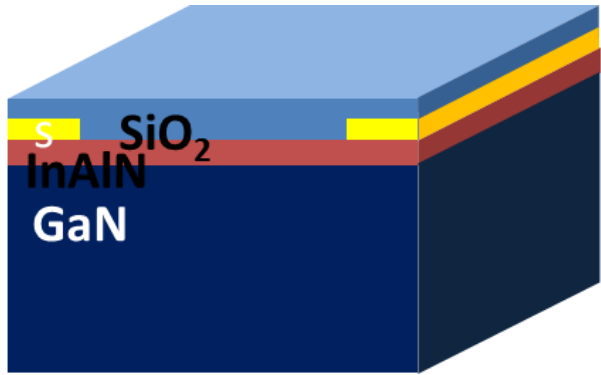


Fig. 5.2 Schematic diagram of InAlN/GaN on Si

The GaN planar nanostrip-channel MISHEMT fabrication process is similar to that described in the last chapter except for the step which the gate oxide was introduced to form the MISHEMTs. As shown in Fig. 2, the fabrication started from mesa isolation using Cl_2/BCl_3 plasma dry etch. Source and drain ohmic contacts were formed after Ti/Al/Ni/Au (20/120/40/50 nm) deposition and annealing at 725°C for 30 s. The contact resistance R_c was $\sim 0.3 \text{ } \Omega\cdot\text{mm}$ measured using the Transmission Line Method (TLM). After ohmic contact formation, a 100-nm SiO_2 layer was deposited by plasma-enhanced

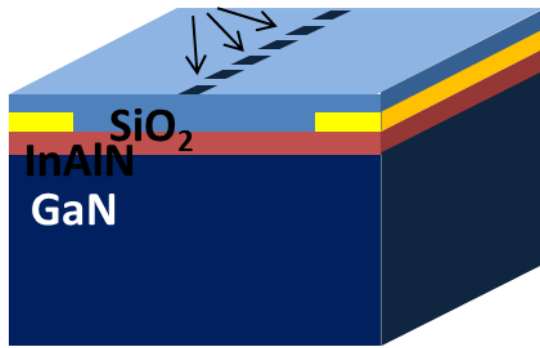
chemical vapor deposition (PECVD), and patterned by electron beam lithography (EBL) and dry etch to form the hard mask for the subsequent ion implantation. Arsenic ions with energy of 30 keV were then implanted into the device channel region to form the planar nanostrip-channels. The line-to-space ratio of the SiO₂ hard mask is 150:150 nm. After removing the SiO₂ hard mask, a 6-nm Al₂O₃ gate dielectric was deposited at 250°C by an Atomic Layer Deposition (ALD) system with TMA and H₂O as precursors. Finally, the gate was defined by EBL and realized using 30/70 nm Ni/Au metallization. For comparison, Schottky-gate GaN HEMTs with planar nanostrip channels were also fabricated at the same time, using almost the same process steps except that the ALD Al₂O₃ deposition was skipped. All the devices in this work have a gate length $L_g = 100$ nm and a source-to-drain distance $L_{sd} = 1$ μm. The gate width (W_g) is 2×100 μm for all devices. The dc characterization was carried out using a Keysight B1505A semiconductor device analyzer and the small signal RF characterization was carried out using a Keysight N5244A PNA-X network analyzer.



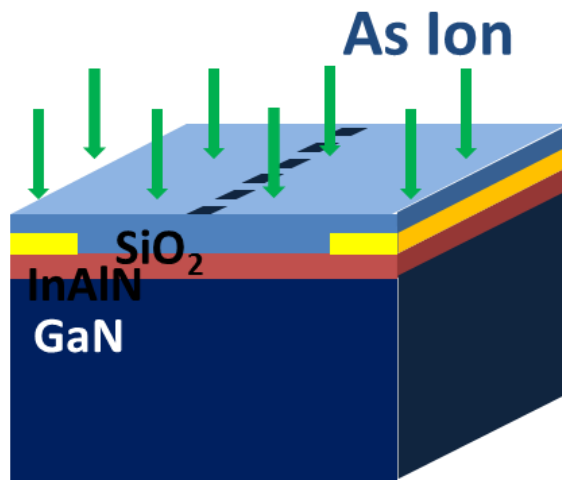


SiO₂ hard mask
deposition

Nanostrip structures patterned by EBL



Nanostrips patterning



Arsenic ion
implantation for
isolation

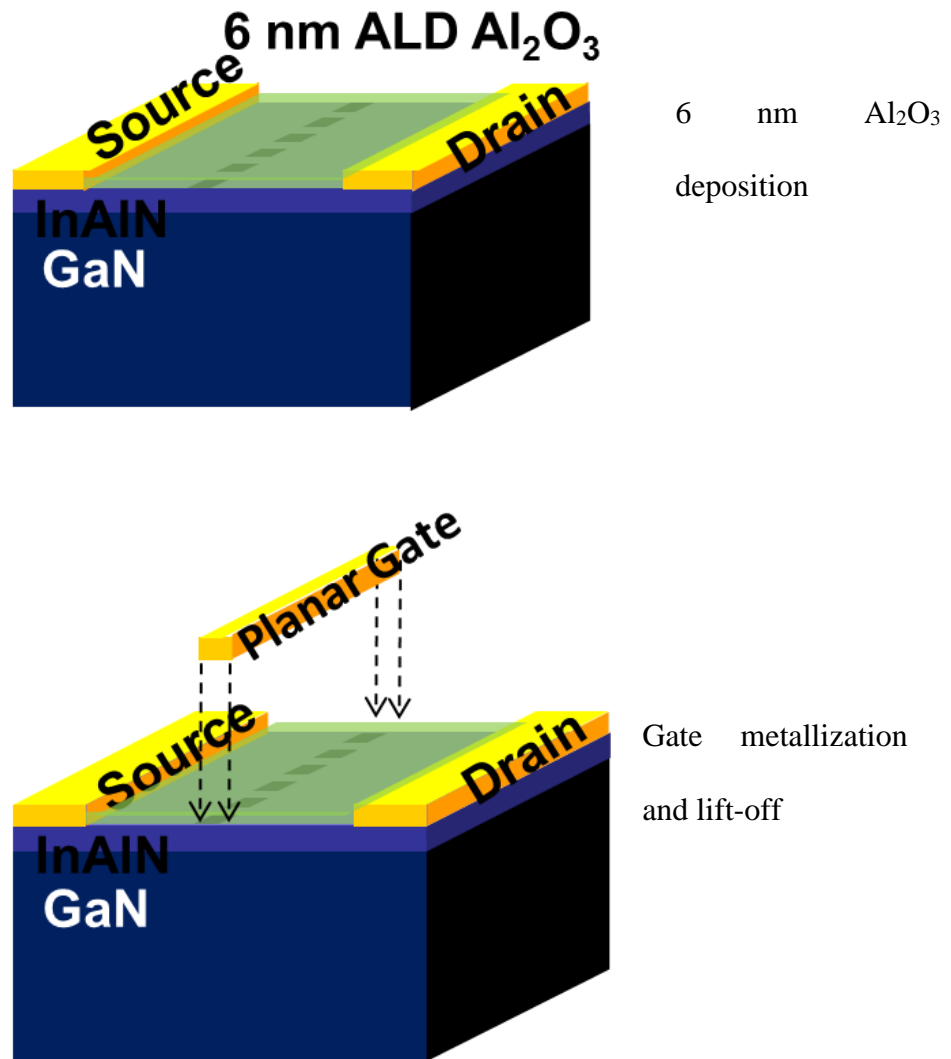


Fig. 5.3 Fabrication flow of the planar nanostrip GaN MISHEMTs

5.4. Device characterization and analysis

The gate leakages I_g of the GaN Schottky-gate HEMTs and MISHEMTs are shown in Fig. 5.4. Compared to the Schottky-gate Planar-nanostrip HEMT, the gate current of the MISHEMT is much lower. The I_g of a Schottky-gate Planar-nanostrip GaN HEMT

reaches $I_g=1$ mA/mm at $V_g = +1.2$ V, whereas at $V_g = +4$ V, the gate current I_g (4×10^{-5} mA/mm) is still much lower than 1 mA/mm for the Planar-nanostrip GaN MISHEMT, which means that it is able to be biased at more than $V_g = +4$ V.

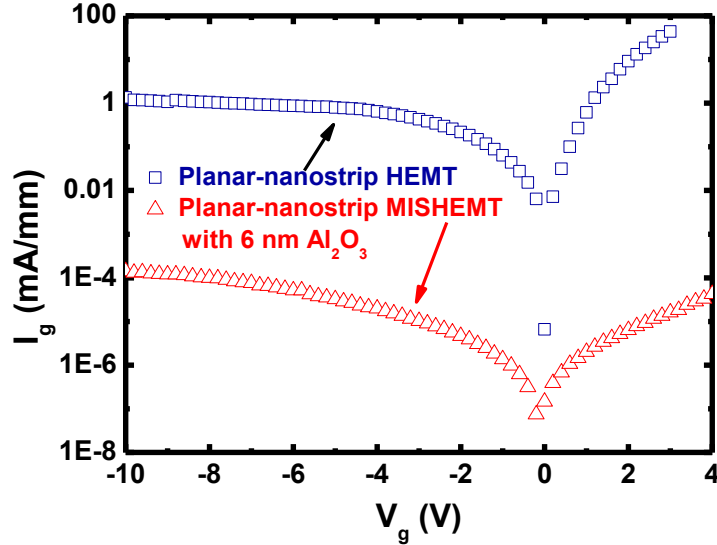


Fig. 5.4 The gate leakage currents of planar-nanostrip channel HEMT and MISHEMT

The dc characteristics of the planar-nanostrip channel GaN HEMT and MISHEMT are shown in Fig. 5.5. The dc current I_d and transconductance g_m were normalized by the effective electrical channel width $W_{eff} = 150 \text{ nm} / (150 + 150) \text{ nm} \times W_{total} = 100 \text{ } \mu\text{m}$, where $W_{total} = 200 \text{ } \mu\text{m}$ is the total width of the access regions and 150 nm is the line or space width of the SiO_2 hard mask. Because the MISHEMT device with Al_2O_3 layer as a gate dielectric layer can be biased over $V_g = +4$ V, a higher drain current drivability can be achieved. As shown in Fig. 5.5 (a), $I_{d,max}$ as high as 2.7 A/mm was achieved at $V_g = +4$ V, which is much higher than $I_{d,max}$ of 2 A/mm for the conventional Schottky-gate Planar-nanostrip GaN HEMT at $V_g = +1$ V. It has been proven in the last chapter that by increasing the relative current drivability of the access region, a nanostrip channel structure effectively suppresses the increase of source access resistance R_s at high gate bias.

Thus, the Planar-nanostrip channel device showed very much improved linearity over conventional GaN HEMT. It can be observed from Fig. 5.5 (b) that the Planar-nanostrip channel GaN MISHEMT has an even broader g_m over the Planar-nanostrip HEMT with conventional Schottky gate, which suggests improved linearity performance. To quantitatively evaluate the linearity performance of different types of devices, we define a figure of merit namely gate-voltage-swing (GVS) which is the gate voltage range that the parameters (g_m and f_T) remain not smaller than 80% of their peak value, similar to that in [3]. For transconductance g_m , the corresponding GVS values of Planar-nanostrip HEMT and MISHEMT are 3.8 V (from -2.8 to 1V) and 5.9 V (from -2.6 to 3.3 V), respectively. Due to the increased gate-to-channel distance, the g_m peak value of the MISHEMT device is lower than that of HEMT device. The corresponding values are 450 mS/mm and 320 mS/mm, respectively.

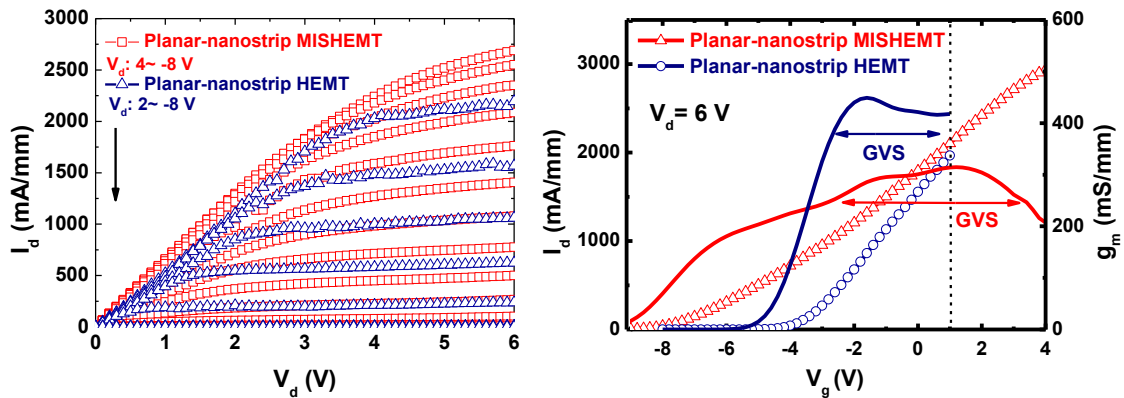


Fig. 5.5 (a) output and (b) transfer characteristics of an InAlN/GaN HEMT with a 40-nm gate

Small-signal S-parameters were measured and the cut-off frequency f_T , after de-embedding the pad capacitance, of the two types of devices as a function of the gate bias

V_g at $V_d=6$ V were shown in Fig. 5.6 It is clear that the MISHEMT has a much flatter shape for f_T . The GVS values for f_T of the planar-nanostrip HEMT and MISHEMT devices are 3.5 V (from -2.5 to 1 V) and 9.4 V (from -7.2 to 2.2 V) respectively. The maximum f_T Planar-nanostrip channel GaN HEMT and MISHEMT are 101 and 68 GHz, respectively.

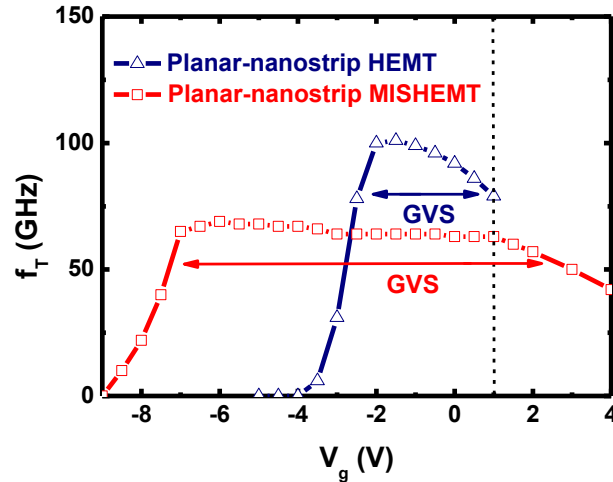


Fig. 5.6 f_T as a function of V_g after pad capacitance de-embedded

Compared with the HEMT device, the MISHEMT reported in this work showed 55% and 168% increase in g_m and f_T GVS values. On the other hand, the maximum values of g_m and f_T drop by 29% and 33% respectively and the threshold voltage V_{th} of MISHEMT is negatively shifted by 4 V. These are believed to be due to the increased spacing between the gate metal and the channel and thereby decreased gate-to-source capacitance C_{gs} [13-18]. The g_m can be approximately expressed by the function below [23].

$$g_m = \frac{v_{sat} C_{gs}}{L_g} \quad (5.1)$$

where v_{sat} is the saturation velocity of electrons and L_g is the gate length, respectively. g_m is supposed to decrease proportionally to C_{gs} . The f_T decrease reveals the enhanced short-

channel effect due to the increased gate-to-channel distance by the introduction of the gate oxide. To circumvent this issue, a high-permittivity (high-k) insulating material such as HfO₂ ($k_{\text{ox}} \sim 20\text{--}25$) [14] or ZrO₂ ($k_{\text{ox}} \sim 23\text{--}30$) [17, 18] can be applied as the gate insulator instead of Al₂O₃ ($k_{\text{ox}} \sim 9$). With a high-k gate dielectric, the gate leakage can be effectively lowered and at the same time the drop in g_m and f_T can be reduced.

For a more direct evaluation of the linearity of fabricated devices, a two-tone intermodulation characteristics measurement was carried out for conventional HEMT, Planar nanostrip-channel HEMT and Planar nanostrip-channel MISHEMT. The devices were biased at $V_d = 6$ V and two-tone class A operation at 10 GHz with an offset of 10 MHz.

In this measurement, intermodulation distortion (IMD) signals of different types of device have been measured and compared. As shown in Fig. 5.7 (a), the two-tone input signal consists of two signals at frequencies f_1 and f_2 which are very closely spaced. For an ideal amplifier without any non-linear effect, only the same frequency components can be found in the output signal. However, for device in practice as shown in Fig. 5.7 (b), frequencies components besides the input signal can be observed in the output signal due to the non-linearity of the device. These additional frequency components are intermodulation distortion signals [19]. For example, the third order intermodulation distortion signals (IM3) are $2f_1 - f_2$ and $2f_2 - f_1$. Since f_1 and f_2 are very close to each other, the IM3 signal is also close to the main frequency components in the output signal. Thus, the IM3 signal is difficult to be removed by filter. As the power level of IMD3 is due to the non-linearity of the device, it is one of the most important parameters to evaluate the linearity of GaN HEMTs.

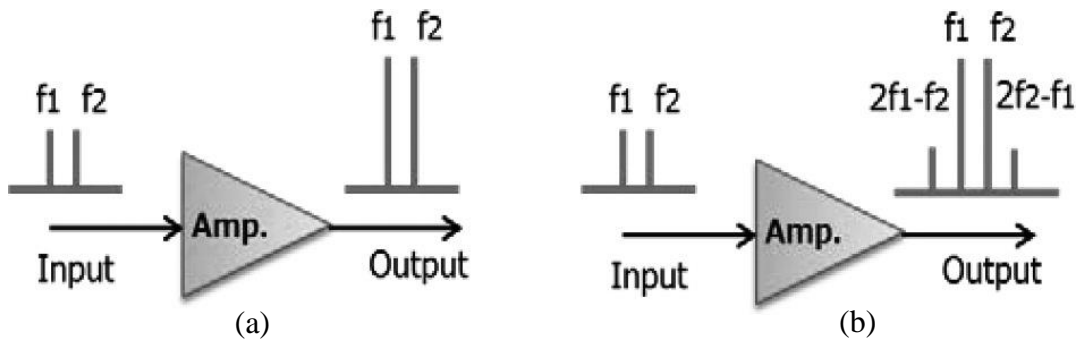


Fig. 5.7 (a) ideal amplifier without non-linearity and (b) actual amplifier [19]

Another useful parameter for linearity characterization is the third-order intercept (OIP3) value, which is defined as the point that the power levels of IM3 and output signals becomes equal by extrapolating the measured output power and IM3 in the linear region. Fig. 5.8 presents the extraction of OIP3 value of the conventional GaN HEMT.

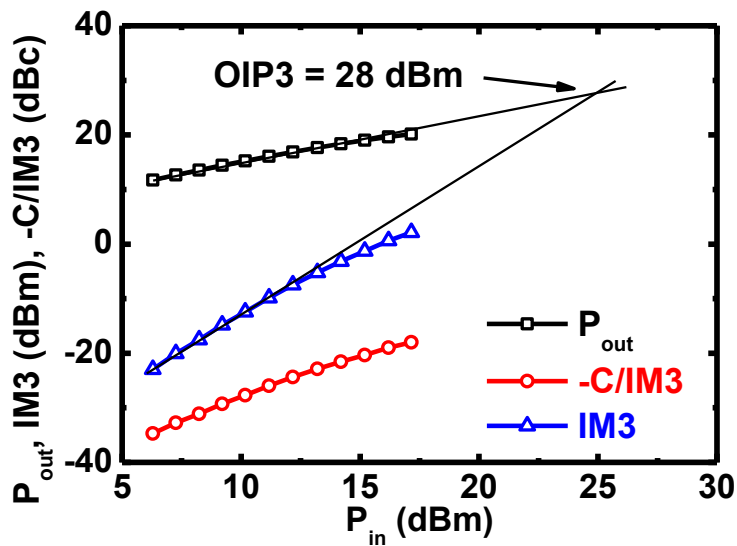


Fig. 5.8 OIP3 extraction of a conventional GaN HEMT

As shown in the figure, P_{out} represents the output power, IM3 is the third-order intermodulation distortion and $-C/IM3$ is the IM3-to-carrier ratio. An OIP3 of 28 dBm

was extracted for the conventional GaN HEMT. The OIP3 values of 32 and 39 dBm for planar nanostrip-channel GAN HEMT and Planar nanostrip-channel GaN MISHEMT respectively were extracted using the same method.

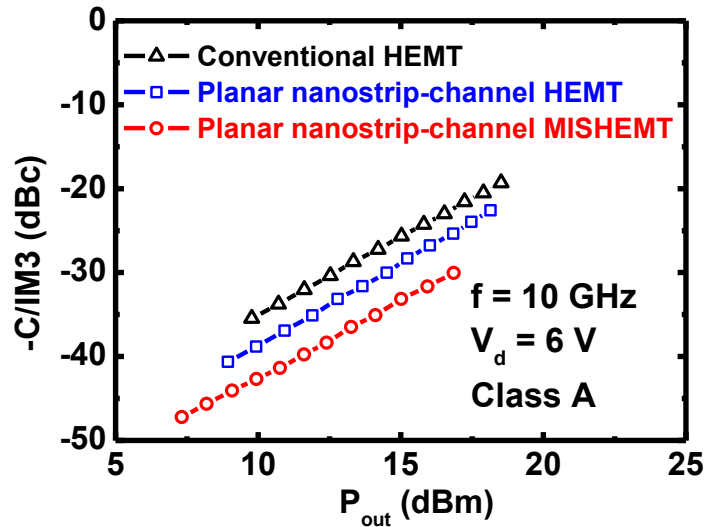


Fig. 5.9 Intermodulation distortion (IMD) characteristics of conventional HEMT, Planar nanostrip-channel HEMT and Planar nanostrip-channel MISHEMT

Intermodulation characteristics of conventional HEMT, Planar nanostrip-channel HEMT and Planar nanostrip MISHEMT are shown in Fig. 5.9. The values of IM3-to-Carrier ratio ($-C/IM3$) as a function of the output power are shown in the figure. For any of the values of P_{out} , the planar nanostrip-channel MISHEMT has the lowest $-C/IM3$ values while the conventional HEMT has the highest. For example, at $P_{out}= 15$ dBm, the $-C/IM3$ of the planar nanostrip-channel MISHEMT is 5 dBm lower than that of planar nanostrip-channel HEMT and 8 dBm better than that of conventional HEMT. It is worth noting that if normalized by the effective channel width (total nanostrisps width), the improvement in $-C/IM3$ of the planar nanostrip-channel devices can be even larger. The lower $-C/IM3$ and larger OIP3 values clearly indicate that the linearity of GaN HEMT

was improved by the planar nanostrip-channel structure as well as the insertion of 6-nm Al_2O_3 gate insulator.

5.5. Conclusion

In conclusion, a planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMT on a Si substrate with improved g_m and f_T linearity has been demonstrated in this chapter. Benefiting from the 6 nm Al_2O_3 gate insulator, the gate voltage and drain current swing of the MISHEMT device increased by 3 V and 700 mA/mm, respectively, compared with the Planar-nanostrip Schottky gate HEMT. The two-tone measurement indicated that the introduction of MIS structure further improves the linearity performance of the nanostrip-channel HEMT. The degradation in maximum g_m and f_T can be suppressed by applying high-k material as gate insulator in the future.

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Chapter 6 Conclusions and recommendations for future work

6.1. Conclusions

GaN HEMTs have demonstrated great performances for high power and high frequency applications due to its outstanding intrinsic electrical properties, such as high electron saturation velocity, high sheet carrier density, and wide band gap, etc. Conventionally, AlGaN with low Al concentration is used for top barrier to form a HEMT structure. The performance of conventional AlGaN/GaN HEMTs has been improved continuously in the past decades. High output power, high operation frequency and low noise figures have been achieved in AlGaN/GaN HEMTs. Recently, novel barrier materials such as InAlN, AlN and InAlGaN have also been demonstrated. Among them, InAlN is especially attractive due to its unique properties. Due to the advantages of lattice-match with GaN, high 2DEG density and smaller InAlN barrier layer thickness, InAlN/GaN HEMTs have shown dramatic improvements in high frequency performance in recent years. Another area which attracted a lot of interests is GaN HEMTs on silicon substrates. Use of large size Si substrate makes it possible for GaN HEMTs to be fabricated in high-volume and low-cost, which is critical for the commercialization of such devices. A lot of efforts have been made on the development of epitaxial growth of GaN on Si substrate and great progresses have been made. Crack-free AlGaN/GaN HEMT structure can be grown on large diameter (e.g. 200 mm) Si substrate with low value of wafer bowing and low dislocation densities.

However, despite all these significant improvements, there are still other critical issues facing GaN HEMTs. One key issue is that the performance of GaN HEMTs reported on low-cost Si substrate still lags behind that on SiC substrate. The other one is that the poor linearity performance of GaN HEMTs especially for sub-100 nm gate limits its application at high gate bias condition. This thesis addresses these two key issues regarding the GaN HEMTs for RF application.

Firstly, in order to obtain high operation frequency in GaN HEMTs on Si substrate, delay components of the devices have been analyzed in detail. It has been clarified that the fundamental strategy to overcome intrinsic limitation of GaN HEMT device is to scale down the gate and maintain good gate modulation efficiency. For the extrinsic delay, sheet resistance of heterostructure and ohmic contact resistance between ohmic metal and 2DEG are the most concerned parameters. Extrinsic delay is closely related to device design including gate geometry and heterostructure properties. Passivation also has influence on extrinsic delay through introducing gate fringing capacitance.

Based on the theoretical analysis, a deeply scaled GaN HEMT structure with thin InAlN lattice matched top barrier on Si substrate has been put forward. The combination of deeply scaled gate and channel help to decrease both intrinsic and parasitic charging delay through lowering intrinsic gate capacitance and access resistance. The use of thin InAlN top barrier instead of conventional AlGaIn not only resulted in improved gate modulation efficiency, lower ohmic contact resistance and higher current drivability, but also has the potential for highly reliable application of GaN HEMTs due to absence of strain between InAlN and GaN interface. The use of Si substrate is preferred for commercialization of the devices due to low cost.

Electron beam lithography (EBL) technology was introduced. Sub-100 nm gate and sub-micron channel have been developed based on the EBL system. Maximum f_T of 250 GHz was successfully obtained in a 40-nm gate device, higher than any other GaN HEMTs demonstrated on Si substrate previously. The achieved f_T performance of our device is comparable with that on SiC with similar geometry, which indicates the great potential of GaN HEMTs on Si for high frequency and low cost application. 10 nm Al_2O_3 as surface passivation was performed. The effects on DC and RF performance were also investigated. Current collapse was greatly suppressed while speed degradation was observed.

In this work, the mechanisms of the poor linearity performance of the g_m and f_T at high gate bias were also clarified. It has been proven that this problem is caused by extrinsic device limiting elements of highly scaled GaN HEMTs rather than the intrinsic limitation of GaN HEMTs device. To overcome the poor linearity in GaN HEMTs, a novel planar-nanostrip GaN HEMTs structure using ion implantation technology was developed to improve the linearity performance and maintain f_T at a high level without introducing too much gate parasitic capacitance. Novel fabrication techniques were developed including Arsenic ion implantation for isolation application, nanostrip-channel formation using HSQ-PMMA self-aligned and SiO_2 -PMMA approaches. Moreover, the planar-nanostrip device also showed much improved maximum drain current I_{dmax} up to 2.6 A/mm, which is close to theoretical expectation. Also, device geometries including line-to-space ratio of the nanostrip-channel and gate-to-source distance have been studied. These results do not only identify the origins of the non-linear performance in GaN HEMTs, but also

provides good guidelines for designing GaN HEMTs with improved RF performance for high linearity applications.

Moreover, to overcome the high gate leakage current in Schottky-gate GaN HEMT, a Planar nanostrip-channel $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMT on a Si substrate with improved g_m and f_T linearity has been demonstrated. Benefiting from the 6 nm Al_2O_3 gate insulator, the gate voltage and drain current swing of the MISHEMT device increased by 3 V and 700 mA/mm, respectively, compared with the Planar-nanostrip Schottky gate HEMT. The two-tone measurement indicated that the introduction of MIS structure further improves the linearity performance of the nanostrip-channel channel HEMT. The degradation in maximum g_m and f_T can be suppressed by applying high-k material as gate insulator in the future.

6.2. Key contributions of this work

The motivation of this thesis is to clarify the limiting factors of GaN HEMTs for high frequency and high linearity applications and develop novel devices to overcome those limitations. The key contributions of this work are listed as follow.

- An InAlN/GaN HEMT with 40 nm rectangular gates and 300 nm source-to-drain distances was fabricated on Si substrates. The device exhibited a high drain current of 2.66 A/mm, a transconductance (g_m) of 438 mS/mm and a high current gain cut-off frequency (f_T) of 250 GHz. This is the highest f_T value reported so far for GaN based transistors on Si. An effective electron velocity of 1.1×10^7 cm/s was extracted which is comparable to those reported for InAlN/GaN HEMTs on

SiC. These excellent results indicate that GaN HEMTs on Si have a great potential for low-cost emerging mm-Wave applications.

- A novel InAlN/GaN HEMT with a planar nanostrip channel design to improve its transconductance g_m and cut-off frequency f_T linearity was demonstrated for the first time. The planar nanostrips were formed by partial arsenic ion implantation isolation in the channel under the gate. Devices with a gate length (L_g) of 80 nm and a source-to-drain distance (L_{sd}) of 1 μm were fabricated. It was observed that the nanostrip and nanowire channel structures can both suppress the access resistance increase at the high output current level, and thereby improve the device's g_m and f_T linearity. Compared to the one using etching to form a fin-like nanostrip channel, the GaN HEMT with a planar nanostrip channel has demonstrated reduced parasitic capacitance and improved RF performance.
- A 100 nm-gate $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ metal-insulator-semiconductor MISHEMT with a planar nanostrip-channel was fabricated on a Si substrate and its DC, small-signal RF and two-tone intermodulation characteristics were measured. The use of a planar nanostrip-channel and MIS structure allows these devices to have close to 10 dB better intermodulation distortion (IMD) than traditional InAlN/GaN high electron mobility transistors (HEMTs). In addition, the GaN planar nanostrip-channel MISHEMT shows five orders of magnitude lower gate current I_g , 30% higher current drivability and much improved g_m and f_T gate voltage swing than a planar nanostrip-channel GaN HEMT with a Schottky-gate. This allows the planar nanostrip-channel GaN MISHEMT to be able to operate at

higher input gate voltage (more than $V_{g=+4}$ V) and achieve higher output current with better linearity performance.

6.3. Recommendations for future work

So far, the solutions for some of the main challenges to obtain high frequency and high linearity GaN HEMTs on Si substrate have been addressed in this thesis. In spite of the excellent results demonstrated in this work, there are still several areas which can be improved, which are:

- The maximum operation frequency of InAlN/GaN HEMTs on Si can be further increased by applying a shorter gate length and source-to-drain distance (the shortest L_g and L_{sd} reported for GaN HEMTs on SiC is 20 nm and 100 nm using a self-align approach), and/or adoption of other advanced technologies, such as regrown n^{++} GaN for ohmic contact.. For example, by further scaling down L_g to 20 nm and L_{SD} to 150 nm, and adopting regrown n^{++} GaN ohmic contact ($R_c \sim 0.1 \Omega \cdot \text{mm}$), it is projected that a much higher f_T of 440 GHz can be achieved, which is very close to the best value reported on SiC (454 GHz).
- The effects of device geometry in the Planar nanostrip-channel device on the linearity and device speed can be further studied to give clearer direction for the device design. Also, such devices can be combined with T-shaped gate with short gate foot print to achieve high power performance as well as high linearity at higher operation frequency.
- To suppress the g_m and f_T degradation in the GaN MISHEMT, a high-permittivity (high-k) insulating material such as HfO_2 ($k_{ox} \sim 20\text{--}25$) or ZrO_2 ($k_{ox} \sim 23\text{--}30$)

can be applied as the gate insulator instead of Al_2O_3 ($k_{\text{ox}} \sim 9$). With a high-k gate dielectric, the gate leakage can be effectively lowered and at the same time the drop in g_m and f_T can be reduced.

List of Publications

Journal Papers:

1. **W. Xing**, Z. Liu, H. Qiu, G. I. Ng and T. Palacios, “Planar-Nanostrip-Channel InAlN/GaN HEMTs on Si With Improved g_m and f_T Linearity” IEEE Electron Device Lett, vol. 38, no. 5, pp. 619–622, May. 2017. DOI: [10.1109/LED.2017.2689810](https://doi.org/10.1109/LED.2017.2689810).
2. **W. Xing**, Z. Liu, H. Qiu, K. Ranjan, Y. Gao, G. I. Ng and T. Palacios, “InAlN/GaN HEMTs on Si With High f_T of 250 GHz,” IEEE Electron Device Lett, Nov. 2017. DOI: [10.1109/LED.2017.2773054](https://doi.org/10.1109/LED.2017.2773054).
3. **W. Xing**, Z. Liu, H. Qiu, K. Ranjan, G. I. Ng and T. Palacios, “Planar Nanostrip-Channel Al₂O₃/InAlN/GaN MISHEMTs on Si with Improved Linearity,” IEEE Electron Device Lett. Accepted.
4. Y. Li, G. I. Ng, S. Arulkumaran, Z. H. Liu, K. Ranjan, **W. C. Xing**, K. S. Ang, P. P. Murmu, and J. Kennedy, “AlGaIn/GaN High electron mobility transistors on Si with sputtered TiN gate”, *Physica Status Solidi (a)*, Vol. 214, No. 3, pp. 1600555, Mar. 2017. DOI: [10.1002/pssa.201600555](https://doi.org/10.1002/pssa.201600555).

Conference Papers:

1. **W. Xing**, Z. Liu, G. I. Ng and T. Palacios, “Temperature dependent characteristics of InAlN/GaN HEMTs for mm-wave applications,” 8th International Conference on Materials for Advanced Technologies (ICMAT), Singapore, Jun. 2015.

2. **W. Xing**, Z. Liu, G. I. Ng and T. Palacios, “Planar-Nanostrip-Channel InAlN/GaN HEMTs on Si with Improved g_m and f_T Linearity” International Workshop in Nitride Semiconductors (IWN 2016), Orlando. USA. October. 2016.
3. **W. Xing**, Z. Liu, G. I. Ng and T. Palacios, “Fin-like Nanowire InAlN/GaN MISHEMTs on Si with Improved g_m and f_T Linearity” International Conference on Nitride Semiconductors (ICNS 2017), Strasbourg, France. July. 2017.
4. **W. Xing**, Z. Liu, G. I. Ng and T. Palacios, “Fin-like nanowire-channel InAlN/GaN HEMTs on Si with Improved g_m and f_T Linearity,” 9th International Conference on Materials for Advanced Technologies (ICMAT), Singapore, Jun. 2017.
5. Z. Liu, C. C. Huang, **W. Xing**, C. Fahle, M. Heuken, G. I. Ng and T. Palacios, “Si ion implantation and activation in NH₃ for CMOS-compatible fabrication of GaN HEMTs on Si substrates,” International Conference on Nitride Semiconductors (ICNS), Sept. 2015, Beijing, China.
6. Z. Liu, C. C. Huang, D. Fahle, **W. Xing**, M. Heuken, G. I. Ng and T. Palacios, “Si ion implantation technology to reduce the access resistance in GaN HEMTs on sapphire and Si substrates,” International Symposium of Compound Semiconductors (ISCS), Jun. 2015, Santa Barbara, USA.
7. Z. Liu, **W. Xing**, H. Hou, C. C. Huang, G. I. Ng, and T. Palacios, “600 V GaN MOSHEMTs Fabricated on a 200 mm-Diameter 725 mm-Thick Si(111) Substrate using CMOS-Compatible Process,” International Workshop on Nitride semiconductors (IWN), Oct. 2016, Orlando, USA.