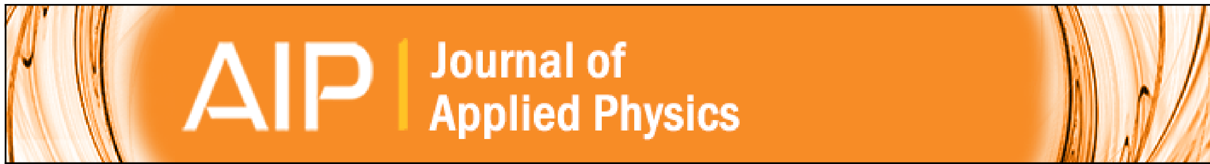

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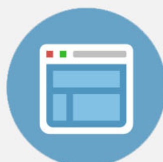
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Characterization of thin-film GaAs diodes grown on germanium-on-insulator on Si substrate

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In this study, we report the characterization of thin-film GaAs grown on germanium-on-insulator (GeOI) on Si substrate. A GaAs/GeOI diode with a 600 nm buffer layer showed a rectification of 1.0×10^7 at ± 2 V and had an electrical performance similar to that of the reference sample grown on GaAs substrate. We demonstrate two thin diodes (<350 nm in thickness) that still showed high forward densities and rectification properties. The electrical performances of the diodes degraded as the diode active regions were grown closer to the GaAs/Ge interface due to the increase of defects propagating into the active regions. The experimental results were fitted with the thermionic emission equation and the Frenkel-Poole model. © *2012 American Institute of Physics.*
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I. INTRODUCTION

III-V direct monolithic integration with Si has attracted considerable attention because of its strong potential industry applications. Achievements in this area will bring about unprecedented opportunities to produce high performance devices using the low-cost silicon manufacturing infrastructure. These devices include optoelectronics integrated circuits, on-chip optical interconnects, Si photonics, and memory devices.

To overcome the large lattice mismatch (~4.1%) and the large difference in the thermal expansion coefficient (~110%) between GaAs and Si, GaAs has been grown on a Ge virtually terminated layer through either a compositionally graded $Si_{1-x}Ge_x$ layer or a germanium-on-insulator (GeOI) on Si substrate (GeOI/Si), since there is a small lattice mismatch (~0.08%) and close thermal expansion coefficients between GaAs and Ge.[1,2] It has also been reported that growing a thick GaAs buffer layer suppressed the propagation of threading dislocations from the GaAs/Ge interface.[3] However, for logic device applications, a thinner III-V layer thickness is desirable for lower cost and higher density integration. Thus, the quality of thin GaAs grown on a Ge layer is important.

In this paper, we present characterization of several thin-film GaAs epitaxial structures (within a few hundred nanometers) grown on GeOI/Si. The tested GaAs/GeOI/Si diode devices showed high forward current densities and rectifying ratios.

II. EXPERIMENT PROCEDURE AND DEVICE FABRICATION

The GaAs epitaxial layer was grown by the solid-source molecular beam epitaxy (MBE) technique on GeOI/Si substrate. The substrate consisted of a 70 nm un-doped Ge 10° off-cut toward the $\langle 111 \rangle$ plane on top of a 1 μm SiO_2 on the Si host substrate. The GeOI/Si substrate was cut into a 2 cm $\times$ 2 cm area and treated by rinsing in HF (HF:H_2O in 1:10 ratio) and washing in running de-ionized water followed by H_2O_2 (H_2O_2:H_2O in 1:10 ratio). This process etched off the native oxide layer and formed a new oxide layer on the Ge surface.[4] The cleaned substrate was carried in a vacuum holder and was loaded into the MBE UHV chamber. The substrate was degassed at 350 °C in the preparation chamber. Surface oxide was desorbed at 640 °C, and the substrate was *in situ* annealed at 680 °C in the growth chamber. The formation of double-atomic surface steps on the Ge surface was observed from the RHEED pattern. A 10-monolayer migration-enhanced epitaxy (MEE) of GaAs was first grown at a low temperature as a seeding layer.[1] The GaAs junction was grown at a standard MBE growth temperature of 580 °C at 1 μm/hr. The tested epilayer structures are shown in Table I. The *p*-type contact layer was doped with Be with a concentration of 1.3×10^{19} cm^{-3}, and the *n*-type contact layer was doped with Si with a concentration of 6.6×10^{18} cm^{-3}.

The devices were fabricated using the standard dry etch and photolithography techniques. Ti/Au was used for the *p*-contact metallization and Ni/Ge/Au was used for the *n*-contact for all samples except for Sample A, which had an additional $In_{0.2}Ga_{0.8}As$ layer to enable Ti/Au metallization on top of the *n*-type GaAs. After forming the contacts, the devices were isolated by etching down to the SiO_2 layer. The diode junction has an area of 1.45×10^{-4} cm^{-2} (Fig. 1).

III. DEVICE CHARACTERIZATION

A. Surface morphology

Figure 2(a) and the inset of Fig. 2(b) show the cross-sectional transmission electron microscopy (X-TEM) from

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TABLE I. Epilayer structures (indicated with nominal thickness).

Structure	Sample A	Sample B, C, D	Sample E	Sample F
Cap layer	InGaAs: Si (6.6×10^{18} cm^{-3}) 15 nm	…	…	…
Diode	GaAs: Si (6.6×10^{18} cm^{-3}) 100 nm	GaAs: Be (1.3×10^{19} cm^{-3}) 100 nm	GaAs: Si (6.6×10^{18} cm^{-3}) 20 nm	GaAs: Si (6.6×10^{18} cm^{-3}) 20 nm
	GaAs: Si (5×10^{16} cm^{-3}) 250 nm	GaAs: Be (1.3×10^{16} cm^{-3}) 200 nm	GaAs n.i.d. 150 nm	GaAs n.i.d. 100 nm
	GaAs: Be (1.3×10^{19} cm^{-3}) 400 nm	GaAs: Si (6.6×10^{18} cm^{-3}) 400 nm	GaAs: Be (1.3×10^{19} cm^{-3}) 180 nm	GaAs: Be (1.3×10^{19} cm^{-3}) 80 nm
Buffer layer	GaAs n.i.d 600 nm	GaAs n.i.d B: 200 nm C: 100 nm D: 50 nm	…	…
Substrate		GeOI/Si		

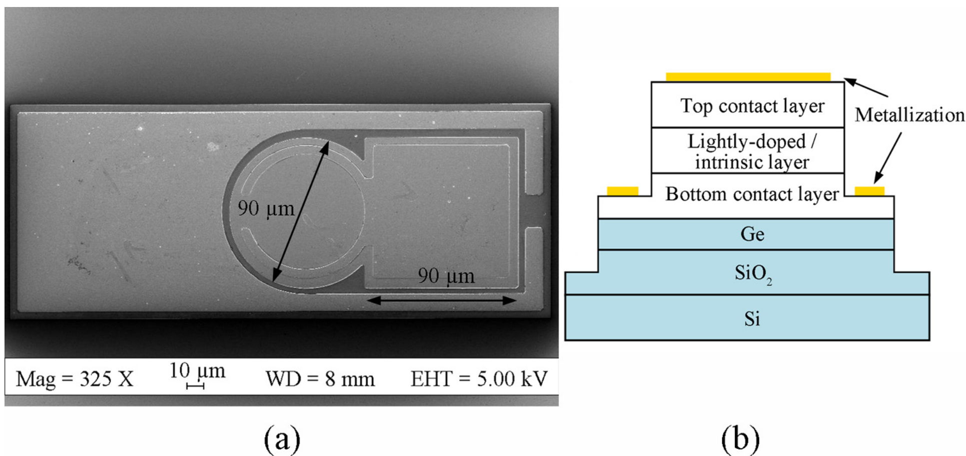

FIG. 1. (Color online) (a) A photograph of the top-view of a GaAs on GeOI/Si diode with a mesa diameter of 90 μm and a top contact size of 90 μm × 90 μm. (b) A diagram of the diode's cross-sectional view.

two GaAs/GeOI samples. The anti-phase domains (APDs) were observed and self-annihilated within ~100 nm from the GaAs/Ge interface. Tanoto *et al*. reported that the APDs will mostly be confined in the ⟨111⟩ plane and the rest will be self-annihilated in pairs.[1] Therefore, we should expect few APDs to propagate into the active region, since this region is far away from the GaAs/Ge interface.

Figure 2(b) shows the plane-view of the scanning electron microscopy (SEM) image of Sample F with a total GaAs thickness of 200 nm. The V-groove patterns were

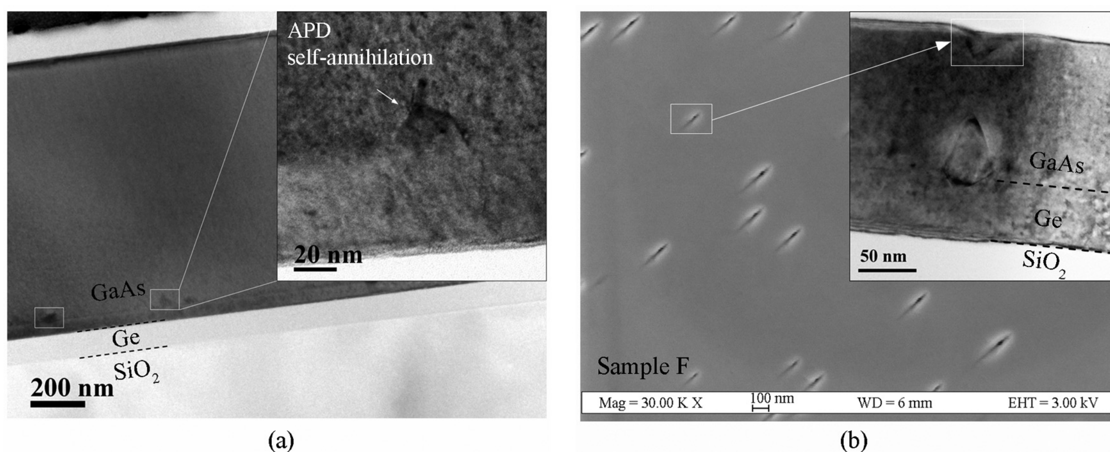

FIG. 2. (a) An X-TEM image of GaAs on GeOI/Si calibration sample. (b) A plane-view SEM image of Sample F (Inset: X-TEM image of Sample F).

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observed on the surface, and they are possibly the signs of thread dislocations. A similar observation was reported by Bordel *et al*. in Ref. 2. Based on the scanned sample, the estimated thread dislocation density (TDD) on the Sample F surface was about $3 \times 10^8/\text{cm}^2$.

B. Current-voltage characteristics

Current density–voltage (J-V) characteristics were measured with Agilent Precision Semiconductor Parameter Analyzer HP4156B. Sample A consisted of a 600 nm GaAs buffer and a 400 nm bottom contact layer, which effectively separated the diode active region further away from the GaAs/Ge interface. Sample A started a soft reverse breakdown from −8 V and it broke down at around −9 V, which was close to that of the reference sample with the identical epilayer structure grown on a GaAs substrate (Fig. 3(a)). The rectification of Sample A was 1.0×10^7 at ±2 V.

Samples B, C, and D had a reduced GaAs buffer thickness, and their polarity was inverted. The breakdown voltage decreased from −7.8 V in Sample B to −5.8 V in Sample D, as shown in Fig. 3(b). Consequently, an increase in the leakage current levels was observed as the GaAs buffer layer was reduced. Hence, the rectification current ratios were reduced. Sample D (the worst case in the second series) showed a forward current density of 135 A/cm^2 at +2 V and a rectification of 6.2×10^3 at ±2 V.

Compared to the previous samples, Samples E and F eliminated the dedicated GaAs buffer layer. To maintain a relatively low reverse current, a non-intentionally doped (n.i.d.) layer was used. At +2 V, the forward current densities were 448 A/cm^2 and 350 A/cm^2 for Samples E and F, respectively (Fig. 3(c)). The increase in the forward current densities was due to the reduction of the thickness of the contact layers. Theoretically, a higher forward current density could be achieved with such high doping levels and thin epilayers. The loss in the forward current density was attributed to the carrier recombination, and this agreed with the calculated ideality factor shown in Sec. III C.

As the diode active region formed closer to the GaAs/Ge interface, both diodes exhibited higher leakage current levels. At ±2 V, the rectifications were 2.1×10^2 and 42 for Samples E and F, respectively. The higher leakage current levels are believed to be related to the presence of TDD, since TDD leads to the increase of leakage current density and the reduction of minority carrier lifetime.[5,6]

C. Current conduction analysis

Samples E and F had compact structures grown on GeOI/Si and yet they demonstrated proper rectifying behaviors. The experimental results were fitted with current conduction models. Under the forward bias condition, we neglected any shunt resistance forming an additional conducting path, and the thermionic emission model was found to be sufficient in this case. The thermionic emission equation is given as

$$J = J_{sth}\left[\exp\frac{q(V - R_s J \cdot A_{diode})}{nkT} - 1\right], \qquad (1)$$

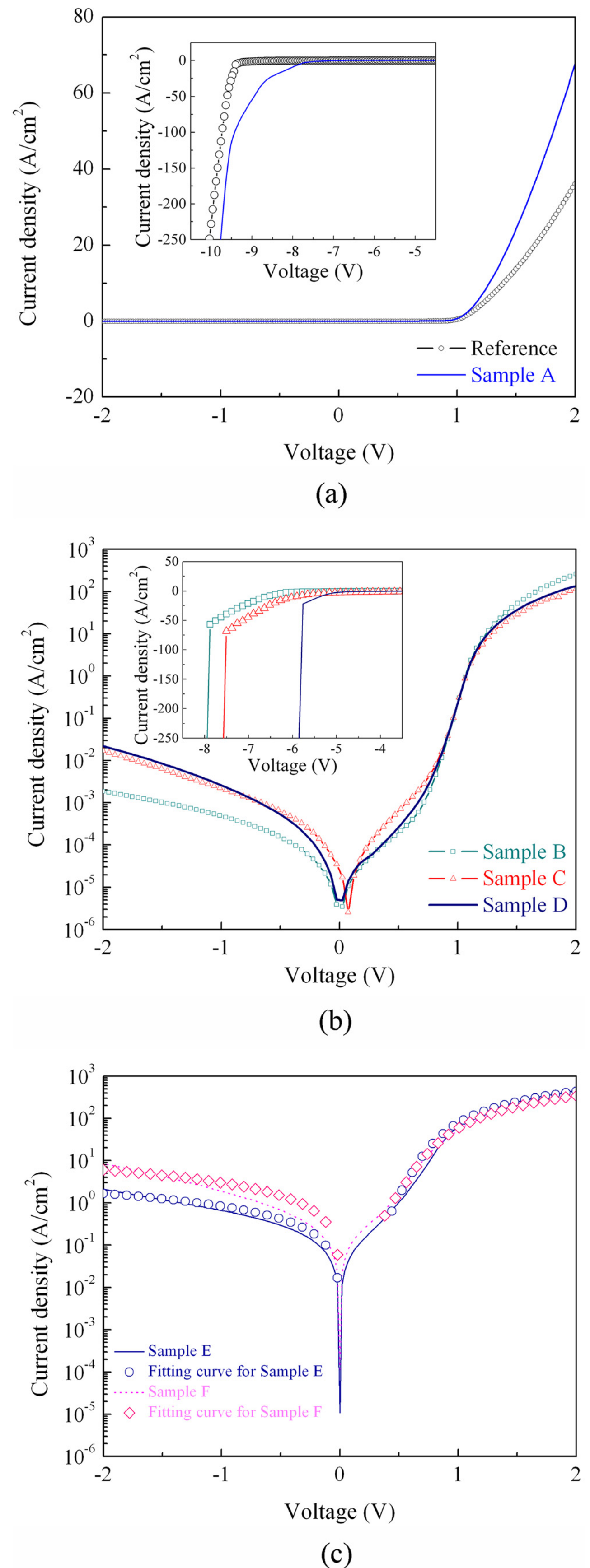

FIG. 3. (Color online) J-V characteristics for (a) Sample A and the reference sample (Inset: Reverse breakdown behavior). (b) Samples B, C, and D with a reduced GaAs buffer layer thickness (Inset: Reverse breakdown behavior). (c) Samples E and F with fitting results.

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TABLE II. Fitting parameters for J-V measurements.

Fitting parameter	Sample E	Sample F
J_{sth}(A/cm^2)	0.00247	0.01
$R_s(\Omega)$	16.6	20.1
n	2.99	3.75
T(K)	304.9	297.6
n_0(cm^{-3})	2.39×10^{15}	1.27×10^{18}
μ(cm^2/(V.s))	4538	3738
φ(V)	0.323	0.441
ε_r	12.2	12.0
W (cm)	9.49×10^{-6}	8.76×10^{-6}

where J_{sth} is the saturation current density, q is the elementary electron charge, R_s is the series resistance consisting of the resistance from the doped layers and the semiconductor/metal contact, k is the Boltzmann constant, n is the ideality factor, A_{diode} is the diode junction area, and T is the ambient temperature, which was around room temperature.

Under the reverse bias condition, practical diodes do not ideally have constant reverse currents as $-J_{sth}$, and their leakage current has to be taken into consideration. A correlation between the leakage current density and TDD has been reported, and the defect states related to the threading dislocations caused a higher leakage current density.[5,7,8] In this approach, the reverse bias–dependent leakage current was calculated by the Frenkel-Poole model,[9,10] given as

$$J = \frac{qn_0\mu V}{W}\exp\left[-\frac{q}{kT}\left(\phi - \sqrt{\frac{qV}{\pi\varepsilon_r\varepsilon_0 W}}\right)\right], \qquad (2)$$

where n_0 is the trap density, μ is the mobility, ϕ is the barrier height, ε_r is the semiconductor relative permittivity, ε_0 is the permittivity in vacuum, and W is the depletion width, which was assumed to be close to the nominal thickness of the non-intentionally doped layer.

The fitted curves are plotted in Fig. 3(c), and the fitting parameters are shown in Table II. For both samples, the ideality factors were larger than 2, which indicated the presence of the recombination mechanism. The recombination current was caused by the threading dislocations in the GaAs layer, particularly in the region across the junction. Furthermore, the fitted trap density (n_0) for Sample F was three orders higher than that of Sample E, which suggests that more threading dislocations propagated into the active region of Sample F, since it was much closer to the GaAs/Ge interface. Although the APDs seen in the TEM image self-annihilated within 100 nm from the GaAs/Ge interface, they could affect the active region by the APD-induced local electric field that leads to a large leakage current density and to premature breakdown behavior.[11] From Eq. (1), an even higher forward current density is expected if the device area (A_{diode}) is further reduced.

IV. CONCLUSION

In conclusion, we have characterized several GaAs diodes on GeOI on Si substrate. By reducing the thickness of the GaAs layer, the tested diodes exhibited a higher leakage current and a smaller breakdown voltage. These were mainly due to the presence of conductive dislocations in the active region. Two compact GaAs diodes had total thicknesses of 350 nm and 200 nm, showed high forward current densities of 448 A/cm^2 and 350 A/cm^2, and showed rectifications of 2.1×10^2 and 42 at ± 2 V, respectively. The current–voltage experimental results were fitted using the thermionic emission equation and the Frenkel-Poole model.

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