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TOPICAL REVIEW

Recent Development of High-PCE CMOS RF-DC Rectifier With Wide P_{IN} Dynamic Range: Strategies and Trends–Review

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ABSTRACT This review explores the various strategies used to widen the input power (P_{IN}) dynamic range of an RF-DC rectifier and analyzes the recent developments reported in the literature. This development is insightful as the P_{IN} dynamic range is crucial for systems adopting wireless power transfer (WPT) or wireless energy harvesting (EH) for both near- and far-field applications to mitigate the reliance on the battery as its primary power source. However, the RF-DC rectifier exhibits non-linear characteristics, resulting in a narrow P_{IN} band for reasonable power conversion efficiency (PCE). The different strategies reported in the literature are discussed and classified into three main concepts: reconfigurable, multi-path, and self-biased rectifiers. Despite having different design constraints and considerations during the inception of the reported work in the literature, this article analyzes and provides the general development trend, merits, and demerits.

INDEX TERMS CMOS, energy harvesting, wireless power transfer (WPT), RF-DC converter, rectifier, efficiency, dynamic range, sensitivity, power conversion.

I. INTRODUCTION

Over the years, there has been a steady demand and uptake of Internet-of-Things (IoT) devices [1]. These devices range from wearable for consumers, such as smartwatches, to industrial radio frequency identification (RFID) tags used in logistic tracking. Many industries and businesses use IoT to understand consumer behavior better, anticipate market shifts, and increase productivity with automation. However, there is still a reliance on the battery as the primary power source, which limits the form factor of the IoT device and incurs high maintenance costs due to periodical battery replacement.

Harvesting radio frequency (RF) energy is a promising alternative towards achieving a battery-less system. However, such systems are plagued by many losses, such as free-space path loss and obstacle obstruction in far-field applications [2]. Despite these losses being of lesser concern in the near field, the system's front-end consists of a rectifier with non-linear characteristics, exhibiting severe power conversion efficiency (PCE) performance degradation and limited input power (P_{IN}) dynamic range. Despite the low RF power density [3], [4] and a slew of losses, the ease of integration in standard CMOS technology and system scalability makes it highly attractive.

The Dickson rectifier and the complementary cross-coupled rectifier are the two most popular topologies found in many RF energy harvesting (RFEH) applications due to their simplicity [5]. The diode voltage (V_{DIODE}) in the Dickson

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rectifier results in poorer sensitivity and lower achievable PCE_{PEAK} [6], [7]. In the CMOS implementation of the Dickson rectifier, the diode-configured transistor will incur a threshold voltage (V_{TH}) drop instead of V_{DIODE}. In contrast, the cross-coupled rectifier has demonstrated remarkable sensitivity and achieved a higher PCE_{PEAK} [8]. However, compared to the Dickson rectifier, the cross-coupled rectifier suffers from a series of losses due to the bidirectional conduction characteristics of the CMOS transistors. These losses are primarily the reverse conduction (P_{REV}) loss due to the reverse conduction current (I_{REV}) and the shoot-through loss (P_{SHOOT}) due to the shoot-through current (I_{SHOOT}) [9]. Particularly, I_{REV} occurs when the output voltage (V_{OUT}) is larger than the voltage-boosted RF input (V_{RF}). On the other hand, due to the inherent cross-coupled inverter structure, I_{SHOOT} occurs when $V_{OUT} > V_{THN} + |V_{THP}|$ where V_{THN} and $|V_{THP}|$ are the V_{TH} of NMOS and PMOS, respectively. In this condition, PMOS and NMOS experience simultaneous conduction during V_{RF} transition, resulting in I_{SHOOT}. I_{REV} and I_{SHOOT} manifest during high P_{IN} operation, leading to rapid PCE degradation and a narrow P_{IN} dynamic range.

There are several design strategies and circuit techniques to provide a wide P_{IN} dynamic range while preserving high PCE and sensitivity. However, there are no clear deciding factors on their merits and demerits when choosing the optimal strategies for a given application. Hence, a more quantitative review is necessary to provide a design reference and guideline when given certain design constraints.

This review article overviews the various strategies and techniques to widen the P_{IN} dynamic range. The merits and demerits of the different classes will be discussed. In Section II, a brief overview of the two primary types of rectifier is discussed; Section III provides the common performance metrics for the rectifier; from Section IV to Section VII, the different techniques employed by different classes to achieve a wide P_{IN} dynamic range are reviewed; Section VIII explores the current trend and the impact of the different strategies class; Section IX concludes this review article.

II. RECTIFIER TOPOLOGIES OVERVIEW

A. DICKSON RECTIFIER

The Dickson rectifier in Figure 1 was demonstrated in the '70s by Dickson [10]. In recent times, due to the practicality and simplicity of the Dickson rectifier, it has commonly been found and implemented in various charge pump and voltage doubler circuitry [11], [12], [13], [14], [15], [16]. The coupling capacitor C_1 charges during $V_{RF} < -V_{DIODE}$ through D_1 and functions as a doubler during $V_{RF} > V_{DIODE}$ through D_2 to transfer the charges to C_L to generate $V_{OUT} = 2(|V_{RF}| - V_{DIODE})$. The unidirectional current conduction in a fast-switching diode prevents a sizeable I_{REV} from discharging the C_L, thereby achieving half-wave rectification [17].

This design is commonly used in high V_{RF} design when V_{DIODE}, typically 0.7 – 1V, is tolerable as it imposes a

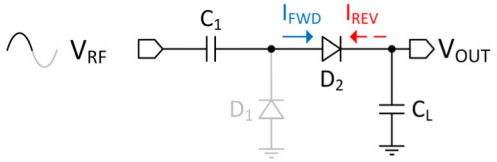

FIGURE 1. A single unit dickson rectifier.

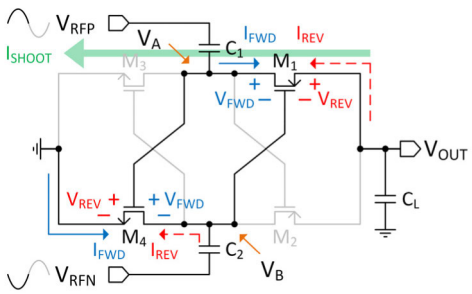

FIGURE 2. A single unit complementary cross-coupled rectifier.

$|V_{RF}|_{(MIN)} = V_{DIODE}$. As such, the Dickson rectifier needs a greater number of stages to meet the required V_{OUT} while also suffering from a lowered PCE due to the inherent dropout voltage V_{DIODE}. To overcome this undesirable V_{DIODE}, the Schottky diode with a lower V_{DIODE} and faster reverse recovery time (t_{rr}) is utilized to improve the PCE [17]. However, the modelling of the non-linear performance for the required Schottky diode is non-trivial for high-frequency design [18]. For example, the injection of the minority carriers from the PN junction form by the guard ring to the Schottky diode may not be sufficiently modelled in its simulation model [19]. This injection leads to an increase in t_{rr} and, consequentially, an increase in loss for the high-frequency rectifier. The Dickson rectifier can also be implemented with CMOS and has the V_{TH} compensated for improved sensitivity and PCE performance [20], [21], [22], [23], [24], [25], [26], [27]. However, by introducing the compensating voltage, it weakly biases the diode-configured CMOS devices in an on-state, which provides a leakage path during the transition of V_{RF} when $V_{OUT} > V_{RF} + V_{C1}$ and diminishes the PCE improvement.

B. CROSS-COUPLED RECTIFIER

The complementary cross-coupled MOS rectifier in Figure 2 utilizes the differential-ended input V_{RFP} and V_{RFN} to provide full-wave rectification when $V_{RFP} > V_{RFN}$ ($\varphi 1$) and also during $V_{RFP} < V_{RFN}$ ($\varphi 2$). It was demonstrated in [8] and [28] that this rectifier can achieve a high PCE with a lower sensitivity for high-frequency applications. The sensitivity for this structure was also demonstrated in [29] with a 7-stage cross-coupled rectifier operating in a subthreshold region ($< |V_{THP}|$) and can generate a V_{OUT} of 1V with a PCE of 42.3% for 10kΩ load at a P_{IN} of –6dBm. The $V_{OUT} = 2(|V_{RFP}| - V_{DS,M1}) \approx 2|V_{RFP}|$ can be achieved theoretically with a small dropout voltage $V_{DS,M1}$ and $V_{DS,M2}$ from the switch on-resistance $r_{ON,M1}$ and $r_{ON,M2}$.

There are various loss mechanisms associated with this rectifier structure. These loss mechanisms are the P_{REV}, the P_{SHOOT}, the subthreshold leakages (P_{LEAK}), and the parasitic capacitance coupling efficiency [9]. The losses exhibit a non-linear characteristic, which is exacerbated at higher P_{IN}, leading to a narrower PCE profile due to a rapid PCE degradation. The bidirectional characteristic of the MOSFET contributes to the P_{REV}; as such, when $V_{OUT} > V_{A,\varphi 1}$ and $V_{REV,\varphi 1} = V_{OUT} - V_{B,\varphi 1} > |V_{THP,MP1}|$, M_1 provides a discharging path and depletes the charges stored in C_L and reduces V_{OUT}. On the other hand, when $V_{B,\varphi 1} > V_{SS}$ and $V_{A,\varphi 1} - V_{SS} > V_{THN,M4}$, M_4 discharges the charges stored in C_2 and reduces the benefit of the voltage boosting provided by the C_1 and C_2. Furthermore, during the transition of V_A and V_B, and when $V_{OUT} > |V_{THP}| + V_{THN}$, both the PMOS and NMOS can still be biased in the conducting region, resulting in a P_{SHOOT}. The PCE degradation at high P_{IN} is severe due to these losses. To address these losses, various bias techniques discussed in Section VII are commonly implemented to modulate the overdrive voltage.

III. PERFORMANCE METRICS

A. POWER CONVERSION EFFICIENCY (PCE)

The PCE metric effectively determines the ability to transfer the P_{IN} to the output. The PCE is determined by the ratio between the output power (P_{OUT}) typically delivered to an equivalent resistive load (R_{LOAD}) emulating the actual load and the effective P_{IN} to the rectifier as follows:

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}^2/R_{LOAD}}{P_{IN}} \tag{1}$$

While it is true that the overall system efficiency is also dependent on the matching network preceding the rectifier, the PCE of the rectifier can be characterized by de-embedding the reflected power and losses from the test setup to determine the P_{IN} (dBm) as follows:

$$P_{IN} - P_{SOURCE} - L_{INSERT} + 10log(1 - |S_{11}|^2) \tag{2}$$

where P_{SOURCE} (dBm) is the output power from the test equipment, L_{INSERT} (dB) is the insertion loss from the test setup, and S_{11} is the measured reflected s-parameter of the rectifier input.

B. INPUT POWER (P_{IN}) DYNAMIC RANGE

The P_{IN} dynamic range (dB) measures the ability of the rectifier to maintain a high PCE between two P_{IN}(dBm), as shown in (3). The P_{IN} dynamic range is typically determined for a PCE > 20% (PR #1). However, other characterization criteria are also reported, such as PCE > 30% [30], PCE > 0.8xPCE_{PEAK} (PR #2) [31], [32] and PCE > 0.9 × PCE_{PEAK} [33].

$$P_{IN}\ Dynamic\ Range = P_{IN(MAX)} - P_{IN(MIN)} \tag{3}$$

Regarding system design, evaluating the rectifier for PCE > 0.8xPCE_{PEAK} is more prudent as it provides information on the PCE profile quality.

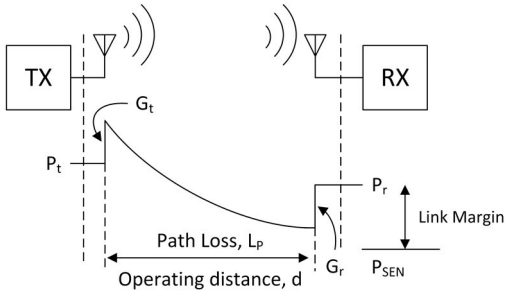

FIGURE 3. Overall system link budget consideration.

C. SENSITIVITY

The sensitivity measures the minimum P_{IN} to generate a V_{OUT} of 1V for an intended load. The intended load varies across publications, with the open load or 1MΩ commonly reported alongside the targeted loading. The open load is useful to determine the ability of the rectifier to establish reasonable V_{OUT} for the system with minimal power consumption, which is typical in sleep mode or at the point of system initialization. On the other hand, it is insightful to emulate the leakage from the storage capacitor and the system in sleep or standby mode using 1MΩ ($I_{LOAD} = 1\mu A$ @ $V_{OUT} = 1V$). The sensitivity at the operating load determines the minimum P_{IN} to sustain the system in typical operating conditions. This sensitivity metric is crucial during the feasibility studies similar to the link budget performed in a wireless communication system to determine the system operating range and link margin (L_{margin}) shown in Figure 3. L_{margin} is the difference between the minimum received power (Pr) and maximum sensitivity at the receiver side. In this case, the maximum sensitivity at the receiver refers to the sensitivity of the rectifier. For instance, when there is a $L_{margin} = 3$dB, the RFEH system can endure an additional uncertainty in the transmission link or performance degradation due to the rectifier.

D. LINK BUDGET FOR FEASIBILITY STUDIES

A sufficient link budget can be established during the RF energy harvester conceptualization stage as follows:

$$P_{SEN} = P_t + G_t - L_p + G_r - L_{margin} \tag{4}$$

where P_{SEN} is the rectifier sensitivity (dBm), P_t is the transmitter P_{OUT} (dBm), G_t is the transmitter antenna gain (dBi), L_p is the free-space path loss (dB), G_r is the receiver antenna gain (dBi), and L_{margin} is the link margin (dB). L_p can be determined as follows:

$$L_p = \left(\frac{4\pi fd}{c}\right)^2 \tag{5}$$

where f is the transmitted frequency, d is the distance between the transmitter and receiver, and c is the speed of light.

Performing initial link budgeting allows the designer to 1) determine the viability of the system given a set of constraints and 2) study the required specification of the

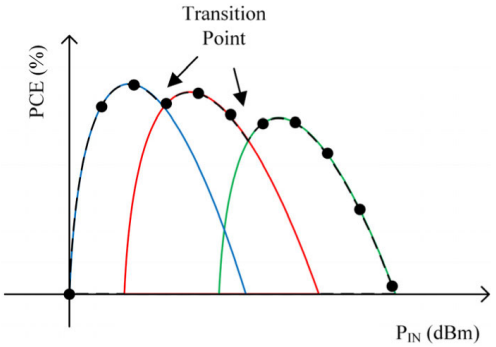

FIGURE 4. General concept of different strategy by superimposing different PCE profiles and selecting at appropriate P_{IN}.

functional blocks. As an example, the following assumptions are made:

- The transmission source provides $P_t = 20$dBm
- The antenna on the transmit side has $G_t = 3$dBi
- The antenna on the receive side has $G_r = 3$dBi

There are two trains of thought for the analysis to consider. Firstly, given an operating distance d, the required P_{SEN} can be determined and used as an initial specification during the design of the rectifier. For example, to operate at d = 8m, the rectifier needs a $P_{SEN} = -23.6$dBm or lower ($L_{margin} = 0$dB). This calculated P_{SEN} includes the matching network preceding the rectifier. It is common to co-design the rectifier with the matching network as the matching network not only provides the required impedance matching but also introduces a passive voltage boost to assist in lowering P_{SEN}. However, the non-idealities in the matching network also introduce insertion loss and component tolerance, which must be accounted for in the design. As such, a sufficient L_{margin} ensures that the system is resistant to component variation and environmental factors for reliable system operation. Secondly, in the case of a discrete implementation, it allows the designer to assess the suitability of an existing device for a given set of application-specific constraints. For instance, given a $P_{SEN} = -20$dBm, it can be estimated that a maximum operating distance d = 5.3m for $L_P = -46$dB is plausible.

IV. WIDE P_{IN} RANGE STRATEGIES

Numerous works demonstrated remarkable improvement in PCE, P_{IN} dynamic range, and sensitivity. However, application-specific design constraints and methodologies make it challenging to appreciate the merits and demerits of adopting and choosing those ideas based on the system requirements. This section attempts to classify the literature into three distinct classes. The three classes are, namely, the Reconfigurable Stages (RCS), Multi-path Selection (MPS), and Self-bias Generation (SBG). As illustrated in Figure 4, these three classes achieve a wide P_{IN} dynamic range by reconstructing the desired PCE profile by superimposing a group of narrow P_{IN} band PCE profiles and subsequently selecting the most appropriate PCE profile at a given P_{IN}.

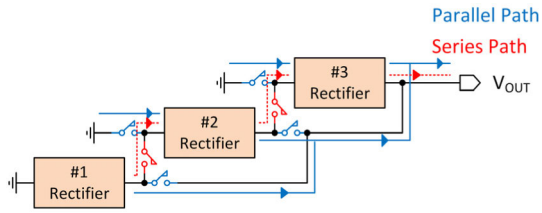

FIGURE 5. Series-parallel reconfigurable rectifier concept.

V. RECONFIGURABLE CAPABILITY STAGES (RCS)

A multi-stage rectifier can be reconfigured to achieve different PCE profiles, as shown in Figure 5. A cascading series of N_{CONFIG}-stage rectifiers provides the necessary V_{OUT} stacking by $N_{CONFIG} \cdot V_{OUT,UNIT}$ while paralleling these N_{CONFIG}-stage rectifiers provides a summation of I_{OUT} by $N_{CONFIG} \cdot I_{OUT,UNIT}$. The series configuration allows a higher V_{OUT} to be generated even at a lower P_{IN}, making it essential for load with minimum V_{DD} requirement [34]. In contrast, the parallel configuration allows lower I_{OUT} per rectifier, resulting in a lower r_{ON} dropout and improving the PCE [35]. One such implementation was demonstrated by [36], [37], and [38] with $N_{CONFIG} = 2$. Auxiliary circuitry is typically required to track the P_{IN} to determine the optimal trip point between the different configurations. V_{OUT} is commonly compared to a reference voltage (V_{REF}) due to the relationship between V_{OUT} and P_{IN}. Two distinct PCE_{PEAK} at two different P_{IN} was reported by [36], and by switching the configuration, a P_{IN} dynamic range of 19dB (-17dBm $< P_{IN} <$ 2dBm) is achieved for a PCE $>$ 20%. A more extensive demonstration by [39] with an $N_{CONFIG} = 4$ with the use of a $N_{UNIT} = 3$ rectifiers results in an $N_{TOTAL} = N_{CONFIG} \times N_{UNIT} = 12$. The $N_{TOTAL} = 12$ stages rectifier by [39] achieved a similar widening of the P_{IN} dynamic range by 2dB compared to the P_{IN} dynamic range of 13dB by an equivalent cross-coupled rectifier.

While this approach generally widens the P_{IN} dynamic range, adding V_{REF} and control circuitry increases the complexity and deteriorates the overall system PCE. One such concern is the availability of V_{REF} during initialization, resulting in the need for an additional supply. Furthermore, the reconfiguration changes the input impedance (Z_{IN}), which leads to varying s-parameter S_{11} performance across the entire P_{IN} dynamic range [40], [41]. As such, [36] demonstrated a co-optimized rectifier with a custom antenna, thereby eliminating the losses from the matching network to achieve high-PCE performance. Besides just configuring N_{CONFIG} for P_{IN} dynamic range, various maximum power point tracking (MPPT) algorithms are used to optimize rectifier output impedance (Z_{OUT}) with the R_{LOAD} [41], [42], [43], [44] or Z_{IN} with the antenna [45]. A DC-DC converter can be implemented to provide a regulated R_{LOAD} to the rectifier [46], [47], [48] to improve the PCE performance. Instead, [49] applies the MPPT on the reconfigurable rectifier to achieve a regulated input to the DC-DC converter while using the DC-DC converter to provide a regulated V_{OUT}.

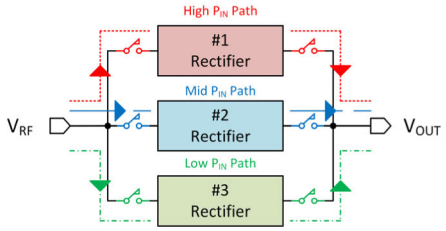

FIGURE 6. Multiple path selection rectifier concept.

Another type of RCS involves the transformation of topology. A cross-coupled rectifier is reconfigured into a partial Dickson rectifier was demonstrated [50]. The cross-coupled rectifier is used for low P_{IN} to maintain high PCE and sensitivity, while the partial Dickson rectifier reduces I_{REV} at high P_{IN}. It achieved a P_{IN} dynamic range of 23dB for a PCE > 20%.

VI. MULTI-PATH SELECTION (MPS)

The PCE profiles depend on the optimization constraint and the choice of rectifier topology. It was reported by [51] that at a particular P_{IN}, the PCE_{PEAK} of the cross-coupled rectifier depends on the V_{TH} and aspect ratio (W/L) of the device. Hence, intuitively, a PCE profile with a wider P_{IN} dynamic range can be achieved by superimposing different PCE profiles with rectifiers under different optimizing constraints and V_{TH}. Figure 6 shows the conceptual principle of a rectifier with multi-path selection with $N_{PATH} = 3$. While any arbitrary N_{PATH} can be implemented conceptually, the increasing complexity of the control circuitry and the necessary P_{IN} awareness algorithm may result in degraded PCE_{PEAK} and sub-optimal transition.

The dual-path rectifier proposed by [51] demonstrated such an $N_{PATH} = 2$ implementation with two distinct PCE_{PEAK} resulting from a low-power path rectifier which has a $PCE_{PEAK,1} = 32.5\%$ at $P_{IN,1} = -15$dBm and a high-power path rectifier which has $PCE_{PEAK,2} = 35\%$ at $P_{IN,2} = -9.5$dBm. As expected, the transition from this implementation was sub-optimal, transiting at a P_{IN} of –10.5dBm instead of the optimal P_{IN} of –12.5dBm. Furthermore, due to the unavailability of a reliable V_{DD} supply, the control strategy uses the output of an additional auxiliary mid-power rectifier as a V_{REF} to compare with V_{OUT} and determine the appropriate P_{IN} path. This auxiliary mid-power rectifier also serves as an alternate V_{DD} supply for the control circuitry. It should be evident that under-voltage lockout during the system initialization devastates the control logic, making the rectifier highly inefficient, missing its optimal operation, and not forgetting that a portion of the P_{IN} needs to be diverted for the auxiliary and control circuitry, which limits the PCE of the system.

Besides simply imposing different constraints on a rectifier topology, the adoption of different rectifier topologies for different P_{IN} is also viable. The dual-topology rectifier by [52] uses two rectifier topologies for different P_{IN} paths. The cross-coupled rectifier is used for low $P_{IN,}$ while the Dickson rectifier is used for high P_{IN}. This approach has the merit of combining the high sensitivity from the cross-coupled rectifier and the low I_{REV} from the Dickson rectifier. The use of the Dickson rectifier greatly overcomes the cross-coupled rectifier losses due to I_{REV} and I_{SHOOT} during high P_{IN}. It is important to note that the reported PCE_{PEAK} of the Dickson rectifier is lower than the cross-coupled rectifier by about 40% due to V_{DIODE} [52]. Subsequently, [53] developed this principle into a multi-stage rectifier with the dual-topology rectifier providing the topology amalgamation in the last stage to prevent high I_{REV} from discharging V_{OUT}. It was demonstrated by [53] that this approach has a $PCE_{PEAK} = 79.77\%$ with a P_{IN} dynamic range = 21dB for PCE > 20% at an $R_{LOAD} = 100k\Omega$. A hybrid of MPS with RCS was also reported by [54] and [55], particularly for [54], where a DC-DC boost converter was used as a low P_{IN} path and switching over to a $N_{CONFIG} = 2$ RCS serving as the high P_{IN} path when $P_{IN} > -16$dBm.

While multi-path selection seems strictly a system solution at first glance, diverting the P_{IN} to the appropriate device with the optimal V_{TH} and W/L within the rectifier is possible. This paradigm shift achieves a rectifier capable of performing adaptive PCE optimization like the study by [51]. A reconfiguration stack rectifier by [56] diverts the P_{IN} through devices with different V_{TH} at different P_{IN}, thereby altering the effective V_{TH} and W/L. In [56], the native NMOS was also utilized due to its zero-V_{TH} (V_{ZTH}), making the rectifier highly sensitive at low P_{IN}. The control logic allows three modes progressively providing the series reconfiguration with other low-V_{TH} (V_{LVT}) and high-V_{TH} (V_{HVT}) devices to limit the I_{REV} and adjust the effective W/L. A remarkable $PCE_{PEAK} = 57.75\%$ with a P_{IN} dynamic range = 22.8dB for PCE > 20% at an $R_{LOAD} = 100k\Omega$ was achieved by [56] with extensive study.

VII. SELF-BIAS GENERATION (SBG)

Unlike the previous strategies, the self-bias generation (SBG) using the generated V_{OUT}, or the V_{RF} input, has a wider variety of implementations. The objective is to suppress I_{REV} that rapidly degrades the PCE performance at high P_{IN} in the cross-coupled rectifier. Figure 7 shows the general concept of self-bias to limit V_{REV} and I_{REV} for P_{REV} loss mitigation. It is paramount for $I_{FWD} > I_{REV}$ across the period for rectification to be successful and generate a V_{OUT}.

Due to the symmetry of the cross-coupled topology, the following discussion will consider only $V_{RFP} > V_{RFN}$ ($\varphi 1$) and the operation of M_1 and M_4 (along with other relevant devices for the self-bias) for simplicity and conciseness. M_2 and M_3 function complementary to M_1 and M_4 when $V_{RFP} < V_{RFN}$ (φ_2).

A. V_{OUT} SENSING FEEDBACK

The V_{OUT} sensing feedback (VSF) technique in Figure 8(a) uses additional detection circuitry to detect V_{OUT} and bias M_1 to limit the amount of I_{REV} [33]. This feedback technique is

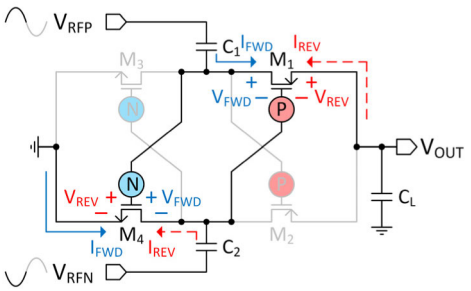

FIGURE 7. Self-bias generation rectifier concept.

accomplished by sensing V_{OUT} with M_{FB1} and M_{FB2} in the Sooch diode configuration, forming a long-length transistor, with M_{FB2} functioning as a source degeneration for M_{FB1}, to minimize the quiescent current consumption. The feedback voltage (V_{FB}) to turn on M_{B1} can be designed by properly sizing the W/L between M_{FB1} and M_{FB2}.

M_1 has a $V_{REV,M1,VSF} = V_{OUT} - (V_{C4} + V_{RFN,\varphi1}) = V_{GS,MFB1} + V_{GS,MB1}$, thereby reducing the I_{REV} compared to the cross-coupled (CC) rectifier with a $V_{REV,M1,CC} = V_{OUT}$. The voltage stored in C_4 is $V_{C4} = V_{OUT} - V_{GS,MFB1} - V_{GS,MB1} - V_{RFN,\varphi1}$. However, there is a reduction of V_{FWD} in the cross-coupled rectifier from $V_{FWD,M1,CC} = V_{RFP,\varphi1} - V_{RFN,\varphi1}$ to VSF having $V_{FWD,M1,VSF} = (1/2\ V_{OUT} + V_{RFP,\varphi1}) - (V_{C4} + V_{RFN,\varphi1})$. It was reported to have a significant P_{IN} dynamic range = 13.3dB, a 4.7dB extension compared to the cross-coupled rectifier P_{IN} dynamic range of 8.6dB [33].

B. RESISTIVE FEEDBACK BIAS

The resistive feedback (RFB) configuration in Figure 8(b) eliminates the static losses from the quiescent current by feeding V_{OUT} directly through R_{B1} [31]. Under the steady-state condition, C_4 prevents a static quiescent loss while R_{B1} configures M_1 into the diode configuration by forming a DC-short between the gate terminal and V_{OUT} node, forming a structure like the Dickson rectifier. The impedance of R_{B1} also performs the crucial function of an RF choke by effectively coupling the V_{RFN} to the gate terminal of M_1 and preventing leakage to V_{OUT}.

The biasing voltage stored in C_4 is $V_{C4} = V_{OUT} - V_{RFN,\varphi1}$. This provides $V_{REV,M1,RFB} = V_{OUT} - (V_{C4} + V_{RFN,\varphi1}) \approx$ 0V to M_1, effectively reducing the I_{REV}. This is at the expense of M_1 having a $V_{FWD,M1,RFB} = (1/2\ V_{OUT} + V_{RFP,\varphi1}) - (V_{C4} + V_{RFN,\varphi1})$. This $V_{FWD,M1,RFB}$ reduces sensitivity and requires a higher P_{IN} to overcome the $|V_{THP,M1}|$. The PCE profile shows that the PCE_{PEAK} is shifted towards the high P_{IN} region due to reduced V_{FWD}. It is also evident that I_{REV} has been reduced with a PCE improvement by about 10% at 50kΩ due to the equivalent diode-configured M_1. It also has a P_{IN} dynamic range of 16.2dB for a 0.8 × PCE_{PEAK}.

C. DIODE–CONFIGURED MOS BIAS

RFB configuration presents distinct disadvantages, such as needing a large silicon area for a large resistor and degradation in V_{FWD}. The MOS diode feedback (DFB) configuration in Figure 8(c) by [57], also known as single-sided bias, replaces the resistors with a diode-configured PMOS to achieve better performance. Single-sided bias has the advantage of inhibiting the generation of the bias at low P_{IN} due to the minimum $|V_{THP,D1}|$ requirement [57]. However, during high P_{IN}, with sufficient V_{OUT}, the diode-configured D_1 provides a charging path to charge C_4 to $V_{C4} = V_{OUT} - |V_{THP,D1}| - V_{RFN,\varphi1}$. This V_{C4} limits I_{REV} by $V_{REV,M1,DFB} = V_{OUT} - (V_{C4} + V_{RFN,\varphi1}) \approx |V_{THP,D1}|$. However, $V_{FWD,M1,DFB} = (1/2\ V_{OUT} + V_{RFP,\varphi1}) - (V_{C4} + V_{RFN,\varphi1}) = V_{RFP,\varphi1} - 1/2\ V_{OUT} + |V_{THP,D1}|$ has been improved by $|V_{THP,D1}|$.

This biasing technique has been widely adopted for its simplicity in achieving a reasonably high PCE across a wider P_{IN} range [57], [58], [59], [60]. The PCE_{PEAK} of the single-sided bias has an improvement of 20% compared to the resistive feedback despite an increase in the I_{REV}. It also has a P_{IN} dynamic range of 6.8dB for a 0.8xPCE_{PEAK}.

The single-sided bias can be further improved by biasing the NMOS. Figure 8(d) shows that the double-sided bias by [57] also generates a positive bias for M_4 for improved sensitivity. A similar bias by [61], [62], [63], [64], and [65] also reported an enhanced sensitivity performance. This bias voltage on M_4 is generated during φ_2 and is stored in C_5. The stored voltage $V_{C5} = V_{SS} - |V_{THP,D3}| - V_{RFP,\varphi2}$ is charged by the conduction path from the diode-configured PMOS D_4. The PCE at high P_{IN} yields minimal improvement because I_{REV} is still primarily limited by D_1. However, a positive voltage boost from V_{C5} adversely delays turning off M_4, leading to an undesirable discharge of C_2 and diminishing the effect of voltage doubling during φ_2. As a result, even though there is an improved PCE_{PEAK} by approximately 5-10%, the benefit quickly diminished and converged towards the single-sided bias at an even higher P_{IN} [57]. The bootstrapped gate by [66] mitigates the I_{REV} loss by biasing the gate terminal of M_1 for V_{TH}–cancellation using bootstrapping and achieves an overall PCE improvement of 10% – 20% compared to its predecessor [67] and [68]. In contrast, [69] and [70] bias M_4 with a negative voltage with a negative voltage charge pump to limit I_{SHOOT} while trading off sensitivity. This negative biasing allows a much better performance at an even higher P_{IN}, resulting in a secondary PCE_{PEAK}. However, the negative voltage charge pump must be properly designed to prevent generating a bias voltage for NMOS during low P_{IN}, increasing the effective V_{THN} and unnecessarily degrade the sensitivity.

D. AUXILIARY BOOSTED GATE

The auxiliary boosted gate (ABG) in Figure 8(e) attempts to offset the V_{TH} using several auxiliary floating rectifiers [71]. Unlike the main rectifier, the floating rectifier can produce higher V_{OUT} due to the absence of loading at the output node. The boosted gate achieves better sensitivity with a 30% PCE improvement at low P_{IN} from –38dBm < P_{IN} < –13dBm with a 50-kΩ load while preserving the PCE profile [71]. Under

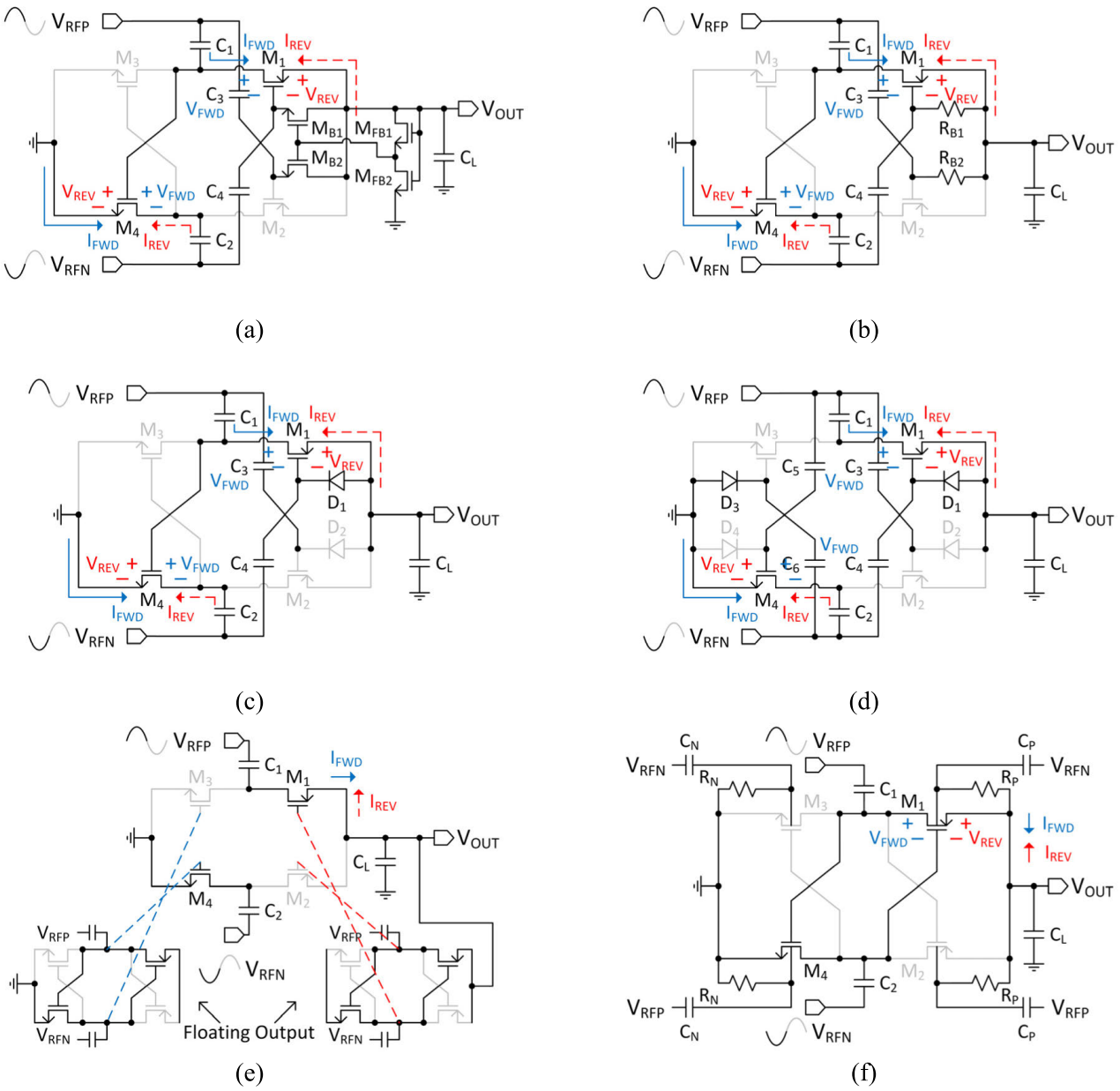

FIGURE 8. Biasing technique (a) V_{OUT} Sensing Feedback [33] (b) Resistive Feedback [31] (c) Diode-configured MOS Feedback: Positive PMOS bias [57] (d) Diode-configured MOS Feedback: Positive PMOS and NMOS bias [57] (e) Auxiliary Boosted Gate [71] (f) Dynamic V_{TH} Body Bias [82].

steady-state, the bias voltage stored in the coupling capacitor of the floating rectifier is 1/2 ($V_{OUT} - V_{OUT,FP}$) for M_1 and 1/2 ($V_{OUT,FN} - V_{SS}$) for M_4 [72].

It is worth noting that an additional eight devices are required to implement the biasing circuit. Furthermore, proper optimization is required to prevent excessive gate boosting, which results in a large I_{REV} and the discharge of the coupling capacitor in the main rectifier from the persistent conduction of the NMOS. It was demonstrated by [73], [74], and [75] that the preceding rectifier stages can also function similarly to the auxiliary rectifiers. On the other hand, an auxiliary self-bias circuitry was used by [30] to increase the charge transfer capability by generating a lower bias for PMOS and a higher bias for NMOS to increase the I_{FWD}.

Another example of the boosted gate is the all-NMOS rectifier [76]. It uses cross-coupled low and half-diode high sides to maintain good sensitivity at low P_{IN} and eliminate I_{REV}. The double-sided self-bias [57] was also incorporated onto the cross-coupled low side to improve the conduction of the NMOS by allowing more charges to replenish the coupling capacitors, thereby improving the PCE and sensitivity. It demonstrated an improvement of >50% compared to the Dickson rectifier and >100% compared to the cross-coupled rectifier at low and high $P_{IN,}$ respectively [76].

On the other hand, [77] demonstrated a half-diode low and cross-coupled high sides with active bias tuning to achieve a wide P_{IN} dynamic range. The improvement demonstrates the combined effect and merits of the cross-coupled low and half-diode high sides similar to the study by [78] and subsequently developed in [79] into an RCS implementation.

E. DYNAMIC V_{TH} WITH BODY BIAS

Most SBG involves biasing the gate terminal while connecting the body terminal to the source terminal to achieve I_{REV} reduction. Another form of bias involving the body terminal allows the modification of the V_{TH} of the transistor as follows:

$$V_{TH(P,N)} = V_{TH0(P,N)} + \gamma\left(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) \tag{6}$$

where V_{TH0} is the $V_{SB} = 0$V body bias V_{TH}, γ is the body effect coefficient, and ϕ_F is the Fermi potential. Note that γ is positive for NMOS and negative for PMOS, while ϕ_F is negative for NMOS and positive for PMOS.

Higher V_{TH} has a lower I_{REV}, while lower V_{TH} improves I_{FWD}. A lower DC feeding body bias by [80] biases the current k^{th} stage PMOS body terminal using V_{OUT} from the previous stage $V_{OUT,k-1}$. It was demonstrated by [80] that lowering $|V_{THP}|$ improves the PCE by as much as 9.5% at a lower P_{IN}. This body bias was further expanded upon by [81], having the current k^{th} stage NMOS body terminal connected to the current output, reducing the V_{THN}.

Despite reducing V_{TH} to improve sensitivity by increasing I_{FWD}, the performance at high P_{IN} is degraded due to an increase in I_{REV}. Providing an adaptive body bias to adjust the V_{TH} dynamically is useful. One such implementation is by [82], where the complementary phase of V_{RFP} or V_{RFN} is coupled into the body terminal, shown in Figure 8(f). I_{FWD} is increased due to a lowering of V_{TH} during ϕ_1 charging phase while the I_{REV} is reduced by an increase of V_{TH} during ϕ_2 discharging phase. It was reported to achieve an improved sensitivity of –23.4dBm and a P_{IN} dynamic range of 14.3dB.

VIII. CURRENT TRENDS AND DISCUSSION

Some of the most recent and notable developments of wide P_{IN} dynamic range rectifiers are listed in Table 2. Though it is not exhaustive, Table 2 shows works from the various discussed strategies and implementations. An overview of the various strategies in terms of the mean $\bar{x}$ and the standard deviation σ from the reported performance in Figure 9 is tabulated in Table 1. Even though different constraints were reported in the literature, a general trend still emerges between the different strategies. From this study, there was more work exploring the SBG with a wide range of different implementations.

Figure 9(a) shows the PCE_{PEAK} versus P_{IN} dynamic range for PCE > 20% (PR #1). All three strategies using the cross-coupled rectifier have comparable $PCE_{PEAK} > \sim$60%, and as expected, the strategies that employ the Dickson rectifier generally yield lower PCE_{PEAK}. Note that [52] and [53] use the Dickson rectifier and cross-coupled rectifier as part of MPS. It can be observed that RCS and MPS can easily achieve higher PR #1 than SBG. Each rectifier or configuration in RCS or MPS is subjected to different optimization constraints to cover different P_{IN} domains, leading to a wider PCE profile. However, to better assess the PCE profile quality, the P_{IN} dynamic range is determined for PCE > 0.8 × PCE_{PEAK} (PR #2), as shown in Figure 9(b). PR #2 for all three strategies is centred around PR #2 $\bar{x} \approx 7.63$dB. This observation indicates a PCE profile with abrupt PCE transition even though all three strategies have a wider PR #1 $\bar{x} > 14$dB. This difference between PR #1 and PR #2 indicates that a particular configuration contributes most of the performance improvement with rapid PCE degradation in the RCS and MPS, while occasional non-dominant PCE_{PEAK} stretches PR #1. On the other hand, though SBG reduces the I_{REV}, it is still ineffective in reducing the rate of PCE degradation during higher P_{IN}.

RCS and MPS fare better than SBG in terms of PR #2 because MPS uses a specifically optimized rectifier to accommodate different P_{IN} domains, while RCS tends to use the same rectifier core in different configurations, resulting in better PR #2 $\bar{x}$. Also, it is quite evident that RCS has a better PR #2 $\sigma = 2.75$dB than MPS from the use of the same rectifier core. However, the PR #2 σ for RCS and MPS has a larger variation than SBG, likely due to the process variation between multiple rectifiers. A single rectifier core is typically used in SBG, where different biasing or V_{TH} compensation techniques are applied. It is also important to note that RCS is usually implemented as part of a system where a better algorithm or trimming can provide correction and adjust the PCE profile to achieve better P_{IN} coverage, unlike SBG, with the biasing built-in with minimal available tuning.

Figure 9(c) shows the Sensitivity versus P_{IN} dynamic range for PCE > 0.8 × PCE_{PEAK} (PR #2). RCS has the best trade-off between having a sensitivity of $\bar{x} \approx$ –16.74dBm and a wide PR #2 of $\bar{x} \approx 8.83$dB. On the other hand, SBG generally yields good performance in sensitivity $\bar{x} \approx$ –17.05dBm and $PCE_{PEAK}\bar{x} \approx 57.12\%$, as shown in Figure 9(d). It is because the same rectifier core is utilized without major or abrupt changes on the V_{OUT}/N_{CONFIG} or I_{OUT}/N_{CONFIG} experience per unit rectifier, yielding better optimization. Furthermore, RCS and MPS require a portion of the P_{OUT} to be diverted to the control circuitries to facilitate the operational requirement, thereby incurring quiescent power loss and degrading PCE.

As validated in the literature, the design based on the Dickson rectifier indeed offers a lower PCE and sensitivity. Interestingly, such a design seems to offer wider PR #1 despite the limiting dropout voltage V_{DIODE} or V_{TH}. The widening of Dickson rectifier PR #1 is likely due to a lower rate of PCE degradation ($\Delta PCE/\Delta P_{IN}$) in the high P_{IN} domain. The lower $\Delta PCE/\Delta P_{IN}$ makes the switchover transition between the MPS paths less abrupt, easing the required responsiveness of the control circuitry during the switchover.

TABLE 1. Performance metrics of various strategies.

Strategy	PR #1[c] (dB)		PR #2[d, e] (dB)		Sensitivity[f] (dBm)		PCE_{PEAK} (%)	
	$\bar{x}$	σ	$\bar{x}$	σ	$\bar{x}$	σ	$\bar{x}$	σ
RCS (11)	14.84	4.48	8.83	2.75	-16.74	9.46	47.90%	16.37%
D [a]	13.89	3.61	8.30	1.88	-15.20	9.06	42.71%	18.76%
CC [b]	15.88	5.31	9.36	3.60	-14.74	14.10	61.98%	11.76%
MPS (8)	17.25	4.20	8.13	3.24	-16.50	9.13	57.10%	15.42%
D [a, f]	19.07	2.00	7.33	3.51	-12.00	8.32	67.72%	19.69%
CC [b, f]	17.29	4.54	7.71	3.26	-18.50	7.74	58.83%	15.80%
SBG (22)	14.04	4.60	7.21	2.17	-17.05	5.36	57.12%	18.59%
D [a]	10.67	3.28	6.80	3.21	-16.00	7.48	38.73%	7.80%
CC [b]	15.31	4.44	7.36	1.75	-17.45	4.58	64.01%	16.66%

[a] Dickson rectifier, [b] Cross-coupled rectifier, [c] PCE > 20%, [d] PCE > 0.8xPCE_{PEAK}
[e] Estimated from the publications' figures, [f] for reference only as R_{LOAD} varies across publication
[*] [52] [53] [78] inclusive of structure consists of both D & CC, [**] [55] involves both MPS and RCS, [***] [83] involves both MPS and SBG

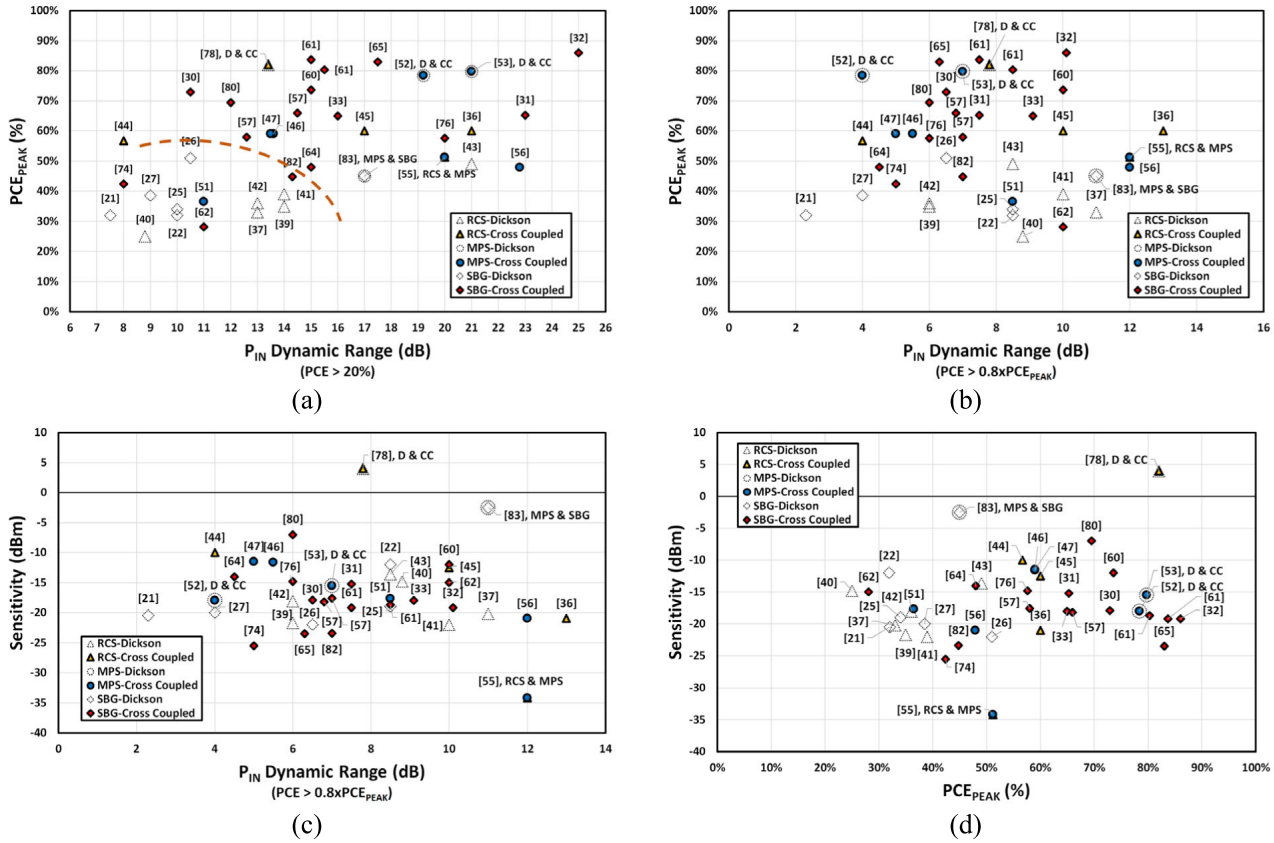

FIGURE 9. Current trends from recent literature (a) PCE_{PEAK} versus P_{IN} Dynamic Range: PCE > 20% (b) PCE_{PEAK} versus P_{IN} Dynamic Range: PCE > 0.8PCE_{PEAK} (c) Sensitivity versus P_{IN} Dynamic Range for PCE > 0.8PCE_{PEAK} (d) Sensitivity versus PCE_{PEAK}.

At the same time, the SBG strategy yields limited results across all the metrics for the Dickson rectifier. The study suggests that while the dropout voltage has been largely eliminated using a V_{TH}-compensated structure, it also inherited I_{REV} and increased I_{LEAK} due to the diode-configured transistors being biased into a weakly on-state. As a result, the diode-configured transistor (with V_{TH}-compensated) provides a discharging path when $V_{OUT} > V_{RF}$. As a result, the inclusion of additional discharging mechanisms (previously absence) diminished the benefit of reduced the dropout voltage.

Cross-coupled rectifiers are more versatile as they generally offer better PCE_{PEAK} and sensitivity. It is reasonable to simply seek an effective approach to widen its lacklustre dynamic range. As a result, SBG offers reduced system and control complexity, making it a popular approach with the

TABLE 2. Overview of recent and notable development in Wide P_{IN} dynamic range MOS rectifier in the literature.

Ref	Technique	Tech Node	Freq (MHz)	R_{LOAD} (kΩ)	PR#1 (dB)	PR#2 (dB)	Sensitivity (dBm) @ 1V	PCE_{PEAK} @ P_{IN}	Stages
[21] [c, d, h, i]	Adaptive V_{TH} Compensation	130nm	902 - 928	1000	7.5 [j]	2.3 [j]	–20.5 1-MΩ	32% –15 dBm	12
[25] [c, d, h, i]	Local Self-Calibrator V_{TH}	180nm	433	100	10 [j]	8.5 [j]	–19 1-MΩ	34% –7 dBm	4
[26] [c, d, h]	Subthreshold V_{TH} Compensation	130nm	896	1000	10.5	6.5 [j]	–22 1-MΩ	51% –11 dBm	4
[33] [c, e, g]	Adaptive Feedback	180nm	1000	100	16 [j]	9.1 [j]	–18 100-kΩ	65% –20 dBm [j]	1
[36] [a, e, h, i]	Reconfiguration	130nm	868	cap	21 [j]	13 [j]	–21 2V, ∞-Ω	60% –9 dBm [j]	2, 1
[37] [a, d, h, i]	Reconfiguration	180nm	902	200	13	11 [j]	–20.2 1-MΩ	33% –8 dBm	2, 1
[39] [a, d, g]	Reconfiguration	130nm	900	1000	14	6 [j]	–21.7 1-MΩ	34.93% –10 dBm	12, 3
[41] [a, d, h, i]	Reconfiguration	130nm	820	4.7	14	10 [j]	–3 4.7-kΩ	39% –5 dBm	1,2, 4,8
[47] [b, e, h, i]	Tri-path PMU Aware	180nm	400	100	13.5	5 [j]	–11.5 ∞-Ω	60% –8 dBm [j]	5
[51] [b, e, h, i]	Dual-Path	65nm	900	147	11	8.5 [j]	–17.7 ∞-Ω	36.5% –15 dBm [j]	5
[52] [b, d, e, g]	Dual Topology	130nm	900	100	19.5	4 [j]	–18 100-kΩ	78.4% –16 dBm	3
[53] [b, d, e, g]	Topology Amalgamation	65nm	900	100	21	7 [j]	–15.5 100-kΩ	79.77% –18 dBm	2+1
[56] [b, e, g]	Reconfiguration Stack	130nm	900	100	22.8	12 [j]	–21 1-MΩ	47.91% –14 dBm	3
[57] [c, e, g]	Double-sided	180nm	900	100	14.5 [j]	6.8 [j]	–18.2 1-MΩ	66% –19 dBm [j]	1
[60] [c, e, h, i]	Boosted Gate	65nm	2450	13.8	15 [j]	10 [j]	–12 ∞-Ω	73.6% –6 dBm	2
[61] [c, e, g]	Shared-Cap Coupling	130nm	900	100	15 [j]	7.5 [j]	–19.2 100-kΩ	83.7% –18 dBm	3
[80] [c, e, g]	Lower DC Feed Self-body-bias	130nm	953	2	12 [j]	6 [j]	–7 [j] 50-kΩ	69.5% 5 dBm [j]	3
[82] [c, e, h, i]	Dynamic body bias	90nm	900	200	14.3	7 [j]	–23.4 1-MΩ	44.8% –17.9 dBm [j]	5

[a] RCS, [b] MPS, [c] SBG, [d] Dickson rectifier, [e] Cross-coupled rectifier,
[g] wafer probe measurement, [h] board measurement, [i] Inclusive of matching network, [j] Estimated from figures reported in publications

cross-coupled rectifier. From the study, a larger performance variation was observed from the system using the cross-coupled rectifier. These are possibly the two key reasons: 1) process variations involving both PMOS and NMOS are present and shift the optimal operating condition in the cross-coupled rectifier, and 2) different device types (such as HVT) are often required to generate the appropriate bias. The use of different device types is essential as the bias structure also aims to exploit the inherent characteristic of the cross-coupled rectifier at low P_{IN} by delaying the onset of the bias. Furthermore, the sensitivity of the cross-coupled rectifier is not guaranteed, as the inclusion of the bias structure introduces additional parasitic capacitance. Extensive optimization and iterative cycles are required to address the performance deficiency while also seeking to widen the dynamic range.

IX. CONCLUSION

This review presented the three major strategies to improve the P_{IN} dynamic range of a CMOS RF-DC rectifier. The three strategies are Reconfigurable Structure (RCS), Multi-path Selection (MPS) and the Self-bias Generation (SBG). The implementation of SBG is varied, with techniques primarily revolving around I_{REV} reduction and I_{FWD} improvement within a rectifier. Although some exceptions are also

reported, RCS and MPS are generally considered system approaches to widen the P_{IN} dynamic range. Depending on the intended application, different strategies offer different merits and trade-offs between achieving a wide P_{IN} dynamic range and maintaining reasonable PCE profile performance. From the trend presented in this study, SBG offers a promising compromise between the different performance metrics, leading to the numerous works reported. Future development in wide P_{IN} dynamic range rectifiers will likely adopt a combination of the different strategies.

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