High-Frequency Low-Power Local Oscillator Generation

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Table of Acronyms

BPF	band-pass filter
CML	current mode logic
CP	charge pump
DFF	D-flip-flop
DUT	device under test
E-TSPC	extended-TSPC
ESD	electrostatic discharge
FCC	federal communications commission
FD	frequency divider
FFM	fractional frequency multiplier
FM	frequency multiplier
FoM	figure of merit
IF	intermediate frequency
ILFD	injection-locked frequency divider
ILFM	injection-locked frequency multiplier
ILO	injection-locked oscillator
ISF	impulse sensitivity function
ISM	instrumentation, scientific and medical
LNA	low-noise amplifier
LO	local oscillator
LPF	low pass filter
LTI	linear time invariant
LTV	linear time variant

PFD	phase frequency detector
PLL	phase-locked loop
PSD	power spectrum density
TSPC	true-single-phase-clock
UNII	unlicensed national information infrastructure
UWB	ultra-wide band
VCO	voltage-controlled oscillator
WLAN	wireless local area network

SUMMARY

With rapid development in the area of RF and wireless communication, the interest in frequency synthesizers has grown rapidly in the last few years. Frequency synthesizer is used for local oscillator (LO) generation. In this thesis, our aim is to explore high-frequency low-power LO generation in CMOS technology. We focus on three most power-hungry blocks in a frequency synthesizer, which dominate the total power consumption due to their high-frequency operation, namely voltage-controlled oscillator (VCO), frequency divider and frequency multiplier, as these circuits are the bottleneck to achieve the above mentioned aim. Through reducing their power consumption, the total power consumption of the frequency synthesizer can be reduced significantly. Moreover, the phase noise of the frequency synthesizer is significantly dependent on the VCO and the frequency multiplier. Thus, novel ideas for these circuits are proposed in Chapter 3, Chapter 4 and Chapter 5. Finally, these ideas are implemented in a frequency synthesizer as a design example in Chapter 6. The frequency synthesizer can operate at the 24-GHz Instrument, Scientific and Medical (ISM) band, which can be used for automotive short range radar. With these ideas in these proposed circuits, the proposed frequency synthesizer can have better performances than those previous designs [1] [2] [3].

Firstly, a divide-by-2/3 injection-locked frequency divider (ILFD) is proposed based on a conventional ILFD with a fixed division ratio, which can be used to design a programmable frequency divider in an integer-N phase-locked loop (PLL). As the most critical characteristic in the low-power and high-frequency ILFD, the operation range is analyzed and then its design

equations are derived mathematically. Thus, the mutual operation range in both the divide-by-2 and divide-by-3 modes can be optimized. With a power consumption of 3.15 mW, the operation range of the proposed circuit in the divide-by-2 mode is 3.44~5.02 GHz while the operation range in the divide-by-3 mode is 4.28~4.81 GHz. Moreover, the figure of merit (FoM) for the ILFD is 1.527 GHz/mW.

Secondly, a dual-band VCO is designed with a VCO stacking on top of an ILFD for a dual-band frequency synthesizer. With a power consumption of 3.2 mW, the tuning ranges of the dual-band VCO's frequency bands are 4.48~5.86 GHz and 2.24~2.93 GHz, respectively. Moreover, the FoM for the upper and lower frequency bands are -187.1 and -190.1 dB, respectively.

Thirdly, a ×2 injection-locked frequency multiplier (ILFM) is proposed with high operation frequency and high conversion gain, while has low power consumption. Moreover, the topology of the proposed circuit is analyzed and its design equations for operation range and conversion gain are derived. A ×(3/2) fractional frequency multiplier (FFM) is also proposed based on the novel topology and optimized for its operation range. The proposed FFM also has high conversion gain and low power consumption at high-frequency operation.

Finally, a 24-GHz frequency synthesizer is proposed for low-power operation. Contribution and generation of the phase noise in the frequency synthesizer are analyzed in detail. Through the measured results, it is shown that the frequency synthesizer has very low power consumption of 11.86 mW and low phase noise of -104 and -113 dBc/Hz at 1-MHz and 10-MHz offset frequencies, respectively.

CHAPTER 1

Introduction

1.1 Motivation

A frequency synthesizer is used to generate a signal at a precise frequency, which is found in test and measurement equipments, as well as in communication equipments. In general, RF frequency synthesizers are designed based on the concept of phase-locked loop (PLL).

In a transceiver design, there is a clear trend towards full integration of the RF front-end on a single die for low cost and low power consumption. The design of RF building blocks in a CMOS technology is now an important research topic in order to replace the more expensive bipolar technology. Although CMOS technology suffers from inferior device physics, continued investment on a large scale has increased its suitability for being used at high frequencies [4]. Another noteworthy advantage is the large number of interconnect layers now commonly available in CMOS RF/analog/logic processes, which leads to more compact designs. Therefore, a deep sub-micrometer CMOS technology can be used to incorporate the RF circuits with the baseband circuits on the same chip. Fully integrated CMOS RF building blocks are crucial and have been widely explored [5] [6].

However, there are still some limitations in the current CMOS technology, such as low transconductance of CMOS transistor at high-frequency operation. As a result, the implementation of high-frequency fully integrated frequency synthesizer still remains a challenge. Firstly, the transit frequency f_t of CMOS

transistor limits the operating frequencies of the CMOS in high-frequency circuits. The voltage-controlled oscillator (VCO) and the first-stage frequency divider, known as a prescaler, operate at the highest frequency in a frequency synthesizer, so they are the crucial blocks in the design of a frequency synthesizer. Secondly, high-frequency circuits often have high power consumption in RF circuits. In the frequency synthesizer, the total power consumption normally increases with its operation frequency. Generally, the VCO and the first-stage frequency divider dominate the total power consumption of the frequency synthesizer.

Currently, there are still many challenges in the design of high-frequency and low-power frequency synthesizer using the low-cost technology. This can be illustrated in the following examples. In [7], an integer-N charge-pump PLL in 0.13 μm CMOS technology achieved the high operating frequency of 21 GHz. In this design, a differential LC VCO and a group of current mode logic (CML) frequency dividers are used. However, the power consumption of this circuit is high. In [8], a Ku-band frequency synthesizer in 0.18 μm CMOS technology demonstrates the highest frequency 16.9 GHz only. In [9], a 24-GHz PLL is designed in a 0.18 μm CMOS technology under 1-V supply power, but it needs a very high reference frequency of 12 GHz.

1.2 Objectives

In this thesis, our aim is to explore high-frequency low-power LO generation in CMOS technology. We focus on three most power-hungry blocks in a frequency synthesizer, which dominate the total power consumption due to

their high-frequency operation, namely voltage-controlled oscillator (VCO), frequency divider and frequency multiplier. Through reducing their power consumption, the total power consumption of the frequency synthesizer can be reduced significantly.

For high-frequency and low-power LO generation, three approaches are investigated in this thesis. Firstly, it is found from literature that an injection-locked oscillator (ILO) has considerable advantages for low-power and high-frequency operation [10] [11]. With this concept, a frequency divider and a frequency multiplier can be designed based on the ILO, namely injection-locked frequency divider (ILFD) and injection-locked frequency multiplier (ILFM), respectively. Thus, both the ILFD and the ILFM can operate at high frequency and consume low power. Secondly, a stacking topology is implemented in order to reuse the current. If two blocks, such as the VCO and the first-stage frequency divider, are designed in the stacking topology, it is possible to reduce the total power consumption. Finally, the power consumption of a frequency synthesizer can be reduced by incorporating an ILFM. In addition, the phase noise of the output signal from the frequency synthesizer can be improved through the ILFM.

1.3 Major Contributions of the Thesis

There are four important contributions in this research. Firstly, a divide-by-2/3 ILFD is proposed based on an ILFD, which has a pair of switched capacitors in order to switch the division modes [MYN, J1]. The ILFD's operation range is analyzed based on gain and phase conditions and then its

design equations are derived mathematically. Thus, the mutual operation range in the two division modes can be optimized based on these equations. The proposed circuit has lower power consumption and better figure of merit (FoM) than other dual-modulus frequency dividers.

Secondly, a dual-band VCO is designed with a VCO stacking on top of an ILFD [MYN, J2]. The biased current in the VCO is reused by the ILFD, so the total power consumption can be reduced significantly. With low power consumption, the proposed circuit provides both the upper and lower band frequency. Moreover, the dual-band VCO performs excellently on the typical VCO's FoM.

Thirdly, a ×2 ILFM is proposed based on a novel topology for low-power and high-frequency operation, while the proposed circuit is analyzed mathematically [MYN, J3]. The design equations of the conversion gain and operation range are derived against the magnitude of the injection current. Similarly, a $\times(n+1)/n$ fractional frequency multiplier (FFM) is proposed for high-frequency operation, where n is 2 in this design [MYN, J4]. The operation range of the ×(3/2) FFM is optimized with low power consumption.

Finally, a 24-GHz frequency synthesizer is designed for low-power operation. Phase noise generation and contribution in the frequency synthesizer are analyzed in detail. It is shown through theoretical analysis and measurement that the frequency synthesizer has very low power consumption and low phase noise.

1.4 Organization of the Thesis

This thesis is organized into seven chapters. In Chapter 1, the motivation, objective and contributions of the thesis are introduced, followed by an outline of the thesis. In Chapter 2, the topology of a basic PLL is reviewed. Based on the topology, the linear model of the PLL is described mathematically. Then, the performance of a PLL is discussed, including reference spur, phase noise and lock time. Moreover, some VCOs and frequency dividers are investigated in detail as the most important building blocks in a PLL. At the end, the model of an ILO is analyzed.

In Chapter 3, conventional divide-by-2/3 frequency dividers are studied. The proposed divide-by-2/3 ILFD is presented and its operation range is analyzed. In Chapter 4, the proposed dual-band VCO is described, and then the design techniques are explained in detail. In Chapter 5, the ×2 ILFM is presented with the detail analysis on its performance, including the injection current, conversion gain and operation range. Furthermore, the ×(3/2) FFM is presented with the analysis on the optimized operation range. In Chapter 6, the proposed frequency synthesizer is described, then the analysis on its phase noise is discussed and verified through measurement.

Finally, the thesis conclusions are given in Chapter 7. Moreover, some interesting research areas are discussed for future work.

CHAPTER 2

Overview of Phase-Locked Loop

Frequency synthesizer is commonly used to generate LO signal in a wireless transceiver. The LO signal is required to down-convert the RF to a lower Intermediate Frequency (IF), or to up-convert the IF to the RF [12]. The design of a frequency synthesizer still remains one of the challenging tasks in RF systems because it must meet very stringent requirement, such as phase noise, power consumption and tuning range. Typically, the frequency synthesizer is designed based on a PLL that is also used in clock data recovery circuits [13] [14]. The quality of the LO signal is fully dependent on the design of the PLL.

2.1 Topology of a PLL

A PLL is a negative feedback system, which achieves a precise definition of the output frequency. A general topology of a basic PLL is shown in Figure 2.1. It consists of a phase detector, a loop filter, and a VCO. If the PLL is designed as a frequency synthesizer, a frequency divider is used in the feedback path. Thus, the output signal operates at the frequency f_{out} that is the N times of the frequency f_{ref} of the reference signal, where N is the division ratio of the frequency divider.

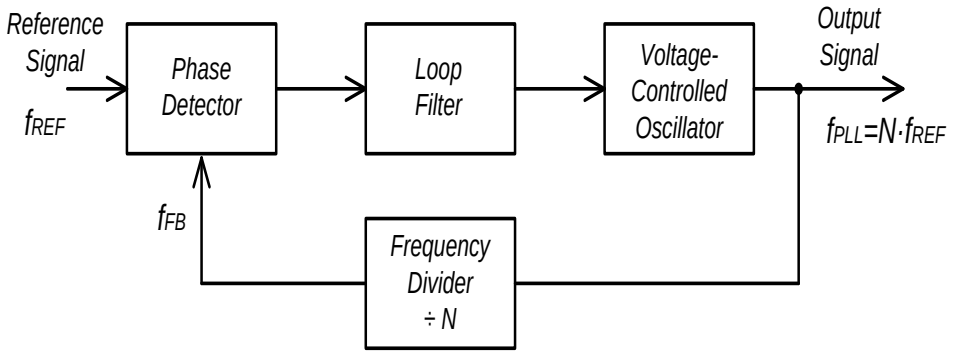

Figure 2.1: Topology of a basic PLL

In the PLL, the output of the phase detector is proportional to the phase difference between its two input signals. One of the input signals is fixed at a very stable frequency, which is generally generated by a quartz crystal in practical applications or by a signal generator for measurement in laboratory. Meanwhile, the other input signal is less stable and comes from the frequency divider or directly from the VCO. The phase detector can be implemented in four main methods [15]. The first method is a multiplying phase detector, which is based on the multiplication of two sinusoidal signals from the same frequency. The second and third methods are an OR-exclusive-based and a flip-flop-based phase detectors, respectively, which operate with the zero crossings of the input signals. The last method is a phase frequency detector (PFD). Its output is dependent on both the phases and frequencies of its two inputs. Comparing with the first three methods, the PFD is aimed to lock both frequency and phase. A charge pump with the PFD instead of a phase detector is used to improve the performance of the PLL [12].

The loop filter is usually a low-pass filter in which the phase detector's output is filtered to produce the VCO’s tuning voltage. The filter is required to suppress the voltage ripple and to reduce spurious tones and distortions of the oscillator. The dynamic of the PLL is closely dependent on the design of the

filter, including natural frequency, damping factor and loop bandwidth. In addition, a passive filter is usually preferred than an active filter because the latter results higher complexity, cost and noise.

The VCO has a tunable output frequency as the PLL's output. The VCO's output angular frequency ω_{PLL} is the function of a tuning voltage V_{tune} that is the voltage after the loop filter.

$$\omega_{PLL}(t) = \omega_0 + K_{VCO} \cdot V_{tune} \tag{2.1}$$

where ω_0 is the angular frequency of the VCO at V_{tune}=0 and K_{VCO} is the gain or sensitivity of the VCO.

Integrating (2.1) with respect to time, the excess output phase $\theta_{PLL}(t)$ can be given by

$$\theta_{PLL}(t) = K_{VCO} \cdot \int V_{tune}(t)dt \tag{2.2}$$

With the input signal from the VCO, the frequency divider is used to generate its output signal at the corresponding output frequency. With the divide-by-*N* frequency divider, the output frequency of the VCO is divided by *N*. Thus, the output angular frequency of the frequency divider can be expressed as

$$\omega_{FD}(t) = \frac{\omega_{PLL}(t)}{N} \tag{2.3}$$

Integrating (2.3) with respect to time, the phase of the frequency divider's output $\theta_{FD}(t)$ can be given by

$$\theta_{FD}(t) = \frac{\theta_{PLL}(t)}{N} \tag{2.4}$$

When the two inputs of the phase detector are equal, the phase difference at the phase detector's output is constant with time. After the loop filter, V_{tune} is constant so that the VCO oscillates at a fixed frequency. Thus, all signals in the

PLL reach a steady state and the PLL is in the locked state.

$$\theta_{FD}(t) = \theta_{ref}(t) \tag{2.5}$$

where $\theta_{ref}(s)$ is the reference's phase signal. Substituting (2.5) into (2.4),

$$\theta_{ref}(t) = \frac{\theta_{PLL}(t)}{N} \tag{2.6}$$

Differentiating (2.6) with respect of time,

$$f_{PLL} = f_{ref} \cdot N \tag{2.7}$$

where the division ratio N can be changed to synthesize the different frequencies. If N is an integer, this is an integer-N frequency synthesizer. If the output frequency step has to be smaller than the reference frequency, N should be a fractional number. Thus, this is a fractional-N frequency synthesizer for high resolution and small channel spacing transceivers.

2.2 Linear Model of a PLL

Due to non-linearity of phase detector, VCO, and frequency divider, the analysis on the PLL is complicated. For simplicity, the PLL in the locked state can be analyzed based on a linear model. The model for all PLL's building blocks are summarized in Figure 2.2. For some applications without the frequency divider, N in the below analysis can be equal to one.

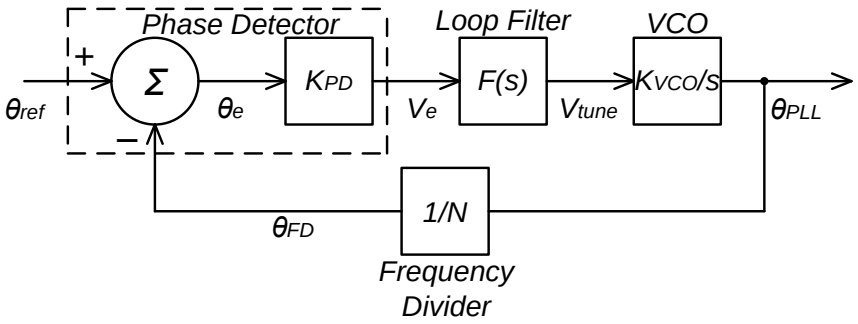

Figure 2.2: A linear model for the PLL

The phase error signal V_e is produced by the phase detector. Based on the function of the phase detector, it can be expressed as

$$V_e(s) = K_{PD} \cdot \left[\theta_{ref}(s) - \theta_{FD}(s)\right] = K_{PD}\theta_e(s) \tag{2.8}$$

where K_{PD} is the gain of the phase detector and $\theta_e(s)$ is the phase difference between two input signal.

After the loop filter, V_{tune} is given by

$$V_{tune}(s) = V_e(s)F(s) = K_{PD} \cdot \left[\theta_{ref}(s) - \theta_{FD}(s)\right] \cdot F(s) \tag{2.9}$$

where $F(s)$ is the transfer function of the loop filter.

From (2.2), $\theta_{PLL}(t)$ can be expressed in *s*-domain

$$\theta_{PLL}(s) = \frac{K_{VCO}V_{tune}(s)}{s} \tag{2.10}$$

Thus, the transfer function of the forward path, including the phase detector, the loop filter and the VCO, can be expressed as

$$H(s)|_{FW} = \frac{\theta_{PLL}(s)}{\theta_e(s)} = \frac{K_{PD}K_{VCO}F(s)}{s} \tag{2.11}$$

From (2.4), the transfer function of the feedback path can be expressed as

$$H(s)|_{FB} = \frac{\theta_{FB}(s)}{\theta_{PLL}(s)} = \frac{1}{N} \tag{2.12}$$

Combining (2.11) and (2.12), the transfer function of the PLL can be expressed as

$$H(s)|_{PLL} = \frac{H(s)|_{FW}}{1+H(s)|_{FW} \cdot H(s)|_{FB}} = \frac{K_{PD}K_{VCO}F(s)}{s+\frac{K_{PD}K_{VCO}F(s)}{N}} \tag{2.13}$$

Meanwhile, the phase error transfer function can be expressed as

$$H(s)|_{err} = \frac{\theta_e(s)}{\theta_{ref}(s)} = \frac{s}{s+\frac{K_{PD}K_{VCO}F(s)}{N}} \tag{2.14}$$

Conclusively, the transfer function of the PLL has a low-pass characteristic while the phase error transfer function has a high-pass characteristic.

2.2.1 Passive lag-RC filter

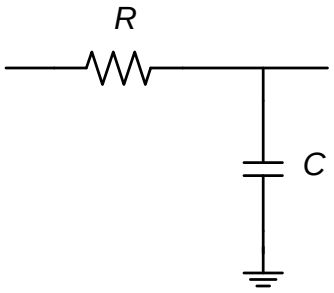

Figure 2.3: A passive lag-RC filter

The dynamic of the PLL is dependent on the transfer function of the loop filter *F(s)*. A passive lag-RC filter is shown in Figure 2.3. The transfer function of the loop filter can be expressed as

$$F(s) = \frac{1}{1+sRC} \tag{2.15}$$

Thus, the PLL's transfer function is given by

$$H(s)|_{PLL} = \frac{NK_{PD}K_{VCO}}{s^2NRC+sN+K_{PD}K_{VCO}} \tag{2.16}$$

The denominator can be rewritten as a familiar form of $s^2 + 2\xi\omega_n s + \omega_n^2$ in control theory, where ω_n and ξ are defined as natural frequency and damping factor, respectively. Thus, (2.16) can be expressed as

$$H(s)|_{PLL} = \frac{N\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2} \tag{2.17}$$

where $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NRC}}$ and $\xi = \frac{1}{2}\sqrt{\frac{N}{K_{PD}K_{VCO}RC}}$.

This PLL with the passive lag-RC filter has a constraint that the natural frequency and the damping factor cannot be designed by selecting the values of *R* and *C* independently. Therefore, there is a trade-off in determining these two parameters in the design of the PLL.

2.2.2 Passive lag-lead filter

To avoid the trade-off between the natural frequency and the damping factor, a passive lag-lead filter is shown in Figure 2.4, where one more resistor is added in series with the capacitor. The transfer function of the filter can be expressed as

$$F(s) = \frac{1+\tau_2 s}{1+\tau_1 s} \tag{2.18}$$

where $\tau_1 = (R_1 + R_2)C$ and $\tau_2 = R_2 C$.

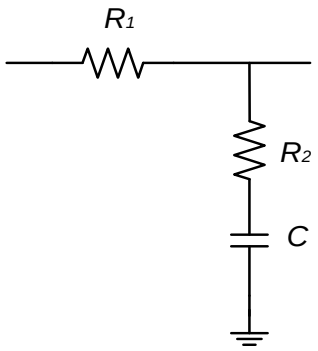

Figure 2.4: A passive lag-lead filter

Thus, the PLL's transfer function is changed to

$$H(s)|_{PLL} = \frac{\omega_n\left(2\xi - \frac{N^2\omega_n}{K_{PD}K_{VCO}}\right)s + N\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.19}$$

where $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}}$ and $\xi = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}\left(\tau_2 + \frac{N}{K_{PD}K_{VCO}}\right)}$.

Based on this improved filter, the natural frequency and damping factor can be designed independently.

2.2.3 Charge-pump PLL

A charge-pump PLL has two remarkable advantages over the traditional design with the phase detector. Firstly, the capture range is only limited by the

output frequency range of the VCO, where the capture range is defined as the range of frequencies over which the PLL will grab and lock the input signal. Secondly, the static phase error is zero if mismatches and offsets are negligible.

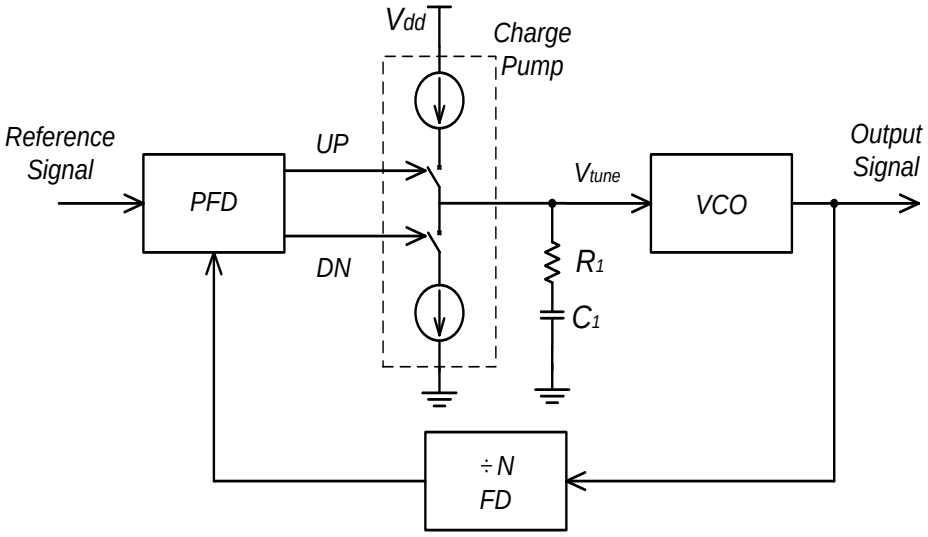

Figure 2.5: Topology of the charge-pump PLL

The topology of the charge-pump PLL with a simple loop filter is shown in Figure 2.5. The charge pump is driven by the *UP* and *DN* signals those are the PFD's output signals. The VCO's tuning voltage V_{tune} is controlled by charging or discharging of the charge pump. The transfer function of the charge pump is given by

$$K_\phi = \frac{I_d(s)}{\theta_e(s)} = \frac{I_{CP}}{2\pi} \tag{2.20}$$

where $I_d(s)$ is the charging or discharging current and I_{CP} is the average current over a cycle.

The impedance of the loop filter in the charge-pump PLL can be expressed as

$$Z(s) = R_1 + \frac{1}{C_1 s} \tag{2.21}$$

where R_1 and C_1 are the resistor and capacitor in series.

Thus, the transfer function of the forward path in the charge-pump PLL, including the PFD, the charge pump, the loop filter and the VCO, can be expressed as

$$H(s)|_{FW} = \frac{K_\phi K_{VCO} Z(s)}{s} = \frac{\frac{I_{CP}}{2\pi} K_{VCO}\left(R_1 + \frac{1}{C_1 s}\right)}{s} \tag{2.22}$$

Hence, the transfer function of the PLL is given by

$$H(s)|_{CPPLL} = \frac{\frac{I_{CP} K_{VCO}}{2N\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_{CP}}{2N\pi} K_{VCO} R_1 s + \frac{I_{CP}}{2N\pi C_1} K_{VCO}} \tag{2.23}$$

The natural frequency and damping factor can be obtained as

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2N\pi C_1}} \tag{2.24}$$

$$\xi = \frac{R_1}{2}\sqrt{\frac{I_{CP} K_{VCO} C_1}{2N\pi}} \tag{2.25}$$

The charge-pump PLL is currently prevailing in the RF system design, so any PLL in this research is defaulted as a charge-pump PLL.

2.3 Performance of a PLL

A frequency synthesizer is designed based on a PLL in many applications in which a frequency is required to be synthesized. The design of the frequency synthesizer depends on some specifications of the PLL's performance, such as reference spur, phase noise and lock time [16].

2.3.1 Reference spur

When the PLL is in the locked status, there is a periodic jitter in its VCO's tuning path, which has the same frequency as the reference frequency. Thus, the

spurious output is called reference spur, which is generally caused by leakage or mismatch of the charge pump. Normally, either the Banerjee's model [17] or the Maxim's model [18] is used to determine the reference spur level. To understand the causes of the reference spur, the Banerjee's model is introduced in detail.

Spur gain

Spur gain is the product of the VCO gain, the charge pump gain and the loop filter impedance evaluated at the spur frequency. Thus, it can be expressed as

$$SpurGain = 20log\left(\left|\frac{K_\phi \cdot Z(s) \cdot K_{VCO}}{s}\right|_{s=j2\pi f_{spur}}\right) \quad (2.26)$$

where *Z(s)* is the filter loop impedance and f_{spur} is the offset frequency that is a multiple of f_{ref}.

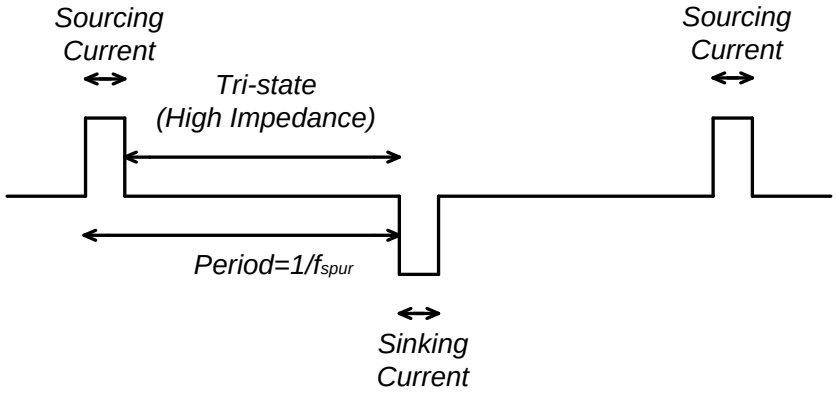

Figure 2.6: The charge pump output of the locked PLL

Leakage spurs

When the PLL is in the locked status, the charge pump periodically generates narrow pulses of currents. In Figure 2.6, it is shown that there is a long period of time between any two pulses, where the charge pump is in the

tri-state status with high impedance. However, there are still some parasitic leakages through the charge pump, the VCO and the capacitor in the loop filter. These parasitic currents cause a modulation in the tuning path of the VCO, and the reference spurs are produced. In [17],

$$LeakageSpur = BaseLeakageSpur + 20log\left|\frac{Leakage}{K_\phi}\right| + SpurGai \quad (2.27)$$

where *Leakage* refers to the charge pump current loss and *BaseLeakageSpur* is a universal constant at an approximate value of 16 dBc applicable to whatever type of integer PLL.

Pulse spurs

With the decrease of the leakage current in a currently available PLL, the spur level is also affected by pulse spurs. The charge pump in the locked PLL is activated for only short periods, generating positive and negative current pulses those do not change V_{tune} but cause some jitters in its tuning path. The pulse spurs are generated by these small pulses.

There are several factors those influence the width of these pulses, such as charge pump mismatch, unequal turn-on time of PMOS and NMOS transistors, and dead-zone elimination circuitry. In [17], the reference spurs produced by these factors can be expressed as

$$PulseSpur = BasePulseSpur + 40log\left(\frac{f_{spur}}{1\ Hz}\right) + SpurGain \quad (2.28)$$

where the value of *BasePulseSpur* differs with different frequency synthesizers.

Combination of leakage spurs and pulse spurs

Generally, the total spur level in the PLL is equal to the sum of both leakage

and pulse spurs, which can be expressed as

$$Spur = 10log\left(10^{LeakageSpur/10} + 10^{PulseSpur/10}\right) \quad (2.29)$$

To conclude the Banerjee's model, it can be pointed out that the prediction based on the model is simple and practical. However, the disadvantage of this model is that the prediction is based on some empirical constants. In addition, the Maxim's model [18] is used to overcome the problem.

2.3.2 Phase noise

Phase noise is an important parameter for the characterization of the frequency synthesizer, which has a great impact over the noise performance of the RF receiver [19]. Analog circuits in any frequency synthesizer introduce various types of non-idealities, so it is impossible that the PLL's output is an ideal sine wave at an oscillating frequency. Several prediction models of phase noise have been presented in [20] [21].

In [22], phase noise $\mathcal{L}\{\Delta\omega\}$ is defined as the ratio of the noise power in a bandwidth of 1 Hz at an offset frequency $\Delta\omega$ to the carrier power $P_{carrier}$. The result is a single-sided spectral noise density in the unit of dBc/Hz, where dBc indicates a measurement in dB relative to the carrier power.

$$\mathcal{L}\{\Delta\omega\} = 10log\left(\frac{P_{noise}}{P_{carrier}}\right) \quad (2.30)$$

The total phase noise at the PLL output is obtained through multiplying each source by its corresponding transfer function and adding all these resulting products [23] [24]. The phase noise of the PLL is further discussed in Chapter 6.

2.3.3 Lock time

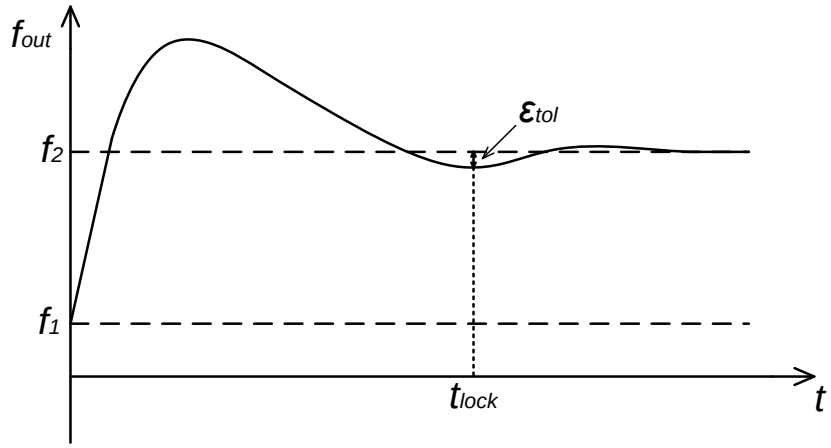

Figure 2.7: Transient response for a frequency change from f_1 to f_2

In a frequency synthesizer, the PLL's output frequency can be changed from one locked frequency f_1 to another frequency f_2 through the division ratio, as shown in Figure 2.7. This will cause successive changes in the phase error, the tuning voltage and the VCO's output frequency. Through this feedback mechanism, the PLL is locked again. The time required for this complete procedure is defined as lock time, which is an important requirement in the frequency synthesizer design.

Theoretically, the lock time is infinite and has an exponential behaviour. Therefore, the specific output frequency error tolerance ε_{tol} is introduced. The lock time of the PLL can be defined as

$$t_{lock} = \{t_{lock} : |f_{out}(t) - f_{out}(\infty)| < \varepsilon_{tol}\} \quad (2.31)$$

where $f_{out}(t)$ and $f_{out}(\infty)$ are the output frequency at the time t and at the PLL's steady state, respectively.

The analysis of the transient response can be obtained from a linear model. For the charge-pump PLL in Section 2.2.3, the lock time for the new division

ratio can be approximated by [17].

$$t_{lock} = \frac{-ln\left(\frac{\varepsilon_{tol}}{f_{out}(t)-f_{out}(\infty)}\cdot\sqrt{1-\xi^2}\right)}{\xi\cdot\omega_n} \tag{2.32}$$

2.4 Voltage-Controlled Oscillator

VCO is one of the most critical blocks in a PLL, which operates at the highest frequency and generally dominates the out-band phase noise. As an oscillator, its resonant frequency is controlled by a DC voltage V_{tune} from the charge pump through the loop filter. In addition, other performance parameters of the VCO, such as the tuning range, power consumption and output amplitude, are also important for the design of frequency synthesizers.

2.4.1 Concept of oscillation

To design a VCO with good performances, such as low phase noise and low power consumption, the fundamental concept of oscillation must be understood. Most oscillators can be viewed as feedback circuits [12], where noise in the circuit is amplified to a finite output at a selected angular frequency ω_0, as shown in Figure 2.8.

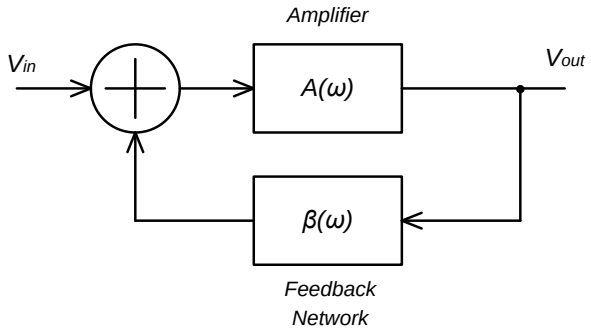

Figure 2.8: Feedback diagram of an oscillator

$A(\omega)$ and $\beta(\omega)$ are the gains of the amplifier and the feedback network, respectively. Thus, the transfer function of the oscillator can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{A(\omega)\beta(\omega)}{1-A(\omega)\beta(\omega)} \tag{2.33}$$

According to Barkhausen's Criteria, the system will oscillate at ω_0 with the infinite closed-loop gain under the following conditions: (1) the open-loop gain is equal to unity, i.e. $A(\omega_0)\beta(\omega_0) = 1$; (2) the total phase shift of the loop is equal to $2\pi n$, where n is an integer or $Im\{A(\omega_0)\beta(\omega_0)\} = 0$. In order to ensure the proper startup of the oscillation, the loop gain is typically chosen to be 2~3 times of the required value to counter the temperature and process variations [25].

2.4.2 Noise performance of an oscillator

In the design of an oscillator, the noise sources can affect both the amplitude and phase of the output signal. The output signal according to time can be modeled by

$$V_{out}(t) = A(t) \cdot sin[\omega_0 t + \theta(t)] \tag{2.34}$$

where $A(t)$ and $\theta(t)$ are the amplitude and phase from the output signal, respectively. The amplitude noise can be reduced by the amplitude-limiting mechanism in the oscillator, so the amplitude noise is usually negligible [26]. On the other hand, phase noise can be regarded as the fluctuation of the zero crossing locations of a signal. The detailed explanation of this fluctuation can be found in [22].

The Leeson's phase noise model

The analysis in the frequency domain is based on the Leeson's phase noise model, which assumes that the oscillator is a linear time invariant (LTI) model. The phase noise at the oscillator's output is theoretically estimated based on some certain simplifications and empirical modifications those introduce to fit the final spectrum to the real case. Thus, the phase noise can be expressed as

$$\mathcal{L}\{\Delta\omega\} = 10log\left[\frac{2FkT}{P_{sig}}\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\omega_{1/f}^3}{|\Delta\omega|}\right)\right] \qquad (2.35)$$

where F is an empirical parameter, k is the Boltzman's constant, T is the absolute temperature, P_{sig} is the average power dissipated in the resistive part of the tank, $\Delta\omega$ is the offset frequency from the carrier, and $\omega_{1/f}$ is the angular frequency of the corner between the $1/f^3$ and $1/f^2$. The phase noise of the oscillator is shown in Figure 2.9.

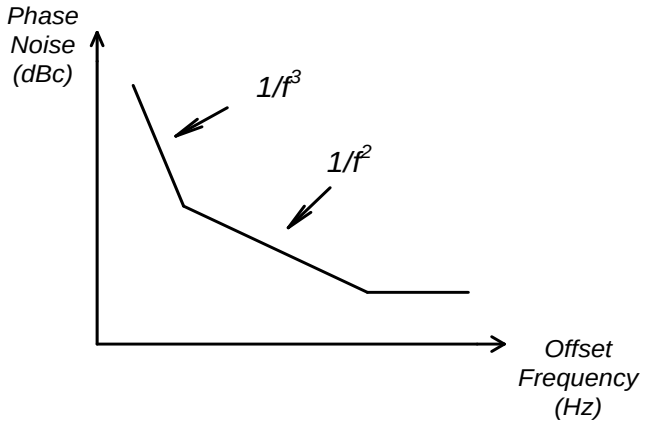

Figure 2.9: Spectrum of the oscillator's phase noise

The Hajimiri's phase noise model

This Hajimiri's phase noise model is more complex than the Leeson's phase noise model, but its theoretical prediction adapts well to the characteristic of a real oscillator. In this model, the oscillator is assumed as a linear time variant

(LTV) model and the influence of total phase noises from both active and passive elements is studied based on the impulse sensitivity function (ISF), which is a dimensionless, frequency-independent and amplitude-independent periodic function with a period of 2π [27]. If an impulse charge is introduced into the capacitance seen from the output node of an oscillator in its steady state, amplitude and phase errors will be generated. When the charge is injected into the model, the phase error is the function of the time τ. Hence, the unit impulse response for the excess phase can be expressed as

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{2.36}$$

where q_{max} is the maximum charge displacement across the capacitor on the node and $u(t-\tau)$ is the unit step. $\Gamma(\omega_0\tau)$ is the ISF, which is a function of the waveform or the shape of the limit cycle governed by the nonlinearity and the topology of the oscillator. As a result, the sideband power of the phase noise caused by the charge injection can be expressed as

$$S_n(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \tag{2.37}$$

where Γ_{rms}^2 is the rms value of the ISF and $\overline{i_n^2}/\Delta f$ is the input noise source power spectral density.

2.4.3 Ring oscillator

Ring oscillators are commonly used in a PLL-based frequency synthesizer or a clock recovery circuit [28] [29] [30] [31]. The implementation of the ring oscillator in the CMOS technology is easier than an LC-tank oscillator, because it consists of only transistors and hence requires smaller silicon area [32] [33] [34]. It is usually designed by cascading an odd number of inverters in a loop

configuration [35] [36] [37]. A three-stage ring oscillator is shown in Figure 2.10 as an example.

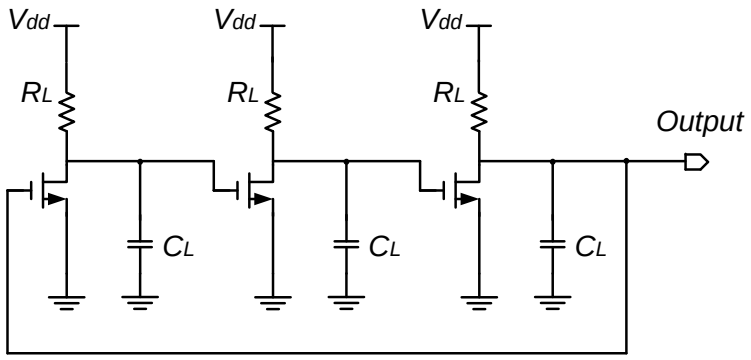

Figure 2.10: A three-stage ring oscillator

Linear model

For the circuit in Figure 2.10, neglecting the effect of the gate-drain overlap capacitance, the transfer function of each stage can be expressed as [12]

$$H_1(j\omega) = \frac{-A_0}{1+\frac{j\omega}{\omega_0}} \tag{2.38}$$

where A_0 and ω_0 are the gain and the -3-dB bandwidth of each stage. Thus, the loop gain of the ring oscillator, including three identical stages, can be given by

$$H(j\omega) = \left(H_1(j\omega)\right)^3 = -\frac{A_0^3}{\left(1+\frac{j\omega}{\omega_0}\right)^3} \tag{2.39}$$

For the oscillation of the three-stage ring oscillator, the phase shift is equal to 180 ° and hence each stage contributes 60 °. Thus, the oscillating angular frequency can be obtained by

$$\omega_{osc} = \omega_0 \, tan\, 60° = \sqrt{3}\omega_0 \tag{2.40}$$

At ω_{osc}, the magnitude of the loop gain can be expressed as

$$\frac{A_0^3}{\left[\sqrt{1+\left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^3} = 1 \tag{2.41}$$

Substituting (2.40) into (2.41), it can be obtained that A_0 is equal to 2.

Frequency tuning

From large signal analysis, the oscillating frequency of the ring oscillator can be decided by the time delay of each stage [38]. The oscillating frequency can be expressed as

$$f_0 \approx \frac{1}{2Nt_{delay}} \approx \frac{I_p}{2NC_LV_p} \quad (2.42)$$

where t_{delay} is the time delay for each delay cell, I_p is the current passing through each delay cell, C_L is the load capacitance of each stage and V_p is the peak output voltage. Therefore, the oscillating frequency can be tuned by using variable capacitors, or variable supply voltage, or the current-starved method [22]. Generally, the ring oscillator has larger tuning range than an LC-tank oscillator [39].

Phase noise

In the absence of a frequency selective network, the ring oscillator is easy to implement with the current integration technology, but suffers from high phase noise level [35]. Compared to VCOs using LC tank with the operating frequency mainly determined by the passive inductance and capacitance, VCOs in the form of ring oscillators with active delay cells are more susceptible to supply noise as the operating frequency depends heavily on the supply voltage [40]. The switching activities in a ring oscillator introduce a lot of disturbances in the oscillator. In addition, the multiple-stage design also increases the noise level, making the ring oscillator unpopular in RF systems. A general resulting phase noise of the ring oscillator is given by

$$\mathcal{L}\{\Delta\omega\} = 10log\left[A_k \cdot \frac{kTR_n}{V_A^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \quad (2.43)$$

where A_k is the factor depending on the noise generation mechanism studied, R_n is the equivalent noisy resistor, V_A is the voltage amplitude of the signal, ω_0 is the oscillation frequency, and $\Delta\omega$ is the angular offset frequency. The way to improve the phase noise is to decrease R_n, but this inherently implies larger power consumption.

2.4.4 LC-tank oscillator

The general topology for an LC-tank oscillator is shown in Figure 2.11. It consists of an active circuit and an LC tank that is the key block in the VCO, so it is instructive to analyze the LC tank in the oscillator.

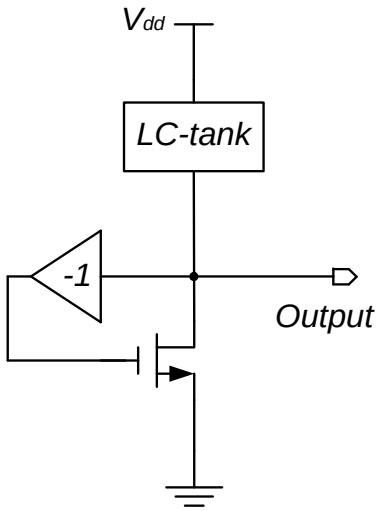

Figure 2.11: General topology of an LC-tank oscillator

LC tank

In an ideal LC tank as shown in Figure 2.12 (a), an inductor L_1 and a capacitor C_1 are connected in parallel. Thus, the angular resonant frequency is given by

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{2.44}$$

where the angular resonant frequency can be tuned in different ways [41] [42] [43].

At this frequency, the impedances of the inductor and capacitor are $jL_1\omega_0$ and $1/(jC_1\omega_0)$, respectively. As a result, both the impedances are equal and opposite, thereby yielding an infinite impedance.

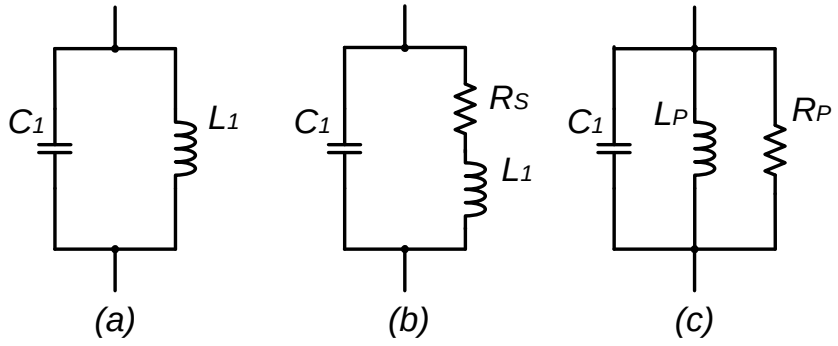

Figure 2.12: Models of three simplified LC tanks

In practical, inductors suffer from resistive loss in the model, which is shown in Figure 2.12 (b). The quality factor of the LC-tank Q is defined as $\omega L_1/R_s$, which is an important factor to decide the phase noise of the LC-tank oscillator [44]. The model can be converted to the equivalent model in Figure 2.12 (c). Thus, the parallel inductor and resistor can be expressed as

$$L_P = L_1\left(1 + \frac{R_S^2}{L_1^2\omega^2}\right) \tag{2.45}$$

$$R_P = \frac{L_1^2(\omega^2 + R_S^2/L_1^2)}{R_S} \tag{2.46}$$

The overall impedance does not go to infinity at any frequency but reaches a peak in the vicinity of ω_0. Note that the actual resonant frequency has some dependency on R_S.

Types of LC-tank oscillators

An LC-tank oscillator can be designed as either single-ended or differential type. The differential type has higher rejection of common mode interferers, stronger attenuation of even-order harmonics and lower phase noise [45] than the single-ended type. Therefore, the differential type is commonly required in most applications although it needs more components and power consumption.

Furthermore, the differential oscillators can be integrated on-chip according to different topologies, each having its own advantages and shortcomings in connection to the power dissipation, the frequency tuning range, the phase noise and the voltage swing [46]. They can be classified into NMOS type [25], PMOS type and CMOS type [47]. In Figure 2.13 (a), it is shown that the active circuit of the oscillator is formed by a pair of cross-coupled NMOS, which has the main advantage of simplicity and hence has low noise and requires low supply voltage. The PMOS type uses two PMOS transistors instead of two NMOS transistors. The main problem lies in the usual worse performance of PMOS transistor than that of NMOS transistor [16]. Generally, PMOS transistor requires three times bigger areas than NMOS transistor in order to achieve the same negative resistance with the same power consumption. As a result, the PMOS type is not frequently used. In Figure 2.13 (b), it is shown that the CMOS-type oscillator uses both NMOS and PMOS transistors to regenerate the signal. It requires lower current consumption than the other two types for the same output signal.

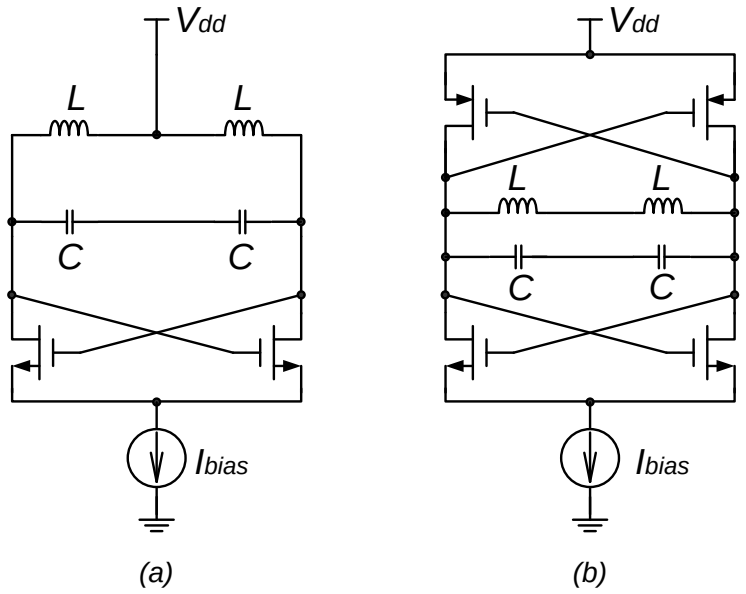

Figure 2.13: (a) NMOS and (b) CMOS types of LC-tank oscillators

Phase noise

Generally, an LC-tank oscillator has smaller phase noise than a ring oscillator, and it is less sensitive to variations of MOSFETs' characteristics and fluctuations of supply voltage and temperature because of the stability of the passive on-chip components [48]. In [27], based on these assumptions (1) the LC-tank oscillator is an LTI model, (2) all noise sources are stationary, (3) only the noise in the vicinity of the resonant frequency is important and (4) the noise-free waveform is a perfect sinusoid, the phase noise of an LC-tank oscillator is given by

$$\mathcal{L}\{\Delta\omega\} = 10log\left[\frac{1}{2}\cdot\frac{kT}{V_{max}^2}\cdot\frac{1}{R_p\cdot(C\omega_0)^2}\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \qquad (2.47)$$

where $\Delta\omega$ is the angular offset frequency, R_p is the parallel resistor, C is the tank capacitor, and V_{max} is the maximum voltage swing across the tank.

Furthermore, the FoM is commonly used to determine the phase noise performance of a VCO, with respect to the power and oscillation frequency at a

certain offset frequency [49].

$$\text{FoM} = 10log\left(\frac{\left(\frac{\omega_0}{\Delta\omega}\right)^2}{P_{VCO}L(\Delta\omega)}\right) \quad (2.48)$$

where P_{vco} is the VCO's total power consumption in mW.

2.4.5 Comparison between ring oscillator and LC-tank oscillator

The characteristics of both ring and LC-tank oscillators are summarized and shown in Table 2.1. Ring oscillator is suitable to be used in some applications for low-frequency operation and low requirement on the phase noise. It is because that ring oscillator has low power, small size and wide tuning range.

LC-tank oscillator is used in some applications for high-frequency operation and high requirement on the phase noise. However, it has high power consumption and large chip size due to its on-chip inductor. In this thesis, the VCOs are designed based on the LC-tank oscillator. Thus, the designs with LC-tank VCO focus on reducing the power consumption.

Table 2.1: Comparison between ring oscillator and LC-tank oscillator

	Ring oscillator	LC-tank oscillator
Operation frequency	Low	High
Tuning range	Wide	Narrow
Phase noise	High	Low
Power consumption	Low	High
Chip size	Small	Large

2.5 Frequency Divider

Frequency divider is another challenging block in a PLL, especially for high-frequency and low-power operation. In the feedback path, the frequency divider can be designed with a fixed division ratio or with a programmable division ratio for channel selection in a frequency synthesizer. Moreover, the division ratio is correct only when the input frequency stays within a certain range that is denoted as the operation range of the frequency divider.

2.5.1 Programmable frequency divider

For channel selection, it is necessary to implement a programmable frequency divider, which has wide bandwidth and variable division ratio.

Reloadable digital counter

A reloadable digital counter has a frequency division ratio continuously ranging from 3 to 2^N, where N is the number of divide-by-2 stages [50]. In the reloadable digital counter, the number of the input pulses is accumulated until it is equal to a value of *PRESET* when the counter is reloaded. By changing the value of *PRESET*, a programmable division ratio is achieved. However, the counter has poor performance in the high-frequency and low-power operation because the additional logic gates besides the divide-by-2 units introduce additional power consumption and propagation delays. Therefore, the reloadable digital counter is usually limited to low-frequency operation.

Pulse-swallow frequency divider

As shown in Figure 2.14, a pulse-swallow integer frequency divider is the most common method to achieve a programmable frequency division for high-frequency and low-power operation [51] [52]. It consists of a dual-modulus prescaler, a swallow counter and a programmable counter. Based on the topology, the size of counters can be significantly reduced and the programmable division ratio is $N \times P+S$, where N, P, and S are decided by the prescaler, the programmable counter and the swallow counter, respectively. In addition, the dual-modulus prescaler can perform the two division ratios of N and $N+1$, which is switched on or off by the signal of a *Modulus Control* from the swallow counter. The dual-modulus prescaler, such as a divide-by-4/5 or divide-by-2/3 frequency divider, can be implemented based on a phase switching technique or a synchronous divider.

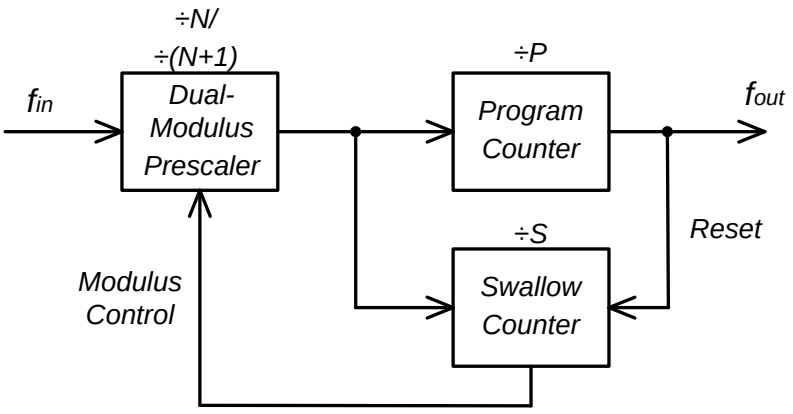

Figure 2.14: Topology of a pulse-swallow frequency divider

2.5.2 Regenerative frequency divider

Regenerative frequency divider is also called Miller divider, as shown in Figure 2.15 [53]. In the frequency divider with a division ratio of n, the input frequency f_{in} is mixed with the feedback frequency f_{fb} to generate two

frequencies $f_{in}+f_{fb}$ and $f_{in}-f_{fb}$. After passing through a low pass filter (LPF), only the wanted frequency of $f_{in}-f_{fb}$ is selected as the output frequency f_{out} while the other one is suppressed by the LPF. In the feedback path, there is a frequency multiplier with a multiplier of $\times(n-1)$. Thus, f_{fb} is equal to $(n-1)f_{out}$. However, the frequency divider requires many functional blocks such as frequency multiplier and mixer to guarantee the frequency division. As a result, it is not the best solution for low-power system [54].

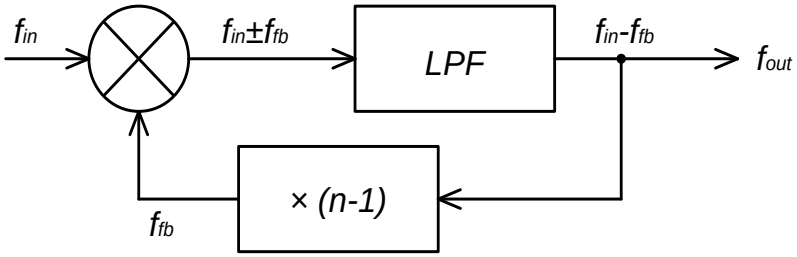

Figure 2.15: Topology of a regenerative frequency divider

2.5.3 D-flip-flop frequency divider

In Figure 2.16, it is shown that a simple divide-by-2 D-flip-flop (DFF) frequency divider consists of two D-latches in cascade and in a negative feedback configuration. Its digital operation provides the advantage on suppressing the sensitivity to waveform distortions. Dependent on the different types of DFFs, the DFF frequency dividers are further categorized into two groups: dynamic and static DFF frequency dividers.

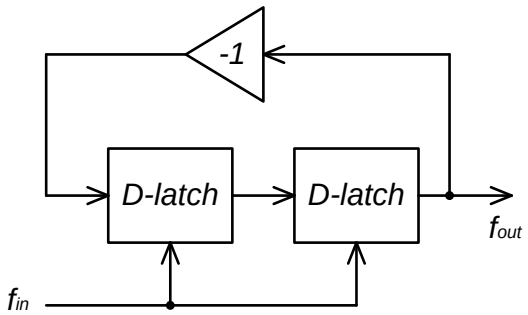

Figure 2.16: Topology of a DFF frequency divider

Dynamic DFF frequency divider

If the frequency divider dissipates most power during charging and discharging, it is called dynamic frequency divider. The dynamic frequency divider consumes less DC power than static frequency divider. However, its maximum operation frequency is lower than that of static frequency divider.

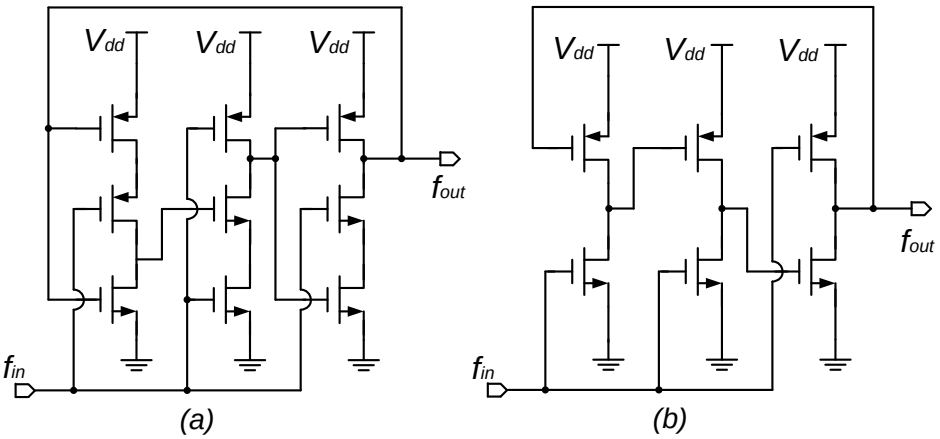

Figure 2.17: (a) TSPC frequency divider and (b) E-TSPC frequency divider

Shown in Figure 2.17 (a), the true-single-phase-clock (TSPC) structure is used to design a dynamic DFF frequency divider. In the DFF, the dynamic latch is driven by a single clock phase, thus avoiding the clock skew problem. Another advantage of the circuit is the reduced capacitive loads. With lower

capacitance, the *W/L* of the transistors can be decreased and the power consumption is decreased.

Furthermore, the extended-TSPC (E-TSPC) structure is shown in Figure 2.17 (b) [55]. In the circuit, the stacked MOS structure is avoided. Thus, the switching frequency is increased and all the transistors are free from body effect. As a result, E-TSPC structure allows a higher operating frequency, although it has larger static power dissipation than TSPC structure.

Static DFF frequency divider

In contrast to the dynamic frequency divider, a static frequency divider constantly dissipates DC current. However, its maximum operation frequency is higher than that of a dynamic frequency divider [56]. Shown in Figure 2.18, the CML structure is used to design a static DFF frequency divider. The maximum operation frequency is generally limited by the parasitic capacitances.

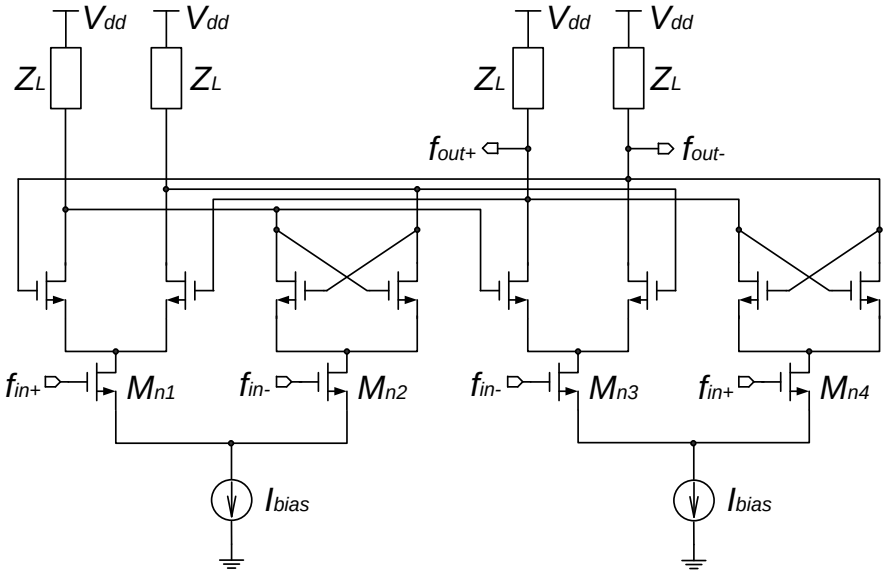

Figure 2.18: CML frequency divider

However, with scaling-down of the supply voltage, the voltage headroom is a critical issue due to its cascaded structure. Therefore, the pseudo-differential topology can be used to improve the structure [57]. In order to reduce voltage headroom, the tail current source is removed. Thus, the four NMOS transistors M_{n1}, M_{n2}, M_{n3} and M_{n4} are used to decide the static bias current as well as to sense the input signal by their gates connecting to the input signal.

Initially, the four static loads Z_L are implemented by fixed resistors those suffer seriously from the process variations. In [58], the resistors are replaced by four transistors, called active loads or dynamic loads. In the 'sense' mode, the loaded transistors are on and their resistances are small. Thus, the RC constant is small and the switching speed is fast. In the 'hold' mode, the loaded transistors are off and their resistances are large. Consequently, the RC constant becomes large and the switching speed is slow. Furthermore, the transistors can be replaced by four inductors for inductive peaking to reduce the rise and fall times, and thereby enhance the operation frequency [59].

2.5.4 Injection-locked frequency divider

The phenomenon that an oscillator is locked by injection of a periodic signal has been studied for many decades [10] [60] [61]. In many prevalent transceivers and frequency synthesizers, the phenomenon has attracted more interest from many outstanding RF researchers [54] [11] [62]. Based on an ILO, many practical circuits can be designed for different applications.

Dependent on the ratio of the input frequency to the resonant frequency, three types of injection locking can be defined: sub-harmonic [63] fundamental harmonic [64], super-harmonic [54]. An ILFD is the type of super-harmonic

injection locking. Its input frequency is in the vicinity of the *n*-th harmonic of the resonant frequency, where *n* is an integer. Without any input, the ILFD performs as a free-running oscillator, which resonates at an angular frequency ω_0. With a finite input signal operating at ω_{in}, the ILFD's output angular frequency ω_{out} is shifted from ω_0 to $(1/n)\omega_{in}$.

The ILFD performs its frequency division correctly only when the input frequency stays within a range, denoted as the ILFD's operation range, which is dependent on the locking range of the ILO. Comparing with other types of frequency dividers, the ILFD has higher operation frequency and lower power consumption, but exhibits a narrower operation range. Therefore, in the ILFD design, the operation range is one of the most important parameters, which has been analyzed in [11] [54].

In addition, the ILFD can be designed based on a ring oscillator [65] or an LC-tank oscillator [62].

Ring-oscillator-based ILFD

Typically, the ring-oscillator-based ILFD has a wider operation range than the LC-tank-oscillator-based ILFD [66]. The schematic of the ring-oscillator-based divide-by-2 ILFD in [67] is shown in Figure 2.19 (a). The ring oscillator consists of three stages of NMOS inverters with PMOS active loads in a ring. The input signal is injected into one stage of inverter by connecting an NMOS transistor to the NMOS inverters in series. However, this architecture requires higher supply voltage.

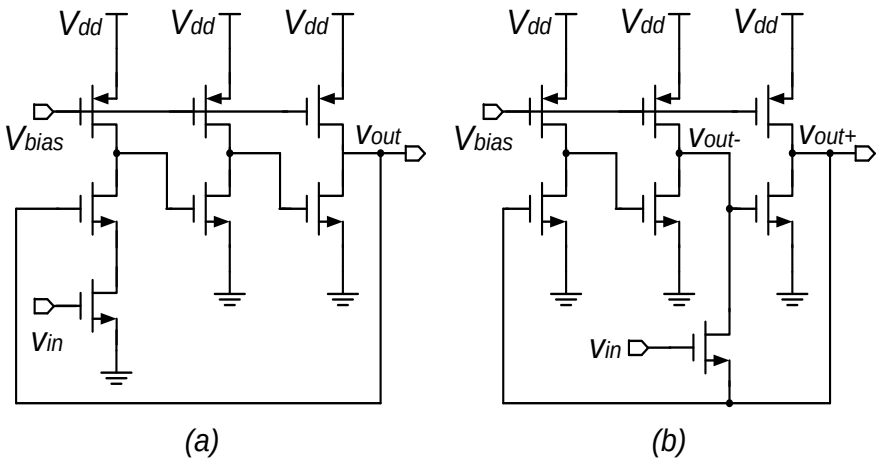

Figure 2.19: Ring-oscillator-based ILFDs with (a) single injection (b) quasi-differential output

A quasi-differential ILFD in [67] is used to solve this problem, which is shown in Figure 2.19 (b). A switch transistor is inserted between two inverter outputs to modulate the oscillation frequency, where the voltages v_{out+} and v_{out-} at two output points can be used as quasi-differential outputs. When the switch is turned on, the output nodes of the second and third stages are shorted. Consequently, v_{out+} and v_{out-} are forced to be equal. If v_{out+} and v_{out-} are defined as the differential output voltages, the positive peaks of the input signal will be locked to the zero-crossing points of the differential output voltage in locked state. When the ILFD is injection-locked, the output frequency is equal to half of the input frequency.

More stages of inverters can be used to enhance the division ratio. As an example in [68], the ring-oscillator-based ILFD has the division ratio of 8, which consists of five stages of inverters. In addition, multi-phase injection with a specific phase difference can maximize the locking range of the ring-oscillator-based ILFD [69] [70] [71].

LC-tank-oscillator-based ILFD

The LC-tank-oscillator-based ILFD is frequently used at higher operation frequency, which is also called LC-tank ILFD. The conventional LC-tank ILFD with tail injection is shown in Figure 2.20 (a), which has the division ratio of 2. The main disadvantages are its large input capacitance and its narrow operation range [62]. For improvement on the performance of the ILFD, another type of ILFD is designed based on the topology of direct injection, as shown in Figure 2.20 (b).

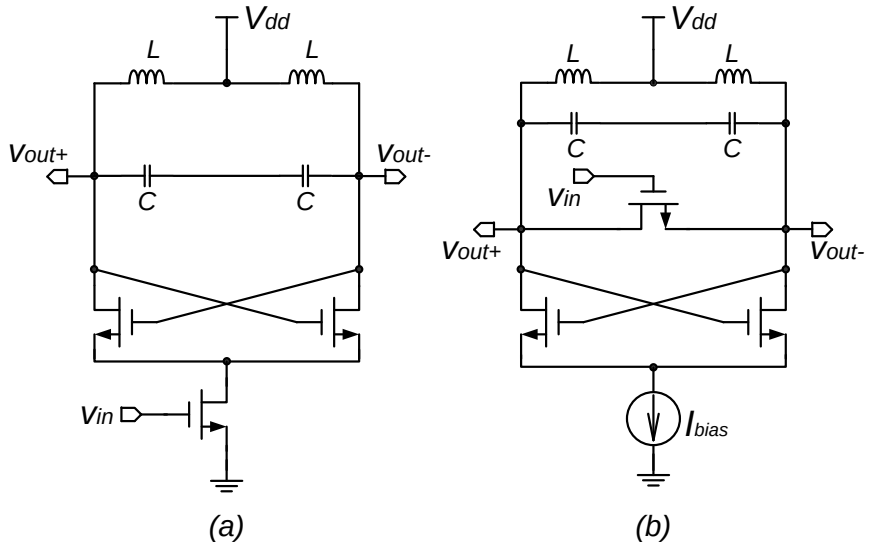

Figure 2.20: LC-tank ILFDs (a) with tail injection (b) with direct injection

Despite the topology of direct injection, the LC-tank ILFD's operation range is narrower than other types of frequency dividers, especially for higher division ratio [72] [73] [74]. Hence, it is important to optimize the ILFD's operation range, which is analyzed in detail in Chapter 3. For excellent performance in different RF system designs, the LC-tank ILO can be also used as an ILFM [75] [76]. The design of ILFM is discussed in Chapter 5 and Chapter 6.

2.5.5 Comparison among different frequency dividers

Different frequency dividers are summarized and compared based on four main characteristics in Table 2.2. It is observed that only ILFD and static DFF frequency divider (FD) can be used for high-frequency operation. ILFD is preferred because it has lower power consumption than static DFF FD. However, it is a critical limitation that the division ratio of a conventional ILFD is fixed. Therefore, it is beneficial to design an ILFD with variable division ratio.

Table 2.2: Comparison among different frequency dividers

	Programmable FD	Regenerative FD	Dynamic DFF FD	Static DFF FD	ILFD
Variable division	Yes	Yes	Yes	Yes	No
Operation frequency	Low	Low	Low	High	High
Operation range	Wide	Wide	Wide	Medium	Narrow
Power consumption	Low	High	Low	High	Medium

2.6 Injection-Locked Oscillator

As discussed above, the ILFD or ILFM is designed based on an ILO. For low phase noise and high frequency operation, the ILO is usually implemented based on the structure of an LC-tank oscillator rather than that of a ring oscillator.

2.6.1 Conceptual model of ILO

To design an ILO with good performance, the fundamental concept of ILO should be understood first. The models of both a free-running oscillator and an

ILO are shown in Figure 2.21 (a) and (b), respectively.

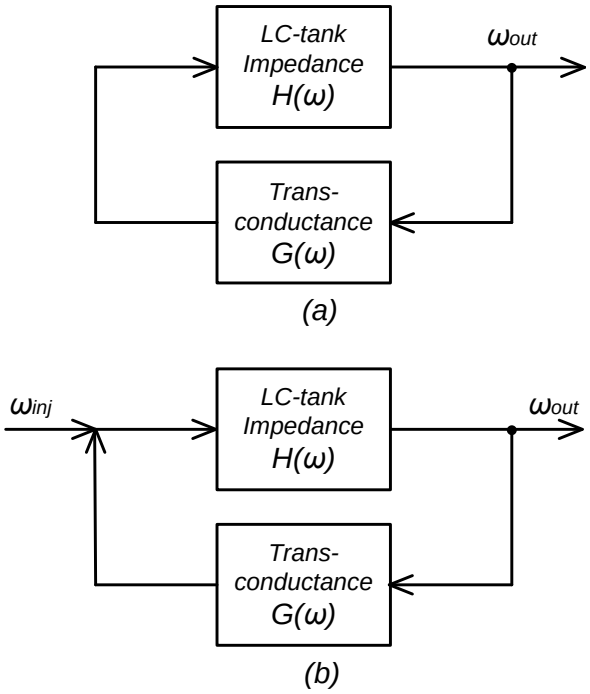

Figure 2.21: Models of (a) a free-running oscillator and (b) an ILO

If no signal is injected into the oscillator, the oscillator in Figure 2.21 (a) will be at the free-running status, where its output angular frequency ω_{out} is equal to the free-running angular frequency ω_0. If a signal at an angular frequency ω_{inj} is injected into the oscillator, the oscillator in Figure 2.21 (b) will be injection-locked, where ω_{out} is equal to ω_{inj}.

The conceptual model of an ILO [11] is shown in Figure 2.22, which consists of an LC tank, an NMOS transistor *M*, an inverter and a current source. Without injection, ω_{out} is equal to $\omega_0 = 1/\sqrt{LC}$, where L and C are cancelled. Thus, the LC tank does not contribute to any phase shift. The current I_{tank} through the LC tank is equal to I_{osc} that passes through the NMOS transistor *M*.

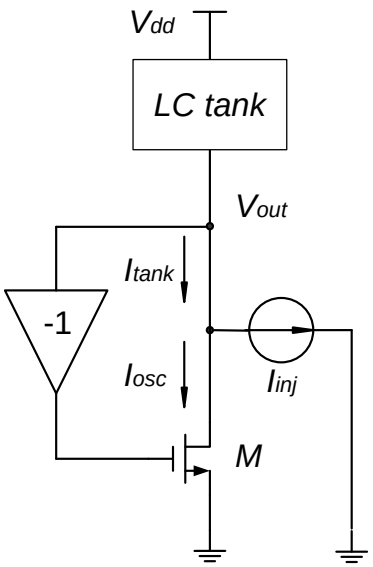

Figure 2.22: Conceptual model of an ILO

I_{inj} is a current input from the current source, which is injected into the oscillator. According to Kirchhoff's Law, I_{tank} is equal to the vector-sum of I_{inj} and I_{osc}. In Figure 2.23 (a), it is shown that the phase α between I_{tank} and I_{osc}, as well as the phase β between I_{inj} and I_{osc}, is produced by I_{inj}.

In Figure 2.23 (b), it is shown that ω_{out} is shifted away from ω_0 due to the phase shift of α. If ω_{out} is not equal to ω_{inj}, both α and β are changed continuously. Finally, the ILO becomes stable when a specific phase shift of α is produced, which makes ω_{out} equal to ω_{inj}.

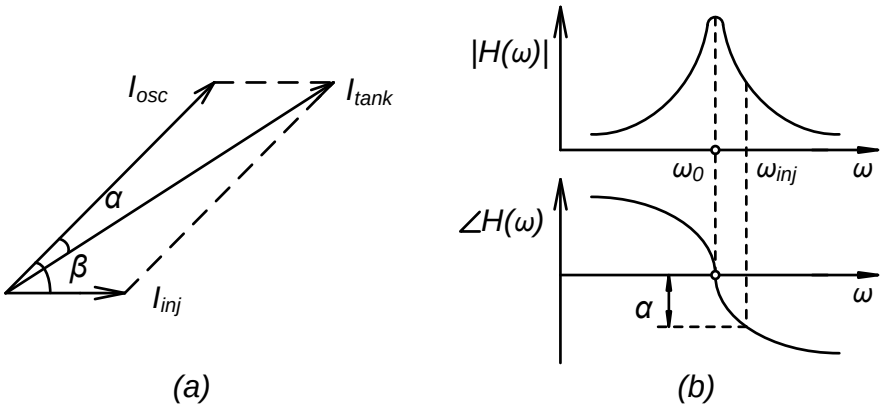

Figure 2.23: (a) Phasor diagram and (b) open-loop characteristic of the conceptual model

2.6.2 Important benefits brought by the ILO

An important benefit brought by the ILO is to amplify a small input with large voltage gain. With small AC input signal and low DC power consumption for oscillation, the ILO can provide large output signal. Comparing with a conventional amplifier, the ILO has an obvious advantage on the voltage gain, especially when the input signal is small.

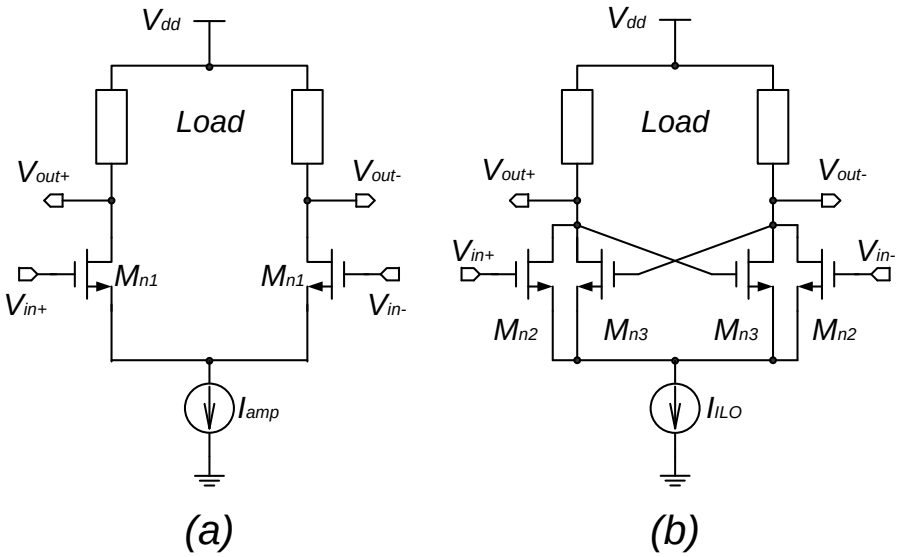

Figure 2.24: Schematics of (a) a conventional amplifier and (b) an ILO

Both a conventional amplifier and an ILO are shown in Figure 2.24 (a) and (b). Both the two schematics are only basic models to be used for comparisons. With the same supply voltages and bias currents (I_{amp}=I_{ILO}), the simulation results for the both circuits are shown in Figure 2.25.

The ILO has higher voltage gain than the conventional amplifier. With a small input, the conventional amplifier's output is small but the ILO has consistently larger output signal. Therefore, it is used extensively for the proposed circuits in this thesis.

However, the ILO has narrower operation range than the amplifier. In this

research, it is important to widen the operation range when the ILO is used in the proposed circuits. In addition, the ILO can be designed to improve the phase noise. When a frequency synthesizer is designed with the ILO in a frequency multiplier, the output phase noise of the frequency synthesizer can be considerably suppressed by the ILFM as discussed in Chapter 6.

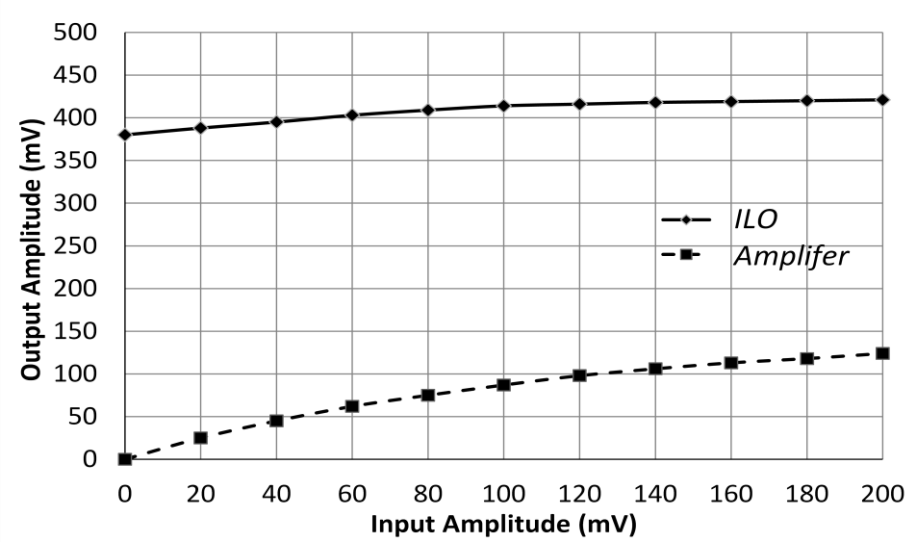

Figure 2.25: Simulated output amplitude versus input amplitude for the amplifier and the ILO models

2.7 Summary

In this chapter, the topology of a basic PLL is introduced, then its operation and transfer function are analyzed based on a linear model. Moreover, the performances of the PLL, such as reference spur, phase noise and lock time, are discussed. Finally, the most challenging blocks, such as VCO and frequency divider, are reviewed.

In Section 2.4, the concept of oscillation and VCO's noise performance are studied. Both ring oscillator and LC-tank oscillator are introduced separately. With comparisons between these two types, the VCO's performance, such as

frequency tuning and phase noise, are discussed. Finally, it is decided that the LC-tank oscillator is used in the research.

In Section 2.5, four types of frequency dividers, such as programmable frequency divider, regenerative frequency divider, DFF frequency divider and ILFD, are introduced. Among these frequency dividers, the LC-tank ILFD is the most suitable to be used in a PLL for high-frequency and low-power operation.

In Section 2.6, the ILO is analyzed based on its conceptual mode and its important benefits are discussed for using in high-frequency and low-power circuits.

CHAPTER 3

Novel Dual-Modulus Injection-Locked Frequency Divider

A dual-modulus frequency divider is widely used as a prescaler in a programmable frequency divider for channel selection in a frequency synthesizer [51] [77]. Generally, its two division ratios are n and n+1, where n is an integer. For example, n=4 in the divide-by-4/5 frequency divider [78], n=8 in the divide-by-8/9 frequency divider [51], and n=128 in the divide-by-128/129 frequency divider [79]. The division ratio is selected by a binary input, which is named as Modulus Control, *MC*. A divide-by-2/3 circuit is the basic unit, which can be used to build a dual-modulus frequency divider with higher division ratio.

3.1 Divide-by-2/3 Frequency Divider

In Section 2.5, different types of divide-by-2 frequency divider have been introduced, such as dynamic DFF, static DFF and ILFD. Correspondingly, a divide-by-2/3 frequency divider can be designed based on a modified divide-by-2 frequency divider with the binary input of the modulus control.

3.1.1 Dynamic divide-by-2/3 frequency divider

A dynamic divide-by-2/3 frequency divider consists of dynamic latches, which is faster and more compact than a static one [77]. Compared with the classical TSPC circuit, the E-TSPC circuit avoids the stacked MOS structure, so

all the transistors in this circuit are free from the body effect. For these reasons, E-TSPC logic can be used for higher operating frequencies. In [77], the divide-by-2/3 frequency divider is designed based on the E-TSPC logic. Its topology and schematic are shown in Figure 3.1 (a) and (b), respectively. The AND gate and OR gate in Figure 3.1 (a) are realized by adding only one transistor each in Figure 3.1 (b).

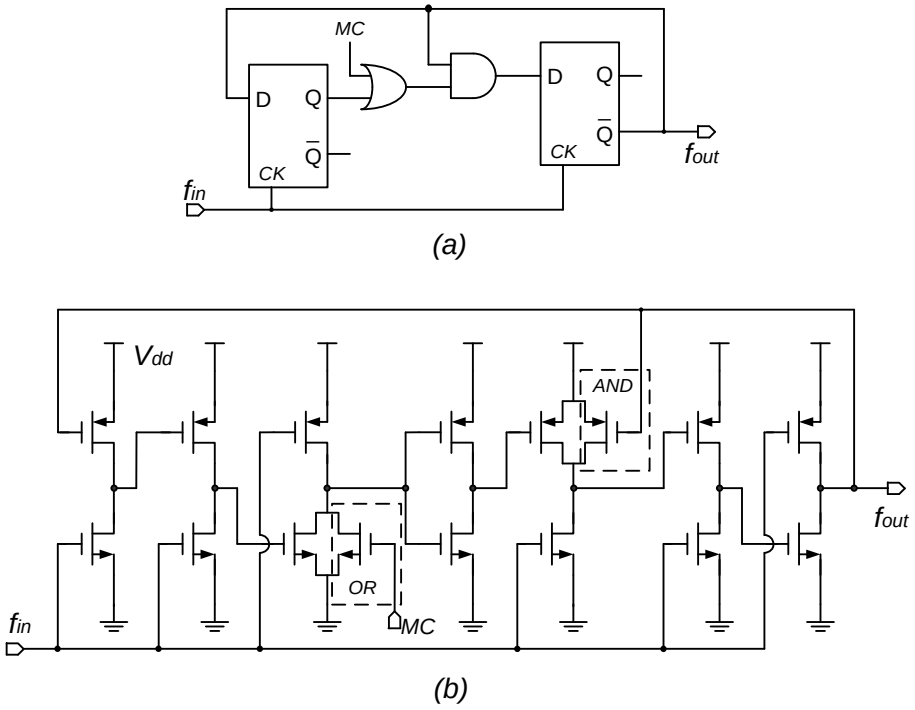

Figure 3.1: (a) Topology and (b) schematic of the dynamic divide-by-2/3 frequency divider

3.1.2 Static divide-by-2/3 frequency divider

A divide-by-2/3 frequency divider can be implemented based on a static circuit, which consists of static latches. As a static CMOS logic, the CML circuit has small internal voltage swing for high-frequency operation [56]. In [51], the divide-by-2/3 frequency divider is designed based on the static logic. Its topology and schematic are shown in Figure 3.2 (a) and (b), respectively. In

order to increase the maximum operation speed, the topology in Figure 3.2 (a) is used instead of the topology in Figure 3.1 (a). The schematic of the NOR/DFF combination is shown in Figure 3.2 (b), where V_b is the bias voltage.

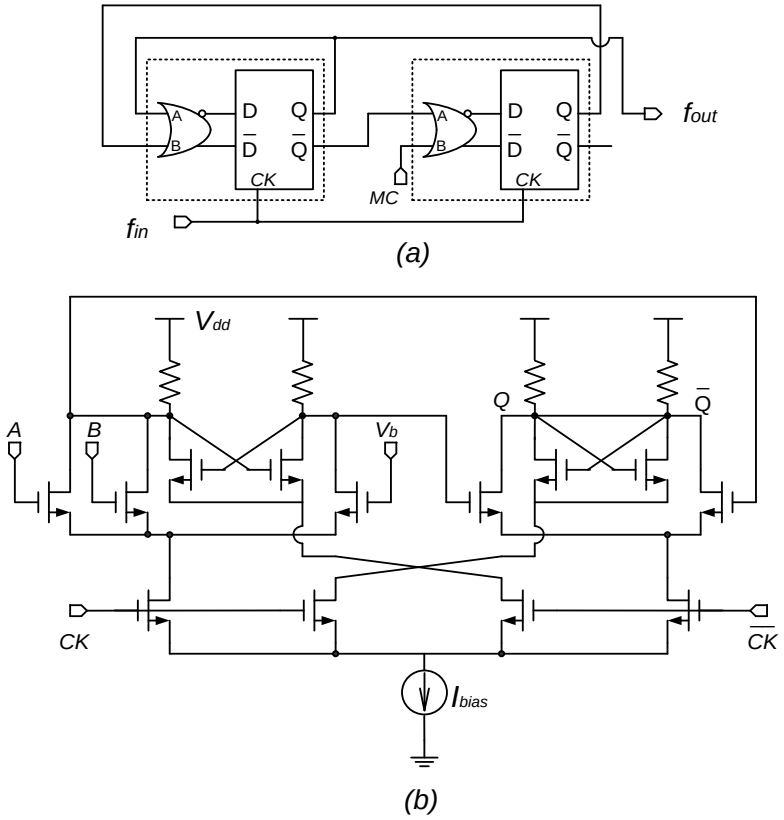

Figure 3.2: (a) A static divide-by-2/3 frequency divider and (b) schematic in each dotted box

3.2 Divide-by-2/3 Injection-locked Frequency Divider

Including the two types of divide-by-2/3 frequency dividers presented in Section 3.1, most of these prevailing divide-by-2/3 frequency dividers are limited by their low operation frequency or high power consumption. In Section 2.5, it is introduced that an ILFD has high operation frequency and low power consumption. Therefore, it is possible to design a divide-by-2/3 ILFD based on the concept of the ILO for high-frequency and low-power application.

Moreover, the ILFD performs properly only when the injection frequency is in the ILO's locking range.

3.2.1 Schematic of the proposed divide-by-2/3 ILFD

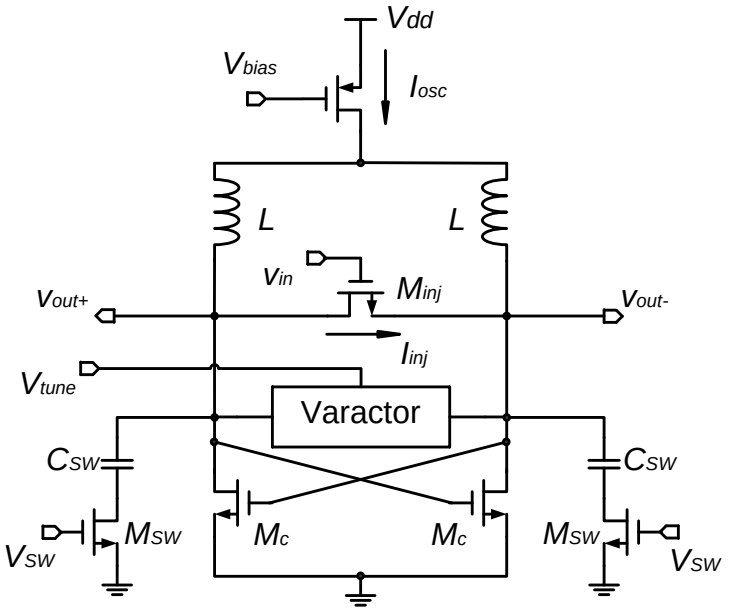

Figure 3.3: Schematic of the proposed divide-by-2/3 ILFD

The schematic of the proposed divide-by-2/3 ILFD is shown in Figure 3.3. The proposed circuit consists of an LC-tank ILFD and a pair of switched capacitors. The ILFD is designed based on an NMOS-type cross-coupled LC-tank VCO with an injection transistor M_{inj}. The VCO is kept in oscillation with a bias current I_{osc} and a bias voltage V_{bias}. Comparing to the ILFD in [80], the proposed circuit has the biasing current source implemented on top of the VCO by a PMOS transistor to reduce phase-noise contribution due to flicker noise [81].

The ILFD's input v_{in} is connected to the gate of M_{inj} while the drain and source of M_{inj} are connected to the ILFD's differential outputs, v_{out+} and v_{out-}.

The injected current I_{inj} passing through M_{inj} is produced by the input voltage signal. In the injection-locked status, the output frequency is equal to a half and a third of the input frequency in the divide-by-2 and divide-by-3 modes, respectively.

The pair of switched capacitors are connected to the differential output as capacitive loads. Each switched capacitor consists of a fixed capacitor C_{SW} and an NMOS transistor M_{SW}, which is switched on or off by a DC voltage V_{SW}. When V_{SW} is 0 V, the switched capacitor is cut-off and then the ILFD is in the divide-by-2 mode. When V_{SW} is 1.8 V, the switched capacitor is connected to the LC tank and then the ILFD is in the divide-by-3 mode.

3.2.2 Design of the switched capacitor

The switched capacitor can be used to select the division ratio because the capacitance in the LC tank can be changed by V_{SW} and, consequently, the ILO's resonant frequency. When the switched capacitor is switched off, the capacitance of the LC tank is $C_{1/2}$ in the divide-by-2 mode. Thus, the resonant frequency is $\omega_{1/2} = \frac{1}{\sqrt{LC_{1/2}}}$, which is close to a half of the input frequency. Alternatively, the capacitance of the LC tank is $C_{1/3}$ in the divide-by-3 mode when the switched capacitor is switched on. Thus, the resonant frequency is $\omega_{1/3} = \frac{1}{\sqrt{LC_{1/3}}}$, which is close to a third of the input frequency.

The relationship between the resonant frequencies in the two division modes is expressed as

$$2\omega_{1/2} = 3\omega_{1/3} \tag{3.1}$$

Substituting $\omega_{1/2} = \frac{1}{\sqrt{LC_{1/2}}}$ and $\omega_{1/3} = \frac{1}{\sqrt{LC_{1/3}}}$ into (3.1), the relationship

between the capacitances in the divide-by-2 or divide-by-3 modes should be designed as

$$C_{1/3} = \frac{9}{4} C_{1/2} \tag{3.2}$$

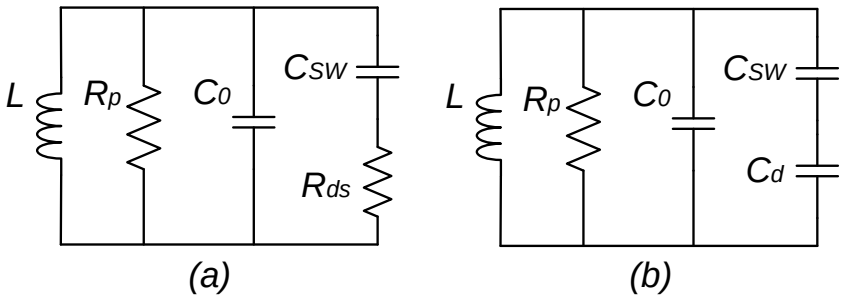

Figure 3.4: LC-tank models (a) in the divide-by-3 mode and (b) in the divide-by-2 mode

At V_{SW}=1.8 V, the LC tank with the switched-on capacitor in the divide-by-3 mode is modeled in Figure 3.4 (a), where R_{ds} is the resistance of M_{SW} from the drain to the ground. Based on the assumption that R_{ds} is very small, $C_{1/3}$ can be expressed as

$$C_{1/3} = C_0 + C_{SW} \tag{3.3}$$

where C_0 is the fixed capacitance of the LC tank.

At V_{SW}=0 V, the LC-tank with the switched-off capacitor in the divide-by-2 mode is modeled in Figure 3.4 (b), where C_d is the capacitance of M_{SW} between the drain and the ground. Based on the assumption that C_d is very small, $C_{1/2}$ can be expressed as

$$C_{1/2} = C_o + C_{SW} \parallel C_d = C_0 + \frac{C_{SW} C_d}{C_{SW} + C_d} \approx C_0 \tag{3.4}$$

Substituting (3.3) and (3.4) into (3.2),

$$C_{SW} = \frac{5}{4} C_0 \tag{3.5}$$

Therefore, the switched capacitor is designed based on (3.5). In practical, it is necessary to do some modification based on the post-layout simulation.

3.3 Analysis of ILFD's Operation Range

With the division ratio of *n*, the ILFD's operation range Δf_{in} is equal to *n* times of the ILO's locking range. Thus, it is very important to analyze the conditions of the injection locking in the ILFD. In order to achieve the proper frequency division, both the gain and phase conditions in the ILFD must be satisfied simultaneously [54].

3.3.1 Injection locking of the ILFD

For the analysis on the injection locking of the ILFD, the proposed circuit can be simplified to a half of the circuit with an inverter. The simplified circuit is shown in Figure 3.5, where R_p represents the parallel resistor in the LC tank while the switched capacitors and all other parasitic capacitances are lumped into a capacitor C_p. Note that C_p is equal to $C_{1/2}$ in the divide-by-2 mode and $C_{1/3}$ in the divide-by-3 mode, respectively. Without injection, ω_{out} is equal to $\omega_0 = 1/\sqrt{LC_p}$, where L and C_p are cancelled. Thus, the LC tank does not contribute to any phase shift. The current I_{tank} through the LC tank is equal to I_{osc} passing through the cross-coupled transistor M_c.

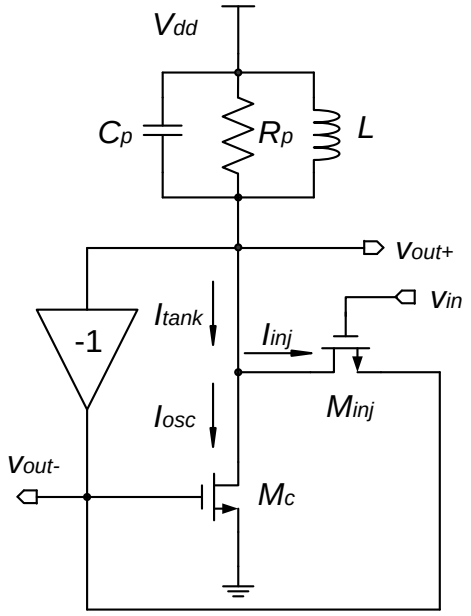

Figure 3.5: Simplified model of the proposed ILFD

When v_{in} is connected to the gate of M_{inj}, I_{inj} is generated and injected into the oscillator. According to Kirchhoff's Law, I_{tank} is equal to the vector-sum of I_{inj} and I_{osc}. In Figure 3.6, it is shown that the phase α between I_{tank} and I_{osc}, as well as the phase β between I_{inj} and I_{osc}, is produced by I_{inj}. Similar to the ILO in Section 2.6.1, the ILFD becomes stable when a specific phase shift of α is produced, which makes ω_{out} equal to ω_{inj}.

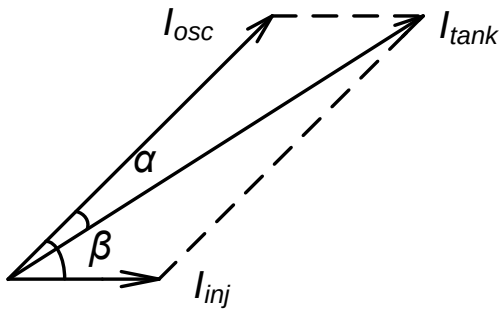

Figure 3.6: Phasor diagram of I_{osc}, I_{tank} and I_{inj} in the ILFD

3.3.2 Phase condition of the ILFD

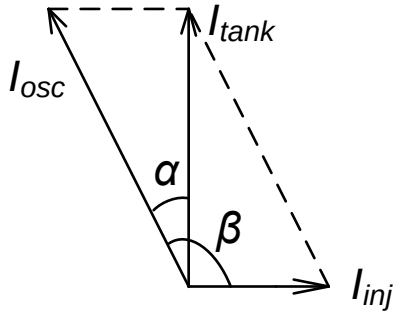

Figure 3.7: Phasor diagram of I_{osc}, I_{tank} and I_{inj} with the maximum α

Based on the injection locking of the ILO, the phase condition can be analyzed for the ILFD. From the general phasor diagram in Figure 3.6, sine of α can be expressed as

$$sin\,\alpha = \frac{I_{inj}}{I_{tank}} sin\,\beta = \frac{I_{inj}\,sin\,\beta}{\sqrt{I_{osc}^2+I_{inj}^2+2I_{osc}I_{inj}\,cos\,\beta}} \tag{3.6}$$

It will reach a maximum value of

$$sin\,\alpha_{max} = \frac{I_{inj}}{I_{osc}} \tag{3.7}$$

if

$$cos\,\beta = -\frac{I_{inj}}{I_{osc}} \tag{3.8}$$

The phasor diagram for the maximum α is shown in Figure 3.7. From the diagram,

$$tan\,\alpha_{max} = \frac{I_{inj}}{I_{tank}} \tag{3.9}$$

where

$$I_{tank} = \sqrt{I_{osc}^2 - I_{inj}^2} \tag{3.10}$$

Base on the definition of the LC-tank's quality factor $Q = \frac{\omega_0}{2}\left|\frac{d\alpha}{d\omega}\right|$ in [12] and

the assumption of $\omega_0 \approx \omega_{inj}$, it is derived as

$$tan\,\alpha \approx \frac{2Q}{\omega_0}(\omega_0 - \omega_{inj}) \tag{3.11}$$

Substituting (3.9) and (3.10) into (3.11), the maximum deviation of the injection angular frequency from the resonant angular frequency can be expressed as

$$\omega_0 - \omega_{inj} = \frac{\omega_0}{2Q} \cdot \frac{I_{inj}}{\sqrt{I_{osc}^2 - I_{inj}^2}} \tag{3.12}$$

Referred to the input frequency and double side deviation, the operation range limited by the phase condition can be expressed as

$$\Delta f_{in,phase} = \frac{n \cdot f_0}{Q} \cdot \frac{I_{inj}}{\sqrt{I_{osc}^2 - I_{inj}^2}} \tag{3.13}$$

where *n* is the division ratio of the ILFD. Noted that I_{inj} is always smaller than I_{osc} in the ILFD.

3.3.3 Gain condition of the ILFD

For a steady oscillation of the ILO, it is maintained that

$$|g_m Z(j\omega)| = 1 \tag{3.14}$$

where $Z(j\omega)$ is the effective impedance of the LC tank and g_m is the transconductance of M_c.

$$Z(j\omega) = \frac{1}{\frac{1}{j\omega L} + j\omega C + \frac{1}{R_p}} = \frac{j\omega L R_p}{R_p - \omega^2 LCR_p + j\omega L} = \frac{R_p}{1 + j2Q(\frac{\omega - \omega_0}{\omega_0})} \tag{3.15}$$

$$g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_{M_c} I_D} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_{M_c} I_{osc}} \tag{3.16}$$

where μ_n is the electron mobility, C_{ox} is the capacity per unit gate area, *W* and *L* are the size of M_c, I_D is the drain current of M_c and I_{osc} is equal to I_D based on the assumption that M_c is completely switched on or off in the whole period.

Substituting (3.15) and (3.16) into (3.14), the maximum deviation from ω_0 is given by

$$\omega - \omega_0 = \frac{\omega_0}{2Q} \cdot \sqrt{2\mu_n C_{ox}(\frac{W}{L})_{M_c} I_{osc} R_p^2 - 1} \tag{3.17}$$

Referred to the input frequency and double side deviation, the operation range limited by the gain condition is expressed as

$$\Delta f_{in,gain} = \frac{n \cdot f_0}{Q} \cdot \sqrt{2\mu_n C_{ox}(\frac{W}{L})_{M_c} I_{osc} R_p^2 - 1} \tag{3.18}$$

3.3.4 Optimized operation range of the ILFD

Both the phase and gain conditions must be satisfied simultaneously, so the ILFD's operation range is limited by the smaller one between $\Delta f_{in,phase}$ and $\Delta f_{in,gain}$. However, $\Delta f_{in,phase}$ is reduced in (3.13) through increasing I_{osc} while $\Delta f_{in,gain}$ is reduced in (3.18) through decreasing I_{osc}. In short, Δf_{in} is optimized at the specific value of I_{osc}, where $\Delta f_{in,phase}$ of the ILFD is equal to $\Delta f_{in,gain}$.

For equalization of the $\Delta f_{in,phase}$ and $\Delta f_{in,gain}$, it can be expressed as

$$\frac{n \cdot f_0}{Q} \cdot \frac{I_{inj}}{\sqrt{I_{osc}^2 - I_{inj}^2}} = \frac{n \cdot f_0}{Q} \cdot \sqrt{2\mu_n C_{ox}(\frac{W}{L})_{M_c} I_{osc} R_p^2 - 1} \tag{3.19}$$

Thus, for the maximum operation range, the optimized value of I_{osc} is given by

$$I_{osc} = (4\mu_n C_{ox}(\frac{W}{L})_{M_c} R_p^2)^{-1} + \sqrt{(4\mu_n C_{ox}(\frac{W}{L})_{M_c} R_p^2)^{-2} + I_{inj}^2} \tag{3.20}$$

Substituting (3.20) into (3.18), the maximum operation range is given by

$$\Delta f_{in} = \frac{n \cdot f_0}{Q} \cdot \sqrt{\sqrt{(2\mu_n C_{ox}(\frac{W}{L})_{M_c} R_p^2 I_{inj})^2 + \frac{1}{4}} - \frac{1}{2}} \tag{3.21}$$

3.3.5 Injection current of the ILFD

The maximum operation range in (3.21) is dependent on the magnitude of I_{inj}, which is different in the divide-by-2 and divide-by-3 modes. Based on the expression of the drain current of M_{inj} in [82], the simplified expression can be given by

$$i_{inj} = a_0 v_{in} + a_1 v_{in} v_{out} + a_2 v_{in} v_{out}^2 + \cdots \quad (3.22)$$

where a_0, a_1, and a_2 are cross-modulation coefficients.

In the divide-by-2 mode, $a_1 v_{in} v_{out}$ is a significant item because the ILFD is injection-locked only by the item with the frequency in the vicinity of the resonant frequency. Thus, the magnitude of I_{inj} is expressed as $0.5 a_1 V_{IN} V_{OUT}$, where V_{IN} and V_{OUT} are the amplitudes of input and output voltage signals, respectively. Similarly, the magnitude of I_{inj} in the divide-by-3 mode is expressed as $0.25 a_2 V_{IN} V_{OUT}^2$. Through simulation for M_{inj}, it is known that a_2 is smaller than a_1 in the proposed circuit. With the different magnitudes of I_{inj} in the divide-by-2 and divide-by-3 modes, the maximum operation range in the divide-by-2 mode is generally larger than the one in the divide-by-3 mode. Therefore, in the design of the proposed circuit, it is more important to extend the operation range in the divide-by-3 mode, which limits the mutual operation range of the two division modes.

3.4 Simulated and Experimental Results of the Proposed Divide-by-2/3 ILFD

The proposed divide-by-2/3 ILFD has been designed and fabricated in the 0.18 μm CMOS technology. The die microphotograph is shown in Figure 3.8.

The size of the proposed circuit is 1.03 mm × 0.47 mm. In this thesis, all measurements have been conducted on wafer, using a probe station with DC connection and RF probes. The probe station is placed inside a metal cage providing a common ground potential for all measurement equipment and wafer chuck to remove any potential electrostatic discharge (ESD) problem.

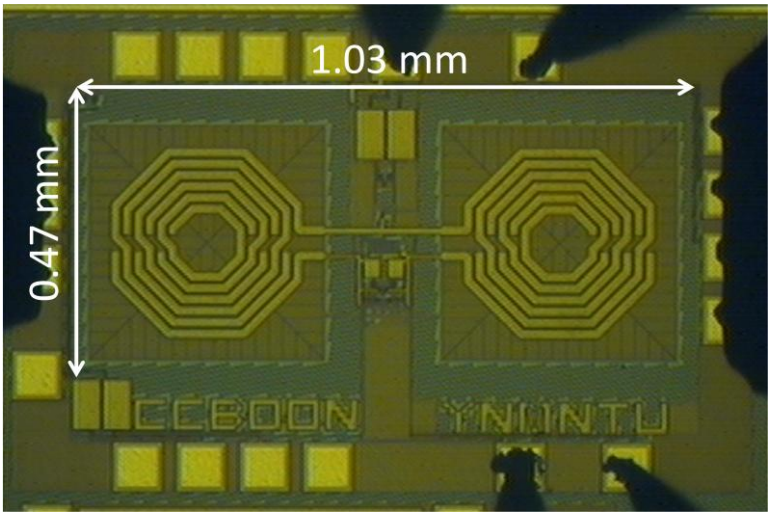

Figure 3.8: Die microphotograph of the proposed circuit

The measurement setup for the proposed circuit is shown in Figure 3.9, which is labeled as the device under test (DUT). Similar measurement setup is used to test other proposed circuits in this thesis. Through the DC connections, the DC voltage supply and DC signals are provided by the HP 4142 modular DC source/monitor unit. From our experiment, there is no significant difference between using the modular DC source/monitor unit and using batteries as the DC voltage supply for phase noise measurement because the modular DC source/monitor unit has very clean output. Single and differential signals are provided with the RF probes of Ground-Signal-Ground and Ground-Signal-Signal-Ground, respectively. The input AC signal is generated from the Rohde & Schwarz SMF 100A signal generator. The waveform of the output signal can

be observed with RF probe connecting to (1) LeCroy Oscilloscope. The maximum frequency of the oscilloscope is 6 GHz. In addition, (2) Agilent Spectrum Analyzer 8563E can be used instead of the oscilloscope to measure the phase noise and frequency spectrum. The frequency range of the spectrum analyzer is from 9 kHz to 26.5 GHz.

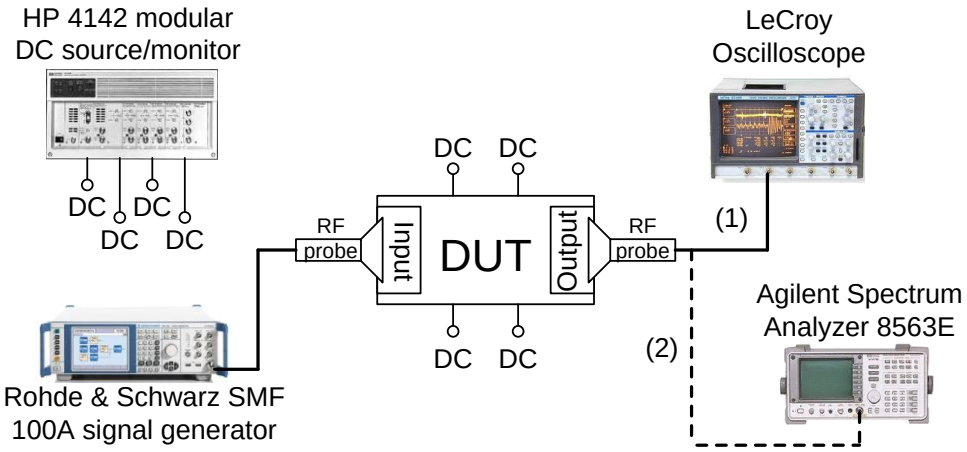

Figure 3.9: Measurement setup for the proposed circuit

With the supply voltage of 1.8 V, the measured current and power consumption for the core circuit are 1.75 mA and 3.15 mW, respectively. The operation range of the proposed divide-by-2/3 ILFD is 4.28~4.81 GHz. In the divide-by-2/3 ILFD, the division ratio is 2 or 3, according to the binary selection between V_{SW}=0 V and V_{SW}=1.8 V. In Figure 3.10, the transient responses of the input and output signals are shown from simulation. With the same input signal of 4.8 GHz, the output signals in the '/2' and '/3' modes are at the frequency of 2.4 GHz and 1.6 GHz, respectively.

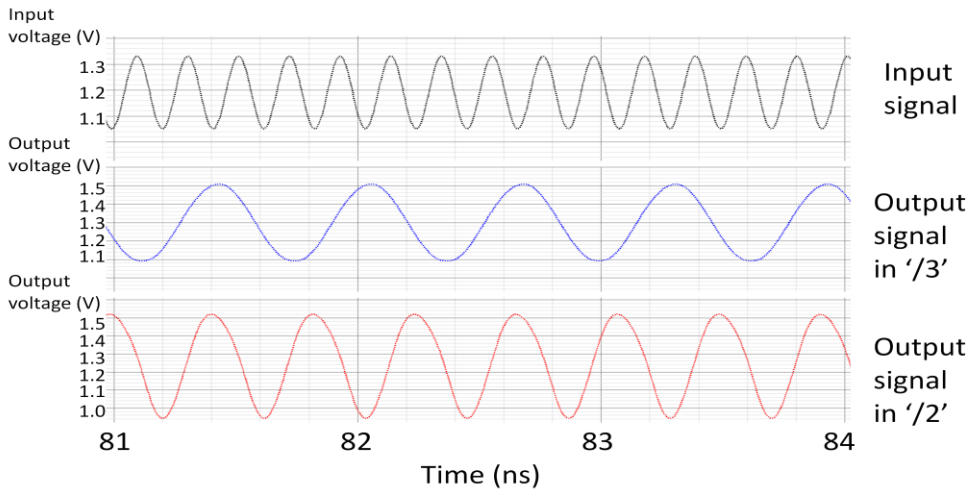

Figure 3.10: Transient responses of the input and output signals in the '/2' and '/3' modes

Without input signal, the output frequency of the free-running ILFD is equal to its resonant frequency. The measured tuning characteristics in the divide-by-2 and divide-by-3 modes are shown in Figure 3.11. When V_{tune} is increased from 0 to 1.8 V, the resonant frequency is tuned from 2.26 to 1.96 GHz in the divide-by-2 mode and from 1.58 to 1.45 GHz in the divide-by-3 mode.

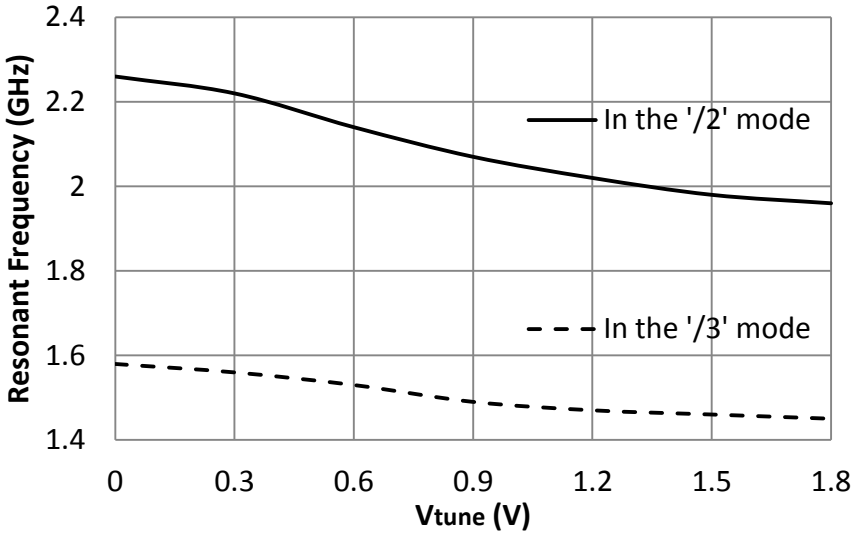

Figure 3.11: Measured tuning characteristics in the '/2' and '/3' modes

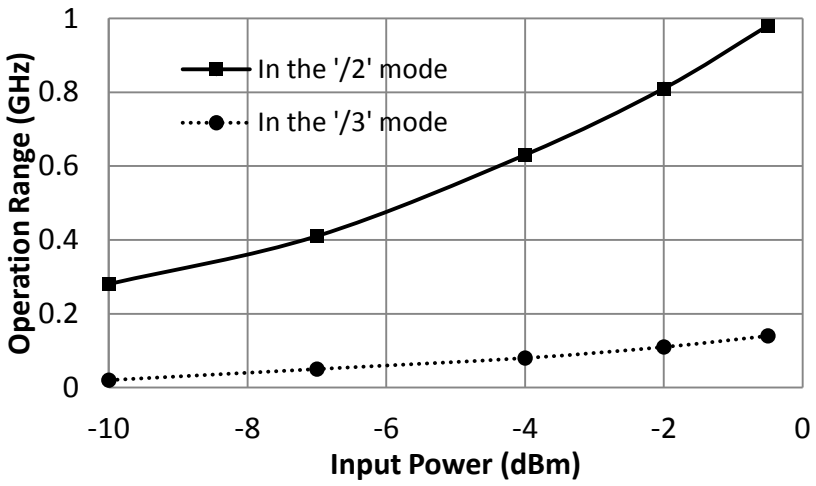

Figure 3.12: Measured operation ranges versus the input power in the '/2' and '/3' modes

With an input signal, the ILFD is in the status of injection locking if the input frequency is in the operation range. The measured operation ranges versus the input power of the ILFD in the divide-by-2 and divide-by-3 modes are shown in Figure 3.12. For example, with an input power of -0.5 dBm, the operation range is about 0.98 GHz and 0.14 GHz in the divide-by-2 and divide-by-3 modes, respectively. Generally, the operation ranges are increased with the input power.

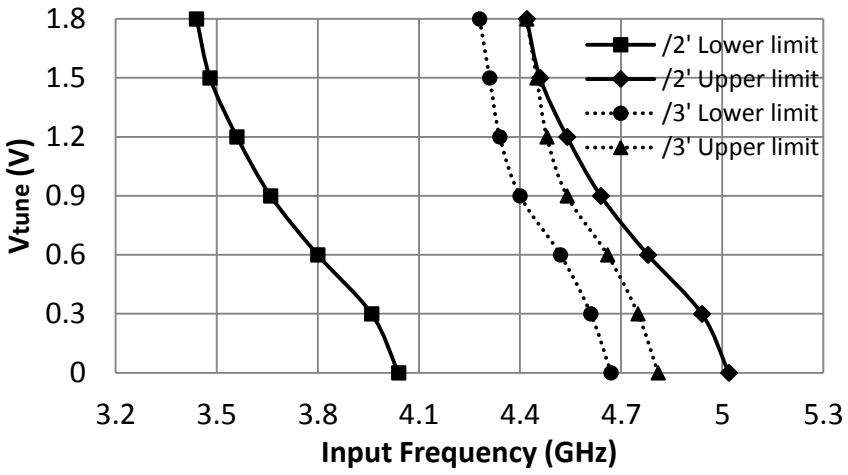

Figure 3.13: Measured operation ranges in the '/2' and '/3' modes

With the input power of -0.5 dBm, the measured operation ranges in the divide-by-2 and divide-by-3 modes are also shown in Figure 3.13. With increasing V_{tune} from 0 to 1.8 V, the operation ranges in the divide-by-2 and divide-by-3 modes are shifted to left. Consequently, the overall operation ranges are 3.44~5.02 GHz in the divide-by-2 mode and 4.28~4.81 GHz in the divide-by-3 mode, respectively. Through both the measurement results in Figure 3.12 and Figure 3.13, it is shown as expected that the ILFD's operation range is obviously narrower in the divide-by-3 mode than in the divide-by-2 mode with the same input power.

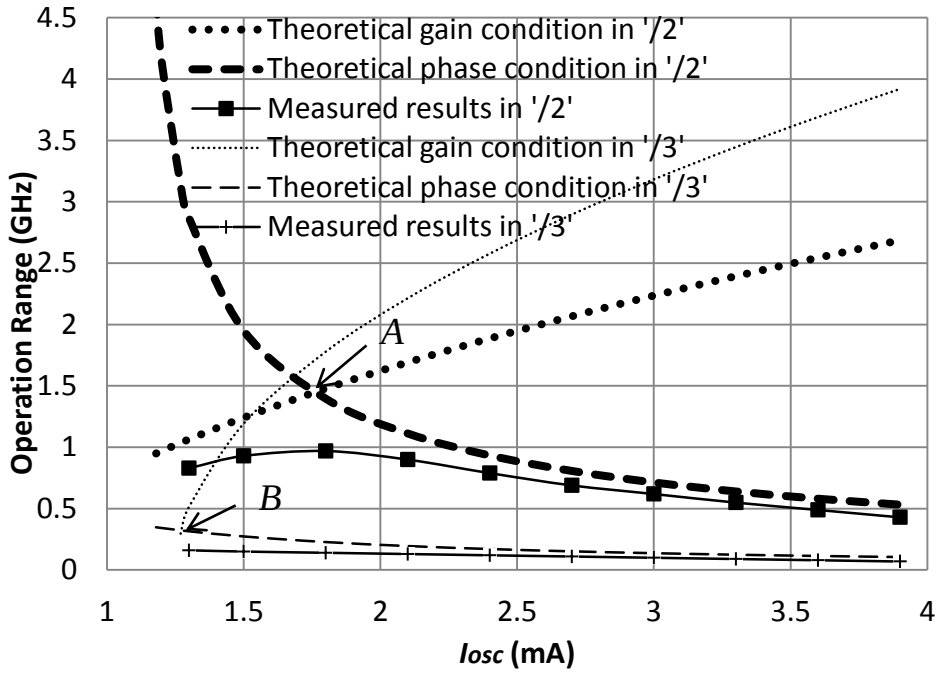

Figure 3.14: Theoretical and measured operation ranges limited by the phase and gain conditions in the '/2' and '/3' modes

In Figure 3.14, both $\Delta f_{in,phase}$ and $\Delta f_{in,gain}$ versus I_{osc} in the divide-by-2 and divide-by-3 modes with the input power of -0.5 dBm are shown, respectively.

The two thick dotted lines show the theoretical gain and phase conditions in the divide-by-2 mode, which crosses at Point *A*. Therefore, it is shown that the optimized value of I_{osc} for the divide-by-2 mode is 1.75 mA.

Similarly, the two thin dotted lines represent the theoretical gain and phase conditions in the divide-by-3 mode, which crosses at Point *B*. Thus, it is shown that the optimized value of I_{osc} for the divide-by-3 mode is 1.27 mA. The operation range in the divide-by-2 mode is larger than that in the divide-by-3 mode, so the maximum operation range for the divide-by-2/3 ILFD is achieved by setting I_{osc} of 1.27 mA. However, I_{osc} is biased at 1.75 mA in this design to provide sufficient output swing and design margin for process variation.

In order to compare with the theoretical calculation, the measured operation ranges versus I_{osc} in the divide-by-2 and divide-by-3 modes with the input power of -0.5 dBm are shown in Figure 3.14. The measured operation range in the divide-by-2 mode initially increases with I_{osc}, then decreases after the optimized value of I_{osc} at 1.8 mA, which verifies the theoretical calculation. Similarly, it is also shown in Figure 3.14 that the operation range in the divide-by-3 mode is increased with reducing I_{osc}. However, I_{osc} cannot be too low in measurement as in order to maintain the ILFD's oscillation. Due to this reason, the operation range for I_{osc} smaller than 1.2 mA cannot be measured. This observation verifies the theoretical analysis, shown in Figure 3.14, where the operation range in the divide-by-3 mode approaches to zero when I_{osc} is equal to 1.2 mA.

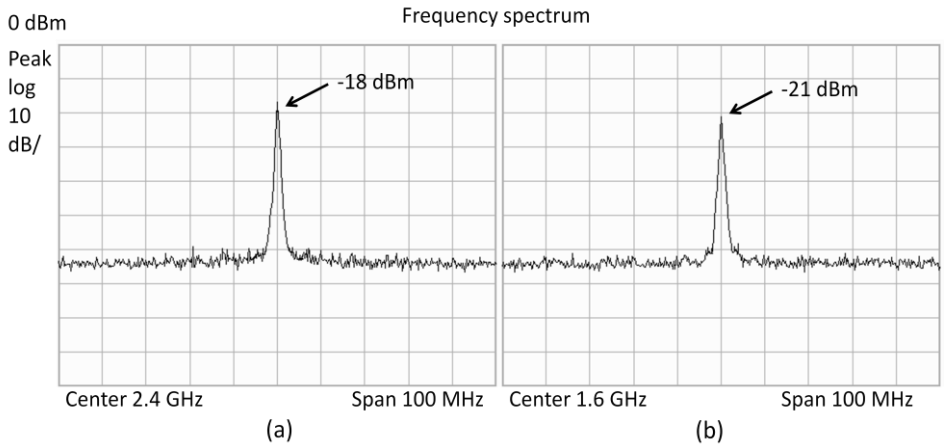

Figure 3.15: Output frequency spectrums of the dual-modulus FD (a) in the '/2' mode and (b) in the '/3' mode

The frequency spectrums of the dual-modulus FD in the '/2' and '/3' modes are shown in Figure 3.15 (a) and (b), respectively. Their output frequencies are 2.4 GHz and 1.6 GHz in the divide-by-2 and divide-by-3 modes, respectively. The measured phase noises of the input and outputs in the divide-by-2 and divide-by-3 modes are shown in Figure 3.16. Due to injection-locked by the input signal, the phase noises of the output signals are dependent on the input, especially at low offset frequency. Theoretically, the phase noises of the divide-by-2 and divide-by-3 outputs are 6 (≈20log2) dB and 9.5 (≈20log3) dB lower than that of the input, respectively. In the measured results, as expected, the input phase noise is -98 dBc/Hz at 10 kHz offset frequency while the output phase noises in the divide-by-2 and divide-by-3 modes are -104 dBc/Hz and -107 dBc/Hz, respectively. In addition, the output phase noises in the divide-by-2 and divide-by-3 modes are -125 dBc/Hz and -125.5 dBc/Hz at 1-MHz offset frequency, respectively, which are worse than their theoretical values due to the thermal noise from the dual-modulus FD.

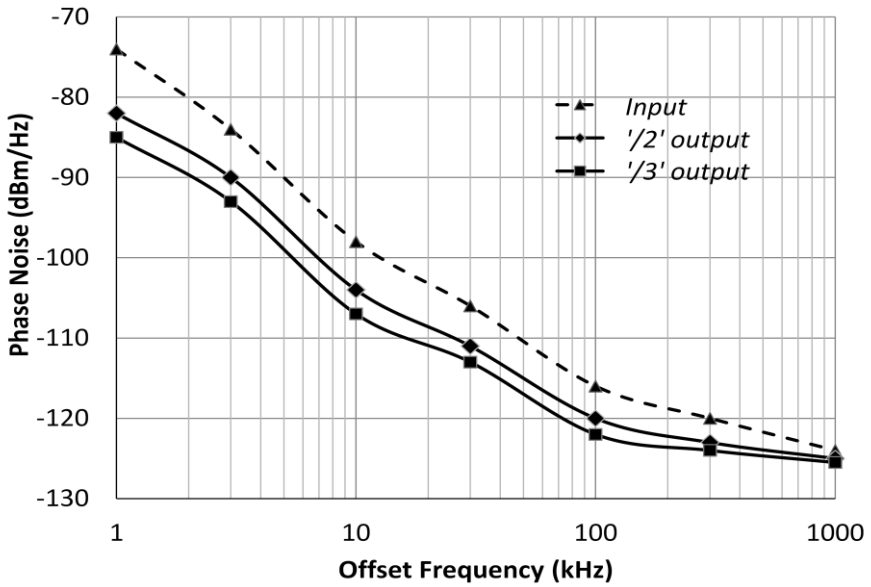

Figure 3.16: Measured phase noises of the input and outputs in the '/2' and '/3' modes

3.5 Summary

In this chapter, the proposed divide-by-2/3 ILFD is presented after reviewing conventional dual-modulus frequency dividers. The circuit has been designed and fabricated in the 0.18 μm CMOS technology. With the power consumption of 3.15 mW and the input power of -0.5 dBm, the operation range of the divide-by-2/3 ILFD is from 4.28 GHz to 4.81 GHz. The optimized bias current for the ILFD's maximum operation range is analyzed based on the gain and phase conditions. Finally, the analysis is verified through the measured results.

Table 3.1 summarizes the performances of some dual-modulus frequency dividers. A popular frequency divider's FoM can be used for comparisons [86] [87]. Based on the calculated FoM in Table 3.1, the proposed circuit has the best FoM and the lowest power consumption. This makes the proposed divide-by-2/3 ILFD a suitable design for low-power frequency synthesizer.

Table 3.1: The performance comparison of the dual-modulus FDs

	[83]	[84]	[85]	[80]	This work
Technology	GaInP/GaAs HBT	0.12 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Division ratio	2/3	4/5	2/3	2/3	2/3
V_{dd} (V)	4.2	1.5	1.5	1.8	1.8
Max. f_{in} (GHz)	9	15	8.4	2.5	4.81
P_{DC} (mW)	256.2	54	10	7.6	3.15
FoM* (GHz/mW)	0.035	0.278	0.84	0.329	1.527

* FoM=Max. f_{in}/P_{DC}

CHAPTER 4

Novel Dual-Band Voltage-Controlled Oscillator

The application of wireless local area network (WLAN) at the 2.4 GHz Instrumentation, Scientific and Medical (ISM) band has been experiencing significantly growth in the recent years. The newer WLAN at 5 GHz in the Unlicensed National Information Infrastructure (UNII) band has more bandwidth for more channels and higher data rates. With the increase in the demand for higher data rates, WLAN chips must be able to cover both the ISM and UNII bands to ensure smooth migration.

One of the major problems in a dual-band transceiver is the implementation of a dual-band VCO. A VCO with wide tuning range is a simple method to cover the two bands. However, the VCO needs a varactor with large variable percentage in capacitance, which is usually unavailable in a standard CMOS technology. Another method is that switchable devices are used in the LC tank of the VCO to change either capacitance [88] or inductance [89]. The resistance of the switchable capacitors or inductors, however, is likely to cause the degradation of the tank quality factor (Q) and, consequently, the phase noise of the VCO. Moreover, two independent VCOs in a stacking topology can be used to provide two frequencies [90], but their phase noises are deteriorated due to the limited voltage headroom for both VCOs. In addition, the total power consumption is unavoidably high if two PLLs are implemented in a dual-band transceiver.

4.1 Tank Voltage Amplitude

Tank voltage amplitude of an oscillator has an important effect on the phase noise, as emphasized by the presence of q_{max} in the denominator of the expression for the single-sideband phase noise [27].

$$\mathcal{L}(\Delta\omega) = 10log\left(\frac{\overline{i_n^2}/\Delta f}{q_{max}^2} \cdot \frac{\Gamma_{rms}^2}{2\Delta\omega^2}\right) \tag{4.1}$$

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the parallel current noise, Γ_{rms} is the rms value of the ISF associated with that noise source, q_{max} is the maximum signal charge swing, and $\Delta\omega$ is the offset angular frequency from the carrier.

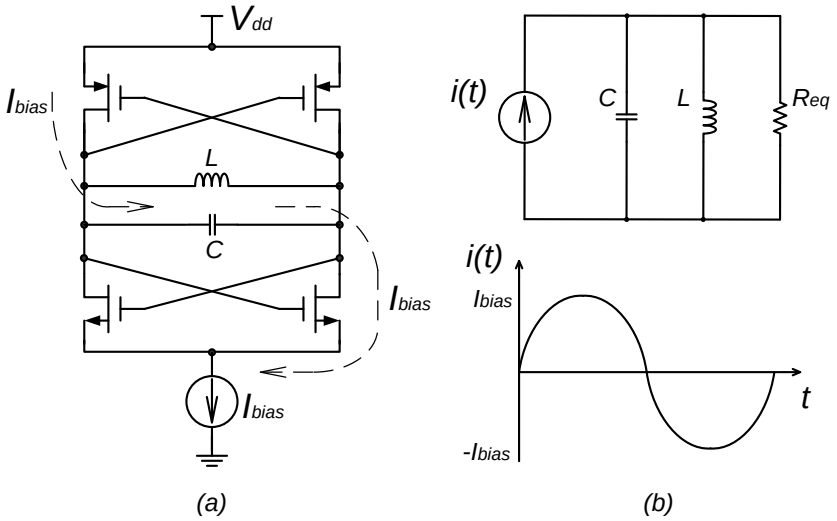

Figure 4.1: Current flow (a) in an LC-tank oscillator and (b) in a simplified model

In Figure 4.1 (a), it is shown that an LC-tank oscillator is biased by a current I_{bias}, which is based on the complementary cross-coupled structure. The current is flowing in the differential oscillator, which is completely switched to either side in turn. As the tank voltage changes, the direction of the current flow through the tank reverses. In Figure 4.1 (b), it is shown that the cross-coupled transistors can be modeled as a current source switching between I_{bias} and -I_{bias}

in parallel with a simplified LC tank, where R_{eq} is the equivalent parallel resistance of the tank. At the resonant frequency, the admittances of the L and C are cancelled, leaving R_{eq} only. At high frequencies, the flowing current can be approximated to be a sinusoidal waveform due to finite switching time and limited gain. Thus, the tank voltage amplitude can be approximated as

$$V_{tank} \approx I_{bias} R_{eq} \tag{4.2}$$

Thus, the operation of the VCO is defined as current-limited operation in which the tank voltage amplitude is solely determined by I_{bias} and R_{eq}.

However, the tank voltage amplitude cannot be estimated based on (4.2) when it approaches the supply voltage. It will be clipped at V_{dd} by the PMOS transistors and at ground by the NMOS transistors. Therefore, the tank voltage amplitude does not significantly exceed V_{dd}. In this case, this operation of the VCO is known as voltage-limited operation.

In the VCO design, it is desirable to increase the tank voltage amplitude for low phase noise based on (4.1). According to this simple model, the tank voltage amplitude cannot be increased beyond due to voltage limiting. In order to optimize the power consumption, the VCO should be designed to operate at the edge of the voltage-limited operation.

4.2 Design of the Proposed Dual-Band VCO

4.2.1 Topology of the proposed dual-band VCO

In a 2.4/5.15 GHz application, the 5.15-GHz frequency band is far away from the 2.4-GHz frequency band, but is near to the frequency of 4.8 GHz that is the second harmonic of 2.4 GHz. Thus, it is not necessary to design a VCO

with wide tuning range from 2.4 GHz to 5.15 GHz. Instead, a VCO with the tuning range from 4.8 GHz to 5.15 GHz is designed. After the VCO, a divide-by-2 frequency divider is designed with the output for the 2.4-GHz frequency band. In this circuit, an ILFD can be used for high frequency operation and low power consumption.

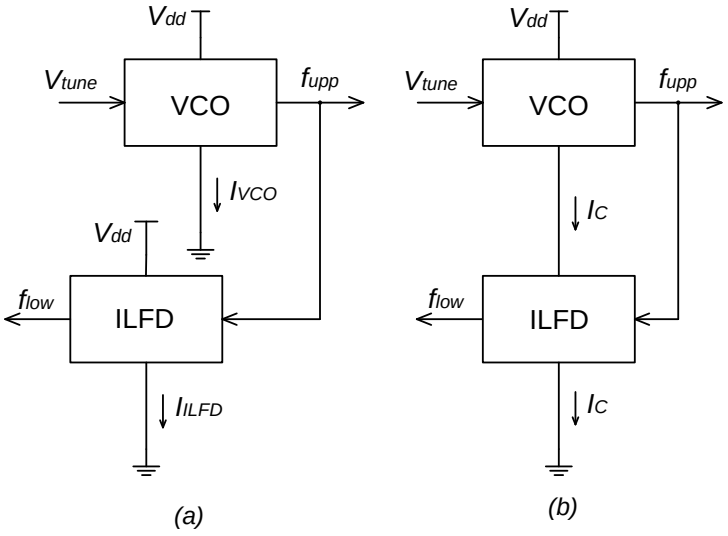

Figure 4.2: A VCO and an ILFD (a) on cascade structure (b) on stacking structure

Based on a conventional topology, the VCO and the ILFD are implemented in cascade, shown in Figure 4.2 (a). For the dual-band VCO, the power is not consumed only by the VCO, but also by the ILFD. Thus, they consume much power, especially at high-frequency operation. The total power consumption P_{total} is $V_{dd}\, I_{VCO}+V_{dd}\, I_{ILFD}$, where I_{VCO} and I_{ILFD} are the bias currents in the VCO and the ILFD, respectively.

Based on a stacking topology, the VCO can be stacked on top of the ILFD to reduce the power consumption, shown in Figure 4.2 (b). Thus, the bias current I_C in the VCO is reused by the ILFD. Conclusively, P_{total} is only $V_{dd}\, I_C$, which is

smaller in the stacking topology than in the conventional topology if I_C is smaller than the sum of I_{VCO} and I_{ILFD}.

4.2.2 Schematic of the proposed dual-band VCO

The schematic of the proposed dual-band VCO is shown in Figure 4.3, which consists of a VCO (in the left box) and an ILFD (in the right box). The VCO is based on a complementary LC-tank oscillator, which consists of an inductor L_1, two NMOS and two PMOS transistors to regenerate the signal. At the differential outputs of the VCO, v_{upp+} and v_{upp-}, the VCO's output frequency f_{upp} is used for the upper band operation. A varactor C_{var1} is connected between v_{upp+} and v_{upp-}, which is tuned by a DC voltage V_{tune} to vary f_{upp}.

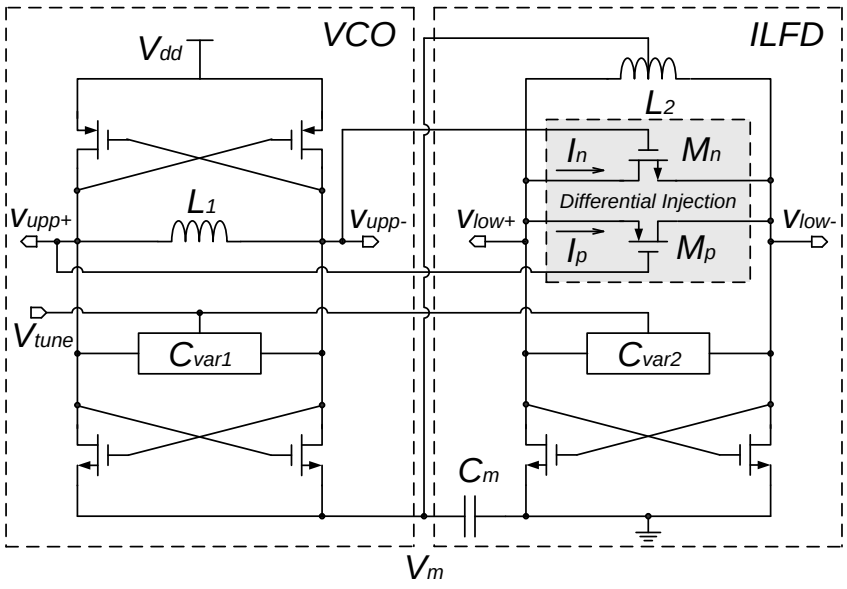

Figure 4.3: Schematic of the proposed dual-band VCO

The ILFD is based on an NMOS-only LC-tank oscillator, which consists of another inductor L_2 and a pair of cross-coupled NMOS transistors to regenerate the signal. At the differential outputs of the ILFD, v_{low+} and v_{low-}, the ILFD's

output frequency f_{low} is used for the lower band operation. One PMOS injection transistor M_p and one NMOS injection transistor M_n are connected in parallel between v_{low+} and v_{low-}. Their gates are connected to v_{upp+} and v_{upp-}, which generate the injection currents I_p and I_n, respectively. Another varactor C_{var2} between v_{low+} and v_{low-} is also tuned by V_{tune}. Moreover, a fixed capacitor C_m is placed between V_m and *gnd*, which is used to decouple the AC signal and to attenuate the voltage variation on V_m. In addition, another varactor is connected in parallel to C_{var2}, which is not shown in Figure 4.3 for simplicity. It will be independently tuned once and then fixed to offset the effect of process variation on the ILFD's resonant frequency f_0.

4.2.3 Design techniques of the proposed dual-band VCO

In a wireless transceiver, phase noise is an important characteristic to measure the quality of an oscillator. In the proposed circuit, the VCO is designed based on the complementary structure, which occupies larger voltage headroom but has better phase noise than the one based on an NMOS-only structure [47]. The phase noise of the ILFD with wide operation range is significantly dependent on the VCO's output [91]. Theoretically, the phase noise of the ILFD at f_{low} is 6 dB better than that of the VCO because f_{low} is equal to $(1/2)f_{upp}$.

For the operation of the dual-band VCO, it is required that f_{upp} is in the ILFD's operation range. In the proposed circuit, the varactors C_{var1} and C_{var2} are implemented in the VCO and the ILFD, respectively, and they are tuned together by V_{tune}. Thus, the capacitance of the LC tanks in the VCO and ILFD can be increased or decreased simultaneously. Consequently, f_{upp} is shifted

together with f_0.

In a conventional ILFD [92], the injection signal is usually single-ended but most VCOs' outputs are differential. Thus, the power consumption and the complexity of the circuit can be increased if a differential-to-single converter is added between the VCO and the ILFD. Otherwise, only one of the VCO's outputs is used while the other is connected to a dummy circuit. As shown in Figure 4.3, differential injection is implemented in the proposed circuit. The differential outputs of the VCO are both connected to the gates of M_p and M_n instead of single injection. The injection currents I_p and I_n are generated in the same direction by v_{upp+} and v_{upp-}, respectively. Based on Adler's lock range equation in [10], the ILFD's operation range is extended by the increased injection current that is the sum of I_p and I_n.

4.3 Simulated and Experimental Results of the Proposed Dual-Band VCO

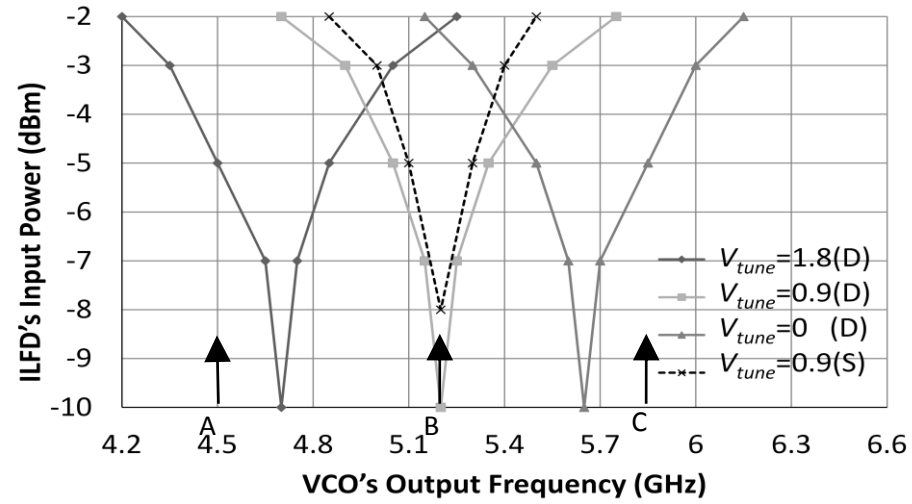

Figure 4.4: Simulated output frequency of the VCO and operation range of the ILFD

These design techniques can be verified through simulation. Firstly, it is shown in Figure 4.4 that the VCO's output frequencies are 4.5 GHz, 5.2 GHz and 5.85 GHz at V_{tune} of 1.8 V, 0.9 V and 0 V, respectively. f_{upp} is shown by three arrows of A, B and C. Simultaneously, the operation ranges of the ILFD with differential injection (D) are shown at V_{tune} of 1.8 V, 0.9 V and 0 V. At the same V_{tune}, f_{upp} is always kept in the ILFD's operation range when the ILFD's input power is larger than -5 dBm. In the proposed circuit, the ILFD is always injection-locked because the VCO's output power can be kept larger than -5 dBm.

Secondly, the operation ranges of the ILFD with differential injection and with single injection (S) are compared in Figure 4.4. It is an example at V_{tune} of 0.9 V that the operation range of the ILFD with single injection is narrower than the one with differential injection. If the ILFD's input power is -5 dBm, the operation ranges of the ILFD with single injection and differential injection are 0.2 GHz and 0.3 GHz, respectively.

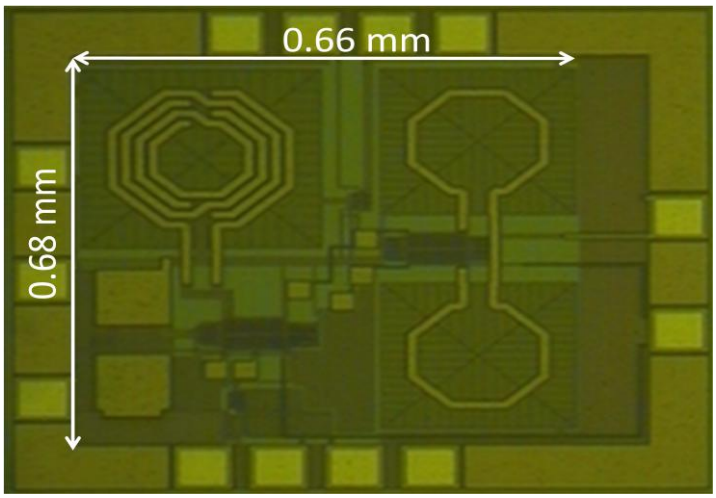

Figure 4.5: Die microphotograph of the proposed circuit

The proposed dual-band VCO has been designed and fabricated in the 0.18 μm CMOS technology. The die microphotograph of the proposed circuit is shown in Figure 4.5. The size of the proposed circuit is 0.66 mm × 0.68 mm. At the supply voltage of 1.8 V, the measured current and power consumption for the core circuit are 1.78 mA and 3.2 mW, respectively. Through de-embedding, the output powers for f_{upp} and f_{low} are measured to be 0.9 dBm and -2 dBm, respectively.

The simulated and measured tuning characteristics of f_{upp}, f_{low} and f_0 are shown in Figure 4.6 and Figure 4.7, respectively. It can be observed that both figures are similar, but the measured frequency is a little lower than the simulated frequency due to parasitic capacitance added to the LC tank. In Figure 4.7, through varying V_{tune} from 0 V to 1.8 V, f_{upp} is tuned from 4.48 GHz to 5.86 GHz while f_{low} is generated from 2.24 to 2.93 GHz. It can be concluded that the ILFD is always injection-locked by the VCO in the whole tuning range because f_{low} is equal to $(1/2)f_{upp}$. In addition, f_0 can be tuned from 2.36 to 2.82 GHz through varying V_{tune}.

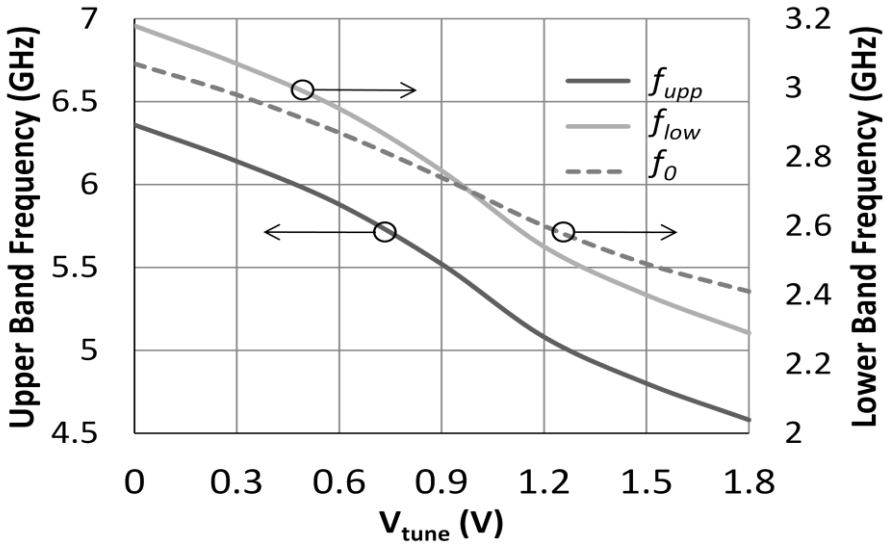

Figure 4.6: Simulated tuning characteristics of the output frequencies

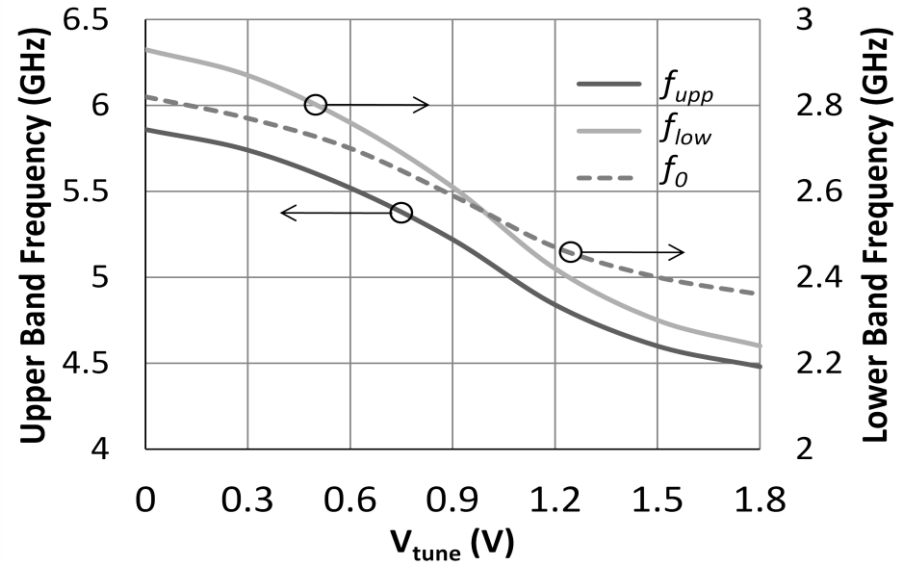

Figure 4.7: Measured tuning characteristics of the output frequencies

The simulated and measured phase noises of the VCO and the ILFD are shown in Figure 4.8. The solid lines represent the measured results while the dotted lines represent the simulated results. At the free-running ILFD, the measured phase noise of f_0 is only -106 dBc/Hz at 1-MHz offset frequency. However, the ILFD's phase noise can be suppressed by injection locking. With proper injection, the measured phase noises of f_{upp} and f_{low} are -115 dBc/Hz and -121 dBc/Hz at 1-MHz offset frequency, respectively. As expected, the ILFD's phase noise is almost 6 dB better than the VCO's phase noise. In comparison with the simulated results, the measured phase noise is worse. At low offset frequency, the measured phase noise is deteriorated due to the parasitic components, which degrade the quality factor of the LC tank. At high offset frequency, the interconnect resistance leads to higher noise floor.

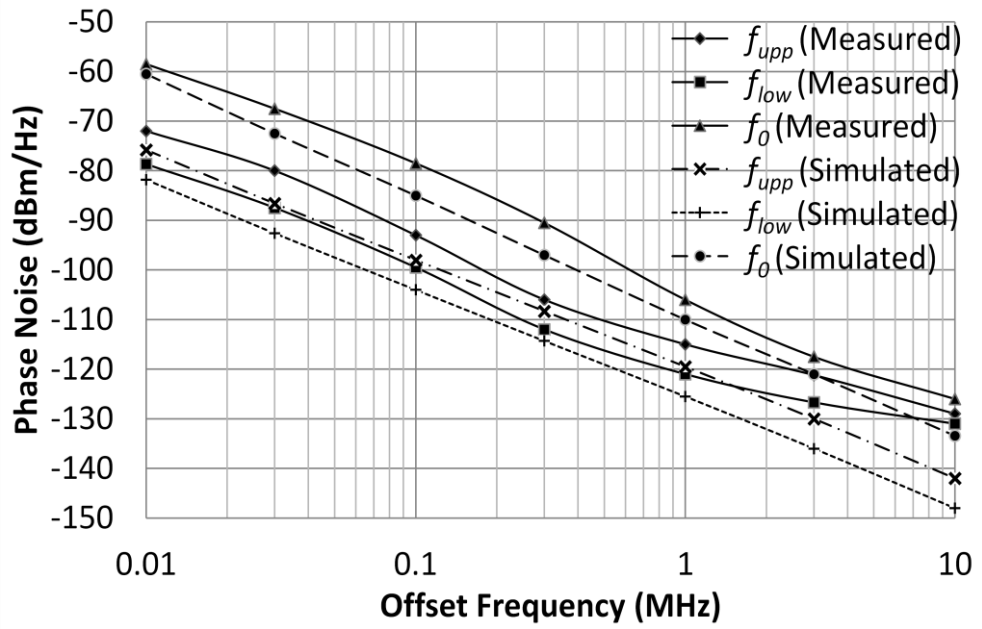

Figure 4.8: Simulated and measured phase noises of the output frequencies

4.4 Summary

In this chapter, the proposed 2.4/5.15 GHz dual-band VCO is presented after reviewing tank voltage amplitude in current-limited and voltage-limited operations. The circuit has been fabricated in the 0.18 µm CMOS technology. Table 4.1 summarizes the measured performances of the proposed dual-band VCO. A popular VCO's FoM is used for comparisons [93].

$$\text{FoM} = \mathcal{L}\{\Delta f\} - 20\,log\left(\frac{f_{op}}{\Delta f}\right) + 10\,log\left(\frac{P_{DC}}{1mW}\right) \quad (4.3)$$

where $\mathcal{L}\{\Delta f\}$ represents the phase noise at the offset frequency Δf, f_{op} is the operation frequency, and P_{DC} is the DC power consumption.

Based on the calculated FoM in Table 4.1, the proposed dual-band VCO has the best FoM, the lowest power consumption and the widest tuning range. This makes the proposed dual-band VCO a suitable design for a low-power dual-band transceiver, which supports both the ISM and UNII bands for WLAN

applications. In a low-power PLL, this proposed circuit can be used as the VCO and the first-stage frequency divider.

Table 4.1: The performance comparison of the dual-band VCOs

	Technology	V_{dd} (V)	P_{total} (mW)	f_{op} (GHz)/ Δf (Hz)	Tuning Range (GHz)	Phase Noise (dBc/Hz)	FoM (dB)
[94]	0.18 µm CMOS	1.8	8	5.7/1M	1.3	-98	-164.1
				2.85/1M	0.65	-110	-170
[90]	0.18 µm CMOS	1.8	6.11	5.23/1M	0.25	-120	-186.6
				2.44/1M	0.11	-126	-186.1
[95]	0.18 µm CMOS	1.8	16.5	5.74/1M	1.01	-118	-184.4
				2.98/1M	0.64	-124	-184.1
[89]	0.18 µm CMOS	1.8	7.56	4.56/1M	1.2	-121	-185
				2.3/1M	0.25	-120	-179
[96]	0.18 µm CMOS	1	5.17	4.23/1M	0.24	-110	-175.4
				2.115/1M	0.12	-116	-175.4
This work	0.18 µm CMOS	1.8	3.2	5.86/1M	1.38	-115	-187.1
				2.93/1M	0.69	-121	-190.1

CHAPTER 5

Novel Injection-Locked Frequency Multiplier

High frequency wireless applications are flourishing due to the increasing demand for high-speed mobile connectivity. A major obstacle to a transceiver in high-frequency application is the degradation of active components with increasing frequency. This is particularly severe in frequency synthesizer, which is important for LO signal generation. Generally, a frequency synthesize needs more power consumption for higher frequency operation.

5.1 Frequency Multiplier

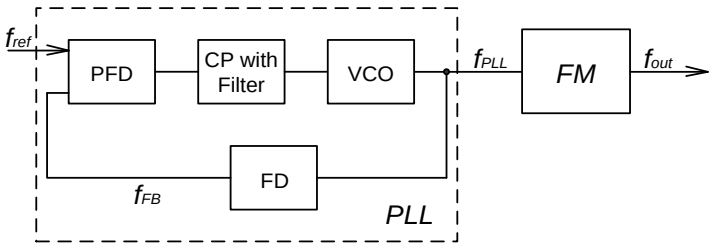

Figure 5.1: Frequency multiplier driven by a PLL in a frequency synthesizer

A frequency multiplier (FM) can be used in a frequency synthesizer for high-frequency and low-power operation. In Figure 5.1, it is shown that the frequency multiplier is driven by a low-frequency PLL. In [97], the design exploits the nonlinearity of active devices to generate the harmonics of the input signal. The circuit has a single-ended input/output, but requires many inductors and high power consumption. In [98], an up-conversion mixer is used to generate the second harmonic as the output of the frequency multiplier. The

circuit has very low conversion gain but also consumes high power. Generally, it is difficult to design such a frequency multiplier in the frequency synthesizer to reduce power consumption.

In Chapter 3 and 4, the ILFDs are designed based on the ILO for low-power and high-frequency operation. Also, an ILFM can be proposed based on the ILO with a novel topology. Thus, the proposed ILFM has lower power consumption, higher operation frequency and higher conversion gain than these conventional frequency multipliers. Similar to the ILFDs, the ILFM has limited operation range due to the locking range of the ILO. In fact, the operation range of the ILFM is the locking range of the ILO, i.e. the output-frequency range of the frequency multiplier.

5.2 Injection-Locked Frequency Multiplier

5.2.1 Topology of the proposed ILFM

A conventional frequency multiplier in Figure 5.2 (a) consists of a frequency pre-generator and an amplifier. The frequency pre-generator is designed based on an up-conversion mixer with both inputs connected to the differential signal, v_{in+} and v_{in-}, at a frequency f_{in}. The mixer's outputs, v_{m+} and v_{m-}, are operating at $2f_{in}$, which are connected to an LC tank H_1 and to a pair of transconductance G_m. With another LC tank H_2 as a bandpass filter, the frequency multiplier's outputs, v_{out+} and v_{out-}, are at a frequency f_{out}, which is also equal to $2f_{in}$. It is noted that v_m is amplified to v_{out} based on a voltage-gain characteristic of the amplifier, which is also shown in Figure 5.2 (a). With increasing v_m, the gain is generally reduced due to the saturation of the amplifying transistor.

The proposed topology of the frequency multiplier is shown in Figure 5.2 (b), which has the same frequency pre-generator as in Figure 5.2 (a). An ILO is in the following stage instead of the amplifier as in Figure 5.2 (a). In the ILO, a pair of G_m form a positive loop with an LC tank H, which serves as a load. When the ILO is injection-locked, f_{out} is equal to $2f_{in}$. In Figure 5.2 (b), it is also shown that v_m is amplified multiple times in the positive feedback loop until the gain reduces to one due to gain compression as input increases. Thus, with the same v_m and characteristic of the voltage gain, v_{out} is larger in Figure 5.2 (b) than in Figure 5.2 (a), especially with small v_m. Note that the input of the ILO is in current rather than voltage, v_m is used here for simple illustration. The overall conversion gain of the frequency multiplier is higher in the proposed topology than in the conventional topology with the same power consumption.

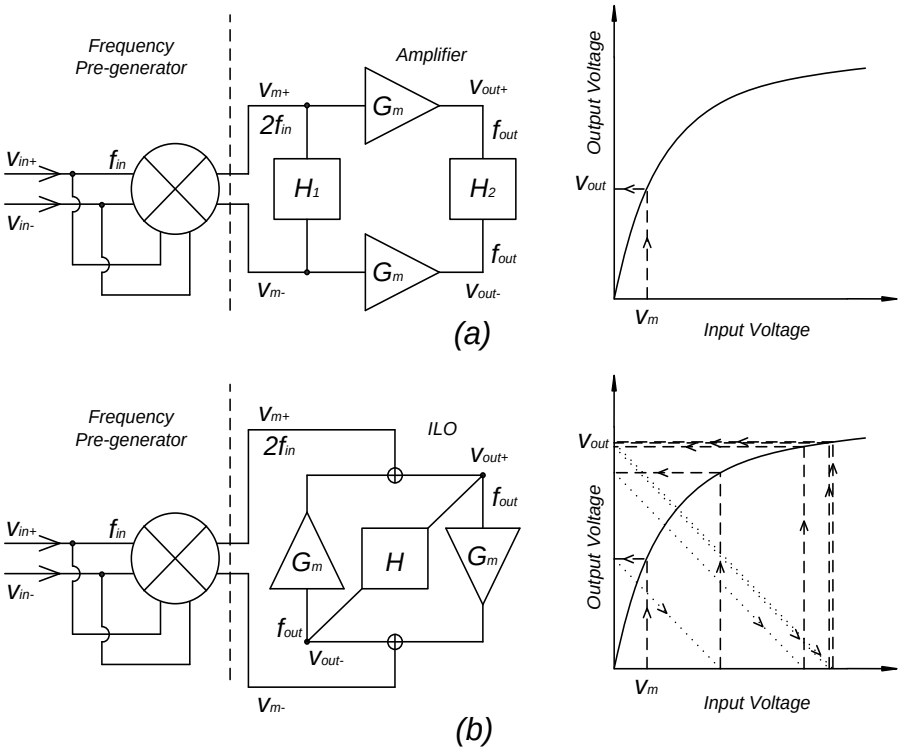

Figure 5.2: (a) Conventional topology and the amplifier's voltage gain (b) proposed topology and the ILO's voltage gain

5.2.2 Schematic of the proposed ILFM

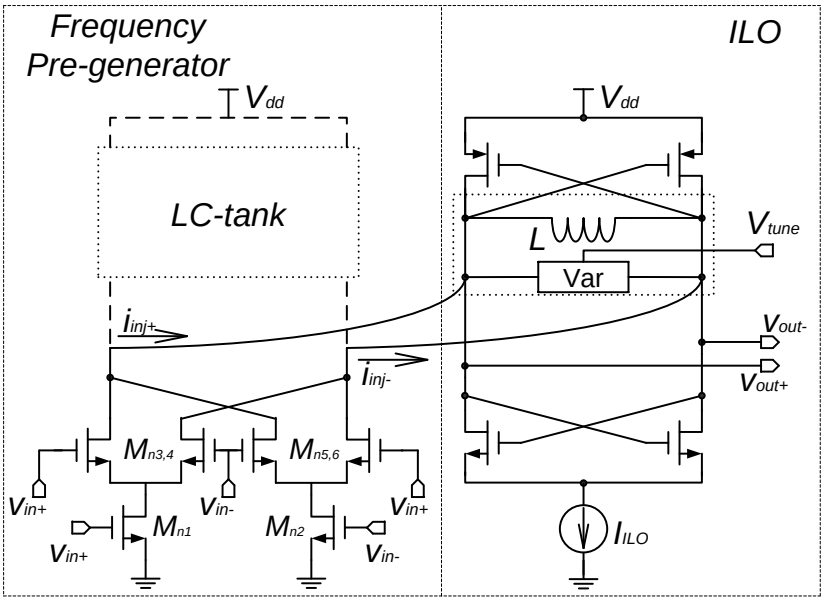

Figure 5.3: Schematic of the proposed ×2 ILFM

Based on the proposed topology, the schematic of the proposed ×2 ILFM is designed and shown in Figure 5.3. In the circuit, the mixer is designed based on a double-balanced Gilbert cell, which consists of six NMOS transistors. M_{n1} and M_{n2} form a transconductance stage and are biased by a DC voltage V_{B1} (not shown). M_{n3}, M_{n4}, M_{n5} and M_{n6} form a switching stage and are biased by another DC voltage V_{B2} (not shown). The inputs v_{in+} and v_{in-} of the proposed circuit are a pair of differential signal from a signal generator or a low-frequency PLL. M_{n1}, M_{n3}, and M_{n6} are connected to v_{in+} while M_{n2}, M_{n4}, and M_{n5} are connected to v_{in-}. The differential injection currents, i_{inj+} and i_{inj-}, are generated from the mixer and connected to the following ILO.

Based on a complementary structure with an LC tank, the ILO consumes a DC current I_{ILO} to keep its self-oscillation at a resonant frequency f_0. The LC tank is also used as the load of the mixer, which serves as a bandpass filter.

Only the frequency close to f_0 is selected at the output of the mixer. If $2f_{in}$ is close to f_0, the ILO is injection-locked to the injection current's frequency f_{inj}, which is equal to $2f_{in}$. Thus, f_{out} is equal to $2f_{in}$. The outputs v_{out+} and v_{out-} are connected to a buffer for measurement. An additional DC voltage V_{tune} is connected to a varactor in the ILO, which is used to tune f_0 through changing the capacitance of the ILO's LC tank and to further extend the ILFM's operation range.

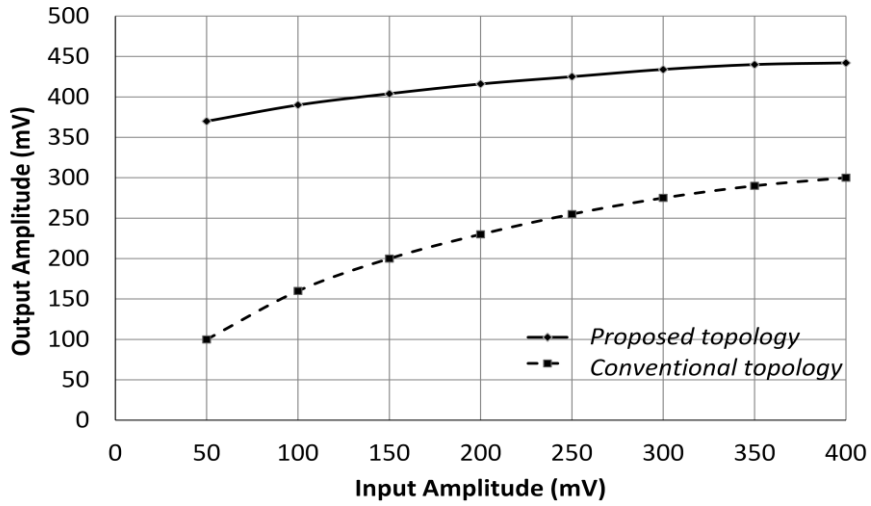

Figure 5.4: Simulated output amplitude versus input amplitude for both the proposed ILFM and the conventional frequency multiplier

In Figure 5.4, the simulated output amplitude versus input amplitude has been shown for both the proposed ILFM and the conventional frequency multiplier. Both these two frequency multipliers consume the same power. As expected, the ILFM has higher conversion gain than the conventional frequency multiplier. With a small input, the conventional frequency multiplier's output is also small. However, the proposed ILFM with the same input signal consistently has large output signal. Thus, the input signal from its previous stage can be reduced.

5.3 Analysis on the ILFM's Performance

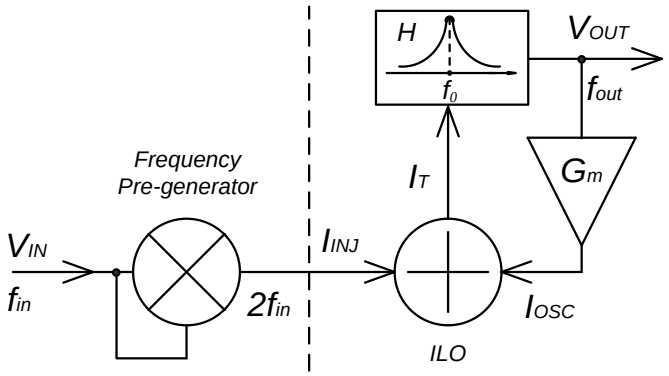

Figure 5.5: Simplified model of the proposed ×2 ILFM

The proposed ×2 ILFM can be analyzed based on the simplified model, which is shown in Figure 5.5. With the input V_{IN}, an injection current I_{INJ} is generated from the mixer, and it can be derived based on the inputs and sizes of the mixer's transistors. Subsequently, the LC-tank current I_T is the vector sum of I_{INJ} and the oscillation current I_{OSC} through the cross-coupled transistors. Note that for simplicity, I_{OSC} is equal to I_{ILO} based on the assumption that the cross-coupled transistors are always fully switched on or off. Finally, the ILFM's output V_{OUT} is generated after the effective impedance $H(f)$ of the LC tank, which can be expressed as

$$H(f) = \frac{R_p}{1+j2Q\left|\frac{f_0-f_{inj}}{f_0}\right|} \tag{5.1}$$

where R_p is the effective resistance of the LC tank with the quality factor of Q. Thus, the equations of the operation range and conversion gain can be derived mathematically.

5.3.1 Injection current in the proposed ILFM

In the transconductance stage of the mixer, the AC and DC voltages at the gates of M_{n1} and M_{n2} can be expressed as

$$v_1 = V_{B1} + V_{IN}\, cos(\omega_{in} t) \tag{5.2a}$$

$$v_2 = V_{B1} - V_{IN}\, cos(\omega_{in} t) \tag{5.2b}$$

where $\omega_{in} = 2\pi f_{in}$. Due to the same transistors sizes, the DC currents passing through M_{n1} and M_{n2} are half of the mixer's current consumption I_{MIX}. With the same transconductance $g_m = \frac{I_{MIX}}{V_{B1} - V_{TH}}$ in this stage, the currents through M_{n1} and M_{n2} are

$$i_1 = \frac{1}{2} I_{MIX} + \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}} \tag{5.3a}$$

$$i_2 = \frac{1}{2} I_{MIX} - \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}} \tag{5.3b}$$

In the switching stage, the AC and DC voltages at the gates of M_{n3}, M_{n4}, M_{n5}, and M_{n6} can be expressed as

$$v_3 = v_6 = V_{B2} + V_{IN}\, cos(\omega_{in} t) \tag{5.4a}$$

$$v_4 = v_5 = V_{B2} - V_{IN}\, cos(\omega_{in} t) \tag{5.4b}$$

With an appropriate value of V_{B2}, these four switching transistors can be swiftly and completely switched on or off by the differential input signals. Ideally, the currents through these four transistors can be expressed as

$$i_3 = \left[\frac{1}{2} I_{MIX} + \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}}\right] \cdot \left(\frac{1}{2} + \frac{1}{2} sgn[cos(\omega_{in} t)]\right) \tag{5.5a}$$

$$i_4 = \left[\frac{1}{2} I_{MIX} + \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}}\right] \cdot \left(\frac{1}{2} - \frac{1}{2} sgn[cos(\omega_{in} t)]\right) \tag{5.5b}$$

$$i_5 = \left[\frac{1}{2} I_{MIX} - \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}}\right] \cdot \left(\frac{1}{2} - \frac{1}{2} sgn[cos(\omega_{in} t)]\right) \tag{5.5c}$$

$$i_6 = \left[\frac{1}{2} I_{MIX} - \frac{I_{MIX} V_{IN}\, cos(\omega_{in} t)}{V_{B1} - V_{TH}}\right] \cdot \left(\frac{1}{2} + \frac{1}{2} sgn[cos(\omega_{in} t)]\right) \tag{5.5d}$$

Applying Fourier transform to the term $sgn[cos(\omega_{in}t)]$ and ignoring the high order harmonics,

$$sgn[cos(\omega_{in}t)] = \frac{4}{\pi}cos(\omega_{in}t) - \frac{4}{3\pi}cos(3\omega_{in}t) + \cdots \quad (5.6)$$

The differential currents from the mixer are obtained as

$$i_{inj+} = i_3 + i_5 = \frac{1}{2}I_{MIX} + \frac{2I_{MIX}V_{IN}}{\pi(V_{B1}-V_{TH})}\left[1 + \frac{2}{3}cos(2\omega_{in}t) - \frac{1}{3}cos(4\omega_{in}t)\right] \quad (5.7a)$$

$$i_{inj-} = i_4 + i_6 = \frac{1}{2}I_{MIX} - \frac{2I_{MIX}V_{IN}}{\pi(V_{B1}-V_{TH})}\left[1 + \frac{2}{3}cos(2\omega_{in}t) - \frac{1}{3}cos(4\omega_{in}t)\right] \quad (5.7b)$$

If f_0 is close to $2f_{in}$, the ILO is injection-locked by the term with $2\omega_{in}$. The effective injection current into the ILO is expressed as

$$i_{inj} = i_{inj+} - i_{inj-} = \frac{8I_{MIX}V_{IN}}{3\pi(V_{B1}-V_{TH})}cos(2\omega_{in}t) \quad (5.8)$$

Therefore, the magnitude of the injection current is

$$I_{INJ} = \frac{8I_{MIX}V_{IN}}{3\pi(V_{B1}-V_{TH})} \quad (5.9)$$

5.3.2 Operation range of the proposed ILFM

In the frequency pre-generator, the double-balanced Gilbert-cell mixer has wide dynamic range, which is much wider than the ILO's locking range. With proper design of f_0, the ILFM's operation range Δf is only limited by the latter, which is the output-frequency range in this circuit. Based on (3.12) in Chapter 3, the ILO's locking range can be derived with the injection current. Therefore, the equation for the maximum deviation of f_{inj} from f_0 is given by

$$f_0 - f_{inj} = \frac{f_0}{2Q} \cdot \frac{I_{INJ}}{\sqrt{I_{ILO}^2 - I_{INJ}^2}} \quad (5.10)$$

With understanding that the ILFM's operation range includes $(f_{inj} - f_0)$ and $(f_0 - f_{inj})$ and by substituting (5.9) into it,

$$\Delta f = \frac{f_0}{Q} \cdot \frac{I_{INJ}}{\sqrt{I_{ILO}^2 - I_{INJ}^2}} = \frac{f_0}{Q} \cdot \frac{8 I_{MIX} V_{IN}}{\sqrt{\left(3\pi I_{ILO}(V_{B1} - V_{TH})\right)^2 - (8 I_{MIX} V_{IN})^2}} \tag{5.11}$$

5.3.3 Conversion gain of the proposed ILFM

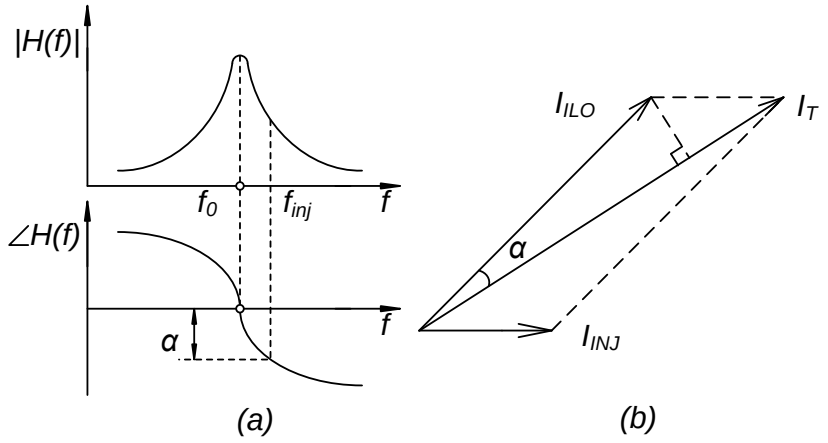

Figure 5.6: (a) Open-loop characteristic and (b) phasor diagram of the LC tank in the ILO

Based on the model in Figure 5.5, the open-loop characteristic of the LC tank and the phasor diagram in the ILO is shown in Figure 5.6. In the vicinity of resonance, a phase shift α in Figure 5.6 (a) is caused by the injection current. In [11],

$$tan\,\alpha \approx \frac{2Q}{f_0} \cdot \left|f_0 - f_{inj}\right| \tag{5.12}$$

Thus, sine and cosine of α can be expressed as

$$cos\,\alpha = \frac{f_0}{\sqrt{f_0^2 + 4Q^2\left(f_0 - f_{inj}\right)^2}} \tag{5.13}$$

$$sin\,\alpha = \frac{2Q\left|f_0 - f_{inj}\right|}{\sqrt{f_0^2 + 4Q^2\left(f_0 - f_{inj}\right)^2}} \tag{5.14}$$

When the ILO is injection-locked, the phase difference of I_{ILO} and I_{INJ} is smaller than (π/2). In Figure 5.6 (b), their sum I_T is shown and derived geometrically.

$$I_T = I_{ILO} \cdot cos\,\alpha + \sqrt{I_{INJ}^2 - (I_{ILO} \cdot sin\,\alpha)^2} \tag{5.15}$$

By substituting (5.13) and (5.14) into (5.15), the magnitude of the LC-tank current is expressed as

$$I_T = \frac{I_{ILO} \cdot f_0 + \sqrt{I_{INJ}^2 \cdot \left(f_0^2 + 4Q^2 (f_0 - f_{inj})^2\right) - I_{ILO}^2 \cdot 4Q^2 (f_0 - f_{inj})^2}}{\sqrt{f_0^2 + 4Q^2 (f_0 - f_{inj})^2}} \tag{5.16}$$

By differentiating (5.15) with respect of I_{ILO},

$$\frac{d\,I_T}{dI_{ILO}} = cos\,\alpha - \frac{sin^2\,\alpha \cdot I_{ILO}}{\sqrt{I_{INJ}^2 - (I_{ILO} \cdot sin\,\alpha)^2}} \tag{5.17}$$

By differentiating (5.17) again, it can been seen that $\frac{d^2\,I_T}{dI_{ILO}{}^2}$ is always negative. Thus, I_T is maximized when $\frac{d\,I_T}{dI_{ILO}} = 0$. At the maximum value, it can be derived as

$$I_{ILO} = I_{INJ} \cdot cot\,\alpha = I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|} \tag{5.18}$$

Therefore, $\frac{d\,I_T}{dI_{ILO}} > 0$ when $I_{ILO} < I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|}$. Conversely, $\frac{d\,I_T}{dI_{ILO}} < 0$ when $I_{ILO} > I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|}$.

Based on the ILFM's model in Figure 5.5, it can be expressed as

$$V_{OUT} = I_T \cdot |H(f)| \tag{5.19}$$

By substituting (5.1) and (5.16) into (5.19),

$$V_{OUT} = \frac{I_{ILO} \cdot f_0^2 R_P + f_0 R_P \sqrt{I_{INJ}^2 \cdot \left(f_0^2 + 4Q^2 (f_0 - f_{inj})^2\right) - I_{ILO}^2 \cdot 4Q^2 (f_0 - f_{inj})^2}}{f_0^2 + 4Q^2 (f_0 - f_{inj})^2} \tag{5.20}$$

Consequently, the conversion gain of the proposed ILFM can be obtained as

$$\frac{V_{OUT}}{V_{IN}} = \frac{I_{ILO} \cdot f_0^2 R_P + f_0 R_P \sqrt{I_{INJ}^2 \cdot \left(f_0^2 + 4Q^2 (f_0 - f_{inj})^2\right) - I_{ILO}^2 \cdot 4Q^2 (f_0 - f_{inj})^2}}{V_{IN} \cdot \left[f_0^2 + 4Q^2 (f_0 - f_{inj})^2\right]} \quad (5.21)$$

By differentiating (5.21) with respect of I_{ILO},

$$\frac{d}{dI_{ILO}}\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{f_0 R_p}{V_{IN} \cdot \sqrt{{f_0}^2 + 4Q^2 (f_0 - f_{inj})^2}} \cdot \frac{d\, I_T}{dI_{ILO}} \quad (5.22)$$

By substituting (5.17) into (5.22),

$$\frac{d}{dI_{ILO}}\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{f_0 R_p}{V_{IN} \cdot \sqrt{{f_0}^2 + 4Q^2 (f_0 - f_{inj})^2}} \cdot \left(cos\, \alpha - \frac{sin^2\, \alpha \cdot I_{ILO}}{\sqrt{I_{INJ}^2 - (I_{ILO} \cdot sin\, \alpha)^2}} \right) \quad (5.23)$$

Based on the conclusion drawn from (5.17), it can be expected that $\frac{d}{dI_{ILO}}\left(\frac{V_{OUT}}{V_{IN}}\right) > 0$ when $I_{ILO} < I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|}$, otherwise $\frac{d}{dI_{ILO}}\left(\frac{V_{OUT}}{V_{IN}}\right) < 0$. Therefore, the conversion gain is increased with I_{ILO} until $I_{ILO} = I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|}$, then is decreased. Note that the lower limit of I_{ILO} is I_{INJ} from (5.11) while its upper limit is $I_{INJ} \cdot \frac{\sqrt{f_0^2 + 4Q^2 (f_0 - f_{inj})^2}}{2Q|f_0 - f_{inj}|}$ from (5.16).

For the lowest power consumption in the proposed ILFM, I_{ILO} can be reduced to as small as I_{INJ}. Thus, the conversion gain is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2I_{INJ} \cdot f_0^2 R_P}{V_{IN} \cdot \left[f_0^2 + 4Q^2 (f_0 - f_{inj})^2\right]} = \frac{16 I_{MIX}}{3\pi (V_{B1} - V_{TH})} \cdot \frac{f_0^2 R_P}{f_0^2 + 4Q^2 (f_0 - f_{inj})^2} \quad (5.24)$$

For high conversion gain in the proposed ILFM, I_{ILO} should be equal to $I_{INJ} \cdot \frac{f_0}{2Q \cdot |f_0 - f_{inj}|}$. Thus, the conversion gain can be maximized to

$$\frac{V_{OUT}}{V_{IN}} = \frac{I_{INJ} \cdot f_0 R_P}{V_{IN} \cdot 2Q|f_0 - f_{inj}|} = \frac{4 I_{MIX}}{3\pi (V_{B1} - V_{TH})} \cdot \frac{f_0 R_P}{2Q \cdot |f_0 - f_{inj}|} \quad (5.25)$$

5.4 Simulated and Experimental Results of the Proposed ILFM

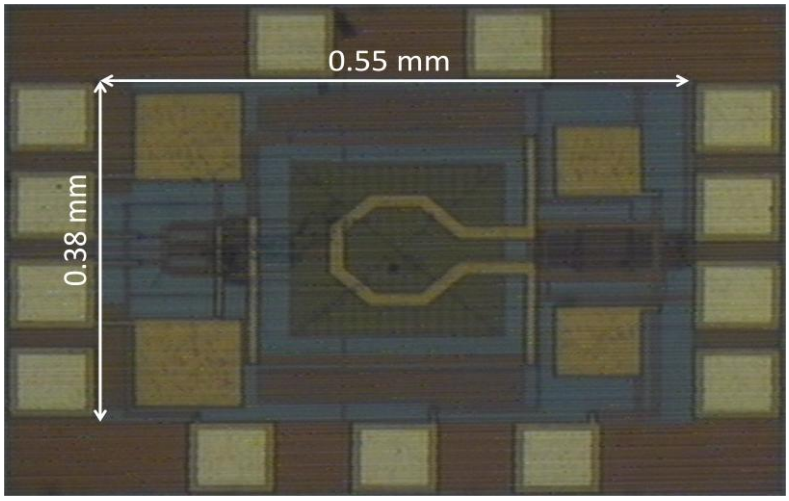

Figure 5.7: Die micrograph of the proposed ILFM

The proposed ILFM has been designed and fabricated in the 0.18 μm CMOS technology. The die microphotograph is shown in Figure 5.7. The size of the proposed circuit is 0.55 mm × 0.38 mm. With the supply voltage of 1.8 V, the measured current and power consumption for the core circuit are 3.7 mA and 6.66 mW, respectively.

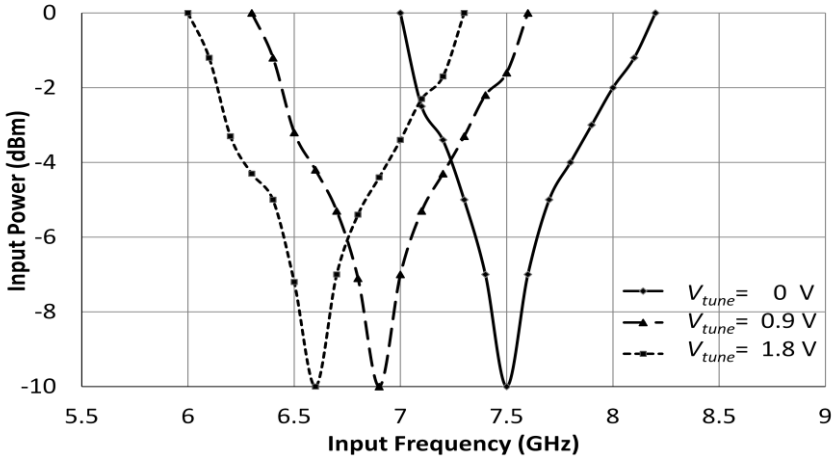

Figure 5.8: Measured input sensitivity of the ×2 ILFM with various V_{tune}

In Figure 5.8, the measured input sensitivity of the ILFM is shown. With V_{tune} of 0 V and the 0 dBm input, the input-frequency range of the ILFM is 7 GHz to 8.2 GHz. Through varying V_{tune} from 0 V to 1.8 V, the input-frequency range is shifted to the left because of f_0 changed from 15 GHz to 13.2 GHz. Thus, with the 0 dBm input and varying V_{tune}, the overall input-frequency range is 6 GHz to 8.2 GHz. As shown in Figure 5.8, even with the input of -10 dBm, the overall input-frequency range is still 6.6 GHz to 7.5 GHz.

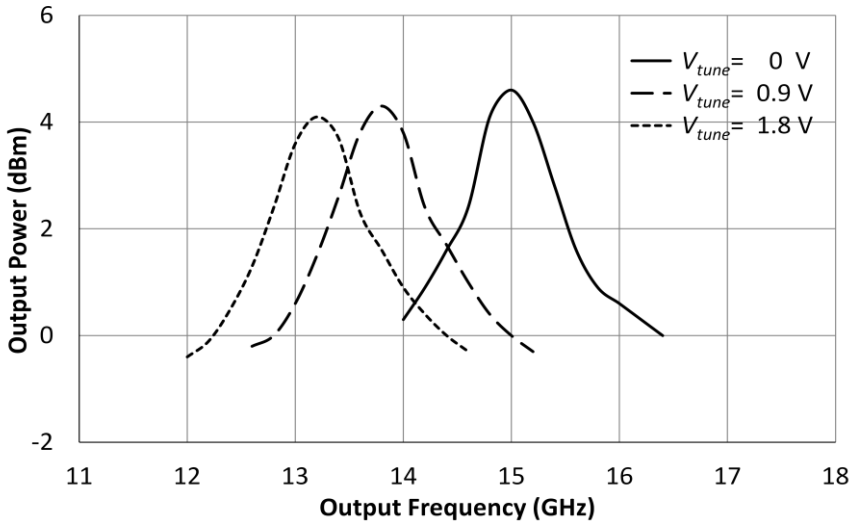

Figure 5.9: Measured output power versus the output frequency of the ILFM with various V_{tune}

In Figure 5.9, the measured output power versus the output frequency of the ILFM is shown with various V_{tune}. With the 0 dBm input, the ILFM's operation range is 12 GHz to 16.4 GHz. The output power is reduced when the output frequency is deviated from f_0. In this circuit, f_0 can be shifted through varying V_{tune}, so the output power can be kept higher than 0 dBm in the operation range from 12.4 GHz to 16.4 GHz.

Fundamental rejection (*FR*) is defined as the difference in the output power

of the desired frequency to that of the fundamental frequency. As shown in Figure 5.10, the *FR* of 38 dB is obtained with the 0 dBm input and the 3.7 mA current consumption in the proposed ILFM. It can be seen that this proposed ILFM is suitable for even-order frequency multiplier as only even-order harmonics of the input frequency can be generated by the doubled-balanced mixer.

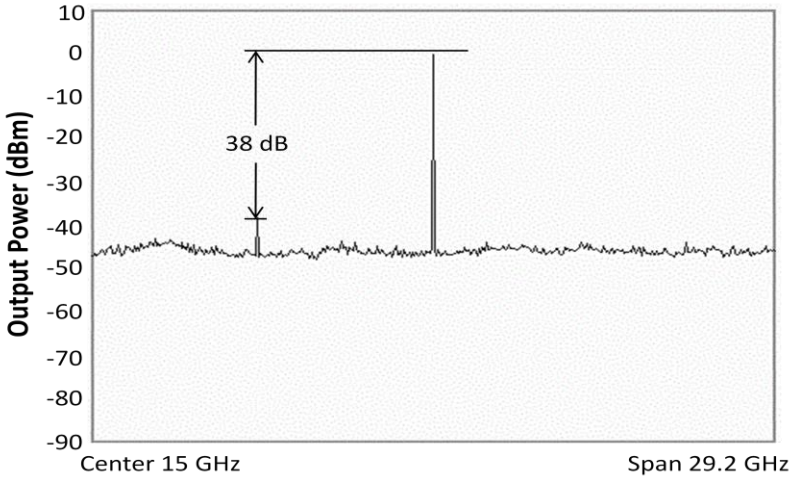

Figure 5.10: Measured output power spectrum of the fundamental and desired frequencies

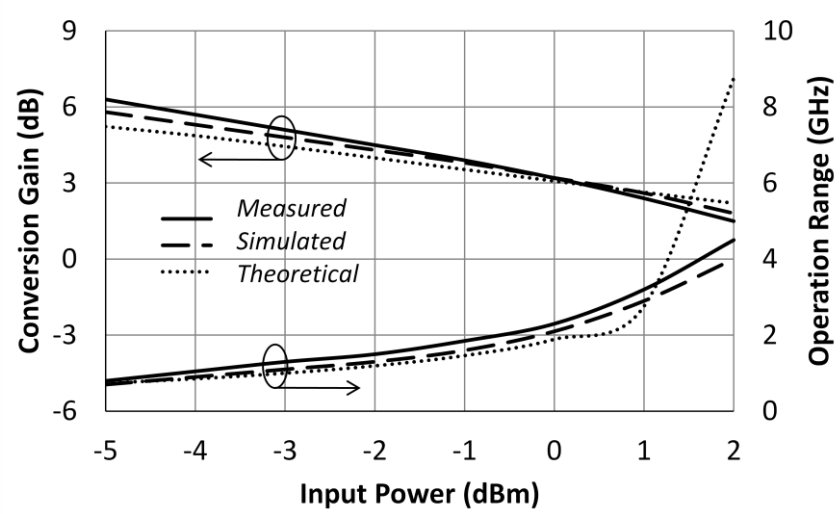

Figure 5.11: Conversion gain and operation range versus the input power

In Figure 5.11, the conversion gain and operation range versus the input power of the ILFM is shown, where the consumed current is 3.7 mA and the output frequency is selected to be 0.3 GHz from f_0. The higher conversion gain will be obtained if the output frequency is selected to be f_0, as shown in Figure 5.9 due to the higher output power. When the input power is changed from -5 dBm to 2 dBm, the theoretical, simulated and measured operation ranges are increased. Conversely, the theoretical, simulated and measured conversion gains are reduced with the input power.

The simulated and measured conversion gains of the ILFM match with its theoretical conversion gain. However, with large input power, there is a discrepancy between its simulated/measured and theoretical operation ranges. Theoretically, the injection current I_{INJ} generated from the double-balanced mixer increases with the input signal V_{IN}. Based on (5.10), the operation range increases with I_{INJ}. However, (5.10) is derived from (3.11) based on the assumption that the deviation of ω_{inj} from ω_0 is much smaller than ω_0. When the operation range is very large due to a large input power, (5.10) is no longer accurate and thus the theoretical results based on (5.10) deviate from the simulated/measured results. In addition, the equation of the conversion gain of the ILFM is still valid with high input power because the conversion gains with different input powers are measured at a fixed input frequency.

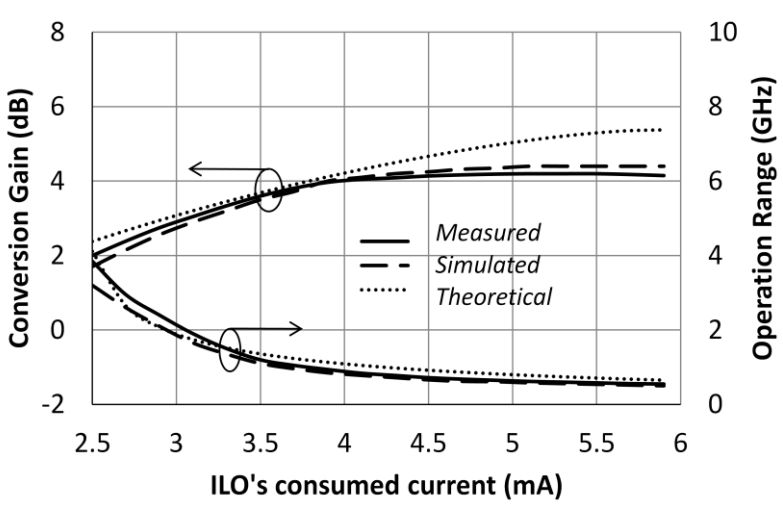

Figure 5.12: Conversion gain and operation range versus the ILO's consumed current

In Figure 5.12, the conversion gain and operation range versus I_{ILO} is shown. Similarly, the input power is 0 dBm and the output frequency is selected to be 0.3 GHz from f_0. It can be seen that the theoretical, simulated and measured conversion gains are increased with increasing I_{ILO}. Conversely, the theoretical, simulated and measured operation ranges are reduced with increasing I_{ILO}.

The simulated and measured operation ranges of the ILFM match with the theoretical results. However, there is a discrepancy between its simulated/measured and theoretical conversion gains when the ILO's consumed current is larger than 4 mA. The discrepancy is because that the ILO will go into voltage limited region [47] when the ILO's consumed current is very large, as its output voltage is clipped by the supply voltage. As a result, the discrepancy between the theoretical and simulated/measured conversion gains of the ILFM increases gradually when the ILO's consumed current increases to be larger than 4 mA.

5.5 Fractional Frequency Multiplier

Including the proposed ILFM, the current designs in [97] [98] have the same severe limitation that their multipliers are all integers but not fractional numbers. However, it is important to design an FFM for many applications. In a frequency synthesizer, the FFM can generate a fixed output frequency as an LO signal, which is driven by a low-frequency PLL.

5.5.1 Topology of the proposed ×*(n+1)/n* ILFM

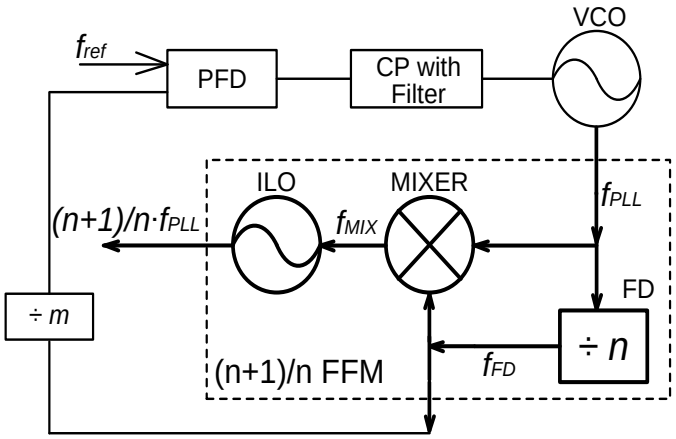

Figure 5.13: Topology of the proposed ×*(n+1)/n* FFM with a PLL for f_{PLL} and *(n+1)/n* f_{PLL}

Generally, a frequency synthesizer is designed based on a PLL, which consists of a PFD, a charge pump (CP) with loop filter, a VCO and many stages of FDs in the feedback path. In Figure 5.13, it is shown that the proposed ×*(n+1)/n* FFM is designed with and driven by the PLL. The proposed FFM consists of an ILO, a mixer and a divide-by-*n* FD, where *n* is an integer. Note that this FD can be reused in the PLL to serve as a the first-stage FD.

The PLL's output frequency f_{PLL} is generated from the VCO and is connected

to the divide-by-*n* FD. Subsequently, a frequency f_{FD} is generated from the FD, which is equal to $(1/n)\ f_{PLL}$. The FD's output signal is connected to both the following divide-by-*m* FD in the PLL and the up-conversion mixer in the FFM. Thus, the mixer's output frequency f_{MIX} is equal to $(n+1)/n\ f_{PLL}$, which is connected to the ILO. In the proposed FFM, the ILO is used to amplify the mixer's output to drive the next stage. When the ILO is injection-locked by f_{MIX}, the ILO's output frequency f_{ILO} is equal to $(n+1)/n\ f_{PLL}$. Therefore, the frequency synthesizer with the $\times(n+1)/n$ FFM can provide the signals of f_{PLL} from the PLL and $(n+1)/n\ f_{PLL}$ from the FFM. This design is useful to support some dual-band applications, which provides two different frequencies based on one PLL operating at the lower frequency.

5.5.2 Schematic of the proposed FFM

Based on the topology of $\times(n+1)/n$ FFM, the schematic of the $\times(3/2)$ FFM is proposed in Figure 5.14, where n=2 for this example. In this design, the divide-by-2 FD is an ILFD based on a complementary cross-coupled oscillator, which consists of an inductor L_1, NMOS and PMOS transistors and an injection transistor M_{inj}. The FD consumes a DC current I_{FD} to resonate at a frequency $f_{0,FD}$ with an LC tank, which has an effective impedance H_{FD} and a quality factor Q_{FD}. An input signal v_{in} is connected to the gate of M_{inj} at a frequency f_{in}. At the FD's outputs, v_{fd+} and v_{fd-}, f_{FD} is generated to be $(1/2)\ f_{in}$.

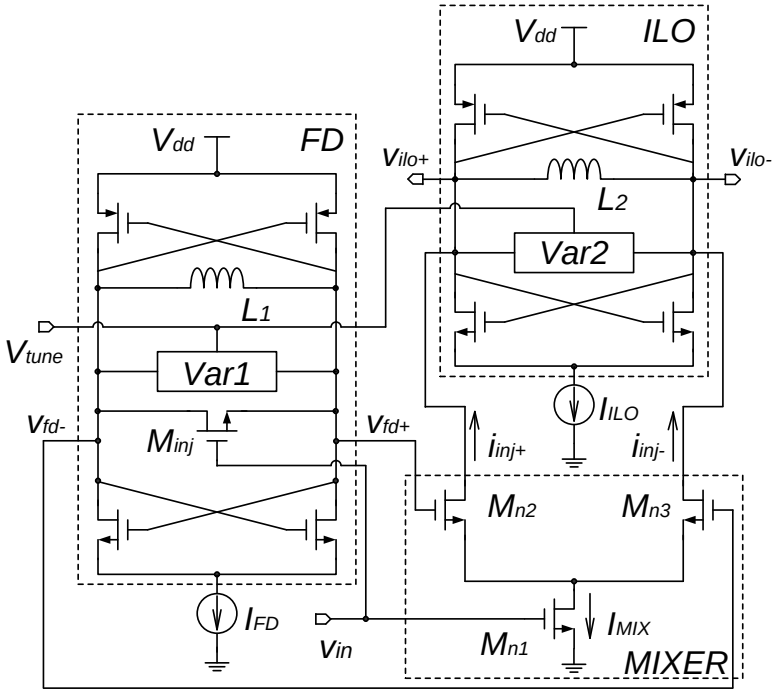

Figure 5.14: Schematic of the proposed ×(3/2) FFM

The mixer is designed based on a single-balanced Gilbert cell, which consists of three NMOS transistors. v_{in} is connected to M_{n1} while v_{fd+} and v_{fd-} are connected to M_{n2} and M_{n3}, respectively. Consequently, the injection currents, i_{inj+} and i_{inj-}, are generated by the mixer at f_{MIX} and connected to the ILO.

The ILO consists of an inductor L_2 and complementary cross-coupled transistors. The ILO consumes a DC current I_{ILO} to resonate at a frequency $f_{0,ILO}$, which has an LC tank with a quality factor Q_{ILO}. The LC tank is also used as the load of the mixer, which serves as a bandpass filter. Thus, only the frequency close to $f_{0,ILO}$ is selected at the mixer's output. In the ILO's operation range, the ILO is injection-locked by the mixer's output operating at f_{MIX}. Thus, the FFM's output frequency f_{ILO} is equal to *(3/2)* f_{in}, where the ILO's outputs, v_{ilo+} and v_{ilo-}, are connected to an output buffer for measurement.

Furthermore, two varactors *Var1* and *Var2* are implemented in the FD and

the ILO, respectively, which are both tuned by a DC voltage V_{tune}. In order to shift both $f_{0,FD}$ and $f_{0,ILO}$ in the same direction, the capacitances in the LC tanks of the FD and ILO are changed simultaneously. Thus, the FFM's operation range can be extended, which is defined as the FFM's output-frequency range. In addition, another varactor is connected in parallel to *Var1*, not shown in Figure 5.14 for simplicity. It will be independently tuned once and then fixed to offset the effect of process variation on $f_{0,FD}$.

5.6 Analysis on Performance of the Proposed FFM

In the proposed FFM, the Gilbert-cell mixer has wide dynamic range, which is much wider than the FD's output-frequency range Δf_{FD} and a third of the ILO's output-frequency range Δf_{ILO}. Thus, it is more important to optimize both Δf_{FD} and Δf_{ILO} than the mixer's input-frequency range. Note that in a proper design, the FFM's operation range will be limited by the smaller of $3\Delta f_{FD}$ and Δf_{ILO}.

5.6.1 Output-frequency range of the FD

In Chapter 3, it is asserted that the ILFD's locking range is dependent on its injection current and its oscillation current. Similar to (5.11), the FD's output-frequency range includes $\left(f_{FD} - f_{0,FD}\right)$ and $\left(f_{0,FD} - f_{FD}\right)$ can be expressed as

$$\Delta f_{FD} = \frac{f_{0,FD}}{Q_{FD}} \cdot \frac{I_D}{\sqrt{I_{FD}^2 - I_D^2}} \tag{5.26}$$

where the FD's injection current I_D is the magnitude of the AC current in the drain of M_{inj} and the FD's oscillation current is equal to I_{FD} based on the

assumption that the cross-coupled transistors are fully switched on and off.

5.6.2 Output-frequency range of the ILO

In [47], the FD's output V_{FD} can be expressed as

$$V_{FD} = I_{FD} \cdot H_{FD} \tag{5.27}$$

Subsequently, V_{FD} can be mixed with the input V_{IN} to generate the injection current from the mixer. Thus, the magnitude of the injection current for the ILO is expressed as

$$I_{INJ} = \alpha \cdot V_{IN} \cdot V_{FD} \tag{5.28}$$

where α is the mixer's conversion constant.

By substituting (5.27) into (5.28),

$$I_{INJ} = \alpha \cdot V_{IN} \cdot I_{FD} \cdot H_{FD} \tag{5.29}$$

Similarly, Δf_{ILO} can be expressed as

$$\Delta f_{ILO} = \frac{f_{0,ILO}}{Q_{ILO}} \cdot \frac{I_{INJ}}{\sqrt{I_{ILO}^2 - I_{INJ}^2}} \tag{5.30}$$

where I_{ILO} is the oscillation current in the ILO.

By substituting (5.29) into (5.30),

$$\Delta f_{ILO} = \frac{f_{0,ILO}}{Q_{ILO}} \cdot \frac{\alpha \cdot V_{IN} \cdot I_{FD} \cdot H_{FD}}{\sqrt{I_{ILO}^2 - (\alpha \cdot V_{IN} \cdot I_{FD} \cdot H_{FD})^2}} \tag{5.31}$$

5.6.3 Optimized operation range of the proposed FFM

In the operation range of the proposed FFM, f_{ILO} is equal to $3f_{FD}$. In order for the FFM to achieve the maximum operation range, the two conditions should be fulfilled simultaneously: (1) Δf_{ILO} should be equal to $3\Delta f_{FD}$; (2) $f_{0,ILO}$ should be close to $3f_{0,FD}$.

In order to satisfy the first condition, both Δf_{ILO} and $3\Delta f_{FD}$ can be optimized based on (5.26) and (5.31). For the second condition, $f_{0,ILO} \approx 3f_{0,FD}$ can be achieved through careful selection of inductor and capacitor values in the ILO. As shown in Figure 5.15, the FFM's operation range is maximized through equalization of Δf_{ILO} and $3\Delta f_{FD}$, which is from f_A to f_B. If the resonant frequency of the ILO is $f_{0,ILO}'$, the FFM's operation range in this figure will be reduced due to the mismatch between Δf_{ILO} and $3\Delta f_{FD}$, which is from f_A to f_C.

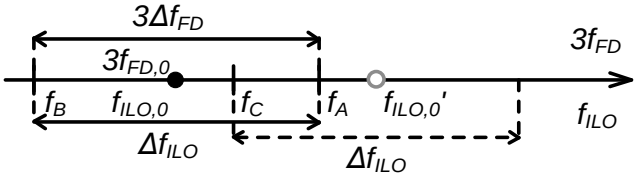

Figure 5.15: Relationship between the output-frequency ranges of the FD and the ILO

5.7 Simulated and Experimental Results of the Proposed ×(3/2) FFM

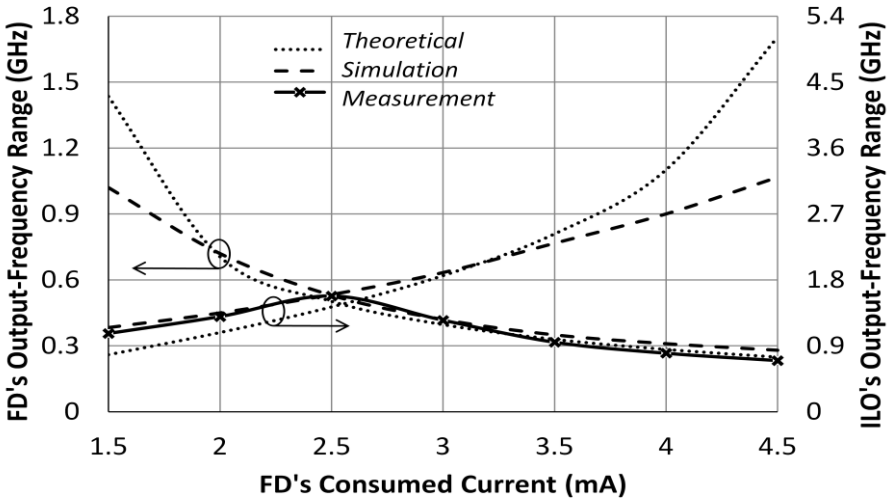

Figure 5.16: The FD's and the ILO's output-frequency ranges and the proposed FFM's operation range versus I_{FD}

Based on (5.26), Δf_{FD} is reduced with increasing I_{FD}. Conversely, based on (5.31), Δf_{ILO} is increased with I_{FD}. The theoretical results for this design with an input of -0.5 dBm are shown in Figure 5.16. It can be observed that Δf_{ILO} is equal to $3\Delta f_{FD}$ when I_{FD} is close to 2.5 mA. In this figure, the simulated results are also shown for Δf_{FD} and Δf_{ILO} versus I_{FD}. With the same input, the simulated Δf_{FD} is reduced from 1.02 GHz to 0.28 GHz with increasing I_{FD} from 1.5 mA to 4.5 mA. Conversely, the simulated Δf_{ILO} is increased from 1.2 GHz to 3.2 GHz. Thus, it is verified through the simulation that Δf_{ILO} is close to $3\Delta f_{FD}$ at I_{FD}=2.5 mA. Conclusively, the FFM's operation range can be maximized when I_{FD} is close to 2.5 mA in this design with the input of -0.5 dBm.

As discussed in Section 5.6.3, the FFM's operation range is limited by the smaller one between the FD's and ILO's output-frequency ranges. Therefore, the measured results are matched well with the simulated results in Figure 5.16. However, the simulated FD's and ILO's output-frequency ranges are smaller than their theoretical values when the FD's consumed current is very small or very large.

Similar to the explanation for Figure 5.11, both (5.26) and (5.31) are derived based on the assumption that the deviation of ω_{inj} from ω_0 is much smaller than ω_0. The FD's output-frequency range is very large due to a small FD's consumed current. As a result, (5.26) is no longer accurate and thus the theoretical results based on (5.26) deviate from the simulated results. Similarly, the ILO's output-frequency range is very large due to a large FD's consumed current. As a result, (5.31) is not accurate and thus the theoretical results based on (5.31) deviate from the simulated results.

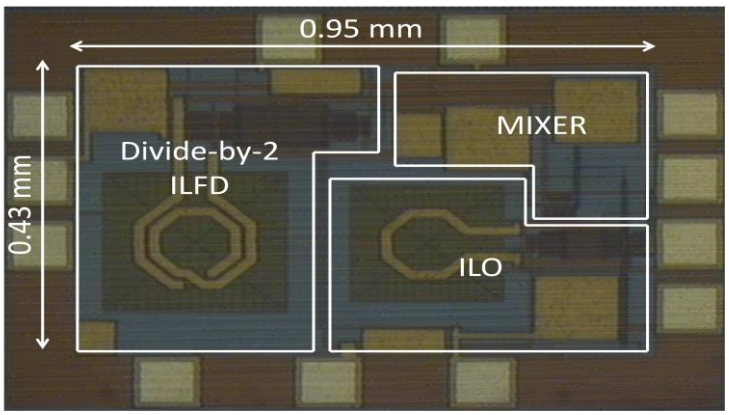

Figure 5.17: Die micrograph of the proposed ×(3/2) ILFM

The proposed ×(3/2) FFM has been designed and fabricated in the 0.18 µm CMOS technology. The die microphotograph is shown in Figure 5.17. The die size of the proposed circuit is 0.95 mm × 0.43 mm. With a supply voltage of 1.8 V, the measured FFM's operation range is shown in Figure 5.16, where the widest operation range appears at I_{FD}=2.5 mA. Hence, the 2.5 mA current is consumed by the divide-by-2 FD for the optimized FFM's operation range. Thus, the total power consumption is 9.54 mW, including the FD, the mixer and the ILO. However, the divide-by-2 FD can be designed as the part of the driving PLL, then the FD's power consumption of 4.5 mW can be reused by the driving PLL. Hence, only the additional power consumption of 5.04 mW is consumed to implement the fractional frequency multiplication.

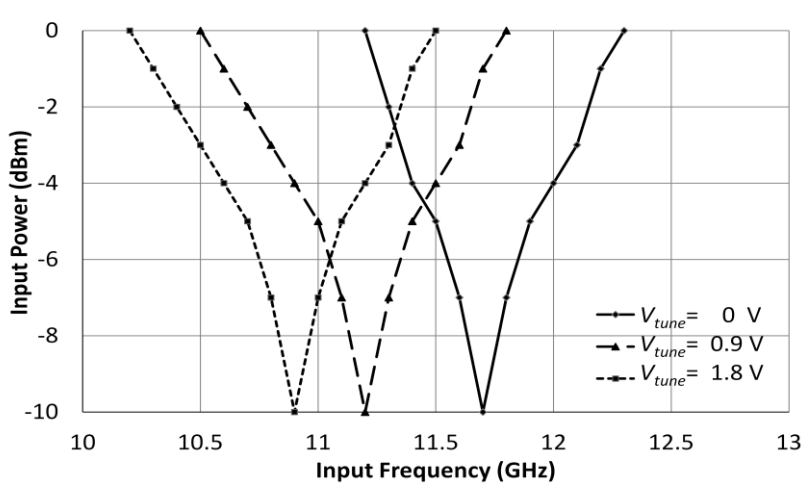

Figure 5.18: Measured input sensitivity of the FFM with various V_{tune}

In Figure 5.18, the measured input sensitivity of the FFM is shown with various V_{tune}. At V_{tune}=0 V, the FFM's input-frequency range with a 0 dBm input is from 11.2 GHz to 12.3 GHz. Through varying V_{tune} from 0 V to 1.8 V, both $f_{0,FD}$ and $f_{0,ILO}$ are changed simultaneously, and then the FFM's input-frequency range is shift to the left. Consequently, the FFM's input-frequency range is 10.2 GHz to 12.3 GHz. Even with a -10-dBm input, the FFM's input frequency range is still 10.9 GHz to 11.7 GHz.

In Figure 5.19, the measured output power versus the output frequency is shown with various V_{tune}. With the 0 dBm input, the FFM's operation range is 15.3 GHz to 18.45 GHz. The FFM's output power is reduced when its output frequency is deviated from $f_{0,ILO}$. Through varying V_{tune}, higher output power can be obtained in the FFM's operation range.

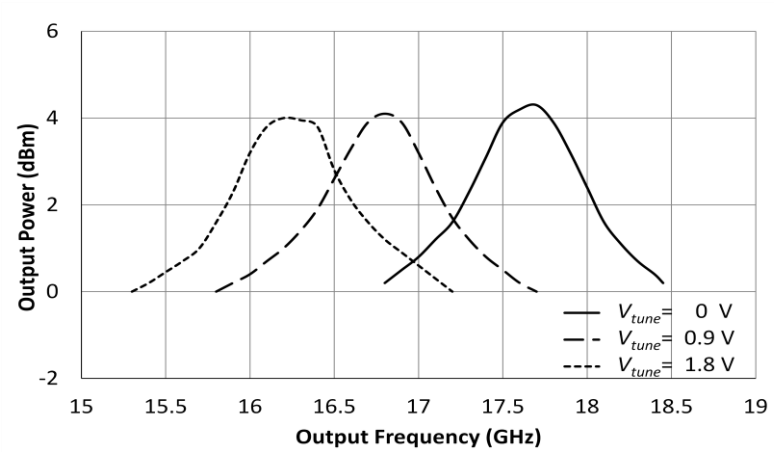

Figure 5.19: Measured output power versus its output frequency with various V_{tune}.

The measured and simulated phase noises of the input and output from 0.1-kHz to 1-MHz offset frequency are shown in Figure 5.20, where the solid and dotted lines represent the measured and simulated results, respectively.

Theoretically, the phase noise of the FFM's output is 3.5 (=20log(3/2)) dB higher than that of its input. As expected, The difference between the upper and lower dotted lines is almost 3.5 dB, where both lines represent the simulated phase noises of the FFM's output and input, respectively.

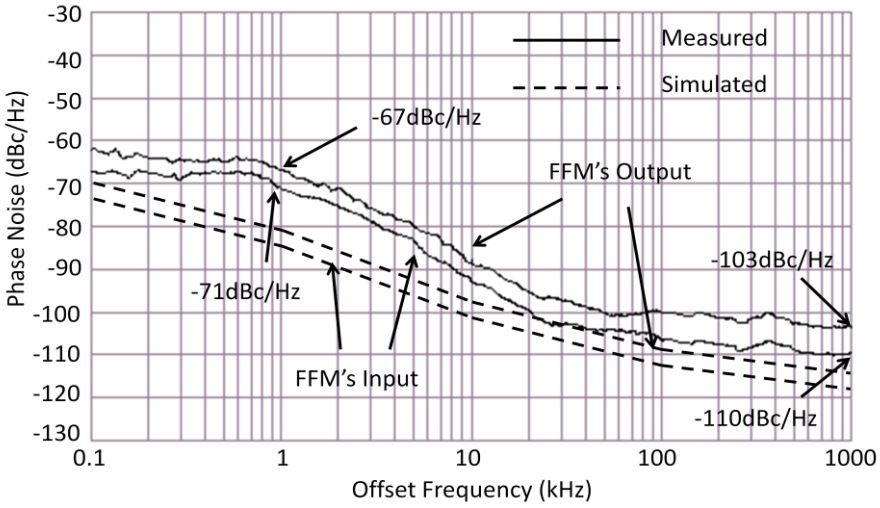

Figure 5.20: Measured and simulated phase noises of the input and output of the proposed FFM

Similarly, the upper and lower solid lines represent the measured phase noise of the FFM's output and input, respectively. The FFM's input is from a signal generator. At 1-kHz offset frequency, the phase noise difference between the input and output signals approaches the theoretical value. However, the phase noise difference is 7 dB at 1-MHz offset frequency. The FFM's phase noise degradation at high offset frequency is mainly contributed by the thermal noise from the FFM.

5.8 Summary

In this chapter, the proposed ×2 ILFM is presented after reviewing some conventional frequency multipliers. The circuit has been fabricated in the 0.18 μm CMOS technology. The equations of operation range and conversion gain in the ILFM are derived and verified through the measured results. In Table 5.1, comparisons are made among different frequency multipliers. Through intensive literature review, there is no well-defined FoM for an ILFM to compare with other frequency multipliers. Hence, an FoM of the ILFM is proposed as

$$\text{FoM} = 10\,log\left(\frac{P_{out}}{P_{in}+P_{DC}}\right) + 20\,log\left(\frac{\Delta f}{f_{out}}\right) + 50 \tag{5.32}$$

where P_{out} is the output power, P_{in} is the input power, P_{DC} is the DC power consumption and $(\Delta f/f_{out})$ is the ratio between the output-frequency range and the output frequency.

The first term $10\,log\left(\frac{P_{out}}{P_{in}+P_{DC}}\right)$ gives the power efficiency. Power efficiency is important for this circuit because the high-frequency circuit is a significant

power-consumed block in a RF system.

The second term $20\,log\left(\frac{\Delta f}{f_{out}}\right)$ normalizes the operation range relative to the output frequency. A wide operation range is an important advantage for high-frequency circuits, which can accommodate wider input frequency ranges for different applications. It is noted that the frequency ratio is in the first order while the power ratio is in the second order.

+50 dB is added to keep every FoM positive. This will not affect the relative FoM, but it is convenient to compare with previous works.

FR as the fundamental rejection at the output is also an important factor, which shows the power passing through the circuit from the input to output. It can be used as a supplementary element in another FoM, which can be defined as FoM*

$$\text{FoM}^* = 10\,log\left(\frac{P_{out}}{P_{in}+P_{DC}}\right) + FR + 20\,log\left(\frac{\Delta f}{f_{out}}\right) + 50 \quad (5.33)$$

Based on the calculated FoM and FoM* in Table 5.1, the proposed ×2 ILFM has high conversion gain, low power consumption, the best FoM and FoM*. This makes the proposed ×2 ILFM a suitable design for high-frequency and low-power applications.

The topology of the *×(n+1)/n* ILFM is proposed for fractional frequency multiplication, where a ×(3/2) FFM is designed as an example. The proposed circuit has been fabricated in the 0.18 μm CMOS technology. The design equations of the FFM's operation range are derived and verified through simulation and measurement. The performances of the FFM are summarized in Table 5.1. Based on comparisons among these frequency multipliers, the FFM has high conversion gain and low requirement on the input power and DC

power consumption. This makes the proposed FFM a suitable design for high-frequency dual-band applications.

Table 5.1: The performance comparison of the frequency multipliers

	[99]	[100]	[101]	[102]	×2 ILFM	×(3/2) FFM
Technology (CMOS)	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Multiplier	2	2	3	2	2	3/2
Supply Voltage (V)	2.6	1.3	1.5	1.8	1.8	1.8
DC Power (mW)	20.8	10.5	7.5	12.6	6.66	5.05 (FFM) 9.55 (with FD)
Input Power (dBm)	0	2	10	-7	0	0
f_{out} (GHz)	20~24	18~26	18~24	5.2~5.8	12~16.4	15.3~18.45
Conversion Gain (dB)	>-4.5	>-12	>-17	>0	>-0.4	>0
FR (dB)	30~50	30~40	10~23	20	38~45	30~38
FoM (dB)	17.31	20.39	25.12	12.7	30.58	25.19
FoM* (dB)	47.31	50.39	35.12	32.7	68.58	55.19

CHAPTER 6

Low-Power 24-GHz Frequency Synthesizer

With the fast-growing market for personal wireless communications, various standards and services have been deployed in the unlicensed frequency bands at 2.4 and 5.2 GHz over the past decade. In order to satisfy the increasing demands for high speed communications and to avoid the severe interference due to overcrowded radio transmission, the Federal Communications Commission (FCC) has allocated the 24-GHz frequency band for unlicensed ISM applications, which can be used for automotive short range radar.

Conventionally, high-frequency ICs were realized by compound semiconductor devices such as GaAs-based HEMTs and HBTs due to the advantages in the carrier mobility [103] [104] [105]. In order to decrease cost and to integrate with digital circuit, some 24-GHz RF systems have been realized using a standard CMOS technology [106] [107] [108]. Due to the limitation of battery capacity, low power is the trend for mobile wireless communication systems. In order to satisfy the system requirement, it is very important to reduce the power consumption.

6.1 Overview of the Direct-Conversion Receiver

For a wireless receiver, the complexity and performance of the overall system are strongly influenced by the architecture of the RF front-end. Typically, the direct-conversion technique is preferred in a fully-integrated design due to its simplicity. Thus, the front-end of a low-power receiver can be

realized with low cost.

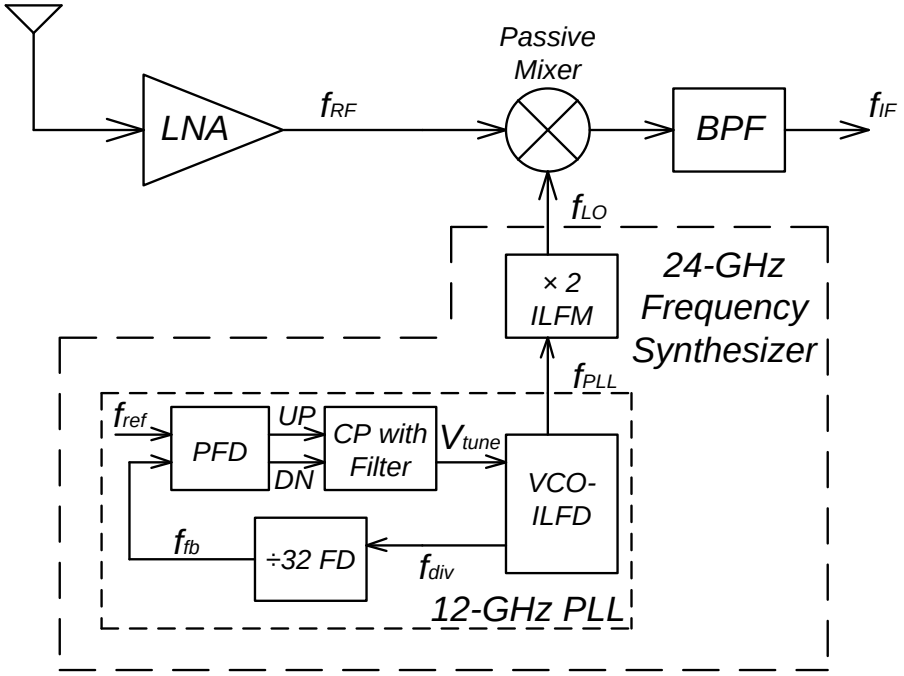

Figure 6.1: The front-end of the direct-conversion receiver

In Figure 6.1, it is shown that the direct-conversion receiver consists of a low-noise amplifier (LNA), a passive mixer with a band-pass filter (BPF) and a 24-GHz frequency synthesizer as an LO signal generator. In this design, the low-power frequency synthesizer consists of a ×2 ILFM and a 12-GHz PLL.

The 24-GHz frequency synthesizer is designed for the automotive radar system, so the specifications of the 24-GHz frequency synthesizer are shown in Table 6.1, which are based on the rules released by FCC [109].

Table 6.1: Design specifications of the 24-GHz frequency synthesizer

Specification of the 24-GHz frequency synthesizer	
Center frequency	24.075~24.675 GHz
Tuning range	2 GHz
Phase noise	-95 dBc/Hz
Power consumption	40 mW

6.1.1 The proposed ×2 ILFM

The ×2 ILFM is an active circuit operating at 24 GHz that is the highest frequency in the proposed frequency synthesizer. Generally, it is difficult to design the active circuit with low power consumption and high-frequency operation. The topology of the ×2 ILFM has been proposed and analyzed in Chapter 5.

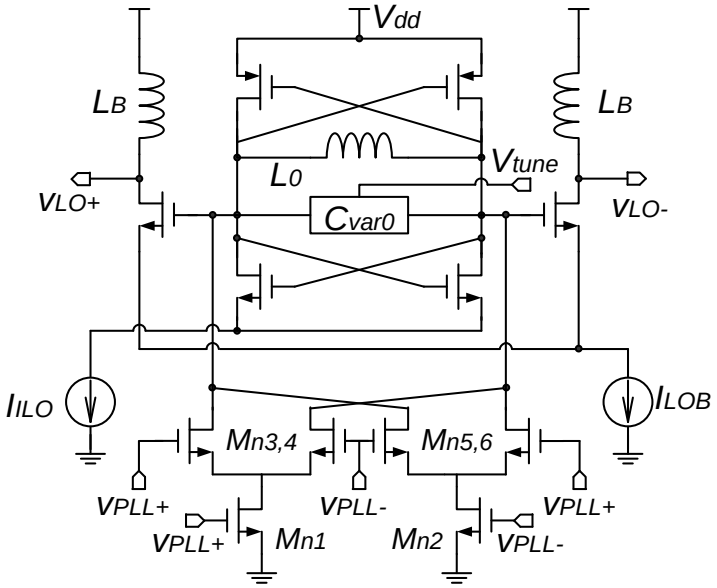

Figure 6.2: Schematic of the ×2 ILFM with an output buffer

Based on the topology, the schematic of the ×2 ILFM with an output buffer is designed and shown in Figure 6.2. With the ILFM's inputs from the 12-GHz PLL, v_{PLL+} and v_{PLL-}, a double-balanced Gilbert cell is designed as the ILFM's frequency pre-generator, which consists of six NMOS transistors. The gates of M_{n1}, M_{n3}, and M_{n6} are connected to v_{PLL+} while the gates of M_{n2}, M_{n4}, and M_{n5} are connected to v_{PLL-}. The ILFM's ILO consumes a DC current I_{ILO} to keep its self-oscillation, which is based on complementary cross-coupled structure with an inductor L_0. A varactor C_{var0} in the ILO is tuned by a DC voltage V_{tune} to

change the capacitance of the ILFM's LC tank and to further extend the ILFM's operation range.

A differential output buffer is used at the output stage of the ILFM, which consumes a DC current I_{LOB}. A pair of identical inductors L_B are used as its inductive loads of the buffer. The ILFM's buffer outputs, v_{LO+} and v_{LO-}, are connected to the passive mixer as the LO signal.

6.1.2 The proposed 12-GHz PLL

The 12-GHz PLL consists of a VCO, an ILFD, a divide-by-32 FD, a PFD and a CP with a loop filter. Both the VCO and the first-stage ILFD operate at the highest frequency and dominate the total power consumption in the 12-GHz PLL. In this proposed PLL, the VCO is stacked on top of the ILFD in order to reduce the power consumption. This topology has been introduced in Chapter 4. Thus, the block of VCO-ILFD is designed as the combination of the VCO and the ILFD.

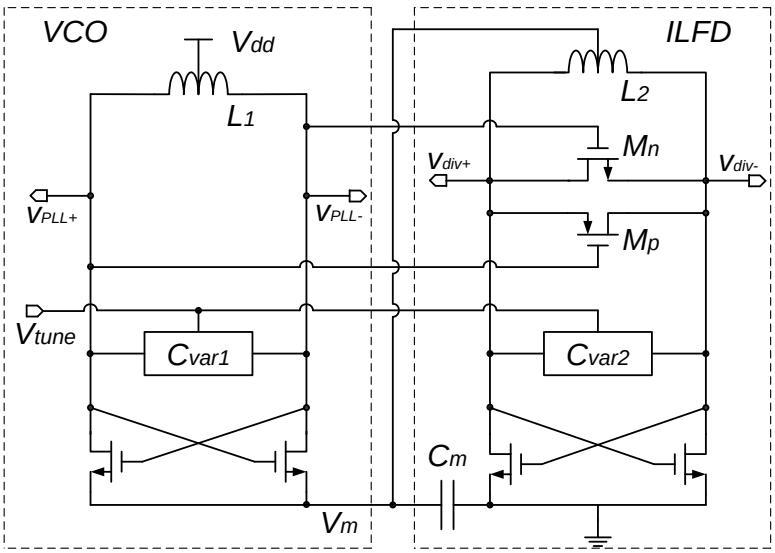

Figure 6.3: Schematic of the VCO-ILFD

The schematic of the VCO-ILFD is shown in Figure 6.3. At the VCO's differential outputs, v_{PLL+} and v_{PLL-}, the output frequency f_{PLL} is around 12 GHz. A varactor C_{var1} is connected between v_{PLL+} and v_{PLL-}, which is tuned by V_{tune}. v_{PLL+} and v_{PLL-} are connected to the gates of two injection transistors M_p and M_n, respectively, where both M_p and M_n are connected in parallel between the ILFD's differential outputs, v_{div+} and v_{div-}. The output frequency f_{div} is around 6 GHz, connected to the following divide-by-32 FDs. Another varactor C_{var2} between v_{div+} and v_{div-} is also tuned by V_{tune} for wider operation range.

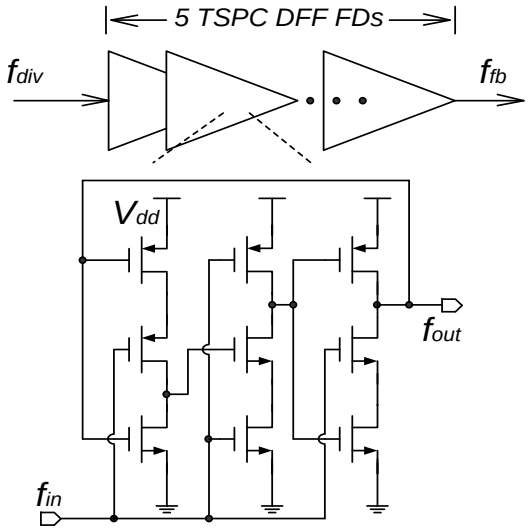

Figure 6.4: Schematic of the TSPC DFF FD

In the feedback path of the 12-GHz PLL, the ILFD is followed by a low-power divide-by-32 FD. In Figure 6.4, it is shown that the divide-by-32 FD consists of 5 TSPC DFF FDs in series, where each DFF FD is a divide-by-2 FD. The input frequency of the divide-by-32 FD is f_{div} from the VCO-ILFD while its output frequency f_{fb} is used to compare with the reference frequency f_{ref} in the PFD. In each DFF FD, the TSPC dynamic circuit is used in designing synchronous circuits, which has advantages of low complexity, high operation

speed, and low power dissipation [110].

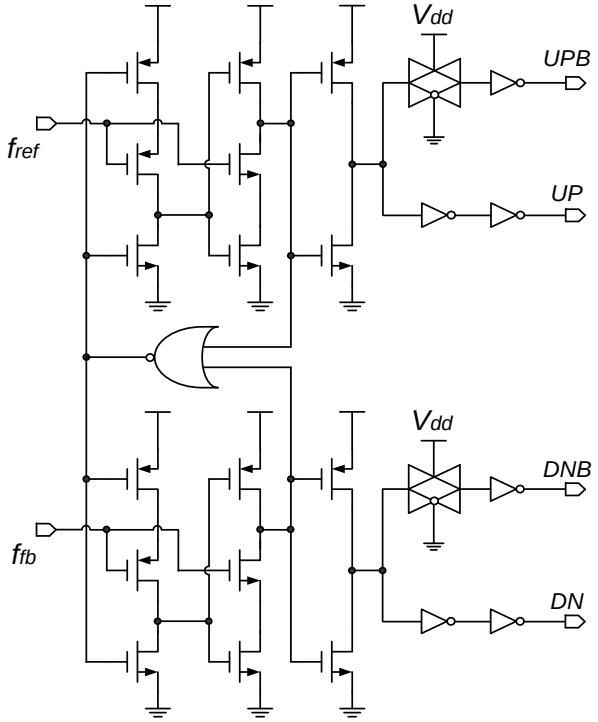

Figure 6.5: Schematic of the PFD

In the 12-GHz PLL, both the PFD and the CP operate at low frequency and consume low power. The schematic of the PFD is shown in Figure 6.5, which is implemented based on the TSPC dynamic circuit for low-frequency and low-power operation [111]. The PFD's two input frequencies f_{ref} and f_{fb} are from the signal generator and the feedback path, respectively. A NOR gate with delay is used in order to reduce the dead-zone problem. At the PFD's outputs, *UP* (*UPB*) and *DN* (*DNB*), inverters are used for complementary outputs generation, where *UPB* and *DNB* are opposite to *UP* and *DN*, respectively. The complementary pass-transistor gates are used to compensate the delay due to these inverters. Therefore, the PFD's outputs are designed to be matched so that the skew between the complementary outputs can be reduced considerably.

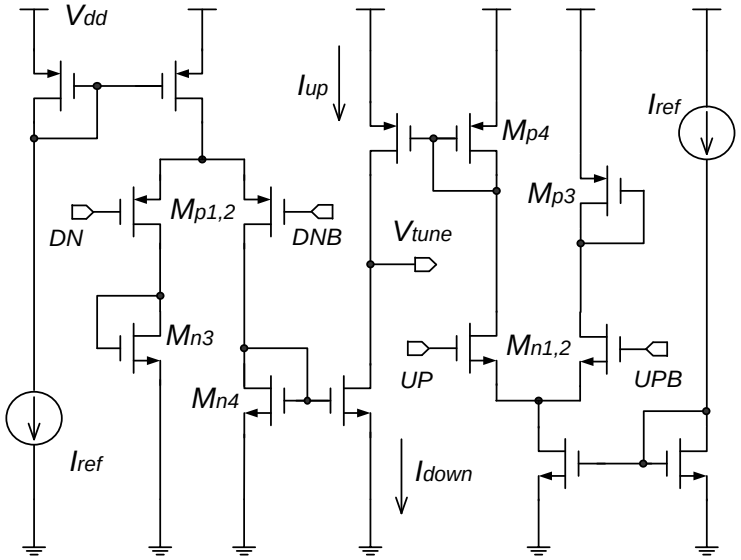

Figure 6.6: Schematic of the double-balanced CP

The schematic of the double-balanced CP is shown in Figure 6.6. The CP's inputs are *UP* (*UPB*) and *DN* (*DNB*) from the PFD while CP's output is V_{tune}. The *UP* and *UPB* signals are connected to a pair of NMOS transistors M_{n1} and M_{n2} while the *DN* and *DNB* signals are connected to a pair of PMOS transistors M_{p1} and M_{p2}. The currents generated by these four transistors can be steered either into a dummy load, M_{n3} or M_{p3}, or into a current-controlled transistor, M_{n4} or M_{p4}. The purpose of this configuration is to make the signal path from the input to the output as equal as possible. Hence, the CP's charging and discharging are balanced to reduce reference spur.

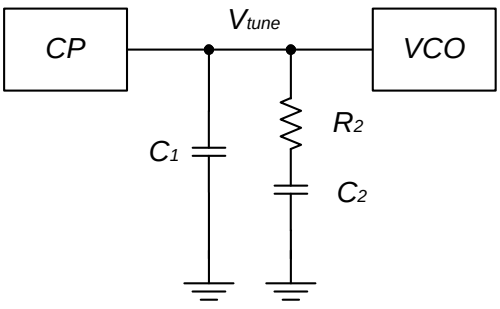

Figure 6.7: Schematic of the loop filter

In Chapter 2, the loop filter has been reviewed, which has important influence on the PLL's performance. In this 12-GHz PLL, a second-order passive loop filter is used, including a resistor R_2 and two capacitors C_1 and C_2, as shown in Figure 6.7.

The loop bandwidth is the most critical parameter of the PLL, which depends on the loop filter. Generally, a narrower loop bandwidth results in a cleaner output signal. However, a wider bandwidth is required to settle and re-obtain lock faster [112]. In this design, the loop bandwidth is set to be a tenth of the reference frequency to achieve short settling time, where the PLL can be settled fast from its initial free-running condition to its locked condition.

The phase margin relates to the stability of a system [113]. The settling time decreases with increasing phase margin, reaching a minimum for phase margin values of around 50 °. Increasing the phase margin further leads to a sharp increase in the settling time [114]. Finally, the phase margin of 50 ° is a good compromise between desired stability and settling time in this design.

In [17], the design equations are derived for the calculation of these loop filter components. The time constants of the first and second poles are given by

$$\tau_1 = \frac{\sec\varphi - \tan\varphi}{\omega_{BW}} \tag{6.1}$$

$$\tau_2 = \frac{1}{\omega_{BW}^2 \cdot \tau_1} \tag{6.2}$$

where $\omega_{BW} = 2\pi \cdot f_{BW}$.

Thus, C_1, C_2, and R_2 can be obtained in sequence.

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_\varphi \cdot K_{VCO}}{N \cdot {\omega_{BW}}^2} \cdot \sqrt{\frac{1+\tau_2^2\omega_{BW}^2}{1+\tau_1^2\omega_{BW}^2}} \tag{6.3}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right) \tag{6.4}$$

$$R_2 = \frac{\tau_2}{C_2} \tag{6.5}$$

In this design, C_1=3.6 pF, C_2=24 pF, and R_2=1 kΩ are chosen based on the design specifications of the 12-GHz PLL in Table 6.2.

Table 6.2: Design specifications of the 12-GHz PLL

Parameter	Value (Unit)
Phase margin (φ)	50 (°)
Loop bandwidth (f_{BW})	18.75 (MHz)
Phase error gain (K_φ)	10 (mA)
VCO gain (K_{vco})	1000 (MHz/V)
Reference frequency (f_{ref})	187.5 (MHz)
Division ratio (N)	64

6.2 Phase Noise Analysis of the Frequency Synthesizer

In previous chapters, it has been demonstrated that the injection-locking technique is an excellent solution for high-frequency and low-power circuits. In the 24-GHz frequency synthesizer, the phase noise of the output signal can also be improved by injection-locking. Thus, the frequency synthesizer can have low phase noise even if the design achieves short settling time through the wide loop bandwidth.

6.2.1 Phase noise from the 12-GHz PLL

The transfer functions of the forward and feedback paths are expressed as

$$H(s)|_{FW} = \frac{K_\phi K_{VCO} Z(s)}{s} \tag{6.6}$$

$$H(s)|_{FB} = \frac{1}{N} \tag{6.7}$$

where the impedance of the second-order passive loop filter in the 12-GHz PLL is

$$Z(s) = \left(R_1 + \frac{1}{C_1 s}\right) \parallel \frac{1}{C_2 s} = \frac{R_1 C_1 s + 1}{R_1 C_1 C_2 s^2 + (C_1 + C_2)s} \tag{6.8}$$

Hence, both the open-loop and closed-loop gains of the PLL are given by

$$G_{OL}(s) = H(s)|_{FW} \cdot H(s)|_{FB} = \frac{K_\phi K_{VCO}(R_1 C_1 s + 1)}{N R_1 C_1 C_2 s^3 + N(C_1 + C_2)s^2} \tag{6.9}$$

$$G_{CL}(s) = \frac{H(s)|_{FW} \cdot H(s)|_{FB}}{1 + H(s)|_{FW} \cdot H(s)|_{FB}} = \frac{K_\phi K_{VCO}(R_1 C_1 s + 1)}{N R_1 C_1 C_2 s^3 + N(C_1 + C_2)s^2 + K_\phi K_{VCO} R_1 C_1 s + K_\phi K_{VCO}} \tag{6.10}$$

For the analysis on phase noise, the power spectrum densities (PSDs) of the reference source, the combination of PFD and CP, the FD, the VCO and the loop filter are represented by $S_{ref}(f_m)$, $S_\phi(f_m)$, $S_{FD}(f_m)$, $S_{VCO}(f_m)$ and $S_{R1}(f_m)$, respectively, where f_m is the offset frequency from the carrier frequency. Based on the phase noise model for noise source elements in [21], the phase noise PSD of the 12-GHz PLL is expressed as

$$S_{PLL}(f_m) = \left(S_{ref}(f_m) + \frac{S_\phi(f_m)}{K_\phi^2} + S_{FD}(f_m)\right)|N \cdot G_{CL}(f_m)|^2 + S_{VCO}(f_m)\left|\frac{1}{1 + G_{OL}(f_m)}\right|^2 + S_{R1}(f_m) \tag{6.11}$$

Hence, it is concluded that the phase noise of the 12-GHz PLL is contributed by these noise sources and shaped by the loop gain of the PLL. In Figure 6.8, the phase noise is shown based on (6.11), where f_{BW} can be obtained from the loop gain of the PLL [17].

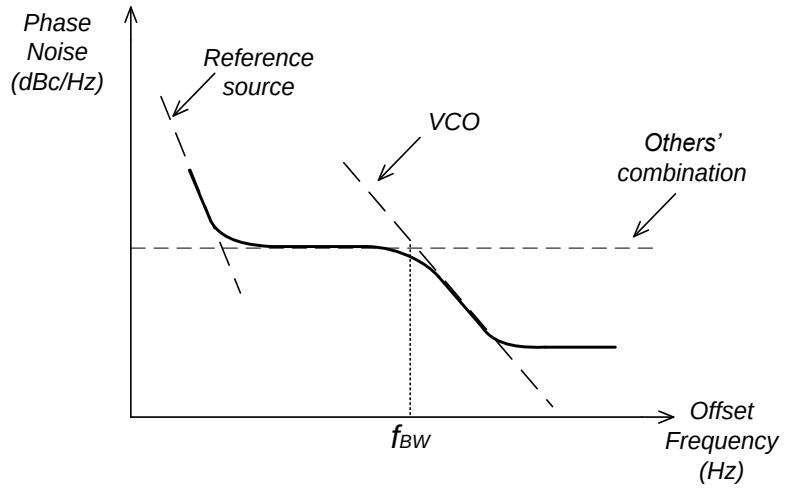

Figure 6.8: Phase noise of the 12-GHz PLL

6.2.2 Phase noise from the ×2 ILFM

In Chapter 5, the maximum deviation of the injection frequency from the resonant frequency is given by

$$f_0 - f_{inj} = \frac{f_0}{2Q} \cdot \frac{I_{INJ}}{\sqrt{I_{ILO}^2 - I_{INJ}^2}} \tag{6.12}$$

Based on the noise behavior of ILO in [91], the corner frequency of the ILFM is defined as

$$f_c = \frac{f_{ILFM}}{4Q} \cdot \frac{I_{INJ}}{\sqrt{I_{ILO}^2 - I_{INJ}^2}} \tag{6.13}$$

where f_{ILFM} is the resonant frequency of the ×2 ILFM in the proposed circuit.

The LO signal is generated by the ILFM with the injection signal from the 12-GHz PLL, so its phase noise PSD can be given in [91]

$$S_{LO}(f_m) = \frac{4f_c^2}{f_c^2 + f_m^2} S_{PLL}(f_m) + \frac{f_m^2}{f_c^2 + f_m^2} S_{ILFM}(f_m) \tag{6.14}$$

where $S_{ILFM}(f_m)$ is the free-running ILFM's phase noise PSD.

Substituting (6.11) into (6.14), it can be obtained that

$$S_{LO}(f_m) = \frac{4f_c^2}{f_c^2+f_m^2} \cdot \left[\left(S_{ref}(f_m) + \frac{S_\phi(f_m)}{K_\phi^2} + S_{FD}(f_m) \right) |N \cdot G_{CL}(f_m)|^2 + S_{VCO}(f_m) \left| \frac{1}{1+G_{OL}(f_m)} \right|^2 + S_{R1}(f_m) \right] + \frac{f_m^2}{f_c^2+f_m^2} \cdot S_{ILFM}(f_m)$$

(6.15)

Therefore, it is observed that the phase noise of the 24-GHz frequency synthesizer is shaped based on both f_{BW} and f_c. When f_c is lower than f_{BW}, the phase noise of the 24-GHz frequency synthesizer is shown in Figure 6.9 (a). After the frequency pre-generator in the ILFM, the carrier frequency is multiplied by 2. Thus, the phase noise after the frequency pre-generator is pushed up by 20log(2) dB ≈ 6 dB due to the frequency multiplication. At offset frequency lower than f_c, the phase noise of the 24-GHz frequency synthesizer is dominated by the phase noise after the frequency pre-generator. At offset frequency higher than f_c, the phase noise of the 24-GHz frequency synthesizer is dominated by the phase noise of the free-running ILFM. Thus, the phase noise of the frequency synthesizer can be improved at high offset frequency if the phase noise of the free-running ILFM is lower than the phase noise after the frequency pre-generator. In this case, it is more important to design the free-running ILFM with low phase noise than to reduce the out-band phase noise of the 12-GHz PLL.

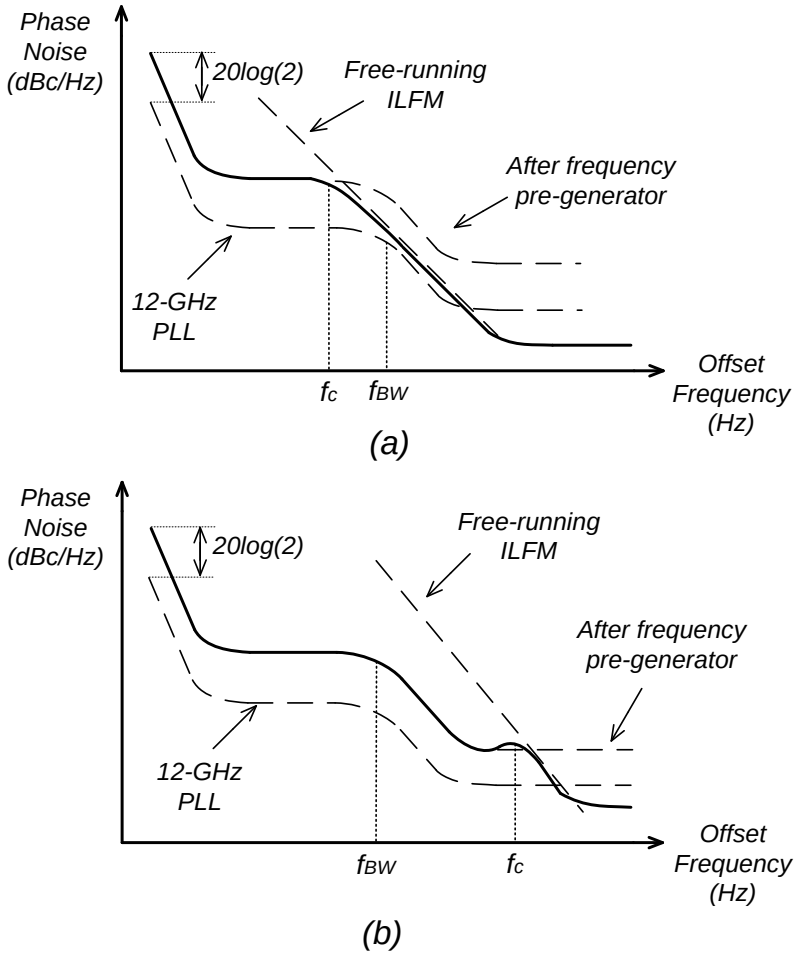

Figure 6.9: Phase noise of the 24-GHz frequency synthesizer (a) $f_c<f_{BW}$ and (b) $f_c>f_{BW}$

When f_c is higher than f_{BW}, the phase noise of the 24-GHz frequency synthesizer is shown in Figure 6.9 (b). Similar to Figure 6.9 (a), the phase noise of the 24-GHz frequency synthesizer is also dominated at low and high offset frequency by the phase noise after the frequency pre-generator and the phase noise of the free-running ILFM, respectively. However, due to large f_c, the phase noise of the free-running ILFM has less effect on the output of the frequency synthesizer. Thus, in this case, it is more important to design the 12-GHz PLL with low noise.

6.3 Simulated and Experimental Results of the Proposed Circuit

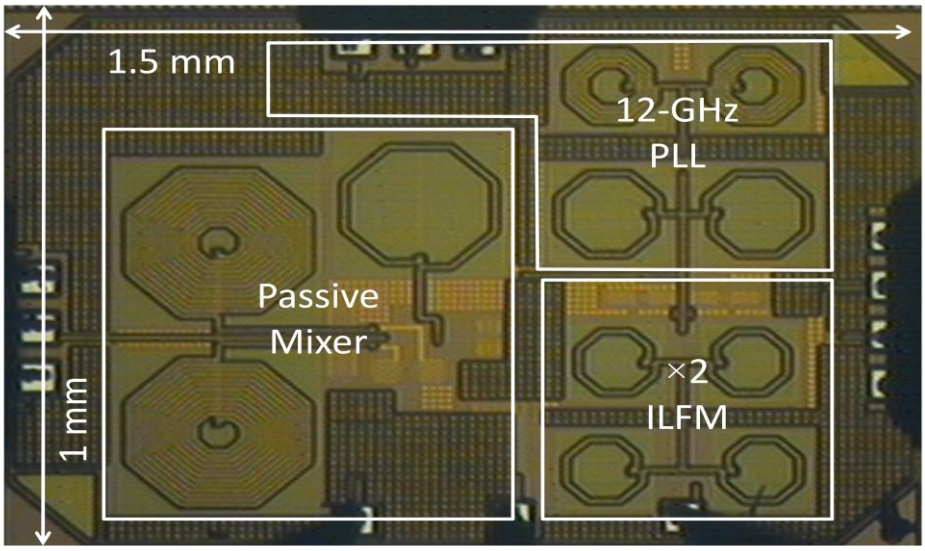

Figure 6.10: Die micrograph of the proposed circuit

The proposed circuit has been designed with the passive mixer at the next stage and fabricated in the 0.13 μm CMOS IBM technology. For measurement, the RF signal and reference signal are from two signal generators instead of from the LNA and a crystal oscillator, respectively. The die microphotograph is shown in Figure 6.10. The total size of the die is 1.5 mm × 1 mm, including all pads. With the supply voltage of 1.3 V, the power consumption is 11.86 mW for the core circuit.

In the proposed frequency synthesizer, the output of the 12-GHz PLL is connected to the ×2 ILFM, so it is important that f_{PLL} is always in the ILFM's input-frequency range, i.e. the ILFM can be injection-locked by the signal from the PLL. In this circuit, no output pad is added between the VCO and the ILFM because it is very sensitive to additional parasitic component. Therefore, the

ILFM's operation range and the VCO's tuning range cannot be measured separately.

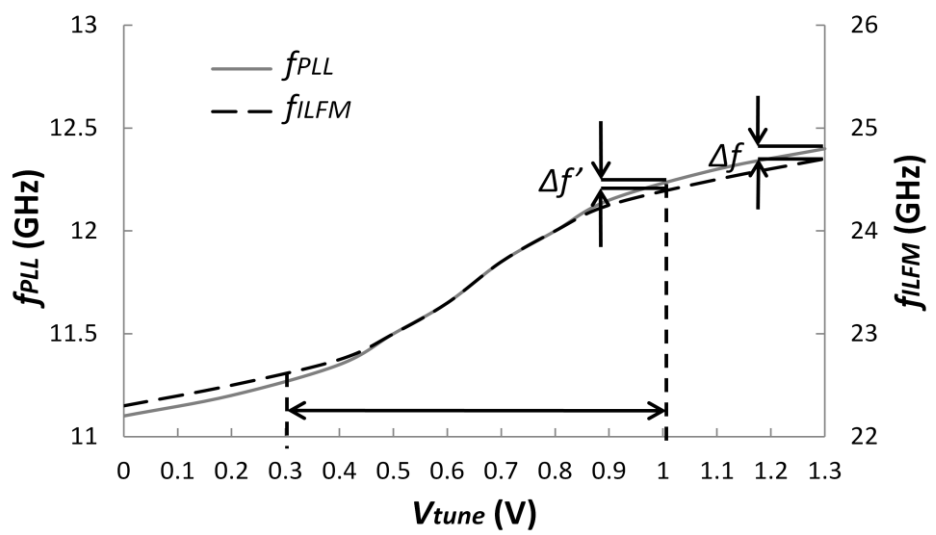

Figure 6.11: Simulated tuning characteristic of the 12-GHz PLL and the ×2 ILFM

In Figure 6.11, the tuning characteristics of the 12-GHz PLL and the ×2 ILFM are shown through the post-layout simulation. With V_{tune} varying from 0 to 1.3 V, f_{PLL} is tuned from 11.1 GHz to 12.4 GHz while f_{ILFM} is also tuned from 22.4 GHz to 24.6 GHz. Based on the definition of f_c, the minimum value of f_c is the maximum frequency difference Δf between $2f_{PLL}$ and f_{ILFM} for V_{tune} from 0 V to 1.8 V. In this frequency synthesizer, f_c is larger than 100 MHz if the ILFM is designed to be injection-locked for the whole tuning range. In addition, smaller f_c can be used to improve the phase noise if Δf is smaller. If V_{tune} is to be biased between 0.3 V and 1 V, f_c can be designed to be as small as $\Delta f'$ (50 MHz) that is smaller than Δf in Figure 6.11.

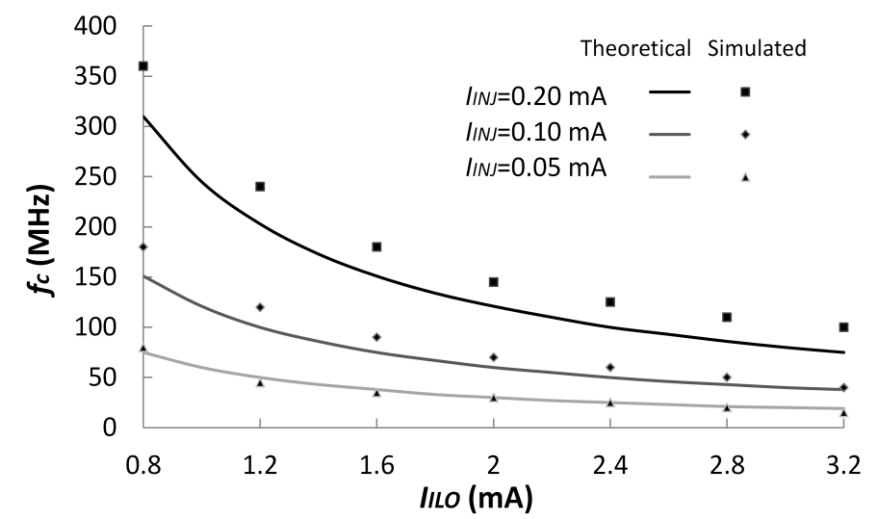

Figure 6.12: Theoretical and simulated results of f_c versus I_{ILO}

In this proposed circuit, f_c can be increased with decreasing I_{ILO} or increasing I_{INJ}. Through the theoretical calculations based on (6.13) and post-layout simulations, f_c versus I_{ILO} and I_{INJ} are shown in both Figure 6.12 and Figure 6.13, respectively. As an example in Figure 6.12 for I_{INJ}=0.05 mA, f_c can be increased from 15 MHz to 80 MHz through decreasing I_{ILO} from 3.2 mA to 0.8 mA. Another example is given in Figure 6.13 for I_{ILO}=2.3 mA that f_c can be increased from 0 MHz to 370 MHz through increasing I_{INJ} from 0 mA to 0.6 mA. When I_{INJ} is increased in the post-layout simulation, the impedance of the injection transistors across the ILFM's LC tank will be lower and, consequently, the quality factor of the LC tank will be decreased. As a result, with larger I_{INJ}, the simulated value of f_c becomes larger than the theoretical value based on (6.13) in both Figure 6.12 and Figure 6.13.

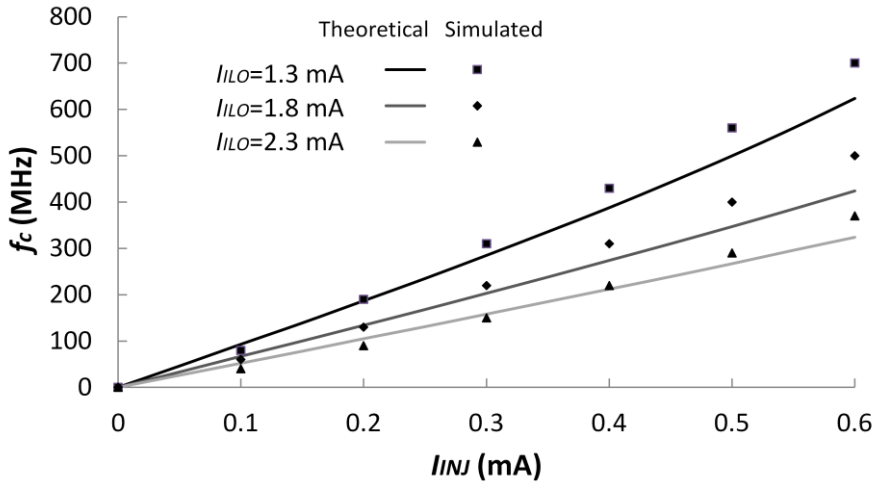

Figure 6.13: Theoretical and simulated results of f_c versus I_{INJ}

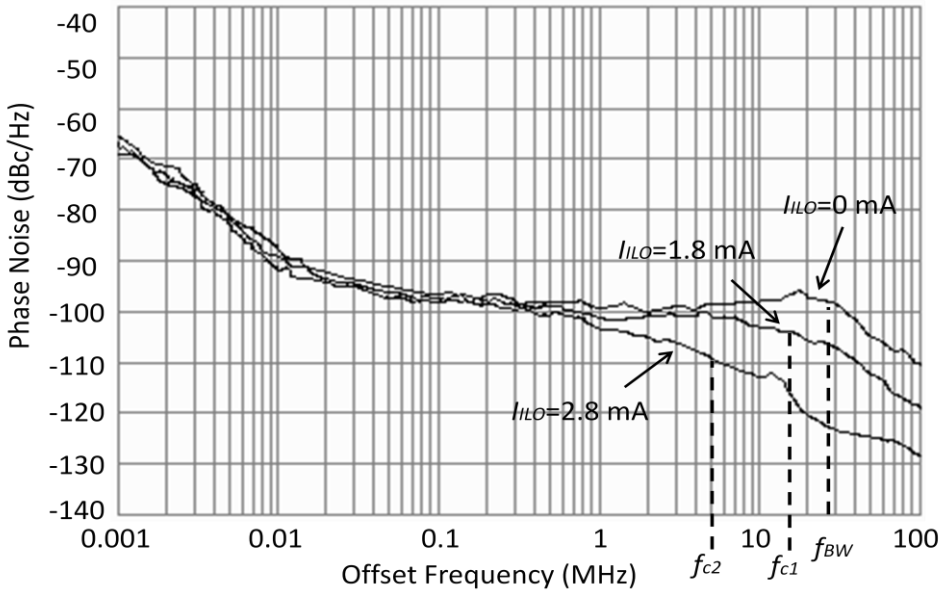

Figure 6.14: Measured phase noises with varying I_{ILO}

Based on (6.15), the phase noise of the frequency synthesizer can be changed with f_c. In order to observe the effect of f_c on the phase noise, f_c is changed through varying I_{ILO} and I_{INJ}. The measured phase noise of the frequency synthesizer with I_{INJ}=0.05 mA and I_{ILO} of 0, 1.8 and 2.8 mA are shown in Figure 6.14. At I_{ILO}=0 mA, the ILFM performs as an active mixer with an LC-

tank. Thus, the phase noise of the frequency synthesizer will not be improved by the ILFM. When I_{ILO} is increased to 1.8 mA, f_c is equal to f_{c1}. In this figure, it is shown that the phase noise of the frequency synthesizer can be improved at high offset frequency. At I_{ILO}=2.8 mA, f_c is reduced to f_{c2} that is much smaller than f_{BW}. Thus, the phase noise of the frequency synthesizer is dominated by the phase noise of the free-running ILFM.

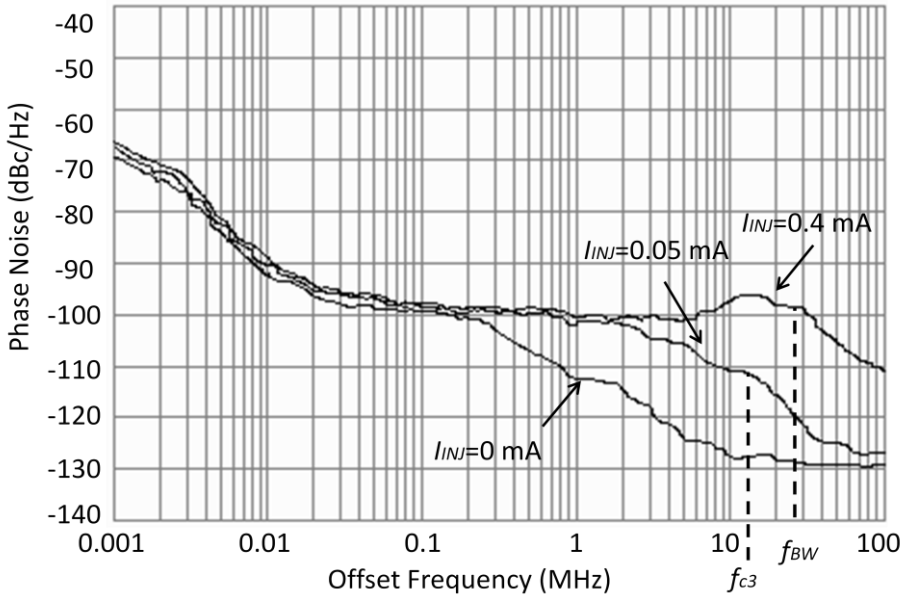

Figure 6.15: Measured phase noises with varying I_{INJ}

The measured phase noises of the frequency synthesizer with I_{ILO}=2.3 mA and I_{INJ} of 0, 0.05 and 0.4 mA are shown in Figure 6.15. At I_{INJ}=0 mA, the ILFM performs as just a VCO without injection. Although there is some leakage from the PLL, the current generated by the leakage is very small. In Chapter 5, it is demonstrated that the ILFM's operation range is very narrow with small injection current. Thus, the ILFM cannot be injection-locked by the leakage current. As a result, the phase noise of the frequency synthesizer depends completely on the free-running ILFM. When I_{INJ} is increased to 0.05

mA, f_c is equal to f_{c3}. At low offset frequency, the phase noise of the frequency synthesizer depends on the PLL's phase noise. At I_{INJ}=0.4 mA, f_c is much higher than f_{BW}. Consequently, the phase noise of the frequency synthesizer is dominated by the PLL's phase noise. Finally, it can be concluded that the phase noise of the frequency synthesizer is improved by the ILFM as the offset frequency is above f_c.

6.4 Summary

Table 6.3: The performance comparison of the 24-GHz frequency synthesizers

	[115]	[2]	[3]	[116]	This work
Technology	0.18 μm BiCMOS	0.13 μm CMOS	SiGe 0.13 μm BiCMOS	0.13 μm CMOS	0.13 μm CMOS
V_{dd} (V)	2.5	1.5	2.5	1.5	1.3
f_{out} (GHz)	24	24	24.12	22.4	24.32
f_{BW} (MHz)	-	0.2	0.2	0.4	20
Phase noise (dBc/Hz) @1MHz	-93	-101	-104.3	-95.7	-104
Tuning range (GHz)	0.4	2.6	4.7	2.2	2.6
DC power (mW)	21	29.6	70	36	11.86

In this chapter, the proposed 24-GHz frequency synthesizer is presented, which has been designed with a passive mixer and fabricated in the 0.13 μm CMOS IBM technology. The phase noise of the frequency synthesizer is analyzed in detail. Furthermore, the phase noise varying with the corner

frequency is discussed. Table 6.3 summarizes the measured performances of the proposed frequency synthesizer.

Based on comparisons among different 24-GHz frequency synthesizers, the proposed frequency synthesizer has the lowest power consumption. This makes the proposed frequency synthesizer a suitable design for a low-power 24-GHz direct-conversion receiver.

CHAPTER 7

Conclusions and Future Works

7.1 Conclusions

This thesis describes a wide range of techniques employed in the frequency synthesizer for LO signal generation. The investigation covers mainly three high-frequency building blocks, which are the VCO, the FD and the FM.

In Chapter 2, the topology of a basic PLL is reviewed. Based on the topology, the linear model of the PLL is described mathematically. Then, the performance of a PLL is discussed, including reference spur, phase noise and lock time. Moreover, the most important building blocks in the PLL, such as VCO and FD, are investigated in detail. Finally, the conceptual model of an ILO is analyzed.

In Chapter 3, some conventional divide-by-2/3 FDs are studied. A divide-by-2/3 circuit is proposed based on the concept of ILFD. This circuit has a pair of switched capacitors in order to switch the division modes. With gain and phase conditions of the ILO, the ILFD's operation range is analyzed and then its design equations are derived mathematically. Thus, the mutual operation range in the two division modes can be optimized based on the design equations. The proposed circuit is fabricated in the 0.18 μm CMOS technology. With the supply voltage of 1.8 V, the power consumption is 3.15 mW. Its operation range in the divide-by-2 mode is 3.44~5.02 GHz while its operation range in the divide-by-3 mode is 4.28~4.81 GHz. Moreover, the FoM for the ILFD is 1.527 GHz/mW.

In Chapter 4, a dual-band VCO is designed with the VCO stacking on top of

the ILFD. The biased current in the VCO is reused in the ILFD, so the total power consumption can be reduced significantly. The proposed circuit is fabricated in the 0.18 μm CMOS technology. With the supply voltage of 1.8 V, the power consumption is 3.2 mW. The tuning range for upper and lower frequency bands are 4.48~5.86 GHz and 2.24~2.93 GHz, respectively. Moreover, the FoMs for the two frequency bands are -187.1 and -190.1 dB, respectively.

In Chapter 5, a ×2 ILFM is proposed and analyzed based on the novel topology. The equations of the conversion gain and operation range in the ILFM are derived mathematically against the magnitude of the injection current. The proposed circuit is fabricated in the 0.18 μm CMOS technology. With the supply voltage of 1.8 V, the power consumption is 6.66 mW. Furthermore, a topology of the $\times(n+1)/n$ ILFM is proposed for fractional frequency multiplication, where a ×(3/2) FFM is designed as an example. This FFM's operation range is optimized and verified through simulation. The proposed circuit is fabricated in the 0.18 μm CMOS technology. With the supply voltage of 1.8 V, the power consumption is 9.54 mW.

In Chapter 6, a 24-GHz frequency synthesizer is suitable for a low-power direct-conversion receiver design. Phase noise generation and contribution in the frequency synthesizer are analyzed in detail. The proposed circuit is fabricated in the 0.13 μm CMOS technology. With the supply voltage of 1.3 V, the power consumption is 11.86 mW. It is shown through theoretical analysis and measurement that the frequency synthesizer has very low power consumption and low phase noise.

7.2 Future Works

With the rapid proliferation of bandwidth intensive content such as uncompressed high-definition video, instantaneous music and image data transmissions, there is a need for supporting multi-gigabits per second data rate. The 60-GHz frequency band opens a new era of multi-Gbps short-range transmission because of the huge bandwidth it can provide in the 57–66 GHz unlicensed spectrum available worldwide [117], listed in Table 7.1 for different regions.

Table 7.1: Regional spectrum allocations

Region	Frequency band (GHz)
Europe	59-66
Canada/USA	57-64
Korea	57-64
Japan	59-66
Australia	59.4-62.9

With the very wide frequency band, some standards have been proposed to fulfil different requirements. For example, IEEE 802.15.3c was introduced to standardize mm-wave wireless personal area network [118]. Another example is IEEE 802.11ad, as an instalment of the successful 802.11 family, which maintained its affinity with 802.11 in many aspects for next generation of Wi-Fi [119].

Moreover, it is important to choose a proper IC technology with considerations to the implementation aspects and system requirements. For bandwidth-demanding mass market, the 60-GHz RF IC can be implemented in

advanced silicon technology, such as 65 nm CMOS or silicon on lattice engineered substrate (SOLES) that is suitable for the practical fabrication of silicon-on-insulator CMOS circuits and III-V compound semiconductor devices (e.g. GaN) on a common silicon substrate [120].

The 60-GHz ISM frequency band is very wide, so it can be divided into many bands and channels. For example, the IEEE 802.15.3c specifies 4 bands around 60 GHz and each of them has a bandwidth of 2.16 GHz. An integer-N frequency synthesizer can be used to support this application. Some considerations for the frequency synthesizer are

1. The frequency synthesizer should cover multiple bands across a wide frequency range.
2. It should dynamically support different channel bandwidths for variable data rates.
3. It should have low integrated phase noise over multiple bands.
4. It should enable fast settling between transmit and receive time slots and between different transmission frequencies.

Generally, the 60-GHz frequency synthesizer for LO generation requires fast settling, high spectral purity and wide bandwidth.

In this thesis, some techniques have been proposed for high-frequency operation, such as injection locking and frequency multiplication. The ideas in these proposed circuits can be used to achieve better performance.

Usually, a dual-modulus FD has limited operation frequency, so a fixed frequency divider is used between the VCO and the dual-modulus FD. Consequently, the frequency step of the integer-N PLL cannot be as small as the reference frequency. With the high-frequency dual-modulus FD proposed in

Chapter 3, the integer-N PLL can be designed with the smallest frequency step that is equal to the reference frequency.

Injection-locked frequency multiplication introduced in Chapter 6 can be used in the 60-GHz frequency synthesizer. The output frequency of VCO in the PLL can be reduced by using the proposed ILFM. Furthermore, the proposed ILFM can improve the phase noise of the frequency synthesizer. With suppression of phase noise at the ILFM, the PLL can be designed with wider loop bandwidth to achieve faster settling. Thus, the frequency synthesizer can have shorter settling time, lower phase noise and lower power consumption. However, for wideband applications, it is necessary to do more research to extend the limited operation ranges of the ILFD and ILFM, although they have low power consumption at high-frequency operation.

Author's Publications

Journal publications:

J1. **Y. N. Miao**, C. C. Boon, M. A. Do, K. S. Yeo and Y. X. Zhang, "High-Frequency Low-Power LC Divide-by-2/3 Injection-locked Frequency Divider," *Microwave and Optical Technology Letters*, v. 53, n 2, pp. 337-340, Feb. 2011.

J2. **Y. N. Miao**, C. C. Boon, M. A. Do, K. S. Yeo and Y. X. Zhang, "Low-power 2.4/5.15 GHz Dual-band Voltage-Controlled Oscillator," *Microwave and Optical Technology Letters*, v. 53, n 11, p 2495-7, Nov. 2011

J3. **Y. N. Miao**, C. C. Boon, M. A. Do and K. S. Yeo, "High-Gain Low-Power LC Injection-Locked Frequency Multiplier", IEEE Trans. MTT. (Under review)

J4. **Y. N. Miao**, C. C. Boon, M. A. Do, K. S. Yeo and W. M. Lim, "High-Frequency Low-Power Fractional Frequency Multiplier", IEEE MWCL. (Under review)

Conference proceedings:

C1. **Y. N. Miao**, C. C. Boon, M. A. Do, K. S. Yeo and Y. X. Zhang, "A Low-Power 24-GHz Frequency Synthesizer for Automotive Radar Application," IEEE The 3rd ICIME, May. 2011.

C2. C. C. Boon, K. S. Yeo, M. A. Do and **Y. N. Miao**, (Invited paper) "Low-Power LC-Tank-Reused Injection-Locked Frequency Multiplier," IEEE The 54th MWSCAS, p 4 pp, Aug. 2011.

C3. **Y. N. Miao**, C. C. Boon, K. S. Yeo, M. A. Do and Y. X. Zhang, "A Stacking Voltage-Controlled Oscillator and Injection-Locked Frequency Divider for Low-Power and 12-GHz Operation," IEEE ICECC2011, Sept. 2011.

C4. Y. X. Zhang, C. C. Boon, **Y. N. Miao**, K. S. Yeo and M. A. Do, "Novel Hybrid Type Automatic Amplitude Control Loop VCO," IEEE ICECC2011, Sept. 2011.

Bibliography

[1] H. Hashemi, G. Xiang, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver-LO phase-shifting approach," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 614-626, 2005.

[2] V. Issakov, M. Tiebout, K. Mertens, C. Yiqun, A. Thiede, W. Simburger, and L. Maurer, "A compact low-power 24 GHz transceiver for radar applications in 0.13 µm CMOS," in *Microwaves, Communications, Antennas and Electronics Systems, 2009. COMCAS 2009. IEEE International Conference on*, 2009, pp. 1-5.

[3] A. Scuderi, E. Ragonese, and G. Palmisano, "24-GHz ultra-wideband transmitter for vehicular short-range radar applications," *Circuits, Devices & Systems, IET,* vol. 3, pp. 313-321, 2009.

[4] T. H. Lee, H. Samavati, and H. R. Rategh, "5-GHz CMOS wireless LANs," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 50, pp. 268-280, 2002.

[5] Y. Koo, H. Huh, Y. Cho, J. Lee, J. Park, K. Lee, D.-K. Jeong, and W. Kim, "A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 536-542, 2002.

[6] W. S. T. Yan and H. C. Luong, "A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM wireless receivers," in *Solid-State Circuits Conference, 2000. ESSCIRC '00. Proceedings of the 26th European*, 2000, pp. 200-203.

[7] Y. Ding and K. K. O., "A 21-GHz 8-Modulus Prescaler and a 20-GHz Phase-Locked Loop Fabricated in 130-nm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 1240-1249, 2007.

[8] Y.-H. Peng and L.-H. Lu, "A Ku-Band Frequency Synthesizer in 0.18-µm CMOS Technology," *Microwave and Wireless Components Letters, IEEE,* vol. 17, pp. 256-258, 2007.

[9] A. W. L. Ng, G. C. T. Leung, K. Ka-Chun, L. L. K. Leung, and H. C. Luong, "A 1-V 24-GHz 17.5-mW phase-locked loop in a 0.18-µm CMOS process," *Solid-State Circuits, IEEE Journal of,* vol. 41, pp. 1236-1244, 2006.

[10] R. Adler, "A Study of Locking Phenomena in Oscillators," *Proceedings of the IRE,* vol. 34, pp. 351-357, 1946.

[11] B. Razavi, "A study of injection locking and pulling in oscillators," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 1415-1424, 2004.

[12] B. Ravazi, *RF Microelectronics*: Prentice Hall, 1997.

[13] J. Savoj and B. Ravazi, *High Speed CMOS Circuits for Optical Receivers*: Kluwer Publishers, 2001.

[14] B. Ravazi, *Design of Integrated Circuits for Optical Communication Systems*: McGraw-Hill, 2003.

[15] R. E. Best, *Phase-Locked Loops Design, Simulation and Applications (5th ed)*: McGraw-Hill, Inc, 2003.

[16] C. Quemada, G. Bistue, and I. Adin, *Design Metholology for RF CMOS Phase-Locked Loops*: Artech House, 2009.

[17] D. Banerjee, *PLL Performance, Simulation, and Design (2nd ed)*: National Semiconductor, 2001.

[18] A. Maxim, "Low-Voltage CMOS Charge-Pump PLL Architecture for Low jitter Operation," in *ESSCIRC*, 2002, pp. 423-426.

[19] B. D. Muer and M. Steyaert, *CMOS Fractional-N Synthesizers, Design for High Spectral Purity and Monolithic Integration*. Boston: Kluwer Academic Publishers, 2003.

[20] A. Mehrotra, "Noise analysis of phase-locked loops," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on,* vol. 49, pp. 1309-1316, 2002.

[21] Y. W. Kim and J. D. Yu, "Phase Noise Model of Single Loop Frequency Synthesizer," *Broadcasting, IEEE Transactions on,* vol. 54, pp. 112-119, 2008.

[22] A. Hajimiri, "Jitter and Phase Noise in Electrical Oscillators," Ph.D. Dissertation, Standford University, 1998.

[23] L. Lascari, "Accurate Phase Noise Prediction in PLL Frequency Synthesizers," *Applied Microwave and Wireless,* vol. 12, pp. 329-330, May 2000.

[24] B. Ravazi, "A Study of Phase Noise in CMOS Oscillators," *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 331-343, 1996.

[25] D. Park and S. Cho, "Design Techniques for a Low-Voltage VCO With Wide Tuning Range and Low Sensitivity to Environmental Variations," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 767-774, 2009.

[26] A. Zanchi, C. Samori, A. L. Lacaita, and S. Levantino, "Impact of AAC design on phase noise performance of VCOs," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 48, pp. 537-547, 2001.

[27] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 179-194, 1998.

[28] D. L. Chen and R. Waldron, "A single-chip 266 Mb/s CMOS transmitter/receiver for serial data communications," in *Solid-State Circuits Conference, 1993. Digest of Technical Papers. 40th ISSCC., 1993 IEEE International*, 1993, pp. 100-101, 269.

[29] M. Banu and A. Dunlop, "A 660 Mb/s CMOS clock recovery circuit with instantaneous locking for NRZ data and burst-mode transmission," in *Solid-State Circuits Conference, 1993. Digest of Technical Papers. 40th ISSCC., 1993 IEEE International*, 1993, pp. 102-103, 270.

[30] A. Pottbacker and U. Langmann, "A 8 GHz silicon bipolar clock-recovery and data-regenerator IC," in *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, 1994, pp. 116-117.

[31] B. Razavi and J. Sung, "A 6 GHz 60 mW BiCMOS phase-locked loop with 2 V supply," in *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, 1994, pp. 114-115.

[32] H. Q. Liu, W. L. Goh, L. Siek, W. M. Lim, and Y. P. Zhang, "A Low-Noise Multi-GHz CMOS Multiloop Ring Oscillator With Coarse and Fine Frequency Tuning," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 17, pp. 571-577, 2009.

[33] O. Nizhnik, R. K. Pokharel, H. Kanaya, and K. Yoshida, "Low Noise Wide Tuning Range Quadrature Ring Oscillator for Multi-Standard Transceiver," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 470-472, 2009.

[34] B. Leung, "A Switching-Based Phase Noise Model for CMOS Ring Oscillators Based on Multiple Thresholds Crossing," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 57, pp. 2858-2869, 2010.

[35] S.-T. Yan and H. C. Luong, "A 3 V 1.3-to-1.8 GHz CMOS voltage-controlled oscillator with 0.3 ps-jitter," in *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, 1997, pp. 29-32 vol.1.

[36] Z.-M. Lin and C. H. Huang, "A current-source driven CMOS voltage-controlled oscillator," in *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on*, 1999, pp. 1337-1339 vol.3.

[37] R. Woogeun, "A low power, wide linear-range CMOS voltage-controlled oscillator," in *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on*, 1998, pp. 85-88 vol.2.

[38] B. Razavi, *Design of Analog Integrated Circuits*: McGraw-Hill, 2000.

[39] C. Li and J. Lin, "A 1-9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application," *Microwave and Wireless Components Letters, IEEE,* vol. 20, pp. 34-36, 2010.

[40] P.-H. Hsieh, J. Maxey, and C. K. K. Yang, "Minimizing the Supply Sensitivity of a CMOS Ring Oscillator Through Jointly Biasing the Supply and Control Voltages," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 2488-2495, 2009.

[41] P. Ruippo, T. A. Lehtonen, and N. T. Tchamov, "An UMTS and GSM Low Phase Noise Inductively Tuned LC VCO," *Microwave and Wireless Components Letters, IEEE,* vol. 20, pp. 163-165, 2010.

[42] J. Kim, J. Shin, S. Kim, and H. Shin, "A Wide-Band CMOS LC VCO With Linearized Coarse Tuning Characteristics," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 55, pp. 399-403, 2008.

[43] E. S. A. Kytonaki and Y. Papananos, "A Low-Voltage Differentially Tuned Current-Adjusted 5.5-GHz Quadrature VCO in 65-nm CMOS Technology," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 58, pp. 254-258, 2011.

[44] J.-Y. Lee, H. Kim, S.-H. Lee, and H.-K. Yu, "A 48 GHz 196 dB-FOM LC VCO With Double Cap-Degeneration Negative-Resistance Cell," *Microwave and Wireless Components Letters, IEEE,* vol. 18, pp. 341-343, 2008.

[45] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*. Norwell, MA: Kluwer Academic Publisher, 2000.

[46] A. Buonomo and A. Lo Schiavo, "Finding the Tuning Curve of a CMOS LC VCO," *Circuits and Systems II: Express Briefs, IEEE Transactions on,* vol. 55, pp. 887-891, 2008.

[47] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *Solid-State Circuits, IEEE Journal of,* vol. 34, pp. 717-724, 1999.

[48] A. Tanabe, K. Hijioka, H. Nagase, and Y. Hayashi, "A Novel Variable Inductor Using a Bridge Circuit and Its Application to a 5-20 GHz Tunable LC-VCO," *Solid-State Circuits, IEEE Journal of,* vol. 46, pp. 883-893, 2011.

[49] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 36, pp. 1018-1024, 2001.

[50] S. K. Misra, R. K. Kolagotia, H. R. Srinivas, J. C. Mo, and M. S. Diamondstein, "VLSI implementation of a 300-MHz 0.35-µm CMOS 32-bit auto-reloadable binary synchronous counter with optimal test overhead delay," in *VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on*, 1998, pp. 326-329.

[51] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4-µm CMOS technology," *Solid-State Circuits, IEEE Journal of,* vol. 35, pp. 788-794, 2000.

[52] X. P. Yu, M. A. Do, L. Jia, J. G. Ma, and K. S. Yeo, "Design of a low power wide-band high resolution programmable frequency divider," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 13, pp. 1098-1103, 2005.

[53] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-µm CMOS technology," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 594-601, 2004.

[54] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *Solid-State Circuits, IEEE Journal of,* vol. 34, pp. 813-821, 1999.

[55] J. Navarro Soares, Jr. and W. A. M. Van Noije, "A 1.6-GHz dual modulus prescaler using the extended true-single-phase-clock CMOS circuit technique (E-TSPC)," *Solid-State Circuits, IEEE Journal of*, vol. 34, pp. 97-102, 1999.

[56] H. Knapp, H. D. Wohlmuth, M. Wurzer, and M. Rest, "25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12 µm CMOS," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, 2002, pp. 302-468 vol.1.

[57] M. Yuan, E. Skafidas, R. Evans, and I. Mareels, "A 40 GHz Power Efficient Static CML Frequency Divider in 0.13-µm CMOS Technology for High Speed Millimeter-Wave Wireless Systems," in *Circuits and Systems for Communications, 2008. ICCSC 2008. 4th IEEE International Conference on*, 2008, pp. 812-815.

[58] C. Cao and K. K. O, "A power efficient 26-GHz 32:1 static frequency divider in 130-nm bulk CMOS," *Microwave and Wireless Components Letters, IEEE,* vol. 15, pp. 721-723, 2005.

[59] U. Singh and M. M. Green, "High-frequency CML clock dividers in 0.13-µm CMOS operating up to 38 GHz," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1658-1661, 2005.

[60] K. Kurokawa, "Injection locking of microwave solid-state oscillators," *Proceedings of the IEEE*, vol. 61, pp. 1386-1410, 1973.

[61] L. J. Paciorek, "Injection locking of oscillators," *Proceedings of the IEEE,* vol. 53, pp. 1723-1727, 1965.

[62] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 1170-1174, 2004.

[63] X. Zhang, X. Zhou, B. Aliener, and A. S. Daryoush, "A study of subharmonic injection locking for local oscillators," *Microwave and Guided Wave Letters, IEEE,* vol. 2, pp. 97-99, 1992.

[64] F.-H. Huang and Y.-J. Chan, "A V-Band CMOS Injection-Locked Oscillator Using Fundamental Harmonic Injection," *Microwave and Wireless Components Letters, IEEE*, vol. 17, pp. 882-884, 2007.

[65] R. J. Betancourt-Zamora, S. Verma, and T. H. Lee, "1-GHz and 2.8-GHz CMOS injection-locked ring oscillator prescalers," in *VLSI Circuits, 2001. Digest of Technical Papers. 2001 Symposium on*, 2001, pp. 47-50.

[66] Y. H. Chuang, S. H. Lee, S. L. Jang, J. J. Chao, and M. H. Juang, "A Ring-Oscillator-Based Wide Locking Range Frequency Divider," *Microwave and Wireless Components Letters, IEEE,* vol. 16, pp. 470-472, 2006.

[67] K. Yamamoto and M. Fujishima, "A 44-μW 4.3-GHz injection-locked frequency divider with 2.3-GHz locking range," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 671-677, 2005.

[68] S. Cheng, H. Tong, J. Silva-Martinez, and A. I. Karsilayan, "A Fully Differential Low-Power Divide-by-8 Injection-Locked Frequency Divider Up to 18 GHz," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 583-591, 2007.

[69] J.-C. Chien and L.-H. Lu, "Analysis and Design of Wideband Injection-Locked Ring Oscillators With Multiple-Input Injection," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 1906-1915, 2007.

[70] X. Yi, C. C. Boon, M. A. Do, K. S. Yeo, and W. M. Lim, "Design of Ring-Oscillator-Based Injection-Locked Frequency Dividers With Single-Phase Inputs," *Microwave and Wireless Components Letters, IEEE,* vol. 21, pp. 559-561, 2011.

[71] A. Mirzaei, M. E. Heidari, R. Bagheri, and A. A. Abidi, "Multi-Phase Injection Widens Lock Range of Ring-Oscillator-Based Frequency Dividers," *Solid-State Circuits, IEEE Journal of,* vol. 43, pp. 656-671, 2008.

[72] L. Tang-Nian, B. Shuen-Yin, and Y. J. E. Chen, "A 60-GHz 0.13-μm CMOS Divide-by-Three Frequency Divider," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, pp. 2409-2415, 2008.

[73] S.-L. Jang, J.-C. Luo, C.-W. Chang, C.-F. Lee, and J.-F. Huang, "LC-Tank Colpitts Injection-Locked Frequency Divider With Even and Odd Modulo," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 113-115, 2009.

[74] H.-H. Hsieh, H.-S. Chen, and L.-H. Lu, "A V-Band Divide-by-4 Direct Injection-Locked Frequency Divider in 0.18-μm CMOS," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 59, pp. 393-405, 2011.

[75] E. Monaco, M. Borgarino, F. Svelto, and A. Mazzanti, "A 5.2mW ku-band CMOS injection-locked frequency doubler with differential input / output," in *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE*, 2009, pp. 61-64.

[76] L. Zhang, D. Karasiewicz, B. Cifctioglu, and H. Wu, "A 1.6-to-3.2/4.8 GHz dual-modulus injection-locked frequency multiplier in 0.18 μm digital CMOS," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, 2008, pp. 427-430.

[77] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 378-383, 2004.

[78] C.-Y. Yang, G.-K. Dehng, and S.-I. Liu, "High-speed divide-by-4/5 counter for a dual-modulus prescaler," *Electronics Letters*, vol. 33, pp. 1691-1692, 1997.

[79] J. Craninckx and M. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7-μm CMOS," in *Solid-State Circuits Conference, 1995. ESSCIRC '95. Twenty-first European*, 1995, pp. 254-257.

[80] H. R. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 780-787, 2000.

[81] W. S. T. Yan and H. C. Luong, "A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 204-216, 2001.

[82] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*: Kluwer academic publishers, 1998.

[83] B. Won, J. Shin, S. Jeon, and H. Shin, "A 9-GHz semi-dynamic frequency divide-by-2/3 in GaInP/GaAs HBT," in *Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings*, 2005, p. 4 pp.

[84] H. D. Wohlmuth and D. Kehrer, "A 15 GHz 256/257 dual-modulus prescaler in 120 nm CMOS," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 77-80.

[85] S.-L. Jang, C.-Y. Lin, and C.-F. Lee, "A Low Voltage 0.35 μm CMOS Frequency Divider With the Body Injection Technique," *Microwave and Wireless Components Letters, IEEE,* vol. 18, pp. 470-472, 2008.

[86] D. Grujic, M. Savic, and J. Popovic-Bozovic, "A Power Efficient Frequency Divider for 60 GHz Band," *Microwave and Wireless Components Letters, IEEE,* vol. 21, pp. 148-150, 2011.

[87] K.-H. Tsai, L.-C. Cho, J.-H. Wu, and S.-l. Liu, "3.5mW W-Band Frequency Divider with Wide Locking Range in 90nm CMOS Technology," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 466-628.

[88] D. Baek, J. Kim, and S. Hong, "A dual-band (13/22-GHz) VCO based on resonant mode switching," *Microwave and Wireless Components Letters, IEEE,* vol. 13, pp. 443-445, 2003.

[89] H. L. Kao, D. Y. Yang, Y. C. Chang, B. S. Lin, and C. H. Kao, "Switched resonators using adjustable inductors in 2.4/5 GHz dual-band LC VCO," *Electronics Letters,* vol. 44, pp. 299-300, 2008.

[90] Y. Li, Y.-O. Jing, Y.-H. Shen, and Z.-S. Lai, "A Stack-Mode Dual-Band Voltage-Controlled Oscillator for Multistandard Wireless Applications," in *Solid-State and Integrated Circuit Technology, 2006. ICSICT '06. 8th International Conference on*, 2006, pp. 1925-1927.

[91] S. Verma, H. R. Rategh, and T. H. Lee, "A unified model for injection-locked frequency dividers," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1015-1027, 2003.

[92] T.-N. Luo and Y. J. E. Chen, "A 0.8-mW 55-GHz Dual-Injection-Locked CMOS Frequency Divider," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 56, pp. 620-625, 2008.

[93] Z. Li and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 1296-1302, 2005.

[94] L. Jia, J. G. Ma, K. S. Yeo, X. P. Yu, M. A. Do, and W. M. Lim, "A 1.8-V 2.4/5.15-GHz dual-band LCVCO in 0.18-μm CMOS technology," *Microwave and Wireless Components Letters, IEEE,* vol. 16, pp. 194-196, 2006.

[95] S. L. Jang, Y. H. Chuang, S. H. Lee, L. R. Chi, and C. F. Lee, "An Integrated 5-2.5-GHz Direct-Injection Locked Quadrature LC VCO," *Microwave and Wireless Components Letters, IEEE,* vol. 17, pp. 142-144, 2007.

[96] L. L. K. Leung and H. C. Luong, "A 1-V 9.7-mW CMOS Frequency Synthesizer for IEEE 802.11a Transceivers," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 56, pp. 39-48, 2008.

[97] D. Y. Jung and C. S. Park, "A Low-Power, High-Suppression V-band Frequency Doubler in 0.13 μm CMOS," *Microwave and Wireless Components Letters, IEEE,* vol. 18, pp. 551-553, 2008.

[98] Y. Gao, K. Cai, Y. Zheng, and B.-L. Ooi, "A Wideband CMOS Multiplier for UWB Application," in *Ultra-Wideband, 2007. ICUWB 2007. IEEE International Conference on*, 2007, pp. 184-187.

[99] J.-H. Chen and H. Wang, "A High Gain, High Power K-Band Frequency Doubler in 0.18 μm CMOS Process," *Microwave and Wireless Components Letters, IEEE,* vol. 20, pp. 522-524, 2010.

[100] K.-Y. Lin, J.-Y. Huang, and S.-C. Shin, "A K-Band CMOS Distributed Doubler With Current-Reuse Technique," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 308-310, 2009.

[101] C.-N. Kuo, H.-S. Chen, and T.-C. Yan, "A K-Band CMOS Quadrature Frequency Tripler Using Sub-Harmonic Mixer," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 822-824, 2009.

[102] K. Yamamoto, "A 1.8-V operation 5-GHz-band CMOS frequency doubler using current-reuse circuit design technique," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 1288-1295, 2005.

[103] C. Meliani, M. Huber, G. Boeck, and W. Heinrich, "A GaAs HBT Low Power 24 GHz Downconverter with On-Chip Local-Oscillator," in *European Microwave Integrated Circuits Conference, 2006. The 1st*, 2006, pp. 141-144.

[104] B. Matinpour, N. Lal, J. Laskar, R. E. Leoni, and C. S. Whelan, "K-band receiver front-ends in a GaAs metamorphic HEMT process," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 49, pp. 2459-2463, 2001.

[105] Y. Mimino, M. Hirata, K. Nakamura, K. Sakamoto, Y. Aoki, and S. Kuroda, "High gain-density K-band p-HEMT LNA MMIC for LMDS and satellite communication," in *Microwave Symposium Digest., 2000 IEEE MTT-S International*, 2000, pp. 17-20 vol.1.

[106] C. Cao, Y. Ding, X. Yang, J.-J. Lin, A. K. Verma, L. Jenshan, F. Martin, and K. K. O, "A 24-GHz Transmitter with an On-Chip Antenna in 130-nm CMOS," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 148-149.

[107] A. Natarajan, A. Komijani, and A. Hajimiri, "A fully integrated 24-GHz phased-array transmitter in CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 2502-2514, 2005.

[108] G. Xiang and A. Hajimiri, "A 24-GHz CMOS front-end," *Solid-State Circuits, IEEE Journal of,* vol. 39, pp. 368-373, 2004.

[109] F. C. Commission, "Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems," vol. FCC 02-48, ed. Washington, D.C., 2002.

[110] M. V. Krishna, M. A. Do, K. S. Yeo, C. C. Boon, and W. M. Lim, "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 57, pp. 72-82, 2010.

[111] C.-Y. Wu, M.-C. Chen, and Y.-K. Lo, "A Phase-Locked Loop With Injection-Locked Frequency Multiplier in 0.18-µm CMOS for V-Band Applications," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 1629-1636, 2009.

[112] H. H. Chung, W. Chen, B. Bakkaloglu, H. J. Barnaby, B. Vermeire, and S. Kiaei, "Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers," *Nuclear Science, IEEE Transactions on,* vol. 53, pp. 3539-3543, 2006.

[113] W. Egan, *Phase-Lock Basics*: John Wiley & Sons, 2008.

[114] C. S. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time," *Solid-State Circuits, IEEE Journal of,* vol. 35, pp. 490-502, 2000.

[115] M. Notten, H. Veenstra, S. Blaakmeer, and R. van Langevelde, "A 24GHz multi-channel frequency synthesizer in a 0.18 µm BiCMOS technology for wireless sensor networks," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2011 IEEE 11th Topical Meeting on*, 2011, pp. 41-44.

[116] C. Cao, Y. Ding, X. Yang, J.-J. Lin, H.-T. Wu, A. K. Verma, L. Jenshan, F. Martin, and K. K. O, "A 24-GHz Transmitter With On-Chip Dipole Antenna in 0.13-µm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 1394-1402, 2008.

[117] H. Singh, J. Hsu, L. Verma, S. S. Lee, and N. Chiu, "Green operation of multi-band wireless LAN in 60 GHz and 2.4/5 GHz," in *Consumer Communications and Networking Conference (CCNC), 2011 IEEE*, 2011, pp. 787-792.

[118] C. W. Pyo and H. Harada, "Throughput analysis and improvement of hybrid multiple access in IEEE 802.15.3c mm-wave WPAN," *Selected Areas in Communications, IEEE Journal on*, vol. 27, pp. 1414-1424, 2009.

[119] E. Perahia, C. Cordeiro, P. Minyoung, and L. L. Yang, "IEEE 802.11ad: Defining the Next Generation Multi-Gbps Wi-Fi," in *Consumer Communications and Networking Conference (CCNC), 2010 7th IEEE*, 2010, pp. 1-5.

[120] C. L. Dohrman, K. Chilukuri, D. M. Isaacson, M. L. Lee, and E. A. Fitzgerald, "Fabrication of Silicon on Lattice-Engineered Substrate (SOLES) as a Platform for Monolithic Integration of CMOS and Optoelectronic Devices," in *SiGe Technology and Device Meeting, 2006. ISTDM 2006. Third International*, 2006, pp. 1-2.