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**TECHNOLOGICAL**  
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# **Ultra-low Power Energy Harvesting and Power Management Circuits For IoT Applications**

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# **Ultra-low Power Energy Harvesting and Power Management Circuits For IoT Applications**

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## Abstract

Recent progress in integrated circuits (IC) technology and design techniques, especially in ultra-low power circuits domain, has led a rapid growth of fully integrated and portable electronics within internet of things (IoT) smart nodes and wearable sensors system on chip (SoC). IoT applications including biomedical sensors, body area networks and wireless sensors, have taken advantage of such a progress. However, with the increase of people needs, numerous blocks must be integrated within the IoT SoC. Hence, a compact, efficient and self-sustained power management circuit (PMC) with a long life-time design becomes crucial for IoT SoC. Thus, energy scavengers, such as photovoltaic cells (PV), thermos-electric generators (TEG) and electro-static harvesters, become an attractive solution to power the PMC, for self-sustaining and prolonged life time systems.

Switched capacitor charge pump (SCCP) along with low drop out (LDO) regulators are an adequate solution for PMC within energy harvesting systems (EHS) for their integrability on-chip, avoiding bulky off-chip inductors, especially for implantable biomedical applications. However, these regulators must be controlled with a maximum power point tracking (MPPT) system to maximize the energy being harvested and to store it efficiently. It should be noted that the MPPT control the regulators whether to maximize the harvested power transfer as per load demand, or to condition the regulator to harvest the maximum available power from the energy harvester. For instance, many MPPT have been developed to track the maximum power point to maximize the tracking efficiency and/or the conversion efficiency.

Several requirements that should be met are wide input voltage handling, wide output load range coverage, output voltage regulation and ultra-low power consumption. The latter one is of a great concern to maximize the EHS overall efficiency and extend its lifetime in case of battery powered PMC.

In the first part of this thesis, I propose a novel ultra-low power MPPT technique with a wide tracking range. The proposed technique is an indirect, non-interrupting approach using a novel timing-based algorithm addressing the tracking efficiency. The proposed time-based MPPT technique is self-adaptive and applicable to several types of PVs and TEGs without external reconfiguration or change of passive components. It reduces the power consumption and design complexity. It consists of an ultra-low power digital processing unit to execute the proposed timing-based algorithm along with an ultra-low power window comparator to track the maximum open circuit voltage ( $V_{mpp}$ ) without the need to voltage references, perturbation steps and power-hungry voltage or current sensors. In addition, a variable gain is employed using a one-hot barrel shift register to reduce the transient response time in case of an abrupt input voltage change. A test chip was fabricated in 65-nm CMOS technology. The test chip can harvest energy with the input voltage range of 0.4 V to 1.7 V and the step response time of less than 100 ms at the minimum supply voltage of 0.8 V. The tracking efficiency is up to 96.2 % when supplied by a photovoltaic (PV) micro-cell array using an irradiation range of 200 lux to 1000 lux.

In the next part of this thesis, a three-dimensional MPPT (3-D MPPT) technique is proposed, addressing the conversion efficiency, for ultra-low power EHS within IoT smart nodes. The proposed MPPT improves the conversion efficiency over

a wide load range using a novel switch width modulation (SWM) technique. It enhances the conversion efficiency at ultra-light load condition by eliminating the trade-off between the gate driver and conduction loss. The proposed SWM technique modulates the SCCP transistors size in proportion to the load condition, input voltage and the swing voltage applied. The tested chip, fabricated in 65-nm CMOS technology, can harvest from 0.35 V and provides a regulated output voltage at 1 V with peak efficiency of 88% at 200  $\mu$ W and conversion efficiency  $> 60\%$  at 100 nW.

The last part of this thesis devoted to a fully integrated, low voltage digital low-dropout voltage (DLDO) regulator for ultra-low power applications with a load current aware clock modulation scheme. The proposed DLDO presents a novel clock modulation scheme that enhances the trainset performance without degrading the overall DLDO current efficiency. The proposed clock modulation (CM) increases the clock frequency when the load current changes abruptly eliminating the speed-efficiency trade-off using a fixed clock frequency. Thus, it enhances the transient response performance without sacrificing the current efficacy. The proposed DLDO chip is fabricated using 65-nm CMOS technology. It operates at 0.6 V voltage supply with 50mV dropout voltage. It achieves of 99.7% as current efficiency with load current range 10  $\mu$ A to 200  $\mu$ A and the quiescent current 0.9  $\mu$ A.

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## Chapter 1. Introduction

Recent progress in IC technology and design techniques, especially in ultra-low power circuits domain, has led the appearance of fully integrated autonomous and implantable SoC with high performance regarding power consumption, silicon area and power efficiency. Many applications have taken advantages of such a progress including the internet of things (IoT) wearable devices, smart nodes and biomedical sensors, which become an emerging technology nowadays (Figure 1-1) [6-16]. The rapid growth of IoT devices and applications due to the increase of people needs, increases the number of integrated blocks within the IoT SoC. Hence, the design of a compact, fully integrated and efficient power management circuit (PMC) becomes crucial, to supply efficiently, each block inside the IoT SoC with its power demands.

Figure 1-2 shows a generic IoT SoC block diagram. It consists of several blocks namely, communication block, signal processing unit, actuators, sensors, energy source and a PMC. Each block requires a different supply level depending on its operation. So for an IoT SoC, multiple supply level have to be provided per block demand [24]. Thus, a PMC is needed to provide a regulated clean voltage level required by each block within the IoT SoC. However, the PMC design faces some challenges regarding the efficiency and power consumption. Thus, to optimize the PMC design, two points must be taken into consideration. First, the PMC operation scheme should be conditioned regarding the power demand mode (i.e. heavy duty, light duty, stand-by or idle mode). Second, it should be flexible to operate under a wide

range of inputs powers, and to supply multiple output power one at a time or simultaneously [32].

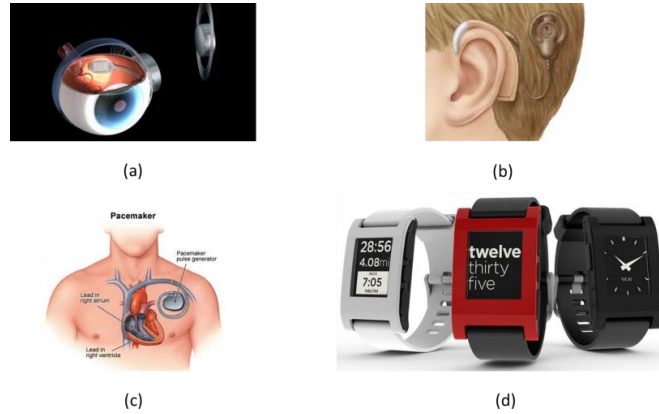


Figure 1-1. Wearable and implantable medical devices examples (a) retina eye sensor, (b) cochlear, (c) pacemaker and (d) smart wearable watch

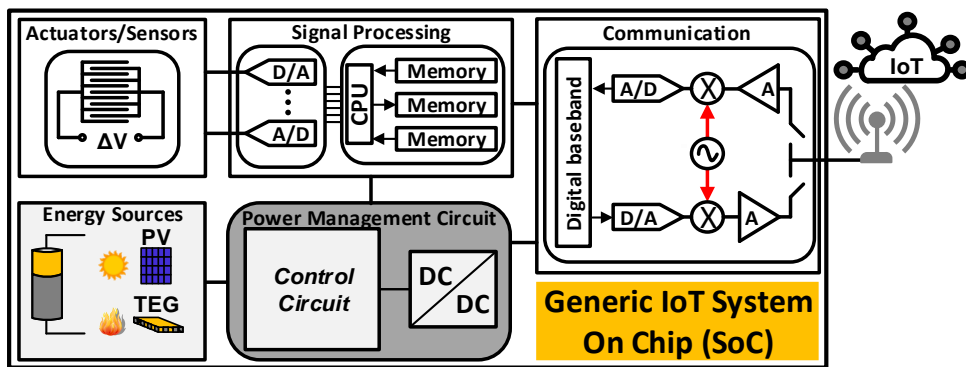


Figure 1-2. Generic IoT SoC with DC energy harvesting systems

## 1.1 Energy Harvesting Power Management Circuits for IoT SoC

Within IoT smart nodes and biomedical devices, the industry cares about size, weight and power consumption, to minimize the cost [32]. With the solid-state circuit developments, the SoC get shrink and following Moore’s law, the supply voltage also gets scaled down with the technology development each 18 month according to Moore’s law, so the trend moves towards decreasing size, increasing performance and functionality and hence decreasing the cost.

The PMC were battery powered for a long time, however, due to the batteries limited life time, a surgical solution for replacement or recharging the battery in case of implantable bio-sensors, or a high maintenance cost for replacement and/or recharging the batteries of more than 50 billion connected devices in case of IoT smart nodes are required. Moreover, the large size of batteries makes them an inadequate solution to power PMC within IoT smart nodes. In this aspect, energy harvester powered PMC garners a considerable attention as it features energy-autonomous IoT smart nodes, and avoid the maintenance cost of recharging and/or replacement of batteries and their bulky size [2, 6, 9, 21, 30, 37-39]. The use of energy harvesting elements (EHL) as an energy source for PMC within bio-sensors and autonomous implantable systems was considered by many literatures the adequate solution [2, 4, 5, 22, 30, 40-51]. Ideally, the use of energy harvesters makes the system fully integrated and has an infinity lifetime.

The EHL such as PV cells, thermoelectric generator (TEG) and piezoelectric transducer scavenge energy from the ambient environment and convert it to electric energy (Figure 1-3). The energy provided by the EHL varies with time, temperature and other environment parameters, as it depends on the environment ambient conditions. Thus, the PMC should be able to deal with all kinds of EHL (DC and AC) and should cover a wide range of input voltages.

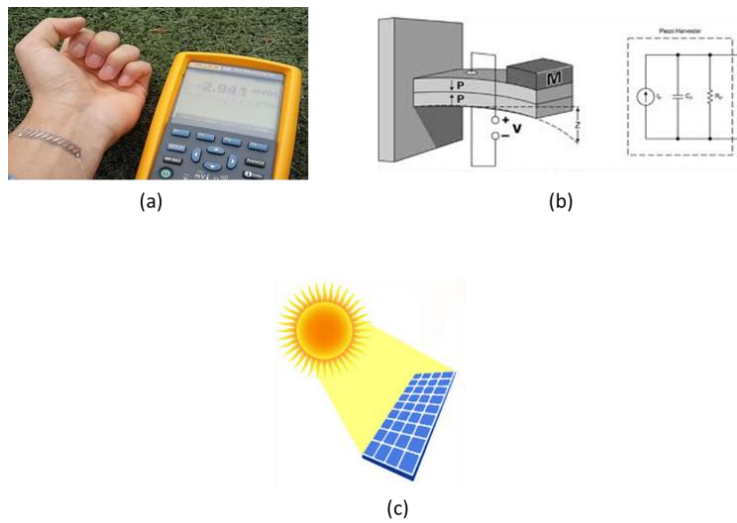


Figure 1-3. Energy harvesting elements example (a) TEG, (b) piezoelectric transducer and (c) photovoltaic cell.

Ideally, the PMC must meet four main design criteria which are considered to be the PMU design challenges [41]:

1. The flexibility to cover a wide range of input voltages.
2. Operates efficiently across its input and output operating range.
3. The ability to regulate the output voltage despite the input voltage variation.
4. Small in size, weight and consume an ultra-low fraction of the input power

A generic PMC within EHS is illustrated in Figure 1-4, the input of which consists of the EHL, and then the harvested power is fed to the PMC. Within the PMC, to maximize the energy being harvested, EHL is connected to a DC-DC power converter controlled by an MPPT circuit, to guarantee that the system operates at its maximum efficiency. The need of an MPPT, along with the DC-DC power converter rises from the harvester nature dependency and load power variability, especially at a

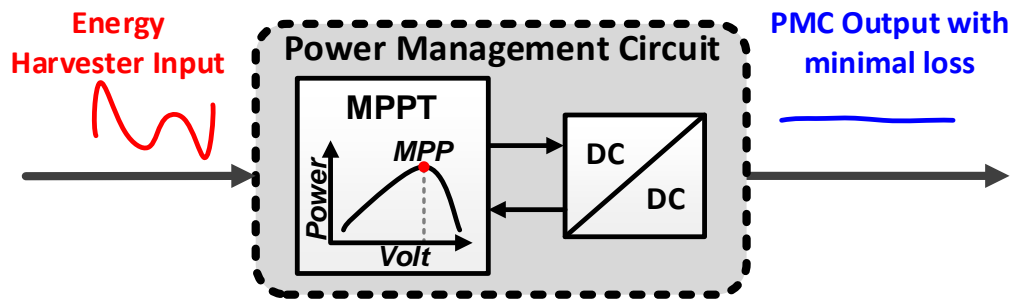


Figure 1-4. A generic PMC within energy harvesting system

regulated output voltage. Finally, the PMC output energy is stored in a super-capacitor/battery or supplied directly to the IoT sensor nodes.

An overview of the DC-DC power converters types and circuit architectures within EHS will be discussed in the next section (Section 1.2), while the MPPT systems roles and existing techniques will be presented in Section 1.3.

## 1.2 DC-DC Power Converters for Energy Harvesting Systems

As shown in Figure 1-1, different blocks within the IoT SoC requires a variety of voltage and power levels. Moreover, modern mobile processors adopt the dynamic voltage scaling (DVS) technique for low power consumption across different operation modes. Thus, a DC-DC power converter becomes an inevitable part of the PMC within EHS for IoT and biomedical applications. The DC-DC converter acts as a voltage regulator which can (i) deal with the variable input power voltage levels due to the EHL small form factor and nature dependency, and (ii) support multiple on-chip voltage levels within IoT SoC.

The DC-DC power converters within PMC can be implemented using linear regulators (e.g. low dropout regulators) or switching regulators (e.g. buck/boost converter and charge pump). Linear regulators, such as low dropout regulators (LDOs), were considered a very good and strong candidate for PMC within EHS [17, 29, 35, 52-64], for their small size, compactness, low noise (i.e. PSRR), high bandwidth, ease of design (i.e. less expensive solution) and can be fully integrated on chip. However, switching regulators have garnered a lot of attention as a DC-DC power converter within EHS PMC for IoT applications [2, 7-9, 21, 26, 30, 31, 34, 36, 37, 39, 42-46, 65-68]. In general, switching regulators offers three main advantages over linear regulators: (i) switching efficiency can be much better because they store energy rather than losing it as a voltage drop (i.e. LDO), (ii) less energy is lost, smaller components and less thermal management are required, and (iii) the input voltage can be stepped up and/or down or can be inverted unlike the linear regulators that only step down their input voltage [41, 69]. However, the choice of the regulator within the PMC depends on the application, the required efficiency and the supported output voltage ripples (i.e. noise).

## 1.2.1 Linear Regulators

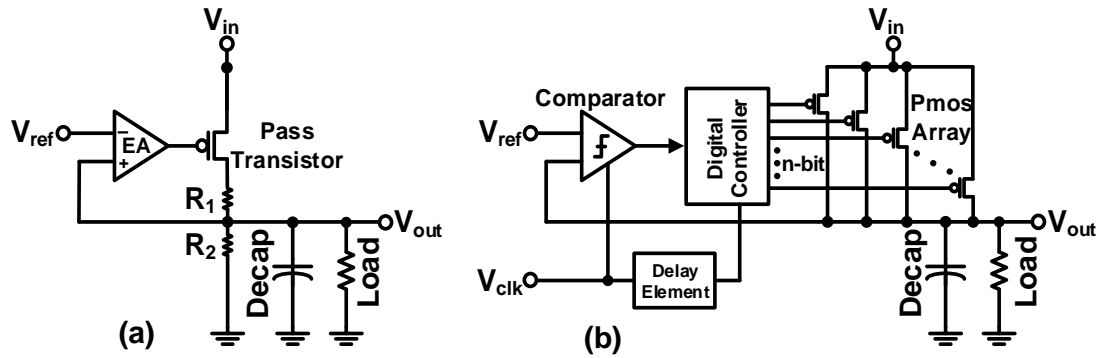


Figure 1-5. Typical architectural of Low dropout regulators (a) Analog LDO and (b) Digital LDO

There are two major types for on-chip LDOs: analog LDO (ALDO) as shown in Figure 1-5 (a), and digital LDO (DLDO), as illustrated in Figure 1-5 (b). The ALDO has been a very strong candidate within PMC for IoT SoC applications [53, 62-64]. ALDOs provide very good performance regarding line regulation, load regulation, and power supply rejection ratio (PSRR). Moreover, they support a fast-transient response due to their high gain loop formed by the error amplifier (EA) gain and the common source gain by the pMOS pass transistor ( Figure 1-5 (b)). However, linear regulators could be designed as a high dropout regulators (HDO) by using an nMOS as a pass transistor. The difference between  $V_{in}$  and  $V_{out}$  in Figure 1-5 (a) equals the dropout voltage ( $V_{DO}$ ). For an analog LDO,  $V_{out-min}$  equals  $V_{ov}$  (i.e. over-drive voltage), while for an analog HDO,  $V_{out-min}$  equals  $2*V_{ov} + V_{thn}$ , where  $V_{thn}$  is the threshold voltage of the nMOS pass transistor. Thus, assuming zero quiescent current, the maximum efficiency that could be achieved by an analog LDO or HDO is given by:

$$\eta_{max} = \frac{V_{in} - V_{out-min}}{V_{in}} \quad (1-1)$$

However, with the IC technology developments, and with the advances in the EHS and IoT SoC designs, the supply voltage scales down to near/sub-threshold [1, 70-72]. ALDO fails to operate with such a low supply voltage since the loop gain degrades at sub- 1V supply which deteriorates its performance regarding the transient response time [53, 57]. Moreover, at sub-1V operation, ALDO PSRR degrades, because the pMOS pass transistor will operate then in the linear region, which will make  $V_{out}$  subjected easily to the noise coming from the  $V_{in}$ . The state of the art ALDO uses a supply voltage above 1V, [63] uses 1.2V as minimum supply while [62] and [64] uses 2V and 1.05V as minimum functional regulated input. ALDO suffers from a high quiescent current within EHS. High quiescent current will increase the PMC power consumption and will degrade the ALDO efficiency. The reason behind the high quiescent current is the error amplifier dc tail current. [62-64] uses 6mA, 20 to 320 $\mu$ A and 4.02 to 164 $\mu$ A as quiescent current respectively, which is considered an inadequate solution for ultra-low power EHS PMC that targets a sub- 1 $\mu$ W power consumption for IoT and bio-medical sensors applications.

For these reasons, many DLDO were proposed in literature [17, 29, 35, 52-61] to regulate the harvested input power. By replacing the analog block with their digital counterpart ( Figure 1-5 (b)), the quiescent current dramatically decreased to 100s of nA range, which solve the problem of the low supply voltage, as the digital circuits successfully operate at sub-1V supply. [29] has proposed a very conventional DLDO block diagram (Figure 1-5 (b)). Each analog block in Figure 1-5 (a) is replaced by its counterpart digital block. For example, the power-hungry EA is replaced by a simple low power latched comparator (Figure 1-5 (b)). The bulky pMOS pass transistor is replaced by an array of parallel pMOS switches which are turned ON or OFF

depending on the load current required, and the number of the switches in this array is decided according to the required output resolution, ripples and maximum output current. The output capacitor is placed to decrease the output ripples hence improving the noise behaviour of the DLDO. Finally, a digital controller consists of a serial-in-parallel-out shift register that turns ON or OFF the pMOS switches within the pMOS array according to the comparator decision made by the negative feedback as illustrated in Figure 1-5 (b).

Despite the wide usage of DLDO over the analog one, DLDO, in fact, suffers from large ripples at the output, and low noise regulation [17, 53, 57]. As the pMOS switches in the switch array are operating in linear region, the output is easily subjected to noise and high ripples, and decrease the transient time response in case of an abrupt load current variation. Contrary, ALDO, has a very high immunity to supply noise, and very fast transient time response, but again it consumes high quiescent current which decrease its current efficiency, a disadvantage that DLDO doesn't have. Two solutions were proposed to alleviate this issue: (i) increase the sampling frequency, will decrease the ripples and increase the transient time performance in DLDO, but at the cost of an increase of the quiescent current hence, which will degrade the efficiency, (i.e. speed-efficiency trade-off) (ii) increase the resolution by increasing the number of switches in the switch array, but again that will increase the quiescent current and the total current efficiency will decrease [53].

Chapter 4 will describe a proposed fully integrated, low voltage DLDO regulator for ultra-low power applications with a load current aware clock modulation scheme. The proposed DLDO presents a novel clock modulation scheme that enhances

the transient performance without degrading the overall DLDO current efficiency eliminating the speed-efficiency trade-off. The proposed DLDO design and architecture will be presented in detail in chapter 4.

### 1.2.2 Switching Regulators

The main difference between switching regulators and linear ones, is that switching regulators store power in one phase, and discharge it in a second phase, so

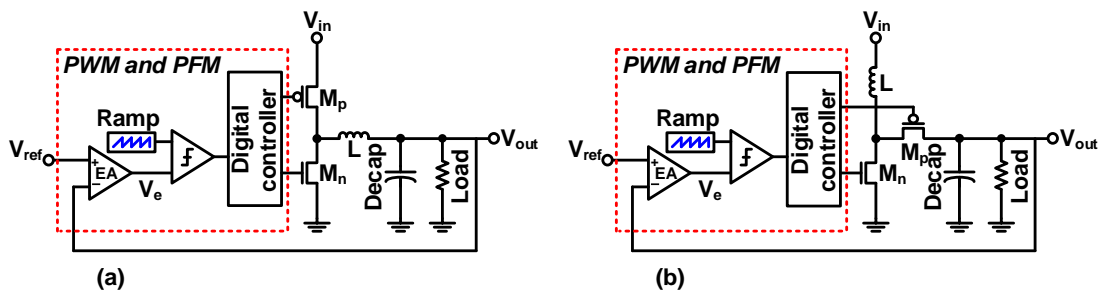


Figure 1-6. Typical architecture of inductive-based switching regulator (a) buck converter, and (b) boost converter

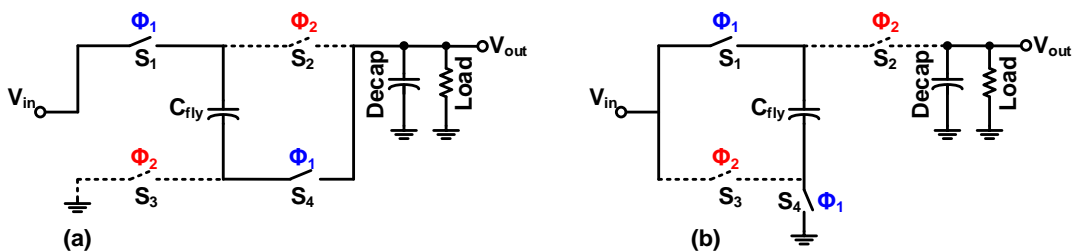


Figure 1-7. Standard cell of a switched capacitor charge pump of a (a) fractional  $\frac{1}{2}$  converter, and (b) 1:2 (doubler) converter

the current is  $90^\circ$  out of phase with the voltage, while linear regulators use voltage drop to regulate the voltage. So, energy within switching regulators can be stored and recovered during the discharge phase of the switching cycle, which makes them higher in efficiency and more attractive for EHS for IoT smart nodes [73-84].

There are two major types of switching regulators used in literature for DC-DC power converter within EHS PMC: inductive based switching regulator that uses an inductor as the energy storage elements as shown in Figure 1-6, and switched capacitor charge pump (SCCP) switching regulators, as described in Figure 1-7.

The inductive based switching regulators can step-down  $V_{in}$  using the buck converter shown in Figure 1-6 (a), or boost  $V_{in}$  to a higher value using the boost converter topology illustrated in Figure 1-6 (b). The main parameter that decides the boosting or step-down ratio is the duty cycle (D). Thus, a pulse width modulation (PWM) block is required to regulate  $V_{out}$  across the variability of output power demanded and input harvested power. The feedback loop shown in Figure 1-6 creates an error voltage ( $V_e$ ) through an EA, then using a ramp generator, a latched comparator tends to change the duty cycle in the direction that makes  $V_{out}$  equals  $V_{ref}$ .

SCCP switching regulators consists only of flying capacitors and CMOS switches as shown in Figure 1-7. A conventional fractional  $\frac{1}{2}$  SCCP is shown in Figure 1-7 (a). It steps-down  $V_{in}$  to half, while a step-up SCCP topology is illustrated in Figure 1-7 (b), where  $V_{in}$  is boosted to ideally  $2*V_{in}$ . Multiple step-down or step-up ratios can be obtained by manipulating the switches configurations with relative to the flying capacitors. The SCCP operation comprises two phases: during the 1<sup>st</sup> phase, the switches notated by  $\Phi_1$  turns on, while the switches notated by  $\Phi_2$  turns off, and vice versa for the second phase. Unlike the inductive based switching regulators, the configuration of the switches in a certain SCCP topology defines the boosting ratio. Thus, for maximum charge transfer efficiency, the clock duty cycle tends to be 50% with a small non-overlap period to avoid shoot-through current.

In EHS, some literature uses the inductive based switching regulators [2, 4, 5, 25-27, 33, 34] as their PMC for its high efficiency (Table 1-I) and the simplicity of controlling its conversion ratio, by simply changing the duty cycle used of the sampling frequency. However, due to the bulky inductor used mostly off chip, which doesn't meet the size and compactness requirement for energy harvesting and wearable sensors system [30, 41], and also introduce EMI noise [85], the SCCP switching regulators become the adequate solution for EHS PMC within IoT smart nodes [22, 30, 31, 41, 42, 86, 87].

Table 1-I: Comparison between inductive based DC/DC converter efficiency

	[2]	[4]	[5]	[25]	[26]	[27]	[33]	[34]
Efficiency	83%	83%	92%	80.8%	72.5%	80%	85-90%	72%

### 1.3 Maximum Power Point Tracking Circuits

In IoT applications, the available power from EHL such as PV cells or TEG cells is limited due to its small form factor. Hence, extracting maximum power from the energy sources is crucial. As mentioned before, to maximize the energy being harvested, a DC-DC power converter controlled by a MPPT is mandatory. The MPPT guarantees that the EHS operates at its maximum power point (MPP). In this aspect, the MPPT has two major roles: (i) maximizing the tracking efficiency ( $\eta_{\text{track}}$ ) by controlling the DC-DC power converter to harvest the maximum power available from the harvester, and/or (ii) maximizing the conversion efficiency ( $\eta_{\text{conv}}$ ) by controlling the DC-DC power converter to maximize the converted harvested power demanded by load.

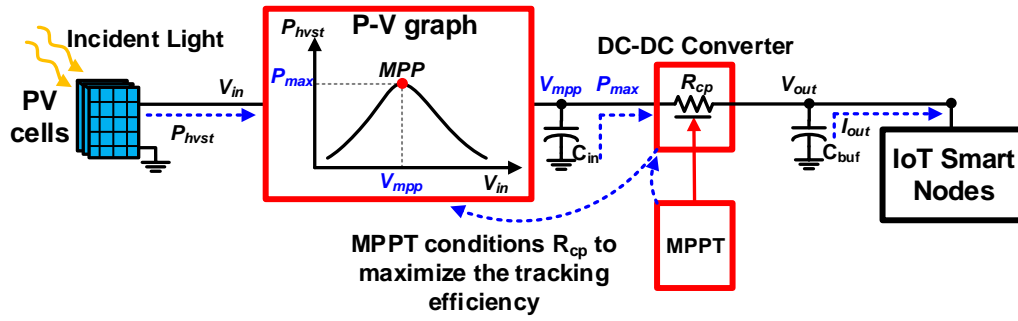


Figure 1-8. MPPT operation principle block diagram to maximize the tracking efficiency for PV EHS

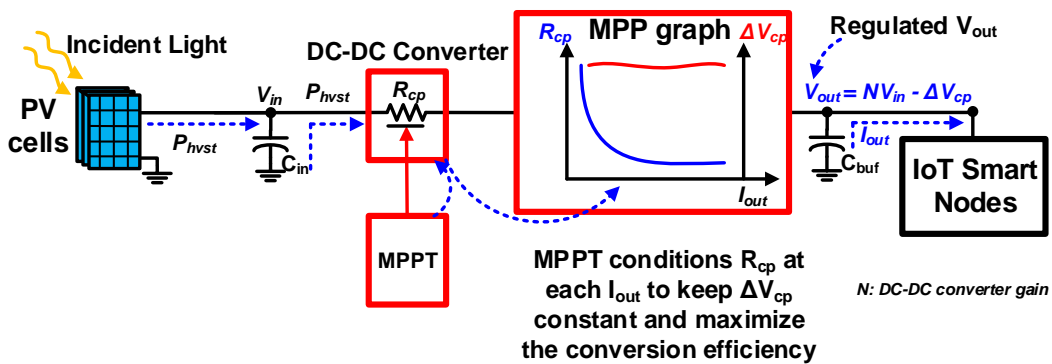


Figure 1-9. MPPT operation principle block diagram to maximize the conversion efficiency for PV EHS

$\eta_{track}$  maximization principle consists of conditioning the DC-DC power converter so that its equivalent impedance ( $R_{cp}$ ) matches the input impedance of the EHL at a given environmental condition (e.g. incident light intensity for PV cells). The MPPT operation principle block diagram for a PV cell as an EHL, is shown in Figure 1-. The target from implementing the MPPT shown in Figure 1- is to increase the tracking efficiency given by:

$$\eta_{track} = \frac{V_{in}}{V_{mpp}} \quad (1-2)$$

Where  $V_{in}$  is the input voltage to the DC-DC power converter and  $V_{mpp}$  is the operating input voltage at which the tracking efficiency is maximized and the MPP condition is satisfied as described in Figure 1-.

$\eta_{conv}$  maximization principle block diagram is illustrated in Figure 1-. The conversion efficiency is defined as follow:

$$\eta_{conv} = \frac{(N * V_{in} - \Delta V_d)}{N * V_{in}} \quad (1-3)$$

Where N is the DC-DC power converter conversion ratio, and  $\Delta V_d$  is the drop voltage across the power converter equivalent resistance ( $R_{cp}$ ), and is described by:

$$\Delta V_d \propto \frac{N * I_{out}}{1/R_{cp}} \quad (1-4)$$

Where  $I_{out}$  is the load current as shown in Figure 1-. Hence, the MPPT, in that role, conditions the  $R_{cp}$  across the output power variability (i.e.  $I_{out}$ ) at a given input condition (e.g. incident light intensity for PV cells), so that  $\Delta V_d$  become constant, at its minimal value, across the output load range. In another word, the MPPT tends to match (i.e. balancing both the instantaneous input and output power) the  $R_{cp}$  with the instantaneous  $I_{out}$  in proportional with the input conditions.

In this aspect, Chapter 2 will present a proposed low-power time-based MPPT to maximize the tracking efficiency ( $\eta_{track}$ ) for PV and TEG EHS for IoT and bio-medical applications along with an overview on the existing MPPT techniques. While a novel ultra-low-power three-dimensional MPPT with improved conversion efficiency ( $\eta_{conv}$ ) for a wide load range is presented and discussed in Chapter 3.

## 1.4 Summary of Thesis Contributions

This thesis makes several contributions and implements some ultra-low-power maximum power point tracking systems for energy harvesting systems for IoT and bio-medical applications. It first proposes a novel time-based MPPT circuit addressing the

tracking efficiency at low-power cost for PV and TEG EHS. It is intended to reduce the power-hungry blocks used in literature such as current or voltage sensors, and reference circuits by proposing a reference-less, indirect, non-interrupting approach using a novel timing-based algorithm addressing the tracking efficiency. The proposed time-based MPPT technique is self-adaptive and applicable to several types of PVs and TEGs without external reconfiguration or change of passive components. It reduces the power consumption and design complexity. It consists of an ultra-low power digital processing unit to execute the proposed timing-based algorithm along with an ultra-low power window comparator to track the maximum open circuit voltage ( $V_{mpp}$ ) without the need to voltage references, perturbation steps and power-hungry voltage or current sensors. A test chip was fabricated in 65-nm CMOS technology, and its functionality is verified at input voltage range of 0.4 V to 1.7 V when supplied by a photovoltaic (PV) micro-cell array using an irradiation range of 200 lux to 1000 lux. The peak tracking efficiency achieved is 96% for PV cells and 97% for TEG.

In continuous of studying MPPT circuits, we have proposed a novel three-dimensional MPPT that addresses the conversion efficiency at wide output load within IoT smart nodes. The power profile in modern wireless sensor nodes technologies varies between idle, normal and heavy-duty modes. Moreover, the weak or light load mode ( $<1 \mu\text{W}$ ) dominates the operation time, which entails that the overall power efficiency is governed by the efficiency within the idle or stand-by mode. Conventionally, the prior state-of-the-art MPPT suffers from modest efficiency at idle modes of operation which degrade their power efficiency. This degradation is due to the gate driver and conduction loss trade-off. In this aspect, the proposed MPPT main

contribution is to improve the conversion efficiency over a wide load range using a novel switch width modulation (SWM) technique. The proposed SWM technique enhances the conversion efficiency at ultra-light load condition by eliminating the trade-off between the gate driver and conduction loss. The tested chip, fabricated in 65-nm CMOS technology, can harvest from 0.35 V and provides a regulated output voltage at 1 V with peak efficiency of 88% at heavy duty modes and conversion efficiency > 60% at idle mode.

The last part of this thesis is devoted to a near-threshold low-power digital LDO chip introduced in Section 1.2.1. The proposed DLDO main contribution is to eliminate the speed-efficiency using a fixed sampling clock frequency trade-off mentioned in Section 1.2.1. The proposed clock modulation (CM) increases the clock frequency when the load current changes abruptly eliminating the speed-efficiency trade-off using a fixed clock frequency. Thus, it enhances the transient response performance without sacrificing the current efficacy. The proposed DLDO chip is fabricated using 65-nm CMOS technology. The proposed DLDO functionality is verified at 0.6 V supply voltage with 50 mV dropout voltage. The tested chip, fabricated in 65-nm CMOS technology, demonstrates the current efficiency of 99.7% with the load current from 10  $\mu$ A to 200  $\mu$ A with and the quiescent current of 0.9  $\mu$ A.

The organization of this thesis is as follows: Chapter 2 explains the prior art MPPT techniques briefly and presents a novel self-adaptive, indirect time-based MPPT for tracking efficiency improvement for EHS IoT smart nodes. Chapter 3 describes a proposed three-dimensional MPPT technique to eliminate the power efficiency limitation issue at wide load range applications, and enhancing the conversion

efficiency at various IoT wireless sensor nodes operation modes. Chapter 4 presents a low voltage low power DLDO design for EHS for IoT applications. Finally, Chapter 5 concludes this thesis and discusses the future work that consists of a PMC powered by novel mechanical energy harvester called triboelectric-nanogenerator (TENG). First a realistic electrical model is developed, then a PMC is employed to validate the developed model and its significance within IoT and bio-medical sensors applications.

## **Chapter 2. Proposed Low Power, Self-adaptive And High Tracking Efficiency Time-based MPPT for IoT Applications**

### **2.1 Introduction**

Distributed sensors for condition monitoring of sustainable buildings, and wearable sensors of body area networks including sensors for biometric, health monitoring, and Internet-of-Things (IoT) applications become emerging technologies [1, 3, 38]. Hence, the design of efficient, self-sustained PMC design becomes crucial in order to realize energy harvesting supplied IoT applications [21, 88, 89]. Recent progress in integrated circuit (IC) technology and design techniques, especially in ultra-low power circuit's domain, have led the appearance of fully integrated autonomous and implantable systems on chip (SoC) with high performance regarding power consumption, silicon area, and power efficiency. Energy harvesters aim to power the PMC that have been battery powered for a long time. Within IoT, replacement of batteries with energy harvesters enables a self-sustained, fully integrated and prolonged lifetime PMC. Fully wireless and self-sustainability paves the way for ease of installation as well as the relocation of such stand-alone and miniaturized IoT systems are important requirements for easy, cost-efficient, and flexible application. As several studies show, the usage of energy harvesting allows a battery-less supply of such systems [90, 91]. Numerous publications demonstrate the use of energy harvesters including solar, thermal and mechanical energy [2, 3, 38, 42-45, 90, 92-96]. Among these energy harvesters, solar energy harvesting is one of the most promising renewable energy sources. Using thin-film and even flexible solar cells is of great advantage for harvesting solar and light energy [19, 20, 23, 97-100].

In IoT applications, the available power from energy sources such as PV cells or TEG cells is limited due to its small form factor. Hence, extracting maximum power from the energy sources is crucial. However, PV input resistance varies continuously with the variation of the incident light irradiance. Thus, in order to maximize the harvested energy and address these variations, a DC-DC converter controlled by a maximum power point tracking system (MPPT) is required. The MPPT guarantees that the energy harvesting system operates at its maximum power point (MPP) voltage ( $V_{mpp}$ ) [101].

The remainder of this chapter is organized as follows. An overview of the existing MPPT techniques is presented in Section 2.2. The state-of-the-art time-based MPPT along with the proposed time-based MPPT (TB-MPPT) operation principle are discussed in Section 2.3. Section 2.5 explains the architecture and the circuit implementation of the proposed TB-MPPT. Design considerations in the proposed MPPT technique are presented in Section 2.6, followed by the measurement results in Section 2.7. Finally, Section 2.8 concludes this chapter.

## 2.2 Overview of Existing MPPT Techniques

Various MPPT methods have been reported in literature. Generally, they can be categorized into two types, direct MPPT and indirect MPPT. A direct MPPT system aims to maximize the output power of the source (PV, TEG) by sensing the output current or voltage of the source and adjusting control of the converter means accordingly. Figure 2-1 shows two conventional direct MPPT examples (options 1 and 2). The simplest direct MPPT method is the fractional open circuit (FOCV) technique (option 1) [92, 101-103]. It depends on the linear empirical relation between the open circuit voltage ( $V_{ph,oc}$ ) and  $V_{mpp}$  ( $V_{ph,oc} = K_{FOC} * V_{mpp}$ ). Although this method is simple and allows a very robust operation, it requires an open circuit situation for sampling the open circuit voltage and multiplying it by the factor  $K_{FOC}$ ,

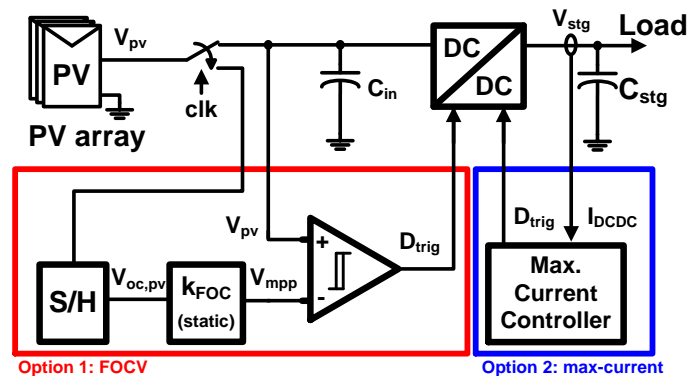


Figure 2-1. Conventional direct MPPT implementations using either (1) fractional-OCV sampling, or (2) maximizing output current which reduces the extraction efficiency.

Moreover,  $K_{FOC}$  varies widely [2, 104, 105] due to various parameters like PV material temperature, light irradiation, and cell-to-cell mismatches within PV arrays [38, 93, 101, 105]. In addition, the study in [105] shows how the PV power and the fill-factor (FF) degrade due to aging effect. As a result, the PV input impedance as

well as the MPP can vary even at the same light irradiance. Thus, FOCV needs a periodic pre-configuration, which makes it unsuitable for portable electronics and smart wireless nodes. Another direct MPPT technique is the perturb and observe (P&O) method (Figure 2-1 : option 2) [21, 41, 42, 45]. In P&O, the output power is periodically calculated by measuring the output voltage and current, and is compared with the previously computed output power. After that, it perturbs the system to track MPP. However, the P&O technique continuously monitors the PV power, i.e.  $V_{pv}$  and

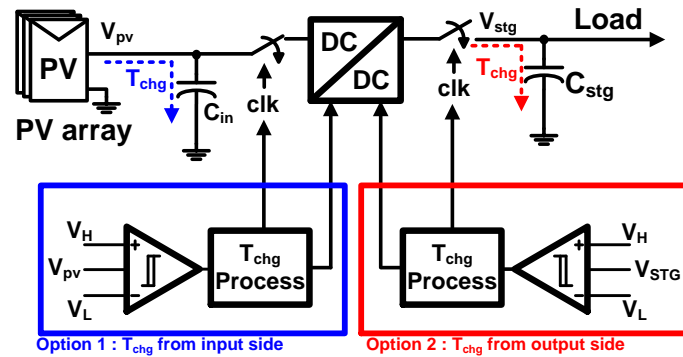


Figure 2-2. Examples of indirect MPPT implementations using either (1)  $T_{chg}$  at the input side, or (2)  $T_{chg}$  at the output side

$I_{pv}$ , at a sufficiently high rate through inbuilt current and voltage sensors (Figure 2-1: option 2), increasing the power overhead. Therefore, it is also not suitable for micro-energy harvesting (MEH) systems.

To overcome the limitations of the direct MPPT techniques, indirect MPPT is introduced where PV power is estimated without directly measuring output voltage or current. Figure 2-2 shows examples of indirect MPPT. Power information can be estimated by measuring charging time ( $T_{chg}$ ) at the input side (option 1) or at the output side (option 2) and processing it (Figure 2-2). This approach was adopted by [18, 94], however, the  $T_{chg}$  processing block was implemented by power hungry analog circuits, which introduces power overhead and increases the design complexity. In [2], an

indirect MPPT for PV cells uses pulse width information of the high-side switch of a boost converter to estimate the MPP. Although this technique achieves a tracking efficiency of 96%, its implementation is limited in dim light conditions where a high conversion ratio DC-DC converter is necessary. The work presented in [23] measures  $T_{\text{chg}}$  at the output (option 2). It uses a window comparator for line regulation and charging phase definition and achieves a tracking efficiency of 86%. However, it still needs a perturbation step to vary the DC-DC converter impedance. The above techniques using time information to estimate the harvested power are called TB-MPPT.

In this work, we propose a novel ultra-low power, TB-MPPT with a novel hill-climbing algorithm using time as a measure for tracking the MPP (i.e. energy-time relation). The proposed TB-MPPT is self-adaptive that provides the maximum harvested power directly to PMCs without the need of voltage references, perturbation step, and current or voltage sensors [21, 41, 42], which consequently reduces the power consumption and the design complexity. In addition, the proposed TB-MPPT provides a wide harvesting range. Therefore, it can be applied to various PV cell types and PMCs at different light conditions. Finally, the proposed TB-MPPT introduces a variable gain technique for reducing the transient response time in case of a sharp step variation in the input light irradiance.

### **2.3 Proposed Time-based MPPT Method**

In this section, the state-of-the-art time-based MPPT techniques are discussed followed by the operation principle of the proposed TB-MPPT, along with the proposed self-adaptive TB-MPPT algorithm. Finally, a proposed energy-to-time

normalization technique for accuracy improvement and tracking efficiency enhancement is presented.

## 2.4 State-of-the-art Time-Based MPPT and Limitations

The main idea of a TB-MPPT for ultra-low power energy harvesting systems

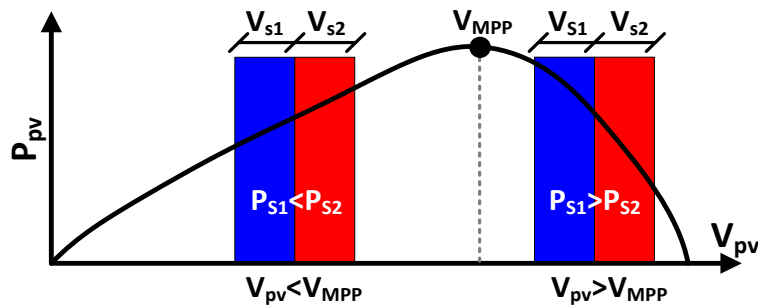


Figure 2-3. Indirect MPPT operation principle [18]

for IoT applications is using time to measure harvested power and track MPP. In [19, 34] a time-based MPPT technique was proposed. It assumes that a capacitor is charged in small voltage or energy steps (Figure 2-3). By investigating the time-voltage or time-energy relations when charging a capacitor from a source, two observations can be obtained:

1. Energy-time relation: the time is minimal for the voltage step overlapping with VMPP, and increases as the voltage step moves away from VMPP.
2. Voltage-time relation: the first half of the voltage steps (VS1) needs more time than the second half of the voltage step (VS2) if the voltage step is located below VMPP, and it is vice versa if the step is above VMPP.

As shown in Figure 2-3, it measures the power in the first half of a charging voltage step (PS1), and the second half of the same step (PS2), separately. After that,

they are compared to track MPP. At MPP (i.e.  $V_{pv}=V_{mpp}$ ),  $P_{S1}$  should be equal to  $P_{S2}$ . However, this method consumes higher power and increases circuit complexity consumption due to three comparators, three threshold levels, one integrator and one sample-and-hold circuit. This technique is proven on a PCB level operating in the 10-mW power range aided by a battery [94, 106].

Another time-based approach for MPPT was introduced in [2]. It extracts, and estimates harvested power from the pulse width in a boost converter. The time of this pulse width is related to the harvested power through the boost converter inductor volt-second rule [2] along with the input power equation. The time-power relation is approximated as follows:

$$t_{high-side} = \frac{1}{V_{load}} \sqrt{\frac{2 * L * P_{in}}{f_s}} \quad (2-1)$$

where  $t_{high-side}$  is the high side switch pulse width for a boost converter,  $V_{load}$  is the boosted voltage,  $L$  is the boost converter inductance,  $P_{in}$  is the input power, and  $f_s$  is the switching frequency. Although this method shows higher efficiency (96% peak efficiency), the approximation made in (2-1) is only valid for high conversion ratios, and will lose accuracy in case of a low conversion ratio boost converter [2]. Moreover, its implementation is limited to inductor based DC-DC converter, which limits its adaptability.

The TB-MPPT presented in [23] uses the technique shown in (Figure 2-2: option 2). Their TB-MPPT measures the  $T_{chg}$  at the output side, and depending on their analyzed power-time relation shown in (2-2).

$$P_{out} = V_{stg} \frac{C_{stg}(V_H - V_L)}{T_{chg}} \quad (2-2)$$

Here,  $P_{out}$  is the output power,  $V_{stg}$  and  $C_{stg}$  are the output voltage and output capacitor respectively (Figure 2-2),  $V_H$  and  $V_L$  are the window voltage as described in Figure 2-2. The technique proposed measures  $T_{chg}$  then perturb a switched capacitor based (SC) DC-DC converter accordingly. The perturbation is accomplished by changing a bank capacitor configuration, so to change the SC converter impedance. So as the computed time decreases, the power increases, and the perturbation keeps the same direction. If the computed time increases, the MPP is reached, and the perturbation toggles its direction. Although the proposed method achieves 86% as tracking efficiency as mentioned before, it needs external references for generating  $V_H$  and  $V_L$ . Moreover, a perturbation step is needed. In their work, they modify a capacitor bank configuration, which needs many switches, increasing the design complexity, power consumption, and the silicon area, makes the design less cost-efficient. In addition, their technique is dependent on the regulated output voltage ( $V_{stg}$ ) and the converter type.

Hence, a time-based MPPT independent of PMC type, with wide harvesting range, along with low power, simple and smart time computation techniques, is mandatory for efficient, self-adaptive and standalone PV harvesting systems for IoT applications.

### 2.4.1 Proposed Time-based MPPT Tracking Principle

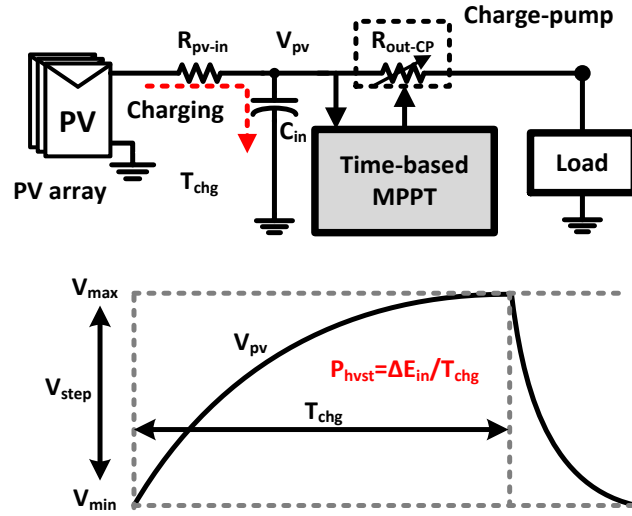


Figure 2-4 Time-based MPPT operation principle

The proposed TB-MPPT supply the maximum power harvested ( $V_{mpp}$ ) directly to the PMC and operates independently of the PV or PMC type (SC or inductor based converter). Figure 2-4 shows the principles of the proposed TB-MPPT. An input capacitor ( $C_{in}$ ) at  $V_{pv}$  is charged by a fixed step voltage ( $V_{step} = V_{max} - V_{min}$ ) which requires a charging time ( $T_{chg}$ ). Hence, the input harvesting power is given by:

$$P_{hvst} = \frac{\Delta E_{in}}{T_{chg}} = \frac{0.5 * C_{in}}{T_{chg}} (V_{max}^2 - V_{min}^2) \quad (2-3)$$

where  $P_{\text{hvst}}$  is the input harvested power,  $\Delta E_{\text{in}}$  is the input energy absorbed by  $C_{\text{in}}$  during each charging phase ( $T_{\text{chg}}$ ).  $T_{\text{chg}}$  is the charging time taken to charge  $C_{\text{in}}$  by  $V_{\text{step}}$ . As shown in (2-3), by tracking towards minimum  $T_{\text{chg}}$ , maximum  $P_{\text{hvst}}$  is indirectly achieved, assuming constant  $V_{\text{step}}$  during the tracking operation. In the circuit shown in Figure 2-4, the charge pump is represented by  $R_{\text{out-cp}}$  whose value is controlled by the proposed TB-MPPT. Also note that  $R_{\text{pv-in}}$  represents the output

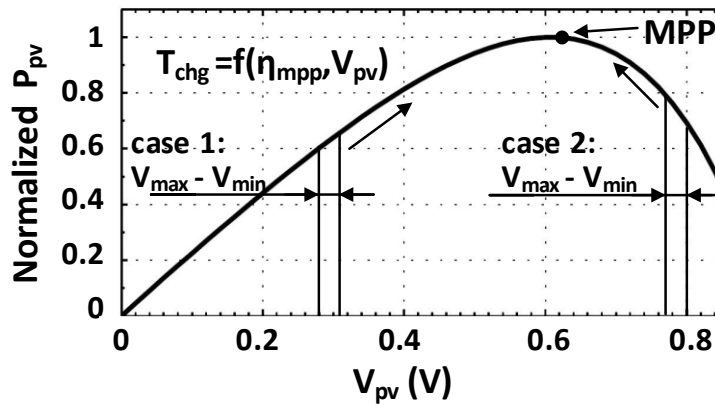


Figure 2-5. Fixed tracking voltage window of 30 mV hill-climbs towards the MPP.

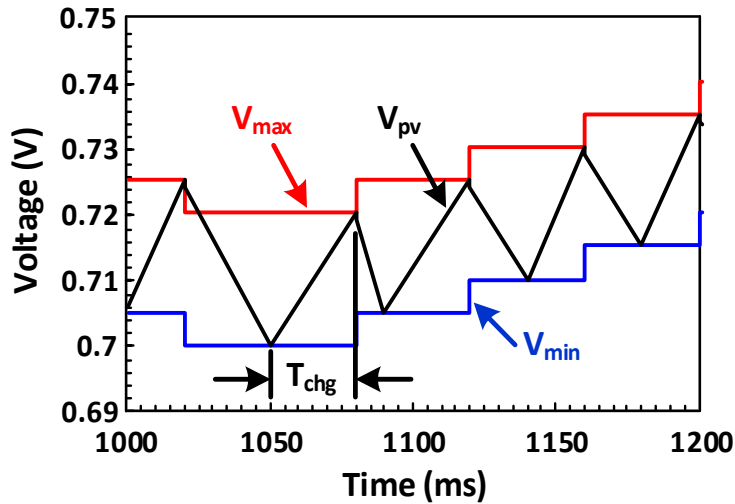


Figure 2-6. Tracking – transient signals capture,  $V_{\text{max}}$ ,  $V_{\text{min}}$ , and  $V_{\text{pv}}$

impedance of the PV array.

The proposed TB-MPPT shows timing based hill-climbing algorithm where it tracks the shortest  $T_{\text{chg}}$ , as illustrated in Figure 2-5 [38]. The input capacitor  $C_{\text{in}}$  is

charged from a start voltage  $V_{\min}$  to a stop voltage  $V_{\max}$  ( $V_{\text{step}}=30\text{mV}$ ), as illustrated in Figure 2-6. As shown in Figure 2-5, these two voltages create a narrow window around the actual MPP. When this window is moved away from the MPP, less source energy is available and  $T_{\text{chg}}$  would increase. Due to the given square-law in (2-3), there will be a dependency of  $\Delta E_{\text{in}}$  on the absolute values of the MPPT window intervals [ $V_{\min}$ ,  $V_{\max}$ ], hence, to validate the assumption, an energy-to-time normalization must be implemented [7]. This normalization will compensate for the non-linearity in (2-3) and makes  $\Delta E_{\text{in}}$  independent of the absolute values of  $V_{\min}$  or  $V_{\max}$ . So, the MPPT will calculate a normalized charging time ( $T_{\text{chg-norm}}$ ) rather than the charging time  $T_{\text{chg}}$  defined in Figure 2-4. The proposed energy-to-time normalization will be discussed in the next section (Section 2.4.2). After the proposed energy-to-time normalization, a digital controller is needed to evaluate the shortest  $T_{\text{chg-norm}}$  for a fixed amount of energy (i.e.  $\Delta E_{\text{in-norm}}$ ). Using this method, only simple time-to-digital conversion is necessary. This has two advantages. Firstly, very low-power implementations are possible, and secondly, the compensated minimum time condition (indirect MPP indication) does not need any reference. Thus, a self-sufficient stand-alone system is easier to realize.

The TB-MPPT realization flow chart is shown in Figure 2-7. During the charging phase, a timer starts calculating the charging time ( $T_{\text{chg}}$ ). Then, during the discharging phase, the calculated  $T_{\text{chg}}$  is processed through a digital controller for non-linearity compensation, and then the obtained  $T_{\text{chg-norm}}$  is being compared with the one obtained in the previous cycle. If  $T_{\text{chg-norm}}$  increases, it means that the power has been decreased and then the MPPT will change the tracking direction, and vice versa. The proposed algorithm tracks the  $V_{\text{MPP}}$  in both cases as shown in Figure 2-5 (i.e. case-1 and case-2). Figure 2-8 and Figure 2-9 illustrate how the proposed TB-MPPT algorithm tracks MPP in case-1 ( $V_{\text{pv}} < V_{\text{MPP}}$ ), and in case-2 ( $V_{\text{pv}} > V_{\text{MPP}}$ ), respectively.

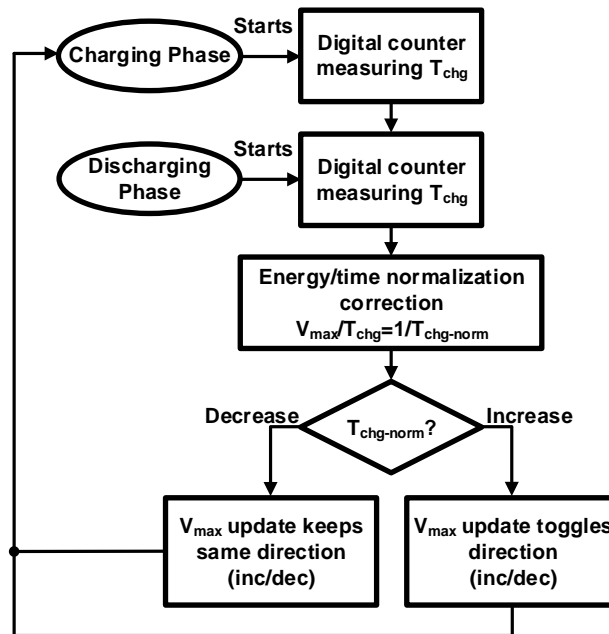


Figure 2-7. Time-based MPPT realization flow chart.

Initially, the window  $[V_{\text{max}}, V_{\text{min}}]$  moves one step up, hence  $V_{\text{pv}}$  increases. Then, if the power increases (i.e.  $T_{\text{chg-norm}}$  decreases) the window keeps the same direction, and if the power decreases (i.e.  $T_{\text{chg-norm}}$  increases) the window toggles the direction.

## 2.4.2 Energy-to-Time Normalization

As described in the previous section (Section 2.4.1), the proposed TB- MPPT digital controller uses the charge up time  $T_{chg}$  as an indirect measure for efficient charging. Thereby, having a minimum  $T_{chg}$  for the same (constant) amount of energy  $E_{in}$  indicates that the harvesting system harvests the maximum power, as shown in (2-4), (i.e. operating at the MPP).

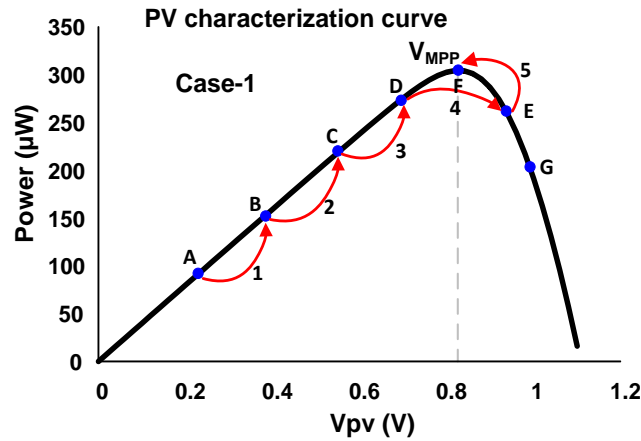


Figure 2-8. TB-MPPT tracking when  $V_{pv}$  is on the left side of  $V_{MPP}$ .

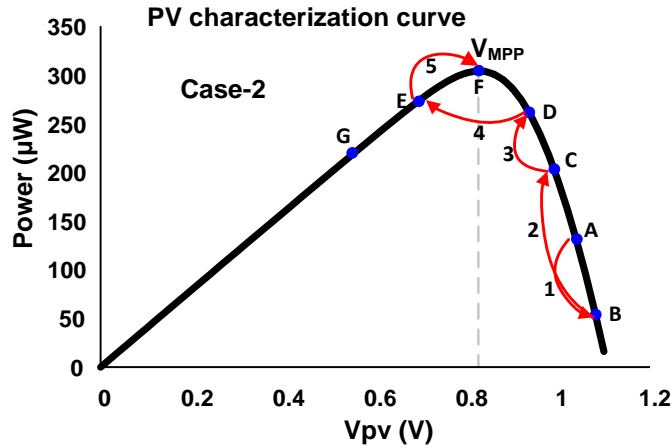


Figure 2-9. TB-MPPT tracking when  $V_{pv}$  is on the right side of  $V_{MPP}$ .

$$\frac{E_{in}}{T_{chg-min}} = P_{hvs-max} \rightarrow max \quad (2-4)$$

However, as shown in (2-3), due to non-linearity in the capacitive charging relation,  $\Delta E_{in}$  varies with the absolute values of  $[V_{min}, V_{max}]$ . Thus, the assumption of a constant amount of energy is corrupted, which implies the employment of an energy-to-time normalization correction technique, so that to compensate for the dependency of  $\Delta E_{in}$  on the absolute values of the MPPT window  $[V_{min}, V_{max}]$ . Even though the energy  $\Delta E_{in}$  changes by a square-law in accordance to the absolute voltage level of the interval  $[V_{min}, V_{max}]$  as shown by (2-3), a simple linear division of either  $V_{max}$  or  $V_{min}$  by  $T_{chg}$  is sufficient as an energy-to-time normalization-correction step, as shown in (2-5).

$$P_{hvst} = 0.5 \frac{C_{in}}{T_{chg-norm}} \left( V_{max} - \frac{V_{min}^2}{V_{max}} \right) \quad (2-5)$$

Here,  $T_{chg-norm}$  is equal to  $T_{chg} / V_{max}$ . The above equation can be simplified to

$$P_{hvst} \approx 0.5 \frac{C_{in}}{T_{chg-norm}} V_{step} \quad (2-6)$$

where  $V_{step}$  is constant within the tracking operation. In general, the use of  $T_{chg}$ , and  $V_{min}$  or  $V_{max}$  is very convenient, since these values are already available in the different registers and counters of the TB-MPPT digital controller. Figure 2-10 shows  $\Delta E_{in}$  variation with  $V_{max}$  before the proposed energy-to-time normalization (Figure 2-10, red) and after the normalization correction step (Figure 2-10, blue). It's clear that  $\Delta E_{in}$  becomes constant regardless of the absolute value of  $V_{max}$  or  $V_{min}$ .

Hence, the expression in (2-6) can be re-written as

$$P_{hvst} = 0.5 \frac{1}{T_{chg-norm}} E_{in-norm} \quad (2-7)$$

where  $E_{in\_norm}$  equals  $(0.5C_{in}V_{step})$ . Hence, the proposed TB-MPPT tracks the shortest  $T_{chg\_norm}$  by periodically calculating  $V_{max}/T_{chg}$  for a constant  $E_{in\_norm}$  ( $V_{step}$ ). Computation of the division is an inexpensive, low power and low-complex operation, which makes it an adequate solution for energy harvesting systems for ultra-low power applications.

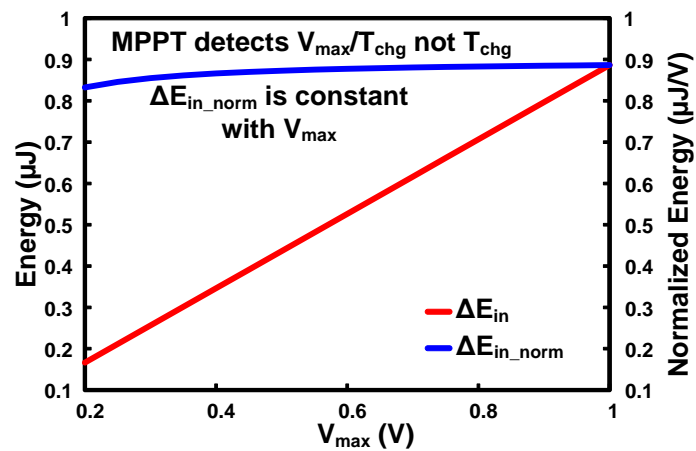


Figure 2-10.  $\Delta E_{in}$  variation across  $V_{max}$  before normalization (red) and after normalization (blue)

## 2.5 Proposed Time-based MPPT Architecture and Circuit Implementation

The proposed TB-MPPT system in Figure 2-11 consists of six main blocks, namely, a digital processing unit (DPU) where the digital algorithm described in Figure 2-7 runs, an 8-bit digital to analog converter (DAC), a window comparator unit (WCU), a bias unit, a ring oscillator (ROSC), and a power-on-reset block (POR). POR enables the bias and oscillator circuits. The WCU output ( $V_{wc}$ ) controls the power nMOS, and is fed to DPU. Thus, DPU, 8-bit DAC, and WCU form the feedback path.

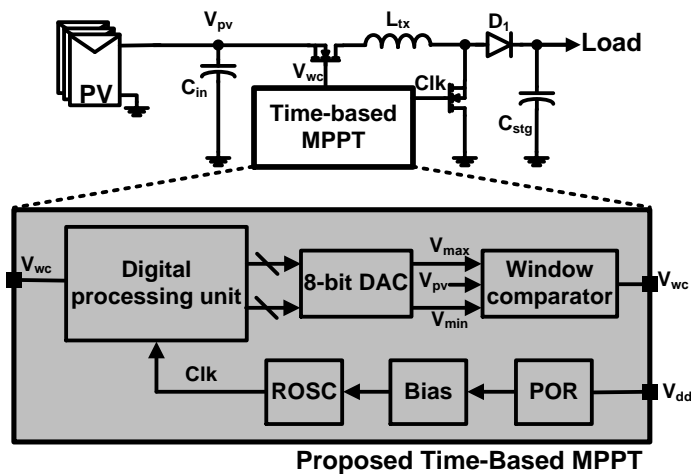


Figure 2-11. The proposed TB-MPPT system architecture ( $L_{tx}=1.20\text{mH}$ )

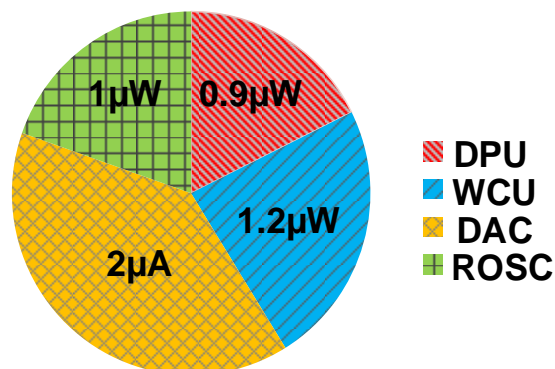


Figure 2-12. Power consumption by building block of the proposed time-based MPPT

Figure 2-12 shows the power consumption breakdown of the major building blocks of the proposed MPPT. The detailed operation of each major block is as follows.

### 2.5.1 Digital Processing Unit (DPU)

Figure 2-13 illustrates the DPU architecture. It consists of three registers ( $R_c$ ,  $R_n$ , and  $R_o$ ), a 14-bit counter, a binary comparator, a  $V_{max}$  counter, a digital divider and

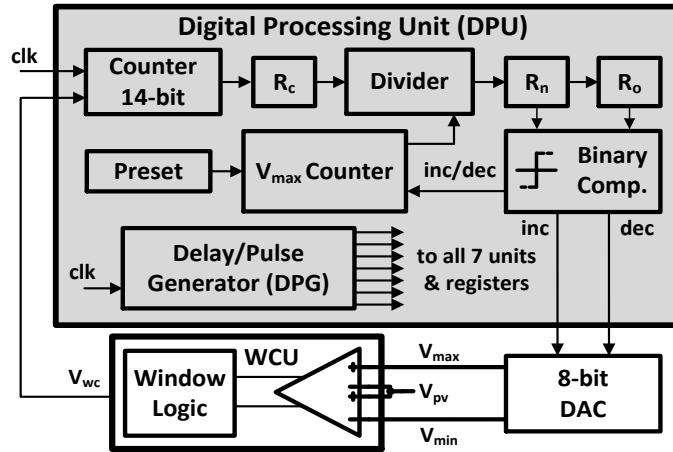


Figure 2-13. Digital processing unit architecture of the proposed TB-MPPT

a delay and pulse generator (DPG). During the charging phase ( $V_{wc}=0$ ), The 14-bit counter measures  $T_{chg}$  by utilizing a reference clock signal (clk), generated by ROSC (Figure 2-11). The  $C_{in}$  value, the clock signal frequency, and  $V_{step}$  determine the counter size. For a large  $C_{in}$ ,  $T_{chg}$  may exceed the 14-bit limit due to the slow charging within the WCU window, so the counter may overflow. Thus, larger  $C_{in}$  requires lower clock frequency. On the other hand, a small  $C_{in}$  needs a smaller counter size, and then faster clock signal can be employed. However, a smaller counter size will reduce the TB-MPPT resolution after the division ( $T_{chg-norm}$ ) and will degrade the tracking efficiency.

During the discharging phase ( $V_{wc} = 1$ ), DPG is triggered to start DPU operation. For timing and delay optimization, DPG is implemented by a finite state machine (FSM) triggering seven clock phases for the functional blocks in DPU. The timing diagram shown in Figure 2-14 describes the DPU operation. First, register  $R_c$  stores the  $T_{chg}$  value from the 14-bit counter. After that, the proposed normalization-correction is executed using the digital divider block.  $V_{max}$  is initially stored digitally in the  $V_{max}$  counter. After calculating  $T_{chg-norm}$ , it is stored in  $R_n$  and compared with the previous  $T_{chg-norm}$  stored in  $R_o$  through a binary comparator. The binary comparator output pulse increments or decrements the 8-bit DAC output ( $V_{max}$  and  $V_{min}$ ) depending on the comparison, and updates the  $V_{max}$  value in the  $V_{max}$  counter, accordingly.

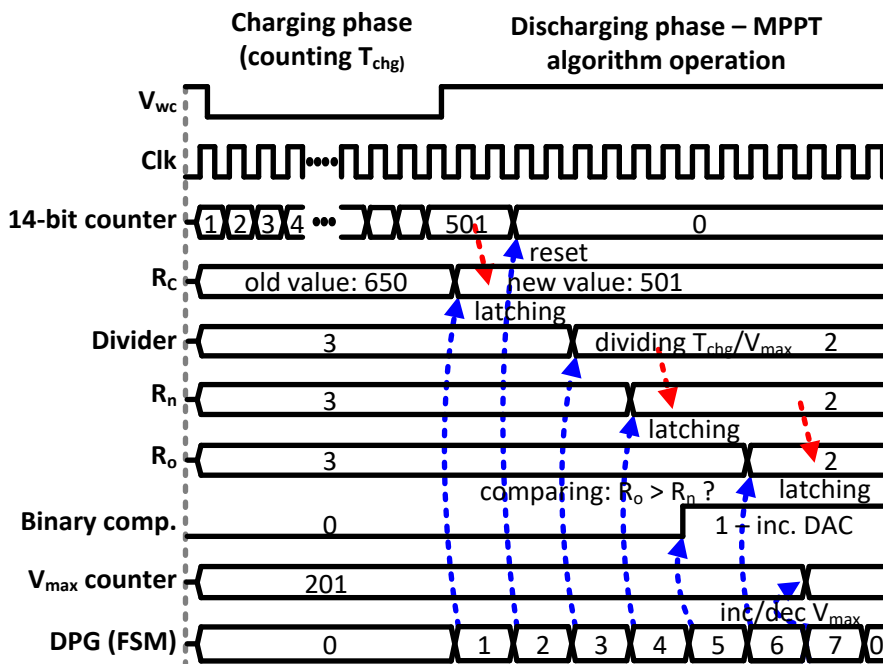


Figure 2-14. Timing diagram of the digital processing unit (DPU)

## 2.5.2 One-hot Barrel Shift Register and DAC

DPU controls DAC through a one-hot barrel shift register (Figure 2-15 (a)). The barrel shift register utilizes the DPU output pulses (i.e. inc and dec) and generate 8-bit binary codes for incrementing or decrementing the DAC output voltage. The barrel shift register output consists of 200 bits and the hot bit ‘1’ is shifted by ‘GT’ bits depending on the inc and dec signals. The inc pulse shifts the hot bit to the right for increasing  $V_{max}$  and  $V_{min}$  by one step while the dec pulse moves the hot bit to the left and decreases  $V_{max}$  and  $V_{min}$ . The ‘GT’ value needs to be selected carefully, which will be discussed in the next section (Section 2.6).

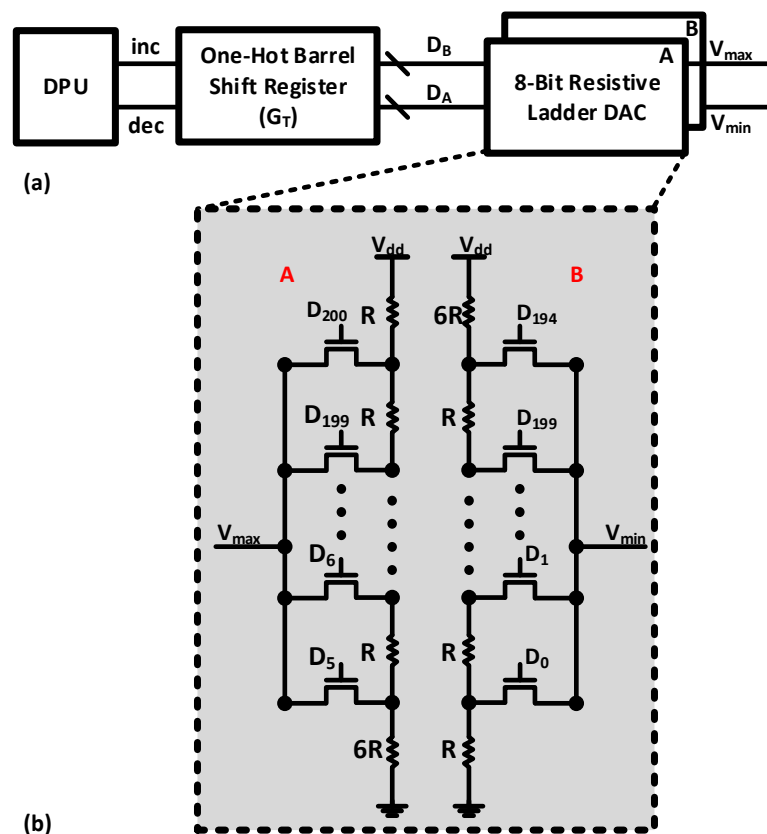


Figure 2-15. Ultra-low power 8-bit DAC (a) schematic of 8-bit DAC with DPU, (b) circuit schematic of the 8-bit resistive ladder DAC

A resistive ladder DAC (Figure 2-15 (b)) is employed because of simplicity. Nonlinearity affects both  $V_{max}$  and  $V_{min}$ . Therefore, it does not affect the operation of

the proposed TB-MPPT. The mismatches in the resistors are minimized through careful layout. The difference ( $V_{step}$ ) between  $V_{max}$  and  $V_{min}$  determines the  $V_{pv}$  ripples ( $V_{pv-rip}$ ). Smaller  $V_{step}$  lowers  $V_{pv-rip}$  and accordingly increases the tracking efficiency. In this design, the DAC employs 8-bit resolution with the step size ( $V_{LSB}$ ) of 5 mV and the window ( $V_{step}$ ) of 30 mV. The 8-bit resolution is chosen to cover all the harvested range based on the  $V_{step}$  and  $V_{LSB}$ .

### 2.5.3 Window Comparator Unit

Figure 2-16 illustrates the window comparator unit. It consists of two comparators (comparator A and B) and window logic (Figure 2-16 (a)). The comparators use conventional dynamic latched comparators with ultra-low power consumption ( $< 600nA$ ). Figure 2-17 explains the window comparator configuration and the window logic. The window comparator (comparator A and B) keeps  $V_{pv}$

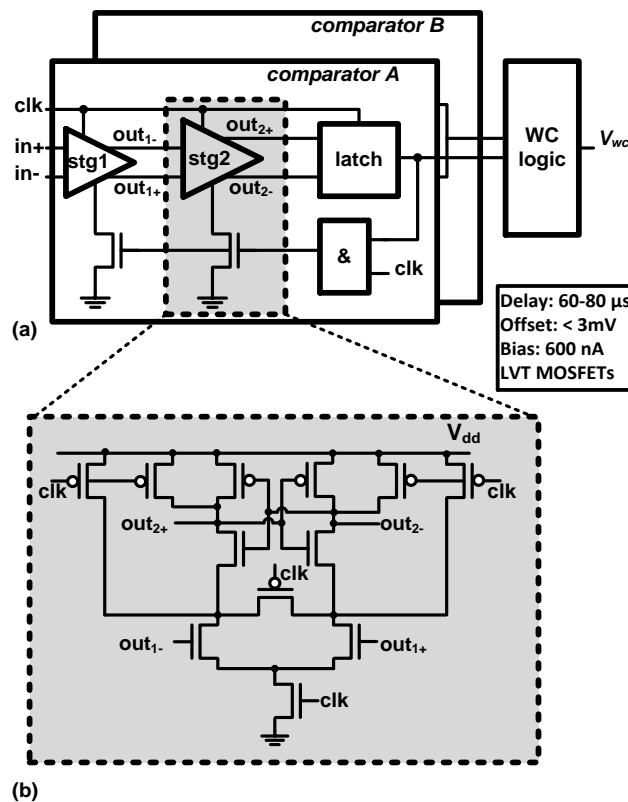


Figure 2-16. Ultra-low power precision window comparator (a) schematic with responsive power gating, (b) regenerative decision stage

within the window ( $V_{step} = 30mV$ ) until it reaches  $V_{mpp}$ . Initially,  $V_{pv}$  is within the window, discharging  $C_{in}$  in Figure 2-11 ( $V_{wc} = 1$ ). Once  $V_{pv}$  hits  $V_{min}$ , the set-reset flip-flop (SR-FF) resets  $V_{wc}$  and  $V_{pv}$  charges  $C_{in}$  ( $V_{wc}=0$ ).  $V_{wc}$  does not change unless  $V_{pv}$  hits one of the window boundaries ( $V_{max}$  or  $V_{min}$ ). Once  $V_{pv}$  hits  $V_{max}$ , the SR-FF sets  $V_{wc}$ , going back to the initial state.

### 2.5.4 Bias and ROSC Circuit

Besides the tracking algorithm building blocks, the chip contains some

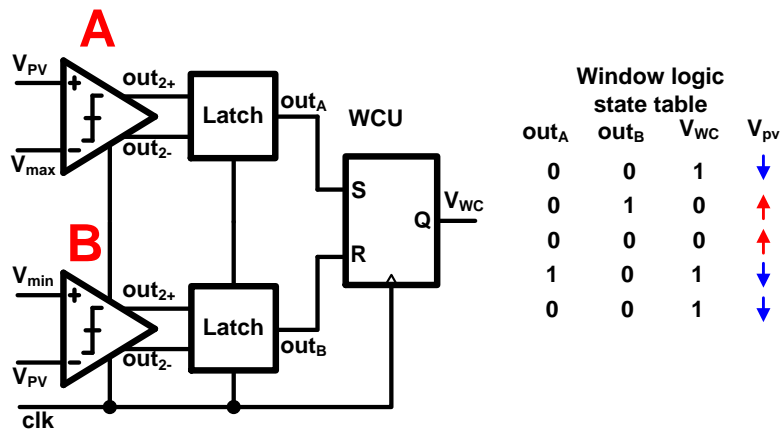


Figure 2-17. Window comparator unit configuration and window logic state table.

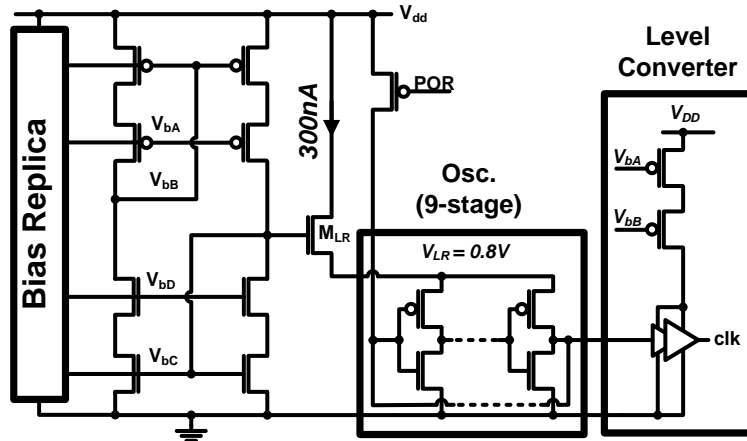


Figure 2-18. Supply-independent bias with oscillator for ultra-low power wide-swing supply operation

auxiliary circuits including a ring oscillator (ROSC) and a supply-independent bias circuit as shown in Figure 2-18. The oscillator's supply is 0.8 V regulated by an

internal line regulator and enabled by POR signal. The ring oscillator is designed with biasing current of 300 nA. The ring oscillator is followed by a level converter (Figure 2-18) with a slew rate of  $> 100 \text{ V}/\mu\text{sec}$  in the slow-slow corner. The level converter output is used by the FSM to generate the seven clock phases and the counter to sample the window logic output. The supply-independent bias is critical in order to provide a constant clock (clk) frequency used for measuring  $T_{\text{chg}}$  in DPU. If the drift in the ROSC supply is large, it will affect the accuracy of the counter output, eventually leading to insufficient  $T_{\text{chg}}$  accuracy or counter overflow. Figure 2-19 shows almost a flat curvature of the clock frequency variation across supply voltages at typical (TT), fast-fast (FF) and slow-slow (SS) corners. Moreover, the Monte-Carlo data shows a worst case ‘ $\sigma$ ’ 6.4KHz, which is affordable by the DPU design. Even though The ROSC frequency varies with temperature, it is not very critical for our application since the temperature variation is limited for PV and TEG EHS.

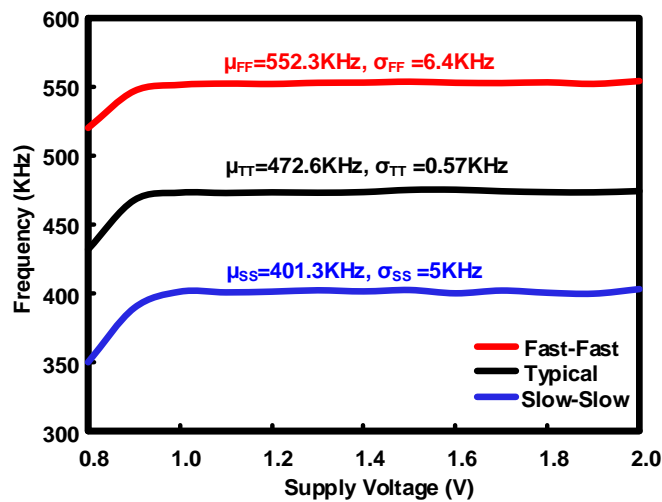


Figure 2-19. ROSC frequency variation across supply voltage at TT, FF and SS corners

## 2.6 Design Consideration in The Proposed Time-based MPPT Technique

As shown in Figure 2-20, the proposed TB-MPPT has several timing parameters ( $T_{chg}$ ,  $T_{trk}$  and  $T_{dig}$ ) defining the overall system operation.  $T_{chg}$  is the charging time,  $T_{trk}$  is discharging time, and  $T_{dig}$  represents the DPU processing time. Note that  $T_{chg}$  and  $T_{trk}$  are influenced by  $C_{in}$ . In addition, the clock (clk) frequency,  $V_{step}$ , and the DPU counter size also affect the overall system operation. In this section, we will explain how the above parameters are considered in the proposed MPPT.

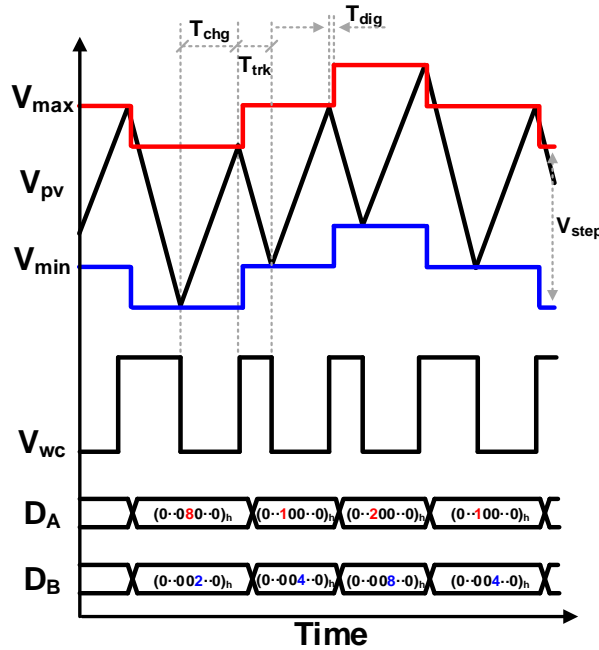


Figure 2-20. TB-MPPT overall operation waveforms

At a given  $C_{in}$ , the average charging time ( $T_{avg}$ ) should meet the following condition to avoid counter overflow:

$$T_{avg} < \frac{2^b - 1}{f_{clk}} \quad (2-8)$$

Here,  $b$  is the DPU counter size in bit,  $f_{clk}$  is the clock frequency, and  $T_{avg}$  is the average charging time with  $V_{step} = 30$  mV. Figure 2-21 illustrates the relationship between  $T_{avg}$  and  $C_{in}$  in the target irradiance range with  $f_{clk} = 500$  kHz. When  $b = 14$  bit, the margin in  $T_{avg}$  ( $T_{avg-margin}$ ) can be expressed as follows:

$$T_{avg-margin} = \frac{2^b - 1}{f_{clk}} - T_{avg} \quad (2-9)$$

The worst case  $T_{avg-margin}$  will occur at the minimum irradiance (i.e. 200 lux). A proper  $C_{in-max}$  value can be chosen using the relations in Figure 2-21. The chosen  $C_{in-max}$  value must guarantee that  $T_{dig}$  is much less than  $T_{trk}$  (Figure 2-20), to make sure that DPU ends its operation and tracking decision (i.e. increment or decrement) during the discharging phase ( $T_{trk}$ ). In this design, the worst  $T_{avg-margin}$  becomes 17 ms with  $b = 14$  bit, and  $T_{dig}$  is designed to be 100  $\mu$ s. Therefore,  $C_{in}$  and  $b$  can be relaxed. However, they are not relaxed for margins in the accuracy of the energy-time normalization process, which is limited by the division.

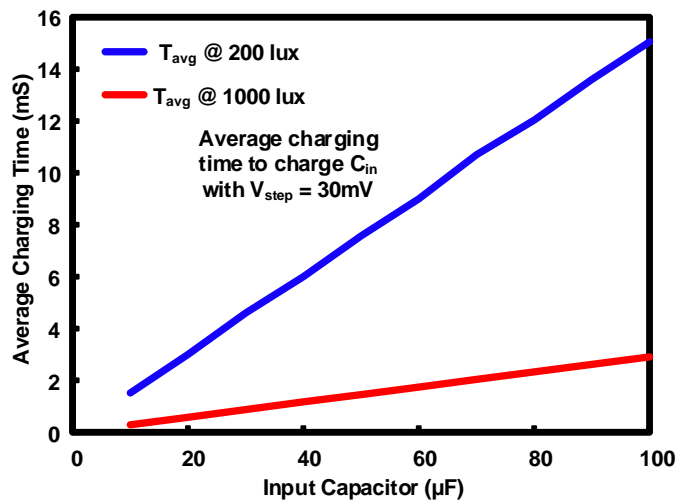


Figure 2-21. Average charging time taken to charge  $C_{in}$  with  $V_{step}$  30mV

The overall response time of the proposed TB-MPPT system is limited by the total capacitance at the  $V_{pv}$  node and the equivalent resistance seen at the  $V_{pv}$  node. The internal PV impedance and the equivalent load ( $R_{load}$ ) decide the equivalent resistance while  $C_{in}$  dominates the total capacitance due to the small nMOS switch. The value of  $C_{in}$  used in this design is 30  $\mu$ F, which dominates the response time of the system. However, when the input irradiance changes abruptly, the transient response time of the proposed TB-MPPT will degrade significantly. To address this issue, we introduce a variable gain technique in the TB-MPPT loop by controlling  $G_T$  in the barrel shift register. The DPU detects sudden input change by averaging the direction of the one-hot barrel shift register over multiple cycles. If the direction does not change over multiple cycles, it is very likely that the input irradiance changes dramatically. If this occurs, the DPU will increase  $G_T$  to reduce the response time. Once it reaches a new  $V_{mpp}$ ,  $G_T$  is set to '1' to avoid high oscillation. Figure 2-22 shows simulated  $V_{pv}$  waveforms with and without the proposed gain control when the input irradiance varies suddenly from 1000 lux to 200 lux.

At  $G_T = 1$  (i.e. one bit shifted per cycle), the response time ( $T_r$ ) is 250 ms while  $G_T = 4$  (i.e. 4-bit shifted per cycle) reduces  $T_r$  to 100 ms. The following expression explains the gain range:

$$1 < G_T < \frac{V_{step}}{V_{LSB}} \quad (2-10)$$

Here,  $V_{LSB}$  is the minimum output voltage step of the 8-bit DAC. If the gain ' $G_T$ ' becomes greater than  $V_{step}/V_{LSB}$ ,  $V_{pv}$  will lose tracking, because in this case,  $T_{dig}$  will become greater than  $T_{trk}$ , and DPU will fail to track the new  $V_{mpp}$ .

The proposed variable gain technique along with the TB\_MPPT step response is tested and demonstrated in Figure 2-23. The input irradiance changes from 1000 lux to 200 lux and vice versa. The proposed variable gain in the one-hot barrel shift register improves the system response by 3× and 5× in the falling input and the rising input, respectively. Figure 2-24, shows the transient response of the proposed TB-MPPT with  $T_{\text{start-up}} = 72\text{ms}$ .  $V_{\text{pv}}$  increases when charging  $C_{\text{in}}$  until it reaches the initial values of  $V_{\text{max}}$  and  $V_{\text{min}}$ , then the proposed TB-MPPT operation starts by tracking  $V_{\text{mpp}}$  using the  $T_{\text{chg}}$  and  $V_{\text{max}}$  information. The settling time ( $T_{\text{settle}}$ ) to reach  $V_{\text{mpp}}$  is 83 ms. MPPT operation starts with  $G_T = 1$ . After several cycles, The DPU algorithm changes  $G_T$  from 1 to 4 in order to reduce  $T_{\text{settle}}$  at steady state,  $G_T$  becomes 1 and  $V_{\text{pv}}$  oscillates around  $V_{\text{mpp}}$ .

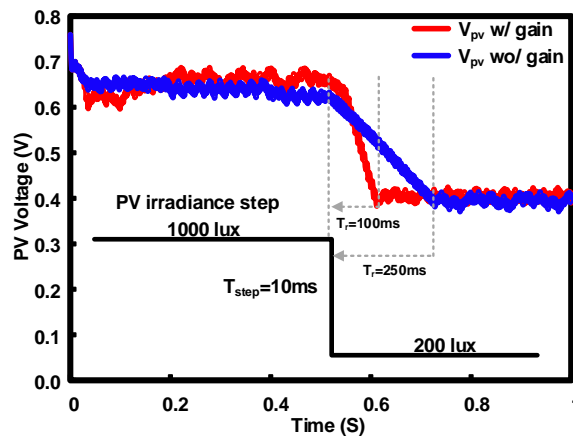


Figure 2-22. Step response to a sudden change in light irradiance from 1000 lux to 200 lux at different gain

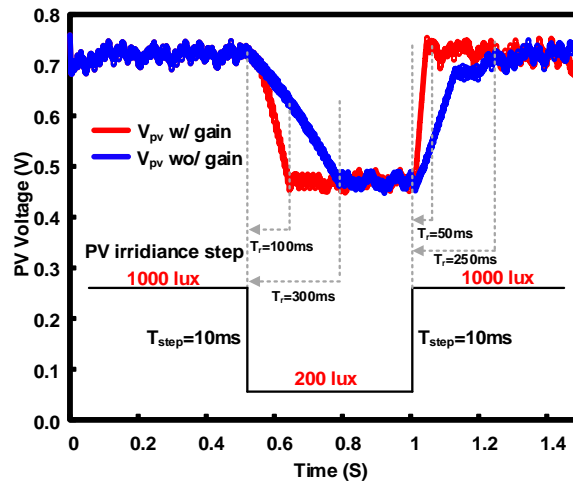


Figure 2-23. Step response for a sudden input light irradiance change

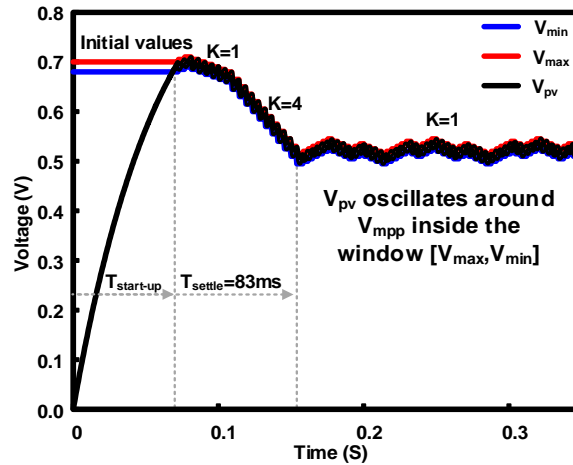


Figure 2-24. Transient response of the proposed TB-MPPT

Since harvesting from spatial temperature differences ( $\Delta T$ ) with a TEG is demonstrated in numerous literature [2, 43-46], a TEG model from Micropelt (MPG-D75100 W/mm<sup>2</sup>) [44] is deployed with the proposed TB-MPPT to proof our TB-MPPT versatility and to extend the functionality test of the proposed variable gain technique. The tracking efficiency for five modules of MPG-D751 devices is shown in Figure 2-25 for  $\Delta T$  from 1 K to 3.5 K. The recorded results are computed based on how the tested  $P_{mpp}$  deviates from the calculated one. The slight variation in the tracking efficiency across  $\Delta T$  is due to the different output power levels and the effect

of the digital division ( $V_{max}/T_{chg}$ ) accuracy at these levels over the  $\Delta T$  range under consideration. Figure 2-26 demonstrates the step response for the proposed TB-MPPT when  $\Delta T$  changes from 3 K to 2 K. The variation range is only 1 K to map the realistic scenario when used with body heat for body-area network IoT applications. The variable gain ( $G_T$ ) is tested with  $\Delta T$  variation for 1 K. At  $G_T=1$ ,  $T_r$  is 230 ms while  $G_T=4$  reduces  $T_r$  to 100 ms when  $\Delta T$  changes from 3 K to 2 K. Similarly,  $T_r$  reduces from 170 ms (i.e.  $G_T=1$ ) to 50 ms (i.e.  $G_T=4$ ) when  $\Delta T$  changes from 2 K to 3 K. The proposed TB-MPPT achieves a maximum tracking efficiency 97 %, for power levels range of 0.075 mW for  $\Delta T = 1$  K, to 0.7 mW for  $\Delta T = 3.5$  K.

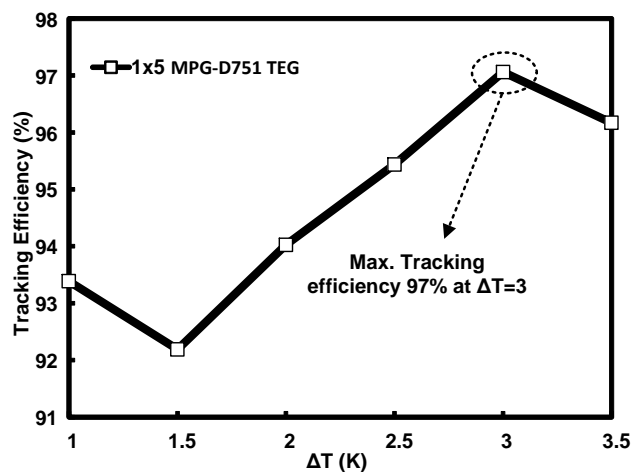


Figure 2-25. Tracking efficiency for MPG-D751 (n=5) from  $\Delta T=1$  K to 3.5 K

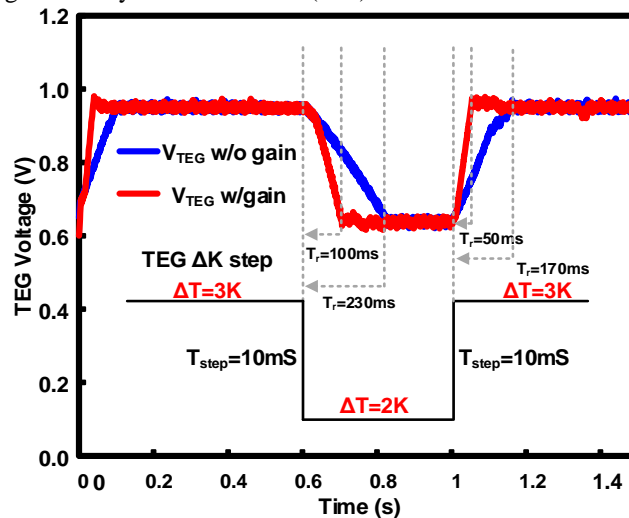


Figure 2-26. Step response waveform with and without gain for 1 K variation.

## 2.7 Measurement Results

The proposed TB-MPPT was implemented in 65 nm CMOS technology. It covers an input range from 0.4 V to 1.7 V with current consumption of 3.4  $\mu\text{A}$ . We used two PV modules, a 1 $\times$ 2 DSC PV array with an area of 9  $\text{cm}^2$  and a 2 $\times$ 2 GaAs PV array with an area of 14.5  $\text{cm}^2$ , respectively. The output current of them changes from 12  $\mu\text{A}$  (DSC at 200 lux) up to 980  $\mu\text{A}$  (GaAs at 1000 lux) [38].

Figure 2-27 and Figure 2-28 demonstrate the step response of the TB-MPPT test chip with two different operating conditions. Figure 2-27 shows  $V_{\text{pv}}$  tracking when the input light irradiation of a 1 $\times$ 2DSC cell varies between 790 lux (bright office) and 395 lux (very dim office) for indoor applications. At transition state, the WCU modulates the  $V_{\text{wc}}$  frequency until it reaches the new  $V_{\text{mpp}}$  as shown in Figure 2-27. Figure 2-28 shows the dynamic tracking as the input light irradiance of 2 $\times$ 2 GaAs cell changes from 200 lux to 1000 lux. As shown in Figure 2-27 and Figure 2-28, the proposed TB-MPPT does not depend on the PV type or any empirical relation as in FOCV; it tracks the  $V_{\text{mpp}}$  and directly supplies it to the PMC ( $R_{\text{load}}$ ). The measured tracking efficiencies under various indoor light levels are recorded in Figure 2-29 for the two different types of PV cells. The test chip achieved the tracking efficiencies ( $\eta_{\text{mpp}} = P_{\text{pv}} / P_{\text{mpp}}$ ) from 3 % at 200 lux to 96.2 % at 100 lux using the two PV cells. It also achieved the harvesting efficiency ( $\eta_{\text{hvst}} = P_{\text{stg}} / P_{\text{mpp}}$ ) up to 87 % at 1000 lux. While the GaAs PV cell has a  $K_{\text{FOC}}$ -ratio of 0.83, the organic DSC cell shows a  $K_{\text{FOC}}$ -ratio of 0.58. The above measurement results validate that the proposed MPPT algorithm shows the intended adaptive behavior not only in the range of light exposure but also in the energy harvester characteristics. This facilitates the application of the proposed TB-MPPT technique to diverse ultra-low power systems.

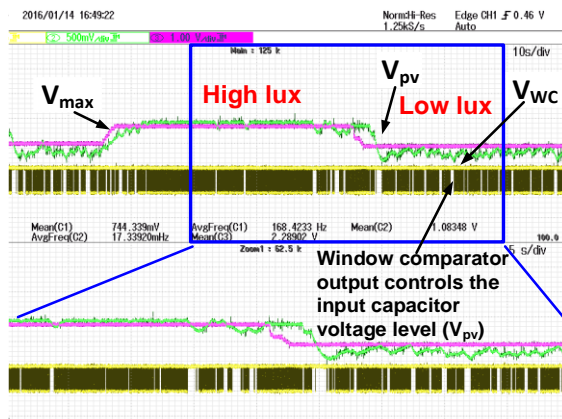


Figure 2-27. MPPT as the 1x2 DSC cell's light irradiation steps between 395 and 790 lux (indoor)

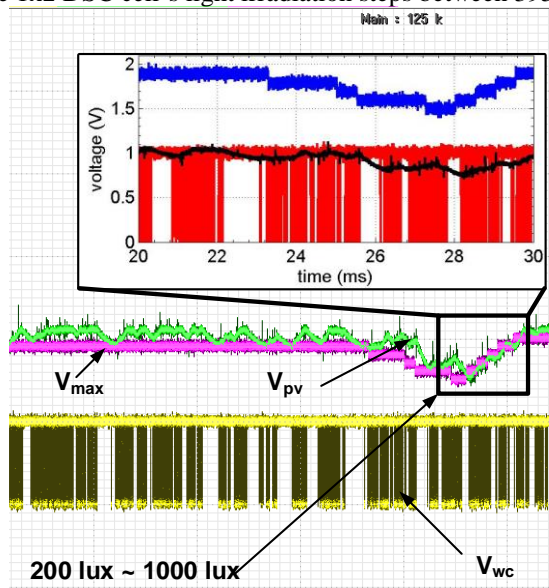


Figure 2-28. Dynamic tracking as the input light irradiance changes from 200 lux to 1000 lux

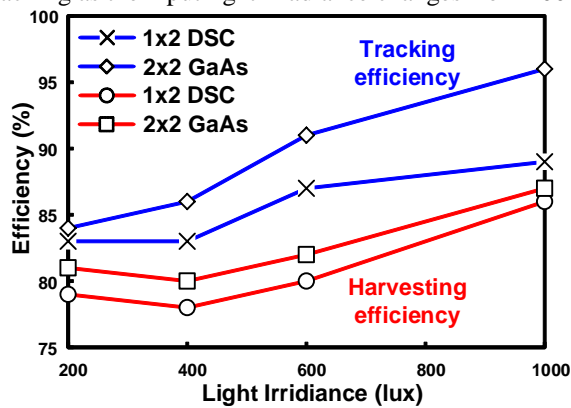


Figure 2-29. Tracking and harvesting efficiency at indoor light levels

Figure 2-30 depicts the test chip measurement setup and the microphotography. The chip has an area of  $0.187 \text{ mm}^2$ . We used a conventional boost converter to validate the proposed TB-MPPT. Table 2-I compares this work with other state-of-the-art MPPT techniques. The proposed TB-MPPT achieves the efficiency of 96% consuming only  $5.1 \text{ } \mu\text{W}$  and provides a wide input voltage range and a wide load range compared with the state-of-the-art works. Moreover, it directly supplies the maximum power from the PV cell to the charge-pump, and no reference voltage is necessary because of the dynamic generation of the window voltage by the 8-bit DAC.

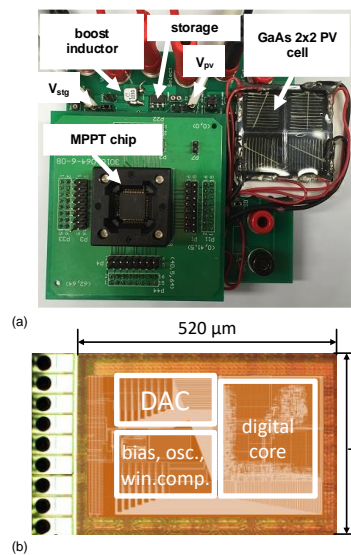


Figure 2-30. (a) measurement setup, and (b) test chip microphotography

Table 2-I. COMPARISON WITH STATE-OF-THE-ART WORKS.

	[1]	[3]	[19]	[20]	[22]	[23]	This work
Process	0.35- $\mu\text{m}$	0.35- $\mu\text{m}$	0.35- $\mu\text{m}$	0.35- $\mu\text{m}$	0.35- $\mu\text{m}$	0.18- $\mu\text{m}$	65-nm
# off-chip components	config.:8. power:11	config.: 0. power: 3	NA	NA	NA	NA	config.: 0, power: 3
Tracking sensors	I- and V-sensors	sensor-less	I- and V-sensors	V- sensor	I- sensor	sensor-less	sensor-less
MPPT scheme	analog	analog	analog	analog**	analog	digital+analog	digital
$V_{\text{hyst}}$ (V)	0.3 – 0.6	1.0 – 5.0	2.1-3.5	1-2.7	>0.6	1.1-1.5	0.4 – 1.7
$V_{\text{min,start}}$	3.3 V	1.2 V	NA	1 V	2 V	NA	0.8 V
Max. $\eta_{\text{track}}$	99%	90%	67%	86%	70%	86.4%	96%
Harvester	DC	AC	DC	DC	DC	DC	DC
$P_{\text{DD}}$	1.3 mW	4.7 $\mu\text{W}$	NA	0.45-0.85 $\mu\text{W}$	2-7 $\mu\text{W}$	0.294 $\mu\text{W}$	5.1 $\mu\text{W}$
Throughput Power	36W	NA	100-775 $\mu\text{W}$	0-80 $\mu\text{W}$	100-1000 $\mu\text{W}$	<21 $\mu\text{W}$	600 $\mu\text{W}$ at $\Delta T=3$ K 670 $\mu\text{W}$ at 1000 lux
Converter	n/a	inductor	switched capacitor	switched capacitor	switched capacitor	switched capacitor	inductor
Cold start-up	no	yes	no	no	no	yes	yes

## 2.8 Conclusion

This chapter has presented a novel time-based maximum-power-point-tracking (TB-MPPT) technique. First, it started by providing an overview on the existing MPPT techniques. Then, the proposed TB-MPPT technique, operation principle and architecture were presented and discussed. The proposed energy-to-time normalization algorithm compensates for the accuracy degradation caused by the time-based approach. A variable gain control is also implemented to boost the step response. The proposed TB-MPPT is self-adaptive without using any external references or specific configuration. Therefore, it can be applied to a wide range of DC energy harvesting devices. The test chip implemented in 65 nm CMOS technology occupies the active area of 0.187 mm<sup>2</sup>, consumes 5.1  $\mu\text{W}$ , and achieves the tracking efficiency up to 96%.

# **Chapter 3. Proposed Low Power Energy Harvesting System with a Novel Three-Dimensional MPPT For Wide Load Applications Within IoT Smart Nodes**

## **3.1 Introduction**

As mentioned in the previous chapter, following the international technology roadmap of semiconductor (ITRS) and the recent advances in integrated circuits technology, IoT smart nodes, including wearable devices, wireless electronics, and implantable sensors proliferate and increasingly become popular. Moreover, the smart nodes within IoT applications will reach nearly 50 billion connected devices by 2020 [1-4]. These smart nodes, are usually implemented as IoT SoC and includes power management circuit (PMC), energy sources, signal processing, communication blocks and sensors and/or actuators, as illustrated in Figure 1-1. Energy harvesting systems garners a considerable attention as it features energy-autonomous IoT smart nodes, and avoid the maintenance cost of recharging and/or replacement of batteries and their bulky size [1, 4-10].

Numerous energy harvesters have been studied and discussed in literature including photovoltaic (PV) [3, 5, 8, 11-14], thermoelectric generators (TEG) [15-17] and piezoelectric [18]. Among these energy scavengers, PV has gained a significant attention and popularity as an energy source for autonomous IoT SoC due to its high-power density and low cost [2]. As mentioned in the previous chapter, to maximize the solar energy being harvested, PV is connected to a DC-DC converter controlled by an MPPT, to guarantee that the system operates at its maximum efficiency. The need of

MPPT, along with the DC-DC converter rises from the harvester nature dependency and load power variability, especially at a regulated output voltage. The solar energy can be harvested using inductive based [4, 16, 19, 20] or switched capacitor-based DC-DC converter [2, 3, 5, 6, 9, 13, 14, 21]. However, the latter is a more suitable solution for fully-integrated IoT SoC, such as smart nodes and body-area-network (BAN), avoiding bulky off-chip inductors.

Many hill-climbing based MPPT principles have been exploited to maximize the converted harvested power as per load demand. Although they achieve a considerable power efficiency (PE) at 100s of  $\mu\text{A}$  output load, they suffer from a modest PE (30%~40%) when supplying 100s of nW load during idle mode. Ref [4] mentioned that the IoT sensor nodes operation profile stays more than 50% of its operation time in idle mode. Moreover, [23] shows a wireless operation scenario (Figure 3-1), that proves the former claim. It shows that the IoT wireless sensor wakes up only during the heavy-duty functions, and operates most of the time in idle or standby mode. According to [4], a typical wireless sensor node wakes up once every 60 seconds, or even more, thus, the conversion efficiency during the idle and standby

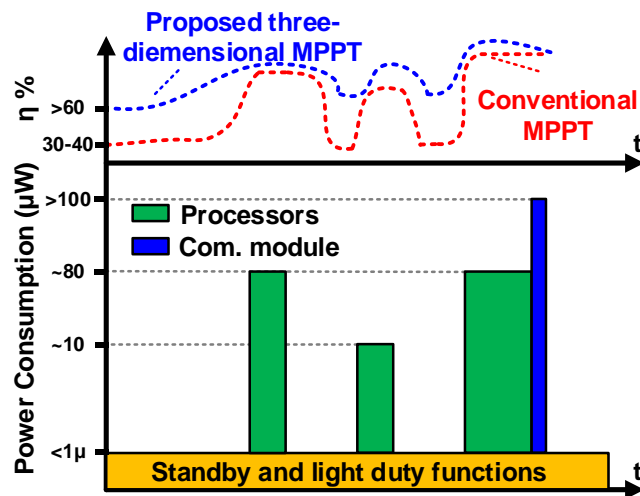


Figure 3-1. Wireless sensor operation scenario and advantage of the proposed 3D-MPPT

(i.e. light load) mode dominates the overall PE of the EHS. Therefore, high PE at ultra-light loads (i.e. 100s of nA) is crucial to avoid the degradation of the EHS PE within IoT smart nodes and implantable sensors.

The remainder of this chapter is organized as follows. An overview of the conventional hill-climbing MPPT and their conversion efficiency imitation issue at wide load applications is presented in Section 3.2. The proposed three-dimensional MPPT (3D- MPPT) along with the switch modulation technique (SWM) operation principles are discussed in Section 3.3. Section 3.4 explains the architecture and the circuit implementation of the proposed 3D-MPPT. The start-up technique, the energy-aware algorithm, and the 3D-MPPT closed-loop operation are presented in Section 3.5, followed by the measurement results in Section 3.6. Finally, Section 3.7 concludes the chapter, Chapter 3.

## **3.2 Conventional Hill-Climbing MPPT and Conversion Efficiency Limitation at Wide Load Application**

Conventionally, the hill-climbing based MPPT reported in literature utilizes conversion ratio modulation (CRM) and/or switching frequency modulation (SFM) techniques limiting their MPP tracking process to one or two dimensions. 1-D MPPT was adopted in [6] and [3] by tuning the switching frequency ( $f_{sw}$ ) and the pumping capacitor values, respectively. Although the high efficiency achieved, the associated PE is limited to 40% at light load ( $<1 \mu A$ ). Moreover, the large area occupied by the capacitor bank in [3] make it less cost-efficient while the lack of a reconfigurability in [3, 6] induces charge redistribution loss (CRL), degrading the PE. Ref [2] introduces a

2-D MPPT by employing the CRM and SFM using a hysteresis control technique to achieve a peak PE of 89%. However, as the output load goes below  $1 \mu\text{A}$ , the PE decreases to less than 50%. The PE limitation of the conventional MPPT is due to the fixed transistor sizes for the DC-DC converter across a wide load range. Figure 3-2 shows the simulated 2X serial-parallel SCCP (SP SCCP) power consumption distribution at idle and heavy-duty operation modes. To analyse the PE limitation issue, a simulation is carried out assuming  $I_{\text{out}}$  equals to  $500 \text{ nA}$  and  $200 \mu\text{A}$  at idle and heavy-duty mode respectively. The simulation results show that the PE limitation issue, across a wide load range, stems from two facts: (i) at heavy-duty modes large

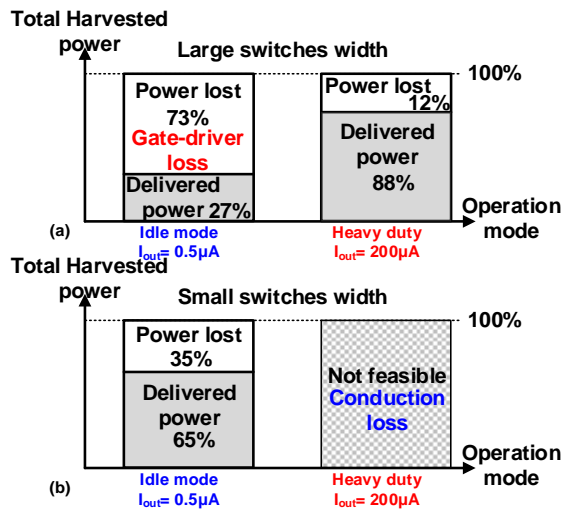


Figure 3-2. Simulated power distribution of a 2X SCCP at idle and heavy operation modes with (a) large transistor width and (b) small transistor width

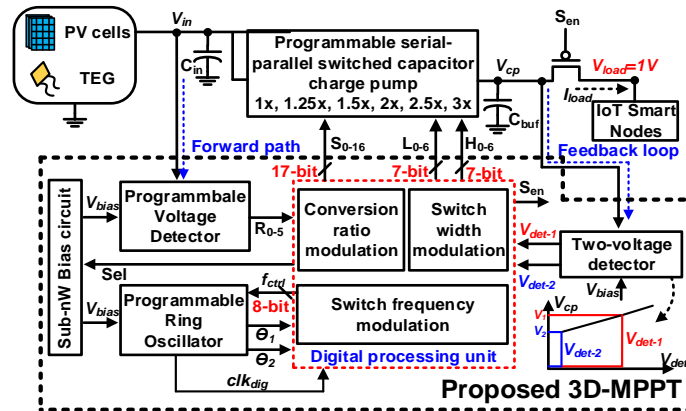


Figure 3-3. Proposed energy harvesting system and 3D-MPPT architecture

transistors are preferable to avoid conduction loss while (ii) at idle scenarios ( $<1\mu\text{A}$ ) small transistors are required, to avoid gate driver loss.

In this work, a reconfigurable SP SCCP and a novel  $V_{gs}$  dependent SWM technique are incorporated into the MPPT procedure along with the SFM and CRM techniques resulting in a 3D-MPPT (Figure 3-3). The proposed fully-integrated 3D-MPPT eliminates the gate-driver/conduction loss trade-off by configuring the SP SCCP transistors width with proportion to the load condition and the input voltage applied (i.e.  $V_{gs}$ ). In addition, the proposed 3D-MPPT is self-adaptive and compatible with various DC energy harvesters' type, such as PV and TEG. Therefore, an energy-aware algorithm is proposed to accommodate multiple harvester inputs, and connect the one with enough energy to the implemented SP SCCP. Finally, the proposed 3D-MPPT improves the PE by at least 20% in the sub- $\mu\text{W}$  load power compared with the conventional MPPT designs, with peak PE of 88% at heavy loads, using ultra-low power control blocks. The proposed 3D-MPPT covers an output power range from 100 nA to 0.3 mW.

### **3.3 Proposed 3D-MPPT Operation Principle and Algorithm**

The main idea of a hill-climbing MPPT is to condition the DC-DC converter equivalent impedance ( $R_{cp}$ ) to minimize the internal losses and transfer the maximum possible amount of the energy being harvested to the load. In that aspect, the proposed 3D-MPPT presents a novel hill-climbing technique to improve the PE across a wide output load range. This section, (Section 3.3) discusses the proposed 3D-MPPT tracking process including the principle behind the proposed SWM technique.

Afterward, a novel  $V_{gs}$  dependent SWM technique, for a further PE improvement, along with the tracking algorithm are presented and discussed.

### 3.3.1 3D-MPPT Tracking Principle

The trade-off between the gate-driver and conduction loss rises at wide load applications within IoT smart nodes that demand 100s of nA to 100s of  $\mu$ A depending on the operating mode. More specifically, the SCCP internal losses including conduction loss and gate driver loss depend on the transistors width and the  $f_{sw}$  at a given operating condition. The PE, in this case, can be expressed as follow:

$$PE = \frac{(N * V_{in} - \Delta V_d) * I_{load}}{N * V_{in} * I_{load} + P_g} \quad (3-1)$$

$$\Delta V_d \propto \frac{N * I_{load}}{1/R_{cp}} \propto \frac{N * I_{load}}{C_{fly} * f_{sw}} \quad (3-2)$$

where  $\Delta V_d$  is the drop voltage across the SCCP due to conduction loss and defined by (3-2),  $C_{fly}$  and  $N$  are the SCCP flying capacitance and conversion ratio, respectively.

$P_g$  is the gate driver loss, and it is defined as follow:

$$P_g \propto C_{sw} V_{gs}^2 f_{sw} \quad (3-3)$$

where  $C_{sw}$  is the transistor gate capacitance and  $V_{gs}$  is applied swing voltage per switch.

At heavy load scenarios,  $P_g$  is far less than  $N * V_{in} * I_{load}$  [67], and can be neglected. In this case, PE can be improved by reducing the conduction loss that arises from the charging and discharging of  $C_{fly}$  through the SCCP switches and limited by  $\Delta V_d$ . According to (3-2), modulating  $f_{sw}$  with  $I_{load}$  and  $N$  variations reduces  $\Delta V_d$ , hence, improving the PE. For a further PE improvement, large SCCP transistors with small  $R_{on}$  are required, to minimize the  $R_{cp}$  and hence minimizing  $\Delta V_d$ .

At light load and idle conditions,  $P_g$ , generated from the switching of  $C_{sw}$  within the SCCP, dominates and significantly decreases the PE (Figure 3-2). There are various means to reduce  $P_g$ . The SFM technique reduces  $f_{sw}$  with  $I_{load}$ , and hence reduces  $P_g$ . However, the effect of this technique on the PE reduces at ultra-light load condition, where  $P_g$  dominates the losses as shown in Figure 3-2 where SFM was already applied. Therefore,  $P_g$  can be further reduced by decreasing the  $C_{sw}$  associated with each SCCP transistor, thus increasing  $R_{cp}$ .

In fact, according to (3-2) and (3-3), assuming same  $V_{in}$ ,  $R_{cp}$  requirements differ across the load range. Large SCCP transistors with small on-resistance ( $R_{on}$ ) and consequently small  $R_{cp}$  are required to maintain regulation and minimize the conduction loss at heavy load conditions. While at light load scenarios, using small transistors with large  $R_{on}$  and reduced  $C_{sw}$  are enough to maintain regulation and reduce  $P_g$ .

Therefore, the proposed 3D-MPPT employs a novel  $V_{gs}$  dependent SWM technique together with SFM and CRM (i.e. three-dimensional tracking process) to improve the PE at idle and heavy load conditions. The basic idea is to modulate the implemented SCCP transistors width in proportion to  $I_{load}$  and  $V_{in}$  values, along with the  $f_{sw}$  and the 'N' to minimize the internal losses, boosting the PE across wide input voltage and output load range. The proposed 3D-MPPT algorithm will be discussed in the next section (Section 3.3.2).

### **3.3.2 $V_{gs}$ Dependent SWM Tracking Algorithm**

Basically, the proposed SWM technique varies the SCCP transistors width (i.e.  $R_{on}$ ) and hence  $R_{cp}$  according to the load condition, to minimize the conduction loss

and  $P_g$  at heavy and light load operating modes, respectively, enhancing the PE across a wide load range. According to (3-3),  $P_g$  can be significantly reduced by an additional proportional transistors width optimization with relative to the  $V_{gs}$  applied. In addition, the transistor  $R_{on}$  varies with  $V_{gs}$  at the same width ( $W$ ) due to the SCCP transistors linear characteristics, as follows:

$$R_{on} \approx \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{th})} \quad (3-4)$$

Utilizing this information for MPPT, the proposed SWM technique optimizes the SCCP transistors width (i.e.  $R_{on}$ ) proportionally with (i)  $I_{load}$ , and (ii) applied  $V_{in}$  which determines  $V_{gs}$ . Figure 3-4 describes the proposed 3D-MPPT operation principle. The  $I_{load}$  condition is sensed by analyzing the time domain of a voltage detectors circuit output pulses ( $V_{det-1}, V_{det-2}$ ) through a feedback path. While  $V_{in}$  range is detected using a programmable voltage detector (PVD) through a forward path. A simple time-to-digital converter (TDC) and two digital registers ( $f_{ctrl}$  and CR) are developed so that  $I_{load}$  condition and  $V_{in}$  detected range can be, digitally, stored. Then, a digital core sets ' $f_{sw}$ ' and ' $N$ ' using  $f_{ctrl}$  and CR digital values, respectively. This has two benefits. Firstly, ' $f_{sw}$ ' and ' $N$ ' can be used by the SWM technique to optimize the SCCP transistors width as indicators for  $I_{load}$  and  $V_{in}$  respectively. Secondly, low-complex operation and low power implementation are feasible, since the SWM can be adopted in the digital domain.

Since the SWM optimization depends on  $V_{gs}$  per each transistor, the SP SCCP switches shown in Figure 3-5 are divided into two types: (i) low side transistors ( $P_{LS}$ ), with  $V_{gs}$  almost equals  $V_{in}$  and (ii) high side transistors ( $P_{HS}$ ) with  $V_{gs}$  equals  $V_{cp}$ , which is regulated and equals 1V. Thus, the  $P_{LS}$  size ( $W_{LS}$ ) is modulated in proportion to  $f_{sw}$

together with  $V_{in}$ , while  $P_{HS}$  size ( $W_{HS}$ ) is proportionally modulated with  $f_{sw}$  only, due to its constant  $V_{gs}$ . Following the flow chart in Figure 3-6,  $f_{sw}$  and  $N$  are stored digitally into 6-bit  $f_{ctrl}$  and 3-bit CR signals, respectively. Initially, CR and  $f_{ctrl}$  are loaded with their initial values. First, if the sensed  $I_{load}$  is increasing, the 3D-MPPT algorithm increments  $f_{ctrl}$  and proportionally widens  $P_{LS}$  and  $P_{HS}$ . Likewise, when  $I_{load}$  decreases, indicating a lighter load demand, the 3D-MPPT algorithm decrements  $f_{ctrl}$  and proportionally decreases the  $P_{LS}$  and  $P_{HS}$  width. Second, to maintain regulation and low CRL, CR is modulated inversely with  $V_{in}$  for a regulated  $V_{cp}$  equals 1 V. As shown in Figure 3-6,  $f_{ctrl}$  and CR are used to update the  $P_{LS}$  size, while  $P_{HS}$  size is updated only according to  $f_{ctrl}$ . Thus, the proposed SWM technique is triggered simultaneously with CRM (case-3), or with SFM (case 2), or with both (case-1), as described in Figure 3-7.

In conclusion, the proposed 3D-MPPT track the MPP by conditioning  $R_{cp}$  using  $N$  (CRM),  $f_{sw}$  (SFM) and  $[W_{HS}, W_{LS}]$  (SWM) at each operating point defined by the pair  $\{I_{load}, V_{in}\}_{cc}$ . Figure 3-8 illustrates the proposed 3D-MPPT tracking process at two different operating points  $\{I_{load}, V_{in}\}_{1/2}$ . Initially, at  $\{I_{load}, V_{in}\}_1$ , the optimum  $R_{CP}$  ( $R_{cp-opt1}$ ) is tracked by adjusting (i) 'N' according to the detected  $V_{in-1}$  and (ii) ' $f_{sw}$ ' according to the sensed  $I_{load-1}$ . Then,  $W_{LS}$  and  $W_{HS}$  are updated in proportional to the adapted  $N$  and  $f_{sw}$  (A to D in Figure 3-8). At point 'D' in Figure 3-8, the tracking algorithm realized a decrease in PE by analyzing  $V_{det-1/2}$ , so it locks the MPPT process at 'C'. When the operating point varies to  $\{I_{load}, V_{in}\}_2$ ,  $R_{cp-opt2}$  is tracked from the last achieved

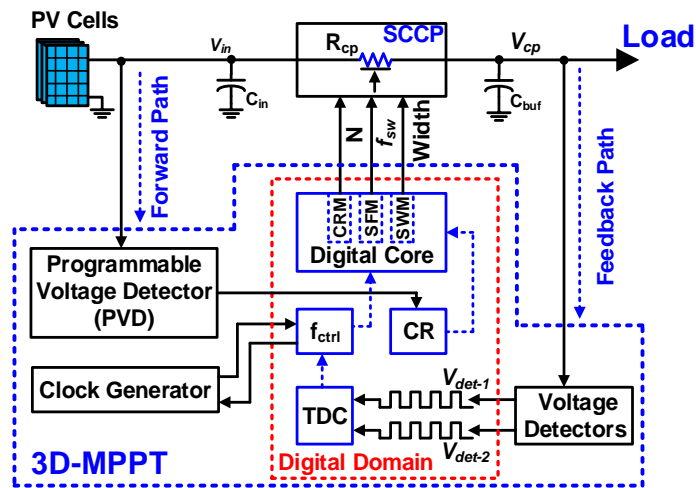


Figure 3-4. Proposed three-dimensional maximum power point tracking behavioral diagram for PV cells

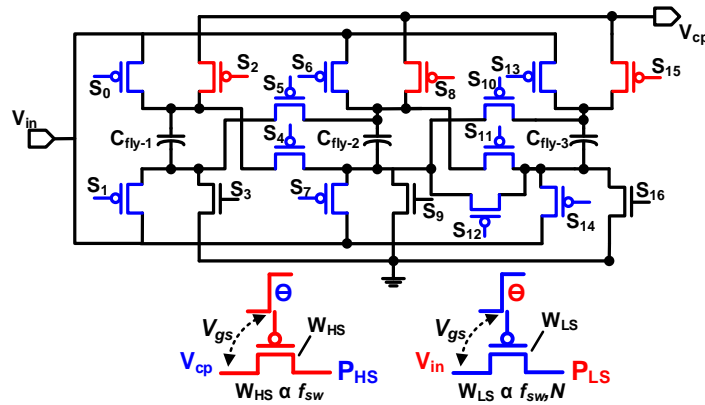


Figure 3-5. Serial-parallel switches capacitor charge pump circuit architecture

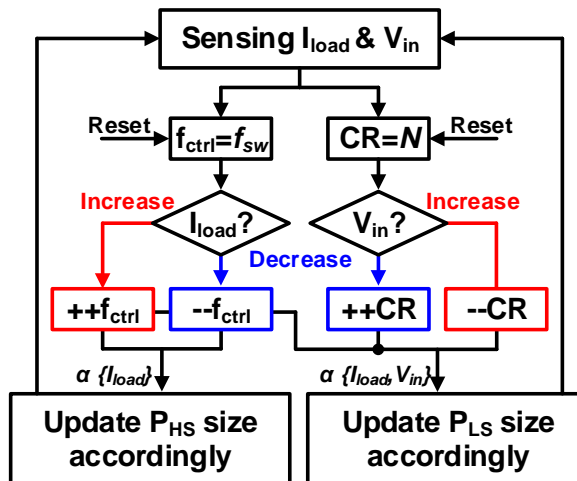


Figure 3-6. Proposed three-dimensional MPPT flow-chart

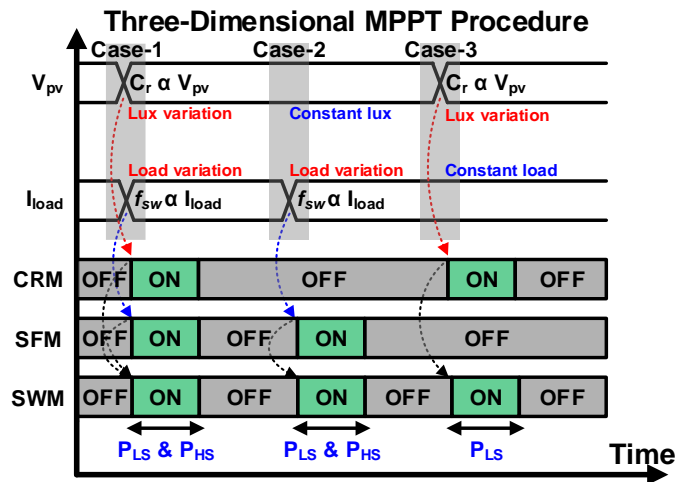


Figure 3-7. The proposed 3D-MPPT operation at different cases

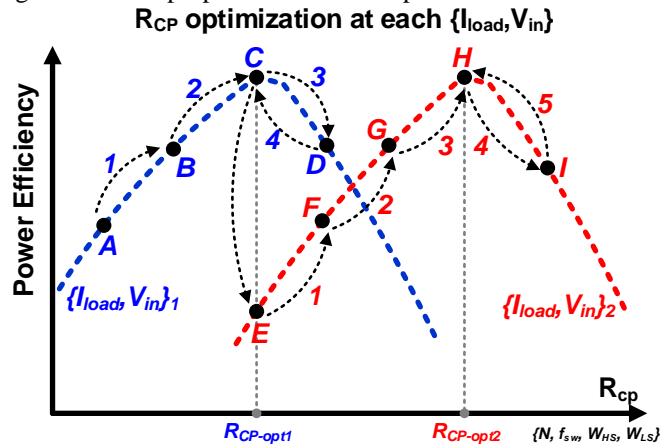


Figure 3-8. Three-dimensional MPPT tracking for  $R_{cp}$  optimization per operating point  $\{I_{load}, V_{in}\}$

$R_{cp-opt}$  as shown in Figure 3-8 (C to H) without the need of re-tuning the  $f_{sw}$  or  $N$  as in [7], making the tracking response faster. The time-to-digital conversion is employed using digital counters and edge detectors, while the PVD detects  $V_{in}$  range without the need of any reference voltages, make it an adequate solution for self-sustained, autonomous and low-power EHS within IoT smart nodes. A detailed study of the 3D-MPPT architecture including the  $I_{load}$  sensing process and the TDC will be presented in the next section (Section 3.4).

### 3.4 Proposed 3D-MPPT Architecture and Circuit Implementation

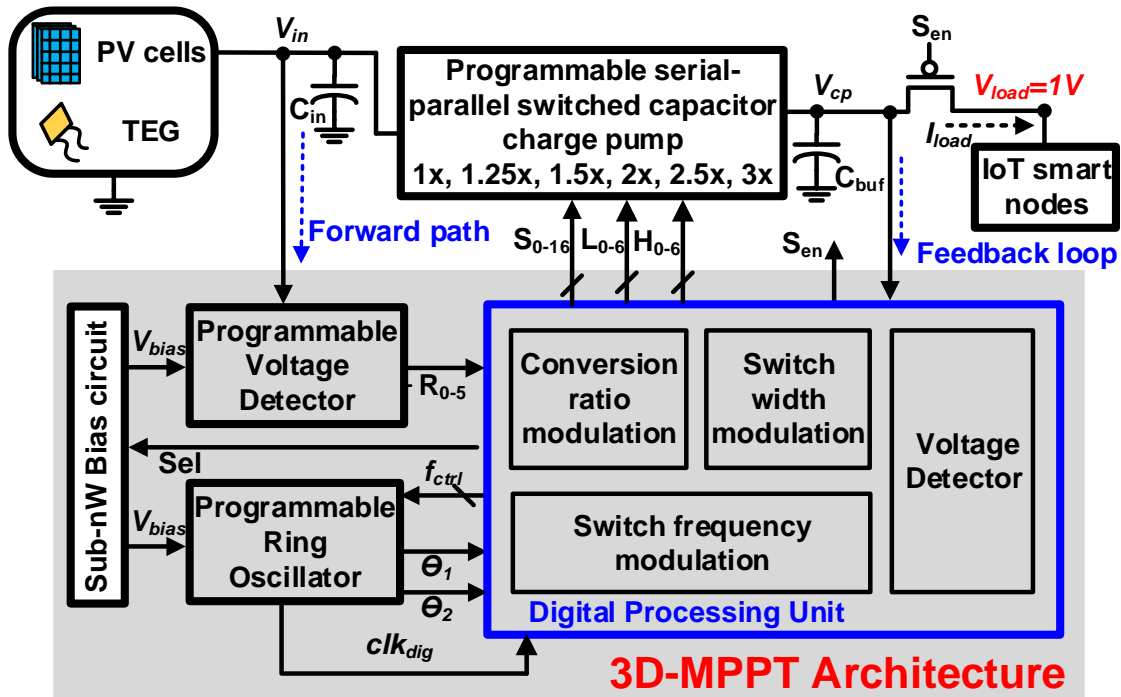


Figure 3-9. Proposed 3D-MPPT system architecture

Figure 3-9 illustrates the proposed EHS along with the novel 3D-MPPT architecture. The proposed EHS harvests solar energy to provide a regulated output voltage (1 V). It is composed of a forward path (FWP) and a feedback path (FBP). The FWP features a continuous  $V_{in}$  range detection, to set the proper SP SCCP conversion ratio. While  $I_{load}$  is sensed using the FBP, to establish the SP SCCP fsw, WHS and WLS accordingly. The proposed 3D-MPPT shown in Fig. 9 consists of five main blocks, namely a reconfigurable SP SCCP, the digital processing unit (DPU) where the proposed 3D-MPPT tracking algorithm runs, PVD to detect the  $V_{in}$  range, ultra-low-power 4T reference circuits, and finally a programmable ring oscillator (PROSC) to generate clock signal for the DPU, SP SCCP and PVD.

### 3.4.1 Serial-Parallel Switched Capacitor Charge Pump

To accommodate a wide input range, a reconfigurable SP SCCP is developed (Figure 3-5). By manipulating the SP SCCP configuration using  $S_{0-16}$ , the implemented SP SCCP can boost  $V_{in}$  with six different N: 1X, 1.25X, 1.5X, 2X, 2.5X and 3X. The SP SCCP configuration at each N is shown in Figure 3-10. The CRM sets the proper N according to the detected  $V_{in}$  range using the PVD. The serial-parallel configuration for  $V_{in}$  boosting can provide multiple N with a fewer number of  $C_{fly}$ , making it an adequate solution to cover a wide input range with low silicon area.

Figure 3-11 shows the  $P_{HS}$  and  $P_{LS}$  segmentation architecture.  $P_{HS}$  and  $P_{LS}$  are divided into smaller transistors connected in parallel. The total width of  $P_{HS}$  ( $W_{HS}$ ) and

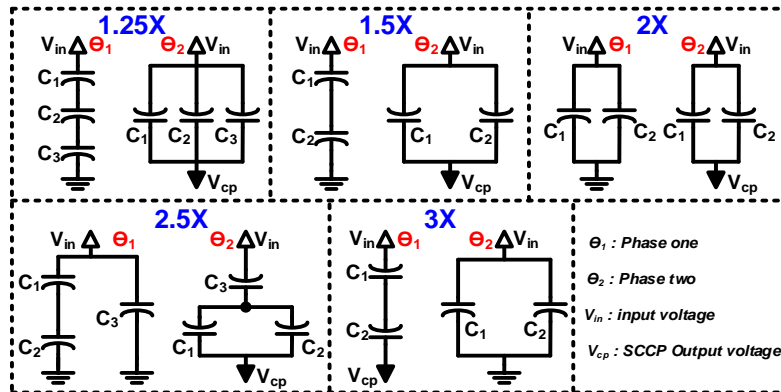


Figure 3-10. SP SCCP configuration at each N

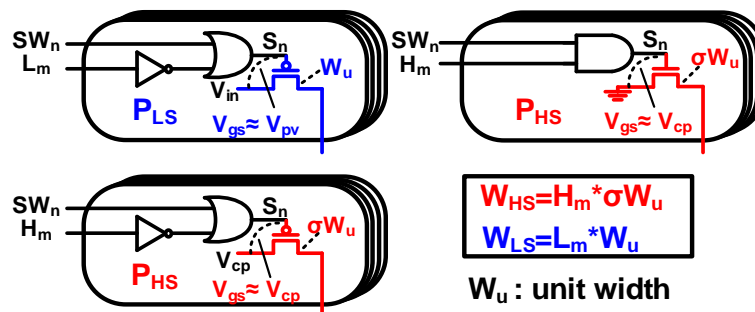


Figure 3-11. SP SCCP transistors segmentation for PHS and PLS

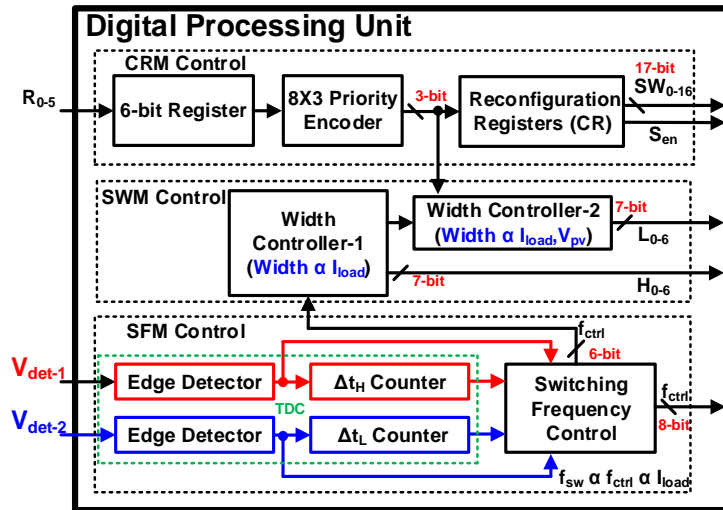


Figure 3-12. Digital processing unit (DPU) with SFM, CRM and SWM control block diagram

$P_{LS}$  ( $W_{LS}$ ) is defined by the digital control signals  $H_{0-6}$  and  $L_{0-6}$  respectively (Figure 3-11). Since  $V_{cp}$  is greater than  $V_{in}$ ,  $W_{HS}$  is less than  $W_{LS}$  by a proportional fraction ‘ $\sigma$ ’.

### 3.4.2 Digital Processing Unit (DPU)

Figure 3-12 illustrates the DPU architecture. It consists of three main control blocks that execute the proposed 3D-MPPT algorithm, namely, CRM, SFM and SWM control.

#### 3.4.2.1 CRM Control Block

It utilizes a 6-bit digital signal ( $R_{0-5}$ ) received from the PVD, holding the  $V_{in}$  range information. Then, it is encoded and stored in a 3-bit reconfiguration register (CR) (Figure 3-4), as explained by the timing diagram depicted in Figure 3-13 (a). The SP SCCP switch configuration ( $S_{0-16}$ ) depends on the digital value stored in CR to set a proper ‘N’, avoiding CRL, and hence, improving the PE across a wide  $V_{in}$  range.

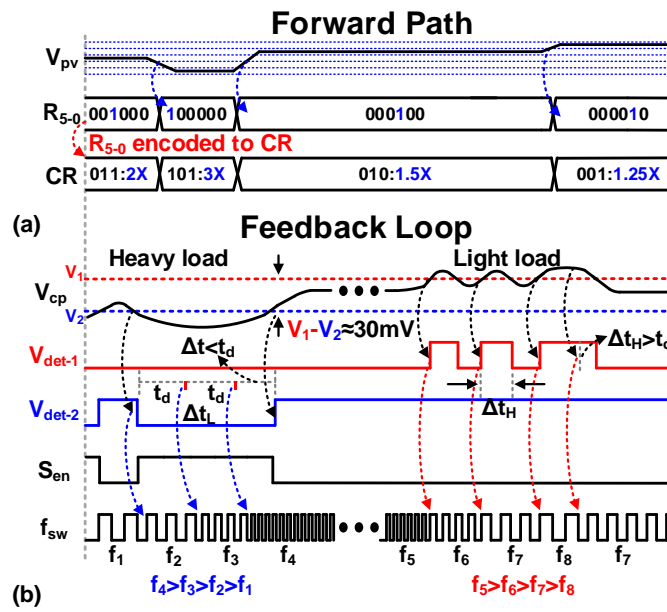


Figure 3-13. Timing diagram for the digital processing unit (a) with the forward path, (b) and feedback loop

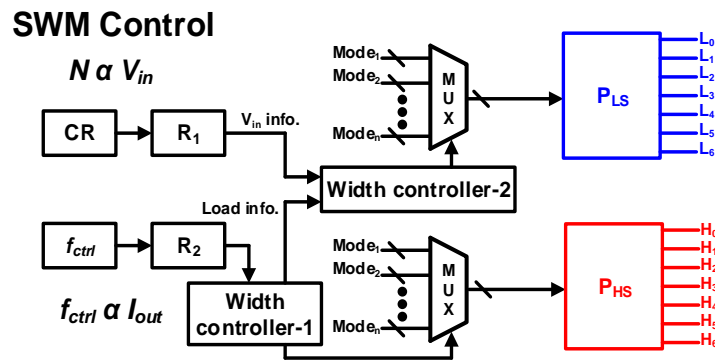


Figure 3-14. Block diagram for the proposed switch width modulation technique

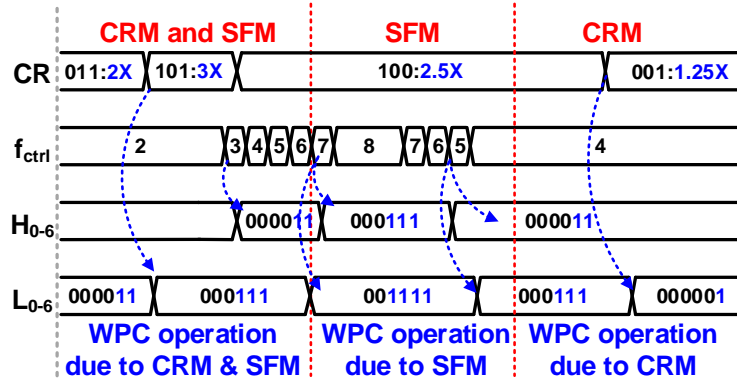


Figure 3-15. Timing diagram of the proposed switch width modulation technique

### 3.4.2.2 SFM Control Block

It adopts a newly event-time driven technique responsible for sensing  $I_{load}$ , setting  $f_{sw}$  and maintaining regulation. The proposed SFM technique is developed using two voltage detectors, that keep  $V_{cp}$  regulated between  $V_1$  and  $V_2$  ( $V_2 < V_{cp} < V_1$ ), a TDC to identify  $I_{load}$  condition and a PROSC to generate  $f_{sw}$  proportionally. Following the timing diagram in Figure 3-13 (b), at heavy  $I_{load}$  demand,  $f_{sw}$  increments one step per each  $V_{det-2}$  negative edge (event-driven), demonstrating a  $V_{cp}$  droop ( $V_{cp} < V_2$ ). However, a one-step increase may not be enough in case of a large  $I_{load}$  step. Thus, a TDC is employed to further increase  $f_{sw}$  ' $\Delta t_L/t_d$ ' steps if the  $V_{det-2}$  low time ( $\Delta t_L$ ) exceeds a predefined time ( $t_d$ ) (time-driven). In like manner,  $f_{sw}$  decrements per each  $V_{det-1}$  positive edge (i.e.  $V_{cp} > V_1$ ) indicating lighter load condition (event-driven). However, if  $V_{det-1}$  high time ( $\Delta t_H$ ) exceeds  $t_d$ ,  $f_{sw}$  further decrements by ' $\Delta t_H/t_d$ ' steps. The event-time driven technique is realized by edge detectors to detect  $V_{det-1/2}$  edges direction, and digital counters to calculate  $\Delta t_H$  and  $\Delta t_L$  as shown in Figure 3-12. Finally, the SFM control block modulates the  $f_{sw}$  according to the sensed  $I_{load}$  condition, as described, by controlling a PROSC using an 8-bit  $f_{ctrl}$  digital signal.

### 3.4.2.3 SWM Control Block

It optimizes the SP SCCP transistors size using  $L_{0-6}$  and  $H_{0-6}$  for  $P_{LS}$  and  $P_{HS}$  respectively (Figure 3-12). Figure 3-14 shows the SWM control block diagram.  $L_{0-6}$  is defined by two width controllers. They use the CR and  $f_{ctrl}$  stored in  $R_1$  and  $R_2$  respectively to proportionally optimize  $P_{LS}$  size with  $I_{load}$  and  $V_{in}$  (i.e.  $V_{gs}$ ) through a mode selector multiplexor and a 7-bit FFs. While  $H_{0-6}$  is only defined by one width controller, as shown in Figure 3-12, since  $P_{HS}$   $V_{gs}$  always equals  $V_{cp}$ . Likewise, the width controller-1 proportionally optimizes  $P_{HS}$  size with  $I_{load}$  through  $f_{ctrl}$  stored in  $R_2$ .

The timing diagram shown in Figure 3-15 explains the proposed SWM technique along with the SFM and CRM.  $L_{0-6}$  is updated with the CR and  $f_{ctrl}$  variations, while  $H_{0-6}$  is updated only with  $f_{ctrl}$ .

### 3.4.3 Programmable Voltage Detector

The proportional modulation scheme of the SP SCCP transistors size with  $I_{load}$  varies according to  $V_{in}$  that defines the  $V_{gs}$  applied per transistor. Furthermore, to maintain regulation ( $V_2 < V_{cp} < V_1$ ), and detect the load condition,  $V_{cp}$  must be continuously monitored. Conventionally, power-hungry blocks were used for this purpose such as voltage and current sensors [41], or a bandgap reference and a comparator [7, 8], increasing the power overhead. Thus, make it unsuitable for micro-energy harvesting systems [38]. In the proposed 3D-MPPT, both the output and input voltages need to be detected for CRM, SFM, and SWM. The key building block in this scheme is the ultra-low PVD (Figure 3-9).

Since the voltage detectors load the input and output nodes, low power operation is required. To fulfill this requirement a modified CMOS PVD version of the one presented in [28, 34, 65] is proposed with  $\approx 2nW$  power consumption to monitor  $V_{cp}$  voltage level and detect  $V_{in}$  range. The implemented PVD is a reference-less circuit with two inputs ( $V_{bias}, V_{in}$ ) (Figure 3-16), eliminating the need for bandgap circuit and power-hungry comparators or voltage and current sensors.

Figure 3-17 shows the circuit schematics of the proposed PVD (Figure 3-17.a) and the one implemented in [28] (Figure 3-17.b). The implemented voltage detector schematic has been modified from the one proposed in [28, 34], by connecting  $M_1$  to  $V_{bias}$  for programmability. As described in [34],  $V_{detect}$  is defined as  $V_{in}$  when the

voltage detector output turns from 0 to 1, and that happens when  $I_{M1}$  equals  $I_{M2}$  as follows (assuming  $V_{ds} > 100$  mV):

$$I_o \frac{w_1}{l_1} e^{\frac{V_{detect}-V_{bias}-V_{th1}}{mV_T}} = I_o \frac{w_2}{l_2} e^{\frac{-V_{th2}}{mV_T}} \quad (3-5)$$

Where  $m$  is the subthreshold coefficient,  $V_T$  is the thermal voltage and  $V_{th1}$  and  $V_{th2}$  are the  $V_{th}$  of  $M_1$  and  $M_2$  respectively. Assuming same  $m$  and  $V_{th}$  for  $M_1$  and  $M_2$  and by solving (3-5),  $V_{detect}$  can be given by:

$$V_{detect} = V_{bias} + mV_T \ln \frac{w_2 l_1}{w_1 l_2} \quad (3-6)$$

Thus, from (3-6), by varying  $V_{bias}$ , at a given  $w_2 l_1 / w_1 l_2$ , the proposed PVD can detect five different ranges of  $V_{in}$  as described in Figure 3-13 (a). Even though  $V_{detect}$  is proportional to temperature, it is not very critical for our application since the temperature variation is limited for PV and TEG EHS. However, the simulation results show a temperature-variation tolerance of 1 mV/°C in 0°C to 60°C and a 4mV variation across process variation.

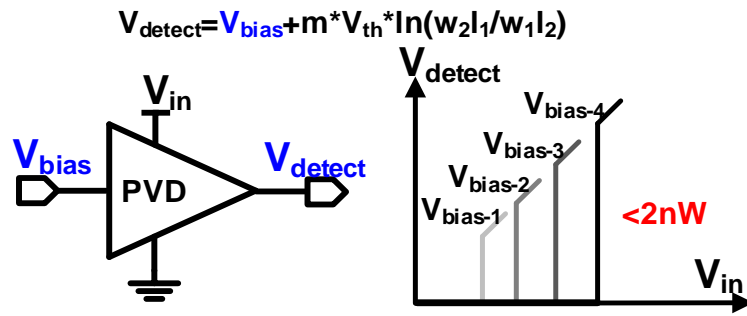


Figure 3-16. Output illustration for the proposed PVD at different  $V_{\text{bias}}$

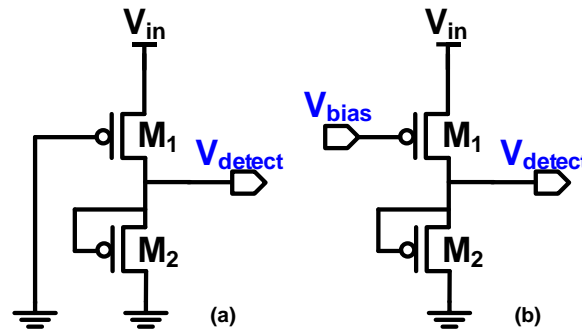


Figure 3-17. Circuit schematic of the (a) conventional voltage detector [28] and (b) the PVD proposed for the 3D-MPPT

### 3.4.4 Programmable Ring OSC (PROSC)

It is a conventional 11-stages current-starved ring oscillator followed by 9-FFs so that the clock could be divided up to ' $f_{\text{clk}}/512$ '. The frequency generated ( $f_{\text{clk}}$ ) is defined by an 8-bit control signal ( $f_{\text{ctrl}}$ ), (Figure 3-12) set by the DPU. The proposed PROSC shows a two-dimensional programmability using: (i)  $V_{\text{bias}}$  which is defined by the most significant 4 bits of  $f_{\text{ctrl}}$  signal, and (ii) the divided ratio ( $D_{\text{R}}=2^b$ ) which is selected using the least significant 4 bits of  $f_{\text{ctrl}}$ .

PROSC is designed to generate  $f_{\text{sw}}$  from 19 KHz to 16 MHz by altering  $V_{\text{bias}}$  and ' $D_{\text{R}}$ ' values (Figure 3-9) using  $f_{\text{ctrl}}$  signal, extending the supported load range.

### 3.4.5 4T Bias Circuit

An ultra-low power 4T voltage reference followed by a diode connected pMOS voltage divider, to afford multiple  $V_{bias}$  values, is employed to bias PVD and PROSC for their programmability scheme (Figure 3-9). The designed 4T reference circuit consumes 200pW at 1V as a voltage supply. With LVT and HVT pMOS devices, the process variation is about 0.5% and 2.3% for temperature variation (0°C-60°C). These numbers are acceptable for energy harvesting application, plus, the range of temperature is adequate for the applications of interest, as the temperature is not supposed to drift away from this range. Figure 3-18 shows the schematic of the proposed 4T voltage reference along with the Monte Carlo data. In [28], a 2T voltage reference was used for another type of voltage detector, however, as the reference voltage required is around 590 mV, 4T reference voltage circuit was used. The design equation that defines  $V_{ref}$  can be deduced by equating the subthreshold currents of  $M_1$  and  $M_2$ , as follow:

$$I_o \frac{w_1}{l_1} e^{\frac{V_{ref}-V_{th1}}{m_1 V_T}} = I_o \frac{w_2}{l_2} e^{\frac{-V_{th2}}{m_2 V_T}} \quad (3-7)$$

So, by rearranging (3-7),

$$e^{\frac{V_{ref}-V_{th1}}{m_1 V_T} + \frac{V_{th2}}{m_2 V_T}} = \frac{w_2 l_1}{w_1 l_2} \quad (3-8)$$

where  $m_1$  and  $m_2$  are the subthreshold slopes of  $M_1$  and  $M_2$  respectively. The temperature dependent term  $V_T$  can be eliminated by equating the right-hand side of (3-8) to 1, in other words, by designing  $M_1$  and  $M_2$  so that  $\frac{w_2 l_1}{w_1 l_2}$  equals 1, so that  $V_{ref}$  can be calculated as following:

$$V_{ref} \approx V_{th1} - \frac{m_1}{m_2} V_{th2} \quad (3-9)$$

Likewise,  $V_{\text{bias}}$ , which is a boosted version of  $V_{\text{ref}}$  by adding  $M_3$  and  $M_4$ , can be deduced using the same design equations of  $V_{\text{ref}}$ .

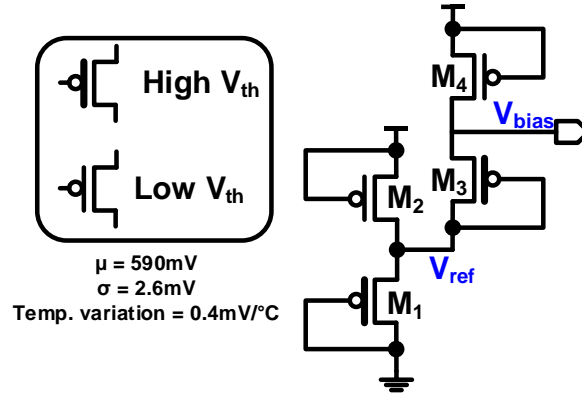


Figure 3-18. Circuit schematic of the 4T voltage reference along with its Monte Carlo data

### 3.5 The Proposed EHS Operation Procedure

The EHS operation scheme includes three different modes, namely, the start-up mode, the standby mode, and the normal mode. A cold start-up technique is executed during the start-up and standby modes, and employed without the need to any external battery or off-chip pre-charging mechanism. While the normal operation mode consists of the closed-loop operation of the proposed 3D-MPPT, and a proposed energy-aware technique. In this section, the proposed EHS operation procedure including the cold start-up, the energy-aware and the closed loop operations are presented and discussed.

### 3.5.1 Cold Start-up Operation

Developing a cold start-up technique is crucial for DC-DC converter within EHS [34, 66]. Figure 3-19 shows the key building blocks for the cold start-up mechanism namely, the supply selector, and the voltage detectors. The circuit schematic of the supply selector is shown in Figure 3-20.  $V_{in}$  and  $V_{cp}$  are applied to  $V_{sup-1}$  and  $V_{sup-2}$  respectively, then the higher voltage is selected ( $V_{sup} = \max(V_{in}, V_{cp})$ ) and used to power (i) a differential ultra-low-power RO at start-up and standby modes and (ii) the 3D-MPPT circuit at normal operation mode. The RO used in start-up and standby modes features high-frequency low power characteristics with temperature variation  $8.9\text{KHz}/^\circ\text{C}$ . It provides at  $V_{in-min}$  (350 mV)  $f_{sw}$  of 1.8 MHz with 22 nW power consumption, which makes it adequate solution for low-power EHS cold start-up. The waveforms of the supply selector across different operation modes are shown in Figure 3-21. Initially, the charges stored in  $C_{buff}$  equals '0', hence, the EHS operation sequence works as follow: first, during the start-up mode,  $V_{in}$  is less than  $V_{cp}$ , so  $M_2$  pulls  $V_1$  up ( $V_1 = V_{in}$ ) and turns  $M_4$  OFF while it pulls  $V_2$  down ( $V_2 = 0$ ) and turns  $M_5$  ON, hence  $V_{sup}$  equals  $V_{in}$ . Second, once  $V_{cp}$  becomes greater than  $V_{in}$ , (standby mode)  $M_1$  pulls  $V_1$  down ( $V_1 = 0$ ) turning  $M_4$  ON and pulls  $V_2$  up ( $V_2 = V_{cp}$ ) turning  $M_5$  OFF, and allowing the start-up circuit to be powered by  $V_{cp}$ . Finally, when the output voltage detectors (Figure 3-21) detects a high voltage at the output node ( $V_{cp} \sim 1\text{ V}$ ), they trigger the DPU to connect the load circuit ( $S_{en} = 0$ ) indicating the start of the normal operation mode. The developed supply selector is modified from the conventional one presented in [68] by adding  $M_3$  that significantly decreases the static on-current in  $M_1$  and  $M_2$  during the standby and normal operation modes. Figure 3-22 shows the

significant decrease in power consumption after adding  $M_3$ , beyond the start-up operation mode.

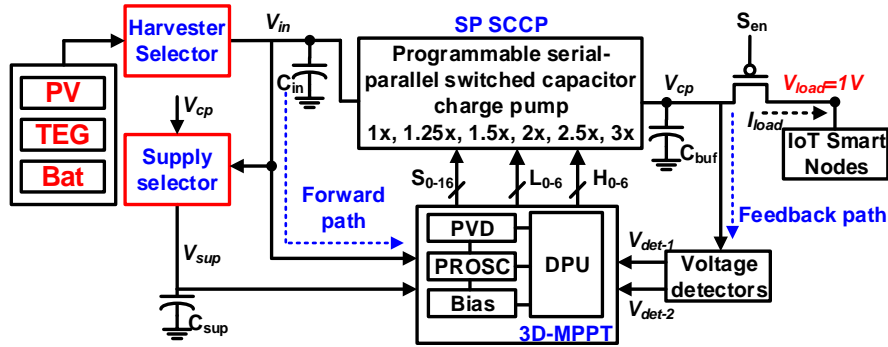


Figure 3-19. Proposed MISO EHS architecture along with the start-up and energy aware blocks

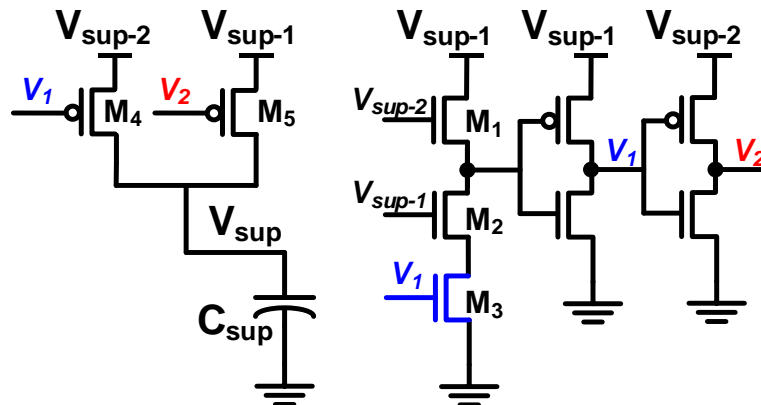


Figure 3-20. Circuit schematic of the supply selector for cold start-up

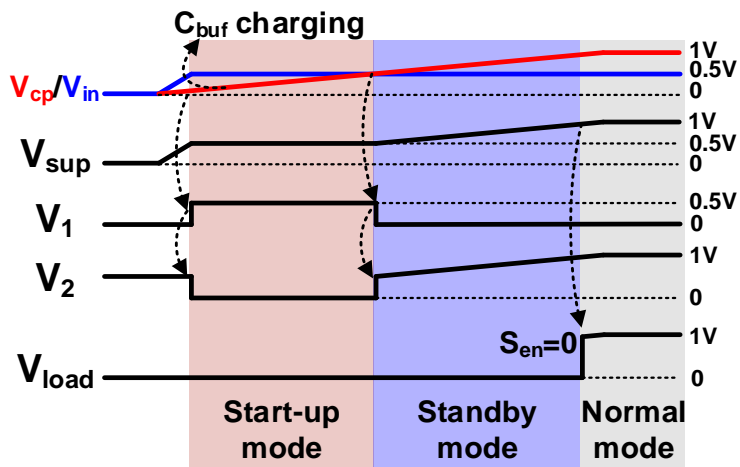


Figure 3-21. Circuit schematic of the programmable current starved ring oscillator

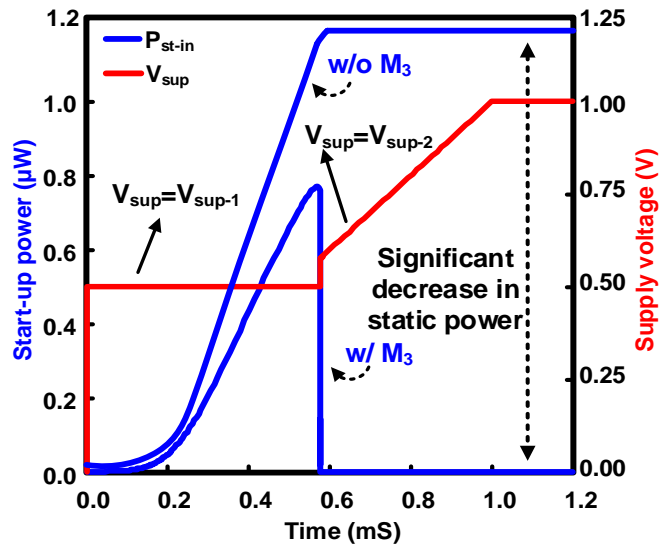


Figure 3-22. Simulation results for the supply selector static power and output selected voltage

### 3.5.2 Energy-Aware Operation

By connecting multiple DC energy scavenger to the EHS, a multiple-input-single-output (MISO) EHS can be obtained. As shown in Figure 3-19 a PV cell, a TEG and a backup battery are connected in parallel to a harvester selector block (HSB) that delivers the harvested energy from the PV cell or the TEG to the SP SCCP, or from the backup battery in case of low harvester energy. The HSB, shown in Figure 3-23 is an energy-aware block that compares  $PV_{in}$  and  $TEG_{in}$  concurrently with  $V_{in-min}$  (i.e. 350 mV) using a set of identical voltage detectors (VD). Each VD triggers its outputs if and only if the harvester input exceeds the  $V_{in-min}$ . The results are fed to a logic circuit (Figure 3-23) that adopts an energy-aware priority algorithm. Finally, S1, S2, and S3 control an IN-OUT selector to determine the energy harvester that will be connected to the SP SCCP. Following the timing diagram in Figure 3-23, in case 1,  $PV_{in}$  is above  $V_{in-min}$ , indicating that it has excess energy, while  $TEG_{in}$  is less than  $V_{in-min}$  which implies that it is low in energy. Thus, power is delivered from the PV to the EHS. Likewise, in case-2,  $TEG_{in}$  is selected to feed the SP SCCP, as it is above  $V_{in-min}$ . In another scenario, in case-3,  $PV_{in}$  and  $TEG_{in}$  are above  $V_{in-min}$ , which entails that both

of them have excess energy. However, following the energy-aware priority algorithm of the logic circuit depicted in Figure 3-23,  $PV_{in}$  is selected as an input for the SP SCCP. When both harvesters' inputs are below  $V_{in-min}$ , implying low harvesting energy, the backup battery is then used to feed the SP SCCP. Here, it is assumed that  $V_{bat}$  is always above  $V_{min}$ , for this reason, no VD is required to check  $V_{bat}$  DC level.

### 3.5.3 Closed-Loop Operation

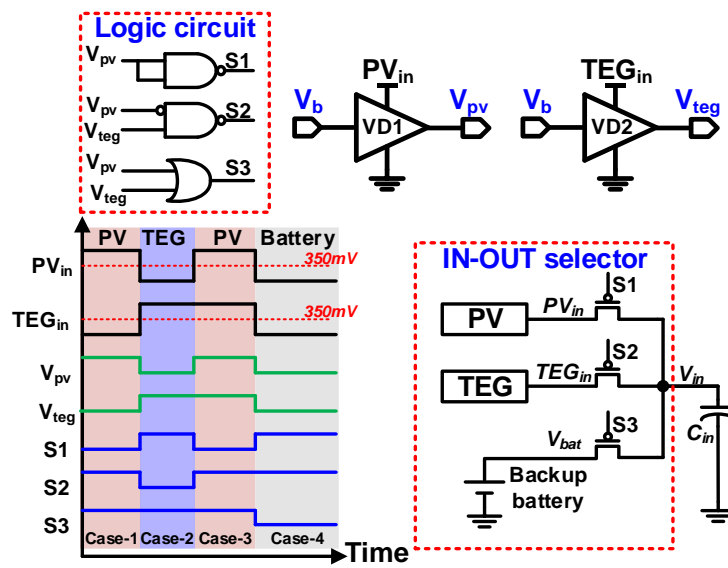


Figure 3-23. The proposed harvester selector block and operation timing diagram

The proposed EHS harvests solar and thermal energy to provide a regulated output voltage (1 V). It is composed of an FWP and an FBP (Figure 3-9). The FWP features a continuous  $V_{in}$  range detection, to set the proper SP SCCP conversion ratio. While the load condition is sensed using the FBP, to establish the SP SCCP  $f_{sw}$ ,  $W_{HS}$  and  $W_{LS}$  accordingly.

### 3.5.3.1 Forward Path

The FWP architecture and flowchart are shown in Figure 3-24. Initially, assuming normal operation mode,  $N$  is set to '1X'. After the bias circuit stabilizes according to the active 4-bit 'Sel' signal fed from the DPU, the PVD compares  $V_{in}$  with a certain boundary voltage equals ' $V_{cp}/N_i$ ' set by the selected  $V_{bias}$  following (3-6). Following the flow chart depicted in Figure 3-24, if the condition is true, the 3D-MPPT locks the SP SCCP conversion ratio ' $N$ ' and set  $W_{LS}$  accordingly. However, if the condition is false, ' $i$ ' is incremented by shifting the 'Sel' signal one bit left, and the same condition is re-checked with the updated boundary voltage ( $V_{bias}$ ) and so on. The loop repetition frequency is limited by the input energy harvester voltage variation.

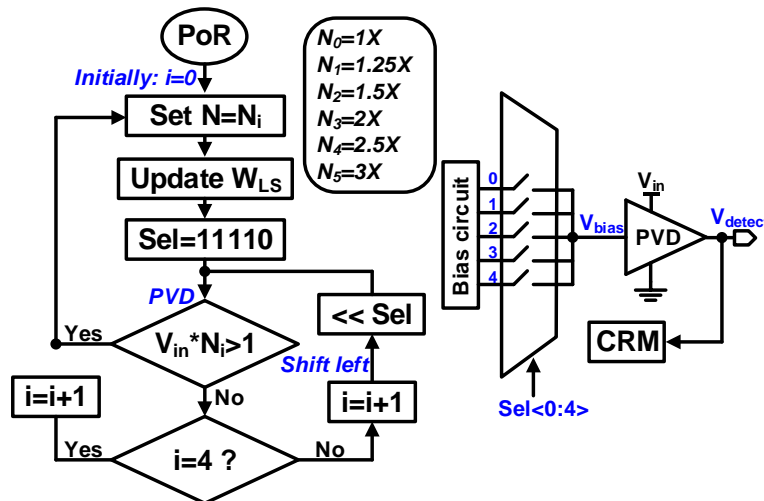


Figure 3-24. Proposed 3D-MPPT forward path flow-chart

### 3.5.3.2 Feedback Path

Within the FBP, the proposed 3D-MPPT maintains regulation, determines the load state, and then updates the SP SCCP  $f_{sw}$ ,  $W_{LS}$  and  $W_{HS}$  accordingly. The output voltage detectors set (Figure 3-9) triggers their outputs,  $V_{det-1}$  and  $V_{det-2}$ , (Figure 3-13) when the  $V_{cp}$  cross the upper voltage boundary  $V_1$  or the lower voltage boundary  $V_2$ , respectively, keeping  $V_{cp}$  within a narrow window  $[V_2, V_1]$ . The implemented TDC,

comprising an edge detector and digital counter (Figure 3-12), senses  $V_{det-1/2}$  edges direction and measures their pulses periods. Figure 3-25 shows the FBP state diagram within the proposed 3D-MPPT. Initially, at a given  $V_{in}$ , if  $V_{cp} < V_2$ , which entails that the applied  $f_{sw}$  is not high enough for the instant  $I_{load}$  the 3D-MPPT DPU increments  $f_{sw}$  and proportionally increases  $W_{HS}$  and  $W_{LS}$ . Likewise, when an increase in  $V_{cp}$  is detected by the TDC, ( $V_{cp} > V_1$ ), indicating an unnecessarily high  $f_{sw}$  for the current  $I_{load}$  (low load condition), the 3D-MPPT DPU decrements  $f_{sw}$  and decreases proportionally  $W_{HS}$  and  $W_{LS}$ . The proposed 3D-MPPT features a novel on-time tracking technique, which allows the MPP to be tracked without the need to re-tune or sweep the conversion ratio, and/or the switching frequency each MPPT cycle, as in [7]. On the contrary,  $f_{sw}$ ,  $N$ ,  $W_{HS}$ , and  $W_{LS}$  are decreased or increased concurrently by sensing the direction of  $I_{load}$  and  $V_{in}$ .

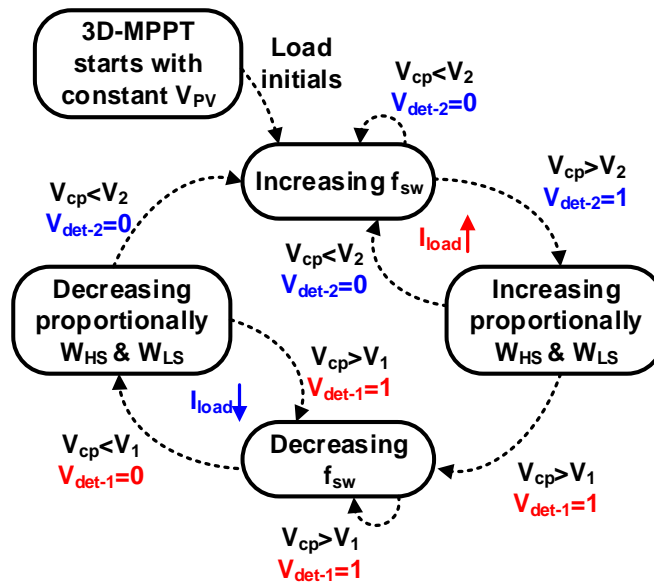


Figure 3-25. Proposed 3D-MPPT feedback path state diagram

### 3.6 Measurements Results

The proposed 3D-MPPT along with the implemented SP SCCP IC chip was designed and fabricated in 65-nm CMOS process. The die microphotography of the fabricated chip is shown in Figure 3-26. The integrated energy harvesting system including the 3D-MPPT and its auxiliary circuits occupies a silicon area of 0.538 mm<sup>2</sup>. Three MIM on-chip capacitors are used for the SP SCCP flying capacitors implementation. The employed energy harvesting system harvests from 0.35 V to 1 V, and provides a regulated output voltage at 1 V with a <2 nW control circuit and an ultra-low power DPU.

The dynamic performance, within the FBP, of the proposed 3D-MPPT, is presented in Figure 3-27. At a given  $V_{in}$ , the dynamic operation assumes three unique states. First, the reset state, where the tracking DPU receives a reset pulse to adjust the initial values of the  $f_{sw}$ ,  $W_{LS}$ , and  $W_{HS}$  of the 3D-MPPT. During this state, the load is isolated from the EHS. Second, the constant load state, where  $I_{load}$  achieves its steady state. At light load (i.e. 500 nA),  $V_{cp} > V_2$  and the resulted  $V_{det-1}$  tends to decrease  $f_{sw}$  and the transistors width. Likewise, at heavy load condition (i.e. 0.3 mA) the output voltage detectors transmit their  $V_{det-1/2}$  pulses to the DPU to maintain regulation and to increase the applied  $f_{sw}$ ,  $W_{LS}$ , and  $W_{HS}$ . The MPP, in both load conditions, is achieved when the SFM and SWM blocks, within the DPU, accommodate a proper switching frequency and transistors width with respect to the load condition. Finally, the transient state, when the load varies abruptly from 500 nA (light condition) to 0.3 mA (heavy condition), the DPU receives  $V_{det-1/2}$  pulses to proportionally modulate the  $f_{sw}$  (SWM) and the SCCP transistors size (SWM)

to track the MPP. Initially,  $V_{\text{det-2}}$  triggers to increase  $f_{\text{sw}}$ ,  $W_{\text{LS}}$ , and  $W_{\text{HS}}$  while  $V_{\text{det-1}}$  turns ‘0’, indicating an abrupt voltage droop due to a heavy load condition (Figure 3-27). Figure 3-28 shows the  $V_{\text{det-1/2}}$  pulses at light load condition. Eventually,  $V_{\text{det-2}}$  equals ‘1’ as  $V_{\text{cp}}$  is greater than  $V_2$ , while  $V_{\text{det-1}}$  pulses tend to maintain regulation and decreases the  $f_{\text{sw}}$  and transistors width to track the MPP.

The measurements depicted in Figure 3-29 shows the output regulation as  $V_{\text{in}}$  varies from 350 mV (low light irradiance) to 1 V (high light irradiance). As  $V_{\text{in}}$  varies across its range, the CRM control within the 3D-MPPT DPU alters  $W_{\text{LS}}$  in proportion to the applied  $V_{\text{in}}$  ( $V_{\text{gs}}$ ) to achieve the MPP at a given output load.

The PE of the proposed 3D-MPPT are recorded in Figure 3-30 at different input voltages across the load range. The tested chip achieved a peak efficiency of 88% at 200  $\mu\text{A}$  (heavy load), and a PE > 60% at 100nA (idle load condition). The efficiency results validate that the proposed 3D-MPPT algorithm as its adopted SWM technique shows the intended behavior not only at ultra-light loads but also at heavy load conditions. The proposed SWM technique improves the PE by at least 20% at light load conditions (<1  $\mu\text{A}$ ), and by 10% at heavy load conditions (> 100  $\mu\text{A}$ ), compared

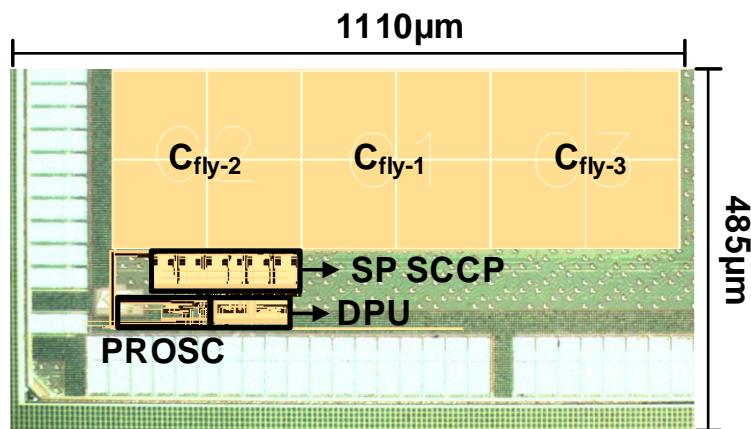


Figure 3-26. Die photo of the proposed EHS system.

with the prior state-of-the-art works. This improvement is due to the proportional optimization of the SCCP transistor size with  $I_{load}$ , along with the SFM and CRM, eliminating the trade-off between the conduction and gate driver power losses.

Table 3-I shows the comparison with prior art EHS. The suggested 3D-MPPT improves the PE by at least 20% as compared with the MPPT design in [8, 21]. Moreover, it can efficiently supply a  $P_{out-max}$  of 0.3 mW using small silicon area, resulting in a higher cost efficiency, and power density compared with the prior art, make it an adequate solution for IoT smart nodes. Ref [8] uses a large capacitor bank

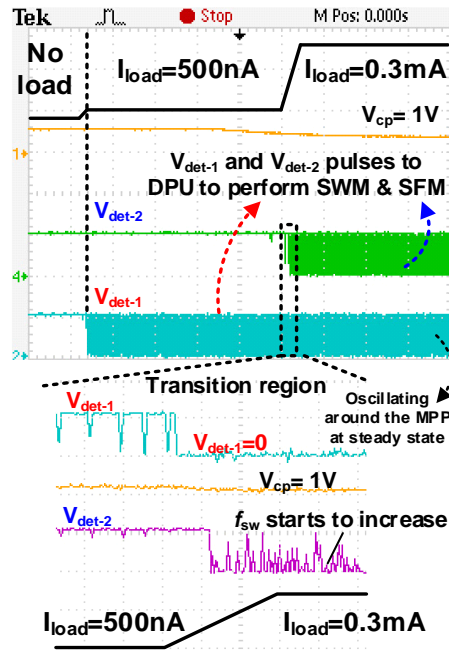


Figure 3-27. Transient response of the proposed 3D-MPPT at a 0.3mA load step

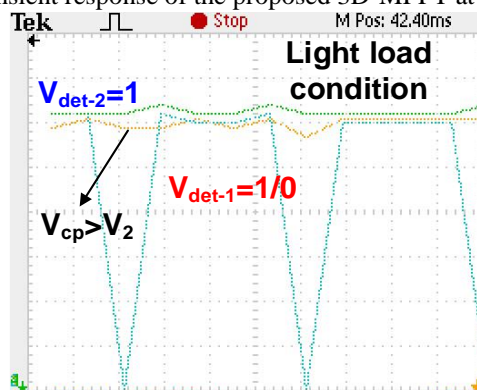


Figure 3-28. Output voltage detectors pulses at light load condition

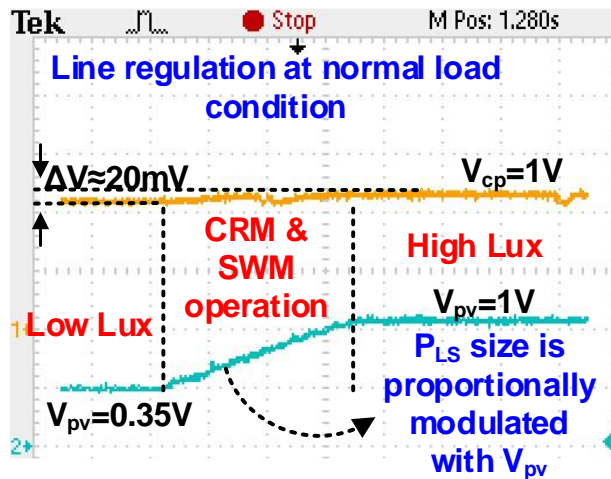


Figure 3-29. Regulation performance of the proposed 3D-MPPT

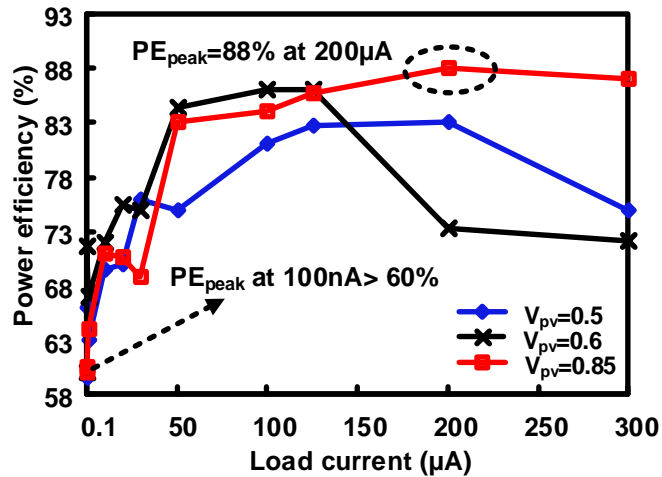


Figure 3-30. Power efficiency at different  $V_{pv}$  across the load range

for MPPT mechanism. Although it achieves a high efficiency of 86%, the PE degrades to less than 40% at light load conditions, moreover, the large die size makes it less cost-effective and degrades its power density. The nested doubler charge pump presented in [7], for conversion ratio configurability, increases the total conduction loss and the silicon area due to the considerable number of switches and pumping capacitors used, make it less cost efficient and low in power density for Our work proposed a novel tracking technique which IoT involves a reconfigurable feature regarding the switching frequency, the conversion ratio, and the charge pump transistors size, resulting in a 3D-MPPT. With total on-chip MIM flying capacitors of

240 pF, the integrated SP SCCP boosts  $V_{in}$  with six different conversion ratios to supply the IoT load with output power range from 100 nW to 0.3 mW, achieving the highest power density compared with the prior state-of-art designs. The implemented 3D-MPPT DPU complexity is reduced by using digital synthesis, minimizing the dynamic power consumption and making the proposed tracking technique scalable with process.

Table 3-I: Comparison with prior art

Parameters	[21] ISSCC'16	[30] ISSCC'14	[31] ISSCC'14	[7] JSSCC'16	[8] JSSCC'15	[36] TCAS'11	This work
Technology	0.18 $\mu$ m	0.18 $\mu$ m	0.13 $\mu$ m	0.18 $\mu$ m	0.18 $\mu$ m	0.13 $\mu$ m	<b>65nm</b>
Fully integrated	Yes	Yes	No	Yes	Yes	Yes	<b>Yes</b>
Conversion ratios	Reconf.	Reconf.	Single	Reconf.	Single	Single	<b>Reconf.</b>
MPPT technique	SFM and CRM	SFM	No MPPT	SFM and CRM	CVM	No MPPT	<b>SFM, CRM and SWM</b>
Regulation	Yes	Yes	No	Yes	Yes	Yes	<b>Yes</b>
Output voltage	1.8V	2.2V-5.2V	0.619V	3.3V	3.3V	1.4V	<b>1V</b>
Input range	0.5V-1.8V	0.14V-0.5V	0.15V-0.45V	0.45-3V	1.1-1.5V	0.42-0.48V	<b>0.35V-1V</b>
Frequency range	NA	70Hz-19MHz	250KHz	20KHz-1MHz	250KHz	0.6MHz-1MHz	<b>19KHz-16MHz</b>
Output power range	<34.8 $\mu$ W	5nW-5 $\mu$ W	<60 $\mu$ W**	<50 $\mu$ W	<21 $\mu$ W	<10 $\mu$ W	<b>100nW-300<math>\mu</math>W</b>
Peak Efficiency	72%	50% @ 0.45V	35% @ 0.18V 72.5% @ 0.45V	89% @ 2.5V 85% @ 1.2V**	86.4%	65% @ 0.45V**	<b>83% @ 0.5V 88% @ 0.85V</b>
Efficiency @ <1 $\mu$ A	NA	40% @ 100nA**	<10% @ 1 $\mu$ A**	<50% @ 1 $\mu$ A**	<40% @ 1 $\mu$ A**	30% @ 1 $\mu$ A**	<b>60.5% @ 100nA</b>
Monolithic area	1.69 mm <sup>2</sup>	0.86 mm <sup>2</sup>	NA	4 mm <sup>2</sup>	2.25 mm <sup>2</sup>	0.42 mm <sup>2</sup>	<b>0.54 mm<sup>2</sup></b>
Power density ( $\mu$ W/mm <sup>2</sup> )	20.6	5.8	NA	12.5	9.3	23.8	<b>555.6</b>
Cold start-up	Yes	Yes	Yes	Yes	Yes	Yes	<b>Yes</b>

\*\* extracted from the measurement results

### 3.7 Conclusion

This chapter shows the implementation of proposed 3D-MPPT using ultra-low power digital and analog circuits. The fabricated IC shows expected results regarding the regulation and transient performance. The motivation behind this work is to

achieve a high PE at the light and idle modes, which occupy the majority of the IoT SoC operation time, without sacrificing the high efficiency achieved under heavy load conditions. To address this challenge, a novel tracking algorithm that eliminates gate-driver/conduction power loss trade-off is proposed, showing a high PE across a wide load range compared with previous works. It successfully achieves a peak PE of 88% at 200  $\mu\text{A}$ , and a PE >60% at ultra-light load. An energy-aware algorithm has been proposed to select the harvester and connect it to the EHS. The input harvesting range is extending from 0.35 V to 1 V with a regulated output voltage at 1 V. The implemented MISO EHS is fully integrated with a cold start-up without the need of external reference voltage or passive off-chip components, making it suitable for ultra-low power applications within IoT smart nodes and wearable sensors.

# Chapter 4. Proposed Low Power High Efficiency DLDO with Fast Transient Response for Energy Harvesting Systems

## 4.1 Introduction

As mentioned in the introduction, in Chapter 1, following the international technology roadmap of semiconductor (ITRS) and the recent advances in integrated circuits technology, IoT smart nodes, including wearable devices, wireless electronics, and implantable sensors proliferate and increasingly become popular. This led the appearance of novel ultra-low-power techniques by the scaling down of supply voltage to near/sub-threshold region (i.e.  $< 0.5$ ) [17, 29]. To satisfy this low power consumption requirement, low power and efficient LDOs need to be designed. As introduced in Section 1.2.1, Analog LDOs have been a very strong choice in designing linear regulator within PMC for various IoT applications [62, 64]. However, analog LDOs suffer from a modest performance at low supply voltage due to high quiescent current [53]. For these reasons, digitally controlled LDOs have drawn the researchers' attention. Figure 1-1 the voltage scaling graph across the technology node. It describes how the digital LDO replaces its analog counterpart at low technology nodes (i.e. voltage down scaling)

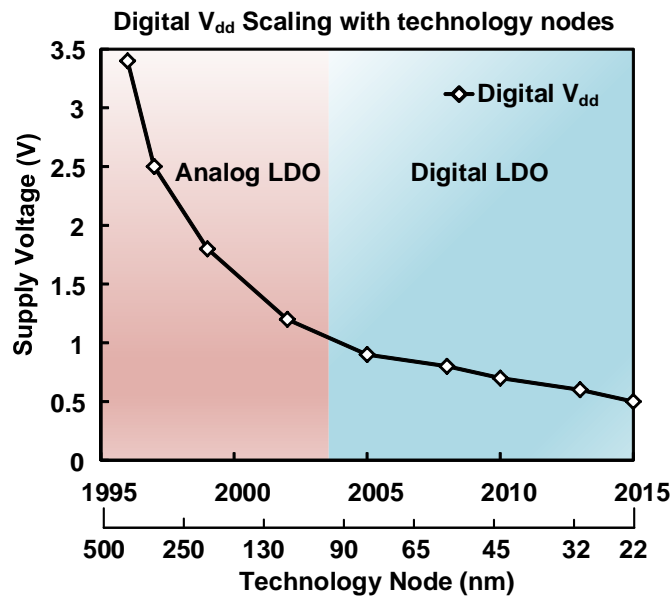


Figure 4-1. Supply voltage scaling across the technology node graph

Several DLDO designs have been discussed in literature. In [29], a DLDO with low quiescent current and supply voltage of 0.5 V is proposed for low power applications. However, the design shows poor transient performance due to the low power consumption achieved. The design was enhanced in [57] by developing an DLDO [29] assisted by an analog LDO connected in parallel. This augmented the quiescent power drastically. The work in [35] presents a reconfigurable DLDO for fast transient response to support a wide load range. However, it is interested in high current range (4.6 mA) with high quiescent current, which is not suitable for our target applications (e.g. biomedical sensors, IoT and energy harvesting applications). In [52], high supply voltage (1.39 V) with a fast transient response DLDO is developed. A low voltage DLDO with 0.39 V is presented in [17]. However, the developed control scheme requires a VCO and assumes digitally converted reference voltage, which implies the design of an ADC.

All the research works mentioned above focuses on either low power or fast

transient for load regulation. This work addresses the gap between the speed and the power of LDOs. This work proposes a clock modulation technique for achieving low power consumption and fast transient response with varying load.

## 4.2 Proposed DLDO Architecture and Circuit Implementation

In this section, the conventional DLDO architecture is first presented with a brief description of each block functionality. Then, the proposed DLDO is presented and discussed in detail showing the main contribution for enhancing the current efficiency and the proposed technique for speed-power trade-off elimination.

### 4.2.1 Conventional DLDO Architecture

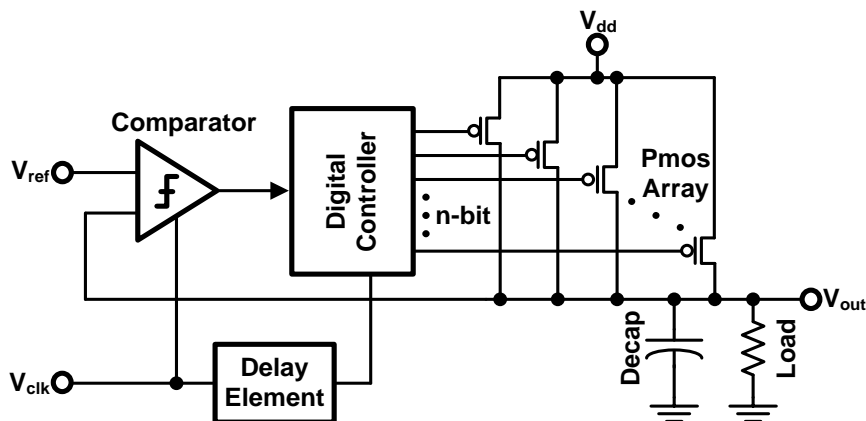


Figure 4-2. Conventional DLDO architecture

Figure 4-2 shows the structure of a conventional DLDO. It consists of mainly four blocks, namely, a comparator, a digital controller, delay elements and a pMOS array as power switches. The comparator takes the feedback voltage  $V_{out}$  and compare it with  $V_{ref}$ , while the digital controller uses the comparator output decision ('1' or '0') to adjust the switches located in the pMOS array through a serial-in-parallel-out bi-directional shift register. The comparator detects the drop/overshoot at  $V_{out}$  and controls the shift register to turn ON/OFF the pMOS switches. The shift register controls the number of ON switches depending on the comparator

output. Each switch is turned ON/OFF with the system clock ( $V_{clk}$ ). Hence, the output voltage regulation speed is dependent on the clock frequency. If the clock frequency is high enough,  $V_{out}$  transient response time decreases. However, this deteriorates the overall efficiency and increases the quiescent current. This requires a trade-off between the transition response time performance and the overall efficiency, which is the main aim of this work.

#### 4.2.2 Proposed DLDO Architecture and Circuit Implementation

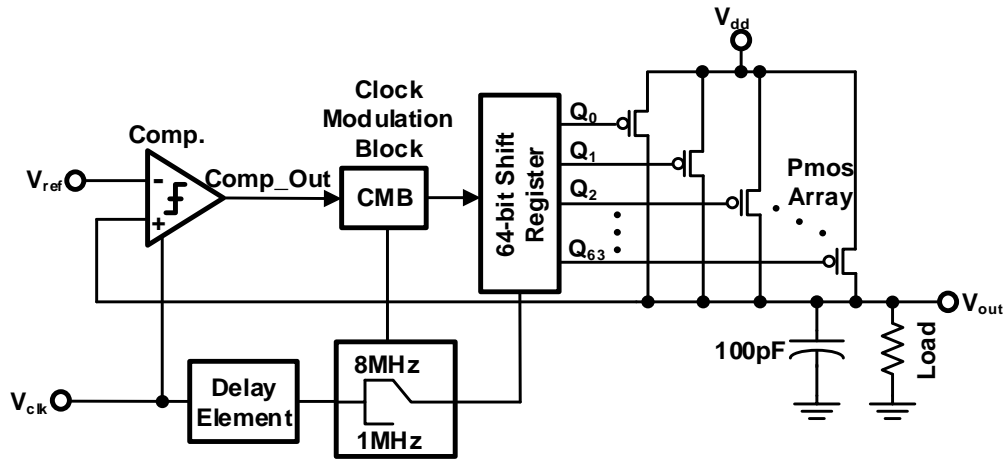


Figure 4-3. Proposed DLDO architecture and circuit implementation

In order to address the speed-power trade-off issue of the conventional DLDO, a DLDO with a novel clock modulation technique (CM) is proposed. The proposed DLDO architecture is illustrated in Figure 4-3. The proposed CM scheme switches the system clock to a higher frequency when a load transition state is detected, as described in Figure 4-4. This allows  $V_{out}$  to track  $V_{ref}$  with a reduced transient time. Once  $V_{out}$  becomes in the vicinity of  $V_{ref}$ , the proposed CM scheme switches the system clock back to a lower frequency to reduce the power consumption at constant load state, thus, increasing the overall efficiency. The proposed CM block detects the abrupt change in the load current whether it substantially decreases or increases. In this work, 8 MHz is used as a high clock frequency while 1 MHz is used as a lower frequency for controlling

the shift register with 64-pMOS switches. This covers the load current from 10  $\mu\text{A}$  to 200  $\mu\text{A}$ . The operation of the proposed CM is explained in detail in the following section, Section 4.2.3.

### 4.2.3 Clock Modulation for Fast Transient Response

the proposed CM scheme is illustrated in Figure 4-5. It consists of a peak

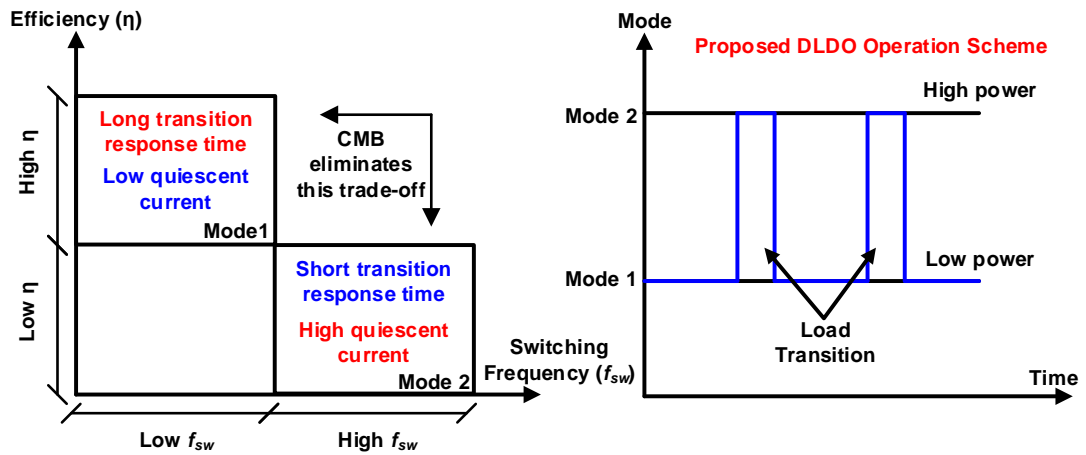


Figure 4-4. Proposed DLDO clock modulation operation principle

detector (PD) and a valley detector (VD) to detect the load current transition from high to low and low to high, respectively. At steady state condition and constant load current,  $V_{\text{out}}$  shows small ripples due to the continuous switching of the pMOS switches by the digital controller. However, at an abrupt load transition from low to high,  $V_{\text{out}}$  suffers from an undershoot and stays below  $V_{\text{ref}}$  for a long time depending on the decoupling capacitor size. If the used decoupling capacitor is too big, it takes several clock cycles so that  $V_{\text{out}}$  follows  $V_{\text{ref}}$ . Thus, a high clock frequency is utilized through the proposed CM block for a faster  $V_{\text{out}}$  recovery. In this work, the higher clock frequency is generated when the comparator signals ‘1’ or ‘0’ continuously over the five clock cycles. This is detected by the VD and the PD shown in Figure 4-6 and

Figure 4-7, respectively. The number of DFFs can be easily controlled based upon the target system requirements.

Figure 4-6 illustrates the VD. It comprises five DFFs connected in series. The outputs of these DFFs are pulled up to  $V_{dd}$  through the pMOS set control. likewise, the PD consists of five series DFFs as described in Figure 4-7 where outputs are tied to  $V_{ss}$  through the nMOS reset switch. Following the timing diagram depicted in Figure

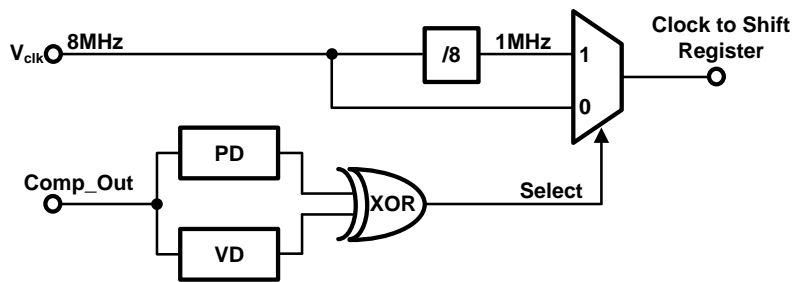


Figure 4-5. Proposed clock modulation (CM) block

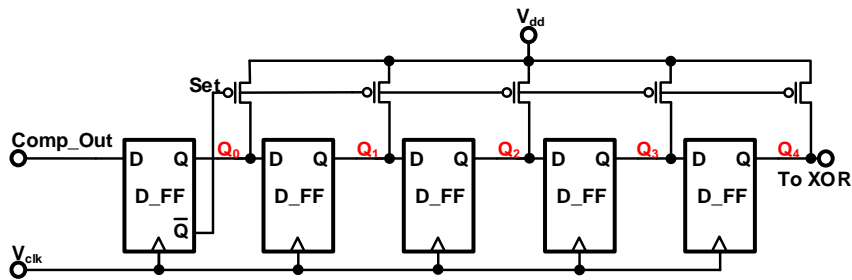


Figure 4-6. Valley detector architecture that detects the current transition from low to high

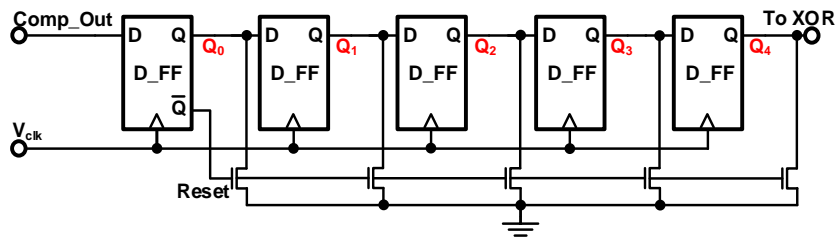


Figure 4-7. Peak detector architecture that detects the current transition from high to low

4-8 the operation concept of the proposed CM scheme is explained as follow. Initially, VD and PD outputs are set to '1' and '0', respectively. The two detectors outputs are then fed to an XOR gate which is set to '1' as an initial condition following the default state of the VD and PD. (Figure 4-5). Following the diagram illustrated in Figure 4-5, the XOR output controls a clock selector (MUX). The MUX output clock frequency is altered between a low frequency (1 MHz) or a high frequency (8 MHz). Initially, the lower frequency is selected (i.e. XOR='1') and supplied to the digital controller. When an undershoot is detected (i.e. the load current increase abruptly),  $V_{out}$  eventually drops below  $V_{ref}$  and the comparator outputs turns into '0' (Figure 4-8). The number of ON pMOS switches within the pMOS array increases with each clock cycle (1 MHz). With the first rising edge sensed by the VD and PD, the series DFFs start to pass the signal serially as a shift register, as shown in Figure 4-6 and Figure 4-7.

Following the waveform depicted in Figure 4-9, within the VD, the pMOS control switches turns 'OFF' since  $Q_{0-BAR}$  is '1', and the comparator output '0' is passed through the DFFs with each clock edge. After four consecutive clock edges, the '0' reaches the last DFF within the VD. On the contrary, in PD, the nMOS reset switches are turning 'ON' pulling the DFFs down (i.e. '0') (Figure 4-7). As described in Figure 4-10, after four clock edges (i.e. detection time proposed by the CM), VD outputs turns to '0' which make the XOR gate triggers '1' indicating a load transition state (Figure 4-8). Finally, the MUX selects the high frequency (i.e. 8 MHz).

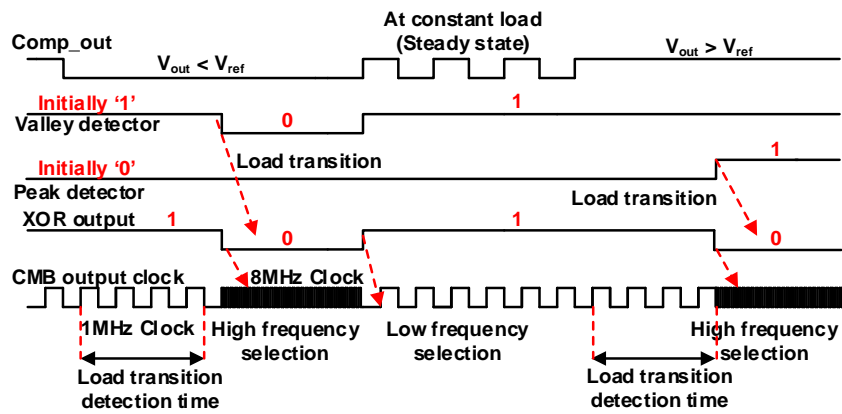


Figure 4-8. Timing diagram for the clock modulation block

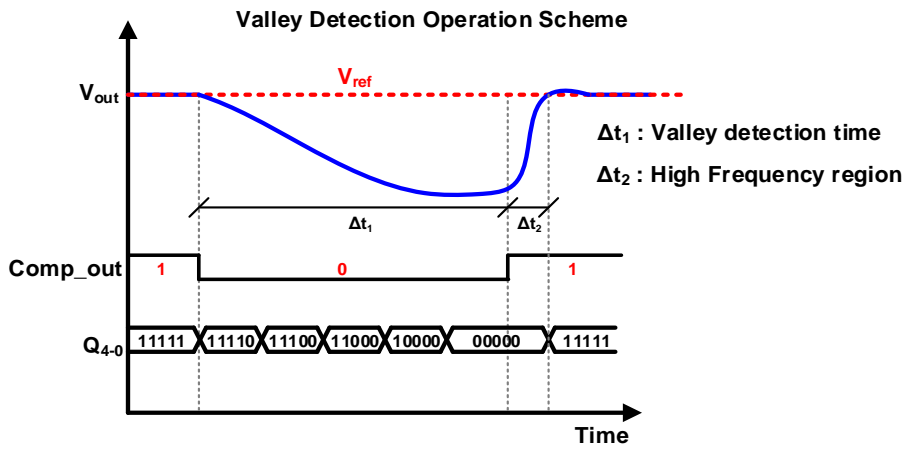


Figure 4-9. Waveforms of  $V_{out}$ , comparator and VD DFFs at low to high load transition

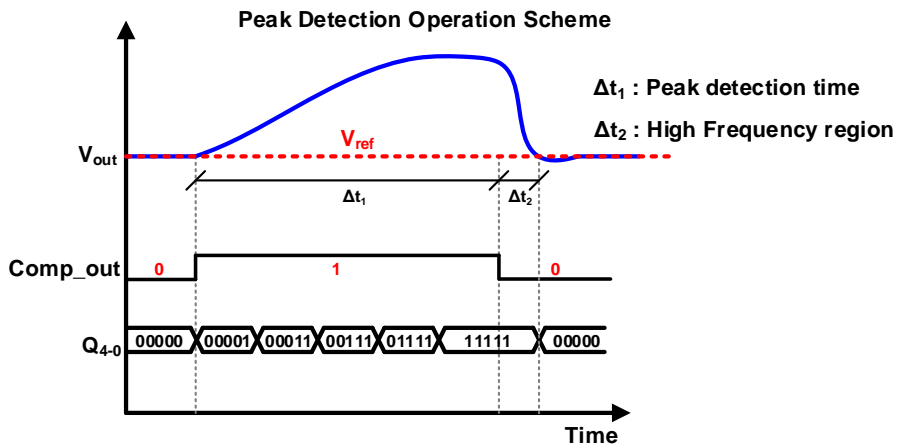


Figure 4-10. Waveforms of  $V_{out}$ , comparator and PD DFFs at high to low load transition

Once  $V_{out}$  hits  $V_{ref}$  due to the higher clock frequency used, the PD and VD restore their initial condition and the controller operates at a low frequency clock (i.e. 1 MHz) reducing the power consumption drastically at steady state.

### 4.3 Measurement Results

The proposed DLDO with CM is implemented in 65nm CMOS process with the area of  $0.037 \text{ mm}^2$ . Figure 4-11 shows the test chip microphotography. It operates at 0.6 V with 50 mV dropout voltage covering load range from 10  $\mu\text{A}$  to 200  $\mu\text{A}$ . The current efficiency results are recorded in Figure 4-12. The proposed DLDO achieves a maximum current efficiency of 99.7% at 200  $\mu\text{A}$  current load, with 0.9  $\mu\text{A}$  quiescent current. Figure 4-13 shows the transient  $V_{out}$  waveform when  $V_{ref}$  and  $V_{dd}$  changes from 0 V to 0.55 V and 0.6 V, respectively. The DLDO requires around 25 mS to start-up and reach the steady state when  $V_{dd}$  turns ON from zero voltage. Figure 4-14 demonstrates the transient response performance of the proposed DLDO. It shows the  $V_{out}$  behavior when the load changes abruptly from 10  $\mu\text{A}$  to 200  $\mu\text{A}$  while the opposite load transition is explained in Figure 4-15. It can be seen that  $V_{out}$  follows  $V_{ref}$  without a noticeable undershoot or overshoot with the aid of the proposed CM scheme where the higher clock frequency is employed. Table 4-1 compares this work with other state-of-the-art DLDOs. It can be seen that the proposed DLDO has the lowest quiescent current with 99.7% current efficiency at a near-threshold supply voltage ( $V_{dd}$ ) 0.6 V with 50 mV dropout voltage and 100 pF on chip decoupling capacitor. Which make it

an adequate solution for on-chip IoT wireless sensors and bio-medical applications that requires a sub/near-threshold regulated voltages.

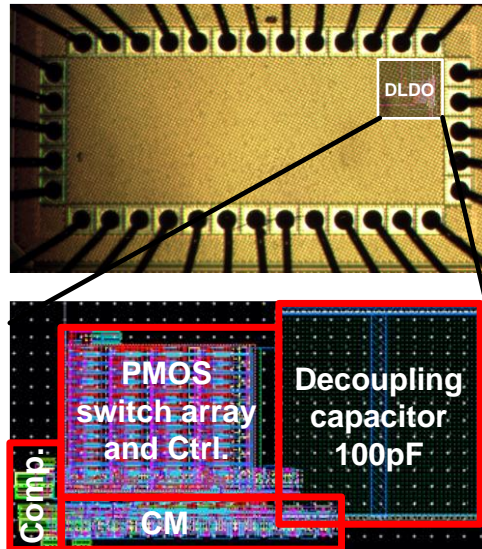


Figure 4-11. Test chip die photo

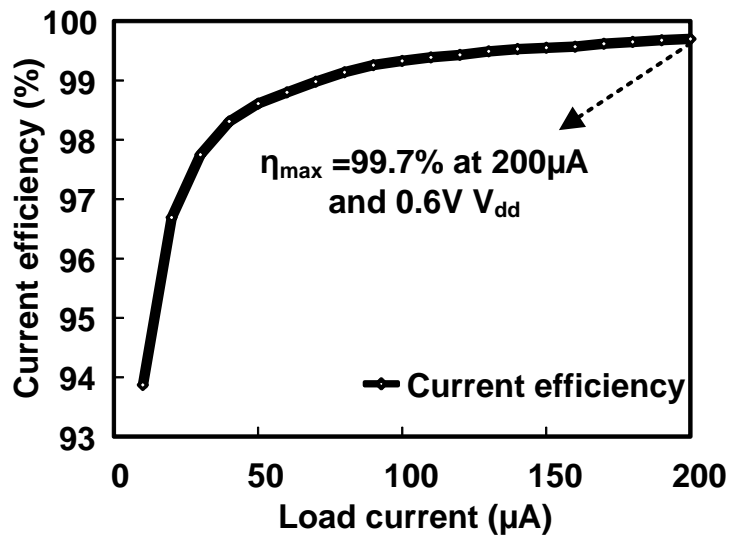


Figure 4-12. Current efficiencies across load range

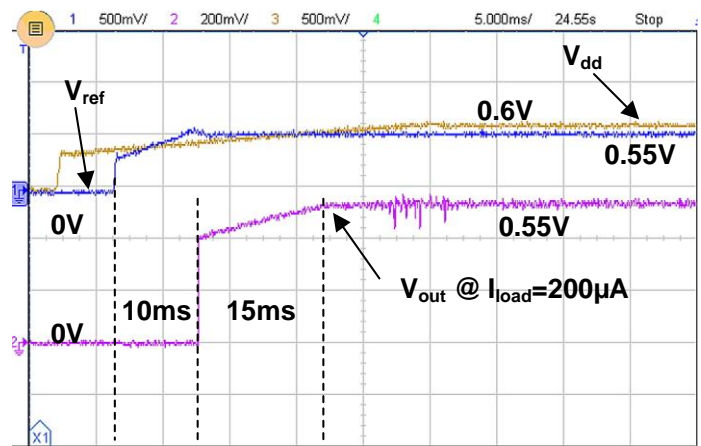


Figure 4-13. Measured transient  $V_{out}$  waveform when  $V_{ref}$  and  $V_{dd}$  changes from 0V to 0.55V and 0.6V respectively

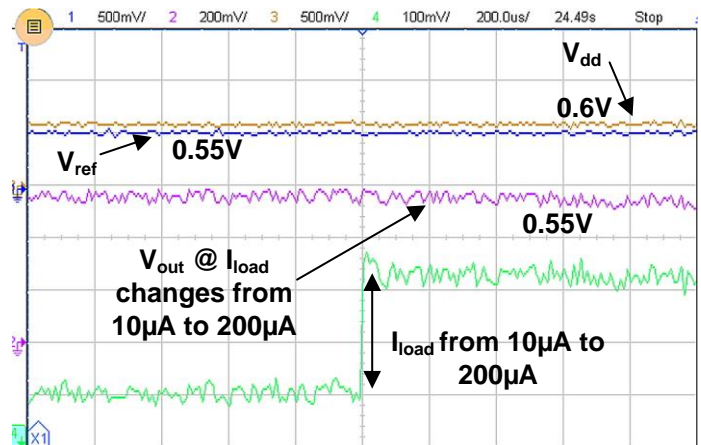


Figure 4-14. Measured transient  $V_{out}$  waveform when  $I_{load}$  changes suddenly from  $10\mu A$  to  $200\mu A$

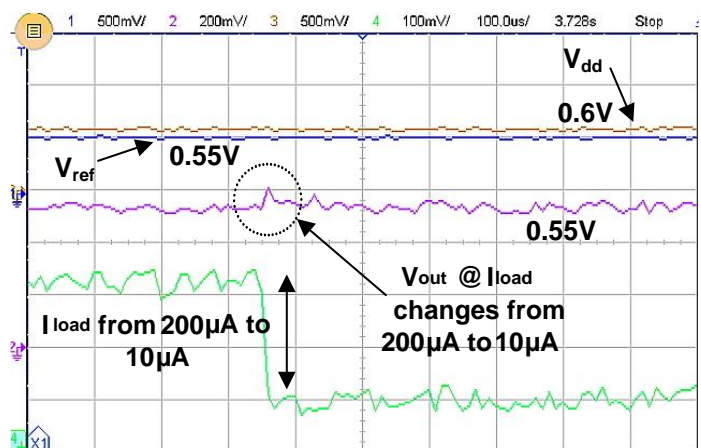


Figure 4-15. Measured transient  $V_{out}$  waveform when  $I_{load}$  changes suddenly from  $10\mu A$  to  $200\mu A$

Table 4-1: Comparison with state-of-the-art regulators

	Unit	[17]	[29]	[35]	[52]	<b>This Work</b>
CMOS Technology		90nm	65nm	130nm	40nm	<b>65nm</b>
Active area	mm <sup>2</sup>	0.026	0.042	0.114	0.057	<b>0.037</b>
Minimum input voltage	V	0.38	0.5	0.5	1.34	<b>0.6</b>
Nominal output voltage	V	0.12-0.32	0.45	1.14	1.2	<b>0.55</b>
Maximum load current	mA	1	0.2	4.6	250	<b>0.2</b>
Line Regulation	mV/V	2.9	3.1	-	-	<b>200</b>
Load Regulation	mV/mA	0.11	0.65	<10	-	<b>65</b>
Decoupling capacitor	uF	0.1	0.1	1000	Not used	<b>0.0001</b>
Quiescent current	uA	6.85	2.7	24-221	130	<b>0.9</b>
Current Efficiency	%	99.3	98.7	98.3	96-99.95	<b>99.7</b>

#### 4.4 Conclusion

The developed DLDO in this work is designed for ultra-low-power IoT and wireless sensors applications. The fabricated chip uses 65 nm CMOS process technology with an on-chip 100 pF decoupling MOS capacitor. The proposed novel CM techniques eliminate the trade-off between transient performance and current efficiency. The tested chip operates at voltage supply 0.6 V with 50 mV dropout voltage, and support a load current from 10  $\mu$ A to 200  $\mu$ A with 99.7% peak current efficiency at 200  $\mu$ A. The fully integrated chip presents an adequate power management solution to various ultra-low power applications, to supply a sub/near-threshold regulated voltage with a high transient performance within IoT SoC.

## **Chapter 5. Conclusion and Future Work**

### **5.1 Thesis Conclusion**

In this thesis, several architectures, system and circuit-level techniques along with novel control algorithms have been developed to address the main limitation issues of tracking PE, conversion PE and design area in designing the ultra-low power MPPT for EHS within IoT smart nodes. MPPT systems are inevitable part of EHS for biomedical and IoT applications where both power consumption, efficiency and area are very critical. To fulfil the stringent power budget within EHS for IoT applications stems from the limited input power provided by the EHL due to its small form factor two MPPT architectures with novel tracking algorithm have been introduced in this thesis. Their main contribution is to improve the tracking and conversion power efficiency, at the cost of an ultra-small fraction of the available harvested power hence, extending the peak output power that can be supported at the same input harvested power.

In chapter 2, a novel Time-based MPPT architecture has been proposed that addresses the tracking efficiency limitation issue. The proposed tracking technique is an indirect, non-interrupting approach using a novel timing-based algorithm addressing the tracking efficiency. It reduces the power consumption and design complexity. It consists of a digital processing unit that executes the proposed tracking algorithm along with ultra-low power auxiliary circuits. The fabricated chip was tested, and its functionality was verified at input voltage range of 0.4 V to 1.7 V. The test shows a transient response time of less than 100 ms at the minimum supply voltage of

0.8 V with peak tracking efficiency of 96.2 % when supplied by a photovoltaic (PV) micro-cell array using an irradiation range of 200 lux to 1000 lux.

Chapter 3 shows the implementation of a novel 3D-MPPT that addresses the power efficiency limitation issue at wide-load range applications within IoT SoC. The proposed MPPT improves the conversion efficiency over a wide load range using a novel switch width modulation (SWM) technique. It consists of a novel tracking algorithm that eliminates gate-driver/conduction power loss trade-off showing a high conversion efficiency across a wide load range compared with previous works. The tested chip shows expected result proving the validation of the proposed SWM technique. It successfully achieves a peak PE of 88% at 200  $\mu$ A, and a PE >60% at ultra-light load. Moreover, an energy-aware algorithm has been implemented for a multiple-input-single-output EHS.

In chapter 4, for ultra-low power IoT applications that requires to step-down the input EHL voltage 10s of mV, a fully integrated, near-threshold digital low-dropout voltage (DLDO) regulator is proposed. It addresses the speed-power trade-off. It consists of a load current aware clock modulation scheme that provides a fast-transient response only during load state transitions. The proposed clock modulation (CM) controls the clock frequency when it senses an abrupt load current transition. A test chip is fabricated using 65-nm CMOS technology and demonstrates the current efficiency of 99.7% with the load current from 10  $\mu$ A to 200  $\mu$ A with and the quiescent current of 0.9  $\mu$ A.

## 5.1 Future Work within Energy Harvesting Systems for IoT applications

As mentioned in the introduction, in Chapter 1, the recent progress in IoT devices including portable electronics and wireless sensor nodes rises the call for the design of an efficient self-sustained PMC. Thus, for future work, designing a PMC is powered by energy harvesters within IoT smart nodes is significant and promising for a self-sustaining systems and prolonged lifetime.

Solar, thermal and mechanical energy harvesters have been explored in many researches [2, 8, 39, 45]. Among these scavengers, mechanical energy is promising due to its common existence in our daily life; it can be harvested from human, vehicles and objects motion. Among those harvesters, a novel mechanical energy harvester called triboelectric-nanogenerator (TENG), has been explored. TENG features low weigh, small size, and high-power density. It generates electricity based on the coupling of triboelectrification and electrostatic induction [107-117]. Hence, this research future work will consist a PMC to harvest energy from the TENG and efficiently charge a super-capacitor or a battery to supply various blocks within IoT SoC.

However, designing an energy harvesting system powered by TENG is challenging due to their electrical characteristics issues. TENG devices generate a very high voltage peak ( $>100V$ ) with an internal impedance in the range of 10s  $M\Omega$ , which make the direct connection between the TENG and the PMU not possible. Furthermore, its high internal impedance is hard to be matched with the IoT electronic

devices, making the design of an interface circuit with high efficiency a non-trivial task.

The main goal of this research is to develop a realistic electrical model for TENG that can be used to develop various MPPT design techniques within the TENG-powered PMC, to overcome the high input impedance issue and extract the maximum amount of the TENG harvested power and convert it efficiently to the output for battery charging.

The success of this research will produce a high-efficient TENG-powered PMC that can harvests and senses various mechanical vibrations such as tapping motions (i.e. hands, feet, etc), buildings vibration, sliding and rotating motions which make it suitable and compatible with numerous applications types within IoT smart nodes. The successful outcome of this research will create more research and product development activities in academia and integrated circuits industry.

## Author's Publications

### Journal Papers

- **K. Rawy**, F. Kalathiparambil, D. Maurath, and T. T. H. Kim, "A Self-adaptive Time-Based MPPT with 96.2% Tracking Efficiency and a Wide Tracking Range of 10- $\mu$ A to 1-mA for IoT Applications " *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, pp. 2334-2345, 2017.
- **K. Rawy**, T. Yoo, and T. T. H. Kim, "An 88% Efficiency 0.1-300- $\mu$ W Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes," *IEEE Journal of Solid-State Circuits*, pp. 1-12, 2018.

### Conference Papers

- K. G. Jayaraman, **K. Rawy**, and T. T. Kim, "A 0.6-V power efficient digital LDO with 99.7% current efficiency utilizing load current aware clock modulation for fast transient response," in 2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2016, pp. 103-106.
- **K. Rawy**, F. K. George, D. Maurath, and T. T. Kim, "A Time-based Self-Adaptive Energy-Harvesting MPPT with 5.1- $\mu$ W Power Consumption and a Wide Tracking Range of 10- $\mu$ A to 1-mA " in ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, 2016, pp. 503-506.
- **Karim Rawy**, T. Yoo, and T. T. Kim, "An 88% efficiency MPPT for PV energy harvesting system with novel switch width modulation for output power 100nW to 0.3mW," in 2017 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2017, pp. 117-120.

### Student Design Contest

- **Karim Rawy**, T. Yoo, and T. T. Kim, "An 88% efficiency MPPT for PV energy harvesting system with novel switch width modulation for output power 100nW to 0.3mW," in 2017 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2017, pp. 117-120. ( **Invited to the student design contest**)

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