A Mixed-Signal GFSK Demodulator Based on Multithreshold Linear Phase Quantization

Dong Han and Yuanjin Zheng, *Member, IEEE*

***Abstract*—An ultralow-power Gaussian frequency-shift keying (GFSK) demodulator with large tolerance for process variations and wide coverage of data rate for low-intermediate-frequency (low-IF) wireless receivers is presented. A novel multithreshold linear phase quantization technique is proposed to improve the demodulator sensitivity and relax the tradeoff between the selection of the IF and the data rate. A dynamic threshold slicer is employed to efficiently overcome the dc drifts caused by the input frequency offset. The demodulator achieves 490-mV input dc offset cancellation, 800-kHz frequency offset tolerance, and data rate coverage from 100 kb/s to 2 Mb/s. The measured signal-to-noise ratio (SNR) is 16.0 dB for a 0.1% bit error rate (BER) and a 0.25 modulation index. The demodulator has been fabricated in a 0.18-μm complimentary metal–oxide–semiconductor process with only 0.14-mm^2 active area and 450-μA current drawn from a 1.8-V power supply.**

***Index Terms*—DC offset cancellation, frequency offset cancellation, Gaussian frequency-shift keying (GFSK) demodulator, multithreshold linear phase quantizer (LPQ).**

I. Introduction

In recent years, the increasing demand for personal healthcare, mobile entertainment, and information services has driven out many short-range wireless standards such as Bluetooth, wireless personal area networks (WPANs), and wireless body area networks (WBANs). A low-intermediate-frequency (low-IF) architecture and a Gaussian frequency-shift keying (GFSK) modulation scheme are widely used in low-power wireless transceivers for these standards [1]–[3]. For recovering data from GFSK signals, several demodulators with good performance have been reported in [4]–[7]. However, the relatively high power consumption and large modulation index may prevent them from being used for some WPAN/WBAN applications with more stringent requirements on power dissipation and spectral efficiency. In this work, through a novel multithreshold linear phase quantizer (LPQ) and dynamic threshold slicer, an ultralow-power GFSK demodulator with wide coverage of data rate and small modulation index is presented for receivers in WPAN, WBAN, and Bluetooth applications.

Manuscript received November 21, 2008; revised April 1, 2009 and July 9, 2009. Current version published September 16, 2009. This work was supported by the Agency for Science, Technology and Research (A*STAR), Singapore, under the Embedded and Hybrid Systems Phase II (EHS-II) Program. This paper was recommended by Associate Editor B. Otis.

The authors are with the Institute of Microelectronics, A*STAR, Singapore 117685 (e-mail: hand@ime.a-star.edu.sg).

Digital Object Identifier 10.1109/TCSII.2009.2027969

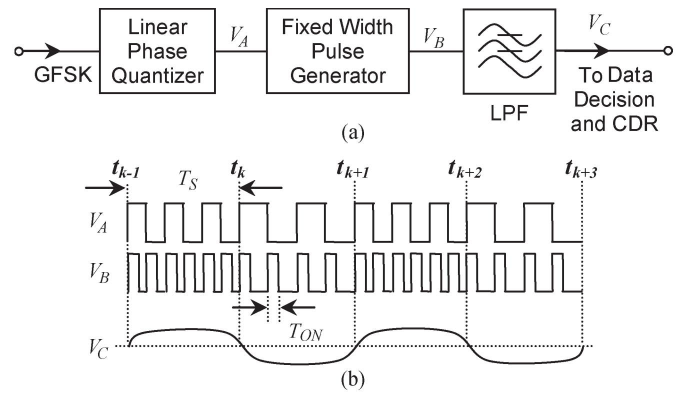

Fig. 1. Typical phase-quantization-based GFSK demodulator. (a) Block diagram. (b) Data flow.

II. Phase-Quantization-Based GFSK Demodulator

Fig. 1 shows the block diagram of a typical phase-quantization-based GFSK demodulator. It is a mixed-signal frequency-to-voltage converter. The frequency information of the GFSK signal is mapped into the density of transition edges (phase quantizing points) by the phase quantizer in V_A, and then through the fixed-width pulse generator (FWPG) and low-pass filter (LPF), this density is extracted into the voltage variation in V_C for data decision [4]. Due to the compact structure, the phase quantization approach can attain good performance with low power consumption. To discriminate the input frequency with a consistent accuracy, the phase quantizer should be linear. Generally, the required modulation index of the demodulator is determined by the quantization size, which is represented as $LSB(\varphi)$, of the LPQ. For a continuous-phase-modulation signal, the increment of the excess phase [8] in $[t_k, t_{k+1}]$ is

$$\left.\begin{aligned} \theta(t,\alpha_k) &= 2\pi\hbar \sum_{i=k-L+1}^{k} \alpha_i q(t - iT_S) \\ q(t) &= \int_{-\infty}^{t} g(\tau)d\tau \end{aligned}\right\} \tag{1}$$

where $\hbar$ is the modulation index, α_k is the baseband bit sequence, T_S is the period of α_k, $g(t)$ is the frequency shape pulse, and L is the pulse length of $g(t)$. The 2-ary data α_k may take any of the values from $\{\pm 1\}$, which represent the baseband logic "1" and "0," respectively. With different baseband logic values, the difference of $\theta(t,\alpha_k)$ is $\Delta\theta = |\theta(t,\alpha_x = +1) - \theta(t,\alpha_y = -1)|$. For frequency-shift keying (FSK) signals, $g(t)$ is the rectangular pulse with a pulse length of 1 (1REC); thus, $\Delta\theta = 2\pi\hbar$. For typical Bluetooth GFSK signals [9], [10], $g(t)$ is the Gaussian pulse, and $\Delta\theta$ is approximated as $2\pi\hbar/1.28$.

1549-7747/$26.00 © 2009 IEEE

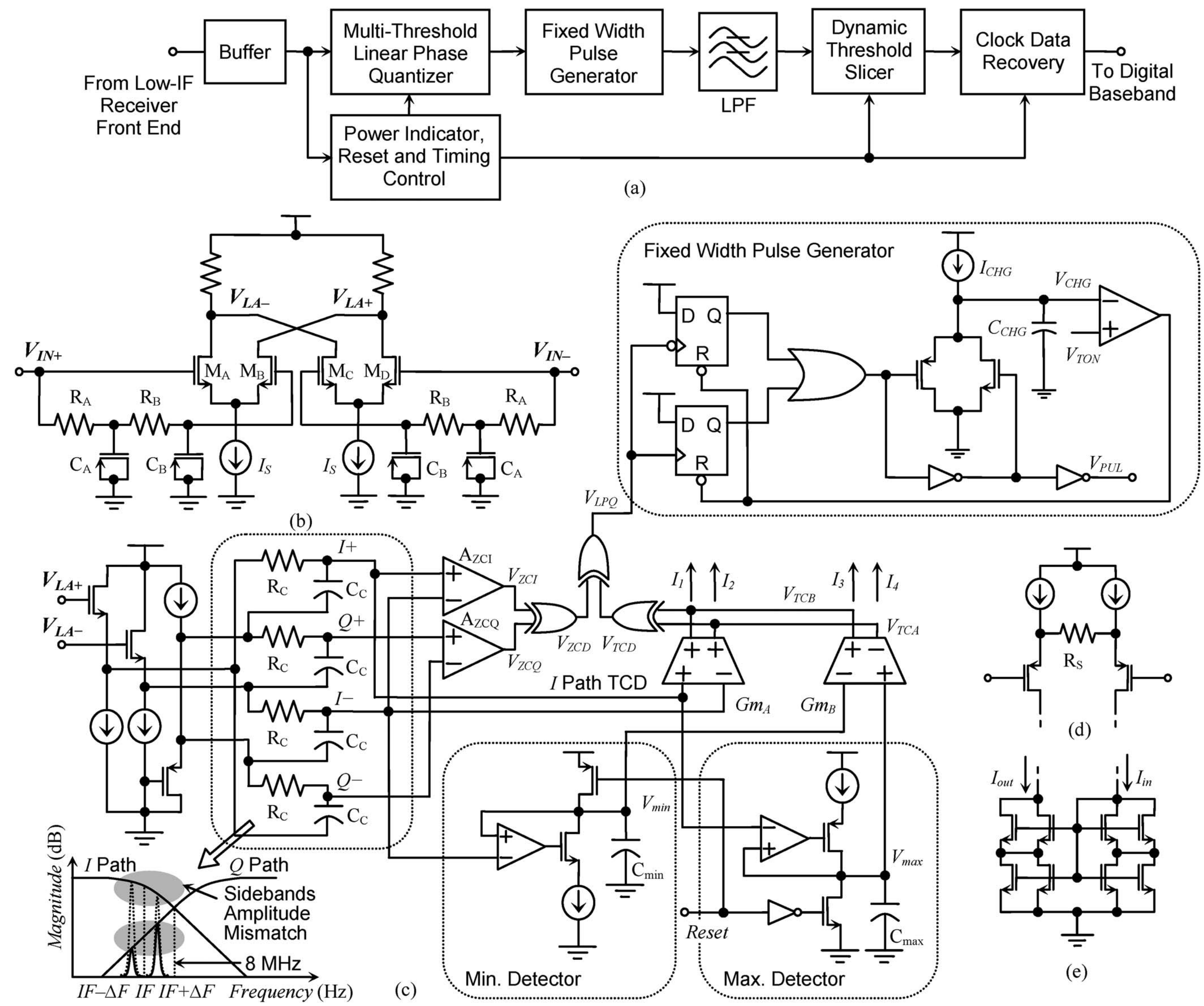

Fig. 2. Proposed multithreshold-LPQ-based GFSK demodulator. (a) System architecture. (b) Buffer. (c) Multithreshold LPQ and FWPG. (d) Input stage of the transconductors. (e) 2 × 2 series-parallel transistor array current mirror.

To demodulate the FSK/GFSK signals, the phase quantization size of the LPQ should be less than $\Delta\theta$. Therefore, for an LPQ-based demodulator, the ideal minimum detectable modulation indexes are $\hbar_{\min,\mathrm{FSK}} = LSB(\varphi)/2\pi$ for FSK signals and $\hbar_{\min,\mathrm{GFSK}} \approx 1.28\hbar_{\min,\mathrm{FSK}}$ for GFSK signals.

To improve the spectral efficiency and/or adjacent channel interference rejection, it is desirable to achieve a lower $\hbar_{\min,\mathrm{GFSK}}$. With both I and Q channels [4], $\hbar_{\min,\mathrm{GFSK}}$ is 0.32. In this work, through an equivalent four-threshold LPQ, we reduce $\hbar_{\min,\mathrm{GFSK}}$ to 0.16, which can fully cover the modulation index of the Bluetooth standard.

III. Multithreshold-LPQ-Based GFSK Demodulator

The block diagram of the proposed GFSK demodulator is presented in Fig. 2(a). It is mainly composed of four functional blocks: an input buffer for removing the input dc offset, a frequency-to-voltage converter (including a multithreshold LPQ, an FWPG, and an LPF) for discriminating the input frequency, a data decision circuitry, and an initialization and timing control circuitry.

A. Buffer and Input DC Offset Cancellation

The buffer with feedforward dc offset cancellation is modified from [11], as shown in Fig. 2(b). The second-order RC LPF networks (R_A, C_A, R_B, and C_B) sense the input dc offset and subtract it from the output through the transistors M_B and M_C. The buffer has 5.5 dB of in-band gain, and the −3-dB bandwidth is from 500 kHz to 8 MHz, which can fully cover the frequency band of interest over process variations. The measured maximum input dc offset cancellation is 490 mV.

B. LPQ and FWPG

The proposed LPQ and the FWPG are presented in Fig. 2(c), and the signal flow is illustrated in Fig. 3. Two types of crossing

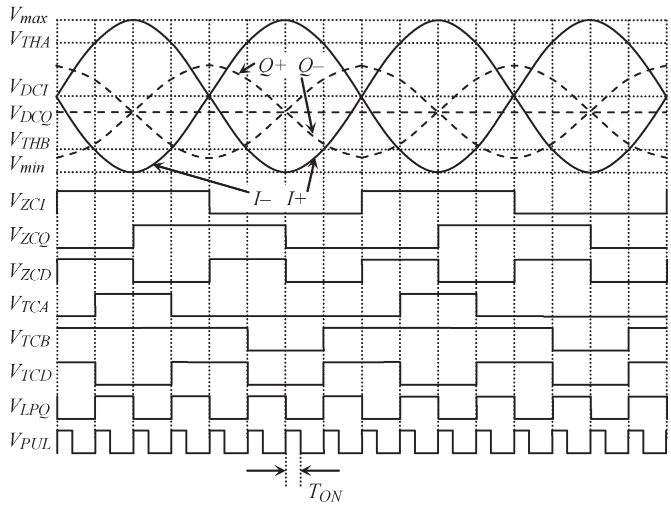

Fig. 3. Operating principle of the proposed multithreshold LPQ and FWPG.

detection, i.e., zero-crossing detection (ZCD) and threshold-crossing detection (TCD), are performed in the LPQ. The differential GFSK signals are first converted into I and Q signals ($I+$, $I-$, $Q+$, and $Q-$) by the RC polyphase filter (PPF), and then, the zero-crossing points of the I and Q signals are captured into $V_{\rm ZCI}$ and $V_{\rm ZCQ}$ by the voltage comparators ($A_{\rm ZCI}$ and $A_{\rm ZCQ}$), respectively. For the I signal, two more thresholds are inserted into the path through the maximum and minimum peak detectors and the transconductors (Gm_A and Gm_B), and then, the detected threshold-crossing points are collected into $V_{\rm TCD}$ by the EXCLUSIVE OR (XOR) gate. To automatically and dynamically set the thresholds of the I path, the peak value ($V_{\max}$) of $I+$ and the valley value ($V_{\min}$) of $I-$ are sensed and stored into capacitors ($C_{\max}$ and $C_{\min}$). The threshold values are then set by the ratios of the transconductors' outputs (I_1 to I_4). In this design, the outputs are defined by $Gm_A = \sqrt{2}Gm_B$, $I_1 = I_2$, and $I_3 = -I_4$. The threshold-crossing points in $V_{\rm TCA}$ and $V_{\rm TCB}$ are determined by the summations of the transconductors' outputs $I_2 + I_4$ and $I_1 + I_3$, respectively. Therefore, the two equivalent thresholds ($V_{\rm THA}$ and $V_{\rm THB}$) are $V_{\rm TH(A,B)} = (V_{\max} + V_{\min})/2 \pm (V_{\max} - V_{\min})/2\sqrt{2}$. As a result, the crossing points corresponding to the thresholds always have $\pi/4$ phase difference to the adjacent zero-crossing points. Due to the quadrature phase between I and Q signals, the zero-crossing points in $V_{\rm ZCD}$ are spaced with $\pi/2$ phase distance, which leads to all the detected crossing points in $V_{\rm LPQ}$ being evenly distributed in the phase domain. Therefore, the LPQ is linear, and the equivalent threshold number of the LPQ is $N = \pi/LSB(\varphi) = 4$. Generally, if K pairs of transconductors are inserted into the TCD path in the same manner as Gm_A and Gm_B with the transconductances of $Gm_{B,i}/Gm_{A,i} = \sin(i\pi/(2K+2))$, $i = 1, 2, \ldots, K$, the LPQ phase quantization size is $LSB(\varphi) = \pi/(2K+2)$. The equivalent threshold number is $2K+2$, and $\hbar_{\rm min,GFSK}$ is reduced to $0.32/(K+1)$, which could be of interest in high-sensitivity frequency discriminators.

Since the thresholds $V_{\rm THA}$ and $V_{\rm THB}$ are dynamically generated according to the strength of the I signal, and the ZCD performed by the comparators ($A_{\rm ZCI}$ and $A_{\rm ZCQ}$) is insensitive to the input signal power, the four-threshold LPQ is able to tolerate large I and Q amplitude mismatch. In this design, the PPF has only one stage, and the -3-dB corner frequency of the PPF is set to 8 MHz instead of 2 MHz (IF), which reduces the area occupied by the passive resistors and capacitors, while retaining a good quadrature phase between the I and Q signals (I/Q phase mismatch less than 1°). The I signals (around 900-mV signal swing) are low passed and retain more than 90% peak-to-peak swing of the buffer output. As shown in Fig. 2(c), setting the PPF's cutoff frequency to 8 MHz makes the IF fall near the flat region of the low-pass transfer function, which reduces the amplitude mismatch of the two sidebands of the GFSK signals in the I path and improves the immunity to process variations. For the Q path (around 170-mV signal swing), only ZCD is performed, and thus, the amplitude mismatch between GFSK sidebands has a minor effect on demodulation performance. The typical input swing of the demodulator is 500 $\rm mV_{pp}$, which is provided by a variable-gain amplifier chain in our low-IF WBAN receiver front end.

To precisely set the thresholds $V_{\rm THA}$ and $V_{\rm THB}$, as shown in Fig. 2(d) and (e), the input stage of the transconductors is degenerated by the polyresistor R_S to achieve high linearity, and the output current mirrors are implemented by the 2×2 series-parallel transistor array to overcome process variations and mismatch [12].

As indicated in Figs. 2(c) and 3, the FWPG produces a positive pulse with the width of $T_{\rm ON} = C_{\rm CHG} \cdot V_{\rm TON}/I_{\rm CHG}$ at each transition edge of $V_{\rm LPQ}$, where $C_{\rm CHG}$, $V_{\rm TON}$, and $I_{\rm CHG}$ are the charging capacitor, control voltage, and charging current, respectively. The control voltage $V_{\rm TON}$ controls the pulse width of $V_{\rm PUL}$ and, thus, the frequency-to-voltage conversion gain of the demodulator. $V_{\rm TON}$ can be provided by the digital baseband through a digital-to-analog converter, which allows the baseband to tweak the demodulator performance. In this prototype, $V_{\rm TON}$ is provided by an external supply, and $T_{\rm ON}$ can be tuned from 5 to 80 ns.

LPQ mismatches such as the PPF RC variations, the ZCD and TCD path delay mismatch, and the offset voltages of the comparators will drive the crossing points away from their ideal phase positions and make the LPQ nonlinear. However, since $V_{\rm PUL}$ is filtered by the LPF, the final bit error rate (BER) is not sensitive to small LPQ nonlinearity. Matlab simulations show that, even with the maximum RC variations of the process, 20-mV offset voltages, and 2-ns ZCD and TCD path delay mismatch, the required SNR for a 0.1% BER is only degraded by 1.3 dB.

C. Data Decision and Frequency Offset Cancellation

The power of $V_{\rm PUL}$ is averaged by the LPF for data decision. Due to the input frequency offset and the variation of the modulation index, the actual dc level of the LPF output $V_{\rm LPF}$ may have a serious drift (up to several hundreds of millivolts). Fig. 4 shows the dynamic threshold slicer with efficient dc offset cancellation for data decision. Here, the maximum and minimum peak detectors sense the peak-to-peak envelope of $V_{\rm LPF}$. The decision threshold is then dynamically generated by averaging the peak and valley values of $V_{\rm LPF}$. The slicer has a wide input common-mode range, i.e., from 0.2 to 1.6 V, which can fully cover the LPF output voltage over process variations,

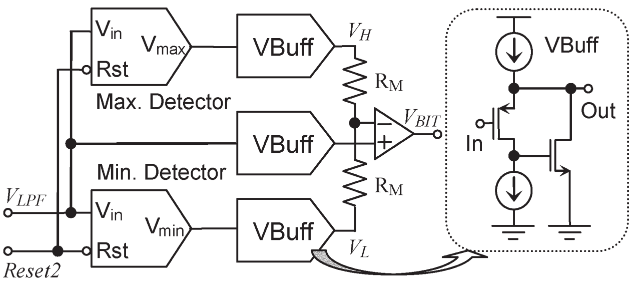

Fig. 4. Dynamic threshold slicer.

and the demodulator achieves an input frequency offset tolerance of 800 kHz, which is sufficient for most applications.

D. Data Rate Coverage

For the GFSK demodulator, one stringent design challenge is to achieve a high data rate with low IF. In this design, the proposed multithreshold LPQ improves the ratio of the data rate to the IF by raising the frequency of V_{PUL} to $2\pi/LSB(\varphi)$ times of the IF. As a result, the requirement on LPF selectivity is relaxed. The LPF is designed as a two-stage fourth-order filter. The first stage is a second-order passive RC LPF, and the second stage is a second-order Butterworth Gm-C low-pass biquad. The overall -3-dB corner frequency of the LPF is set to 1.5 MHz, which gives enough margin to overcome the corner frequency drift caused by process variations. Hence, the frequency tuning circuit for the LPF is not required. In addition to the LPF selectivity, the settling time of the peak detectors in the dynamic threshold slicer may also limit the maximum data rate. In this design, the demodulator achieves a maximum data rate up to 2 Mb/s. The settling time of the peak detectors is less than 0.23 μs, which is sufficiently fast. The decision threshold of the dynamic threshold slicer can be settled just after receiving the first data "1" and data "0." The lowest data rate is determined by the holding time of the dynamic threshold slicer and the continuous bit runs of the baseband bit sequence. In this design, the holding time of the peak detectors is larger than 80 μs, which leads to a minimum data rate down to 100 kb/s with 8-bit continuous bit runs ("11111111" or "00000000").

E. Initialization

For the proposed demodulator, a reset signal is needed to initialize the peak detectors at the beginning of the demodulation. The reset signal can be provided by a received-signal-strength indicator or channel indicator in a low-IF receiver. In this design, a 1-bit power indicator (PI), as shown in Fig. 5, is used to provide the reset signal. The indicator includes a precise full-wave rectifier, an LPF, and a comparator with a preset threshold V_{CS}. Once the output power of the input buffer exceeds the noise level prescribed by V_{CS}, the reset signal rises to supply voltage, and then, the demodulator starts to work. The full-wave rectifier is composed of two half-wave transconductance rectifiers with complementary inputs. The envelope of the full-wave rectifier output is then extracted by the two-stage LPF. An amplitude-shift keying (ASK) signal with 300-mV peak-to-peak swing is used to test the PI sensitivity. Measured results

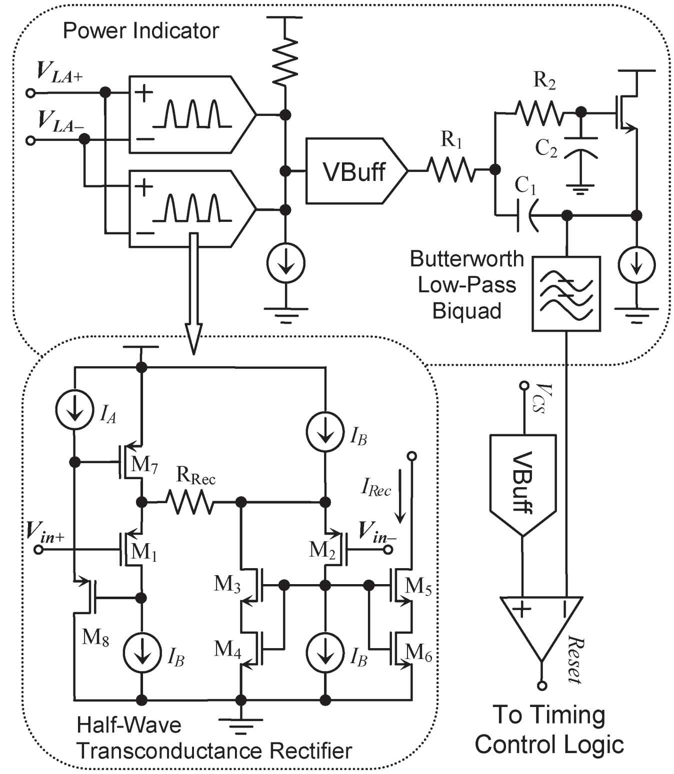

Fig. 5. Reset signal generator.

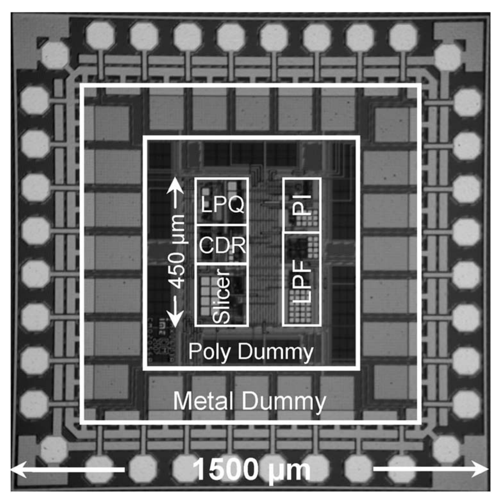

Fig. 6. Micrograph of the demodulator chip.

show that the designed PI can distinguish the ASK signal with a modulation depth as low as 6.7%. The initialization of the demodulator can be finished within four data periods with the 4-bit "1010" training code before the preamble.

IV. Measurement Results

The proposed GFSK demodulator has been implemented in a Chartered 0.18-μm CMOS process. Fig. 6 shows the chip micrograph of the GFSK demodulator. A clock and data recovery (CDR) logic circuit that supports variable data rates has also been implemented into the demodulator chip for testing purposes. The active area of the GFSK demodulator (including the initialization circuit and CDR) is only 0.14 mm^2. Fig. 7

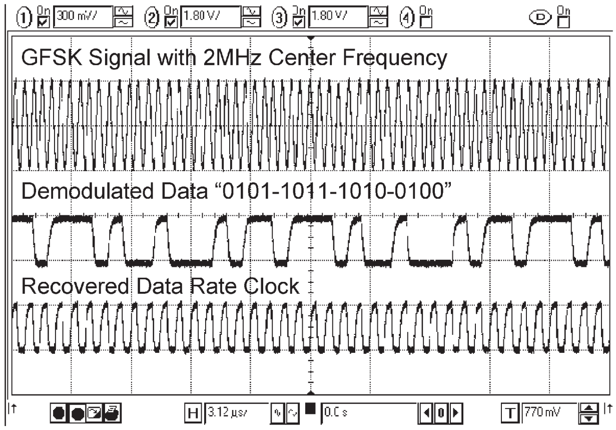

Fig. 7. Measured demodulator performance.

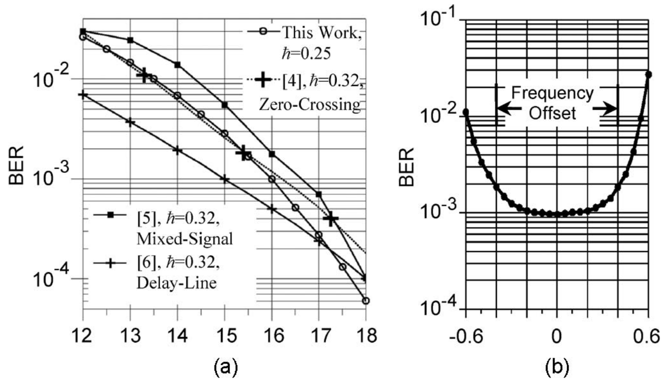

Fig. 8. Measured demodulator performance. (a) BER versus SNR. (b) BER versus input frequency offset (MHz) at 16.0-dB input SNR.

presents the measured demodulator performance in the time domain. The GFSK signal is with 2-MHz center frequency, 160-kHz frequency deviation, and 1.28-Mb/s data rate. The measured BER performance of this work and that of other demodulators are shown in Fig. 8(a). The required SNR for 0.1% BER is 16.0 dB with only 0.81-mW power consumption from a 1.8-V power supply. Fig. 8(b) shows the measured BER performance versus the input frequency offset at 16.0-dB input SNR. The demodulator can tolerate the input frequency offset from −400 to +400 kHz. In this design, the BER degradation is caused by different mechanisms for different frequency offset directions. For a positive frequency offset, the period of $V_{\rm PUL}$ is reduced. With the same $T_{\rm ON}$, the margin for tolerating the LPQ nonlinearity is also reduced; thus, the BER is degraded. For a negative frequency offset, the Q path becomes volatile to large additive white Gaussian noise as the Q path gain of the PPF decreases. Furthermore, a negative frequency offset reduces the frequency of $V_{\rm PUL}$, as the LPF is designed with low selectivity, the SNR at the LPF output decreases, and thus, the BER is degraded.

The measured performance of the proposed demodulator is summarized and compared with other state-of-the-art GFSK demodulators in Table I. Although the proposed multithreshold LPQ is more complex than the conventional zero-crossing detector [4], it is well compensated by the compact LPF and slicer designs. Thanks to the mixed-signal structure adopted, the demodulator does not require strict specifications on comparators, amplifiers, and filters. Overall, the proposed demodulator achieves robust performance over large process variations with a smaller modulation index and lower power consumption.

TABLE I
DEMODULATOR PERFORMANCE SUMMARY AND COMPARISON

Parameters	**This Design**	**[4]**	**[5]**	**[6]**	**Unit**
Technology	0.18	0.35	0.25	0.18	μm
Supply Voltage	1.8	3	2	1.8	V
Power Consumption	0.81	9	6	3.6	mW
Chip Area	0.14	0.7	0.3	0.26	mm^2
Modulation Index ℏ	0.25	0.32	0.28 to 0.35	0.32	-
Data Rate	0.1 to 2.0, 1.28 (Typical)	1	1	1	Mb/s
IF Frequency	2	2	2	5	MHz
Max. Input DC Offset	490	-	-	-	mV
SNR (for 0.1% BER)	16.0	16.2	16.5	14.9	dB

V. CONCLUSION

An ultralow-power CMOS GFSK demodulator integrated circuit has been presented in this brief. Through the proposed multithreshold LPQ and dynamic threshold slicer, the demodulator has improved the data rate coverage, the range of detectable modulation index, and the frequency offset tolerance with reduced power consumption. Covering data rates from 100 kb/s to 2 Mb/s and modulation indexes as low as 0.25, the proposed demodulator is suitable for most Bluetooth, WPAN, WBAN, and other short-range wireless applications.

REFERENCES

[1] B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, “A low-power fully monolithic subthreshold CMOS receiver with integrated LO generation for 2.4 GHz wireless PAN applications,” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.

[2] H. Komurasaki, T. Sano, T. Heima, K. Yamamoto, H. Wakada, I. Yasui, M. Ono, T. Miwa, H. Sato, T. Miki, and N. Kato, “A 1.8-V operation RF CMOS transceiver for 2.4-GHz-band GFSK applications,” *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 817–825, May 2003.

[3] B. W. Cook, A. D. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, “An ultra-low power 2.4 GHz RF transceiver for wireless sensor networks in 0.13μm CMOS with 400 mV supply and an integrated passive RX front-end,” in *Proc. Dig. Tech. IEEE ISSCC*, Feb. 2006, pp. 370–371.

[4] B. Xia, C. Y. Xin, W. J. Sheng, A. Y. Valero-Lopez, and E. Sanchez-Sinencio, “A GFSK demodulator for low-IF Bluetooth receiver,” *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1397–1400, Aug. 2003.

[5] T.-C. Lee and C.-C. Chen, “A mixed-signal GFSK demodulator for Bluetooth,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 3, pp. 197–201, Mar. 2006.

[6] H.-S. Kao, M.-J. Yang, and T.-C. Lee, “A delay-line-based GFSK demodulator for low-IF receivers,” in *Proc. Dig. Tech. IEEE ISSCC*, Feb. 2007, pp. 88–89.

[7] H. Darabi, S. Khorram, B. Ibrahim, M. Rofougaran, and A. Rofougaran, “An IF FSK demodulator for Bluetooth in 0.35μm CMOS,” in *Proc. IEEE CICC*, May 2001, pp. 523–526.

[8] F. Xiong, *Digital Modulation Techniques*. Boston, MA: Artech House, 2000, pp. 259–271.

[9] S. Han, B. Chi, and Z. Wang, “A mixed-loop CMOS analog GFSK modulator with tunable modulation index,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 6, pp. 547–551, Jun. 2007.

[10] H. Darabi, B. Ibrahim, and A. Rofougaran, “An analog GFSK modulator in 0.35-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2292–2296, Dec. 2004.

[11] P. C. Huang, Y. H. Chen, and C. K. Wang, “A 2-V CMOS 455-kHz FM/FSK demodulator using feedforward offset cancellation limiting amplifier,” *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 135–138, Jan. 2001.

[12] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, “Nanowatt, sub-ns OTAs, with sub-10-mV input offset, using series-parallel current mirrors,” *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sep. 2006.